INTERLAN

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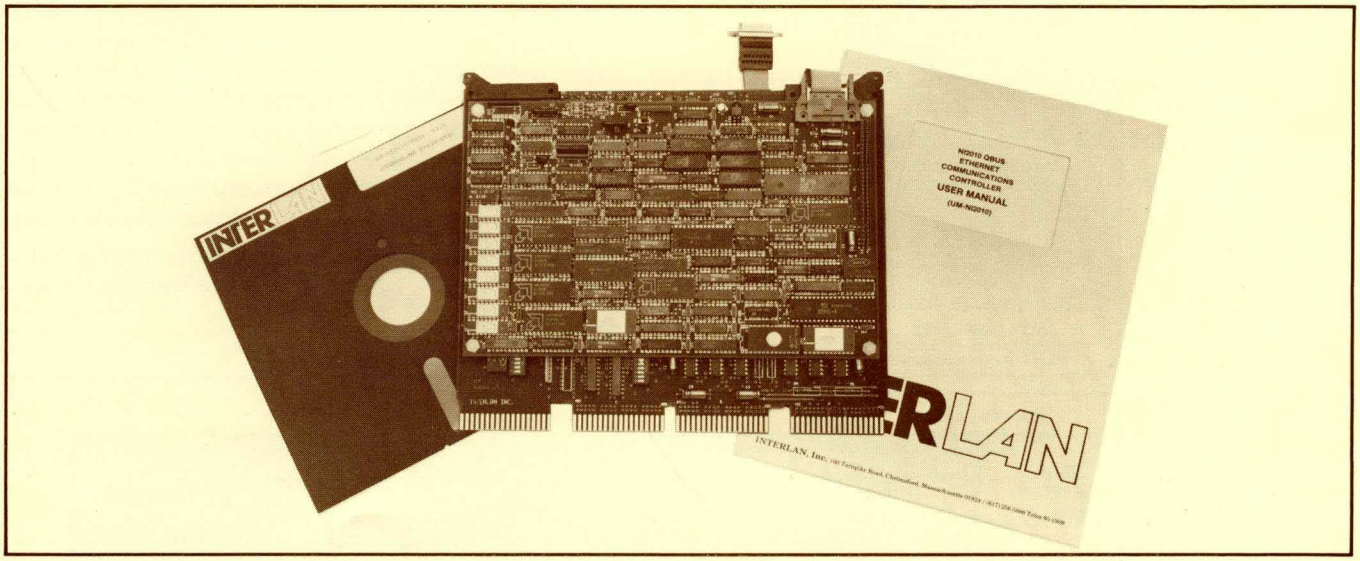
NI2010A Qbus Ethernet™ Communications Controller

FEATURES:

- **Implements Ethernet Version 1.0 Specifications**
- **Performs Ethernet Data Link Layer Functions:**
  - — Data Encapsulation/Decapsulation
  - — Address Recognition
  - — CRC Generation/Checking
  - — CSMA/CD Transmit and Receive Data Link Management
- **Performs Ethernet Physical Channel Functions:**
  - — 10 MBits Per Second Data Rate
  - — Data Encoding and Decoding
  - — Channel Access
  - — Transceiver Cable Interface
- **Collects Network Statistics:**
  - — Tallies Number of Transmissions, Receptions, Errors, and Collisions
- **Supports High Station Performance:**
  - — 13.5 KByte FIFO Buffer For Back-To-Back Frame Reception
  - — 1.5 KByte FIFO Buffer For Frame Transmission
  - — DMA Transfers To/From Qbus Memory
- **Extensive Diagnostic Features:**
  - — Internal and External Loop-Back Operation
  - — Network LED Indicators
  - — Power-Up Confidence Test
  - — Pass/Fail LED Indicator
  - — Diagnostic Software Provided
- **Onboard Boot ROM Sockets**
- **Quad-Height Board-Set**
  - — Occupies Two Quad Slots
  - — Supports 16-, 18-, and 22-Bit Address Ranges
- **Network Software Support Available**

DESCRIPTION

The NI2010A Qbus Ethernet Communications Controller Board is a quad-height board-set that contains all the data communications controller logic required for interfacing DEC's™ family of LSI-11™ and Qbus-based PDP-11™ systems to the Ethernet local area network. Incorporating the Interlan NM10A Ethernet Protocol Module, the board-set complies in full with the Xerox/Intel/DEC Ethernet Specification. It performs the specified data link and physical channel functions, permitting Qbus-based systems to engage in high speed transmission and reception of data with other Ethernet stations on the local area network.



TM Ethernet is a trademark of Xerox Corporation. LSI-11, PDP-11, and DEC are trademarks of Digital Equipment Corporation

IMPLEMENTS ETHERNET SPECIFICATIONS

The NI2010A fully complies with the Xerox/Intel/DEC Ethernet Specification. The board-set performs the specified Data Link and Physical Channel functions permitting 10Mbit per second data communications between stations separated by up to 2500 meters. As shown in Figure 1, the NI2010A, when attached to a transceiver unit, provides a LSI-11 or Qbus-based PDP-11 a complete connection onto the Ethernet local area network.

PERFORMS ETHERNET DATA LINK LAYER FUNCTIONS

Within the Data Link Layer the NI2010A performs the specified Ethernet transmitter processes of Transmit Data Encapsulation and Transmit Link Management, and the Ethernet receiver processes of Receive Data Decapsulation and Receive Link Management.

Transmit Data Encapsulation

Figure 2 shows the Ethernet Frame Format for packet transmissions over the coaxial cable physical channel. For receive synchronization purposes, the frame is preceeded with a 64-bit preamble sequence and terminated with a minimum interframe spacing period of 9.6 microsecond

The Destination Address field specifies the station(s) for which the frame is intended. The address value provided by the user may be either: 1) the physical address of a particular station on the network; 2) a multicast-group address associated with one or more stations; or 3) the broadcast address for simultaneous transmission to all stations on the network. The first bit of the Destination Address distinguishes a physical address from a multicast address (0 = physical, 1 = multicast). For broadcast transmissions an all one-bit pattern is used.

The Source Address field specifies the physical address of the transmitting station. To eliminate the possibility of an addressing ambiguity on a network, associated with each NI2010A is a unique 48-bit physical address value assigned to it at the time of manufacture. A user command permits a different physical address to be assigned to the controller. On transmission, the NI2010A inserts this value into the Source Address field.

The Type field is specified by the user for use by high level network protocols. It specifies to the receiving station(s) how the content of the Data field is to be interpreted.

The Data field may contain a variable number of data bytes ranging from a minimum of 46 bytes to a maximum of 1500 bytes. The NI2010A accepts less than 46 bytes from the user by automatically inserting null characters to complete a 46-byte minimum frame size.

The Frame Check Sequence (FCS) field contains a 32-bit cyclic redundancy check (CRC) value generated by the NI2010A during transmission.

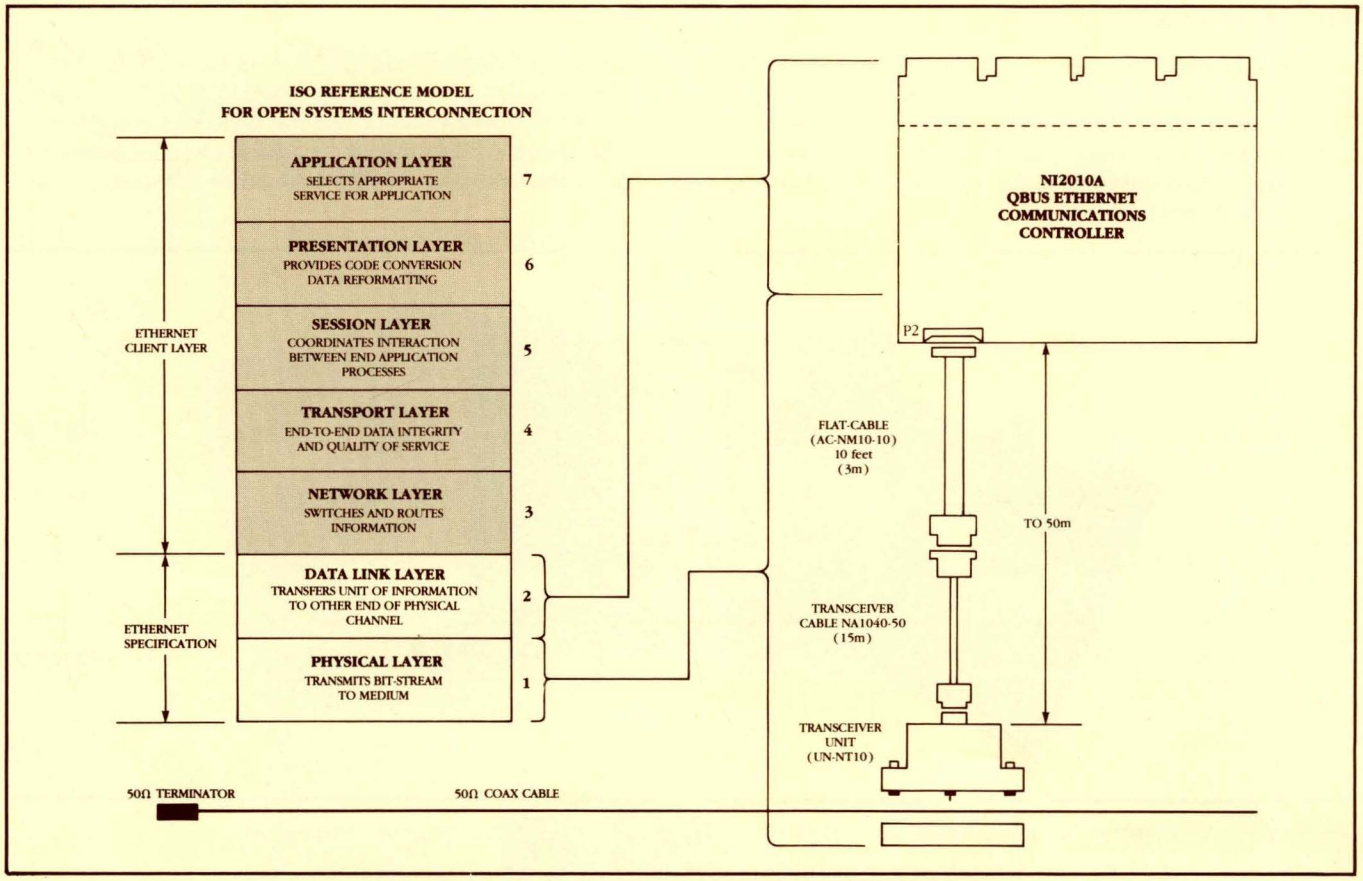


Figure 1. Ethernet Architecture and Implementation

Transmit Link Management

The NI2010A performs all Ethernet Transmit Link Management functions required to successfully deliver a frame onto the network. These functions include:

- Carrier Deference; the NI2010A monitors the physical channel and defers its transmission should the channel be busy carrying other traffic;
- Collision Detection; once the NI2010A has finished deferring to the passing traffic on the network, it proceeds with its own transmission. In the event that another station simultaneously began a transmission, a "collision" occurs. The NI2010A detects this event and terminates its transmission attempt; and
- Collision Backoff and Retransmission; when a transmission attempt has been terminated due to a collision the NI2010A attempts its transmission again after delaying a short random period of time. The scheduling of the retransmission is determined by the Ethernet process called "truncated binary exponential backoff". The NI2010A reports an error should it be unable to deliver its frame onto the network after 16 transmission attempts.

Receive Data Decapsulation

When not transmitting a frame the NI2010A continuously listens to the traffic being carried on the network. After synchronizing to the preamble sequence of a frame on the network, the NI2010A processes the Destination Address field through its address filter logic to determine whether or not the incoming frame is intended for it. The NI2010A controller will only accept a frame from the network with a Destination Address value that either:

1) matches the physical address of the NI2010A board itself;
2) contains the broadcast address; or
3) matches one of the 63 multicast-group logical addresses which the user may assign to the board.

The NI2010A performs high speed multicast-group address recognition. Whenever a multicast-group logical address received on the network, the NI2010A converts the frames 48-bit Destination Address field into a 6-bit table entry pointer through the application of a many-to-few mapping called "hashing." It uses the resulting pointer to look into a table of valid multicast-group addresses to see if the received address is one that the station should accept.

For network management and diagnosis, the NI2010A may be operated in a "promiscuous" receive mode. When in this mode, the NI2010A disables its address filter logic and accepts all undamaged frames passing on the network.

The NI2010A validates the integrity of a received frame by regenerating the 32-bit CRC value on the received bit stream and comparing it against the CRC value found in the frame's Frame Check Sequence field.

Receive Link Management

Since collisions are a normal occurrence in the Ethernet's CSMA/CD link management process, the NI2010A receiver filters out collision fragments from valid frames.

PERFORMS ETHERNET PHYSICAL LAYER FUNCTIONS

Within the Ethernet Physical Layer the NI2010A performs the electrical and procedural specifications required for interfacing to a transceiver unit. Transmissions and receptions take place at a 10Mbits per second data rate under half-duplex operation.

During transmission the NI2010A's physical channel functions include:

- Generating the 64-bit preamble sequence for all receivers on the network to synchronize on;
- Parallel to serial conversion of the frame;
- Calculating a 32-bit CRC value and inserting it into the Frame Check Sequence field;
- Generating a self-synchronizing serial bit stream through Manchester encoding of the data; and
- Providing proper channel access by detecting carrier from another station's frame transmission and sensing the collision presence signal from the transceiver unit.

The NI2010A's physical channel functions during reception include:

- Manchester decoding the incoming bit stream into a data stream and a clock stream;
- Synchronizing to, and removal of, the preamble sequence; and
- Serial to Parallel conversion of the frame.

SUPPORTS HIGH STATION PERFORMANCE

The NI2010A has been designed to offer high network performance while minimizing the service loads placed upon the host Qbus system.

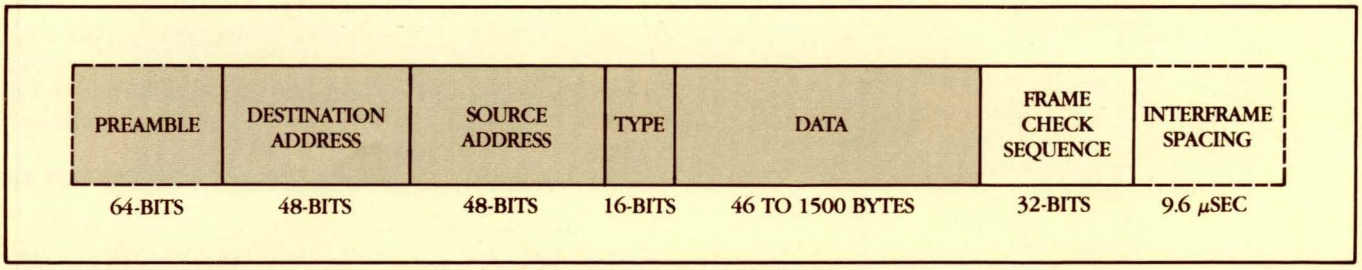


Figure 2. Ethernet Frame Format

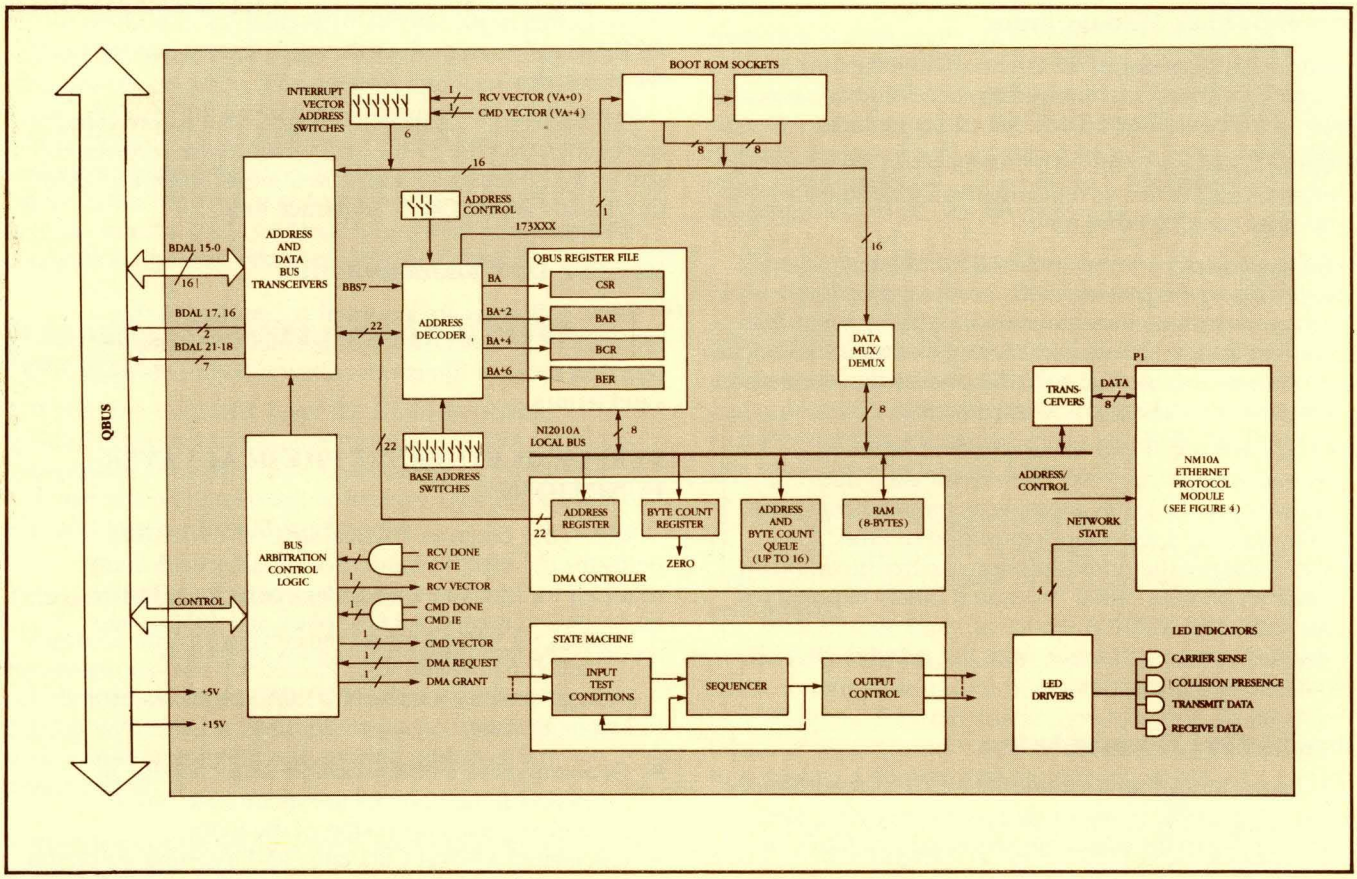


Figure 3. NI2010A Functional Diagram

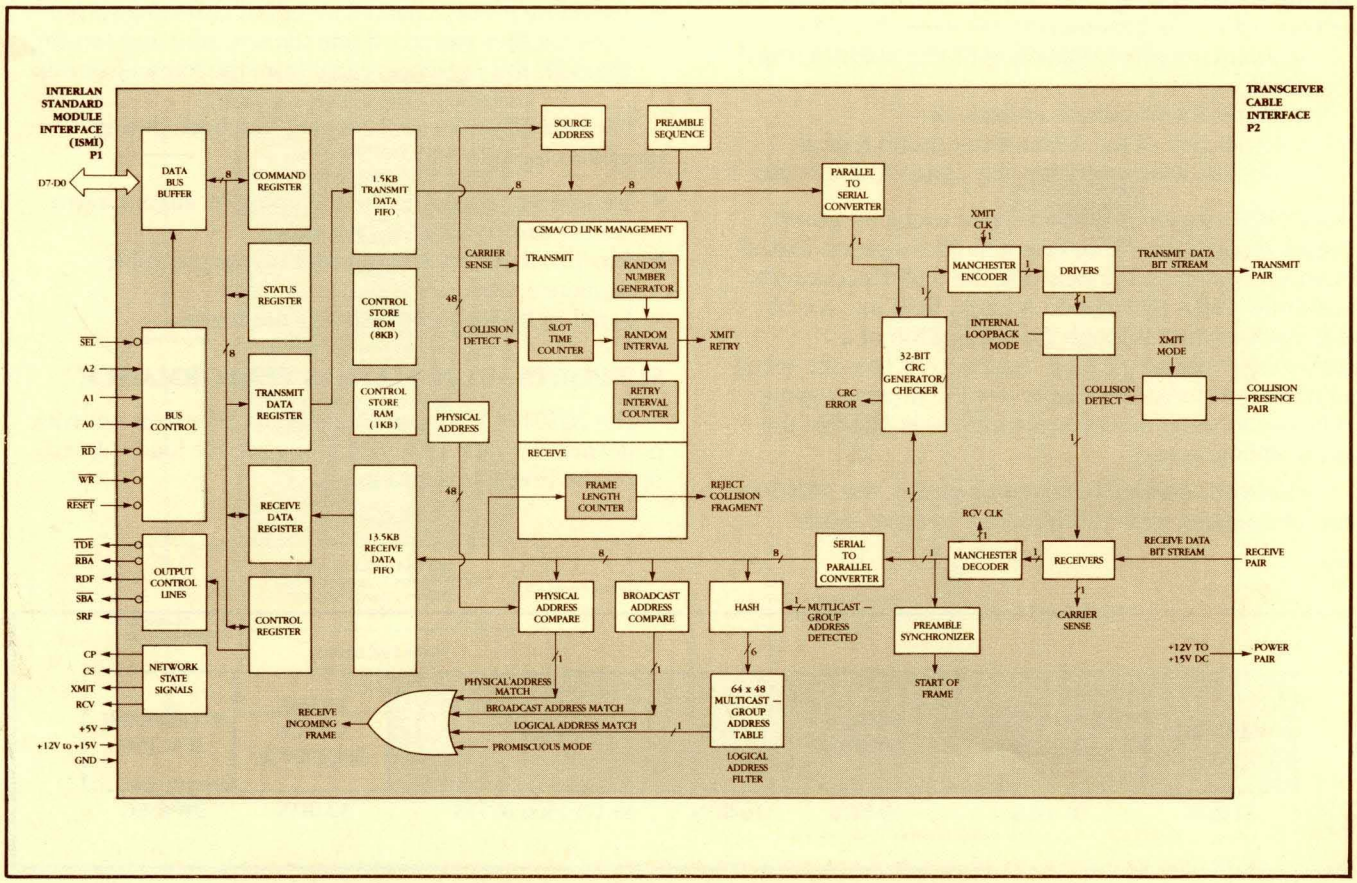


Figure 4. Functional Diagram of the NI2010A's Ethernet Logic (NM10A)

Serving to buffer the system from the unpredictable interarrival times characteristic of network traffic, the board has a FIFO (first-in, first-out) memory which can store up to 13.5 Kbytes of received frames. Because of this extensive front-end buffering, few time-critical service requirements are imposed on the host Qbus system.

For transmission, the NI2010A has a 1.5 Kbyte (1536 bytes) Transmit FIFO which permits the host to perform a one-time transfer of a frame. All retransmissions are performed out of this onboard buffer.

All data block transfers between the NI2010A and Qbus memory are performed under the control of an onboard DMA controller. To maximize system performance during reception, the controller allows the user to preload up to sixteen different memory buffer address and byte count values for DMA of received frames. The DMA controller supports Qbus systems with either a 16-, 18-, or 22-bit address range.

EXTENSIVE DIAGNOSTIC FEATURES

The NI2010A offers comprehensive network and board-level diagnostic tools which greatly simplify the process of identifying a network communication problem. Mounted on the edge of the board are four network state LED indicators which provide a visual indication of whether or not the user's station is communicating onto the network. For a comprehensive station diagnosis, the user can exercise the NI2010A's communication facilities in either internal and external loopback mode; making it possible to detect and isolate a fault to the coaxial cable, transceiver unit, transceiver cable; or the NI2010A board itself.

On power-up the NI2010A performs a confidence test of the onboard memories, register and data paths. A LED indicator shows the pass/fail operational state of the board. To assist in problem identification, Interlan supplies standalone diagnostic software for troubleshooting the NI2010A on an LSI-11 or PDP-11.

COLLECTS NETWORK STATISTICS

The NI2010A collects network statistics to permit the user to characterize network operation. Statistics tallied include:

— number of frames received
— number of frames received with CRC error
— number of frames received with alignment error
— number of frames transmitted
— number of transmit collisions

ONBOARD BOOT ROM SOCKETS

Two boot ROM sockets on the NI2010A permit downline loading to the station over the Ethernet or booting from a local device. The sockets accommodate 512 x 8 ROMs, and support two switch-selectable 256 word boot programs.

NETWORK SOFTWARE SUPPORT AVAILABLE

A wide range of networking and operating system software support is available for the NI2010A. Consult the latest Interlan Product List for details.

Table 1. NI2010A Command and Status Codes

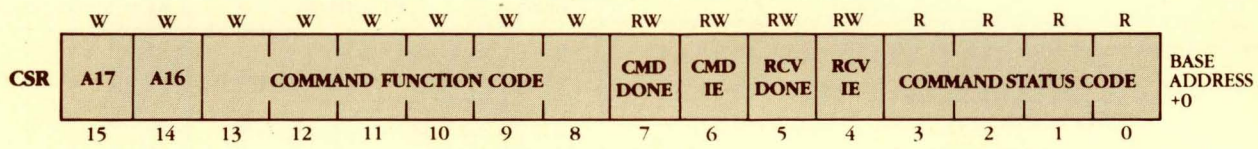
COMMAND FUNCTION CODES

CODE (Octal)	COMMAND FUNCTION	STATUS CODE RETURNED (Octal)
00	Reserved	02
01	Set Module Interface Loopback Mode	00
02	Set Internal Loopback Mode	00
03	Clear Loopback Mode	00
04	Set Promiscuous Receive Mode	00
05	Clear Promiscuous Receive Mode	00
06	Set Receive-On-Error Mode	00
07	Clear Receive-On-Error Mode	00
10	Go Offline	00
11	Go Online	00
12	Run On-board Diagnostics	Diag. Status Code
13-14	Reserved	00
15	Set Insert Source Address Mode	00
16	Clear Insert Source Address Mode	00
17	Set Physical Address to Default	00
20	Set Receive All Multicast Packets	00
21	Clear Receive All Multicast Packets	00
22	Perform Network Loopback Test	00, 01, 03, 04, 05, 14, 15, 16
23	Perform Collision Detect Test	00, 03, 04, 05, 08
24-27	Reserved	02
30	Report and Reset Statistics	00, 17
31	Report Collision Delay Times	00, 17
32	Reserved (Maintenance)	00, 17
33-37	Reserved	02
40	Supply Receive Buffer	00, 17
41-47	Reserved	Undefined
50	Load Transmit Data	00, 05, 17
51	Load Transmit Data and Send	00, 01, 03, 04, 05, 06, 10, 17
52	Load Group Address(es)	00, 05, 12, 17
53	Delete Group Address(es)	00, 05, 12, 17
54	Load Physical Address	00, 12, 17
55-57	Reserved	02
60	Flush Receive BAR/BCR Queue	00
61-67	Reserved	Undefined
70-76	Reserved	Undefined
77	Reset	Diag. Status Code

COMMAND STATUS CODES

CODE (Octal)	COMMAND STATUS
00	Success
01	Success with Retries
02	Illegal Command
03	Inappropriate Command
04	Failure
05	Buffer Size Exceeded
06	Frame Too Small
07	Reserved
10	Excessive Collisions
11	Reserved
12	Buffer Alignment Error
13	No Heartbeat Detected
14	No CRC Error Occured
15	Inappropirate CRC Error
16	Last Data Byte Not Received Correctly
17	Non-existent Memory

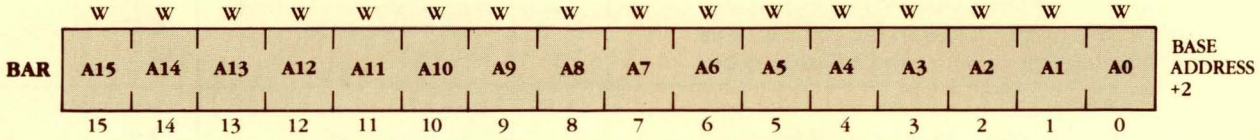
COMMAND AND STATUS REGISTER



CSR BIT DEFINITIONS

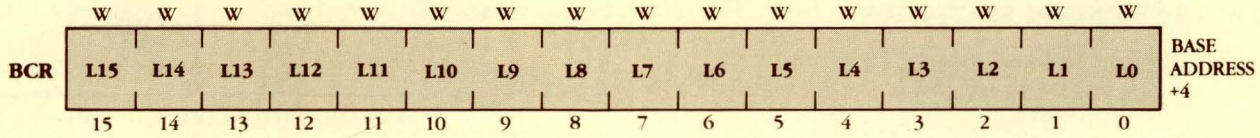
Bit	Name	Function
15-14	A17, A16	Address extension bits for forming an 18-bit Bus Address Register (BAR) value for the 16-and 18-bit address ranges. Should be written by user concurrent with writing of a Command Function Code (Read value undefined)
13-8	COMMAND FUNCTION CODE	Command Codes of Table 1 are written by the user here. (Read value undefined)
7	CMD DONE	Set by NI2010A when command function has been completed. Reading the CSR register resets this bit.
6	CMD IE	User writes 1 to enable interrupt on CMD DONE. Writing 0 disables CMD DONE interrupt
5	RCV DONE	Set by NI2010A after a Qbus memory buffer has been loaded by the NI2010A DMA controller. Reading the CSR register resets this bit.
4	RCV IE	User writes 0 to enable interrupt on RCV DONE. Writing 0 disables RCV DONE interrupt.
3-0	COMMAND STATUS CODE	Status codes of Table 1 are returned here when CMD DONE is set. (No response on write.)

BUS ADDRESS REGISTER



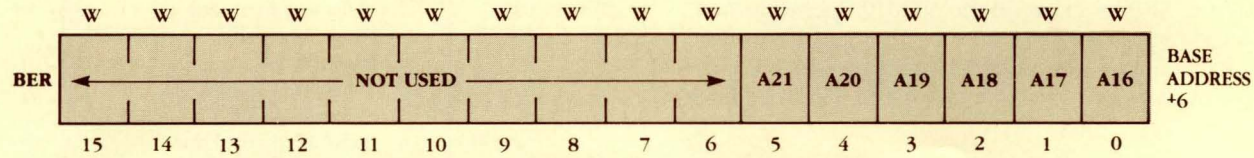
The user writes into this register the low 16-bits of the address of the Qbus memory buffer to be used by the NI2010A DMA Controller. (Reading BAR returns all zeros)

BYTE COUNT REGISTER



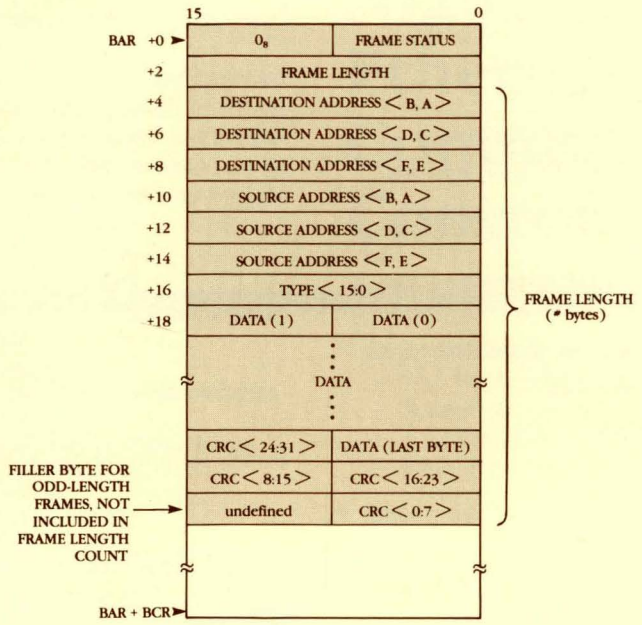
The user writes into this register the binary value for the byte length of the Qbus memory buffer to be used by the NI2010A DMA Controller. (Reading BCR returns all zeros)

BUS ADDRESS EXTENSION REGISTER



The user switch-enables this register (S1-10) when 22-bit addressing mode is required. Address extension bits for forming a 22-bit Bus Address Register (BAR) value are written to this register. A17 and A16 of the CSR register are ignored. (Reading BER returns all zeros)

Figure 5. NI2010A I/O Page Registers



NOTE: If the received frame is larger than the allocated buffer size. (BCR) the NI2010A DMA Controller uses the next preloaded buffer and continues. This feature requires that the value of BCR be an integral multiple of 8 bytes.

RCV DONE is set when either the last word of the frame has been transferred or the last word in the buffer has been loaded.

Figure 6. Receive Data Organization in Qbus Memory

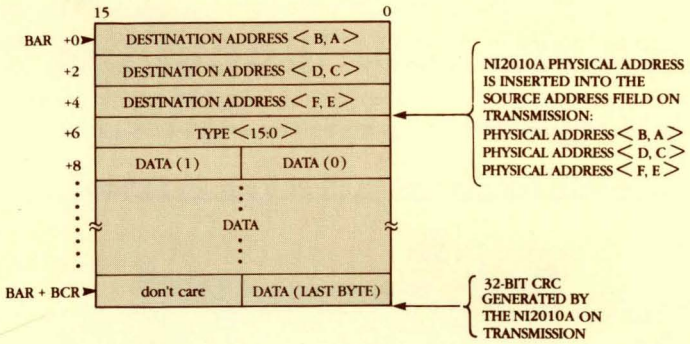
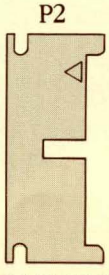


Figure 7. Transmit Data Organization in Qbus Memory



BERG 65496-043 OR EQUIV.

Pin		Pin	
1	N/C	2	Collision Presence —
3	Collision Presence +	4	Transmit—
5	Transmit +	6	N/C
7	N/C	8	Receive —
9	Receive +	10	Transceiver Power
11	Transceiver Power Return	12	N/C
13	N/C	14	N/C
15	N/C	16	N/C

Figure 8. NI2010A Transceiver Cable Connector

SPECIFICATIONS

Network Specifications Supported:

- 10 million bits per second data rate
- Coaxial cable segments up to 500 meters
- Up to 100 transceivers per cable segment
- Up to 2 repeaters in path between any two stations
- Up to 1500 meters of coax cable between any two stations
- Up to 50 meters of transceiver cabling between station and transceiver
- Up to 2500 meter maximum station separation
- Up to 1000 meter point-to-point link
- Up to 1024 stations per network

Transceiver Interface:

All signals Ethernet Specification compatible
Mating connector: 16-pin Berg #65846-01, 3M #3452, or equiv.

Qbus Specifications:

Base address: switch selectable in the I/O page from 160000_8 to 177760_8
Interrupt Vector Address: switch selectable from 000_8 to 770_8
Interrupt Priority Level: BIRQ4, selectable
Qbus Data Transfers: DMA, 4 word burst
Qbus Loading: 1 dc, 1 ac load
Mounting: Occupies two quad slots. Top board (NM10A) does not connect to Qbus. A grant continuity board is supplied for BDMG and BIAK grant continuity.
Boot ROM Sockets: responds to I/O page address 173000_8 to 173777_8. May be switch disabled. Accommodate 20-pin 512 x 8 ROMs such as MMI 6349, AMD 27S29, or equivalent
Power Requirements: +5Vdc +- 5% @ 6.0 A typ.
+12Vdc +- 5% @ 6.7 A max.
(for transceiver only)

Environmental Specifications:

Operating Temperature: 0° C to 55° C
Relative Humidity: to 90%, non-condensing

ORDERING INFORMATION

Model Number	Description
BD-NI2010A	NI2010A Qbus Ethernet Communications Controller (Board)
DS-NI2010A-RX01	NI2010A Standalone Diagnostic on RX01 floppy disk
DS-NI2010A-RX02	NI2010A Standalone Diagnostic on RX02 floppy disk
UM-NI2010A	NI2010A User Manual
AC-NM10-10	Flat Cable with connectors; 10 feet long (3 meters)
NS2010	RSX-11 M/S Device Driver
NS2020	RT-11 Device Driver
NS2040	UNIX V7 PDP-11 Device Driver
UN-NT10	Ethernet Transceiver Unit
NA1040	Ethernet Transceiver Cable with connectors; available in lengths of 10, 50 and 150 feet
NA1020	Ethernet 50Ω Coaxial Cable; available in lengths of 77, 230 and 385 feet

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