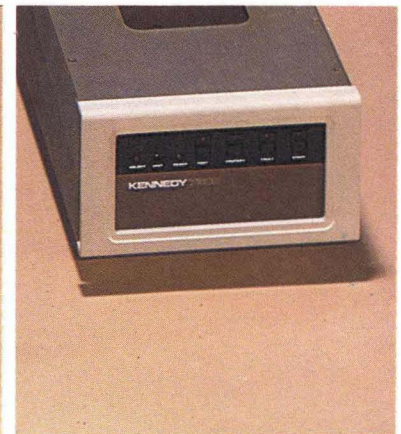
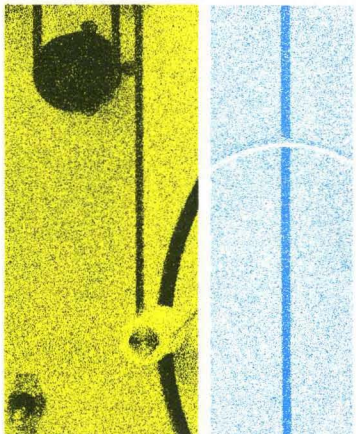
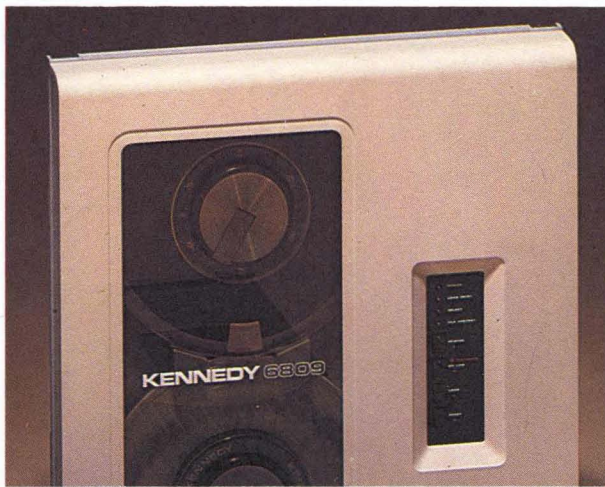
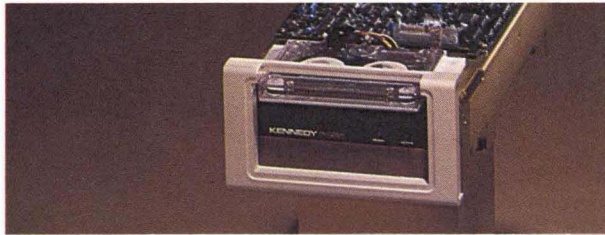


# Series 6170

## 8" Winchester Disk Drive



KENNEDY COMPANY  
An Allegheny International Company

SERIES 6170  
PRODUCT SPECIFICATION  
P/N 102-0036-001

December 16, 1982

Information contained in this document  
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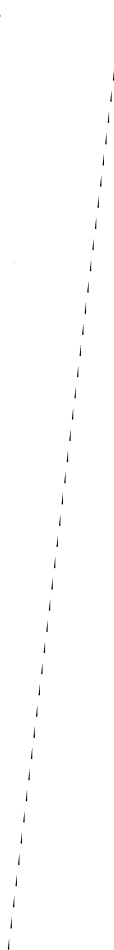






Table of Contents

1	SCOPE.....	1
2	RELATED DOCUMENTATION.....	1
3	GENERAL DESCRIPTION.....	1
3.1	EQUIPMENT DEFINITION.....	1
4	INTERFACE OPTIONS.....	1
5	UNIT DEFINITION.....	2
6	MODELS, OPTIONS, SPARES AND ACCESSORIES.....	5
6.1	MODELS.....	5
6.2	ACCESSORIES.....	6
6.2.1	SIGNAL CABLES.....	6
6.2.2	POWER CABLE.....	6
6.2.3	TERMINATORS.....	6
6.2.4	SHOCK MOUNTS.....	7
7	SPECIFICATIONS.....	7
7.1	RECORDING.....	7
7.1.1	RECORDING METHODS.....	7
7.1.2	RECORDING CHARACTERISTICS.....	7
7.1.3	STORAGE MEDIA.....	8
7.1.4	READ-WRITE HEADS.....	8
7.1.5	DATA CAPACITY.....	8
7.2	ACCESS.....	9
7.2.1	POSITIONING TIME.....	9
7.2.2	ROTATIONAL LATENCY TIME.....	10
7.2.3	OTHER TIMING CONSIDERATIONS.....	10
7.3	RELIABILITY.....	10
7.3.1	SERVICE DATA.....	10
7.3.2	DATA ERROR RATES.....	11
7.3.3	SEEK ERRORS.....	12
7.3.4	ERROR RECOVERY.....	13
7.4	PHYSICAL.....	13
7.4.1	DIMENSIONS.....	13
7.4.2	WEIGHT.....	13
7.4.3	SOUND EMISSION.....	14
7.4.4	PHYSICAL INTERFACE.....	14
7.4.5	POWER REQUIREMENTS.....	14
7.4.6	POWER CONSUMPTION.....	15
7.4.7	SAFETY.....	15
7.5	ENVIRONMENT.....	16
7.5.1	TEMPERATURE.....	16
7.5.2	RELATIVE HUMIDITY.....	16
7.5.3	ATMOSPHERIC PRESSURE.....	16

7.5.4	VIBRATION.....	16
7.5.5	SHOCK.....	17
7.5.6	ELECTROMAGNETIC RADIATION.....	17
8	DATA STORAGE CHARACTERISTICS.....	17
8.1	POWER-UP SEQUENCE.....	19
8.2	DRIVE UNIT SELECTION.....	19
8.3	CYLINDER AND HEAD SELECTION; HEAD TRACKING.....	19
8.4	FORMAT SELECTION.....	20
8.5	DATA PROTECTION AND FAULT SENSING.....	20
8.6	SEEK.....	21
8.7	WRITE.....	21
8.8	READ.....	21
9	SMD DISK DRIVE INTERFACE.....	23
9.1	PHYSICAL AND ELECTRICAL INTERFACE DEFINITION.....	23
9.1.1	BLOCK DIAGRAM.....	23
9.1.2	CABLES.....	25
9.1.3	RECEIVERS/DRIVERS.....	31
9.1.4	TERMINATORS.....	31
9.1.5	SIGNAL LEVELS.....	31
9.1.6	SWITCH-SELECTABLE OPTIONS.....	33
9.1.7	SMD EXCEPTIONS.....	38
9.2	SIGNAL LINE FUNCTIONS AND LOGIC.....	40
9.2.1	UNIT SELECT TAG.....	40
9.2.2	UNIT SELECT BUS LINES.....	40
9.2.3	TAG LINES (TAG 1, 2 AND 3).....	41
9.2.4	BUS LINES (0-9).....	41
9.2.5	OPEN CABLE DETECTOR.....	44
9.2.6	INDEX.....	44
9.2.7	SECTOR.....	44
9.2.8	FAULT.....	44
9.2.9	SEEK ERROR.....	45
9.2.10	ON CYLINDER.....	45
9.2.11	UNIT READY.....	45
9.2.12	WRITE PROTECTED.....	46
9.2.13	WRITE DATA.....	46
9.2.14	WRITE CLOCK.....	46
9.2.15	SERVO CLOCK.....	46
9.2.16	READ DATA.....	47
9.2.17	READ CLOCK.....	47
9.2.18	SEEK END.....	47
9.2.19	UNIT SELECTED.....	47
9.2.20	INDEX.....	47
9.2.21	SECTOR.....	49
9.2.22	GROUND.....	49
9.3	SIGNAL LINE TIMING.....	49
9.3.1	UNIT SELECT.....	49
9.3.2	SEEK.....	49
9.3.3	WRITE.....	52
9.3.4	READ.....	55

9.3.5	WRITE CLOCK GENERATION.....	58
9.3.6	READ CLOCK GENERATION.....	58
9.3.7	INDEX-TO-SECTOR-PULSE TIMING.....	58
9.3.8	OFFSET TIMING.....	58
9.3.9	FAULT RESET.....	60
9.3.10	RETURN-TO-ZERO.....	60
9.3.11	ZERO TRACK SEEK.....	60
9.4	SECTOR FORMATS.....	60
9.4.1	28-BYTE OVERHEAD FORMAT.....	62
9.4.2	44-BYTE OVERHEAD FORMAT.....	65
9.5	POWER LINES.....	67
10	"DISK BUS" DISK DRIVE INTERFACE.....	68
10.1	PHYSICAL AND ELECTRICAL INTERFACE DEFINITION.....	68
10.1.1	BLOCK DIAGRAM.....	68
10.1.2	CABLES.....	73
10.1.3	RECEIVERS/DRIVERS.....	73
10.1.4	TERMINATORS.....	76
10.1.5	SIGNAL LEVELS.....	76
10.1.6	JUMPER-SELECTABLE OPTIONS.....	78
10.2	SIGNAL LINE FUNCTIONS AND LOGIC.....	83
10.2.1	CONTROL BUS.....	83
10.2.2	DIRECTION.....	83
10.2.3	CONTROL WORD 0 (CWD 0) AND CONTROL WORD (CWD 1).....	86
10.2.4	ATTENTION (ATTN) OR BUS REQUEST.....	86
10.2.5	CYCLE ACKNOWLEDGE (CYACK) OR BUS ACKNOWLEDGE.....	86
10.2.6	ATTENTION ACKNOWLEDGE (ATTACK).....	89
10.2.7	SEEK END.....	89
10.2.8	DRIVE FAULT.....	89
10.2.9	UNIT ACK 0 THROUGH UNIT ACK 3.....	89
10.2.10	INDEX.....	92
10.2.11	SECTOR.....	92
10.2.12	MASTER RESET.....	92
10.2.13	READ ENABLE.....	92
10.2.14	WRITE ENABLE.....	95
10.2.15	BI-DATA.....	97
10.2.16	SYSTEM CLOCK.....	97
10.2.17	WRITE CLOCK.....	97
10.2.18	CONTROL BUS SUMMARY.....	97
10.3	SIGNAL LINE TIMING.....	98
10.3.1	POWER-UP SEQUENCE.....	98
10.3.2	UNIT SELECT.....	98
10.3.3	SEEK.....	99
10.3.4	WRITE.....	99
10.3.5	READ.....	102
10.3.6	READ WITH OFFSET.....	105
10.3.7	INDEX-TO-SECTOR TIMING.....	105
10.3.8	STATUS WORD TIMING.....	105
10.4	FUNCTION OF CONTROL BUS COMMANDS AND STATUS.....	108
10.4.1	COMMAND WORDS.....	108
10.4.2	STATUS WORDS.....	115



10. 5	SECTOR FORMATS.....	124
10. 5. 1	28-BYTE OVERHEAD FORMAT.....	124
10. 5. 2	36-BYTE OVERHEAD FORMAT - To be specified.....	125
10. 5. 3	44-BYTE OVERHEAD FORMAT.....	125
10. 6	POWER LINES.....	126
11	ANSI DISK DRIVE INTERFACE.....	127
11. 1	KENNEDY ANSI INTERFACE.....	127
11. 2	KENNEDY ANSI Drive Power Requirements.....	127
11. 2. 1	DC Voltages and Currents.....	127
11. 2. 2	Power Connector Pin Assignments.....	128
11. 2. 3	Grounding.....	131
11. 3	Mechanical Configuration.....	131
11. 4	JUMPER OPTIONS.....	131
11. 4. 1	Description of Jumpers.....	131
11. 4. 2	Drive Select Jumpers.....	131
11. 4. 3	Control Bus Parity Checking Jumper.....	132
11. 4. 4	Model Select Jumpers.....	132
11. 4. 5	Spin Control Jumper.....	132
11. 4. 6	Sector Size Jumpers.....	132
11. 4. 7	Seek Busy Jumper.....	133
11. 4. 8	24 V - Ground Jumper.....	133
11. 4. 9	LED Jumpers and Write Protect Jumper.....	133
11. 5	Operator Controls and Displays.....	133
11. 6	General Interface Description.....	135
11. 6. 1	Definitions - State Nomenclature.....	135
11. 6. 2	Physical Characteristics.....	135
11. 6. 3	Cabling Configuration.....	135
11. 6. 3. 1	Interface Connector Specification.....	136
11. 6. 3. 2	Cable Characteristics.....	136
11. 6. 4	Electrical Characteristics.....	137
11. 6. 4. 1	Bidirectional Control Bus Lines.....	137
11. 6. 4. 2	Control Bus Drivers.....	138
11. 6. 4. 3	Control Bus Receivers.....	138
11. 6. 4. 4	Control Bus Termination.....	140
11. 6. 5	Single Ended Lines.....	140
11. 6. 6	Single Ended Line Drivers.....	140
11. 6. 7	Single Ended Line Receivers.....	140
11. 6. 8	Single Ended Line Termination.....	140
11. 6. 9	Port Enable Termination.....	140
11. 6. 10	Differential Lines.....	143
11. 6. 10. 1	Differential Line Drivers.....	143
11. 6. 10. 2	Differential Line Receivers.....	144
11. 6. 10. 3	Differential Line Termination.....	144
11. 7	Signal Definitions.....	146
11. 7. 1	Control Bus.....	147
11. 7. 1. 1	Radial Mode.....	147
11. 7. 1. 1. 1	Select Out Mode.....	147
11. 7. 1. 1. 2	Attention In Mode.....	147
11. 7. 1. 2	Daisy Chain Mode.....	148
11. 7. 1. 2. 1	Command Out.....	148

11.7.1.2.2	Parameter Out.....	148
11.7.1.2.3	Parameter In.....	149
11.7.1.3	Control Bus Bits 0-7: Select/Attention Drive_	
0-7.....		149
11.7.1.4	Control Bus Parity.....	149
11.7.2	Control Interface.....	149
11.7.2.1	Port Enable.....	149
11.7.2.2	Bus Direction Out.....	151
11.7.2.3	Select Out/Attention In Strobe.....	151
11.7.2.3.1	Select Out Strobe.....	151
11.7.2.3.2	Attention In Strobe.....	151
11.7.2.4	Command Request.....	152
11.7.2.5	Parameter Request.....	152
11.7.2.6	Bus Acknowledge.....	152
11.7.2.7	Busy.....	152
11.7.2.8	Attention.....	153
11.7.2.9	Index.....	153
11.7.2.10	Sector.....	154
11.7.2.11	Read Gate.....	154
11.7.2.12	Write Gate.....	154
11.7.3	Read/Write Signals.....	155
11.7.3.1	Read Data.....	156
11.7.3.2	Read/Reference Clock.....	156
11.7.3.3	Write Data.....	156
11.7.3.4	Write Clock.....	156
11.8	Command Structure.....	156
11.8.1	Commands with Parameter Out.....	161
11.8.1.1	Mandatory Commands with Parameter Out.....	161
11.8.1.1.1	Attention Control (Command Code 40 Hex).....	161
11.8.1.1.2	Write Control (Command Code 41 Hex).....	162
11.8.1.1.3	Load Cylinder Address Commands.....	162
11.8.1.1.3.1	Load Cylinder Address High_	
(Command Code 42 Hex).....		163
11.8.1.1.3.2	Load Cylinder Address Low (Command_	
Code 43 Hex).....		163
11.8.1.1.4	Select Moving Head (Command Codes 44_	
Hex and 45 Hex).....		163
11.8.1.2	Optional Commands with Parameter Out.....	164
11.8.1.2.1	Load Attribute Number (Command Code 50_	
Hex).....		164
11.8.1.2.2	Load Drive Attribute (Command Code 51	
Hex).....		165
11.8.1.2.3	Read Control (Command Code 53 Hex).....	165
11.8.1.2.4	Offset Control (Command Code 54 Hex).....	166
11.8.1.2.5	Spin Control (Command Code 55 Hex).....	167
11.8.1.2.6	Load Bytes Per Sector Commands.....	168
11.8.1.2.6.1	Load Bytes Per Sector High_	
(Command Code 56 Hex).....		168
11.8.1.2.6.2	Load Bytes Per Sector Medium_	
(Command Code 57 Hex).....		168
11.8.1.2.6.3	Load Bytes Per Sector Low (Command_	
Code 58 Hex).....		169

11.8.1.2.7	Load Sector Pulses Per Track Commands.....	169
11.8.1.2.7.1	Load Sector Pulses Per Track High (Cmd. Code 59 Hex).....	169
11.8.1.2.7.2	Load Sector Pulses Per Track_ Medium (Code 5A Hex).....	170
11.8.1.2.7.3	Load Sector Pulses Per Track Low_ (Cmd. Code 59 Hex).....	170
11.8.1.2.8	Load Read Permit Commands.....	170
11.8.1.2.8.1	Load Read Permit High (Command_ Code 6B Hex).....	171
11.8.1.2.8.2	Load Read Permit Low (Command Code_ 6C Hex).....	171
11.8.1.2.9	Load Write Permit Commands.....	171
11.8.1.2.9.1	Load Write Permit High (Command Code 6D Hex).....	172
11.8.1.2.9.2	Load Write Permit Low (Command_ Code 6E Hex).....	172
11.8.1.2.10	Load Test Byte (Command Code 6F Hex).....	172
11.8.2	Commands with Parameter In.....	172
11.8.2.1	Mandatory Commands with Parameter In.....	172
11.8.2.1.1	Report "Illegal Command" (Command Code_ 00 Hex).....	173
11.8.2.1.2	Clear Fault (Command Code 01 Hex).....	173
11.8.2.1.3	Clear Attention (Command Code 02 Hex).....	173
11.8.2.1.4	Seek (Command Code 03 Hex).....	173
11.8.2.1.5	Rezero (Command Code 04 Hex).....	175
11.8.2.1.6	Report Sense Byte 2 (Command Code 0D_ Hex).....	175
11.8.2.1.7	Report Sense Byte 1 (Command Code 0E_ Hex).....	175
11.8.2.1.8	Report General Status (Command Code 0F_ Hex).....	176
11.8.2.2	Optional Commands with Parameter In.....	176
11.8.2.2.1	Report Drive Attribute (Command Code 10 Hex).....	176
11.8.2.2.2	Set Attention (Command Code 11 Hex).....	176
11.8.2.2.3	Selective Reset (Command Code 14 Hex).....	176
11.8.2.2.4	Seek to Outer Stop (Command Code 15 Hex).....	177
11.8.2.2.5	Partition Track (Command Code 16 Hex).....	177
11.8.2.2.6	Report Cylinder Address Commands.....	178
11.8.2.2.6.1	Report Cylinder Address High (Command Code 29 Hex).....	179
11.8.2.2.6.2	Report Cylinder Address Low_ (Command Code 2A Hex).....	179
11.8.2.2.7	Report Read Permit Commands.....	179
11.8.2.2.7.1	Report Read Permit High (Command_ Code 2B Hex).....	179
11.8.2.2.7.2	Report Read Permit Low (Command Code 2C Hex).....	179
11.8.2.2.8	Report Write Permit Commands.....	180

11.8.2.2.B.1 Report Write Permit High (Command Code 2D Hex).....	180
11.8.2.2.B.2 Report Write Permit Low (Command Code 2E Hex).....	180
11.8.2.2.9 Report Test Byte (Command Code 2F Hex)....	180
11.8.2.3 KENNEDY Unique Commands.....	180
11.8.2.3.1 Report Sense Byte 3 (Command Code 30_ Hex).....	181
11.8.2.3.2 Report Diagnostic Results (Command Code 31 Hex).....	181
11.8.2.3.3 Report Sense Byte 4 (Command Code 32_ Hex).....	181
11.8.2.3.4 Report Sense Byte 5 (Command Code 33_ Hex).....	181
11.8.3 Drive Attribute Commands.....	186
11.8.3.1 User ID (Number 00 Hex).....	187
11.8.3.2 Model ID High (Number 01 Hex).....	187
11.8.3.3 Model ID Low (Number 02 Hex).....	187
11.8.3.4 Revision ID (Number 03 Hex).....	188
11.8.3.5 Device Type ID (Number 0D Hex).....	188
11.8.3.6 Table Modification (Number 0E Hex).....	188
11.8.3.7 Table ID (Number 0F Hex).....	189
11.8.3.8 Bytes Per Track.....	189
11.8.3.8.1 Bytes Per Track High (Number 10 Hex).....	190
11.8.3.8.2 Bytes Per Track Medium (Number 11 Hex)....	190
11.8.3.8.3 Bytes Per Track Low (Number 12 Hex).....	190
11.8.3.9 Bytes Per Sector.....	190
11.8.3.9.1 Bytes Per Sector High (Number 13 Hex)....	190
11.8.3.9.2 Bytes Per Sector Medium (Number 14 Hex)...	190
11.8.3.9.3 Bytes Per Sector Low (Number 15 Hex)....	191
11.8.3.10 Sector Pulses Per Track.....	191
11.8.3.10.1 Sector Pulses Per Track High (Number 16 Hex).....	191
11.8.3.10.2 Sector Pulses Per Track Medium (Address 17 Hex).....	191
11.8.3.10.3 Sector Pulses Per Track Low (Number 18 Hex).....	191
11.8.3.11 Sectoring Method (Number 19 Hex).....	191
11.8.3.12 Number of Cylinders.....	192
11.8.3.12.1 Number of Cylinders High (Number 20_ Hex).....	192
11.8.3.12.2 Number of Cylinders Low (Number 21 Hex).....	192
11.8.3.13 Number of Moving Heads (Number 22 Hex).....	192
11.8.3.14 Number of Fixed Heads (Number 23 Hex).....	192
11.8.3.15 Select Head Implementation (Number 24 Hex)....	192
11.8.3.16 Header Encoding Method #1 (Number 30 Hex)....	193
11.8.3.17 Preamble #1 Length (Number 31 Hex).....	193
11.8.3.18 Preamble #1 Pattern (Number 32 Hex).....	193
11.8.3.19 Synchronization #1 Pattern (Number 33 Hex)....	193
11.8.3.20 Postamble #1 Length (Number 34 Hex).....	193

11.8.3.21	Postamble #1 Pattern (Number 35 Hex)	193
11.8.3.22	Gap #1 Length (Number 36 Hex)	194
11.8.3.23	Gap #1 Pattern (Number 37 Hex)	194
11.8.3.24	Data Encoding Method #2 (Number 40 Hex)	194
11.8.3.25	Preamble #2 Length (Number 41 Hex)	194
11.8.3.26	Preamble #2 Pattern (Number 42 Hex)	194
11.8.3.27	Synchronization #2 Pattern (Number 43 Hex)	194
11.8.3.28	Postamble #2 Length (Number 44 Hex)	195
11.8.3.29	Postamble #2 Pattern (Number 45 Hex)	195
11.8.3.30	Gap #2 Length (Number 46 Hex)	195
11.8.3.31	Gap #2 Pattern (Number 47 Hex)	195
11.8.4	Fault Reporting	199
11.8.4.1	General Status Byte	199
11.8.4.1.1	Bit 0 - Not Ready	199
11.8.4.1.2	Bit 1 - Control Bus Error	200
11.8.4.1.3	Bit 2 - Illegal Command	201
11.8.4.1.4	Bit 3 - Illegal Parameter	201
11.8.4.1.5	Bit 4 - Sense Byte 1	202
11.8.4.1.6	Bit 5 - Sense Byte 2	202
11.8.4.1.7	Bit 6 - Busy Executing	202
11.8.4.1.8	Bit 7 - Normal Complete	202
11.8.4.2	Sense Byte 1	202
11.8.4.2.1	Bit 0 - Seek Error	203
11.8.4.2.2	Bit 1 - Read/Write Fault	203
11.8.4.2.3	Bit 2 - Power Fault	204
11.8.4.2.4	Bit 3 - Read/Write Permit Violation	204
11.8.4.2.5	Bit 4 - Speed Error	205
11.8.4.2.6	Bit 5 - Command Reject	205
11.8.4.2.7	Bit 6 - Other Errors/Sense Byte 3	206
11.8.4.2.8	Bit 7 - Diagnostic Byte	206
11.8.4.3	Sense Byte 2	206
11.8.4.3.1	Bit 0 - Initial State	207
11.8.4.3.2	Bit 1 - Ready Transition	207
11.8.4.3.3	Bit 5 - Drive Attribute Table Modified	207
11.8.4.3.4	Bit 6 - Positioned Within Write Protected Area	207
11.8.4.3.5	Bits 2, 3, 4, and 7	208
11.8.4.4	Sense Byte 3	208
11.8.4.4.1	Bit 0 - Spin Error	208
11.8.4.4.2	Bit 1 - PLO Error or Write Gate and Not Fine Track	208
11.8.4.4.3	Bit 2 - Guard Band Error	209
11.8.4.4.4	Bit 3 - Outer Stop	209
11.8.4.4.5	Bit 4 - Park Lock	209
11.8.4.4.6	Bits 5, 6, and 7 - Reserved	209
11.8.4.5	Diagnostic Results Byte	209
11.8.4.5.1	Bit 0 - RAM Error	210
11.8.4.5.2	Bit 1 - PROM No. 1 Error	210
11.8.4.5.3	Bit 2 - PROM No. 2 Error	210
11.8.4.5.4	Bits 3, 4, 5, 6, and 7 - Reserved	210
11.9	Timing Specification	210

11.9.1	Control Bus Timing.....	211
11.9.1.1	Selection Timing.....	211
11.9.1.2	Attention Timing.....	211
11.9.1.3	Control Bus Handshake Timing.....	212
11.9.2	Index and Sector Timing.....	212
11.9.3	Reference Clock Timing.....	212
11.9.4	Read Timing.....	213
11.9.5	Write Timing.....	213
11.10	Formatting Considerations.....	220
11.10.1	Sector Format.....	220
11.10.2	Layout of the Sector.....	221
11.10.2.1	Preamble #1 and Preamble #2.....	221
11.10.2.2	Synchronization #1 and Synchronization #2.....	221
11.10.2.3	Header Information.....	222
11.10.2.4	Gap #1 and Gap #2.....	222
11.10.2.5	Data Information.....	222
11.10.2.6	Postamble #1 and Postamble #2.....	222
11.10.3	Format Examples.....	222
11.10.4	Division of a Track Into Sectors.....	223
11.10.5	Typical Read Sequence.....	224
11.10.6	Typical Write Sequence.....	224



SECTION 1  
BASIC DRIVE UNIT SPECIFICATION

1 SCOPE

This document describes the Kennedy Company Series 6170 fixed Disk Drive and its available configurations.

2 RELATED DOCUMENTATION

6170 Maintenance Manual Part Number 193-6170-001

3 GENERAL DESCRIPTION

3.1 EQUIPMENT DEFINITION

The Series 6170 is a fixed media moving head disk drive utilizing advanced "Winchester" head and media technology. The drive incorporates up to three disks, each of which is 210 millimeters (8.269 inches) in diameter. The Series currently offers two different models; The 6172, offering an unformatted capacity of 24 Megabytes, and the 6173, offering an unformatted capacity of 40 Megabytes. The two models differ only in the number of disks installed. The disks are rotated by a brushless DC motor at a nominal speed of 3600 rpm. A linear voice-coil actuator positions a low mass head-carriage assembly over 614 useable cylinders using a closed-loop servo system. The disks, head-carriage assembly, and heads are enclosed within an ultra-clean sealed environment maintained by a closed-loop air filtration system. The Disk Drive Unit contains four printed circuit board assemblies (PCBA's); one PCB performs read-write functions; the second supports servo positioning; the third is a PCB in the drive motor; and, the fourth is one of three different interfacing boards.

4 INTERFACE OPTIONS

In addition to the defacto industry standard Storage Module interface, the Series 6170, offers an ANSI X3T9.3/1226 or the KENNEDY DISKBUS interface. Refer to the appropriate section in this document.



## 5 UNIT DEFINITION

The Kennedy 6170 Disk Drive Unit is a 210 mm (8.268 inch) fixed disk storage unit which permits random access to concentric tracks, called "cylinders" on up to three storage disks. Data can then be recorded on or read-back from a track using read-write heads to electromagnetically commute the data to or from the disks, which rotate at 3600 rpm.

The 6170 may be mounted within a host system, an operator's console, in a 19-inch RETMA rack, within a desk, or on top of a desk, table or shelf; an air-conditioned environment is not necessary.

Seek, read and write operations in the 6170 are carried out in response to programmed instructions from a host central processing unit (CPU). The host CPU sends instructions to the 6170 via a Controller-Formatter which is supplied by the customer. Nomenclature used throughout this specification and the Interface Specification is as defined in the next paragraph and as shown in Figure 1-1.

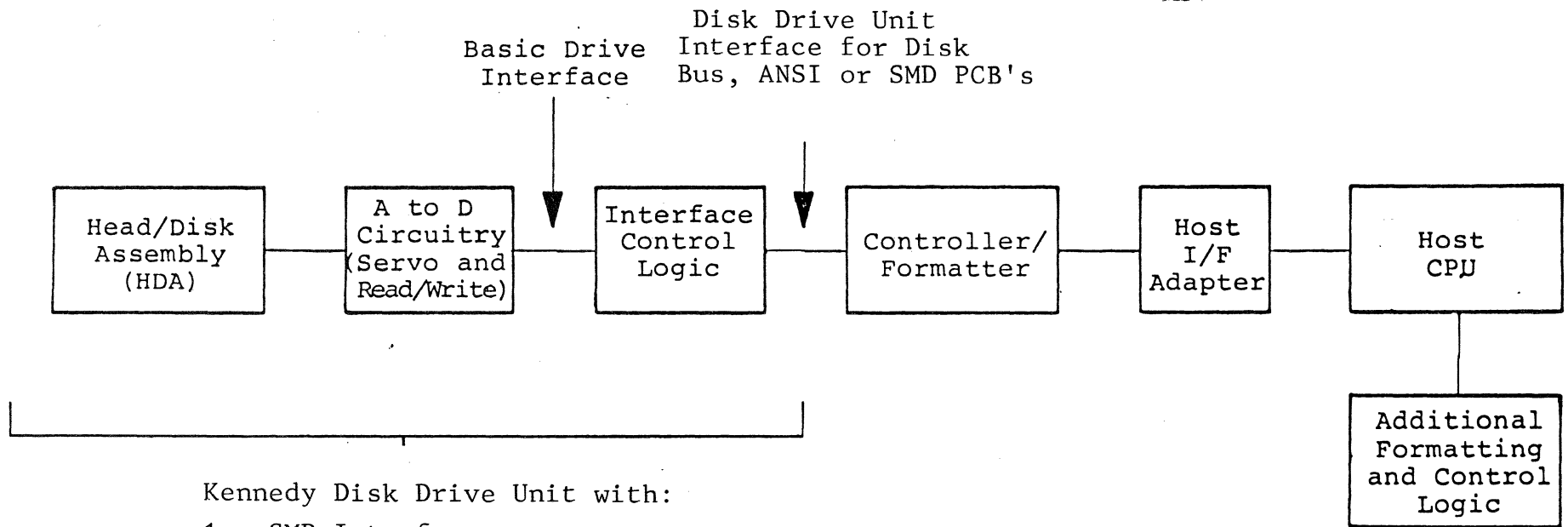
The interface nomenclature for systems which use the 6170 drive is explained further below. Reference should again be made to Figure 1-2.

**HEAD/DISK ASSEMBLY (HDA)** - The HDA contains the disks, drive motor, the heads and head-positioner needed for all models of the 6170. These components are all mounted on a common base assembly and are enclosed in a pressurized clean air chamber. There is an "analog" interface between the HDA and the Servo/Read-Write PCB'S.

**ANALOG TO DIGITAL CIRCUITRY (A TO D)** - The servo PCB controls head positioning circuitry.... The Read/Write PCB controls the transducer action of the read/write heads. There is a digital interface between the Servo and Read/Write PCB's and the interface Board.

**CONTROL LOGIC** - Control Logic is located on the Interface Board, the customer's Controller-Formatter, and the hardware/software of the host central processing unit (CPU).

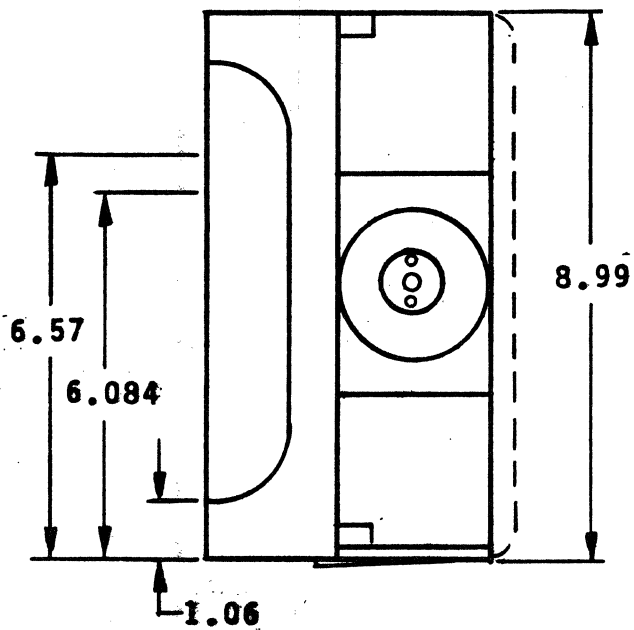
**HOST INTERFACE ADAPTER** - The Host Interface Adapter is also supplied by the customer. It adapts the customer's Controller-Formatter to the I/O front-end of the host CPU. The Controller-Formatter and the Host I/F Adapter may be combined on one PCB.



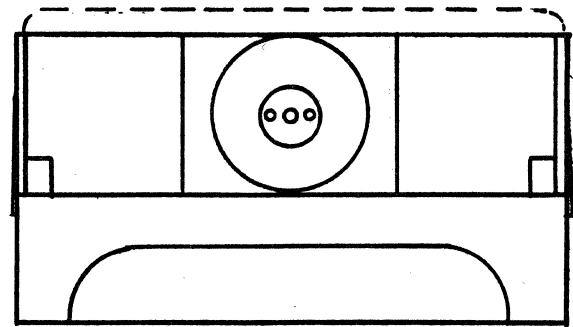
Kennedy Disk Drive Unit with:

1. SMD Interface
2. ANSI Interface
- or . . . . .
3. Disk Bus Interface

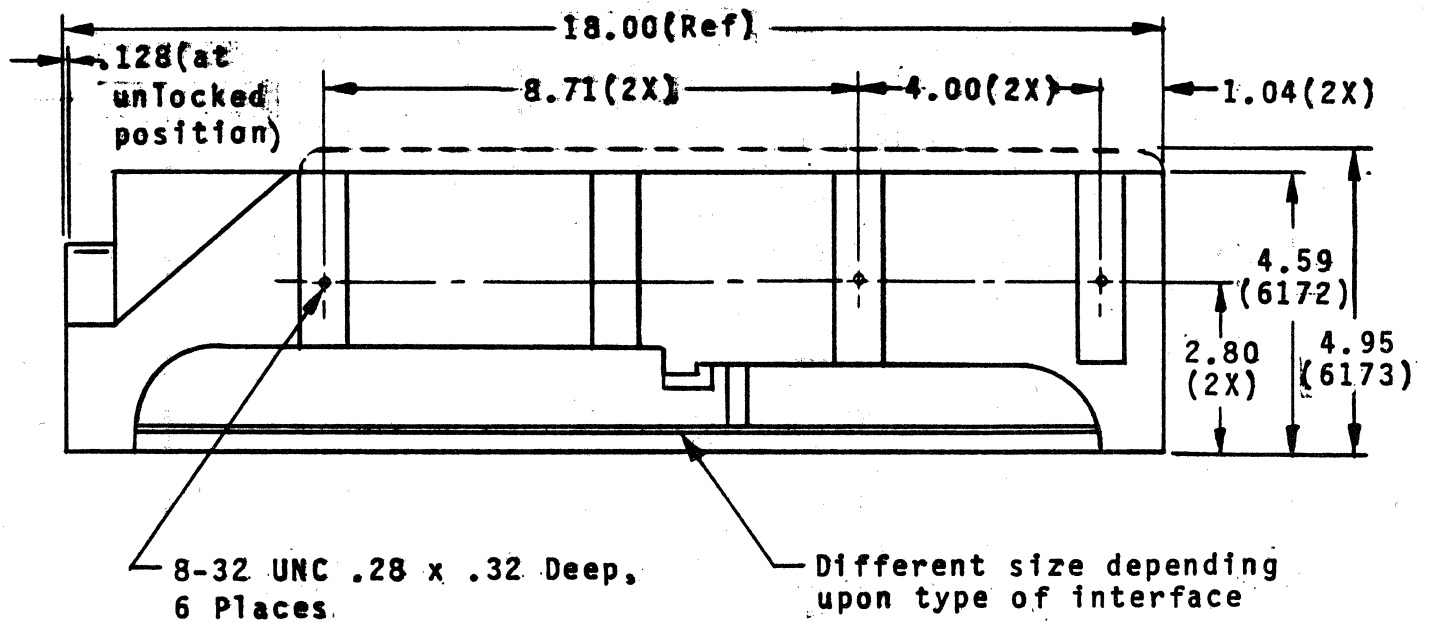
Figure 1-1 Interface Nomenclature



Vertical Mounting Position.



Horizontal Mounting Position



8-32 UNC .28 x .32 Deep, 6 Places.

Different size depending upon type of interface

Notes: Unless Otherwise Specified

1. Maximum screw insertion: .25.  
Maximum torque: 6 in. Lbs.
2. Dimensions in inches.

Figure 1-2 Physical Interface

6 MODELS, OPTIONS, SPARES AND ACCESSORIES

## 6.1 MODELS

Two different models of the 6170 Series are currently available; differentiation is made on the basis of storage capacity. Table 1-1 shows the specifications of the 6170 Series which vary by model number.

TABLE 1-1 SPECIFICATIONS BY MODEL NUMBER

SPECIFICATIONS	MODELS OF THE 6170 SERIES	
	6172	6173
Data Capacity		
Unformatted	24.5 MB	40.9 MB
Formatted*	22.6 MB	37.7 MB

\*Formatting at 512 bytes per sector. See "Recording," in Paragraph 4.1.

## Data Organization:

No. of Disks	2	3
No. of Heads/Surface	1	1
Data Surface	3	5
Total Available Data Tracks	1,842	3,070
Total Available Cylinders	614	614
Guard-Band Tracks* (35 inside, 55 outside)	270	450

\*NOTE: These are not available to the user.

## 6.2 ACCESSORIES

### 6.2.1 SIGNAL CABLES

Signal cable types vary with the types of interface boards that are used. These cables must be fabricated by the user.

A. SMD Interface PCB. Two Types of Signal Cables are used:

Type A - 60-conductor flat ribbon cable, 30 m (100 ft.) maximum cable length. The connector is AMP Part No. 88376-9, or equivalent.

Type B - 26-conductor flat ribbon cable, 15 m (50 ft.) maximum cable length. The connector is AMP Part No. 88376-5, or equivalent.

B. Disk Bus PCB.

40-conductor flat ribbon cable 9.14 m (30 ft.) maximum cable length. The connector is AMP Part No. 88610-7, or equivalent.

C. ANSI

50-conductor flat ribbon cable 3.0 m (10 ft.) maximum length. The connector is AMP Part No 1-102160-0 or equivalent.

### 6.2.2 POWER CABLE

For all interface boards the power cable shall be 10-conductor, 18-gauge wire, 1.2m (4 ft.) total cable length. The connector is AMP Part NO. 1-640426-0, or equivalent. The power supply is supplied by the customer.

### 6.2.3 TERMINATORS

Terminators vary primarily with the way in which the drives are connected ( eg. - daisy-chained or radial). Each drive of a radially-connected subsystem must be individually terminated. Only the last drive of a daisy-chained string needs to be terminated. A description of what is required, by type of interface, is in the interface specifications. Radial connection is always assumed. Customers must remove un-needed terminators from daisychained drives.

#### 6.2.4 SHOCK MOUNTS

Shock mounts must be used in situations where a drive will be subjected to greater shock than specified in paragraph 4.5.4 and 4.5.5. Commercially available shock-mounts (to be specified) are adequate.

### 7 SPECIFICATIONS

#### 7.1 RECORDING

##### 7.1.1 RECORDING METHODS

The Kennedy 6170 uses the modified frequency modulation (MFM) method of recording. Write data is presented serially to the drive from the interface board. Bit cell time is 156 +/- 5 nanoseconds. A logical 1 is represented by a transition at the middle of a bit cell time; a logical zero is represented by a transition at the beginning of a bit cell time, with the exception of a 1 followed by a 0, the transition of which is omitted.

##### 7.1.2 RECORDING CHARACTERISTICS

Minimum Bit Density (Cylinder 000)	4,444 bits/inch
Maximum Bit Density (Cylinder 613)	6,542 bits/inch
Track Density	500 tracks per inch
Nominal Data Transfer Rate	800,640 Bytes/second (6.41 M Bits/second)
Disk Rotation Speed	3,600 RPM+/-1%

7.1.3 STORAGE MEDIA

- A. Storage Media are ferrous oxide coated aluminum alloy disks with inner and outer diameters as listed below:
  - Outer Diameter: 210 +/- .1 mm (8.268 +/- .004in.)
  - Inner Diameter: 100 +/- .1, -0 mm (3.937 + .004, - 0.00 in.)
- B. The thickness of the disk is 1.905 +/- .025 mm (0.075 +/- .001 inch).
- C. The edge chamfer does not exceed 1.3 mm (.05 inch).

7.1.4 READ-WRITE HEADS

The linear voice-coil actuator positions a head assembly which contains one head per disk surface. The disk surface closest to the drive motor contains a servo head; the remaining heads (up to 5) are data heads.

7.1.5 DATA CAPACITY

A. Unformatted Data Capacity

Track Capacity (614 Tracks)	13,344 Bytes
Surface Capacity	8,193,216 Bytes

B. Formatted Data Capacity - 28 Byte sector overhead (allowance for head-switching and PLO lock-up).

BYTES PER SECTOR	SECTORS PER TRACK
-----	-----
128	84
256	46
512	24
1,024	12
2,048	6
4,096	3
13,188	1

C. Formatted Data Capacity - 36-byte sector overhead (allowance for head-switching and PLD lock-up in controllers which are not fast enough to utilize the 28-byte overhead, but do not want to use the 44-byte alternative). NOTE: AVAILABLE ON DISK BUS INTERFACE PCB ONLY.

Bytes per Sector	Sectors per Track
128	80
256	45
512	24
13,180	1

D. Formatted Data Capacity - 44 byte per sector overhead (allowance for head - switching and PLD lock - up in controllers not fast enough to utilize the 28 - byte overhead)

Bytes per Sector	Sectors per Track
128	76
256	44
512	23
1,024	12
2,048	6
4,096	3
13,172	1

## 7.2 ACCESS

### 7.2.1 POSITIONING TIME

Positioning time is defined as the time between the initiation of a seek command and the time when the head carriage is settled at the desired cylinder, as indicated by the activation of the "seek end" signal, in the environment specified herein.

Minimum positioning time is the time that it takes to position from one track to the next adjacent track, in either direction. This time is 8 milliseconds.

Average "total" positioning time can be computed by dividing the time required to perform all possible seeks by the total number of possible seeks. Average positioning time is 40 milliseconds.

Maximum positioning time is defined as the time that it takes to position from track number 0 to track number 613. This time is 80 milliseconds.



### 7.2.2 ROTATIONAL LATENCY TIME

Average rotational latency time is defined as one-half of the nominal time that it takes to complete one disk revolution. It is the average time that is taken to reach a defined place in a cylinder after positioning has been completed.

Average rotational latency time	8.33 ms
Average time for one revolution	16.67 ms

### 7.2.3 OTHER TIMING CONSIDERATIONS

A. Power On Time (time until ready)	20 seconds
B. Power Off to Head Land	20 seconds
C. PLO Lock-up time (read gate to first data character)	7.5 us +/-10%
D. Read/Write transition time	1.2 us max.

## 7.3 RELIABILITY

### 7.3.1 SERVICE DATA

#### A. Service Life

The Kennedy 6170 has an expected life of 5 years or 20,000 hours, whichever comes first. After the service life has been reached, the drive should be returned to the factory for overhaul, upgrade and recertification (i.e., re-establishment of warranty).

#### B. MTBF (Mean Time Between Failures)

$$\text{MTBF} = \frac{\text{No. of Operating Hours (Power On)}}{\text{No. of Equipment Failures}}$$

An equipment failure, for purposes of the above calculation, is any deviation from specified performance as described in these specifications. It does not include failures caused by the following:

- \* Operator error.
- \* User's controller/formatter, host adaptor, CPU or retry procedures not functioning properly.
- \* Opening of the sealed HDA.
- \* Multiple failures resulting from the initial cause
- \* Failures produced by a repairman while attempting to fix a reported problem.
- \* Unauthorized modifications.

MTBF calculations could be made only after 90 days of operating or after 1,500 operating hours following installation (to eliminate the variable of "infant mortality"). In addition, the test sampling should include at least 10 drives which have a combined operating time of at least 10,000 hours.

The MTBF of the Disk Drive Unit (HDA plus three PCB's) is 10,000 hours. The MTBF of the HDA is 25,000 hours.

#### C. MTTR (Mean Time to Repair)

MTTR is defined as the average time required by an adequately trained and competent service person to diagnose and repair a failure at the subassembly level. This does not include the time needed to acquire replacement parts, if applicable.

The specified MTTR is 0.5 hours.

#### D. Preventive Maintenance

The 6170 requires no preventive maintenance.

### 7.3.2 DATA ERROR RATES

Data errors are classified into two categories:

- \* Recoverable:  $<1$  error  $10^{10}$  bits read
- \* Non-recoverable:  $<1$  error  $10^{12}$  bits read

These error rates assume the following:

1. Initially, no media flaws exist; all detectable flawed areas were marked as unusable by the customer using an initialization routine which is executed on the Host CPU.
2. The data is properly written; the user can assure that data is properly written by using the CRC or by comparing what was read against what was written.
3. When properly written data is read-back, the user must program-in up to 27 retries, with track off-set and with data strobe timing variations, before it is assumed to be a hard error.

In actuality, there are 9 combinations of 3 retries required for a total of 27 retries. The retries must include:

- a) center-track
- b) off-track toward the inner diameter, and
- c) off-track toward the outer diameter.

They must also include:

- a) normal read,
- b) data strobe early, and
- c) data strobe late.

If all these attempts fail, the error is a hard error.

### 7.3.3 SEEK ERRORS

A seek error is defined as the inability of the drive to assert "Seek End" within the specified time-frame. Seek errors are assumed to be recoverable. The allowable error rate is as follows:

6

<1 recoverable error in  $1 \times 10^6$  seeks (recoverability is as defined below)

This specification assumes that the user programs-in a verification to assure that the cylinder which was found is the cylinder which was sought. If there is a mis-seek, there must be a reset to cylinder zero followed by a re-seek. There are up to nine of these retries programmed-in by the user, with three levels of track orientation and three levels of data strobing. If after 27 tries, the correct cylinder cannot be verified, the failure is assumed to be unrecoverable read error (i.e., inability to read the correct track ID due to a positioner, head, media or circuitry failure).

#### 7.3.4 ERROR RECOVERY

Disk drives which leave the factory are allowed a maximum of 8 media defects per data surface. Also, it is possible that a media error may develop on the disk over time. The user should be prepared to relocate the sector containing the error to another location on the disk drive and mark the defective sector to make it unusable in the future; this would be done using an initialization routine. The 1 error in one trillion data-bits-read statistic in paragraph 7.3.2 includes errors which occur over time. The media errors are flagged and ignored because of customer action.

#### 7.4 PHYSICAL

##### 7.4.1 DIMENSIONS

	<u>METRIC</u>	<u>ADP</u>
Length	45.72 centimeters	18.00 inches
Width	22.83 centimeters	8.99 inches
Height:		
(6172)	11.66 centimeters	4.59 inches
(6173)	12.57 centimeters	4.95 inches

##### 7.4.2 WEIGHT

Model 6172 - 9.1 Kilograms (20 pounds)

Model 6173 - 9.5 Kilograms (21 pounds)

## 7.4.3 SOUND EMISSION

Meets NC 55 requirements.

## 7.4.4 PHYSICAL INTERFACE

Mounting orientation, connector locations and mounting holes are all shown in Figure 2-3.

## 7.4.5 POWER REQUIREMENTS

The 6170 Series of 8-inch Fixed Disk Drives uses only DC power. The power requirements vary as a function of which interface boards are used with the disk drive unit.

## A. SMD Drive DC Power Requirements:

<u>DC VOLTAGE</u>	<u>MAX CURRENT</u>	<u>MAX RIPPLE (p-to-p)</u>
+24V +/-2V	2A (6A surge)	250 mv
+12V +/-5%	0.5A	100 mv
+5V +/-5%	5A	50 mv
-12V +/-5%	0.5A	100 mv
-5V +/-5%	3A	50 mv

## B. Disk Bus DC Power Requirements:

<u>DC VOLTAGE</u>	<u>MAX CURRENT</u>	<u>MAX RIPPLE (p-to-p)</u>
+24V +/-2V	5A (6A surge)	250 mv
+12V +/-5%	0.5A	100 mv
+5V +/-5%	2A	50 mv
-12V +/-5%	0.5A	100 mv
-5V +/-5%	2A	50 mv

## C. ANSI Interface DC Power Requirements:

<u>DC VOLTAGE</u>	<u>MAX CURRENT</u>	<u>MAX RIPPLE (p-to-p)</u>
+24V +/-2V	5A (6A surge)	250 mv
+12V +/-5%	0.5A	100 mv
+5V +/-5%	2A	50 mv
-12V +/-5%	0.5A	100 mv
-5V +/-5%	2A	50 mv

## 7.4.6 POWER CONSUMPTION

## A. SMD Drive DC Power Consumption

Operating: 75 Watts (random seeks)  
Idle: 50 watts (heads stationary)

## B. Disk Bus Drive DC Power Consumption

Operating: 65 watts (random seeks)  
Idle: 40 watts (heads stationary)

## C. ANSI Drive DC Power Consumption

Operating: 92 watts (random seeks)  
Idle: 68 watts (heads stationary)

## 7.4.7 SAFETY

All models of the 6170 drive series shall meet the requirements of the following national certifying groups:

Underwriter's Laboratories (USA)

Canadian Standards Association (CSA)

VDE (Germany)

British Standards Institution (BSI)

European Common Market Electrical Standards

## 7.5 ENVIRONMENT

The Kennedy 6170 shall perform as specified in this specification and the interface specification when the following environmental conditions are known to exist.

### 7.5.1 TEMPERATURE

Operating:           <sup>o</sup>+10 C to <sup>o</sup>+45 C (<sup>o</sup>+50 F to <sup>o</sup>+113 F)  
Non-operating:   <sup>o</sup>-40 C to <sup>o</sup>+60 C (<sup>o</sup>-40 F to <sup>o</sup>+140 F)

NOTE: Temperature changes shall not exceed <sup>o</sup>20 F per hour (operating and non-operating) and shall not produce condensation.

### 7.5.2 RELATIVE HUMIDITY

Operating and non-operating: 15 to 80 % with a  
maximum wet bulb temperature of <sup>o</sup>27 C (<sup>o</sup>80 F).

NOTE: Humidity changes shall not exceed 20 % per hour, no condensation.

### 7.5.3 ATMOSPHERIC PRESSURE

Operating:           To be specified.

Non-operating: Pressures that would result from -300 meters (-984 ft.) to 11,000 meters (36,080 ft.) in relationship to mean sea level.

### 7.5.4 VIBRATION

A. Operating: The drive shall withstand a peak displacement of +/- .003-inch (.075 mm) within the frequency range of 5 to 58 Hz; the drive shall withstand a peak displacement of +/-1 G of acceleration within the frequency range of 58 to 500 Hz.

Application with over .5 G of acceleration must provide additional shock absorption at the mounting points. These must be supplied by the user.

B. Non-Operating: To be specified.

C. Shipping: When packed for shipment, the drive shall withstand +/-1.5 G's of acceleration from 5 to 58 Hz for one hour along each of three mutually perpendicular axes.

#### 7.5.5 SHOCK

A. Operating: The drive, while positioned on track, reading or writing, shall withstand 18 impact shocks of 3 G's maximum acceleration, consisting of 3 shocks along each direction of 3 mutually perpendicular axes. Each shock impulse shall be a half-sine wave 11 milliseconds (+/-1 millisecond) duration separated by a minimum of 10 seconds.

B. Non-Operating: To be specified.

C. Shipping: To be specified.

#### 7.5.6 ELECTROMAGNETIC RADIATION

Must meet requirements of VDE (Germany) and FCC (USA).

### 8 DATA STORAGE CHARACTERISTICS

The data storage elements of the Kennedy 6170 Series of disk drives are two or three pre-mapped disks. Figure 1-3 shows the data storage characteristics of a two-disk 6172. The two disks, collectively, are called a "disk stack". Each disk consists of an aluminum substrate which is coated with a very thin, even, coating of ferrous oxide and an overcoating of protective lubricant. Data is written on the magnetic coating as described in Recording, Subsection 7.1. Sector sizes are selected using a switch (or jumper) on the interface PCB. The switch/jumper setting must be the same for Read operations as it was for Write.

Each disk stack contains a servo surface which is prerecorded at the factory and which provides signals via the servo head to the interface board to be used:

- a) to decrement a cylinder difference-counter during a seek, and;
- b) for track-following during Read and Write.



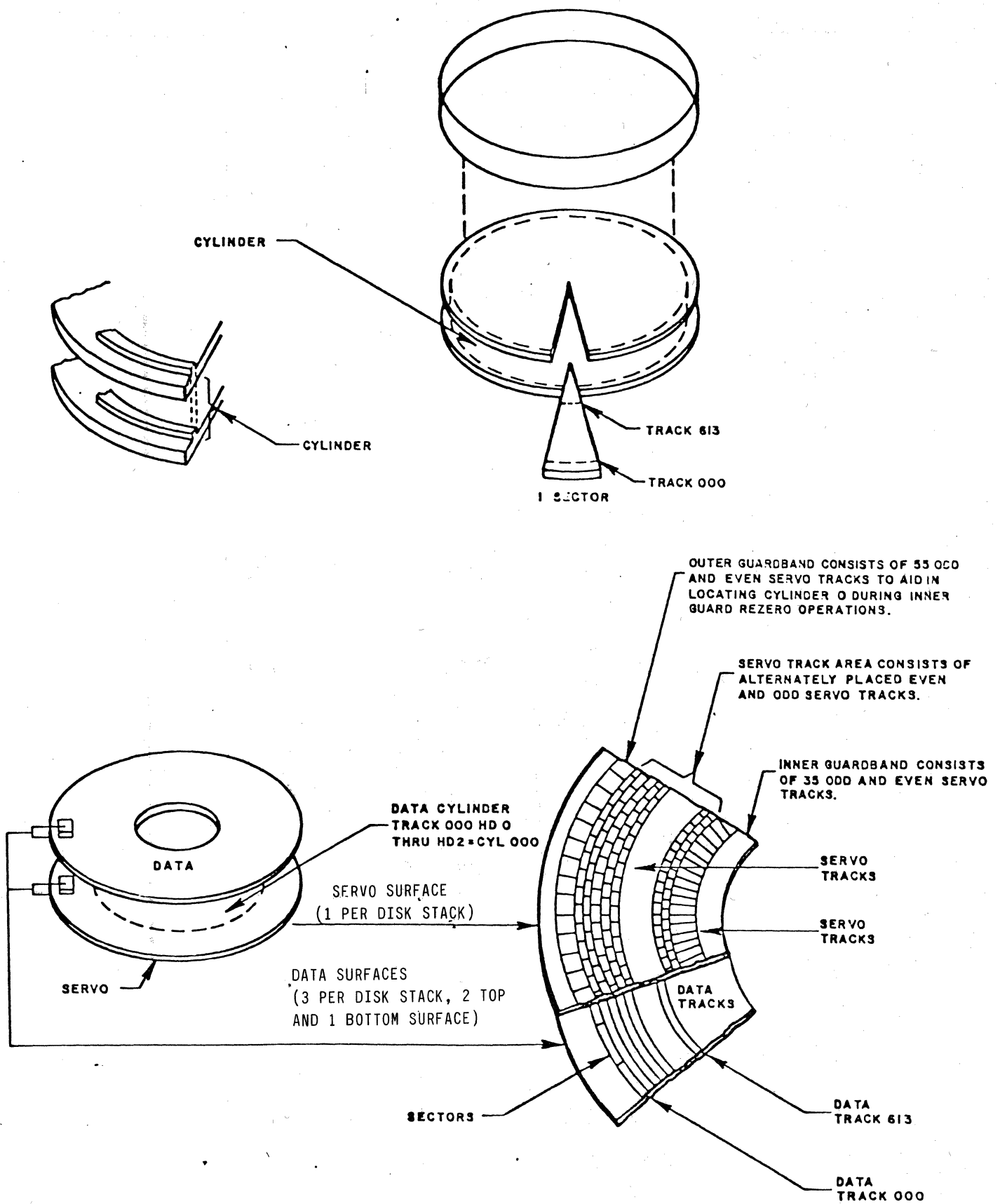


Figure 1-3 Disk Storage Characteristics

The servo surface is the bottom surface of the bottom disk.

The ferrous oxide coating can occupy one of three states: The first state is a non-magnetized state; the other two states are saturation in one direction or saturation in the other direction. Reversals of saturation are detectable and can be coded to represent the presence or absence of a bit of data. Bits of data are serially written in a track under the guidance of logic in the host's Controller-Formatter. Eight bits are assumed to represent a byte. The number of bytes per sector and per track vary as a function of a sector size selection on the Interface Board. Users often include error-detection and correction codes to improve the data error rates which are intrinsic to the storage method.

### 8.1 POWER-UP SEQUENCE

After power is initially applied to the drive, the servo is disabled to allow sufficient time for the spindle motor to come-up to speed and cause the heads to fly stably. After the spindle motor is up to speed and all power supply voltages have stabilized, the drive will automatically recalibrate itself using a Rezero command.

### 8.2 DRIVE UNIT SELECTION

Each interface requires a different unit selection method. Refer to the appropriate section for details.

### 8.3 CYLINDER AND HEAD SELECTION; HEAD TRACKING

While the disk drive is being used by the host computer system, there is a continuing need to position the head carriage assembly at a different one of the 614 possible cylinders. Further, the host will have a need for operating with only specific sectors on specific tracks. The drive responds to the host's desire to access a specific cylinder and a specific head by positioning the head carriage assembly to the desired cylinder and activating the desired head. The action of positioning is called a "Seek".

Logic in the Interface PCB always knows the current cylinder address because it is stored in a register which is called the Present Address Register (PAR). The Controller-Formatter sends over the address of the cylinder it wants to Seek and the head that it wishes to activate for the Seek action. The difference between where the head carriage is and where the Controller-Formatter wants it to go is used to generate a linear motor actuator drive signal and a direction of drive. A closed-loop servo system causes the head carriage to be moved in the direction of the desired cylinder. Once there, the head is "held" on track by servo action i.e., if the heads drift off track, an error voltage will be generated and fed-back in a way that produces drive in a direction that reduces the error. This is called "Servo-tracking" or "head tracking". Tachometer type feed-back controls the velocity of track crossings, and as the desired track is approached, it minimizes any tendency toward oscillating around the desired track.

#### B.4 FORMAT SELECTION

Format control varies according to the interface in use. Refer to the appropriate section of this manual for details.

#### B.5 DATA PROTECTION AND FAULT SENSING

Logic exists to provide the following data protection options:

1. The entire surface is write-protected by the Write Protect Switch (SMD) or Jumper (Disk Bus).
2. The entire drive is write-protected by the Write Protect Jumper (ANSI).
3. The fault signal is given to the Controller-Formatter if any one of the following conditions exist:
  - a) Write enabled while the heads are off track or "offset"
  - b) Write enabled but no write clock.
  - c) Write and Read enabled at the same time.
  - d) More than one head selected at a time.
  - e) Write enabled on a Write protected head.
  - f) PLO unlocks while writing.

### 8.6 SEEK

Seeking is the process of positioning the carriage assembly at the desired cylinder. A linear voice-coil actuator positions the head carriage assembly at varying speeds toward the desired cylinder. "Speed" is related to the size of the displacement between current location and desired location. As successive cylinders are crossed, the register that keeps track of the current location is decremented to reduce the size of the displacement.

### 8.7 WRITE

After it has been ascertained (using a Read operation) that the active head is on the desired track and at the desired sector, writing can take place. Write clock pulses (derived from disk servo pulses) are sent back to the Controller-Formatter where they are used as write clock pulses to synchronize writing on the disk. NRZ (non-return-to-zero) write data is sent to the drive from the Controller-Formatter. It is encoded to MFM (modified frequency modulation) and synchronized by write clock pulses. NOTE: MFM coding permits the storage of more bits to the inch than straight NRZ.

### 8.8 READ

The active head senses the flux changes in the disk coating and sends the resultant analog signal to shaping and amplification circuits. A read clock pulse is generated from the data that is read; the "squared" signals are decoded from MFM to NRZ thus returning the signals to the Controller-Formatter in the same form that they were presented during Write.

## SECTION 2

## INTERFACE SPECIFICATIONS

This section contains the Product Specifications for the "interface" between the three different configurations of 6170 Disk Drives and the host system to which they can be connected.

There is a separate "specification" for each of the three different configurations of 6170 Disk Drives. The drive, including an interface board, is called a Disk Drive Unit; without an interface board, it is called a Basic Drive Unit.

<u>TITLE</u>	<u>PAGE</u>
SMD Disk Drive Unit Interface	23
Disk Bus Disk Drive Unit Interface	68
ANSI Disk Drive Unit Interface	127

Comments, questions and suggestions on these specifications should be sent to:

KENNEDY COMPANY, C/O MARKETING  
1600 SHAMROCK AVENUE  
MONROVIA, CALIFORNIA 91016

## 9 SMD DISK DRIVE INTERFACE

This specification describes the interface between 1) the SMD Interface PCB on the Disk Drive Unit which is described in Section 1 of this manual and 2) a Controller-Formatter which has an SMD Interface.

### 9.1 PHYSICAL AND ELECTRICAL INTERFACE DEFINITION

The "interface" is defined as the signal lines and power lines that must be connected to Jacks JA, JB and JP on the SMD Interface PCB in order for the Series 6170 to function as described in this Product Specification. JA is a receptacle for a 60-conductor ribbon cable; JB is a receptacle for a 26 conductor ribbon cable; JP is the receptacle for a 10-wire power cable. The "interface" has a variety of characteristics such as: physical properties, electrical properties, timing, logical interrelationships, and formatting considerations. All of these are included in the term "interface" and are described in this specification in terms of what can be seen at individual pins of JA, JB and JP, which are collectively called, the SMD INTERFACE. The SMD Interface is shown in Figure 2-1.

A cable diagram showing how the interface bus relates to cables A, B and the power cable is given in Figure 2-2, Interface Cables.

Figure 2-3 is a functional block diagram of the disk drive subsystem which uses the interface lines shown in Figure 2-2.

Subsection 9.1 begins with a summary of what is shown in the Block Diagram; it follows with a description of the Electrical Characteristics of the interface lines, including line transmitters, line receivers and line terminators. Descriptions of functions, logic, timing, and format of the intelligence carried by the signal lines is in subsections 9.2 and 9.3.

#### 9.1.1 BLOCK DIAGRAM

The functional block diagram in Figure 2-3. functionally separates the Kennedy 6170 Disk Drive Unit into the following parts (reading from left to right on the block diagram):

- Controller-Formatter PCB
- SMD Interface PCB
- Read-Write PCB
- Linear Motor Actuator
- Head Carriage Assembly
- Disks
- DC Disk Drive Motor
- Servo PCB

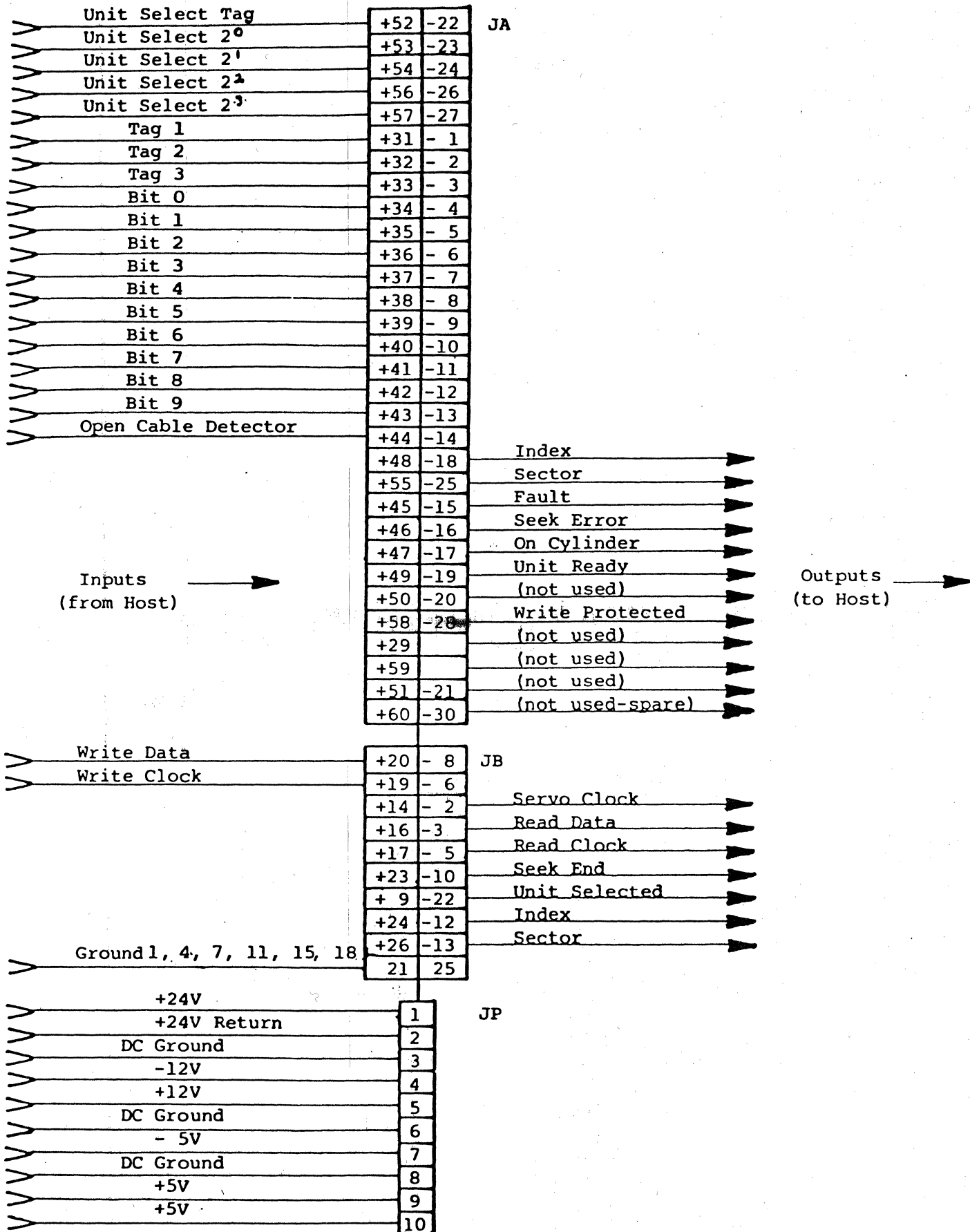


Figure 2-1 SMD Interface

The Controller-Formatter is supplied by the user. It is shown in Figure 2-3 only to give increased meaning to the remaining functional elements, all of which are located in the 6170 Disk Drive Unit.

The SMD Interface Board contains the control logic and timing for executing the principal operations of the disk drive subsystem, which are:

1. Select a Disk Drive Unit - This is done by comparing Unit Select Lines from the Controller-Formatter with the setting of the Unit Address Switch on the SMD I/F PCB and activating the Unit Selected line when they compare. The Unit Selected line is "anded" with the logic on most of the lines between the SMD I/F PCB and the Controller-Formatter PCB. This is symbolically shown using a ganged set of "switches" on Figure 2-3.
2. Seek - The Head Carriage Assembly is positioned at the cylinder where writing or reading is to take place using drive circuitry that is located on the Servo PCB. A head is selected to establish the specific track which is to be written or read, via the Read-Write PCB. Then, the specific sector location where writing or reading is to begin is established by the SMD Interface PCB using Servo pulses which are used to generate read and write clock pulses.
3. Write - Serial binary data from the Controller-Formatter is written into the sectors of a track under control of Index and Sector Pulses from the disk, which are sent to the Controller-Formatter so that they can be synchronized to form "write clock pulses". NRZ bits from the Controller-Formatter are converted to MFM for recording purposes.
4. Read - Data that was written as described above, is readback from the disk and sent to the Controller-Formatter so that it can be acted upon by the host CPU.

Physical connection between the SMD Interface in figure 2-1 and a) other 6170 Disk Drive Units, as well as b) the Controller-Formatter in the host system, is made using two signal cables and one power cable, as described in Paragraph 9.1.2, Cables.

#### 9.1.2 CABLES

The three cables which interface the Kennedy 6170 with an SMD Interface to other Kennedy drives and host system are listed in Table 2-1.



User's  
Controller/  
Formatter

Series Fixed  
Disk Drive  
w/SMD Interface

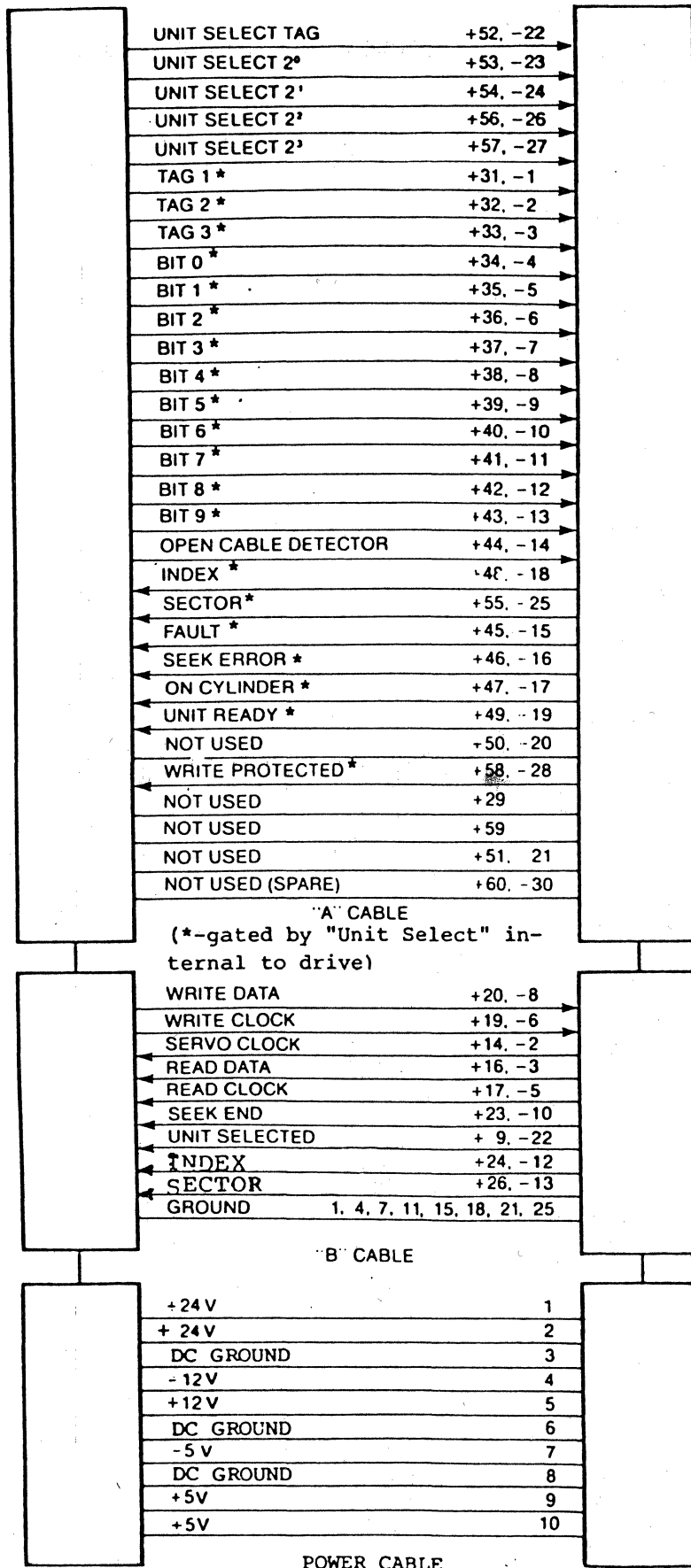


Figure 2-2 Interface Lines - SMD

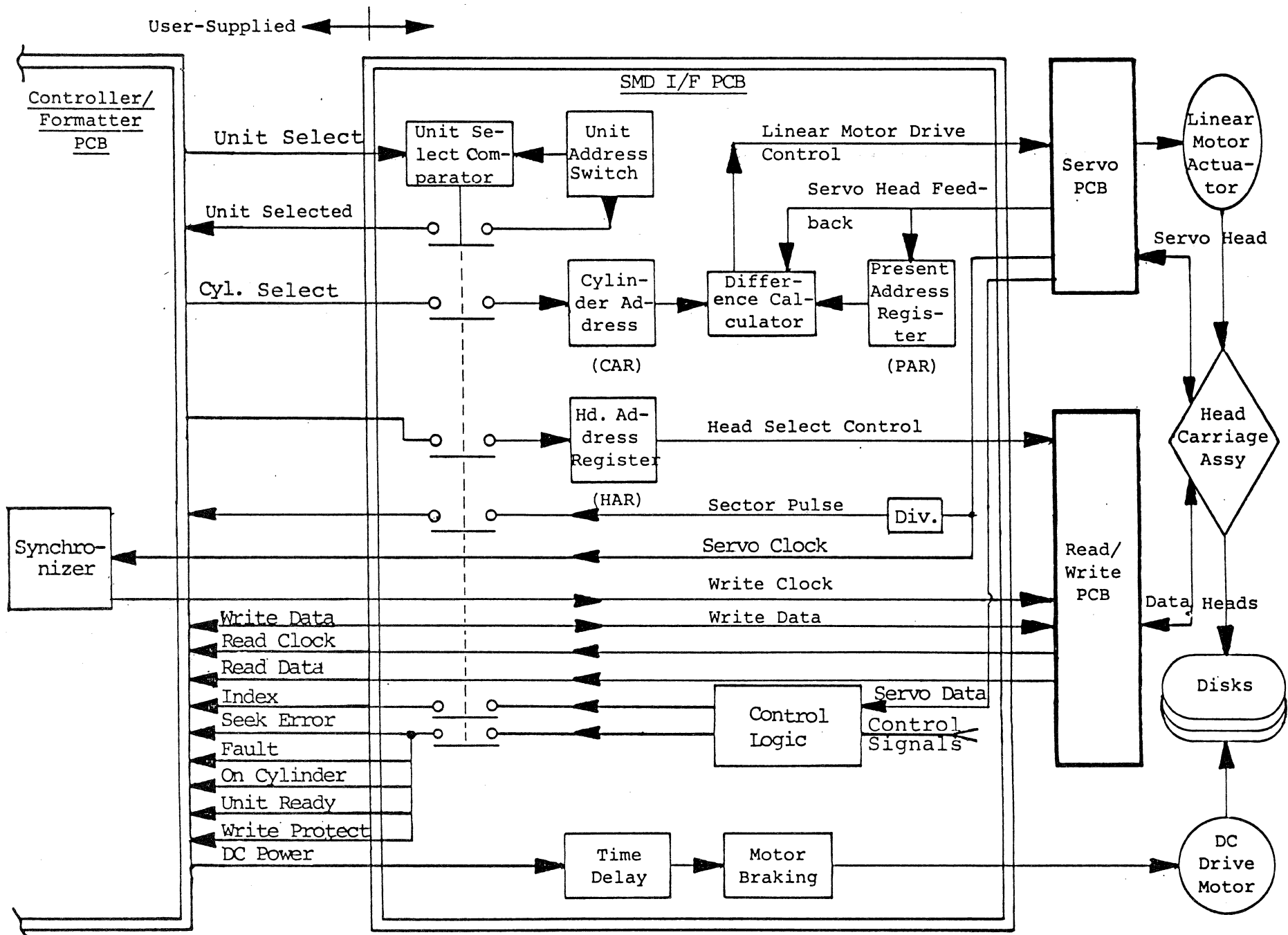


Figure 2-3 Functional Block Diagram -SMD Bus

TABLE 2-1 INTERFACE CABLES

<u>CABLE NAME</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
Signal Cable "A"	60-conductor flat ribbon cable -- maximum of 30 m (100 ft.)	Spectra-Strip 455-248-60
Signal Cable "B"	26-conductor flat ribbon cable -- maximum of 15 m (50 ft.)	Spectra-Strip 455-276-26 or 3M 3476-6
Power Cable	10-conductor, 18-gauge wire -- maximum of 1.2m (4 ft.)	(N/A)

A. Location - The location of each of the above three cables is as shown in Figure 2-4. Marker bands on the ribbon cable are keyed to pin no. 1 of the receptacle on the PCB.

B. Characteristics - The characteristics of the signal cables with part numbers of representative sources is given below. The user supplies his own ribbon cables and ribbon cable connectors.

#### A-Cable

Type:	30 twisted pair, flat cable
Impedance:	105 ohms, nominal
Wire size:	28 AWG, 7 strands, no. 36
Propagation Delay:	1.7 ns per ft., nominal
Maximum Cable Length:	100 ft. (cumulative)
Voltage Rating:	300 V rms
Spectra-Strip Part No.:	455-248-60

#### A-Cable Connector

Positions:	60
Berg Part No.:	65043-007
AMP Part No.:	88376-9



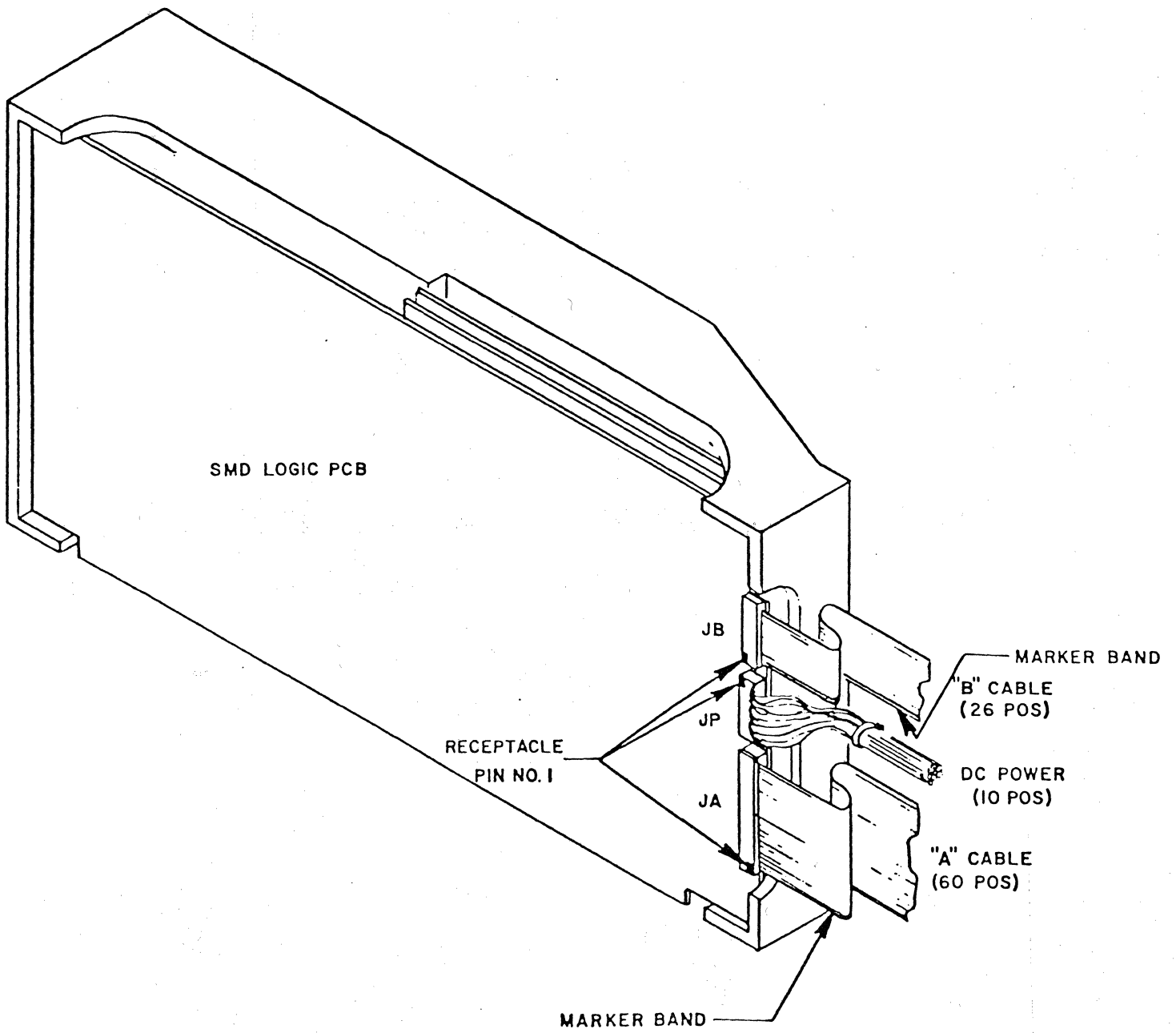


Figure 2-4 Cable Locations

### 9.1.3 RECEIVERS/DRIVERS

All input and output signals are transmitted and received over balanced differential high speed transmission lines using industry standard receivers and drivers, types 75107 and 75110. The transmission system operates in the balanced mode; that is, noise induced on one line is also induced on the other line. The noise appears common-mode at the receiver input terminals, where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit insuring that system performance is isolated from circulating ground currents.

The typical data delay is approximately  $(30 + 1.3L)$  nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and the receiver.

Figures 2-7 and 2-8 show the receiver/driver types that are used with cable A and cable B, respectively. Notes on the two figures describe the exact location of the line terminators; they also summarize wire characteristics and characteristic impedances.

### 9.1.4 TERMINATORS

A. A-Cable - Line terminators (R1 and R2 in Figure 2-7) are located in the Controller-Formatter; they are 56 ohms  $\pm 5\%$  1/10 watt resistors.

Line terminators R3 and R4 in Figure 2-7 are dual-in-line resistor packs which are located in sockets 1A, 3A, 5A and 6A in the SMD interface board. These packs must be unplugged unless the 6170, which contains them, is the last drive on a daisy-chained string of drives.

B. B-Cable - Line terminators (R1 and R2 in Figure 2-8) are located in the Controller-Formatter; Line terminators (R3 or R4) are located in the 6170 drive. These are 82 ohms  $\pm 5\%$  1/10 watt resistors.

### 9.1.5 SIGNAL LEVELS

Typical signal levels are as given below:

Logical 1:	+(High) Signal 0V
	-(Low) Signal - 0.45V
Logical 0:	+(High) Signal - +0.45V
	-(Low) Signal 0V

User's  
Controller-Formatter

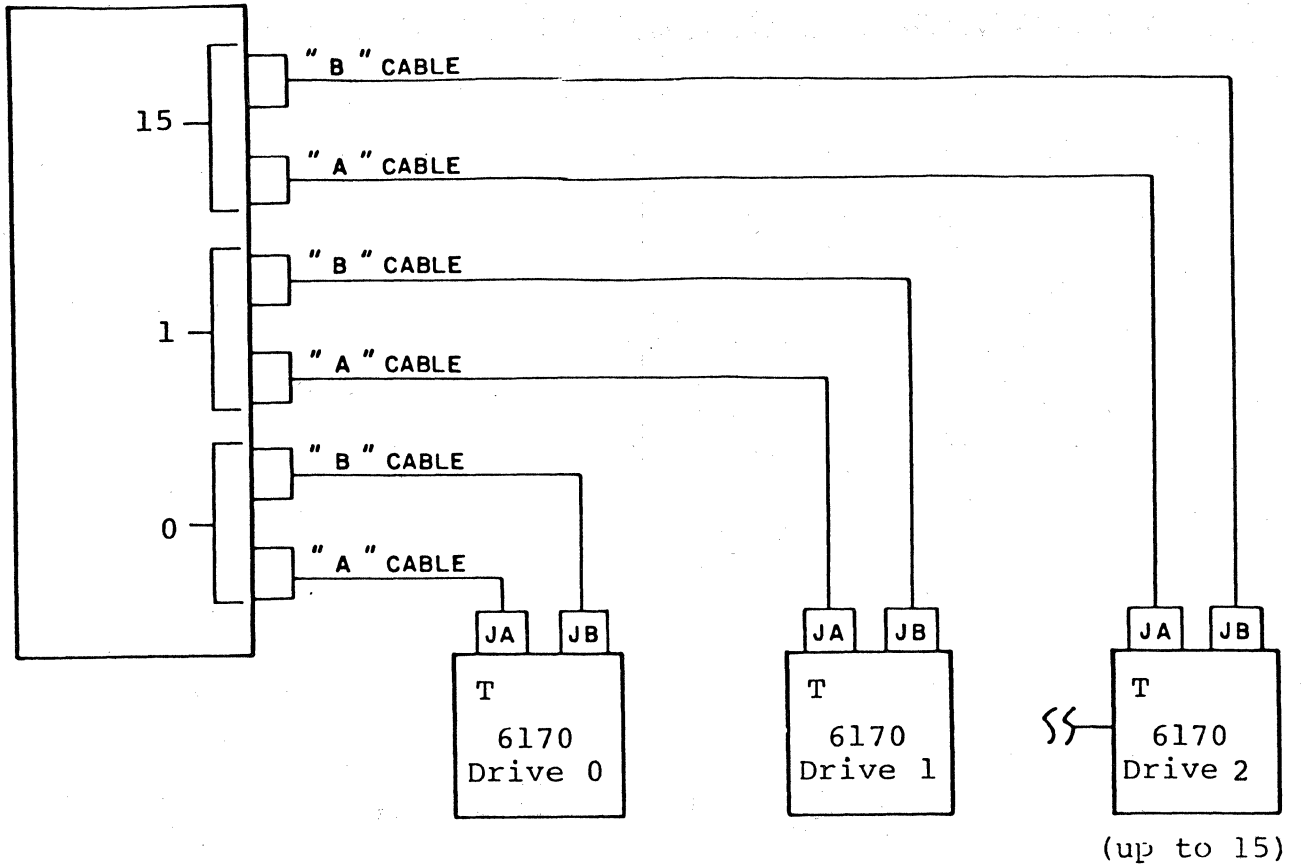


Figure 2-5 Radial (Star) Connection

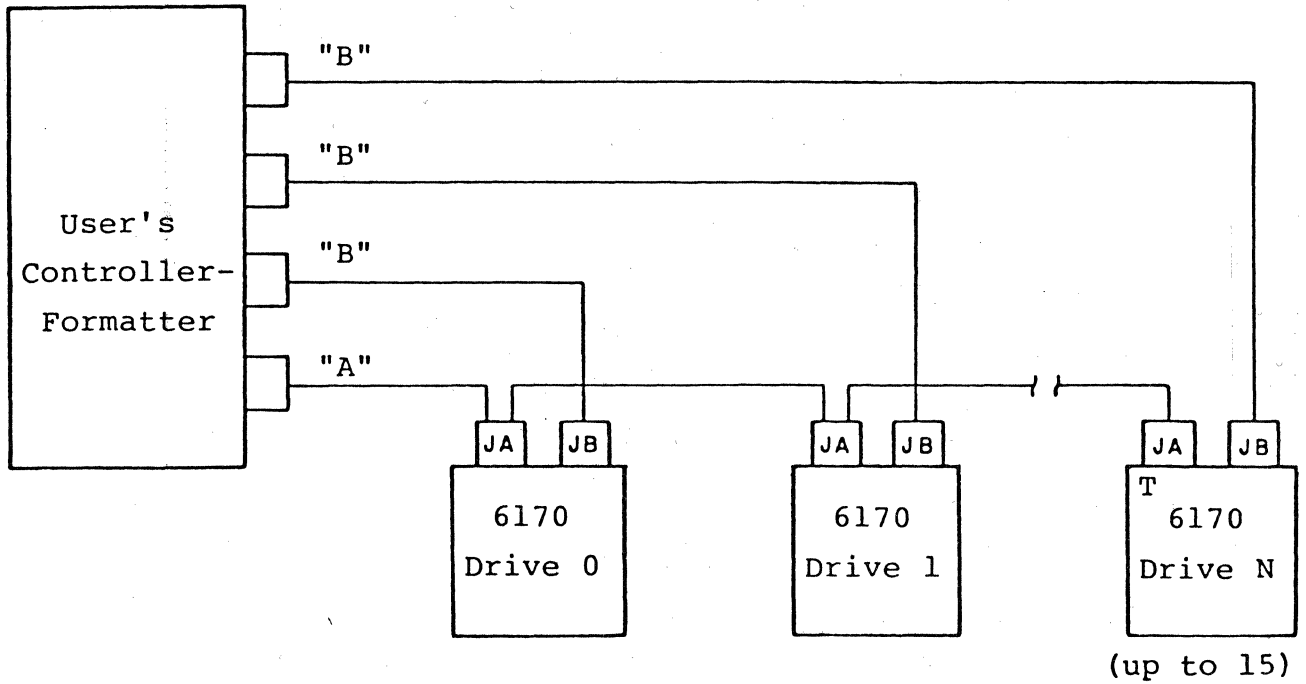


Figure 2-6 Daisy-Chained Connection

NOTE: R1, R2, R3 and R4 are 82 ohms, R5 and R6 are 470 ohms. For line receivers on the BUS cable, located in the disk drive R3 and R4 must be removed in all but the last physical unit on the cable.

#### 9.1.6 SWITCH-SELECTABLE OPTIONS

The SMD Interface Board contains three DIP-switches which are used to select certain interfacing options, as listed below:

Option 1 - Establishes the address of the drive as one of the numbers between 0 and 15 (16 possible "unit address").

Option 2 - Establishes which heads are to be "write protected". The choices are 0-4, depending upon the number of disks/ heads per drive. Note: the servo head is always write protected regardless of the position of the DIP switch.

Option 3 - Establishes sector size with two different amounts of overhead - six different sector sizes per overhead amount are available.

Each of the above three options is described further, below:

A. UNIT ADDRESS SELECTION Table 2-2 shows the effects of the settings of the DIP switch in location 3E. This Dual In-Line Package has four switches which are used to select up to 16 drives.



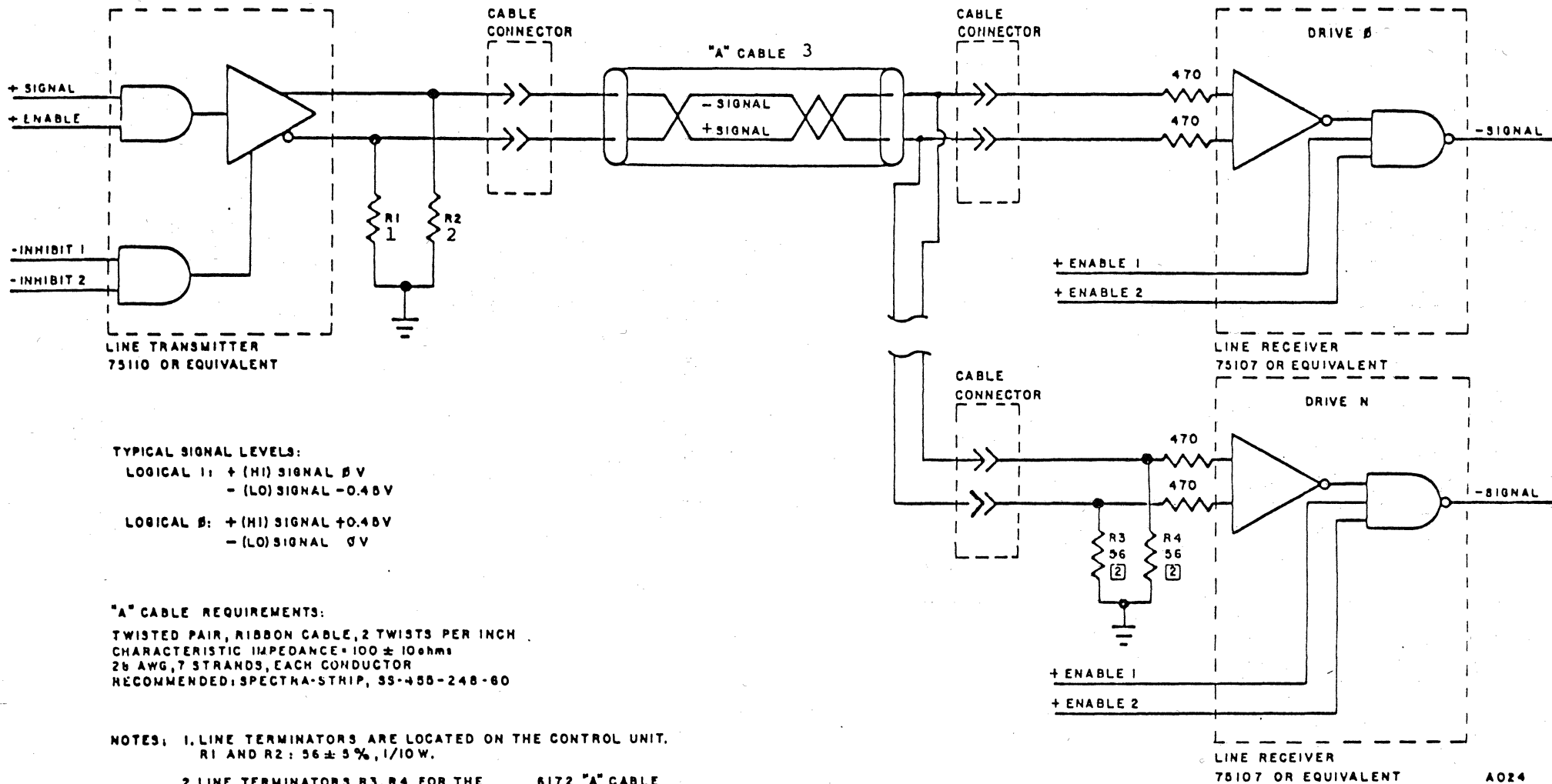
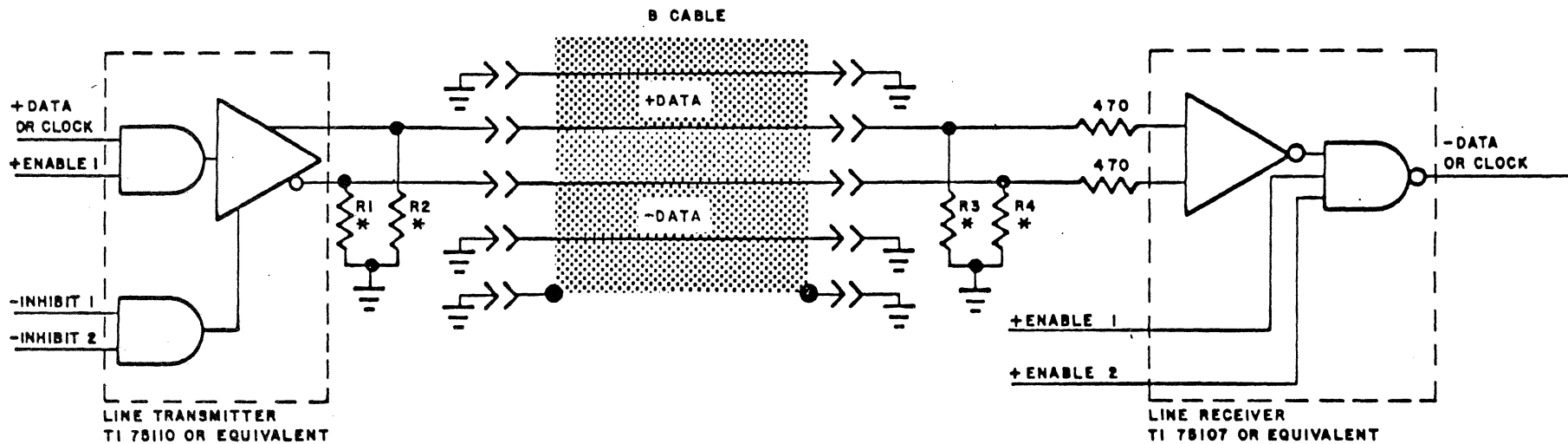


Figure 2-7 Signal Cable "A" Driver/Receiver



**TYPICAL SIGNAL LEVELS:**

LOGICAL 1: + (HI) SIGNAL  $\phi$  V  
 - (LO) SIGNAL -0.45 V

LOGICAL 0: + (HI) SIGNAL  $\pm$ 0.45 V  
 - (LO) SIGNAL  $\phi$  V

**"B" CABLE CHARACTERISTICS:**

FLAT RIBBON CABLE WITH GROUND PLANE AND DRAIN WIRE  
 CHARACTERISTIC IMPEDANCE =  $130 \pm 15$  ohms  
 28 AWG, 7 STRANDS, EACH CONDUCTOR  
 RECOMMENDED: SPECTRA-STRIP, 88-455-276-26  
 3M, 5476-26

\* LINE TERMINATOR RESISTORS LOCATED  
 ON THE DISK DRIVE AND CONTROL UNIT  
 ARE  $82 \Omega$ ,  $\pm 5\%$ , 1/10 WATT.

Maximum Cable Length is 15.1 M (50 ft.)

Figure 2-8 Signal Cable "B" Receiver/Driver

TABLE 2-2 UNIT SELECTION

UNIT SELECT NO.	PHYSICAL UNIT NO.	SW1	SW2	SW3	SW4
0	1	OFF	OFF	OFF	OFF
1	2	ON	OFF	OFF	OFF
2	3	OFF	ON	OFF	OFF
3	4	ON	ON	OFF	OFF
4	5	OFF	OFF	ON	OFF
5	6	ON	OFF	ON	OFF
6	7	OFF	ON	ON	OFF
7	8	ON	ON	ON	OFF
8	9	OFF	OFF	OFF	ON
9	10	ON	OFF	OFF	ON
10	11	OFF	ON	OFF	ON
11	12	ON	ON	OFF	ON
12	13	OFF	OFF	ON	ON
13	14	ON	OFF	ON	ON
14	15	OFF	ON	ON	ON
15	16	ON	ON	ON	ON

NOTE: 'ON' = depress switch on + side; "OFF" = depress switch on blank side.

The address selection may be modified by removing the plastic cap and appropriately depressing the desired rocker-switches using a small blade screw-driver. The switch positions are labeled on the surface of the PCB.

B. HEAD WRITE PROTECTION Table 2-3 shows the switch settings of the 4-switch DIP switch in location 6E. This switch is used to establish which head(s) (i. e., surface(s) is (are) protected from writing. The Servo Head is always protected from writing regardless of DIP switch settings.

TABLE 2-3 HEAD WRITE PROTECTION

HEAD PROTECTED FROM WRITE -----	HD0 SW1 ---	HD1 SW2 ---	HD2 SW3 ---
NONE	OFF	OFF	OFF
HEAD 0	ON	OFF	OFF
HEAD 1	OFF	ON	OFF
HEAD 2	ON	ON	OFF
HEAD 3	OFF	OFF	ON
HEAD 4	ON	OFF	ON
HEADS 0, 1, AND 2	OFF	ON	ON
HEADS 0, 1, 2, 3, AND 4	ON	ON	ON

NOTE: "ON" = Depress + side of switch.

C. SECTOR SIZE SELECTION Table 2-4 shows the switch settings of the 4-switch DIP switch in location 10P. This switch is used to establish:

1. Total number of sectors per track.
2. Resultant data bytes per sector.
3. Overhead bytes per sector.

TABLE 2-4 SECTOR SIZE SELECTION

TOTAL SECTORS/ TRACK	DATA BYTES PER SECTOR	DATA BYTES PER TRACK	SW1	SW2	SW3	SW4
<u>28 Byte Overhead</u>						
84	128	10,752	ON	ON	ON	OFF
46	256	11,676	ON	ON	OFF	ON
24	512	12,288	ON	ON	OFF	OFF
12	1024	12,288	ON	OFF	ON	ON
6	2048	12,288	ON	OFF	ON	OFF
3	4096	12,288	ON	OFF	OFF	ON
<u>44 Byte Overhead</u>						
76	128	9,608	OFF	ON	ON	OFF
44	256	11,264	OFF	ON	OFF	ON
23	512	11,776	OFF	ON	OFF	OFF
6	2048	12,288	OFF	OFF	ON	OFF
3	4096	12,288	OFF	OFF	OFF	ON

NOTE: "ON" = DEPRESS + SIDE OF SWITCH.

#### 9.1.7 SMD EXCEPTIONS

Though the 6170 SMD interface conforms to the functional requirements of the SMD defacto industry standard, differences between 8-inch and 14-inch technology result in the following "exceptions" to specific CDC 9760 SMD specifications:

A. 13,344 bytes per track (unformatted) compared to 20,160 bytes per track on drives with larger diameter disks.

- B. The industry SMD interface for 14-inch drives permits transfer rates up to 9.677 MHz; the Kennedy 6170 system clock is 6.4 MHz.
- C. The industry SMD interface allows an "Address Mark"; the Kennedy 6170 SMD interface does not.
- D. The 6170 has 614 customer-accessible cylinders.
- E. The industry-standard 14-inch SMD drives allow fixed heads; the 6170 with an SMD interface does not.
- F. The Kennedy 6170 SMD interface does not include provision for dual ports; hence, there are no busy, release or priority select "decodes" or bus responses.
- G. The 6170 SMD uses pluggable resistor-packs for termination of the "A" cable.
- H. The Kennedy 6170 SMD does not provide for power-sequencing over the interface bus.
- I. The PLO clock on the 6170 SMD is set at 3.2 MHz. PLO sync-time is 10 microseconds.
- J. The Kennedy 6170 uses three or five data heads, depending upon the model.
- K. Kennedy 6170 SMD I/F Index and Sector pulses have a pulse width of 2.5 microseconds.
- L. The time between the leading edge of "Tag 1" and the trailing edges of "Seek End" or "On Cylinder" is 8 to 10 microseconds (maximum of 15 microseconds).
- M. Following Tag 3, the time between activating "Rezero" and deactivating "Seek End" is 15 to 20 microseconds.
- N. Off-time for "Seek End" is 2.8 milliseconds if track off-set is used.
- O. The drive cannot be selected until the power-up sequence has completed.

## 9.2 SIGNAL LINE FUNCTIONS AND LOGIC

Figure 2-2, earlier in this section, showed the nomenclature for the signals on the lines of the A and B interface cables. This subsection briefly describes the functions that the signals perform and the logic which activates them. The signal lines are described as they are shown in Figure 2-2, from top to bottom. reference is made to timing diagram in subsection 9.3.

NOTE: PARAGRAPHS 9.2.1 THROUGH 9.2.5 COVER INPUT LINES ON THE A-CABLE. PARACRAPHS 9.2.6 THROUGH 9.2.12 COVER OUTPUT LINES.

### 9.2.1 UNIT SELECT TAG

The Unit Select Tag is activated to gate on the "unit select line" in the drive if the unit address comparator finds that the four unit select lines on the interface (2/0, 2/1, 2/2 and 2/3) agree with the unit interface PCB. The Unit Select Switch is further described in Section 9.1.5; unit select timing is shown in Paragraph 9.3.1.

### 9.2.2 UNIT SELECT BUS LINES

The Unit Select Bus Lines contain the binary vaule of the desired unit member; this value is set into the unit address comparator on the rising edge of the Unit Select Tag. Table 2-2, earlier in this section, showed the decoding logic for the Unit Select Switch.

NOTE: ONCE THE COMBINATION OF THE UNIT SELECT TAG, UNIT SELECT BUS LINES AND UNIT SELECT ADDRESS SWITCH CAUSE THE "UNIT SELECT LINE" TO BE ACTIVATED, THE "UNIT SELECT LINE" WILL GATE THE TAG LINES, BUS-BIT LINES AND CONTROL SIGNAL LINES ACTIVE. SEE THE ASTERISKS ON FIGURE 2-2.

### 9.2.3 TAG LINES (TAG 1, 2 AND 3)

The Tag Lines are used in conjunction with Bus Bits 0-9 to establish the command that the selected drive must execute, at what cylinder, and with which head. Tag 1 gates the contents of Bus bits 0-9 into the Cylinder Address Register (CAR); this is the binary value of the desired cylinder (0-613). Tag 2 gates the contents of Bus Bits 0, 1, and 2 into the Head Address Register (HAR); this is the binary value of the desired head (0-4). Tag 3 is a "control select" which indicates the command that should be executed when the cylinder and head of the selected drive are active. The choice of commands are: Write Gate, Read Gate, Servo Offset Forward, Servo Offset Reverse, Fault Clear, Return-to-Zero, Data Strobe Early, and Data Strobe Late. Table 2-5 summarizes the logical relationships between the three Tag Lines. Timing relationships are in Subsection 9.3.

### 9.2.4 BUS LINES (0-9)

The Bus lines perform different functions depending upon the state of the tag lines. As mentioned in Section 9.2.3, they contain the cylinder address at Tag 1 time . . . . the head address at Tag 2 time . . . . and the command to be executed at Tag 3 time. Since the events at Tag 1 and Tag 2 were already described in Paragraph 9.2.3, only the command functions at Tag 3 time are described here.

Bit 0 - Bit 0, in conjunction with Tag 3 enables writing, providing that none of the following conditions exist:

1. Write Protect active.
2. Forward or Reverse Offset in effect.
3. Early or Late Strobe active.
4. Power on Reset (POR).

The write operation is enabled as follows: the index pulse triggers the read gate...the header is read and validated... if the header is the header for the cylinder, head, and sector being sought, the write gate is enabled and writing begins.



TABLE 2-5 TAG AND BUS BITS

TAG BUS	TAG-1 CYLINDER ADDRESS	TAG-2 HEAD SELECT	TAG-3 CONTROL SELECT
Bit 0	CAR 0	HAR 0	Write Enable
1	CAR 1	HAR 1	Read Enable
2	CAR 2	HAR 2	Servo Offset Fwd
3	CAR 3	-	Servo Offset Rev
4	CAR 4	-	Fault Clear
5	CAR 5	-	-
6	CAR 6	-	Return to Zero
7	CAR 7	-	Data Strobe Early
8	CAR 8	-	Data Strobe Late
9	CAR 9	-	-

## BIT 1

Bit 1 in conjunction with Tag 3 enables reading. Read must be enabled in a field that is known to contain zeros and is at least ten microseconds long. The ten microseconds allows time for PLO (Phase-Locked Oscillator) synchronization before the sync character can be read. The data field immediately follows the sync character.

NOTE: Head selection can be changed without deactivating the Read Enable when reading a data field that has not been overwritten since the time the disk was first written. If the data field has been over-written, Read Enable must be deactivated for one microsecond between the header information and reasserted in a field of zeros for at least ten microseconds before valid data can be read.

#### BIT 2

Bit 2 in conjunction with Tag 3 enables offset forward. Offset forward is a 200 u-inch offset of the heads toward the spindle (inward from the nominal "on-cylinder" position). This command is available to the user to enhance the recoverability of "soft" read errors. "Offset" is only permitted during Read operations. See Paragraph 9.3.8.

#### BIT 3

Bit 3 in conjunction with Tag 3 enables offset reverse. Offset reverse is a 200 u-inch offset of the heads away from the spindle (outward from the nominal "on-cylinder" position). This command is also used in the user's retry procedures. "Offset" is only permitted during read operations. See Paragraph 9.3.8.

#### BIT 4

Bit 4 in conjunction with Tag 3 is used to clear a fault. If the condition that caused the fault is still present, the fault signal will again be set when the "fault clear" signal is removed.

#### BIT 6

Bit 6 in conjunction with Tag 3 is used to initiate a Return-to-track 0 regardless of the current cylinder location. If a seek error was being signaled, it would be reset. Cylinder, Head and Present Address Registers would also be reset.

#### BIT 7

Bit 7 in conjunction with Tag 3 is used to data strobe early. Read clock transitions in the read-write circuit are caused to be earlier than nominal by 6 nanoseconds relative to the data window. This can only be done during a read operation. It is used to facilitate read recovery in the user's read-retry procedures.

## BIT 8

Bit 8 in conjunction with Tage 3 is used to data strobe late. When this signal is active, the read clock transitions in the read-write circuit are later than nominal by 6 nanoseconds relative to the data window. This can only be done during a read operation. It is used in conjunction with read-strobe early, in the user's read-retry procedures, to facilitate recovery of soft errors.

## 9.2.5 OPEN CABLE DETECTOR

This is an input signal which becomes active if the A-cable becomes disconnected between the Controller-Formatter in the host and the drive. When the signal is active, the drive is placed in a "power-on-reset" state. This disables all of the line drivers and receivers that are activated by the "unit select signal".

NOTE: Paragraph 9.2.6 through 9.2.12 cover outputs from the interface board to the A-Cable.

## 9.2.6 INDEX

Index is a pulse that is generated from a pattern on the prerecorded servo disk. It is generated once each revolution. Each cylinder is capable of producing an index pulse. The pulse is 2.5 microseconds in duration and occurs every 16.67 milliseconds.

## 9.2.7 SECTOR

Sector pulses are produced to identify individual sectors in a track. Each track contains between 3 and 84 sectors, depending upon the setting of the Sector Size Selection switch on the Interface PCB. The switch setting controls a programmable counter which in turn establishes how frequently a sector pulse will be produced following an index pulse. The Sector Size Selection Switch is also used to select either a 28-byte or a 44-byte sector overhead format, as described in 9.4.

## 9.2.8 FAULT

This line is active (true) to indicate a fault condition which could be any of the following:

1. One of the DC supply voltages is below 10% of nominal.
2. Writing off cylinder
3. Attempting to write on a "write-protected" disk
4. PLD not "locked" during Write
5. Write-gate and read-gate both on at the same time
6. Write current with no Write gate
7. More than one head selected simultaneously
8. Write gate with no write clock transitions

This line may be cleared by Fault Clear (Tag 3 and Bus Bit 4)

#### 9.2.9 SEEK ERROR

This line is active (true) when a seek error has occurred. A seek error will occur as a result of any one of the following:

1. Unable to complete a seek within 800 milliseconds.
2. Heads have been positioned outside of the recordable track area (i.e., into the guard-band area). Note: This forces a power-on reset.
3. An illegal cylinder address has been sent to the drive.

A seek error is assumed to be a soft error; whenever it occurs, retry procedures in the Controller-Formatter must cause the heads to return to track 00 using a Rezero command. This resets the seek error and permits another seek to be initiated, from track 00.

#### 9.2.10 ON CYLINDER

This signal is sent to the Controller-Formatter when the heads are positioned at the desired cylinder. The condition is cleared at the beginning of any new seek and reset at the completion of another successful seek. Any valid "offset" command will result in the loss of "on-cylinder" for 3 msec.

#### 9.2.11 UNIT READY

The unit ready line is true when the drive is selected, disk drive speed is being maintained within tolerances, a successful rezero has been completed, the heads are over valid cylinders, and no fault conditions exist in the drive.

### 9.2.12 WRITE PROTECTED

This line, when true, indicates that the selected head is write protected. If a write operation is initiated on a write protected head, a fault condition is established via the fault line.

NOTE: Paragraphs 9.2.13 and 9.2.14 cover inputs to the interface board from the B-Cable.

### 9.2.13 WRITE DATA

The Write Data line contains serial differential NRZ data from the Controller-Formatter. It is used in conjunction with the write clock line to establish the pattern of information that is written on the disk. Write Data is carried on pins 8 and 20; the line is grounded at pin 7.

### 9.2.14 WRITE CLOCK

The write clock signal which is received at the disk drive from the Controller-Formatter is a retransmitted Servo Clock pulse which was in turn derived from the servo disk. The write clock is synchronized with write data to produce the data patterns which are written on disk. Write clock is carried on pins 6 and 19; ground is obtained at pin 18.

NOTE: Paragraphs 9.2.15 through 9.2.22 cover outputs from the SMD interface board to the Controller-Formatter located in the host system.

### 9.2.15 SERVO CLOCK

The Servo Clock is a 6.4 MHz signal derived from a prerecorded pattern on the servo surface of one of the disks. The signal is 16 times the sync frequency and is used to define bit-cell boundaries during write operations. The signal is sent to the Controller-Formatter which returns it as a "Write Clock". The write clock thus derived will have built-in provisions for variations in disk rotation. The leading edge of the Servo Clock occurs at the center of the data recording window. The servo clock is carried on pins 2 and 14; ground is obtained at pin 1.

#### 9.2.16 READ DATA

This signal line contains data that has been read from disk by the selected head. The data is synchronized such that the leading edge of the read clock is coincident with the center of the data bit. Read Data is carried on pins 3 and 16; ground is obtained at pin 15.

#### 9.2.17 READ CLOCK

The Read Clock is generated from the data that is read from the disk. The raw data, in conjunction with the Phase-locked oscillator (PLO), is used to establish the bit-cell window. The clock pulse is established at the center of the window. Read clock is carried on pin 5 and 17; ground is obtained at pin 4.

#### 9.2.18 SEEK END

The Seek End signal is sent back to the Controller-Formatter to indicate the end of a Seek, Rezero, or Offset Operation. The signal goes false (inactive) at the beginning of a seek, rezero or offset command. Seek End is carried, on pins 10 and 23.

#### 9.2.19 UNIT SELECTED

The Unit Selected line is active (true) when the Unit Select lines at the A-Cable portion of the interface bus compare with the unit address that has been set into the unit address DIP switch on the SMD interface board, and the Unit Select Tag is present. The Unit Selected line activates all status outputs to the A-Cable; it also enables inputs from the Controller-Formatter. Unit Selected is carried on pins 22 and 9; ground is obtained at pin 21.

#### 9.2.20 INDEX

An alternate Index pulse is sent out on the B-Cable since in daisy-chained operations, Index may not always be available via A-Cable (it is gated with Unit Select when it comes via the A-Cable). The B-Cable is always radially-connected. The Index pulse on the B-Cable, like the Index pulse on the A-Cable, is generated once each revolution from a pattern on the prerecorded servo disk. The pulse is carried on pins 12 and 24; ground is obtained at pins 13 and 26.

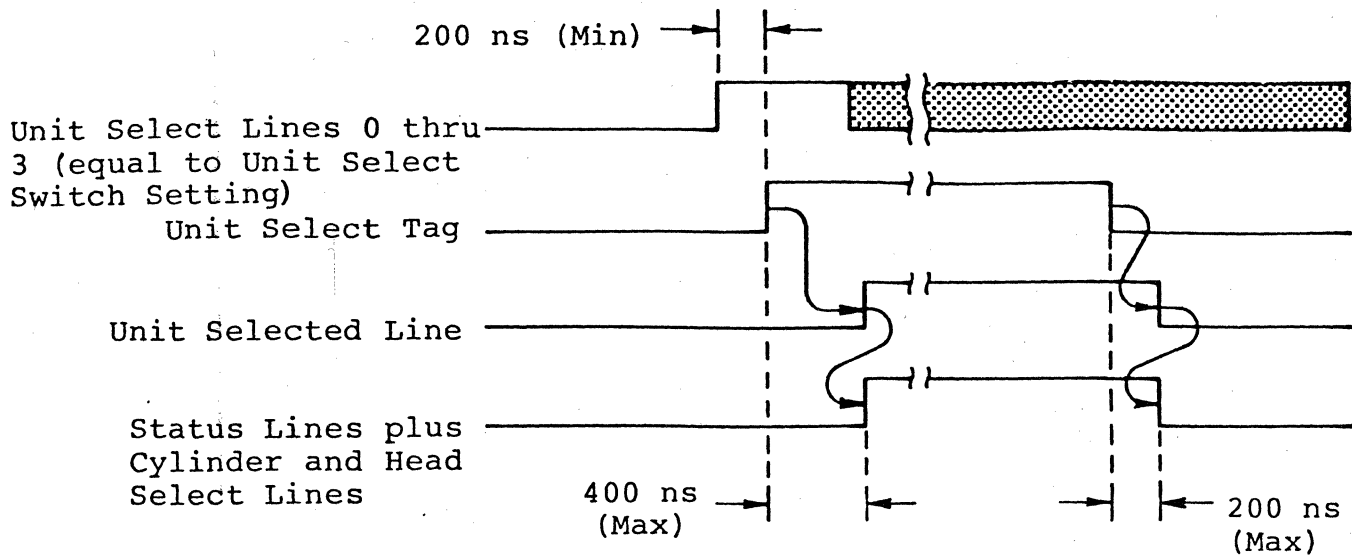


Figure 2-9 Unit Select Timing

### 9.2.21 SECTOR

An alternate Sector pulse is sent out on the B-Cable since in daisy-chained operation, the Sector pulse may not always be available via the A-Cable (it is gated with Unit Select when it comes via the A-Cable). The B-Cable is always radially connected. Sector pulses are produced by a combination of a programmable counter and the sector-size selection switch.

### 9.2.22 GROUND

Ground is DC-ground from the user-supplied power supply.

## 9.3 SIGNAL LINE TIMING

This subsection contains timing relationships between the signals and logic described in Subsection 9.2. Cross-reference is made to specific paragraphs of Subsection 9.2.

### 9.3.1 UNIT SELECT

Figure 2-9 shows the timing relationships between the Unit Select Tag, the Unit Select Address Switch, the Unit Selected Line and the various Status Lines. Reference can be made to Paragraphs 9.2.1, 9.2.2 and 9.2.19. In summary, when the Unit Select Tag is active and the state of the Unit Select Lines equal the state of the Unit Address Switch, the Unit Selected Line is activated on the rising edge of the TAG. With the Unit Selected line active the various Status Lines, plus the Cylinder and Head-Select Lines also become active. A 200 nano-second stabilization time must be allowed for changes in the state of signals, resulting in the switching times that are shown in Figure 2-9.

### 9.3.2 SEEK

Figure 2-10 shows the timing relationships during a "Seek" command. The first thing to happen is the Bus Bits being set to the address of the desired cylinder by the Controller-Formatter. Then, when Tag 1 comes true, provided 200 ns has been allowed for the Bus bit lines to settle, the Cylinder Address Register (CAR) is set to the state of the Bus Bits. The "On Cylinder" and "Seek End" lines go false; this begins a Seek operation. When Tag 2 is received (a minimum of 400 ns later) the low-order contents of the Bus Bits are set into HAR. This causes the desired head to be selected during the next 200 ns. The positioning action of the Seek command now begins.



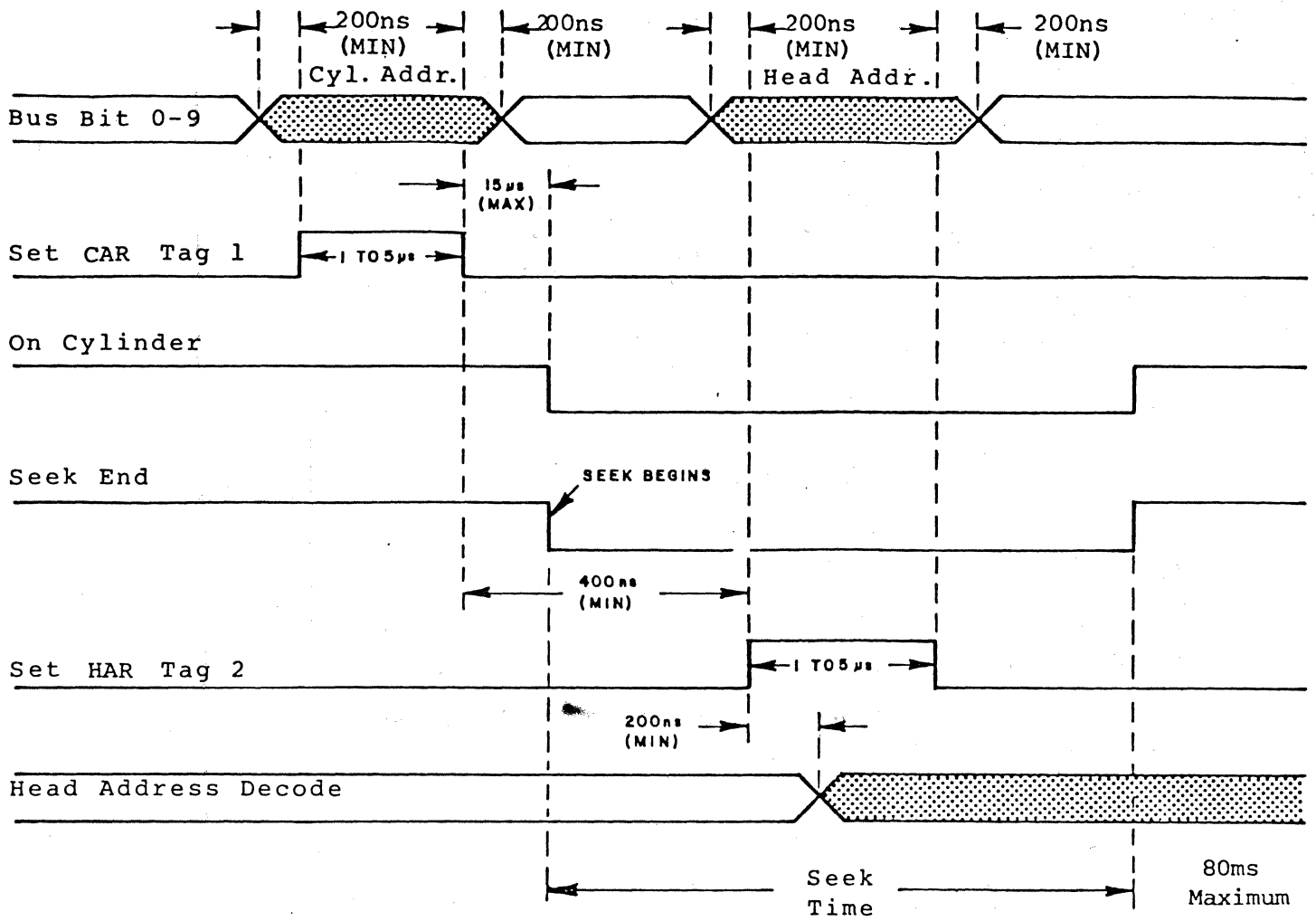


Figure 2-10 Seek Timing

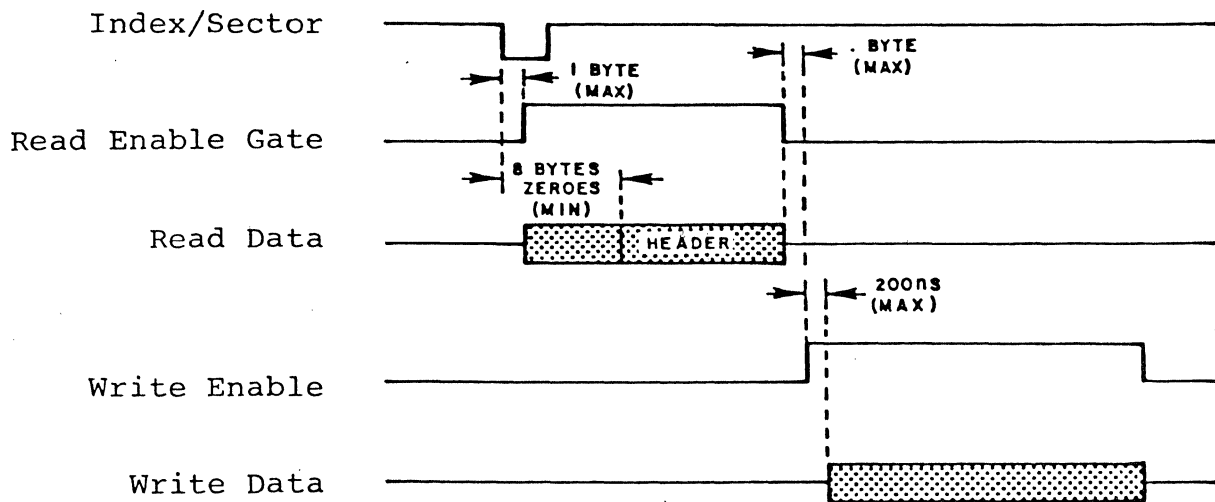


Figure 2-11 Write Enable Timing

NOTE: The Tag 1 and Tag 2 signal lines were used to set in a cylinder address and select a head. If the cylinder or head that was set in turned out to be different from the one that was currently active, a seek to the new cylinder and head began at that time.

Tag 3 is the "control tag". It controls which operation the drive is caused to perform after a seek has been completed. When Tag 3 comes true (controlled by the Controller-Formatter), the drive unit executes a command as determined by the state of the Bus Bits. Reference may be made back to Table 2-5 and the line descriptions which follow it. The descriptions which follow are oriented to the operations which result from specific Bus bit settings at Tag 3 time.

### 9.3.3 WRITE

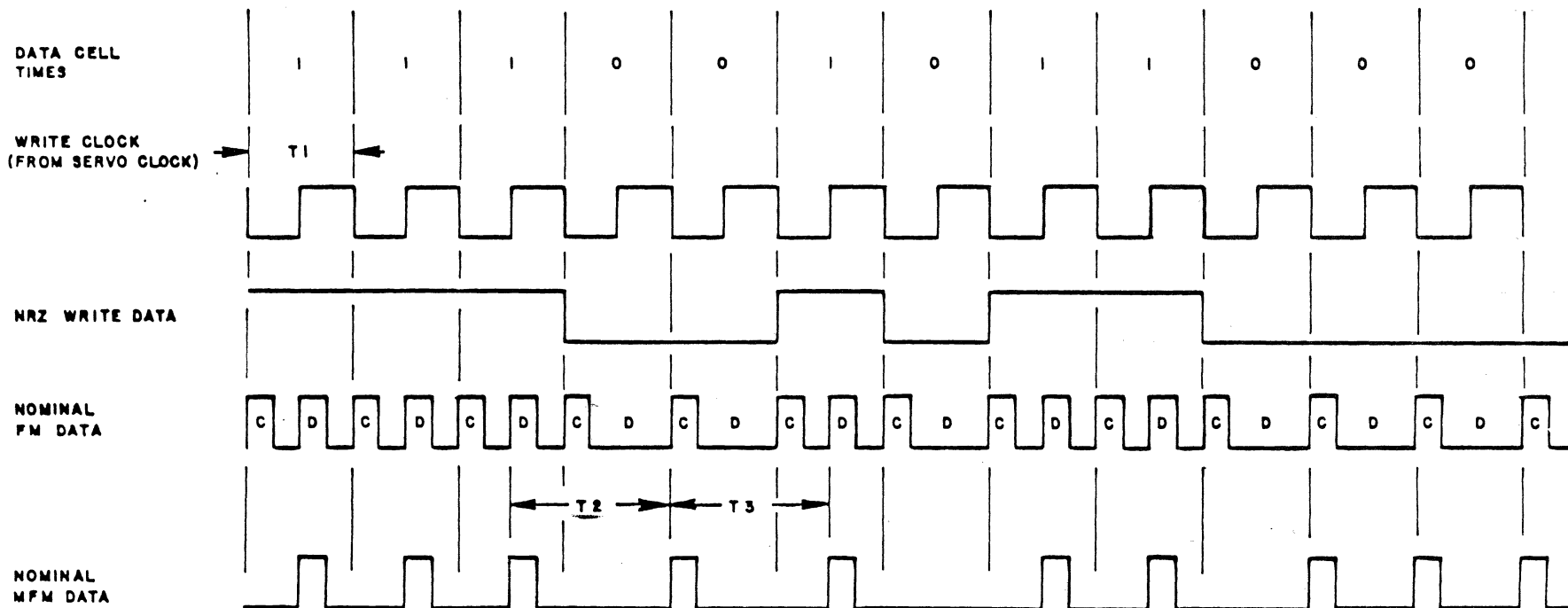
A write operation is begun if Bus Bit 0 is true at Tag 3 time and the following additional conditions exist:

1. No Write Protect
2. No Forward or Reverse Offset
3. No Early or Late Data Strobe
4. No Power-On Reset

Before write is enabled, a search is made to find the desired sector in the track where writing is to begin. The Index pulse and successive Sector Pulses each trigger the Read Enable line as shown in Figure 2-11, Write Enable Timing. Successive Headers are read until the correct header is found, at that time, the Write Enable gate comes true and data is allowed to be written.

The header must be preceded by at least 8-bytes of zeroes to allow time for VFO lock-up before reading the "sync" character which is located at the end of the field of zeroes. The zeroes, sync character and header are supplied by the Controller-Formatter.

Read Enable is activated within one byte time of the leading edge of the Index Pulse. The "read data" which is the header is sent to the Controller-Formatter for comparison. If the header is for the desired sector, Write-Enable is activated in less than one byte-time.



$T_1$  = DATA CELL PERIOD = 156 Nsec

$T_2$  = ONE TO ZERO = 234 Nsec

$T_3$  = ZERO TO ONE = 234 Nsec

Figure 2-12 Write Data Timing

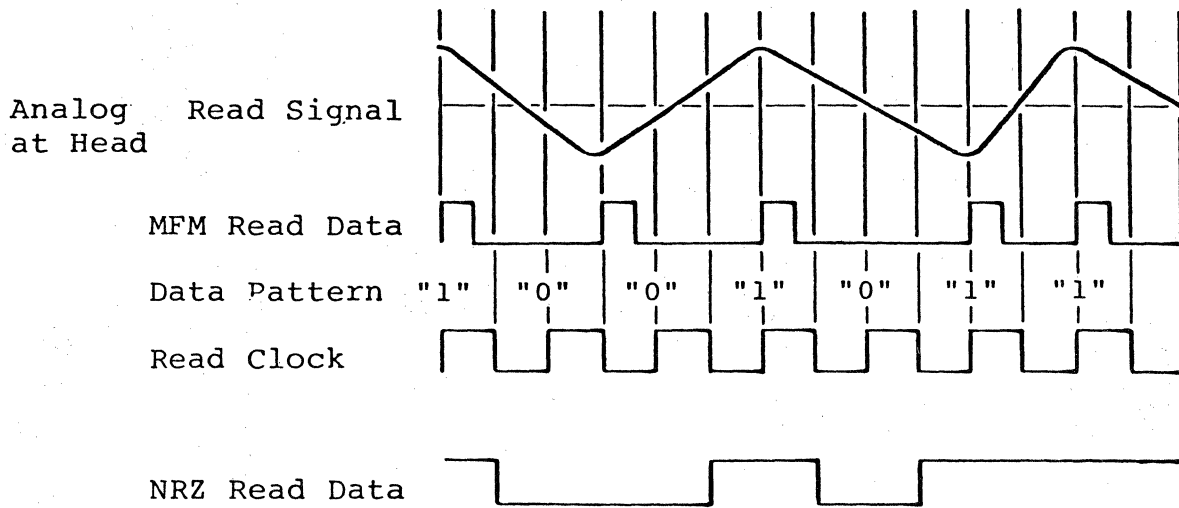


Figure 2-13 Read Data Timing

Figure 2-12 shows the conversion of NRZ data from the Controller-Formatter to MFM. Straight FM is shown for comparison purposes. The top line in Figure 2-12 shows bit-cell times and the value of the bit within each cell. The second line shows write clock pulses which are sent from the Controller-Formatter to the drive (these are generated from the servo clock pulses which the disk drive unit sends to the Controller). The NRZ write data on the third line is in one state for binary 1 and the opposite state for a binary 0. An FM signal would have more flux followed by the presence (1) or absence (0) of a data pulse. When FM is modified to produce MFM, the need for a clock pulse at the beginning of each data cell, is eliminated.

A convention is adopted wherein binary 1's always have a flux transition in the center of a cell. There is no flux transition in the data cell of a binary zero which was either preceded by or followed by, a binary one. There is a flux transition (at the beginning of the data cell) in the data cell of adjoining binary zeroes.

The write signal will magnetize the surface of the disk in one direction or the other. The points of transition from one direction of magnetization to the other will have bit significance.

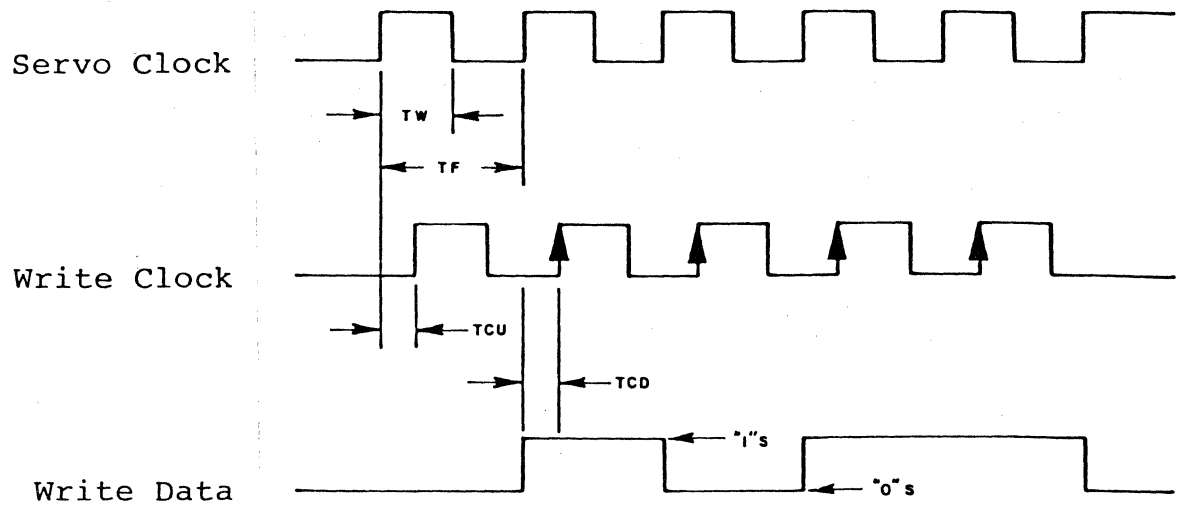
The header must be preceded by at least 8-bytes of zeroes to allow time for VFO lock-up before reading the "sync" character which is located at the end of the field of zeroes. The zeroes, sync character and header are supplied by the Controller-Formatter.

Read Enable is activated within one byte time of the leading edge of the Index Pulse. The "read data" which is the header is sent to the Controller-Formatter for comparison. If the header is for desired sector, Write Enable is activated in less than one byte-time.

#### 9.3.4 READ

A read operation is begun if bus Bit 1 is true at Tag 3 time. This was shown in Figure 2-11, Write Enable Timing. Read Enable is gated by no power-on reset in process. In a read operation, however, Read Enable stays true and Write Enable stays false. "Data" is then read from the sector which follows. The data that is read is as shown on the top line of Figure 2-13

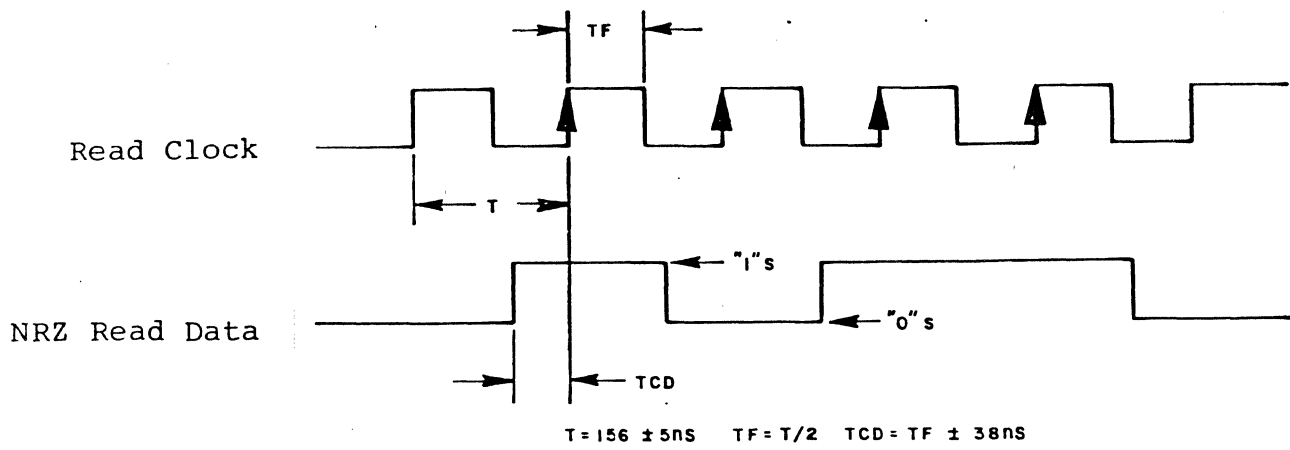
The analog data thus read and amplified is "squared" to the MFM signal which is shown on the second line of Figure 2-13. This is then converted to the NRZ signal which is familiar to the Controller-Formatter.



**TF** =  $156 \text{ ns} \pm 5.0 \text{ ns}$   
**TW** =  $TF/2 = 78.0 \text{ ns}$   
**TCU** = INTERFACE CABLE DELAY  
**TCD** =  $TW \pm 38 \text{ ns}$

- NOTES:
1. WRITE DATA AND DATA CLOCK TIMING SHALL BE SPECIFIED AT THE OUTPUT CONNECTOR OF THE CONTROL UNIT.
  2. THE PERMISSIBLE VALUE OF TF IS  $156 \pm 5 \text{ ns}$  (APPROX.  $\pm 3\%$ ), WHICH INCLUDES THE ROTATIONAL SPEED TOLERANCE.
  3. DIFFERENTIAL NRZ WRITE DATA ISSUED FROM THE CONTROL UNIT IS WRITE-COMPENSATED AND THEN MFM-MODULATED FOR WRITING ON THE DISK SURFACE.

Figure 2-14 Write Clock Generation



- NOTES:
1. READ CLOCK AND READ DATA TIMING SHALL BE SPECIFIED AT THE OUTPUT CONNECTOR OF THE DISK UNIT.
  2. READ DATA SIGNAL SHOULD BE CLOCKED AT THE POSITIVE-GOING EDGE OF DIFFERENTIAL READ CLOCK ON THE CONTROL UNIT.

Figure 2-15 Read Clock Generation

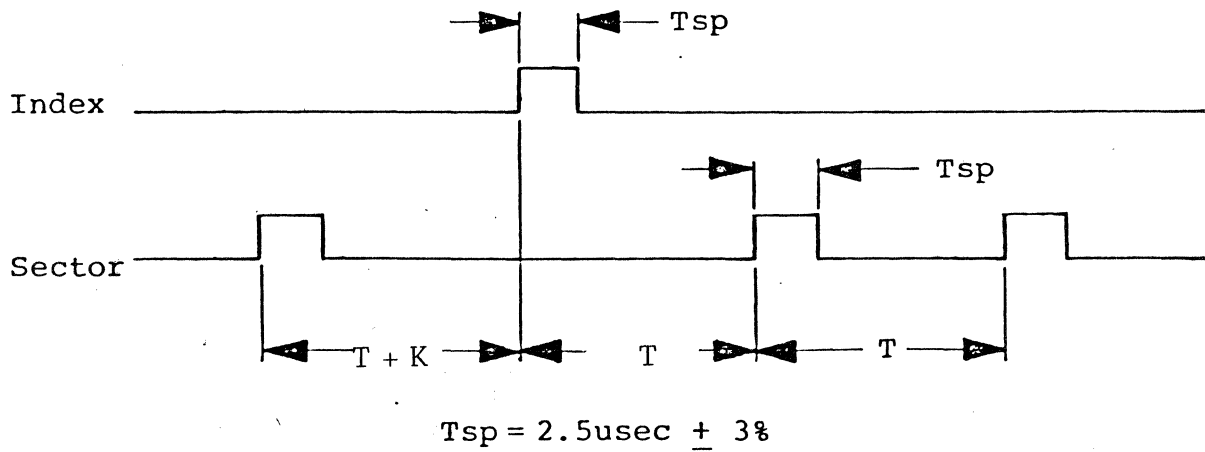


Figure 2-16 Index-to-Sector-Pulse Timing



### 9.3.5 WRITE CLOCK GENERATION

The timing relationships between the Servo Clock (from the disk to the controller) and the Write Clock (from the Controller to the Disk) are as shown in Figure 2-14. As stated in no. 2 of notes, these timings are at the output connector of the control unit.

### 9.3.6 READ CLOCK GENERATION

The timing relationship between the read clock and the NRZ data signal which is derived from data that was read, is as shown in Figure 2-15.

### 9.3.7 INDEX-TO-SECTOR-PULSE TIMING

Index-to-sector pulse timing is as shown in Figure 2-16. The Index and Sector pulses have a 2.5 usec  $\pm 3\%$  duration.

Each sector is of length "T"; however the time between the leading edge of the last sector pulse and the leading edge of Index is "T+K".

"T" is equal to the number of bytes per sector multiplied by 1.249 microseconds.

### 9.3.8 OFFSET TIMING

An Offset Operation is begun if Bus Bits 2 or 3 are true at Tag 3 time. The heads are offset from the selected cylinder by 200 u inch as long as Tag 3 and Bus Bits 2 or 3 remain active. "On Cylinder" and "Seek End" are de-activated for 3 milliseconds. When Tag 3 and Bus Bits 2 or 3 are de-activated, the servo returns to its normal "on-track" position. The Controller must wait until this occurs (approximately 10 ms) prior to issuing any further commands. See Figure 2-17. Note: Bus Bit 2 causes offset toward the inner diameter of the disk (Forward Offset); Bus Bit 3 causes offset toward the outer diameter of the disk (Reverse Offset).

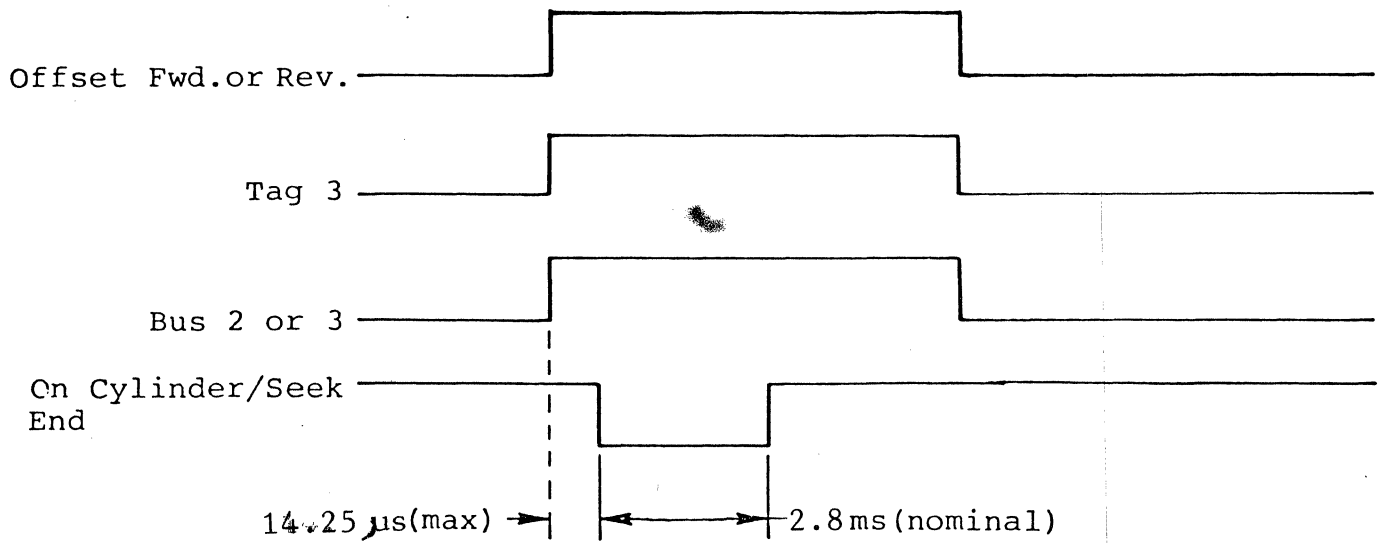


Figure 2-17 Offset Timing

### 9.3.9 FAULT RESET

A "Fault Reset" operation begins if Bus Bit 4 is true at Tag 3 time. The result of a "Fault Reset" is the resetting of the Fault Line which the drive sends to the Controller-Formatter. If the condition which caused the "fault" is no longer present, the "fault" output remains reset; if the condition still exists, the "fault" line will become active again as soon as the fault reset conditions are removed. Tag 3 is active for minimum of 400 ns. It takes up to 8.5 microseconds to reset the Fault Line. See Figure 2-18.

### 9.3.10 RETURN-TO-ZERO

Return-to-Zero is an operation in which the head-carriage assembly is repositioned to Cylinder 0, independent of its present position. It occurs when Bus Bit 6 is true at Tag 3 time. If a seek error was being signaled, the Seek Error would be reset. Cylinder, Head, and Present Address Registers would also be reset. Figure 2-19 shows Return-to-zero timing following a seek error.

### 9.3.11 ZERO TRACK SEEK

Figure 2-10 showed over-all seek timing; Figure 2-19 showed "return-to-zero" timing. Figure 2-20, below, shows a seek to the same cylinder as where the heads are currently located.

## 9.4 SECTOR FORMATS

Two different types of format are available on the SMD Interface PCB. One type includes a 28-byte overhead; the other type includes a 44-byte overhead. The user can select either one of the two formats using the Sector Size Selection Switch in the SMD Interface Board. Table 2-4, earlier in this section, describes the effect of the two different overhead amounts on a) the number of sectors per track, b) the number of bytes per sector, and c) the number of bytes per track. The overhead size that the user selects will depend on the speed of the switching circuitry in the Controller-Formatter and in the other elements of the host system. Systems which include high speed circuitry can use the 28-byte overhead format; slower systems can opt for the 44-byte overhead format.

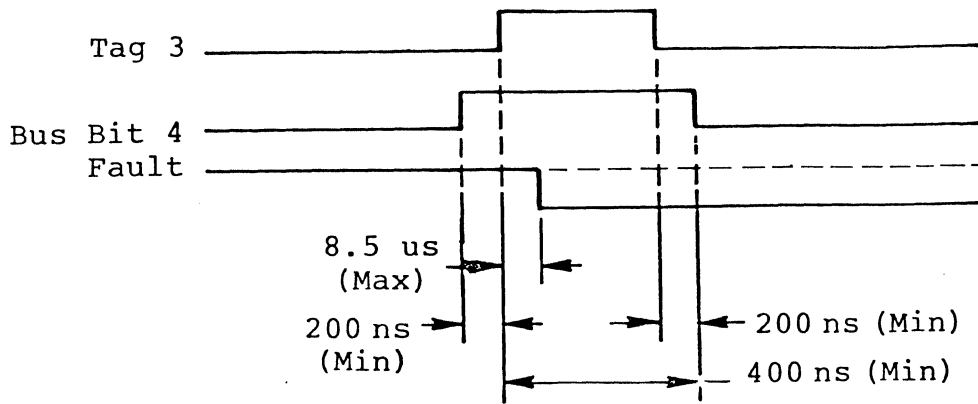
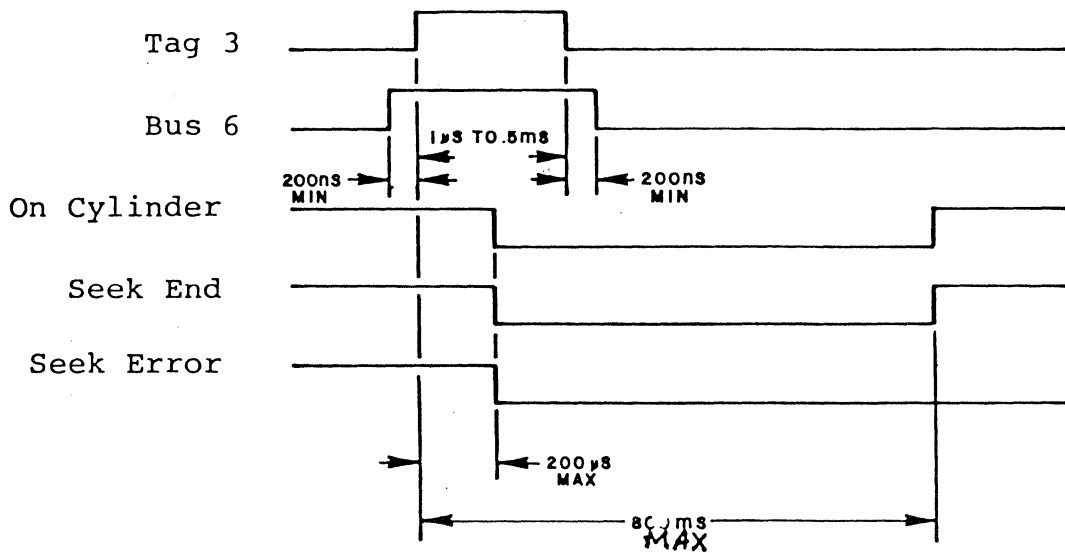


Figure 2-18 Fault Reset



Note: On Cylinder is not always set at Seek Error

Figure 2-19 Return-To-Zero Timing Following a Seek Error

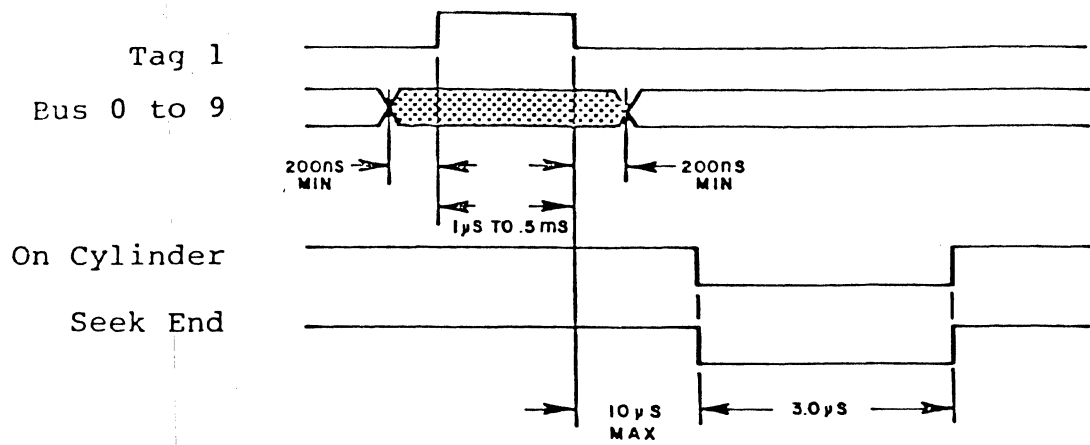
#### 9.4.1 28-BYTE OVERHEAD FORMAT

The sector format with 28-bytes of overhead is shown in Figure 2-21. Quick review of Figure 2-21 will show that a sector consists of two basic fields: a "header" field and a "data" field. Both the header and the data fields are preceded by a "sync" field and followed by a "read-write splice".

The "sync" field consists of eight bytes of zeroes which are needed to synchronize the phase-locked oscillator (PLO) in the read-write circuitry. The PLO must be "locked-up" prior to encountering the Sync Character. The Sync Character is "Hex 19". It serves as a "flag" that signals the beginning of the header that is about to be encountered.

The "header" consists of a two-byte cylinder address, a one-byte head address, a one byte sector address, and two bytes to be used for a check character. The check character could be a parity check...a cyclic redundancy check (CRC)...or an error detect/correct code of the Hamming or Fire-Code type. The user has the option of choosing and implementing the error detection and correction system. The "apparent" data rate will significantly improve if an error-correction system is implemented as opposed to a simple error-detection system. The data error rates given in Section 2 assume that a minimum, a CRC checking system is used.

The header field is followed by a read-write "splice". The splice is a one-byte area which allows for the electronics to "switch" when making the transition from read to write during a Write operation. Next (referring to Figure 2-21) the sync field which precedes the data field is encountered. It is the same as the sync field which preceded the header field and it serves the same purpose. The data field may contain from 128 to 4096 bytes of data; the number of bytes of data in a sector is determined by the setting of the Sector-Size-Selection switch on the SMD Interface PCB, as shown earlier in Table 2-4



Frigure 2-20 Zero Track Seek

SYNC FIELD		HEADER FIELD				SPLICE
PLO SYNC	SYNC CHARACTER	CYLINDER ADDRESS	HEAD ADDRESS	SECTOR ADDRESS	CRC	READ/WRITE SPLICE
S1	S2	HI-2	H3	H4		SPI
8 BYTES	1 BYTE	2 BYTES	1 BYTE	1 BYTE	2 BYTES	1 BYTE

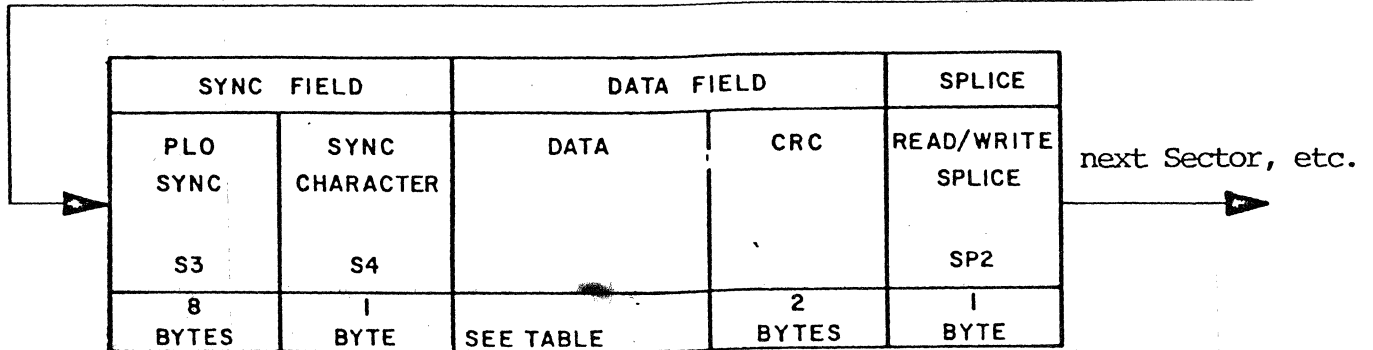


Figure 2-21 Sector Format With 28-Byte Overhead

#### 9.4.2 44-BYTE OVERHEAD FORMAT

The number of sectors per track, the number of data bytes per sector, and the number of data bytes per track for the 44-byte overhead was shown earlier in this section in Table 2-4. Figure 2-22, below, shows the relationship of overhead to data in the 44-byte format.

This is suggested format only; the choice of elements is with the user. An explanation of the various elements of the overhead and data follows the figure.

Each sector contains a Beginning of Record (BOR) and an End of Record (EOR) field to add to the time between sectors when reading. It is suggested that  $m$  (the number of bytes in BOR) and  $n$  (the number of bytes in EOR) total to equal 9. The contents of the BOR and EOR are the user's choice. The PLO sync field must be zeroes.

Actually, only 8 bytes of zeroes are needed by the PLO; eleven are suggested in this format.

The header field is the same as in the 28-byte overhead format, above, with one exception. A byte is added to the header to be used as desired by the user. It could contain a flag bit to indicate unit status to the host; or, it could be used to indicate the unit's I.D. no. to the host operating system. The remaining elements of the overhead are as described in the 28-byte format, above. There is a 2-byte cylinder address, a 1-byte head address, a 1-byte sector address and room for a 2-byte check/correct character. An error correcting system, including a Hamming/Fire-code-character, is recommended.

A one-byte read-write "splice" separates the header field from the sync field for the data field. The number of bytes in the data field is established by the Sector Size Selection switch as shown in Table 2-4. It is between 128 and 4096 bytes, depending upon the setting of the four-switch assembly.

In summary, there must be at least 8 bytes of zeroes preceding the header to insure synchronization of the PLO; in addition, there must be a 1-byte gap or splice between sectors.



BOR	SYNC FIELD		HEADER FIELD				
BEGINNING OF RECORD	PLO SYNC	SYNC CHARACTER	FLAG AND UNIT	CYLINDER ADDRESS	HEAD ADDRESS	SECTOR ADDRESS	CRC
	S1	S2	H1	H2-H3	H4	H5	CRC 1
(m) BYTES	11 BYTES	1 BYTE	1 BYTE	2 BYTES	1 BYTE	1 BYTE	2 BYTES

SPLICE	SYNC FIELD		DATA FIELD		SPLICE	EOR
READ/WRITE SPLICE	PLO SYNC	SYNC CHARACTER	DATA	CRC	READ/WRITE SPLICE	END OF RECORD EOR
SP1	S3	S4		CRC 2	SP2	
1 BYTE	11 BYTES	1 BYTE	SEE TABLE	2 BYTES	1 BYTE	(n) BYTES

next Sector

Figure 2-22 Sector Format With 44-Byte Overhead

## 9.5 POWER LINES

DC power for operating the drive is furnished by the user. One DC power cable must be fabricated for each drive. Figure 2-23 shows the voltages or grounds expected at the pin numbers of Jack JP on the SMD Interface PCB. Note the "caution" on Figure 2-23 regarding the user's choice of frame ground versus DC ground.

## POWER CONNECTOR JP

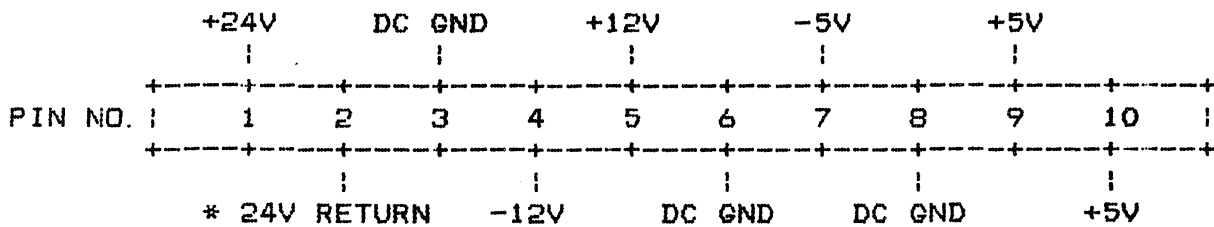


Figure 2-23 Power Lines

**\*CAUTION** Frame Ground is jumpered to DC Ground at the factory. If separate Frame Ground is required, remove the jumper between the pads marked "Frame Ground" and "DC Ground" on the component side of the logic PCB next to the power connector.

## 10 "DISK BUS" DISK DRIVE INTERFACE

This specification describes the interface between 1) the Disk Bus Interface PCB on the Disk Drive Unit which is described in Section 1 of this specification and 2) a Controller-Formatter which is part of the host system and designed to control a drive which has a "Disk Bus" Interface.

### 10.1 PHYSICAL AND ELECTRICAL INTERFACE DEFINITION

The "Interface" is defined as the signal lines and power lines that must be connected to jacks JB and JP on the Disk Bus PCB in order for the Kennedy 6170 to function as described in Section 1. JB is the receptacle for a 40-conductor ribbon cable; JP is the receptacle for a 10-wire power cable. The "interface" has a variety of characteristics such as: physical properties, electrical properties, timing, logical interrelationships, and formatting considerations. All of these are included in the term "interface" and are described in this specification in the term "interface" and are described in this specification in terms of what can be seen at individual pins of JB which are collectively called the Disk Bus Interface. The Disk Bus Interface is shown in Figure 3-1.

A cable diagram showing how the interface bus relates to the 40-pin signal cable and the 10-pin power cable is given in Figure 3-2, Interface Cables.

Figure 3-3 is a functional block diagram of the disk drive subsystem which uses the interface lines shown in Figure 3-2.

Subsection 10.1 begins with a summary of what is shown in the block diagram; it follows with a description of the electrical characteristics of the interface lines, including line transmitters, line receivers and line terminators. Descriptions of functions, logic, timing, and format of the intelligence carried by the signal lines are in Subsections 6.2 and 6.3.

#### 10.1.1 BLOCK DIAGRAM

The block diagram in Figure 3-3 functionally separates the Kennedy 6170 Disk Drive Unit into the following parts (reading from left to right on the block diagram):

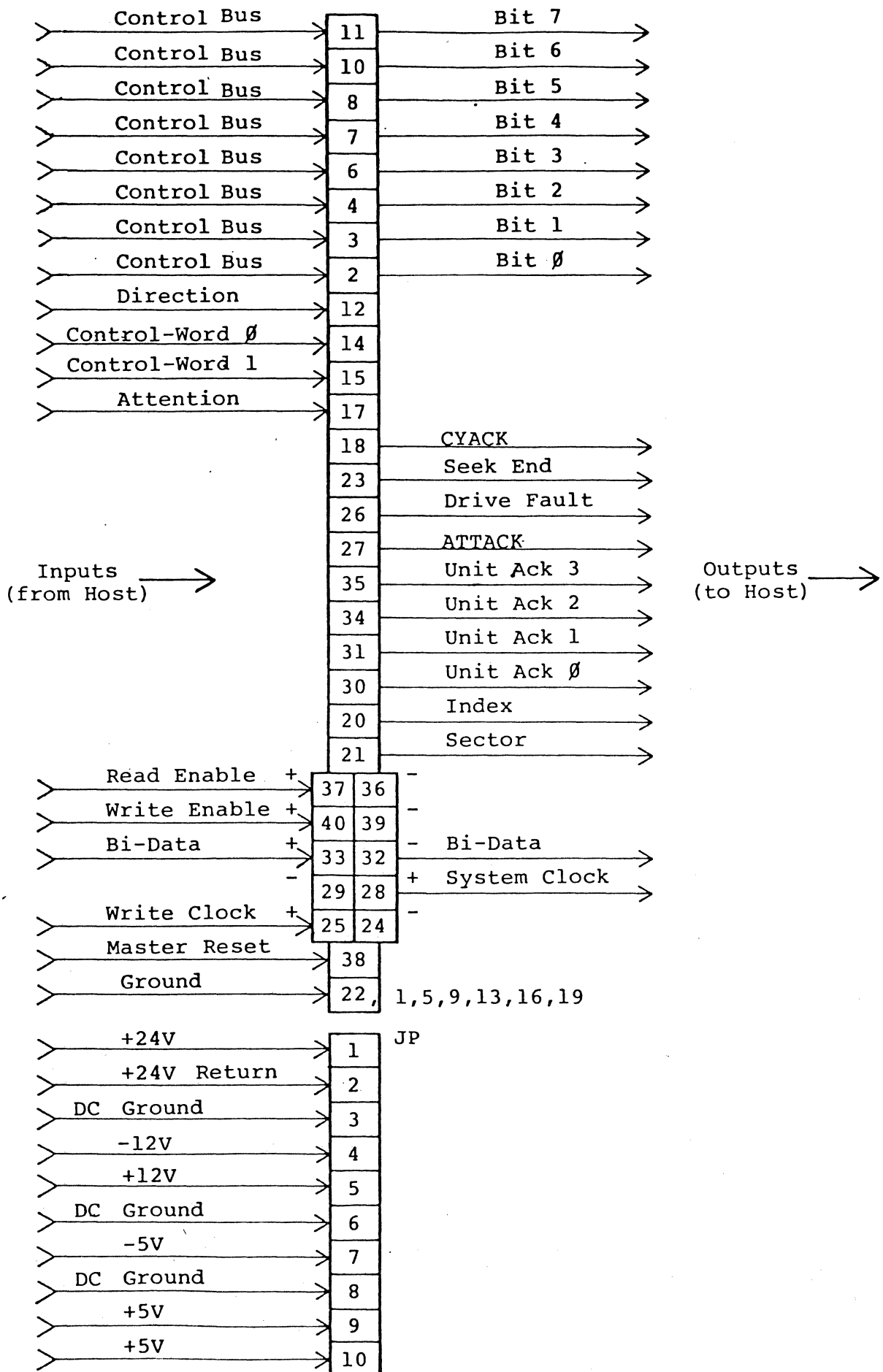
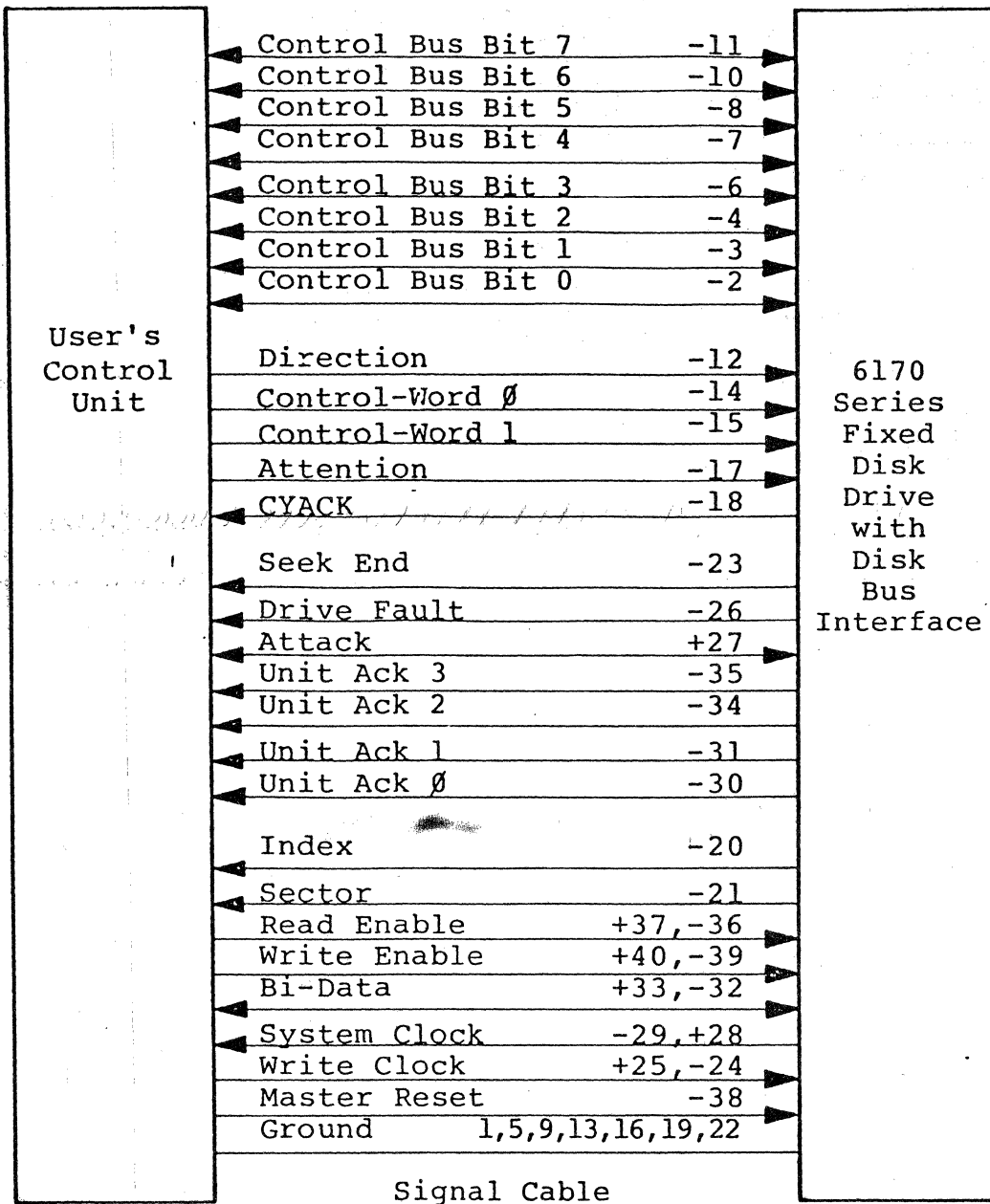


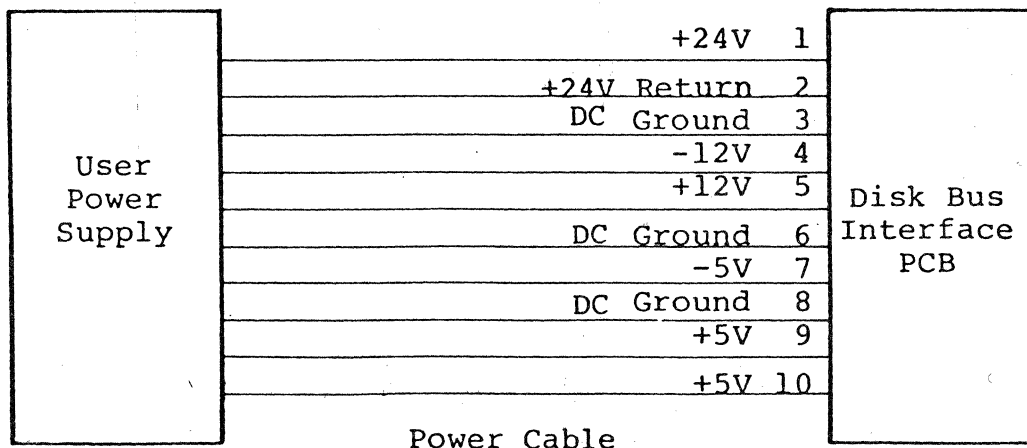
Figure 3-1 Disk Interface Bus

JB



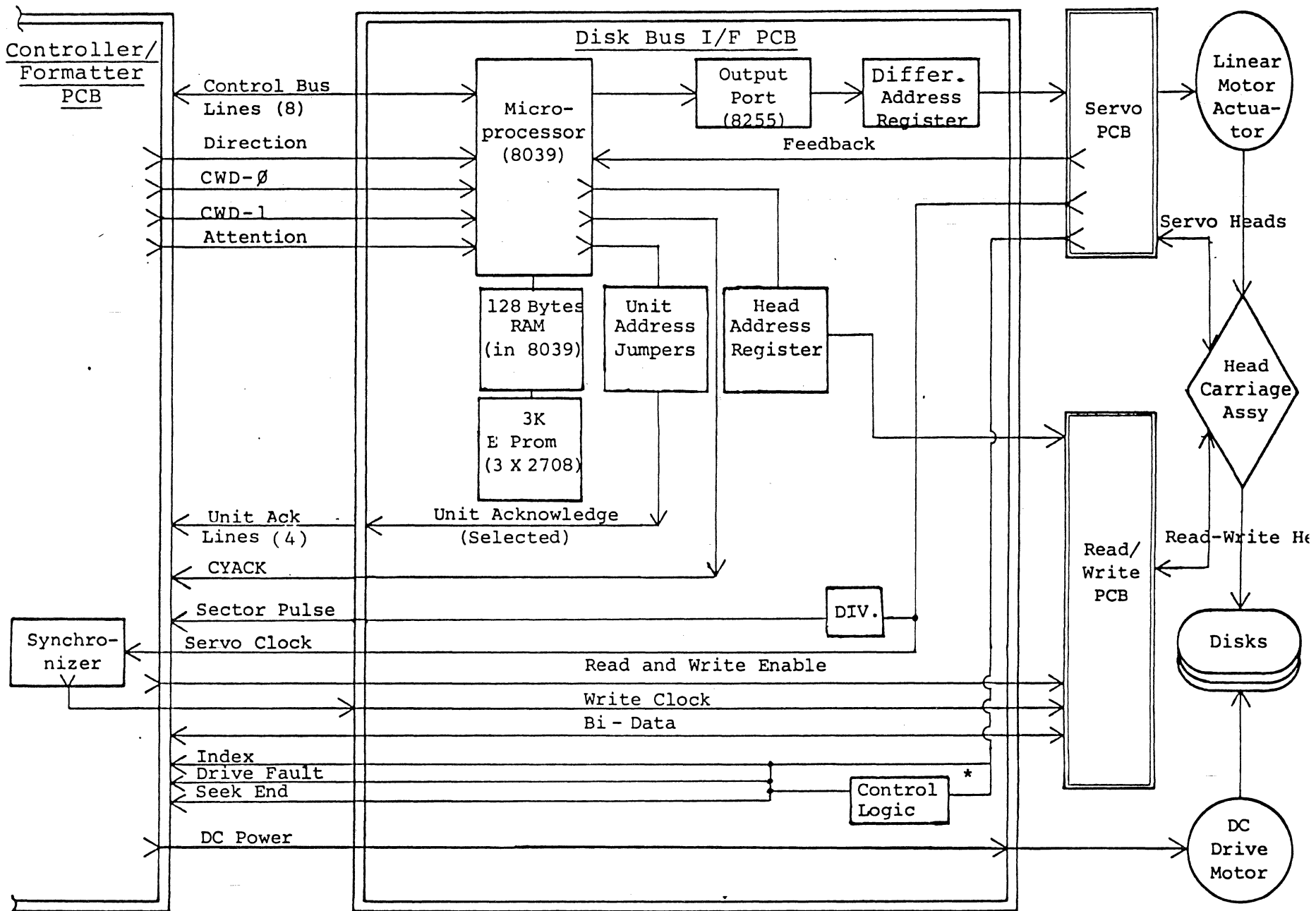
6170 Series Fixed Disk Drive with Disk Bus Interface

JP



Disk Bus Interface PCB

Figure 3-2 Interface Lines



\* Under Microprocessor Control

Figure 3-3 Functional Block Diagram - Disk Bus

- Controller-Formatter PCB
- Disk Bus Interface PCB
- Servo PCB
- Read/Write PCB
- Linear Motor Actuator
- Head Carriage Assembly
- Disks
- DC Disk Drive Motor

The Controller-Formatter is supplied by the user. It is shown in Figure 3-3 only to give increased meaning to the remaining functional elements, all of which are located in the Kennedy 6170 Disk Drive Unit. The Disk Bus Interface Board contains the control logic and timing for executing the principal operations of the disk drive subsystem, which are:

1. Select a Disk Drive Unit - This is done by comparing Unit Address information which comes over the Control Bus from the Controller-Formatter with the configuration of Unit Address jumpers on the Disk Bus Interface PCB. When a given drive's jumper configuration agrees with the Unit Address that is being received, that drive responds to the Controller-Formatter (i. e., the drive is "selected"). A Unit Acknowledge "number" (4 lines) is sent to the Controller-Formatter.
2. Seek - The Head Carriage Assembly is positioned at the cylinder where writing or reading is to take place using drive circuitry that is located on the Servo PCB. A head is selected to establish the specific surface where data is to be written or read, via the Read-Write PCB. Then, the specific track and sector where writing or reading is to begin is established by the Interface PCB. The servo system positions the head at the correct cylinder and holds the head on-cylinder.
3. Write - Serial binary data from the Controller-Formatter is written into the data areas of sectors of a track; timing is synchronized to the disk by using system clock pulses to generate write clock pulses.
4. Read - Data that was written as described above, is read-back from the disk and sent to the Controller-Formatter so that it can be acted upon by the host CPU.

Physical connection between the Disk Bus Interface in Figure 3-1 and a) other 6170 Disk Drive Units, as well as b) the Controller-Formatter in the host system, is made using two signal cables and one power cable, as described in Paragraph 10.1.2. Cables.

## 10. 1. 2 CABLES

The two cables which interface the 6170 with a Disk Bus Interface to other 6170 drives and to the host system are listed in Table 3-1.

TABLE 3-1 INTERFACE CABLES

<u>CABLE NAME</u>	<u>DESCRIPTION</u>	<u>MFTR. &amp; PART NO.</u>
Signal Cable to Jack JB	40-conductor flat ribbon cable -- maximum of	Spectro-Strip No. 455-248-40
	Connector (Open strain relief)	3M 3417-6040
Power Cable	10-conductor, 18-gauge wire -- maximum of 4 ft. (1.2 m)	Fabricated by User
	Connector	AMP 1-640426-0

A. Location - The location of the above two cables is as shown in Figure 3-4. Marker bands on the cable are keyed on pin No. 1 of the receptacle on the PCB.

B. Connections - The signal cable can be connected to up to 15 daisy-chained disk drives. Terminators must be installed in the controller as well as each drive of the daisy-chained string. Figure 3-5 shows as daisy-chained connection.

## 10. 1. 3 RECEIVERS/DRIVERS

The cable connected to JB of the Controller-Formatter contains the following type of information: control signals, status lines, timing pulses, clock pulses and data signals. Command and status transfers are asynchronous, thereby allowing a simple direct interface to the host mainframe. This is especially useful to LSI-type microprocessor-based host CPU's. Signals on the bus use an attention/acknowledge handshake which can be controlled by user hardware or software via microprocessor-port I/O bits.



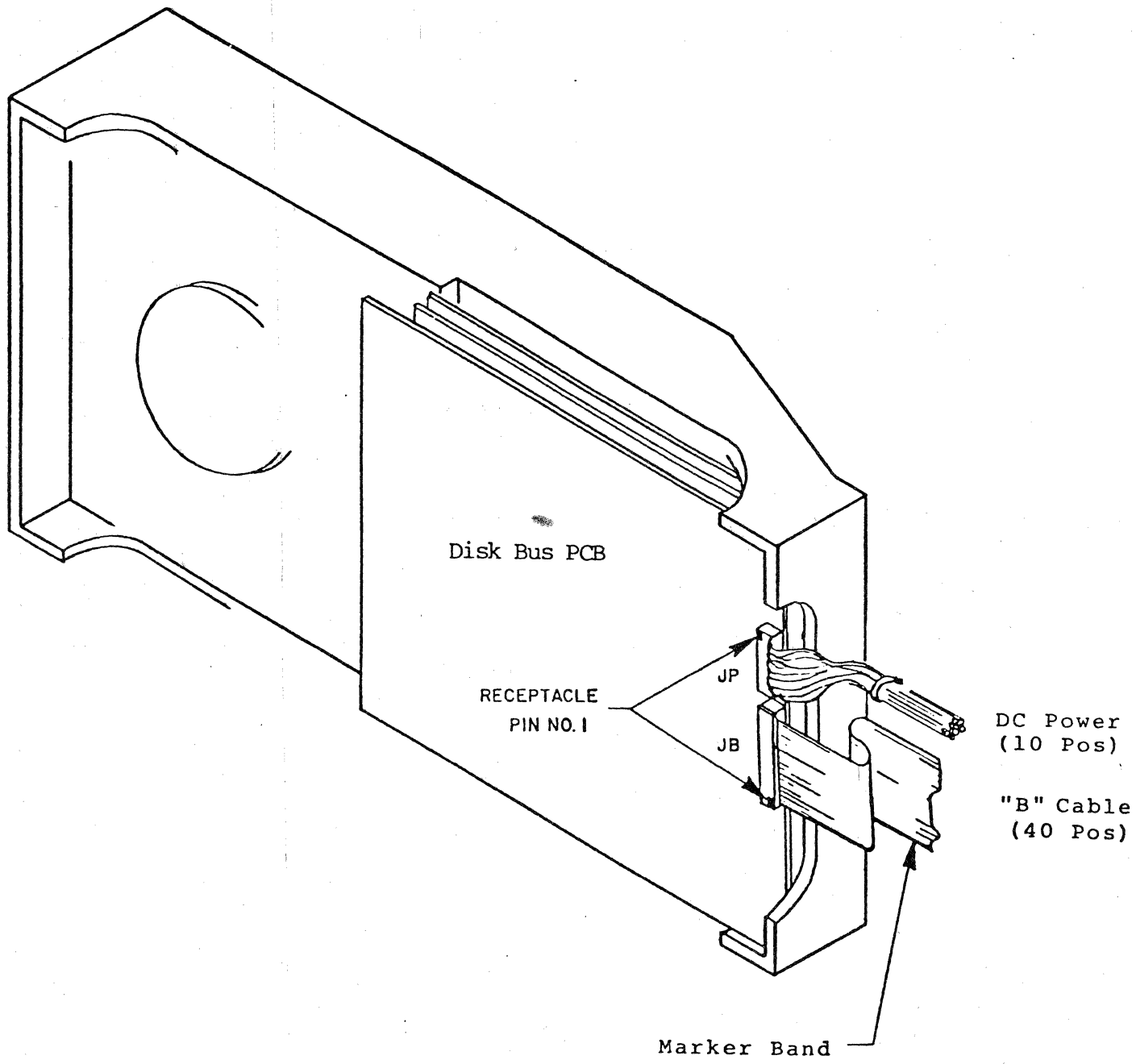


Figure 3-4 Cable Locations

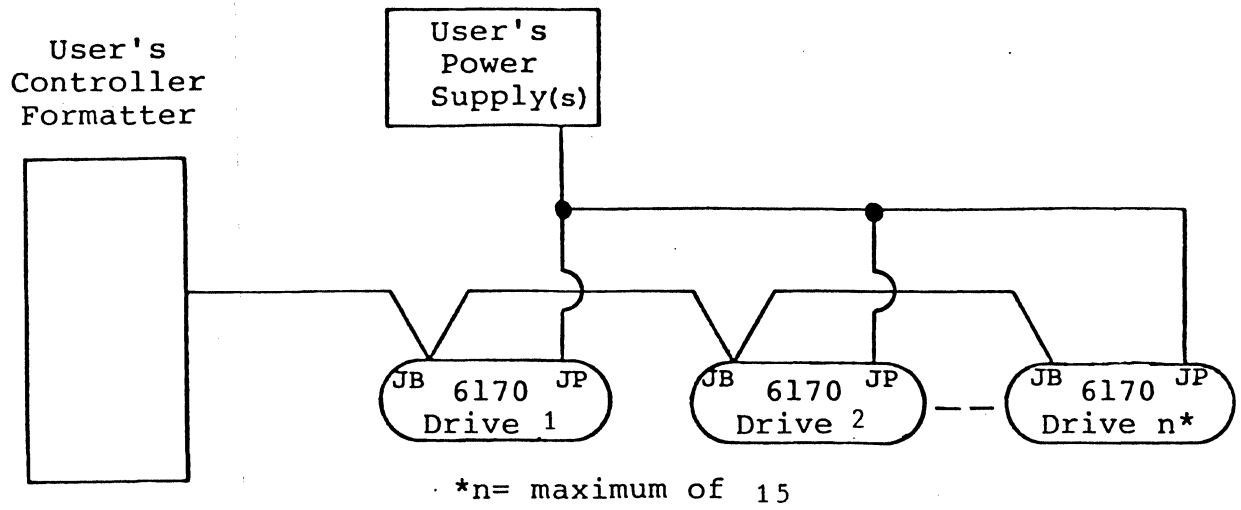


Figure 3-5 Daisy-Chained Connection

All "signals" on the bus are standard TTL levels, with the exception of Read-Write Data and Clocks, Read Enable, and Write Enable, which use industry-standard differential driver/receivers to assure data and timing integrity. The differential driver/receivers operate in a balanced mode; that is, noise induced on one line is common-mode at the receivers input terminals, where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit, insuring that system performance is isolated from circulating ground circuits. The typical delay is approximately  $(30 + 1.3 L)$  nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and the receiver.

Figure 3-6 shows the Receiver/Drivers circuits and terminators for the eight control bus signals.

Figure 3-7 shows the Receiver//Driver circuits and terminators for the various "control" signals.

Figure 3-8 shows the Receiver/Driver circuits for the five differential-pair signal lines.

#### 10.1.4 TERMINATORS

The differential-pair lines on JB are terminated in 56-ohms to ground, as shown in Figure 3-8. The "Bi-Data" lines have additional 10K ohm resistors to +5V and -5V, as shown in Figure 3.207, note 6.

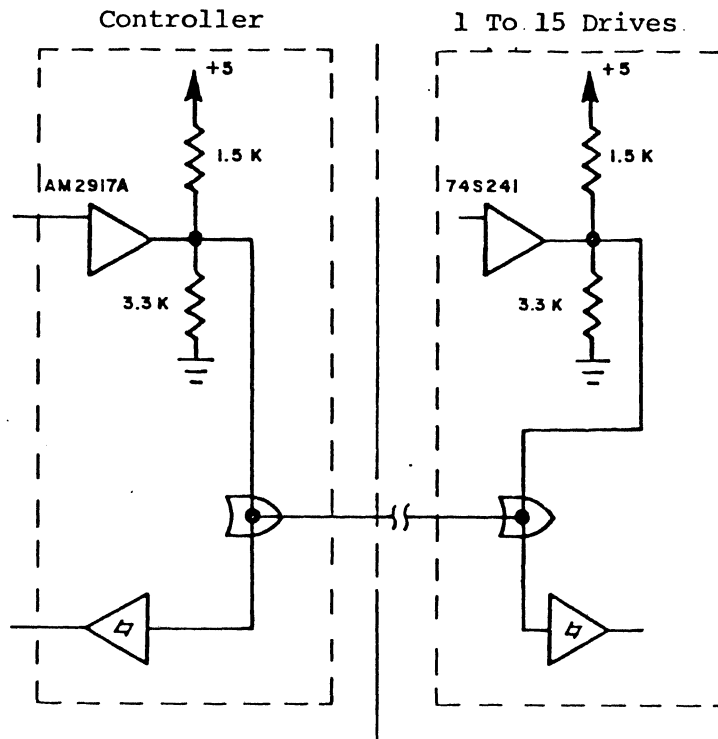
#### 10.1.5 SIGNAL LEVELS

Typical signal levels for differential lines are as given below:

Logical 1:	- (low) signal	-0.45V
	+ (High) signal	0V
Logical 0:	+ (Low) signal	0V
	- (High) signal	+0.45V

Signal levels for standard TTL lines are as follows:

Logical 1 = <0.4 volts = low = Activated  
Logical 0 = >2.4 volts = High = De-activated



- NOTES: 1. BUS CABLE IS 40 CONDUCTOR-26 OR 28 GAUGE FLAT CABLE.  
 2. CONTROLLER AND EACH DRIVE IS TERMINATED WITH 1.5K/3.3K NETWORK.  
 3. MAXIMUM CABLE LENGTH IS 30 FEET. (914 cm)  
 4. 74S241 AND 74LS244 MAY BE SUBSTITUTED FOR AM2917A.

Figure 3-6 Control Bus Drivers, Receivers and Terminators

### 10.1.6 JUMPER-SELECTABLE OPTIONS

The Disk Bus Interface Board contains two Jumper Blocks which are used to enable certain options, as listed below:

Option 1 - Establishes the address of the drive as one of the numbers between 1 and 15 (15 possible unit address).

Option 2 - Establishes the model no. of the drive as follows:

6172	24 MB
6173	40 MB

Option 3 - Establishes sector data sizes with three different amounts of overhead -- two of the overhead amounts (28 and 44) offer six different sector data sizes; the third overhead amount (36) offers three different sector data sizes.

Option 4 - Establishes which heads are to be "write-protected". The choices are 0-5, depending upon the number of disks/heads per drive.

Each of the above four options are described further below.

#### A. UNIT ADDRESS SELECTION

Figure 3-9 shows the effects of jumpers on unit address selection.

There are four jumper locations; they are labeled UN0 through UN3 and are located on the jumper block in PCB location 1C of the Disk Bus Interface board. Some examples follow:

1. In order to establish the drive as unit no. 1, the UN0 jumper must be installed.
2. In order to establish the drive as unit no. 8, the UN3 jumper must be installed.
3. In order to establish the drive as unit no. 14, the UN1, 2 and 3 jumpers must be installed.

#### B. MODEL I. D.

Model I. D. is established by the presence or absence of a jumper across locations labelled ID0-ID2 of the jumper block in PCB location 1C. Figure 3-10 graphically shows this.

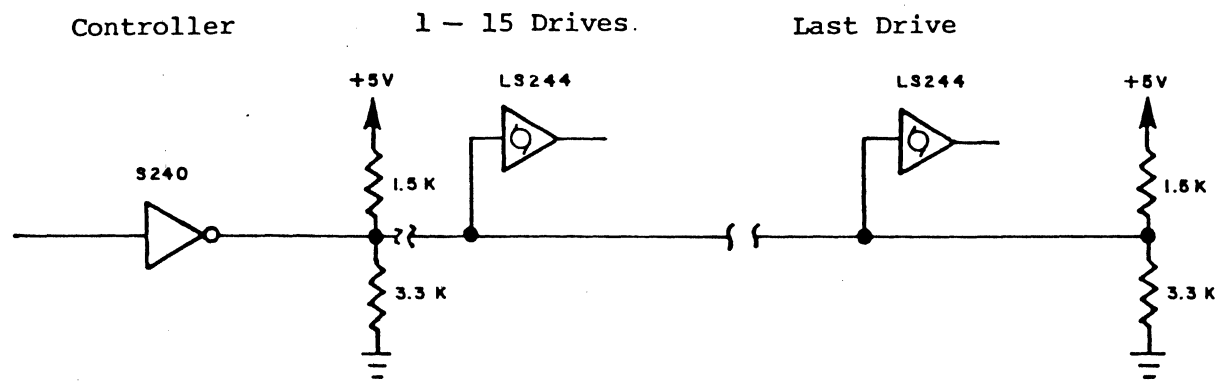
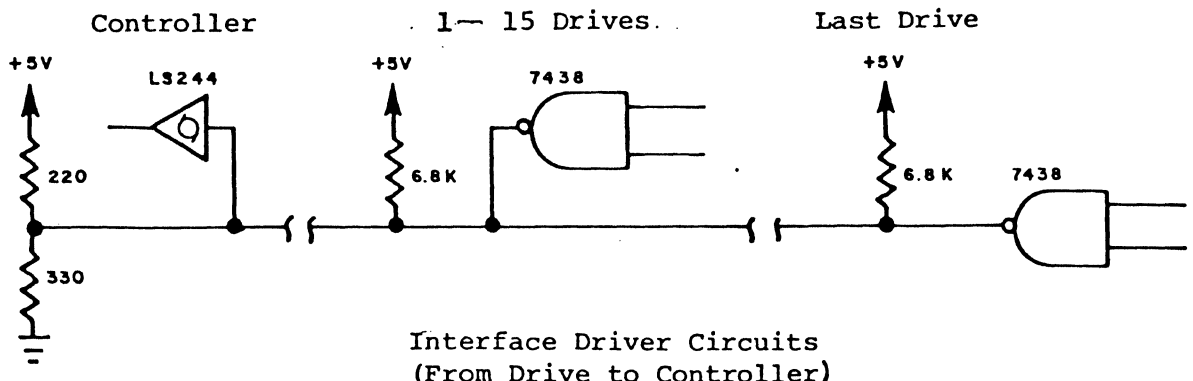


Figure 3-7 Control Signal Drivers, Receivers and Termination

### C. SECTOR SIZE SELECTION

Figure 3-11 shows the jumper locations that result in specific sector-size selections. The sector-size selections in turn affect the number of bytes per sector and hence, the number of bytes per track. Note that the Disk Bus Interface offers a choice of three overhead sizes. The specific contents of the "overhead" are given in specification Section 10.5, Sector Formats.

### D. HEAD WRITE PROTECTION

There are two methods of effecting write protection using the Disk Bus Interface PCB. One method uses jumper plugs; the other method uses programmatic selection. If the jumper plugs are used, they cannot be over-ridden by the programmatic method.

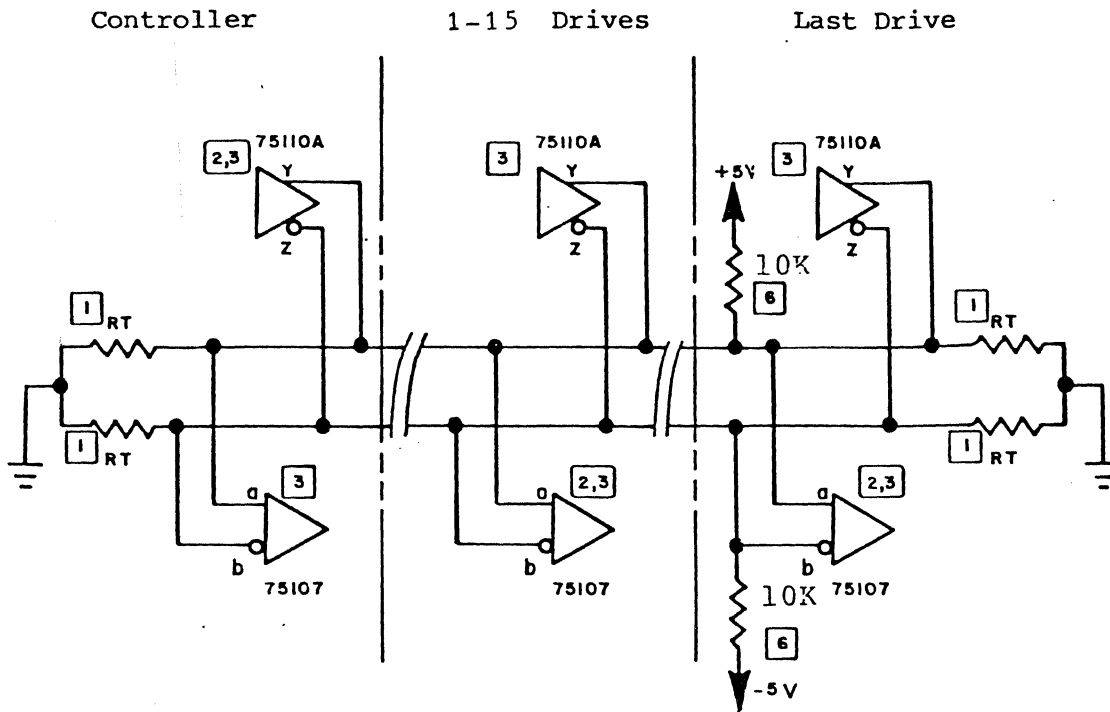
#### 1. JUMPERED WRITE PROTECTION

Figure 3-12 shows the three jumpers that are available for write protection. Jumper locations on the jumper block in PCB location 1B are used. The table in Figure 3-12 shows that if a jumper is installed at WPO, head 0 is write protected; if a jumper is installed WP1, both heads 0 and 1 are write protected, etc.

#### 2. PROGRAMMABLE WRITE PROTECTION

"Programmable" write protection can be effected if there are no jumpers installed in the jumper locations described in 1, above. A special command called "EXT PROT 0, 1 and 2" executed at command-word 3 time. This command must be formed in the host computer and sent to the drive via the Controller-Formatter. The three least significant bits of the command are used for head write protection. These bits remain in the position that they were set until a subsequent command-word-3 command is executed. Figure 3-13 shows the formatting of the command word and the resultant logical functions on write protection.

It can be seen from review of Figure 3-13 that heads 0 and 1 are write-protected as a function of the state of the least significant two bits of the command word.



- NOTES:
1.  $RT = 1/2$  FLAT CABLE LINE IMPEDANCE (56 $\Omega$  TYPICAL).
  2. READ ENABLE, WRITE ENABLE, SYSTEM CLOCK AND WRITE CLOCK ARE SINGLE DIRECTION LINE PAIRS.
  3. BI-DATA IS A BIDIRECTIONAL DATA BUS LINE PAIR.
  4. MAXIMUM CABLE LENGTH-30 FEET.
  5. ALL PAIRS ARE TERMINATED BOTH AT CONTROLLER AND LAST RECIEVER IN DAISY CHAIN.
  6. ONLY DRIVE OR LAST DRIVE, BI-DATA LINES ONLY.

Figure 3-8 Differential Pair Signal Line Drivers/Receivers



Unit Address  
Jumper Configuration

Unit Address	UN 3	UN 2	UN 1	UN 0
Unit 1				●
Unit 2			●	
Unit 3			●	●
Unit 4		●		
Unit 5		●		
Unit 6		●	●	
Unit 7		●	●	●
Unit 8	●			
Unit 9	●			●
Unit 10	●		●	
Unit 11	●		●	●
Unit 12	●	●		
Unit 13	●	●		●
Unit 14	●	●	●	
Unit 15	●	●	●	●

● Indicates Jumper Installed

PCB Location  
1C

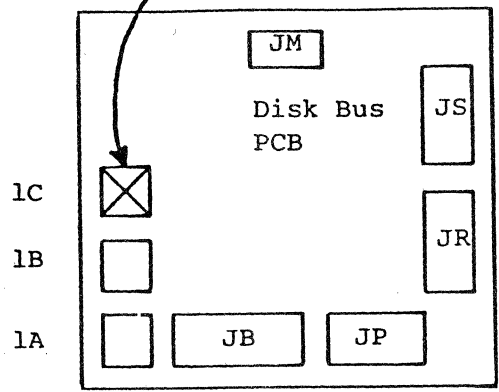
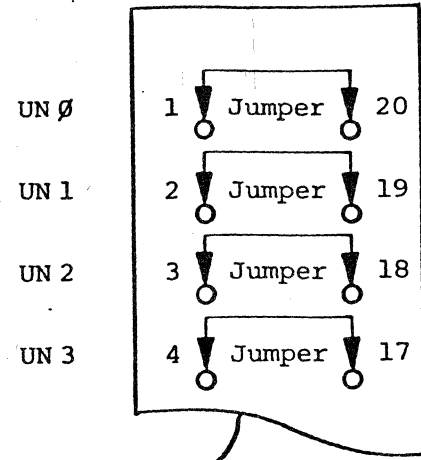


Figure 3-9 Unit Address Selection

## 10.2 SIGNAL LINE FUNCTIONS AND LOGIC

Figure 3-2, earlier in this section, showed the nomenclature for the signals on the lines of the interface cable. This subsection briefly describes the functions that the signals perform and the logic which activates them. The signal lines are described as they are shown in Figure 3-2, from top to bottom. Reference is made to timing diagrams in Subsection 10.3. A summary of the line specifications can be found in Figure 3-15.

### 10.2.1 CONTROL BUS

The Control Bus is an 8-bit bi-directional bus (numbered 0 through 7) that carries "control" information to the drive from the Controller-Formatter, or "status" information from the drive to the Controller-Formatter. The direction in which the bus is operating is controlled by the Controller-Formatter using a line called "Direction" (or Bus Direction). This is described in Paragraph 10.2.2. The meaning of each bit on the control bus is determined by the state of Direction, plus two other lines: Control Word 0, and Control Word 1. Up to 32 bits of control information and up to 32 bits of status information can be transferred between the drive and the controller using these lines. There are four words of eight bits each in both directions. The disk drive will only recognize the Control Bus bits when the Attention (ATTN) line is active. This line is also known as a "Bus Request" line. When ATTN becomes active, the bits on the bus are either read by the Controller-Formatter (Status Information) or executed by the Disk Drive Unit (Control Information). After the bus bits have been activated to signal that the drive has responded to the attention request.

### 10.2.2 DIRECTION

The direction line determines which direction the Control Bus will operate in terms of the Controller-Formatter. A logic "0" (greater than or equal to 2.4 V) on the Direction line indicates that the Controller-Formatter is reading one of the four status bytes from the selected drive. Similarly, a logic "1" (less than or equal to .4 V) on the Direction line indicates that the Controller-Formatter is sending command bytes to the selected drive. Direction must become active 200 ns before Attention becomes active and must remain active until Attention goes inactive. See Figure 3-16 and 3-17.

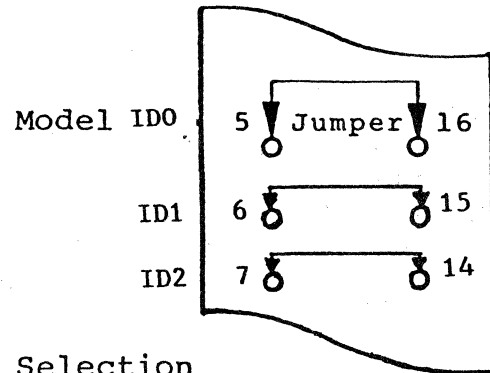
Model ID  
Jumper Configuration

Drive Type	Model ID		
	ID0	ID1	ID2
6172/24MB	●		●
6173/40MB	●	●	

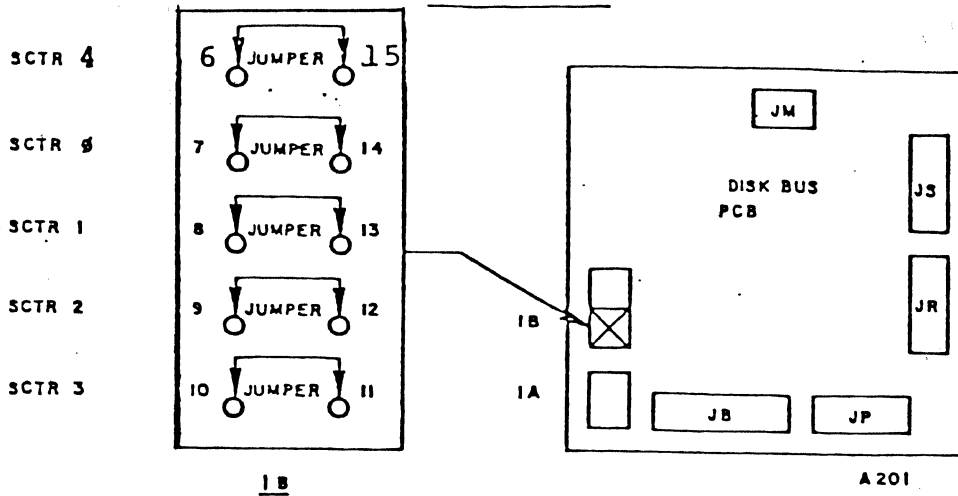
● Indicates Jumper Installed

Figure 3-10 Model ID Selection

Jumper Block in  
PCB Location 1C



## SECTORING



SECTOR FORMAT				JUMPER LOCATIONS				
OVERHEAD BYTES	DATA BYTES	# SECTORS/TRACK		SCTR 4	SCTR 3	SCTR 2	SCTR 1	SCTR 0
		DECIMAL	HEX					
28	128	84	54					
28	256	46	2E					●
28	512	24	18				●	
28	1024	12	0C				●	●
28	2048	6	06			●		
28	4096	3	03			●		●
36	128	80	50			●	●	
36	256	45	2D			●	●	●
36	512	24	18		●			
44	128	76	4C		●			●
44	256	44	2C		●		●	
44	512	23	17		●		●	●
44	1024	12	0C		●	●		
44	2048	6	06		●	●		●
44	4096	3	03		●	●	●	
28	128	85	55	●				
36	128	81	51	●		●	●	
44	128	77	4D	●	●			●
-----UNASSIGNED-----				ALL OTHER COMBINATIONS				

● INDICATES JUMPER IS INSTALLED

Figure 3-11 Sector Size Jumpers

### 10.2.3 CONTROL WORD 0 (CWD 0) AND CONTROL WORD (CWD 1)

The CWD 0 and CWD 1 lines are used to identify the four bytes that can be present on the Control Bus, as shown in Figure 3-14.

CWD 0 and CWD 1 are used to address one of four bytes; Direction determines whether the bytes are "command" bytes or "status". Figure 3-15 in Paragraph 10.2.18 summarizes the various bits of the command and status bytes (excepting ATTACK). CWD 0 and CWD 1 must be activated before Attention is activated. It must remain activated until CYACK (Cycle Acknowledge or Bus Acknowledge) is de-activated.

### 10.2.4 ATTENTION (ATTN) OR BUS REQUEST

The Attention line initiates the Control Bus hand shake; it is generated by the Controller-Formatter and is sent to all disk drives connected to the Controller-Formatter.

When a control byte is sent to the drive, drive logic delays the "latching" of the control word until all transition-induced cross-talk and ringing subsides. The control byte and the Attention line are then polled again.

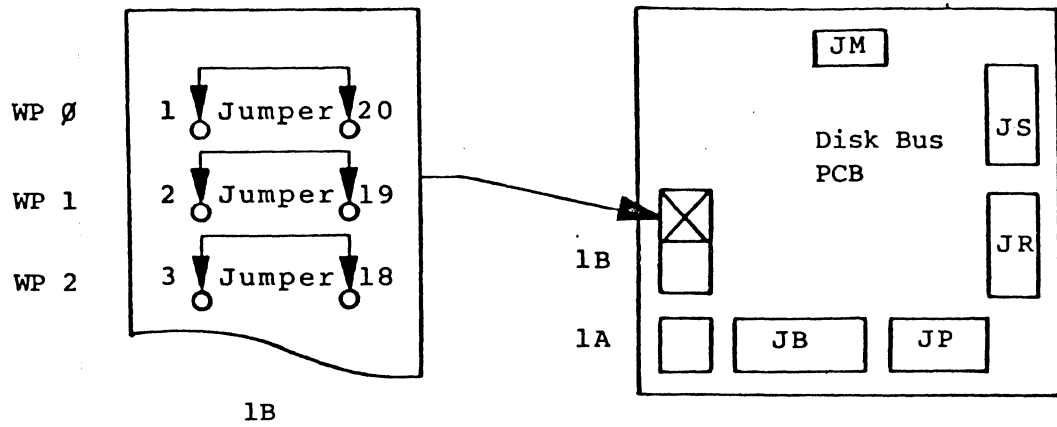
### 10.2.5 CYCLE ACKNOWLEDGE (CYACK) OR BUS ACKNOWLEDGE

The CYACK signal is generated by all drives in response to an Attention (Bus Request) signal from the Controller-Formatter. It signals that the drive "has seen" the Attention request. Only the selected (see 10.1.1-A) drive acts upon the Attention request. The type of action that is taken is determined by the Direction line, as follows:

Direction Line Active (Logical 1): Command Byte

Direction Line Inactive (Logical 0): Status Byte

CYACK stays active until each drive has seen the Attention line go inactive. See subsection 10.3.2, Unit Select Timing.



Write Protect  
Jumper Locations

Protected Head	WP 2	WP 1	WP 0
None			
Head 0			●
Head 1		●	
Head 2		●	●
Head 3	●		
Head 4	●		●
Head 0,1,2	●	●	
Head 0,1,2,3,4	●	●	●

● Indicates Jumper Installed

Note: The Servo Head is always Write Protected.

Figure 3-12 Head Write Protect Jumpers

DIR	CWD1	CWD0	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	Ext. Prot 2	Ext. Prot 1	Ext. Prot 0

External Protect			Function
2	1	0	
0	0	0	No Head Protected
0	0	0	Head 0 Protected
0	1	0	Head 1 Protected
0	1	1	Head 2 Protected
1	0	0	Head 3 Protected
1	0	1	Head 4 Protected
1	1	0	Head 0,1 and 2 Protected
1	1	1	Head 0,1,2,3 and 4 Protected

Figure 3-13 Programmed Head Write Protection

#### 10.2.6 ATTENTION ACKNOWLEDGE (ATTACK)

ATTACK is a signal which is only activated after each drive responds to the Attention line. When ATTACK is activated, it causes CYACK to be activated. See Subsection 10.3.2, Unit Select Timing. "Attack" is an open collector positive true TTL signal terminated by the controller with a 220/330 network but is used only by multiple drives to allow synchronization in response to ATTN. It has no meaning to the Controller and should therefore be ignored by the Controller.

NOTE: ATTACK is active "high" and is an exception to the general rule that interface logic is active when "low".

#### 10.2.7 SEEK END

The Seek End signal is generated by the currently selected drive whenever a Seek operation has been completed or aborted. Sub-section 10.3.3 describes Seek Timing.

#### 10.2.8 DRIVE FAULT

The Drive Fault signal is activated by the selected drive whenever a fault occurs or whenever there is a Power-on-reset (POR) or Master Reset. The following conditions can cause a fault:

- Servo Error
- Read-Write Error
- Drive Error from Status Bits
  - a. PLD Error
  - b. Unsafe
  - c. Speed Error
  - d. Power Loss

The Drive Fault line is de-activated whenever a Fault Clear command to the drive by the Controller-Formatter, provided the condition which caused the fault no longer exists.

#### 10.2.9 UNIT ACK 0 THROUGH UNIT ACK 3

The Unit Acknowledge lines are activated by the selected drive and contain the binary coding of the selected drives address. See 10.1.6-A. The combination of a) the unit address desired by the Controller-Formatter, and b) the jumpers on the Unit Address jumper block, determine the state of the Unit Ack lines.



Direction (state)	CWD 1 (state)	CWD 0 (state)	Control Word No.	Control Word Type
1	0	0	0	Command Word
1	0	1	1	
1	1	0	2	
1	1	1	3	
0	0	0	0	Status Word
0	0	1	1	
0	1	0	2	
0	1	1	3	

Figure 3-14 Control Bus Addressing

Note: "1" = True = Active

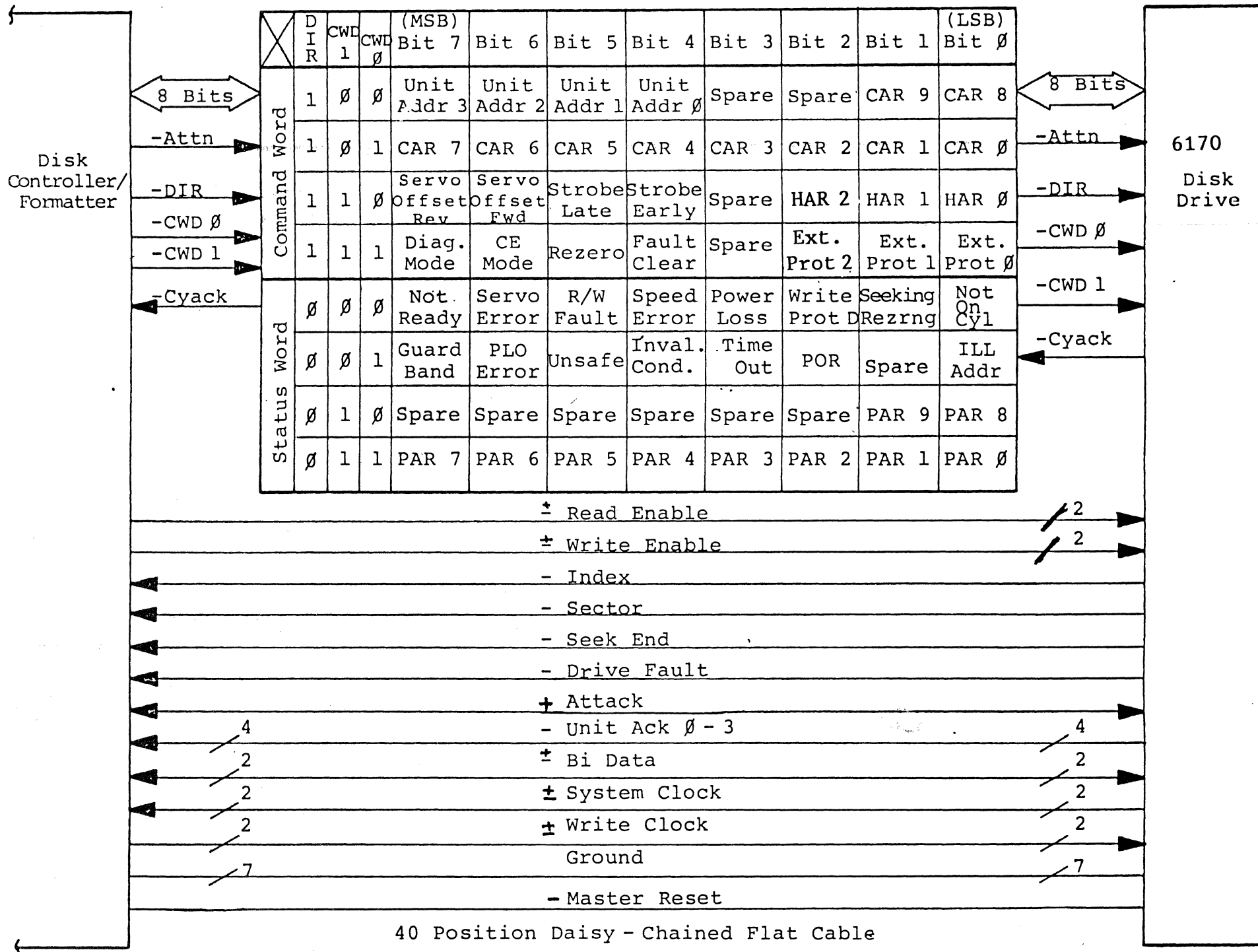


Figure 3-15 Control Bus Bit Definition Chart

### 10.2.10 INDEX

Index is a pulse that is generated from a pattern on the pre-recorded servo disk. It is generated once each revolution. Each cylinder is capable of producing an index pulse. The pulse is 2.5 microseconds in duration and occurs every 16.67 milliseconds. Sector 00 immediately follows the index pulse. The Controller-Formatter uses the index pulse for synchronizing purposes. See Subsection 10.3.7.

### 10.2.11 SECTOR

The Sector signal is generated by the currently selected drive. It is active for 2.5 microseconds. Logic in the Disk Bus Interface PCB counts the number of byte positions from the last Index or Sector pulse and generates Sector pulses depending upon the sector-size selection jumpers. See Paragraph 10.1.6-C for a description of how sector size is selected.

### 10.2.12 MASTER RESET

Master Reset is activated by a transition from "high" to "low". It resets all internal latches and output ports. It has the same effect as Power On Reset which is described in Paragraph 10.3.1.

NOTE: The Signal lines which follow are "differential" lines which as previously specified, use industry standard differential line drivers (75110A or equivalent) and line receivers (75107 or equivalent). All differential lines are terminated with 56 ohm resistors to ground on each line, both in the Controller-Formatter, and in the last drive on the cable. Each "line" is in an active state (logical 1) when the non-inverted line (Output Y, input a) is more positive than the inverted line (Output Z, Input b). See Figure 3-8.

### 10.2.13 READ ENABLE

This line is activated by the Controller-Formatter to enable the read function in the selected drive, at the cylinder over which the heads are currently positioned. Before activating Read Enable, the Controller-Formatter must send a Control Word No. 2 and wait for CYACK to be returned. The procedure for doing this follows:

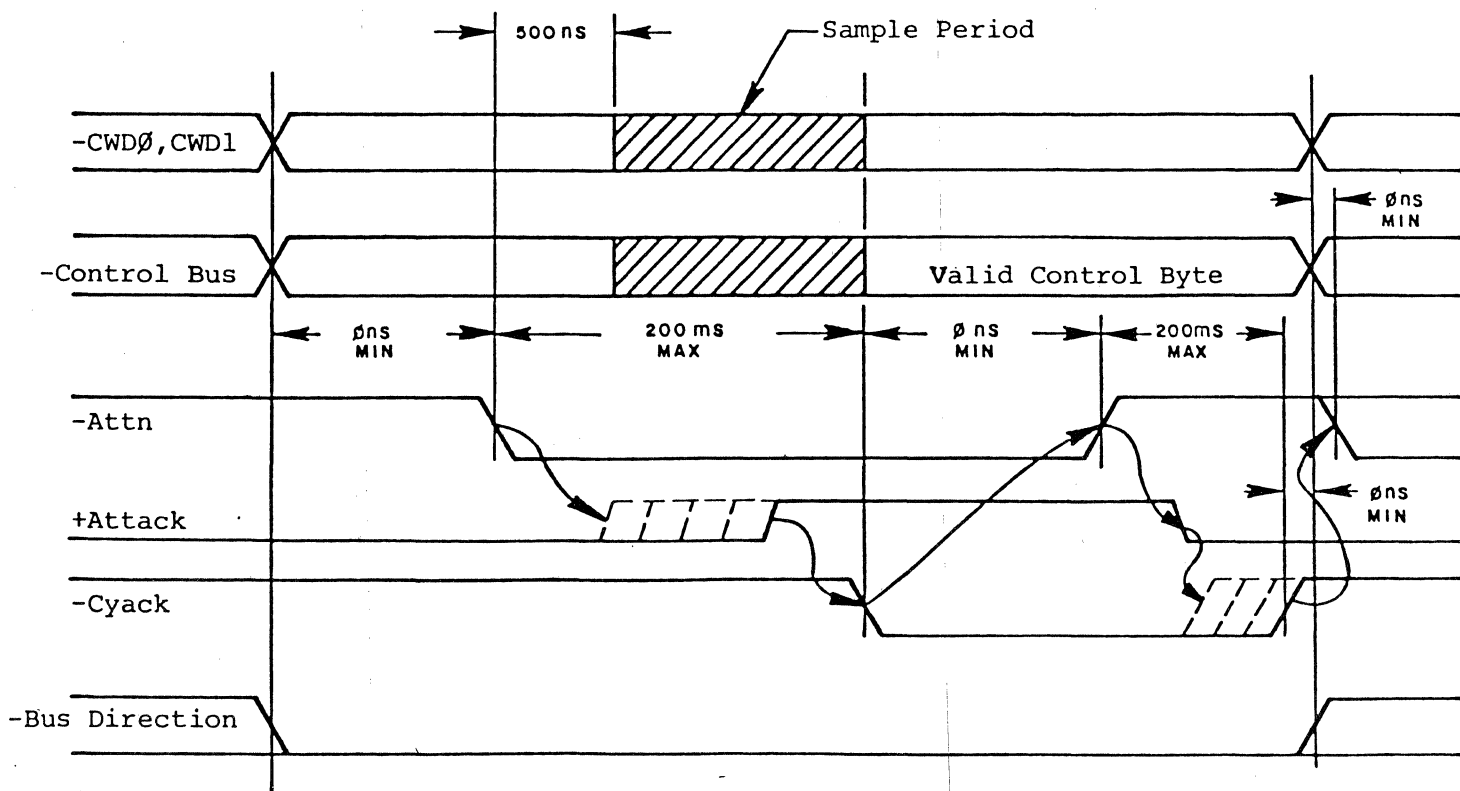
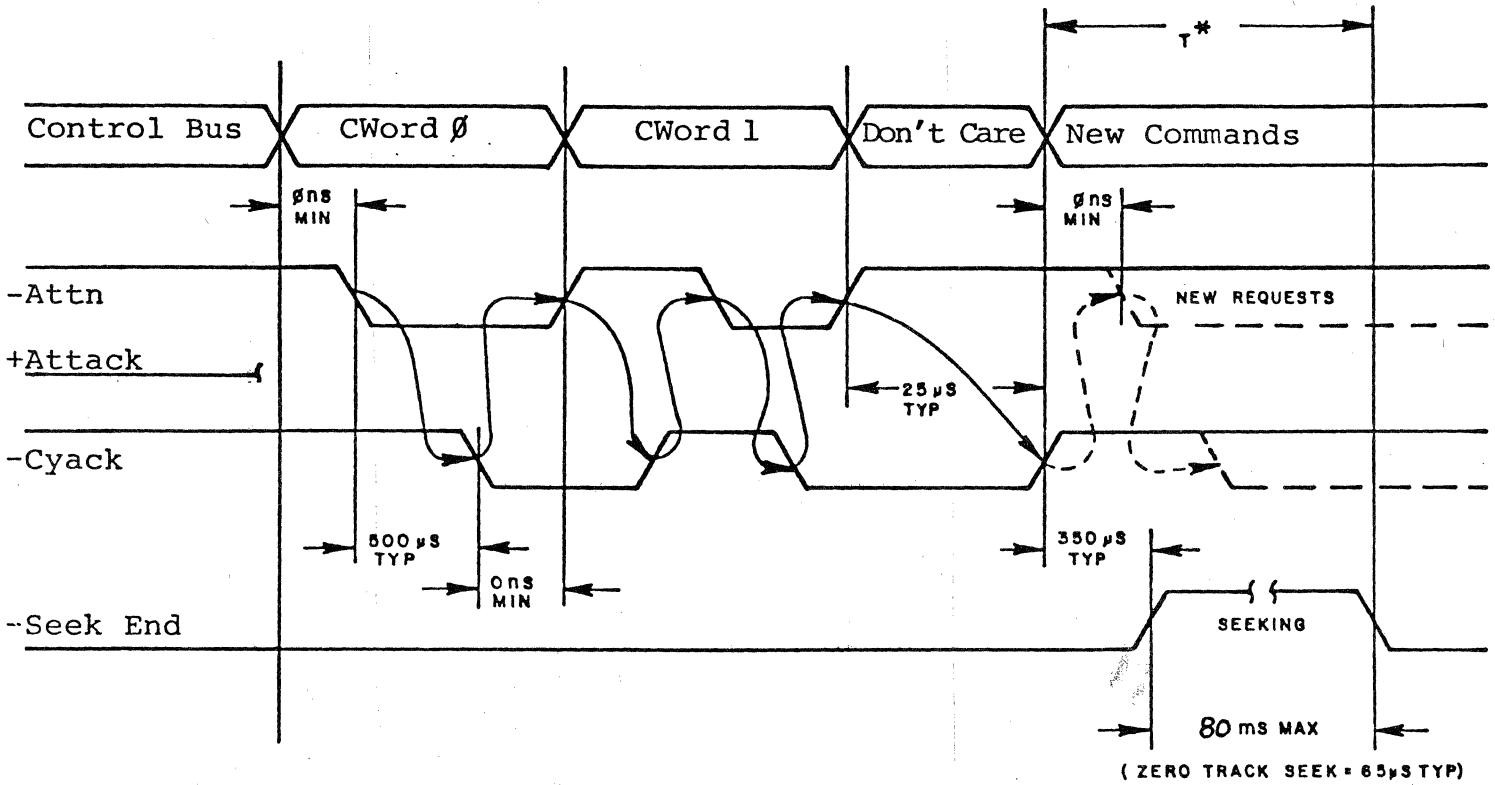


Figure 3-16 Control Word Sampling



\* FOLLOWING A SEEK COMMAND SEQUENCE TO A DRIVE, BUS OPERATIONS TO THAT DRIVE ARE LIMITED TO COMMAND WORD 0 (SELECT OR DE-SELECT) AND STATUS WORD 0 THRU 3 REQUESTS, UNTIL SEEK END IS ASSERTED. AT THIS TIME NORMAL BUS OPERATION MAY BE RESUMED TO THAT DRIVE. HOWEVER, ALL BUS FUNCTIONS TO OTHER NON-SEEKING DRIVES ARE PERMITTED AT ANY TIME.

Figure 3-17 Typical Seek Timings

a) Set the Bus Control Bits as follows:

-CWD 0 = "0"  
-CWD 1 = "1"  
- Direction = "1"

b) Set the Control Bus Bits as follows:

-HAR to desired head  
-Servo offset, if desired  
-Strobe early or late, if desired

The above lines must not be changed while Read Enable is active. They may be changed while Read Enable is inactive (for example, to change the head selection) without having to perform a new bus cycle. Read Timing is covered in Paragraph 10.3.5.

#### 10.2.14 WRITE ENABLE

This line is activated by the Controller-Formatter to enable to write function in the selected drive, at the cylinder over which the heads are currently positioned, provided the heads are not "write protected". If Write Enable is activated while the heads are write protected, the Fault line will be activated and Read-Write Fault status bit will be set. Before activating Write Enable, the Controller-Formatter must send a Control Word No. 2 and wait for CYACK to be returned. The procedure for doing this follows:

a) Set the Bus Control Bits as follows:

-CWD = "0"  
-CWD 1 = "1"  
-Direction = "1"

b) Set the Control Bus Bits to the desired head.

The above lines must not be changed while Write Enable is active. They may be changed while Write Enable is inactive (for example, to change the head selection) without having to perform a new bus cycle. Write Timing is covered in Paragraph 10.3.4.

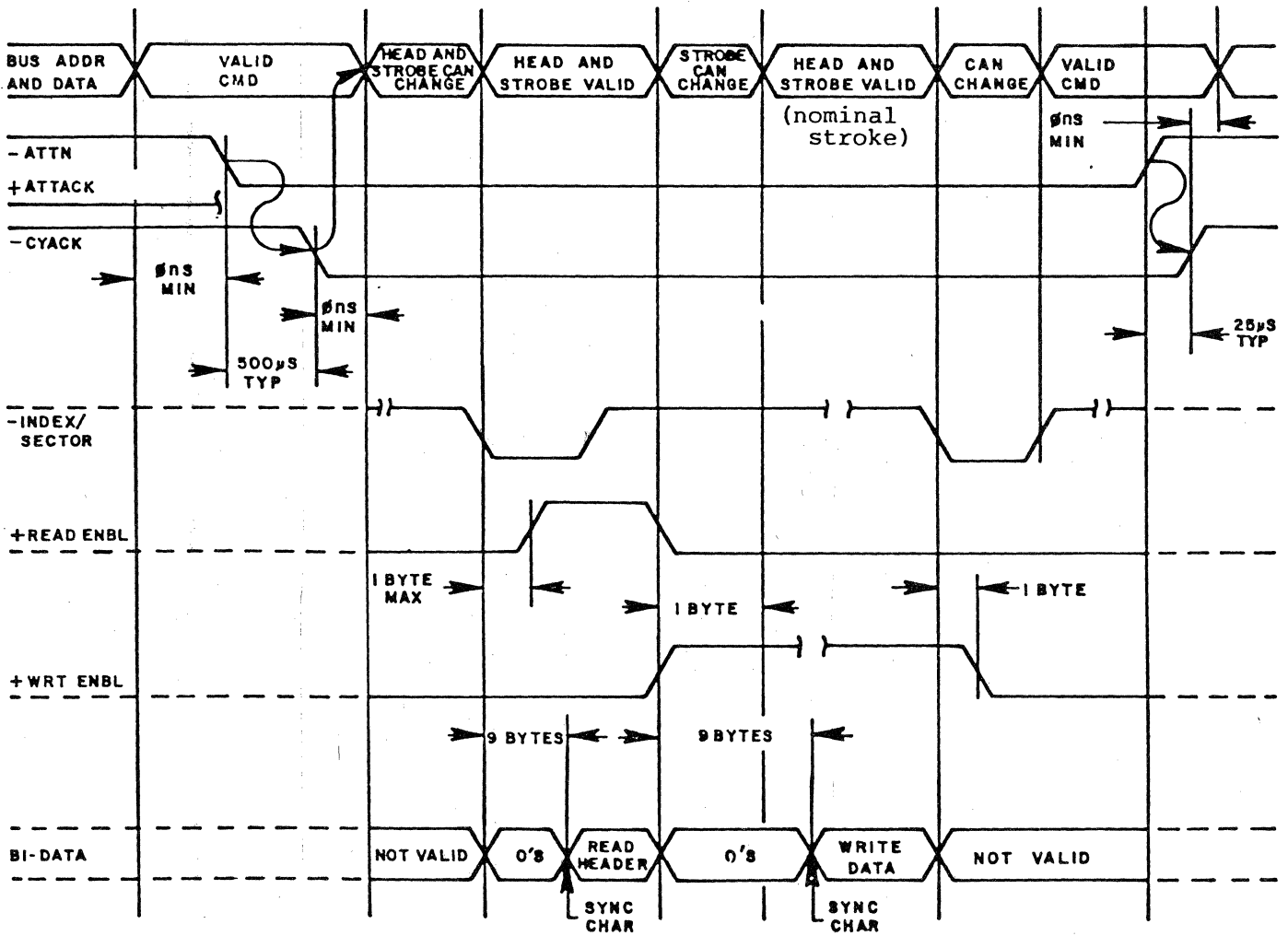


Figure 3-18 Typical Write Timing

#### 10.2.15 BI-DATA

Bi-Data is a bi-directional differential pair of lines that transmit serial NRZ read data from the currently selected drive to the Controller-Formatter whenever Read Enable is active; similarly, NRZ write data from the Controller-Formatter is sent to the drive when Write Enable is active.

These bi-directional data lines include a pair of 10K pull-up/down resistors to hold the lines in a known state when the drive is neither writing nor reading. These resistors should only be in the last drive of the daisy-chained string. Jumpers at locations 3D, 1 to 14, and 2 to 13 are used to connect/disconnect the resistors from the differential lines.

#### 10.2.16 SYSTEM CLOCK

The System Clock is a 6.40 MHz signal derived from a pre-recorded pattern on the servo surface of one of the disks. The signal is 16 times the sync frequency and is used to define bit-cell boundaries during write operations. The signal is sent to the Controller-Formatter which returns it as a "Write Clock". The write clock thus derived will have built-in provision for variations in disk rotation. During read operations, System Clock is synchronized to the data transitions through the data separator's VFO; as a result, the leading edge of the clock is accurately centered on the NRZ data cell.

#### 10.2.17 WRITE CLOCK

Write Clock is a differential signal which is derived from System Clock in the Controller-Formatter. It is transmitted along with write data from the Controller-Formatter, to the drive. The leading edge of the Write Clock must coincide with the center of the NRZ write data bit-cell. See Paragraph 10.3.4.

#### 10.2.18 CONTROL BUS SUMMARY

A summary of the bits in each of the two groups of four words is given in Figure 3-15. Eight bits at a time cross the bus. Each eight-bit grouping is called a word. There are four words per set. "Direction" determines whether the words are control words or status words. CWD 0 and CWD 1 determine which of the four possible words of a set are present on the bus. The significance of the bits in each of the eight 3-15. ATTN and CYACK control the sampling of the bus. All of the remaining lines are single-function lines that were described earlier in this section.



### 10.3 SIGNAL LINE TIMING

This subsection contains timing relationships between the signals and logic described in Subsection 10.2. Cross-reference is made to specific paragraphs of Subsection 10.2.

#### 10.3.1 POWER-UP SEQUENCE

When power is initially applied to the drive, a 15-second power-on reset timer is started. The timer disables the servo and prevents head movement until the disks are rotating sufficiently fast to sustain stable head flight. After the timer has timed-out, a check is made to assure that the drive is up to speed. If all power supply voltages are above their minimums, the drive automatically rezero's (i.e., the heads are positioned over cylinder 00). In addition, the "Unit Ready" and "On-Cylinder" status bits are turned on. "Seek End" is activated.

NOTE: The "Fault" line is set during the power-up sequence and reset at drive "Unit Ready" time.

#### 10.3.2 UNIT SELECT

A unit is "selected" using a control word from the Controller-Formatter. Bits 4 through 7 of Command Word 0 indicate the binary address of the desired unit. The "Attention" line causes the bus containing Command Word 0 to be sampled by all drives in the subsystem. The drive whose address corresponds to the requested address returns its address on the "Unit Acknowledge 0-3" lines. All drives emit a "Cycle Acknowledge" signal. Figure 3-16 shows the sampling of the control word.

When the Controller-Formatter receives a CYACK after having effected a unit selection, it should compare the "Unit Acknowledged" lines with the Unit Address that was sent to assure that the correct drive has been selected. When a different drive is selected by a subsequent Command Word 0, the previously selected drive is de-selected.

All drives on a daisy-chained string may be de-selected using Unit Address (0-Hex). 0-Hex is a non-existent address.

CAUTION: CYACK is returned by all drives on the bus even though none of the drives respond to the address being sought.

Bus Bits 0 through 3 are sampled at the time of drive selection. They must be issued prior to a Command Word 1 in order to effect a valid Seek, since they contain part of the cylinder address.

### 10.3.3 SEEK

A Seek is initiated by executing a Command Word 0 which selects the drive and establishes part of the cylinder address (Paragraph 10.3.2); a Command Word 1 is then executed to establish the remainder of the cylinder address. If the new cylinder address is different from the existing cylinder address, the "Seeking" status bit is set. The cylinder address cannot be changed until the seek is successfully completed, or aborted. After the seek is completed, the "Seek End" signal is activated. If the seek fails to complete, the "Fault", "Seek End" and "Servo Error" signals will be activated. Figure 3-17 shows typical seek timings.

When Command Word 0 is on the control bus, "Attention" can be activated. After the drive(s) has sampled the bus, "Cycle Acknowledge" is activated. This is repeated for Command Word 1. After a typical time of 350 microseconds, seeking begins.

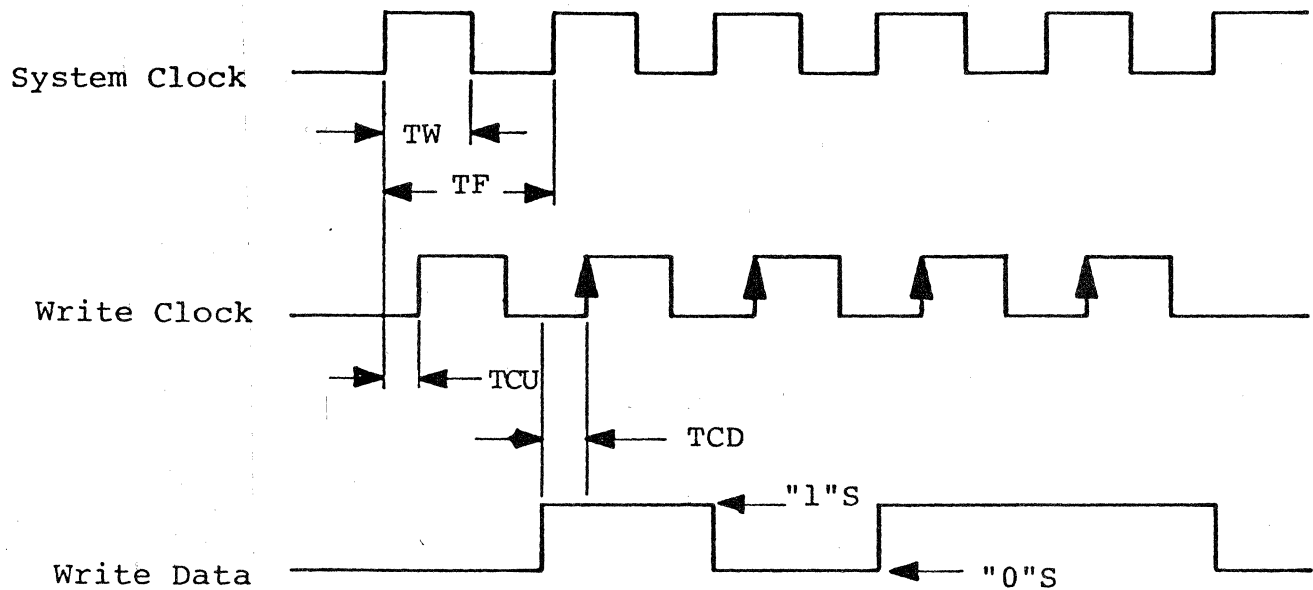
### 10.3.4 WRITE

A Write operation is begun by executing a Command Word 2 after the head-carriage has been positioned at the desired cylinder and the drive has been selected. Every write operation begins with a read operation during which the header is verified. Figure 3-18 shows typical read-write timing.

After the unit has been selected and a cycle acknowledge has been given, the next index or sector pulse activates "Read Enable", "Direction", CWD 0 and CWD 1. They remain activated throughout the read operation. HAR bits 0 - 2 may be changed within the timing constraints shown in Figure 3-18.

In order to properly synchronize the data-separating VFO, "Read Enable" must be activated in a field of zeroes which is at least eight bytes in length. The Controller-Formatter does this by using the leading edge of the sector or index pulse to activate Read Enable.

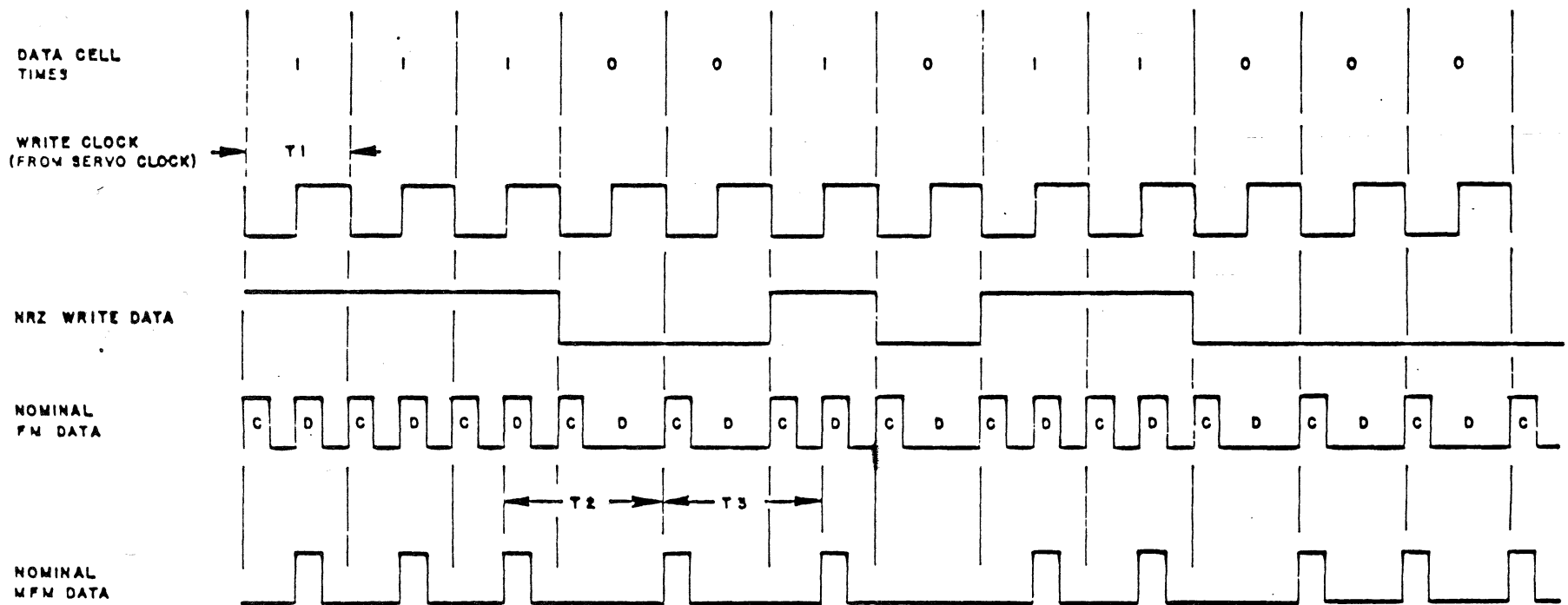
The header is read. If the correct sector is forthcoming "Write Enable" is activated and "Write Data" is written in that sector only. "Read Enable" must be de-activated while "Write Enable" is activated. The switching transition from read to write takes less than the time that it takes to read one byte. Servo offset and data strobe early/late are not allowed during Write. If the Controller-Formatter requests any of these functions during a Write, the "Fault" line is activated.



$TF = 156 \text{ ns} \pm 5.0 \text{ ns}$   
 $TW = TF/2 = 78.0 \text{ ns}$   
 $TCU = \text{INTERFACE CABLE DELAY}$   
 $TCD = TW \pm 38 \text{ ns}$

- NOTES:
1. WRITE DATA AND DATA CLOCK TIMING SHALL BE SPECIFIED AT THE OUTPUT CONNECTOR OF THE CONTROL UNIT.
  2. THE PERMISSIBLE VALUE OF  $TF$  IS  $156 \pm 5 \text{ ns}$  (APPROX.  $\pm 3\%$ ) WHICH INCLUDES THE ROTATIONAL SPEED TOLERANCE.
  3. DIFFERENTIAL NRZ WRITE DATA ISSUED FROM THE CONTROL UNIT IS WRITE-COMPENSATED AND THEN MFM-MODULATED FOR WRITING ON THE DISK SURFACE.

Figure 3-19 Write Clock and Write Data



$T_1$  = DATA CELL PERIOD = 166 Nsec

$T_2$  = ONE TO ZERO = 234 Nsec

$T_3$  = ZERO TO ONE = 234 Nsec

Figure 3-20 Write Data Timing

Write Clock and write data timing are as shown in Figure 3-19.

Figure 3-20 shows the conversion of NRZ data from the Controller-Formatter to MFM. Straight FM is shown for comparison purposes. The top line in Figure 3-20 shows bit-cell times and the value of the bit within each cell. The second line shows write clock pulses which are sent from the Controller-Formatter to the drive (these are generated from the servo clock pulses which the disk unit send to the Controller). The NRZ write data on the third line is in one state for binary 1 and the opposite state for a binary 0. An FM signal would have more flux reversals per bit cell time. Each bit would have a clock pulse followed by the presence (1) or absence (0) of a data pulse. When FM is modified to produce MFM, the need for a clock pulse at the beginning of each data cell, is eliminated.

A convention is adopted wherein binary 1's always have a flux transition in the center of a cell. There is no flux transition in the data cell of a binary zero which was either preceded by or followed by, a binary one. There is a flux transition (at the beginning of the data cell) in the data cell of adjoining binary zeroes.

The write signal will magnetize the surface of the disk in one direction or the other. The points of transition from one direction of magnetization to the other will have bit significance.

The header must be preceded by at least 9-bytes of zeroes to allow time for VFO lock-up before reading the "sync" character which is located at the end of the field of zeroes. The zeroes, sync character and header are supplied by the Controller-Formatter.

Read Enable is activated within one byte time of the leading edge of the Index Pulse. The "read data" which is the header is sent to the Controller-Formatter for comparison. If the header is for the desired sector, Write-Enable is activated in less than one byte time.

#### 10.3.5 READ

A Read operation is begun by executing a Command Word 2 after the drive has been selected and the head carriage has been positioned at the desired cylinder. Figure 3-21 shows typical Read timing. "Read Enable" is activated once for the header and again for the data. "Write Enable" must be held de-activated through-out the Read operation.

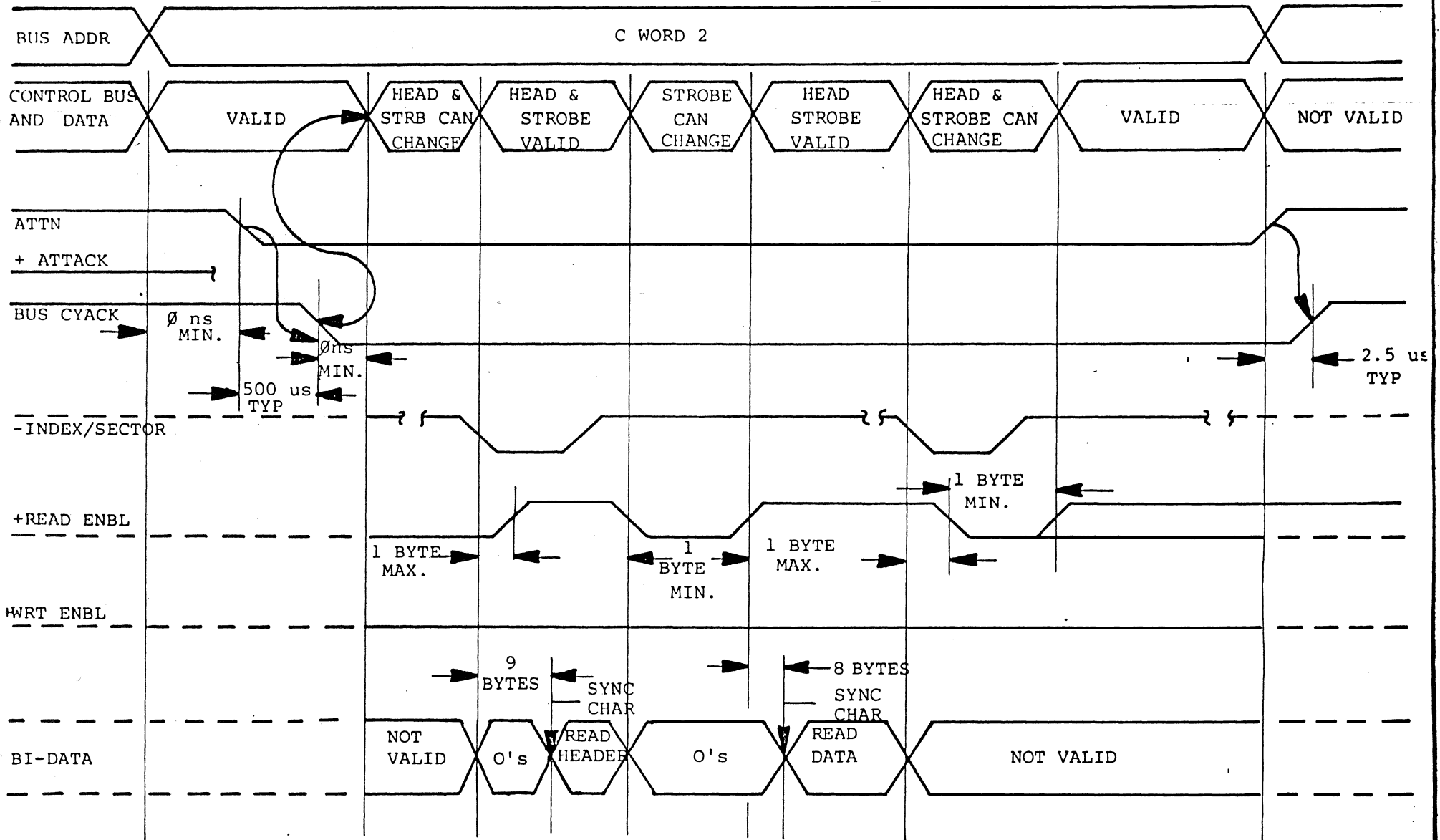
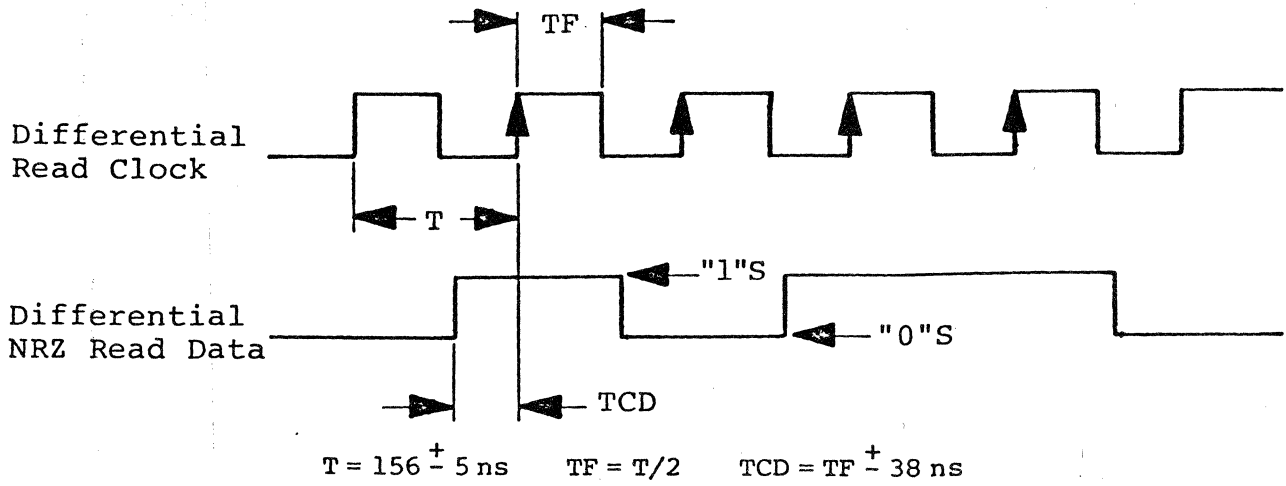


Figure 3-21 Typical Read Timing



- NOTES: 1. READ CLOCK AND READ DATA TIMING SHALL BE SPECIFIED AT THE OUTPUT CONNECTOR OF THE DISK UNIT.
2. READ DATA SIGNAL SHOULD BE CLOCKED AT THE POSITIVE-GOING EDGE OF DIFFERENTIAL READ CLOCK ON THE CONTROL UNIT.

Figure 3-22 Read Clock vs Read Data

During VFD sync time, the data on the "Bi-Data" line is all 0's. Thus, from the moment "Read Enable" is activated until the sync character is encountered (See Subsection 10.2.13) only zeroes are present.

Read clock and read data timing are as shown in Figure 3-22.

#### 10.3.6 READ WITH OFFSET

Read with offset is accomplished when bit 6 or 7 of Command Word 2 is activated. Bit 6 causes forward offset; bit 7 causes reverse offset. Forward and reverse offset are used during read recovery procedures which are activated from the host computer. As soon as it is sensed (from bits 6 or 7) that an offset operation is needed, the "Not On Cylinder" status bit is set and "Seek End" is caused to be reset for 3 ms.

During this time, the heads are positioned 200 micro-inches toward the spindle (forward offset) or 200 micro-inches away from the spindle (reverse offset). "Not On Cylinder" is deactivated and "Seek End" is activated. Read Enable can then be activated (by the Controller-Formatter) to effect the offset read operation. See Figure 3-23.

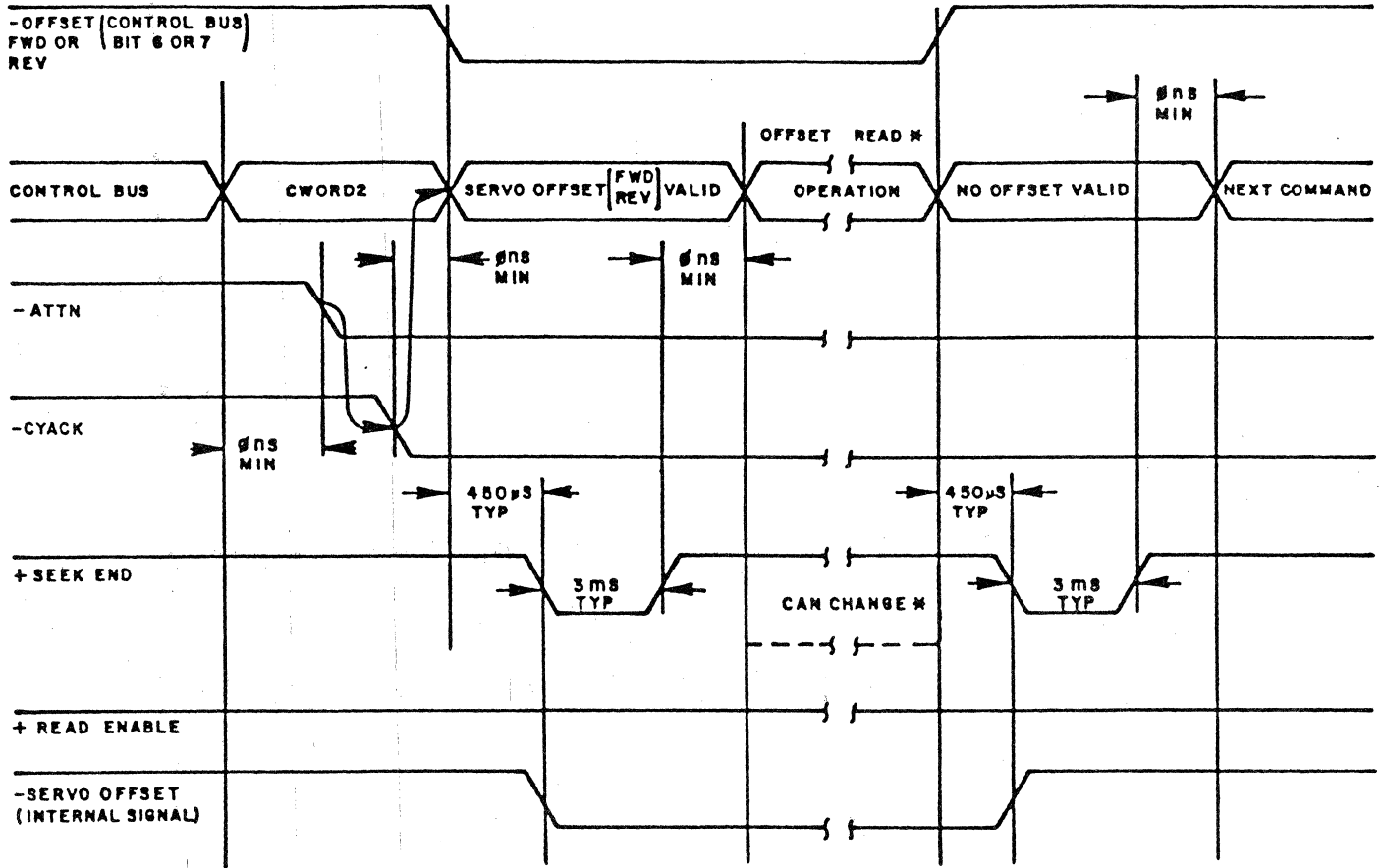
#### 10.3.7 INDEX-TO-SECTOR TIMING

Index-to-sector pulse timing is as shown in Figure 3-24. The index and sector pulses have a 2.5 usec +/-3 % duration. The time between the leading edge of the last sector pulse and the leading edge of the Index pulse is  $T + K$  bytes where  $T$  equals the number of bytes multiplied by 1.249 microseconds.

#### 10.3.8 STATUS WORD TIMING

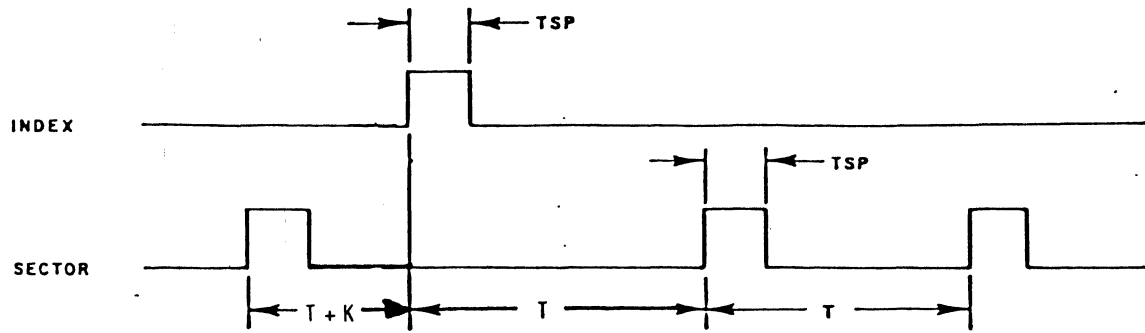
When the "Direction" line is activated, the Control Bus is assumed to contain one of four possible status bytes, as determined by the state of the CWD 0 and CWD 1 bits. Reference should be made to Figure 3-25, which shows how "Attention" must be activated to cause the bus to be sampled...how each drive responds to the "Attention" line causing "ATTACK" to be activated...how 'ATTACK' in turn activates "Cycle Acknowledge" (CYACK)...how CYACK allows time for the bus to be sampled...and how CYACK causes "Attention" to be de-activated...thus deactivating 'ATTACK" and then "CYACK", allowing "Attention" to again be activated.





\* NORMAL READ TIMING APPLIES DURING THIS INTERVAL, HOWEVER WRITE ENABLE IS NOT PERMITTED WHILE A SERVO OFFSET IS ACTIVE. OFFSET REV OR OFFSET FWD MUST REMAIN ACTIVE ON THE CONTROL BUS DURING THE ENTIRE OFFSET READ. OFFSET MUST BE REMOVED AND THE HEADS RETURNED TO THE NORMAL ON TRACK POSITION BEFORE EITHER A SEEK TO ANOTHER CYLINDER, A NORMAL READ, OR AN OPPOSITE OFFSET IS ATTEMPTED.

Figure 3-23 Read With Offset Timing



$TSP = 2.5 \mu S \pm 3\%$

$T = \text{NUMBER OF BYTES} \times 1.249 \mu S/\text{Byte}$

Figure 3-24 Index-to-Sector Pulse Timing

It is recommended that the Controller-Formatter establish the timing shown in Figure 3-25 so that the "sample period" occurs where it is shown on Figure 3-25.

#### 10.4 FUNCTION OF CONTROL BUS COMMANDS AND STATUS

Figure 3-15 showed the eight control words that can be sampled by the selected drive from the Control Bus. This subsection describes the function of each of those control words. A summary of how control words are presented to the drive or Controller-Formatter via the control bus follows. More detail can be found in Paragraph 10.3.2 and 10.3.8, earlier in this section.

**SUMMARY:** All commands and status (control words) transferred over the Disk Bus Interface via "Control Bus" bits 0 through 7 (Note: The "control bus" is a subset of the "disk bus"). Commands are issued as part of four different bytes which are called "Command Word" 0, 1, 2, and 3. Similarly, Status is issued as part of four different bytes which are called "Status Word" 0, 1, 2, and 3. The number of the Command Word or Status Word is determined by the coding of the signals, "CWD 0" and "CWD 1". The fact that the Control Bus contains a Command Word (and not a status word) is determined by the "Direction" line being active. The "Attention" line initiates action within the selected drive for command words; a "Cycle Acknowledge" signal completes the "handshake". The Controller-Formatter must establish its own method for accepting status information from the drive.

##### 10.4.1 COMMAND WORDS

The Control Bus contains a Command Word when the "Direction" line is activated; otherwise, it contains a Status Word (described in Paragraph 10.4.2). The commands (instructions to the drive from the Controller-Formatter) for each of the four possible command words are given below.

###### A. COMMAND WORD 0

Command Word 0 is used to select one of 15 drives; it is also used to establish the state of the high-order bits of the Cylinder Address Register (CAR) in the selected drive prior to a "Seek". Whenever Command Word 0 selects one drive, it de-selects all of the other drives connected to the Controller-Formatter. The actual specifics of selection are: the four-bit unit address (UA) in the Command Word contain the same bit configuration as Unit Select "jumpers" in the "selected" Disk Drive Unit. Figure 3-26 shows the pertinent bits of Command Word 0.

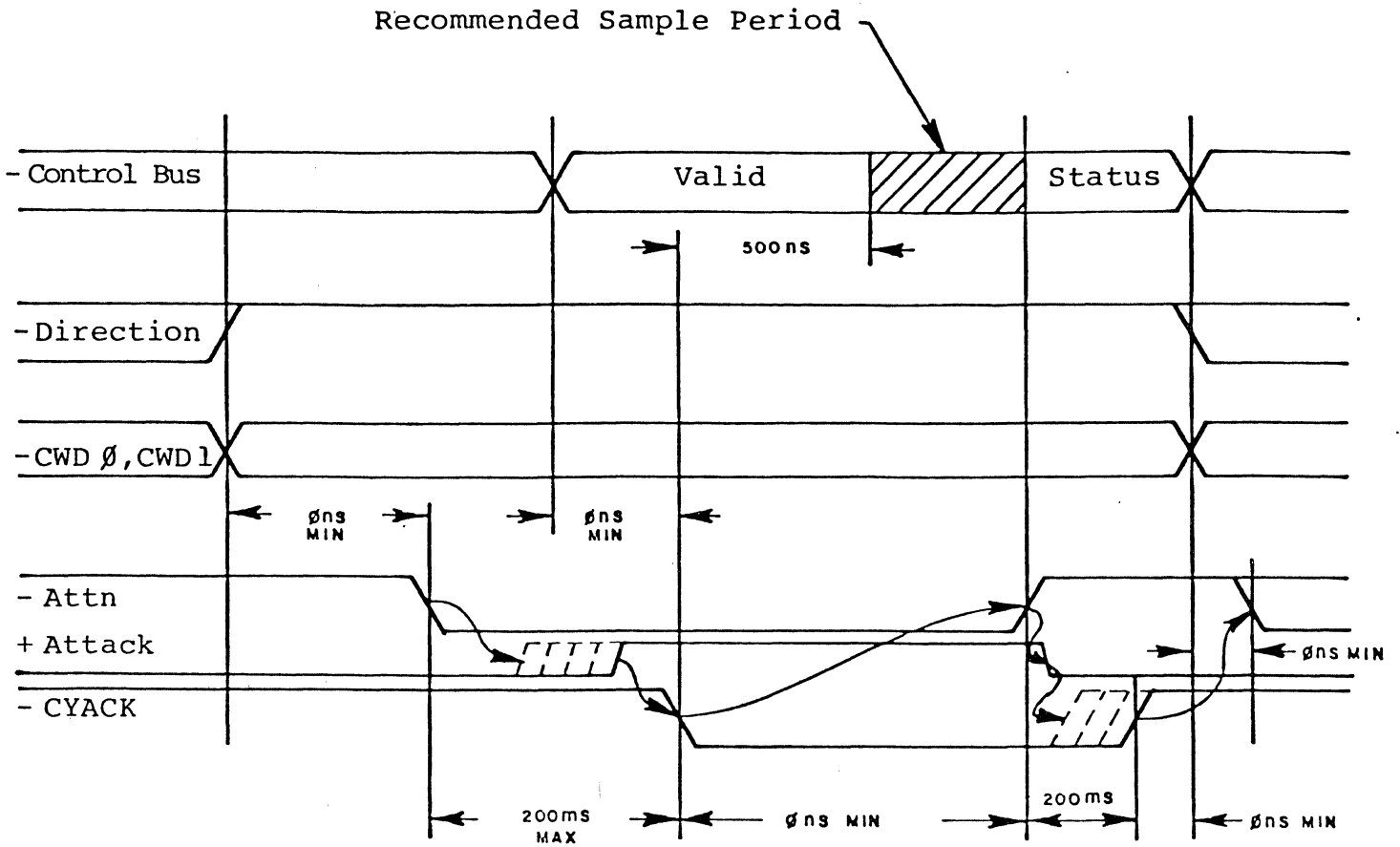


Figure 3-25 Status Word Timing

Bus Control Bits

DIR	CWD1	CWD0
1	0	0

Command Word Bits

7	6	5	4	3	2	1	0
UA 3	UA 2	UA 1	UA 0	0	0	CAR 9	CAR 8

Figure 3-26 Command Word 0

B.    COMMAND WORD 1

Command Word 1 is used in conjunction with the two low-order bits of Command Word 0 to establish the binary address of the desired cylinder. Once the "handshake" (Attention/Sample/Acknowledge) for both Command Word 0 and 1 is completed, the drive will begin a "Seek" to the cylinder specified by the drives CAR (Cylinder Address Register). Figure 3-27 shows the pertinent bits of Command Word 1.

C.    COMMAND WORD 2

Command Word 2 has three basic purposes as listed below:

1.    Select forward or reverse offset
2.    Select early or late data strobe
3.    Select one of five possible heads in preparation for writing or reading

Figure 3-28 shows the bit functions of Command Word 2.

Offset reverse and forward as well as data strobe late and early are used during error recovery procedures. See Paragraph 7.3.2 of Product Specification. The offset amount is 200 microinches; the data strobe variable is 6 ns. Attempts to write during an offset or an early/late strobe result in a "Fault".

HAR 0, 1, and 2 are used to select heads 0 - 4. Once a head has been selected, reading or writing can be initiated using the Write and Read Enable Gates. The way in which the Heads are selected is given below:

	HAR-2	HAR-1	HAR-0
Head 0	0	0	0
Head 1	0	0	1
Head 2	0	1	0
Head 3	0	1	1
Head 4	1	0	0

Bus Control Bits

DIR	CWD1	CWD0
1	0	1

Command Word Bits

7	6	5	4	3	2	1	0
CAR 7	CAR 6	CAR 5	CAR 4	CAR 3	CAR 2	CAR 1	CAR 0

Figure 3-27

Bus Control Bits

DIR	CWD1	CWD0
1	1	0

Command Word Bits

7	6	5	4	3	2	1	0
Offset Rev.	Offset Fwd.	Strobe Late	Strobe Early	0	HAR 2	HAR 1	HAR 0

Figure 3-28 Command Word 2

HAR 0, 1, and 2 are connected directly to the Read-Write PCB; this permits the switching of heads between sectors at TTL logic speeds. The contents of bits 0 - 2 can be changed while Command Word 2 is on the Control Bus provided neither the "Read Enable" or the "Write Enable" gate is active during the head transitions. In the 6172, head 3 is the servo head and is not available for reading or writing. In the 6173 head 5 is the servo head. Any attempt to select the servo head will activate the "Fault" line; in addition, the "Write Protected", "Illegal Address" and "Invalid Command" bits will be set.

#### D. COMMAND WORD 3

Command Word 3 has five basic purposes as listed below:

1. Enter a "Diagnostic Mode" in which the Disk Drive Unit can report its configuration to the Controller-Formatter. Configuration data such as: a) the number of sectors per track; b) Sector size, and; c) number of data heads, and drive model number are reported.
2. Rezero, which causes the carriage assembly to return the heads to cylinder 0.
3. Clear a fault condition by activating the "Fault Clear" line.
4. Establish which heads are to be write protected if they are not already write protected using jumpers on the interface board.

The four purposes of Command Word 3 are further described below:

##### 1. DIAGNOSTIC MODE

The Diagnostic Mode is entered when bit No. 7 of Command Word 3 is on. When in the Diagnostic Mode, the disk drive substitutes four special status words for the four standard status words. Note: Standard Status Words are described in Paragraph 10.4.2.

The Controller-Formatter usually uses the Diagnostic Mode following a power-up sequence. The Diagnostic Mode is maintained until bit number 7 is changed with a subsequent Command Word 3.

The four status words that are substituted for the standard status words during a Diagnostic Mode operation are as given in Figure 3-30.

Bus Control Bits

Dir.	CWD1	CWD0
1	1	1

Command Word Bits

7	6	5	4	3	2	1	0
Diag Mode	CE Mode	Re- Zero	Flt. Clr.	0		Ext. Prot. 1	Ext. Prot. 0

Figure 3-29 Command Word 3



Status Word

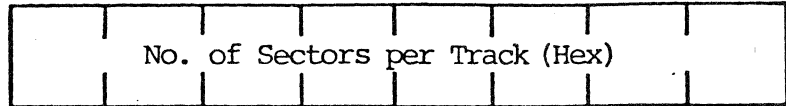
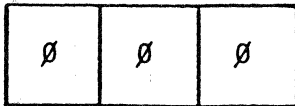
Bus Control Bits

Command Word Bits

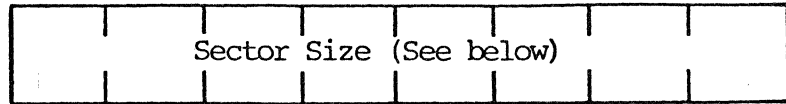
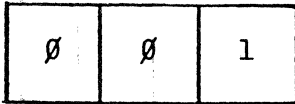
DIR CWD1 CWD0

7 6 5 4 3 2 1 0

0

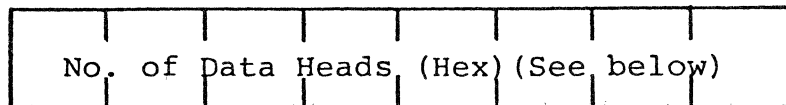
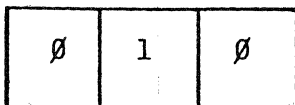


1



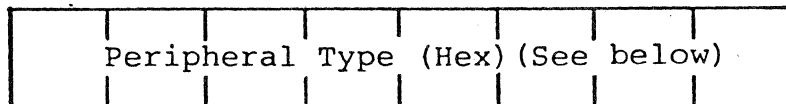
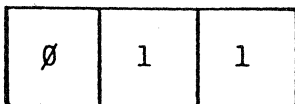
01<sub>H</sub> = 128 Bytes  
 02<sub>H</sub> = 256 Bytes  
 04<sub>H</sub> = 512 Bytes  
 08<sub>H</sub> = 1024 Bytes  
 10<sub>H</sub> = 2048 Bytes  
 20<sub>H</sub> = 4096 Bytes

2



03<sub>H</sub> = 3 Heads (24MB)  
 05<sub>H</sub> = 5 Heads (40MB)

3



00<sub>H</sub> = 6170 Series Fixed Disk Drive

Figure 3-30 Diagnostic Mode Status Words

## 2. REZERO (RETURN-TO-ZERO)

The "Rezero" command is as shown in Figure 3-28 with bit 5 set. The Controller-Formatter issues this command in order to return the heads to cylinder 0 regardless of where they are currently located. The following actions also occur:

- a) "Servo Error" is de-activated
- b) "Seeking/Rezeroing" bit is set
- c) "Not on Cylinder" is set
- d) "Seek End" is de-activated

After the rezeroing has been completed (a maximum of 800 msec), "Seeking/Rezeroing" and "Not on Cylinder" are reset; "Seek End" is activated.

## 3. FAULT CLEAR

The "Fault Clear" command is as shown in Figure 3-29 with bit 4 set. The Controller-Formatter issues this command in order to de-activate the "Fault" line. At the same time, "Read-Write Fault", "Speed Error", and "Power Loss" (standard status bits in Status Word 0) are reset. Also at the same time, "Invalid Command", "Time-Out Error", and "Illegal Address" (standard status bits in Status Word 1) are reset. All micro-processor internal errors are also reset.

## 4. EXTERNAL WRITE PROTECT

The "External Write Protect" commands are as shown in Figure 3-29, earlier in this section. Bits 0, 1, and 2 of Command Word 3 are set to establish which disk heads are write protected. See Figure 3-13, earlier in Subsection 7.2.6, D.

Once set during Command Word 3, the write protect bits remain set in the disk drive and require a subsequent Command Word 3 to change them. Attempts to write using write protected head cause the "Read-Write Fault" status list to be set and the "Fault" line to be activated. Note: External Write Protect commands cannot override "jumpered" write protection.

### 10.4.2 STATUS WORDS

The Control Bus contains a Status Word when the "Direction" line is de-activated; otherwise, it contains a Command Word (described in Paragraph 10.4.1). The status for each of the four possible standard status words are given below:

## A. STATUS WORD 0

Status Word 0 is used to communicate error conditions to the Controller-Formatter when a "Fault" condition exists. Eight different error conditions can be monitored as indicated in Figure 3-31, and as described in 1 through 8, below.

### 1. NOT READY

The "Not Ready" bit is set to inform the Controller-Formatter that the selected drive is "Not Ready" and will only respond to Command Word 0 and Status requests. "Not Ready" is set throughout the power-up sequence; it remains set until sufficient time has been allowed for the disk drive to come up to speed. "Not Ready" is also set if "Power Loss" or "Speed Error" are detected while the drive is operating.

### 2. SERVO ERROR

The "Servo Error" bit is set to inform the Controller-Formatter that a servo error has been detected in the selected drive as evidenced by one of the following seven occurrences:

- a) "Seek End" not active within 200 ms after the initiation of a seek operation.
- b) "Seek End" not active within 800 ms after the initiation of a Rezero command.
- c) "Fine Track" lost while the servo is in the linear (track-following) mode.
- d) Guard band detected during a seek operation.
- e) PLD (Phase-locked oscillator) error detected.
- f) Speed error detected.
- g) Illegal cylinder address sent during Command Word 0 and 1.

"Servo Error" can only be reset by the Controller-Formatter with a Rezero Command. While "Servo Error" is set, the drive will only respond to Command Words 0 and 3 and to Status Word requests.

Bus Control Bits

DIR	CWD $\emptyset$	CWD1
$\emptyset$	$\emptyset$	$\emptyset$

Status Word Bits

7	6	5	4	3	2	1	$\emptyset$
Not Ready	Servo Error	R/W Fault	Speed Error	Power Loss	Write Prot'd	Seek Re-Zero	Not on Cyl.

Figure 3-31 Status Word  $\emptyset$

Bus Control Bits

DIR	CWD1	CWD $\emptyset$
$\emptyset$	$\emptyset$	1

Status Word Bits

7	6	5	4	3	2	1	$\emptyset$
Guard Band	PLO Error	Un-Safe	Inval. Comnd	Time Out	POR/MR	Spare	Ill. Addr.

Figure 3-32 Status Word 1

### 3. READ-WRITE FAULT

The "Read-Write Fault" bit is set to inform the Controller-Formatter that an error has been detected during a Read or Write command or a condition has occurred in the drive that could cause a loss of data. The "Fault" line is also activated. The two conditions which can cause a read-write "Fault" are:

- a) "Unsafe" received from the Read-Write PCB.
- b) "Write Enable" activated when any of the following bits are set:
  - 1) Write Protected (Status Word)
  - 2) Not on Cylinder (Status Word)
  - 3) PLD Error (Status Word)
  - 4) Speed Error (Status Word)
  - 5) Illegal Address (Status Word)
  - 6) Servo Error (Status Word)
  - 7) Offset Forward or Reverse (Command Word 2)

### 4. SPEED ERROR

A speed error is indicated via bit 4 of Status Word 0, whenever a) the sequence timer has timed-out, and b) the motor speed is more than 3 percent below the rated rpm's for the drive motor. A "Speed Error" also causes the "Not Ready" bit to be set and the "Fault" line to be activated. The drive remains not ready until the proper speed is attained and a "Fault Clear" command is executed.

### 5. POWER LOSS

Any loss of DC power on the +/-5V or the +/-12V DC power supply lines, below 10 percent of nominal, sets the "Power Loss" bit. If the DC loss continues for more than 50 msec., the Power-On Reset (POR)/Master Reset bit will be set; the Fault line is activated.

### 6. WRITE PROTECTED

Write Protected is signaled via Status Word 0 bit 2 whenever a head is selected which is write protected, either by a previous Controller-Formatter command, or by internal jumpers.

Bus Control Bits

Status Word Bits

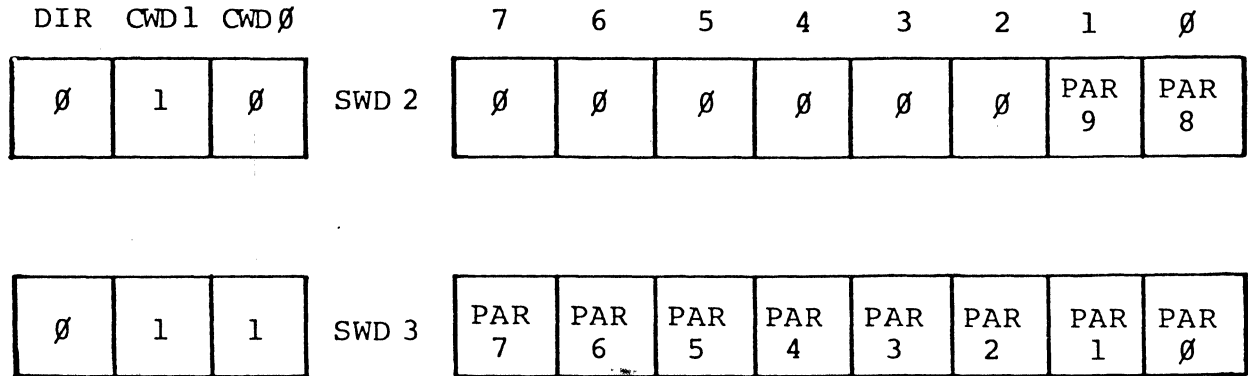


Figure 3-33 Status Words 2 and 3

## 7. SEEKING/REZEROING

Bit 1 of Status Word 0 is set to 1 during the execution of a Rezero Command; it is reset to 0 during a normal seek. The state of the bit is only valid while the "Seek End" line is de-activated; it has no meaning while "Seek End" is activated.

## 8. NOT ON CYLINDER

Bit 0 of Status Word 0 is set to 1 whenever a) the head-carriage is moving from one track to another; b) the servo is off track while in the linear mode (track following); or c) an Offset operation is in effect.

## B. STATUS WORD 1

Status Word 1 contains seven different error/exception conditions that are signaled to the Controller-Formatter. See Figure 3-32 and the descriptions which follow.

### 1. GUARD BAND DETECTED

The "Guard Band" status bit is set whenever the inner or outer guard band is detected by the guard-band detection circuitry. It remains set until reset by Re-zero command.

### 2. PLO ERROR

The "PLO Error" status bit is set if the PLO in the circuitry "unlocks". The "Fault" line is activated at the same time.

### 3. UNSAFE

The "Unsafe" status bit, bit 5, is set when an unsafe condition is detected in the Read-Write electronics. The "Fault" line is activated as is the Read/Write Status bit.

SYNC FIELD		HEADER FIELD				SPLICE
PLO SYNC	SYNC CHARACTER	CYLINDER ADDRESS	HEAD ADDRESS	SECTOR ADDRESS	CRC	READ/WRITE SPLICE
S1	S2	H1-2	H3	H4		SPI
8 BYTES	1 BYTE	2 BYTES	1 BYTE	1 BYTE	2 BYTES	1 BYTE

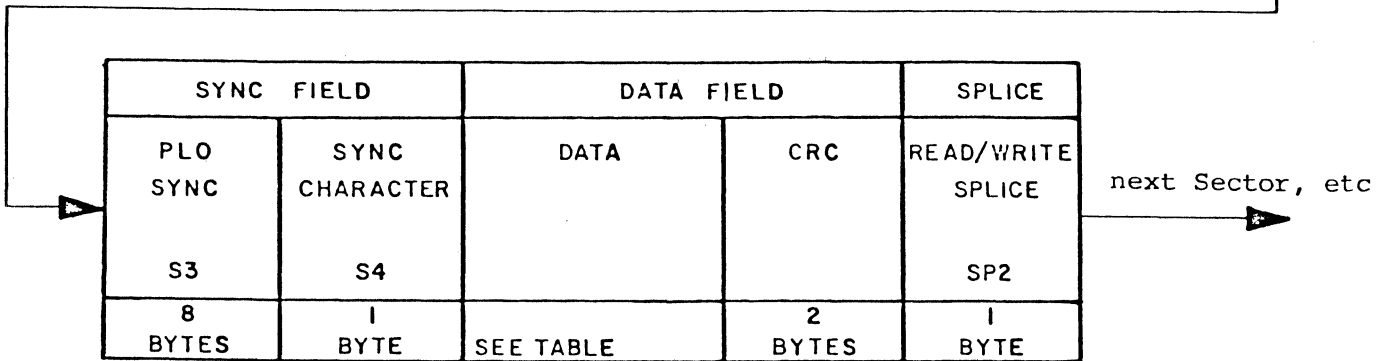


Figure 3-34 Sector Format With 28-Byte Overhead



#### 4. INVALID COMMAND

"Invalid Command" status bit 4 is set when an illegal command is passed to the drive on the Control Bus at "Attention" time. Some examples of illegal commands are given below:

- a) Command Word 1 during A Seek
- b) Read Enable and Write Enable active at the same time
- c) Illegal Head Address
- d) Early or Late Strobe active with Write Enable
- e) Control Bus changing before Cycle Acknowledge is returned

#### 5. TIME-OUT

"Time-Out" status bit 3 is set whenever the Disk Drive Unit is unable to complete either one of the below listed functions in the specified time.

<u>FUNCTION</u>	<u>SPECIFIED TIME</u>
Motor Start-up	20 seconds
Seek	200 ms
Rezero	800 ms

#### 6. POR/MR

"Power on Reset/Master Reset" is set a) when power is initially applied to the system, and b) when the Master Reset line is activated and the initialize routine is executed. During the initialization routine, a 15-second timer is started; all registers and status bits are reset. "Fault" is active throughout this time. If loss of power for greater than 50 msec. is detected, POR/MR is set along with "Power Loss"; the initialization routine is started. At the completion of the 15-second POR time-out, "Fault" is cleared and a Rezero is initiated, provided the disk drive motor is up to speed.

BOR	SYNC FIELD		HEADER FIELD				
BEGINNING OF RECORD	PLO SYNC	SYNC CHARACTER	FLAG AND UNIT	CYLINDER ADDRESS	HEAD ADDRESS	SECTOR ADDRESS	CRC
	S1	S2	H1	H2-H3	H4	H5	CRC 1
(m) BYTES	11 BYTES	1 BYTE	1 BYTE	2 BYTES	1 BYTE	1 BYTE	2 BYTES

SPLICE	SYNC FIELD		DATA FIELD		SPLICE	EOR
READ/WRITE SPLICE	PLO SYNC	SYNC CHARACTER	DATA	CRC	READ/WRITE SPLICE	END OF RECORD EOR
SPI	S3	S4		CRC 2	SP2	
1 BYTE	11 BYTES	1 BYTE	SEE TABLE	2 BYTES	1 BYTE	(n) BYTES

NEXT SECTOR

Figure 3-35 Sector Format With 44-Byte Overhead

## 7. ILLEGAL ADDRESS

"Illegal Address" bit 0 is set whenever the cylinder address that is transferred to the drive exceeds 613. A "Seek" is inhibited; the "Fault" line is activated.

"Illegal Address" is also set if a nonexistent data head is "selected". "Illegal Address" is reset using a "Fault Clear" command.

## C. STATUS WORDS 2 AND 3

Status Words 2 and 3 together contain the contents of the Position Address Register (PAR). The Position Address Register contains the current location of the heads at all times. It is cleared only during a power-up sequence and during a Rezero Operation. Figure 3-33 shows the PAR contents of Status Words 2 and 3.

## 10.5 SECTOR FORMATS

Three different types of format are available on the Disk Bus Interface PCB. They vary depending upon the number of bytes that are allocated to Sector overhead. Sector overheads of 28, 36, and 44 bytes are available. The user can select one of the three overhead sizes using jumpers as shown in Figure 3-9, earlier in this section. The overhead size that the user selects will depend on the speed of the switching circuitry in the Controller-Formatter and in other elements of the host system. Systems which include high-speed circuitry may opt for the 28-byte overhead. Slower systems may choose the 36-byte or the 44-byte overhead.

### 10.5.1 28-BYTE OVERHEAD FORMAT

The sector format which 28-bytes of overhead is shown in Figure 3-34. Quick review of Figure 3-34 will show that a sector consists of two basic fields: a "header" field and a "data" field. Both the header and the data fields are preceded by a "sync" field and followed by a "read/write splice".

The "sync" field consists of eight bytes of zeroes which are needed to synchronize the phase-locked oscillator (PLO) in the read/write circuitry. The PLO must be "locked-up" prior to encountering the sync character. The sync character is a "Hex 19". It serves as a "flag" that signals the beginning of the header is about to be encountered.

The "header" consists of a two-byte cylinder address, a one-byte head address, a one-byte sector address, and two bytes to be used for a check character. The check character could be a parity check...a cyclic redundancy check (CRC)...or an error detect/correct code (ECC). The user has the option of choosing and implementing the error detection and correction system. The data error rates given in Section 2 assume that at a minimum, a CRC checking system is used.

The Header Field is followed by a read/write "splice". The splice is a one-byte area which allows the electronics to "switch" when making the transition from read to write during a write operation. Next (referring to Figure 3-34) the sync field which precedes the field is encountered. It is the same as the sync field which preceded the header field and it serves the same purpose. The data field may contain from 128 to 4096 bytes of data; the number of bytes of data in a sector is determined by the position of jumpers on the Disk Bus Interface PCB as shown earlier in Figure 3-11.

10.5.2 36-BYTE OVERHEAD FORMAT - To be specified.

#### 10.5.3 44-BYTE OVERHEAD FORMAT

The number of sectors per track, the number of bytes per sector, and the number of bytes per track for the 44-byte overhead was shown earlier in this section in Figure 3-11. Figure 3-35, below, shows the relationship of overhead to data in the 44-byte format. An explanation of the various elements of the overhead and data follows the figure.

Each sector contains a Beginning of Record (BOR) and an End of Record (EOR) field to add to the time between sectors when reading. It is suggested that  $m$  (the number of bytes in BOR) and  $n$  (the number of bytes in EOR) total to equal 9. The contents of BOR and EOR are the user's choice. The PLO sync field must be zeroes. Actually, only 8 bytes of zeroes are needed by the PLO; eleven are suggested in this format.

The header field is the same as in the 28-byte overhead format, below, with one exception. A byte is added to the header to be used as desired by the user. It would contain a flag bit to indicate unit status to the host; or, it could be used to indicate the unit's I.D. No. to the host operating system. The remaining elements of the overhead are as described in the 28-byte format. There is a 2-byte cylinder address, a 1-byte head address, a 1-byte sector address and room for a 2-byte check/correct character.

A one-byte read/write "splice" separates the header field from the sync field for the data field. The number of bytes in the data field is established by jumpers as shown in Figure 3-11. It is between 128 and 4096 bytes, depending upon the state of the four-switch assembly.

## 10.6 POWER LINES

DC power for operating the drive is furnished by the user. One DC power cable must be fabricated for each drive as described in Paragraph 3.2.2 of this manual. Figure 3-36 shows the voltages or grounds expected at the pin numbers of Jack JP on the Disk Bus Interface PCB. Note the "caution" on Figure 3-36 regarding user's choice of frame ground versus DC ground.

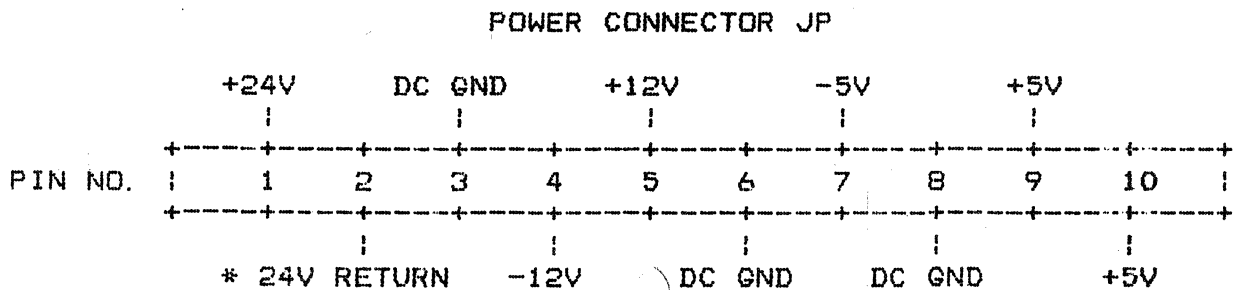


FIGURE 3-36

**CAUTION:** Frame Ground is jumpered to DC Ground at the factory. If separate Frame Ground is required, remove the jumper between the pads marked "DC Ground" and "Frame Ground" on the component side of the interface PCBA next to the power connector.

## 11 ANSI DISK DRIVE INTERFACE

This specification describes the interface between 1) the ANSI Interface PCB on the Disk Drive Unit which is described in Section 1 of this specification and 2) a Controller-Formatter which is part of the host system and designed to control a drive which has an "ANSI" interface.

### 11.1 KENNEDY ANSI INTERFACE

The ANSI disk drive interface standard allows to the vendor the choice of how to implement a number of details.

This specification describes the KENNEDY unique implementation of the ANSI standard.

The KENNEDY ANSI Interface is implemented in such a way that a host is able to operate the drive with the mandatory command set only. However, a number of optional commands and KENNEDY unique commands are available to increase the degree of comfort and flexibility.

### 11.2 KENNEDY ANSI Drive Power Requirements

#### 11.2.1 DC Voltages and Currents

##### Operating Current

DC Voltage	Static	Maximum	Max. Ripple p_p
+5V +/-5%	1.6 A	2.0 A	50 millivolts
-5V +/-5%	1.6 A	2.0 A	50 millivolts
+12V +/-5%	0.3 A	0.5 A	100 millivolts
-12V +/-5%	0.23 A	0.5 A	100 millivolts
+24V +/-10%	1.9 A	5.0 A *	250 millivolts

- \* Surge current during spin up cycle (approx. 15 seconds)  
 The peak operating current is 4.2 A.  
 The 24 V current step rate is 2 A/millisecond.

The operating power is : 68 Watts static  
91.6 Watts at random seek  
142 Watts during spin up

The voltages are defined at the power connector of the Interface board.

11.2.2 Power Connector Pin Assignments

The power connector on the KENNEDY ANSI is AMP 1-640389-0 or equivalent.

DC Voltage JP Connector Pin

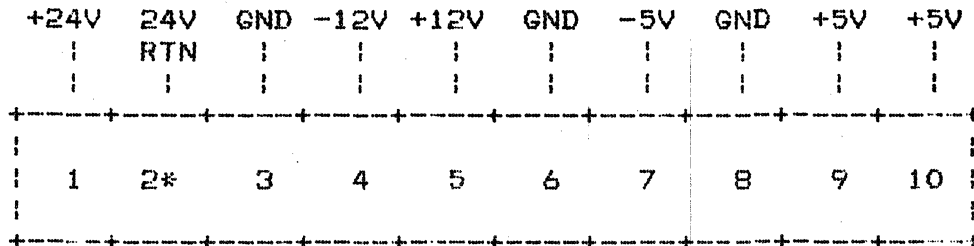
+24 V	1
24 V RTN	2
GND	3
-12 V	4
+12 V	5
GND	6
-5 V	7
GND	8
+5 V	9
+5 V	10

The recommended power cable connector is AMP Part No. 1-640599-0 or equivalent.

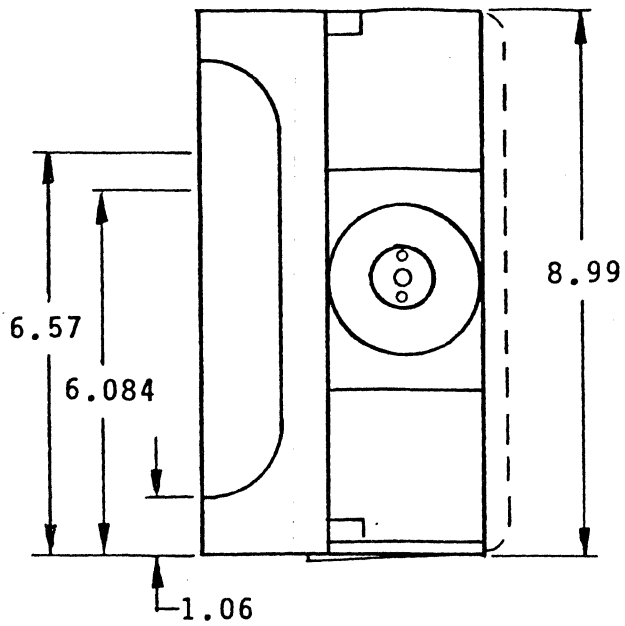
The recommended wire size is AWG 18 (0.82 square mm).

Figure 4-1

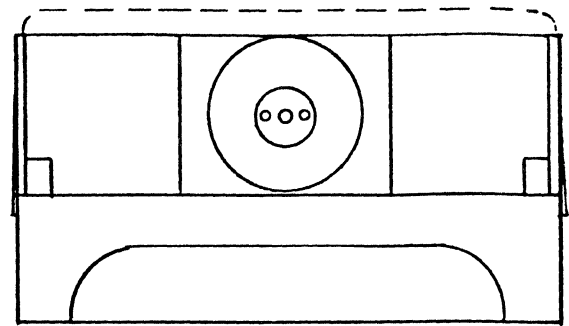
Power Connector (Top View)



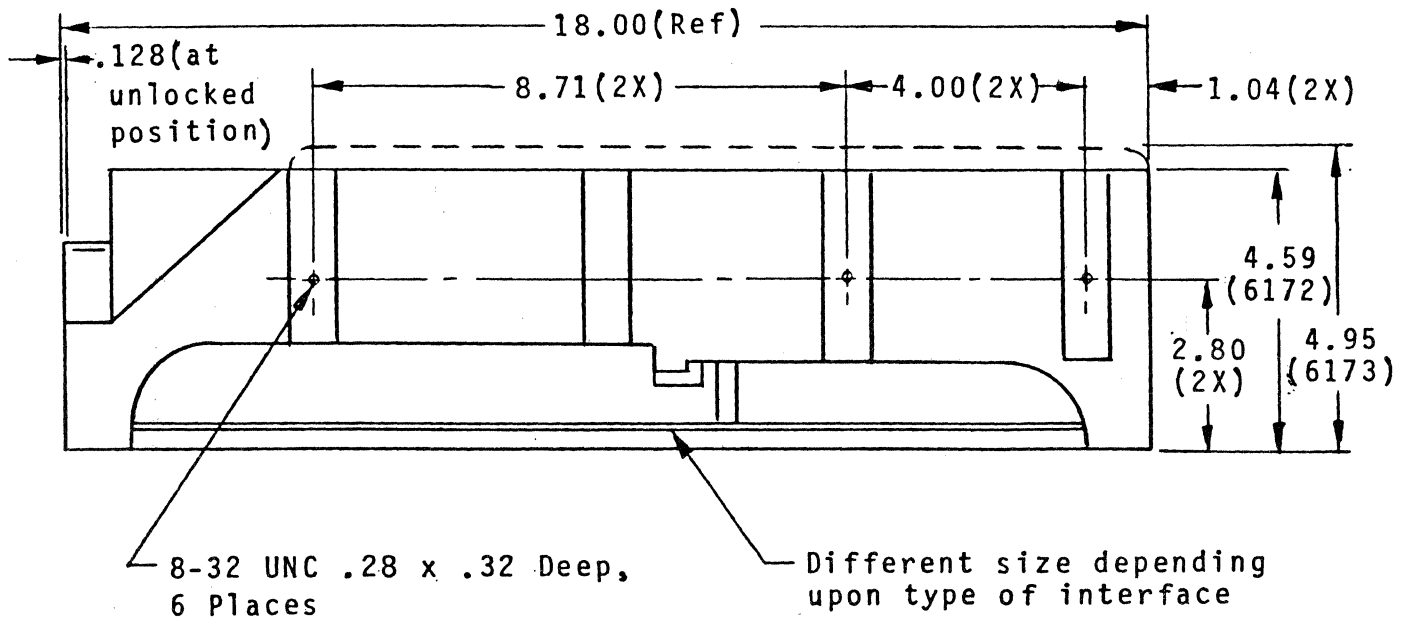
\* There is a jumper on the ANSI board to connect this pin to pin 3 of the power connector (see Figure 4-3).



Vertical Mounting Position.



Horizontal Mounting Position

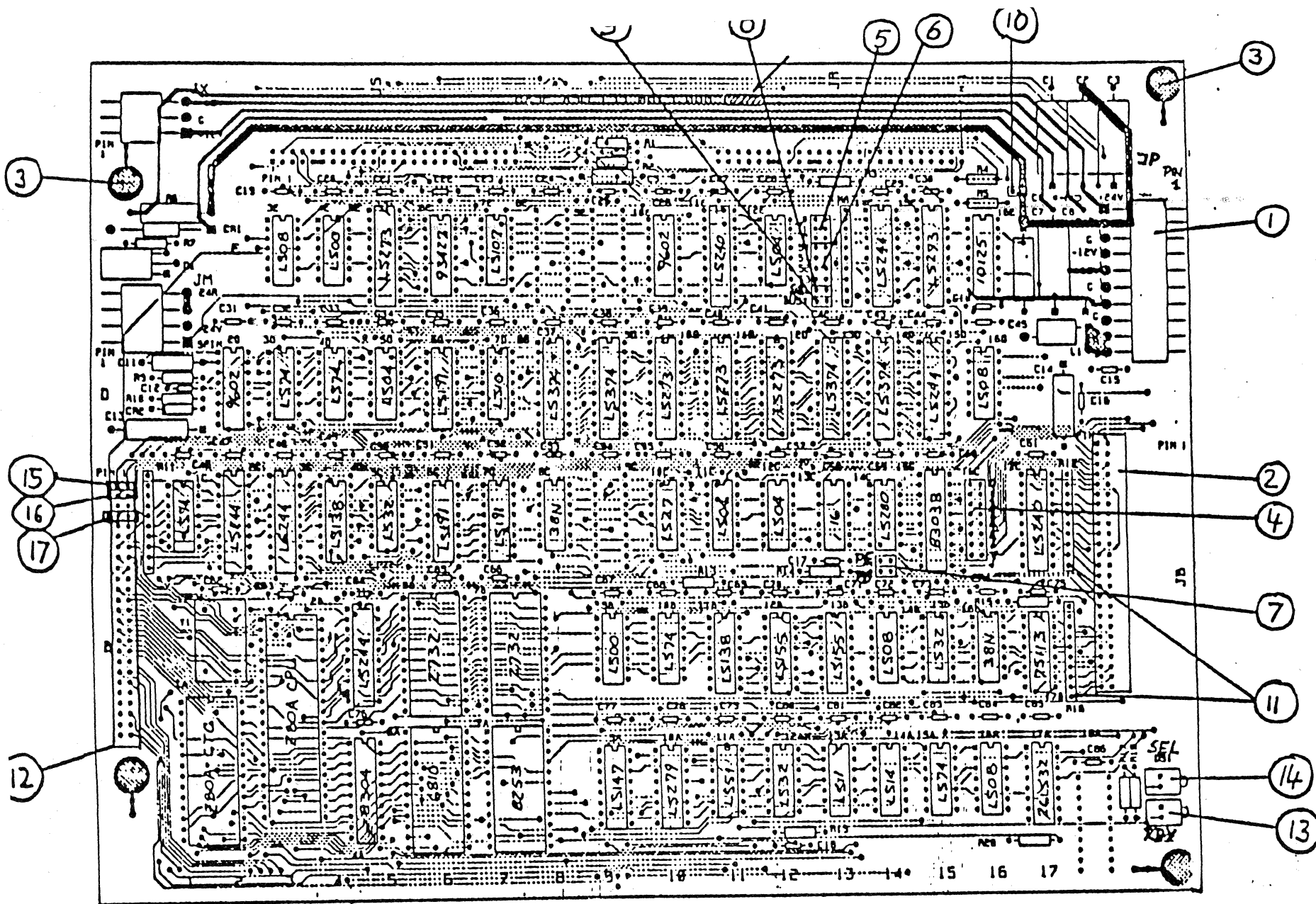


Notes: Unless Otherwise Specified

1. Maximum screw insertion: .25.  
Maximum torque: 6 in. Lbs.
2. Dimensions in inches.

Figure 4-2 Physical Interface





- |   |                            |    |                      |
|---|----------------------------|----|----------------------|
| 1 | Power Connector            | 10 | 24 V-Return JUMPER   |
| 2 | Interface Connector        | 11 | Terminators          |
| 3 | External Grounding Point   | 12 | Test Connector       |
| 4 | Drive Select JUMPERS       | 13 | Ready Indicator      |
| 5 | Model Select JUMPERS       | 14 | Selected Indicator   |
| 6 | Sector Size Select JUMPERS | 15 | Select LED JUMPER    |
| 7 | Parity Check JUMPERS       | 16 | Ready LED JUMPER     |
| 8 | Spin Control JUMPER        | 17 | Write Protect JUMPER |
| 9 | Seek Busy JUMPER           |    |                      |

Figure 4-3

### 11.2.3 Grounding

For separate grounding all mounting holes of the interface board are padded and connected to DC ground.

If additional grounding is required, separate ground lines of sufficient size shall be connected from each drive to a central grounding point.

### 11.3 Mechanical Configuration

Figure 4-2 shows the physical interface of the KENNEDY 6170 series disk drives.

Figure 4-3 shows the outline of the ANSI printed circuit board, the locations of the connectors, the locations of the jumpers, the locations of the terminators, and the locations of the indicators.

### 11.4 JUMPER OPTIONS

#### 11.4.1 Description of Jumpers

There are a number of jumpers on the ANSI interface PCBA. For the location of these jumpers see Figure 4-3.

To ensure proper operation of the drive, the jumpers shall be installed or removed prior to applying DC power to the drive.

#### 11.4.2 Drive Select Jumpers

There are 8 locations for jumpers labelled (A0...A7). In one and only one of these locations a jumper must be installed to identify the logical number of the drive in the daisy chain.

For each drive a different jumper number has to be installed according to its logical number. If more than one jumper is installed to the same logical number in the drives on a daisy chain or no jumper is installed in a drive or more than one jumper is installed in one drive, malfunction of the select/attention mechanism will occur.

#### 11.4.3 Control Bus Parity Checking Jumper

In one of the locations PE (parity enable) or PD (parity disable) a jumper must be installed to enable or disable the Control Bus Parity checking. The generation of Control Bus Parity in the drive shall not be affected by this jumper.

#### 11.4.4 Model Select Jumpers

There are three jumpers to identify the specific KENNEDY 6170 model, labelled (M0...M2).

They have to be set in the following way:

Jumpers	Model	
	6172	6173
M0	-	*
M1	*	-
M2	*	*

\* indicates jumper installed, - indicates jumper missing. Further combinations are reserved for future use.

#### 11.4.5 Spin Control Jumper

There is a jumper labelled (SC) to select the spin up mode. Without this jumper the spindle motor shall spin up or down whenever power is applied to or removed from the drive. In this case the Spin Control Command (see Section 11.8.1.2.5) is illegal. If the jumper is installed, the Spin Control Command shall affect the spindle motor.

The state of this jumper is available to the host in the Model ID High Attribute (see Section 11.8.3.2).

Note: Current Models 6172 and 6173 do not allow Spin Control.

#### 11.4.6 Sector Size Jumpers

There are four jumpers labelled (S0...S3) to select the default size and number of sectors.

See Sections 11.8.3.9 and 11.8.3.10 and Table 4-6 for the function of these jumpers.

The state of these jumpers is available to the host in the Model ID High Attribute (see Section 11.8.3.2). A one bit indicates a missing jumper.

#### 11.4.7 Seek Busy Jumper

The Seek Busy Jumper labelled (BY) will change the operation of the Busy Signal.

Normally the KENNEDY ANSI Interface does not make the Busy Signal active during a Seek Command. If for compatibility reasons the Busy Line must be active during a seek operation, the Jumper 'BY' has to be installed.

The state of this jumper is available to the host in the Model ID High Attribute (see Section 11.8.3.2). If Bit 7 is set, then the jumper is missing.

#### 11.4.8 24 V - Ground Jumper

In cases where no separate return line is supplied for the +24 Volts (pin 2 of the power connector), the 'RT' - jumper connects pin 2 to pin 4 of the power connector.

Note: In the current design the 24 V Return is connected to Ground on the Servo Board.

#### 11.4.9 LED Jumpers and Write Protect Jumper

The LED Jumpers connect the drivers for the Ready LED and the Selected LED to the LED's on the ANSI Interface Board.

The Write Protect Jumper allows protection against writing.

See Section 11.5 for the installation of these jumpers.

### 11.5 Operator Controls and Displays

For the operation of the Series 6170 disk drive no operator intervention or display is required. Users may, at their option, apply the following control and displays.

There are two light emitting diodes on the ANSI Interface board to display the Ready State (regardless of selection) and the Selected State.

The LEDs and their drivers (SN 7438) are connected to the Test Connector (see Fig. 4-3). If there are jumpers from pin 1 to pin 2 and from pin 3 to pin 4 of this connector, the on-board LEDs are operating. It is possible to connect external indicators with a maximum current of 48 milliamps each. For this purpose + 5 V is brought to pin 6 of the Test Connector.

The Test Connector also provides an input for an external write protect switch. The write protection is enabled by a jumper from pin 7 to pin 8. This write protection affects the hardware directly (as opposed to the Write Control Command, which performs a software controlled write protect).

Fig. 4-4 shows the assignment of signals for external controls and indicators to the pins of the connector. Other pins of this connector must not be connected. They are intended for diagnostic purposes.

The Test Connector is a 50 pin dual inline header with vertical pins, spaced 0.1 inch.

Figure 4-4  
Pin Assignment of the Test Connector

Pin	Signal
1	-SELECTED DRIVER
2	SELECTED LED
3	-READY DRIVER
4	READY LED
5	not connected
6	+5V (96 milliamps max.)
7	-WRITE PROTECT SWITCH
8	GND

## 11.6 General Interface Description

### 11.6.1 Definitions - State Nomenclature

The nomenclature used to define voltage levels and signal states on the interface and to define logical states internally to the drive and their correlation is defined in Table 4-1.

Table 4-1  
State Nomenclature

Interface		Internal			
Voltage Level	Signal State	Logical State		Logical Transition	
		Tables	Text		
Single Ended	Differential				
"LOW"	+ line >= - line	Active	1	one	Set= x to one
"HIGH"	- line > + line	Inactive	0	zero	Reset= x to zero

### 11.6.2 Physical Characteristics

Unless otherwise indicated, all values are specified with a plus or minus five percent tolerance.

### 11.6.3 Cabling Configuration

The disk drives shall be connected to a host by means of a 50 conductor flat ribbon or equivalent cable. Three meters (3 m) is the maximum length of the interface cable. Note that the cumulative length of the cable in a daisy chain string shall not exceed three meters. See Figure 4-5.

When shipped, all drives have terminator networks installed. These networks (see Figure 4-3) shall be removed in all but the last (or only) drive.

Note: To make the termination operable, the last drive on the daisy chain must have DC power applied (see Figures 4-6 and 4-7).

For DC power connection see Paragraph 11.2.2

For additional ground connections see Sections 11.2.3 and 11.4.8.

#### 11.6.3.1 Interface Connector Specification

The connector type shall be a 50 pin two row, inline flat ribbon connector (AMP Part Number 1-102160-0 or equivalent).

Pin assignments and signal nomenclature are illustrated in Table 4-2. Termination of the individual cable lines shall be at the host and at the last drive according to the electrical requirements of Section 11.6.4.

The cable plug shall be polarized and polarization shall be done with a center top tab. The recommended cable plug is AMP Part Number 88610-B Kit (consisting of Housing P/N 88608-4 and Strain Relief P/N 88340-4) or equivalent.

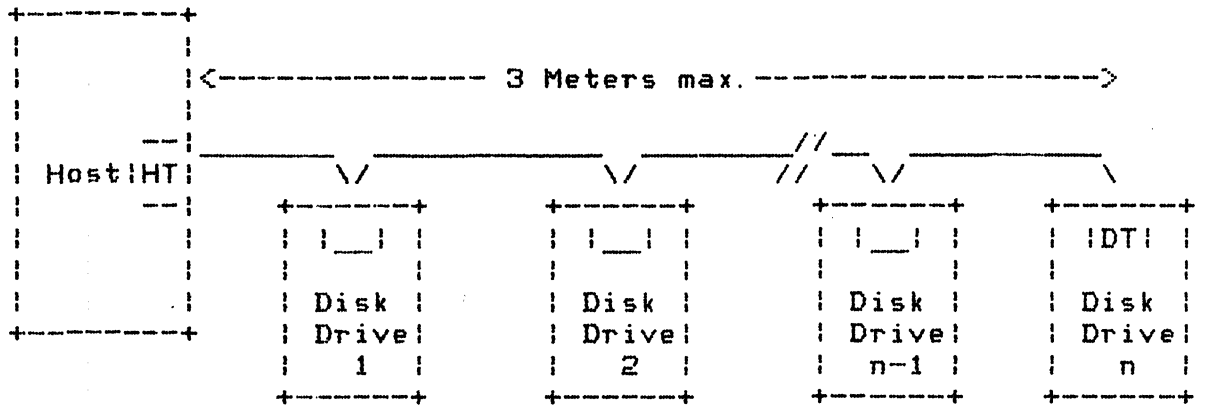
#### 11.6.3.2 Cable Characteristics

The flat ribbon or equivalent cable shall consist of 50 conductors of 28 AWG. The characteristic impedance of the lines shall be 100 ohms plus or minus 10%. Conductor spacing shall be 1.27 millimeters (0.050 inches) center to center to provide for mechanical termination. Additionally, the flat ribbon cable shall be marked in such a way as to identify line number one (pin 1).

If the cable contains a shield ground it shall be connected to pin number one of the interface connector.

The cable shall not be twisted pair.

Figure 4-5  
Interface Configuration



The maximum number of drives connected to one daisy chain cable shall be eight.

HT = Terminator installed at the host

DT = Terminator installed at the last drive only. Remove terminators in other drives (see Figure 4-3)

11.6.4 Electrical Characteristics

11.6.4.1 Bidirectional Control Bus Lines

The bidirectional Control Bus is used in two different modes:

Daisy Chain Mode and Radial Mode

In the Daisy Chain Mode eight bits of information and an optional parity bit shall be transferred between the host and the selected drive.

In Radial Mode each of the eight Control Bus lines shall be used separately for communication with one specific drive. In this way, one bit of information is transferred to or from all drives simultaneously. Each drive shall have a jumper to connect the radial signal to any one of the eight Control Bus lines. The parity bit shall not be used in the Radial Mode. The configuration of the bidirectional Control Bus lines is shown in Figure 4-6.



#### 11.6.4.2 Control Bus Drivers

The bus drivers for the parallel information shall be either three-state or open collector. Three-state drivers are used in the drive. The driver for the radial signal in the drive shall be open collector.

All bus driver outputs for "LOW" level shall sink 24 milliamps minimum. The "LOW" level output voltage shall be 0.5 volt maximum. Driver outputs for "HIGH" level shall source 5 milliamps minimum and shall have a "HIGH" level output voltage of 2.4 volts minimum, 5.25 volts maximum. A 10 milliamps source current is provided by the 470 ohms terminator discussed in Section 11.6.4.4.

The leakage current in the high impedance state ("OFF" state for open collector) shall not exceed 0.25 milliamp for either "HIGH" or "LOW" level on the Control Bus.

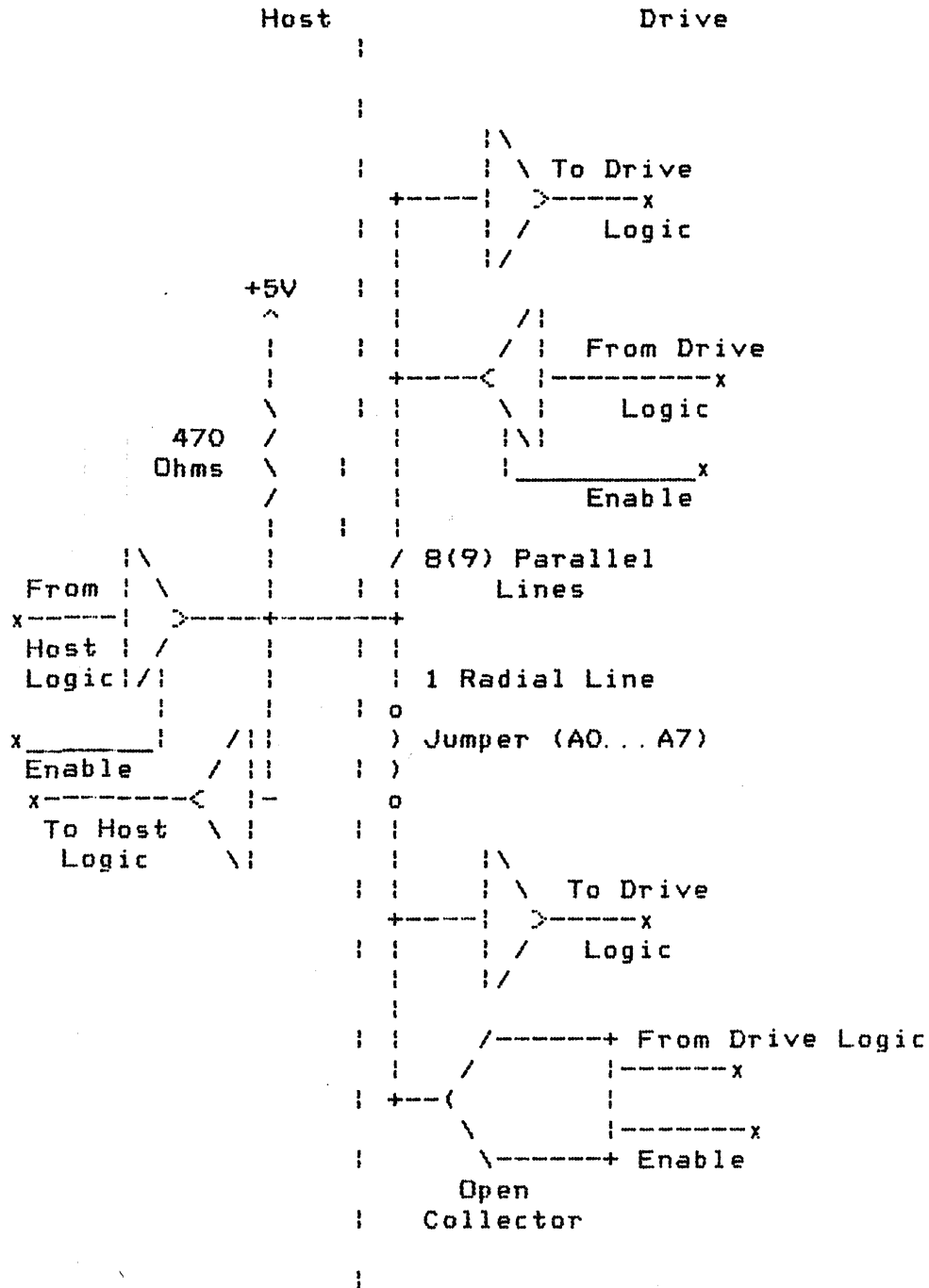
The total number of drivers connected to any Control Bus line shall not exceed ten (one in the host, one in each of the eight drives for the parallel information, and one in a single drive for the radial signal).

#### 11.6.4.3 Control Bus Receivers

The maximum "LOW" level input current shall be 400 microamps. The maximum "HIGH" level input current shall be 80 microamps. The maximum "LOW" level input voltage shall be 0.9 volts. The minimum "HIGH" level input voltage shall be 2.0 volts.

The total number of receivers connected to any Control Bus line shall not exceed ten (one in the host, one in each of the eight drives for the parallel information, and one in a single drive for the radial signal).

Figure 4-6  
Cable Configuration for Bidirectional Control Bus Lines



#### 11.6.4.4 Control Bus Termination

A 470 ohms resistor, plus or minus 10% shall be installed at the host end of all Control Bus lines (Bus Bits 0-7 and Bus Parity), connected to +5 volts plus or minus 5%.

#### 11.6.5 Single Ended Lines

The cable configuration of the single ended lines shall be as shown in Figures 4-7 to 4-9.

#### 11.6.6 Single Ended Line Drivers

The drivers shall have open collector outputs capable of sinking 40 milliamps at "LOW" levels. "LOW" level output voltage shall not exceed 0.4 volts. The high level leakage current shall not exceed 250 microamps.

#### 11.6.7 Single Ended Line Receivers

The receivers accept TTL logic levels. For noise immunity the receiver shall have an input hysteresis of 0.4 volts minimum, positive going threshold voltage between 1.4 and 2.0 volts and a negative going threshold voltage between 0.5 and 1.1 volts. Low level input current shall be 1.2 milliamps or less. The high level input current shall be 40 microamps maximum.

#### 11.6.8 Single Ended Line Termination

All single ended lines originating at the host shall be terminated at the last disk drive with 330 ohms, plus or minus 5%, to ground and 220 ohms, plus or minus 5%, to plus 5 volts. All single ended lines originating at the disk drives shall be terminated in the same way at the host.

#### 11.6.9 Port Enable Termination

A 10 k ohms plus or minus 10% pullup resistor to +5 volts shall be added to the Port Enable line in each drive to generate an inactive signal level whenever the drive is not connected to the Control Bus (see Figure 4-8).

Figure 4-7  
Cable Configuration for Unidirectional  
Single Ended Lines from Host (except Port Enable)

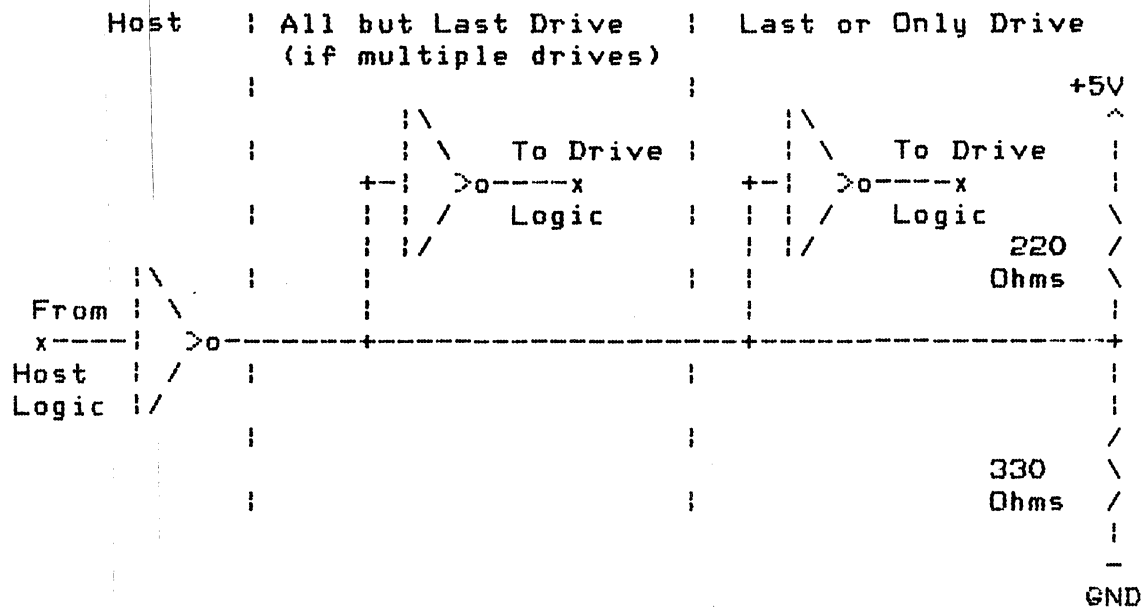


Figure 4-8  
Cable Configuration for Port Enable

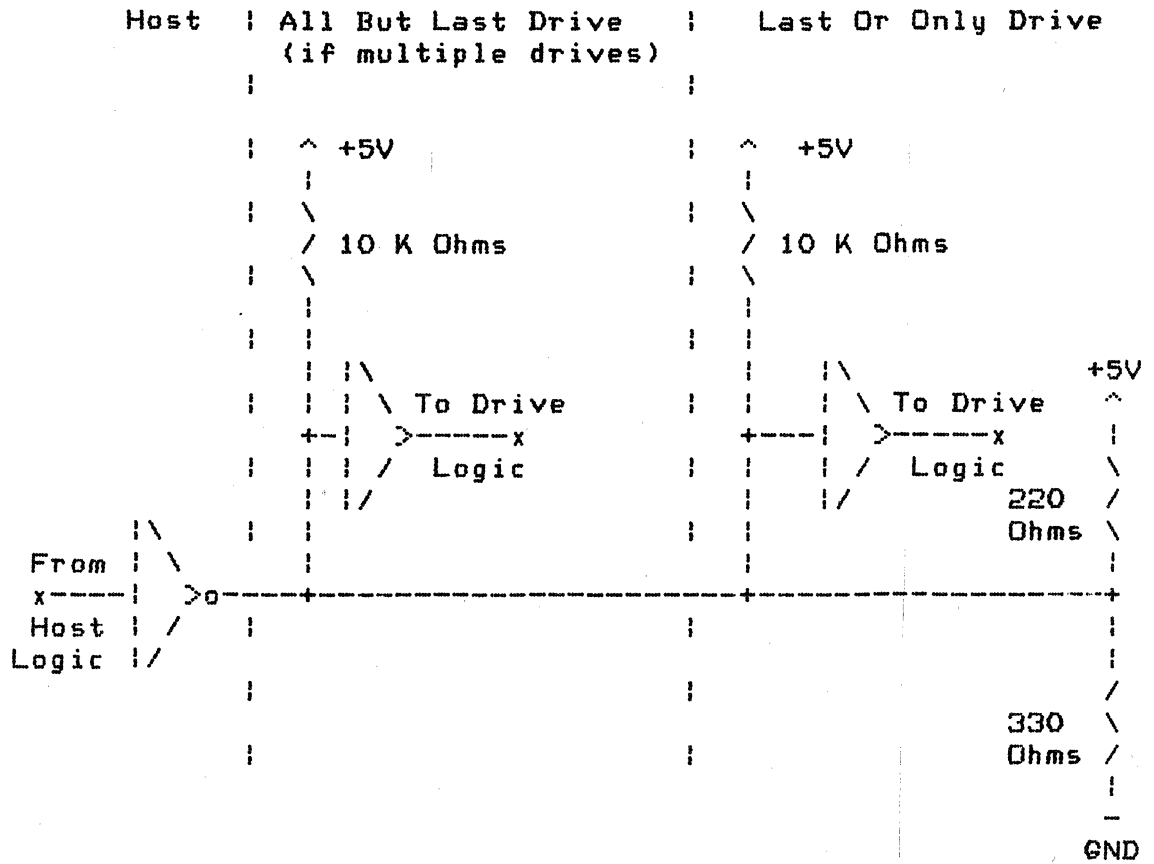
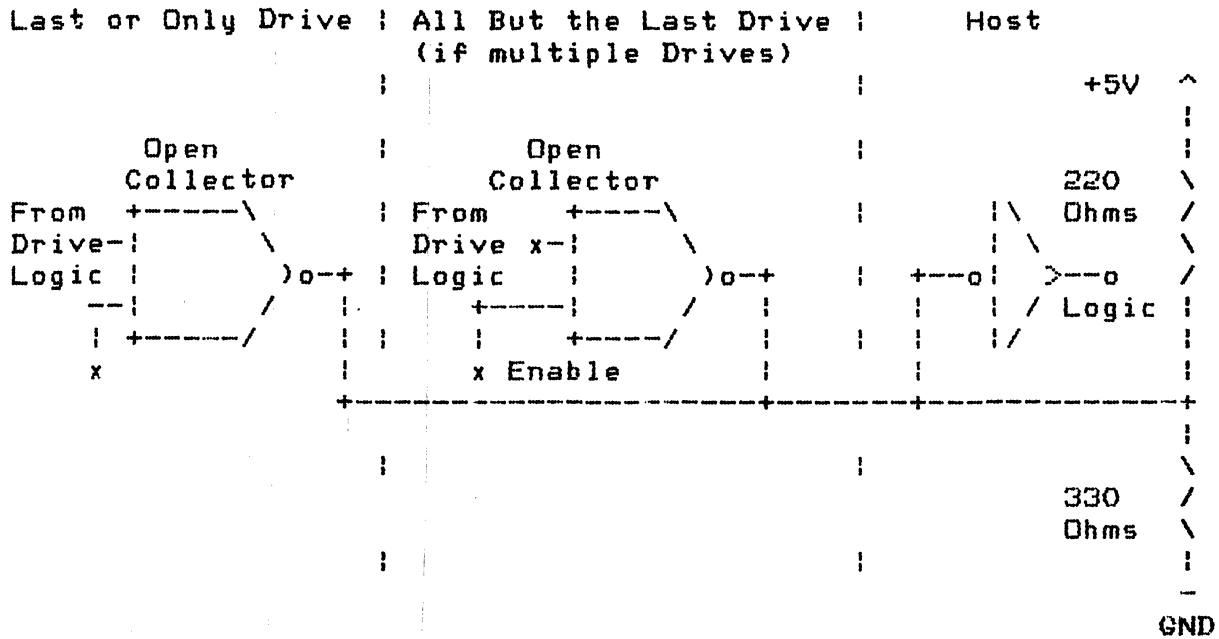


Figure 4-9 Cable Configuration for Unidirectional Single Ended Lines from Drive



11.6.10 Differential Lines

The differential line drivers and receivers shall operate from a single + 5 volts supply. They shall operate to 10 MHz and shall be capable of meeting the timing requirements of Sections 11.9.3 through 11.9.5 while operating the recommended terminated cable configuration.

The cable configuration of the differential lines shall be as shown in Figures 4-10 and 4-11.

An active signal state shall be defined as the "+" line being equal or more positive than the "-" line.

An inactive signal state is defined as the "-" line being more positive than the "+" line.

11.6.10.1 Differential Line Drivers

The differential line drivers shall have a three-state output and be capable of sinking or sourcing a minimum of 20 milliamps in the active state. In the inactive or high impedance state, leakage current shall not exceed plus or minus 20 microamps.

11.6.10.2 Differential Line Receivers

The common mode input range shall be at least +7 to -7 volts. The differential input voltage shall be -0.2 volts minimum and +0.2 volts maximum. The input hysteresis should be 140 millivolts minimum (plus or minus 70 millivolts).

11.6.10.3 Differential Line Termination

Each line of all pairs of differential lines shall be terminated with 100 ohms, plus or minus 10 the host and the last drive.

Figure 4-10  
Cable Configuration for Differential Lines from Host

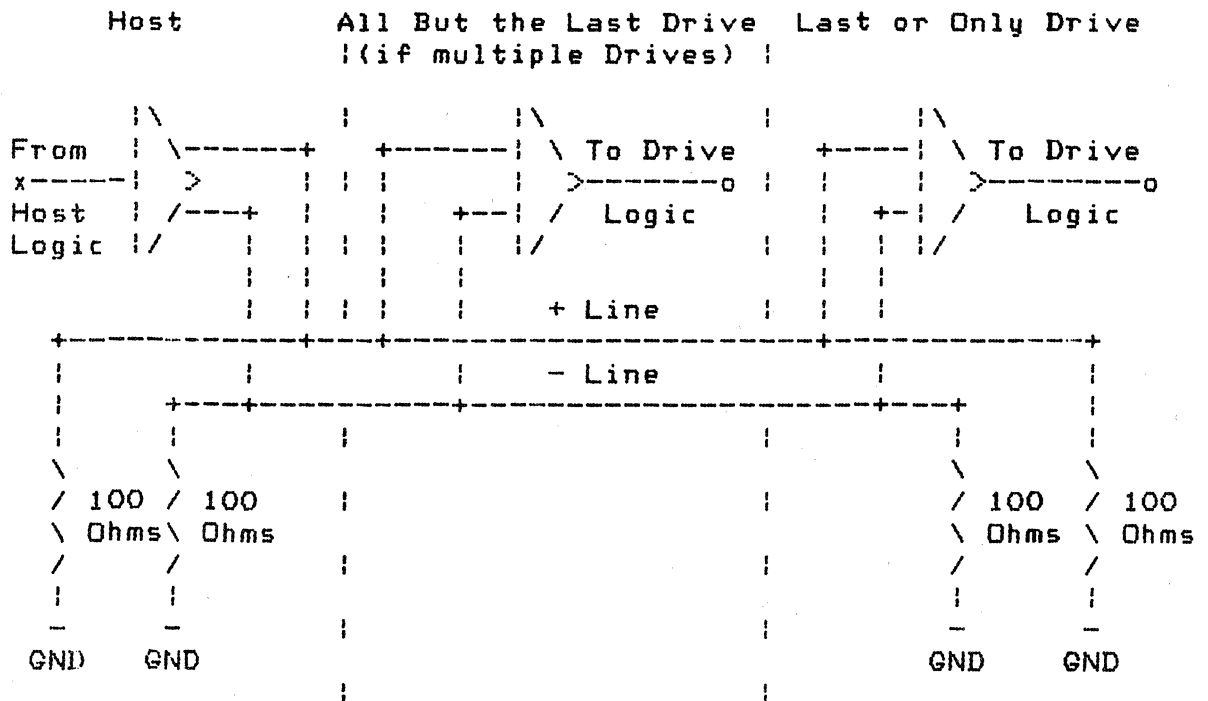


Figure 4-11  
Cable Configuration for Differential Lines from Drive

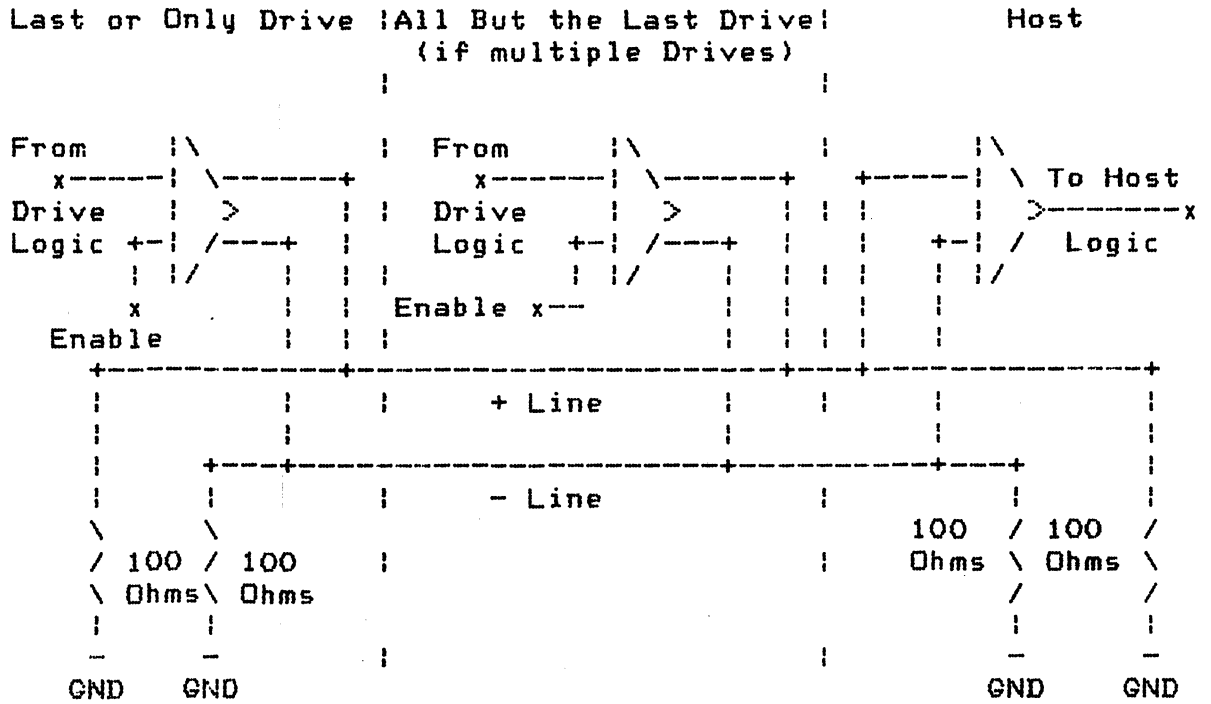




Table 4-2  
Pin Assignment

Sig- nal Pin	GND Pin	Signal Name	Signal Source	Fig. 5.2-
1		Ground	---	
2	10	Control Bus Bit 0, Select/Attn. Drive	0 Host/Drive	2
3	10	Control Bus Bit 1, Select/Attn. Drive	1 Host/Drive	2
4	10	Control Bus Bit 2, Select/Attn. Drive	2 Host/Drive	2
5	10	Control Bus Bit 3, Select/Attn. Drive	3 Host/Drive	2
6	10	Control Bus Bit 4, Select/Attn. Drive	4 Host/Drive	2
7	10	Control Bus Bit 5, Select/Attn. Drive	5 Host/Drive	2
8	10	Control Bus Bit 6, Select/Attn. Drive	6 Host/Drive	2
9	10	Control Bus Bit 7, Select/Attn. Drive	7 Host/Drive	2
11	12	Control Bus Parity	Host/Drive	2
13	14	Select Out/Attn. In Strobe	Host	3
15	16	Command Request	Host	3
17	18	Parameter Request	Host	3
19	20	Bus Direction Out	Host	3
21	22	Port Enable	Host	4
23	24	Not Used (Address Mark Control)	(Host)	
25	26	Read Gate	Host	3
27	28	Write Gate	Host	3
29	30	Bus Acknowledge	Drive	5
31	32	Index	Drive	5
33	34	Sector	Drive	5
35	36	Attention	Drive	5
37	36	Busy	Drive	5
39	38	Read Data +	Drive	7
40	38	Read Data -	Drive	7
42	41	Read/Reference Clock +	Drive	7
43	41	Read/Reference Clock -	Drive	7
45	44	Write Clock +	Host	6
46	44	Write Clock -	Host	6
48	47	Write Data +	Host	6
49	47	Write Data -	Host	6
50		Ground	-----	

### 11.7 Signal Definitions

This section provides signal definitions and their intended operation and/or states. Relative signal timing and tolerance is defined in Section 11.9.

Note: The timing diagrams of Section 11.9 take precedence over all other timing definitions.

### 11.7.1 Control Bus

The Control Bus shall be used for bidirectional transfer of information. The direction of transfer shall be determined by the Bus Direction Out Signal. The electrical characteristics of the Control Bus Signals are defined in Section 11.6.4.1. The Control Bus Signals shall be "LOW" active.

Throughout the specification of this interface the controller shall be in control of the bus. All communications between the controller and the selected drive shall be determined by the host. Upon power up all drives shall be deselected. The host shall be responsible for initiating the selecting process.

The Control Bus is used in two modes. When Select Out/Attention In Strobe is active, the Control Bus shall be in Radial Mode. When the Command Request, Parameter Request, or Bus Acknowledge is active, the Control Bus shall be in Daisy Chain Mode.

#### 11.7.1.1 Radial Mode

Each drive shall be assigned a unit number 0-7, by radially attaching with a Drive Select Jumper (see Section 11.4.2) to one Select/Attention Drive line as per Table 4-2.

##### 11.7.1.1.1 Select Out Mode

When both Bus Direction Out and Select Out/Attention In Strobe are active, each radial line shall transfer the selection information to the corresponding drive.

##### 11.7.1.1.2 Attention In Mode

When Bus Direction Out is inactive and Select Out/Attention In Strobe is active, each drive shall gate its internal Attention Condition via the Drive Select Jumper onto its corresponding Control Bus line.

### 11.7.1.2 Daisy Chain Mode

When in Daisy Chain Mode, all bus transfers shall consist of a two byte sequence. The transfer is asynchronous and controlled with a handshake protocol. The first byte is transferred using a handshake between the Command Request and Bus Acknowledge signals. The second byte is transferred using a handshake between the Parameter Request Signal and the Bus Acknowledge Signal. Refer to Section 11.8 for the command definitions.

#### 11.7.1.2.1 Command Out

When both the Bus Direction Out and Command Request are active, the host shall transfer a Command Byte to the selected drive.

When bit 6 in the Command Code (first byte) is one, the second byte is Parameter Out. Refer to Section 11.7.1.2.2 and Table 4-3.

When bit 6 in the Command Code (first byte) is zero, the second byte is Parameter In. Refer to Section 11.7.1.2.3 and Table 4-4.

When the Bus Direction Out Signal for the transfer of the parameter (second byte) does not comply with the definition of Bit 6 of the Command Code, this condition shall set the Attention Condition and the Control Bus Error Bit in the General Status Byte (see Section 11.8.4.1).

The condition of the Bus Direction Out Signal being inactive and the Command Request Signal being active is a violation of protocol and shall set the Attention Condition and the Control Bus Error Bit of the General Status Byte (see Section 11.8.4.1).

#### 11.7.1.2.2 Parameter Out

When both Bus Direction Out and Parameter Request are active, the controller is transferring a Parameter Byte to the selected drive (see Table 4-3).

### 11.7.1.2.3 Parameter In

When the Bus Direction Out Signal is inactive and Parameter Request Signal is active, the host is requesting a Parameter Byte (status) to be transferred from the selected drive (see Table 4-4).

### 11.7.1.3 Control Bus Bits 0-7, Select/Attention Drive 0-7

The eight Control Bus Signals, 0-7, shall be used for communication between the host and the drive as defined in Sections 11.7.1.1 and 11.7.1.2. Control Bus Bit 0 is the least significant bit.

### 11.7.1.4 Control Bus Parity

The Control Bus Parity Bit shall always be generated in the drive in Daisy Chain Mode.

Control Bus Parity checking and the generation of a Control Bus Error (see Section 11.8.4.1.2) upon wrong parity can be disabled by the Control Bus Parity Checking Jumper (see Section 11.4.3).

When the Control Bus is used in daisy chain mode the bidirectional Control Bus Parity Signal shall be odd parity of the eight Control Bus Bits and the Parity Bit.

When the Control Bus is used in the radial mode, the Control Bus Parity Signal is not used and shall be inactive.

## 11.7.2 Control Interface

This group of signals are uni-directional in nature. The electrical characteristic of the control interface lines is defined in Section 11.6.5. All control interface lines are "LOW" for active signal states and "HIGH" for inactive signal states.

### 11.7.2.1 Port Enable

This signal is normally held active by the host. When this signal is active, all drives attached to the interface shall respond to the interface protocol as described by this specification.

When this signal changes from active to inactive and stays inactive for longer than 500 nanoseconds, all drives shall be logically disconnected from the bus within 1 microsecond. The drive shall remain deselected while Port Enable is inactive.

This signal may be used to disable all drives when host power is lost and/or as a programmed reset. If the interface cable is being disconnected from a drive, the drive shall be reset by the active to inactive transition on this line.

Upon detecting Port Enable going inactive each drive must go to its Initial State as defined below. After Port Enable changes from inactive to active and after the initial state is reached the drive shall set the Attention Condition.

#### Initial State

This is the state reached after a drive has been powered up, Port Enable has become active or a Selective Reset Command has been received and performed.

The conditions are:

1. Drive shall be deselected.
2. Drive shall respond to the Select Out/Attention In Strobe Signal.
3. All parameters of commands with Parameters Out in Table 4-3 shall be reset to zero.
4. The Drive Attribute Table shall be set to its initial state.
5. All resettable error conditions shall be reset. If the cause of the error still exists, it shall set the error conditions again.
6. Sector Pulses shall be generated according to the setting of the Sector Jumpers (see Table 4-6).
7. The Initial State Bit in Sense Byte 2 shall be set (see Section 11.8.4.3.1).
8. Self test diagnostics shall be executed.
9. Drive spun down (only if Initial State is reached after Power Up. Port Enable and the Selective Reset Command shall not affect the spin state).

### 11.7.2.2 Bus Direction Out

The Bus Direction Out Signal is transferred from the controller to all attached drives. Bus Direction Out controls the direction of transfer on the Control Bus. When the Bus Direction Out Signal is active this defines a transfer from the host to the drive.

### 11.7.2.3 Select Out/Attention In Strobe

This signal is transferred from the host to all attached drives. It has two different functions depending on the state of the Bus Direction Out Signal.

When the Bus Direction Out Signal is active, the signal is Select Out Strobe.

When the Bus Direction Out Signal is inactive, the signal is Attention In Strobe.

#### 11.7.2.3.1 Select Out Strobe

Only one drive shall be selected at any one time. When the Bus Direction Out Signal is active, the active going edge of the Select Out Strobe Signal is used for selecting/deselecting the drive.

When any one of the Control Bus Signals is active and Select Out Strobe transitions to active, the drive connected to that specific Control Bus line shall become selected.

When any Control Bus Signal is inactive and Select Out Strobe transitions to active, the drive connected to that specific Control Bus line shall become deselected.

When all Control Bus Signals are inactive and the Select Out Strobe transitions to active, all attached drives shall become deselected.

#### 11.7.2.3.2 Attention In Strobe

When the Bus Direction Out Signal is inactive, the Attention In Strobe is used to gate the Radial Attention Condition of the drive (see Section 11.7.2.8) onto the corresponding Control Bus line connected to that drive.

#### 11.7.2.4 Command Request

This signal initiates the handshake control from the controller to the selected drive. The active state of this signal signifies the transfer of the first byte of each two-byte transfer. Until the receipt of Bus Acknowledge, the Command Request Signal shall remain active.

#### 11.7.2.5 Parameter Request

This signal is also a handshake control line from the controller to the selected drive. The active state of this signal for a Parameter Out command indicates that the output Parameter Byte is valid on the Control Bus. The active state of this signal for a Parameter In Command requests the selected drive to place the Parameter Byte on the Control Bus. Until the receipt of Bus Acknowledge, the Parameter Request Signal shall remain active.

#### 11.7.2.6 Bus Acknowledge

This signal is returned from the selected drive to the controller. The Bus Acknowledge Signal has two functions.

When the Control Bus is used in Radial Mode (Select Out/Attention In Strobe active), the selected drive shall make the Bus Acknowledge Signal active to acknowledge its selection.

When the Control Bus is used in Daisy Chain Mode, the Bus Acknowledge Signal performs the asynchronous handshake with the Command Request Signal or the Parameter Request Signal.

#### 11.7.2.7 Busy

This signal shall be held active by the selected drive if the selected drive is unable to accept additional commands. The Busy Signal shall change to the active state before the active going edge of the Bus Acknowledge of a Time Dependent Command that causes the drive to become busy. The Busy Condition shall occur during power up sequencing, a Selective Reset Command, a Spin Command, a Rezero Command, an Offset Command, a Partition Track Command, or a Seek to Outer Stop Command. The Busy Signal shall also be set during a self-initiated Rezero operation upon a failing Seek or upon detection of a Guard Band Error (see Sections 11.8.2.1.4 and 11.8.4.4.3).

When the Seek Busy Jumper (see Section 11.4.7) is installed, the Busy Signal shall also be made active during a Seek Command and a Time Dependent Select Moving Head Command.

The Busy Signal shall not be made active if the drive can accept commands.

The Busy to not Busy transition within the drive shall set the Attention Condition (see Section 11.7.2.8).

If Command Request becomes active when the Busy Signal is already active the drive shall not respond with Bus Acknowledge before the function is completed and the Busy Signal is made inactive. No Control Bus time out check is performed in this case.

#### 11.7.2.8 Attention

This signal is a party line signal ("wired OR") from all drives to the controller, independent of the selection of a drive.

The Attention Signal shall be made active by a drive, if the drive's internal Attention Condition is set to one and if Attention is enabled. The Attention Condition shall be set if the drive requires service from the controller. The detailed conditions to set the Attention Condition are defined in Section 11.8.

The Attention Condition of the selected drive shall only be cleared by the Clear Attention Command or the Clear Fault Command. Issuing the Clear Fault Command shall reset only those error status bits and the resulting Attention Condition the error condition of which can be reset. A Clear Attention Command shall reset the Attention Condition independent of error conditions.

#### 11.7.2.9 Index

A valid Index Signal is transferred from the selected drive to the controller whenever the drive is ready.

Index is a signal that indicates to the controller that a reference point or index area is passing under the heads of the selected drive. One Index Pulse shall be generated by the selected drive per revolution of the recording media. The Index Pulse shall have a length of 2.5 microseconds plus or minus 100 nanoseconds.



#### 11.7.2.10 Sector

A valid Sector Signal is transferred from the selected drive to the controller whenever the drive is ready and no Partition Track Command (see Section 11.8.2.2.5) is being performed.

The Sector Signal establishes rotational reference points on the recording surface. Each track may be divided into equal length sectors with the initial sector ("zero") starting coincident with the Index Pulse. When the Index Pulse is activated, the Sector Pulse is omitted. The Sector Pulse shall have a length of 2.5 microseconds plus or minus 100 nanoseconds.

For the possible numbers of Sector Pulses Per Track see Section 11.8.3.10.

#### 11.7.2.11 Read Gate

The Read Gate Signal is transferred from the controller to the selected drive.

The Read Gate Signal enables and synchronizes the read circuitry to transfer the serialized data information on the Read Data lines from the recording medium.

If Read Gate is made active when the drive has positioned to a cylinder where reading is not permitted (see Section 11.8.1.2.8), the Read/Write Permit Violation Bit in Sense Byte 1 and the Attention Condition shall be set. The Read Data Lines shall be held static, if this error occurs.

If Read Gate and Write Gate are active simultaneously, the Read/Write Fault Bit in the Sense Byte 1 and the Attention Condition shall be set.

Read Gate being active, when a Seek, Partition Track, Select Moving Head, Read Control or Load Read Permit Command is issued, is a violation of protocol and shall set the Command Reject Bit in the Sense Byte 1 and the Attention Condition.

#### 11.7.2.12 Write Gate

The Write Gate Signal is transferred from the controller to the selected drive.

The Write Gate Signal enables the write circuitry in the drive to transfer the serialized information on the Write Data Lines to the recording medium.

Note: A write operation shall not take place unless a write enable condition has been established by a previous Write Control Command (see Section 11.8.1.1.2).

Making Write Gate active when no previous Write Control Command was issued to permit writing shall set the Read/Write Fault Bit in Sense Byte 1 and the Attention Condition.

Making Write Gate active when writing to the current cylinder is not allowed by a previous Load Write Permit Command shall set the Read/Write Permit Violation Bit in the Sense Byte 1 (see Section 11.8.4.2.4) and the Attention Condition.

Making Write Gate active when the drive is in an Offset State shall set the Read/Write Fault Bit and the Command Reject Bit (see Sections 11.8.4.2.2 and 11.8.4.2.6) and the Attention Condition.

When Write Gate and Read Gate are active simultaneously, the Read/Write Fault Bit in the Sense Byte 1 and the Attention Condition shall be set.

Making Write Gate active when the Busy Signal is active or the Busy Executing Bit in the General Status Byte is set is a violation of protocol and shall set the Read/Write Fault Bit in the Sense Byte 1 and the Attention Condition.

Write Gate being active when a Seek, Partition Track, Write Control, Select Moving, Head or Write Permit Command is issued, is a violation of protocol and shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition.

No write operation shall take place when these errors occur.

### 11.7.3 Read/Write Signals

This section describes the signals used when transferring data to and from the controller. These signals are only valid if a drive is selected. All of these signals are driven differentially (see Section 11.6.10). All data sent to the drive or host shall be Non-Return-to-Zero (NRZ).

### 11.7.3.1 Read Data

When Read Gate is active, the Read Data lines carry the serial NRZ read data. This data is synchronized with Read Clock. The Read Data Signal shall be static when Read Gate is not active.

### 11.7.3.2 Read/Reference Clock

The Read/Reference Clock is transferred from the selected drive to the controller. This signal transfers Read Clock when Read Gate is active. Read Clock is synchronous with serial NRZ read data.

This signal shall transfer the Reference Clock at all other times.

### 11.7.3.3 Write Data

When Write Gate is active, the Write Data lines shall transfer the serial NRZ data to the selected drive for recording. The serial write data is synchronized to the Write Clock. This signal shall be held static at all times except when Write Gate is active.

### 11.7.3.4 Write Clock

Write Clock is used by the selected drive to properly phase the Write Data lines while recording. Write Clock is generated in the controller by returning the Reference Clock Signal back to the selected drive at the same frequency with an unspecified but constant shift in phase. This signal shall be held static at all times except when used to precede the active going edge of Write Gate by at least one bit cell but not more than 16 bit cells and when Write Gate is active.

## 11.8 Command Structure

All command, status, and parameter information passed between the selected drive and the host shall be transferred via the Control Bus and shall conform to the command protocol defined in this specification.

The command protocol requires that each command consists of a two byte transfer. The first byte, the Command Byte, shall always be transferred from the controller to the selected drive. The second byte, the Parameter Byte, may be transferred from the controller to the selected drive or from the selected drive to the controller. The direction of the transfer of the Parameter Byte is determined by the Bus Direction Out Signal.

Command Codes 80-FF Hex are reserved for commands outside the scope of the ANSI specification. It is desirable that this device dependent level interface operates with an as yet undefined higher level interface. By reserving the most significant bit of the Command Code a simple check can identify commands that are either executed or passed on by such a higher level interface. If a reserved command is received, the drive shall set the Attention Condition and the Illegal Command Bit in the General Status Byte.

The Command Byte, therefore, indicates the particular function that the selected drive is to perform. This may include functions such as accepting parametric information from the controller, performing requested head motion, or reporting specific status conditions. The Command Byte also conditions the drive as to the direction of the transfer of the Parameter Byte of the command sequence.

The Parameter Byte completes the command sequence by providing the parameter or status information demanded by the Command Byte. In cases where the Command Byte is sufficient to indicate the complete nature of the command, the General Status Byte is transferred as Parameter Byte to complete the command sequence.

Below all defined command sequences are specified. They are divided into two groups: One which requires the Parameter Byte transferred to the drive (Parameter Out) and one which requires the Parameter Byte transferred to the controller (Parameter In).

Note that there is a further subdivision in each group. There are Mandatory Commands which shall be implemented in all drives conforming to the ANSI standard.

There is a second class of commands that are defined and implemented in the KENNEDY ANSI according to the ANSI standard. They are called Optional Commands.

A third class of commands are the KENNEDY Unique Commands.

The KENNEDY ANSI is designed so that the drive is operational with the Mandatory Command Set. The Optional Commands which are implemented and the KENNEDY Unique Commands may be used however to increase the degree of comfort and flexibility. There are two classes of commands:

Immediate Commands and  
Time Dependent Commands

For Immediate Commands the active going edge of the second Bus Acknowledge shall not be generated until the required action has been performed. In the case that the action is not performed, the Attention Condition shall be set prior to the active going edge of the Bus Acknowledge Signal that is returned as a response to Parameter Request.

For Time Dependent Commands, the Attention Condition shall be set when the action for the Time Dependent Command is completed. The resetting of the Attention Condition by the Immediate Command, Clear Fault or Clear Attention, completes the Time Dependent Command.

All commands, once in progress, shall proceed to completion utilizing parameters established prior to the issuance of the command. While a Time Dependent Command (denoted in Tables 4-3 and 4-4 by a \*) is in progress, and if the drive is not busy, a new Time Dependent Command is issued, the new Time Dependent Command shall be rejected by setting the Attention Condition and the Command Reject Bit in Sense Byte 1.

A new Time Dependent Command may be issued only after the current Time Dependent Command has been completed.

Also, while a Time Dependent Command is in progress, the drive shall accept Immediate Commands if the Busy Signal is not set.

While all commands are defined individually, there are logical groupings of commands that represent functional operations. For example, the loading of parameter information (cylinder address) and the execution of a particular operation (seek).

Possible violations of the protocol and the resulting status are indicated in the description of the signals (see Section 11.7) and in the description of the commands (see Sections 11.8.1 and 11.8.2).

Table 4-3  
Commands With Parameters Out

Function	Command Code	Parameter Out
Attention Control	40 Hex	Bit 7 0 = Enable Attention 1 = Disable Attention
Write Control	41 Hex	Bit 7 0 = Write Disable 1 = Write Enable
Load Cylinder Address High	42 Hex	MSB of Cylinder Address
Load Cylinder Address Low	43 Hex	LSB of Cylinder Address
Select Moving Head (Immediate)	44 Hex	Head Number
<u>Sel. Moving Head (Time Dep.) *</u>	<u>45 Hex</u>	<u>Head Number</u>
Load Attribute Number	50 Hex	Address Byte
Load Drive Attribute	51 Hex	Information Byte
Read Control	53 Hex	Bits 7,6 0X = Nominal Strobe 10 = Strobe Early 11 = Strobe Late
Offset Control *	54 Hex	Bits 7,6 0X = No Offset 10 = Offset Forward 11 = Offset Reverse
Spin Control * **	55 Hex	Bit 7 0 = Spin Down 1 = Spin Up
Load Bytes Per Sector High	56 Hex	MSB of # of Bytes P. S.
Load Bytes Per Sector Medium	57 Hex	MedSB of # of B. P. S.
Load Bytes Per Sector Low	58 Hex	LSB of # of Bytes P. S.
Load Sect. Pulses Per Tr. High	59 Hex	MSB of # of Sect. P.
Load Sect. Pulses Per Tr. Med.	5A Hex	MedSB of # of Sect. P.
Load Sect. Pulses Per Tr. Low	5B Hex	LSB of # of Sect. P.
Load Read Permit High	6B Hex	MSB of Cylinder Address
Load Read Permit Low	6C Hex	LSB of Cylinder Address Read enabled only on cylinder equal to or greater than the above
Load Write Permit High	6D Hex	MSB of Cylinder Address
Load Write Permit Low	6E Hex	LSB of Cylinder Address Write enabled only on Cylinder equal to or greater than the above
Load Test Byte	6F Hex	Test Byte

All unused bits in parameters are zero (0).

\* This command is a Time Dependent Command and shall set the Attention Condition upon completion.

\*\* There is a jumper on the ANSI board to allow the acceptance of this command. Without this jumper the drive shall spin up upon receipt of power (see Section 11.4.5).

Commands with codes 40 Hex through 4F Hex are Mandatory Commands, commands with codes 50 Hex through 6F Hex are Optional Commands.

Table 4-4  
Commands With Parameter In

<u>Function</u>	<u>Command Code</u>	<u>Parameter In</u>
Report 'Illegal Command' **	00 Hex	General Status Byte
Clear Fault	01 Hex	General Status Byte
Clear Attention	02 Hex	General Status Byte
Seek *	03 Hex	General Status Byte
Rezero *	04 Hex	General Status Byte
Report Sense Byte 2	0D Hex	Sense Byte 2
Report Sense Byte 1	0E Hex	Sense Byte 1
Report General Status	0F Hex	General Status Byte
Report Drive Attribute	10 Hex	Drive Attribute Byte
Set Attention **	11 Hex	General Status Byte
Selective Rreset *	14 Hex	General Status Byte
Seek to Outer Stop *	15 Hex	General Status Byte
Partition Track *	16 Hex	General Status Byte
Report Cylinder Address High	29 Hex	MSB of Cyl. Address
Report Cylinder Address Low	2A Hex	LSB of Cyl. Address
Report Read Permit High	2B Hex	MSB of Cyl. Address
Report Read Permit Low	2C Hex	LSB of Cyl. Address
Report Write Permit High	2D Hex	MSB of Cyl. Address
Report Write Permit Low	2E Hex	LSB of Cyl. Address
Report Test Byte	2F Hex	Test Byte
Report Sense Byte 3	30 Hex	Sense Byte 3 ***
Report Diagnostic Results	31 Hex	Diagnostic Byte ***
Report Sense Byte 4	32 Hex	Sense Byte 4 ***
Report Sense Byte 5	33 Hex	Sense Byte 5 ***

All unused bits in parameters are zero (0).

\* This command is a Time Dependent Command and shall generate the Attention Condition upon completion.

\*\* This command is an Immediate Command and shall set the Attention Condition.

\*\*\* These Bytes are KENNEDY Unique. See Section 11.8.2.3.

Commands with codes 00 Hex through 0F Hex are Mandatory Commands, commands with codes 10 Hex through 2F Hex are Optional Commands, and commands with codes 30 Hex to 3F Hex are KENNEDY Unique Commands.

### 11.8.1 Commands with Parameter Out

All commands defined in this section require a Parameter Byte to be transferred to the drive. These commands are summarized in Table 4-3.

#### 11.8.1.1 Mandatory Commands with Parameter Out

All Mandatory Commands are implemented in the KENNEDY ANSI interface.

##### 11.8.1.1.1 Attention Control (Command Code 40 Hex)

This command shall condition the drive to enable or disable its attention circuitry based on the value of the Parameter Byte as shown below.

Bit	7	6	5	4	3	2	1	0
	+	+	+	+	+	+	+	+
		X		0		0		0
		0		0		0		0
		0		0		0		0
	+	+	+	+	+	+	+	+
		_____ X = 0 Enable Attention						
		_____ X = 1 Disable Attention						

This command allows the host to selectively ignore attention requests from certain drives on the interface. This might be done in response to a drive that generates spurious attention requests due to a malfunction.

The Enable Attention Command shall cause the selected drive to gate its internal Attention Condition onto the party line ("wired OR") Attention Signal.

The Disable Attention Command shall cause the selected drive to disable the gating of the internal Attention Condition onto the party line Attention Signal.

This command shall have no impact on the function of the radial status returned with the Attention In Strobe Signal (see Section 11.7.2.3.2).

Drives shall be initialized with the attention circuitry enabled.



## 11.8.1.1.2 Write Control (Command Code 41 Hex)

This command shall condition the selected drive to enable or disable its write circuitry and thus declare the selected drive as being write protected, based on the value of the Parameter Byte as shown below.

Bit	7	6	5	4	3	2	1	0
	X	0	0	0	0	0	0	0
	<div style="display: flex; align-items: center; margin-left: 20px;"> <span style="font-size: 2em; margin-right: 5px;"> </span> <span style="border-bottom: 1px solid black; width: 100px; display: inline-block; margin-right: 5px;"></span> <span>X = 0 Write Disable</span> </div> <div style="display: flex; align-items: center; margin-left: 20px;"> <span>X = 1 Write Enable</span> </div>							

This command is used in conjunction with the Write Gate Signal and therefore merely enables the write circuitry while the Write Gate Signal activates the circuitry at the proper time. An active Write Gate Signal while the drive's write circuitry is disabled shall result in no data being recorded, Bits 1 and 5 of Sense Byte 1 being set, and an Attention Condition being generated.

If the drive is in a Write Disabled State, the 'Positioned Within Write Protected Area' Bit in the Sense Byte 2 shall be set.

A Write Control Command issued during a write operation is a violation of protocol and shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition.

Drives shall be initialized with the write circuitry disabled.

## 11.8.1.1.3 Load Cylinder Address Commands

These two commands shall transfer by their parameter portions a 16 bit cylinder address to the selected drive.

These commands are used in conjunction with the Seek Command (see Section 11.8.2.1.4) and therefore are a means of supplying a target cylinder address.

These commands shall not cause any head motion. Loading a cylinder address outside the range of the drive shall not cause an error unless a subsequent Seek Command is issued to that illegal cylinder.

Issuing these commands while a Seek Command is performed is a violation of protocol and shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition.

The sequence of these Commands may be either way.

Drives are initialized with the target cylinder address equal to zero.

11.8.1.1.3.1 Load Cylinder Address High (Command Code 42 Hex)

This command shall condition the selected drive to accept the Parameter Byte as the most significant byte of the 16 bit target cylinder address.

11.8.1.1.3.2 Load Cylinder Address Low (Command Code 43 Hex)

This command shall condition the selected drive to accept the Parameter Byte as the least significant byte of the 16 bit target cylinder address.

11.8.1.1.4 Select Moving Head (Command Codes 44 Hex and 45 Hex)

There are two Command Codes for the Head Selection. Command Code 45 Hex is used by drives, which need a considerable amount of time to select the heads.

For compatibility reasons the 6170 ANSI interface accepts both codes. On Command Code 44 Hex no Attention Condition is set.

On Command Code 45 Hex the Busy Signal is set temporarily, if the Seek Busy Jumper is installed, during the Bus Acknowledge for Parameter Request. Then the Attention Condition is set.

These commands shall condition the selected drive to accept the Parameter Byte as the binary address of the head selected for read or write operations.

A Select Moving Head Command executed during a read or write operation is a violation of protocol and shall set the Command Reject Bit and the Attention Condition.

The drive shall set the Attention Condition and the Illegal Parameter Bit in the General Status Byte upon receipt of a head address outside the head address range of the drive.

See Table 4-7 for the valid head addresses of the drive models.

Drives shall be initialized with head zero selected.

#### 11.8.1.2 Optional Commands with Parameter Out

The following optional commands with Parameter Out are implemented in the 6170 ANSI interface.

Issuance of other optional commands with Parameter Out shall set the Attention Condition and the Illegal Command Bit in the General Status Byte.

##### 11.8.1.2.1 Load Attribute Number (Command Code 50 Hex)

This command shall condition the selected drive to accept the Parameter Byte as the Number of a Drive Attribute as defined in Table 4-5 and Section 11.8.3. This command prepares the drive for a subsequent Load Drive Attribute Command or Report Drive Attribute Command (see Sections 11.8.1.2.2 and 11.8.2.2.1). This command may be issued at any time.

If for a received Number no Attribute is assigned, the Illegal Command Bit in the General Status Byte and the Attention Condition shall be set.

The Attribute Number shall be initialized to zero, so that a Load/Report Drive Attribute Command without a preceding Load Attribute Number Command shall use Attribute Number zero.

An Attribute Number established with a Load Attribute Number Command shall be used for all further Load/Report Attribute Commands unless changed by another Load Attribute Number Command or by entering Initial State.

## 11.8.1.2.2 Load Drive Attribute (Command Code 51 Hex)

This command shall condition the selected drive to accept the Parameter Byte as the new value of a Drive Attribute. The number of the Drive Attribute must have been previously defined by the Load Attribute Number Command (see Section 11.8.1.2.1).

If the selected Attribute is Read Only, then the Illegal Command Bit in the General Status and the Attention Condition shall be set.

The Attributes 00 Hex, 0E Hex, 33 Hex, and 43 Hex can be loaded.

## 11.8.1.2.3 Read Control (Command Code 53 Hex)

This command shall condition the selected drive to modify its read timing. The modification to the timing is defined by the value of the Parameter Byte as shown below.

Bit	7	6	5	4	3	2	1	0
			0	0	0	0	0	0
	0	X	= Nominal Read Strobe					
	1	0	= Read Strobe Early					
	1	1	= Read Strobe Late					

X = don't care

When set the read control shall remain in the one state and shall only return to the Nominal Strobe state by a new Read Control Command, Seek Command or Rezero Command or by entering Initial State.

Issuing this command while Read Gate is active shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition. Writing shall not be affected by the Strobe Early or Strobe Late state.

The drive shall be initialized with the Nominal Strobe timing.

## 11.8.1.2.4 Offset Control (Command Code 54 Hex)

This command shall condition the selected drive to modify the position of the moving heads. The offset modification is defined by the value of the Parameter Byte as shown below.

Bit	7	6	5	4	3	2	1	0
			0	0	0	0	0	0
	0	X	= No Offset					
	1	0	= Offset Forward					
	1	1	= Offset Reverse					

X = don't care

Furthermore, the setting of any offset has the effect of disabling the write circuitry and any write operation attempted shall set the Command Reject Bit and the Read/Write Fault Bit in the Sense Byte 1 and the Attention Condition.

The Offset Control Command is in effect a seek command and as such shall set the Attention Condition upon the completion of the offset operation.

The typical time for an Offset Command to move the heads from a No Offset condition to Offset or for return from Offset to No Offset shall be 3.7 milliseconds. If the offset already exists in the desired direction, no time is required. If the Offset Command requires the opposite direction of an already existing offset, the time shall be 7.5 milliseconds typical.

The offset control shall be reset to No Offset positioning by every Seek Command and Rezero Command.

The drive shall be initialized with No Offset.

Issuing this command while a Seek Command is performed  
 Issuing this command while a Seek Command is performed or when the Not Ready Bit in the General Status Byte is a one shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition.

11.8.1.2.5 Spin Control (Command Code 55 Hex)

A jumper within the 6170 ANSI interface allows two modes of controlling the spindle motor.

Note: The current KENNEDY 6170 Models do not allow the Spin Control Command.

Without the jumper the motor shall spin up or down when power to the drive is applied or removed. In this case the Spin Command is illegal. If it is received then the Attention Condition and the Illegal Command Bit in the General Status Byte shall be set.

When the jumper is installed, the Spin Control Command shall be allowed.

This command shall condition the selected drive to enter a spin up or spin down cycle based upon the state of the Parameter Byte as shown below.

Bit	7	6	5	4	3	2	1	0
	X	0	0	0	0	0	0	0

|  
 +--- X = 0 Spin Down  
       X = 1 Spin Up

When the Spin Control Jumper is installed, the drive shall be initialized upon Power On in the Spin Down State. The Selective Reset Command and the Port Enable Signal shall not change the state of spin control.

A spin up cycle consists of starting the rotation of the spindle, waiting for the rotational speed to get within the given tolerance, and a self-initiated rezero operation. A spin down cycle initiates the stopping of the spindle rotation.

Upon completion of a spin up sequence the drive shall set the Attention Condition. Issuing a Spin Up Command to a drive already in "up" condition or a Spin Down Command to a drive already in "down" condition shall cause the Attention Condition to be set.

If 15 seconds after receipt of a Spin Up Command the final speed was not reached or 15 seconds after the receipt of a Spin Down Command the speed did not decrease, the Spin Error Bit in Sense Byte 3 and the Attention Condition shall be set.

It is not recommended to spin down the drive except before shutting off the power to the system.

#### 11.8.1.2.6 Load Bytes Per Sector Commands

These three commands shall condition the selected drive to accept the Parameter Bytes as a 24 bit number that represents the total number of bytes that will occur between active going edges of Sector Pulses, and between the active going edge of the Index Pulse and the active going edge of the first Sector Pulse when a Partition Track Command is executed.

Note that only even numbers of Bytes Per Sector are used. The least significant bit of the number of Bytes Per Sector is discarded.

These commands are used in conjunction with the Partition Track Command (see Section 11.8.2.2.5).

Upon completion of the execution of the Partition Track Command, the content of the Parameter Bytes transferred by these commands shall be loaded into the corresponding Bytes Per Sector Attributes (see Section 11.8.3.9 and Table 4-5).

The default value of these parameters is zero, while the default value of the corresponding Attributes is given by the Sector Size Select Jumpers.

##### 11.8.1.2.6.1 Load Bytes Per Sector High (Command Code 56 Hex)

This command supplies the most significant byte of the 24 bit number which represents the Number of Bytes Per Sector (see Section 11.8.1.2.6).

##### 11.8.1.2.6.2 Load Bytes Per Sector Medium (Command Code 57 Hex)

This command supplies the medium significant byte of the 24 bit number which represents the Number of Bytes Per Sector (see Section 11.8.1.2.6).

### 11.8.1.2.6.3 Load Bytes Per Sector Low (Command Code 58 Hex)

This command supplies the least significant byte of the 24 bit number which represents the Number of Bytes Per Sector (see Section 11.8.1.2.6).

### 11.8.1.2.7 Load Sector Pulses Per Track Commands

These three commands shall condition the selected drive to accept the Parameter Bytes as a 24 bit number that represents the total number of Sector Pulses between (but excluding) Index Pulses generated by the drive when a Partition Track Command is executed.

These commands are used in conjunction with the Partition Track Command (see Section 11.8.2.2.5).

Upon completion of the Partition Track Command, the content of the Parameter Bytes transferred by these commands shall be loaded into the corresponding Sector Pulses Per Track Attribute (see Table 4-5 and Section 11.8.3.10).

The default value of these parameters is zero, while the default value of the corresponding Attributes is given by the Sector Size Select Jumpers.

The minimum number of Sector Pulses Per Track is three (3).

#### 11.8.1.2.7.1 Load Sector Pulses Per Track High (Cmd. Code 59 Hex)

This command shall condition the selected drive to accept the Parameter Byte as the most significant byte of the 24 bit number that represents the total number of Sector Pulses. See Section 11.8.1.2.7.

If the Parameter of this command is 80 Hex, its value shall be considered to be zero, and a subsequent Partition Track Command (see Section 11.8.2.2.5) shall allow an additional Sector Pulse in the calculation of the resulting overall byte count.



#### 11.8.1.2.7.2 Load Sector Pulses Per Track Medium (Code 5A Hex)

This command shall condition the selected drive to accept the Parameter Byte as the medium significant byte of the 24 bit number that represents the total number of Sector Pulses. See Section 11.8.1.2.7.

#### 11.8.1.2.7.3 Load Sector Pulses Per Track Low (Cmd. Code 59 Hex)

This command shall condition the selected drive to accept the Parameter Byte as the least significant byte of the 24 bit number that represents the total number of Sector Pulses. See Section 11.8.1.2.7.

#### 11.8.1.2.8 Load Read Permit Commands

These two commands shall condition the selected drive to accept the Parameter Bytes as a 16 bit cylinder address defining a programmable read permit area on the drive.

The drive shall allow read operations to occur only on cylinders with an address equal to or greater than the cylinder address programmed in the drive via these commands.

Issuing these commands while Read Gate is active is a violation of protocol and shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition.

If Read Gate is made active and the drive is positioned to a cylinder where reading is not permitted, the Read/Write Permit Violation Bit in Sense Byte 1 and the Attention Condition shall be set.

The drive shall be initialized with Read Permit Address equal to zero.

The sequence of these commands may be either way. Note that between the first and the second Load Read Permit Command there may exist an unwanted read permit boundary.

#### 11.8.1.2.8.1 Load Read Permit High (Command Code 6B Hex)

This command shall condition the selected drive to accept the Parameter Byte as the most significant byte of a 16 bit cylinder address defining a programmable read permit area on the drive. See Section 11.8.1.2.8.

#### 11.8.1.2.8.2 Load Read Permit Low (Command Code 6C Hex)

This command shall condition the selected drive to accept the Parameter Byte as the least significant byte of a 16 bit cylinder address defining a programmable read permit area on the drive. See Section 11.8.1.2.8.

#### 11.8.1.2.9 Load Write Permit Commands

These commands shall condition the selected drive to accept the Parameter Bytes as a 16 bit cylinder address defining a programmable write permit area on the drive.

If Write Gate is made active and the drive is positioned to a cylinder where writing is not permitted, the Read/Write Permit Violation Bit in Sense Byte 1 and the Attention Condition shall be set.

No write operation shall take place when this error occurs.

Issuing these commands while Write Gate is active is a violation of protocol and shall set the Command Reject Bit in Sense Byte 1 and the Attention Condition.

The drive shall be initialized with the Write Permit Address equal to zero.

If the heads are positioned to a cylinder where writing is not permitted, the 'Positioned Within Write Protected Area' Bit in the Sense Byte 2 shall be set.

If these commands are issued during a Seek Command, the 'Positioned Within Write Protected Area' Bit in Sense Byte 2 shall reflect the cylinder address, which the drive had before the Seek. Upon completion of the Seek the new cylinder address is reflected in the 'Positioned Within Write Protected Area' Status Bit.

The sequence of these commands may be either way. Note that between the two Load Write Permit Commands there may

exist an unwanted write permit boundary.

11.8.1.2.9.1 Load Write Permit High (Command Code 6D Hex)

This command shall condition the selected drive to accept the Parameter Byte as the most significant byte of a 16 bit cylinder address defining a programmable write permit area on the drive.

11.8.1.2.9.2 Load Write Permit Low (Command Code 6E Hex)

This command shall condition the selected drive to accept the Parameter Byte as the least significant byte of a 16 bit cylinder address defining a programmable write permit area on the drive.

11.8.1.2.10 Load Test Byte (Command Code 6F Hex)

This command shall condition the selected drive to accept the Parameter Byte as a special test byte that shall be returned to the host as the Parameter of the Report Test Byte Command (see Section 11.8.2.2.9).

This command pair allows the host to test the integrity of the data transfer over the Control Bus.

The default value of the Test Byte shall be zero.

11.8.2 Commands with Parameter In

The commands defined in this section require a Parameter Byte to be transferred to the host. These commands are summarized in Table 4-4.

11.8.2.1 Mandatory Commands with Parameter In

All Mandatory Commands are implemented in the KENNEDY ANSI.

#### 11.8.2.1.1 Report "Illegal Command" (Command Code 00 Hex)

This command shall force the Illegal Command Bit to be set in the General Status Byte (see Section 11.8.4.1). The General Status Byte, with the Illegal Command Bit equal to one, shall be returned to the host by the Parameter Byte of the command sequence.

This command shall set the Attention Condition.

#### 11.8.2.1.2 Clear Fault (Command Code 01 Hex)

This command shall cause fault status bits of the selected drive to be reset, provided the fault condition has passed, see Tables 4-8, 4-9, and 4-11. If the fault condition persists the appropriate status bit shall continue to be equal to one. The General Status Byte, cleared of previous fault status, shall be returned by the Parameter Byte of the command sequence.

The Clear Fault Command shall also reset the Attention Condition caused by the fault condition, again only if the fault condition no longer exists.

#### 11.8.2.1.3 Clear Attention (Command Code 02 Hex)

This command shall cause the Attention Condition to be reset in the selected drive. The General Status Byte shall be returned by the Parameter Byte of the command sequence.

If the error or other condition that caused the Attention Condition persists, the Attention Condition shall not be set again. If, however, the condition is reset and then the error reoccurs, the Attention Condition shall be set again.

This command shall reset the Normal Complete Bit in the General Status and the Initial State Bit, the Ready Transition Bit and the Drive Attribute Table Modified Bit in Sense Byte 2.

#### 11.8.2.1.4 Seek (Command Code 03 Hex)

This command shall cause the selected drive to seek to the cylinder identified as the target cylinder by the Load Cylinder Address Commands (see Section 5.4.1.1.3). The General Status Byte shall be returned to the host by the

Parameter Byte of the command sequence.

The General Status Byte, which is returned by the Parameter Byte of this command or by a Report General Status Command during the execution of the Seek shall have the Busy Executing Bit set.

The Seek Command shall set the Attention Condition and the Illegal Parameter Bit in the General Status Byte if the target cylinder address is outside the cylinder address range of the drive. The KENNEDY models 6172, and 6173 each have 614 cylinders.

Upon completion of any seek (including a zero length seek) the drive shall set the Attention Condition.

If the drive cannot complete the seek correctly or within 200 milliseconds, a self-initiated rezero operation shall be performed. This shall cause the Busy Signal to become active until the end of this rezero cycle. The Seek Error Bit in Sense Byte 1 and the Attention Condition shall be set in this case.

If the self-initiated rezero operation also fails, the Not Ready Bit in the General Status Byte shall be set. In this case a Rezero Command (see 11.8.2.1.5) only can be used to recover from this error condition.

The Busy Signal shall not be set during this command, unless the Seek Busy Jumper (see Section 11.4.7) is installed.

This command shall return the Offset Control to No Offset and the Read Control to Nominal Strobe timing.

Any seek, including a zero length seek, if performed by a drive being in an Offset State, shall last approximately 3.5 milliseconds longer until completion.

If Immediate Commands are issued to a drive which performs a seek operation, the seek times indicated in the section 1 of this specification may be prolonged by the time needed to handle the handshake sequence of these commands.

If Time Dependent Commands are issued during this command, or if Read Gate or Write Gate are active when this command is issued, or if the Not Ready Bit in the General Status is set, the Command Reject Bit in Sense Byte 1 and the Attention Condition shall be set.

#### 11.8.2.1.5 Rezero (Command Code 04 Hex)

This command shall cause the selected drive to position the heads over cylinder zero and reset Read Control to Nominal Strobe and Track Offset Control to No Offset. The General Status Byte shall be returned to the host by the Parameter Byte of the command sequence.

This Command shall reset the Guard Band Error Bit and the Outer Stop Bit in Sense Byte 3.

This command shall be used to recover from a Seek Error condition, when the self-initiated rezero operation had failed (i. e. when Not Ready was the consequence of a seek operation, see Section 11.8.1.2.4).

This command shall set the Busy Signal.

Upon the completion of the positioning of the heads over cylinder zero the drive shall set the Attention Condition.

The maximum time for a Rezero Command shall be 1700 milliseconds, the nominal time is 500 milliseconds from cylinder 613 and 20 milliseconds from cylinder zero.

If this command is issued when the Speed Error Bit in Sense Byte 1 is set or Write Gate is active, the Command Reject Bit in General Status and the Attention Condition shall be set.

This command shall not reset the target cylinder and moving head address parameters.

#### 11.8.2.1.6 Report Sense Byte 2 (Command Code 0D Hex)

This command shall cause the selected drive to return Sense Byte 2 by the Parameter Byte of the command sequence. No other action shall be taken in the drive.

#### 11.8.2.1.7 Report Sense Byte 1 (Command Code 0E Hex)

This command shall cause the selected drive to return Sense Byte 1 by the Parameter Byte of the command sequence. No other action shall be taken in the drive.

#### 11.8.2.1.8 Report General Status (Command Code OF Hex)

This command shall cause the selected drive to return the General Status Byte by the Parameter Byte of the command sequence. This command shall not perform any other function in the drive and acts as a "no-op" in order to allow the host to monitor the drive's General Status Byte without changing any drive condition.

#### 11.8.2.2 Optional Commands with Parameter In

The following Optional Commands with Parameter In are implemented in the 6170 ANSI interface.

Issuance of other Optional Commands with Parameter In shall set the Attention Condition and the Illegal Command Bit in the General Status Byte.

##### 11.8.2.2.1 Report Drive Attribute (Command Code 10 Hex)

This command shall cause the selected drive to return a byte of information that is the Drive Attribute whose number was defined in the Load Attribute Number Command (see Section 11.8.1.2.1). The contents of the implemented Attributes is defined by Tables 4-5 and 4-7.

##### 11.8.2.2.2 Set Attention (Command Code 11 Hex)

This command shall cause the selected drive to set the Attention Condition. No other action shall be caused.

The General Status Byte shall be transferred to the host by the Parameter Byte of the command sequence.

##### 11.8.2.2.3 Selective Reset (Command Code 14 Hex)

This is a Time Dependent Command.

This command shall cause the selected drive to reach Initial State (see Section 11.7.2.1).

All resettable parameters, errors, and attentions shall be reset prior to the transfer of the General Status Byte, which is returned by the Parameter Byte of this command.

This command shall set the Busy Signal. During the process of reaching Initial State the drive shall become deselected.

When the Initial State is reached, the Initial State Bit in Sense Byte 2 shall be set. This shall cause the Attention Condition to be set.

The state of Spin Control shall not be affected by this command.

If this command is issued while a Seek Command is performed the Command Reject Bit in Sense Byte 1 and the Attention Condition shall be set.

#### 11.8.2.2.4 Seek to Outer Stop (Command Code 15 Hex)

This command shall cause the selected drive to seek to the outer mechanical stop to allow locking of the positioner prior to shipping the drive or the system, which contains the drive.

The General Status Byte shall be returned by the parameter portion of the command sequence.

Upon positioning the heads at the outer stop, the drive shall set the Attention Condition, the Not Ready Bit in the General Status Byte and the Outer Stop Bit in Sense Byte 3.

If the drive cannot successfully seek to the outer stop, it shall set the Seek Error Bit in Sense Byte 1 and the Attention Condition.

A Rezero Command shall revert the drive to normal operation, when this command was issued.

The maximum time for this command shall be 1200 milliseconds.

#### 11.8.2.2.5 Partition Track (Command Code 16 Hex)

This command shall cause the selected drive to reconfigure the arrangement of the Sector Pulse generation according to parameters received via the Load Bytes Per Sector Commands (see Section 11.8.1.2.6) and/or the Load Sector Pulses Per Track Commands (see Section 11.8.1.2.7).



If this command is issued while Read Gate or Write Gate are active or if Write Gate or Read Gate are made active while this command is executed, the Read/Write Violation Bit in the Sense Byte 1 and the Attention Condition shall be set. No write operation shall take place when this error occurs.

This command shall make the Busy Signal active. The maximum time for this command shall be 22 milliseconds.

Upon completion of the execution of this command, the Bytes Per Sector and the Sectors Per Track Attributes shall be updated to the new values, Bits 5 and 6 of the Attribute Byte Number OE Hex shall be reset, Bit 4 shall be set, if Bit 5 was set before, and the Attention Condition shall be set.

The Sector Signal shall be invalid during the execution of this command.

The Illegal Parameter Bit in the General Status Byte and the Attention Condition shall be set, if the resulting overall number of bytes exceeds the total number of Bytes Per Track.

For systems which require an additional Sector Pulse at the end of the last Sector, the following feature is provided:

If the Parameter of the Load Sector Pulses Per Track High Command is 80 Hex, the check for validity of the track configuration parameter set allows an additional Sector Pulse. An adequate number of Bytes Per Sector has to be chosen to allow this last Sector Pulse to occur prior to the Index Pulse.

#### 11.8.2.2.6 Report Cylinder Address Commands

These two commands shall cause the selected drive to return a byte of information that is part of a 16 bit number that indicates the cylinder address of the current position of the moving heads. This number shall not reflect the most recent cylinder address set by the Load Cylinder Address Commands (see Section 11.8.1.1.3) unless there has been an intervening Seek Command (see Section 11.8.2.1.4).

If executed during a seek operation, the information returned shall be the cylinder address, which the drive had before the Seek Command.

The information shall be transferred by the Parameter Byte of the command sequence.

11.8.2.2.6.1 Report Cylinder Address High (Command Code 29 Hex)

This command shall cause the selected drive to return a byte of information that is the most significant byte of a 16 bit number that indicates the cylinder address of the current position of the moving heads.

11.8.2.2.6.2 Report Cylinder Address Low (Command Code 2A Hex)

This command shall cause the selected drive to return a byte of information that is the least significant byte of a 16 bit number that indicates the cylinder address of the current position of the moving heads.

11.8.2.2.7 Report Read Permit Commands

These two commands shall cause the selected drive to return a byte of information which is part of a 16 bit number that indicates the minimum cylinder address accessible for read operations. This number is programmed by the Load Read Permit Commands (see Section 11.8.1.2.8).

The information shall be transferred by the Parameter Byte of the command sequence.

11.8.2.2.7.1 Report Read Permit High (Command Code 2B Hex)

This command shall return the most significant byte of the 16 bit read permit address.

11.8.2.2.7.2 Report Read Permit Low (Command Code 2C Hex)

This command shall return the least significant byte of the 16 bit read permit address.

#### 11.8.2.2.8 Report Write Permit Commands

These two commands shall cause the selected drive to return a byte of information that is part of a 16 bit number that indicates the minimum cylinder address accessible for write operations. This number is programmed by the Load Write Permit Commands (see Section 11.8.1.2.9).

The information shall be transferred by the Parameter Byte of the command sequence.

##### 11.8.2.2.8.1 Report Write Permit High (Command Code 2D Hex)

This command shall transfer the most significant byte of the 16 bit write permit address.

##### 11.8.2.2.8.2 Report Write Permit Low (Command Code 2E Hex)

This command shall transfer the least significant byte of the 16 bit write permit address.

#### 11.8.2.2.9 Report Test Byte (Command Code 2F Hex)

This command shall cause the selected drive to return a copy of the Test Byte transferred to the drive via the Load Test Byte Command (see Section 11.8.1.2.10).

If there was no previous Load Test Byte Command, the Test Byte shall be reported as zero.

The Test Byte shall be transferred by the Parameter Byte of the command sequence.

#### 11.8.2.3 KENNEDY Unique Commands

As these functions are not contained in the ANSI-proposed repertoire, they are implemented as KENNEDY Unique Commands.

#### 11.8.2.3.1 Report Sense Byte 3 (Command Code 30 Hex)

This command shall cause the selected drive to return Sense Byte 3 by the Parameter Byte of the command sequence. No other action shall be taken in the drive. See Section 11.8.4.4 for the Sense Byte 3 Bits.

#### 11.8.2.3.2 Report Diagnostic Results (Command Code 31 Hex)

This command shall cause the selected drive to return the Diagnostic Byte by the Parameter Byte of the command sequence. No other action shall be taken in the drive.

See Section 11.8.4.5 for the Diagnostic Byte Bits.

#### 11.8.2.3.3 Report Sense Byte 4 (Command Code 32 Hex)

This command shall cause the selected drive to return Sense Byte 4 by the Parameter Byte of the handshake sequence. No other action shall be taken in the drive.

Sense Byte 4 contains the actual Head Address as transferred by the Select Moving Head Commands.

#### 11.8.2.3.4 Report Sense Byte 5 (Command Code 33 Hex)

This command shall cause the selected drive to return Sense Byte 4 by the Parameter Byte of the handshake sequence. No other action shall be taken in the drive.

Sense Byte 5 allows reporting of drive internal status. The bits are defined as follows:

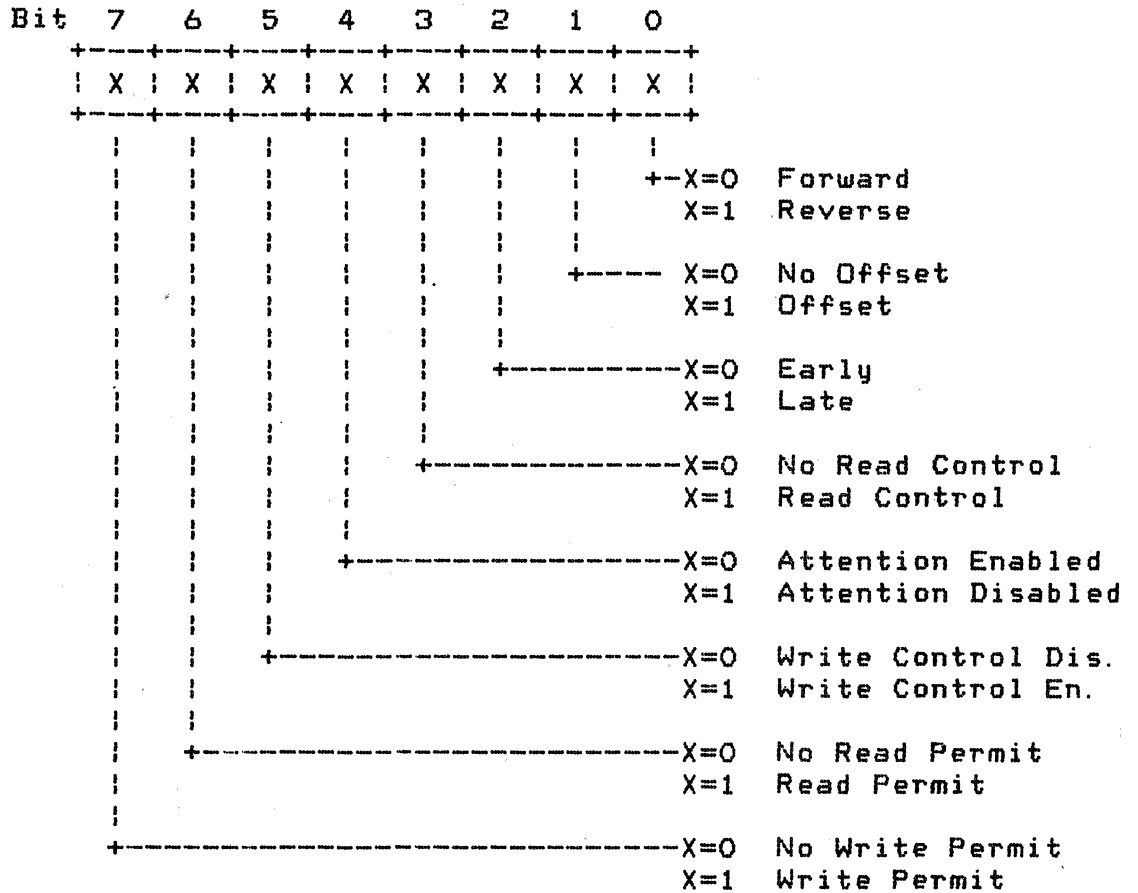


Table 4-5  
Drive Attributes

<u>Attribute</u>	<u>Number</u>	<u>Parameter</u>
User ID	00 Hex	User defined
Model ID High	01 Hex	See Section 5.4.3.2
Model ID Low	02 Hex	See Section 5.4.3.3
Revision ID	03 Hex	See Section 5.4.3.4
Device Type ID	0D Hex	See Section 5.4.3.5
Table Modification	0E Hex	See Section 5.4.3.6
Table ID	0F Hex	See Section 5.4.3.7
Bytes Per Track High	10 Hex	MSB of # of Bytes
Bytes Per Track Medium	11 Hex	MedSB of # of Bytes
Bytes Per Track Low	12 Hex	LSB of # of Bytes
Bytes Per Sector High	13 Hex	MSB of # of Bytes
Bytes Per Sector Medium	14 Hex	MedSB of # of Bytes
Bytes Per Sector Low	15 Hex	LSB of # of Bytes
Sector Pulses Per Track High	16 Hex	MSB of # of Sect. Pulses
Sector Pulses Per Track Med	17 Hex	MedSB of # Sect. Pulses
Sector Pulses Per Track Low	18 Hex	LSB of # of Sect. Pulses
Sectoring Method	19 Hex	Sectoring Method
Number of Cylinders High	20 Hex	MSB of # of Cylinders
Number of Cylinders Low	21 Hex	LSB of # of Cylinders
Number of Moving Heads	22 Hex	Number of Moving Head s
Number of Fixed Heads	23 Hex	Number of Fixed Heads
Select Head Implementation	24 Hex	See Section 5.4.3.15
Encoding Method #1	30 Hex	Encoding Method
Preamble #1 Length	31 Hex	Number of Bytes
Preamble #1 Pattern	32 Hex	Preamble Pattern
Sync #1 Pattern	33 Hex	Sync Pattern
Postamble #1 Length	34 Hex	Number of Bytes
Postamble #1 Pattern	35 Hex	Postamble Pattern
Gap #1 Length	36 Hex	Number of Bytes
Gap #1 Pattern	37 Hex	Gap Pattern
Encoding Method #2	40 Hex	Encoding Method
Preamble #2 Length	41 Hex	Number of Bytes
Preamble #2 Pattern	42 Hex	Preamble Pattern
Sync #2 Pattern	43 Hex	Sync Pattern
Postamble #2 Length	44 Hex	Number of Bytes
Postamble #2 Pattern	45 Hex	Postamble Pattern
Gap #2 Length	46 Hex	Number of Bytes
Gap #2 Pattern	47 Hex	Gap Pattern

All unused bits in the Attributes shall be zero (0).

All Attributes except 00 Hex, 0E Hex, 33 Hex, and 43 Hex shall be read only.

Table 4-6  
Sector Sizes Selectable by Jumpers  
 (This Table is valid for Models 6172 and 6173)

Sector Jumpers				# of Sectors	# of Sect. Pulses	Bytes per Sector	
IS3	IS2	IS1	IS0				
-	-	-	-	141	140	94	64+ 30
-	-	-	*	85	84	156	128+ 28
-	-	*	-	82	81	162	128+ 34
-	-	*	*	78	77	170	128+ 42
-	*	-	-	76	75	174	128+ 46
-	*	-	*	47	46	282	256+ 26
-	*	*	-	46	45	290	256+ 34
-	*	*	*	45	44	296	256+ 40
*	-	-	-	44	43	302	256+ 46
*	-	-	*	24	23	556	512+ 44
*	-	*	-	23	22	580	512+ 68
*	-	*	*	12	11	1112	1024+ 88
*	*	-	-	6	5	2224	2048+176
*	*	-	*	1	0	13344	full track

\* Indicates jumper installed

- indicates jumper missing

The other combinations of jumpers are reserved for future use.

The numbers in this table are decimal.

Note that in the reporting of the Jumpers in the Model ID High Attribute (see Section 11.8.3.2) a missing jumper equals to a "ONE"-bit.

Table 4-7  
Drive Attributes for Different Models  
 (Values in Hex)

Attrib.		KENNEDY 6170 Model			
		6171	6172	6173	
No.	Hex	Attribute			
00		User ID	00*	00*	00*
01		Model ID High	X	X	X
02		Model ID Low	00	01	02
03		Revision ID	XX	XX	XX
0D		Device Type	01	01	01
0E		Table Modification	40*	40*	40*
0F		Table ID	01	01	01
10		Bytes Per Track High	00	00	00
11		Bytes Per Track Medium	34	34	34
12		Bytes Per Track Low	20	20	20
13		Bytes Per Sector High	**	**	**
14		Bytes Per Sector Medium	**	**	**
15		Bytes Per Sector Low	**	**	**
16		Sectors Per Track High	**	**	**
17		Sectors Per Track Medium	**	**	**
18		Sectors Per Track Low	**	**	**
19		Sectoring Method	01	01	01
20		Number of Cylinders High	02	02	02
21		Number of Cylinders Low	66	66	66
22		Number of Moving Heads	01	03	05
23		Number of Fixed Heads	00	00	00
24		Select Head Implementation	02	02	02
30		Encoding Method #1	00	00	00
31		Preamble #1 Length	08	08	08
32		Preamble #1 Pattern	00	00	00
33		Sync #1 Pattern	00*	00*	00*
34		Postamble #1 Length	00	00	00
35		Postamble #1 Pattern	00	00	00
36		Gap #1 Length	01	01	01
37		Gap #1 Pattern	00	00	00
40		Encoding Method #2	00	00	00
41		Preamble #2 Length	08	08	08
42		Preamble #2 Pattern	00	00	00
43		Sync #2 Pattern	00*	00*	00*
44		Postamble #2 Length	00	00	00
45		Postamble #2 Pattern	00	00	00
46		Gap #2 Length	01	01	01

\* These Attributes can be changed by the host via Load Drive Attribute Commands. The values given are for the Initial State.



\*\* These values are set according to Table 4-6 upon reaching Initial State and may be changed by the host via the Load Bytes Per Sector and the Load Sectors Per Track Commands, followed by a Partition Track Command.

X Depending on jumper setting. See Section 11.8.3.2.

XX Binary number of revision level.

### 11.8.3 Drive Attribute Commands

These optional commands allow the host to manage the drive's mass memory configuration. The host can interrogate each drive on the daisy chain bus to determine each drive's attributes. The host may then modify attributes of the drives to optimize parameters of the subsystem. Device type, model IDs, etc. are also provided.

The Drive Attribute Commands are:

Load Attribute Number, Load Drive Attribute, and Report Drive Attribute.

They are used to load and/or report drive attributes, but do not cause any operation that affects the characteristics of the drive. All Drive Attribute Commands are optional.

The Parameter Byte transferred with the Load Attribute Number Command is used as a number to select a Drive Attribute. This number remains valid for all subsequent Load and Report Drive Attribute Commands until changed by another Load Attribute Command.

If for a received number no attribute is assigned or the function is not implemented in the 6170 ANSI interface, the Attention Condition and the Illegal Command Bit in the General Status Byte shall be set.

The Load Drive Attribute Command shall set the selected attribute to the value transferred with the Parameter Byte. If the selected attribute can be read only and not be altered, the Attention Condition and the Illegal Command Bit in the General Status Byte shall be set.

The Report Attribute Command shall cause the selected drive to return the current value of the selected attribute. This command shall work for all implemented attributes (see Table 4-5).



11.8.3.4 Revision ID (Number 03 Hex)

This attribute is a read only byte that KENNEDY shall set to a value to identify the revision level of the drive.

11.8.3.5 Device Type ID (Number 0D Hex)

This attribute is a read only byte that identifies the drive as defined below:

01 Hex = Non-removable disk

11.8.3.6 Table Modification (Number 0E Hex)

The purpose of this byte is to permit an orderly modification of the Attribute Table (see Table 4-5), especially in a multi-host environment.

During the Initial State generation the drive initializes the Attribute Table. When the table is initialized by the drive bit 7 is reset and bit 6 is set. A host may at its option modify any of the writeable attributes and if it does the drive must reset bit 6.

After all bytes have been modified the host sets bit 5 to indicate that the first modification process is complete.

When any subsequent byte, except number 0E Hex, is modified, bit 5 is reset and bit 4 is set. After the host has modified the byte(s) it must execute a Load Drive Attribute Command with number 0E Hex selected. This command shall set bit 5. When either bit 7 or bit 4 is equal to one or no bit is set, the Attribute Table is partially modified and is not safe to use. Bit 5 is set to establish that the table values have been modified and are safe to use. As long as bit 6 remains set the table contains the initial values set by the drive.

This attribute is defined as follows:

Bit	7	6	5	4	3	2	1	0
	1	1	1	1	0	0	0	0

Bit 7 = One: The Attribute Table is being modified by the drive. This bit is set by the drive and is reset by the drive upon completion of the modification process (this is for reference only; during the Initialization Sequence the KENNEDY ANSI has the Busy Signal set).

Bit 6 = One: The drive attribute values have not been modified. This bit is set by the drive upon attaining the Initial State and is reset when any Load Attribute Command (except to number OE Hex) or the Partition Track Command is executed.

Bit 5 = One: This bit, which is set by a Load Attribute Command to Number OE Hex, is used to signify that the Attribute Table is complete and ready for use. This bit is reset on any Load Drive Attribute Command except to number OE Hex. This bit can be set only by executing a Load Attribute Command to number OE Hex.

Bit 4 = One: This bit is set by the drive after a Load Drive Attribute Command or a Partition Track Command is executed after bit 5 was equal to one. This bit can only be reset by executing a Load Drive Attribute Command to number OE Hex. The setting of this bit causes Bit 5 of Sense Byte 2 (Attribute Table Modified) and the Attention Condition to be set.

Bits 0, 1, 2, and 3 shall be zero.

#### 11.8.3.7 Table ID (Number OF Hex)

This read only attribute defines the meaning of Attributes with Numbers 10 - FF Hex.

This attribute has always a value of 01 Hex, thus indicating that the values of Table 4-7 are valid and according to the ANSI standard.

#### 11.8.3.8 Bytes Per Track

The three read only "Bytes Per Track" attributes define a 24 bit number that represents the total number of unformatted bytes that occur between consecutive active going edges of Index Pulses. The KENNEDY models 6172, and 6173 have 13,344 Bytes Per Track. See Table 4-7 for the Hex values.

#### 11.8.3.8.1 Bytes Per Track High (Number 10 Hex)

This attribute is the most significant byte of the Bytes Per Track Attributes.

#### 11.8.3.8.2 Bytes Per Track Medium (Number 11 Hex)

This attribute is the medium significant byte of the Bytes Per Track Attributes.

#### 11.8.3.8.3 Bytes Per Track Low (Number 12 Hex)

This attribute is the least significant byte of the Bytes Per Track Attributes.

#### 11.8.3.9 Bytes Per Sector

The three read only 'Bytes Per Sector' attributes define a 24 bit number that represents the total number of bytes that occur between active going edges of Sector Pulses, and between the active going edge of the Index Pulse and the active going edge of the first Sector Pulse.

The three attribute bytes shall be initialized to the values as defined by the setting of the Sector Size Select Jumpers (see Table 4-6).

These attributes may be changed by a host using the Load Bytes Per Sector Commands (see Section 11.8.1.2.6) and a subsequent Partition Track Command (see Section 11.8.2.2.5).

#### 11.8.3.9.1 Bytes Per Sector High (Number 13 Hex)

This attribute is the most significant byte of the Bytes Per Sector Attributes.

#### 11.8.3.9.2 Bytes Per Sector Medium (Number 14 Hex)

This attribute is the medium significant byte of the Bytes Per Sector Attributes.

### 11.8.3.9.3 Bytes Per Sector Low (Number 15 Hex)

This attribute is the least significant byte of the Bytes Per Sector Attributes.

### 11.8.3.10 Sector Pulses Per Track

The three read only 'Sector Pulses Per Track' attributes define a 24 bit number that indicates the number of Sector Pulses between but excluding Index Pulses generated by the drive per revolution.

The three attribute bytes shall be initialized to the values as defined by the setting of the Sector Size Select Jumpers (see Table 4-6).

These attributes may be changed by a host using the Load Sector Pulses Per Track Commands (see Section 11.8.1.2.7) and a subsequent Partition Track Command (see Section 11.8.2.2.5).

#### 11.8.3.10.1 Sector Pulses Per Track High (Number 16 Hex)

This attribute defines the most significant byte of the Sector Pulses Per Track Attributes.

#### 11.8.3.10.2 Sector Pulses Per Track Medium (Address 17 Hex)

This attribute defines the medium significant byte of the Sector Pulses Per Track Attributes.

#### 11.8.3.10.3 Sector Pulses Per Track Low (Number 18 Hex)

This attribute defines the least significant byte of the Sector Pulses Per Track Attributes.

### 11.8.3.11 Sectoring Method (Number 19 Hex)

This read only attribute defines the sectoring method used in the drive.

The value of 01 Hex indicates that hard sectoring is used.

### 11.8.3.12 Number of Cylinders

The two read only 'Number of Cylinder' attributes define a 16 bit number that represents the number of cylinders implemented in the drive. This number is one greater than the maximum allowable cylinder address that can be addressed. The KENNEDY models 6172 and 6173 have 614 cylinders. See Table 4-7 for the Hex values.

#### 11.8.3.12.1 Number of Cylinders High (Number 20 Hex)

This attribute is the most significant byte of the Number of Cylinder Attributes.

#### 11.8.3.12.2 Number of Cylinders Low (Number 21 Hex)

This attribute is the least significant byte of the Number of Cylinder Attributes.

### 11.8.3.13 Number of Moving Heads (Number 22 Hex)

This read only attribute represents the number of moving heads implemented in the drive. This number is one greater than the maximum allowable head address that can be addressed.

The value of this attribute depends on the model and is determined by the Model Select Jumpers. See Table 4-7 for the values.

### 11.8.3.14 Number of Fixed Heads (Number 23 Hex)

This read only attribute represents the number of fixed heads implemented in the drive. The KENNEDY 6170 has no fixed heads, this attribute has always a value of zero.

### 11.8.3.15 Select Head Implementation (Number 24 Hex)

This read only attribute indicates which of the two Select Moving Head Commands (Command Code 44 Hex and 45 Hex) are accepted by the drive.

The value of 02 Hex indicates that both Command Codes are accepted.

#### 11.8.3.16 Header Encoding Method #1 (Number 30 Hex)

See Section 6 for the assignment of the format elements.

This read only attribute represents the header encoding method used for all fields labeled "#1". The value of zero indicates that Modified Frequency Modulation (MFM) is used.

#### 11.8.3.17 Preamble #1 Length (Number 31 Hex)

This read only attribute represents the minimum number of header preamble bytes required by the drive. The value of eight (08 Hex) indicates that at least 8 bytes are required by the drive.

#### 11.8.3.18 Preamble #1 Pattern (Number 32 Hex)

This read only attribute represents the pattern to be recorded in the header preamble bytes. The pattern is required to be all zeroes.

#### 11.8.3.19 Synchronization #1 Pattern (Number 33 Hex)

This writeable and readable attribute represents the pattern to be recorded in a one byte synchronization field following the preamble. The pattern shall be recorded starting with the most significant bit.

The drive requires no specific pattern, so the initial value of this attribute shall be zero.

#### 11.8.3.20 Postamble #1 Length (Number 34 Hex)

This read only attribute represents the minimum number of postamble bytes required by the drive. The value is zero and indicates that no postamble is required by the drive.

#### 11.8.3.21 Postamble #1 Pattern (Number 35 Hex)

This read only attribute represents the pattern to be recorded in the postamble bytes. The value of zero indicates that the drive does not require a specific postamble pattern.



#### 11.8.3.22 Gap #1 Length (Number 36 Hex)

This read only attribute represents the minimum number of bytes in the header gap (splice area) between postamble and the next preamble. The value of one (01 Hex) indicates that one byte is required by the drive.

#### 11.8.3.23 Gap #1 Pattern (Number 37 Hex)

This read only attribute represents the pattern to be recorded in the gap bytes. The value of zero indicates that no specific pattern is required by the drive.

#### 11.8.3.24 Data Encoding Method #2 (Number 40 Hex)

This read only attribute represents the data encoding method used in all fields labeled "#2". The value of zero indicates that Modified Frequency Modulation (MFM) is used.

#### 11.8.3.25 Preamble #2 Length (Number 41 Hex)

This read only attribute represents the minimum number of preamble bytes required by the drive. The value of eight (08 Hex) indicates that at least eight bytes are required.

#### 11.8.3.26 Preamble #2 Pattern (Number 42 Hex)

This read only attribute represents the pattern to be recorded in the preamble bytes. The value of zero indicates that an all zeroes pattern is required.

#### 11.8.3.27 Synchronization #2 Pattern (Number 43 Hex)

This writeable and readable attribute represents the pattern to be recorded in a one byte synchronization field following the preamble. The pattern shall be recorded starting with the most significant bit. The initial value of zero indicates that no specific pattern is required by the drive.

## 11.8.3.28 Postamble #2 Length (Number 44 Hex)

This read only attribute represents the minimum number of postamble bits required by the drive. The value of zero indicates that no postamble is required.

## 11.8.3.29 Postamble #2 Pattern (Number 45 Hex)

This read only attribute represents the pattern to be recorded in the postamble bytes. The value of zero indicates that no specific pattern is required by the drive.

## 11.8.3.30 Gap #2 Length (Number 46 Hex)

This read only attribute represents the minimum number of bytes in the gap (splice area) between postamble and the next preamble. The value of one (01 Hex) indicates that one byte is required by the drive.

## 11.8.3.31 Gap #2 Pattern (Number 47 Hex)

This read only attribute represents the pattern to be recorded in the gap bytes. The value of zero indicates that no specific pattern is required by the drive.

Table 4-8  
General Status Byte

<u>Bit #</u>	<u>Meaning</u>	<u>Mandatory/Optional</u>	<u>Method of Clearing</u>
0	Not Ready **	M	Self Clearing
1	Control Bus Error *	M	Clear Fault Command
2	Illegal Command *	M	Clear Fault Command
3	Illegal Parameter *	M	Clear Fault Command
4	Sense Byte 1	M	See Sense Byte 1
5	Sense Byte 2	M	See Sense Byte 2
6	Busy Executing	M	Self Clearing
7	Normal Complete *	M	Clear Attention Command

\* A zero to one transition of this bit shall set the Attention Condition.

\*\* The zero to one transition and the one to zero transition of this bit shall set the Attention Condition.

Table 4-9  
Sense Byte 1

<u>Bit #</u>	<u>Meaning</u>	<u>Mandatory/Optional</u>	<u>Method of Clearing</u>
0	Seek Error *	M	Clear Fault Cmd. **
1	Read/Write Fault *	M	Clear Fault Command
2	Power Fault *	O	Clear Fault Command
3	Read/Write Permit Violation *	O	Clear Fault Command
4	Speed Error *	O	Clear Fault Command
5	Command Reject *	M	Clear Fault Command
6	Other Err./Sense Byte 3****	O	Clear Fault Command
7	Diagnostic Errors ***	O	See Diagnostic Byte

\* A zero to one transition of this bit shall set the Attention Condition.

\*\* If this bit was set during a rezero operation, a Rezero Command shall reset the error condition.

\*\*\* This is a KENNEDY Unique Status Bit.

\*\*\*\* See Sense Byte 3.

Table 4-10  
Sense Byte 2

<u>Bit #</u>	<u>Meaning</u>	<u>Mandatory/Optional</u>	<u>Method of Clearing</u>
0	Initial State *	M	Clear Attention Command
1	Ready Transition *	M	Clear Attention Command
2	Unused	--	----
3	Unused	--	----
4	Unused	--	----
5	Drive Attribute Table Modified *	O	Clear Attention Command
6	Positioned Within Write Protected Area	M	Self Clearing
7	Unused	--	----

Note: The unused bits shall be reported as zero.

\* A zero to one transition of this bit shall set the Attention Condition.

Table 4-11  
Sense Byte 3 (KENNEDY Unique)

<u>Bit #</u>	<u>Meaning</u>	<u>Method of Clearing</u>
0	Spin Error *	Clear Fault Command
1	PLD Error or Write Gate and Not Fine Track ** *	Clear Fault Command
2	Guard Band Error *	Rezero Command
3	Positioner at Outer Stop * **	Rezero Command
4	Parking Lock Engaged *	Self Clearing
5	Reserved for future use	---
6	Reserved for future use	---
7	Reserved for future use	---

\* A zero to one transition of this bit shall set the Attention Condition.

\*\* This error shall also set the Not Ready Bit in the General Status Byte.

Table 4-12  
Diagnostic Results Byte (KENNEDY Unique)

<u>Bit #</u>	<u>Meaning</u>	<u>Method of Clearing</u>
0	RAM Error	*
1	PROM No. 1 Error	*
2	PROM No. 2 Error	*
3	Reserved for future use	---
4	Reserved for future use	---
5	Reserved for future use	---
6	Reserved for future use	---
7	Reserved for future use	---

\* These error bits cannot be cleared. They also cause the Not Ready Bit in General Status to be set.

Table 4-13  
Command Busy/Not Ready Relationships

Function	Busy Signal Status	Not Ready Status	Busy Executing Status
No Power	N/A	N/A	N/A
Idle Condition	0	0	0
Spinning Up *	1	(1)	(1)
Spinning Down*	1	1	(1)
Rezeroing *	1	0	(1)
Seeking *	0 ****	0	1
Offsetting *	1	0	(1)
Power Fault **	0	1	0
Error Conditions as Speed Error, Guard Band Error, PLO Error	0	1	0
Seek Error on Rezero Operation	0	1	0
Power Up Sequence and Diag. ***	1	(1)	(1)
R/W Operation	0	0	0
Partition Track *	1	0	(1)
Seek to Outer Stop *	1	1	(1)

\* Indicates Time Dependent Operation

\*\* Status is indicated for non-catastrophic power fault. Catastrophic power failure results in undefined state of the signals.

\*\*\* Including the Selective Reset Command.

\*\*\*\* If the Seek Busy Jumper (see Section 11.4.7) is installed, the Busy Signal shall be set during the Seek Command.

( ) Indicates that the status is not accessible because the Busy Signal is set.

#### 11.8.4 Fault Reporting

##### 11.8.4.1 General Status Byte

See Table 4-8.

###### 11.8.4.1.1 Bit 0 - Not Ready

A light emitting diode on the ANSI board indicates the Ready State (if lighted) at all times, regardless of the selection status.

The Not Ready Bit shall be set if the drive is unable to perform a Seek or Offset Command or a read/write operation. The drive shall accept a Rezero Command, if no Speed Error exists and the internal diagnostics have been performed successfully.

The Not Ready conditions are:

- Internal diagnostics during power up failed.
- Spindle speed not within tolerance
- Seek Error, when a rezero operation (either a Rezero Command or a self-initiated rezero operation) failed
- Power Fault
- Power Up sequence and internal diagnostics performing
- The 'first seek' after spinning up could not be achieved.
- A Seek to Outer Stop Command has been performed.
- One of the following errors has been detected: Guard Band Error, Write Gate and Read Gate active simultaneously, PLD Error or Write and not Fine Track.

Index, Sector, and Read/Reference Clock are invalid when the drive is not ready.

The Not Ready Bit shall be reset by a Clear Fault Command if the reason for Not Ready no longer exists.

The Not Ready Bit shall be cleared by a Rezero Command, if the condition was caused by one of the following events:

Failing Rezero operation, Seek to Outer Stop Command, or Guard Band Error.

The ready to not ready and not ready to ready transition shall set the Ready Transition Bit in Sense Byte 2 and the Attention Condition.

See Table 4-13 for the Busy/Not Ready relationship.

#### 11.8.4.1.2 Bit 1 - Control Bus Error

This bit shall be set if the drive detects a protocol or Control Bus Parity error during the transfer of a command or parameter such as:

- Control Bus Parity error (if enabled by the Control Bus Parity Checking Jumper)
- Command Request active and Bus Direction Out inactive
- The level of the Bus Direction Out Signal for the transfer of the Parameter Byte does not comply with Bit 6 of the Command Code (see Section 5.3.1.2.1).
- Two consecutive Parameter Cycles
- Time out condition on a handshake sequence
- Command Request and Parameter Request active simultaneously.

The drive shall not act upon the command transferred during a Command/Parameter cycle resulting in a Control Bus Error. If the Bus Direction Out Signal is inactive for the second byte and a Control Bus Error has been detected, the drive shall return the General Status Byte.

The Control Bus Error Bit shall be reset by the Clear Fault Command.

The detection of a Control Bus Error shall set the Attention Condition.

#### 11.8.4.1.3 Bit 2 - Illegal Command

This bit shall be set if the drive detects an illegal command such as:

- The command received is not implemented in the drive or not allowed by the configuration (e. g. Spin Command issued when the jumper for enabling the Spin Command is not installed).
- The drive detected a parity error in the Command Byte which shall also set the Control Bus Error Bit. The checking of Control Bus Parity can be enabled or disabled by the Control Bus Parity Checking Jumper (see Section 11.4.3).
- An attempt is made to write a read only attribute in the Attribute Table.
- An illegal Attribute Number has been selected.

This bit shall be set when a 'Report Illegal Command' Command is received.

The Illegal Command Bit shall be reset by the Clear Fault Command.

This error shall set the Attention Condition.

#### 11.8.4.1.4 Bit 3 - Illegal Parameter

This bit shall be set if the drive detects an illegal parameter or part of a parameter such as:

- The parameter is an address and exceeds the valid range (e. g. illegal head address).
- Any other illegal parameter value.
- The drive detected a parity error in the Parameter Byte which shall also set the Control Bus Error Bit. The checking of Control Bus Parity can be enabled or disabled by the Control Bus Parity Checking Jumper (see Section 11.4.3).

The Illegal Parameter Bit shall be reset by the Clear Fault command.

This error shall set the Attention Condition.



#### 11.8.4.1.5 Bit 4 - Sense Byte 1

This bit shall be generated by an "OR" function of all bits in the Sense Byte 1 status byte. The Sense Byte 1 Bit shall be reset if all bits of the Sense Byte 1 are zero.

#### 11.8.4.1.6 Bit 5 - Sense Byte 2

This bit shall be generated by an "OR" function of all bits in the Sense Byte 2 status byte. The Sense Byte 2 Bit shall be reset if all bits of the Sense Byte 2 are zero.

#### 11.8.4.1.7 Bit 6 - Busy Executing

This bit shall be set during the execution of a Seek Command, if the Seek Busy jumper (see Section 11.4.7) is not installed. All other Time Dependent Commands have the Busy Signal active during their execution, so that no status transfer is possible during their execution.

Note: This status bit is different from the Busy Signal (see Section 11.7.2.7).

#### 11.8.4.1.8 Bit 7 - Normal Complete

This bit shall be set if the drive has successfully completed a Time Dependent Command. See Tables 4-3 and 4-4.

The Normal Complete Bit shall be reset by the Clear Attention Command.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2 Sense Byte 1

See Table 4-9.

#### 11.8.4.2.1 Bit 0 - Seek Error

The Seek Error Bit shall be set if a head positioning command (Seek, Rezero, Seek to Outer Stop) cannot be completed successfully.

This Bit shall also be set if the automatic rezero operation included in the Initial Sequence cannot be completed successfully.

The time out condition for a Seek Command is 200 milliseconds and is 1700 milliseconds for a Rezero Command.

If a Seek Error is detected in a seek operation, an automatic rezero operation is initiated in the drive. Thus the heads are positioned on cylinder zero when a Seek Error is reported. During the rezero portion of this sequence the drive shall set the Busy Signal. The Attention Condition shall not be generated until the end of the rezero portion.

A Clear Fault Command or a Rezero Command shall reset this bit, if the automatic rezero operation was successful.

A Rezero Command shall reset this bit, if the error condition occurred during a Rezero Command or an automatic rezero operation, in which case the Not Ready Bit in the General Status was also set.

A zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2.2 Bit 1 - Read/Write Fault

This bit shall be set if the drive is not able to execute a read function or a write function or detects a fault during the reading or writing. Two kinds of faults are distinguished:

- a) Bit 1 and Bit 5 shall be set if the execution of a write function requested by making Write Gate active is prevented by one of the following conditions:
- Write Gate active and writing disabled by a Write Control Command (see Section 11.8.1.1.2).
  - Write Gate active and Offset (see Section 11.8.1.2.4).
- b) Bit 1 only shall be set if the drive detects a fault in its read/write section such as:
- Simultaneous selection of more than one head.
  - Write Gate active but no write current.
  - Write Gate and Read Gate active simultaneously

The Read/Write Fault Bit shall be reset by the Clear Fault Command.

A zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2.3 Bit 2 - Power Fault

This bit shall be set if the drive detects a failure such as overvoltage or undervoltage in one of its supply voltages.

This bit shall be reset by the Clear Fault Command if the power failure no longer exists and is non-catastrophic.

A zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2.4 Bit 3 - Read/Write Permit Violation

This bit shall be set if writing to the currently accessed track is not permitted (see Section 11.8.1.2.9) and Write Gate is active. No write operation shall take place if this error occurs.

This bit shall be set if reading the currently accessed track is not permitted (see Section 11.8.1.2.9) and Read Gate is active. The Read Data Lines shall be held static if this error occurs.

This bit shall be set if the Busy Executing Bit in the General Status Byte is set and Write Gate or Read Gate are active.

This bit shall be reset by the Clear Fault Command.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2.5 Bit 4 - Speed Error

This bit shall be set if the drive detects that the spindle speed is not within the specified tolerances (see the first part of this document).

This bit shall be reset by the Clear Fault Command if the spindle speed is within the specified tolerance.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2.6 Bit 5 - Command Reject

This bit shall be set if the drive received a command which it cannot execute at this time because of some interlocking condition or command sequence error.

This status bit may be set in combination with another status bit that defines the reason why the command was rejected.

- The drive is Not Ready and has received a command that cannot be executed (such as, Seek when the disk is not rotating).
- A Time Dependent Command is received when a seek operation is in progress.
- A Write Control Command is received during a write operation.
- A Load Write Permit Command is received during a write operation.
- A Load Read Permit Command is received during a read operation.

The Command Reject Bit shall be reset by the Clear Fault Command.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.2.7 Bit 6 - Other Errors/Sense Byte 3

This bit is KENNEDY unique.

This bit shall be generated by an "OR" function of all bits in the Sense Byte 3 status byte. The Sense Byte 3 Bit shall be reset when all bits of the Sense Byte 3 are zero.

#### 11.8.4.2.8 Bit 7 - Diagnostic Byte

This bit is KENNEDY unique.

This bit shall be generated by an "OR" function of all bits in the Diagnostic Byte status byte. The Diagnostic Byte Bit shall be reset when all bits of the Diagnostic Byte are zero.

#### 11.8.4.3 Sense Byte 2

See Table 4-10.

#### 11.8.4.3.1 Bit 0 - Initial State

This bit shall be set if an initialize procedure has been entered and the procedure has been completed. The Initial State Bit shall be reset by a Clear Attention Command.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.3.2 Bit 1 - Ready Transition

This bit shall be set if a one to zero or zero to one transition has occurred on the Not Ready Bit (see Section 11.8.4.1.1). The Ready Transition Bit shall be reset by a Clear Attention Command.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.3.3 Bit 5 - Drive Attribute Table Modified

This bit shall be set if Bit 4 of the Table Modification Attribute Number OE Hex (see Section 11.8.3.6) transitions to a one. This bit shall be reset by a Clear Attention Command.

The zero to one transition of this bit shall set the Attention Condition.

#### 11.8.4.3.4 Bit 6 - Positioned Within Write Protected Area

This bit shall be set by the drive whenever Write Control (see Section 11.8.1.1.2) has placed the drive in the write disable state.

This bit shall be set if the external write protect switch (see Section 11.5) is set to write protect and a subsequent Seek, Rezero, Read Permit, Write Permit or Selective Reset Command has been performed. Note that the write protection by this switch is enabled immediately.

This bit shall be set by the drive whenever the heads are positioned within an area that has been defined as write protected by a Load Write Permit Command (see Section 11.8.1.2.9) and the drive is write enabled.

This bit shall be reset if the heads are positioned outside the write protected area and writing is enabled by a Write Control Command.

#### 11.8.4.3.5 Bits 2, 3, 4, and 7

Bits 2, 3, and 4 are reserved and shall be reported as zero.

#### 11.8.4.4 Sense Byte 3

This Sense Byte is a KENNEDY unique feature. It reports additional errors which are not covered by Sense Byte 1 or Sense Byte 2.

To transfer this byte the Report Sense Byte 3 Command (see Section 11.8.2.3.1) shall be used.

##### 11.8.4.4.1 Bit 0 - Spin Error

This bit shall be set if during a spin up operation the disks do not come up to speed within 15 seconds.

This bit shall be set if during a spin down operation the disks do not slow down after 15 seconds.

The zero to one transition of this bit shall set the Attention Condition.

This bit shall be cleared by the Clear Fault Command.

##### 11.8.4.4.2 Bit 1 - PLD Error or Write Gate and Not Fine Track

This bit shall be set if the PLD in the servo circuit of the drive is not operating correctly.

This bit shall be set if Write Gate is active and the heads are not positioned in the center of a track.

The zero to one transition of this bit shall set the Not Ready Bit in the General Status Byte and the Attention Condition.

This bit shall be cleared by the Rezero Command.

#### 11.8.4.4.3 Bit 2 - Guard Band Error

This bit shall be set if a drive detects that the heads are not positioned over the data area except during a Rezero Command or a Seek to Outer Stop Command. Upon detection of this error an automatic rezero operation shall be performed. This shall set the Busy Signal for the duration of the rezero.

This error shall set the Not Ready Bit in General Status and the Attention Condition.

A Rezero command shall clear the Guard Band Error Bit.

#### 11.8.4.4.4 Bit 3 - Outer Stop

This bit shall be set if a Seek to Outer Stop Command has been performed. This shall also set the Not Ready Bit in the General Status.

#### 11.8.4.4.5 Bit 4 - Park Lock

This bit is applicable for drives with the parking lock installed.

This bit shall be set when the positioner parking lock is engaged. The parking lock is engaged when the drive motor is shut off.

#### 11.8.4.4.6 Bits 5, 6, and 7 - Reserved

These bits are reserved for future use and shall be reported as zero.

#### 11.8.4.5 Diagnostic Results Byte

The Diagnostic Results Byte is a KENNEDY unique feature. It reports the result of built-in drive diagnostics.

To transfer this byte the Report Diagnostic Results Command (see Section 11.8.2.3.2) shall be used.



#### 11.8.4.5.1 Bit 0 - RAM Error

This bit indicates a malfunction of the RAM circuit within the drive.

The drive shall not become ready if this error occurs.

This error cannot be cleared.

#### 11.8.4.5.2 Bit 1 - PROM No. 1 Error

This bit indicates a malfunction of the PROM No. 1 memory circuit within the drive.

The drive shall not become ready if this error occurs.

This error cannot be cleared.

#### 11.8.4.5.3 Bit 2 - PROM No. 2 Error

This bit indicates a malfunction of the PROM No. 2 memory circuit within the drive.

The drive shall not become ready if this error occurs.

This error cannot be cleared.

#### 11.8.4.5.4 Bits 3,4,5,6, and 7 - Reserved

These bits are reserved for future expansion of the diagnostics and shall be reported as zero.

### 11.9 Timing Specification

The timing characteristics described in the following sections are referenced to the signals at the drive interface connector. The controller timing shall be designed to accommodate cable delays and signal skew within the cable.

Note: This section takes precedence, with respect to actions and timing, over all preceding sections. All waveforms in the timing diagrams show the voltage levels of the signals. A "-" in front of a signal name indicates a "LOW"-active, "HIGH"-inactive signal. A "+" in front of a signal name indicates a "HIGH"-active, "LOW"-inactive signal.

### 11.9.1 Control Bus Timing

#### 11.9.1.1 Selection Timing

The active going edge of the Select Out/Attention In Strobe shall be used to clock the select information on the dedicated Control Bus Line into the drive. A successful selection shall be acknowledged by making Bus Acknowledge active. In the controller the inactive going edge of the Select Out/Attention In Strobe signal shall be used to sample the Bus Acknowledge signal. If Bus Acknowledge is not active within the specified time, the controller shall assume that the desired drive does not exist or is inoperable. The state of the Busy signal indicates to the controller if the selected drive will accept commands and respond to the Control Bus handshake.

Deselecting all drives shall be accomplished by an active going edge of Select Out/Attention In Strobe with none of the Control Bus Lines active.

The select timing is defined in Figure 14-12.

#### 11.9.1.2 Attention Timing

In general the timing of the party line Attention signal (see Section 11.7.2.8) is asynchronous to the Control Bus signals. However, if a command error or parameter error is detected, the Attention Condition shall be set and if enabled the Attention signal shall be made active prior to the active going edge of Bus Acknowledge which is returned as a response to Parameter Request. All other events (completion or errors) shall make Attention (if enabled) active immediately, when they occur.

Attention shall be made inactive prior to the active going edge of Bus Acknowledge which is returned as a response to Parameter Request of a Clear Attention Command or Clear Fault Command. Attention shall not be made inactive by a Clear Fault Command if the error that caused Attention to be made active still exists.

To determine which one of the attached drives has caused the party line Attention Signal, the controller polls all drives simultaneously by making the Bus Direction Out signal inactive and changing the Select Out/Attention In Strobe from inactive to active. Each drive shall then immediately gate its internal Attention Condition onto its dedicated Control Bus line. Additionally, the selected drive, if any, shall make the Bus Acknowledge Signal active.

The Attention timing is defined in Figure 4-13.

#### 11.9.1.3 Control Bus Handshake Timing

The Control Bus handshake is performed by three interface signals: Command Request, Parameter Request, and Bus Acknowledge.

The Control Bus handshake timing is defined in Figures 4-14 and 4-15.

#### 11.9.2 Index and Sector Timing

The timing of the Index signal and the Sector signal is shown in Figure 4-16. There is one and only one Index Pulse per revolution. The Sector Pulses are used to divide a track into equal length sectors. The drive inhibits the Sector Pulse during the Index Pulse such that a Sector Pulse is not transmitted at index time.

The Index signal and the Sector signal are enabled with drive selection. The Index signal and the Sector signal shall not be considered valid until at least 500 nanoseconds after the active going edge of the Select Out/Attention In Strobe signal which caused the selection of the drive.

The Index Pulse is not valid if the drive is not up to speed.

Sector Pulses are not valid if the drive is Not Ready or if a Partition Track Command is being performed.

#### 11.9.3 Reference Clock Timing

The Reference Clock timing is defined in Figure 4-17.

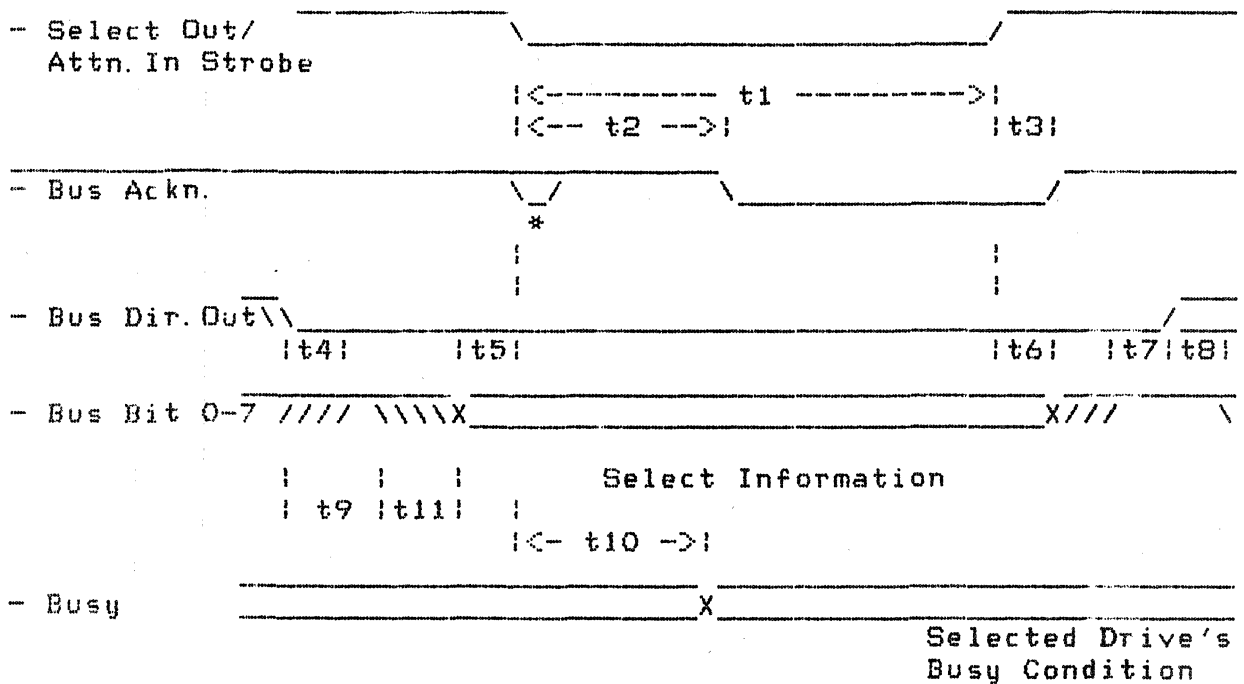
#### 11.9.4 Read Timing

The read timing is defined in Figure 4-18.

#### 11.9.5 Write Timing

The write timing is defined in Figure 4-19. The Write Clock shall be generated in the controller from the Reference Clock. The delay time from the Reference Clock to Write Clock is a function of cable length and circuit delays. The phase difference between the two signals shall be constant during the complete write operation. The Write Data signal and the Write Clock signal shall be synchronized as defined in Figure 4-19. The Read Data signal is undefined during a write operation, but shall be held static.

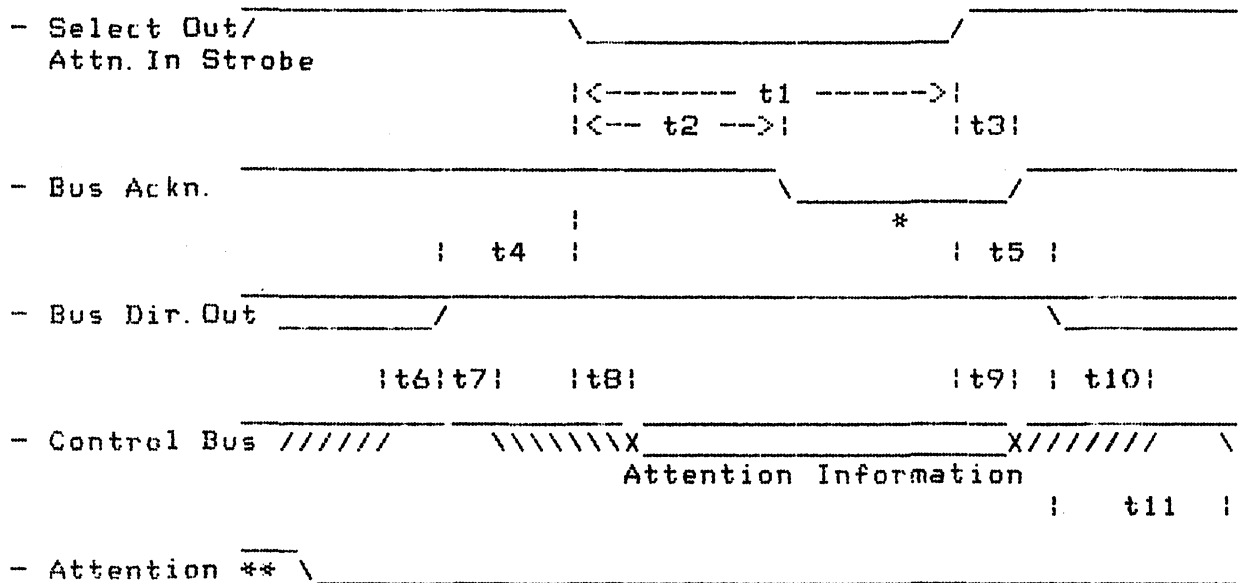
Figure 4-12  
Select Timing



\* Glitch possible - due to previously selected drive.  
To avoid glitch first deselect all drives and then reselect.

Label	Description	min.	max.	Units
t1	Select/Attention Strobe width	500	---	nanoseconds
t2	Bus Acknowledge invalid	0	300	nanoseconds
t3	Bus Acknowledge hold time	0	100	nanoseconds
t4	Drive - Contr. Bus release time	0	100	nanoseconds
t5	Control Bus - Data setup time	100	---	nanoseconds
t6	Control Bus - Data hold time	0	---	nanoseconds
t7	Controller - Control Bus release time	100	---	nanoseconds
t8	Drive - Control Bus access time	0	---	nanoseconds
t9	Controller - Control Bus access time	100	---	nanoseconds
t10	Busy invalid	0	300	nanoseconds
t11	Drive - Controller transition time	0	---	nanoseconds

Figure 4-13  
Attention Timing

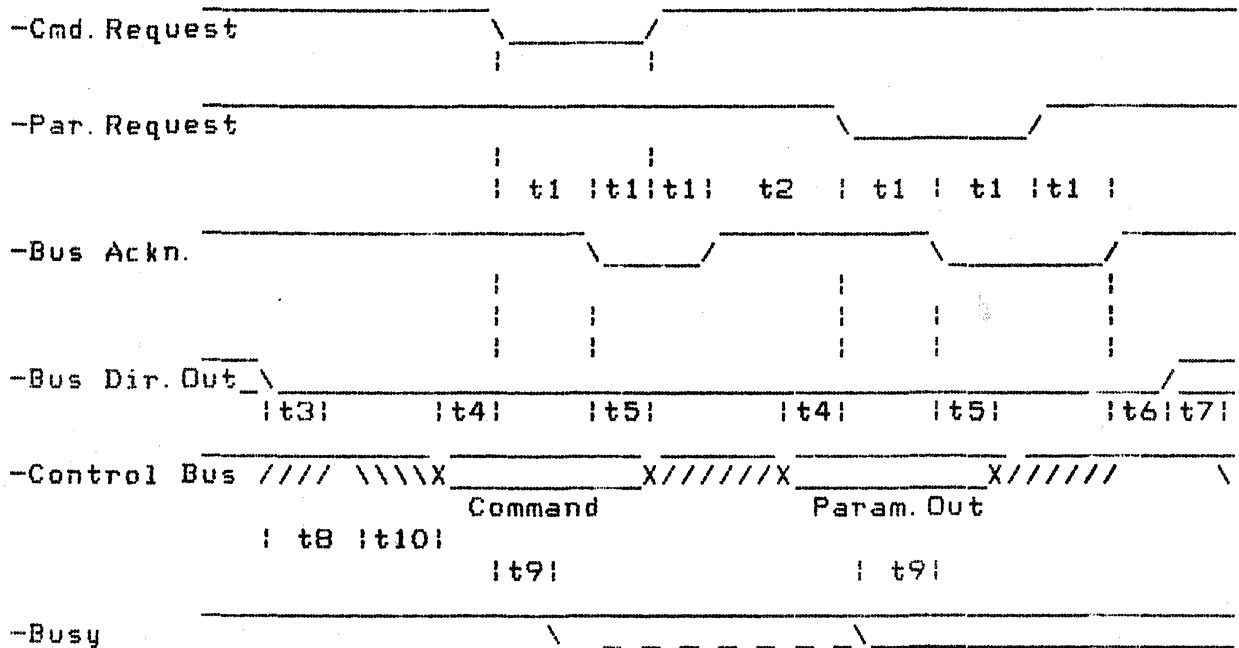


\* Active only if there is a previously selected drive, inactive if all drives are deselected.

\*\* Some drives may have Attention active causing the controller to perform the Attention timing sequence.

Label	Description	min.	max.	Units
t1	Select/Attention Strobe width	500	---	nanoseconds
t2	Bus Acknowledge invalid *	0	300	nanoseconds
t3	Bus Acknowledge hold time	0	100	nanoseconds
t4	Bus Direction Out - setup time	100	---	nanoseconds
t5	Bus Direction Out - hold time	0	---	nanoseconds
t6	Controller - Control Bus release time	100	---	nanoseconds
t7	Drive - Control Bus access time	0	---	nanoseconds
t8	Attention Information invalid	0	100	nanoseconds
t9	Attention Information hold time	0	---	nanoseconds
t10	Drive - Contr. Bus release time	0	100	nanoseconds
t11	Controller - Control Bus access time	100	---	nanoseconds

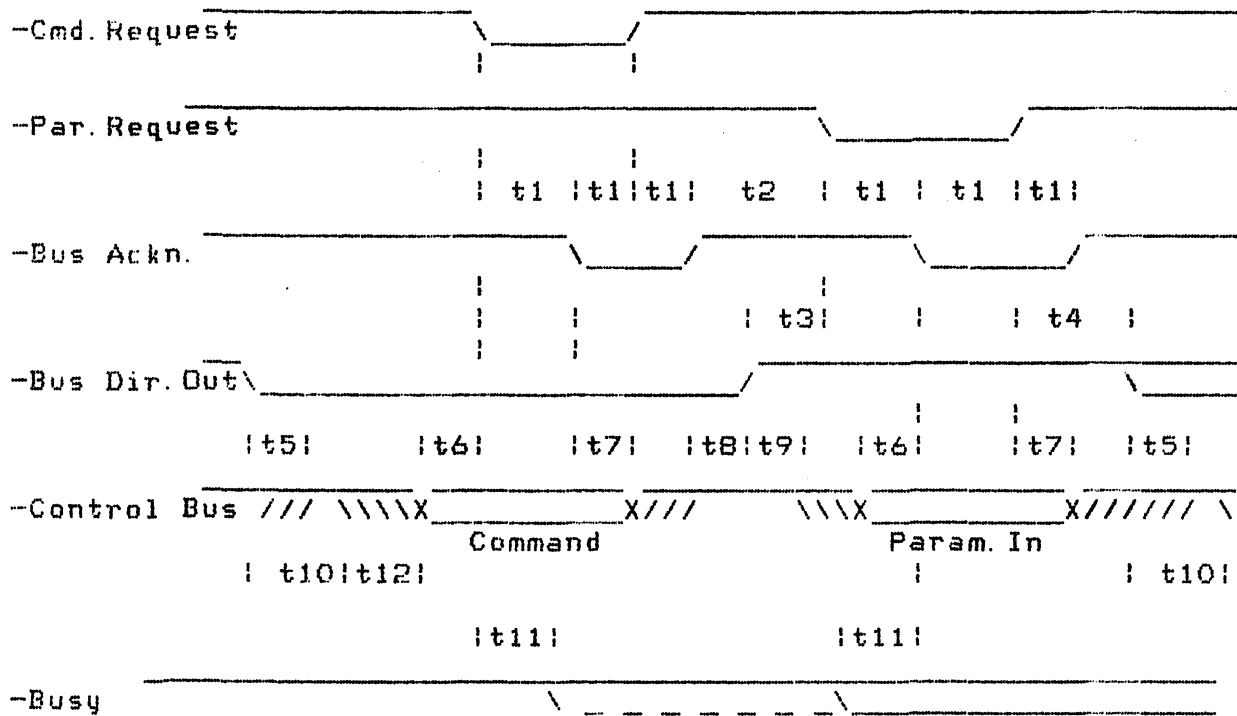
Figure 4-14  
Command/Parameter Out Sequence



Label	Description	min.	max.	Units
t1	Handshake response time	0	10 *	milliseconds
t2	Spacing	0	10 *	milliseconds
t3	Drive - Control Bus release time	0	100	nanoseconds
t4	Control Bus - Data setup time	100	---	nanoseconds
t5	Control Bus - Data hold time	0	---	nanoseconds
t6	Controller - Control Bus release time	100	---	nanoseconds
t7	Drive - Control Bus access time	0	---	nanoseconds
t8	Controller - Control Bus access time	100	---	nanoseconds
t9	Busy setup time	0	*	nanoseconds
t10	Drive - Controller transition time	0	---	nanoseconds

\* This value is valid only if the Busy Signal is not active at the beginning of the sequence.

Figure 4-15  
Command/Parameter In Sequence

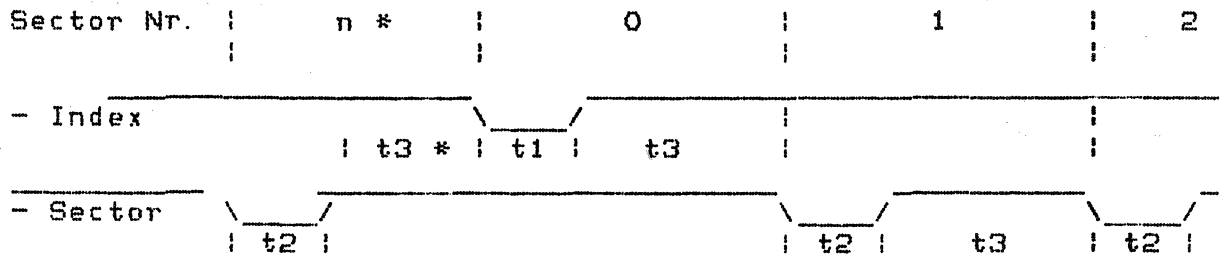


Label	Description	min.	max.	Units
t1	Handshake response time	0	10 *	milliseconds
t2	Spacing	0	10 *	milliseconds
t3	Bus Direction Out - setup time	100	---	nanoseconds
t4	Bus Direction Out - hold time	0	---	nanoseconds
t5	Drive - Control Bus release time	0	100	nanoseconds
t6	Control Bus - Data setup time	100	---	nanoseconds
t7	Control Bus - Data hold time	0	---	nanoseconds
t8	Controller - Control Bus release time	100	---	nanoseconds
t9	Drive - Control Bus access time	0	---	nanoseconds
t1	Controller - Control Bus access time	100	---	nanoseconds
t11	Busy setup time	0*	---	nanoseconds
t12	Drive - Controller transition time	0	---	nanoseconds

\* This value is valid only if the Busy Signal is not active at the beginning of the sequence.



Figure 4-16  
Index/Sector Timing



Label	Description	min.	typ.	max.	Units
t1	Index Pulse width	2.4	2.5	2.6	microseconds
t2	Sector Pulse width	2.4	2.5	2.6	microseconds
t3	Interpulse spacing	0.5	---	---	microseconds

\* The last sector may be shorter or longer than the other sectors, depending on the selected partitioning. See Section 11.10.4.

The distance between active going edges of two consecutive Index Pulses is defined by the rotational speed and shall be 16.67 milliseconds plus or minus 1 % for the KENNEDY drive models 6172 and 6173.

Figure 5.5-6  
Reference Clock Timing

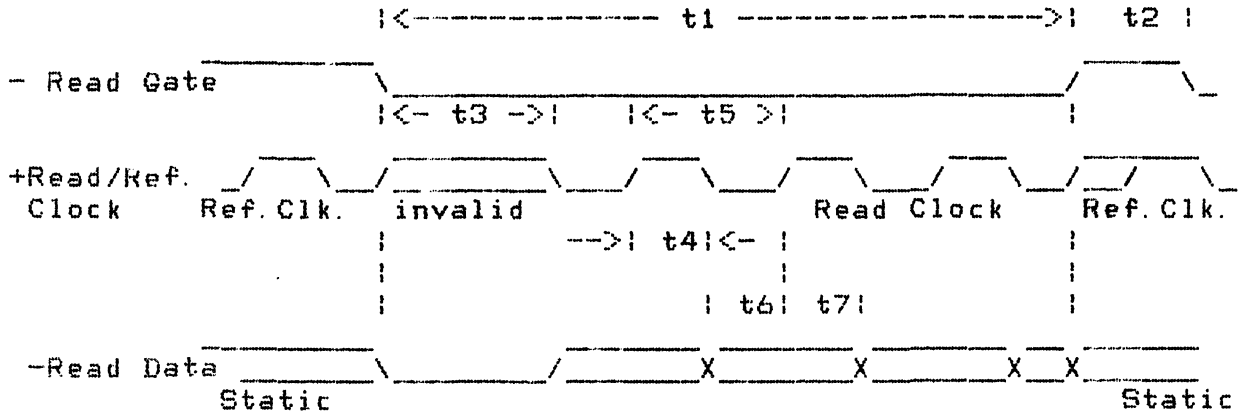


Label	Description	Min.	Typ.	Max.
t1	Reference Clock active time	0.4*tp	0.5*tp	0.6*tp
t2	Reference Clock period	0.95*tp	1.0*tp	1.05*tp

tp nominal Reference Clock period for models 6172 and 6173 shall be 156 nanoseconds.

\* = Multiply

Figure 4-18  
Read Timing

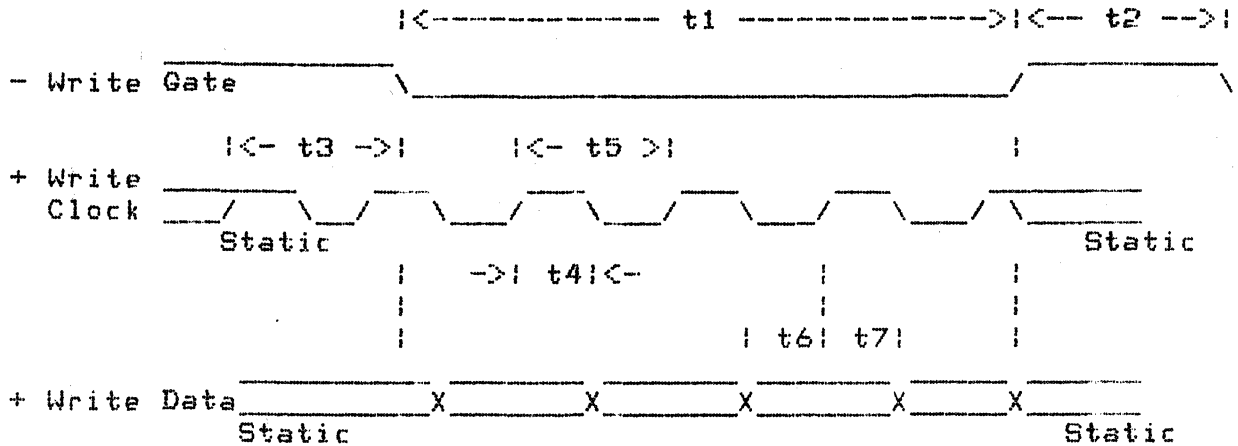


Label	Description	min.	typ.	max.	Units
t1	Read Gate active	0	---	---	microseconds
t2	Read Gate inactive	3*tp	---	---	---
t3	Read Gate to valid Read Data and Read Clock	6.75	7.5	8.25	microseconds
t4	Read Clock active time	0.4*tp	0.5*tp	0.6*tp	---
t5	Read Clock period	0.95*tp	1.0*tp	1.05*tp	---
t6	Read Data setup time	0.25*tp	---	---	---
t7	Read Data hold time	0.25*tp	---	---	---

tp The nominal Reference Clock period shall be 156 nano-seconds for the models 6172 and 6173.

\* = Multiply

Figure 4-19  
Write Timing



Label	Description	min.	typ.	max.
t1	Write Gate active	0	---	----
t2	Write Gate inactive	0	---	----
t3	Write Clock valid	tp	---	16*tp
t4	Write Clock active time	0.4*tp	---	0.6*tp
t5	Write Clock period	---	tp	----
t6	Write Data setup time	0.25*tp	---	----
t7	Write Data hold time	0.25*tp	---	----

tp The nominal Reference Clock period shall be 156 nano-seconds for the models 6172 and 6173.

Note: The first eight bytes of Write Data must be zeroes.

\* = Multiply

### 11.10 Formatting Considerations

Field lengths are indicated in bytes (one byte equal to 8 bits). This is no formatting restriction, because writing and reading is bit-serial.

#### 11.10.1 Sector Format

For the sector format one of the formats in Figure 4-22 is recommended. When format B is used, the header must also be rewritten, whenever data is to be recorded.



#### 11.10.2.3 Header Information

The header contains the address of the sector, usually cylinder, head and sector number.

It may contain additional information regarding the data integrity of the sector or of the track and an alternate address.

It is recommended to append cyclic redundancy check bytes or an error correction code to the header information.

#### 11.10.2.4 Gap #1 and Gap #2

These gaps provide the space needed to switch from write to read and read to write. Read Gate shall not be held active during this area.

Because the Reference Clock is derived from the servo surface, there is no need for a tolerance gap at the end of a sector.

#### 11.10.2.5 Data Information

This field contains the actual data.

It is recommended to append cyclic redundancy check bytes or an error correction code to the data information.

#### 11.10.2.6 Postamble #1 and Postamble #2

The postambles are used to provide extra read and write clocks for the serializer-deserializer circuit in the controller. They also may provide time for the controller to decide upon the next operation.

### 11.10.3 Format Examples

Two format examples are given. Example A shows a format with CRC (cyclic check characters), example B shows a format with ECC (error correction code).

	Example A	Example B	
Preamble #1	10	10	Bytes
Sync #1	1	1	Byte
Header Information	4	4	Bytes
CRC	2	-	Bytes
ECC	-	6	Bytes
Postamble	2	2	Bytes
Gap #1	1	1	Byte
Preamble #2	10	10	Bytes
Sync #2	1	1	Byte
Data Information	512	512	Bytes
CRC	2	-	Bytes
ECC	-	6	Bytes
Postamble	2	2	Bytes
Gap #2	1	1	Byte
<hr/>			
Total	548	556	Bytes

In both examples the 24-sector-format (see Table 4-6) would be used. In Example A any of the gaps or preambles would be increased to accommodate to the 556 bytes of sector length.

#### 11.10.4 Division of a Track Into Sectors

Either by using the Sector Size Select Jumpers (see Section 11.4.6) or by using the Load Sector Pulses Per Track Commands (see Section 11.8.1.2.7) and the Load Bytes Per Sector Commands (see Section 11.8.1.2.6) and a subsequent Partition Track Command, the track can be divided into sectors.

The spacing between the Index Pulse and the first Sector Pulse and between the Sector Pulses is equal and given by the number of Bytes Per Sector. Note that only even numbers of Bytes Per Sector are used.

The division of the number of Bytes Per Track (13,344 for KENNEDY models 6172 and 6173) by the number of Bytes Per Sector results in the number of sectors, which fit on a track. If there is a remainder in this division, then the last sector is longer than the other sectors.

For the possibility of having an additional Sector Pulse at the end of the last sector see Section 11.8.2.2.5.

Note that the minimum number of Sector Pulses Per Track is three.

#### 11.10.5 Typical Read Sequence

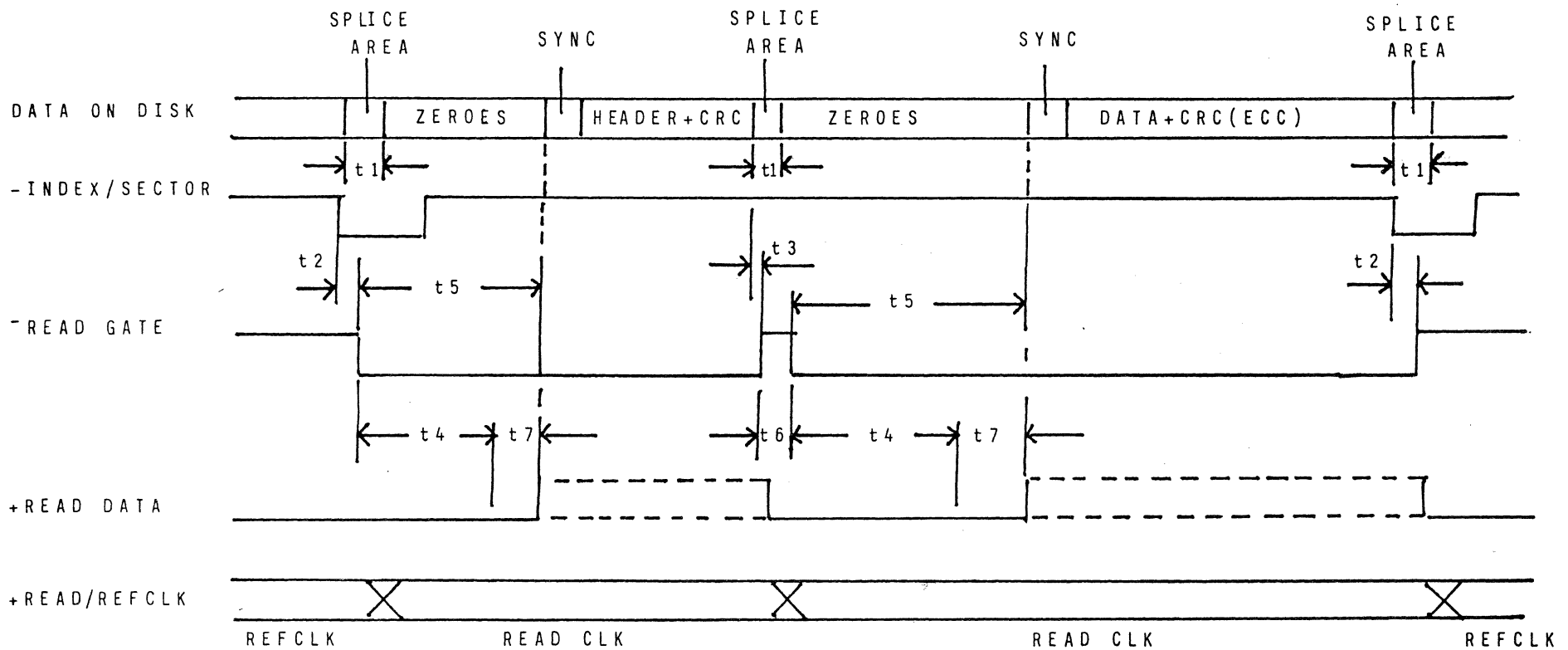
Figure 4-21 shows a typical read sequence.

Note that Read Gate may not be held active during the Gaps #1 and #2.

#### 11.10.6 Typical Write Sequence

Figure 4-22 shows a typical write sequence.

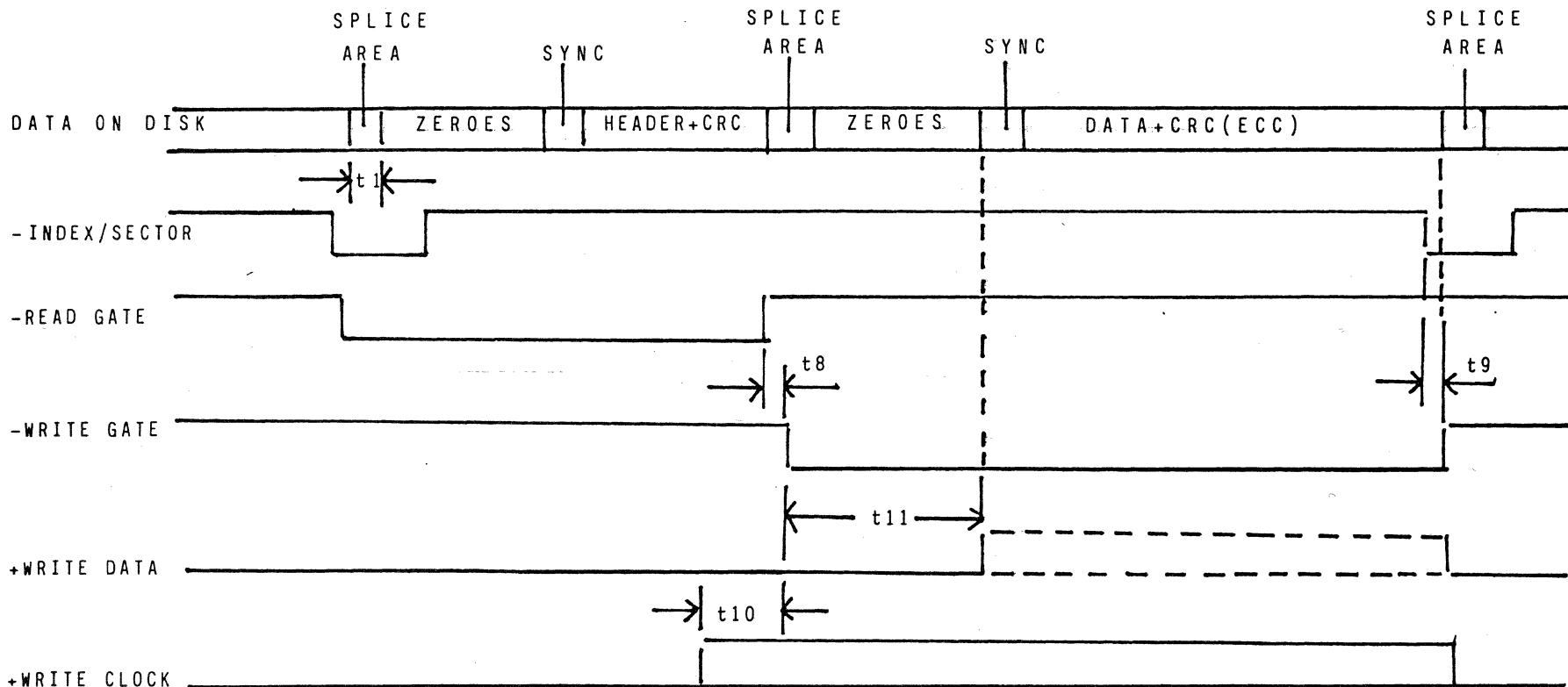
The splice is generated by the transitions of the Write Gate Signal.



	MIN.	TYP.	MAX.	UNIT
t1 SPLICE AREA	---	1.25	---	MICROSECONDS
t2 INDEX/SECTOR TO READ GATE	0	---	1.25	MICROSECONDS
t3 LAST READ BIT TO END OF READ GATE	0	0.1	1.25	MICROSECONDS
t4 READ GATE TO READ DATA VALID	6.75	7.5	8.25	MICROSECONDS
t5 READ GATE TO SYNC BYTE	8	---	---	BYTES
t6 READ GATE INACTIVE	0.5	---	---	MICROSECONDS
t7 READ GATE VALID TO SYNC BYTE	0.3	---	---	MICROSECONDS

Figure 4-21





t1	SPLICE AREA	---	1.25	---	MICROSECONDS
t8	READ GATE INACTIVE TO WRITE GATE*	0.1	---	---	MICROSECONDS
t9	INDEX/SECTOR OR LAST BIT TO WRITE GATE INACTIVE *	0	---	---	MICROSECONDS
t10	WRITE CLODK TO WRITE GATE	0.16	---	2.5	MICROSECONDS
t11	WRITE PREAMBLE	8	---	---	BYTES

\* NOTE THAT THE START OF THE SPLICE AREA IS GIVEN BY THE TRANSITIONS OF WRITE GATE.

Figure 4-22

# Warranty

The Company warrants its devices against faulty workmanship or the use of defective materials (except in those cases where the materials are supplied by OEM) for a period of one year from the date of shipment to OEM, with the exception of  $\frac{1}{4}$ " cartridge products which are warranted for a period of ninety (90) days.

The liability of the Company under this warranty is limited to replacing, repairing, or issuing credit (at the Company's discretion) for any devices which are returned by OEM during such period provided that (a) the Company is promptly notified in writing upon discovery of such defects by OEM; (b) the defective unit is returned to the Company, transportation charges prepaid by OEM; and (c) the Company's examination of such unit shall disclose to its satisfaction that such defects have not been caused by misuse, neglect, improper installation, repair alteration or accident.

Kennedy Company is continually striving to provide improved performance, value and reliability in its products and reserves the right to make these changes without being obligated to retrofit delivered equipment.

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