REFERENCE MANUAL

ADM-1

CRT DATA DISPLAY TERMINAL

by

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PREFACE

This reference manual is published as an aid to users of the ADM-1 CRT Data Display Terminal. Included are specifications, theory of operations, operational logic description and diagrams, description of CRT, monitor, keyboard, main logic board and power supply, and a section on trouble shooting or failure analysis. Options available with the ADM-1, complete parts lists and schematic drawings are included in the Appendix.

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I. ADM-1 SPECIFICATIONS

	Standard	Optional
Display		
Lines	12	24
Character Positions	960	1920
Character Set	64 USASCII	
Screen Phosphor	P4	P31
Face Plate	Plain	Etched
Refresh Rate	60 Hz	
Protected Fields	Reduced Intensity	
Cursor		
Format	Reverse Image Block	
Controls	Forespace, Backspace, Upline, Downline, New Line, Return Home, Tab, Absolute Cursor Addressing, Read Cursor Addressing	
Data Transmission		
Codes	Seven Channel USASCII	
Circuit	Full or Half Duplex	
Interface	RS-232-C or 20ma Loop	Serial Printer or RS-232 Extension
Parity	Even	Odd or Fixed Parity Bit
Modes	Conversational Page Roll Polling Block Text Block Text or Text Only Line and Page	 Partial Page
Rates	Two baud rates selected from following: 110, 300, 600, 1200, 1800, 2400, 4800 and 9600	
Keyboard		
Keys	53	60
Construction	Solid State Circuitry	
Repeat Key	15 CPS	

I. ADM-1 SPECIFICATIONS (Continued)

	Standard	Optional
Data Editing		
Character	Type Over	Insert, Delete
Line		Insert, Delete
		Back Tab
		Erase to End of Line
Unprotected Fields	Clear to Spaces	Erase to End of Field
Screen	Clear to Nulls	Erase to End of Page
		Send Partial Page
Physical Characteristics		
Dimensions	12" high, 16" wide, 21" deep	
Weight	45 lbs	
A-C Power Requirements	115V, 60 Hz, 130 watts	230V, or 50Hz
Environment	5–50°C or 41–122°F 5–95% Relative Humidity without condensation	

II. THEORY OF OPERATION

The ADM-1 Data Display Terminal is designed to provide input/output access to an electronic computer. The terminal consists of three principal functional modules:

(1) Cathode Ray Tube (CRT)

(2) Keyboard

(3) Main Circuit Board and Power Supply

assembled in an attractive lightweight housing, together with necessary hardware, cabling, switches, etc., needed to complete the ADM-1 terminal system. A functional block diagram of the system is shown in Figure II.1, and each of the modules is discussed in the following sections.

CRT DISPLAY

The ADM-1 uses a cathode ray tube (CRT) and solid state circuitry with raster scan for converting alphanumeric data from a remote computer or its own memory into a screen display format.

Displayed characters are represented with a 5 x 7 dot matrix on the screen of the CRT. An example of the display format used is shown in Figure II.2. Note that each character row is allocated nine raster lines, seven for the character and two for vertical interline spacing. Horizontal intercharacter spacing is assured by the ADM-1 reserving two dot rows between characters. Reverse image display is used to indicate cursor position superimposed over data. Protected fields on the display are distinguished by reduced luminance.

A complete field of characters in the standard ADM-1 consists of 960 Character patterns organized of 12 rows of 80 characters each. Display fields are refreshed at a rate set by a stable crystal oscillator approximately synchronously with input power, or at 60 Hz in the standard terminal. This rapid field refresh rate generates flicker-free luminance levels and high contrast display even in bright ambient illumination.

Both vertical and horizontal beam deflections are generated directly by trigger signals derived from the system clock and input to the TV monitor. The TV monitor is a solid-state unit designed for reliability and high quality video reproduction in industrial and

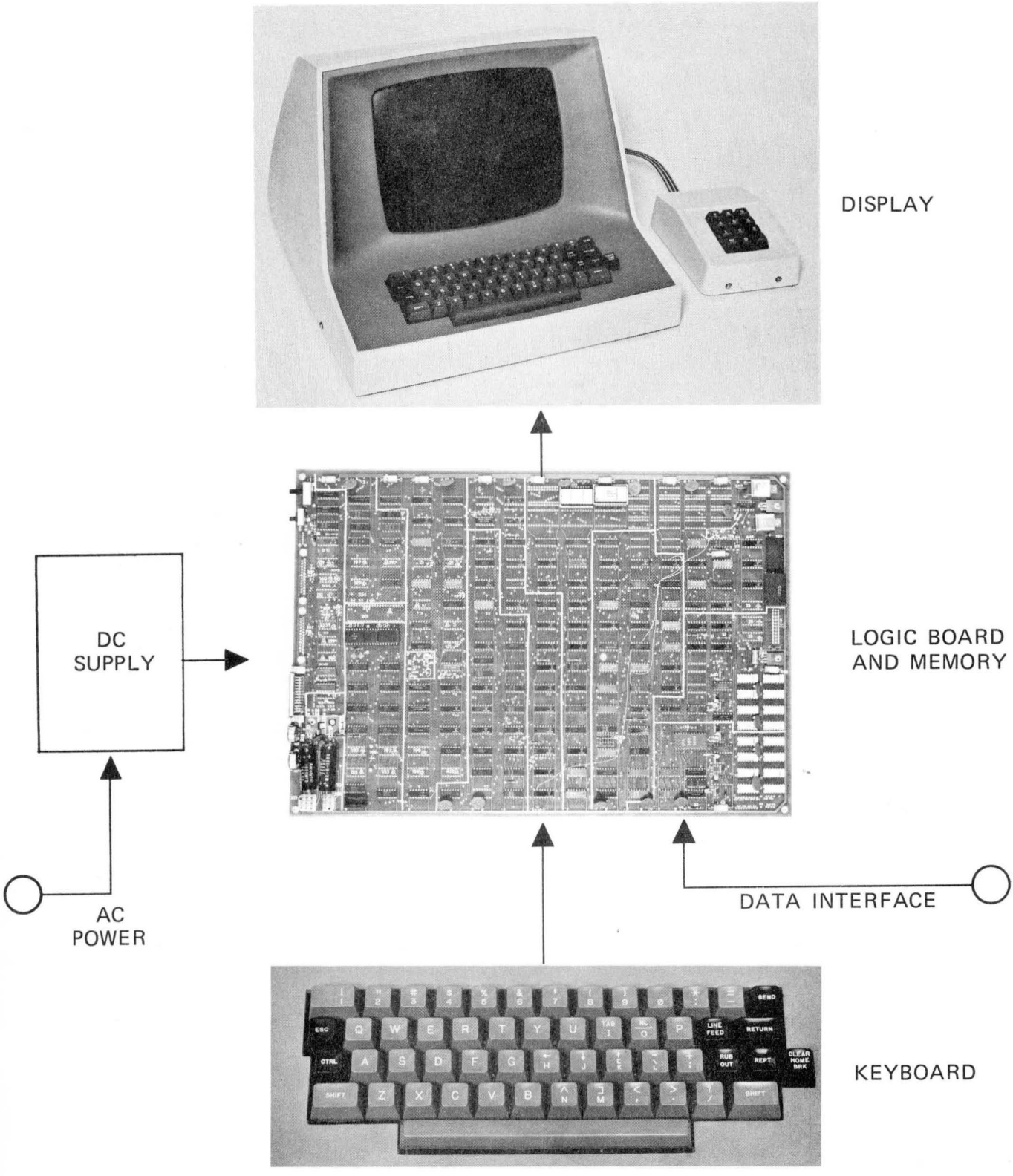


Figure II-1. ADM-1 Functional Layout

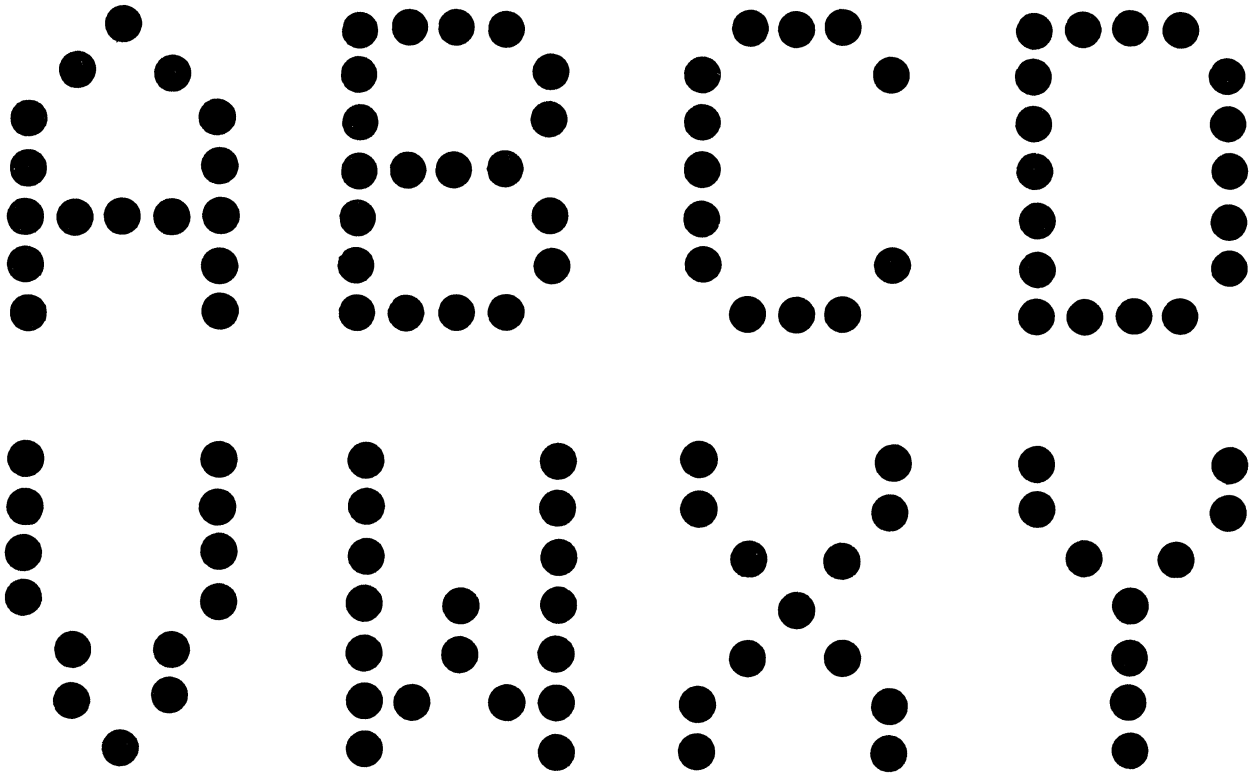


Figure II.2 – ADM-1 Display Format

commercial installations. Theory of Operation of the TV monitor is covered in Section IV of this manual.

KEYBOARD

An ADM-1 Terminal is equipped with either a standard (53 key) or optional (60 key) extended keyboard. Both keyboards provide all ADM-1 functions, with the extended keyboard offering additional cursor control keys. A facsimile of the ADM-1 keyboard is shown in Figure II.3.

Keys are positioned on 3/4" centers, with 2 oz. operating force, and two key rollover interlocking.

The keyboard is used by depressing any of the keys individually, in combination with other keys simultaneously, or in sequences of keystrokes.

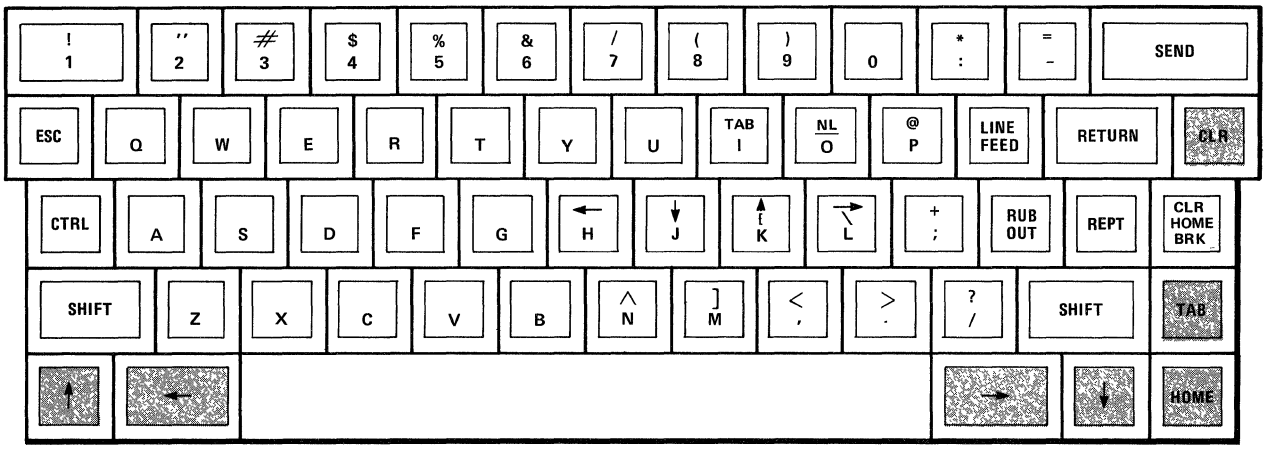


Figure II.3 – ADM-1 Keyboard with Optional Keys

RESET

To reset the ADM-1 to an idle clear state, depress the following keys simultaneously: CTRL, SHIFT, REPT, HOME CLR, BRK. This operation forces the control program to begin execution at location zero and clears all of the program control flags. The entire display screen is cleared to "spaces", the protect mode is reset, and the cursor is positioned at the "home" position. In the event RESET doesn't operate, refer to keyboard Enable/Disable below.

NORMAL KEYBOARD OPERATION

Single or simultaneous multiple keystrokes are translated into USASCII seven channel binary codes which are stored in memory, stored and transmitted, or transmitted only, depending on the ADM-1's mode.

Operation of the standard and optional extended keyboard is given in the following listing in Table II.1 and Table II.2.

TABLE II.1 – ADM-1 KEYBOARD OPERATIONS

	Keys Used	
	Standard Keyboard	**Extended Keyboard**
A. CHARACTER DISPLAY		
1. Alphabetic Upper Case	A to Z	A to Z
2. Numeric	0 to 9	0 to 9
3. Special Characters	: – ; , . /	: – ; , . /
4. Special Characters with SHIFT key	! " # $ % & / ( ) * = @ _ [\ + ^] < > ?	! " # $ % & / ( ) * = @ _ [\ + ^] < > ?
5. No Display – USASCII SP	SPACE	SPACE
6. No Display – USASCII DEL	RUBOUT	RUBOUT
B. CURSOR CONTROL		
1. Position Home	CLR SHIFT/HOME, BRK CTRL/SHIFT/N	HOME
2. Position New Line	LINE FEED RETURN CTRL/SHIFT/O	LINE FEED RETURN CTRL/SHIFT/O
3. Position New Field	CTRL/I	TAB
4. Suppress Character Type-over	Consecutive SPACES after RETURN	Consecutive SPACES after RETURN
5. Increment Up	CTRL/K	↑
Down	CTRL/J	↓
Right	CTRL/L	→
Left	CTRL/H	←
C. TERMINAL CONTROL		
1. Break – USASCII	CLR HOME BRK	CLR HOME BRK
2. Clear Screen	CLR CTRL/HOME BRK	CLEAR
3. Audible Tone	CTRL/G	CTRL/G
4. Send Line Unprotected	SHIFT/SEND	SHIFT/SEND
5. Send Page Unprotected	SHIFT/CTRL/SEND	SHIFT/CTRL/SEND
6. Keyboard Unlock	CLR CTRL/SHIFT/HOME BRK	CLR CTRL/SHIFT/HOME BRK

TABLE II.2 – ADM-1 BINARY CODES

	CONTROL FUNCTIONS			DISPLAYABLE CHARACTERS					
BITS	BITS	0	1	2	3	4	5	6*	7*
4321	765	000	001	010	011	100	101	110	111
0000		NUL	DLE	SP	Ø	@	P	\	P
0001		SOH	DC1	!	1	A	Q	a	q
0010		STX	DC2	"	2	B	R	b	r
0011		ETX	DC3	#	3	C	S	c	s
0100		EOT	DC4	$	4	D	T	d	t
0101		ENQ	NAK	%	5	E	U	e	u
0110		ACK	SYN	&	6	F	V	f	v
0111		BEEP	ETB	'	7	G	W	g	w
1000		← BS	CAN	(	8	H	X	h	x
1001		SKIP HT	EM	)	9	I	Y	i	y
1010		↓ LF	SUB	*	:	J	Z	j	z
1011		VT ↑	ESCAPE ESC	+	;	K	[	k	{
1100		FF →	FS	,	<	L	\	l	¦
1101		RETURN CR	GS	–	=	M	]	m	}
1110		SO	HOME RS	.	>	N	^	n	~
1111		SI	NEW LINE US	/	?	O	_	o	DEL

*DISPLAYED as UPPER CASE characters as given in columns 4 and 5, respectively. Exception is DEL which is not received by ADM-1. Lower case codes are stored in ADM-1 memory and displayed as upper case.

In addition to using single keys or combinations of keys to provide functions described above, keys may be used in sequence to cause operations as follows:

ESCAPE SEQUENCES

ESCAPE sequences are initiated by using the ESC key to transmit a USASCII ESC code which enables the ADM-1 under program control to interpret the next character or string of characters as special control instructions. These sequences are used for:

(1) Keyboard enabling/disabling

(2) Display Clearing

(3) Field Protection Control

(4) Message Transmissions Control

(5) Absolute Cursor Addressing/Cursor Address Read

(6) Data Editing (optional)

Details of specific sequences follow:

ENABLE/DISABLE KEYBOARD

These functions are normally used when the ADM-1 is connected on-line to a computer which transmits the following sequences:

ESC #	disables all keyboard functions except KEYBOARD UNLOCK
ESC "	restores keyboard control

Since ESC # sequence may be accidentally initiated manually, the keyboard will need to be unlocked by simultaneously depressing:

CTRL/SHIFT/$\frac{\text{CLR}}{\text{HOME}}$/$\frac{\text{}}{\text{BRK}}$	unlocks keyboard

CLEAR DISPLAY

The ADM-1 screen may be cleared in several ways:

Locally the operator can clear the foreground (unprotected characters) to "space" codes by use of the CTRL and $\frac{\text{CLR}}{\text{HOME}}$/$\frac{\text{}}{\text{BRK}}$ keys (or the CTRL and CLEAR key on the 60 key keyboard).

By operator or computer control, the entire display may be cleared or only the foreground may be cleared to either "spaces" or to NULS by the use of the following escape sequences:

ESC	;	clear foreground to spaces
ESC	+	clear all to spaces
ESC	:	clear foreground to NUL
ESC	*	clear all to NUL

Upon completion, the cursor will be in the first unprotected position on the screen.

FIELD PROTECTION CONTROL

Writing of protected characters is accomplished by sending or typing various ESC sequences.

ESC	)	set WRITE PROTECT mode
ESC	(	reset WRITE PROTECT mode
ESC	&	set PROTECT mode
ESC	'	reset PROTECT mode

When in PROTECT MODE, characters that have been written with the WRITE PROTECT set cannot be overwritten. The PROTECT MODE is also reset by the CLEAR operations.

ESC	*	clear all to NUL
ESC	+	clear all to spaces

The WRITE PROTECT mode is also reset by the following CLEAR operations:

ESC	;	clear foreground to spaces
ESC	+	clear all to spaces
ESC	:	clear foreground to NUL
ESC	*	clear all to NUL

or by initiation of a SEND operation:

SHIFT/SEND	Send line unprotected
SHIFT/CTRL/SEND	Send page unprotected

When the EDIT and PRINT options are provided, the WRITE PROTECT mode will terminate when any of the following operations are performed:

ESC	Q	character insert
ESQ	W	character delete
ESC	E	line insert
ESC	R	line delete
ESC	T	line erase
ESC	Y	page erase
ESC	P	print

The cursor will not reside in a protected position. Following any cursor motion operation, the content of the position indicated by the cursor is tested for protected status. If that position is protected, the cursor moves forward (or backward in the event of an original backward motion) until an unprotected location is reached.

CAUTION:

If the entire display area is protected, the cursor will have no place to stop, causing the terminal to "lock up" in a search for an unprotected position. This search may be "broken" by the operator depressing the CLR HOME BRK key.

MESSAGE TRANSMISSION CONTROL

ESC 4 SEND line unprotected

In block mode, an ESC 4 (or Send Key) sequence causes the unprotected character positions from the beginning of the current line through the cursor position to be transmitted to the remote computer. The last character position transmitted is followed by transmission of a RETURN code.

ESC 5 SEND page unprotected

In block mode an ESC 5 (or Shift Send Key) sequence causes the unprotected character positions from the beginning of the page through the cursor to be transmitted to the remote computer. The last character position transmitted is followed by transmission of a RETURN code.

ESC 6 SEND line protected

In block mode, an ESC 6 sequence causes all character positions (protected and unprotected) from the beginning of the line through the cursor to be transmitted to the remote computer. During transmission, ESC) and ESC (sequences for setting and resetting WRITE PROTECT are executed as protected fields are entered and exited.

ESC 7 SEND page protected

In block mode, an ESC 7 sequence causes all character positions (protected or unprotected) from the beginning of the page through the cursor to be transmitted to the remote computer. During transmission, ESC) and ESC (sequences are executed as protected fields are entered and exited.

ESC S partial SEND

In block mode, an ESC S sequence causes an USASCII FS code to be stored in display

memory at the cursor location. The cursor backspaces until a previously stored FS code is encountered, then advances to the first unprotected character position and transmits through the next FS code. (If there are no previous FS codes, the transmission begins at home position, or the first unprotected position.) (Optional)

CURSOR ADDRESSING

The computer can position the ADM-1 cursor to any position by a 4 character sequence:

ESC = Y X position cursor

where Y and X represent the row and column coordinates of the cursor position desired. The HOME position (top row, leftmost column) is addressed by ESC + SPACE SPACE, and successive positions (down for Y or to the right for X) use codes ascending in the ASCII character set as in Table II.3.

TABLE II.3 – ABSOLUTE CURSOR POSITIONING

X or Y	ASCII CODE	X	ASCII CODE	X	ASCII CODE
1	SPACE	28	;	55	V
2	!	29	<	56	W
3	"	30	=	57	X
4	#	31	>	58	Y
5	$	32	?	59	Z
6	%	33	@	60	[
7	&	34	A	61	\
8	'	35	B	62	]
9	(	36	C	63	^
10	)	37	D	64	_
11	*	38	E	65	`
12	+	39	F	66	a
13	,	40	G	67	b
14	–	41	H	68	c
15	.	42	I	69	d
16	/	43	J	70	e
17	0	44	K	71	f
18	1	45	L	72	g
19	2	46	M	73	h
20	3	47	N	74	i
21	4	48	O	75	j
22	5	49	P	76	k
23	6	50	Q	77	l
24	7	51	R	78	m
25	8	52	S	79	n
26	9	53	T	80	o
27	:	54	U		

After the 'X' coordinate is loaded, the position of the cursor is tested for protected status. If that position is protected, the cursor automatically skips to the first unprotected location in the direction it previously moved. An ESC ? sequence causes the Y and X coordinates of the cursor followed by a CR code (expressed as three USASCII characters) to be transmitted to the computer.

ESC ? read cursor position (Y X CR)

EDIT OPERATION (OPTION)

ESC Q character insert

a) Resets WRITE PROTECT mode.

b) Moves the character under the cursor and all following characters on that line (or field) one space to the right.

c) Write a space at the original position of the cursor and leaves the cursor at that position.

ESC W character delete

a) Resets WRITE PROTECT mode.

b) Deletes the character under the cursor by moving all following characters on that line or field one space to the left.

c) Writes a 'space' in the last position of the line or field.

d) Cursor does not move.

ESC E line insert

a) Is not executed if PROTECT MODE is set.

b) Resets WRITE PROTECT mode.

c) Inserts a line of unprotected spaces at the line occupied by the cursor by moving the contents of that line and all lines below down one line.

d) Bottom line is lost.

e) At completion cursor is at first character position of inserted line.

ESC R line delete

a) Is not executed if PROTECT MODE set.

b) Resets WRITE PROTECT mode.

c) Deletes line of data occupied by cursor.

d) Moves following lines up one line.

e) Bottom line becomes unprotected spaces.

f) Cursor is at first position of original line count.

ESC T line erase

a) Replaces contents of unprotected positions with space beginning at cursor position and ending at last character of line or field.

b) If WRITE PROTECT mode is true, the spaces will be protected.

c) Cursor will remain at original position, except when WRITE PROTECT mode=true and PROTECT mode=true, then the cursor will move to the first unprotected position following.

ESC Y page erase

a) Resets WRITE PROTECT mode.

b) Writes SPACE in all unprotected positions beginning with position of cursor to the end of the screen.

c) Cursor does not move.

ESC I back tab cursor

Moves cursor to first position of current unprotected field. If at first position, move to first position of previous unprotected field. If backward motion passes through HOME, the cursor stops at last unprotected position on the screen.

PRINT OPERATION – (OPTION)

When received in text or entered from keyboard, an ESC P sequence causes an EM code to be written at the cursor position. Then the cursor is moved to the HOME position. If the ESC P command originated from the ADM-1 keyboard, the print operation begins

immediately; if the command is from the computer, the print operation begins following the termination of the message procedure.

ESC P print

Printing takes place in the following manner:

1. CR LF NUL
2. Each line of text followed by CR LF NUL

Transmission of trailing spaces is suppressed in order to reduce printing time.

The PRINT operation terminates when the cursor reaches the EM code at which time a final CR LF NUL is sent to the printer.

A summary of ESC sequences is given in Table II.4.

TABLE II.4 – ADM-1 DATA DISPLAY ESC SEQUENCES

			P PRINT
!		A	Q CHARACTER INSERT
" KEYBOARD ENABLE		B	R LINE DELETE
# KEYBOARD DISABLE		C	S PARTIAL SEND
$	4 SEND LINE (FOREGROUND)	D	T LINE ERASE
%	5 SEND PAGE (FOREGROUND)	E LINE INSERT	U FREE FORM ENTRY
& SET PROTECT MODE	6 SEND LINE (ALL)	F	V
/ RESET PROTECT MODE	7 SEND PAGE (ALL)	G	W CHARACTER DELETE
(END WRITE PROTECT		H	X
) START WRITE PROTECT		I BACK TAB	Y PAGE ERASE
* CLEAR ALL TO NULL	: CLR FOREGROUND TO NULL	J	Z
+ CLEAR ALL TO SPACES	; CLR FOREGROUND TO SPACES	K	[
		L SPECIAL PRINT	\
	= LOAD CURSOR	M	]
		N	^
	? READ CURSOR	O	_

III. MICROPROGRAMING CONTROL

The organization of data transmission and control for the ADM-1 interactive data display terminal is given in general fashion in the block diagram of Figure III.1. A detailed description of logic for the ADM-1 follows. Specific reference should be made to schematic drawing 129311, sheets 1 through 16, in Appendix C.1. In particular, Drawing 129311, sheet 2, contains a detailed functional block diagram of the ADM-1 logic.

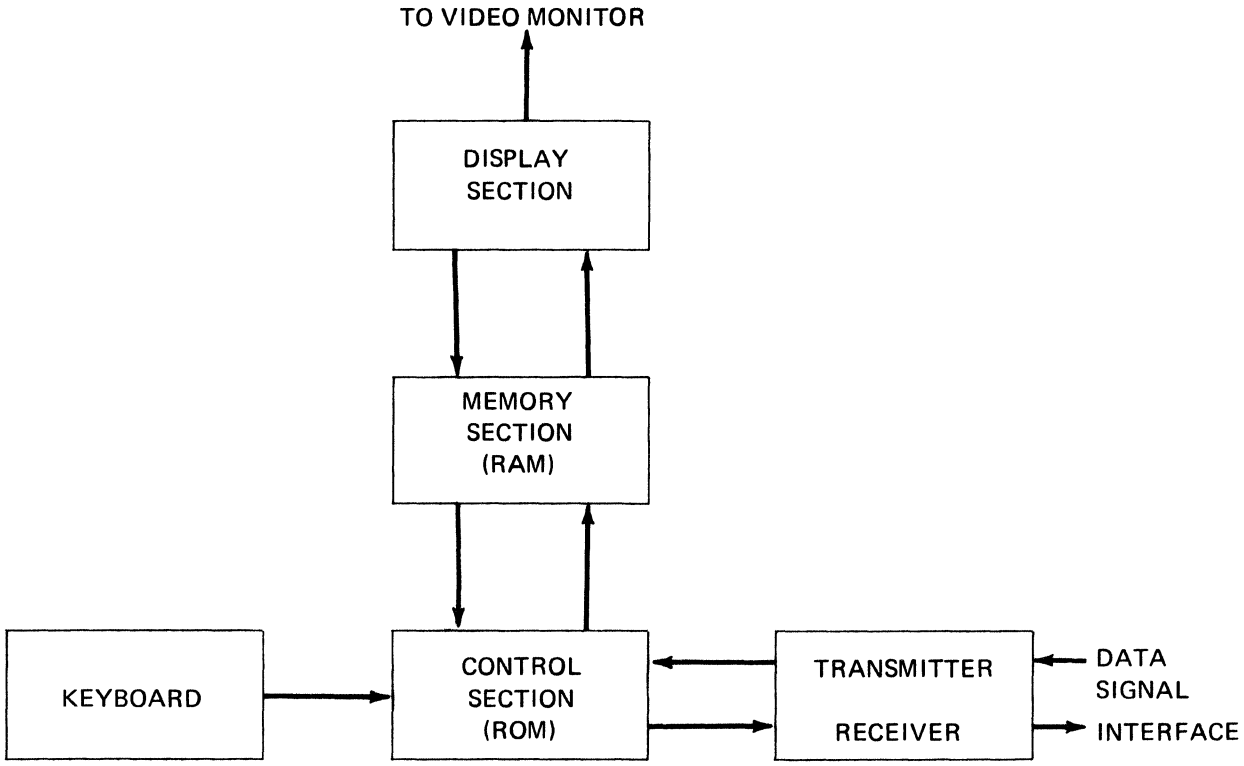


Figure III.1 – ADM-1 Data Flow Block Diagram

The basic concept of the ADM-1 data organization is memory timesharing, with highest priority assigned to the display section (about 20-30% utilization) and second priority given to the control section which has approximately 70-80% utilization.

The memory sharing organization provides greater reliability of display and control operations by using fewer components to provide both functions.

Data information and control commands are transferred to the different components over a tri-state (memory, control, timing) bus.

The display section is comprised of four sub-sections as follows:

(1) Parallel-Serial Converter
(2) Character Generator
(3) Row Refresh Logic
(4) Timing Control

The memory section is a standard RAM memory of 8 bit words and can store 960 words (12 lines of 80 characters) in the standard ADM-1 display. A factory option is provision of 1920 words to give 24 lines of 80 character display.

The memory section includes the conversion logic necessary for maintaining knowledge of display cursor position. Binary codes for cursor position are given as USASCII equivalents in Table II.2 above.

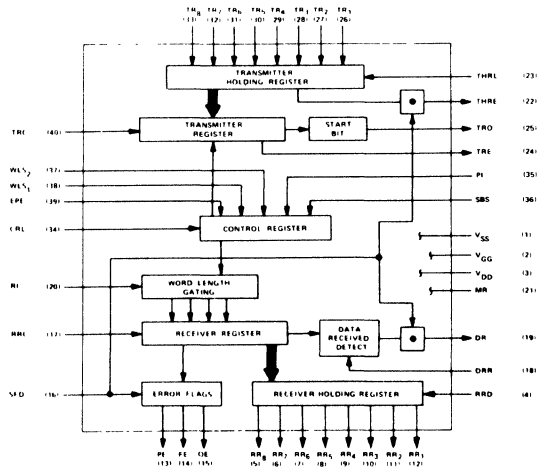
Included with the keyboard assembly are the electronics for encoding key strokes to 8 bit parallel data codes, as well as strobe and repeat signals.

The transmitter/receiver is a standard 1402 or 1602 LSI chip serial asynchronous device which accepts serial 9, 10 or 11 bit patterns (depending upon word structure option) from an RS232C or 20ma current loop interface and transmits 8 bit parallel words to the control section. Likewise, the transmitter receiver can receive 8 bit parallel words from the control section and transmit the appropriate serial bit pattern to a computer over the data signal interface. See Figure III.2 below and Drawing 129311, sheet 13 in Appendix C for further information on the 1402/1602 transmitter/receiver.

Information transfer is controlled in the ADM-1 by the read only memory, ROM. The standard functions are provided by two pages of 256 8 bit words each. These functions may be extended by adding up to six additional pages. This section describes the microprogram language and the structure of the extendable microprogrammed control.

Information is transferred between functional units by way of the tri-state bus, TSB, under microprogram control. This information transfer consists of eight bit characters

BLOCK DIAGRAM



DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 volts Supply
2	V_{GG} POWER SUPPLY	V_{GG}	−12 volts Supply
3	V_{DD} POWER SUPPLY	V_{DD}	Ground
4	RECEIVER REGISTER DISCONNECT	RRD	A high-level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8–RR_1 data outputs (pins 5-12).
5–12	RECEIVER HOLDING REGISTER DATA	RR_8–RR_1	The contents of the RECEIVER HOLDING REGISTER appear on these lines in parallel if a low-level input voltage, V_{IL}, is applied to RRD. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 12) is the least significant bit of the character.
13	PARITY ERROR	PE	The status of the parity verification circuit appears on this line if a low-level input voltage, V_{IL}, is applied to the STATUS FLAGS DISCONNECT (pin 16) control line. Wired-OR capability is provided on this line allowing PE lines from other arrays to be OR-tied. A high-level output voltage, V_{OH}, on this line (under the conditions above) indicates a PARITY ERROR in the received parity bit as programmed by the EVEN PARITY ENABLE control line (pin 39). The status is updated each time a character is transferred from the RECEIVER REGISTER to the RECEIVER HOLDING REGISTER.
14	FRAMING ERROR	FE	The status of the STOP bit detection circuit appears on this line if a low-level input voltage, V_{IL}, is applied to the STATUS FLAG DISCONNECT (pin 16) control line. Wired-OR capability is provided on this line allowing FE lines from other arrays to be OR-tied. A high-level output voltage, V_{OH}, indicates that the received
15	OVERRUN ERROR	OE	
16	STATUS FLAGS DISCONNECT	SFD	
17	RECEIVER REGISTER CLOCK	RRC	
18	DATA RECEIVED RESET	DRR	
19	DATA RECEIVED	DR	
20	RECEIVER INPUT	RI	
21	MASTER RESET	MR	
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	
24	TRANSMITTER REGISTER EMPTY	TRE	

Figure III.2 — ADM-1 Asynchronous Transmitter/Receiver Interface

character has no valid STOP bit. i.e. the bit following the parity bit is not a high-level input voltage, V_{IH}. The status is updated each time a character is transferred from the RECEIVER REGISTER to the RECEIVER HOLDING REGISTER.			TER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
The status of the DATA RECEIVED circuit appears on this line if a low-level input voltage, V_{IL}, is applied to the STATUS FLAG DISCONNECT (pin 16) control line. Wired-OR capability is provided on this line allowing OE lines from other arrays to be OR-tied. A high-level output voltage, V_{OH}, indicates that the previously received character was not read (DR line not reset) before the present character was transferred to the RECEIVER HOLDING REGISTER.	25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit DATA bits, PARITY bit, and STOP bit), are serially shifted out on this line. This line will remain at a high-level output voltage, V_{OH}, when no data is being transmitted. A start of transmission is defined as the transition from a high-level output voltage, V_{OH}, to a low-level output voltage, V_{OL}, of the START bit.
A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE circuit outputs.	26–33	TRANSMITTER REGISTER DATA INPUTS	TR_1–TR_8	Parallel 8 bit characters are input on these lines into the TRANSMITTER HOLDING REGISTER with THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the least significant bits only are accepted. The character is right justified into the least significant bit. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted
This clock is sixteen (16) times faster than the desired receiver shift rate.				
A low-level input voltage, V_{IL}, applied to this line resets the DR line.	34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.				
Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.	35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits. The STOP bit(s) will immediately follow the last data bit on transmission if parity is inhibited. A low-level input voltage, V_{IL}, enables the parity generation and verification circuits. PI will, when a high-level input voltage, V_{IH}, is applied, also clamp the PE line (pin 13) to a low-level output voltage, V_{OL}
This line is strobed to a high-level input voltage, V_{IH}, to clear the logic after power turn-on. It resets all registers and sets the serial output line to a high-level output voltage, V_{OH}.				
A high-level output Voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.	36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits generated after the PARITY bit during transmission. A high level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit.
A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is transferred simultaneously with the initiation of the serial transmission of the new character.	37–38	WORD LENGTH SELECT	WLS_2 – WLS_1	These two lines select the character length to be 5, 6, 7 or 8 bits WLS_2 / WLS_1 / WORD LENGTH V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
	39	EVEN PARITY ENABLE	EPE	This line selects either even or odd PARITY to be generated by the transmitter and checked by the receiver. A high level input voltage, V_{IH}, selects even PARITY and a low level input voltage, V_{IL}, selects odd PARITY
A high-level output voltage, V_{OH}, on this line indicates that the TRANSMIT-	40	TRANSMITTER REGISTER CLOCK	TRC	This CLOCK is sixteen (16) times faster than the desired transmitter shift rate

Figure III.2 – ADM-1 Asynchronous Transmitter/Receiver Interface (Continued)

SWITCHING WAVEFORMS

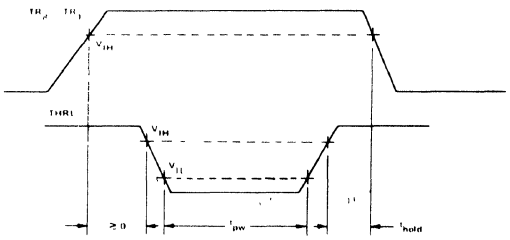


FIGURE 1. DATA INPUT LOAD CYCLE

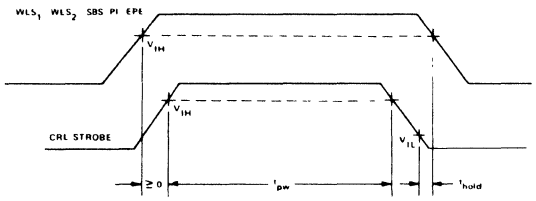


FIGURE 2. CONTROL REGISTER LOAD CYCLE

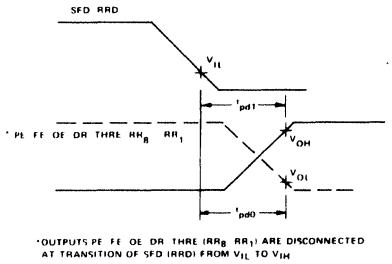


FIGURE 3. OUTPUT DELAYS

TTL-MOS INTERNAL INTERFACE

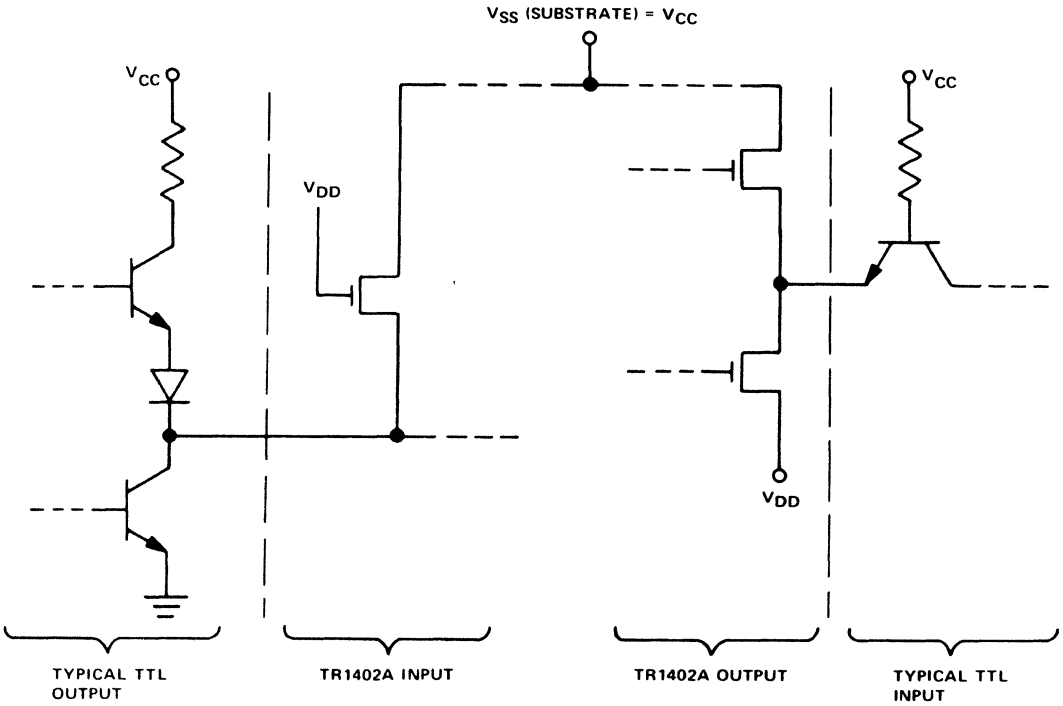


Figure III.2 – ADM-1 Asynchronous Transmitter/Receiver Interface (Continued)

transmitted in parallel between the following units:

MNEMONIC	
RCV	External source via Receiver and serial to parallel converter
KEY	Keyboard
CPR	Cursor position row register
CPC	Cursor position character register
LIT	Eight bit literal register
RDR	Random access page buffer via the Read Data Register
WDR	Random access page buffer via the Write Data Register
LRC	Modulo 2 adder and accumulator *7 bits)
XRS	UART and interface status
ADD	Switch (8 bits) internal, manually set
STB	8 flip flops set and cleared by program
MACR	Random access page buffer row counter (address register high order five bits)
MACC	Random access page buffer character counter (address register low order seven bits)

Character transfer between the tri-state bus and sources or destinations is enabled by the BUS CONTROL microprogram commands (see instruction repertory) and are initiated by the INPUT/OUTPUT microprogram commands.

Status of hardware functional units is indicated by the setting of conditions and determines the execution sequence of the microprogram by use of the CONDITIONAL JUMP instructions (see instructions repertory and TABLE OF CONDITIONS).

TABLE III.1 – TABLE OF REGISTER USAGE

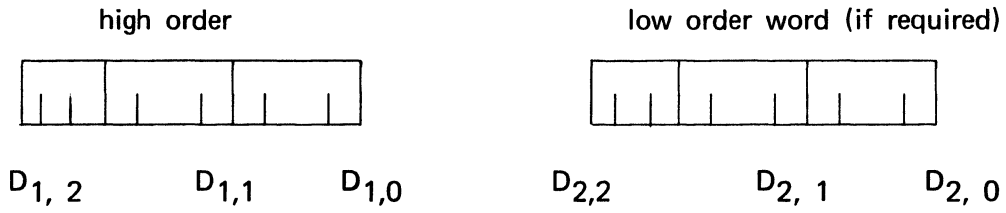
Register Symbol	Register Name	Description
WDR	Write Data Register	Eight bit character register contains characters to be written into the RAM from tri-state bus.
RDR	Read Data Register	Eight bit register to contain characters read from the RAM for transfer to tri-state bus
MACC	Memory Address Counter – Character	Contains low order 7 bits of the RAM address accessible to the tri-state bus.
MACR	Memory Address Counter – Row	Contains high order 5 bits of the RAM address accessible to the tri-state bus.
ARTO	Communications Interface UART	
ART1	Auxiliary Interface UART (Printer, etc.)	
LIT	Literal (8 bit) Register	Used to transfer constants from ROM to tri-state bus.
CPR	Cursor Row Position Register	
CPC	Cursor Character Position Register	
KEY	Keyboard Register	
LRC	Longitudinal Transmissions Check Register	For modulo 2 sum check of transmission characters.
REV		
ADD	Address Register	Switches set manually inside cabinet
XRS	Transmit–Receive Status	
STB	Status bits 1 through 8	Global status for Microprograming

TABLE III. 2 -- TABLE OF CONDITION SIGNIFICANCE

Name of Condition	Use or Action Resulting
WPROT	Write Protect bit copies into RAM each Write.
PROTM	Write Protect mode, disallows overwriting protected characters
BEEP	Causes beep and clears automatically (optional)
STB 1 2 3 4 5 6 7 8	Status Bits set by microprogram for global control
RTSO	Request to send (Main ART)
RTS1	Request to send (Auxiliary ART)
TSB 1 2 3 4 5 6 7 8	Tri-State Bus Bits
KEYSTR	Keyboard Strobe
KEYBRK	Keyboard Break Key
KEYHIS	Keyboard Send Key

INSTRUCTION SET

Instructions may be partitioned into two classes, those which occupy two eight bit bytes and those which occupy one eight bit byte. We shall represent these as six or three octal digits, respectively, and assume the high order bit in each word to be zero. This high order or ninth bit is, of course, not actually present in the eight bit hardware.



Where $D_{i,j}$ is the jth octal digit for the ith 8 bit word.

Subfields of instructions will be indicated by only the high order and low order octal digits in parentheses, for example:

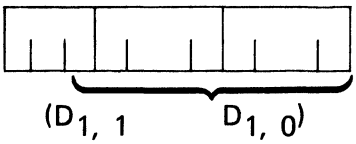


TABLE III.3 – RANDOM ACCESS MEMORY CONTROL

Mnemonic	$(D_{1,2}\ D_{1,0})$	Description
READ	001	Transfers the contents of the RAM location indicated by the contents of MACR, MACC into the RDR
WRITE	003	Transfers the contents of the WDR into the RAM location indicated by the contents of MACR, MACC
LOA WDR	005	Replaces the contents of the WDR with the contents currently on the TRB
CLR WDR	004	Clears the WDR
TSB=RDR	160	Sets the contents on the TSB equal to the contents of the RDR
SET WPROT	006	Sets the write protect bit on all words subsequently written into the RAM
CLR WPROT	007	Clears the write protect bit on all words subsequently written into the RAM
SET PROTM	016	Set the PROTM. This status bit is used as a global condition by the program to disable the overwriting of any characters in the RAM for which the WPROT bit is set.
CLR PROTM	017	Clear the PROTM. This global condition enables the overwriting of write protected characters.

TABLE III.4 – ROM INSTRUCTION EXECUTION SEQUENCE CONTROL

Mnemonic	($D_{1,2}$ $D_{2,0}$)	Description
JMP	10P LLL	Causes next instructions to be taken from the location indicated by LLL on page P.
JTC	3CC LLL	Causes next instructions to be taken from the location indicated by LLL on the local page if the condition indicated by CC is true. Instructions are taken in normal sequence otherwise. (See table of conditions for values of CC.)
JFC	2CC LLL	Causes next instructions to be taken from the location indicated by LLL on the local page if the condition indicated by CC is false. Instructions are taken in normal sequence otherwise. (See table of conditions for values of CC.)

TABLE III.5 – TABLE OF CONDITIONS

Mnemonic	Condition Identifier	Description
TSB 1	00	Character in RDR
2	01	RDR Parity error
3	02	Framing Error (stop bit missing)
4	03	Receives overflow (unread character overwritten)
5	04	Transmitter holding register empty
6	05	Clear to send (from data set)
7	06	Main transmitter register clear (for request to send)
8	07	Auxiliary transmitter register clear (for request to send)
KEYSTR	10	Keyboard strobe
KEYBRK	11	Break key
KEYHIS	12	Send key
KEYSTR2	13	Keyboard strobe (optional 2nd keyboard)
OFLO	20	MACC/MACR overflow or underflow
MAC=CPR	21	Set if (MACR/MACC) equals (CPR/CPC)
OPT1	22	Wire straps on main logic board
OPT2	23	Wire straps on main logic board
OPT3	24	Wire straps on main logic board
PROTM	40	Set if in character protection mode
PROT	41	Character protect bit in RAM
KEYCTRL	42	Keyboard Control Test
KEYSHFT	43	Keyboard Shift Test
ONLINE	44	On line switch setting
CONV	45	Conversation mode
FULLDX	46	Full duplex
OPT4	47	Wire straps on main logic board

TABLE III.6 – RAM ADDRESS CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
CLR MACC	020	Set character counter to left margin
CLR MACR	030	Set row counter to top row
LOA MACC	021	Set character counter to value on tri-state bus
LOA MACR	031	Set row counter to value on tri-state bus
LOA CPR	027	Sets contents of CPC and CPR equal to current contents of MACC and MACR respectively
SET MACC	022	Set character counter to right margin
SET MACR	032	Set row counter to bottom row
INC MACC	023	Move character counter right one position†
INC MACR	033	Move row counter down one line†
DEC MACC	024	Move character counter left one position†
DEC MACR	034	Move row counter up one line†

†These operations will set OFLO if they cause character address to run off either margin or if they cause row address to run off top or bottom of page.

FLAG CONTROL

Flags are set or cleared by the microprogram to either control certain hardware functions or set global conditions controlling the microprogram actions (see of table of flags below). General instructions for flags are as follows:

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Action
CLR	CAA	Clears the indicated flag. (See table flags for values of CAA)
SET	CAA	Sets the indicated flag. (See table flags for value of CAA)

TABLE III.7 – TABLE OF FLAGS

Mnemonic	Set	CLR	Description
WPROT	006	007	Write Protect
PROTM	016	017	Protect Mode
STB1	061	060	Program Global
STB2	063	062	Program Global
STB3	065	064	Program Global
STB4	067	066	Program Global
STB5	071	070	Program Global
STB6	073	072	Program Global
STB7	075	074	Program Global
STB8	077	076	Program Global
BEEP	037	(Clears automatically)	Causes one BEEP
RTS0	121	122	
RTS1	131	132	

LITERAL CONTROL

The literal register provides a means of entering a constant from the ROM onto the tri-state bus (TSB). This command is:

Mnemonic	$(D_{1,2}\ D_{1,0})$	$(D_{2,2}\ D_{2,0})$
LOA LIT	150	XXX

and causes the contents of LIT to be replaced by XXX.

ASYNCHRONOUS RECEIVER/TRANSMITTER CONTROL

In addition to the main transmitter/receiver interface normally associated with the computer, an additional transmitter/receiver interface is accommodated by the following instructions. This facilitates such optional devices as an auxiliary printer.

TABLE III.8 – ASYNCHRONOUS RECEIVER/TRANSMITTER CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
SEL ARTO	120	Selects main receiver transmitter interface
SEL ART1	130	Selects auxiliary receiver transmitter interface
LOA ART0	123	Loads main transmitter from TSB
LOA ART1	133	Loads auxiliary transmitter from TSB
CLR ART0	124	Clear main data ready flag
CLR ART1	134	Clear auxiliary data ready flag

TRANSMISSION LONGITUDINAL CHECKING

A 7 bit modulo 2 adder, LRC, is provided for transmission checking as follows:

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
CLR LRC	156	Clear LRC
CLR LRC	157	Replace each bit of the LRC with the Modulo 2 sum of its prior setting and the corresponding bit of the TSB.

TRI STATE BUS CONTROL

The tri state bus contents are set equal to any one of the following registers by the indicated command. (See Table of Register Usage, Table III.1).

TABLE III.9 – TRI STATE BUS CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
TSB=RDR	160	Set the TSB contents equal to RDR
TSB=KEY	161	Set the TSB contents equal to KEY
TSB=REV	162	Set the TSB contents equal to REV
TSB=LIT	163	Set the TSB contents equal to LIT
TSB=CPC	164	Set the TSB contents equal to CPC
TSB=CPR	165	Set the TSB contents equal to CPR
TSB=LRC	166	Set the TSB contents equal to LRC
TSB=XRS	167	Set the TSB contents equal to XRS
TSB=ADD	170	Set the TSB contents equal to ADD
TSB=STB	171	Set the TSB contents equal to STB

To illustrate actual program control of the ADM-1, five examples of programs for basic display functions are included as follows:

(1) RESET

(2) DATA from Keyboard

(3) Receive DATA

(4) DATA from Memory

(5) IDLE

RESET

```
  0      124      RESET      CLR ARTO
  1       17      .          CLR PROTM
  2      320      .          JTC OFLO       RESET1
  3        4
  4      100      RESET1     JMP            CLEAR

 73      163      CLEAR      TSB=LIT
 74      150      . .        LOA LIT
 75       40
 76        5      .          LOA WDR
 77        7      CLEAR1     CLR WPROT
100       30      .          CLRMACR
101       20      .          CLR MACC
102        1      CLEAR3     READ
103      341      .          JTC PROT       CLEAR4
104      106
105        3      .          WRITE
106       23      CLEAR4     INC MACC
107      220      .          JFC OFLO       CLEAR3
110      102
111       20      .          CLR MACC
112       33      .          INC MACR
113      220      .          JFC OFLO       CLEAR3
114      102
115       30      .          CLR MACR
116      101      .          JMP            SKIP21

 27        1      SKIP21     READ
 30      341      .          JTC PROT       SKIP2
 31       15
 32      100      IDLE1      JMP            IDLE
 33       21
```

DATA FROM KEYBOARD

```
127     161     KEYST       TSB=KEY
130     245     .           JFC CONV        KEYST3
131     144     .
132     167     .           TSB=XRS
133     121     KEYST1      SET RTSO
134     205     .           JFC TSB6        KEYST1
135     133
136     204     KEYST2      JFC TSB5        KEYST2
137     136
140     161     .           TSB=KEY
141     123     .           LOA ARTO
142     146     .           JTC FULLDX      IDLE
143      21
144      62     KEYST3      CLR STB2
145     100     .           JMP             CSD
160     306     CSD         JTC TSB7        CD7
161     207
162     205     x           JFC TSB6        CD
163       6
164     304     .           JTC TSB5        CHAR
165     230
166     303     .           JTC TSB4        CHAR
167     230
170     302     .           JTC TSB3        CHAR
171     230
172     301     .           JTC TSB2        CHAR
173     230
174     300     .           JTC TSB1        CHAR
175     230
230       5     CHAR        LOA WDR
231       3     CHARO       WRITE
232      64     .           CLR STB3
233      23     FORSP       INC MACC
234     220     .           JFC OFLO        HOME1
235      67
236      20     NEWLIN      CLR MACC
237      64     DNLIN       CLR STB3
240      33     .           INC MACR
241     220     .           JFC OFLO        HOME1
242      67

 67     101     .           CLR MACC
 70      27     HOME1       JMP             SKIP21
```

RECEIVE DATA

```
147   124   RCVDAT    CLR ARTO
150   302   .         JTC TSB3     IDLE
151    21
152   303   .         JTC TSB4     IDLE
153    21
154   301   .         JTC TSB2     RCVPE
155   225
156    63   .         SET STB2
157   162             TSB=RCV
```

DATA FROM MEMORY

```
 34   171   ESC       TSB=STB
 35   301   .         JTC TSB2     ESCRCV
 36    44
 37   210   ESCKEY    JFC KEYSTR   ESCKEY
 40    37
 41   161   .         TSB=KEY
 42   101   .         JMP          DESC
 43    51
 44   167   ESCRCV    TSB=XRS
 45   200   .         JFC TSB1     ESCRCV
 46    44
 47   124   .         CLR ARTO
 50   162   .         TSB=RCV
 51   306   DESC      JTC TSB7     DESC7
 52   126
 53   205   .         JFC TSB6     IDLE1
 54    32
 55   304   .         JTC TSB5     DESC65
 56   132

132   303   DESC65    JTC TSB4     DESC654
133   150
134   202   .         JFC TSB3     DESC7
135   126
136    27   ESCSEND   LOA CPR
137    64   .         CLR STB3
140    62   x         CLR STB2
141   201   .         JFC TSB2     ESCSEND1
142   144
143    65   .         SET STB3
144   300   ESCSEND1  JTC TSB1     SEND1
145   233
146   101   .         JMP          SEND2
234    20   SEND2     CLR MACC
235   121   .         SET RTSO
236   171   SEND2     TSB=STB
237     1   .         READ
240   341   .         JTC PROT     SEND4
```

DATA FROM MEMORY (Continued)

```
241     333
242     202     .       JFC TSB3        SEND3
243     271
244     201     .       JFC TSB2        SEND3
245     271

271     167     SEND3   TSB=XRS
272     205     .       JFC TSB6        SEND3
273     271
274     204     .       JFC TSB5        SEND3
275     271
276     160     .       TSB=RDR
277     123     .       LOA ARTO
300     321     SEND30  JTC MAC=CPR     SEND31
301     312
302      23     .       INC MACC
303     220     .       JFC OFLO        SEND2
304     236
305      20     .       CLR MACC
306      33     .       INC MACR
307     220     .       JFC OFLO        SEND2
310     236
311      30     .       CLR MACR
312     167     SEND31  TSB=XRS
313     204     .       JFC TSB5        SEND31
314     312
315     163     .       TSB+LIT
316     150     .       LOA LIT
317      15
320     123     .       LOA ARTO
321     167     SEND32  TSB=XRS
322     204     .       JFC TSB5        SEND32
323     321
324     206     .       JFC TSB7        SEND32
325     321
326     122     .       CLR RTSO
327     340     .       JTC PROTM       IDLE1
330      32
331     100     .       JMP             NEWLIN
332     236
333     202     SEND4   JFC TSB3        SEND30
334     300
335     301     .       JTC TSB2        SEND3
336     271
337     167     SEND41  TSB=XRS
340     205     .       JFC TSB6        SEND41
341     337
344     163     .       TSB=LIT
345     150     .       LOA LIT
346      33
347     123     .       LOA ARTO
```

DATA FROM MEMORY (Continued)

```
350     167     SEND42      TSB=XRS
351     205     .           JFC TSB6        SEND42
352     350
353     204     .           JFC TSB5        SEND42
354     350
355     163     .           TSB=LIT
356     150     .           LOA LIT
357      51
360     123     .           LOA ARTO
361      63     .           SET STB2
362     101     .           JMP             SEND3
```

IDLE

```
21      317     IDLE        JTC KEYRES      RESET
22        0
23      120     .           SEL ARTO
24      167     .           TSB=XRS
25      300     .           JTC TSB1        RCVDAT
26      147
27      204     .           JFC TSB5        IDLEO
30       34
31      206     .           JFC TSB7        IDLEO
32       34
33      122     .           CLR RTSO
34      171     IDLEO       TSB=STB
35      311     .           JTC KEYBRK      KBRK
36       57
37      300     .           JTC TSB1        IDLE
40       21
41      310     .           JTC KEYSTR      KEYST
42      127
43      212     .           JFC KEYHIS      IDLE
44       21
```

TABLE III.10 – ADM-1 INSTRUCTION SET

001	READ		123	LOA	ARTO	223	JFC	OPT2
003	WRITE		124	CLR	ARTO	224	JFC	OPT3
004	CLR	WDR	130	SEL	ART1	240	JFC	PROTM
005	LOA	WDR	131	SET	RTS1	241	JFC	PROT
006	SET	WPROT	132	CLR	RTS1	242	JFC	KEYCTRL
007	CLR	WPROT	133	LOA	ART1	243	JFC	KEYSHFT
016	SET	PROTM	134	CLR	ART1	244	JFC	ONLINE
017	CLR	PROTM	150	LOA	LIT	245	JFC	CONV
020	CLR	MACC	156	CLR	LRC	246	JFC	FULLDX
021	LOA	MACC	157	CLK	LRC	247	JFC	OPT4
022	SET	MACC	160	TSB =	RDR	300	JTC	TSB1
023	INC	MACC	161	TSB =	KEY	301	JTC	TSB2
024	DEC	MACC	162	TSB =	RCV	302	JTC	TSB3
027	LOA	CPR	163	TSB =	LIT	303	JTC	TSB4
030	CLR	MACR	164	TSB =	CPC	304	JTC	TSB5
031	LOA	MACR	165	TSB =	CPR	305	JTC	TSB6
032	SET	MACR	166	TSB =	LRC	306	JTC	TSB7
033	INC	MACR	167	TSB =	XRS	307	JTC	TSB8
034	DEC	MACR	170	TSB =	ADD	310	JTC	KEYSTR
037	SET	BEEP	171	TSB =	STB	311	JTC	KEYBRK
060	CLR	STB1	177	ERROR		312	JTC	KEYHIS
061	SET	STB1	200	JFC	TSB1	313	JTC	KEYSTR2
062	CLR	STB2	201	JFC	TSB2	314	JTC	KEYLCL
063	SET	STB2	202	JFC	TSB3	315	JTC	KEYRCV
064	CLR	STB3	203	JFC	TSB4	316	JTC	KEYPRT
065	SET	STB3	204	JFC	TSB5	317	JTC	KEYRES
066	CLR	STB4	205	JFC	TSB6	320	JTC	OFLO
067	SET	STB4	206	JFC	TSB7	321	JTC	MAC=CPR
070	CLR	STB5	207	JFC	TSB8	322	JTC	OPT1
071	SET	STB5	210	JFC	KEYSTR	323	JTC	OPT2
072	CLR	STB6	211	JFC	KEYBRK	324	JTC	OPT3
073	SET	STB6	212	JFC	KEYHIS	340	JTC	PROTM
074	CLR	STB7	213	JFC	KEYSTR2	341	JTC	PROT
075	SET	STB7	214	JFC	KEYLCL	342	JTC	KEYCTRL
076	CLR	STB8	215	JFC	KEYRCV	343	JTC	KEYSHFT
077	SET	STB8	216	JFC	KEYPRT	344	JTC	ONLINE
100	JMP		217	JFC	KEYRES	345	JTC	CONV
120	SEL	ARTO	220	JFC	OFLO	346	JTC	FULLDX
121	SET	RTSO	221	JFC	MAC=CPR	347	JTC	OPT4
122	CLR	RTSO	222	JFC	OPT1			

IV. MONITOR DESCRIPTION

The TV monitor is a solid-state unit for use in industrial and commercial installations where reliability and high quality video reproduction are desired.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized. The synchronization circuits have been custom designed to accept vertical and horizontal drive signals thus enabling the interfacing of this monitor with industrial or simple sync sources. This feature simplifies the user's sync processing and mixing and allows the unit to operate without requiring composite sync. The electronic packaging has been miniatured for compatibility with small volume requirements.

MONITOR ELECTRICAL SPECIFICATIONS

TABLE IV.1 – INPUT DATA SPECIFICATIONS

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory – Available) Printed circuit board card edge connector – Viking No. 2VK10S/1-2 or Amphenol No. 225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec or greater	Pulse Rate: 47 to 63 pulses/sec	Pulse Rate: 15,000 to 16,500 pulses/sec
Amplitude	Low = Zero $^{+0.4}_{-0.0}$ volts (See Section 1, paragraph 1.5) High = 4 ± 1.5 volts (See Section 4, paragraph 4.4)		
Signal Rise and Fall Times (10% to 90% amplitude)	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec
Input Signal Format	See Figure 1		

DATA DISPLAY SPECIFICATIONS

Input Impedance

	Minimum Shunt Resistance	Maximum Shunt Capacitance
(a) Video Input:	3.3 k ohms	40 pF
(b) Vertical Drive Input:	3.3 k ohms	40 pF
(c) Horizontal Drive Input:	470 ohms	40 pF

Video Amplifier

(a) Bandwidth:	12 MHz (-3 dB)
(b) Rise and Fall Times (10% to 90% amplitude):	Less than 35 nsec (linear mode)
(c) Storage Time:	15 nsec, maximum (linear mode)

Retrace and Delay Times

(a) Vertical:	900 μsec retrace, maximum
(b) Horizontal:	7 μsec retrace plus 4 μsec delay, maximum

TABLE IV.2 – CATHODE RAY TUBE DISPLAY SPECIFICATIONS

Nominal Diagonal Measurement (inches)	Phosphor	*Resolution (TV Lines)	
		Center	Corner
12	P4	900 at 40 fL	800 at 40 fL
12	P31	900 at 20 fL	800 at 20 fL

*Resolution is measured in accordance with EIA RS-375 except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within ±1.5% of the rectangle height.

Power Requirements

Input Connector	Receptacle, Molex No. 03-06-1041 Supplied with Unit Mating Plug, Molex No. 03-06-2041 – Necessary Accessory (Available)
Input Voltage	105 V to 130 V rms (120 V nominal); 50/60 Hz
Input Power	24W (Nominal)
Output Voltages	+15 V DC (short circuit protected) +12 kV DC; 12.6 V rms

ENVIRONMENTAL SPECIFICATIONS

Temperature (Chassis or Custom Unit)

Operating Range:	5°C to 55°C Ambient
Storage Range:	-40°C to 65°C

Humidity

5 to 80 percent (Noncondensing)

Altitude

Operating Range:	Up to 10,000 feet

HUMAN FACTORS SPECIFICATIONS

X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78

CONTROLS

(1) Contrast, 500 ohm potentiometer carbon composition $\geq$ 1/8 Watt

(2) Brightness, 100 kilohm potentiometer $\geq$ 1/8 Watt

Optional: The Brightness Control can be mounted on the printed circuit board as an internal set up control.

Internal Set Up Controls

(1) Height

(2) Vertical Linearity

(3) Vertical Hold

(4) Focus

(5) Width

(6) Low Voltage Adjust

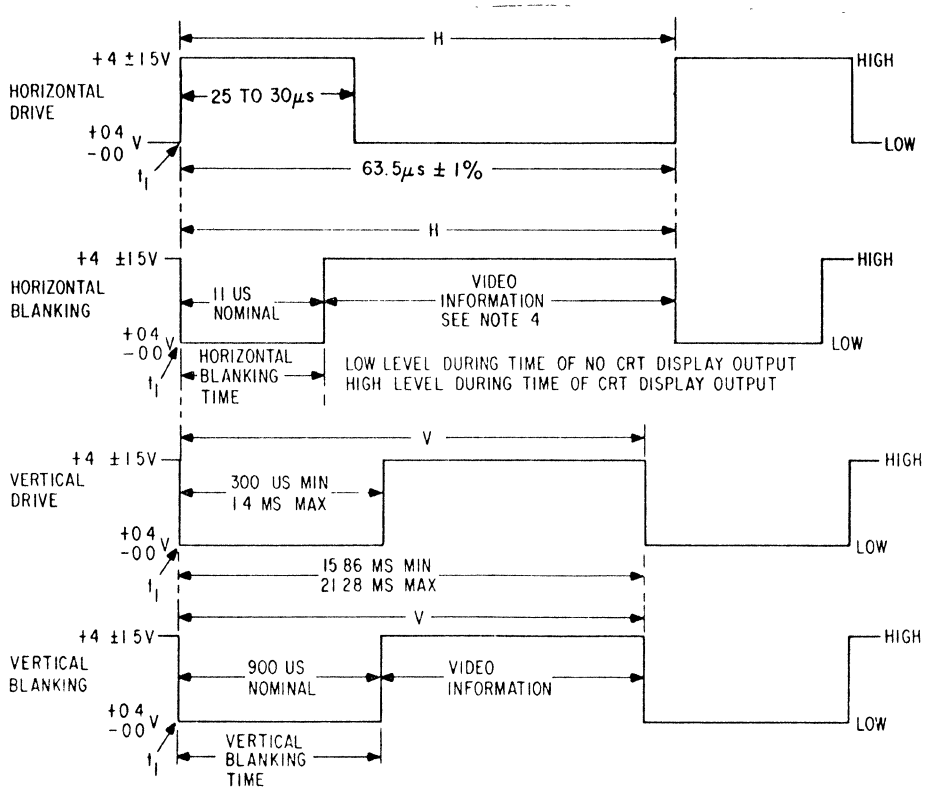


Figure IV.1 — Synchronization and Blanking Generator Waveforms

NOTES:

1. The leading edges of Drive and Blanking waveforms must start at time t_1. Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17. Q104, operating as a class B amplifier, remains cutoff until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

VERTICAL DEFLECTION

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and Capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gage "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional unijunction transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During re-

trace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

HORIZONTAL DEFLECTION

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (Section 1.2) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on

its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 kV (9 and 12 inches) or 9 kV (5 inches), "C" VDC, and "B" VDC respectively. 12 kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

LOW VOLTAGE REGULATED SUPPLY

All models use a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener voltage of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201 where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector

voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are often used for this purpose; however, in the majority of cases, these devices are not fast enough to protect transistors.

V. INSTALLATION, MAINTENANCE AND FAILURE ANALYSIS

The ADM-1 Data Display Terminal is self-contained, suitable for desk or tabletop mounting in a normal office or commercial environment. It requires both power connection and data signal interface connection to the computer or optional printer.

INSTALLATION

Prior to installing the ADM-1, make sure the ON-OFF switch is in the OFF position.

(1) Connect the data interface cable to the terminal with a 25-pin connector using the appropriate pins designated in Table V.1 below, depending upon whether the installation is 20 ma current loop interface or RS-232-C standard.

NOTE:

If the data interface in use does not supply a clear-to send (CB) signal on pin 5, then jumper pins 4-5.

(2) Plug in the ADM-1 into a grounded A.C. outlet of the proper voltage and frequency.

(3) Turn the ON-OFF rocker switch to ON.

TABLE V.1 – DATA INTERFACE CONNECTOR J1 SIGNAL/PIN LIST (AMPHENOL Part No. 17-304-01)

Pin No.	Signal Function			Code
1	Equipment Ground			AA
2	Transmit Data			BA
3	Receive Data			BB
4	Request to Send			CA
5	Clear to Send			CB
6	Data Set Ready			
7	Signal Ground			AB
8	Received Line Signal Detector			
9	Current Loop Power			
*10	Current Loop OUTPUT	+	Receive	
*11	Current Loop RETURN	-	Receive	
*12	Current Loop INPUT	+	Transmit	
*13	Current Loop RETURN	-	Transmit	
15	Transmitter Signal Element Timing			
17	Receiver Signal Element Timing			
20	Data Terminal Ready			CD

* Current Loop Interface Only

CARE OF THE ADM-1

Your ADM-1 Terminal with its solid state and modular electronics is easier to care for than an electric typewriter. Just give it a light cleaning from time to time, and it will remain as attractive as it is functional.

Lightly dust the unit using a brush or soft damp lint-free cloth. Paper towels are fine. Conventional spray cleaners work great for stubborn smudges and fingerprints. Do not use petroleum-base cleaners such as lighter fluids. These could harm the plastic or painted surfaces. Avoid wiping dust or lint into the keyboard area. If using a spray cleaner, prevent excessive spraying which could run down between the keys.

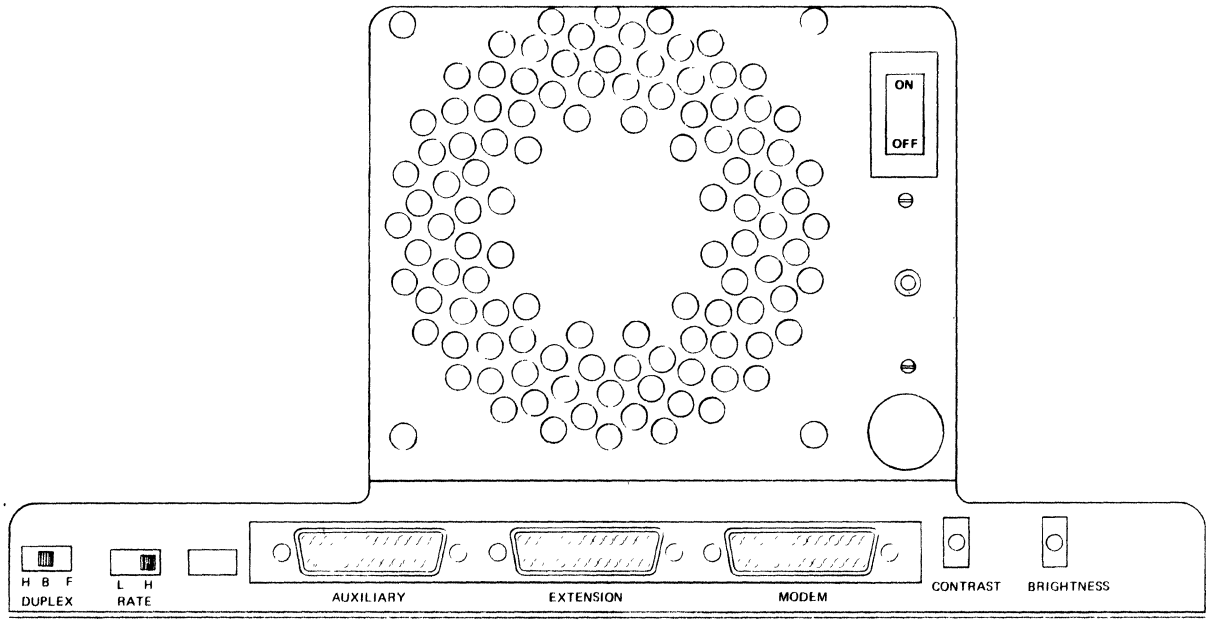


Figure V.1 — ADM-1 Back Panel View

ADJUSTMENTS

External controls on the rear of the ADM-1 assembly include the following which are illustrated in Figure V.1.

On/Off Switch

This two position switch controls the A.C. power to the unit and certain power-up and power-down sequences. Setting the switch to the ON position resets the circuitry within the ADM-1, positions the cursor to home and clears the display memory to unprotected nulls.

Baud Rate

The baud rate selector switch selects the desired baud rate as specified on equipment purchase. The "High" position is normally set for 1200 unless specified to the contrary. The "Low" position selects the lower of two specified rates. Baud rates can be changed replacing a plug-in piggy back terminal trip containing necessary resistors and diodes. (See Options, Appendix A).

Mode Selector Switch

This three position switch selects the mode of operation. The Block position sets the "Block" mode. The Full and Half positions select the appropriate full or half-duplex conversational mode.

Brightness Control

This potentiometer controls the overall brightness of the CRT display. Brightness is usually adjusted so the display raster (background) is barely visible or just below the point of visibility.

Contrast Control

The contrast adjustment potentiometer controls the character brightness relative to the background. Contrast is usually adjusted after the brightness control.

KEYBOARD MAINTENANCE

The keyboard is considered a single replacement part except for the keys and mounting hardware. The standard keyboard assembly has 53 keys which operate switches and provide pulses to the logic board which generates the ASCII characters for transmission or display.

The keyboard assembly may be replaced as a complete unit or by replacing integrated key rows. To remove the keyboard for trouble-shooting or replacement, first disconnect the connector at the rear of the keyboard. Then remove the two screws on each end and lift the keyboard out. When a keyboard is replaced, re-install the cover and check to see if any keys are binding against the case.

The ASCII code generated by each key is shown in Table II.2 and the electrical input-output identifications are shown in Table V.3. below.

TV MONITOR ADJUSTMENTS

SYNCHRONIZATION AND DRIVE SIGNALS

Apply horizontal and vertical drive signals to the horizontal and vertical drive terminals as indicated on your schematic. Adjust their levels to a nominal +4 V peak-to-peak. The duty cycle of each signal must be adjusted as described above.

The horizontal drive signal is required to initiate horizontal scan and high voltage, and should be connected before applying power to the monitor.

LOW VOLTAGE SUPPLY

Set the DC voltage by variable resistor R208 as indicated on the schematic. This voltage can be monitored at the junction of R114 and R130.

BRIGHTNESS

Normally, the monitor will be used to display alphanumeric or other black and white information. Moreover, the usual video polarity produces white characters on a black background.

The brightness control should be adjusted at a point where the white raster is just extinguished. The CRT will then be at its cutoff point, and a maximum contrast ratio can be obtained when a video signal is applied.

VIDEO CONTRAST

Q101 is designed to operate linearly when a +2.5 V signal is applied to its base. The ADM-1 incorporates a 500 ohm external contrast control to maintain this level. This control should be adjusted for a typical signal level of +2.5 V peak-to-peak when measured at the video input terminal of the printed circuit board edge connector. (Refer to the schematic.)

In all cases, the output DC impedance of the video signal source must be 500 ohms, or less.

VERTICAL ADJUSTMENTS

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

(1) Apply video and synchronization signals to the monitor.

(2) Set the vertical frequency control, R116, near the mechanical center of its rotation.

(3) Adjust the vertical height control, R124, for desired height.

(4) Adjust the vertical linearity control, R121, for best vertical linearity.

(5) Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

(6) Readjust the vertical frequency control, R116, until the picture rolls up slowly.

(7) Restore vertical drive to the monitor.

(8) Recheck height and linearity.

HORIZONTAL ADJUSTMENTS

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

(1) Apply video and synchronization signals to the monitor. Inser the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.) If the linearity sleeve is inserted farther than necessary, excessive power will be consumed, and the horizontal output circuitry could be overstressed.

(2) Adjust the horizontal width coil, L101, for the desired width.

(3) Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

(4) Readjust L101 for proper width.

(5) Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor. The raster should be properly locked and centered when the horizontal drive signals as described above are used.

FOCUS ADJUSTMENT

The focus control, R107, provides an adjustment for maintaining best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large effect on focus.

CENTERING

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

PHILOSOPHY OF FAILURE ANALYSIS

Effective trouble shooting is accomplished in a minimum of time by following a series of logical steps. The ultimate aim is to effectively pinpoint the actual problems using all the information available.

Locating the malfunction is then the first logical step. The following is a suggested plan for effective casualty analysis.

(1) Investigate – record the state of the machine when the error occurred. Look for obvious symptoms including operator error, loose plugs or connectors, data set error, blown fuses or computer error.

(2) Isolation – Modular replacement is the quickest method of isolation where the replacement is available. Isolation to one of the following: circuit board, keyboard module, video monitor, power supply or inter-connecting wires should be the first step in isolation.

(3) Component Isolation – Isolation to a smaller component may be accomplished in some cases with the use of oscilloscope and multimeter.

(4) Replace the faulty module or component and retest by running the same operation in the same state the error occurred.

(5) Record for future reference the symptoms, cause and module or component isolation method used.

FAILURE ISOLATION

This section will explain briefly the approach to failure isolation and then describe a simple checkout procedure upon power turn-on.

The display terminal consists of a monitor assembly, power supply, keyboard and logic board. All assemblies are replaceable by simply disconnecting cables and removing attaching screws. To remove the cover for inspection or assembly replacement, remove the five screws on the side and back of the terminal.

The following will give you some helpful things to look and listen for what might indicate the problem area. Each assembly is described as to the function it performs along with a brief procedure to replace the assembly. At the end of this section is Table V.2, describing problems or symptoms and the most likely assembly to be at fault.

(1) Ensure the ADM-1 power cord is plugged into a grounded A.C. outlet of the proper voltage and frequency.

(2) Set the ON/OFF Switch on the rear of the ADM-1 to the "ON" position.

(3) Check to see if the fan starts when power is turned on. If it does not, check the power switch and push red circuit reset button.

(4) At turn on, listen for an audible 1 to 2 KHz tone that lasts approximately one second (only in units with beeper). This tone is caused by the horizontal oscillator starting and may not be heard where there is high ambient noise. If no tone is heard, look for cursor as in (5) below.

(5) If the cursor does not appear after a normal warm-up period, type the HOME key. If this fails to produce the cursor, reset the display by simultaneously pressing

the CTRL, SHIFT, REPT and CLR HOME BRK keys. If still no cursor, it is possible the brightness and/or contrast controls are misadjusted. They are adjusted as follows:

(a) Set the contrast control to the middle of its range.

(b) Turn the brightness control clockwise until the screen is bright, then reduce brightness slowly until the background is barely visible. The cursor should be present.

(c) Adjust brightness and contrast for desired presentation.

(d) If the cursor does not appear, check the power supply voltage; replace the monitor if necessary.

(6) If the problem is associated with transmitting and receiving of data to and from the computer, use the following procedure: Place the full-half duplex switch in full position. Remove the cable from the terminal output connector and jumper pins 2 and 3 and jumper pins 4 and 5 on the terminal connector together. Now, whatever is typed on the keyboard should appear on the screen. This test checks the transmission of characters from the keyboard and display of those characters in non-BLOCK mode. To test the function of character storage in memory, run the cursor to the bottom of display and test page ROLL functioning of displayed characters roll upward as expected, memory storage of characters is functional.

TROUBLESHOOTING THE MONITOR

The monitor receives video and sync signals from the control board and performs normal TV functions. The high voltage for the monitor is generated from its own self-contained power supply. In addition, the monitor assembly includes its own low voltage (15V D.C.) power supply.

CAUTION

DISCHARGE HIGH VOLTAGE BEFORE ATTEMPTING TO REMOVE MONITOR ASSEMBLY.

TABLE V.2 – ADM-1 FAILURE ANALYSIS GUIDE

Type of Failure	Probable Location of Failure			
	Logic Board	Keyboard	Power Supply	Monitor
Audio Signal	1	2		
Clear Memory	1	2		
Clear Memory (Power Up)	1			
Cursor Control	1	2		
EDIT Control Option	1	2		
Parity Error	1			
Receive Data*	1			
Transmit Data*	1	2		
Video:				
Character/No Cursor	1			
No Character/Cursor	1			
No Character/No Cursor	3		1	2
Data/No Sync	2			1
Data Wavy			1	2
Randomly Generated, Wrong Characters**	2	1		

*Check word structure specification and baud rate.

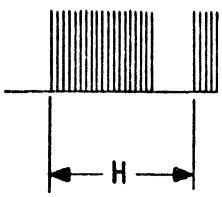
**Insure good connection of cable from keyboard to logic board.

MONITOR TROUBLESHOOTING GUIDE

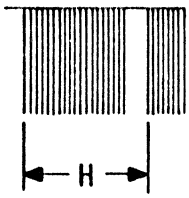
	Symptom	Possible Remedy
1.	Screen is dark	Check "A" bus Q106, Q105, CR2
2.	Loss of video	CR105, Q101
3.	Power consumption is too high	Check horizontal drive waveform; Check proper placement of horizontal linearity sleeve; Q105, Q106
4.	Low voltage bus incorrect (for units with a low voltage supply)	Q202, Q203, Q1 (Note: Low voltage supply will indicate low or "0" volts due to its current limiting action if a short is evident in the "A" volt line.

The voltage waveforms are shown in Figure V.2. Refer to Appendix C for interconnecting cabling diagrams, circuit board component locations and monitor schematic.

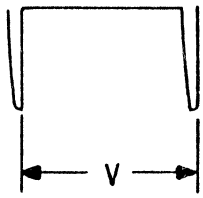
WAVEFORMS



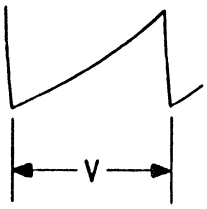
Q101-B
2.5V P-P



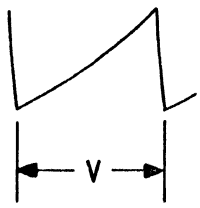
VI-CATHODE
20V P-P



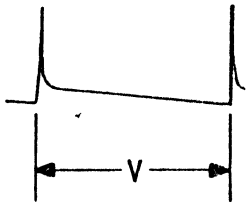
CR101-ANODE
3V P-P



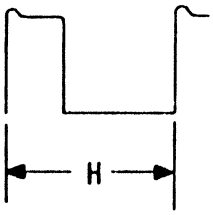
Q103-B
4.5V P-P



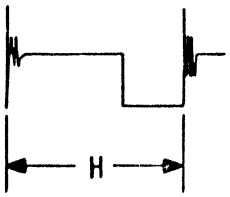
Q104-B
1.2V P-P



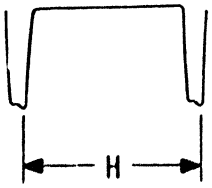
Q104-C
45V P-P



Q105-B
3V P-P



Q105-C
30V P-P



Q106-C
170V P-P

Figure V.2 — Voltage Waveforms for Monitor

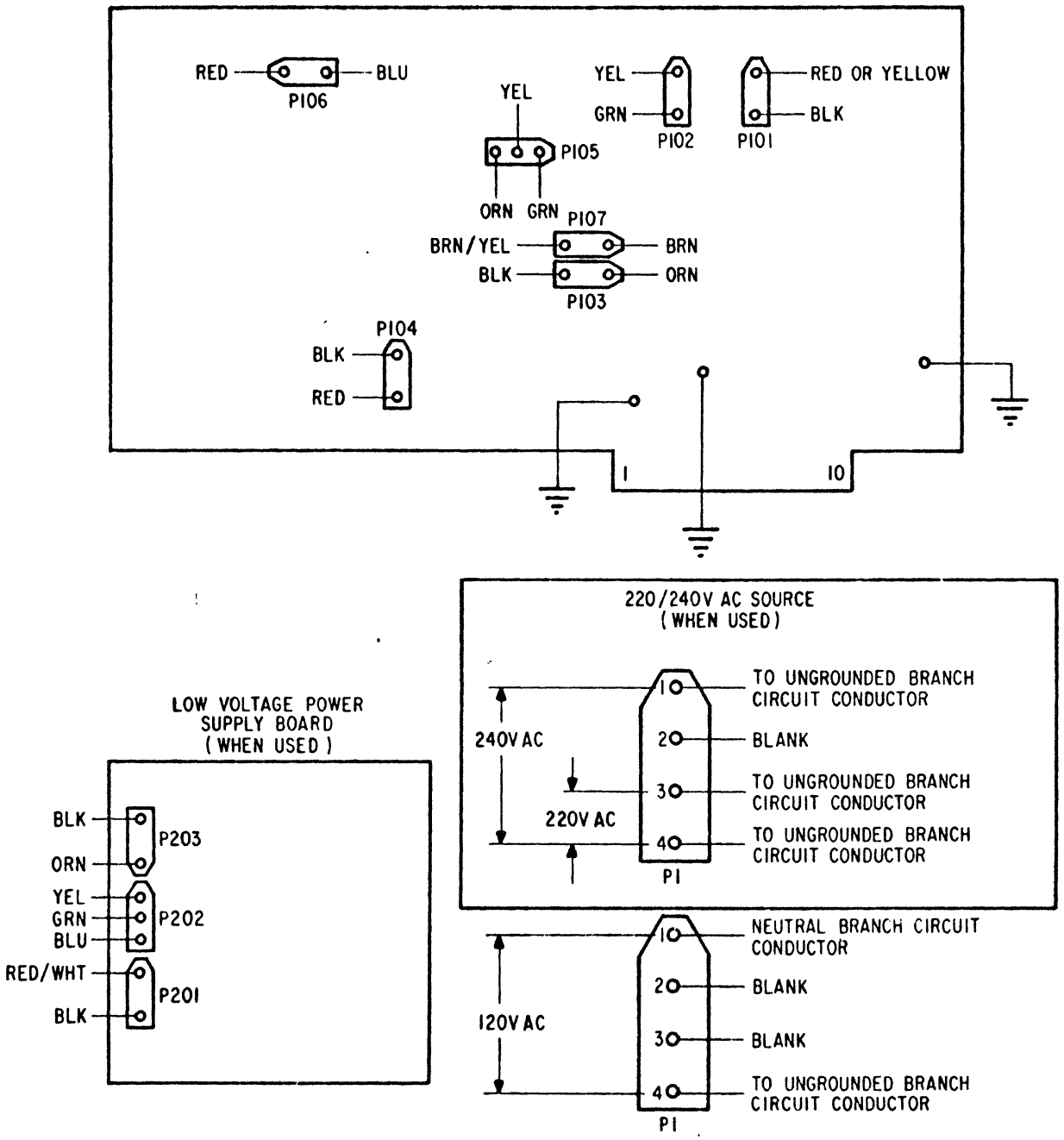


Figure V.3 – Monitor Interconnecting Cabling Diagram

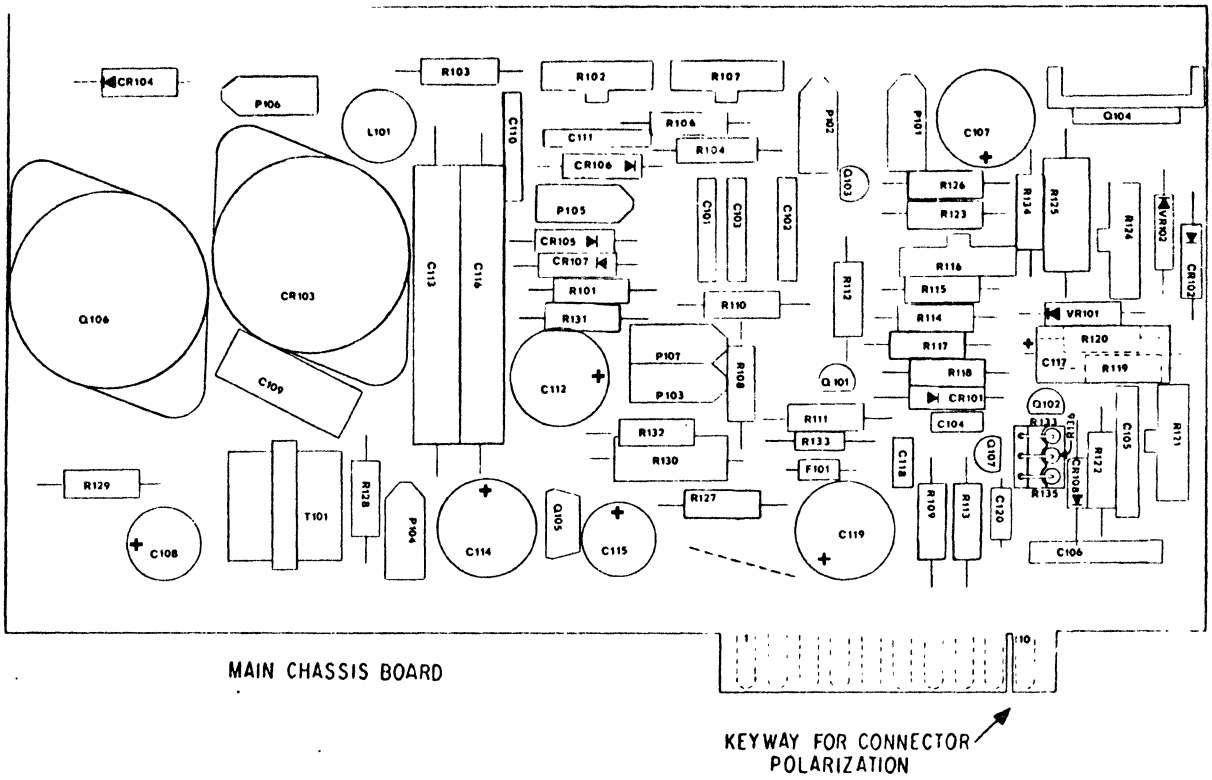


Figure V.4 – Monitor Circuit Board Components Location

MAINTENANCE OF MAIN LOGIC BOARD AND POWER SUPPLY

The main logic board is essentially a self-contained functional unit with one exception: D-C logic level +5 Volts is obtained from a separate POWERTEC power supply.

For maintenance and trouble shooting, refer to Table V.3 for identification of connectors and terminals external to the main logic board and normal input-output signals.

Connector J1 is used for Data Signal interface connection to the main logic board. Connectors J2 and J3 are used for the same purpose with RS232C Extension Option and Serial Printer Option, respectively.

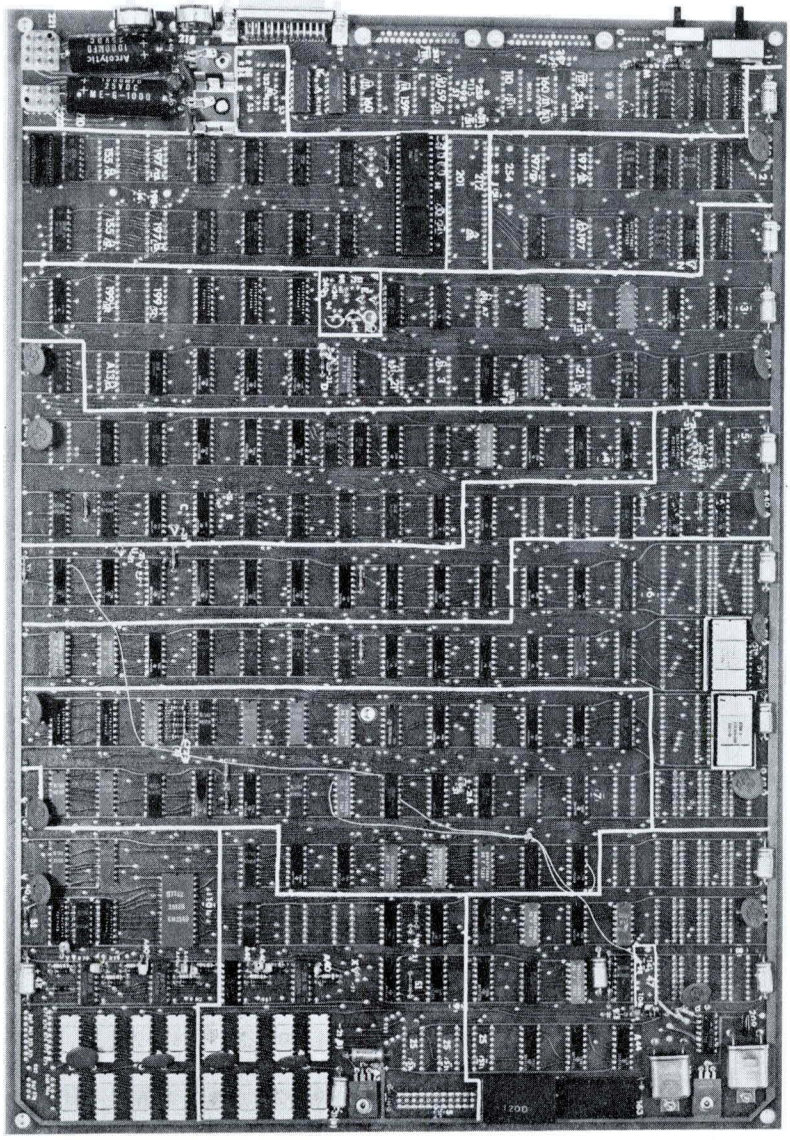


Figure V.5 — Main Logic Printed Circuit Board Assembly

TABLE V.3 – MAIN LOGIC BOARD TERMINAL IDENTIFICATION CHART

Connector	Symbol	Pins	Function
RS232C Interface	J1	1-25	See Table V.1
RS232C Extension	J2	1	Equipment Ground
		2	Transmit Data
		3	Receive Data
		4	Request to Send
		5	Clear to Send
		6	Data Set Ready
		7	Signal Ground
		8	Received Line Signal
		15	Transmitter Signal Element Timing
		17	Receiver Signal Element Timing
		20	Data Terminal Ready
Serial Printer (Option)		1	Equipment Ground
		2	–
		3	Receive Data
		6	Printer Ready
		7	Signal Ground
		8	Receiver Line Signal
		20	Printer Ready
Monitor I/O	J4	1	Brightness
		2	Brightness
		3	Brightness
		4	Contrast
		5	Chassis Ground
		6	Video & Video Ground
		7	Horizontal Ground
		8	Horizontal Drive
		9	Vertical Drive
Logic Board Power	J5	1	AC Feed
		2	AC Feed
		3	Equipment Ground
		4	Speaker
		5	Speaker
		6	D-C Feed
Keyboard I/O	J6	1	Power
		2	SHIFT
		3	CTRL
		4	BRK
		5	SEND
		6	STROBE
		7	REPEAT
		8	SIGNAL COMMON
		9	BIT1
		10	BIT2
		11	BIT3
		12	BIT4
		13	BIT5
		14	BIT6
		15	BIT7
		16	LINE16

			TSB 1	2	3	4	5	6	7	8
INPUTS to	RDR	sh 12	M1-3	M1-4	M1-5	M1-6	M2-3	M2-4	M2-5	M2-6
	KEY	sh 16	C1-8	C1-6	C1-11	C1-3	B1-8	B1-6	B1-11	B1-3
	RCV	sh 13	C5-8	C5-6	C5-11	C5-3	B7-8	B7-6	B7-11	B7-3
	LIT	sh 22	C14-8	C14-6	C14-11	C14-3	B14-8	B14-6	B14-11	B14-3
	CPC	sh 23	C6-8	C6-6	C6-11	C6-3	B5-8	B5-6	B5-11	B5-3
	CPR	sh 23	C4-8	C4-6	C4-11	C4-3	B4-8	B4-6	B4-11	B4-3
	LRC	sh 23	C3-8	C3-6	C3-11	C3-3	B3-8	B3-6	B3-11	B3-3
	XRS	sh 13	C7-8	C7-6	C7-11	C7-3	B6-8	B6-6	B6-11	B6-3
	ADD	sh 26	C12-8	C12-6	C12-11	C12-13	B12-8	B12-6	B12-11	B12-3
	STB	sh 26	C11-8	C11-6	C11-11	C11-13	B11-8	B11-6	B11-11	B11-3
OUTPUTS of	COND	sh 24	B13-4	B13-3	B13-2	B13-1	B13-15	B13-14	B13-13	B13-12
	MACC	sh 7	F7A-1	F7A-12	F7A-4	F7A-9	H6-1	E1-5 / F2-2	F2-1	
	MACR	sh 7	H6-10	E3-4	E3-9	E3-1	E3-12			
	WDR	sh 12	L1-4	L1-5	L1-12	L1-13	L2-4	L2-5	L2-12	L2-13
	$\overline{\text{NULLO}}$	sh 12	C14-9	C14-5	C14-4	C14 3	C14-11	C14.2	C14-10	
	XMTR	sh 13	B8-26	B8-27	B8-28	B8-29	B8-30	B8-31	B8-32	B8-33
	OPTION 51	sh 15	B10-26	B10-27	B10-28	B10-29	B10-30	B10-31	B10-32	B10-33
	LRC	sh 23	C2-9	C2-5	C2-12	C2-2	B2-9	B2-5	B2-12	
	COND INHIBIT	sh 24	A13-10	A13-11	A13-12	A13-13	A13-14			

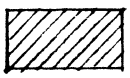
OPTIONS = 

Figure V.6 — Tri-State Bus Signal Locations

Connector J4 is used to supply output signals from the main logic board to the CRT monitor. If proper signals are present at terminals of connectors J5 and J6, examine the integrity of connector pins on P4. Examine for obvious faults on main logic board. It is strongly recommended that no involved repairs be attempted on this board. Instead, contact the factory or authorized service representative.

Connector J5 primarily handles inputs to main logic. Therefore, the absence of proper inputs at terminals 1, 2, and 3 indicates failure in AC power feed. Likewise, lack of proper voltage at terminal 6 indicates problem with chassis mounted power supply or connector cable. Improper signals on terminals 4 and 5 indicate trouble with main logic board.

If noted signal levels are not present at terminals of connector J6 as keyboard is operated, examine keyboard assembly for obvious faults. Either repair or replace keyboard assembly.

Keyboard output levels are compatible with TTL circuits with logic "1" greater than +2.6V at .10 ma and logic "0" less than 0.6V. The outputs are bounce free so that only one signal will be generated for each key depression. Two-key rollover interlocking is provided for all encoded keys. If a key is depressed before a previous operated key is released, the second key code is transmitted after the first key is released. A strobe pulse is provided with each encoded key output.

POWER SUPPLY

D.C. Voltages of -5, +12 and -12 volts utilized within the main logic board are generated by regulator IC chips on that board. A separate +5 volt power supply for logic level voltage is mounted above the main circuit board on the chassis.

Recommended adjustment procedure for the separate power supply is as follows:

(1) Adjust current limit potentiometer to maximum current output (this should correspond to normal operating position).

CAUTION:
DISCONNECT OUTPUT LOAD BEFORE PROCEEDING THROUGH THE FOLLOWING STEPS.

(2) Adjust overvoltage protection potentiometer to the maximum position.

(3) Adjust output voltage to 6 volts D.C.

(4) Adjust the overvoltage protection potentiometer down to the point where output voltage shuts off.

(5) Turn down output voltage to overvoltage protection control or lowest setting, then bring the output voltage back up again and adjust the output (watching the output meter) until it gets to 6 volts D.C., then the output should go back to overvoltage D.C.

(6) If the overvoltage protection adjustment is correct, then adjust the output voltage control up to 5.2 volts D.C., which is the normal operating voltage.

Maintenance and trouble shooting of the separate power supply are included in the following pages.

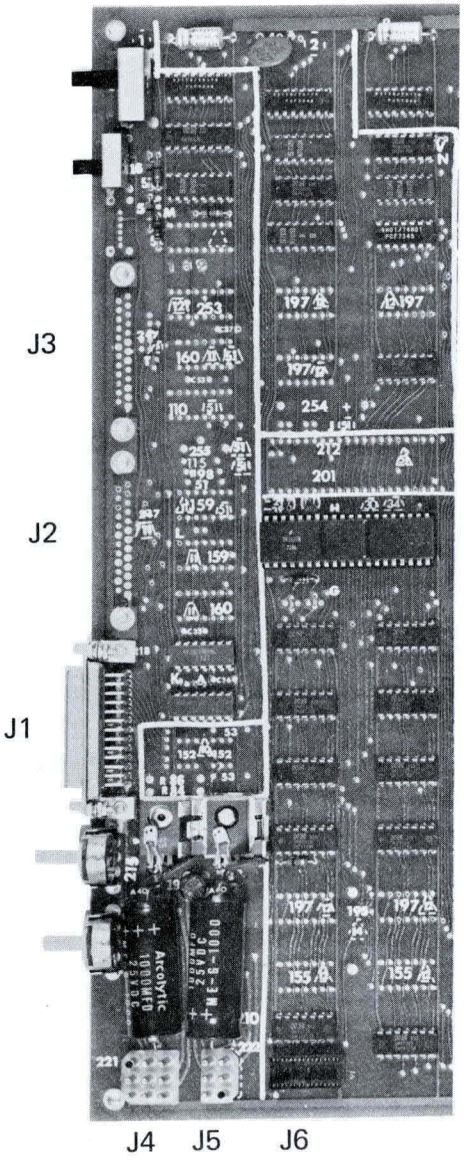


Figure V.7 – Main Logic Printed Circuit Board Connections

POWERTEC
AN AIRTRONICS SUBSIDIARY
9168 DESOTO AVENUE
CHATSWORTH, CALIFORNIA 91311
(213) 882-0004 TWX 910-494-2092

SUB-MODULAR D.C. POWER SUPPLY

MODULE 22C-100

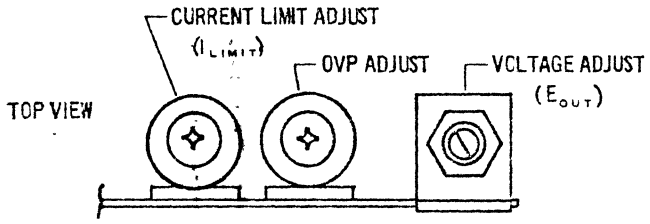
MODEL NUMBER–

ASSEMBLY NUMBER–

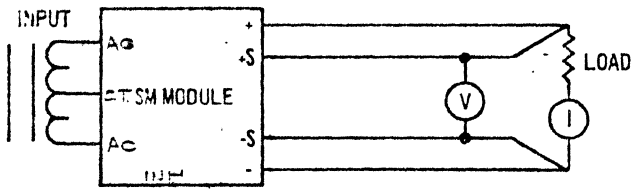
SPECIFICATIONS

WARNING: Requires power transformer to reduce line voltage to recommended input level.

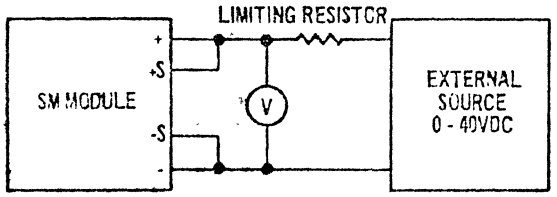
OUTPUT VOLTAGE	4.75V TO 7.0V
OUTPUT CURRENT	6.0A @ 5V- 5.2A @ 6V
LINE REGULATION	± .075%
LOAD REGULATION	± .075%
RIPPLE PEAK-PEAK	<5MV
OVERCURRENT	50-130% OF FULL RATED LOAD
OVER VOLTAGE	105-135% OF RATINGS



POTIENTIOMETER LOCATION
FIGURE 1



CONNECTION DIAGRAM
FIGURE 2



OVP ADJUST SET-UP
FIGURE 3

ADJUSTMENT PROCEDURE

VOLTAGE ADJUST

Adjust output voltage to desired level at no load with unit connected as shown in figure 2. (Make sure OVP is in maximum clockwise position).

CURRENT LIMIT ADJUST

Adjust I_{LIMIT} to maximum clockwise position. Apply 125% of full load and adjust I_{LIMIT} until unit drops out of regulation 50 to 100mV.

CAUTION: SO NOT RUN UNITS OVER 5 MINUTES WITH OUT ADDITIONAL HEAT SI NK

OVP ADJUST

Remove input power and load and apply an external voltage through a limiting resistor as shown in figure 3. Adjust OVP adjust until firing occurs at desired voltage as the external source is slowly increased. Select limiting resistor to limit current to 0.5ADC maximum after firing.

Refer to SM sales brochure PT3-9-72 for additional information and design parameters.

COMPONENT REPLACEMENT

The replacement of a component on any printed circuit board requires care to prevent damage to circuit board etch. Clipping a component from the circuit board rather than unsoldering is the preferred method. Excessive heat from a soldering iron may result in damage to the component being replaced. The use of a soldering iron with an isolation transformer, a small copper alligator clip as a heat sink, and a delay between the soldering of individual pins of a chip are recommended.

In accordance with good maintenance practices, Lear Siegler does not recommend individual component replacement on any printed circuit board. Instead, it is recommended the factory be contacted relative to availability of special test equipment or factory rebuilt and tested replacement assemblies.

WARRANTY

Lear Siegler, Incorporated, Electronic Instrumentation Division certifies that each ADM-1 data display terminal will be free from defective materials and workmanship for a period of 90 days from date of shipment to the original customer. Lear Siegler agrees to correct any defects within warranty when the ADM-1 is returned, freight prepaid, to the factory at Anaheim, California. Written authorization must be obtained and confirmed in writing by Lear Siegler.

MALFUNCTION REPORT

Dear Customer:

We are trying to manufacture the most reliable product possible. You would do us a great courtesy by completing this form should you experience any failures.

1. Type Unit _____ Serial No. _____
   Module (if applicable) _____

2. Part failed (Name and Number) _____

3. Cause of failure (if readily available) _____
   _____
   _____
   _____

4. Approximate hours/days of operation to failure _____

5. Failure occurred during:
   ☐ Final Inspection ☐ Customer Installation ☐ Field Use

6. Personal Comment:
   _____
   _____
   _____

Customer _____
Address _____
Signed _____
Date _____

Mail to: DATA PRODUCTS CUSTOMER SERVICE

APPENDIX A

APPENDIX A

ADM-1 CONFIGURATION CONTROL

MONITOR – OPTION 1, 2

The standard monitor with P4 Phosphor is replaced by one of the following:

1. P4 Phosphor, Etched Face Plate:

   Instructions – Remove 129302-1 Monitor
   Install F/N 1 Monitor Etched Face Plate 129302-3

2. P31 Phosphor, Etched Face Plate

   Instructions – Remove 129302-1 Monitor
   Install F/N 1 Monitor 129302-4

KEYBOARD – OPTION 4

The standard keyboard and case are replaced by the following:

60 Key Option

Instructions – Remove 129304-1 Housing
Remove 129301-1 Keyboard
Install F/N 1 Keyboard and F/N 2 Case

CURRENT LOOP, 20 MA OPTION 10

Current Loop, 20 MA

Instructions – At location D7 install components:

F/N 2 Transistor	Q1, Q2	2N3904
F/N 3 Diode	CR19	1N914
F/N 4 Resistor, 39 1W	R40	
F/N 5 Resistor, 3K	R39	
F/N 6 Resistor 1K	R41	
F/N 7 Resistor 470	R42	

Remove Jumpers

Add Jumpers

(See Figure 1)

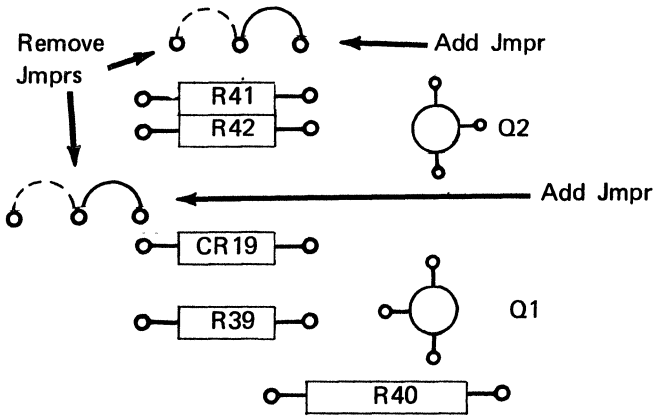


Figure 1

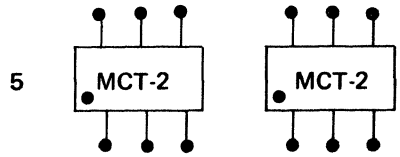


Figure 2

At location A5 install optical couplers F/N 1 (See Figure 2) MCT2 (Motorola)

RS 232 EXTENSION – OPTION 11

RS 232 Extensions

Instructions – Install Connector at J2

F/N 3 Bracket (Mount to Board with 1/8 pop-rivet or equivalent)

F/N 4 Conn. Body

F/N 7 Jack Screw

F/N 5 Pin, Short (at 15, 17, 20)

F/N 6 Pin, Long (at 1, 2, 3, 4, 5, 6, 7, 8)

Install Components

F/N 1 I.C.-1488 (at location A8, A9)

F/N 2 I.C.-1489 (at location A7.5, A11)

POLLING – OPTION 12

Parts List – I.C. (128578-XX)

Instructions – Install Components:

F/N 1 I.C. -30 at Location E2
F/N 2 I.C. -86 at Location B2, C2
F/N 3 I.C. -103 at Location D12, E12
F/N 4 I.C. -125 at Location B3, C3, B11, B12, C12
F/N 5 I.C. -175 at Location D2, D3
F/N 6 Switch at Location A12

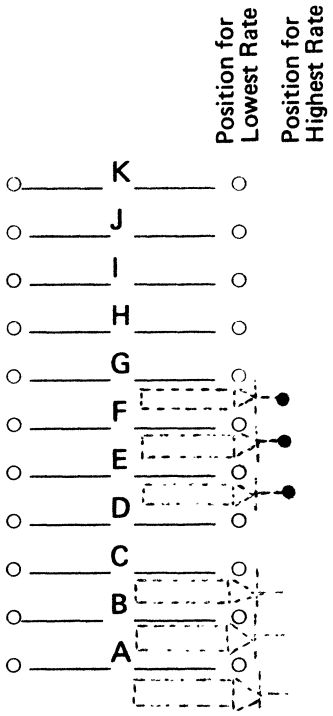
BAUD RATE – OPTION 20

(If no baud rate is selected, see attached sheet)

Parts List – Diode 1N914

Instructions – Install a diode (F/N 1) at each location indicated in the table below. The quantity of diodes to be installed will vary according to the baud rate. If highest rate is not 1200, see Note below.

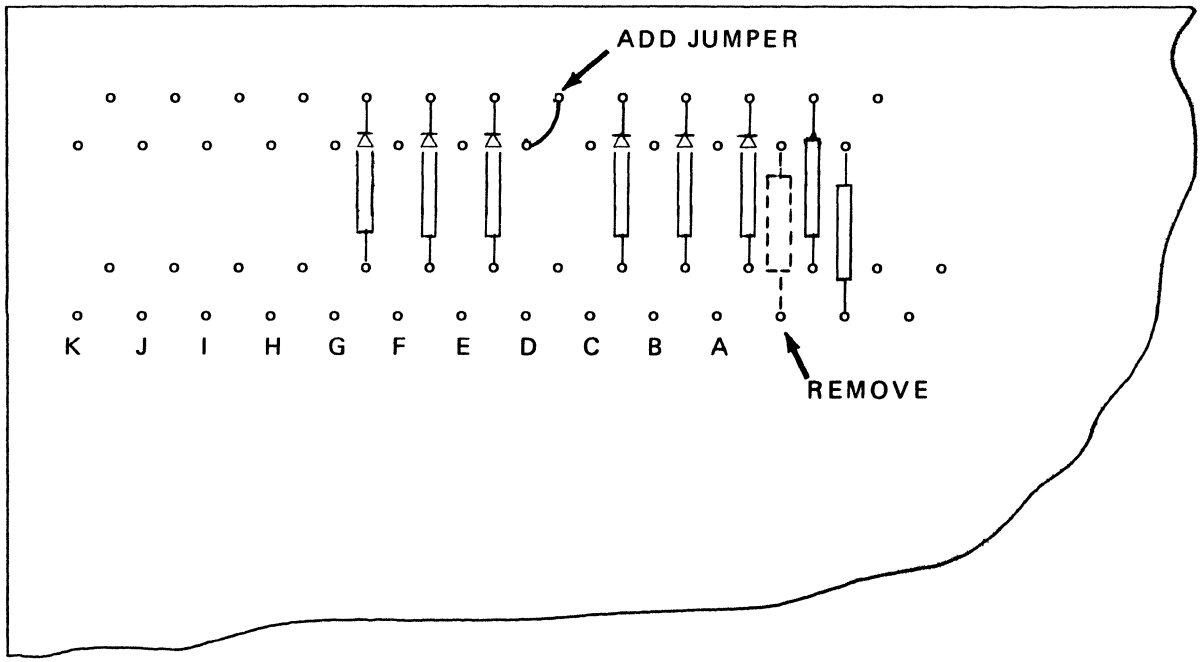
Location	BAUD RATE (Diode = 0)												
	110	150	300	600	1000	1800	2000	2400	3600	4800	7200	9600	1200
K	◁												
J		◁											
I	◁	◁	◁										
H		◁	◁	◁	◁								
G			◁	◁		◁	◁						◁
F		◁		◁				◁	◁				◁
E	◁	◁	◁					◁		◁	◁		◁
D	◁	◁	◁	◁	◁	◁		◁		◁		◁	
C	◁	◁	◁	◁	◁	◁	◁		◁	◁		◁	◁
B		◁	◁	◁	◁	◁	◁	◁	◁		◁	◁	◁
A		◁	◁	◁	◁	◁	◁	◁	◁	◁	◁		◁
Qty DIO	5	9	8	7	5	5	4	5	4	4	3	3	6



NOTE: 1200 baud is installed in the "H" position. If another rate is required, remove and add diodes as needed for the new rate.

BAUD RATE – OPTION 20 (Continued)

If no baud rate is selected, remove R21 and jumper as shown below. Baud rate will be 1200 in either switch position.



Diodes shown are 1200 baud per assy 129310.

Install baud rate module to select baud rates desired.

P/N 129307-XXXX

Where XXXX = baud rate

TO SELECT SPECIAL BAUD RATES

$$\text{Baud Rate} = \frac{4608000}{32 \cdot N}$$

Where $7 \leqslant N \leqslant 2048$

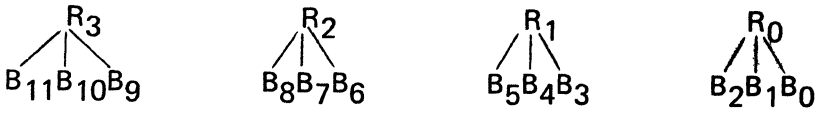
the limits are N = 7, Baud Rate = 20,571.5
N = 2048, Baud Rate = 70.3

To select the diodes required after N is known

1. Convert N to a 4 digit octal number called $N_3N_2N_1N_0$
2. Determine the 2's complement of N called R, i.e.

$$\begin{array}{rr} & 7\ 7\ 7\ 7 \\ - & N_3N_2N_1N_0 \\ \hline & M_3M_2M_1M_0 \\ + & \qquad 1 \\ \hline & R_3R_2R_1R_0 \end{array}$$

3. Convert R to binary B



Circuit Locations K J I H G F E D C B A

4. Install diodes for all zero's in the binary number B

5. Example:

$$\text{Baud Rate} = 75 = \frac{4608000}{32 \cdot N}, \quad N = 1920$$

$$\begin{array}{r} 240 \\ 8\,\overline{)\,1920} \\ 11 \\ \hline 320 \\ 320 \\ 000 \end{array}$$

Remainder 0

$$\begin{array}{r} 30 \\ 8\,\overline{)\,240} \\ 240 \\ \hline \end{array}$$

Remainder 0

$$\begin{array}{r} 3 \\ 8\,\overline{)\,30} \\ 24 \\ \hline 6 \end{array}$$

Remainder 6

$$\begin{array}{r} 0 \\ 8\,\overline{)\,3} \\ 0 \\ \hline \end{array}$$

Rema

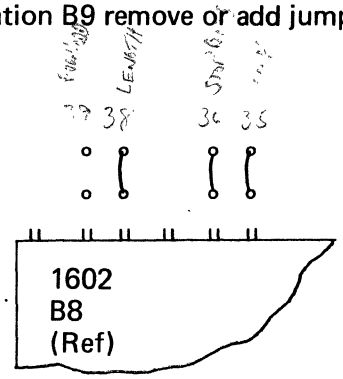
$$\text{N Octal} = 3600_8$$

		7777		
		3600		
M =		4177		
	+	1		
R =		4200		
B =	4 / 100	2 / 010	0 / 000	0 / 000
Diodes Needed	KJ	I – G	F E D	C B A

WORD STRUCTURE – OPTION 30, 31, 32, 33, 34

Instruction – At location B9 remove or add jumpers as indicated below:

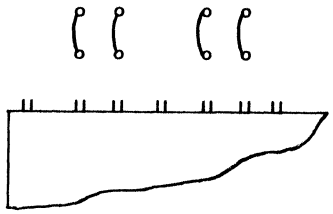
Parity Even
1 Stop
(10 Bit)



Standard Configuration
(Shown for Reference only)

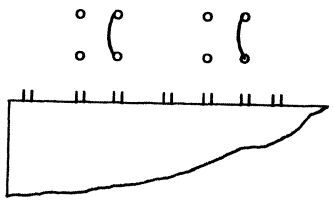
-30

Parity Odd
1 Stop
(10 Bit)



-31

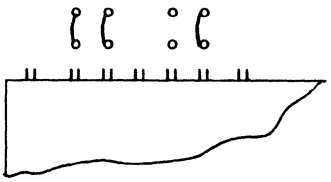
Parity Even
2 Stop
(11 Bit)



WORD STRUCTURE – OPTION 30, 31, 32, 33, 34 (Continued)

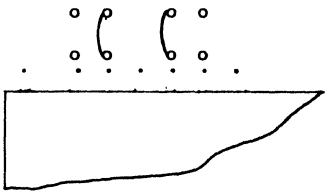
-32

Parity Odd
2 Stop
(11 Bit)



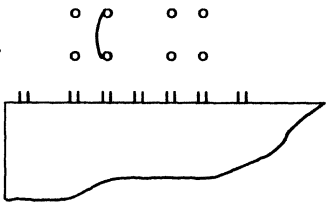
-33

No Parity
1 Stop
(9 Bit)



-34

No Parity
2 Stop
(10 Bit)



EDIT – OPTION 50

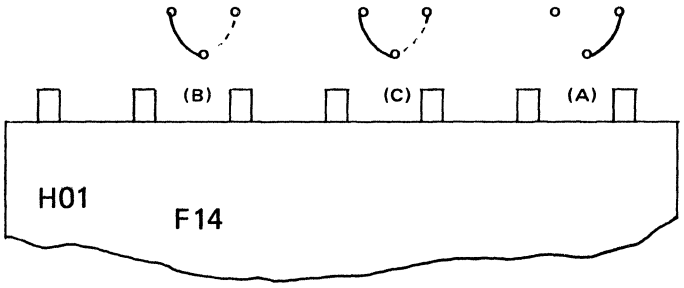
Parts List – 129314-010 ROM
CA-245-10SD Socket

Instructions – F/N 1 I.C. at Location K15
F/N 2 Socket at location K15

Replace the following key tops on keyboard:

Remove Q	Replace with	CI/Q
Remove W	Replace with	CD/W
Remove E	Replace with	LI/E
Remove R	Replace with	LD/R
Remove T	Replace with	LE/T
Remove Y	Replace with	PE/Y
Remove I	Replace with	BT/I
Remove S	Replace with	/S

At Location F14 jumper as follows:



PRINTER OUTPUT – OPTION 51

Parts List:

1.	CA-40S-10SD	Socket, 40 Pin C	Circuit Assy Corp.
2.	CA-24S-10SD	Socket, 24 Pin	Circuit Assy Corp.
3.	128534-3	Bracket, Conn.	
4.	17-305-01	Connector Body	Amphenol
5.	17-1207	Pin, Long, P.C.	Amphenol
6.	17-893	Jack Socket	Amphenol
7.	129314-020	ROM	
8.	128348-1602	I. C.	
9.	128578-10	I. C.	
10.	128348-103	I. C.	
11.	128348-02	I. C.	
12.	128348-161	I. C.	
13.	128348-1489	I. C.	
14.	128348-123	I. C.	
15.	128348-1488	I. C.	
16.	TE-1059.5	Capacitor, 100 uF, 3V	Sprague
17.	79PR20K	Pot., 20K	Helipot
18.	1N914	Diode	
19.	128533-512	Res, 5.1K	
20.	128533-102	Res, 1K	

Instructions — Install Connector at J3:

F/N 3 Bracket (Mount to Bd. with 1/8 Pop-Rivets or equivalent)
F/N 4 Connector Body
F/N 6 Pin, Long (Installed at 2, 3, 4, 5)
F/N 7 Jack Screw

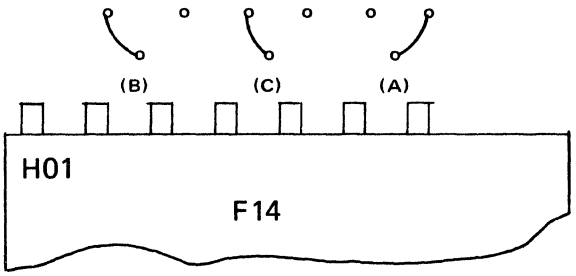
Install Sockets and I.C.'s:

F/N 1	Socket, 40 Pin	Locate at B10
F/N 2	Socket, 24 Pin	Locate at K15*
F/N 8	I. C. ROM	Locate at K15*
F/N 9	I. C. -1602	Locate at B10
F/N 10	I.C. -10	Locate at D10
F/N 11	I.C. -103	Locate at E8
F/N 12	I. C. -02	Locate at E9
F/N 13	I. C. -161	Locate at S6, S7, S8
F/N 14	I. C. -1489	Locate at A11
F/N 15	I. C. -123	Locate at A10
F/N 16	I. C. -1488	Locate at A9

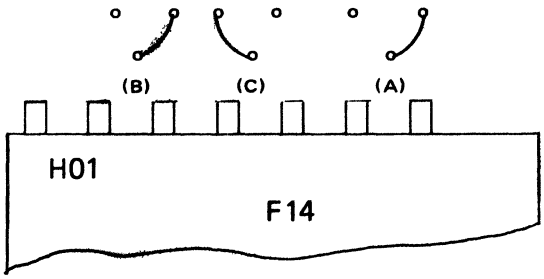
(*NOTE — If option No. 50 is also installed, locate ROM at K14).

At Location F14 jumper as follows:

(Jumper for -51 Option Only)



(Jumper for -50 and -51 Options)



At location T6 and T7, install 11 jumpers to select baud rate. (See following table).

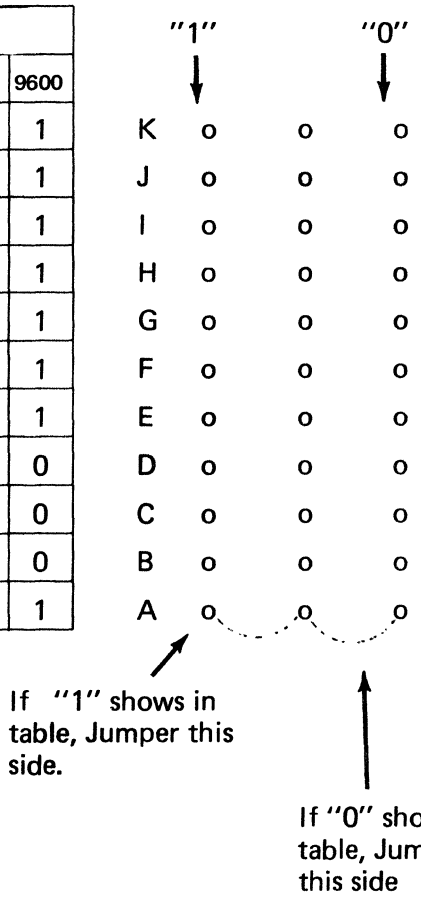
At location B10 jumper to select word structure. (See following table).

Install components at Location A10:

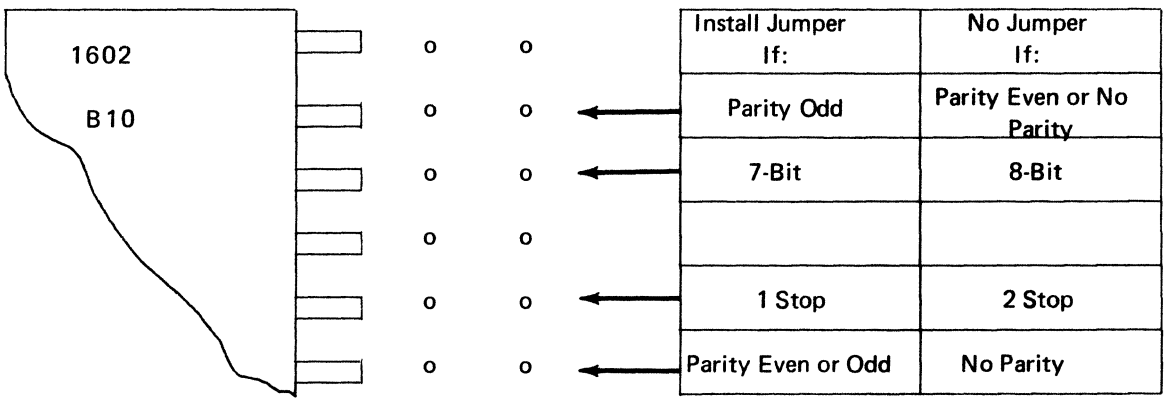
F/N 17	Capacitor	F/N 20	Resistor
F/N 18	Pot	F/N 21	Resistor
F/N 19	Diode		

Install Jumper at each location to either the "1" side or the "0" side as tabulated below for the baud rate required:

Location	BAUD RATE												
	110	150	300	600	1000	1200	1800	2000	2400	3600	4800	7200	9600
K	0	1	1	1	1	1	1	1	1	1	1	1	1
J	1	0	1	1	1	1	1	1	1	1	1	1	1
I	0	0	0	1	1	1	1	1	1	1	1	1	1
H	1	0	0	0	0	1	1	1	1	1	1	1	1
G	1	1	0	0	1	0	0	0	1	1	1	1	1
F	1	0	1	0	1	0	1	1	0	0	1	1	1
E	0	0	0	1	1	0	1	1	0	1	0	0	1
D	0	0	0	0	0	1	0	1	0	1	0	1	0
C	0	0	0	0	0	0	0	0	1	0	0	1	0
B	1	0	0	0	0	0	0	0	0	0	1	0	0
A	1	0	0	0	0	0	0	0	0	0	0	0	1



Install Jumpers as required at Location B10:



Install Jumper If:	No Jumper If:
Parity Odd	Parity Even or No Parity
7-Bit	8-Bit
1 Stop	2 Stop
Parity Even or Odd	No Parity

NUMERIC KEYBOARD – OPTION 60

Instructions – Plug F/N 1 60 Key Keyboard into ADM-1 Keyboard.

OUTPUT CABLE, RS 232 – OPTION 61

Parts List – 128557-91

Instructions – Install cable on Output Connectors

APPENDIX A
SECTION 2 – ADM-1 POLLING

POLLING/ADDRESSING DIALOG (PROTOCOL)

The control sends a four or five character sequence to initiate operations. This sequence consists of an EOT followed by two address characters, followed by a function character, and depending upon the function character, an ENQ.

For the ADM-1 the two address characters are the same character transmitted twice. The set of characters usable for ADM-1 addresses are from space thru DEL inclusive, providing 96 unique addresses.

Detection of a parity error in any of the header sequence will cause the header to be ignored.

The function codes are the lower case graphic characters p, q, r, s, t, and u.

p	=	POL
q	=	SELECT
r	=	SEQUENTIAL SELECT
s	=	FAST SELECT
t	=	BROADCAST SELECT
u	=	SEND

p – POL is a function code that must be followed by an ENQ.

When a terminal is properly addressed in a POL sequence (EOT A_1A_1p ENQ), it will respond in one of two ways.

1. No message waiting to be sent:
   The terminal sends an EOT.

2. Message waiting to be sent:
   The terminal sends the message (see "SENDING DATA").

q – SELECT (Must be followed by ENQ)

When a terminal is properly addressed in a SEL sequence (EOT A.A.2 q ENQ), it will respond in one of two ways.

1. Busy – Transmit a NAK.
2. Not Busy – Transmit an ACK.

The BUSY condition will exist if any one of the following conditions exist:

1. Waiting to be polled.
2. Operator is entering data.
3. The terminal is transmitting to the printer.

After transmitting the NAK, the terminal will disconnect.

In the NOT BUSY condition, the terminal transmits ACK then waits for the start of text transmission STX. (Any characters received prior to the STX will be ignored.)

Upon receipt of the STX, the LRC accumulator is cleared. As the text characters are received, the LRC check character is accumulated and the character written in the display memory or acted upon in accordance to the nature of the character.

When the ETX character is received, the operation is ended and the LRC character is expected to follow.

After the LRC character is received, the LRC accumulator and the parity error flag are tested for the occurrence of an error.

If no errors had been detected, the ADM-1 will send an ACK and disconnect in the idle state.

If a parity or LRC error was detected, the ADM-1 sends NAK, and remains connected waiting for retransmission of the message.

The message retransmission begins with the STX. If the computer wishes to terminate the operation offer receiving a NAK from the terminal an EOT in place of the STX text sequence will place the terminal in the idle state.

r – SEQUENTIAL SELECT

The SEQUENTIAL SELECT function provides a method of sequentially addressing a number of terminals with a single header so that they will all prepare (if not busy) to receive the same message.

Example 1:

E										S				E	L	
O	A_1	A_1	r	A_2	A_2	r	A_3	A_3	s	T	TEXT			T	R	
T										X				X	C	

In the example terminals with address character A_1 and A_2 will connect and wait for the STX if they were idle when their respective 'r' function was received. The terminal whose address is A_3 will connect unconditionally (see "s – FAST SELECT).

Following the ETX LRC terminals A_1 and A_2 will disconnect without responding. Terminal A_3 will send ACK or NAK depending upon whether a parity or LRC error had been detected and then it will disconnect.

Upon receiving an 'r' in the function position of an addressing sequence, the ADM-1 tests to see if its address code had been received in the address positions. If the address had not been for that terminal, the ADM-1 will look at the next two characters for its address. If the ADM determines that its address had preceded the SEQ function (r) it will test its busy status. If not busy, it will wait for an STX indicating the start of a message text block. If busy, it will disconnect without responding.

s – FAST SELECT

FAST SELECT provides a method of fast selection of a terminal. In this mode of selection the function 's' is immediately followed by the STX – Text ETX, LRC.

There is no response from the terminal until after the LRC character. This mode will also override the 'Busy' status. That is to say, the terminal will unconditionally connect and prepare for the STX.

t – BROADCAST SELECT

BROADCAST SELECT is similar to FAST SELECT in that a 'Busy' condition is overridden. In this case all terminals receiving the 't' in the proper position of a header will immediately connect and wait for STX.

At the end of the message following ETX – LRC, the terminal whose address preceded the function will respond with ACK/NAK and disconnect. All other terminals will disconnect.

u – SEND

EOT A_1 A_1 u

The SEND function (u) will cause the terminal whose address preceded the function code to perform the "SEND" operation.

The GS code will be written at the cursor position; then the cursor will move back to the position following the first previous GS code or to the Home position. At this point the ADM will wait for a poll operation.

The Sequence

EOT A_1 A_1 u, p, ENQ

will perform the above operation with the addition of an immediate poll.

SENDING DATA

When the SEND key is operated, a 'GS' code is written into t he cursor location, the cursor position is saved and then the cursor is moved backwards to the position following the first detected 'GS' or to the Home position if no 'GS' is located. The keyboard becomes locked at this time and remains so until the poll operation is completed.

NOTE: The operator can remove the terminal from the 'waiting for poll' state and recover control by depressing the CTRL, SHIFT and BREAK Keys.

Upon receiving a valid (error free) Poll sequence (EOT A_i A_i p ENQ), the terminal then sends ETX followed by the text, and ETX and the LRC character. The LRC character is the modulo 2 sum of the text characters and the ETX character.

The text is transmitted in one of two forms depending upon the state of the protect mode:

1. Protect mode off:

   All characters (except 'NUL') are transmitted. When the cursor moves from the end of one line to the beginning of the next line a 'US' code is inserted in the character string.

2. Protect mode on:

   All foreground (unprotected) characters are transmitted. As the protected fields are encountered, an 'FS' code is transmitted.

After the LRC character is sent, the terminal waits for acknowledgment from control. There are four actions that the terminal will take depending upon the response.

Response	Terminal Action
ACK	Send EOT and disconnect.
NAK	Retransmit the message and wait for response.
EOT	Position the cursor to the start of the message and go to the 'wait for poll' state. The next character may be an address character. (Terminal does not respond.)
None of the above or parity error	No response from terminal. Terminal repositions cursor to the beginning of the message and waits to be polled again.

MISCELLANEOUS

Reset

To reset the ADM-1 to an idle clear state, depress the following keys simultaneously in any order: CTRL, SHIFT, REPEAT, BREAK. This operation forces the control program to begin execution at location zero and clears all of the program control flags. The entire display screen is cleared to 'spaces', the protect mode is reset, and the cursor is positioned at the 'home' position.

Clear

The ADM-1 screen may be cleared in several ways:

Locally the operator can clear the foreground (unprotected) character spaces to 'space' codes by use of the CTRL and BREAK keys (or the CLEAR key on the 60 key keyboard).

By operator or computer control, the entire display may be cleared or only the foreground may be cleared to either 'spaces' or to NULS by the use of the following escape sequences:

ESC	;	clear FG to space
ESC	+	clear all to spaces (resets protect mode)
ESC	:	clear FG to NUL
ESC	*	clear all to NUL (resets protect mode)

Upon completion, the cursor will be in the first unprotected position on the screen.

Load Cursor

The computer can position the ADM-1 cursor to any position for a 4 character sequence.

ESC = Y X

where Y and X represent the row and column coordinates of the cursor position desired. The HOME position (top row, leftmost column) is addressed by 'space' codes, successive positions (down and to the right) use codes ascending in the ASCII character set.

'sp', !, " . . . etc.

After the 'X' coordinate is loaded, the position of the cursor is tested for protected status. If that position is protected, the cursor automatically skips forward to the first unprotected location.

Protect Control

Writing of protected characters is accomplished by sending or typing an ESC) sequence. This sequence sets the WRITE PROTECT mode.

The WRITE PROTECT mode is reset by an ESC (sequence.

The PROTECT MODE is set by an ESC & sequence and cleared by an ESC ' sequence.

When in PROTECT MODE, characters that have been written with the WRITE PROTECT set cannot be overwritten.

The PROTECT MODE is also cleared by the CLEAR operations.

ESC *

ESC +

The WRITE PROTECT mode is cleared:

By the clear operations:

ESC +

ESC *

ESC :

ESC ;

By initiation of a SEND operation,

After selection, before the STX is received.

At the end of a receiving text operation, either a normal (ETX) or an EOT termination.

When the EDIT and PRINT OPTIONS are provided, the WRITE PROTECT mode will terminate when any of the following operations are performed:

LINE INSERT

CHARACTER INSERT

LINE DELETE

CHARACTER DELETE

PAGE ERASE

PRINT

The cursor will not reside in a protected position. Following any cursor motion operation, the content of the position indicated by the cursor is tested for protected status. If that position is protected, the cursor moves forward (or backward) in the event of an original backward motion) until an unprotected location is reached.

CAUTION

If the entire display area is protected, the cursor will have no place to stop, causing the terminal to 'lock up' in a search for and unprotected position. This search may be 'broken' by the operator depressing the BREAK key.

EDIT OPERATION (OPTION)

Character Insert – ESC Q

a) Resets WRITE PROTECT mode.

b) Moves the character under the cursor and all following characters on that line (or field) one space to the right.

c) Writes a space at the original position of the cursor and leaves the cursor at that position.

Character Delete – ESC W

a) Resets WRITE PROTECT mode.

b) Deletes the character under the cursor by moving all following characters on that line or field one space to the left.

c) Writes a 'space' in the last position of the line or field.

d) Cursor does not move.

Line Insert – ESC W

a) Is not executed in PROTECT MODE is set.

b) Resets WRITE PROTECT mode.

c) Inserts a line of unprotected spaces at the line occupied by the cursor by moving the contents of that line and all lines below down one line.

d) Bottom line is lost.

e) At completion cursor is at first character position of inserted line.

Line Delete – ESC E

a) Is not executed if PROTECT MODE set.

b) Resets WRITE PROTECT mode.

c) Deletes line of data occupied by cursor.

d) Moves following lines up one line.

e) Bottom line becomes unprotected spaces.

f) Cursor is at first position of original line count.

Line Erase – ESC T

a) Replaces contents of unprotected positions with space beginning at cursor position and ending at last character of line or field.

b) If WRITE PROTECT mode is true, the spaces will be protected.

c) Cursor will remain at original position, except when WRITE PROTECT mode = true and PROTECT MODE = true, then the cursor will move to the first unprotectec position following.

Page Erase – ESC Y

a) Resets WRITE PROTECT mode.

b) Writes SPACE in all unprotected positions beginning with position of cursor to the end of the screen.

c) Cursor does not move.

Backtab – ESC I

Moves cursor to first position of current unprotected field. If at first position, move to first position of previous unprotected field. If backward motion passes through HOME, the cursor stops at last unprotected position on the screen.

PRINT OPERATION – ESC P

When received in text or entered from keyboard, the ESC P sequence will cause an EM code to be written at the cursor position. The cursor is then moved to the HOME position. If the command originated from the keyboard, the print operation will begin immediately; if from the computer, it will begin following the termination of the message procedure (i.e. following the ETX LRC and acknowledge response if required).

Printing takes place in the following manner:

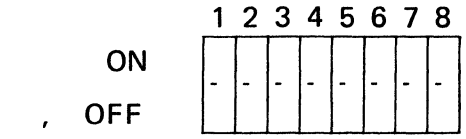
1. CR LF NUL
2. Each line of text followed by CR LF NUL

Trailing spaces will not be printed in order to reduce printing time.

The PRINT operation will terminate when the cursor reaches the EM code at which time a final CR LF NUL will be sent to the printer.

POLLING ADDRESS SELECTION

The AMP switch on the logic card at A12 sets the address character for the terminal. Character Space thru DEL is selected in ASCII where TRUE=OFF



Test Address is "?"

APPENDIX A

SECTION 3 – SERIAL PRINTER INTERFACE OPTION

INTRODUCTION

This interface option will allow ADM-1 Inquiry Display Terminals to control an RS232C compatible printer.

Operation of the printer may be initiated from the terminal keyboard or remotely from the computer. In addition, a vareity of baud rates may be selected to accommodate various types of printers.

OPERATING MODES

The Printer Interface will allow the printer to receive data in either the Page Mode or Free Form Entry Mode.

Page Mode

In the Page Mode characters are transmitted from the terminal to the printer in formatted form at a printer compatible baud rate. Printing can be initiated either from the terminal keyboard, or remotely, by computer command. Data is first entered on the screen from either the keyboard or computer. The cursor is placed at the location the print operation is to stop and ESC P is entered from either the keyboard or computer.

The ADM-1 then moves the cursor to the Home position and begins output to the printer. Transmission to the printer continues until the location when the ESC P was entered is reached and the print operation is terminated.

Free Form Entry Mode

In this mode formatting of the printed page on the printer is not automatically generated by the ADM-1. That is the Carriage Return and Line Feed must be imbedded in the text on the screen. This gives the operator the ability to format many (up to 640) lines of print on a single screen of the ADM-1.

Operation:

From the keyboard or computer the Free Form Entry mode is started with ESC U sequence. This allows the control codes normally associated with ADM-1 control to be

written into the buffer.

ESC L initiates the special print operation.

In this mode printing begins at the cursor position and continues to the end of the screen or to detecting a GS code on the screen which terminates the print operation.

Depressing the break key or transmission of ESC X from the computer will take the ADM-1 out of the Free Form Entry Mode.

INTERFACE CONNECTOR

The Interface Connector is a 25-pin connector utilizing the following pins for printer operation:

1	Chassis ground
3	Serial data to printer
7	Signal common
8	ADM READY (to PRINTER)
20	PRINTER READY (to ADM)

Signal levels at the connector must conform to RS232.

ON, SPACE, "0" > +3V

OFF, MARK, "1" < -3V

PROGRAMMING PRINTER OPERATION

There are two print modes of operation. These modes are envoked by escape sequences ESC P and ESC L.

1. ESC P: provides the basic page print operation.
   When ESC P is executed GS code ⍈ is written into the ADM-1 page buffer. This code is used to terminate the print operation.

   The ADM-1 moves the cursor to the Home position and prepares to output to the printer. The ADM raises the ADM-READY line (8) in preparation for sending to the printer. If the printer is "ready" to receive data it must provide a high signal on the printer ready line (10). The ADM-1 then outputs a CR, LF, NUL sequence to the printer to initialize the printer.

   Following the output of LF the ADM-1 drops the ADM Ready line and raises it again before proceeding to output the data.

Data is output to the printer in an asynchronous character bit serial format with a parity bit preceding the stop bit. The standard format provides a 10 unit code (single stop bit) with an even parity bit.

Characters are read from the ADM-1 display buffer beginning at the home position and output to the printer. As each character is accessed it is tested to see if it is a space or if it is the GS code. If it is space, the remaining characters on the line are tested for space. If there are no non-space characters remaining on that line, the ADM outputs a CR, LF, NUL to the printer and drops the "ADM ready" line for a short time.

When the end of a line is reached a CR, LF, NUL is output, and the ADM ready line drops.

When the GS code is detected signaling the end of the print operation, the ADM prints a CR LF NUL sequence, replaces the GS code with a space and returns to the Idle state.

If the print command was issued by the computer, the ADM will send a single CR character to the computer to indicate completion of the print operation.

While printing, the ADM is "blind" to all other activity.

Use of ADM-Ready and Printer Ready

If the attached printer provides a Ready/Busy status while printing, such as from a Centronics printer, the ADM Ready will have no effect on the operation, and the Printer Ready/Busy will effectively "interlock" the ADM/Printer interface to inhibit the ADM from transferring data to the printer while the printer is busy.

2. ESC L: provides a special print operation
In this mode format, control (CR, LF etc.) of the printer is not generated by ADM but must be imbedded in the text on the ADM screen. (See (3) below for method of writing control characters on screen.)

In this print mode printing begins at the cursor position and continues to the end of the screen or to sensing a GS code.

The ADM ready line is not pulsed – it is raised at the beginning and remains raised until the end of the print operation.

3. In order to write the control codes for a "Free Form Entry" print, the ADM-1 must be put into a mode where the control codes normally associated with ADM- control (CR, LF, FF, VT, BEL, ESC, BS, RS, US) will be written into the buffer. This is accomplished by executing an ESC U sequence.

   Having done this, all control codes normally acted upon by the ADM will be stored in the buffer. In order to remove the ADM from this mode, the computer should execute an ESC X sequence, or the operator depress the Break key.

APPENDIX B

RENEWAL PARTS INFORMATION

If it becomes necessary to order spare or renewal parts for your ADM-1 terminal from Lear Siegler/Electronic Instrumentation Division, include the following:

(1) Part Description
(2) Part Number
(3) ADM-1 Serial Number

Routine parts orders should be sent to:

Lear Siegler, Inc.
Electronic Instrumentation Division
Data Products Customer Service
714 North Brookhurst Street
Anaheim, California 92803

Emergency parts information and/or order placement can be made by telephoning:

Data Products Customer Service
Telephone: (714) 774-1010

ADM-1 ASSEMBLY PARTS LIST

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE	QTY	NOTE
1	ADM-1 Assembly	129300-1				
2	Keyboard	129301-1			1	
3	Monitor	129302			1	
4	Housing	129304			1	
5	Top Plate	129305-3			1	
6	Chassis Base	129305-5			1	
7	Keyboard Bracket	129305-7			2	
8	Blower Bracket	129305-9			1	
9	Printed Circuit Board Assembly	129310-1			1	
10	Power Supply – Reg. & Transformer	129312			1	
11	Wiring	129319-1			1	
12	Blower		3-15-2450	Howard	1	
13	Cable, Keyboard		5142-024	Spc-Str	1	
14	Capacitor		5HK-S10	Sprague	2	
15	Circuit Breaker		81504.5	Ltlefuse	1	
16	Terminal Block		912-2-KT79-KT74-KT-75	Kulka	1	
17	Pop Rivet		AD56ABS	USM	6	
18	Circuit Board Support		CBS-3N	Richco	6	
19	Sponge Rubber, Black Neoprene			Richco	4	
20	Pad			3M	6	
21	Speaker		S2-200	Calectro	1	
22	Strain Relief		SR-6P3-4	Heyco	1	
23	Switch, Rocker (Imprinted On-Off)		TA101-TWB	Carling	1	

LOGIC BOARD PARTS LIST

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE	QTY	NOTE
1	P11, N8	128348-00			2	
2	C13, F14	128348-01			2	
3	F9, F13, H7, H10, J9, J11, J12, K8, K10, K11, N7, L12, N12	128348-02			13	
4	K1, M9, N10	128348-04			3	
5	M5	128348-06			1	
6	E3, F2, F7B, H6, M6, M8, H2	128348-08			7	
7	K3	128348-20			1	
8	D13, F11, M10, P12, C14	128348-27			5	
9	D8, F3, H5, M3, F7A	128348-32			5	
10	A14, J13, K13, L13, P10	128348-42			5	
11	D14, J7, M12, N6	128348-74			4	
12	L3, L5, L6	128348-83			3	
13	E4, E5, E6, J4, J5, J6	128348-85			6	
14	N5	128348-86			1	
15	D11, E11, F10, K2,L10,N9,M7,P13,R12	128348-103			10	
16	E7	128348-106			1	
17	R1, R3, R5, R7	128348-107			4	
18	R13	128348-123			1	
19	B1,4,5,6,7,14, C1,4,5,6,7,11,14	128348-125			13	
20	A13, B13, E13	128348-151			3	
21	K4, K5, K6	128348-157			3	
22	H14,H15,J1,J2,J3,R8,R9,R10,S11,S12 S13	128348-161			11	
23	M4	128348-166			1	
24	M1, M2	128348-173			2	
25	A15, B15, C15, D4, D5, D6, E15, L1, L2, P1, P2	128348-175			11	
26	F4, 5, 6	128348-193			3	
27	A6	128348-1488			1	
28	A7	128348-1489			1	
29	B8	128348-1602			1	
30	P3	128348-2513			1	
31	N1, N2	128348-2532			2	
32	S1,2,3,4A,4B,5,6A,6B	128348-4008 (-21)			8	
33	T1, 2, 3, 4A, 4B, 5, 6A, 6B	128348-4008 (-31)			16	
34	S15	128348-4024			1	
35	T15	128348-7805			1	
36	A5	128348-7812			1	
37	T7	128348-7905			1	
38	A5	128348-7912			1	
39	Capacitor,.1uf, C41-48, 55, 56	128349-104			10	
40	Capacitor, 50uf, C5	128349-506			1	
41	Capacitor, .1uf, C2, 8-18, 32, 33, 49-52	128518-104			18	
42	Capacitor, 100uf, C30, C31	128518-108			2	
43	Capacitor, 2.2uf, C6	128518-225			1	
44	Capacitor, 270 pf, C3	128518-271			1	

LOGIC BOARD PARTS LIST (Continued)

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE	QTY	NOTE
45	Resistor, 1K (R1-4, 6, 8-14, 17, 18, 20, 22, 23, 25, 26, 31-34, 88-90, 36, 62	128533-102			28	
46	Resistor, 10K, R29	128533-103			1	
47	Resistor, 1.2K, R91	128533-122			1	
48	Resistor, 12K R54-61	128533-123			8	
49	Resistor, 150K R15	128533-151			1	
50	Resistor, 18K R27	128533-183			1	
51	Resistor, 220Ω, R46-53	128533-221			8	
52	Resistor, 270K, R16	128533-271			1	
53	Resistor, 390K, R24	128533-391			1	
54	Resistor, 39K, R30	128533-393			1	
55	Resistor, 470, R8-14	128533-471			7	
56	Resistor, 6.8K, R92	128533-682			1	
57	Bracket, Connector	128536-3			2	
58	D1, D15, F8, F15, H12, H4, H9, J8, K9 K12, L11	128578-00			13	
59	E1, 10, F12, H8, H13, J10, N11, R11	128578-04			8	
60	D9, H1, M11, B14A, P8	128578-10			5	
61	E14, H3, R9	128578-20			3	
62	K7, P5, P1A	128578-30			3	
63	L4	129303-01			1	
64	Baud Rate Module	129310-13			1	
65	Printed Circuit Board Assy, 12 Lines	129310-21				
66	Printed Circuit Board Assy, 24 lines	129310-31				
67	L15	129313-01			1	
68	Wafercon, 9 Pin J4		09-18-5094	Molex	1	
69	Wafercon, 6 Pin J5		09-18-5061	Molex	1	
70	Socket, Short		17-1208	Amph	3	
71	Socket, Long		17-1209	Amph	12	
72	Connector, Socket J1		17-304-01	Amph	1	
73	Jack Socket		17-893	Amph	1	
74	Capacitor, .33 uf		196D334X0035HA1	Sprague	2	
75	Crystal (with 1½" Wire Leads)		816D-4608.0Khz	S.C.	1	
76	Crystal (with 1½" Wire Leads)		816D-1096.0Khz	S.C.	1	
77	Pop Rivet		AD32BS	USM	2	
78	Pop Rivet		AD42ABS	USM	6	
79	Socket, 24 Pin Dip 6		CA24S-105D	C.A.	4	
80	Socket, 40 Pin Dip 6		CA40S-105D	C.A.	1	
81	Socket, 16 Pin Dip		CSA-2900-16B	SAE	1	
82	Diode		1N914		3	
83	Switch		MSS-2250R	Alco	1	
84	Switch		MSS-4350R	Alco	1	
85	Bridge		W005	G. I.	1	
86	Potentiometer, 100K, Linear Taper		YQ8383	CTS	1	
87	Potentiometer, 500K, Linear Taper		YQ8384-1	CTS	1	

INTEGRATED CIRCUIT IDENTIFICATION REF. P/N 128348

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE QTY	NOTE
-00	Quad 2 NAND		SN74H00N		1
-01	Quad 2 NAND (O.C.)		SN74H01N		1
-02	Quad 2 NOR		SN7402N		1
-04	Hex 1 NAND		SN74H04N		1
-05	Hex 1 NAND (O.C.)		SN74H05N		1
-06	Hex 1 NAND (O.C.) Buffer/Driver		SN7406N		1
-08	Quad 2 AND		SN7408N		1
-10	Triple 3 NAND		SN74H10N		1
-12	Triple 3 NAND (O.C.)		SN7412N		1
-17	Hex Buffer, H. V.		SN7417N		1
-20	Dual 4 NAND		SN74H20N		1
-22	Dual 4 NAND (O.C.)		SN74H22N		1
-25	Dual 4 NOR		SN7425N		1
-26	Quad 2 NAND (H. V.)		SN7426N		1
-27	Triple 3 NOR (Same as -875)		SN7427N		1
	(Same as -875)		N8875A	Signetics	
-30	Single 8 NAND		SN74H30N		1
-32	Quad 2 OR		SN7432N		1
-37	Quad 2 NAND Buffer		SN7437N		1
-38	Quad 2 NAND Buffer (O.C.)		SN7438N		1
-40	Dual 4 NAND Buffer		SN74H40N		1
-42	1 of 10 Decoder		SN7442N		1
-51	Dual 2 AND/OR		SN74H51N		1
-74	Dual D Flip-Flop		SN7474N		1
-75	Quad Bistable Latch		SN7475N		1
-83	4 Bit Binary Adder		SN7483N		1
-85	5 Bit Comparator		SN7485N		1
-86	Quad 2 Exclusive OR		SN7486N		1
-96	5 Bit Shift Register		SN7496N		1
-103	Dual J-K Flip-Flop		SN74H103N		1
-106	Dual J-K Flip-Flop		SN74H106N		1
-107	Dual Line Receiver		SN75107AN		T.I.
-108A	Line Receiver		SN75108AN		T.I.
-110	Line Driver		SN75110N		T.I.
-121	One-Shot		SN74121N		1
-123	Dual One-Shot		SN74123N		1
-125	Quad 1 Buffer 3-State		SN74125N		1
-150	Data Selector/Multiplexer (16 to 1 Line)		SN74150N		1
-151	Data Selector/Multiplexer (8 to 1 Line)		SN74151N		1
-153	Data Selector/Multiplexer (Quad 4 to 1 Line)		SN74153N		1
-154	4 to 16 Decoder		SN74154N		1
-157	Quad 2 Line to 1 Line Multiplexer		SN74157N		1
-161	4 Bit Binary Counter		SN74161N		1
-164	8 Bit Shift Register		SN74164N		1

NOTE 1: Part Numbers are Texas Instrument. Direct Replacement Parts may be ordered from National, Signetics or Motorola.

INTEGRATED CIRCUIT IDENTIFICATION (Continued) REF P/N 128348

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE	QTY	NOTE
-166	8 Bit Shift Register		SN74166N			1
-173	Quad D Flip-Flop, 3-State		SN74173N	T. I.		
			8T10	Signetics		
			DM8551	National		
-175	Quad D Flip-Flop		SN74175N	T.I.		
			N74175B	Signetics		
			DM74175	National		
-193	4 Bit Binary Counter		SN74193N			1
-199	8 Bit Shift Register		SN74199N			1
-328	Dual 8 Bit Shift Register		9328PC	Fairchild		
			N8277B	Signetics		
			U6M932859X	Advanced Micro		
			ITT9328-5D	ITT		
-416	Dual 4 NAND (Exp.)		N8416A	Signetics		
			SN15832N	T.I.		
			DM832N	National		
			M832P	Motorola		
			UCA993259	Fairchild		
-450A	Line Driver		SN75450AN	T.I.		
-533	T. V. Jungle		SN76533N	T.I.		
-723	Voltage Regulator		U6A7723393	Fairchild		
-741	Operational Amp		U6A7741393	Fairchild		
			SN72741N	T.I.		
-835	Hex Inv, (O. Base Input) DTL		SN15835N	T.I.		
-875	Triple 3 NOR		N8875A	Signetics		
	(Same as -27)		SN7427N	T.I.		
-1402	Quad 256 Bit Shift Reg.		1402	Intel		
			2502B	Signetics		
			MF1402A	Microsystem,Int		
-1488	Quad Line Driver		MC1488L	Motorola		
-1489	Quad Line Receiver		MC1489AL	Motorola		
-1602	Asynchronous Receiver/Transmitter		TR1602B	West. Digital		
-2257	Terminal Transmitter		MC2257L	Motorola		
-2259	Terminal Receiver		MC2259L	Motorola		
-2403	Read Only Memory		TMS2403	T.I.		
-2501	Read Only Memory		TMS2501	T.I.		
-2513	Character Generator		2513N/I CM2140	Signetics		
-2519	Hex 40 Bit Shift Reg.		2519B	Signetics		
-2532	Quad 80 Bit Shift Reg.		2532B	Signetics		
-2602	Static Random Access Memory		2602-1B	Signetics		
			S236	Intel		
-4024	Voltage Controlled Multivibrator(VCM)		MC4024P	Motorola		
-4044	Phase Detector		MC4044P	Motorola		
-7805	Positive Voltage Reg. (+5)		MC7805CP	Motorola		
			UGH7805393	Fairchild		
			LM340T-5	National		

NOTE 1: Part Numbers are Texas Instrument. Direct Replacement Parts may be ordered from National, Signetics or Motorola.

INTEGRATED CIRCUIT IDENTIFICATION (Continued) REF P/N 128348

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE	QTY	NOTE
-7812	Positive Voltage Reg. (+12)		MC7812CP	Motorola		
			LM340T-12	National		
-7905	Negative Voltage Reg. (—5)		MC7905CP	Motorola		
-7912	Negative Voltage Reg. (—12)		MC7912CP	Motorola		

MONITOR PARTS LIST

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
	Capacitor, Fixed: μF Unless Otherwise Stated			
C1	3300; 60V, Electrolytic	BBRC		1-012-2156
C101	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C102	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C103	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C104	0.001 ± 10%; 1000V, Ceramic Disc	ERIE	Type 801	1-012-0540
C105	0.47 ± 10%, 100V, Mylar	PAK	MF830	1-012-1005
C106	0.47 ± 10%; 100V, Mylar	PAK	MF830	1-012-1005
C107	500; 6V, Electrolytic	BBRC		1-012-2158
C108	100; 6V, Electrolytic	BBRC		1-012-2160
C109	0.022 ± 10%, 400V, Mylar	SPRA	Type 225P	1-012-0800
C110	.1 ± 10%; 200V, Mylar	PAK	MF580	1-012-0870
C111	0.02 ± 20%; 1000V, Ceramic Disc	ERIE	Type 841	1-012-0780
C112	50; 50V, Electrolytic	BBRC		1-012-2157
C113	10 ± 10%, 63V, Mylar	BBRC		1-012-1130
C114	200; 25V, Electrolytic	BBRC		1-012-2159
C115	50; 25V, Electrolytic	BBRC		1-012-2165
C116	20; 150V, Electrolytic	BBRC		1-012-1260
C117	6μf; 25V, Electrolytic	SPRA	TE1203	1-012-2066
C118	820pf ± 5%; 500V, Dipped Mica	ARCO	Type DM	1-012-0482
C119	25; 50V, Electrolytic	BBRC		1-012-2193
C120	.01 ± 20%; 1000 Ceramic Disc	ERIE	Type 811	1-012-0740
C201	50; 50V, Electrolytic	BBRC		1-012-2157
C202	0.01 ± 20%; 1000V, Ceramic Disc	ERIE	Type 841	1-012-0780
C203	50; 50V, Electrolytic	BBRC		1-012-2157
CR1	VS148, Bridge Rectifier	VARO	VS148	1-021-0413
CR2	H510, High Voltage Rectifier	VARO	H510	1-021-0424
CR101	1N3605	SYL	1N3605	1-021-0410
CR102	1N3605	SYL	1N3605	1-021-0410
CR103	1N4785	RCA	1N4785	1-021-0360
CR104	1N3279	DI	1N3279	1-021-0380
CR105	1N3279	DI	1N3279	1-021-0380
CR106	1N3279	DI	1N3279	1-021-0380
CR107	1N3279	DI	1N3279	1-021-0380
CR108	1N3605	SYL	1N3605	1-021-0410
F1	Fuse, 0.6A-250V, ¼ x 1¼, Slo-Blo	LF	Type AGC	1-028-0244
or	Fuse, 0.6A-250V, 9/32 x 1¼, Slo-Blo (TV-B12)	BUSS	Type MDM	1-028-0245
F101	Fuse, 2A-125V, Picofuse	LF	276002	1-028-0247
L1	Vertical Choke	BBRC		6-003-0321
L101	Coil, Width	BBRC		1-016-0303
	TRANSISTOR			
Q1	2N3055	RCA	2N3055	1-015-1134
Q101	2N5830	MOT	2N5830	1-015-1172
Q102	D13T1	GE	D13T1	1-015-1157

MONITOR PARTS LIST (Continued)

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
	Resistor, Film: ½W ± 5% Unless otherwise stated			
R133	4.7K; 1/4W			70-16-0472
R134	Not Used			
R135	22K			70-16-0223
R136	22K			70-16-0223
R137	33K; 1W Composition			1-011-2448
R201	1K			1-011-2270
R202	1K			1-011-2270
R203	10K			1-011-2294
R204	0.68Ω ± 10%; 2W, Wirewound	IRC	Type BHW	1-011-2217
R205	1.5K			1-011-2274
R206	470Ω			1-011-2262
R207	470Ω			1-011-2262
R208	Var; 500Ω ± 20%; 1/5W, Composition	CTS	Type 201	1-011-5604
R209	470Ω			1-011-2262
	TRANSFORMER			
T1	Power	BBRC		1-017-5390
T2	High Voltage (TV-12C, TV-A12, & TV-E12)	BBRC		6-003-0320
or	High Voltage (TV-B12, TV-TC12, & TV-C12)	BBRC		6-003-0325
or	High Voltage (TV-T12)	BBRC		6-003-0326
or	High Voltage (TV-D12)	BBRC		6-003-0333
T101	Horizontal Driver	BBRC		1-017-5338
VR101	1N758	T1	1N758	1-021-0180
VR102	VR56	ST	VR56	1-021-0420
	MISCELLANEOUS			
	Socket, CRT (TV12)	BBRC		1-022-0427
	Fuseholder, Extractor Post, Fuse Size: ¼ x 1¼	LF	342012	1-028-0210
	Fuseholder, Extrator Post, Fuse Size: 9/32 x 1¼ (TV-B12 Only)	BUSS	Type HCM	1-028-0246
	Low Voltage Circuit Board Assembly	BBRC		6-003-0459
	Main Chassis Circuit Board Assembly	BBRC		6-003-0500
	Main Chassis Circuit Board Assembly (TV-T12)	BBRC		6-002-0476
	Main Chassis Circuit Board Assembly (TV-TC12)	BBRC		6-002-0502
	Main Chassis Circuit Board Assembly (TV-C12)	BBRC		6-002-0504
	Main Chassis Circuit Board Assembly (TV12, Tektronics)	BBRC		6-002-0506
	Cable Assembly; 8 Inch	BBRC		6-004-0630
	Cable Assembly; 5 Inch	BBRC		6-004-0631
	Power Supply Module (TV-12, 120VAC)	BBRC		6-003-0371
	Power Supply Module (TV-12, 220VAC)	BBRC		6-003-0372
	Power Supply Module (TV-B12, 120VAC)	BBRC		6-003-0368
	Power Supply Module (TV-B12, 220VAC)	BBRC		6-002-0370
	Deflection Coil Assembly	BBRC		6-004-0314
	Deflection Coil Assembly (TV-B12)	BBRC		6-004-0321
V1	CRT, 12 Inch, P4 Phosphor	BBRC		1-014-0737
or	CRT, 12 Inch, P39 Phosphor	BBRC		1-014-0738
	Power Cable Assembly, 120VAC	BBRC		6-003-0645
	Power Cable Assembly, 220VAC	BBRC		6-003-0652

MONITOR VENDOR CODES AND LOCATIONS

Code	Manufacturer	Location
BBRC	Ball Brothers Research Corporation Miratel Division	Roseville, Minnesota
BUSS	Bussman Manufacturing	St. Louis, Missouri
CRL	Centralab	Milwaukee, Wisconsin
CTS	CTS Corporation	Elkhart, Indiana
DI	Diode, Inc.	Chatsworth, California
ERIE	Erie Technological Products, Inc.	Erie, Pennsylvania
GE	General Electric	Syracuse, New York
IRC	IRC Corporation	Philadelphia, Pennsylvania
LF	Littelfuse Company, Inc.	Des Plaines, Illinois
MALL	P. R. Mallory Company, Inc.	Indianapolis, Indiana
MOT	Motorola Semiconductor Products	Phoenix, Arizona
NPC	Neucleonics Products	Los Angeles, California
PAK	Paktron	Alexandria, Virginia
RCA	RCA Semiconductor Division	Harrison, New Jersey
SPRA	Sprague Electric Co.	North Adams, Massachusetts
ST	Sarkes Tarzian, Inc.	Bloomington, Indiana
SYL	Sylvania Electric Products	Seneca Falls, New York
TI	Texas Instrument	Dallas, Texas
VARO	Varo Corporation	Garland, Texas

APPENDIX C

INTEGRATED CIRCUIT IDENTIFICATION REF P/N 128578

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG CODE	QTY	NOTE
-00	Quad 2 NAND		SN7400N	T.I.		
			SN74H00N	T.I.		
-03	Quad 2 NAND (O.C.)		SN7403N	T.I.		
			SN74H01N	T.I.		
-04	Hex 1 NAND		SN7404N	T.I.		
			SN74H04N	T.I.		
-05	Hex 1 NAND O. C.		SN7405N	T.I.		
			SN74H05N	T.I.		
-10	Triple 3 NAND		SN7410N	T.I.		
			SN74H10N	T.I.		
-20	Dual 4 NAND		SN7420N	T.I.		
			SN74H20N	T.I.		
-30	Single 8 NAND		SN7430N	T.I.		
			SN74H30N	T.I.		
-40	Dual 4 NAND Buffer		SN7440N	T.I.		
			SN74H40N	T.I.		
-50	Dual 2 AND/OR		SN7451N	T.I.		

REVISIONS					
SHT	ZONE	LTR	DESCRIPTION	DATE	APPROVED

129311

DASH NO.	NEXT ASSY	USED ON
	129310	ADM-1
APPLICATION		

UNLESS OTHERWISE SPECIFIED
DIM. IN INCHES
TOLERANCES
.X ± .1
.XX ± .03
.XXX ± .010
ANGLES ± 0.5°
MACH. FIN.

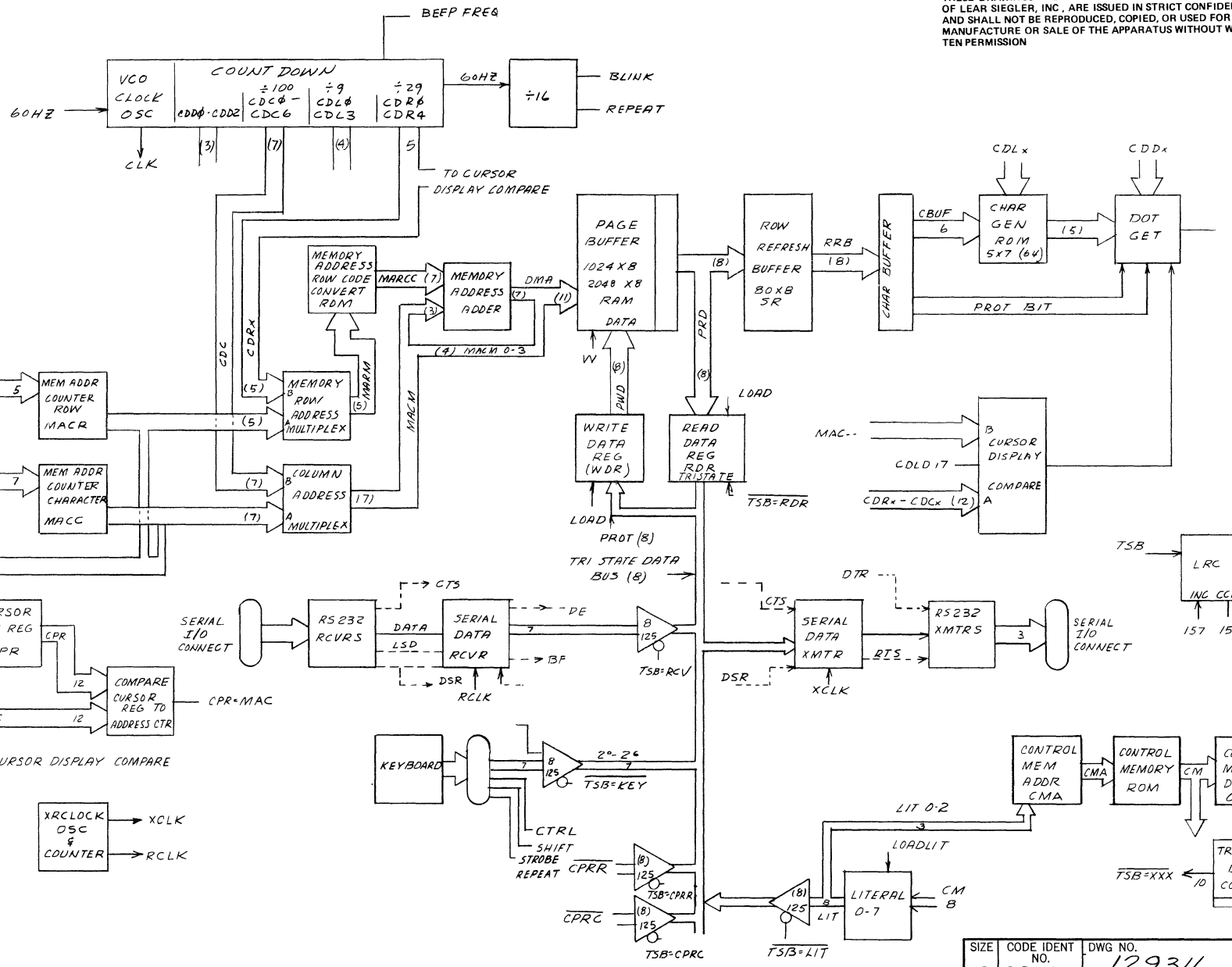
CONTR NO.
DR Mamer & Kelly
CHK
DSGN
ENGR
PROJ
REL
APPD
APPD

LEAR SIEGLER, INC.
ELECTRONIC INSTRUMENTATION DIVISION
ANAHEIM, CALIFORNIA 92803

LOGIC DIAGRAM

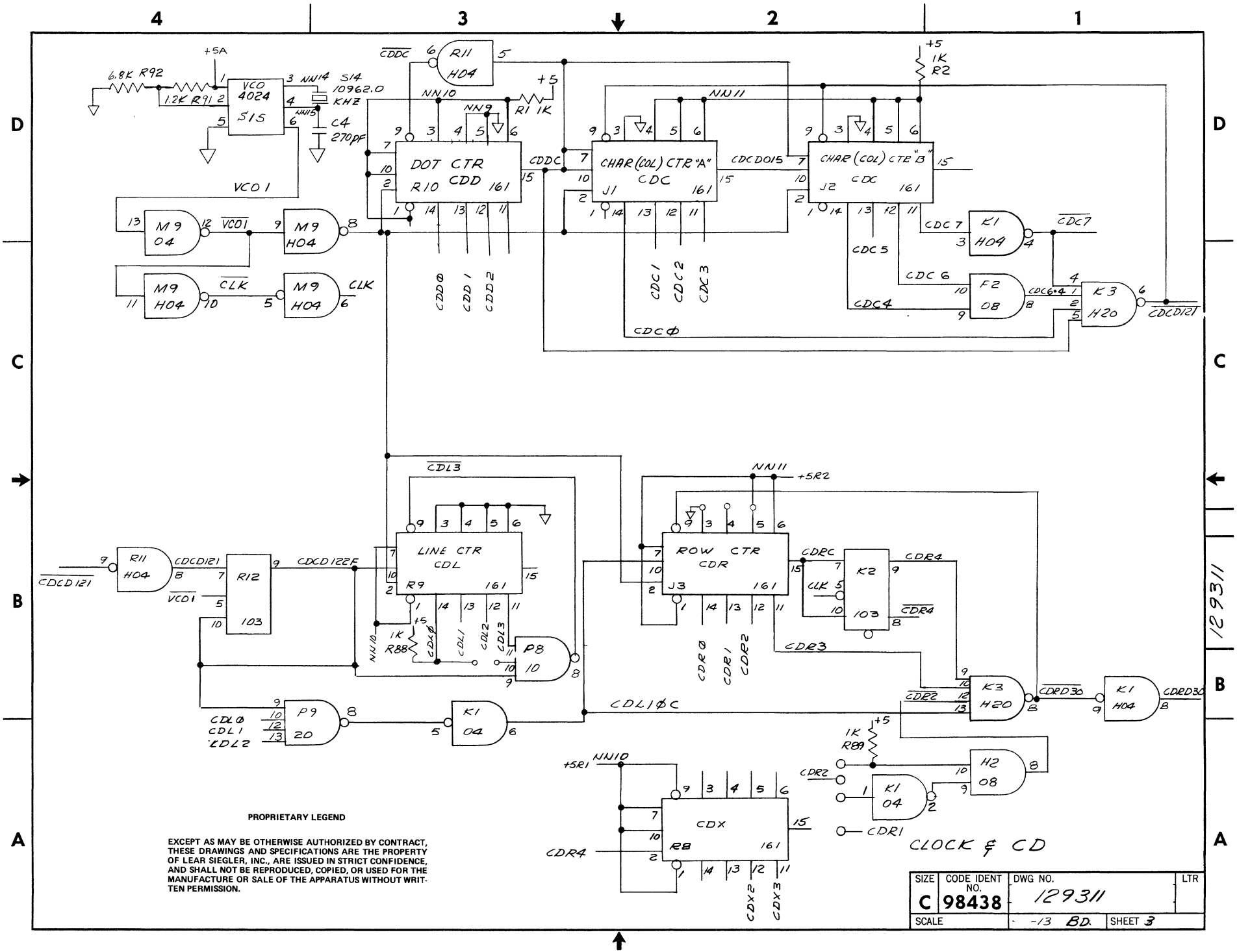
ADM-1

SIZE	CODE IDENT NO	DWG NO	LTR
C	98438	129311	
SCALE		-13 BD	SHEET 1 OF 26



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE		-13 BD	SHEET 2

129311



PROPRIETARY LEGEND

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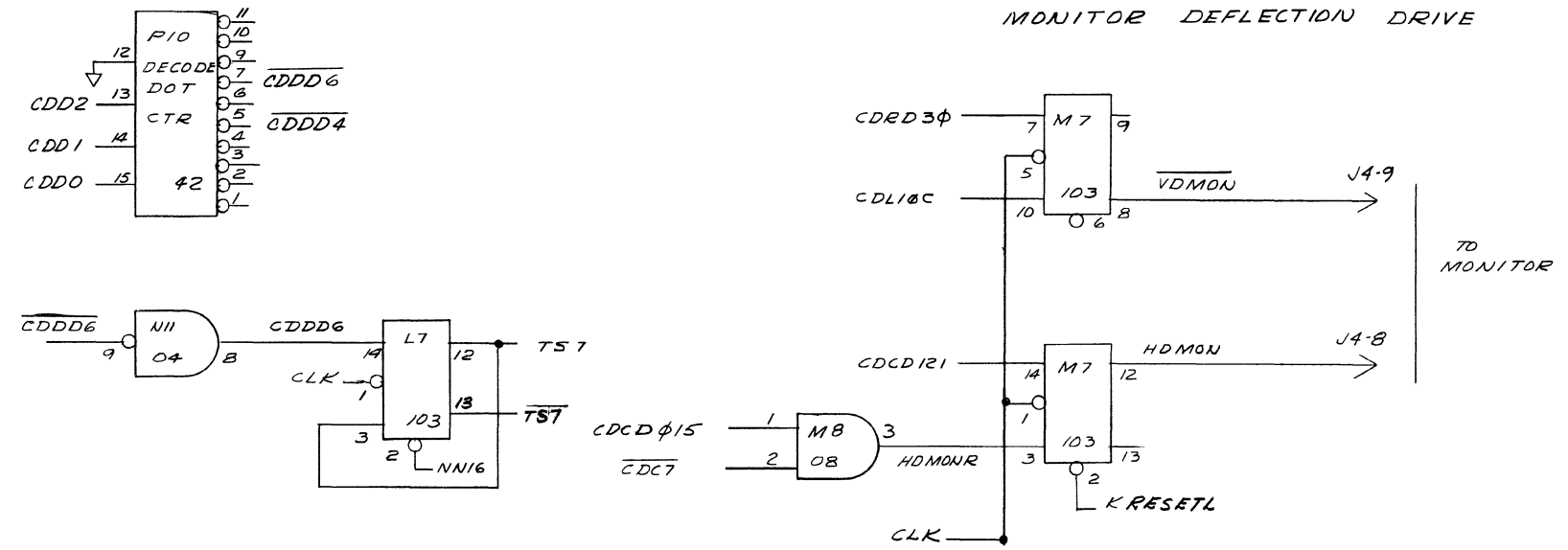
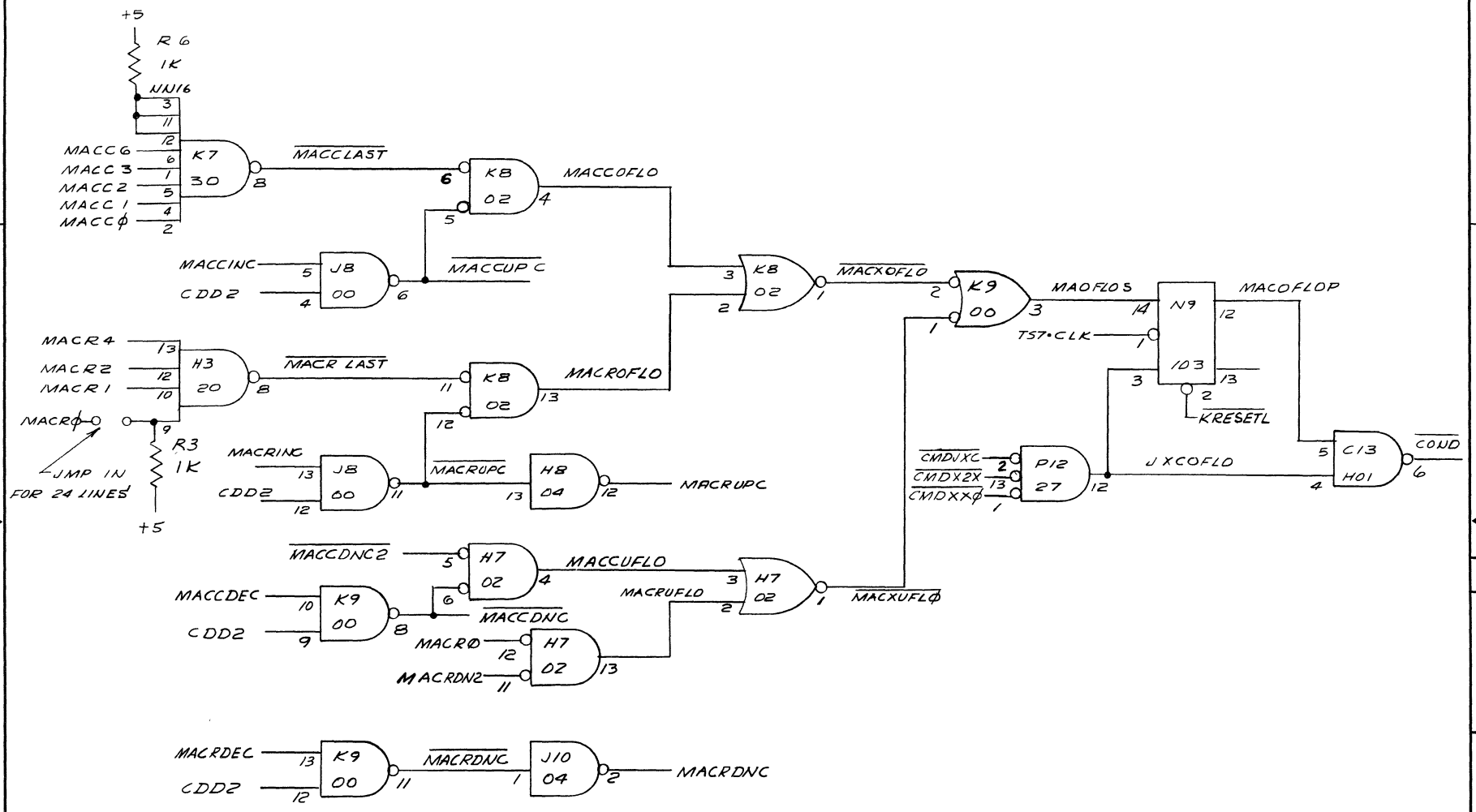
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE		-13 BD.	SHEET 3



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE		-/3 BD	SHEET 4

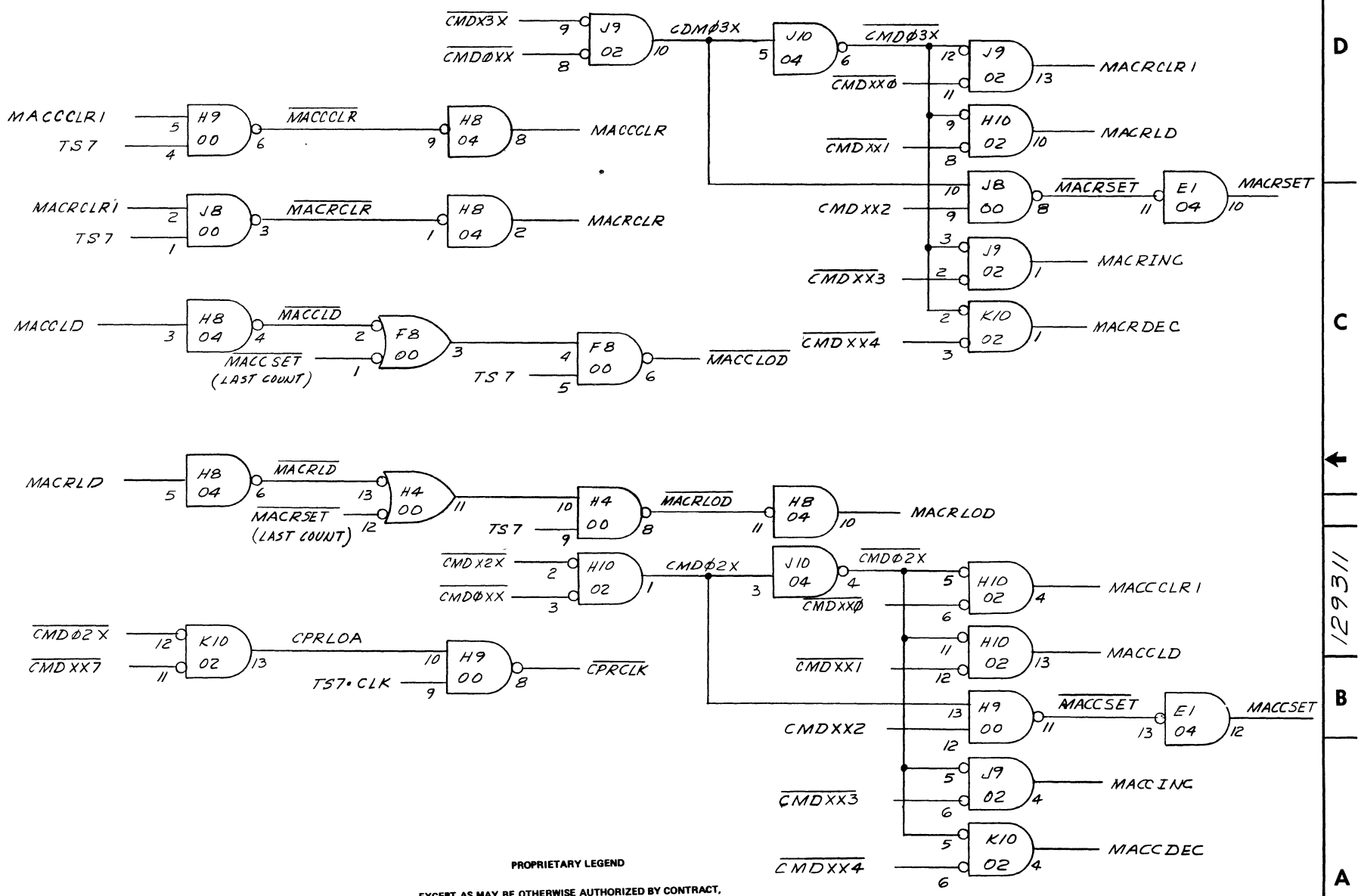
129311



MAC CONTROL

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE	-/3 BD	SHEET 5	

129311


4
3
2
1
D
C
B
A
CMDX3X
CMDØXX
J9 02
CDMØ3X
J10 04
CMDØ3X
CMDXXØ
MACRCLR1
MACRLD
CMDXX1
MACRSET
E1 04
CMDXX2
MACRINC
CMDXX3
MACRDEC
CMDXX4
MACCCLR1
TS7
H9 00
MACCCLR
H8 04
MACRCLR1
J8 00
MACRCLR
MACCLD
MACCLR
MACC SET
(LAST COUNT)
F8 00
MACCLOD
MACRLD
MACRSET
(LAST COUNT)
H4 00
MACRLOD
CMDX2X
CMDØXX
H10 02
CMDØ2X
CMDØ2X
CMDXX7
K10 02
CPRLOA
TS7·CLK
CPRCLK
J10 04
CMDXXØ
MACCCLR1
MACCLD
MACCSET
MACCINC
MACCDEC
129311
PROPRIETARY LEGEND
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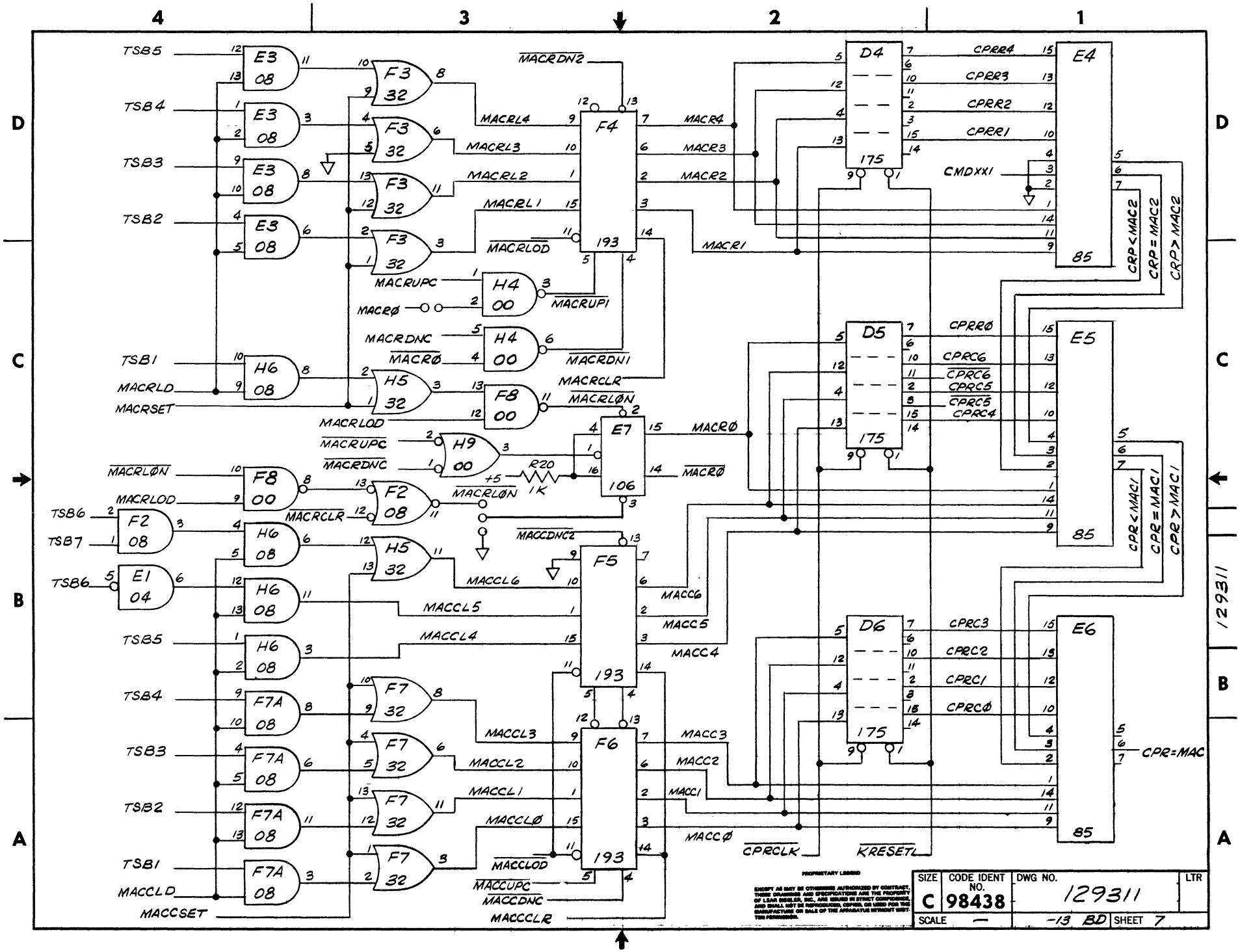
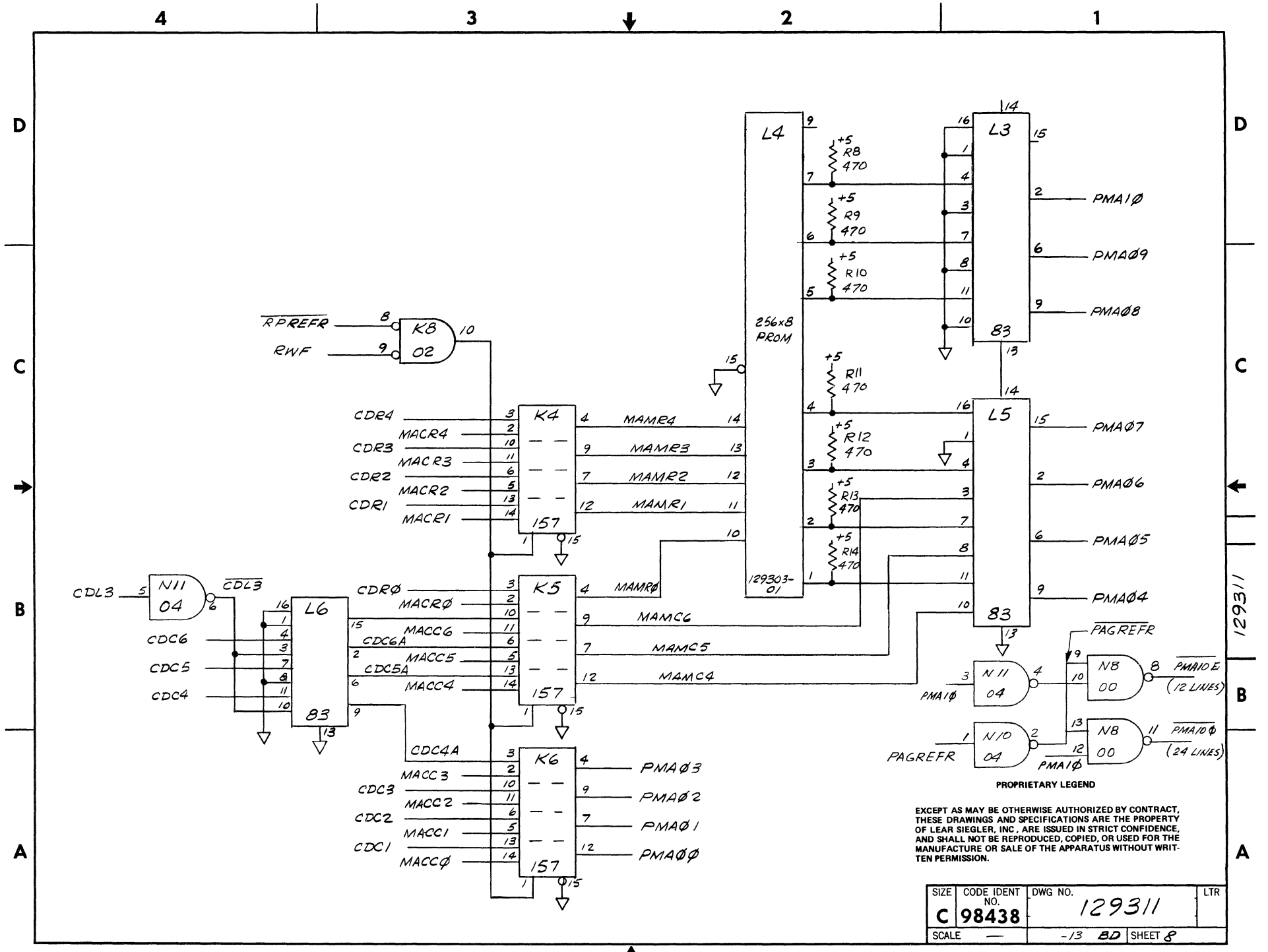
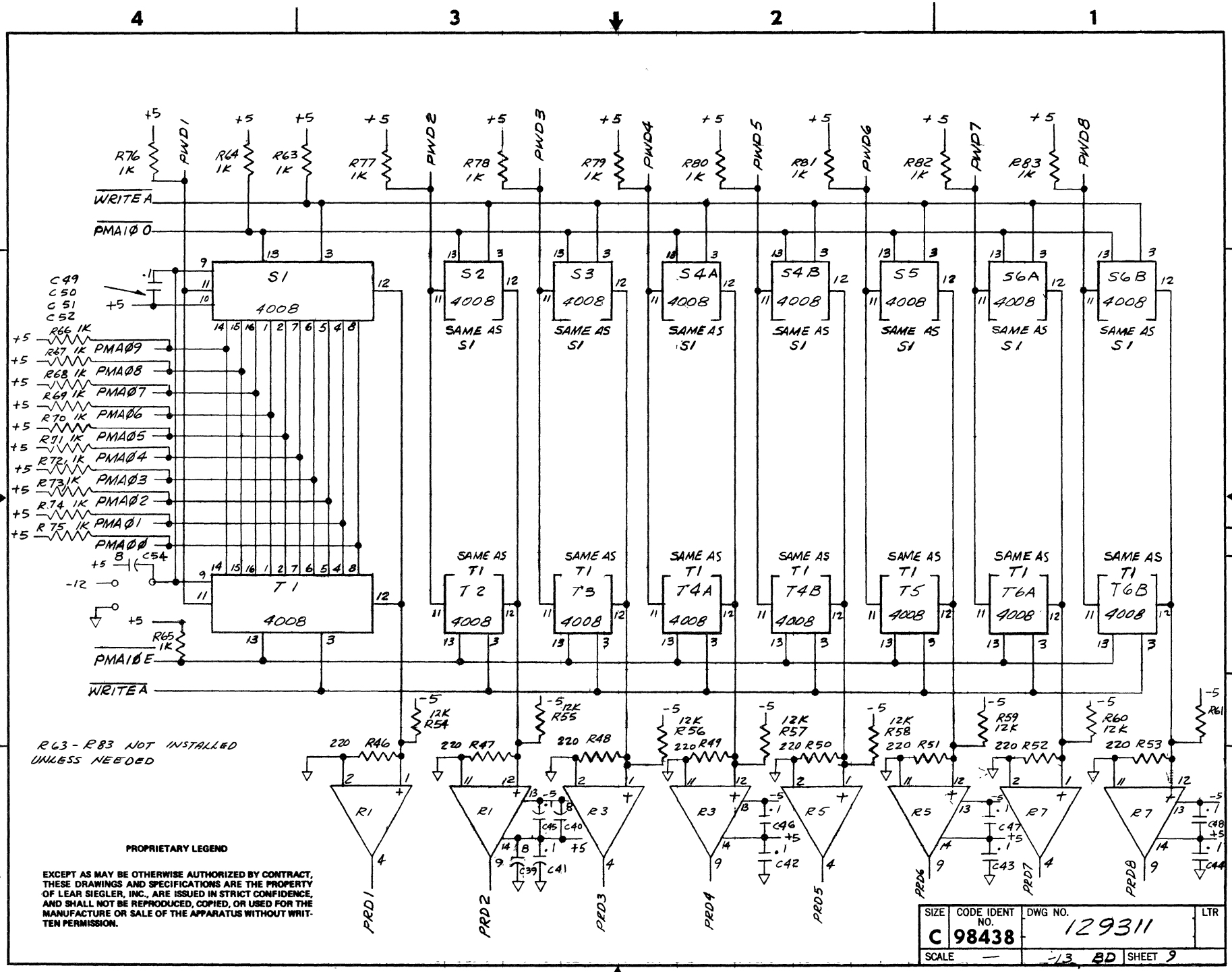
MAC CONTROL
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE
-13 BD
SHEET 6


4
3
2
1
D
C
B
A
TSB5
TSB4
TSB3
TSB2
TSB1
MACRLD
MACRSET
MACRLOD
MACRLØN
MACRCLR
MACRUPC
MACRDNC
MACRØ
MACRDN2
MACRL4
MACRL3
MACRL2
MACRL1
MACRLOD
MACRUPC
MACRØ
MACRUPI
MACRDNC
MACRØ
MACRDNI
MACRCLR
MACRLØN
MACRUPC
MACRDNC
MACRLØN
R20
1K
+5
MACRØ
MACRØ
MACCDNC2
MACCL6
MACCL5
MACCL4
MACCL3
MACCL2
MACCL1
MACCLØ
MACCLOD
MACCUPC
MACCDNC
MACCCLR
MACCSET
MACCLD
TSB6
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
MACR4
MACR3
MACR2
MACR1
MACC6
MACC5
MACC4
MACC3
MACC2
MACC1
MACCØ
CPRCLK
KRESETL
CPRR4
CPRR3
CPRR2
CPRR1
CMDXX1
CPRRØ
CPRC6
CPRC6
CPRC5
CPRC5
CPRC4
CPRC3
CPRC2
CPRC1
CPRCØ
CRP<MAC2
CRP=MAC2
CRP>MAC2
CPR<MAC1
CPR=MAC1
CPR>MAC1
CPR=MAC
E3 08
F3 32
F4
193
H4 00
H6 08
H5 32
F8 00
H9 00
E7
106
F2 08
E1 04
F5
F7A 08
F7 32
F6
D4
175
D5
D6
E4
85
E5
E6
PROPRIETARY LEGEND
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE —
-13 BD
SHEET 7
129311


4
3
2
1
D
C
B
A
RPREFR
RWF
K8
02
L4
256x8
PROM
129303-
01
+5
R8
470
R9
470
R10
470
R11
470
R12
470
R13
470
R14
470
L3
83
L5
83
L6
83
PMAIØ
PMAØ9
PMAØ8
PMAØ7
PMAØ6
PMAØ5
PMAØ4
CDR4
MACR4
CDR3
MACR3
CDR2
MACR2
CDR1
MACR1
K4
157
MAMR4
MAMR3
MAMR2
MAMR1
MAMRØ
CDL3
N11
04
CDRØ
MACRØ
CDC6
MACC6
CDC6A
CDC5
MACC5
CDC5A
CDC4
MACC4
K5
157
MAMC6
MAMC5
MAMC4
CDC4A
MACC3
CDC3
MACC2
CDC2
MACC1
CDC1
MACCØ
K6
157
PMAØ3
PMAØ2
PMAØ1
PMAØØ
PAGREFR
N11
04
N8
00
PMAIØE
(12 LINES)
PMAIØ
N10
04
N8
00
PMAIØØ
(24 LINES)
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE —
-13 BD
SHEET 8
129311


4
3
2
1
D
C
B
A
WRITE A
PMAIØ 0
PMAIØE
S1
S2
S3
S4A
S4B
S5
S6A
S6B
T1
T2
T3
T4A
T4B
T5
T6A
T6B
4008
SAME AS S1
SAME AS T1
C49
C50
C51
C52
C54
R63 - R83 NOT INSTALLED UNLESS NEEDED
PROPRIETARY LEGEND
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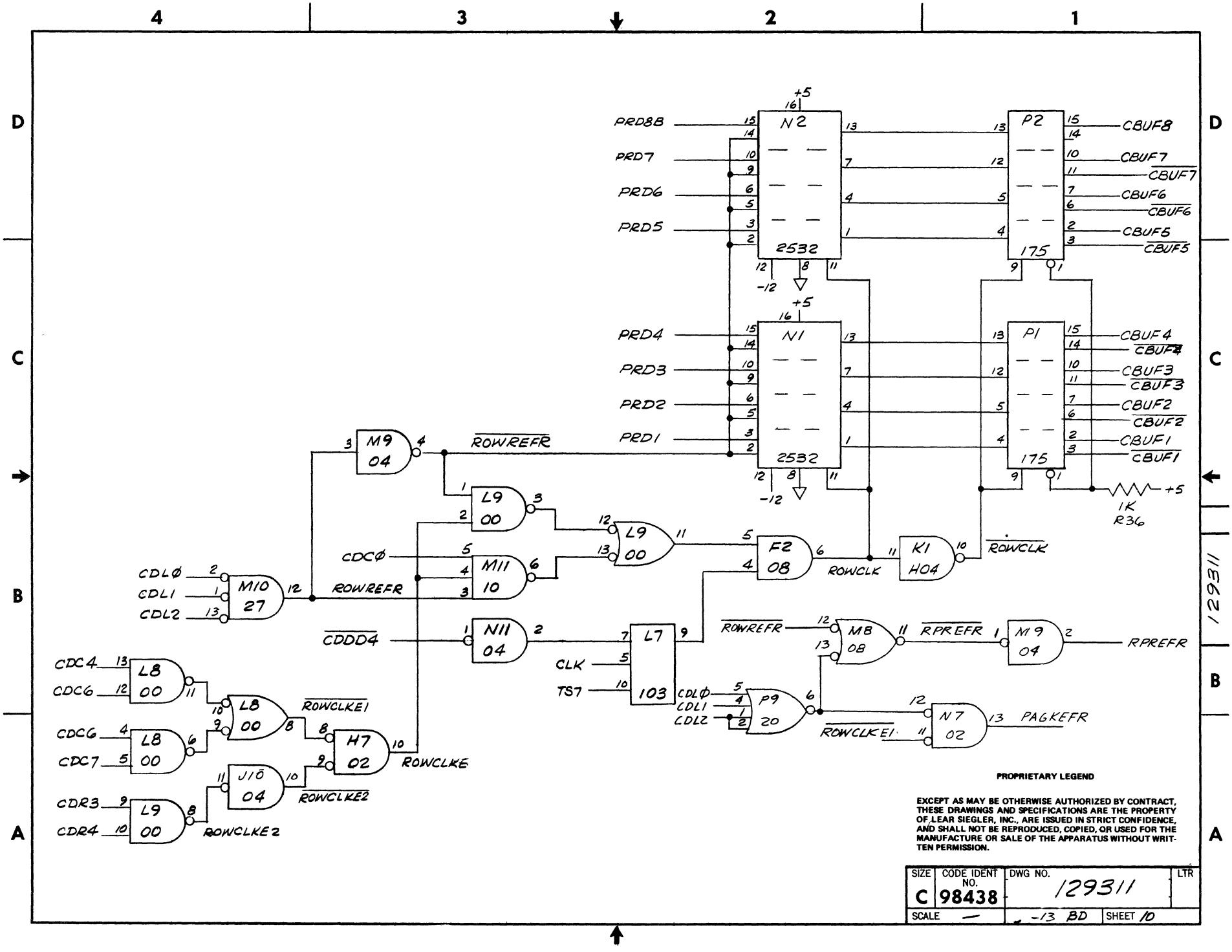
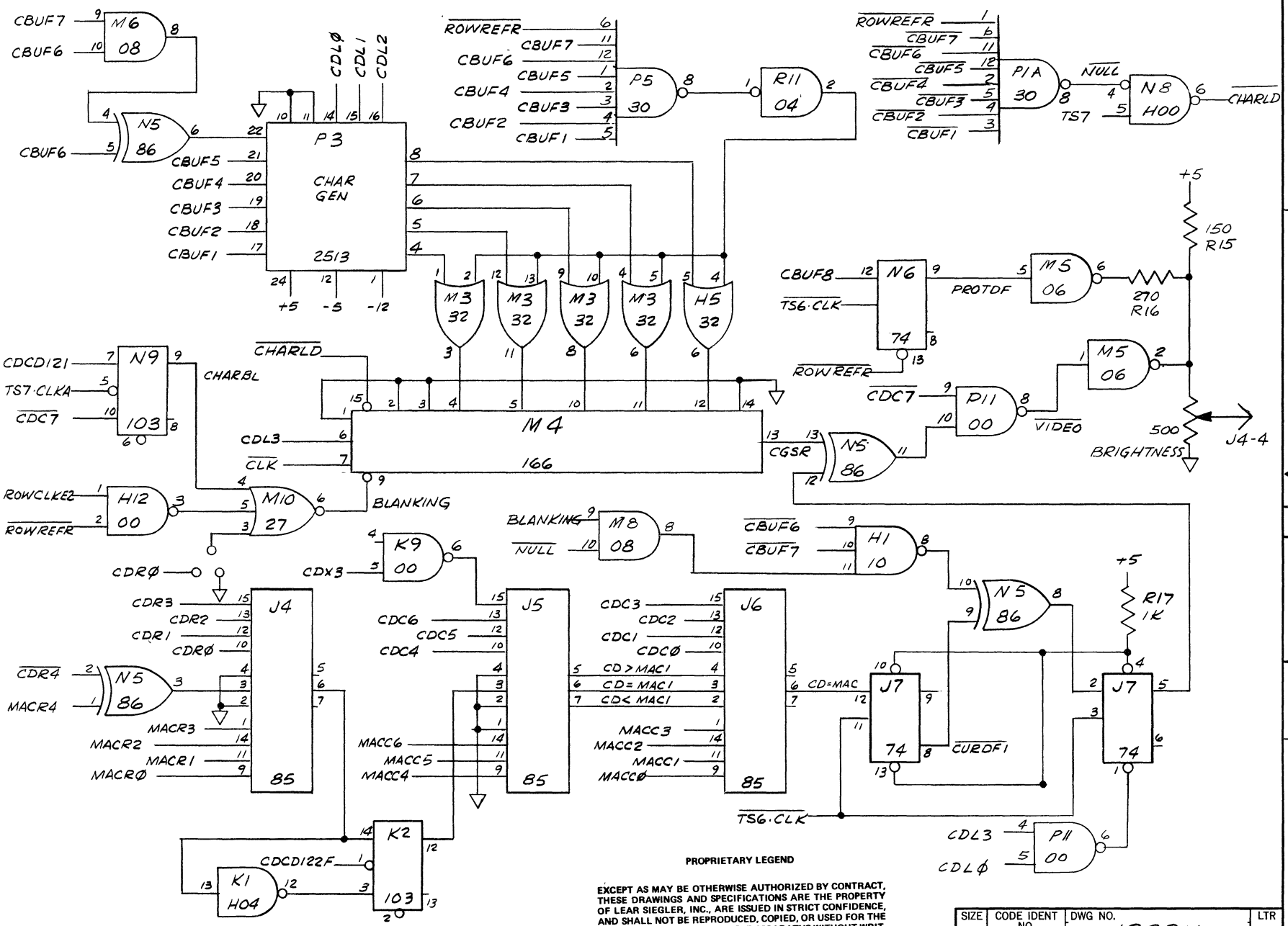
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE —
SHEET 9
129311



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 10

129311



PROPRIETARY LEGEND

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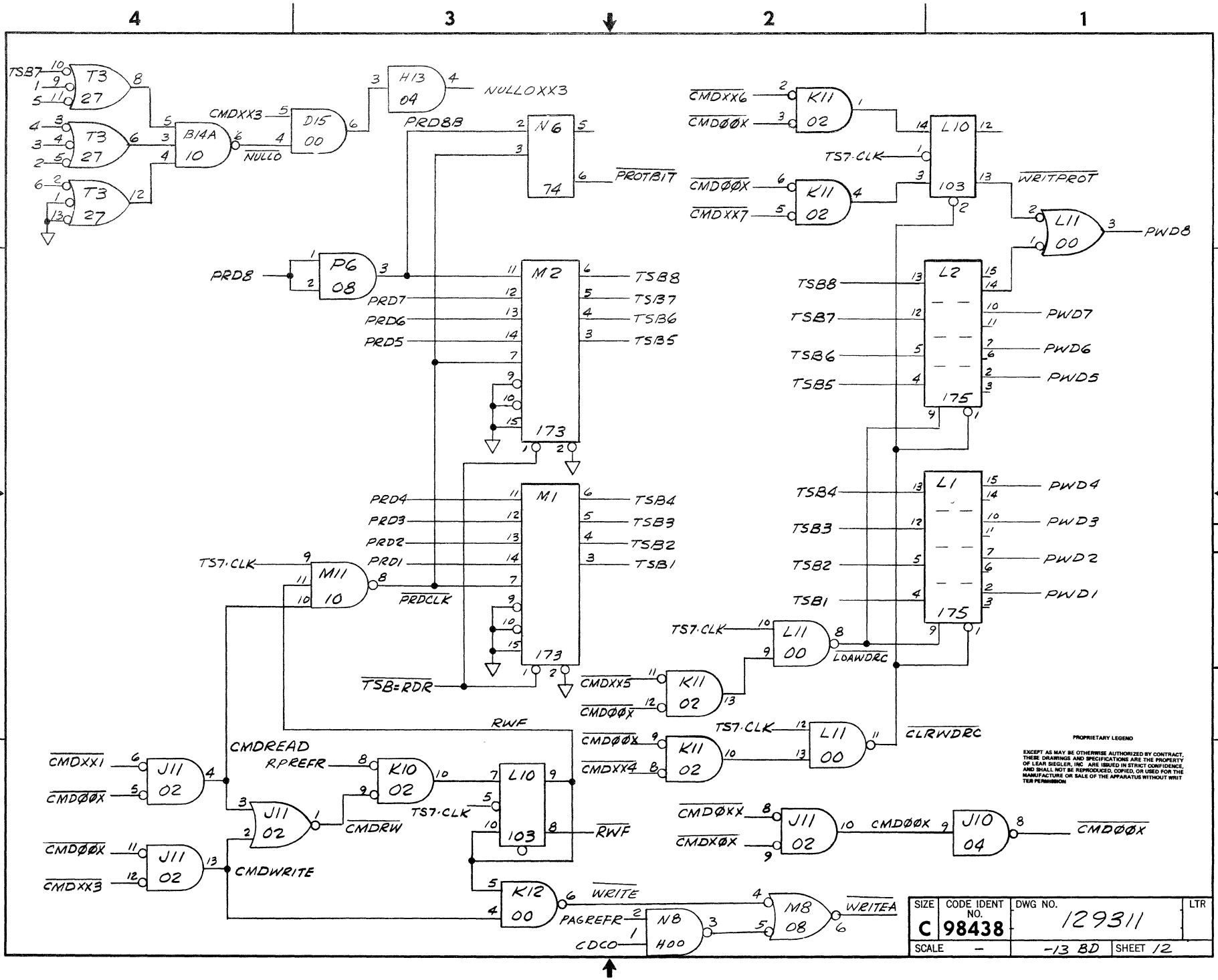
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 11


4
3
2
1
D
C
B
A
TSB7
T3 27
B14A 10
CMDXX3
D15 00
H13 04
NULLOXX3
NULLO
PRD8B
N6 74
PROTBIT
PRD8
P6 08
M2 173
TSB8
TSB7
TSB6
TSB5
PRD7
PRD6
PRD5
M1 173
TSB4
TSB3
TSB2
TSB1
PRD4
PRD3
PRD2
PRD1
TS7·CLK
M11 10
PRDCLK
TSB=RDR
CMDXX6
CMDØØX
K11 02
CMDXX7
L10 103
WRITPROT
L11 00
PWD8
L2 175
PWD7
PWD6
PWD5
L1 175
PWD4
PWD3
PWD2
PWD1
LOAWDRC
CMDXX5
CLRWDRC
CMDØØX
CMDXX4
RWF
CMDREAD
CMDXX1
J11 02
RPREFR
K10 02
CMDRW
CMDØØX
CMDXX3
CMDWRITE
K12 00
WRITE
PAGREFR
N8 H00
CDCO
M8 08
WRITEA
CMDØØX
CMDXØX
J10 04
PROPRIETARY LEGEND
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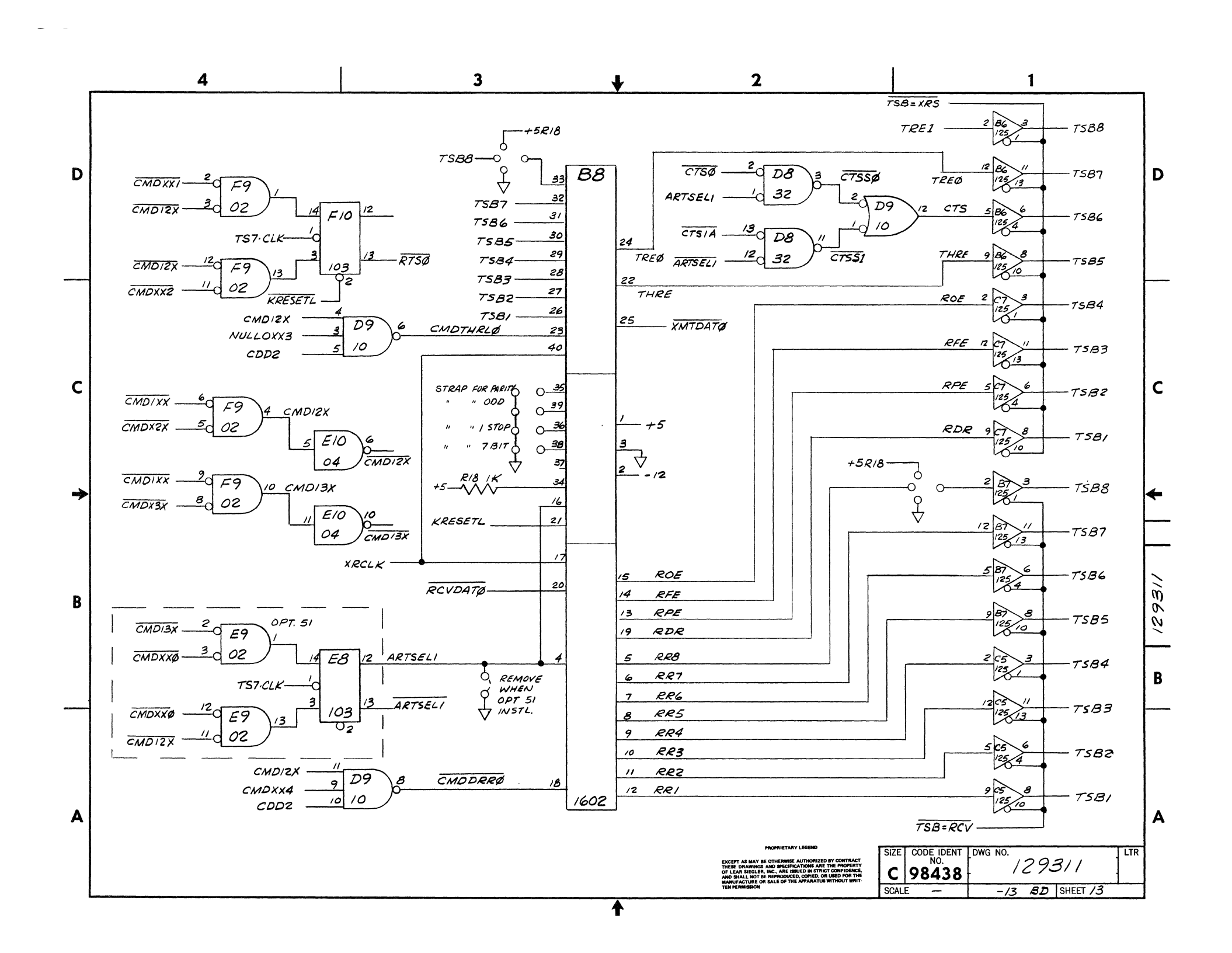
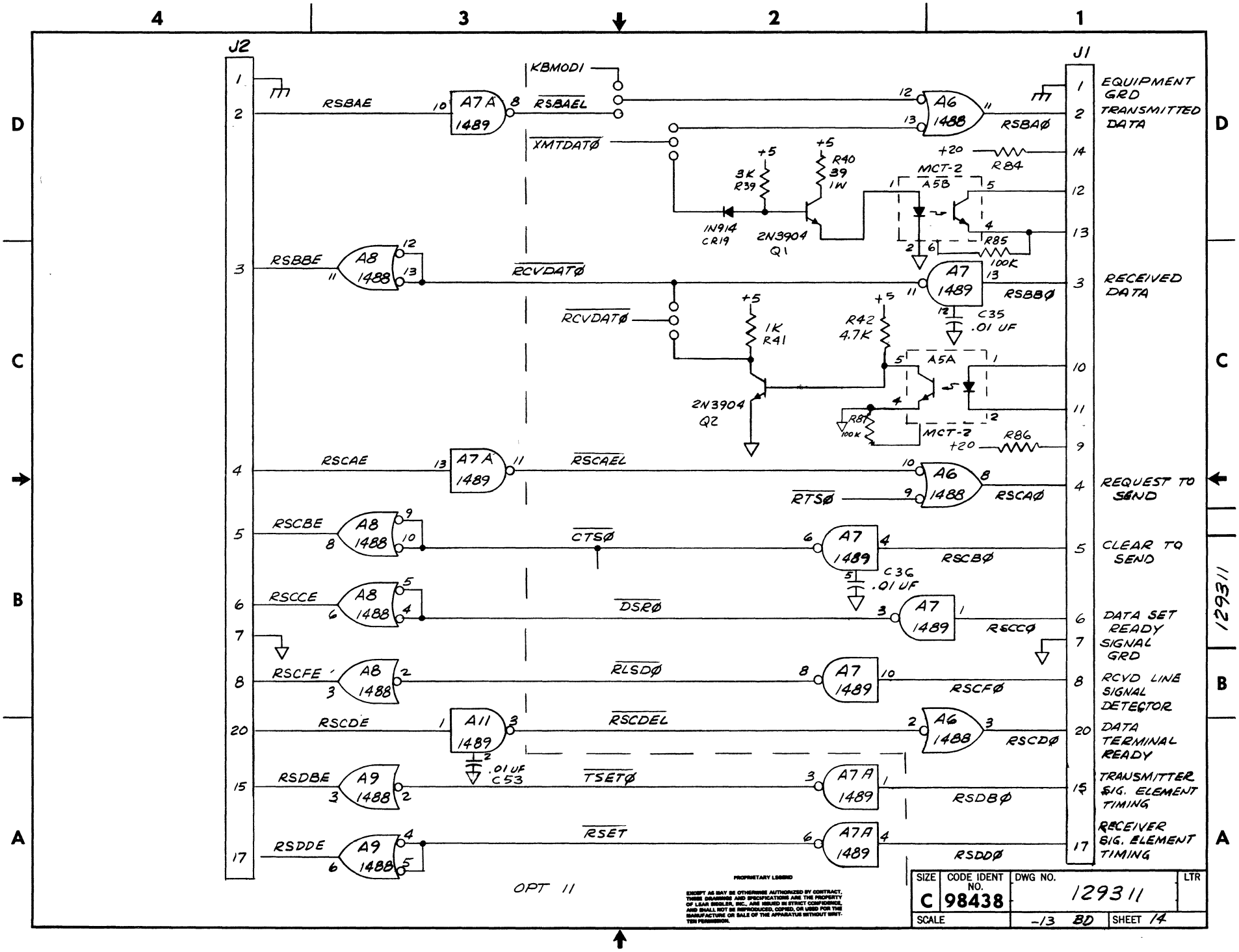
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE –
-13 BD
SHEET 12
129311



SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 13


J2
J1
KBMODI
RSBAE
A7A 1489
RSBAEL
A6 1488
RSBAØ
XMTDATØ
+5
3K R39
R40 39 1W
IN914 CR19
2N3904 Q1
+20
R84
MCT-2 A5B
R85 100K
RSBBE
A8 1488
RCVDATØ
A7 1489
RSBBØ
C35 .01 UF
1K R41
R42 4.7K
2N3904 Q2
A5A
R87 100K
MCT-2
R86
RSCAE
A7A 1489
RSCAEL
RTSØ
A6 1488
RSCAØ
RSCBE
A8 1488
CTSØ
A7 1489
RSCBØ
C36 .01 UF
RSCCE
DSRØ
RSCCØ
RSCFE
RLSDØ
RSCFØ
RSCDE
A11 1489
RSCDEL
RSCDØ
.01 UF C53
RSDBE
A9 1488
TSETØ
A7A 1489
RSDBØ
RSDDE
RSET
RSDDØ
1 EQUIPMENT GRD
2 TRANSMITTED DATA
3 RECEIVED DATA
4 REQUEST TO SEND
5 CLEAR TO SEND
6 DATA SET READY
7 SIGNAL GRD
8 RCVD LINE SIGNAL DETECTOR
20 DATA TERMINAL READY
15 TRANSMITTER SIG. ELEMENT TIMING
17 RECEIVER SIG. ELEMENT TIMING
OPT 11
PROPRIETARY LEGEND
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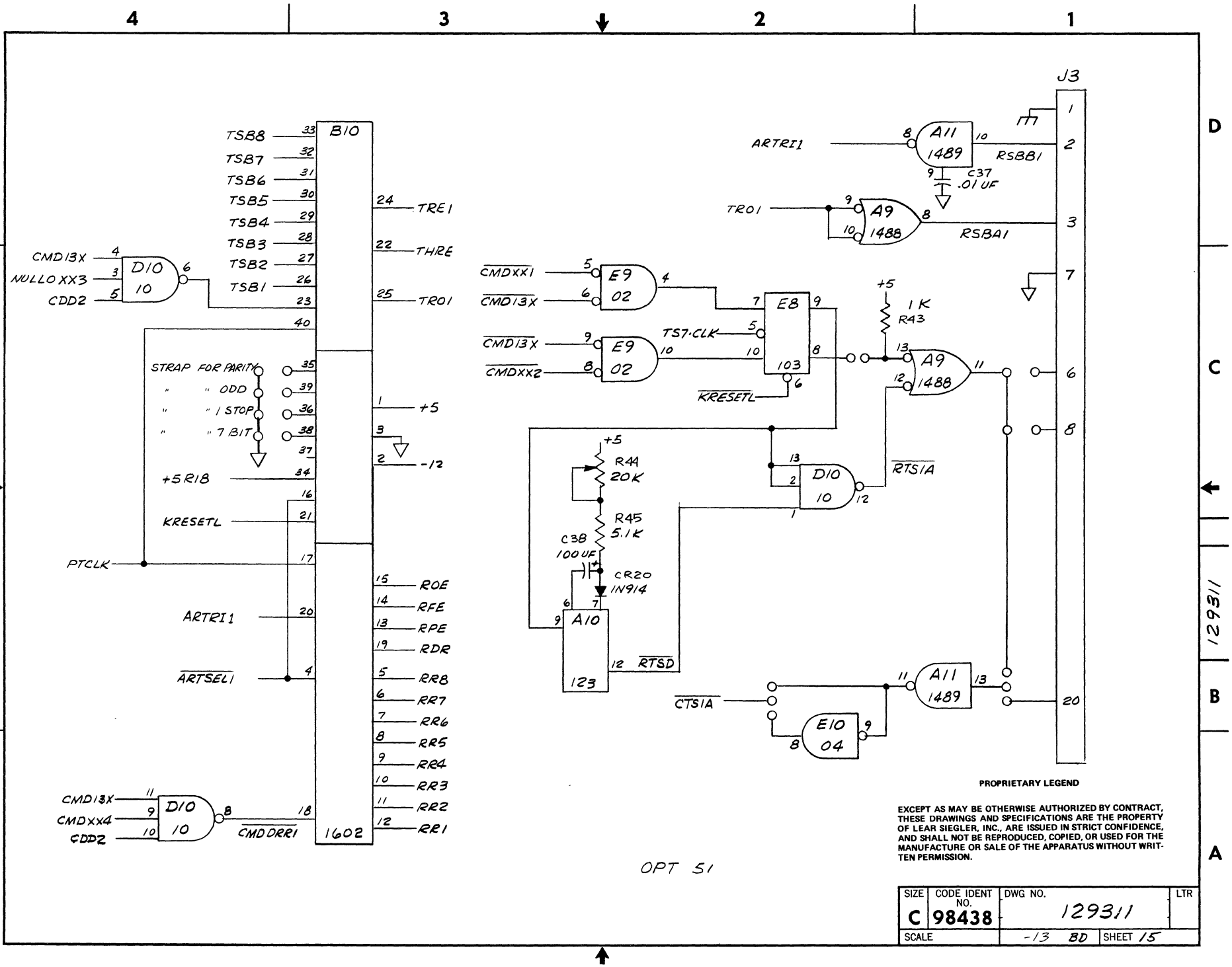
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE
-13 BD
SHEET 14
129311


4
3
2
1
D
C
B
A
B10
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
TRE1
THRE
TRO1
+5
-12
ROE
RFE
RPE
RDR
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
1602
CMD13X
NULLOXX3
CDD2
D10
10
STRAP FOR PARITY
" " ODD
" " / STOP
" " 7 BIT
+5 R18
KRESETL
PTCLK
ARTRI1
ARTSEL1
CMDXX4
CMDDRR1
J3
ARTRI1
A11
1489
RSBB1
C37
.01 UF
TRO1
A9
1488
RSBA1
CMDXX1
E9
02
E8
TS7·CLK
103
KRESETL
+5
1K
R43
R44
20K
R45
5.1K
C38
100 UF
CR20
IN914
A10
123
RTSD
RTSIA
CTSIA
E10
04
PROPRIETARY LEGEND
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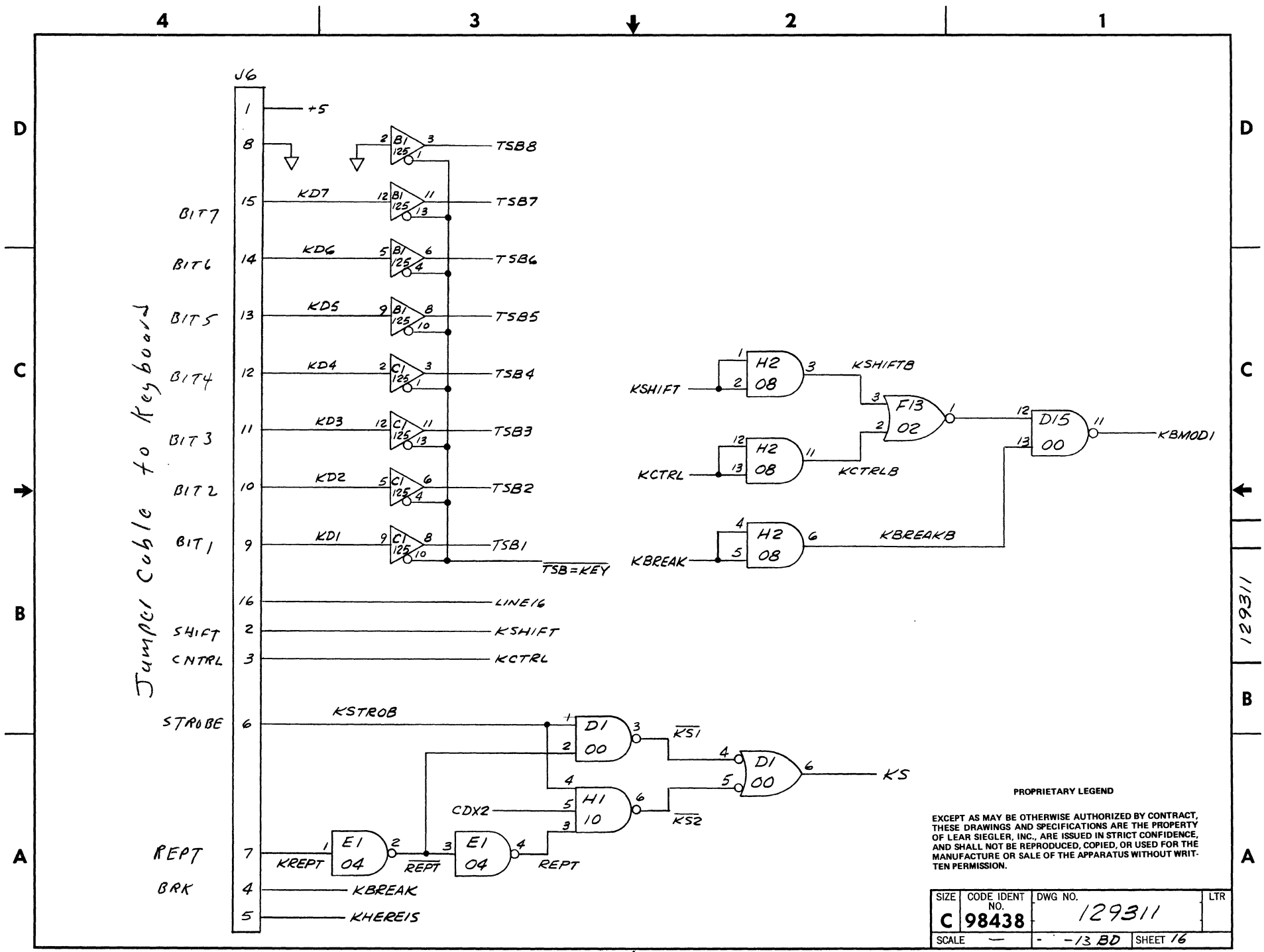
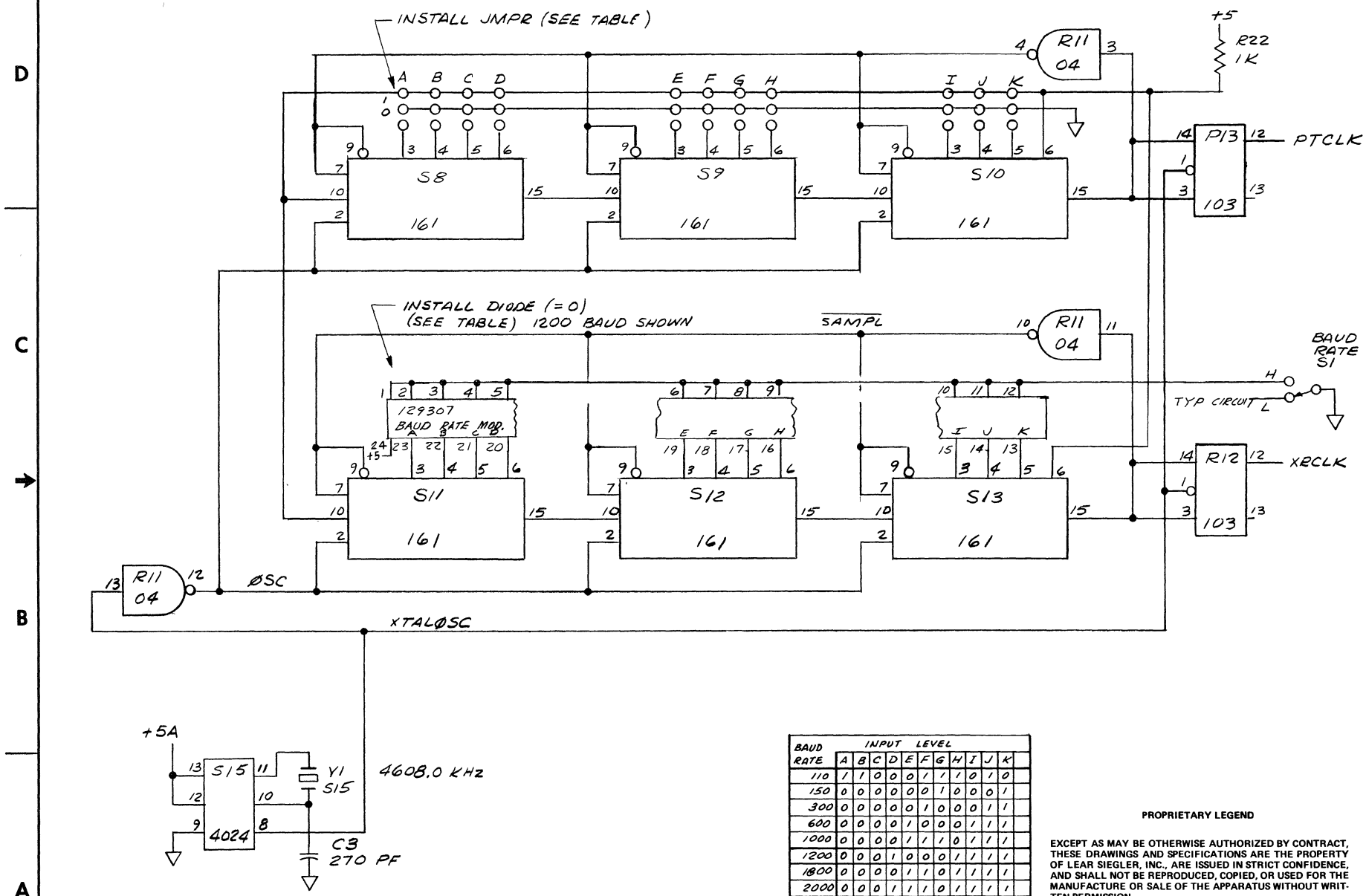
OPT 51
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE
-13 BD
SHEET 15
129311



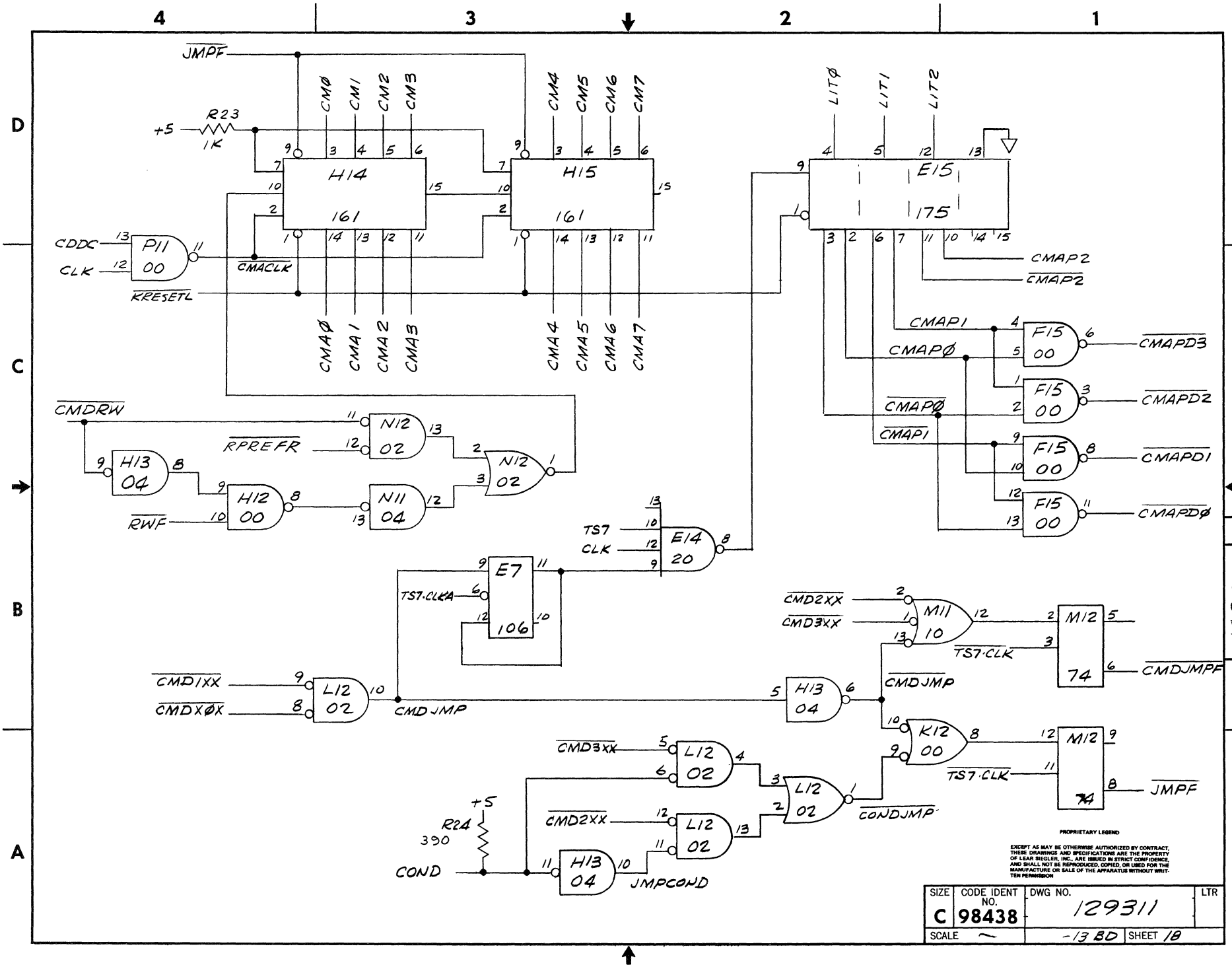
KEYBOARD INTERFACE



BAUD RATE	INPUT LEVEL A	B	C	D	E	F	G	H	I	J	K
110	1	1	0	0	0	1	1	1	0	1	0
150	0	0	0	0	0	0	1	0	0	0	1
300	0	0	0	0	0	1	0	0	0	1	1
600	0	0	0	0	1	0	0	0	1	1	1
1000	0	0	0	0	1	1	1	0	1	1	1
1200	0	0	0	1	0	0	0	1	1	1	1
1800	0	0	0	0	1	1	0	1	1	1	1
2000	0	0	0	1	1	1	0	1	1	1	1
2400	0	0	1	0	0	0	1	1	1	1	1
3600	0	0	0	1	1	0	1	1	1	1	1
4800	0	1	0	0	0	1	1	1	1	1	1
7200	0	0	1	1	0	1	1	1	1	1	1
9600	1	0	0	0	1	1	1	1	1	1	1

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 17

129311


JMPF
CMØ
CM1
CM2
CM3
CM4
CM5
CM6
CM7
+5
R23
1K
H14
161
H15
161
LITØ
LIT1
LIT2
E15
175
CDDC
CLK
P11
00
CMACLK
KRESETL
CMAØ
CMA1
CMA2
CMA3
CMA4
CMA5
CMA6
CMA7
CMAP2
CMAP2
CMAP1
CMAPØ
CMAPØ
CMAP1
F15
00
CMAPD3
CMAPD2
CMAPD1
CMAPDØ
CMDRW
RPREFR
RWF
H13
04
H12
00
N12
02
N12
02
N11
04
TS7
CLK
E14
20
E7
106
TS7·CLKA
CMD1XX
CMDXØX
L12
02
CMDJMP
CMD2XX
CMD3XX
M11
10
TS7·CLK
M12
74
CMDJMPF
H13
04
CMDJMP
K12
00
TS7·CLK
JMPF
CMD3XX
CMD2XX
L12
02
L12
02
L12
02
CONDJMP
+5
R24
390
COND
H13
04
JMPCOND
PROPRIETARY LEGEND
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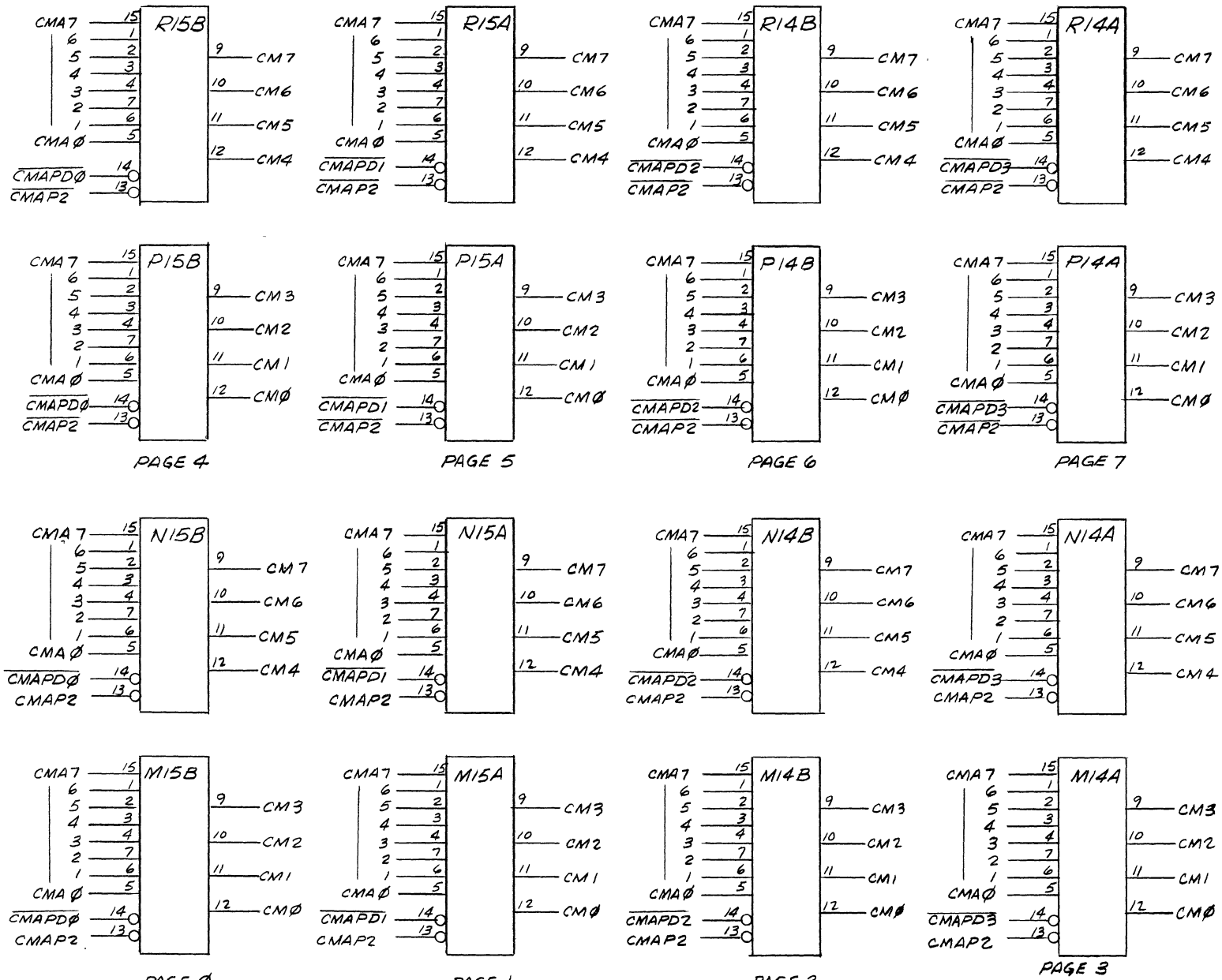
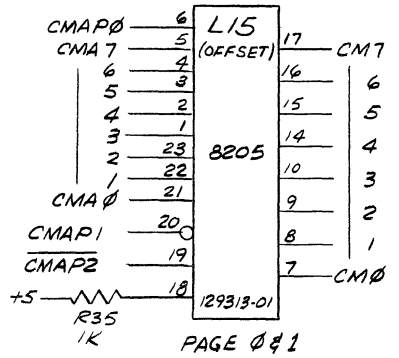
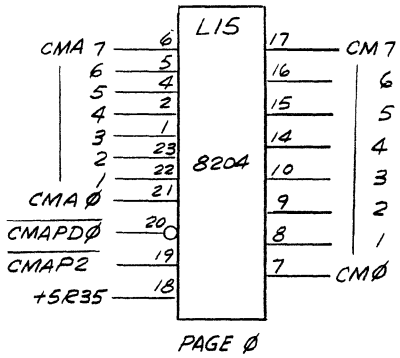
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE —
-13 BD
SHEET 18
129311

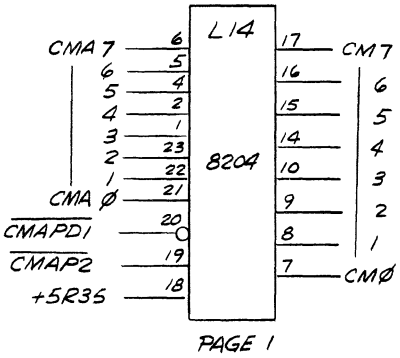


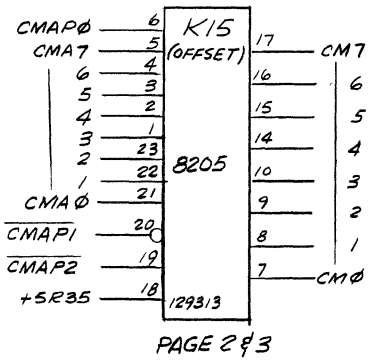
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 19

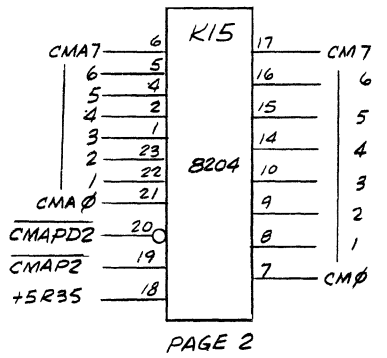
129311

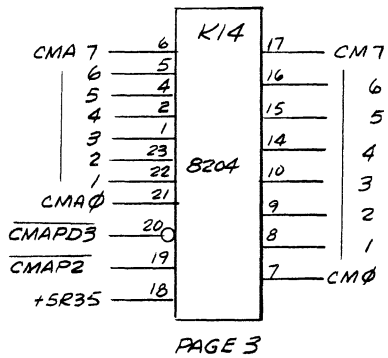


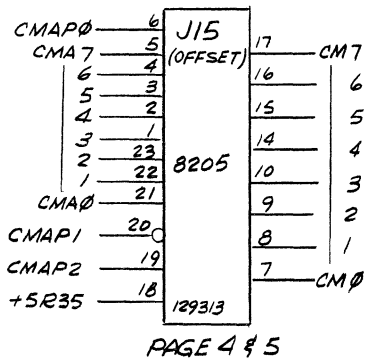


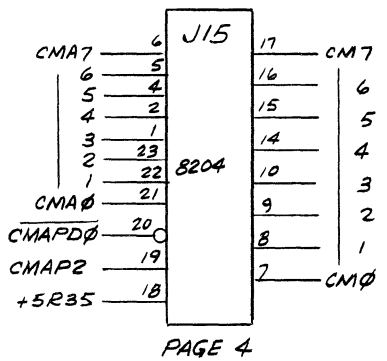


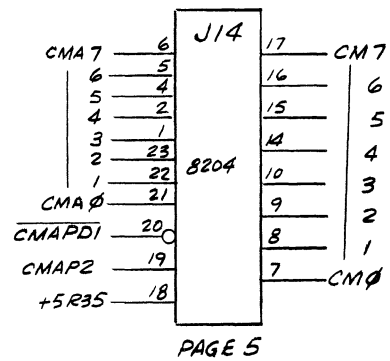






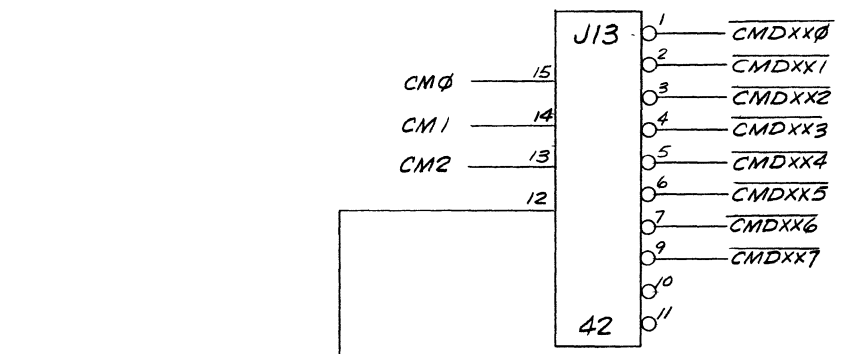


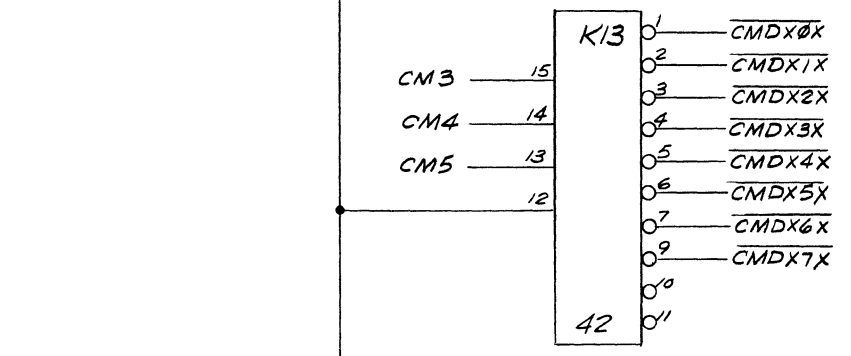


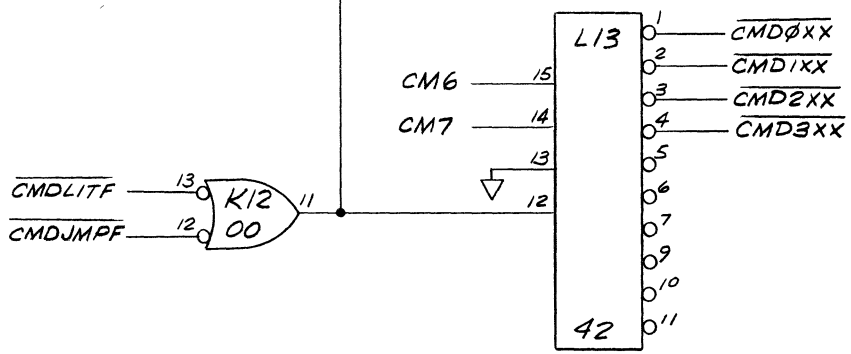


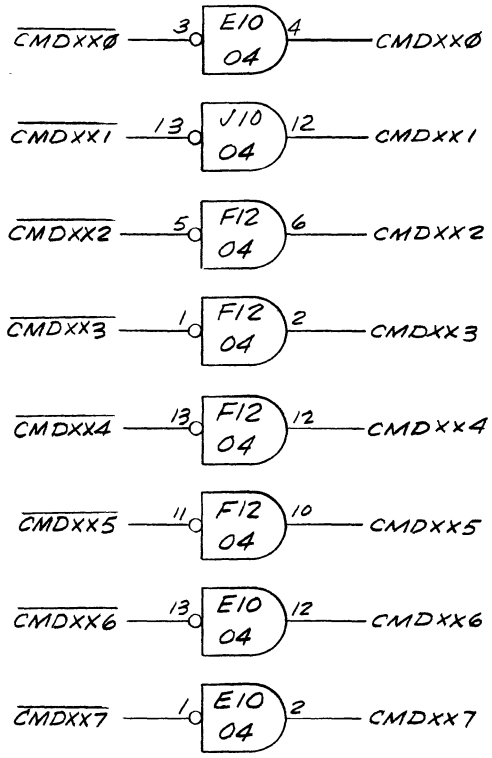
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 20

129311



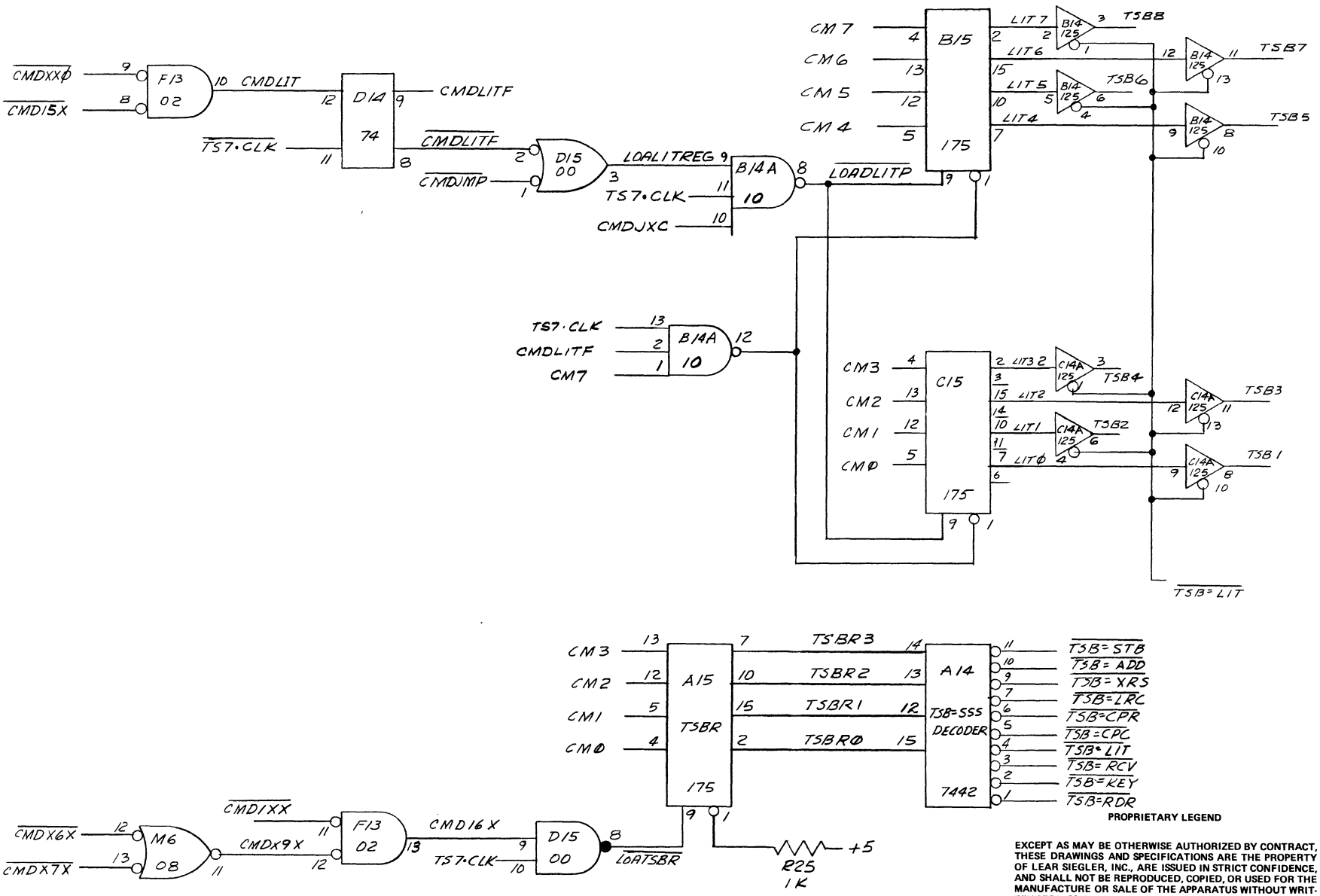






SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 21

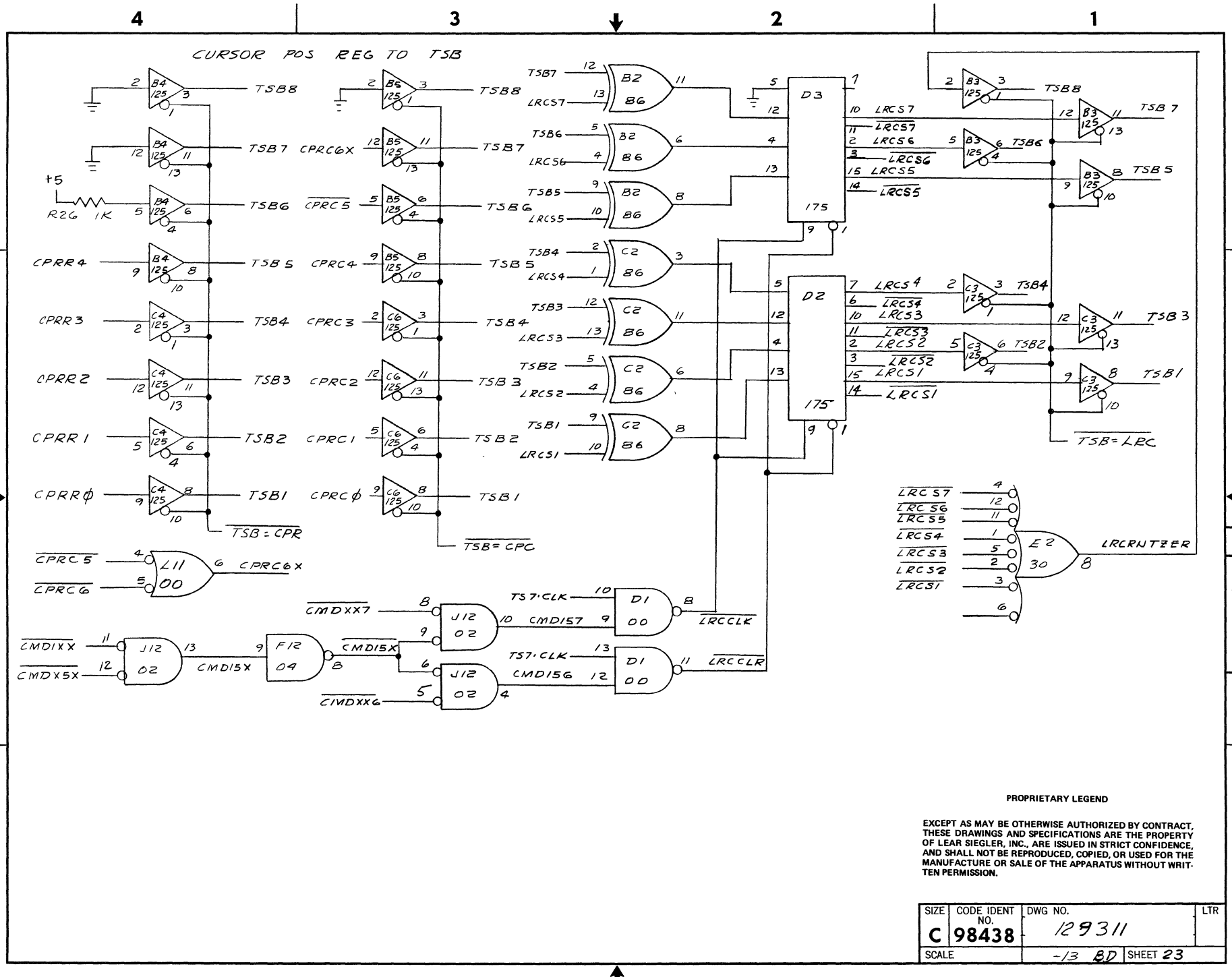
129311



TRI STATE BUS A REG – LITERAL BUFFER

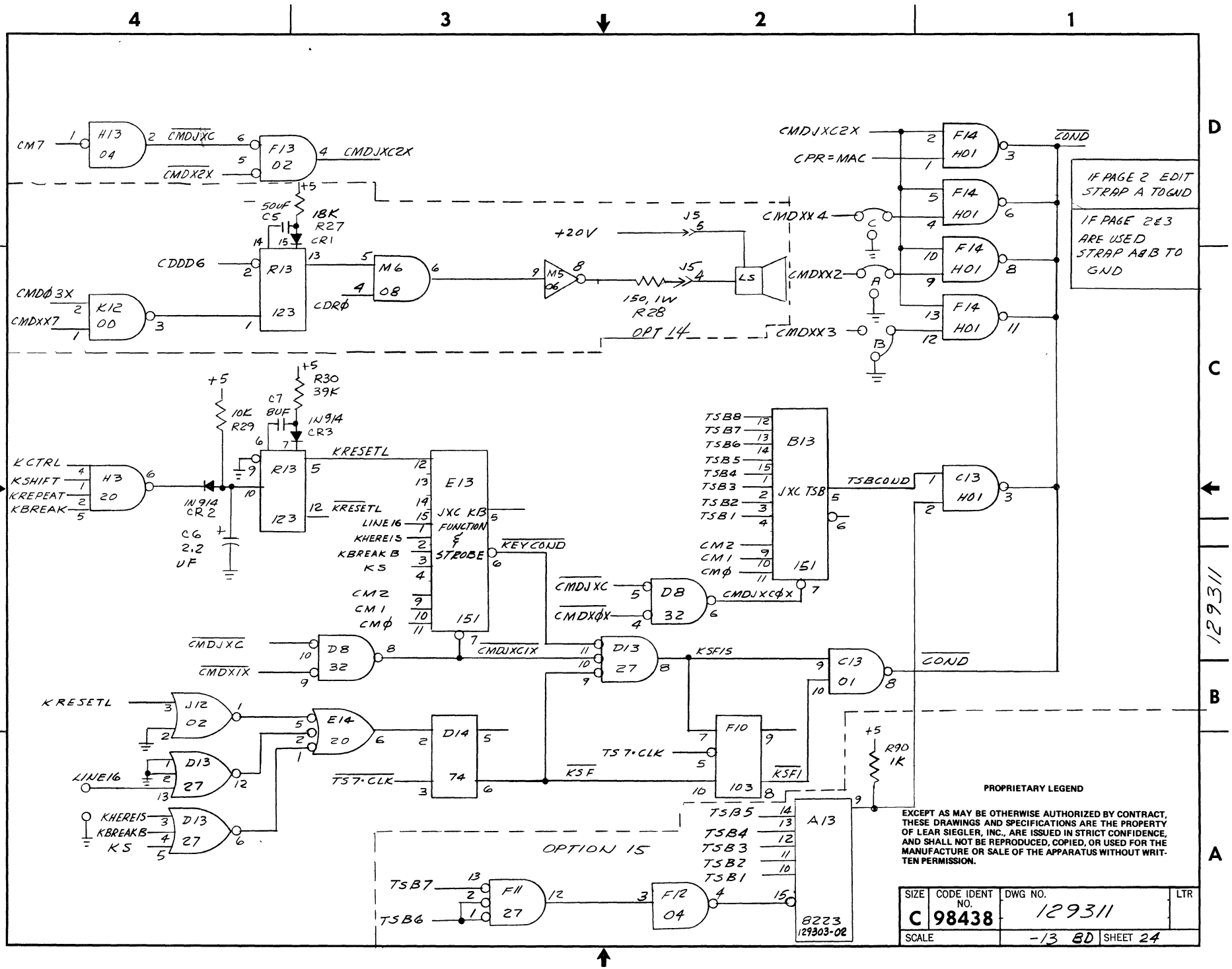
SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE		-13 80	SHEET 22

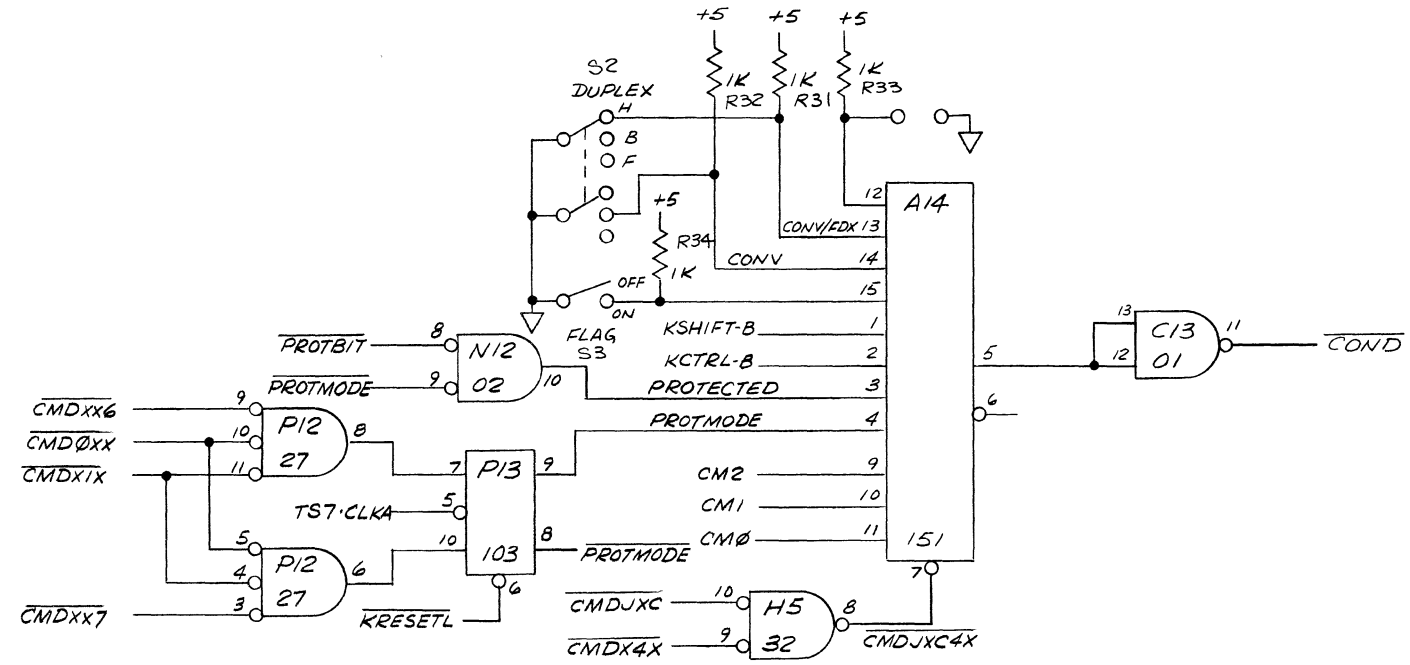
129311

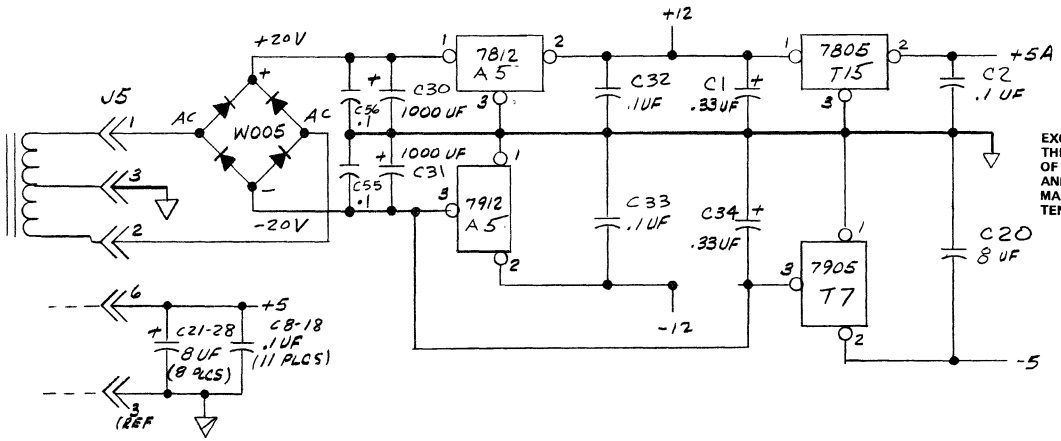


SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE		-13 BD	SHEET 23

129311

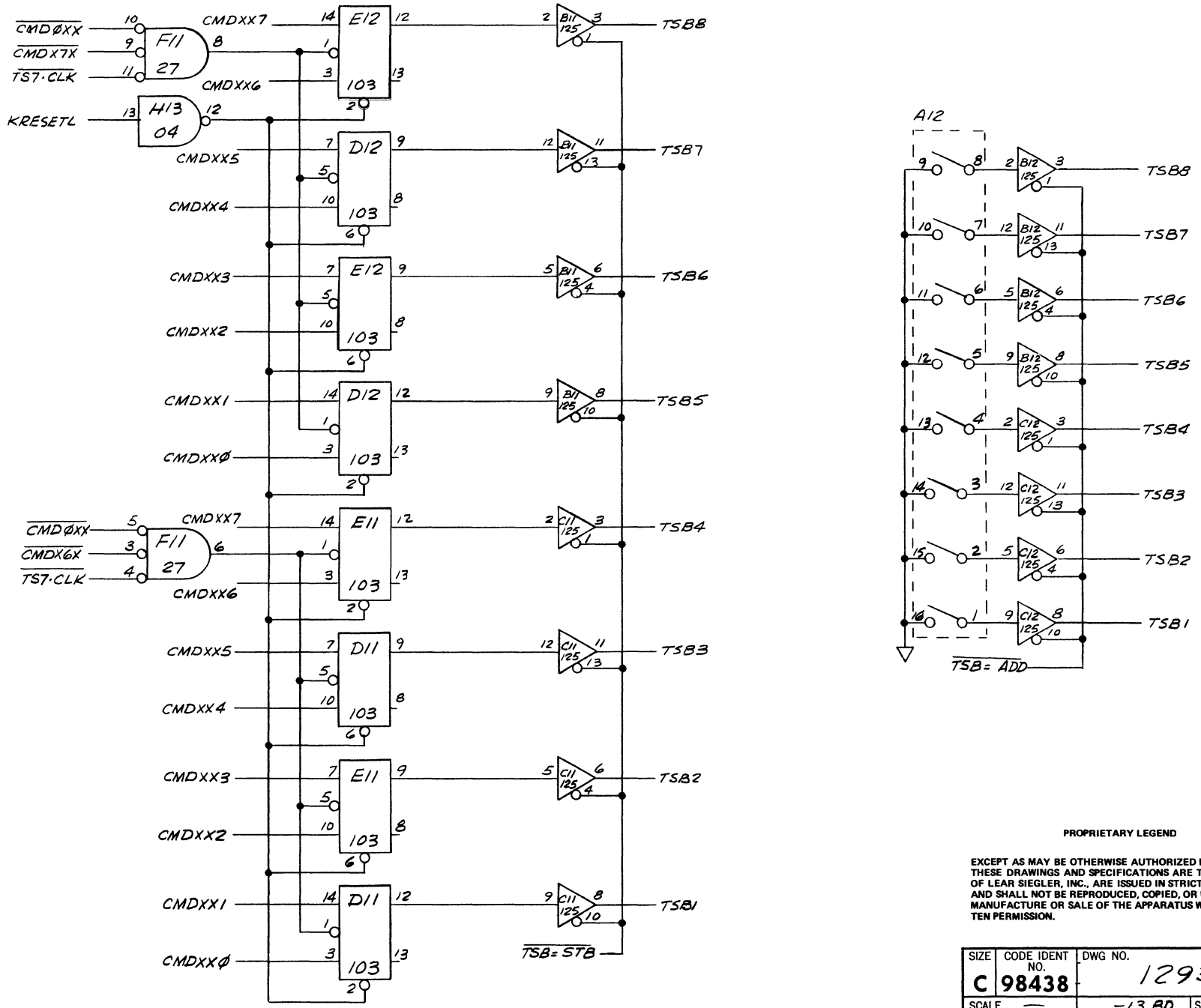

CM7
H13 04
CMDJXC
CMDX2X
F13 02
CMDJXC2X
+5
50UF C5
18K R27
CR1
CDDD6
R13
M6 08
CDRØ
CMDØ3X
CMDXX7
K12 00
+20V
J5
M5 06
150, 1W R28
LS
OPT 14
CMDXX4
CMDXX2
CMDXX3
CMDJXC2X
CPR=MAC
F14 H01
COND
IF PAGE 2 EDIT STRAP A TO GND
IF PAGE 2&3 ARE USED STRAP A&B TO GND
+5
10K R29
C7 8UF
R30 39K
IN914 CR3
KCTRL
KSHIFT
KREPEAT
KBREAK
H3 20
IN914 CR2
C6 2.2 UF
R13
KRESETL
E13
JXC KB FUNCTION & STROBE
LINE16
KHERE15
KBREAK B
KS
CM2
CM1
CMØ
KEYCOND
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
B13 JXC TSB 151
TSBCOND
C13 H01
CMDJXC
CMDXØX
D8 32
CMDJXCØX
CMDXIX
CMDJXCIX
D13 27
KSF15
C13 01
KRESETL
J12 02
E14 20
D14 74
TS7·CLK
KSF
F10 103
KSF1
R90 1K
LINE16
KHERE15
KBREAK B
KS
A13
8223 129303-02
OPTION 15
TSB7
TSB6
F11 27
F12 04
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE
-13 BD
SHEET 24
129311



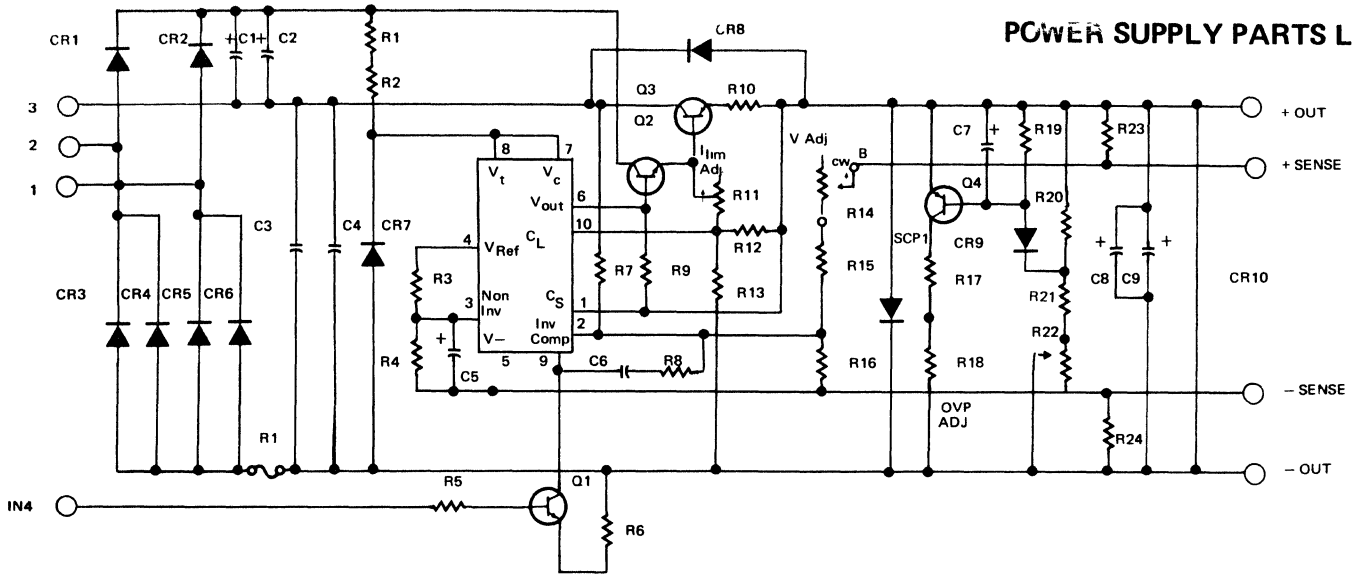


129311

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129311	
SCALE —		-13 BD	SHEET 25


4
3
2
1
D
C
B
A
CMDØXX
CMDX7X
TS7·CLK
F11
27
CMDXX7
CMDXX6
KRESETL
H13
04
CMDXX5
CMDXX4
CMDXX3
CMDXX2
CMDXX1
CMDXXØ
CMDØXX
CMDX6X
TS7·CLK
F11
27
CMDXX7
CMDXX6
CMDXX5
CMDXX4
CMDXX3
CMDXX2
CMDXX1
CMDXXØ
E12
D12
E12
D12
E11
D11
E11
D11
103
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
TSB= STB
A12
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
TSB= ADD
PROPRIETARY LEGEND
EXCEPT AS MAY BE OTHERWISE AUTHORIZED BY CONTRACT, THESE DRAWINGS AND SPECIFICATIONS ARE THE PROPERTY OF LEAR SIEGLER, INC., ARE ISSUED IN STRICT CONFIDENCE, AND SHALL NOT BE REPRODUCED, COPIED, OR USED FOR THE MANUFACTURE OR SALE OF THE APPARATUS WITHOUT WRITTEN PERMISSION.
SIZE C
CODE IDENT NO. 98438
DWG NO. 129311
LTR
SCALE —
-13 BD
SHEET 26
129311

POWER SUPPLY PARTS LIST

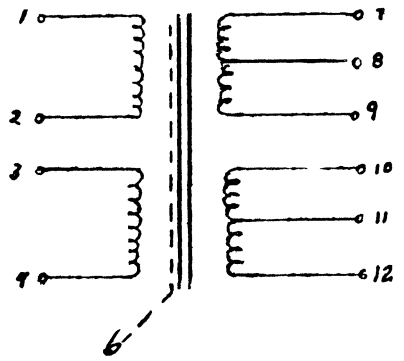


REF DES	DESCRIPTION	VALUE	POWERTEC PART NO.
C1	CAP ELECT	470/15V	32-13006-002
C2	CAP ELECT	470/15V	32-03006-002
C3	CAP ELECT	9000/15V	32-13007-001
C4	CAP ELECT	9000/15V	32-13007-001
C5	CAP ELECT	1/50V	32-03006-001
C6	CAP FILM	.001/100V	31-13005-008
C7	CAP ELECT	1/50V	32-13006-001
C8	CAP ELECT	470/15V	32-13006-002
C9	CAP ELECT	470/15V	32-13006-002
CR1	DIODE	S1-2	11-13009-001
CR2	DIODE	S1-2	11-13009-001
CR3	DIODE	351S	11-13010-001
CR4	DIODE	351S	11-13010-001
CR5	DIODE	351S	11-13010-001
CR6	DIODE	351S	11-13010-001
CR7	DIODE	–	
CR8	DIODE	S1-2	11-13009-001
CR9	DIODE, ZENER	1N751A	12-13025-006
CR10	DIODE	351S	11-13010-001
R1	RES 1/2W, 5%	51Ω	20-13004-042
R2	RES, 1/2W, 5%	51Ω	20-13004-042
R3	RES, RNGOC	3.01KΩ	21-13050-239
R4	RES, RNGOC	4.02KΩ	21-13050-251
R5	RES, 1/2W, 5%	47KΩ	20-13004-113
R6	RES, 1/2W, 5%	1KΩ	20-13004-073
R7	RES	–	
R8	RES, 1/2W 5%	3.3KΩ	20-13004-085
R9	RES, 1/2W 5%	1KΩ	20-13004-073

REF DES	DESCRIPTION	VALUE	POWERTEC PART NO.
R10	RES, 5W	.05Ω	22-13049-001
R12	RES	–	
R13	RES, 1/2W, 5%	510Ω	20-13004-066
R15	RES	JUMPER	
R16	RES, RN60C	1.5KΩ	21-13050-210
R17	RES, 1/2W, 5%	100Ω	20-13004-049
R18	RES, 1/2W, 5%	1KΩ	20-13004-073
R19	RES, 1/2W, 5%	1KΩ	20-13004-073
R20	RES, RN60C	1KΩ	21-13050-193
R21	RES	JUMPER	
R23	RES, 1/2W, 5%	10Ω	20-13004-025
R24	RES, 1/2W, 5%	10Ω	20-13004-025
R11	POT	100Ω	23-13016-004
R14	POT	1.5KΩ	23-13032-006
R22	POT	500Ω	23-13016-007
Q1	TSTR	2N2222A	10-13019-001
Q2	TSTR	13159-2	10-13159-002
Q3	TSTR	13002-3	10-13002-003
Q4	TSTR	2N2907A	10-13020-001
SCR1	SCR	2N4441	13-13015-001
UI	I.C.	723CE	14-13034-001
F1	FUSE	15A	63-16045-013

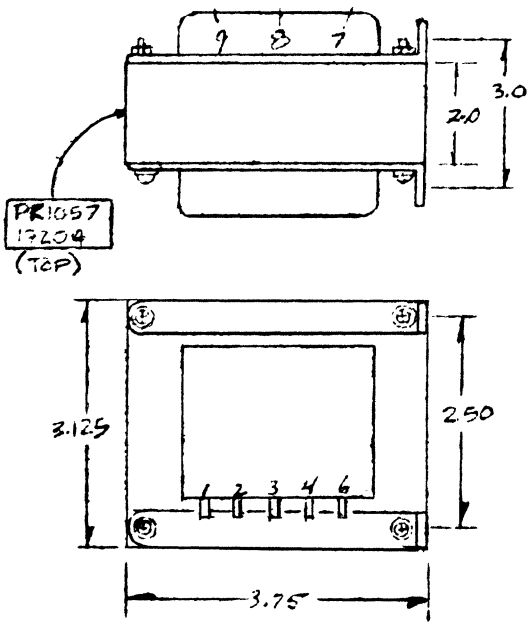
Input fuse blows	(1) check fuse rating (2) possible overload (3) Ovp triggering with Q2, Q3, CR8 shorted (4) CR1, CR2, CR3, CR4, CR5, CR7, C1, C2, C3, C4 shorted
Low output voltage, poor regulation, high ripple, loaded	(1) possible overload or current limit adj. R11 improperly adjusted (should be set for 120% of full load current prior to foldback) (2) possible Ovp triggering check setting of R22 (3) U1 defective (4) CR7, C1, R4, C5, R14, C8, CR10, R11, Q1, R15 shorted (5) R1, R2, R3, R13, R16 open
High output voltage, poor regulation, high ripple, loaded	(1) U1 defective (2) Q2, Q3, CR8, R3, R16 shorted (3) R4, R14, R15 open
High output voltage unloaded. OK loaded	(1) U1 defective (2) Q3, Q3 high leakage
Output noise	(1) U1 defective (2) C5, C8, C9 open
Output oscillation	(1) U1 defective (2) C6, R8, C8, C9 open
OVP triggers under normal operation	(1) check Ovp setting (2) SCR1, Q4, CR9, R21, R22 shorted (3) C7, R20 open
OVP fails to trigger	(1) SCR1, R17, Q4, CR9, R21, R22 open (2) C7, R19, R18 shorted
Inhibit does not function	(1) Q1, R5, R6 open
Excessive unit heating	(1) possible overload (2) inadequate heat sinking or heat sink bolted to uneven surface, no thermal compound used in heat sinking (3) input voltage too high

SCHEMATIC DIAGRAM:



LEAD BREAKOUT

ASSEMBLY:



CABLE ASSEMBLIES

REF DES	DESCRIPTION	LSI PART NO.	MFG PART NO./ MIL TYPE DES	MFG. NAME	NOTE
1	Cable – Monitor	129318-1			
2	Cable – Power Dist.	129318-11			
3					
4	Receptacle, 9 Pin		03-09-1093	Molex	
5	Contact, Male, 22-18		1380 or 02-09-2116 (Reel)	Molex	
6	Contact, Female, 22-18		1381 or 02-09-1116 (Reel)	Molex	
7	Receptacle, 6 Pin		03-09-1063	Molex	
8	Contact, Male, 20-14		1190 or 02-09-2101 (Reel)	Molex	
9	Contact, Female, 20-14		1189 or 02-09-1101 (Reel)	Molex	
10	Housing		583479-1	Amp	
11	Contact		583259-2	Amp	
12	Wire, 22 AWG (7 x 30), .095 O.D.		8920 (See List for Colors)	Belden or Eq.	
13	Wire, 18 AWG (16 x 30), 112 O.D.		8918 – Wht or Blk (See List)	Belden or Eq.	
14	Spade Term, Insulated		50225	Ark-Less or Equiv.	
15					
16	Key		583462-1	Amp	

WIRE LIST

LINE NO.	TERMINATION INFORMATION					
	CABLE NO.	WIRE NO. OR COLOR	FROM		TO	
			REF DES	PIN	REF DES	PIN
1	129318	BRN	P4	1	MONP1	3
2		RED		2		4
3	–1	ORG		3		2
4		YEL		4		8
5		WHT		5		5
6		WHT		6		10
7		WHT		7		1
8		GRN		8		6
9		BLK		9		9
10					NOT USED	7
11	129318	RED	P5	1	T1	7
12		RED		2	T1	8
13	–11	WHT		3	T1	9
14		WHT		3	REG-V	
15		BRN		4	SPKR	
16		YEL		5	SPKR	
17		BLK		6	REG+V	
18						

ASSEMBLY WIRE LIST

LINE NO.	TERMINATION INFORMATION					
	SEE FIG. NO.	WIRE NO. OR COLOR	FROM		TO	
			REF DES	PIN	REF DES	PIN
1	2		P4		MON P1	
2	2		P5		(1)	
3	1	BLK			S1	2
4		WHT			TB1	2A
5		GRN			(2)	
6	1	BLK	FAN	1	TB1	1B
7	1	WHT	FAN	2	TB1	2B
8	1	BLK	S1	1	CB1	1
9	1 (5)	BLK	CB1	2	TB1	1A
10	2 (5)	BLK	T1	1	TB1	1C
11	2 (5)	WHT	T1	2	TB1	2C
12	2	BLK	MON (3)		TB1	1D
13		WHT	MON (3)		TB1	2D
14	2	BRN	T1	11	REG	3
15	2	WHT	T1	12	REG	2
16	2	YEL	T T1	10	REG	1
17	2 (5)	BLK	T1	1	T1	3
18	2 (5)	WHT	T1	2	T1	4

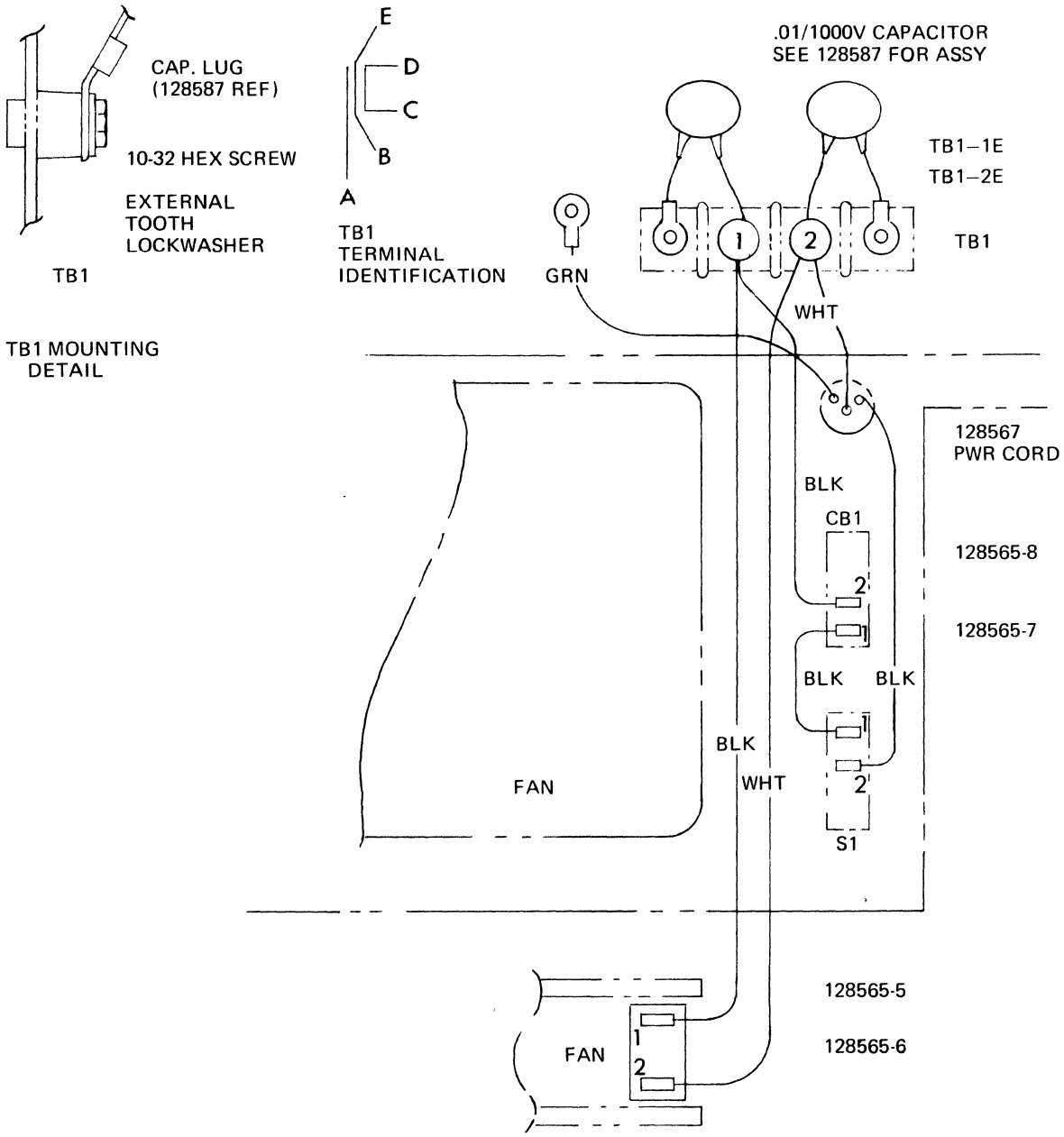
CODE NOTES:

(1) See 129318-11 for terminations.

(2) Terminate at Grd Stud.

(3) Reterminate existing wires from monitor power supply with .250 tab receptacles, F/N 17, flush sleeve

(5) Fro 230V – replace Blk CB1-2 to TB1-1A with CB1-2 to T1-1. See Detail A of Figure 2 for T1 term.


CAP. LUG
(128587 REF)
10-32 HEX SCREW
EXTERNAL
TOOTH
LOCKWASHER
TB1
TB1 MOUNTING
DETAIL
E
D
C
B
A
TB1
TERMINAL
IDENTIFICATION
.01/1000V CAPACITOR
SEE 128587 FOR ASSY
TB1–1E
TB1–2E
TB1
GRN
WHT
128567
PWR CORD
BLK
CB1
128565-8
128565-7
BLK
BLK
BLK
WHT
FAN
S1
128565-5
128565-6
FAN

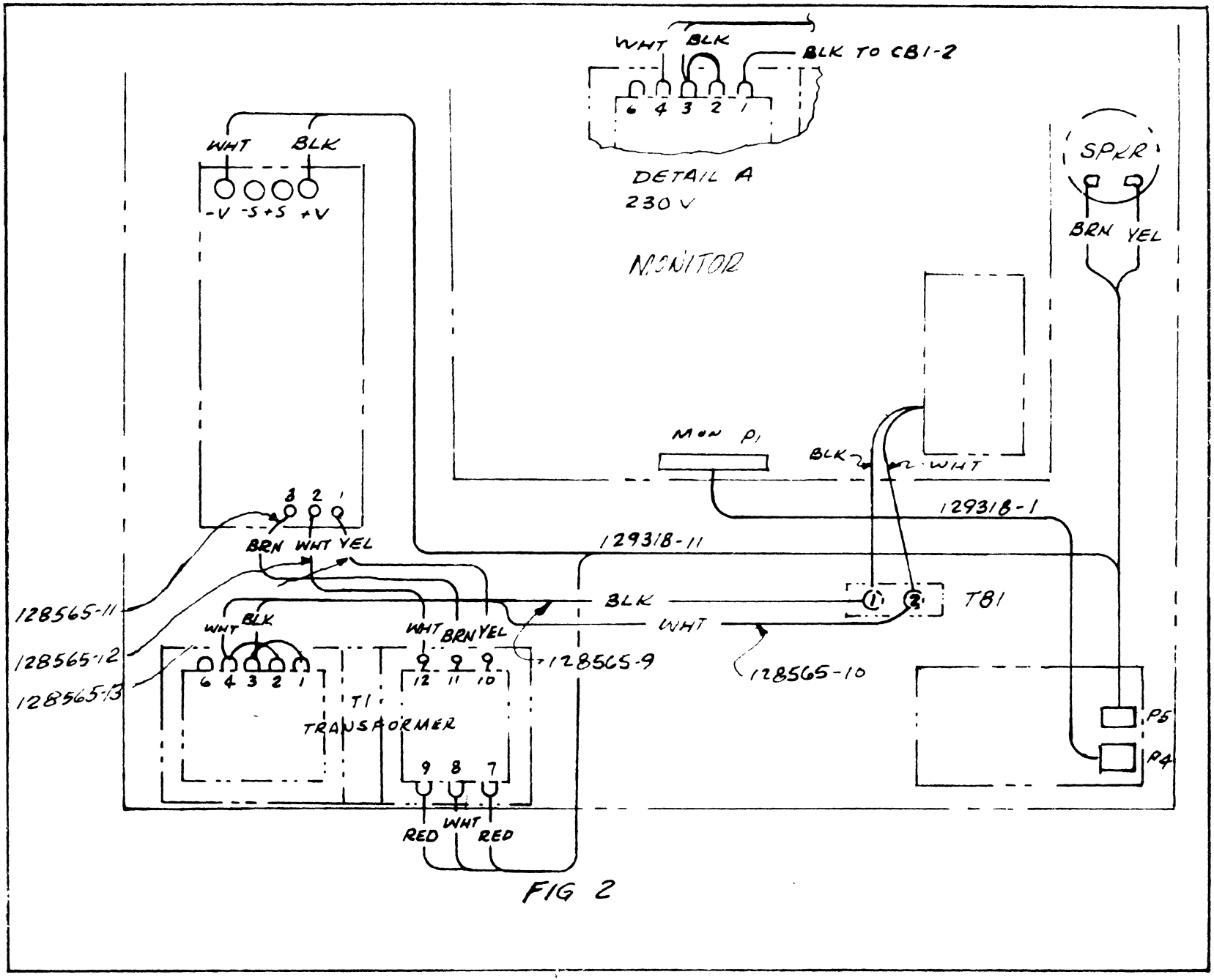

WHT
BLK
BLK TO CB1-2
6 4 3 2 1
DETAIL A
230 V
MONITOR
SPKR
BRN YEL
WHT BLK
-V -S +S +V
MON P1
BLK
WHT
129318-1
129318-11
3 2 1
BRN WHT YEL
128565-11
128565-12
128565-13
BLK
WHT
TB1
WHT BLK
WHT BRN YEL
6 4 3 2 1
12 11 10
128565-9
128565-10
T1
TRANSFORMER
9 8 7
RED WHT RED
P5
P4

FIG 2

1-010068

KEY NO.	PART NO.	-0001 COLOR	-0001 FILL	-0002 COLOR	-0002 FILL
1		10	22	-0020	-22
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
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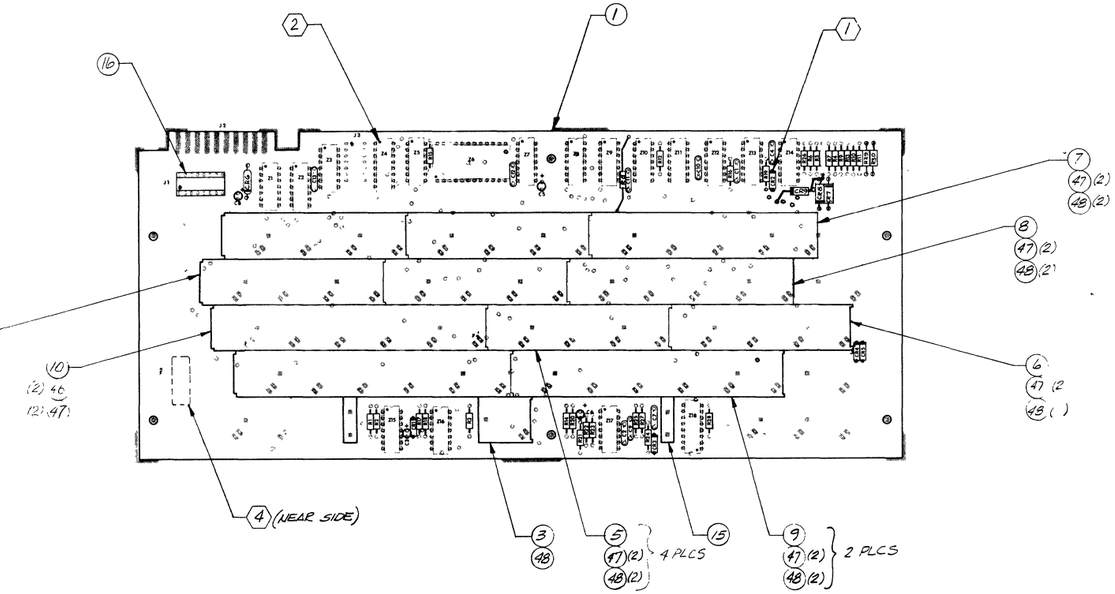
81					



REVISIONS					
REV LTR	DESCRIPTION	BY	DATE	APP	DATE
API	FIRST RELEASE - PROTOTYPE	RL	7-5-74	[illegible]	8/1/75
A	SEE CN 01301	RL	11-6-74	[illegible]	8/1/75
B	INC CN01315	CEL	5/19/75	[illegible]	8/1/75
C	INC CN01330	CEL	6/4/75	[illegible]	8/1/75
D	INC CN 01461	[illegible]	[illegible]	[illegible]	[illegible]
E	SEE CN 3473	RL	[illegible]	[illegible]	[illegible]

ITM	NOMENCLATURE	PART NO.	MISC	QTY
50				
49				
48	UNIT	[illegible]	[illegible]	1
47	SCREW	[illegible]	[illegible]	3
46				
45	RESISTOR	[illegible]	[illegible]	1
44		[illegible]	[illegible]	
43		[illegible]	[illegible]	
42		[illegible]	[illegible]	
41		[illegible]	[illegible]	1
40		[illegible]	[illegible] R30	2
39	RESISTOR	[illegible]	[illegible]	12
38				
37	CAPACITOR	[illegible]	[illegible]	5
36		F15020-1001	C11	1
35		F1501[illegible]-0001	C5, C8	2
34		F1501[illegible]-0001	C9, C6	2
33				
32	CAPACITOR	F15021-0001	C4, C7	2
31	CABLE ASSY	F15022-0001	C1	1
30	DIODE	F20010	CR1-CR4	3
29				
28	INTEGRATED CIRCUIT	F25012	Z13	1
27		F25015	Z17	1
26		F25003	Z16	1
25		F25011	Z15	1
24		F25027	Z14	1
23		F25023	Z10	1
22		F25014	Z8 Z1, Z11, Z12	4
21		F25018	Z7 Z13	2
20		F25010	Z6	1
19		F25004	Z4	1
18		F25017	Z4, Z5	2
17	INTEGRATED CIRCUIT	F25013	Z1, Z2	2
16	SOCKET IC.	[illegible]	U1	1
15	SPACER SUB ASSY	[illegible]	SUNIT	1
14				
13				
12				
11				
10	SWITCH ASSY, 40-PIN	[illegible]	-1B-2B-3B-4B-5B-6B	1
9		[illegible]	-1A-2A-3A-4A-5A-6A	1
8		[illegible]	-3B-4B-5B-6B	1
7		[illegible]	-2B-3B-4B-5B	1
6		[illegible]	-2A-3A-4A-5A	1
5		[illegible]	-1B-2B-3B-4B	1
4		[illegible]	-1A-2A-3A-4A	1
3	SWITCH ASSY, 24-PIN	[illegible]	-1B	1
2				
1	PRINTED CIRCUIT BD.	N10013		1

MATERIAL LIST

Controls Research Corp.
Santa Ana, Calif. a subsidiary of MITEX

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON:
DECIMALS: .XX = ±.03, .XXX = ±.010
ANGLES: = ±1/2°

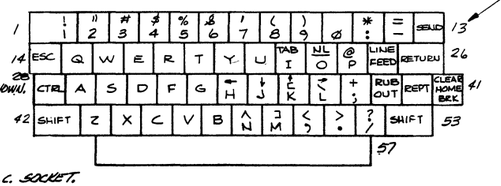
DRAWN BY	RL	8/1/75
CHECKED	[illegible]	8/1/75
APPROVED	[illegible]	8/1/75

COMPONENT OVERLAY
LEAR SIEGLER
W/2 KEY ROLLOVER
SCALE FULL
B30010-C
SIZE E

DO NOT SCALE PRINT

—THIS REVISION APPLIES TO 'C&D' REV REWORKED P.C.B. — ONLY

KEYTOP LOCATION CHART
REF KEYTOP TABULATION BLOCK

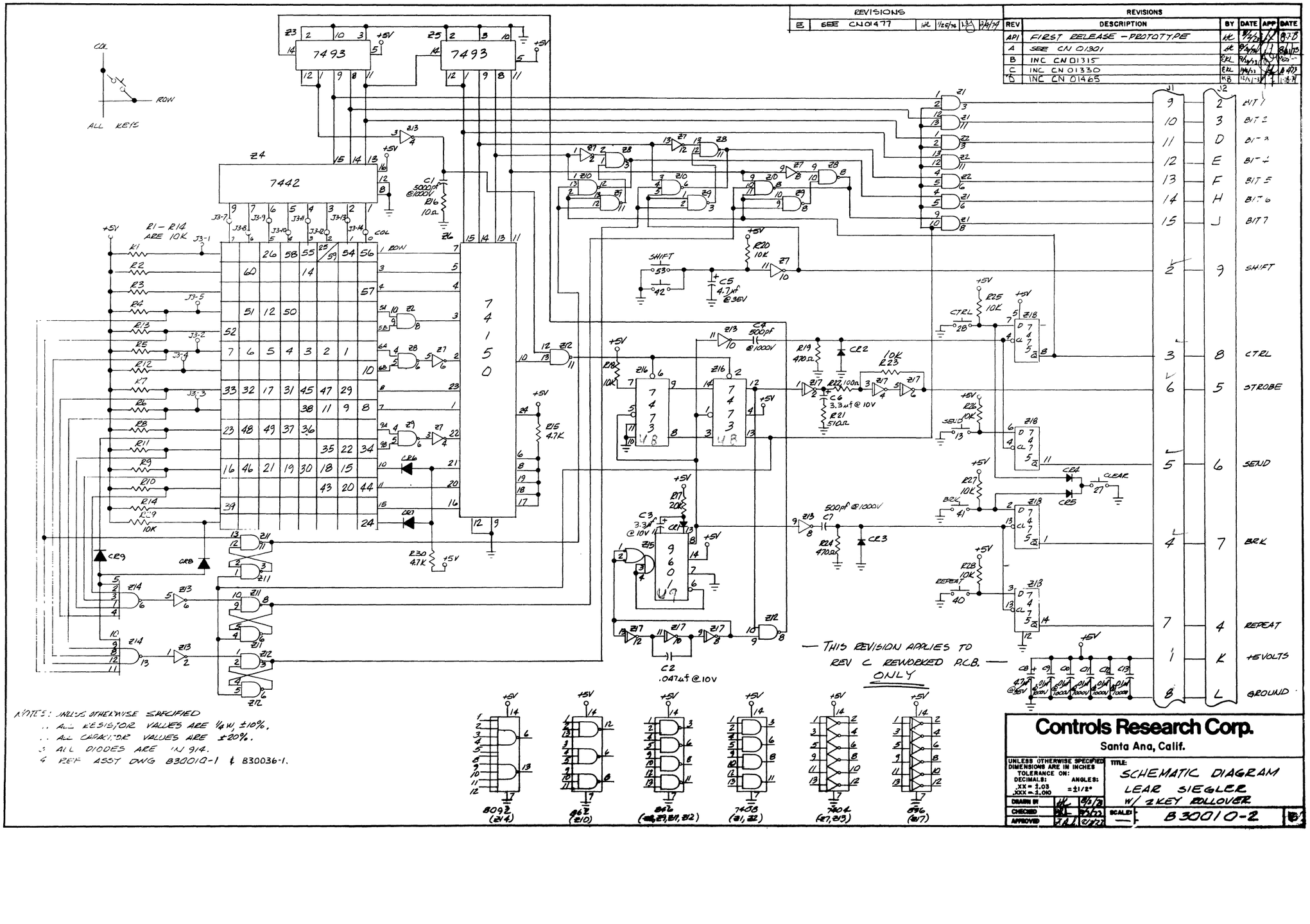


NOTE: UNLESS OTHERWISE SPECIFIED

1. BAR DENOTES CATHODE END OF DIODE
2. DOT DENOTES PIN NO. 1 OF INTEGRATED CIRCUIT
3. REF. LEAR SIEGLER, INC. DWG NO. 129301
4. RUBBER STAMP CURRENT ASSY REV. LEVEL APPROX. WHERE SHOWN.
5. REF. SCHEMATIC B30010-2
6. TEST AND ACCEPT PER ES-1003,
7. REF. CONNECTOR J2 CINCH PART NO. 251-10-30-160.
8. REF. CONNECTOR J3 IS FOR ANY DUAL-IN-LINE 14 PIN I.C. SOCKET.

REVISIONS					
E	SEE CN01477	HK	12/5/78	[illegible]	3/4/79

REVISIONS					
REV	DESCRIPTION	BY	DATE	APP	DATE
API	FIRST RELEASE – PROTOTYPE	HK	8/2/78	[illegible]	8/7/78
A	SEE CN 01301	HK	8/29/78	[illegible]	8/31/78
B	INC CN01315	EKL	10/3/78	[illegible]	10/20/78
C	INC CN 01330	EKL	10/27/78	[illegible]	11/8/78
*D	INC CN 01465	KB	12/1/78	[illegible]	1/8/79



— THIS REVISION APPLIES TO REV C REWORKED P.C.B. — ONLY

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE 1/4 W, ±10%.
2. ALL CAPACITOR VALUES ARE ±20%.
3. ALL DIODES ARE 1N 914.
4. REF ASST DWG B30010-1 & B30036-1.

Controls Research Corp.
Santa Ana, Calif.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE ON:
DECIMALS: XX = ±.03, XXX = ±.010
ANGLES: = ±1/2°

DRAWN BY	HK	8/1/78
CHECKED	EKL	8/2/78
APPROVED	[illegible]	8/2/78

TITLE: SCHEMATIC DIAGRAM LEAR SIEGLER W/ 2KEY ROLLOVER

SCALE: —

B30010-2

D

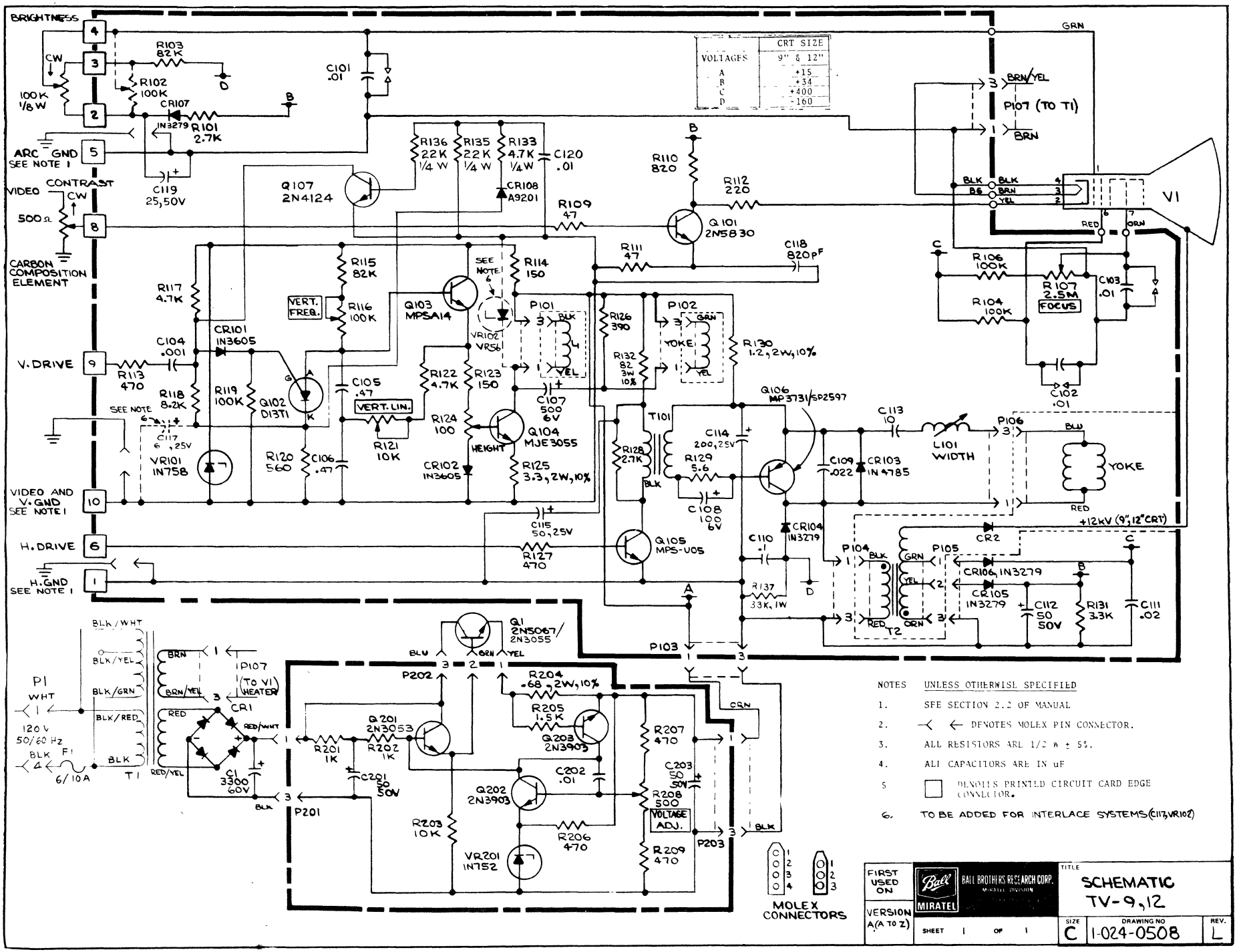


Fig. 5 Schematic, TV 9 and 12 With Power Supply