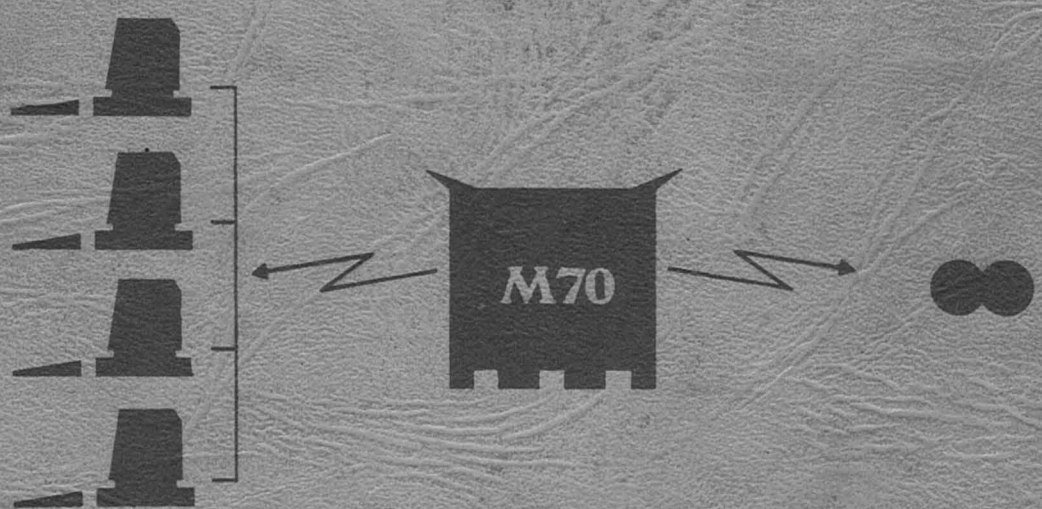
SBC M70

SINGLE BOARD COMPUTER

User Guide



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ADDITIONAL CONFIGURATION INFORMATION

The SBCM70/SBCM71 in this package is a new artwork, all functions available on previous artworks have not changed. Additional functions that have been added are :

SBCM70 (new artwork Rev H)

1. Backplane battery backup is now supported.

2. The timeout can be changed from 12 microsecs to 24 microsecs for older controllers.

3. IDC cables can now be used for serial lines.

SBCM71 (new artwork Rev C)

1. Backplane battery backup is now supported.

2. The timeout can be changed from 12 microsecs to 24 microsecs for older controllers.

3. The EPROM sockets can now be configured for any of :

   512K EPROM
   256k EPROM and 128k NVRAM
   256k NVRAM

W A R N I N G

1. The backplane Pin AS1 in some backplanes can be used for either +12VB or +5VB battery backup. With the latest revision of the SBCM71 and SBCM70 this must be either +5VB or disconnected, otherwise shorting of the power supply will occur.

2. On M70/M71 boards with battery backup the power up algorithm has been changed so that memory is not erased on zeroes on the assertion of "DCOK" on the backplane. "DCOK" is asserted by the power supply on power-up and also by the "RESTART" switch.

N.B. Some older M.T.I. controllers may have problems with the battery backup power-up algorithm. This is under investigation by M.T.I.. The symptoms of this problem are that the M70/M71 will now power up with M.T.I. controller present in the backplane.

If you experience this problem, please contact the factory.

ADDENDUM

First Edition, November 1st 1987.

The material in this **SBC-M70 User Guide** may be subject to modification. Notification of any modifications may not be given but copies of any such changes will be available.

The following are trade marks of **Digital Equipment Corporation** used in this manual:

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- LSI-11
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- FALCON 11/21
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- PDP-11
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PREFACE

AUDIENCE

This document is intended for two specific types of user. Firstly, the engineer or technician who wants to configure and install the SBC M70 single board computer. Secondly, the programmer who wants to write applications software for the module. An overview of the architecture is given, but the document is not intended as a tutorial on PDP-11's.

ORGANISATION

Configuration, programming and installation details are divided among the chapters as follows:

CHAPTER 1: PRODUCT OVERVIEW
Chapter 1 describes the main functions and features of the SBC M70.

CHAPTER 2: SPECIFICATIONS
Chapter 2 gives a quantitative description of the features of the SBC M70.

CHAPTER 3: UNPACKING AND CONFIGURATION
Chapter 3 outlines the steps a user must follow in order to successfully unpack and configure the module.

CHAPTER 4: INSTALLATION
Chapter 4 explains how the SBC M70 is installed assuming it has been configured as required.

CHAPTER 5: SYSTEM ARCHITECTURE
Chapter 5 gives an overview of the architecture of the SBC M70 module. It describes how the PDP-11 architecture is implemented on the SBC M70.

CHAPTER 6: SERIAL I/O
Chapter 6 details the architecture, programming and cables of the serial-line sub-system.

APPENDIX A: BACKPLANE PIN UTILISATION
Appendix A lists the Q-Bus signals and indicates their positions on the module.

APPENDIX B: DIAGNOSTICS & PRODUCTION TESTS
Appendix B describes a selection of diagnostic programs which may be used to verify the operation of the SBC M70.

APPENDIX C: OP CODES & TRAPS
Appendix C contains a list of PDP-11 OP Codes.

APPENDIX D: I/O PAGE MEMORY MAP
Appendix D contains a memory map of the I/O page for the SBC M70.

APPENDIX E: DEVICE MNEMONICS
Appendix E contains the device mnemonics as used in the boot prompts.

RELATED DOCUMENTS

The following Digital Equipment Corporation publications provide additional information on DEC PDP-11.

DCJ11 User Guide
Micro PDP-11 Hand Book
Micro PDP-11 Interface Hand Book

CHAPTER 1

PRODUCT OVERVIEW

1 PRODUCT OVERVIEW

1.1 INTRODUCTION

The SBC M70 is a complete computer on a quad height card. It is Q-BUS compatible and supports the full PDP-11 instruction set (including floating point instructions). The board contains up to 2 Mb of DRAM incorporating error checking and correction. The module also contains EPROM memory space for boot code, four serial lines and a selection of real time clocks. This chapter gives an outline description of the main hardware elements of the module.

The positions of the main hardware components on the SBC M70 module are shown in figure 1.1. Figure 1.2 is a schematic which indicates how the main elements of the architecture interact.

1.2 PROCESSOR

The processor for the module is the DEC DCJ11. This 60 pin VLSI microprocessor provides the full PDP 11/70 instruction set, including floating point instructions. An integral memory-management unit maps a sixteen bit virtual address into an addressing space of 4 Mb. The processor can operate in three modes: Kernel, User and Supervisor, allowing protection to be implemented in a multi-user environment. The virtual addressing space can be doubled by enabling the Instruction/Data Space mode of operation. In this case instructions and data are mapped to different parts of physical memory. The DCJ11 has a multi-level interrupt and trap structure with four external interrupts. It also supports DMA arbitration and a cache memory system.

Chapter 6 gives further information on the DCJ11.

1.3 MEMORY

Three types of SBC M70 are available, containing 1/2, 1 or 2 Mb of DRAM, controlled by the INTEL 8207 Advanced Dynamic RAM Controller. Extra memory space holds six bits of error checking information for each sixteen bit data word. Error checking and correction is supervised by the INTEL 8206 Error Detection and Correction Unit. This unit can correct all single bit errors and can detect double bit errors as well as most other multi-bit errors.

The last 4k words of physical memory are reserved for system registers and external device CSRs. This area is referred to as the I/O page.

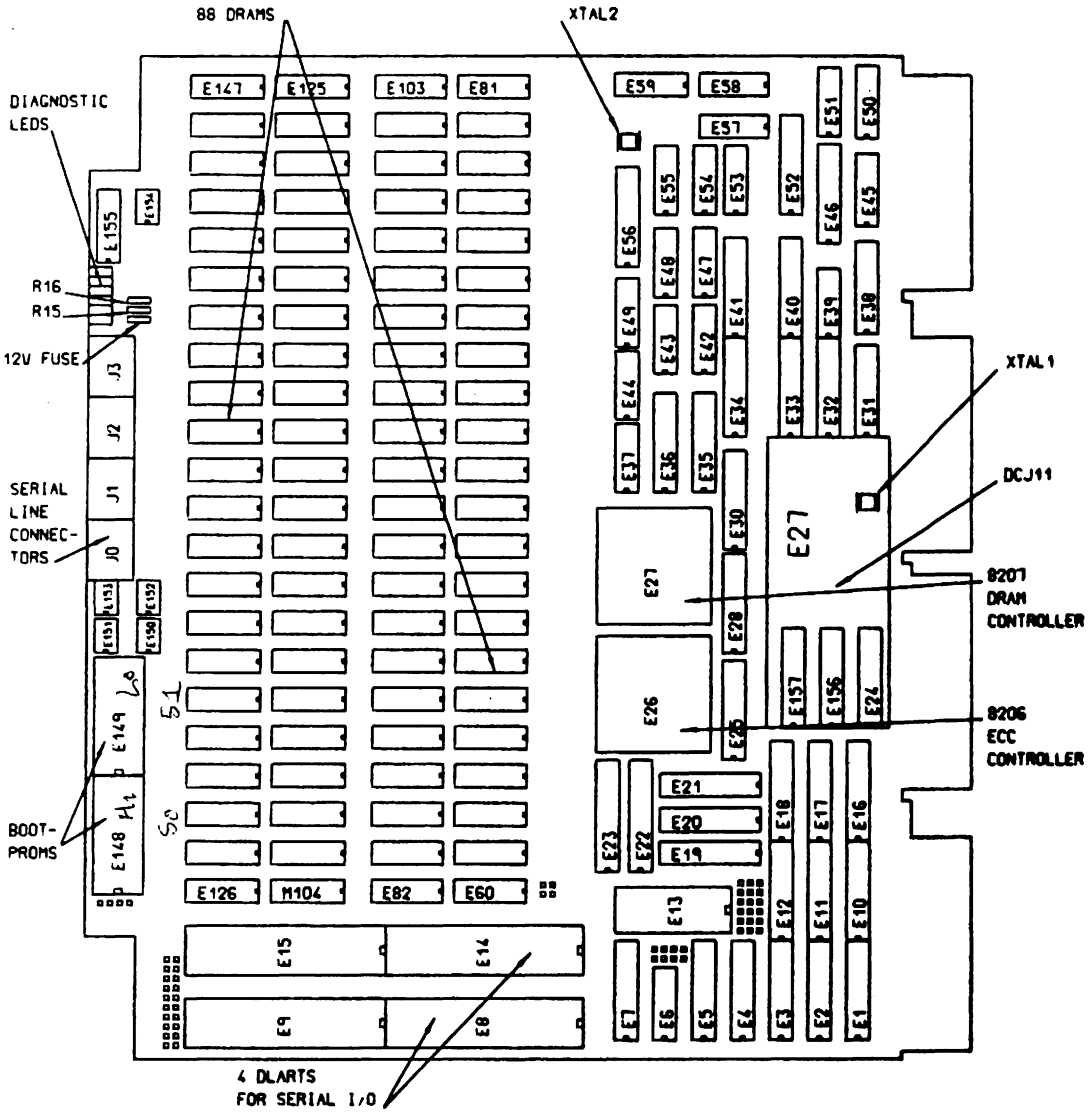

Fig. 1.1 SBC M70 Module (Rev. E)

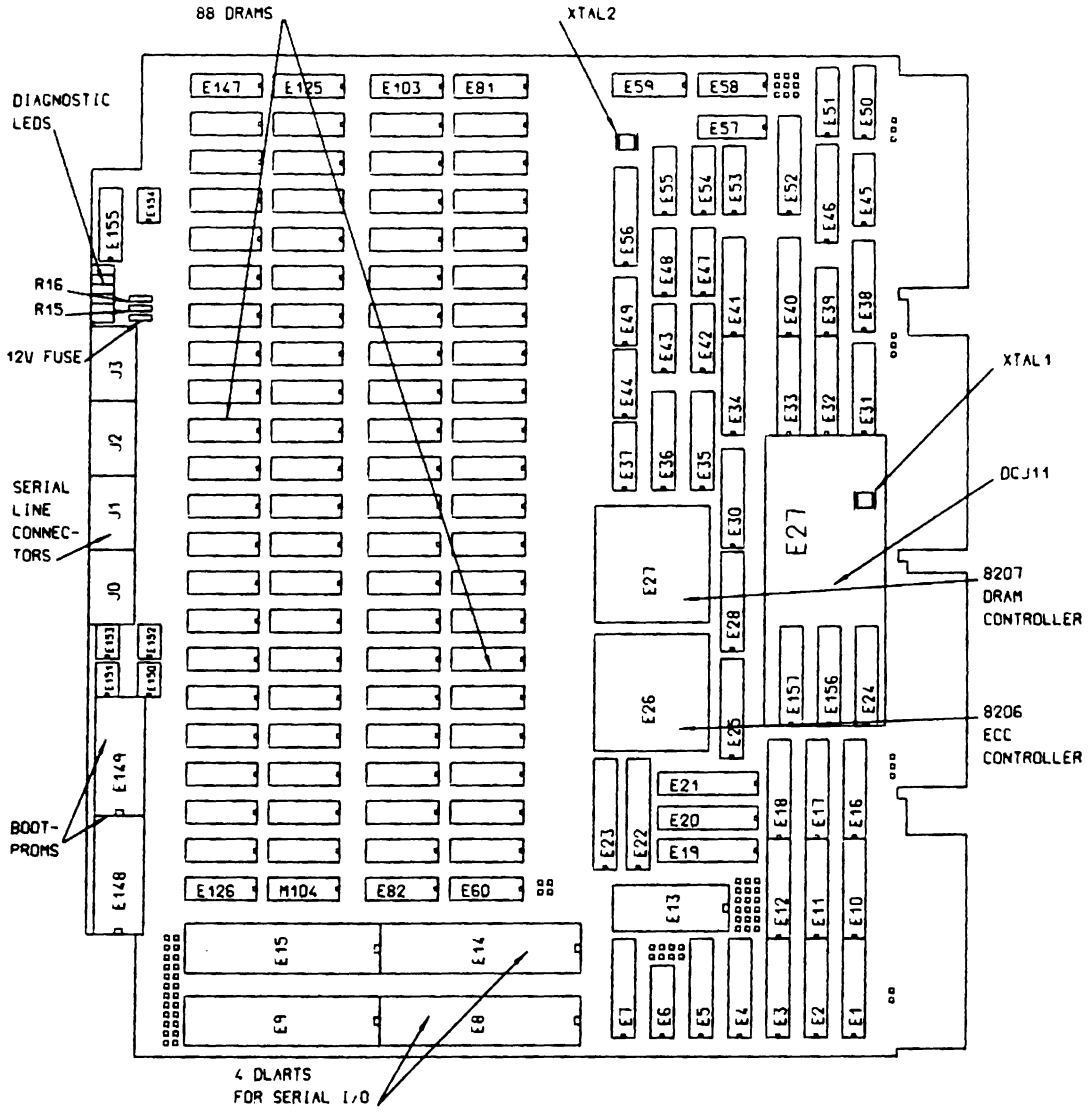

Fig. 1.1 SBC M70 Module (Rev. F).

Main memory on the SBC M70 is designed to operate as cache for most memory accesses. This leads to a very high performance for the module.

1.4 LSI-11 BUS INTERFACE

The SBC M70 interfaces to the LSI-11 bus (Q-Bus). This allows it to be installed in a standard Q-Bus backplane and to communicate with a wide range of Q-Bus modules. These include peripheral device controllers and offboard memory (Refer to the Micro PDP-11 Interface Handbook). The bus specification defines 22 multiplexed data/address lines and a variety of handshaking and control lines. Appendix A lists the Q-Bus signals and indicates their positions on the SBC M70 edge connector.

1.5 SERIAL LINES

The SBC M70 has 4 serial line units (SLU 0-3), implemented using four DEC DLART DC319-AA chips. A user connects to each one by means of a 2x5 pin AMP female connector.

The serial line sub-system has the following features:

a). Each serial line unit presents four registers to the programmer. Each unit also provides two vectored interrupts which can be enabled or disabled.

b). Each SLU is configured to comply with either of the following Electronics Industries Association standards: RS-232C; RS-423A.

c). The baud rate of each SLU is user configurable by wire-wrapping.

d). SLU3 may be enabled or disabled as a console by means of wire-wraps.

e). The system considers the four serial line units as a group. The base address of the sixteen registers associated with the group may be decided from a number of options.

f). The base vector of the eight interrupt vectors associated with the group is also configurable within certain limits.

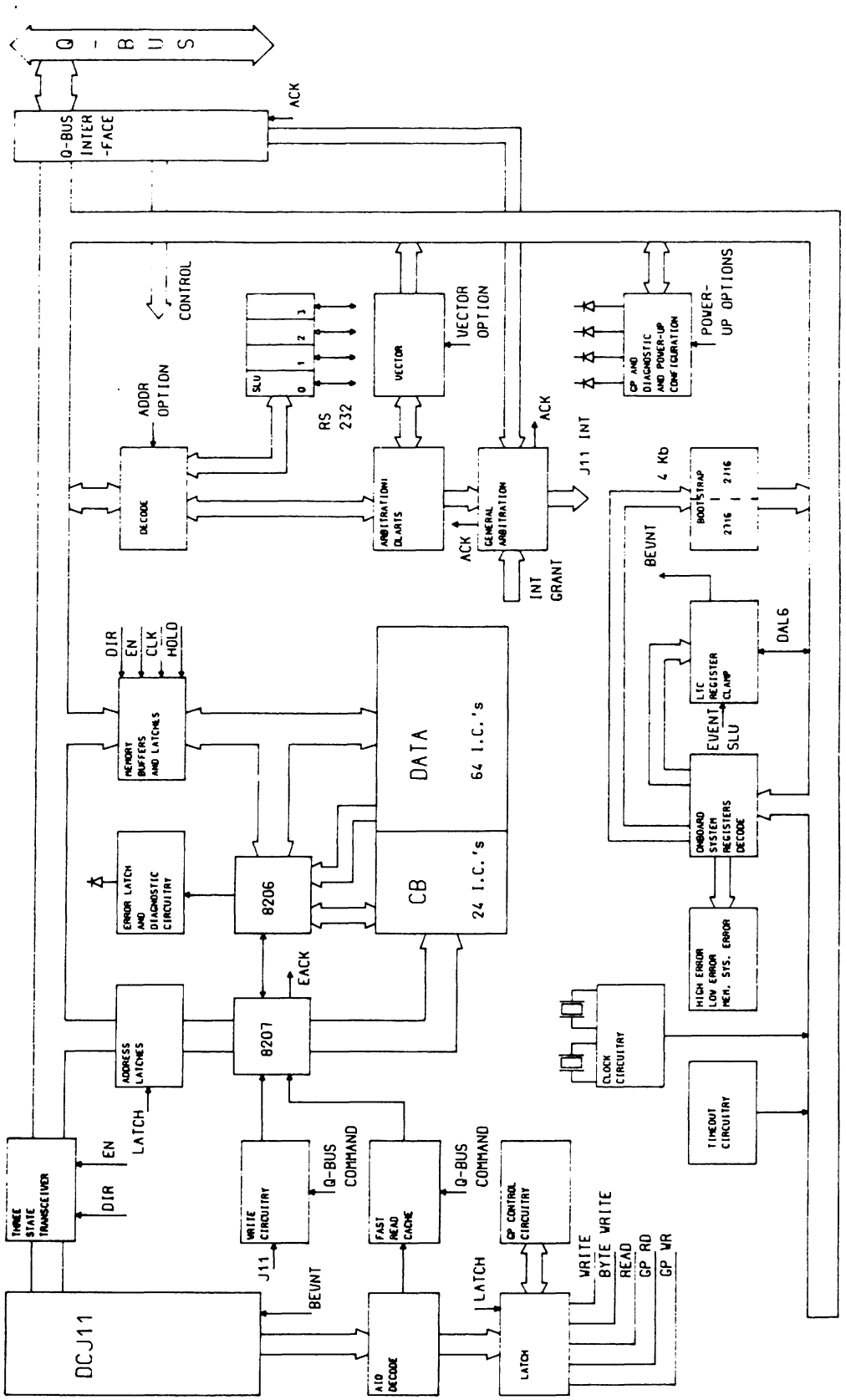

Fig. 1.2 SBC M70 Schematic.

g). The slewing rate of data transmission may be varied by means of user-installed resistors. Two resistors are shared between the four serial line units. Additional information on the Serial Lines can be obtained in chapters 3 and 6.

1.6 CLOCKS

Four clock signals are available on wire-wrap pins on the SBC M70. Three of these have frequencies of 50 Hz, 60 Hz and 800 Hz respectively. The fourth has a frequency sixteen times the SLU0 baud rate. The BEVNT signal from the bus is also available on a wire-wrap pin. Any of these may be wrapped to the EVENT pin of the DCJ11 which uses it as a line-time clock or real-time clock. The line-time clock function can be inhibited under program control. Refer to chapter 5 for further details.

1.7 BOOTSTRAPS

The SBC M70 contains 4 Kb of EPROM (2x2716 EPROMs) which contain bootstrap code. This space is divided into four windows, each 1 Kb in length. Only one window is accessible at any particular time; the choice is made by wire-wrapping. Alternatively the onboard bootstrap can be disabled entirely, allowing offboard bootstrap code to be used. Chapter 3 gives details on configuring the windows and enabling/disabling the onboard bootstraps.

1.8 LED DISPLAY

Six LEDs are provided on the SBC M70 module as a trouble-shooting facility. Details of the LEDs are given in chapter 4.

1.9 BATTERY BACKUP

Boards of Rev. F and higer are configurable for battery backup.

CHAPTER 2

SPECIFICATIONS

2 SPECIFICATIONS

2.1 PHYSICAL

Height 12 mm (0.5")
Length 228 mm (8.9")
Width 264 mm (10.4")
Weight 750 grms

2.2 POWER REQUIREMENTS

Power Supply:

The following power specifications apply to all versions of the SBC M70 module ie. 1/2, 1 and 2 Mb.

+5.0V +/- 5%	4.0 A Typical
	4.5 A Max
12.0V +/- 5%	100 mA Typical
	150 mA Max

2.3 ENVIRONMENTAL

Temperature:

Storage :- -10 to 60 deg C (14 to 140 deg F)
Operating:- 0 to 55 deg C (32 to 130 deg F)

NOTE:- The module must be brought into the operating temperature environment and allowed to stabilise before operating.

NOTE:- Derate the maximum operating temperature by 1 deg C (1.8 deg F) for each 300m (1000 ft) of altitude above 2.4 km (8000 ft).

Relative Humidity:

Storage :- 10% to 90% (no condensation)
Operating:- 10% to 90% (no condensation)

Altitude:

Storage :- Up to 7.5 km (25,000 ft)
Operating:- Up to 7.5 km (25,000 ft).

(i.e. the board needs a minimum pressure of 90 mm. of mercury).

2.4 AIRFLOW

Air must be non-caustic.

Operating:- Adequate airflow must be provided to limit the inlet to outlet temperature rise across the module to 5 deg C (40 deg F) when the inlet temperature is 35 deg C (95 deg F).

NOTE:- These are design limits. Lower temperature limits will serve to increase the life of the product.

2.5 INTERFACE CHARACTERISTICS

Bus:

LSI-11 BUS (Refer to Appendix A).

Serial Lines:

4 x RS-232C/RS-423A
compatible serial line units.

2.6 CONNECTORS AND CABLES:

Connectors:

J0 to J3:- AMP 2x5 pin male.

Cables:

RS232 Null Modem:- DEC BC20N-05 [2x5 pin AMP female to RS-232C female (25-way Cannon D-type)]. (Rev. F only).

CHAPTER 3

UNPACKING & CONFIGURATION

3 UNPACKING AND CONFIGURATION

3.1 INTRODUCTION

This chapter explains how to unpack the SBC M70 and how to configure it for use once it is unpacked. Configuration mainly consists of wire-wrapping. It is advisable to leave the module in the factory configuration until its operation has been verified.

3.2 UNPACKING

The following four steps outline how the SBC M70 should be unpacked. (If there is visible damage to the shipping carton then the module should be unpacked in the presence of the delivering carriers agent).

1). Lay the shipping carton on a flat surface and open out the flap.

2). Ensure that an anti-static wrist-strap is being worn.

3). Remove the module from the anti-static bubble-wrap. Allow a moment for any static to leak away to ground and then remove the module from the anti-static bag.

4). Inspect the module for damage. If none is found then move on to section 3.3.

If the module is damaged then no installation or repair should be undertaken. If the delivering carriers agent was not present during the unpacking then an insurance inspection claim should be called for. If the board is to be repaired then it should be returned to the distributor.

WARNING

Static electricity can damage components on the SBC M70. Proper precautions should be taken during any operation which involves handling the board.

3.3 SELECTING OPERATIONAL FEATURES

The module has fifty-four (Rev. E or lower) or seventy-four (Rev. F or higher) wire-wrap pins with which the user configures the module for the different operating modes. This is achieved by either installing or removing jumper wires between the wire-wrap pins. The locations and identification numbers of the wire-wrap pins are illustrated in figure 3.1 (figure 3.2(a) for Rev. F and higher). Table 3-1 gives the name of the signal on each wire-wrap pin.

The selectable features are power-up mode, starting address, halt option, serial line addresses, serial line interrupt, serial line baud rates, console configuration, bootstrap software and line-time clock. On boards of Rev. F and higher battery backup and length of time to timeout are configurable.

The slew rate of serial data transmission is also selectable on all versions of the SBC M70, but this is achieved by resistor insertion rather than by wire-wrapping.

Most of the signals appearing on the pins must be configured as logical HI or LO. This is achieved by tying them to +3Vdc or GND, respectively, within each main wire-wrap group. Connections may be made by daisy-chaining to avoid multiple wrappings of the HI and LO pins. HI and LO wirewraps are colour coded at the factory using blue and black wire respectively.

The exceptions to this procedure are the HALT input to the DCJ11, the EVENT input to the DCJ11, the battery backup option and the timeout option. Each of these must be fed from one of a number of options chosen by wire-wrapping.

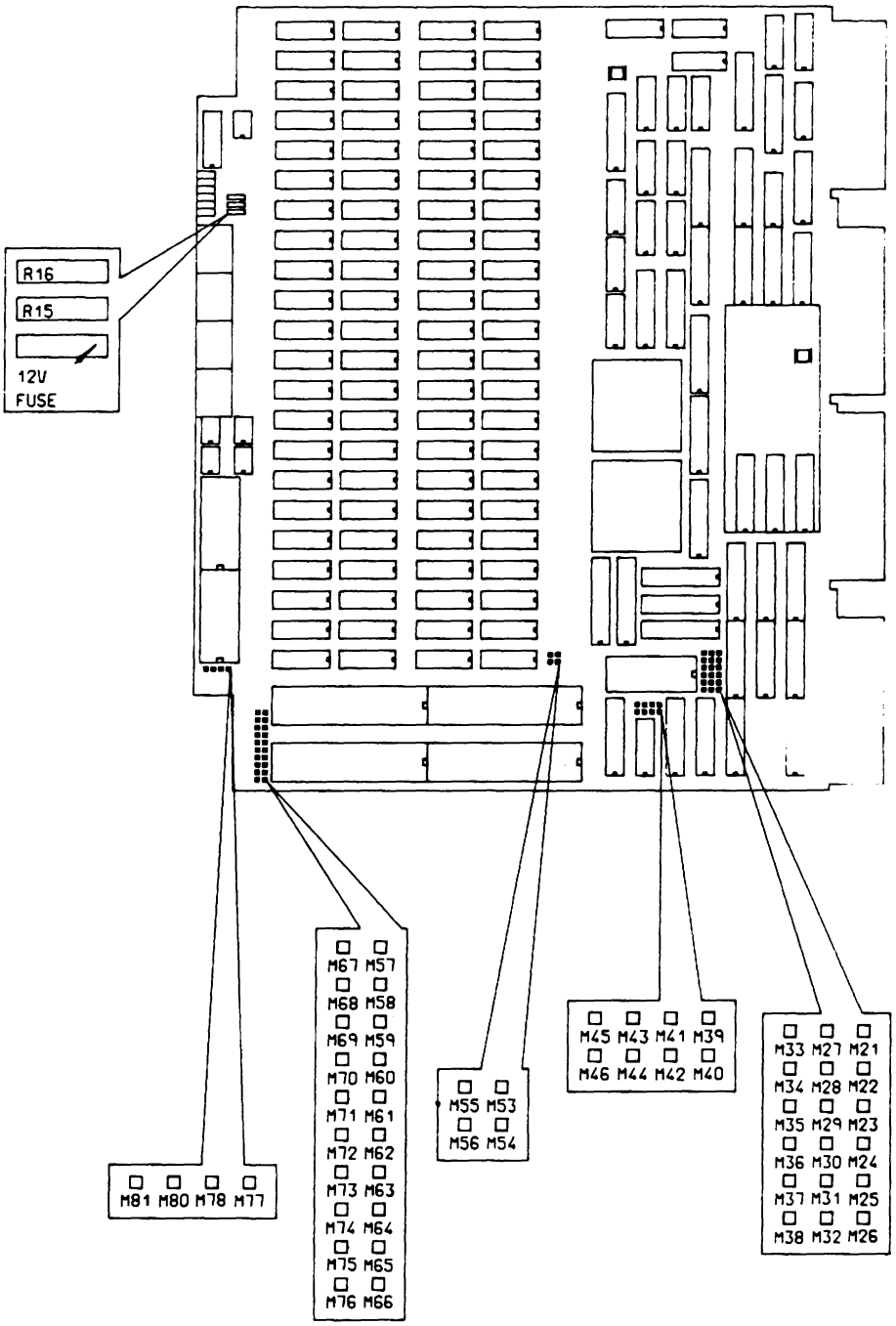

Fig. 3.1. Location of Wire-Wrap Banks.
(Rev. E and lower).

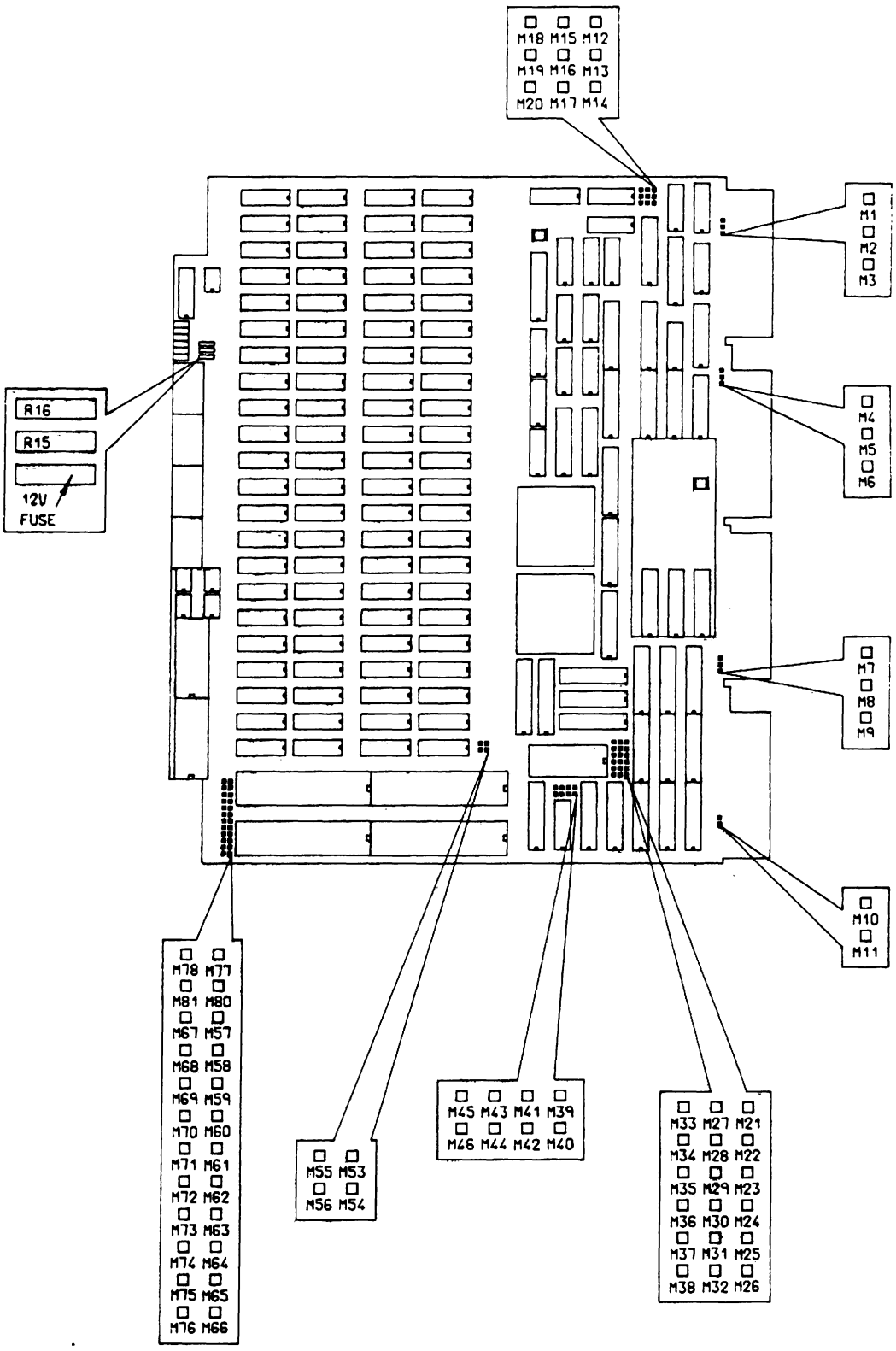

Fig. 3.2(a). Location of Wire-Wrap Banks.
(Rev. F and higher).

TABLE 3-1 CONFIGURATION PIN DEFINITIONS *

Pin	Description
M1	+5Vdc power from bus (AA2)
M2	Onboard +5Vdc power
M3	+5Vdc battery power from bus (AS1)
M4	+5Vdc power from bus (BA2)
M5	Onboard +5Vdc power
M6	+5Vdc battery power from bus (AV1)
M7	+5Vdc power from bus (CA2)
M8	Onboard +5Vdc power
M9	+5Vdc battery power from bus (CV1)
M10	Onboard +5Vdc power
M11	+5Vdc power from bus (DV1)
M12	+12Vdc power from bus (AD2)
M13	Onboard +12Vdc power
M14	+12Vdc battery power from bus (BS1)
M15	1Mb Memory Configuration
M16	Memory Configuration
M17	1/2-2Mb Memory Configuration
M18	12.5 us. Timeout
M19	Timeout Configuration
M20	25 us. Timeout

* Pins M1 to M20 Rev. F only.

TABLE 3-1 Contd. CONFIGURATION PIN DEFINITIONS

Pin	Description
M21	Power-up bit 2
M22	Power-up bit 3
M23	Power-up bit 13
M24	HI logic level (+5Vdc via pullup)
M25	System GND
M26	Serial Lines Vector bit 6
M27	Power-up bit 1
M28	Power-up bit 10
M29	Power-up bit 12
M30	Power-up bit 15
M31	CE Console Enable (17777560)
M32	Serial Lines Address Decode Bit 07
M33	Power-up bit 08
M34	Power-up bit 09
M35	Power-up bit 11
M36	Power-up bit 14
M37	Serial Lines Vector bit 7
M38	Serial Lines Address Decode bit 08
M39	Serial Lines Address Decode bit 05
M40	Serial Lines Address Decode bit 10
M41	Serial Lines Address Decode bit 06
M42	Serial Lines Address Decode bit 11
M43	No Connection
M44	Serial Lines Address Decode bit 09
M45	On-board Boot PROM Enable
M46	Serial Line Vector bit 5
M53	HI logic level (+5Vdc via pullup)
M54	Break detect from SLU3
M55	System GND
M56	DHALT Asserts HALT on DCJ11

TABLE 3-1 Contd. CONFIGURATION PIN DEFINITIONS

Pin	Description
M57	16 times SLU0 baud rate.
M58	800 Hz Line Time Clock 1.25 mS
M59	BEVNT Real Time Clock from the Bus
M60	SLU0 Baud rate select bit 1
M61	SLU3 Baud rate select bit 1
M62	SLU3 Baud rate select bit 2
M63	System GND
M64	SLU1 Baud rate select bit 0
M65	SLU1 Baud rate select bit 2
M66	SLU2 Baud rate select bit 2
M67	50 Hz Line Time Clock 20mS
M68	60 Hz Line Time Clock 16.66mS
M69	EVENT signal to J11 for LTC
M70	SLU0 Baud rate select bit 0
M71	SLU0 Baud rate select bit 2
M72	SLU3 Baud rate select bit 0
M73	HI logic level (+3Vdc via pullup)
M74	SLU1 Baud rate select bit 1
M75	SLU2 Baud rate select bit 0
M76	SLU2 Baud rate select bit 1
M77	System GND
M78	HI logic level (+5Vdc via pullup)
M80	BS1 Bootstrap Prom Window Select Bit 1
M81	BS0 Bootstrap Prom Window Select Bit 2

Link ~~80~~ 78 & 81 for M/B
M77 & 80 M720 program

3.3.1 Power-up Configuration Register

On power-up the DCJ11 reads a register known as the power-up configuration register. Some of the bits in this register may be set to HI or LO logic values by wire-wrapping. The power-up register determines the power-up mode and the boot address. Figure 3.2 shows the layout of the power-up configuration register. The bits in the register are explained in detail in table 3-2. Table 3-2 also indicates the bits which are configurable. These are all available in wire-wrap bank M21-M38. (Refer to figure 3.3). The location of this bank on the SBC M70 module is given in figure 3.1.

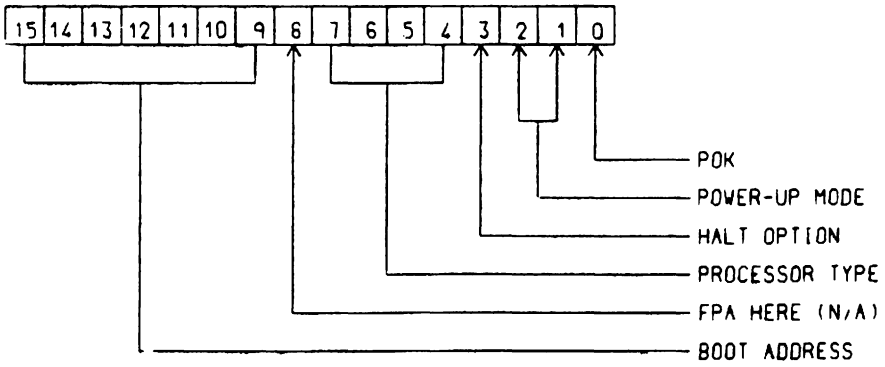

Fig. 3.2 Power-Up Register.

M33 P. up bit 8	M27 P. up bit 1	M21 P. up bit 2
M34 P. up bit 9	M28 P. up bit 10	M22 P. up bit 3
M35 P. up bit 11	M29 P. up bit 12	M23 P. up bit 13
M36 P. up bit 14	M30 P. up bit 15	M24 +3Vdc
M37 SLU vector bit 7	M31 Console enable	M25 System GND
M38 SLU addr. bit 8	M32 SLU addr. bit 7	M26 SLU vector bit 6

Fig. 3.3 Wire-Wrap Bank M21-M38.

TABLE 3-2 POWER-UP CONFIGURATION REGISTER

Bit(s)	Name	Wire-Wrappable	Description
<15:9>	Boot Address	yes	These represent bits 15-09 of the boot address. They are tied HI or LO as required. Bits 08-00 of the boot address are always 0. Note that bits <2:1> of the register must both be tied HI for this feature to be active (Refer to warning).
8	FPA Here	yes	The bit is set to a 1 when a floating point accelerator is present. Since the SBC M70 does not support this option the bit must be read as 0.
7	Reserved	no	Reserved for future use.
<6:4>	-	no	Processor Type - Bits read 1.
3	HALT Option	yes	The DCJ11 has two ways of responding to a HALT instruction. If this bit is set to 1 it traps through location 4 and sets bit 7 of the CPU error register. If 0 it enters console ODT.
<2:1>	Power-up Mode	yes	The DCJ11 reads these bits to determine how it will power-up. The power-up modes are as follows: Bits Mode 2 1 0 0 Trap through location 24. 0 1 Enter Console ODT. 1 0 Power-up to 17773000(8). 1 1 Power-up to the user-defined address specified by bits <15:9>.
0	POK	no	This bit is not configurable by the user. Onboard logic asserts it to notify the DCJ11 that system power is at an acceptable level.

WARNING

If bits <15:9> are to be used as part of the boot address then bit 9 must be tied LO if DEC operating systems are to be used.

3.3.2 Serial Line Address Selection

The serial line sub-system considered as a group has sixteen registers associated with it - four for each serial line, as follows:

Receive Control/Status Register (RCSR)

Receive Buffer (RBUF)

Transmit Control/Status Register (XCSR)

Transmit Buffer (XBUF)

Chapter 6 describes these registers in detail.

The address of the RCSR on SLU0 is the base address for the serial line sub-system. The remaining device registers are addressable as the 15 subsequent words of memory. The bits [5,11] of the base address are variable. Each of these 8 bits can be made HI or LO by connecting the relevant 'Serial Line Address bit' to +3Vdc or to GND respectively. The relevant pins are available in two wire-wrap banks: M21-M38 and M39-M46. (Refer to figures 3.3 and 3.5 respectively). The locations of these banks on the SBC M70 module are given in figure 3.1. Figure 3.4 shows what the serial line address bits represent.

An exception to this procedure is when SLU3 is selected as console by tying M31 HI. In this case its RCSR must be 17777560 with its other three registers following contiguously. Note that the SLU0 RCSR address will still be the base address of the other twelve registers and is configurable as before. Table 3-3 shows the complete factory configuration. (Note that SLU3 is configured as a console).

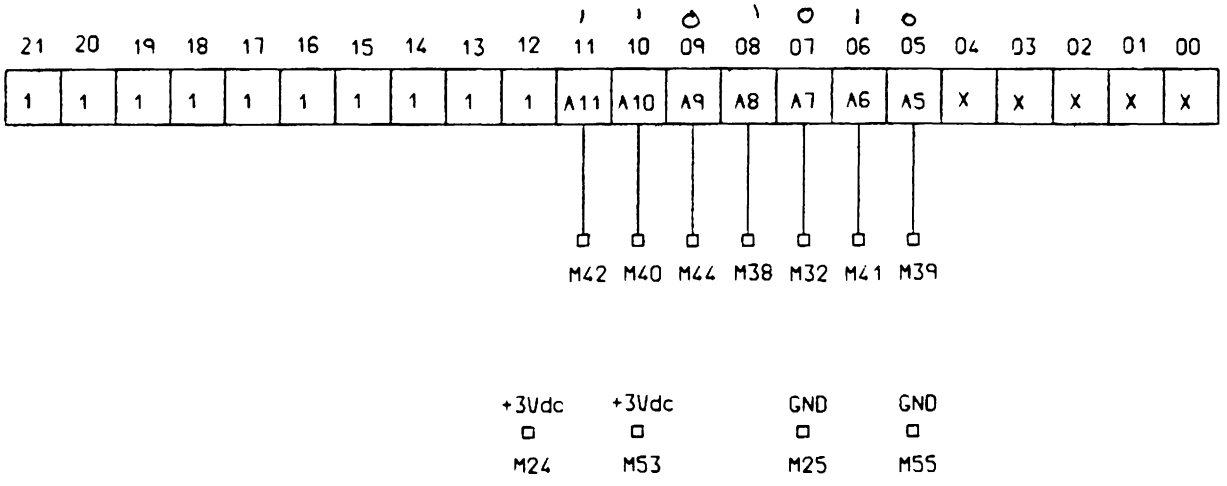

Fig. 3.4 Serial Line Address Selection.

TABLE 3-3 SERIAL LINE FACTORY ADDRESSES

Address	Register	Vector*	Channel
17776500	RCSR		
17776502	RBUF	300	
17776504	XCSR		Channel 0
17776506	XBUF	304	
17776510	RCSR		
17776512	RBUF	310	
17776514	XCSR		Channel 1
17776516	XBUF	314	
17776520	RCSR		
17776522	RBUF	320	
17776524	XCSR		Channel 2
17776526	XBUF	324	
17777560	RCSR		
17777562	RBUF	60	
17777564	XCSR		Channel 3
17777566	XBUF	64	

* See section 3.3.3 for information on vectors, SLU3 configured as console.

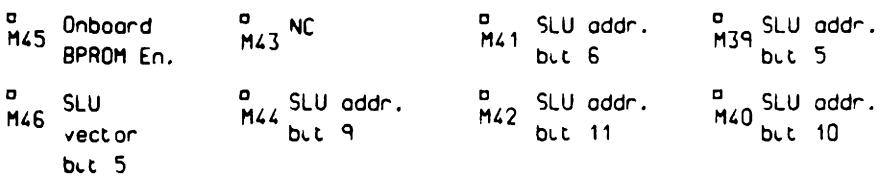

Fig. 3.5 Wire-Wrap Bank M39-M46.

3.3.3 Serial Line Vector Selection

Each SLU has two vectored interrupts which may be enabled under program control:

1). When it has received a full byte of data.

2). When it is ready to transmit a byte.

Each vector is two words in length, and so sixteen byte locations must be provided in memory. The address of the vector for the SLU0 receive interrupt is chosen as the base address. The other seven locations follow contiguously. Bits [5,7] of the base address can be chosen as logical HI or LO by tying the respective wire-wraps to +3Vdc or ground. The three relevant wire-wrap pins M37, M26 and M46 are available in bank M21-M38 and bank M39-M46 (Refer to figures 3.3 and 3.5). Figure 3.1 gives the location of these banks on the SBC M70 module.

The configuration with SLU3 selected as console is an exception to this procedure. With this setup the vectors for SLU3 are restricted to 60 and 64. The other six vectors remain configurable as before. Fig. 3.6 shows what the wire-wrap pins represent. Table 3-3 shows the complete factory configuration with console selected.

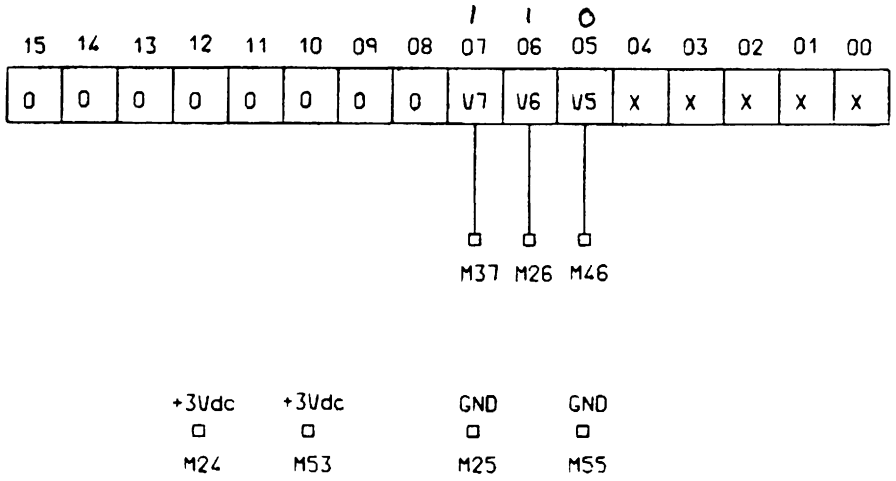

Fig. 3.6 Serial Line Vector Selection.

3.3.4 Console Configuration

SLU3 may be enabled as a console by tying wire-wrap pin M31 HI in wire-wrap bank M21-M38 (Refer to figure 3.3). Table 3-4 summarises enabling and disabling of the console. The addresses of the SLU3 registers with SLU3 selected as console are indicated in table 3-3.

TABLE 3-4 CONSOLE CONFIGURATION

Disable	Enable
M31 to M25	M31 to M24

3.3.5 Break Configuration

BRK IRQ (pin 33) on a DLART is asserted HI each time a break signal is detected by that DLART. This happens when the break key on a terminal or teletype is pressed. BRK IRQ from SLU3 is available on wire-wrap pin M54. It may be connected to M56 which goes to the HALT line for the DCJ11. Thus a break from a terminal connected to SLU3 would cause the processor to halt. Figure 3.8 shows wire-wrap bank M53-M56. Table 3-5 summarises HALT enable and disable.

TABLE 3-5 BREAK CONFIGURATION

Disable HALT	HALT on BREAK
M56 to M55	M54 to M56

3.3.6 Baud Rates

Each SLU channel speed can be chosen from a selection of baud rates in the range 300 to 38,400 bits per second. This is achieved by means of 3 input pins on each DLART (pins 31,37,38). The twelve baud rate select inputs are all available on wire-wrap pins in the bank M57-M76 (Refer to figure 3.7). They are M60, M61, M62, M64, M65, M66, M70, M71, M72, M74, M75 and M76. The location of the wire-wrap bank on the SBC M70 module is given in figure 3.1. Both the transmitter and receiver for a given channel must operate at the same baud rate; split baud rate operation can not be configured.

The baud rates are configured by determining the 3-bit code for the required baud rate and installing a jumper between GND and the baud-rate pins requiring a logic LO. The baud rate select pins are tied high internally so only the LO pins need to be wrapped. Table 3-6 lists the baud rate select codes.

M67	50 Hz LTC	M57	16 X SLU0 BAUD RATE
M68	60 Hz LTC	M58	800 Hz LTC
M69	EVENT t/p to J11	M59	BEVNT LTC from bus
M70	SLU0 brs bit 0	M60	SLU0 brs bit 1
M71	SLU0 brs bit 2	M61	SLU3 brs bit 1
M72	SLU3 brs bit 0	M62	SLU3 brs bit 2
M73	+3Vdc	M63	GND
M74	SLU1 brs bit 1	M64	SLU1 brs bit 0
M75	SLU2 brs bit 0	M65	SLU1 brs bit 2
M76	SLU2 brs bit 1	M66	SLU2 brs bit 2

Fig. 3.7 Wire-Wrap Bank M57-M76.

TABLE 3-6 BAUD RATE SELECT CODES

SLUX			Baud Rate
BRS2	BRS1	BRS0	
H	H	H	300
H	H	L	600
H	L	H	1200
H	L	L	2400
L	H	H	4800
L	H	L	9600
L	L	H	19200
L	L	L	38400

L = Logic Zero --> Install jumper between baud rate select pin and GND.

H = Logic One --> Pulled to HI logic level internally.

X = Serial Line Unit number 0,1,2,3

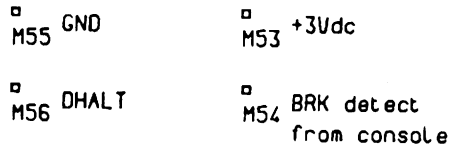

Fig. 3.8 Wire-Wrap Bank M53-M56.

3.3.7 Slew Rate Resistors

The slew rate resistors are represented on the SBC M70 schematic as R15 for SLU0 and SLU1 and R16 for SLU2 and SLU3. These resistors connect between the wave-shape terminals of the 9636 ICs and ground. The wave of the output signal is shaped in accordance with data rate and wire length to control reflections and cross-talk. This facility provides compliance with the RS-423A specification and is also advisable when RS-232C is being used. The resistor values should be chosen in accordance with table 3-6. Figure 3.1 shows the location of the resistors on the SBC M70 module.

TABLE 3-7 EIA RS-232C SLEW RATE RESISTOR VALUES

Baud Rate	Value of resistor R15 and R16
38,400	22k
19,200	51k
9,600	120k *
4,800	200k
2,400	430k
1,200	820k
600	1M
300	1M

* --> Factory installed value

3.3.8 Bootstrap Configuration

The SBC M70 provides 4 Kb of EPROM space for boot code. 1 Kb of this can be enabled at any one time. Each 1 Kb area is known as a window and wire-wraps are used to select between the windows. The relevant pins are M77, M78, M80 and M81 (Refer to figure 3.9). Table 3-8 shows the connections required to select individual windows and indicates the devices bootable through the factory-supplied boot PROMs. Figure 3.9 illustrates the relevant wire-wrap bank. Chapter 5 gives further information about the location of the boot PROMs in the PDP-11 addresssing space. Appendix E gives the meanings of the device mnemonics.

Pin 45 must be tied LO to enable onboard boot PROMs. They can be disabled by tying pin 45 HI. This will allow the use of another bootstrap program, such as the MXV11-B2 PROM pair in a MRV11-D. Pin 45 is in bank M39-M46 (Refer to figure 3.5).

Fig. 3.9 Wire-Wrap Bank M78-M81.

TABLE 3-8 BOOTSTRAP WIRE-WRAP CONFIGURATION

Connect	Window	Factory Bootstraps *
M81 and M80 to M77	0	DX DY DL DU DM DB MS MT
M81 to M78 and M80 to M77	1	VM DL DU DD MU
M81 to M77 and M80 to M78	2	DX DY DD VM DM DB
M81 and M80 to M78	3	UNUSED

* M7-50C, M7-51C BootPROMS only.

3.3.9 Clock Configuration

Pin 8 of the DCJ11 is the EVENT input. A low-going edge to this pin will cause the processor to trap to location 100. The input is available to the user as wire-wrap pin M69. (Refer to figure 3.7). It is usually driven by a clock, five of which are available in wire-wrap bank M57-M76 (See figure 3.7).

WARNING

The line time clock function must be enabled under program control. Refer to Section 5.10.

3.3.10 Battery Backup Configuration (REV. F and higher)

The LSI-11 bus specification provides for the possibility of battery backup. Normal power and the battery backup power are both taken onto the SBC M70 module from the contact fingers and jumpers can be used to decide which set is to feed the board.

The wire-wrap pins for configuring 5 volt power are to be found in banks M1-M3, M4-M6, M7-M9 and M10-M11 (refer to figures 3.10 to 3.13). The wire-wrap pins for configuring 12 volt power are M12 to M14, found in bank M12-M20 (refer to figure 3.14). Table 3-9 indicates how jumpers should be placed to choose either normal or battery backup power.

Figure 3.1 shows the positions of all of these pins on the SBC M70 module. Table 3-1 gives the meanings of each pin. This table also indicates which bus contact fingers are connected to the wire-wrap pins which bring power on to the SBC M70.

TABLE 3-9 BATTERY BACKUP CONFIGURATION

Normal Power	Battery Backup Power
Jumpers Installed:	Jumpers Installed:
M1-M2	M2-M3
M4-M5	M5-M6
M7-M8	M8-M9
M10-M11	M13-M14
M12-M13	(NO JUMPER BETWEEN M10 and M11).

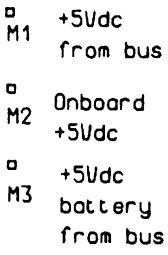

Fig. 3.10 Wire-Wrap Bank M1-M3

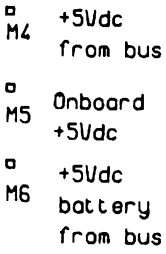

Fig. 3.11 Wire-Wrap Bank M4-M6

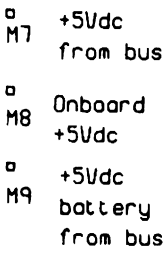

Fig. 3.12 Wire-Wrap Bank M7-M9

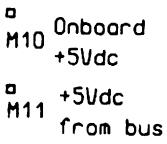

Fig. 3.13 Wire-Wrap Bank M10-M11

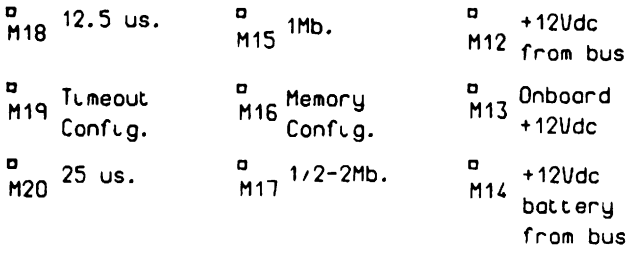

Fig. 3.14 Wire-Wrap Bank M12-M20

3.4 FACTORY CONFIGURATION

Table 3-12 shows the factory configuration for all revs. of the SBC M70 module. Pins M1 to M20 refer to rev. F only.

TABLE 3-12 STANDARD FACTORY CONFIGURATION

Pin	Signal Mnemonic	Function	Remarks
M1	M70AA2	Normal Power (not battery)	Jumper to M2
M2	M705	" "	Jumper to M1
M3	M70AS1	" "	No jumper
M4	M70BA2	" "	Jumper to M5
M5	M705	" "	Jumper to M4
M6	M70AV1	" "	No Jumper
M7	M70CA2	" "	Jumper to M8
M8	M705	" "	Jumper to M7
M9	M70CV1	" "	No Jumper
M10	M705	" "	Jumper to M11
M11	M70DV1	" "	Jumper to M10
M12	M70AD2	" "	No Jumper
M13	M7012	" "	Jumper to M14
M14	M70BS1	" "	Jumper to M13
M15	MB1	" "	*
M16	M70MEM	" "	*
M17	MB2	" "	*
M18	T125	" "	No jumper
M19	M70T	" "	Jumper to M20
M20	T25	" "	Jumper to M19

* Dependent on Memory Size. Refer to section 3.3.12.

WARNING

All jumpers must be correctly installed for either battery backup power OR normal power. Incorrectly installed jumpers could lead to the SBC M70 acting as a power source for the LSI-11 bus with consequent damage to components.

3.3.11 Timeout Configuration (Rev. F and higher)

The SBC M70 will trap to location 4 if it tries to access a location which does not exist. The length of time before timeout can be chosen as 12.5 microseconds or 25 microseconds. Thus, even controllers which are relatively slow to respond may be accommodated.

Timeout configuration is achieved wire-wrapping. The relevant pins are M18, M19 and M20 (Refer to figure 3.14). Jumper placement is summarised in table 3-10.

TABLE 3-10 TIMEOUT CONFIGURATION

12.5 us.	25 us.
Jumper Installed	Jumper Installed:
M18-M19	M19-M20

3.3.12 Memory Size Configuration (Rev. F and higher)

The SBC M70 is available in three memory sizes. 1Mb. boards require forty-four RAM chips (two banks) and 1/2 or 2 Mb. boards require eighty-eight RAM chips (two banks). The relevant pins are M15, M16 and M17 (refer to figure 3.14). If the board has two banks of RAMs then the jumper should be placed M15 and M16. If it has four banks then the jumper should be between M16 and M17. The correct jumper positioning is summarised in table 3-11.

WARNING

Memory Size is configured at the factory. Configuration is not a user option.

TABLE 3-11 MEMORY SIZE CONFIGURATION

1Mb.	1/2-2Mb.
Jumper Installed:	Jumper Installed:
M15-M16	M16-M17

3.3.13 Backplane Pin Configuration

The SBC M70 is hard-wired to run in an ABAB backplane. BIAKI L (CM2) is connected to BIAKO L (CN2), and BDMGI L (CR2) is connected to BDMGO L (CS2). These connections may need to be cut if the board is to be used in an ABCD backplane. Care should be taken to ensure that no signals are interfered with, by any board using the CD backplane. The tracks are to be found near the relevant contact fingers. There are also holes which will accept links near these contact fingers for reconnection of above signals.

TABLE 3-12 Contd. STANDARD FACTORY CONFIGURATION

Pin	Signal Mnemonic	Logic Level	Function
M21	PU02	HI	AutoBoot on power-up to 173000
M22	PU03	LO	J11 halts on HALT instruction
M23	PU13	LO	Bit 13 of user boot address LO
M26	V6	HI	Vector bit 6 of Serial Lines
M27	PU01	LO	AutoBoot on power-up
M28	PU10	LO	Bit 10 of user boot address
M29	PU12	LO	Bit 12 of user boot address
M30	PU15	LO	Bit 15 of user boot address
M31	CE	HI	On-board console enabled
M32	A07	LO	Serial Line addr decode bit 07
M33	PU08	LO	Bit 08 FPA not available
M34	PU09	LO	Bit 09 of user boot address LO
M35	PU11	LO	Bit 11 of user boot address
M36	PU14	LO	Bit 14 of user boot address
M37	V7	HI	Vector bit 7 of Serial Lines
M38	A08	HI	Serial Lines addr decode bit 08
M39	A05	LO	Serial Lines address decode bit 05
M40	A10	HI	Serial Lines address decode bit 10
M41	A06	HI	Serial Lines address decode bit 06
M42	A11	HI	Serial Lines address decode bit 11
M43			Not connected
M44	A09	LO	Serial Lines address decode bit 09
M45	BPEN-	LO	On-board Boot Prom enabled
M46	V5	LO	Vector bit 5 of Serial Lines

TABLE 3-12 contd. STANDARD FACTORY CONFIGURATION

Pin	Signal Mnemonic	Logic Level	Function	Remarks
M54	HLT	N/A	Break Detect from SLU3	Connected to M56
M56	DHALT	N/A	DCJ11 Halt	Connected to M54
M70	SLU00	LO	SLU0 BRS bit 0 *	
M60	SLU01	HI	SLU0 BRS bit 1 *	Hi via internal p-up
M71	SLU02	LO	SLU0 BRS bit 2	
M64	SLU10	LO	SLU1 BRS bit 0	
M74	SLU11	HI	SLU1 BRS bit 1	Hi via internal p-up
M65	SLU12	LO	SLU1 BRS bit 2	
M75	SLU20	LO	SLU2 BRS bit 0	
M76	SLU21	HI	SLU2 BRS bit 1	Hi via internal p-up
M66	SLU22	LO	SLU2 BRS bit 2	
M72	SLU30	LO	SLU3 BRS bit 0	
M61	SLU31	HI	SLU3 BRS bit 1	Hi via internal p-up
M62	SLU32	LO	SLU3 BRS bit 2	
M67	CLK50	N/A	50Hz Onboard LTC	Connected to M69
M69	EVNT	N/A	J11 EVENT signal	Connected to M67
M80	BS1	LO	Select Window 0 of BOOTPROM	
M81	BS0	LO	Select Window 0 of BOOTPROM	

* BRS - baud rate select, p-up = pull-up.

NOTE:- All channels factory set for 9600 baud.

CHAPTER 4

INSTALLATION

4 INSTALLATION

4.1 INTRODUCTION

This chapter details the installation of the SBC M70. Bus connections and user connections are decribed. Full details of the LED display on the front of the module are also given since monitoring these is the first step in verifying the correct operation of the SBC M70 module.

4.2 BUS CONNECTIONS

The following should be verified before the module is installed in the backplane:

1). The backplane is a correct Q-Bus backplane.

2). +5Vdc and +12Vdc are available at the correct points on the backplane.

3). There is adequate power reserve for the SBC M70 and any other Q-Bus modules which are to be inserted in the backplane.

4). The backplane is adequately cooled.

5). The board is configured as required. It is advisable to leave the module in the factory configuration until it has been verified.

WARNING

It is inadvisable to remove a board from a powered backplane. This can cause damage to the module or other parts of the system. The board should also be correctly configured for battery backup power OR normal power. See section 3.3.10.

The SBC M70 may now be installed as follows.

1). Place the SBC M70 in the backplane along with any other Q-Bus cards which are to be used. The SBC M70 should occupy the topmost slot. The other cards should be placed in such as way as to ensure interrupt continuity. The respective backplane documentation should give details. Section 3.3.13 details how to configure SBC M70 for an ABCD backplane.

2). Apply power to the backplane.

4.3 USER CONNECTION

Serial communication with the SBC M70 is by means of the four AMP ten-way connectors on the front of the module (Refer to figure 1.1). A suitable DEC cable is BC20N-05 (Rev. F and higher only, details for construction of a suitable cable are given in chapter 6).

For initial module verification a single cable should be connected to J3.

4.4 DIAGNOSTIC LED's AND POWER-UP

The LED display on the front of the module should be observed while the power is being switched on. Table 4-1 summarises LED details. Figure 4.1 shows the relative positions of the diagnostic LEDs on the SBC M70 module.

When power is applied, the bus signal BINIT-L is temporarily asserted LO and resets all the devices on the bus. Two further bus signals, BDCOK-H and BPOK-H, are then asserted HI. These signals indicate to the module that the correct DC power is available to it. The green LED relays this information to the user. The green LED should always be on when the SBC M70 module is operating.

BDCOK-H lights the three red diagnostic LEDs. The DCJ11 now runs some power-up diagnostics to test CPU, memory and console. There is a LED associated with each one and if a diagnostic test runs successfully then the respective LED is extinguished.

The yellow ECC memory LED switches on when multi-bit error has occurred in ECC RAM. Chapter 5 gives more details on ECC memory.

TABLE 4-1 LED DESCRIPTION

Led	Colour	Description
1	Yellow	ECC Memory Error. Set by bit 15 of the memory CSR under diagnostic control or by detection of a memory error during READ.
2	Red	CPU Test. Cleared on power-up if internal CPU diagnostic is passed.
3	Red	Memory Test. Cleared on power-up if internal memory test is passed.
4	Red	Console Test. Cleared on power-up if console is present.
5	Red	Processor in ODT. Set if processor is running console ODT.
6	Green	Power. Set if 5V dc power is present.

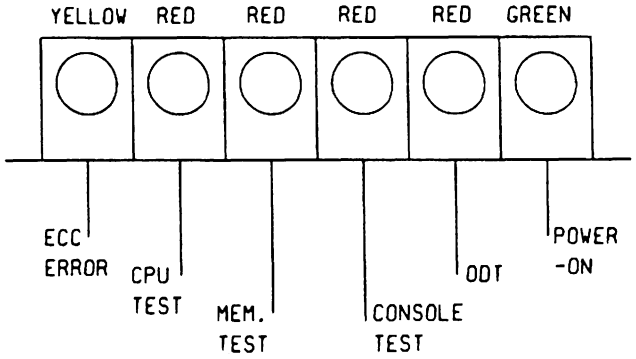

Fig. 4.1 LED Display.

4.5 BOOTING

The action taken by the DCJ11 at this point depends on the value of the power-up configuration register. Refer to section 3.3.1 for details.

In the factory configuration, program execution begins from location 17773000(8). This is the start of the onboard bootcode, which is also enabled in the factory configuration. A boot prompt, such as the following, is transmitted to the printer or terminal:

```
SBC M70-V01.02

DX DY DL DU DM DB MS MT

M70>
```

Any device listed in the prompt may now be booted.

NOTE:- Upper case should be entered.

It is also possible to disable onboard bootcode and to use bootcode held offboard, for example in the PROM of an MRV11-D. The module may also be configured to begin program execution at addresses other than 17773000(8). Another power-up mode allows the DCJ11 to power-up to console ODT (see chapter 6). In this mode the ODT LED would be on and the terminal or printer would display the @ prompt. Finally, the module can be configured so that the DCJ11 traps to location 24 on power-up. Chapter 5 gives further information on bootstraps.

CHAPTER 5

SYSTEM ARCHITECTURE

5 SYSTEM ARCHITECTURE

5.1 INTRODUCTION

This chapter describes the architecture of the SBC M70 with special reference to how the DCJ11 interfaces with other system components.

5.2 PROCESSOR MODES

There are three processor modes - Kernel, Supervisor and User. Each one has a different degree of control over the operation of the DCJ11. They are chosen by setting bits 14 and 15 in the Processor Status Word (PSW). The existence of different processor modes allows security to be implemented in a multi-programming environment. For example, WAIT, RESET and HALT statements can only be executed in Kernel mode. Certain bits in the PSW may only be written to in Kernel mode. (Refer to section 5.4.1.1). Thus, non-privileged users are kept from having too much control over the system. (Refer to Appendix E for a listing of device mnemonics and/or DEC documentation on the DCJ11 for explanation of instruction mnemonics).

5.3 GENERAL PURPOSE REGISTERS

The DCJ11 has sixteen general purpose registers. These registers do not reside in the addressing space. Twelve of the registers are true general purpose registers. These are arranged as two sets, R0 to R5 and R0' to R5'. Only one of these sets is available to the user at any one time. The choice is made by setting bit 11 in the Processor Status Word. These registers may be used as accumulators or as base or index registers for memory addressing. The existence of two sets means that fast context switching is possible. There are three registers used as stack pointers - one for each of the operating modes. Thus there is a kernel stack pointer (KSP), a supervisor stack pointer (SSP) and a user stack pointer (USP). The mode is chosen by setting bits 14,15 in the PSW and the stack pointer is then referred to as register R6.

The stack moves downwards in memory when items are pushed on to it. The stacks can be used to provide linkage information when the processor modes are switched. The DCJ11 provides hardware stack protection for the Kernel stack. Yellow and Red stack traps are described in table 5-3.

The final register is the program counter (instruction pointer). It is incremented by two every time a word is fetched from memory. It is accessed as register R7. R7 may also be used as a base or index registers for addressing. This has the effect of extending the power of the addressing modes.

5.4 SPECIAL PURPOSE REGISTERS

As well as the general purpose registers the SBC M70 implements a set of special purpose registers. These registers are used by the user to set some of the operational features of the system or by the system to provide status information to the user.

There are four sub-divisions of special purpose registers. These are the Internal Registers, the System Registers, the External Registers and the Power-Up Register. They all differ from the General Purpose Registers in that they have addresses in the 4K words of memory reserved for I/O addresses (the I/O page).

5.4.1 Internal Registers

The Internal Registers are so named because they are implemented in the logic of the DCJ11 itself. Unlike the General Purpose Registers, however, the user accesses them by addressing locations in the I/O page. Table 5-1 lists the Internal Registers. The Processor Status Word and CPU Error Register are described here. Descriptions of the other registers are reserved until the relevant sections of the architecture are being described.

TABLE 5-1 INTERNAL REGISTERS

Abbrv.	Register	Address
PSW	Processor Status Word	17777776
PIRQ	Program Interrupt Request Register	17777772
CPUERR	CPU Error Register	17777766
HMR	Hit/Miss Register (Cache)	17777752
-	Memory Management Registers	*
-	Floating Point Registers	**

* Refer to Appendix D.
** Floating point registers do not have addresses; they are referenced using special instructions.

5.4.1.1 The Processor Status Word

The Processor Status Word (PSW) contains information about current processor status. It also contains information about the result of the current instruction. By writing to it the user can provide the DCJ11 with information about how it is to run. Figure 5.1 gives a schematic of the PSW. Table 5-2 explains each bit in detail.

TABLE 5-2 PROCESSOR STATUS WORD

Bit	Name	Description
15:14	Current Mode (RW)	The state of these bits indicates the current processor mode as follows: **Bits** **Mode** 15 14 0 0 Kernel 0 1 Supervisor 1 0 N/A 1 1 User
13:12	Previous Mode (RW)	The bits indicate the previous processor mode. The bits have the same meaning as bits 15 and 14.
11	Register Set (RW)	If bit 11 is 0 then R0-R5 is used. If bit 11 is 1 then R0'-R5' is used.
10:9	Unused (Read Only)	These bits are unused and read back as 0's.
8	Reserved (RW)	This bit is reserved.
7:5	Priority (RW)	The bits are read as a 3 bit binary number with bit 5 as the least significant bit. An interrupt needs a priority greater than this number before it can interrupt the processor. Interrupt priority is explained in section 5.6.

TABLE 5-2 Contd. PROCESSOR STATUS WORD

Bit	Name	Description
4	Trace Trap (RW)	If this bit is set then the processor traps to location 14 at the end of the instruction currently being executed. The bit may not be set directly - it must be set via an RTI or RTT instruction.
3	N (Read Only)	The bit is set if the result of the previous operation was negative.
2	Z (Read Only)	The bit is set if the result of the previous operation was 0.
1	V (Read Only)	The bit is set if the previous operation resulted in an arithmetic overflow.
0	C (Read Only)	The bit is set if the most significant bit of the result of the previous operation was carried out.

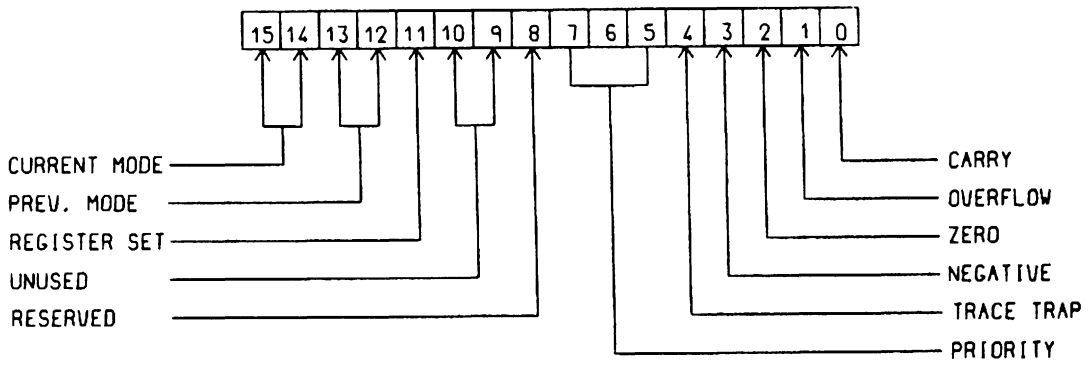

Fig. 5.1 Processor Status Word.

5.4.1.2 The CPU Error Register

The DCJ11 traps to location 4 when a CPU error occurs. The CPU error regiser is used to log the nature of the error. Only bits [7;3] of the CPU error regiser are used and these bits can only be read. All of the other bits return 0's when read. The CPU error register is summarised in Table 5-3 and figure 5.2.

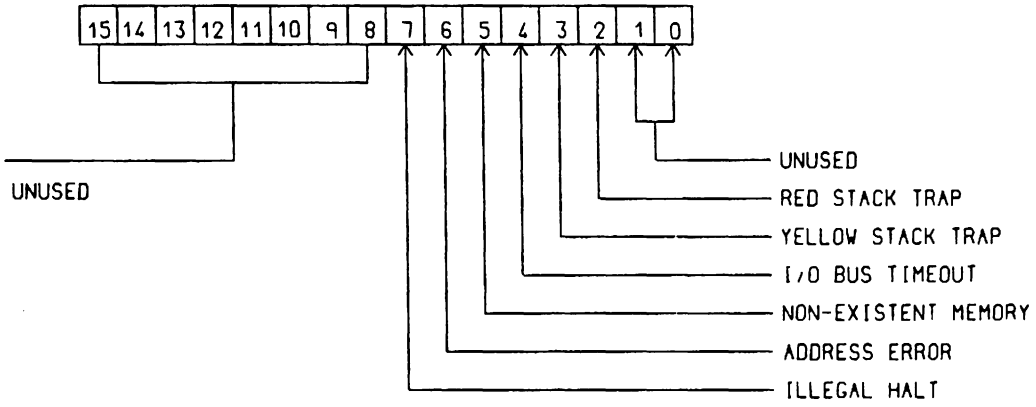

Fig. 5.2 CPU Error Register.

TABLE 5-3 CPU ERROR REGISTER

Bit	Name	Description
15:8	Unused	Return 0's when read.
7	Illegal HALT	A HALT instruction is illegal if executed in user or supervisor mode. A trap 4 will occur and this bit will be set. A HALT will cause this sequence of events in all three modes if bit 3 in the power-up configuration register is set. Refer to section 3.3.1.
6	Address Error	A trap to 4 will occur if an attempt is made to address a word with an odd address or if an attempt is made to fetch an address from an internal register. Bit 6 in the CPU error register is set in these instances.
5	Non-Existent Memory	An attempted access to a memory location which does not exist will cause a trap to 4. Bit 5 of the CPU Error Register is set. If the location is in the I/O page then bit 4 is set instead.
4	I/O Bus Timeout	If a non-existent location is in the I/O page then bit 6 is set.
3	Yellow Stack Trap	Set when a yellow zone stack trap occurs i.e. when a Kernel stack reference has a virtual address of less than octal 400.
2	Red Stack Trap	If a Kernel stack abort occurs during an interrupt, trap or abort sequence then a red stack trapis flagged and locations 0 and 2 are used as an emmergency stack, vectoring through location 4.
1:0	Unused	Return 0's when read.

5.4.2 The System Registers

The registers classed as system registers all have addresses in the range 17777740 to 17777750. The SBC M70 has three system registers - the Maintenance Register, the Memory Error Register, and the Cache Control Register. Table 5-4 gives the addresses of these registers.

The Cache Control Register is implemented internally to the DCJ11. The Memory Error Register and the Maintenance Register are implemented in logic external to the DCJ11. Some operating systems check for the existence of the latter two registers and this is the main reason for their inclusion. The maintenance register is described in section 5.4.2.1. Descriptions of the other two system registers are reserved for section 5.9.4.

5.4.2.1 The Maintenance Register

The Maintenance Register (MR) has the same bit definitions as the Power-up and Configuration Register. The latter is an external register and is described in section 3.3.1 and section 5.4.4.

TABLE 5-4 SYSTEM REGISTERS

Abbrv.	Register	Address
MR	Maintenance Register	17777750
MER	Memory Error Register	17777744
CCR	Cache Control Register	17777746

5.4.3 The External Registers

Some of the special registers are implemented in logic external to the DCJ11. These are the Line-Time Clock Register, The Error Checking and Correction Control and Status Register (ECCCSR). Table 5-5 lists the external registers.

TABLE 5-5 EXTERNAL REGISTERS

Abbrv.	Register	Address
LTC	Line-Time Clock Register	17777546
ECCCSR	Error Checking and Correction Control and Status Register	17777530

5.4.4 The Power-Up Register

The Power-Up Configuration Register is fully described in section 3.3.1. It differs from other external registers in that it does not have an address in the I/O page. The DCJ11 reads it on power-up using special read commands. The information in the Power-up Register may however be read at run-time through the Maintenance Register. The latter is described in section 5.4.2.1.

5.5 INSTRUCTIONS, DATA TYPES AND ADDRESSING MODES

The purpose of this section is to give some insight into the programming of the DCJ11.

5.5.1 Instructions

PDP-11 instructions can be either single-operand or double-operand. Each instruction consists of an op-code and six bits describing each operand. These six bits can be divided into two sets with three bits in each. The first set define the addressing mode and the second set defines the relevant register. All of the addressing modes need one of the DCJ11 internal registers (except the PSW, which cannot be used in this context). The single-operand and double-operand formats are summarised in figures 5.3 and 5.4. The PDP-11 instruction mnemonics are summarised in Appendix C.

5.5.2 Integer Data Types

The basic PDP-11 instruction set operates on integer data. Integers are stored in 2's complement notation and can occupy either bytes or words. A byte integer can represent any number between -128 and +127. A word integer can represent any number between -32768 and +32767.

5.5.3 Addressing Modes

There are eight basic PDP-11 addressing modes. These are described in table 5-6. R7, the program counter, can be used with all of these modes. In some cases this leads to very useful constructions. These are treated as separate addressing modes by DEC PDP-11 assemblers.

For example, if an instruction using R7 with mode 2 has been loaded by the DCJ11, the program counter will automatically point to the next word location in memory. Table 5-7 shows that the program counter is taken as holding the address of the operand. Thus it is possible to hold operands directly after the instructions in memory. The autoincrement function means that once the instruction is executed the program counter points to the next instruction. This is known as immediate addressing. Other constructions are derived analagously and are summarised in table 5-7.

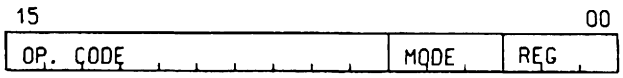

Fig. 5.3 Single-Operand Instruction Format.

Fig. 5.4 Double-Operand Instruction Format.

TABLE 5-6 ADDRESSING MODES

Mode	Name	Mnemonic	Address of Operand
0	Register	Rn	Operand in Register.
1	Register Deferred	@Rn or (Rn)	Register contains address of Operand.
2	Autoincrement	(Rn)+	Register contains address of Operand. Register is then incremented once if you are operating on a byte and twice if you are operating on a word.
3	Autoincrement Deferred	@(Rn)+	Register contains address of address of operand. Register is then incremented once for bytes and twice for words.
4	Autodecrement	-(Rn)	Register is decremented to get address of operand. Decremented once for words and twice for bytes.
5	Autodecrement Deferred	@-(Rn)	Register is decremented to get address of address of operand; once for bytes and twice for words.
6	Index	X(Rn)	X is added to register to get address of operand.
7	Index Deferred	@X(Rn)	X is added to register to get address of address of operand.

TABLE 5-7 ADDRESSING MODES USING R7

Mode	Name	Mnemonic	Address of Operand
2	Immediate	#n	The operand immediately follows the instruction in memory.
3	Absolute	@#A	The address of the operand immediately follows the instruction in memory.
6	Relative	X(PC) or A	X is added to R7 to get the address of the operand. R7 points to the next instruction when the calculation is done. Thus X gives an offset from the current location to the operand.
7	Relative Deferred	@X(PC) or @A	Analagous to Relative Addressing, except the offset locates the address of address of the operand.

5.6 INTERRUPTS AND TRAPS

Traps are caused by events internal to the DCJ11. Interrupts are caused by external events. Thus an illegal instruction would cause a trap whereas a request for service by a peripheral device would cause an interrupt. The DCJ11 implements a vectored interrupt mechanism whereby each trap or interrupt has a two word vector associated with it. The first word of the vector is used to hold a program counter value, the second holds a PSW value.

The following sequence of events takes place on occurrence of a trap or interrupt. The values of the PC and PSW at the time the trap or interrupt occurred are saved on the stack (the PS is saved first). The PC and PSW are loaded with the values in the interrupt vector. The user can thus provide routines to handle any possible traps or interrupts - program control will jump to them on occurrence of the relevant trap or interrupt.

The DCJ11 has nine levels of interrupt priority. Bits [7,5] in the PSW are used to determine the level of interrupt necessary to interrupt the processor at any particular time. These bits hold a binary number and only interrupt levels greater than this number can interrupt. If interrupts with levels 5,6 or 7 are to be acknowledged, for example, then bits [7,5] must hold binary 100 (decimal 4).

5.6.1 The Program Interrupt Request Register

The Program Interrupt Request Register (PIRQ) can interrupt the processor at any one of the seven levels of interrupt priority. An interrupt will occur if one of the bits [15,9] in the PIRQ is set. The PIRQ has two sets of read only bits which hold the binary value of the priority. The vector for a trap instigated by the PIRQ is 240.

Table 5-8 describes each bit in the PIRQ. Figure 5.5 shows the PIRQ in schematic form.

TABLE 5-8 PROGRAM INTERRUPT REQUEST REGISTER

Bit	Name	Description
15:9	PIR7 to PIR1 (RW)	When bit 15 is set an interrupt with priority level of 7 is requested. Bit 14 is used to request an interrupt with priority level 62 and so on down to bit 9 which requests an interrupt with a priority of 1.
7:5	- Read only	Contains the binary value of the highest program interrupt pending.
3:1	- Read Only	These bits hold the same information as bits 7:5.

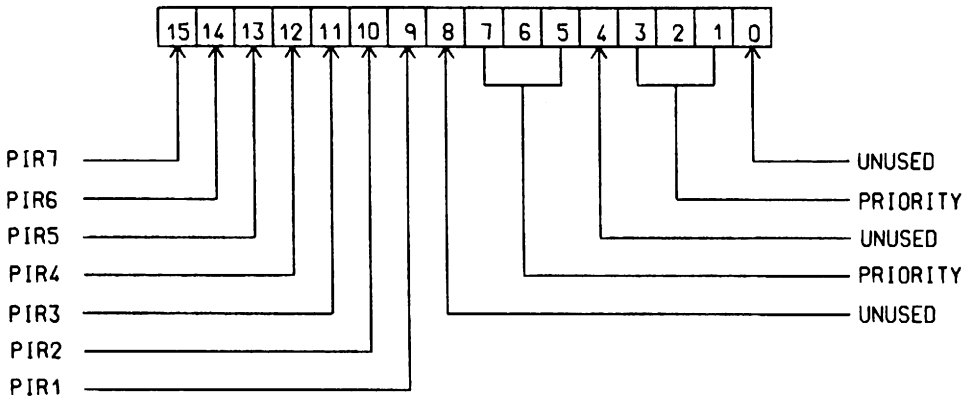

Fig. 5.5 Program Interrupt Request Register.

5.7 FLOATING POINT

A floating point processor is an optional part of the PDP-11 architecture which the DCJ11 implements as standard. The floating point processor has three status and control registers and six floating point accumulators which it uses to hold data on which it is operating. All of these internal registers are accessed using special floating point instructions.

Floating point data can be stored in memory in single-precision format (stored as two words), or double-precision format (stored as four words). A floating point number consists of a fraction and an exponent stored in binary form. The single precision and double precision formats are shown in figures 5.6 and 5.7, respectively. The range of numbers which can be represented is approximately 0.29×10^{-38} to $1.7 \times 10^{+38}$.

As well as operating on floating point data, the floating point processor can convert from integer to floating point format and vice-versa. It recognizes two integer formats for these purposes - single precision and double precision. These are detailed in figure 5.8 and 5.9.

The addressing modes for the floating point instructions are the same as those used for integers.

5.7.1 Floating Point Registers

Information passes between the user and the floating-point processor through three status and control registers - the Floating-Point Status Register, the Floating Exception Code Register and the Floating Exception Address Register.

NOTE:- The descriptions of the floating point registers are only included for completeness. Someone who wants to use the floating point implementation should refer to DEC documentation to acquaint themselves with its peculiarities.

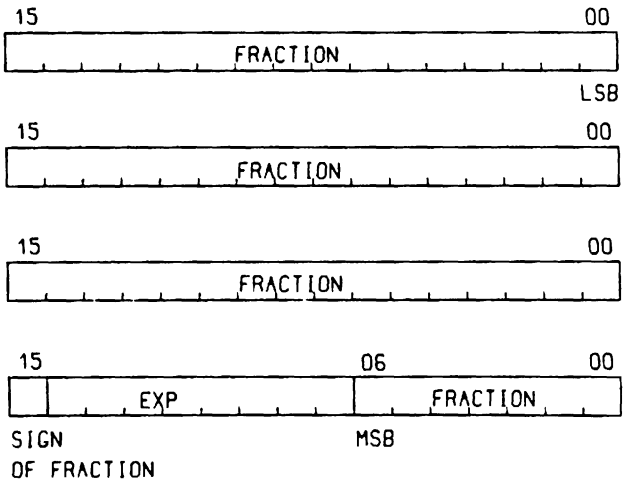

Fig. 5.6 Double Precision Floating Point.

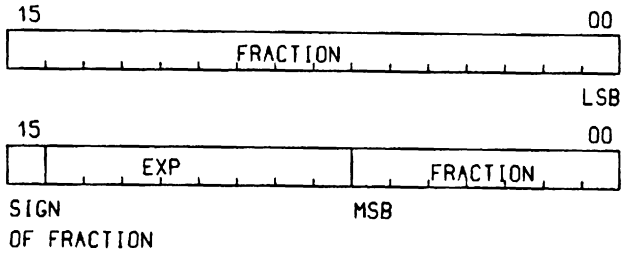

Fig. 5.7 Single Precison Floating Point.

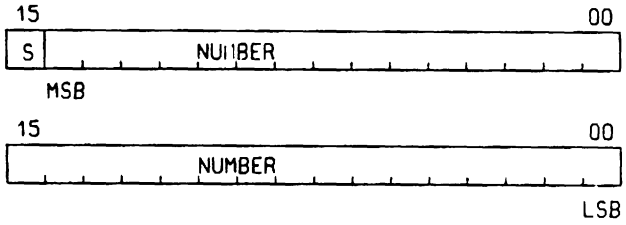

Fig. 5.8 Double Precision
2's Compliment Integer.

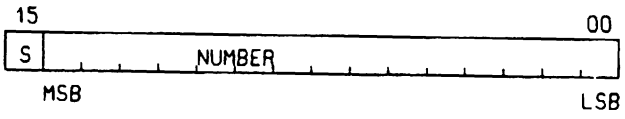

Fig. 5.9 Single Precision
2's Compliment Integer

5.7.1.1 Floating Point Status Register

Table 5-9 and figure 5.10 describe the floating point status register.

TABLE 5-9 FLOATING POINT STATUS REGISTER

Bit	Name	Description
15	FER	This bit is set if an error occurs. The error is logged in the FEC.
14	FID	This bit is set when it is required to disable all floating point interrupts.
13:12	-	Reserved for future use.
11	FIUV	Interrupt on undefined variable is enabled when this bit is set.
10	FIU	Interrupt on underflow is enabled when this bit is set.
9	FIV	Interrupt on overflow is enabled when this bit is set.
8	FIC	Interrupt when conversion to integer instruction fails.
7	FD	When set to a 1 this bit enables the double-precision mode for floating point calculations. Otherwise the single-precision mode is assumed.
6	FL	When set to a 1 this bit ensures that double precision integers are used when converting between integer and floating point numbers. Otherwise single precision integers are used.
5	FT	
4	-	Reserved for future use.
3	FN	Floating Negative.
2	FZ	Floating Zero.
1	FV	Floating Overflow.
0	FC	Floating Carry.

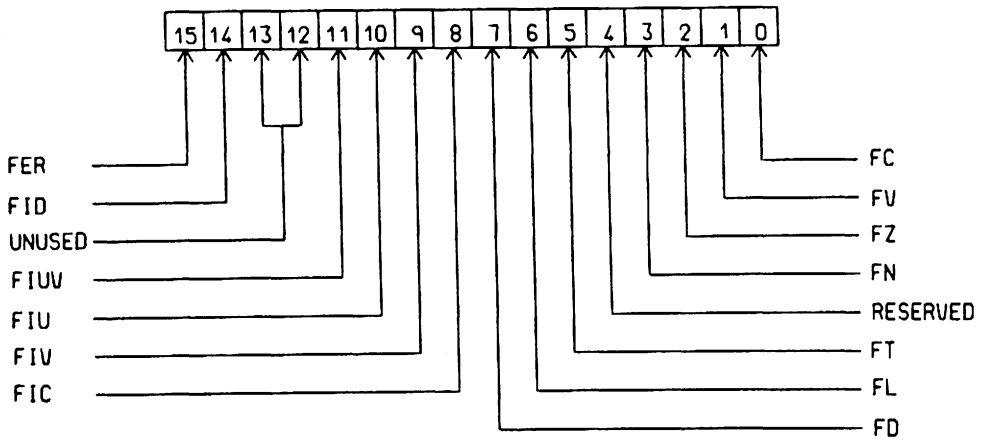

Fig. 5.10 Floating Point Status Register.

5.7.1.2 Floating Exception Code Register

Only the four least significant bits of this register are used. They are used to pass error information to the user and represent a four-bit code as shown in table 5-10.

TABLE 5-10 FLOATING EXCEPTION CODE

Code	Meaning
10	Floating Op-Code Error.
100	Floating Divide by 0.
110	Floating-to-integer or double-to-integer conv. err.
1000	Floating Overflow.
1010	Floating Underflow.
1100	Floating Undefined Variable.

5.7.1.3 Floating Exception Address

The Floating Exception Address Register (FEA) contains the address of an instruction causing an error.

5.8 MEMORY MANAGEMENT

The DCJ11, like all other PDP-11s is functionally a sixteen-bit machine. This basically limits the virtual address space to 64k bytes. The DCJ11 Memory Management Unit (MMU) allows the effective memory to be expanded. The MMU maps a sixteen bit virtual address space (64 Kb) to a twenty-two-bit physical address space (4 Mb) using a paging system. The user can decide where each page is to reside in physical memory by writing to registers in the MMU. The only restriction on the mapping of virtual addresses to physical memory is that they should start at locations which are multiples of 64 bytes.

5.8.1 Active Page Registers

The user decides where the pages are to be mapped by writing to the Active Page Registers. The MMU maintains one of these for each page that it maps. Each one consists of two sixteen-bit registers, the Page Address Register (PAR) and the Page Descriptor Register (PDR).

Each processor mode can map eight pages. This gives twenty-four Actve Page Registers. If the Instruction/Data space mode of operation is enabled (Refer to table 5-13), then these twenty-four pairs are used to map to the instruction Space and a further twenty-four are available to map to the Data Space. The Instruction/Data space mode of operation is described in section 5.8.4.

5.8.1.1 Page Address Register

This register contains the block number in physical memory to which the page is to be mapped.

5.8.1.2 Page Descriptor Register

The PDR allows the user to set some of the features of the mapped page. It is described in table 5-11 and figure 5.11.

NOTE:- Refer to Appendix D, Table D-6 for addresses of Memory Management Registers.

TABLE 5-11 PAGE DESCRIPTOR REGISTER

Bit	R/W	Description
15	R/W	If this bit is set then references to this page will bypass cache.
14:8	R/W	The length of the page in blocks is contained in bits 14:8. An attempt to access data in a longer page will lead to a page length abort.
7	R	Reserved for future use.
6	R	If this bit is set then the page has been written to since the last time its PAR or PDR was modified.
5:4	R	Reserved for future use.
3	R/W	This bit indicates in which direction the page expands. When set to a 1 the page will expand downwards.
2:1	R/W	Access Control Field. These bits represent a code as follows: 00 Non Resident - Abort all. 01 Read Only - Abort on write. 10 Unused - Abort all. 11 Read/Write - Full Access.
0	R	Reserved for future use.

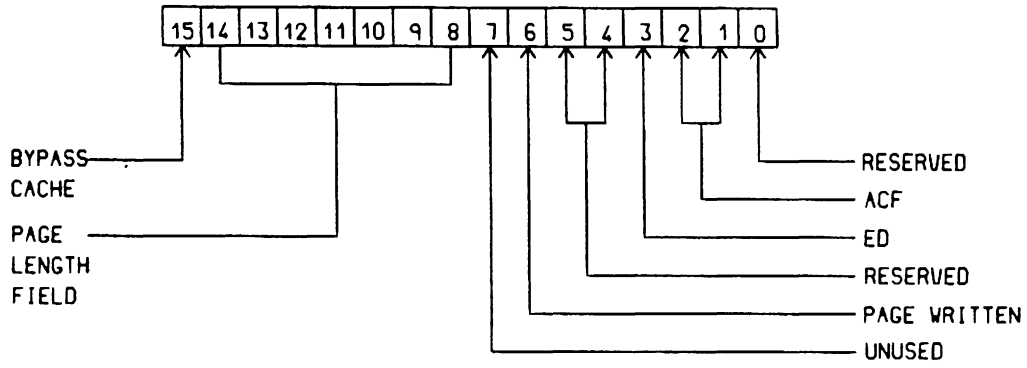

Fig. 5.11 Page Descriptor Register.

5.8.2 The Memory Management Registers

The user interacts with the MMU through a series of registers in the I/O page. There are four status and control registers - MMR0-3. These are used to enable and disable the MMU and to decide some other features of its operation.

5.8.2.1 Memory Management Register 0

Memory Management Register 0 gives status and control information for the memory management unit. Refer to figure 5.12 and table 5-12.

TABLE 5-12 MEMORY MANAGEMENT REGISTER 0

Bit		Description
15	R	If an attempt is made to access a non-resident page then an abort will occur and this bit will be set.
14	R	MMU will abort if program tries to access memory beyond the page length indicated in the PDR. This bit will also be set.
13	R	If an attempt is made to access a page which has been set as read-only then an abort will occur and this bit will be set.
12:7	R	Reserved for future use.
6:5	R	Indicates which processor mode is causing the abort. Code is same as
4	R	that for PSW.
3:1	R	These bits contain the number of the page causing the abort in binary form.
0	R/W	**This bit must be set if the MMU is * to be enabled.**

NOTE:- This bit must be set to 1 if MMU is to be used since the DCJ11 powers up as a sixteen-bit machine.

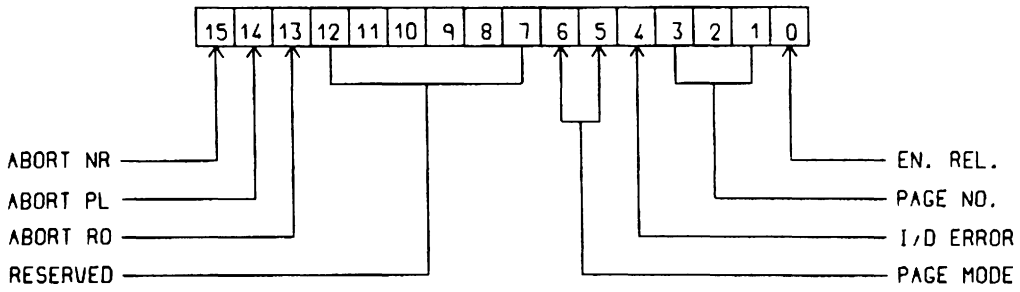

Fig. 5.12 Memory Management Register 0.

5.8.2.2 Memory Management Register 1

If a memory management trap occurs then Memory Management Register 1 (MMR1) records any changes to the general purpose registers. Figure 5.13 gives the format of the register. The register number is given in binary form. The amount by which the register has changed is given in 2's compliment format.

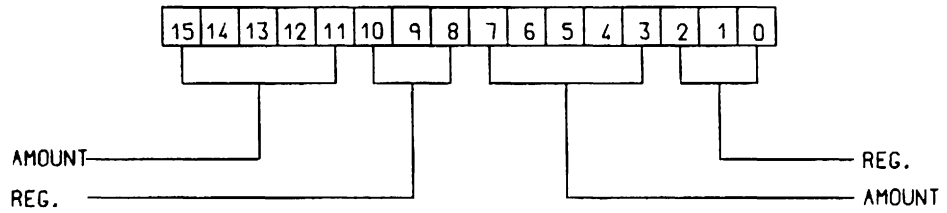

Fig. 5.13 Memory Management Register 1.

5.8.2.3 Memory Management Register 2

Memory Management Register 2 (MMR2) holds the virtual address of the instruction which is currently being fetched.

5.8.2.4 Memory Management Register 3

Memory Management Register 3 (MMR3) gives further status and control information. It is summarised in figure 5.14 table 5-13.

TABLE 5-13 MEMORY MANAGEMENT REGISTER 3

Bit	Description
15:6	Reserved for future use - always read back as 0.
5	The MAP output of the DCJ11 can be enabled by setting this bit to a 1.
4	If this bit is 0 when the MMU is enabled then 18-bit mapping is used. To enable 22-bit mapping the bit should be set to a 1. This should be done for the SBC M70.
3	Enable CSM instruction.
2	Enable Kernel Data Space
1	Enable Supervisor Data Space
0	Enable User Data Space

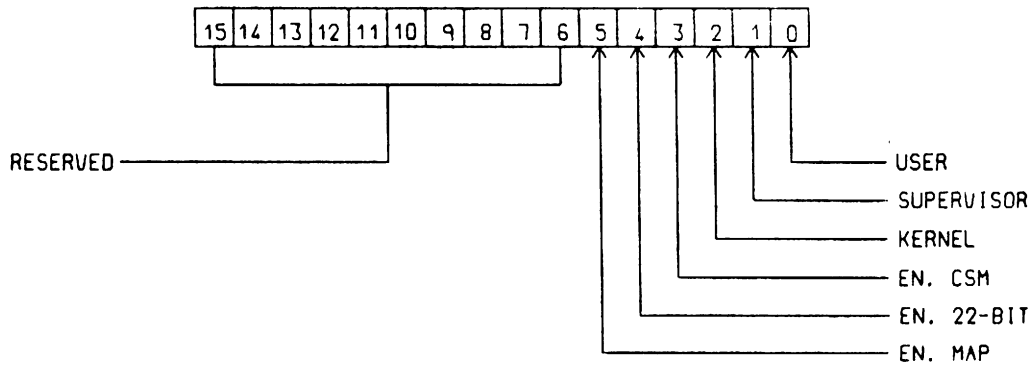

Fig. 5.14 Memory Management Register 3.

5.8.3 Mapping from Virtual to Physical Memory

The mapping procedure is now considered. The MMU contains a PAR for every page that it maps. The three most significant bits in the virtual address are used to choose between the pages. The number in the PAR must be shifted six bits to the left to give the address in physical memory to which the page is to be mapped. The sixteen least significant bits of the virtual address are used as the displacement within the page. The mapping procedure is summarised in figure 5.15.

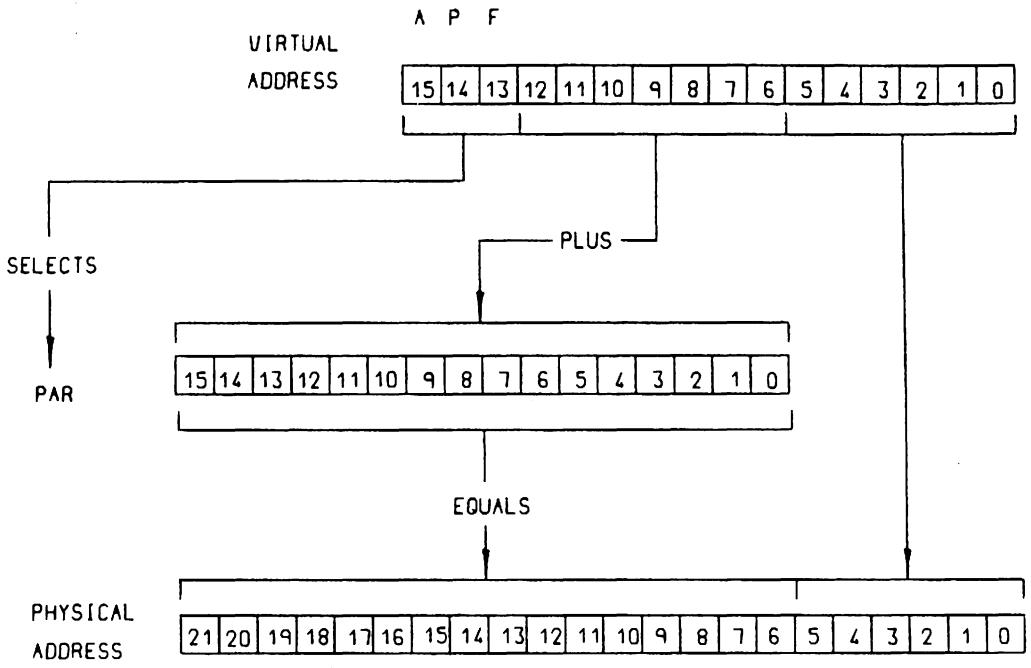

Fig. 5.15 Virtual To Physical Address Mapping.

5.8.4 Instruction and Data Space

The Instruction/Data space mode of operation can be enabled through the memory management registers. In this mode of operation the user has access to sixteen pages instead of the normal eight. Eight of the pages are reserved for data and eight are reserved for instructions.

5.9 SBC M70 MEMORIES

The SBC M70 memories are as follows. 1: Main RAM memory, 2: Bootproms. The location of these on the module is shown in figure 1.1.

5.9.1 Random Access Memory

The main memory on the SBC M70 consists of 1/2 Mb, 1Mb or 2Mb of dynamic random access ECC Error Checking and Correction (ECC) memory. It is addressed from location 0 upwards and may not be moved from there. The Intel 8207 Advanced Dynamic RAM Controller (Refer figure 1.1) controls it. This converts DCJ11 addresses to the form required by the RAMs and also provides the logic which initialises and refreshes them. Error correction is provided by the Intel 8206 Error Detection and Correction Unit. This unit supports full detection and correction for single bit errors and full detection for double bit errors and most other multi-bit errors.

5.9.1.1 Memory Layout

The dynamic memory consists of either 64 Kbit or 256 Kbit dynamic RAMs arranged in banks. Each bank contains twenty-two RAMs and so can hold either 64K or 256K twenty-two-bit words. Thus the 1/2 Mb version requires four banks with twenty-two 64 Kbit RAMs. The 1Mb version of the SBC M70 requires two banks with twenty-two 256 Kbit RAMs. The 2 Mb version requires 4 banks with twenty-two 256 Kbit RAMs.

Each twenty-two bit word consists of an ordinary sixteen -bit data word and six checkbits. The checkbits are maintained by the 8206.

The memory layout for a 1 Mb SBC M70 is shown in figure 5.16. The layout for a 1/2 Mb or 2 Mb SBC M70 is shown in figure 5.17.

5.9.2 ECC Memory User Information

User interaction with the ECC memory is by means of one system register - the ECC Control Register (ECCCSR), and the yellow LED on the front of the SBC M70. To fully use the features of the memory it is necessary to understand something of its operation. Towards this end, a brief description of the error-correction procedure is given.

The basic function of the ECC unit is to generate a code, known as a syndrome, for each word in error. The syndrome gives information on whether the error is correctable, and, if it is, in which bit it is to be found.

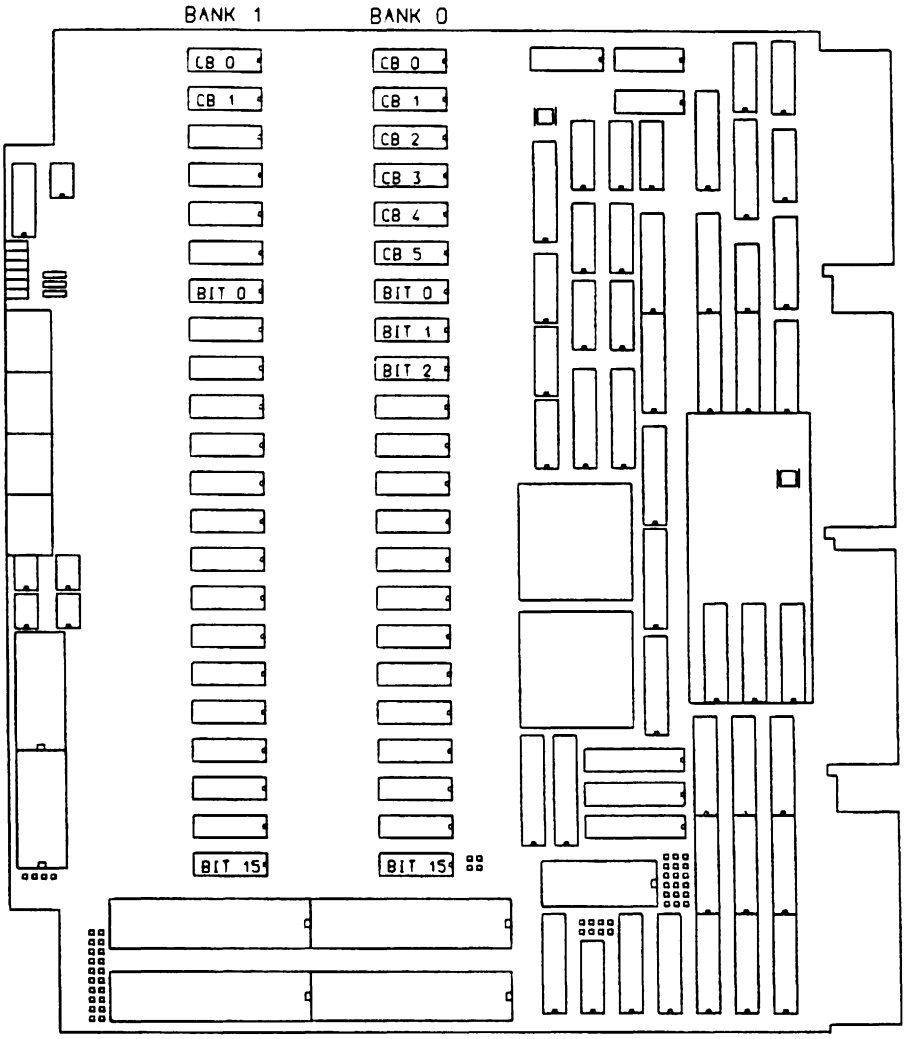

Fig. 5.16 Memory Map - 1Mb SBC M70.

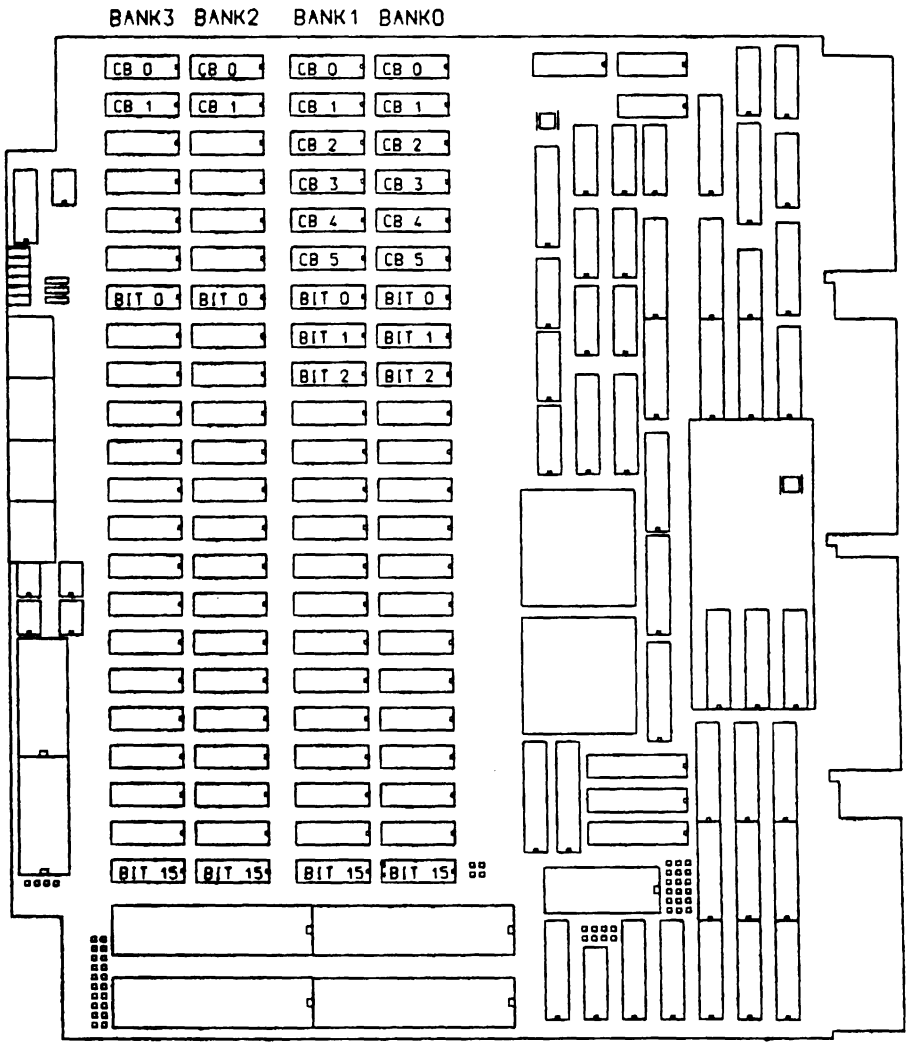

Fig. 5.17 Memory Map - 1/2 or 2 Mb SBC M70.

5.9.2.1 Write Cycle

During a WRITE cycle, the data is written to the 8206 as well as being written directly to the DRAM array. The 8206 then uses a modified Hamming code to generate checkbits. The code generates five checkbits for error detection on sixteen-bit data and a sixth checkbit for error detection on the checkbits themselves. Once generated the checkbits are stored in their own section of the RAM.

5.9.2 Read Cycle

During a READ cycle, the data and checkbits pass into the 8206 where a new set of checkbits are generated. They are compared with those originally stored. If the two sets are the same then the data appears unchanged at the 8206 outputs. If they are different then the 8206 provides a syndrome, based on the differences, on six of its output pins. The syndrome is logged in the ECCCSR and the yellow LED is illuminated. If the syndrome indicates a single bit error then the error may be corrected and the corrected data appears at the 8206 outputs. For a double-bit error, and most other multi-bit errors, the system traps to location 114. Note that a trap to 114 will also occur if the system detects a bus parity error from offboard memory.

5.9.3 The ECCCSR

The part of the RAM which stores the checkbits may not be addressed directly. The user only has access to error information through the ECCCSR when an error is detected. The ECCCSR register is addressable at location 17777530. The ECCCSR also allows the user to inhibit data being written to the checkbit section of the RAM. This feature is used by diagnostics to verify ECC operation as follows. Data is written to memory with checkbit memory enabled. Checkbit memory is then disabled and new data is written to memory. If this data is then read back the ECC should notify an error since it will be using the checkbits generated for the original data. The bit designations of the ECCCSR are shown in figure 5.18 and the bit functions are summarised in table 5-14. Table 5-15 gives a list of all possible syndromes and the errors which they represent.

5.9.4 Refresh

The 8207 is responsible for refreshing the memory. Note that as part of the refresh cycle memory is constantly being error scrubbed. The result of this is that all of ECC memory is error scrubbed approximately once every 12 seconds. However, errors detected through this process are not logged in the ECCCSR.

TABLE 5-14 ECCCSR BIT DEFINITIONS

Bit	Mnemonic	Description
15	ERROR R/W	Set when a single or double bit error occurs in memory during a local memory read. When set the error LED is illuminated.
14:9	SY5-SY0 Read Only	When ERROR is set these bits give the syndrome. These bits are not valid until the first ERROR.
8:7	BS1-BS0 Read Only	When ERROR is set these bits indicate in which bank the error occurred: 1/2-2mb 1mb 00 BANK3 BANK1 01 BANK2 BANK0 10 BANK1 BANK1 11 BANK0 BANK0
6:3	-	Reserved for future use.
2	WEC R/W	Bit is set to a 1 if it is required to disable checkbit memory for diagnostics.
1:0	-	Reserved for future use.

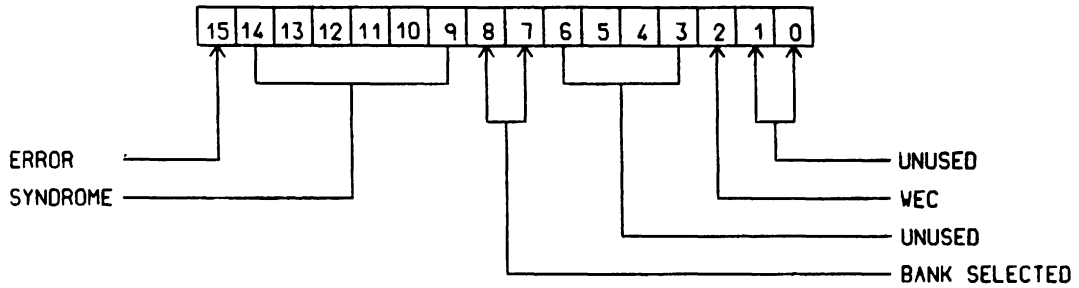

Fig. 5.18 ECCCSR Bit Designations.

TABLE 5-15 SYNDROME DECODING

0 1 2 543	0 0 0	1 0 0	0 1 0	1 1 0	0 0 1	1 0 1	0 1 1	1 1 1
000	N	C0	C1	D	C2	D	D	D
001	C3	D	D	0	D	1	2	D
010	C4	D	D	5	D	6	7	D
011	D	3	D	D	4	D	D	D
100	C5	D	D	11	D	D	12	D
101	D	8	9	D	10	D	D	D
110	D	13	14	D	15	D	D	D
111	D	D	D	D	D	D	D	D

Using the table

The numbers in the top left hand corner are the numbers of the syndrome bits. The values along the top and side are the values these bits can take. The table shows the meaning of any possible syndrome word using the following notation:

N = No Error.
Decimal Digit X = Error in bit X.
C followed by digit X = Error in checkbit X.
D = Double or Multiple Bit Error.

5.9.3 BOOTPROMS

DEC reserve two areas of 1/2 Kb in length in the I/O page for boot code. They stretch from memory location 17765000 to 17765776 and from 17773000 to 17773776. These two areas taken together represent a window.

The SBC M70 boot code is contained in two 2716 EPROMS. The high byte is contained in one EPROM (E148) and the low byte in the other (E149). As two 2716's contain 4Kb of code this allows four seperate sets of code or "windows". Section 3.3.8 explains how wire-wrapping can be used to choose between the windows. Figure 5.19 illustrates how the bootcode is distributed in the memory space. Figure 5.20 shows the boot PROM windows.

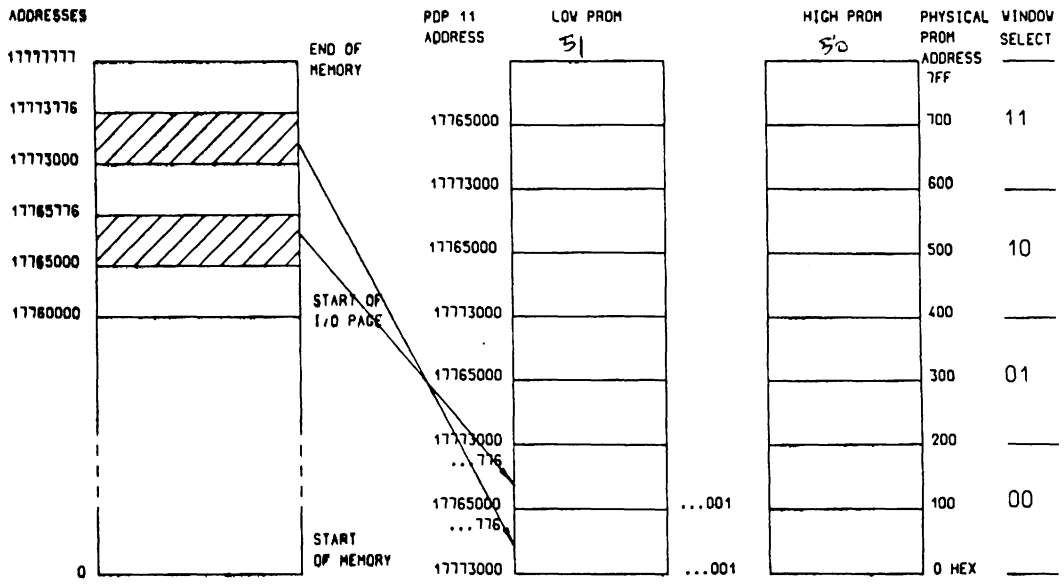

Fig. 5.19 Bootstrap Layout.

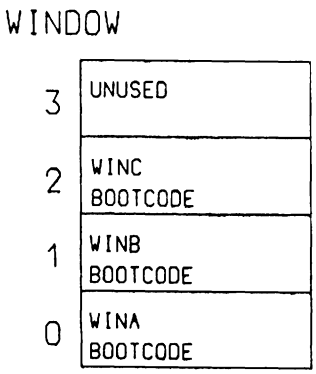

Fig. 5.20 Bootstrap Windows.

5.9.4 Cache Memory Registers

The DCJ11 is designed to support a system with cache memory. The SBC M70 is designed in such a way that the whole of main memory appears as cache to the DCJ11. A series of registers is associated with control and monitoring of the cache implementation.

5.9.4.1 Cache Hit/Miss Register

This register should be considered in conjunction with the Cache-Control Register (CCR). The CCR is classed as a system register and is described in section 5.9.4.2. The Hit/Miss register (HMR) is used to notify a user of the nature of the six most recent cache memory references. The register is summarised in Table 5-16 and figure 5.21.

TABLE 5-16 CACHE HIT/MISS REGISTER

Bit	Name	Description
15:6	Unused	Return 0's when read.
5:0	-	These read-only bits indicate whether the last six cache accesses were succesful or not. A cache hit will generate a logical 1 and a cache miss will generate a logical 0. The bits enter the register at bit position 0 and are shifted left.

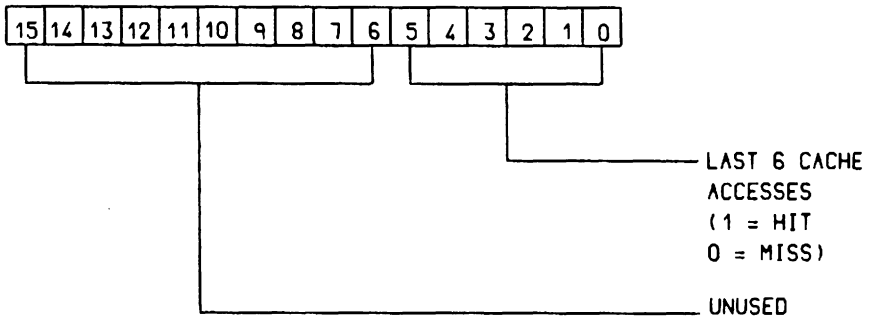

Fig. 5.21 Cache Hit/Miss Register.

5.9.4.2 Cache Control Register

The Cache Control Register (CCR) allows a user to pass information to the cache system. Only bits [3:2] and bit 9 of the CCR are active. The CCR is summarised in Table 5-17 and figure 5.22.

TABLE 5-17 CACHE CONTROL REGISTER

Bit	Name	Description
15:11	Unused	These bits can only be read; when they are read they return 0's.
10	Unused	This bit can be read from or written to but the DCJ11 does not interpret the contents.
9	Uncon-ditional Cache Bypass	If a user sets this bit to a 1 then all cache hits are invalidated and all memory references are forced cache misses.
8	Unused	This bit can only be read; when it is read it returns a 0.
7:4	Unused	These bits can be read from or written to but the DCJ11 does not interpret the contents.
3:2	Force Cache Miss	If a user sets either of these bits to a 1 then the cache system is disabled completely. All memory references are forced cache misses.
1:0	Unused	These bits can be read from or written to but the DCJ11 does not interpret the contents.

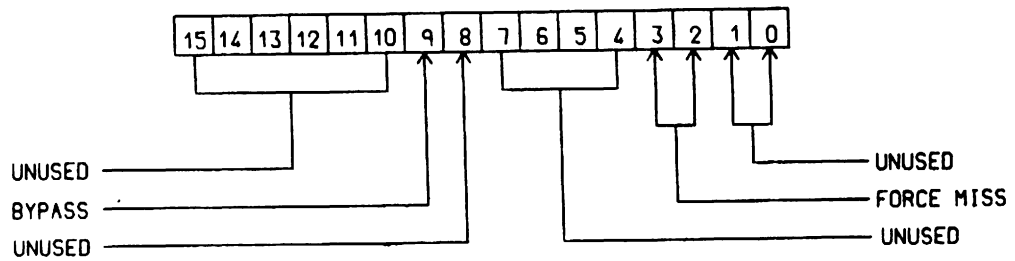

Fig. 5.22 Cache Control Register.

5.9.4.3 Memory Error Register

Certain PDP-11 systems use the Memory Error Register (MER) to report errors in the cache system. The register is included in the SBC M70 design solely because some operating systems check for its existence. The MER returns all 0's when read. If it reported errors then software might attempt to disable cache and this would deteriorate system performance.

WARNING

Care should be taken when using the Cache Subsystem. Disabling Cache will seriously degrade system performance.

5.10 PROGRAM CONTROL OF THE LINE-TIME CLOCK

The line-time clock function is controlled through the LTC register, addressable at location 17777546. The only accessible bit in this register is bit 6. It must be set to 1 if the clock signal is to reach the EVENT input. This is done by writing 100 to the register. Note that the bit is cleared on power-up. It will also be cleared by a RESET instruction. The line-time clock is a write-only register. It will not return valid information on being read.

CHAPTER 6

SERIAL I/O

6 SERIAL I/O

6.1 INTRODUCTION

This chapter describes the EIA standards used by the serial line units, the programming of the serial line units, and the cables used for serial communications. The console ODT feature of the DCJ11 is also described.

6.2 EIA STANDARDS

Each SLU complies with the following Electronics Industries Standards: RS-232 and RS-423. RS-232 specifies single-ended teransmission and reception. RS-432 specifies single-ended transmission and differential reception. Refer to figures 6.1(a) and 6.1(b). RS-423A specifies higher rates of data transmission over longer distances. The main requirements of each standard are given in table 6-1.

If a 20 mA. device is required then the DLV11-KA option may be used. The DLV11-KA is a converter box with a cable (BC21A-03) which connects to the SBC M70. It connects to the standard 20 mA. cable. (This option will not support the Reader Run strobe or a baud rate of 110, so some devices, such as the LA33, may not be used).

6.3 SERIAL LINE ARCHITECTURE

The main components of the serial line sub-system are shown in figure 6.2. The main component in each serial line is the DEC DC319-AA Asynchronous Receiver and Transmitter (DLART). Line drivers and receivers are then used to interface these to the serial line cable connectors. There are two uA9636 dual line drivers and two uA9637 dual differential line receivers.

Figure 6.2 also shows the slew rate resistors. These are fully explained in section 3.3.7.

TABLE 6-1 EIA STANDARDS

Standard	Line Length	Data Rate	No. of Drivers	No. of Receivers
RS-232C	16 M	20 kb/s	1	1
RS-423A	10 M	100 kb/s	1	10
	100 M	10 kb/s	1	10
	1300 M	1 kb/s	1	10

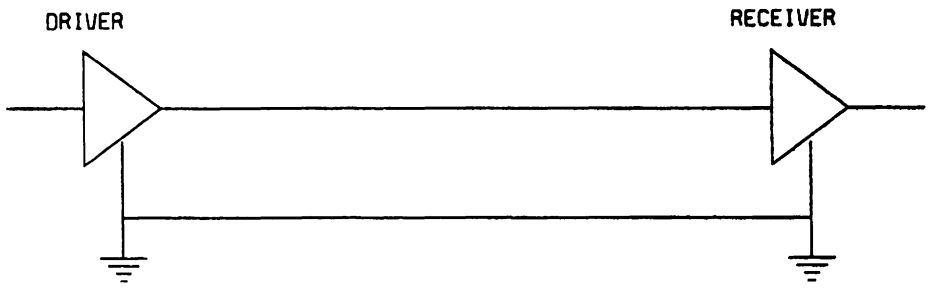

Fig. 6.1(a) RS-232.

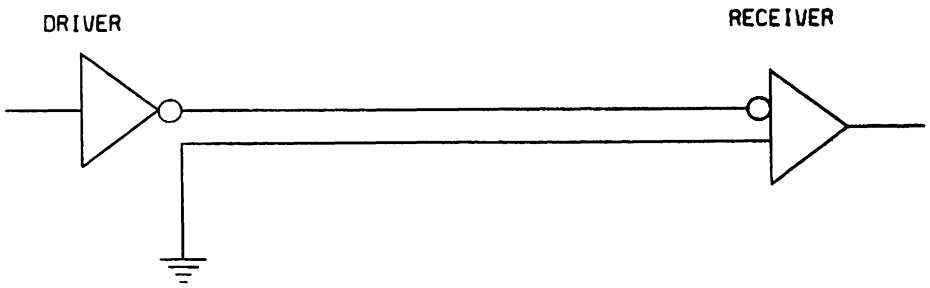

Fig. 6.1(b) RS-423.

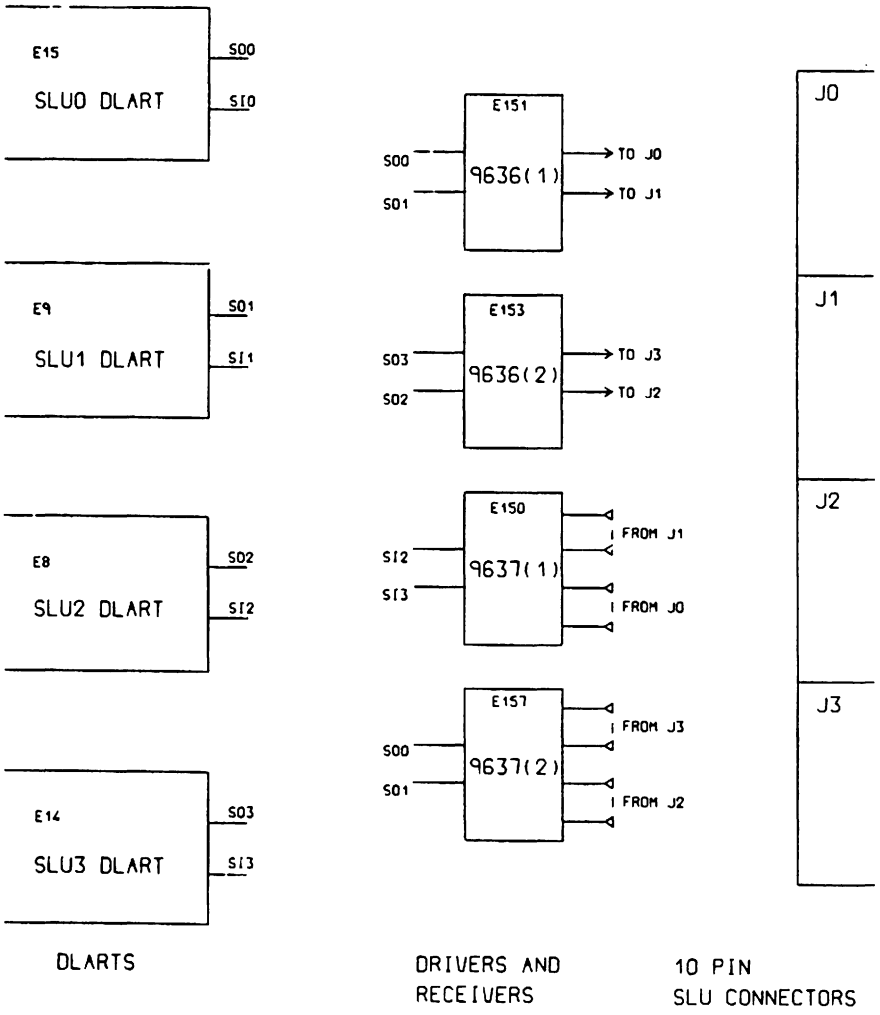

Fig. 6.2 Serial Line Hardware.

6.4 DC319-AA DLART

Each serial line presents four registers to the user as follows: The Transmitter Control and Status Register (XCSR), the Transmitter Buffer (XBUF), the Receiver Control and Status Register (RCSR) and the Receiver Buffer (RBUF). All of these registers are internal to the DLARTS.

NOTE:- The only available setting is 1 start bit, 1 stop bit and no parity.

The DLARTs operate by converting parallel data from the DCJ11 processor DAL (data address) lines to serial data and vice-versa. This is achieved using shift registers. The Transmit Data Buffer and the Receive Data Buffer will only accept 8 bits of information. Seven bits of this can be used to define an ASCII character.

The operation of the device during serial transmission and reception is now described in general terms. The bits which are mentioned all reside in the device registers. Their exact locations in the registers are described in tables 4-3 to 4-6. The tables also contain further information on the particular operation of these bits as well as information concerning error bits.

Each packet sent out on the serial line consists of the eight bits of data written to the transmit buffer. It will be trailed by a single stop bit. This is a HI bit which indicates to the receiving device that the complete character (byte) has been transmitted. Data being received along the serial line by the DLART is expected to be in the same form.

6.4.1 Transmission

If the XMIT RDY bit is set then a byte can be written to the transmit buffer. This bit will go LO as soon as the byte is written to indicate that the transmit section of the device is in the busy state. As soon as the byte has been completely placed on the serial line the XMIT RDY bit will once again go HI to indicate readyness to transmit. An interrupt can be arranged to occur at the same time a XMIT RDY if so required.

6.4.2 Reception

Reception is more difficult since some allowance must be made for the fact that erroneous data may be received. The basic concept is that the receiver has two buffers. Serial input data is placed in the first, bit by bit, as it is received. When a byte is received it is moved from this first buffer to the Receive Buffer which is transparent to the user. At this point the Receive Done bit is set. Ideally the character is read and this bit will go LO to indicate that the DLART has not yet received the next character. If the old character has not been read, or has only been partially read, before the

new character is written into the receive buffer then an overrun error will be flagged. If a valid stop bit is not found then a framing error is flagged. An interrupt can be arranged to coincide with RCV DONE so that the chances of an overrun error may be reduced.

6.4.3 Serial Line Interrupt Priorities

Interrupts can be configured to occur an completion of a transmission or reception cycle. This leads to eight possible interrupts. These all interrupt the DCJ11 with a priority of 4. If more than one of the DLARTs try to interrupt the DCJ11 at any one time then the interrupts are presented to the DCJ11 in the order indicated in table 6-2.

TABLE 6-2 SLU INTERRUPT PRIORITIES

Device	Interrupt	DCJ11 Priority	Acceptance Order
SLU0	RX	4	
SLU1	RX	4	
SLU2	RX	4	Order of decreasing priority (i.e. SLU0 RX will interrupt before SLU1 RX).
SLU3	RX	4	
SLU0	TX	4	
SLU1	TX	4	
SLU2	TX	4	V
SLU3	TX	4	

6.5 SERIAL LINE REGISTERS

This ection summerises the serial line registers. Figures 6.3(a) to 6.3(d) give bit maps for the serial line registers. Tables 6-3 to 6-6 give bit descriptions.

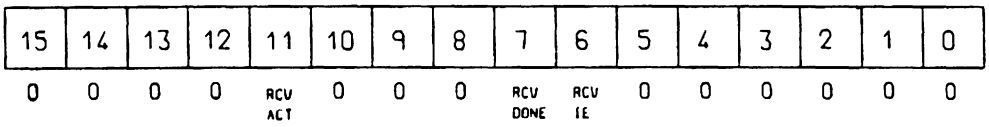

Fig. 6.3(a) Receiver Control and Status Register.

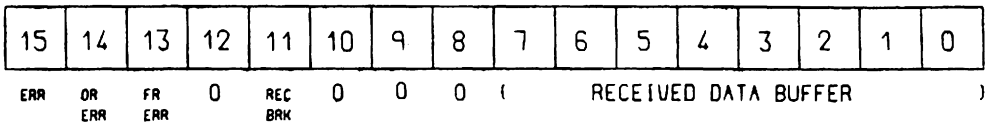

Fig. 6.3(b) Receiver Data Buffer Register.

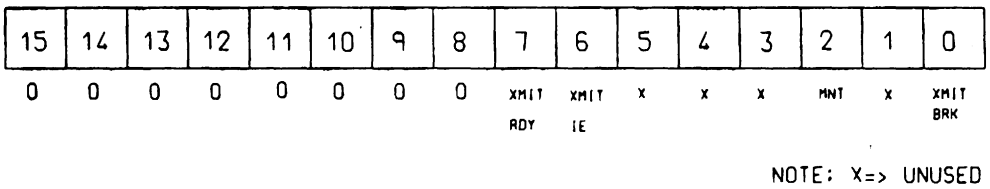

Fig. 6.3(c) Transmitter Control and Status Register.

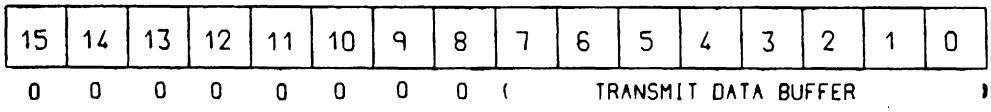

Fig. 6.3(d) Transmitter Data Buffer Register.

TABLE 6-3 RECEIVER CONTROL AND STATUS BIT DESCRIPTION

Bits	Name	Direction	Function
12-15	Not used	Read only	Reserved for future use.
11	Receiver Active (RCV ACT)	Read only	This bit is set to a 1 by the start bit at the end of each byte. It is also cleared to a 0 on power-up.
08-10	Not used	Read only	Reserved for future use.
07	Receiver done (RCV DONE)	Read only	This bit is set to a 1 when the byte received is transferred into the RCV data buffer. It is cleared to a 0 when the RCV data buffer is read. It is also cleared to a 0 on power-up.
06	Receiver Interrupt Enable (RCV IE)	Read/Write	This bit is set in software if it is desired that RCV IRQ be able to interrupt on pin 26 of the DLART. The interrupt will occur when data has been received i.e. when the RCV DONE bit has been set. It can be cleared by software. A power-up or bus reset will also clear it.
00-05	Not used	Read only	Reserved for future use.

TABLE 6-4 RECEIVER DATA BUFFER BIT DESCRIPTION

Bits	Name	Direction	Function
15	Error (ERR)	Read Only	There are two errors associated with the use of RBUF - the overrun error and the framing error. These set this bit as well as bits 14, 15 respectively.
14	Overrun Error (OR ERR)	Read only	If a new character is placed in the received data buffer before the previous one has been read then this bit is set. Bit 7 of the RCSR (RCV DONE) is cleared by reading the buffer. The bit is cleared when the next character along is moved in. It is also cleared on power-up.
13	Framing Error (FR ERR)	Read only	A framing error occurs if the DLART moves a byte into the buffer and is then unable to read a valid stop bit. This renders the character and the one following invalid. The next byte with a valid stop bit will cause the bit to be cleared. The bit is also cleared on power-up.

TABLE 6-4 RECEIVER DATA BUFFER BIT DESCRIPTION

Bits	Name	Direction	Function
12	Not used	Read only	Reserved for future use.
11	Received break (RCV BRK)	Read only	This bit is used to indicate that the DLART has started to receive. If the incoming signal, (SI), goes LO after a certain period it indicates that the DLART has finished receiving stop bits and has recieved a start bit. If this is the case then this bit goes LO for 11 bit periods. The bit will be reset by SI going HI again or by power-up.
08-10	Not used	Read only	Reserved for future use.
00-07	Received data buffer (RCV DATA BUFFER)	Read only	The 8 bits represent a buffer which contains the last byte which was received. The bits are cleared on power-up.

TABLE 6-5 TRANSMITTER CONTROL AND STATUS DESCRIPTION

Bits	Name	Direction	Function
08-15	Not used	Read only	Reserved for future use.
07	Transmitter ready (XMIT RDY)	Read only	A 1 in this position indicates that the current character has been sent. A new byte may be placed in the XMIT data buffer. Writing the byte in the buffer will clear the bit. Power-up will also clear it.
06	Transmitter interrupt enable (XMIT IE)	Read/write	This bit can be set by software and enables XMIT IRQ to be asserted on pin 29 of the DLART. This will occur at the same time as XMIT RDY is set and notifies the processor that the DLART is ready to transmit. The signal can be cleared under program control, by power-up and by bus reset.
03-05	None		Reserved for future use.

TABLE 6-5 TRANSMITTER CONTROL AND STATUS DESCRIPTION

Bits	Name	Direction	Function
02	Maintenance (MAINT)	Read/Write	This bit is not DLV11J compatible. It can be set or reset under program control. It disconnects SI from the AMP connector and connects it to SO for diagnostics.
01	None		Reserved for future use.
00	Transmit Break (XMIT BRK)	Read/write	Used under program control to start communication with external devices. When the bit is set HI SO will be held LO. The bit can be cleared by software. A power-up or bus reset will also reset it.

TABLE 6-6 TRANSMITTER DATA BUFFER BIT DESCRIPTIONS

Bits	Name	Direction	Function
08-15	Not used	Read only	Reserved for future use.
00-07	Transmit data buffer (XMIT DATA BUFFER)	Read/write	These 8 bits represent a data buffer which contains the next byte to be transmitted. Writing a byte to this buffer causes the XMIT RDY bit in the XCSR to be cleared. Power-up will clear these bits.

6.6 SERIAL LINE CABLES

Each serial line interfaces to the outside world through a 2X5 pin AMP connector. The positions of these connectors on the SBC M70 module are shown in figure 6.4. Figure 6.5 shows the AMP connector pin numbers. Table 6-7 gives the signal associated with each number.

For boards of Rev. F and higher, DEC provide cables suitable for communications with peripheral devices These are described in section 6.6.1. Guidelines for a user wishing to construct his own cables are given in section 6.6.2.

6.6.1 Digital Cables (Rev. F and higher only)

BC20N-05 A 5 foot RS-232C null modem cable used to interface to a local terminal (e.g. VT220). One end of the cable consists of an AMP 2x5 female connector and the other of RS-232C D-type female connector. Refer to figure 6.6.

BC20M-50 This cable is 50 feet long and requires that RS-423A be used. The cable can be use for transmission rates of up to 19,200 baud. Both ends consist of an AMP 2x5 female connector. A typical use would be communication between two SBC M70s by means of their serial lines.

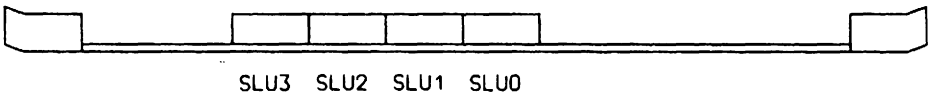

Fig. 6.4 Module Edge View.

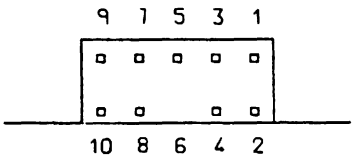

Fig. 6.5 AMP Connector.

TABLE 6-7 SLU CONNECTOR PIN DESIGNATIONS

Pin	Designation
1	NC
2	SIGNAL GND
3	TRX DATA+
4	SIGNAL GND
5	SIGNAL GND
6	INDEX KEY (no pin)
7	RECEIVED DATA-
8	RECEIVED DATA+
9	SIGNAL GND
10	12V (fused)

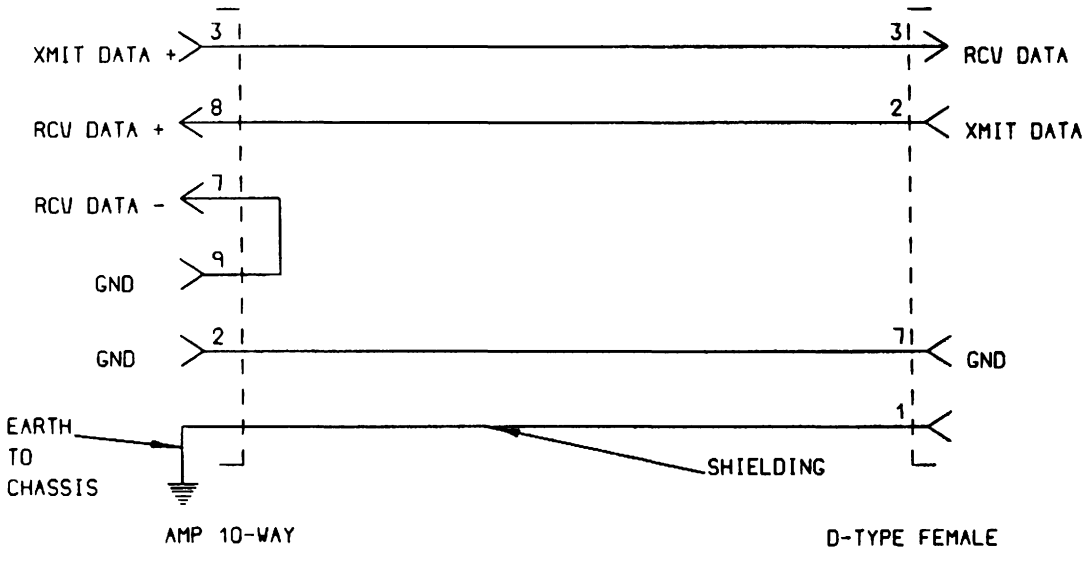

Fig. 6.6 Null Modem Cable.

6.6.2 User Cable Construction

This section outlines the factors which must be taken into consideration when designing a cable for use with the RS-232 standard. It does this by giving sample design procedures.

If the cable is intended to join the SBC M70 to an RS-232 terminal then the first step is the procurement of an AMP 2x5 female connector and a D-type female RS-232 connector. A loopback for the AMP connector is required. The objective is to connect the inverted inputs of the differential receivers to ground. Pin 7 (RECEIVE DATA-) is normally connected to pin 9 (ground).

For the SBC M70 to communicate correctly with the terminal it is necessary for transmit data outputs on the SBC M70 to connect to receive data inputs on the terminal and vice-versa i.e. the cable must be constructed as a null modem. Figure 6.5 and table 6-6 show where the relevant signals are on the AMP connector. Figure 6.7 and table 6-7 show the signals on the D-type female connector.

The connector is shown with the solder buckets facing outwards. Pin 3 on the SBC M70 (TRANSMIT DATA+) should be connected to pin 3 on the D-type connector (RS-232 RECEIVED DATA). Pin 8 on the SBC M70 (RECEIVED DATA+) should be connected to pin 2 of the D-type connector (RS-232 TRANSMITTED DATA). It is also usual to common the ground signals at each end by connecting Pin 2 on the SBC M70 (GROUND) to pin 7 on the D-type connector (RS-232 SIGNAL GROUND/COMMON RETURN).

Lastly, a shield connection is made from the chassis containing the SBC M70 to pin 1 on the D-type connector (PROTECTIVE GROUND). The cable length limitations of RS-232 should not be neglected in designing the cable. These are shown in table 6-1.

If the cable is to be used for communication between two SBC M70s or between one SBC M70 and a DL type device then two AMP female connectors are used and table 6-6 is used to determine which pins should be connected together. Transmit data pins should join to receive data pins and an earth should also be taken across.

The following AMP/DEC parts will be needed if cables are being constructed:

1). Cable receptacle:
AMP PN 87133-5
DEC PN 12-14268-02

2). Locking clip contacts:
AMP PN 87124-1
DEC PN 12-14267-00

3). Key pin (pin 6):
AMP PN 87179-1
DEC PN 12-15418-00

NOTE:- A Berg Header connector is used for SBC M70 module rev E and lower.

TABLE 6-7 D-TYPE CONNECTOR PIN DESIGNATIONS

Pin	Signal
1	Protective Ground
2	Transmitted Data
3	Received Data
7	Signal Ground/Common Return

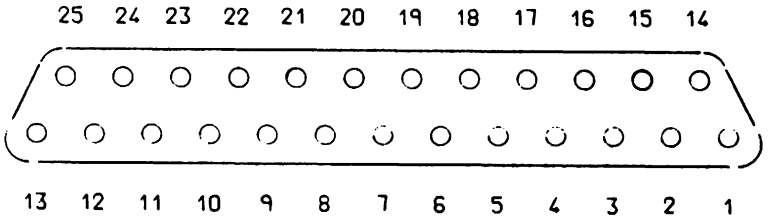

Fig. 6.7 25-Way Female D-type.
(View of Solder Buckets).

6.7 CONSOLE ODT

Octal Debugging Technique (ODT) is a program which is micro-coded in the DCJ11. When in ODT mode the processor will respond to certain commands sent to it from SLU3 when the latter is enabled as a console. These commands allow memory locations and registers to be examined and modified and programs to be started. Access to ODT is dependent on the processor mode and the state of the power-up register. Refer to DEC documentation for further information on console ODT.

APPENDIX A

BACKPLANE PIN UTILISATION

APPENDIX A - BACKPLANE PIN UTILISATION

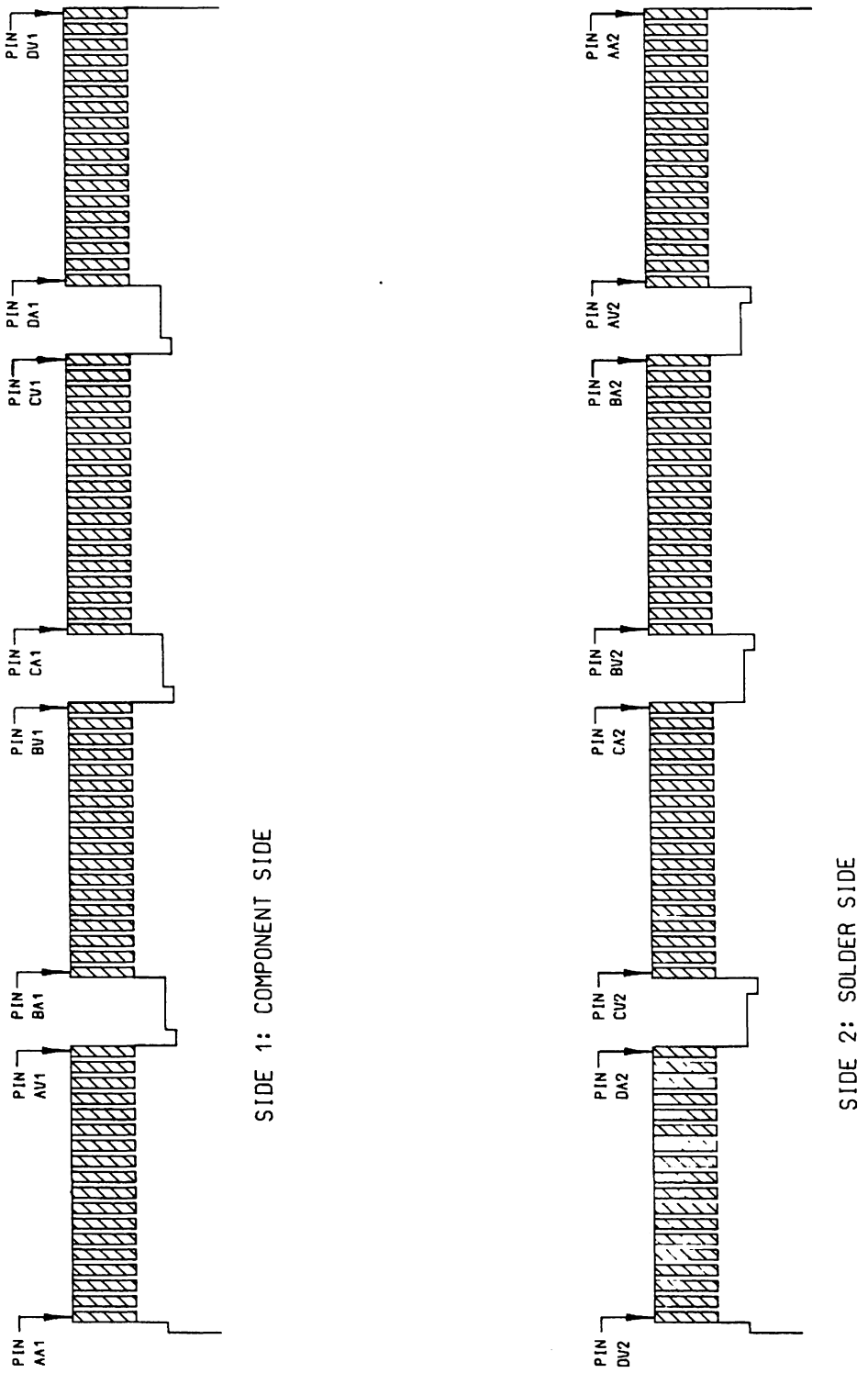

Fig. A.1 Backplane Edge Connector.

TABLE A-1 COMPONENT SIDE (Side 1)

Backplane Pin	SBC M70 Signal Function	LSI-11 Bus Signal Name
AA1	BIRQ5 L	BIRQ5 L
AB1	BIRQ6 L	BIRQ6 L
AC1	BDAL16 L	BDAL16 L
AD1	BDAL17 L	BDAL17 L
AE1	Not connected	SSPARE 1
AF1	SRUN	SRUN
AH1	Not connected	SSPARE 3
AJ1	GND	GND
AK1	Not connected	MSPAREA
AL1	Not connected	MSPAREB
AM1	GND	GND
AN1	BDMR L	BDMR L
AP1	BHALT	BHALT
AR1	Bus Terminator	BREF L
AS1	+5B	+5B
AT1	GND	GND
AU1	Not connected	PSPARE 1
AV1	+5B	+5B
BA1	BDCOK H	BDCOK H
BB1	BPOK H	BPOK H
BC1	BDAL18 L	BDAL18 L
BD1	BDAL19 L	BDAL19 L
BE1	BDAL20 L	BDAL20 L
BF1	BDAL21 L	BDAL21 L
BH1	Not connected	SSPARE8
BJ1	Not connected	GND
BK1	Not connected	MSPAREB
BL1	Not connected	MSPAREB
BM1	Not connected	GND
BN1	BSACK L	BSACK L
BP1	BIRQ7 L	BIRQ7 L
BR1	BEVNT L	BEVNT L
BS1	+12B	+12B
BT1	GND	GND
BU1	Not connected	PSPARE2
BV1	Not connected	+5V

WARNING

LSI-11 bus specification allows AS1 to be used for +12B or +5B. It must be +5B on the SBC M70 module.

TABLE A-1 Contd. COMPONENT SIDE (Side 2)

Backplane Pin	SBC M70 Signal Function	LSI-11 Bus Signal Name
AA2	+5 V	+5 V
AB2	Not connected	-12 V
AC2	GND	GND
AD2	+12 V	+12 V
AE2	BDOUT L	BDOUT L
AF2	BRPLY L	BRPLY L
AH2	BDIN L	BDIN L
AJ2	BSYNC L	BSYNC L
AK2	BWTBT L	BWTBT L
AL2	BIRQ4 L	BIRQ4 L
AM2	BIAKI L	BIAKI L
AN2	BIAKO L	BIAKO L
AP2	BBS7 L	BBS7 L
AR2	BDMGI L	BDMGI L
AS2	BDMGO L	BDMGO L
AT2	BINIT L	BINIT L
AU2	BDAL0 L	BDAL0 L
AV2	BDAL1 L	BDAL1 L
BA2	+5 V	+5 V
BB2	Not connected	-12 V
BC2	GND	GND
BD2	Not connected	+12 V
BE2	BDAL2 L	BDAL2 L
BF2	BDAL3 L	BDAL3 L
BH2	BDAL4 L	BDAL4 L
BJ2	BDAL5 L	BDAL5 L
BK2	BDAL6 L	BDAL6 L
BL2	BDAL7 L	BDAL7 L
BM2	BDAL8 L	BDAL8 L
BN2	BDAL9 L	BDAL9 L
LP2	BDAL10 L	BDAL10 L
BR2	BDAL11 L	BDAL11 L
BS2	BDAL12 L	BDAL12 L
BT2	BDAL13 L	BDAL13 L
BU2	BDAL14 L	BDAL14 L
BV2	BDAL15 L	BDAL15 L

NOTE:

The following pins on the C and D sections of the backplane edge connector are also used:

CA2 +5V power
CV1 +5V battery power
DV1 +5V power
CM2, CM2 BIAKI L, BIAKO L (linked)
CR2, CS2 BDMGI L, BDMGO L (linked)

APPENDIX B

DIAGNOSTICS AND PRODUCTION TESTS

APPENDIX - DIAGNOSTICS & PRODUCTION TESTS

B.1 INTRODUCTION

The purpose of the this chapter is to outline a scheme wherby the operation of the SBC M70 may be verified. The scheme includes environmental tests, power supply tests and software tests, including the running of self-test diagnostic programs. The operation of the SBC M70 with various DEC and DEC-compatible controllers is also verified.

B.2 DCJ11 DIAGNOSTICS

DEC do not provide diagnostics which will test the DCJ11 directly. Standard F11 diagnostics will run, however, if some slight variations are made to the programs. The programs which must be modified are as follows:

1). CJKDAD1 KT11 MMU diagnostic.

2). CJKDBD0 DCF11 processor diagnostic.

3). CJKDCB0 KEF11 floating point unit part 1.

4). CJKDDB0 KEF11 floating point unit part 2.

NOTE:- The leading C in the above names is a package designator and is not included in file names on disk.

The program CVMSAA0 will test memory in a DCJ11 based system without any alteration. Similarly, no alterations need be made to any diagnostics intended for peripheral controllers operating with a DCJ11 based system. Note, however, that the DEC DLART does not implement the reader run bit of the DLV11J. therefore the reader run test in the DLV11J diagnostic (CVDLAB0) must be patched out if it is intended to use this program to test serial lines implementing the DLART.

Table B-1 gives a representative selection of diagnostics which should run.

TABLE B-1 SBC M70 DIAGNOSTICS

Diagnostic	Device
VMSAA0	Memory
ZRLMB1 ZRLKB3 ZRLHB1	RL02 Disk
ZRMLB1 ZRMUB1	RM Disk
ZRXDC0	RX Floppy
ZRQBC1	RQ Floppy
ZTSHC0	TS11 Tape

B.3 DIAGNOSTIC PATCHING

The most convenient way to patch diagnostics, assuming that a version of the XXDP operating system is being used, is as follows:

The diagnostic is loaded into memory. A patch file which contains only the sections of code which are to be altered is then loaded over it. The relevant sections of the diagnostic are thus overwritten and the result may be saved back to disk or tape as a new program.

Mentec provides patch files for use with the five diagnostics which require alteration. These are supplied on a distribution medium, e.g. RX02 floppy disk. The medium also contains a command file to automatically perform the patching procedure. All of the files on the distribution medium should be copied to the system device before the patching procedure is attempted. The command file is called MPATA0.CMD. The following naming convention is used for the patch files:

The J in the original diagnostic name is replaced with an M and the file names have the extension .PAT. For example, the patch file for JKDAD1.BIC is MKDAD1.PAT. Listings of the patch files are available which give details of the patches and the reasons for them.

To execute the command file, proceed as follows. For XXDP+, run UPD2 and type: "DO MPATA0.CMD". For XXDP version 2, run UPDAT and type: "DO MPATA0.CMD".

NOTE:- That in both cases the command file must be on the system disk since the DO command will not accept device specifications.

The DO command also requires that the command file name extension be specified. In both cases the result of the command file execution is to write patched diagnostics to the system disk with the following naming convention: The original diagnostic name is retained with the J replaced with an M. For example, the patched version of JKDAD1.BIC is MKDAD1.BIC.

NOTE:- This procedure will not work unless the specified versions of the diagnostics are available on the system disk.

If it is desired to perform patching without using the command file then proceed as follows: Run UPD2 or UPDAT, depending on which version of XXDP is being used. Load the file to be patched using the LOAD command. Then load the relevant patch file. When XXDP loads these files it also provides the HICORE and LOCORE values and the transfer addresses. The core values give the highest and lowest addresses of the loaded image. The loaded image of the patch file will probably occupy different locations to the diagnostic image. Thus, to ensure that the full updated program will be saved back to the system device, the LOCORE value must be set to 0. The HICORE value is set to the HICORE value with which the original diagnostic was loaded or is left with the HICORE value of the patch file - the larger value is chosen. Refer to XXDP documentation for details of HICORE and LOCORE commands. Also, the updated program will be saved with the transfer address of the last loaded file i.e the patch file. This must be set to 200 if it does not already have this value. The updated program may be saved back to the system device with the DUMP command with whatever name is desired.

The complete procedure for the diagnostic JKDCB0 is now given. It is assumed that UPD2 or UPDAT is running:

```
*
*LOAD JKDCB0.BIC<CR>
JKDCB0.BIC    XFR:000001     CORE:000000,063117

*LOAD MKDCB0.PAT<CR>
MKDCB0.PAT    XFR:000000     CORE:056552,056554

*LOCORE<CR>
056552  0<CR>

*HICORE<CR>
056554  63117<CR>

*XFR<CR>
000000  200<CR>

*DUMP MKDCB0.BIC<CR>
*
*
```

APPENDIX C

OP CODES AND TRAPS

C APPENDIX C

C.1 NUMERICAL OP CODE LISTINGS

TABLE C-1 NUMERICAL OP CODES

OP Code	Mnemonic
00 00 00	Halt
00 00 01	Wait
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	Reset
00 00 06	RTT
00 00 07	Unused
00 00 77	Unused
00 01 DD	JMP
00 02 OR	RTS
00 02 10 to 00 02 27	Unused
00 02 3N	SPL
00 02 40	NOP
00 02 41 to 00 02 77	Cond Codes
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 65 SS	MFPI
00 66 DD	MTPI
00 67 DD	SXT
00 70 00 to 00 77 77	Unused
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD

TABLE C-1 contd. NUMERICAL OP CODES

OP Code	Mnemonic	OP Code	Mnemonic
07 0R SS	MUL	10 50 DD	CLRB
07 1R SS	DIV	10 51 DD	COMB
07 2R SS	ASH	10 52 DD	INCB
07 3R SS	ASHC	10 53 DD	DECB
07 4R DD	XOR	10 54 DD	NEGB
		10 55 DD	ADCB
10 65 SS	MFPD	10 56 DD	SBCB
10 67 DD	MFPS	10 57 DD	TSTB
00 00 07	MFPT		
10 66 DD	MTPD		
10 64 SS	MTPS	10 60 DD	RORB
		10 61 DD	ROLB
		10 62 DD	ASRB
07 50 40		10 63 DD	ASLB
to	Unused		
07 67 77			
		10 64 00	
		to	Unused
07 7R NN	SOB	10 64 77	
10 00 XXX	BPL		
10 04 XXX	BMI		
10 10 XXX	BHI		
10 14 XXX	BLOS		
10 20 XXX	BVC	10 67 00	
10 24 XXX	BVS	to	Unused
10 30 XXX	BCC, BHIS	10 77 77	
10 34 XXX	BCS, BLO		
		11 SS DD	MOVB
10 40 00		12 SS DD	CMPB
to	EMT	13 SS DD	BITB
10 43 77		14 SS DD	BICB
		15 SS DD	BISB
		16 SS DD	SUB
10 44 00			
to	TRAP		
10 47 77		00 70 DD	CSM
		00 72 DD	TSTSET
		00 73 DD	WRTLCK

TABLE C-1 contd. NUMERICAL OP CODES

OP Code	Mnemonic	OP Code	Mnemonic
1706 fdst	ABSD	171 (AC) fsrc	MULD
1706 fdst	ABSF	171 (AC) fsrc	MULF
172 (AC) fsrc	ADDD	1707 fdst	NEGD
172 (AC) fsrc	ADDF	1707 fdst	NEGE
170000	CFCC	170011	SETD
1704 fdst	CLRD	170001	SETF
1704 fdst	CLRF	170002	SETI
173 (AC+4)	CMPD	170012	SETL
173 (AC+4)	CMPF	176 (AC) fdst	STCDF
174 (AC+4)	DIVD	176 (AC) fdst	STCDI
174 (AC+4)	DIVF	176 (AC) fdst	STCDL
177 (AC+4)	LDCDF	176 (AC) fdst	STCFD
177 (AC+4)	LDCFD	175 (AC+4)	STCFI
177 (AC) src	LDCID	175 (AC+4)	STCFL
177 (AC) src	LDCIF	174 (AC) fdst	STD
177 (AC) src	LDCLD	175 (AC) dst	STEXP
177 (AC) src	LDCLF	174 (AC) fdst	STF
172 (AC+4)	LDD	1702 dst	STFPD
176 (AC+4)	LDEXP	1703 dst	STST
172 (AC+4)	LDF	173 (AC) fsrc	SUBD
1701 src	LDFPS	173 (AC) fsrc	SUBF
171 (AC+4)	MODD	1705 fdst	TSTD
171 (AC+4)	MODF	1705 fdst	TSTF

C.2 INTERRUPTS ASYNCHRONOUS & SYNCHRONOUS

TABLE C-2 INTERRUPTS

Interrupt	Vector Address
Address error (CPU error register, bit 6)	4
Red stack trap (CPU error register, bit 2)	4
Yellow stack trap (CPU error register, bit 3)	4
Timeout/nonexistent memory (CPU error register bits 4-5)	4
Parity error (Parity, Abort)	114
Memory management violation (MMR0, bits 13-15)	250
Trace (T bit) Trap (PSW, bit 4)	14
Power fail (PWRF)	24
FP exception (FPE)	244
EVENT/LTC	100
PIR 1 (PIRQ, bit 9)	240
PIR 2 (PIRQ, bit 10)	240
PIR 3 (PIRQ, bit 11)	240
PIR 4 (PIRQ, bit 12)	240
PIR 5 (PIRQ, bit 13)	240
PIR 6 (PIRQ, bit 14)	240
PIR 7 (PIRQ, bit 15)	240
Memory management	250
FP instruction exception (FPS bits <11:8> & 15	244
PIRQ	240
Memory parity error	114
TRAP (trap instruction)	34
EMT (emulator trap instruction)	30
IOT (I/O trap instruction)	20
BPT (breakpoint trap instruction)	14
Time out & reserved instruction	4

APPENDIX D

I/O PAGE MEMORY MAP

E APPENDIX E - DEVICE MNEMONICS

TABLE E-1 DEVICE MNEMONICS

Mnemonic	Device	Address
DX	RX01 Floppy	17777170
DY	RX02 Floppy	17777170
DL	RL01, RL02 Removable Disk	17774400
DU	MSCP Devices	17772150
DM	RK06/RK07 Removable Disk	17777440
DB	RM03 Fixed Disk	17776700
MS	TS11, TK25, TSV05, TU80 Tapes	17772522
MT	TS03, TU10, TE10 Tapes	17772522
DD	TU58 Tape Cartridge	17776500
VM 1	Not Applicable	
VM 2	Not Applicable	
MU	TK50 Tape Cartridge	17774500

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