LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1753
******* DIP MAP *******

26S10 DCXBUS x F30	74S260 DCECC xx E30	74LS273 DCECC x D30	74LS374 DCECC x C30	74S163 DCPOSC x B30	74S240 DCSTS x A30
26S10 DCXBUS x F29	26S10 DCXBUS x E29	74LS273 DCECC x D29	74LS374 DCECC x C29	74S163 DCPOSC x B29	74S133 DCPOSC x A29
26S10 DCXBUS x F28	26S10 DCXBUS x E28	74LS273 DCECC x D28	74S260 DCECC xx C28	74S163 DCPOSC x B28	74LS00 DCCMD xxxx A28
26S10 DCXBUS x F27	74LS86 DCECC xxxx E27	74LS273 DCECC x D27	74S133 DCECC x C27	74S163 DCPOSC x B27	74LS153 DCHDCM x A27
26S10 DCXBUS x F26	74LS374 DCCCW x E26	74LS374 DCCLP x D26	74S260 DCPOSC xx C26	74S133 DCPOSC x B26	74LS153 DCHDCM x A26
26S10 DCXBUS x F25	74LS374 DCCCW x E25	74LS569 DCCLP x D25	74LS374 DCCLP x C25	74LS244 DCPOSC x B25	74LS153 DCHDCM x A25
26S10 DCXBSA x F24	26S10 DCXBSA x E24	74LS273 DCSTS x D24	74LS374 DCCLP x C24	74LS244 DCPOSC x B24	74LS153 DCHDCM x A24
26S10 DCXBSA x F23	26S10 DCXBSA x E23	74LS569 DCCLP x D23	74LS04 DCCLP xxxxxx C23	74LS374 DCCLP x B23	25LS2536 DCHDCM x A23
26S10 DCXBSA x F22	74LS569 DCCCW x E22	74LS569 DCCLP x D22	25LS2521 DCHDCM x C22	74LS193 DCDA x B22	-------- -------- A22
26S10 DCXBSA x F21	74LS569 DCCCW x E21	74LS569 DCCLP x D21	74LS175 DCCMD x C21	74LS193 DCDA x B21	74LS193 DCDA x A21
26S10 DCPAR x F20	74LS74 DCCCW xx E20	9S42 DCUC xx D20	TD250 DCCHAN x C20	74LS244 DCDA x B20	74LS193 DCDA x A20

LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1754
******* DIP MAP *******

26S10 DCCHAN x F19	TD100 DCCHAN x E19	74S04 DCXBSA xxxxxx D19	74LS10 DCCMD xxx C19	74LS244 DCDA x B19	74LS193 DCDA x A19
26S10 DCCHAN x F18	74S11 DCCHAN xxx E18	74LS00 DCUC xxxx D18	74S51 DCCLK xx C18	74LS244 DCDA x B18	74LS193 DCDA x A18
9S42 DCCHAN xx F17	74S74 DCCHAN xx E17	74S08 DCUC xxxx D17	74S37 DCCLK xxxx C17	74LS244 DCDA x B17	74LS193 DCDA x A17
74LS74 DCCLK xx F16	74S02 DCREG xxxx E16	74LS08 DCUC xxxx D16	74LS32 DCCMD xxxx C16	74LS02 DCCLP xxxx B16	74LS86 DCSH xxxx A16
93S48 DCPAR x F15	74S133 DCREG x E15	74LS74 DCCLK xx D15	74LS08 DCRBUF xxxx C15	74LS21 DCBUSY xo B15	74LS244 DCSTS x A15
93S48 DCPAR x F14	25LS2521 DCREG x E14	74LS08 DCSH xxxx D14	74LS74 DCCLK xx C14	74S74 DCBUSY xx B14	74LS244 DCSTS x A14
93S48 DCPAR x F13	TD250 DCREG x E13	74LS138 DCUC x D13	74S74 DCCLK xx C13	74S260 DCBUSY xx B13	74LS244 DCSTS x A13
93S48 DCPAR x F12	74S138 DCREG x E12	74LS153 DCUC x D12	74LS273 DCSTS x C12	74LS279 DCSTS x B12	74LS244 DCSTS x A12
93S48 DCPAR x F11	74LS02 DCREG xxxx E11	74LS86 DCPAR xxxx D11	25LS2521 DCHDCM x C11	74LS32 DCSH xxxx B11	74S161 DCUC x A11
74LS374 DCRBUF x F10	67401 DCRBUF x E10	74S299 DCSH x D10	74LS273 DCCMD x C10	74S74 DCSH xx B10	75107 DCTRID xx A10
74LS374 DCRBUF x F09	67401 DCRBUF x E09	74LS11 DCCCW xxx D09	74LS244 DCDBUS x C09	26S02 DCTMOT xx B09	DUMMY DCTRID x A09

LISP Machine Disk Controller CADRDC:DC UML 10-DEC-80 1758
******* DIP MAP *******

74LS374 DCRBUF x F08	74LS175 DCRBUF x E08	74LS273 DCUI x D08	74LS244 DCDBUS x C08	74LS569 DCTRID x B08	75110 DCTRID x A08
74LS374 DCRBUF x F07	TD100 DCRBUF x E07	74LS273 DCUI x D07	74LS244 DCDBUS x C07	74LS569 DCTRID x B07	74LS14 DCTRID xxxxxo A07
74LS374 DCWBUF x F06	74LS21 DCRBUF xx E06	74LS273 DCUI x D06	74LS157 DCDBUS x C06	74LS74 DCBUSY xo B06	SIP330-1 DCTRSG x A06
74LS374 DCWBUF x F05	74LS08 DCSH xxxx E05	74S472 DCUI x D05	74LS04 DCDBUS xxxxxx C05	75452 DCTRSG xx B05	DUMMY DCTRSG x A05
74LS374 DCWBUF x F04	74LS00 DCSH xxox E04	74S472 DCUI x D04	DUMMY DCTMOT x C04	74LS124 DCTMOT xx B04	74LS14 DCTRSG xxxxxx A04
74LS374 DCWBUF x F03	74LS175 DCWBUF x E03	74S472 DCUI x D03	74 393 DCTMOT xx C03	75452 DCTRSG xx B03	DUMMY DCTRSG x A03
67401 DCWBUF x F02	74LS74 DCRBUF xx E02	-------- -------- D02	74LS569 DCUC x C02	SIP100-8 DCTRSG x B02	75452 DCTRSG xx A02
67401 DCWBUF x F01	TD100 DCWBUF x E01	74S299 DCSH x D01	74LS569 DCUC x C01	75452 DCTRSG xx B01	SIP100-8 DCTRSG x A01

LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1759
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-A-	-B-	-C-	-D-
A1 -XBUS35 A2 +5.0V++++++++++++++++++	A1 -XBUS5 A2 +5.0V++++++++++++++++++	#|A1 A2 +5.0V++++++++++++++++++	A1 A2 +5.0V++++++++++++++++++
B1 -XBUS34 B2 -6.0V	B1 -XBUS4 B2 -6.0V	#|B1 -XBUS41 B2 -5.0V	B1 B2 -5.0V
C1 -XBUS33 C2 GND---------- @	C1 -XBUS3 C2 GND---------- @	#|C1 -XBUS40 @|C2 GND---------- @	C1 C2 GND---------- @
D1 -XBUS32 D2 -XBUS31	D1 -XBUS2 #|D2 -XBUS1	#|D1 -XBUS39 #|D2 -XBUS.RQ	D1 #|D2 XINIT #
E1 -XBUS30 E2 -XBUS29	#|E1 -XBUS0 #|E2 -XBUS.PAR	#|E1 -XBUS38 #|E2 -XBUS.ACK	E1 #|E2 SEL UNIT ATTENTION
F1 GND F2 -XBUS28	@|F1 GND #|F2 -XADDR.PAR	@|F1 GND #|F2 -XBUS.WR	@|F1 GND @ #|F2 ANY ATTENTION
H1 -XBUS27 H2 -XBUS26	#|H1 -XADDR21 #|H2 -XADDR20	#|H1 -XBUS.EXTGRANT.IN #|H2 -XBUS.IGNPAR	#|H1 #|H2 UNIT 0 ATTENTION #
J1 -XBUS25 J2 -XBUS24	#|J1 -XADDR19 #|J2 -XADDR18	#|J1 -XBUS.EXTGRANT.OUT #|J2 -XBUS.INIT	#|J1 #|J2 -LOAD DA H #
K1 -XBUS23 K2 -XBUS22	#|K1 -XADDR17 #|K2 -XADDR16	#|K1 XBUS.POWER.OK #|K2 -XBUS.EXTRQ	K1 #|K2 NC #
L1 -XBUS21 L2 -XBUS20	#|L1 -XADDR15 #|L2 -XADDR14	#|L1 -XBUS37 #|L2 -XBUS.BUSY	L1 #|L2 NO SELECT #
M1 -XBUS19 M2 -XBUS18	#|M1 -XADDR13 #|M2 -XADDR12	#|M1 -XBUS36 #|M2 -XBUS.SYNC	M1 #|M2 MULTIPLE SELECT
N1 GND N2 -XBUS17	@|N1 GND #|N2 -XADDR11	@|N1 GND #|N2	@|N1 GND @ N2 WRITE DATA #
P1 -XBUS16 P2 -XBUS15	#|P1 -XADDR10 #|P2 -XADDR9	#|P1 #|P2 -XBUS.INTR	P1 +12.0V #|P2 WRITE GATE #
R1 -XBUS14 R2 -XBUS13	#|R1 -XADDR8 #|R2 -XADDR7	#|R1 #|R2	R1 +12.0V R2 DISK.CLK^ #
S1 -XBUS12 S2 -XBUS11	#|S1 -XADDR6 #|S2 -XADDR5	#|S1 #|S2	S1 +12.0V S2 READ DATA #
T1 GND---------- @ T2 -XBUS10	@|T1 GND---------- @ #|T2 -XADDR4	@|T1 GND---------- @ #|T2	T1 GND---------- @ T2 BLOCK.CLK^ #
U1 -XBUS9 U2 -XBUS8	#|U1 -XADDR3 #|U2 -XADDR2	#|U1 #|U2	U1 U2 BLOCK.CTR0 #
V1 -XBUS7 V2 -XBUS6	#|V1 -XADDR1 #|V2 -XADDR0	#|V1 #|V2	V1 V2 BLOCK.CTR1 #

LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1759
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-E-		-F-		-J01-		-J02-	
A1		A1		01 TRIDENT.CYL.TAG/	#	01	
A2 +5.0V++++++++++++++++++		A2 +5.0V++++++++++++++++++		02 TRIDENT.CONTROL.TAG/	#	02	
B1		B1		03 TRIDENT.TER.IN/		03	
B2 -5.0V		B2 -5.0V		04 GND	@	04	
C1		C1		05 GND	@	05	
C2 GND----------	@	C2 GND----------	@	06 GND	@	06	
D1		D1		07 GND	@	07	
D2 BLOCK.CTR2	#	D2		08 GND	@	08	
E1		E1		09 GND	@	09	
E2 BLOCK.CTR3	#	E2		10 GND	@	10	
F1 GND	@	F1 GND	@	11 GND	@	11	
F2 BLOCK.CTR4	#	F2		12 GND	@	12	
H1		H1		13 GND	@	13	
H2 BLOCK.CTR5	#	H2		14 GND	@	14	
J1		J1		15 GND	@	15	
J2 BLOCK.CTR6	#	J2		16 GND	@	16	
K1		K1		17 +5.0V		17	
K2 BLOCK.CTR7	#	K2		18 +5.0V		18	
L1		L1		19 TRIDENT.ADDR.MK.DET/		19	
L2 XBI28	#	L2		20 TRIDENT.SECTOR/		20	
M1		M1		21		21	
M2 XBI29	#	M2		22		22	
N1 GND	@	N1 GND	@	23		23	
N2 XBI30	#	N2		24		24	
P1		P1		25		25	
P2 UNIT0		P2		26 TRIDENT.HEAD.TAG/------	#	26 ----------	
R1		R1		27 TRIDENT.BUS0/----------	#	27 ----------	
R2 UNIT1		R2		28 TRIDENT.BUS1/----------	#	28 ----------	
S1		S1		29 TRIDENT.BUS2/----------	#	29 ----------	
S2 UNIT2		S2		30 TRIDENT.BUS3/----------	#	30 ----------	
T1 GND----------	@	T1 GND----------	@	31 TRIDENT.BUS4/----------	#	31 ----------	
T2 -CYLINDER TAG H	#	T2		32 TRIDENT.BUS5/----------	#	32 ----------	
U1		U1		33 TRIDENT.BUS6/----------	#	33 ----------	
U2 -HEAD TAG H	#	U2		34 TRIDENT.BUS7/----------	#	34 ----------	
V1		V1		35 TRIDENT.BUS8/----------	#	35 ----------	
V2		V2		36 TRIDENT.BUS9/----------	#	36 ----------	
				37 TRIDENT.SPARE/----------		37 ----------	
				38 TRIDENT.SEEK.INC/------	@	38 ----------	
				39 TRIDENT.ON.LINE/-------	@	39 ----------	
				40 TRIDENT.DEVICE.CHECK/--	@	40 ----------	
				41 TRIDENT.READ.ONLY/-----	@	41 ----------	
				42 TRIDENT.READY/---------	@	42 ----------	
				43 TRIDENT.INDEX/---------		43 ----------	
				44 TRIDENT.OFFSET/--------		44 ----------	
				45 TRIDENT.END.OF.CYL/----		45 ----------	
				46 ----------		46 ----------	
				47 ----------		47 ----------	
				48 ----------		48 ----------	
				49 ----------		49 ----------	
				50 ----------		50 ----------	

LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1759
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-J03-		-J04-		-J05-		-J06-	
01 GND	@	01	@	01 HI1	@	01	
02 GND	@	02		02 AD14		02	
03 GND	@	03	@	03 HI1	@	03	
04 GND	@	04		04 AD13		04	
05 GND	@	05	@	05 HI1	@	05	
06 GND	@	06		06 AD6		06	
07 GND	@	07	@	07 HI1	@	07	
08 GND	@	08		08 AD5		08	
09 GND	@	09	@	09 HI1	@	09	
10 +5.0V		10		10 AD4		10	
11		11	@	11 HI1	@	11	
12		12		12 AD3		12	
13		13	@	13 HI1	@	13	
14		14		14 AD2		14	
15		15	@	15 HI1	@	15	
16		16		16 -TIMEOUT ENB H		16	
17		17		17		17	
18		18		18		18	
19		19		19		19	
20		20		20		20	
21 TRIDENT.0.CLOCK.M------		21 ----------		21		21	
22 TRIDENT.0.CLOCK.P------		22 ----------		22		22	
23 TRIDENT.0.DATA.M-------	#	23 ----------		23		23	
24 TRIDENT.0.DATA.P-------	#	24 ----------		24		24	
25 TRIDENT.0.SELECT/------	#	25 ----------		25		25	
26 TRIDENT.0.SEQUENCE/----	#	26 ----------		26 ----------		26 ----------	
27 TRIDENT.0.SELECTED/----	@	27 ----------		27 GND----------	@	27 ----------	
28 TRIDENT.0.ATTENTION/---	@	28 ----------		28 ----------		28 ----------	
29 TRIDENT.0.COMPSECIDX/--	@	29 ----------		29 GND----------	@	29 ----------	
30 +5.0V----------		30 ----------		30 ----------		30 ----------	
31 ----------		31 ----------		31 GND----------	@	31 ----------	
32 ----------		32 ----------		32 ----------		32 ----------	
33 ----------		33 ----------		33 GND----------	@	33 ----------	
34 ----------		34 ----------		34 ----------		34 ----------	
35 ----------		35 ----------		35 GND----------	@	35 ----------	
36 ----------		36 ----------		36 ----------		36 ----------	
37 ----------		37 ----------		37 GND----------	@	37 ----------	
38 ----------		38 ----------		38 ----------		38 ----------	
39 ----------		39 ----------		39 GND----------	@	39 ----------	
40 ----------		40 ----------		40 ----------		40 ----------	
				41 GND----------	@	41 ----------	
				42 ----------		42 ----------	
				43 ----------		43 ----------	
				44 ----------		44 ----------	
				45 ----------		45 ----------	
				46 ----------		46 ----------	
				47 ----------		47 ----------	
				48 ----------		48 ----------	
				49 ----------		49 ----------	
				50 ----------		50 ----------	

LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1800
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-J07-	-J08-	-J09-	-J10-
01 02	01 02	01 02	01 02
03 04	03 04	03 04	03 04
05 06	05 06	05 06	05 06
07 08	07 08	07 08	07 08
09 10	09 10	09 10	09 10
11 12	11 12	11 12	11 12
13 14	13 14	13 14	13 14
15 16	15 16	15 16	15 16
17 18	17 18	17 18	17 18
19 20	19 20	19 20	19 20
21 ---------- 22 ----------	21 ---------- 22 ----------	21 22	21 22
23 ---------- 24 ----------	23 ---------- 24 ----------	23 24	23 24
25 ---------- 26 ----------	25 ---------- 26 ----------	25 26 ----------	25 26 ----------
27 ---------- 28 ----------	27 ---------- 28 ----------	27 ---------- 28 ----------	27 ---------- 28 ----------
29 ---------- 30 ----------	29 ---------- 30 ----------	29 ---------- 30 ----------	29 ---------- 30 ----------
31 ---------- 32 ----------	31 ---------- 32 ----------	31 ---------- 32 ----------	31 ---------- 32 ----------
33 ---------- 34 ----------	33 ---------- 34 ----------	33 ---------- 34 ----------	33 ---------- 34 ----------
35 ---------- 36 ----------	35 ---------- 36 ----------	35 ---------- 36 ----------	35 ---------- 36 ----------
37 ---------- 38 ----------	37 ---------- 38 ----------	37 ---------- 38 ----------	37 ---------- 38 ----------
39 ---------- 40 ----------	39 ---------- 40 ----------	39 ---------- 40 ----------	39 ---------- 40 ----------
		41 ---------- 42 ----------	41 ---------- 42 ----------
		43 ---------- 44* ----------	43 ---------- 44 ----------
		45 ---------- 46 ----------	45 ---------- 46 ----------
		47 ---------- 48 ----------	47 ---------- 48 ----------
		49 ---------- 50 ----------	49 ---------- 50 ----------

LISP Machine Disk Controller CADRDC;DC UML 10-DEC-80 1800
******* EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *******

-J11-		-J12-
01 LED.READ ACTIVE	#	01
02 LED.WRITE ACTIVE	#	02
03 LED.SEEK	#	03
04 LED.TRANSFER LOSSAGE	#	04
05 LED.FORMAT LOSSAGE	#	05
06 LED.ECC LOSSAGE	#	06
07 LED.DISK LOSSAGE	#	07
08 LED.UNUSED	#	08
09		09
10		10
11		11
12		12
13		13
14		14
15		15
16		16
17		17
18		18
19		19
20		20
21 ----------		21 ----------
22 ----------		22 ----------
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24 ----------		24 ----------
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26 ----------		26 ----------
27 ----------		27 ----------
28 ----------		28 ----------
29 ----------		29 ----------
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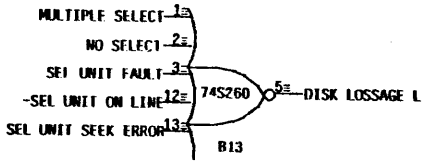
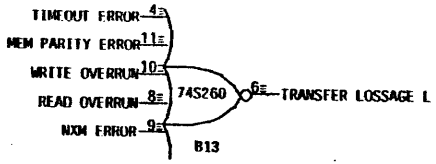
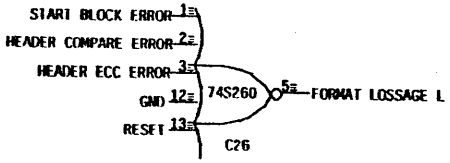
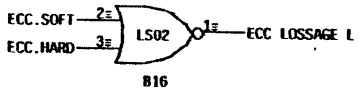
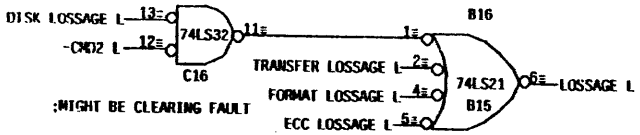
32 ----------		32 ----------
33 ----------		33 ----------
34 ----------		34 ----------
35 ----------		35 ----------
36 ----------		36 ----------
37 ----------		37 ----------
38 ----------		38 ----------
39 ----------		39 ----------
40 ----------		40 ----------

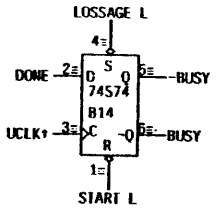


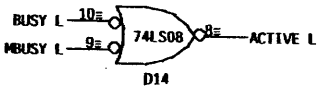


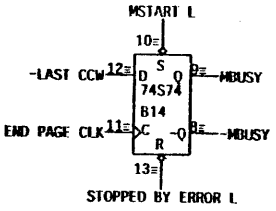


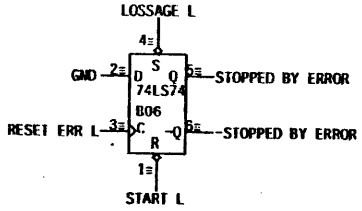




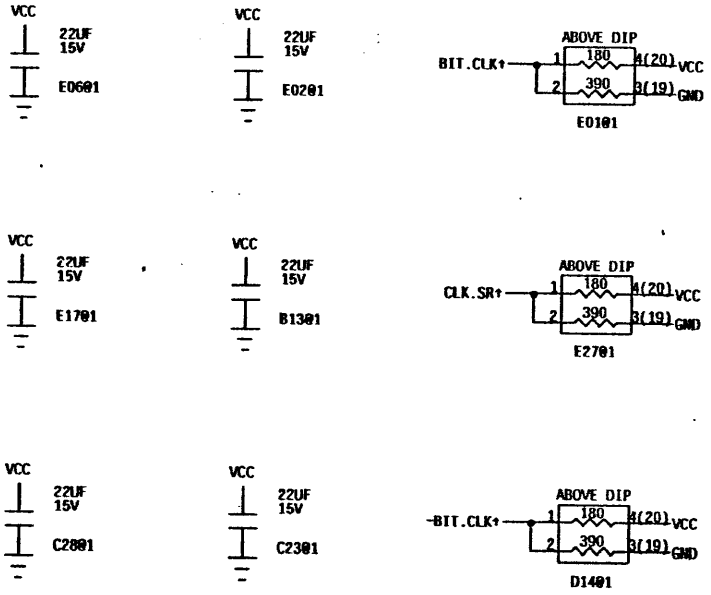


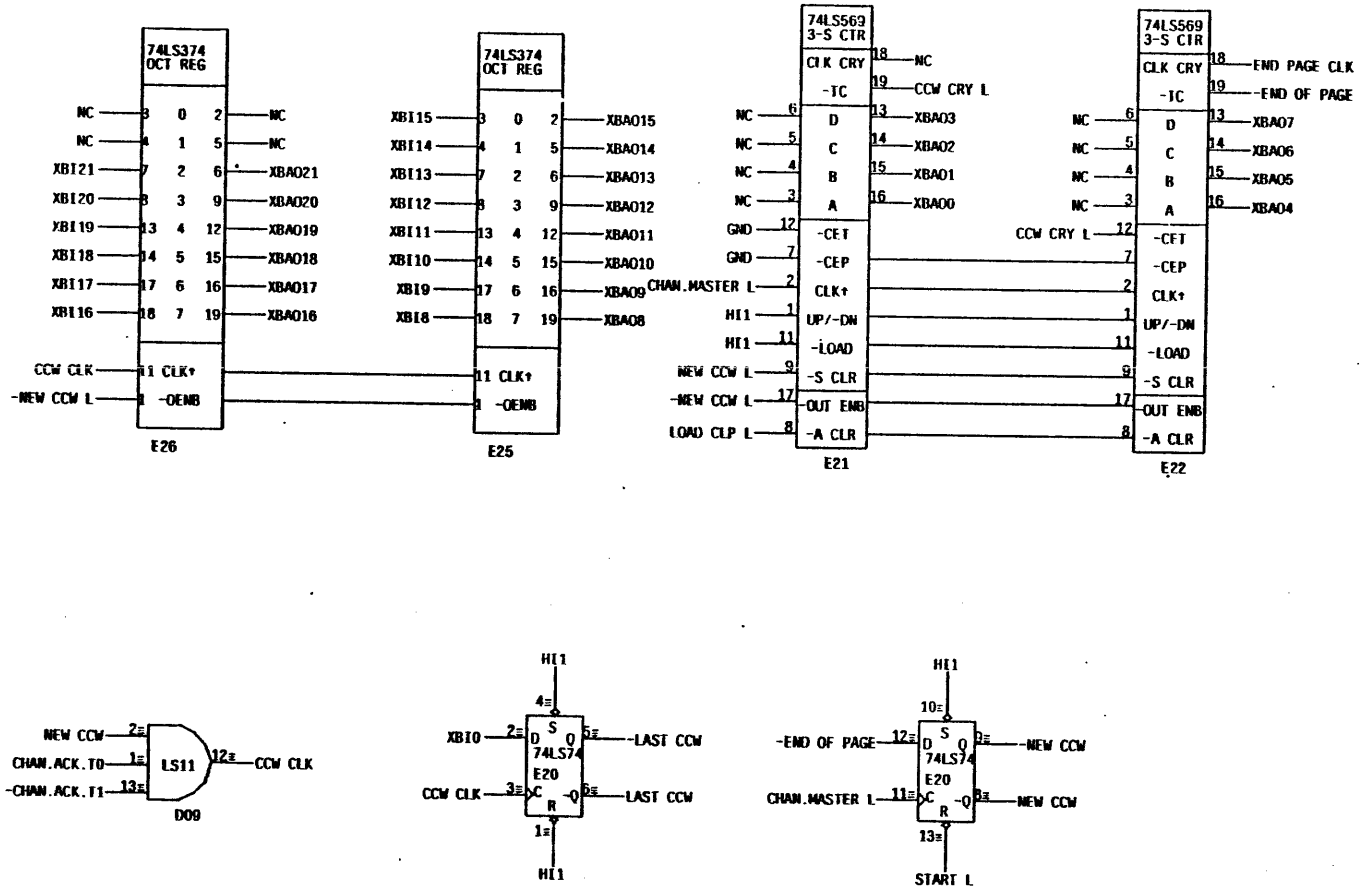


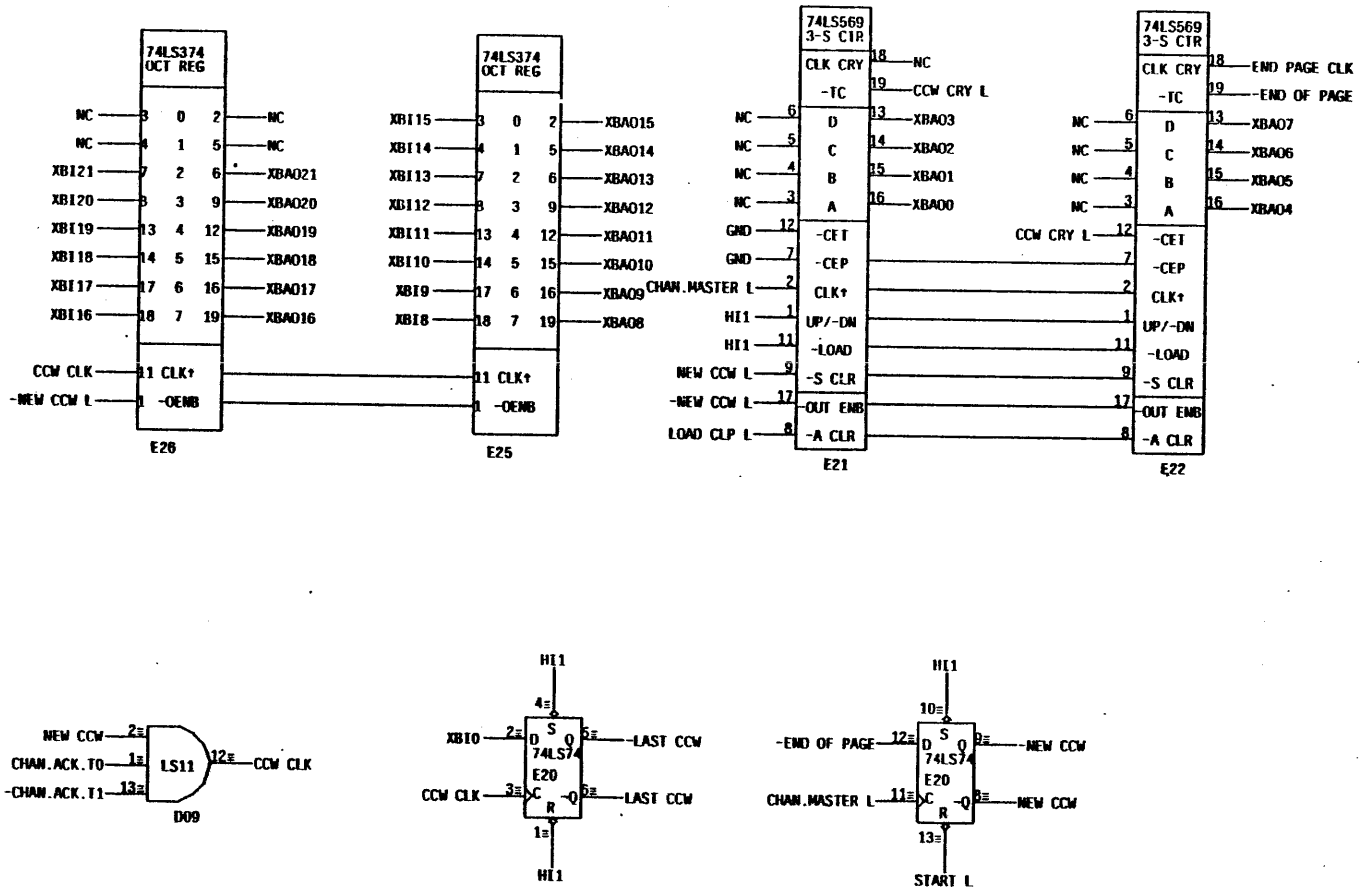


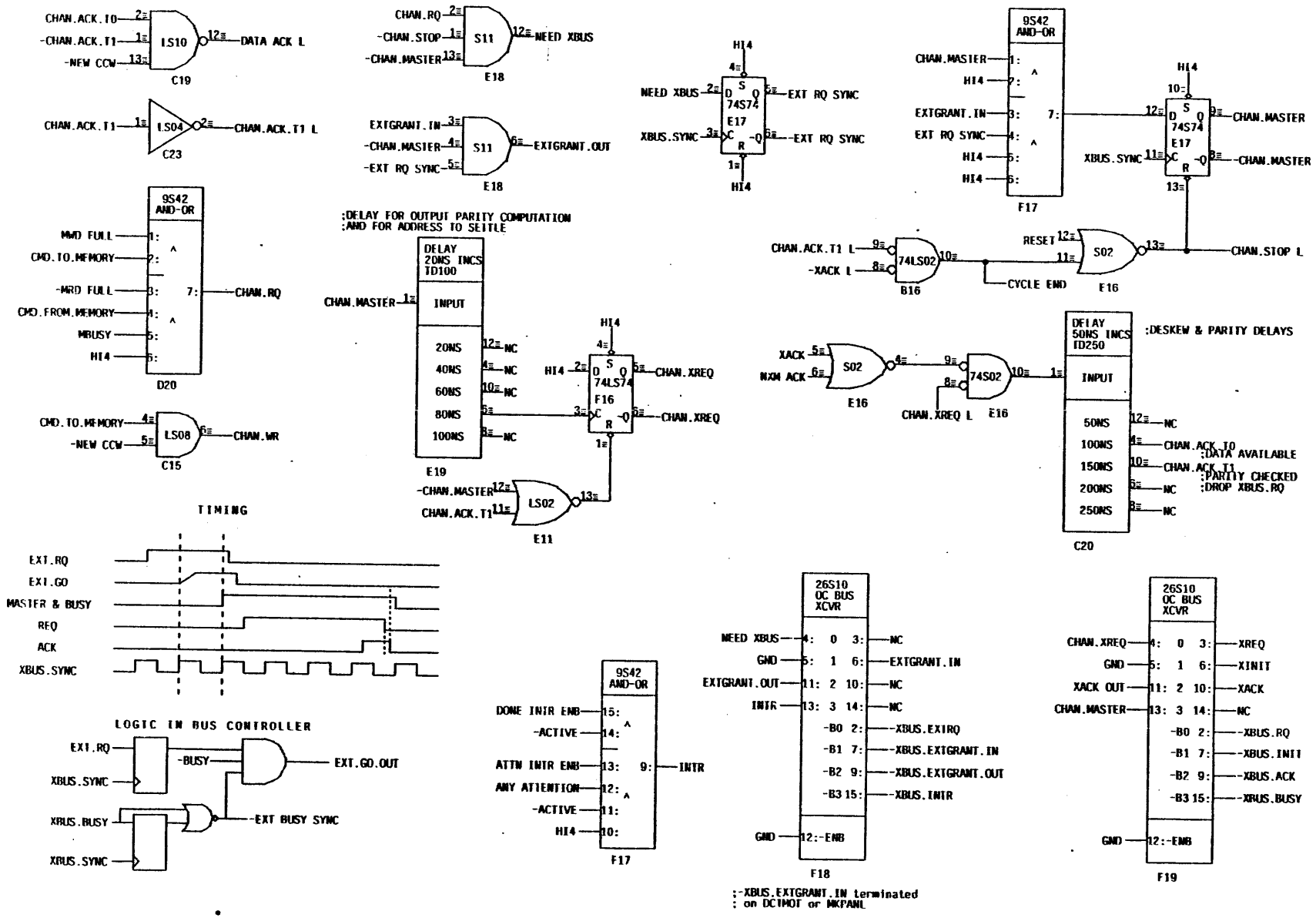


DISK CONTROL	BUSY, LOSSAGE	7-OCT-1980 21:32	AI: CADRDC; DCBUSY

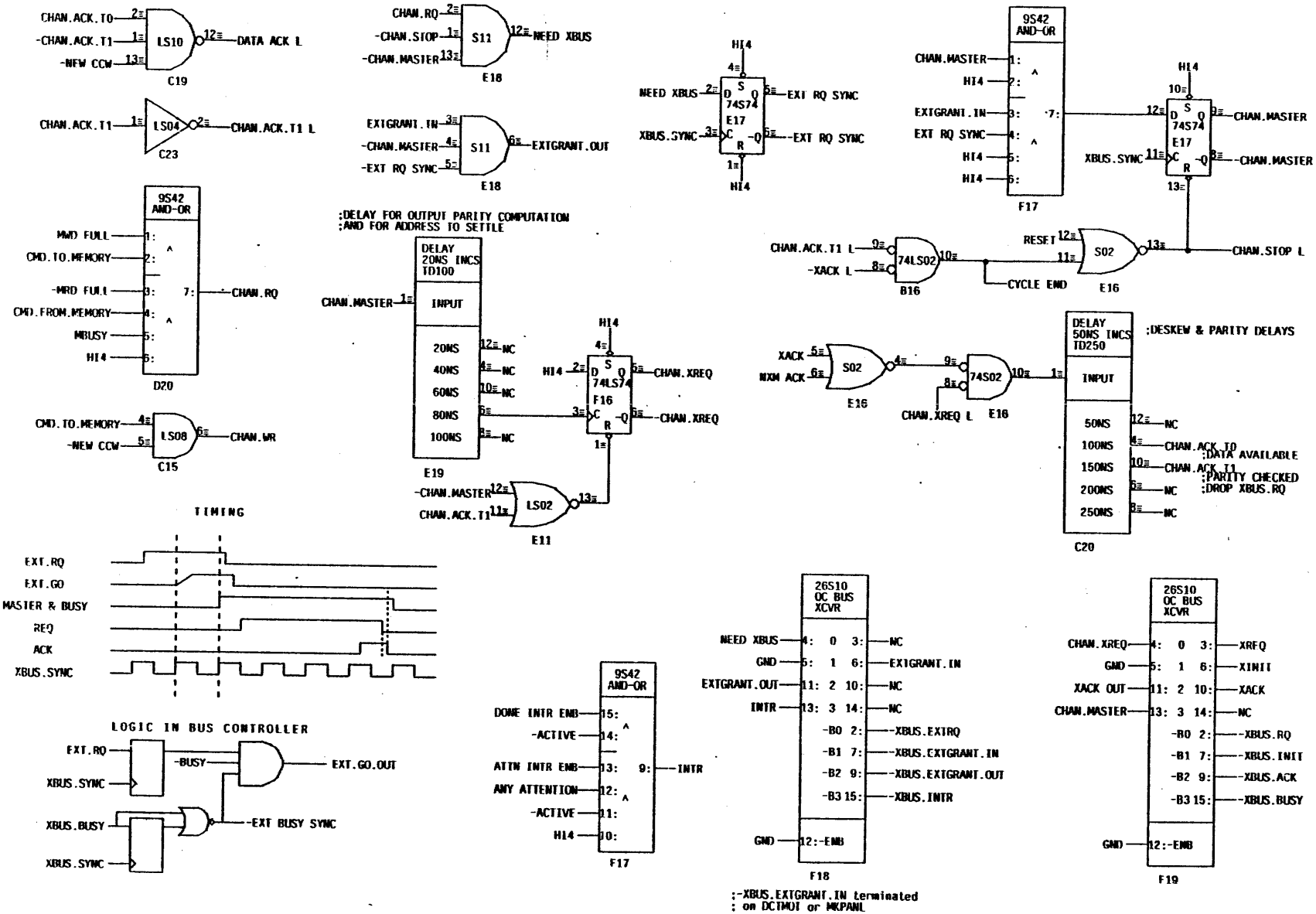

VCC
22UF
15V
E0601
VCC
22UF
15V
E0201
ABOVE DIP
BIT.CLK↑
180
390
4(20)
VCC
3(19)
GND
E0101
VCC
22UF
15V
E1701
VCC
22UF
15V
B1301
ABOVE DIP
CLK.SR↑
180
390
4(20)
VCC
3(19)
GND
E2701
VCC
22UF
15V
C2801
VCC
22UF
15V
C2301
ABOVE DIP
-BIT.CLK↑
180
390
4(20)
VCC
3(19)
GND
D1401


74LS374
OCT REG
NC
NC
XBI21
XBI20
XBI19
XBI18
XBI17
XBI16
CCW CLK
-NEW CCW L
XBA021
XBA020
XBA019
XBA018
XBA017
XBA016
E26
XBI15
XBI14
XBI13
XBI12
XBI11
XBI10
XBI9
XBI8
XBA015
XBA014
XBA013
XBA012
XBA011
XBA010
XBA09
XBA08
E25
74LS569
3-S CTR
CLK CRY
-TC
D
C
B
A
-CET
-CEP
CLK↑
UP/-DN
-LOAD
-S CLR
OUT ENB
-A CLR
GND
CHAN.MASTER L
HI1
NEW CCW L
-NEW CCW L
LOAD CLP L
CCW CRY L
XBA03
XBA02
XBA01
XBA00
E21
END PAGE CLK
-END OF PAGE
XBA07
XBA06
XBA05
XBA04
E22
NEW CCW
CHAN.ACK.T0
-CHAN.ACK.T1
LS11
CCW CLK
D09
XBI0
74LS74
E20
-LAST CCW
LAST CCW
-END OF PAGE
-NEW CCW
START L

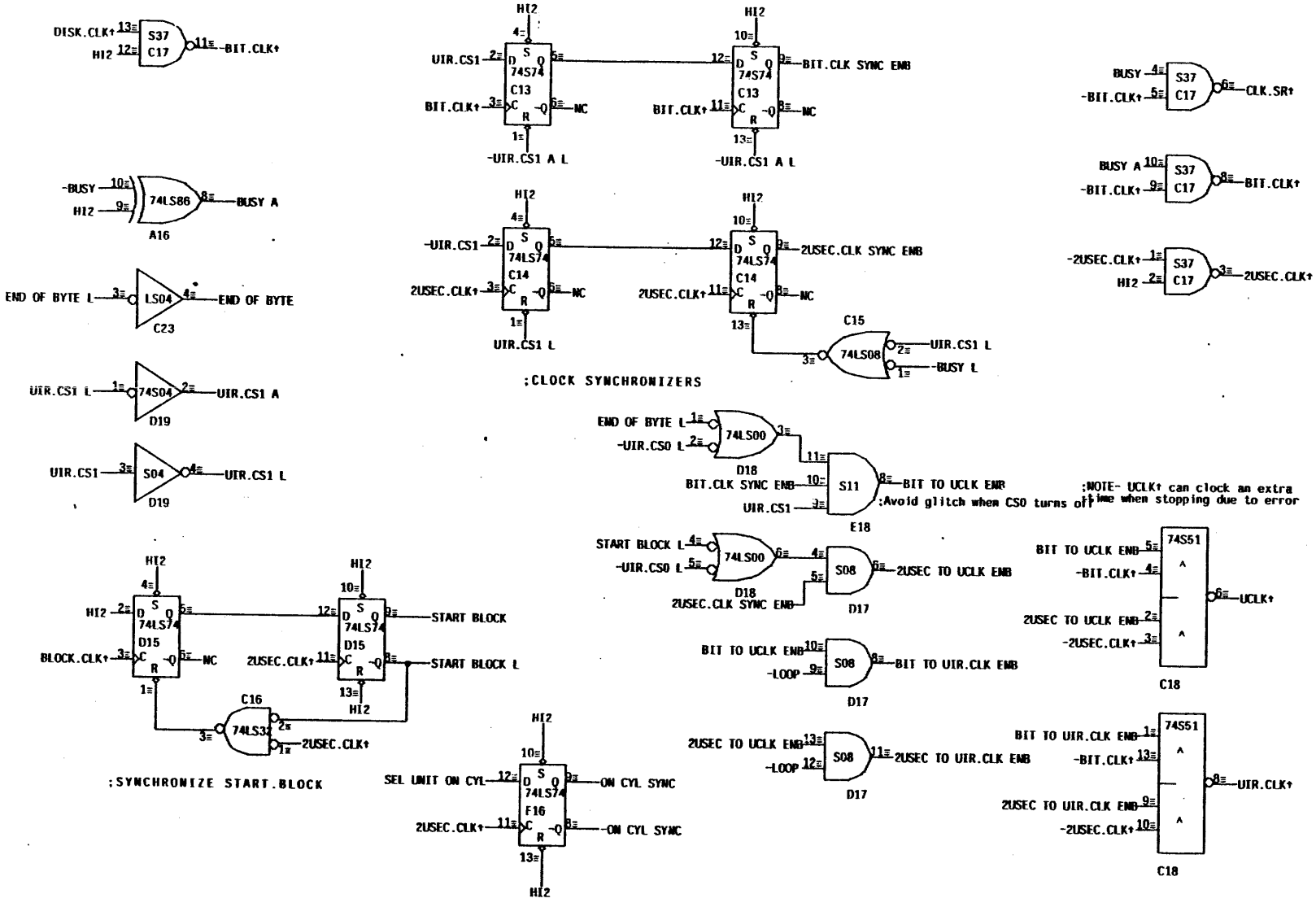

74LS374
OCT REG
NC
NC
XBI21
XBI20
XBI19
XBI18
XBI17
XBI16
XBA021
XBA020
XBA019
XBA018
XBA017
XBA016
CCW CLK
-NEW CCW L
E26
74LS374
OCT REG
XBI15
XBI14
XBI13
XBI12
XBI11
XBI10
XBI9
XBI8
XBA015
XBA014
XBA013
XBA012
XBA011
XBA010
XBA09
XBA08
E25
74LS569
3-S CTR
CLK CRY
-TC
D
C
B
A
-CET
-CEP
CLK↑
UP/-DN
-LOAD
-S CLR
-OUT ENB
-A CLR
NC
CCW CRY L
XBA03
XBA02
XBA01
XBA00
GND
CHAN.MASTER L
HI1
NEW CCW L
LOAD CLP L
E21
END PAGE CLK
-END OF PAGE
XBA07
XBA06
XBA05
XBA04
E22
NEW CCW
CHAN.ACK.T0
-CHAN.ACK.T1
LS11
CCW CLK
D09
XBI0
74LS74
E20
LAST CCW
-END OF PAGE
NEW CCW
START L



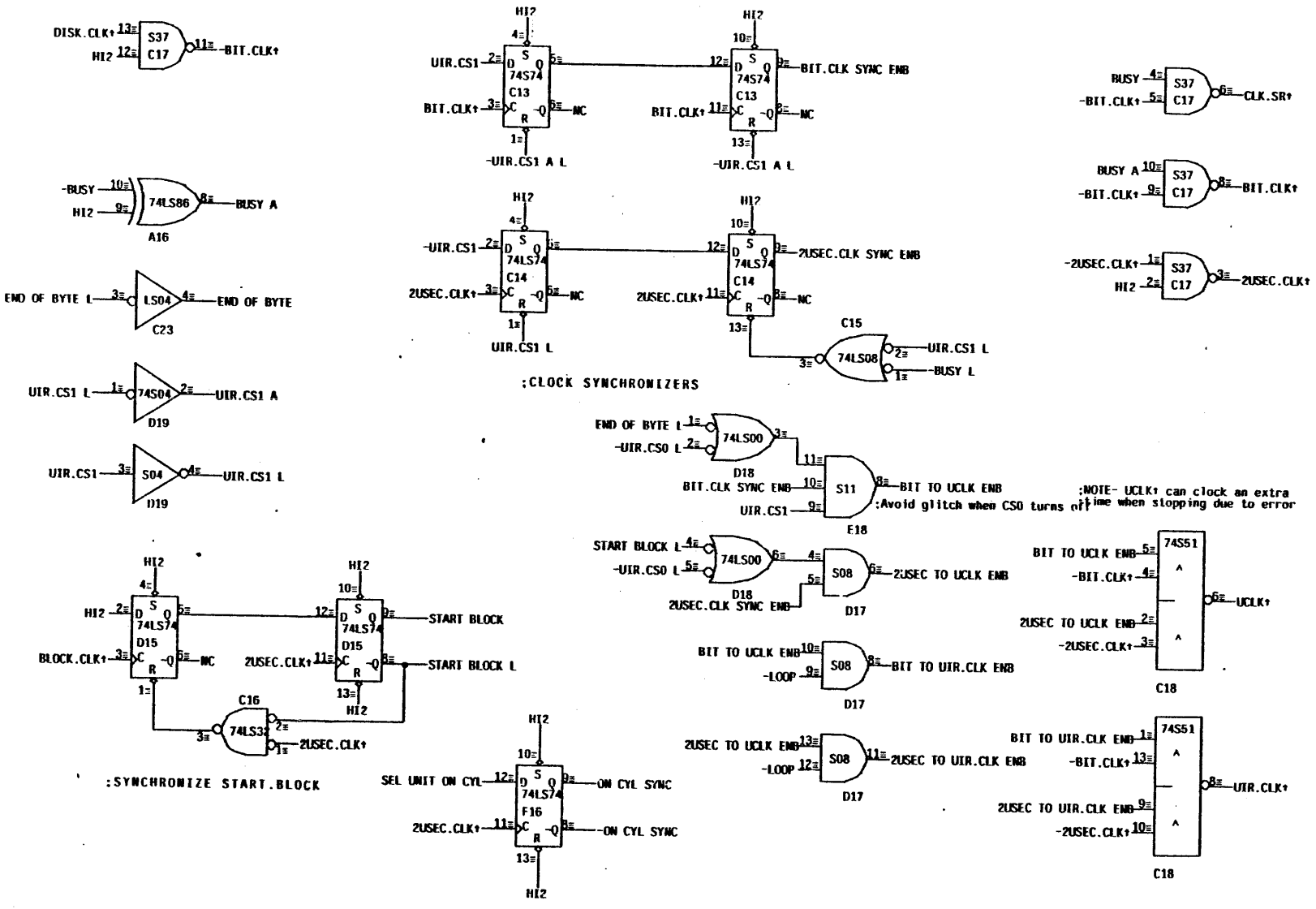
DISK CONTROL	DMA CHANNEL CONTROL	6-FEB-1980 00:48	AI: CADRDC; DCCHAN



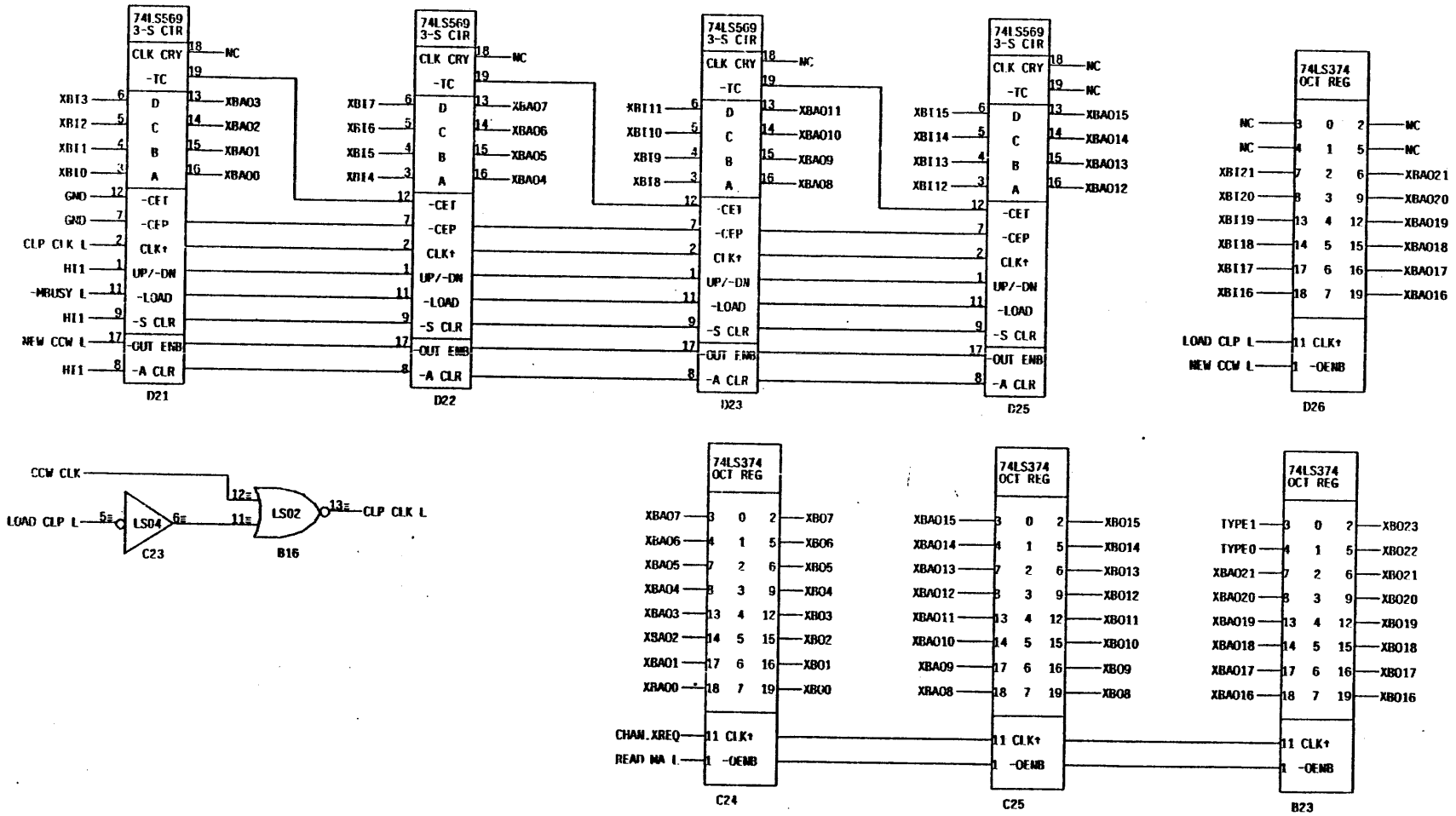
DISK CONTROL	DMA CHANNEL CONTROL	6-FEB-1980 00:48	AI: CADRDC; DCCHAN

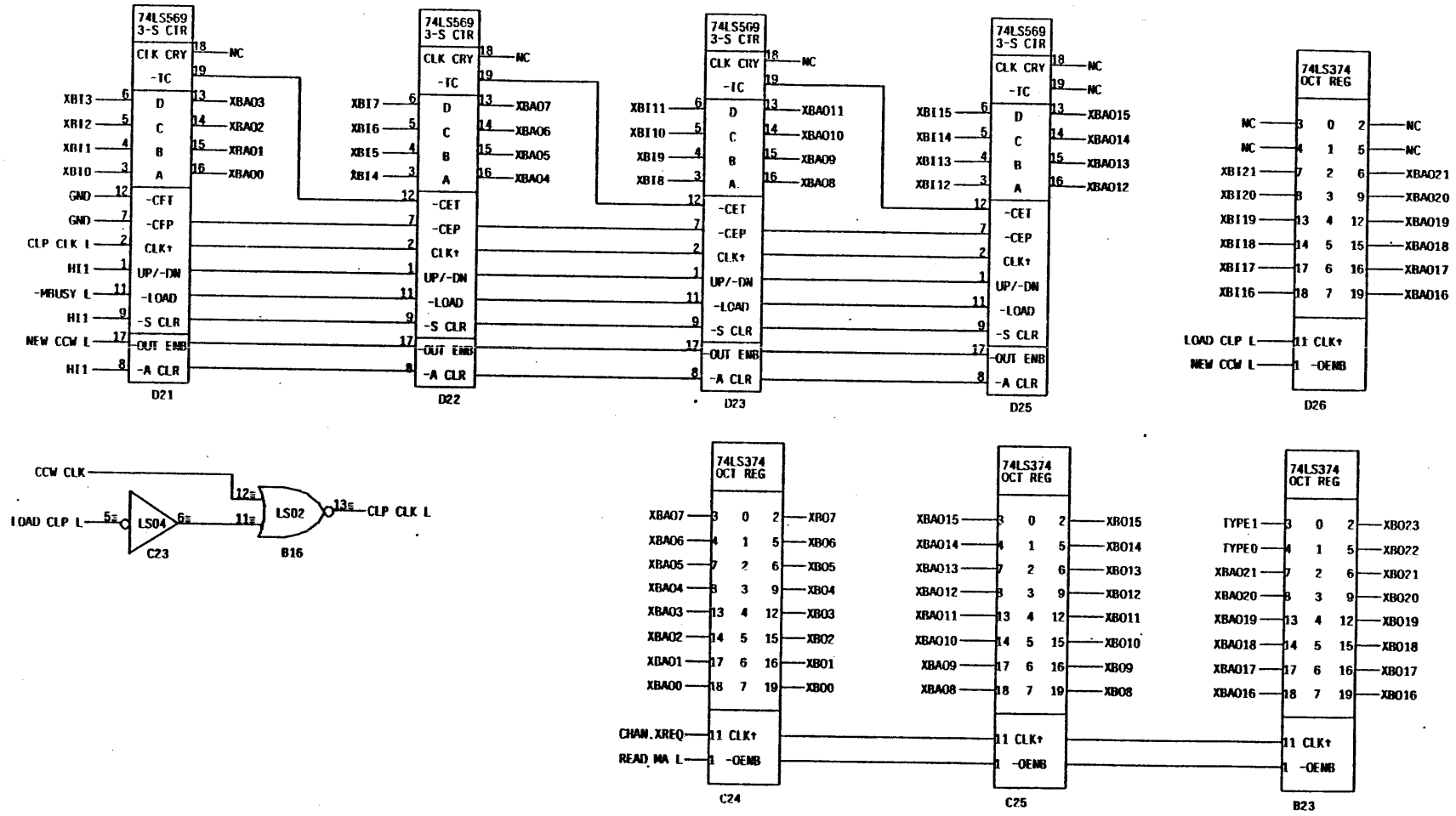


DISK CONTROL	CLOCKS	8-OCT-1978 16:48	AI: CADRDC; DCCLK



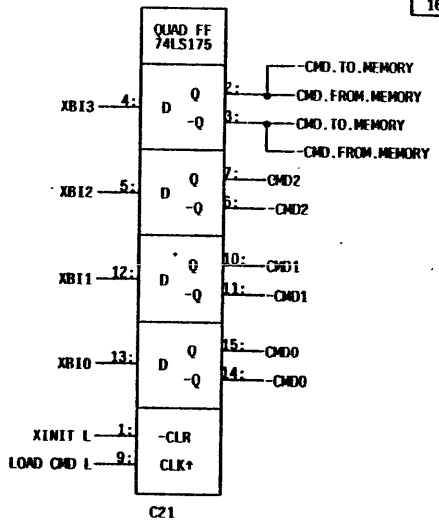
DISK CONTROL	CLOCKS	8-OCT-1978 16:48	AI: CADRDC; DCCLK

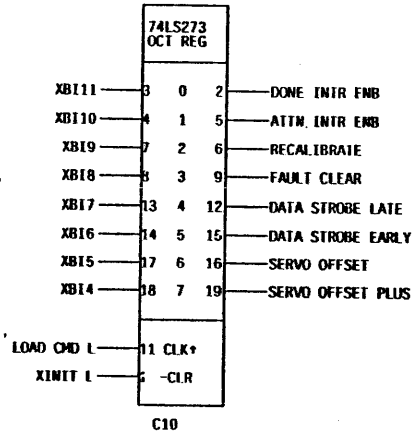

74LS569
3-S CTR
CLK CRY
-TC
D
C
B
A
-CET
-CEP
CLK↑
UP/-DN
-LOAD
-S CLR
-OUT ENB
-A CLR
NC
XBI3
XBI2
XBI1
XBI0
GND
GND
CLP CLK L
HI1
-MBUSY L
HI1
NEW CCW L
HI1
XBA03
XBA02
XBA01
XBA00
D21
XBI7
XBI6
XBI5
XBI4
XBA07
XBA06
XBA05
XBA04
D22
XBI11
XBI10
XBI9
XBI8
XBA011
XBA010
XBA09
XBA08
D23
XBI15
XBI14
XBI13
XBI12
XBA015
XBA014
XBA013
XBA012
D25
74LS374
OCT REG
NC
NC
XBI21
XBI20
XBI19
XBI18
XBI17
XBI16
LOAD CLP L
NEW CCW L
CLK↑
-OENB
XBA021
XBA020
XBA019
XBA018
XBA017
XBA016
D26
CCW CLK
LOAD CLP L
LS04
LS02
CLP CLK L
C23
B16
XBA07
XBA06
XBA05
XBA04
XBA03
XBA02
XBA01
XBA00
CHAN.XREQ
READ MA L
XB07
XB06
XB05
XB04
XB03
XB02
XB01
XB00
C24
XBA015
XBA014
XBA013
XBA012
XBA011
XBA010
XBA09
XBA08
XB015
XB014
XB013
XB012
XB011
XB010
XB09
XB08
C25
TYPE1
TYPE0
XBA021
XBA020
XBA019
XBA018
XBA017
XBA016
XB023
XB022
XB021
XB020
XB019
XB018
XB017
XB016
B23

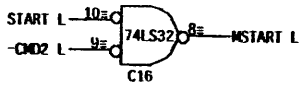


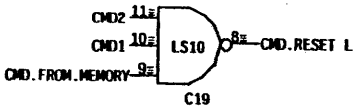
DISK CONTROL	COMMAND LIST POINTER	10-JUN-1979 21:52	AI: CADRDC; DCCLP

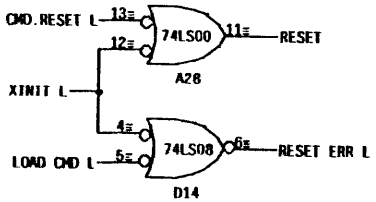
CMD	OPERATION
00	READ
10	READ COMPARE
11	WRITE
02	READ ALL
13	WRITE ALL
04	SEEK
05	AT EASE
1005	RECALIBRATE
405	FAULT CLEAR
06	OFFSET CLEAR
16	STOP, RESET

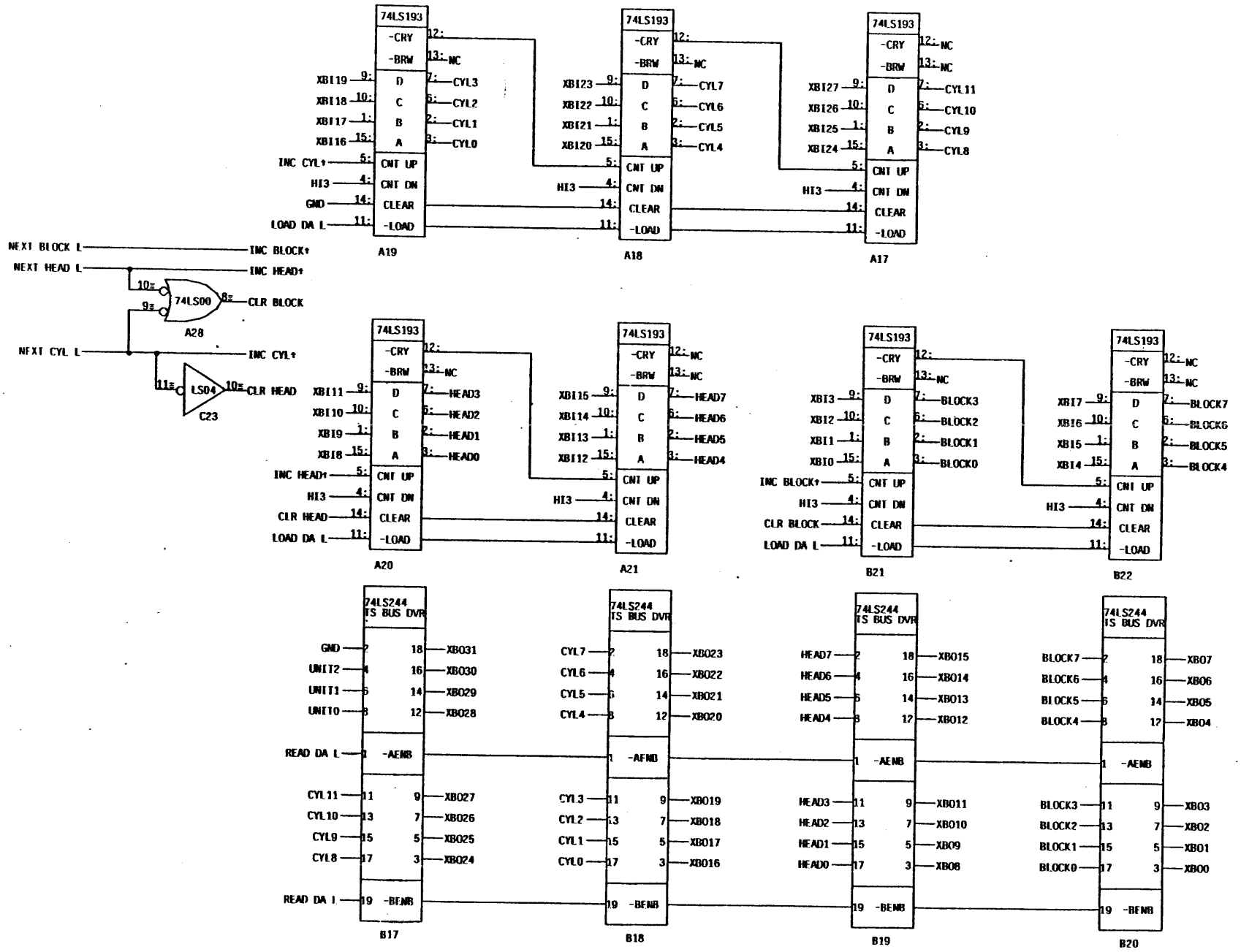


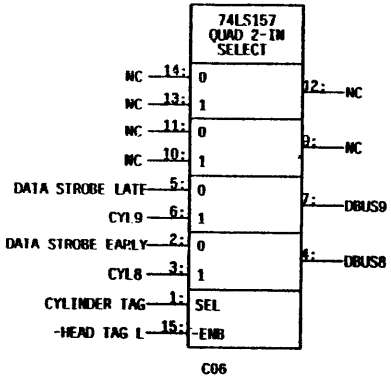


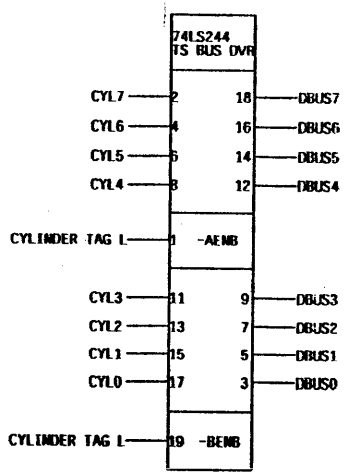


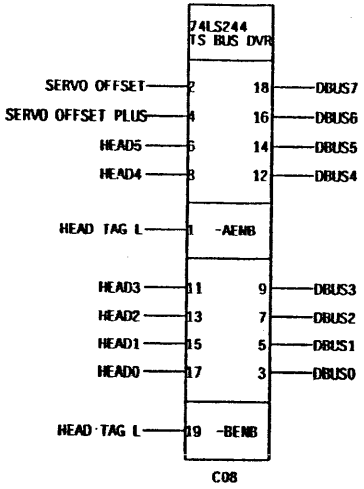


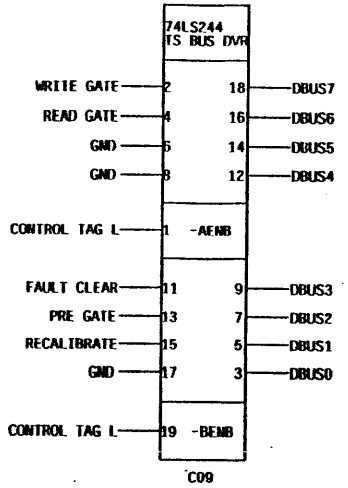


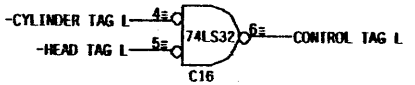

74LS193
-CRY
-BRW
D
C
B
A
CNT UP
CNT DN
CLEAR
-LOAD
A19
A18
A17
A20
A21
B21
B22
74LS00
A28
LS04
C23
74LS244
TS BUS DVR
-AENB
-BENB
B17
B18
B19
B20
NEXT BLOCK L
NEXT HEAD L
NEXT CYL L
INC BLOCK↑
INC HEAD↑
INC CYL↑
CLR BLOCK
CLR HEAD
LOAD DA L
READ DA L
HI3
GND
NC
CYL0
CYL1
CYL2
CYL3
CYL4
CYL5
CYL6
CYL7
CYL8
CYL9
CYL10
CYL11
HEAD0
HEAD1
HEAD2
HEAD3
HEAD4
HEAD5
HEAD6
HEAD7
BLOCK0
BLOCK1
BLOCK2
BLOCK3
BLOCK4
BLOCK5
BLOCK6
BLOCK7
UNIT0
UNIT1
UNIT2
XB031
XB030
XB029
XB028
XB027
XB026
XB025
XB024
XB023
XB022
XB021
XB020
XB019
XB018
XB017
XB016
XB015
XB014
XB013
XB012
XB011
XB010
XB09
XB08
XB07
XB06
XB05
XB04
XB03
XB02
XB01
XB00

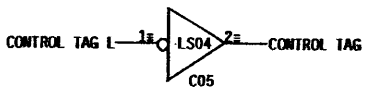

74LS157
QUAD 2-IN
SELECT
NC
NC
NC
NC
DATA STROBE LATE
CYL9
DATA STROBE EARLY
CYL8
CYLINDER TAG
-HEAD TAG L
SEL
-ENB
NC
NC
DBUS9
DBUS8
C06

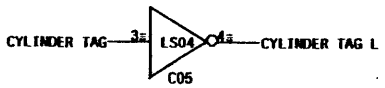

74LS244
TS BUS DVR
CYL7
CYL6
CYL5
CYL4
CYLINDER TAG L
CYL3
CYL2
CYL1
CYL0
CYLINDER TAG L
-AENB
-BENB
DBUS7
DBUS6
DBUS5
DBUS4
DBUS3
DBUS2
DBUS1
DBUS0
C07

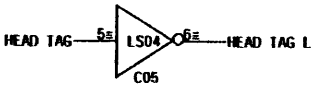

74LS244
TS BUS DVR
SERVO OFFSET
SERVO OFFSET PLUS
HEAD5
HEAD4
HEAD TAG L
HEAD3
HEAD2
HEAD1
HEAD0
HEAD TAG L
-AENB
-BENB
DBUS7
DBUS6
DBUS5
DBUS4
DBUS3
DBUS2
DBUS1
DBUS0
C08

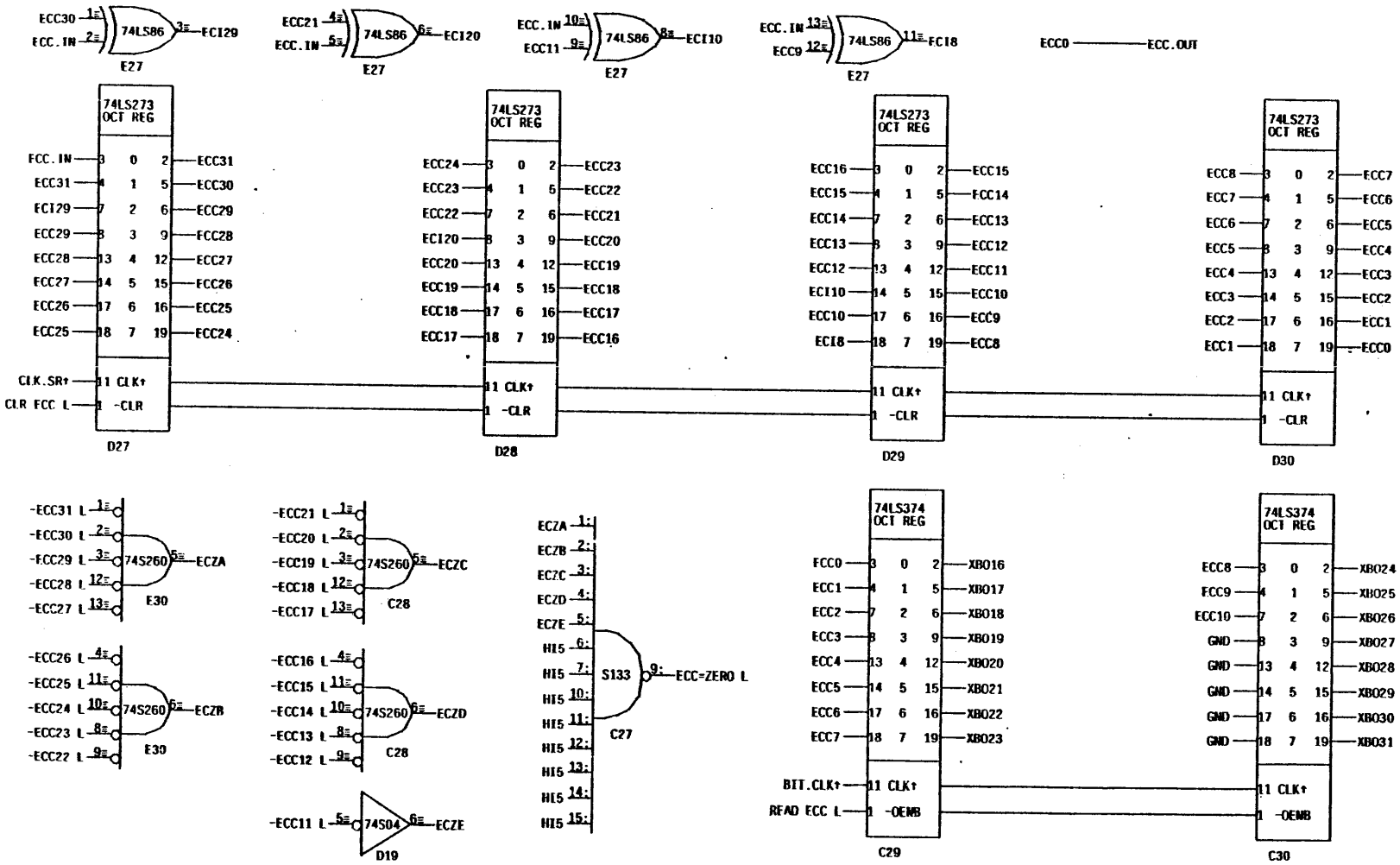

74LS244
TS BUS DVR
WRITE GATE
READ GATE
GND
GND
CONTROL TAG L
FAULT CLEAR
PRE GATE
RECALIBRATE
GND
CONTROL TAG L
-AENB
-BENB
DBUS7
DBUS6
DBUS5
DBUS4
DBUS3
DBUS2
DBUS1
DBUS0
C09


-CYLINDER TAG L
-HEAD TAG L
74LS32
CONTROL TAG L
C16

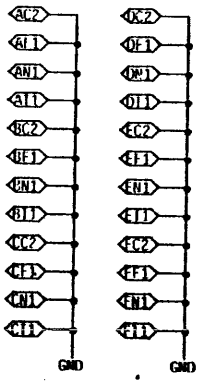

CONTROL TAG L
LS04
CONTROL TAG
C05


CYLINDER TAG
LS04
CYLINDER TAG L
C05


HEAD TAG
LS04
HEAD TAG L
C05


ECC30
ECC.IN
74LS86
ECI29
E27
ECC21
ECC.IN
74LS86
ECI20
E27
ECC.IN
ECC11
74LS86
ECI10
E27
ECC.IN
ECC9
74LS86
ECI8
E27
ECC0
ECC.OUT
74LS273 OCT REG
ECC.IN
ECC31
ECI29
ECC29
ECC28
ECC27
ECC26
ECC25
CLK.SR↑
CLR ECC L
ECC31
ECC30
ECC29
ECC28
ECC27
ECC26
ECC25
ECC24
D27
74LS273 OCT REG
ECC24
ECC23
ECC22
ECI20
ECC20
ECC19
ECC18
ECC17
ECC23
ECC22
ECC21
ECC20
ECC19
ECC18
ECC17
ECC16
D28
74LS273 OCT REG
ECC16
ECC15
ECC14
ECC13
ECC12
ECI10
ECC10
ECI8
ECC15
ECC14
ECC13
ECC12
ECC11
ECC10
ECC9
ECC8
D29
74LS273 OCT REG
ECC8
ECC7
ECC6
ECC5
ECC4
ECC3
ECC2
ECC1
ECC7
ECC6
ECC5
ECC4
ECC3
ECC2
ECC1
ECC0
D30
-ECC31 L
-ECC30 L
-ECC29 L
-ECC28 L
-ECC27 L
74S260
ECZA
E30
-ECC26 L
-ECC25 L
-ECC24 L
-ECC23 L
-ECC22 L
74S260
ECZB
E30
-ECC21 L
-ECC20 L
-ECC19 L
-ECC18 L
-ECC17 L
74S260
ECZC
C28
-ECC16 L
-ECC15 L
-ECC14 L
-ECC13 L
-ECC12 L
74S260
ECZD
C28
-ECC11 L
74S04
ECZE
D19
ECZA
ECZB
ECZC
ECZD
ECZE
HI5
HI5
HI5
HI5
HI5
HI5
HI5
HI5
S133
ECC=ZERO L
C27
74LS374 OCT REG
ECC0
ECC1
ECC2
ECC3
ECC4
ECC5
ECC6
ECC7
BIT.CLK↑
READ ECC L
XB016
XB017
XB018
XB019
XB020
XB021
XB022
XB023
C29
74LS374 OCT REG
ECC8
ECC9
ECC10
GND
GND
GND
GND
GND
XB024
XB025
XB026
XB027
XB028
XB029
XB030
XB031
C30

GROUNDS



JUMPERS FOR 1-BOARD VERSION:

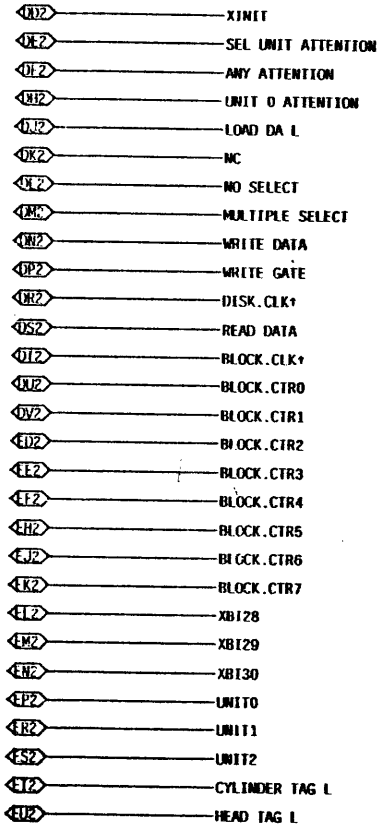
DE2 - DF2 - DH2
DN1 - DM2
ET1 - EP2 - ER2 - ES2

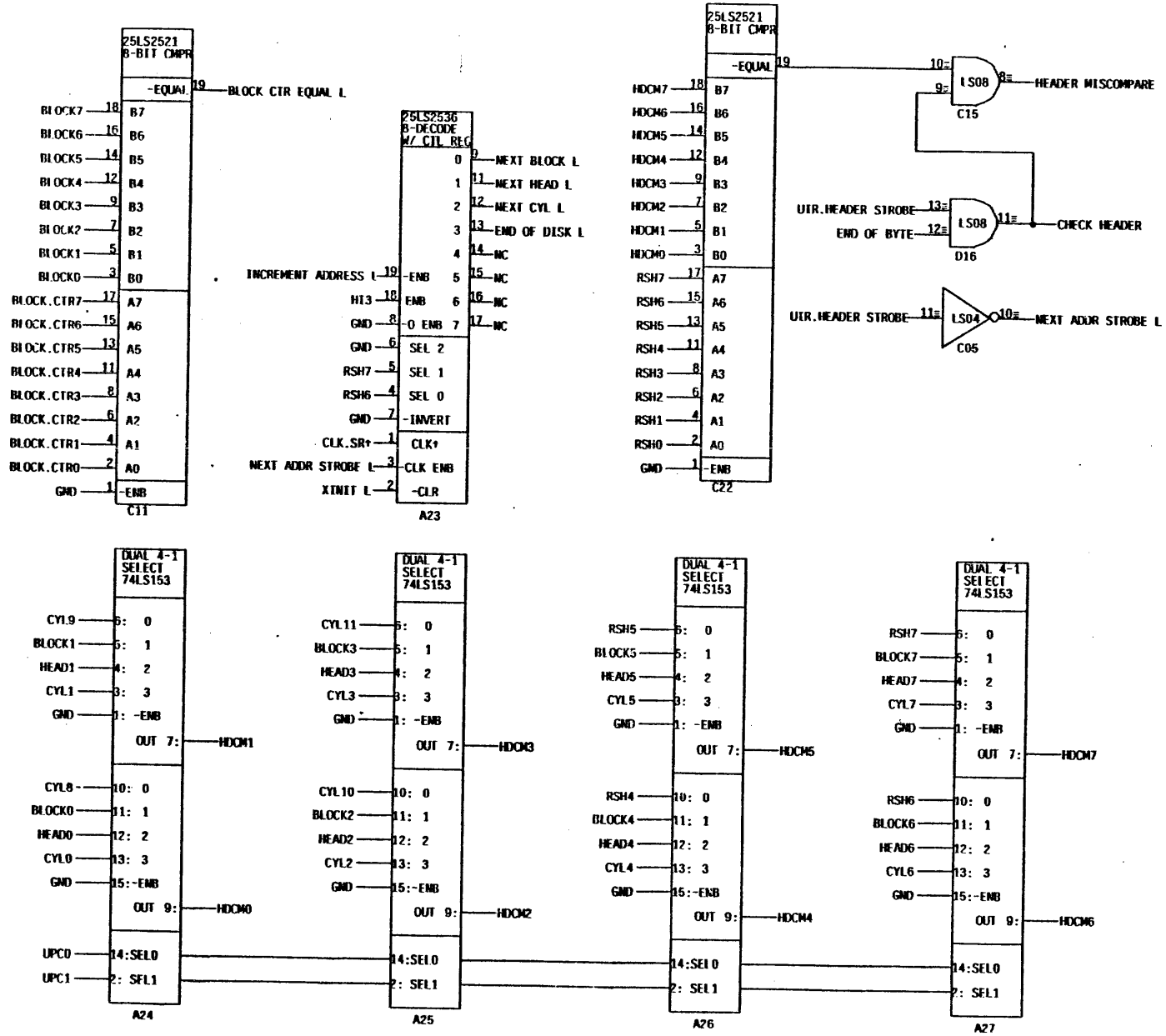
OMITTED DIPS IN 2-BOARD VERSION:

A7 A8 A9
A10 B7 B8

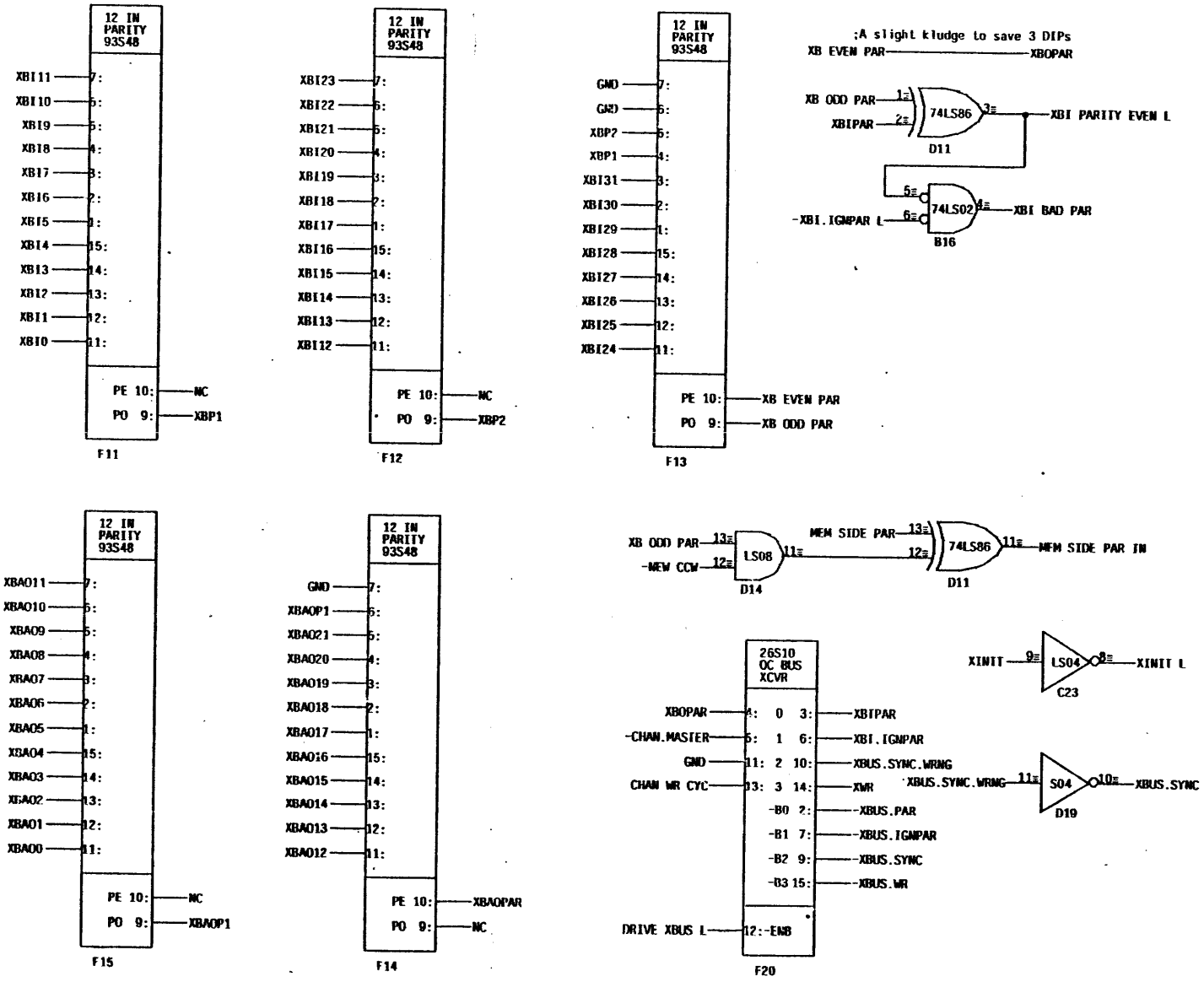
BE CERTAIN TO EDIT THE
RAY FILE FOR UNDEDICATED
GROUND PINS ON J1, J3

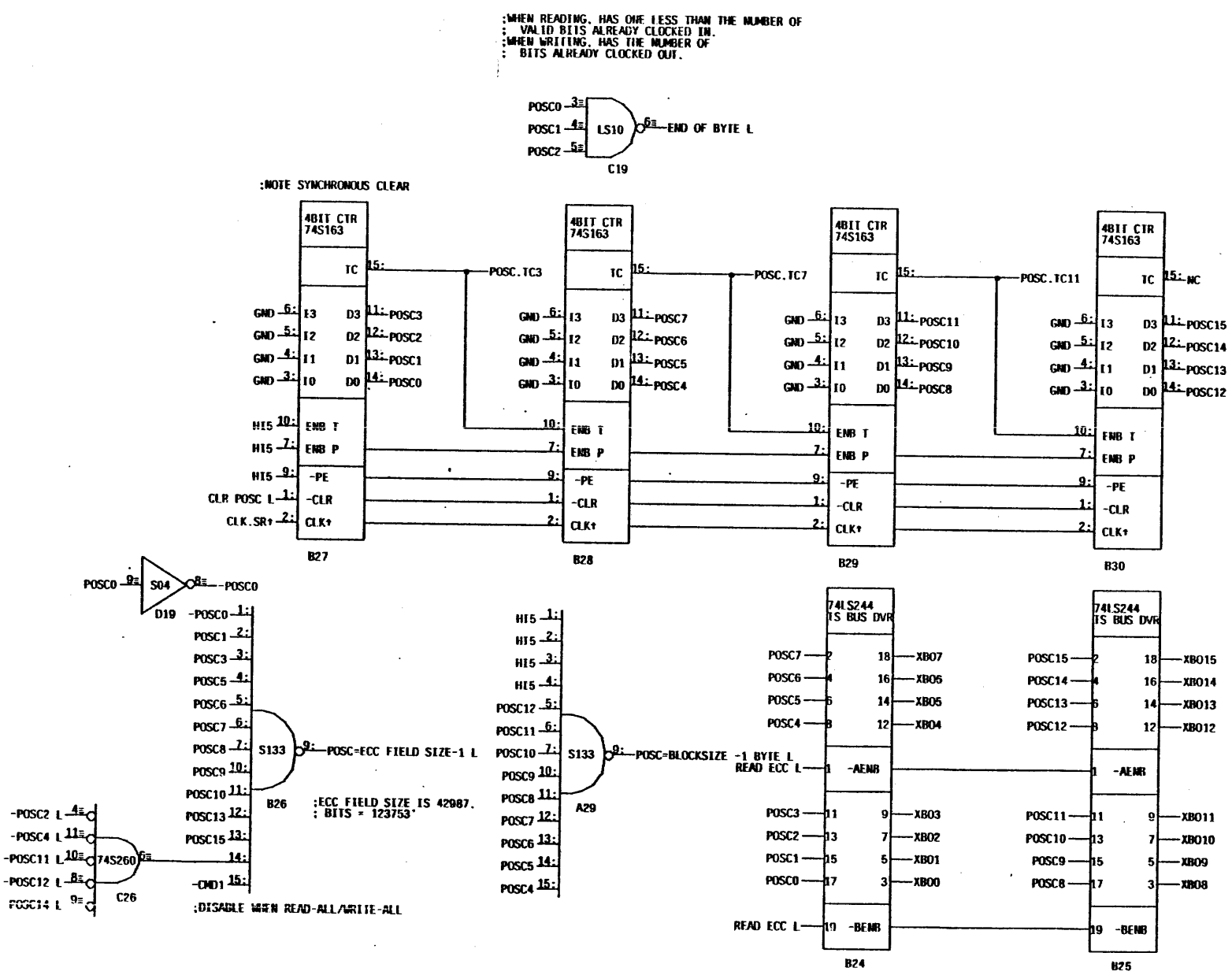
TO DISK MUX BOARD

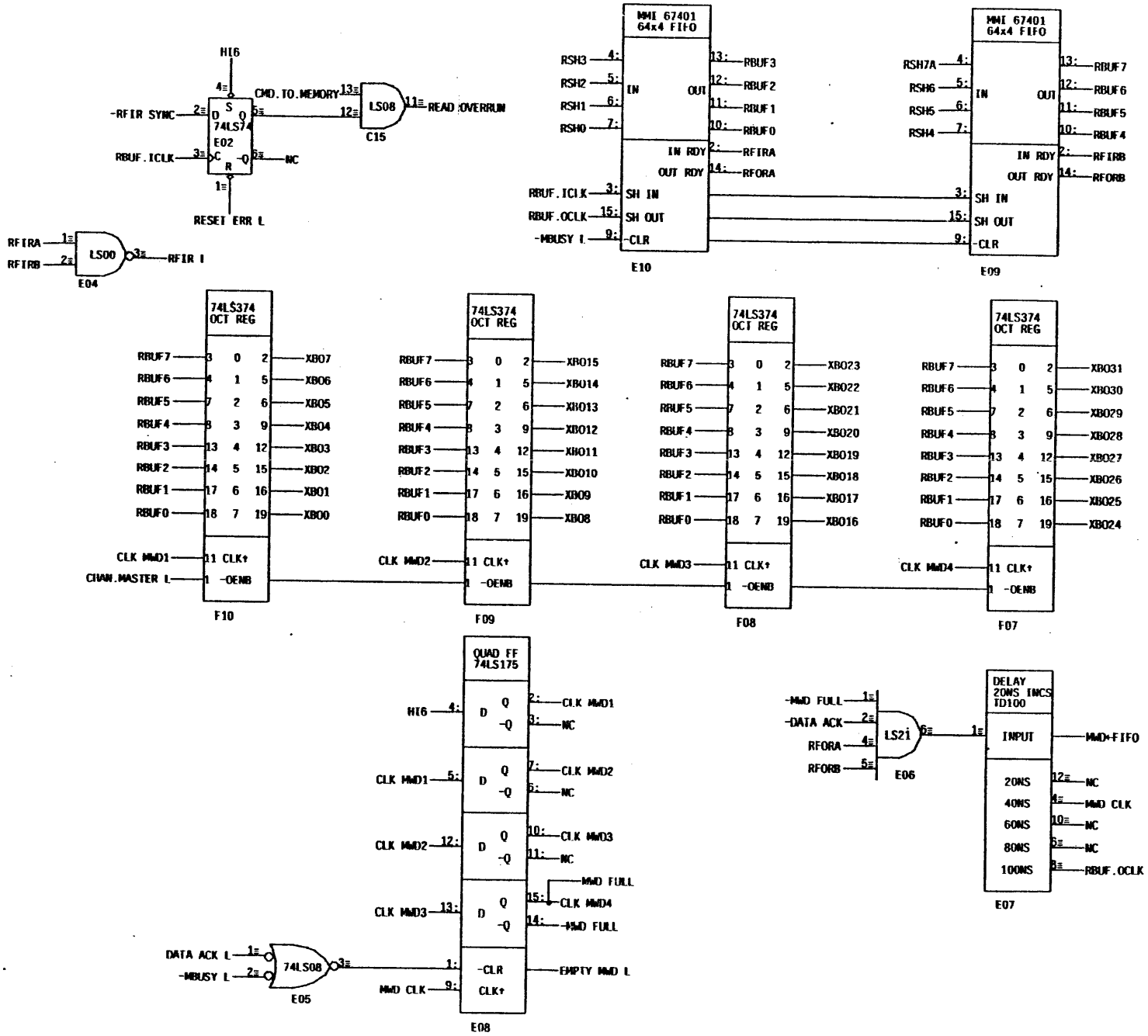




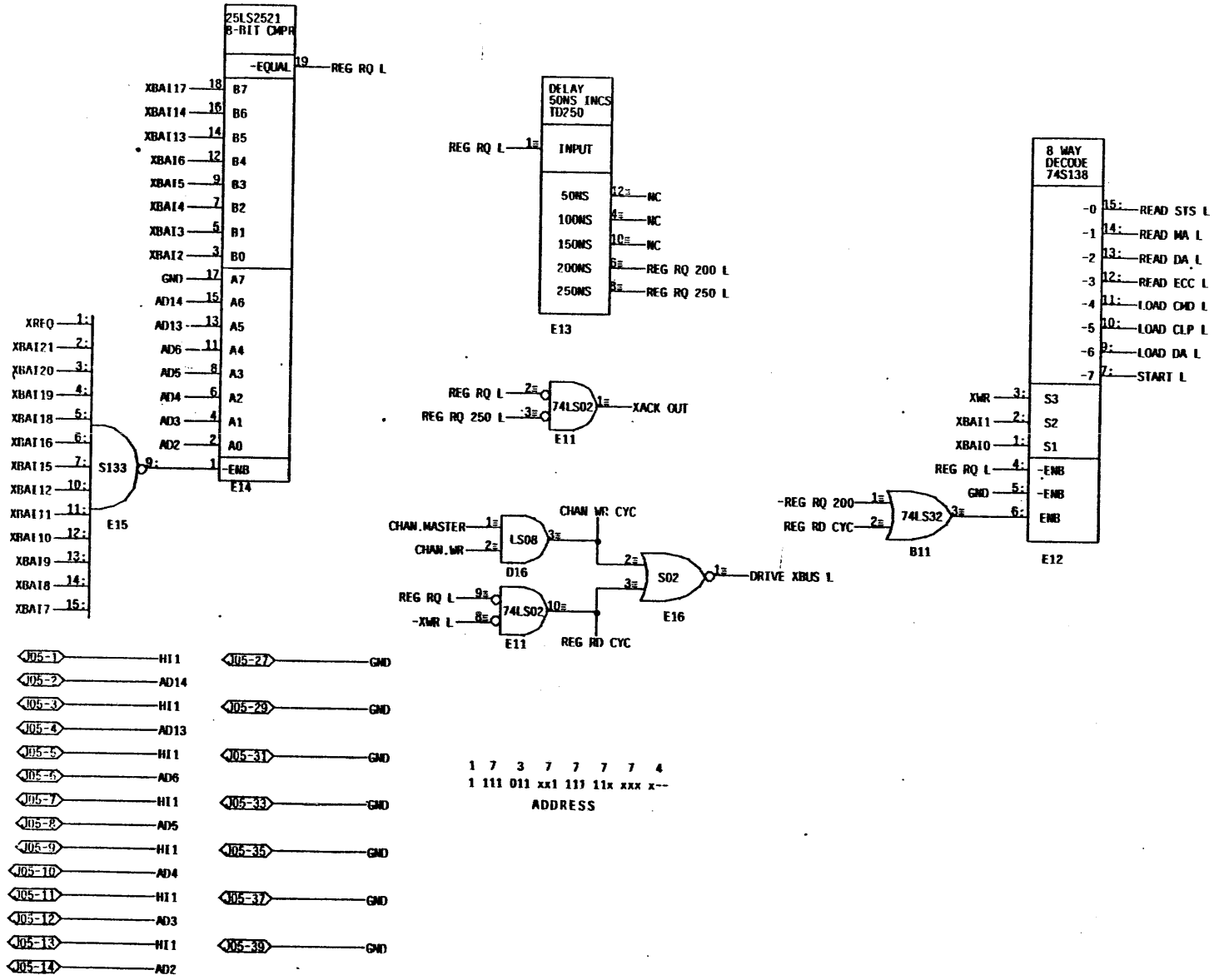
DISK CONTROL	HEADER COMPARE	10-JUN-1979 20:34	AI: CADRDC; DCHDCM


12 IN PARITY 93S48
XBI11 7:
XBI10 6:
XBI9 5:
XBI8 4:
XBI7 3:
XBI6 2:
XBI5 1:
XBI4 15:
XBI3 14:
XBI2 13:
XBI1 12:
XBI0 11:
PE 10: NC
PO 9: XBP1
F11
12 IN PARITY 93S48
XBI23 7:
XBI22 6:
XBI21 5:
XBI20 4:
XBI19 3:
XBI18 2:
XBI17 1:
XBI16 15:
XBI15 14:
XBI14 13:
XBI13 12:
XBI12 11:
PE 10: NC
PO 9: XBP2
F12
12 IN PARITY 93S48
GND 7:
GND 6:
XBP2 5:
XBP1 4:
XBI31 3:
XBI30 2:
XBI29 1:
XBI28 15:
XBI27 14:
XBI26 13:
XBI25 12:
XBI24 11:
PE 10: XB EVEN PAR
PO 9: XB ODD PAR
F13
;A slight kludge to save 3 DIPs
XB EVEN PAR
XBOPAR
XB ODD PAR
XBIPAR
74LS86
D11
XBI PARITY EVEN L
74LS02
B16
-XBI.IGNPAR L
XBI BAD PAR
12 IN PARITY 93S48
XBAO11 7:
XBAO10 6:
XBAO9 5:
XBAO8 4:
XBAO7 3:
XBAO6 2:
XBAO5 1:
XBAO4 15:
XBAO3 14:
XBAO2 13:
XBAO1 12:
XBAO0 11:
PE 10: NC
PO 9: XBAOP1
F15
12 IN PARITY 93S48
GND 7:
XBAOP1 6:
XBAO21 5:
XBAO20 4:
XBAO19 3:
XBAO18 2:
XBAO17 1:
XBAO16 15:
XBAO15 14:
XBAO14 13:
XBAO13 12:
XBAO12 11:
PE 10: XBAOPAR
PO 9: NC
F14
XB ODD PAR
-MEM CCW
LS08
D14
MEM SIDE PAR
74LS86
D11
MEM SIDE PAR IN
26S10 OC BUS XCVR
XBOPAR 4: 0 3: XBIPAR
-CHAN.MASTER 5: 1 6: XBI.IGNPAR
GND 11: 2 10: XBUS.SYNC.WRNG
CHAN WR CYC 13: 3 14: XWR
-B0 2: -XBUS.PAR
-B1 7: -XBUS.IGNPAR
-B2 9: -XBUS.SYNC
-B3 15: -XBUS.WR
DRIVE XBUS L 12: -ENB
F20
XINIT
LS04
C23
XINIT L
XBUS.SYNC.WRNG
S04
D19
XBUS.SYNC

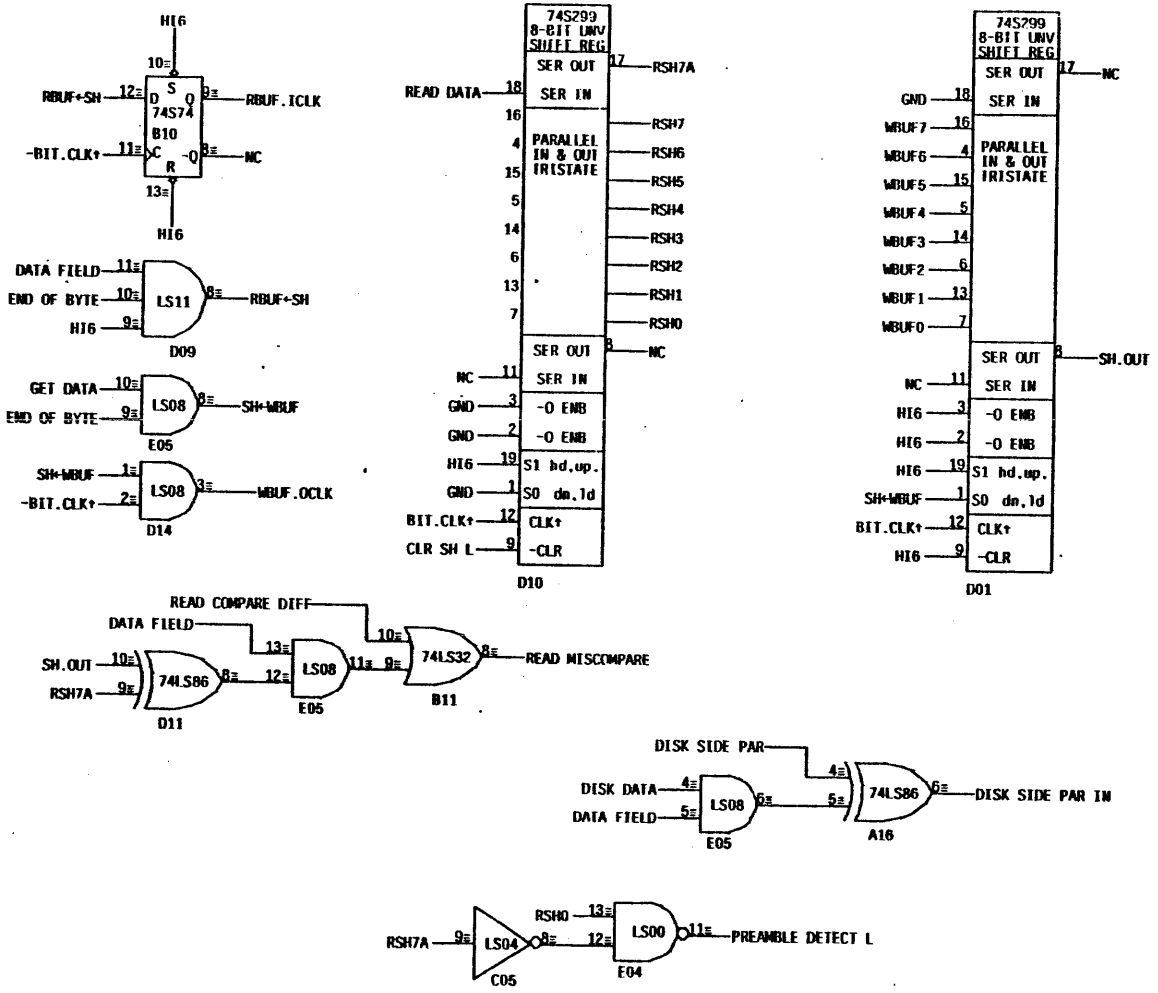

;WHEN READING, HAS ONE LESS THAN THE NUMBER OF
; VALID BITS ALREADY CLOCKED IN.
;WHEN WRITING, HAS THE NUMBER OF
; BITS ALREADY CLOCKED OUT.
POSC0
POSC1
POSC2
LS10
END OF BYTE L
C19
:NOTE SYNCHRONOUS CLEAR
4BIT CTR 74S163
TC
POSC.TC3
POSC.TC7
POSC.TC11
NC
GND
I3
I2
I1
I0
D3
D2
D1
D0
POSC3
POSC2
POSC1
POSC0
POSC7
POSC6
POSC5
POSC4
POSC11
POSC10
POSC9
POSC8
POSC15
POSC14
POSC13
POSC12
HI5
ENB T
ENB P
-PE
CLR POSC L
-CLR
CLK.SR↑
CLK↑
B27
B28
B29
B30
POSC0
S04
-POSC0
D19
-POSC0
POSC1
POSC3
POSC5
POSC6
POSC7
POSC8
POSC9
POSC10
POSC13
POSC15
-CMD1
S133
POSC=ECC FIELD SIZE-1 L
B26
;ECC FIELD SIZE IS 42087.
; BITS = 123753'
-POSC2 L
-POSC4 L
-POSC11 L
-POSC12 L
POSC14 L
74S260
C26
;DISABLE WHEN READ-ALL/WRITE-ALL
HI5
POSC12
POSC11
POSC10
POSC9
POSC8
POSC7
POSC6
POSC5
POSC4
S133
POSC=BLOCKSIZE -1 BYTE L
A29
74LS244 TS BUS DVR
POSC7
POSC6
POSC5
POSC4
POSC3
POSC2
POSC1
POSC0
XB07
XB06
XB05
XB04
XB03
XB02
XB01
XB00
READ ECC L
-AENB
-BENB
B24
POSC15
POSC14
POSC13
POSC12
POSC11
POSC10
POSC9
POSC8
XB015
XB014
XB013
XB012
XB011
XB010
XB09
XB08
B25



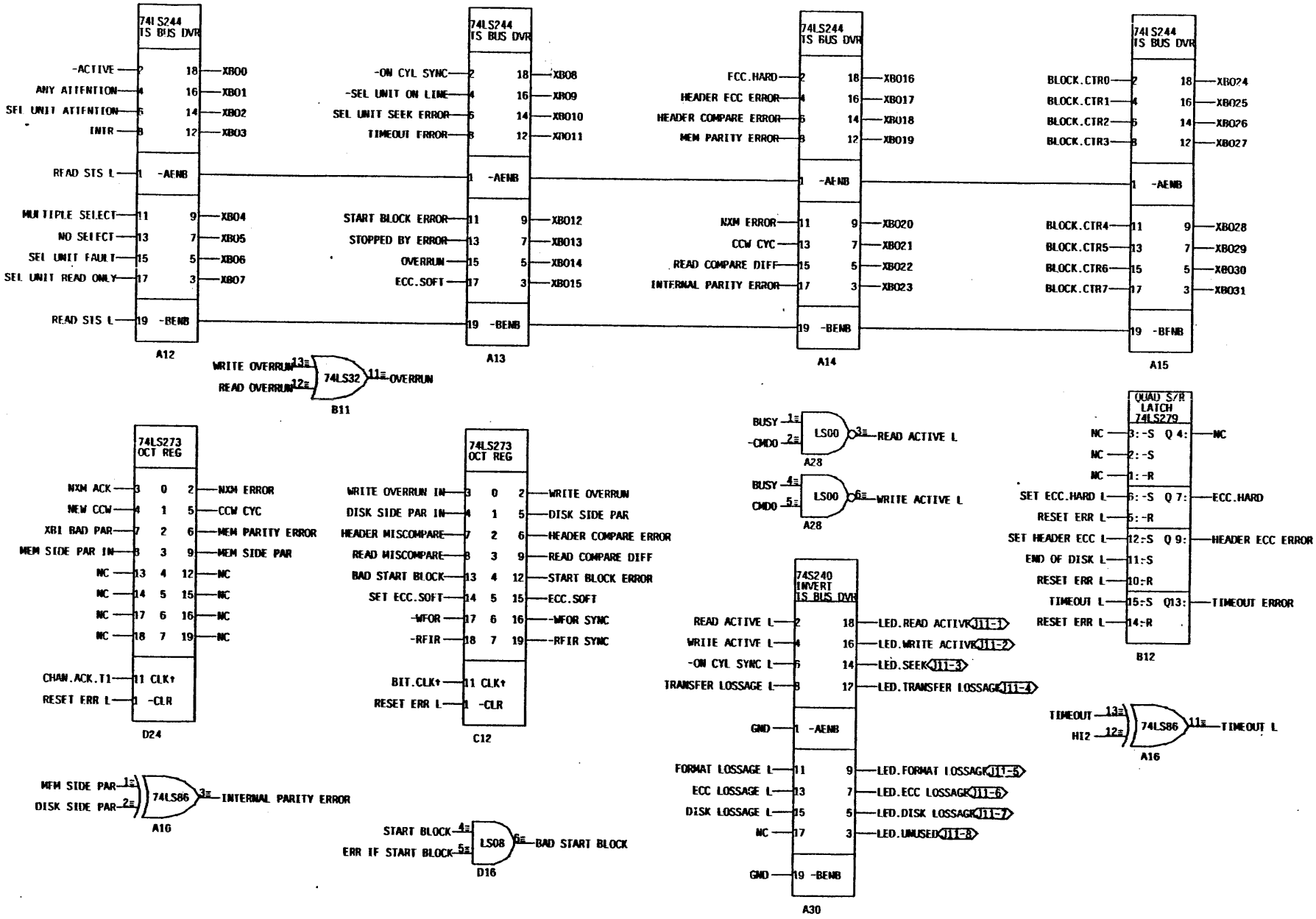
DISK CONTROL	READ BUFFER	30-SEP-1978 04:07	AI: CADRDC; DCRBUF



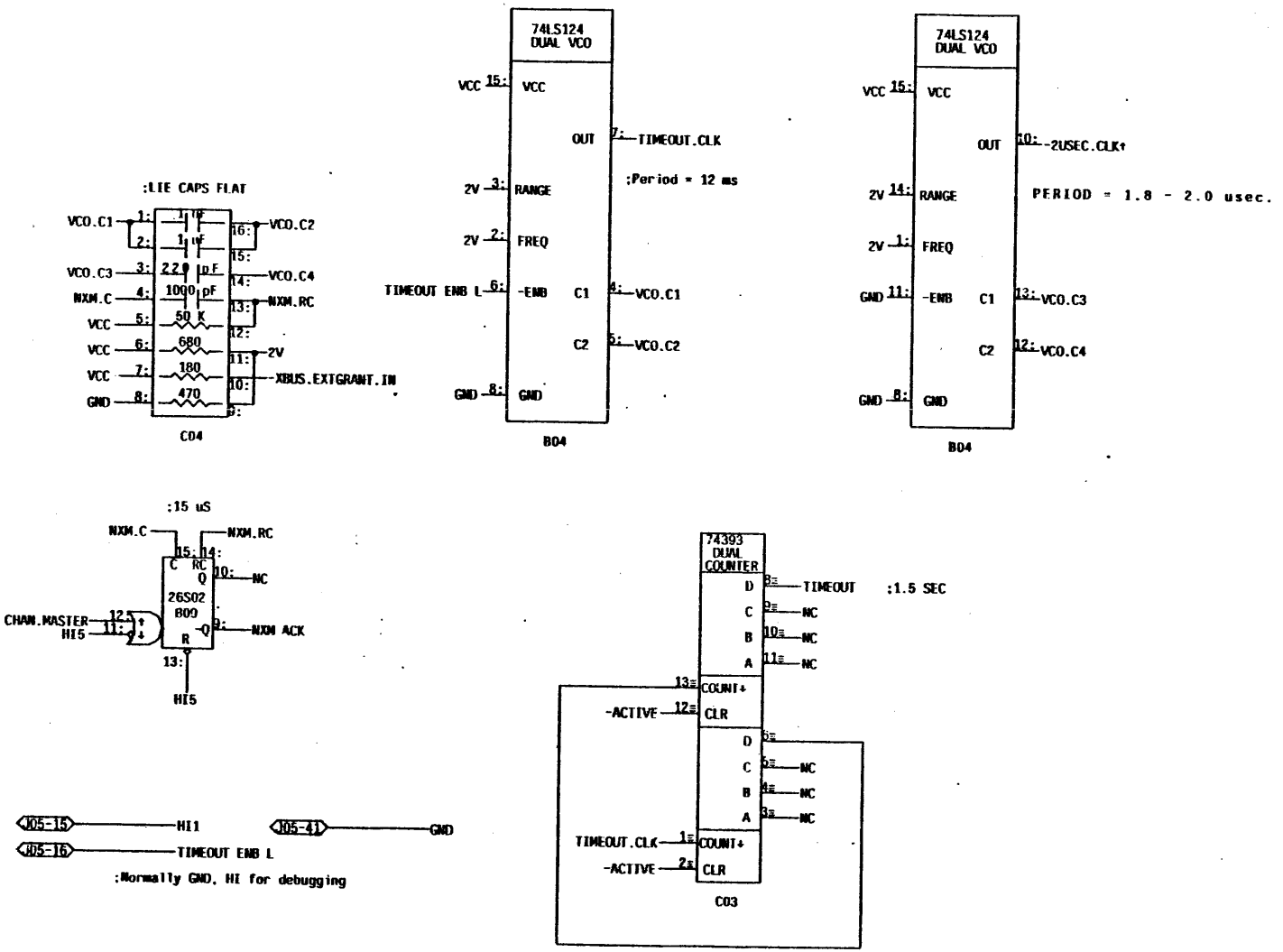
DISK CONTROL	REGISTER ADDRESSING	8-OCT-1978 16:56	AI: CADRDC; DCREG

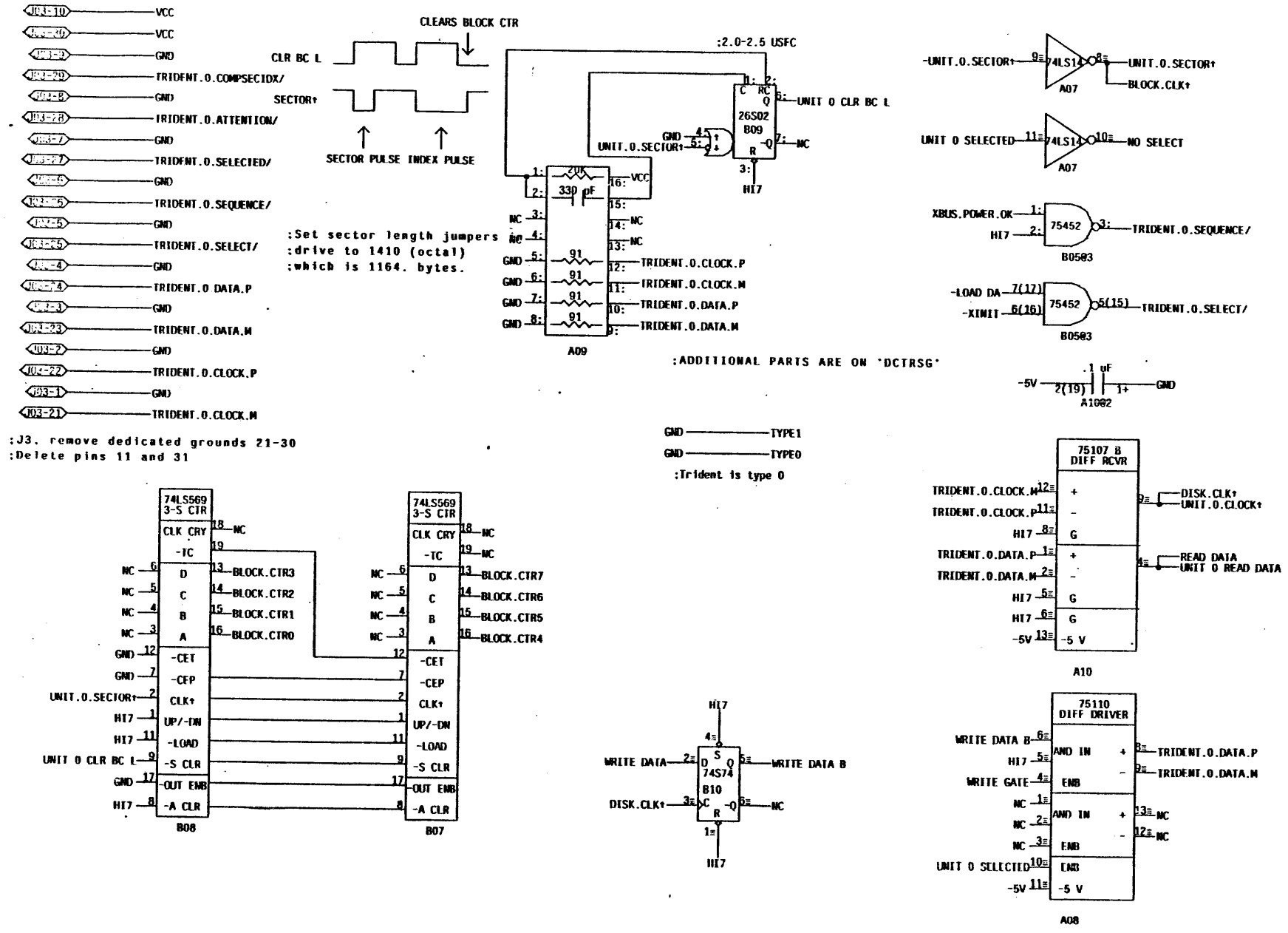


DISK CONTROL	SHIFT REGISTER	10-JUN-1979 20:37	AI: CADRDC; DCSH

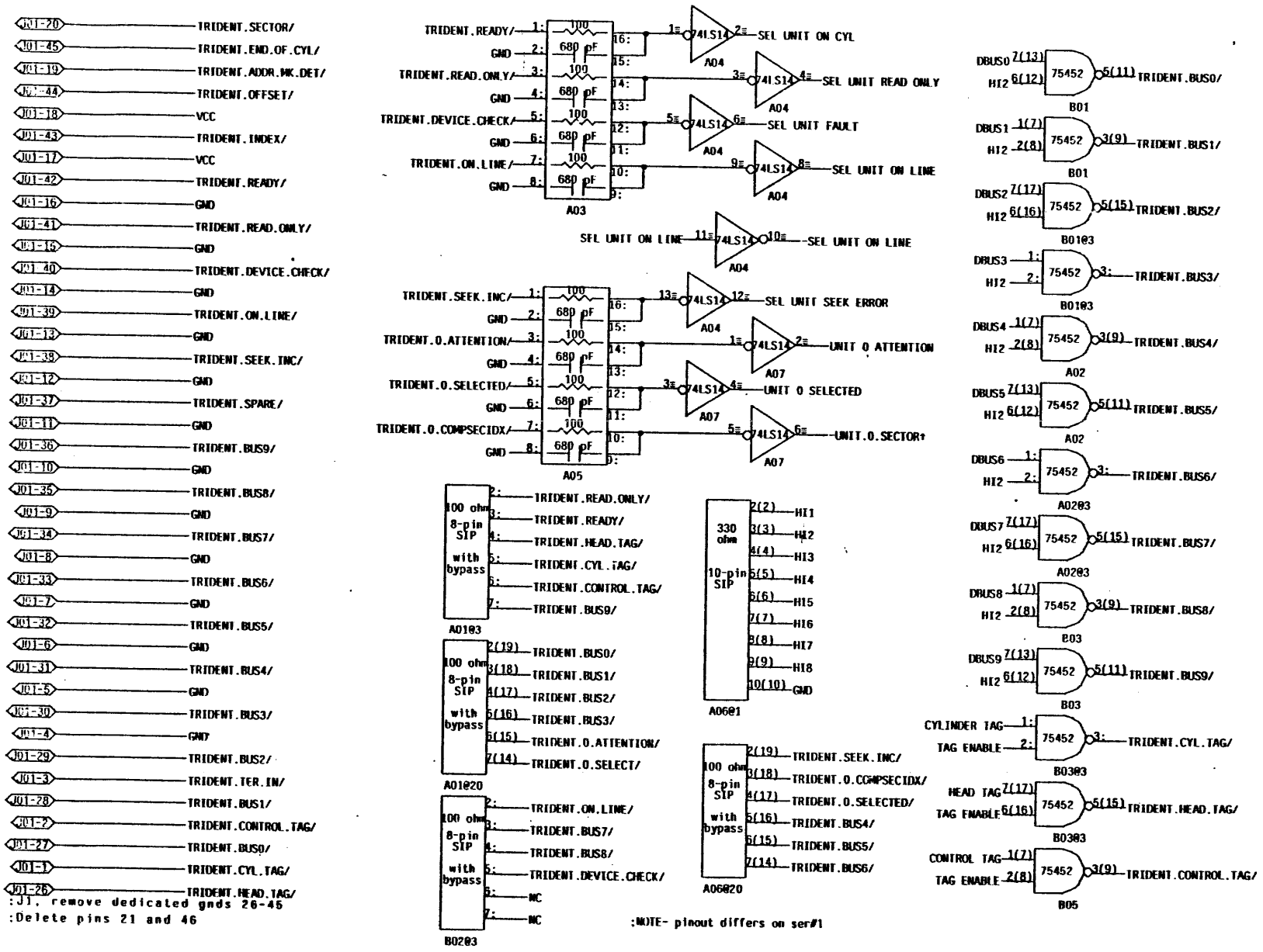


DISK CONTROL	STATUS	5-FEB-1980 01:50	AI: CADRDC; DCSTS

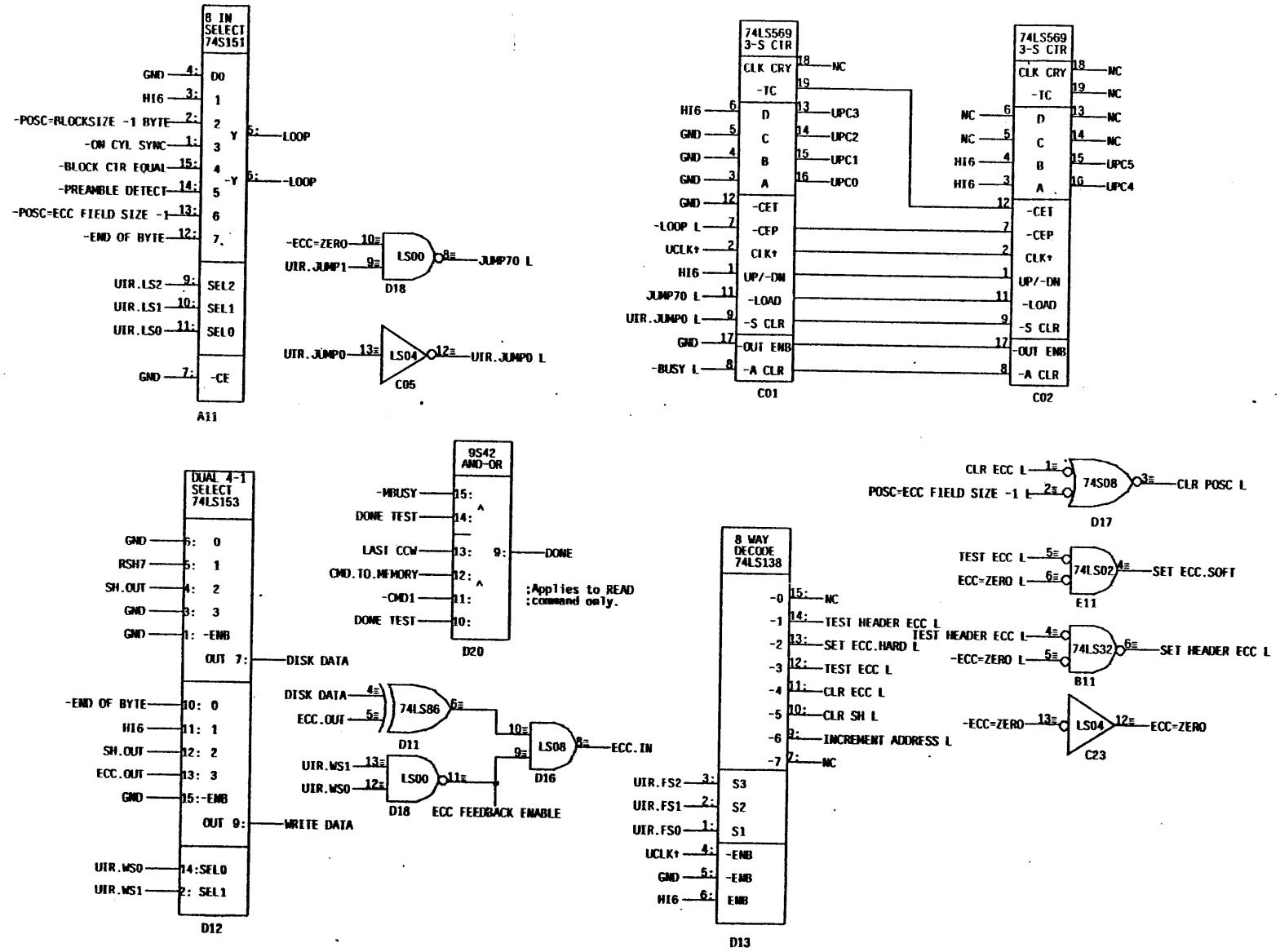

:LIE CAPS FLAT
VCO.C1
1 uF
VCO.C2
1 uF
VCO.C3
220 pF
VCO.C4
NXM.C
1000 pF
NXM.RC
VCC
50 K
VCC
680
2V
VCC
180
XBUS.EXTGRANT.IN
GND
470
C04
74LS124
DUAL VCO
VCC
OUT
TIMEOUT.CLK
:Period = 12 ms
2V
RANGE
2V
FREQ
TIMEOUT ENB L
-ENB
C1
VCO.C1
C2
VCO.C2
GND
GND
B04
74LS124
DUAL VCO
VCC
OUT
-2USEC.CLK↑
PERIOD = 1.8 - 2.0 usec.
2V
RANGE
2V
FREQ
GND
-ENB
C1
VCO.C3
C2
VCO.C4
GND
GND
B04
:15 uS
NXM.C
NXM.RC
C
RC
Q
NC
26S02
B09
CHAN.MASTER
HI5
-Q
NXM ACK
R
HI5
74393
DUAL
COUNTER
D
TIMEOUT
:1.5 SEC
C
NC
B
NC
A
NC
COUNT↓
-ACTIVE
CLR
D
C
NC
B
NC
A
NC
TIMEOUT.CLK
COUNT↓
-ACTIVE
CLR
C03
J05-15
HI1
J05-41
GND
J05-16
TIMEOUT ENB L
:Normally GND, HI for debugging

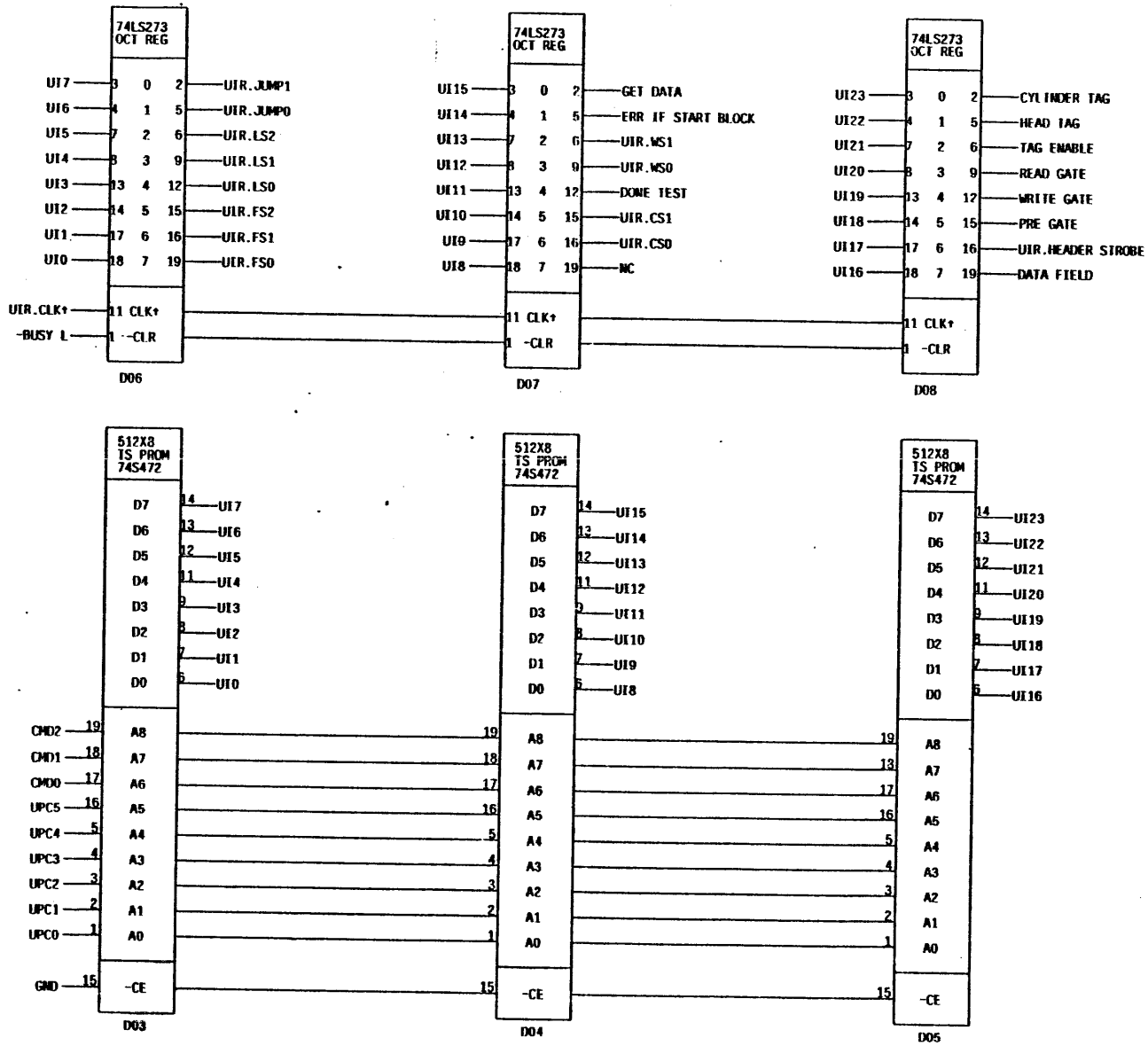


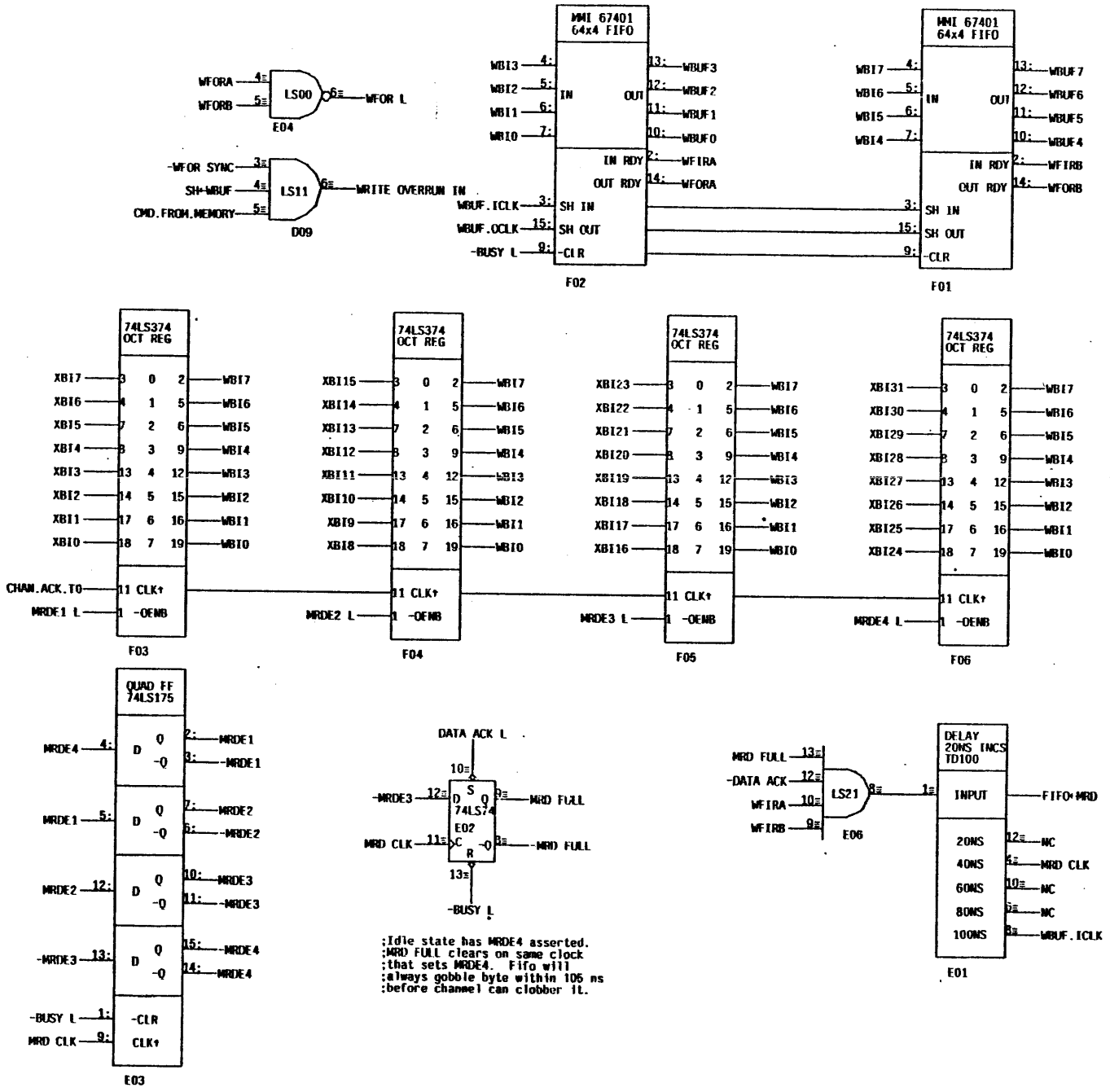
DISK CONTROL	SINGLE TRIDENT	10-JUN-1979 21:54	AI: CADRDC; DCTRID



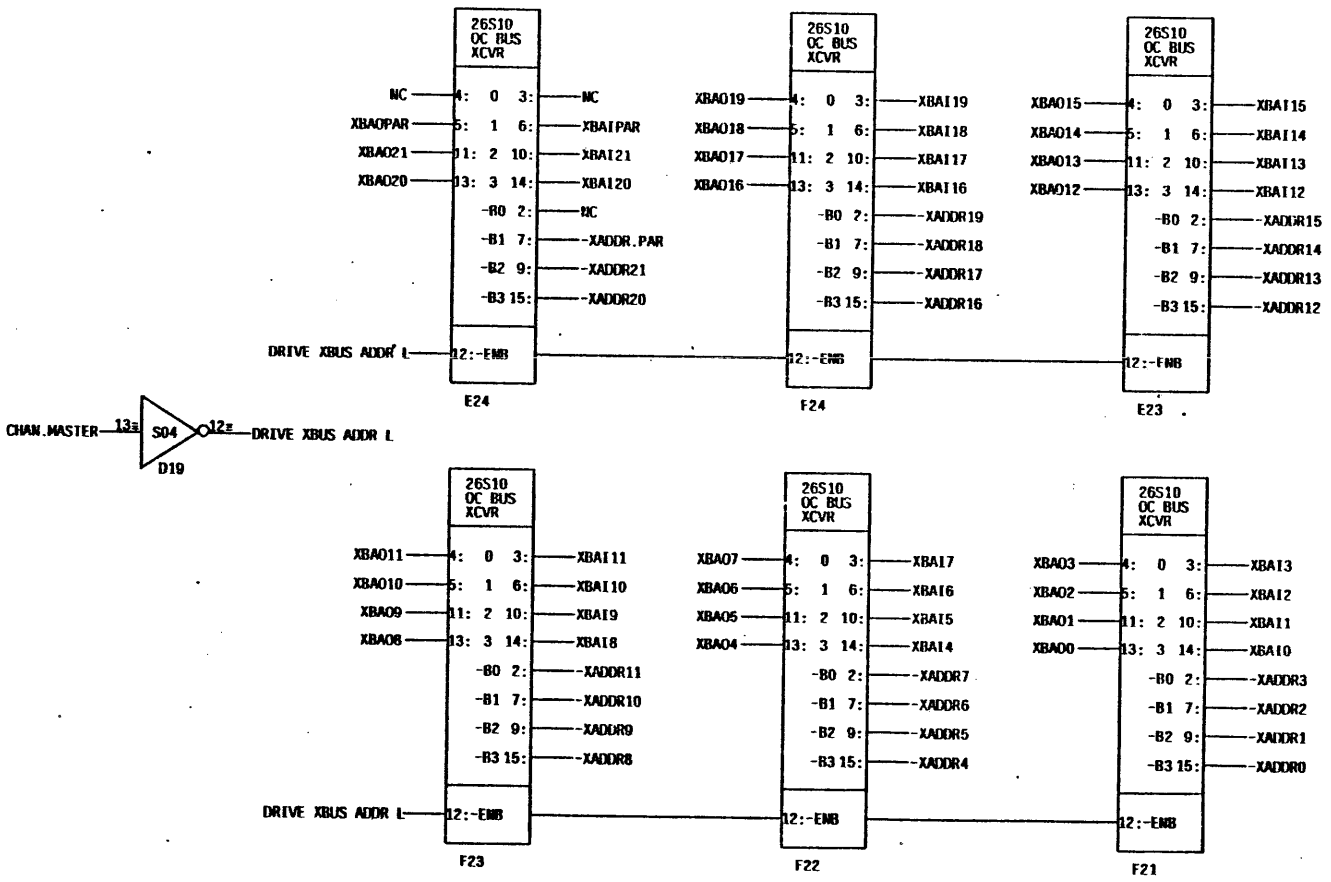
DISK CONTROL	TRIDENT SIGNAL CABLE	30-JUL-1979 02:11	AI: CADRDC; DCTRSG

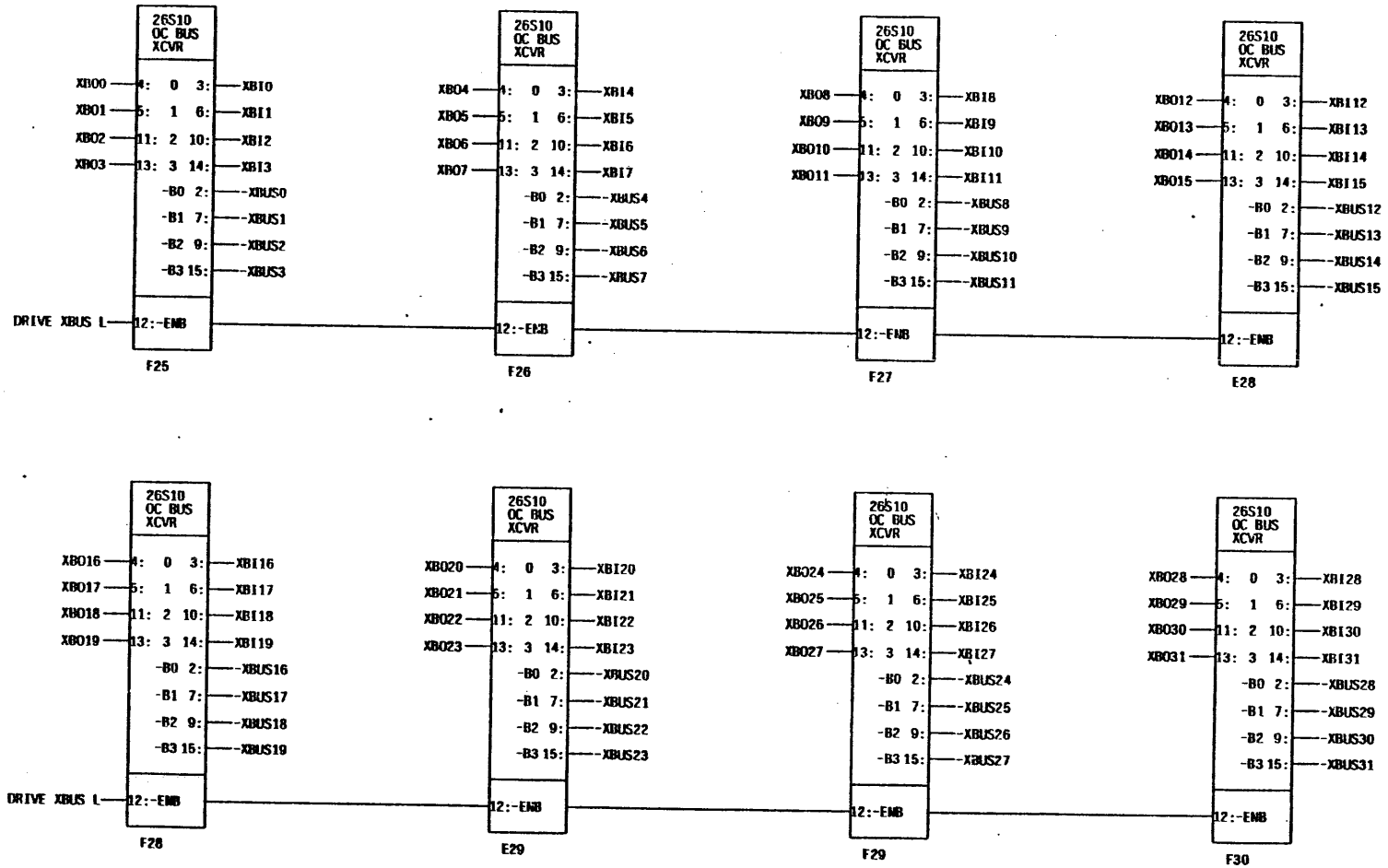

8 IN SELECT 74S151
GND
HI6
-POSC=BLOCKSIZE -1 BYTE
-ON CYL SYNC
-BLOCK CTR EQUAL
-PREAMBLE DETECT
-POSC=ECC FIELD SIZE -1
-END OF BYTE
D0
1
2
3
4
5
6
7
Y
-Y
LOOP
-LOOP
UIR.LS2
UIR.LS1
UIR.LS0
SEL2
SEL1
SEL0
GND
-CE
A11
-ECC=ZERO
UIR.JUMP1
LS00
JUMP70 L
D18
UIR.JUMP0
LS04
UIR.JUMP0 L
C05
74LS569 3-S CTR
CLK CRY
-TC
HI6
GND
GND
GND
GND
-LOOP L
UCLK↑
HI6
JUMP70 L
UIR.JUMP0 L
GND
-BUSY L
D
C
B
A
-CET
-CEP
CLK↑
UP/-DN
-LOAD
-S CLR
-OUT ENB
-A CLR
NC
UPC3
UPC2
UPC1
UPC0
C01
74LS569 3-S CTR
NC
NC
HI6
HI6
UPC5
UPC4
C02
DUAL 4-1 SELECT 74LS153
GND
RSH7
SH.OUT
GND
GND
-END OF BYTE
HI6
SH.OUT
ECC.OUT
GND
UIR.WS0
UIR.WS1
-ENB
OUT
DISK DATA
WRITE DATA
SEL0
SEL1
D12
9S42 AND-OR
-MBUSY
DONE TEST
LAST CCW
CMD.TO.MEMORY
-CMD1
DONE TEST
DONE
;Applies to READ
;command only.
D20
DISK DATA
ECC.OUT
74LS86
D11
LS08
ECC.IN
D16
UIR.WS1
UIR.WS0
LS00
D18
ECC FEEDBACK ENABLE
8 WAY DECODE 74LS138
-0
-1
-2
-3
-4
-5
-6
-7
NC
TEST HEADER ECC L
SET ECC.HARD L
TEST ECC L
CLR ECC L
CLR SH L
INCREMENT ADDRESS L
NC
UIR.FS2
UIR.FS1
UIR.FS0
UCLK↑
GND
HI6
S3
S2
S1
-ENB
-ENB
ENB
D13
CLR ECC L
POSC=ECC FIELD SIZE -1 L
74S08
CLR POSC L
D17
TEST ECC L
ECC=ZERO L
74LS02
SET ECC.SOFT
E11
TEST HEADER ECC L
-ECC=ZERO L
74LS32
SET HEADER ECC L
B11
-ECC=ZERO
LS04
ECC=ZERO
C23


74LS273
OCT REG
UI7
UI6
UI5
UI4
UI3
UI2
UI1
UI0
UIR.JUMP1
UIR.JUMP0
UIR.LS2
UIR.LS1
UIR.LS0
UIR.FS2
UIR.FS1
UIR.FS0
UIR.CLK↑
-BUSY L
11 CLK↑
1 -CLR
D06
UI15
UI14
UI13
UI12
UI11
UI10
UI9
UI8
GET DATA
ERR IF START BLOCK
UIR.WS1
UIR.WS0
DONE TEST
UIR.CS1
UIR.CS0
NC
D07
UI23
UI22
UI21
UI20
UI19
UI18
UI17
UI16
CYLINDER TAG
HEAD TAG
TAG ENABLE
READ GATE
WRITE GATE
PRE GATE
UIR.HEADER STROBE
DATA FIELD
D08
512X8
TS PROM
74S472
D7
D6
D5
D4
D3
D2
D1
D0
A8
A7
A6
A5
A4
A3
A2
A1
A0
-CE
CMD2
CMD1
CMD0
UPC5
UPC4
UPC3
UPC2
UPC1
UPC0
GND
D03
D04
D05

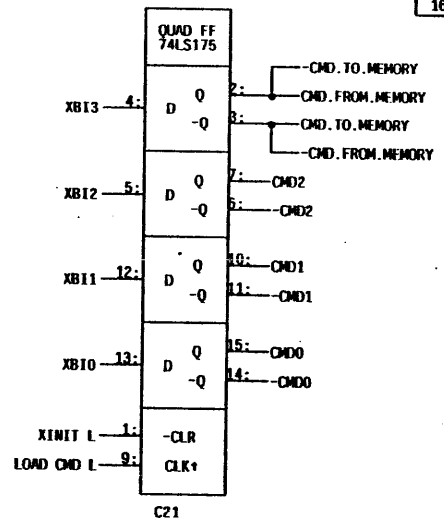


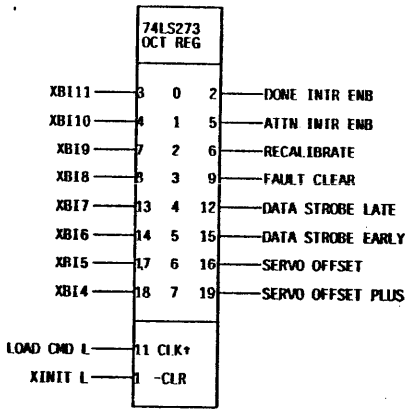
DISK CONTROL	WRITE BUFFER	30-SEP-1978 02:27	AI: CADRDC; DCWBUF

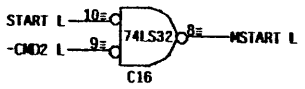

26S10
OC BUS
XCVR
NC
XBAOPAR
XBAO21
XBAO20
4: 0 3:
5: 1 6:
11: 2 10:
13: 3 14:
-B0 2:
-B1 7:
-B2 9:
-B3 15:
NC
XBAIPAR
XBAI21
XBAI20
NC
-XADDR.PAR
-XADDR21
-XADDR20
DRIVE XBUS ADDR L
12:-ENB
E24
XBAO19
XBAO18
XBAO17
XBAO16
XBAI19
XBAI18
XBAI17
XBAI16
-XADDR19
-XADDR18
-XADDR17
-XADDR16
F24
XBAO15
XBAO14
XBAO13
XBAO12
XBAI15
XBAI14
XBAI13
XBAI12
-XADDR15
-XADDR14
-XADDR13
-XADDR12
E23
CHAN.MASTER
13≡
S04
12≡
DRIVE XBUS ADDR L
D19
XBAO11
XBAO10
XBAO9
XBAO8
XBAI11
XBAI10
XBAI9
XBAI8
-XADDR11
-XADDR10
-XADDR9
-XADDR8
F23
XBAO7
XBAO6
XBAO5
XBAO4
XBAI7
XBAI6
XBAI5
XBAI4
-XADDR7
-XADDR6
-XADDR5
-XADDR4
F22
XBAO3
XBAO2
XBAO1
XBAO0
XBAI3
XBAI2
XBAI1
XBAI0
-XADDR3
-XADDR2
-XADDR1
-XADDR0
F21

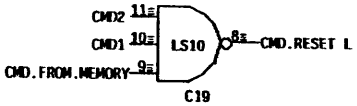

26S10
OC BUS
XCVR
XBO0
XBO1
XBO2
XBO3
4: 0 3:
5: 1 6:
11: 2 10:
13: 3 14:
-B0 2:
-B1 7:
-B2 9:
-B3 15:
XBI0
XBI1
XBI2
XBI3
-XBUS0
-XBUS1
-XBUS2
-XBUS3
DRIVE XBUS L
12:-ENB
F25
XBO4
XBO5
XBO6
XBO7
XBI4
XBI5
XBI6
XBI7
-XBUS4
-XBUS5
-XBUS6
-XBUS7
F26
XBO8
XBO9
XBO10
XBO11
XBI8
XBI9
XBI10
XBI11
-XBUS8
-XBUS9
-XBUS10
-XBUS11
F27
XBO12
XBO13
XBO14
XBO15
XBI12
XBI13
XBI14
XBI15
-XBUS12
-XBUS13
-XBUS14
-XBUS15
E28
XBO16
XBO17
XBO18
XBO19
XBI16
XBI17
XBI18
XBI19
-XBUS16
-XBUS17
-XBUS18
-XBUS19
F28
XBO20
XBO21
XBO22
XBO23
XBI20
XBI21
XBI22
XBI23
-XBUS20
-XBUS21
-XBUS22
-XBUS23
E29
XBO24
XBO25
XBO26
XBO27
XBI24
XBI25
XBI26
XBI27
-XBUS24
-XBUS25
-XBUS26
-XBUS27
F29
XBO28
XBO29
XBO30
XBO31
XBI28
XBI29
XBI30
XBI31
-XBUS28
-XBUS29
-XBUS30
-XBUS31
F30

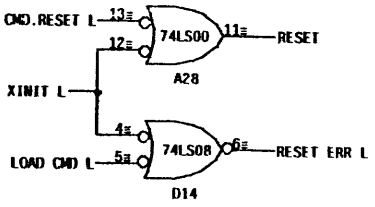
CMD	OPERATION
00	READ
10	READ COMPARE
11	WRITE
02	READ ALL
13	WRITE ALL
04	SEEK
05	AI EASE
1005	RECALIBRATE
405	FAULT CLEAR
06	OFFSET CLEAR
16	STOP, RESET

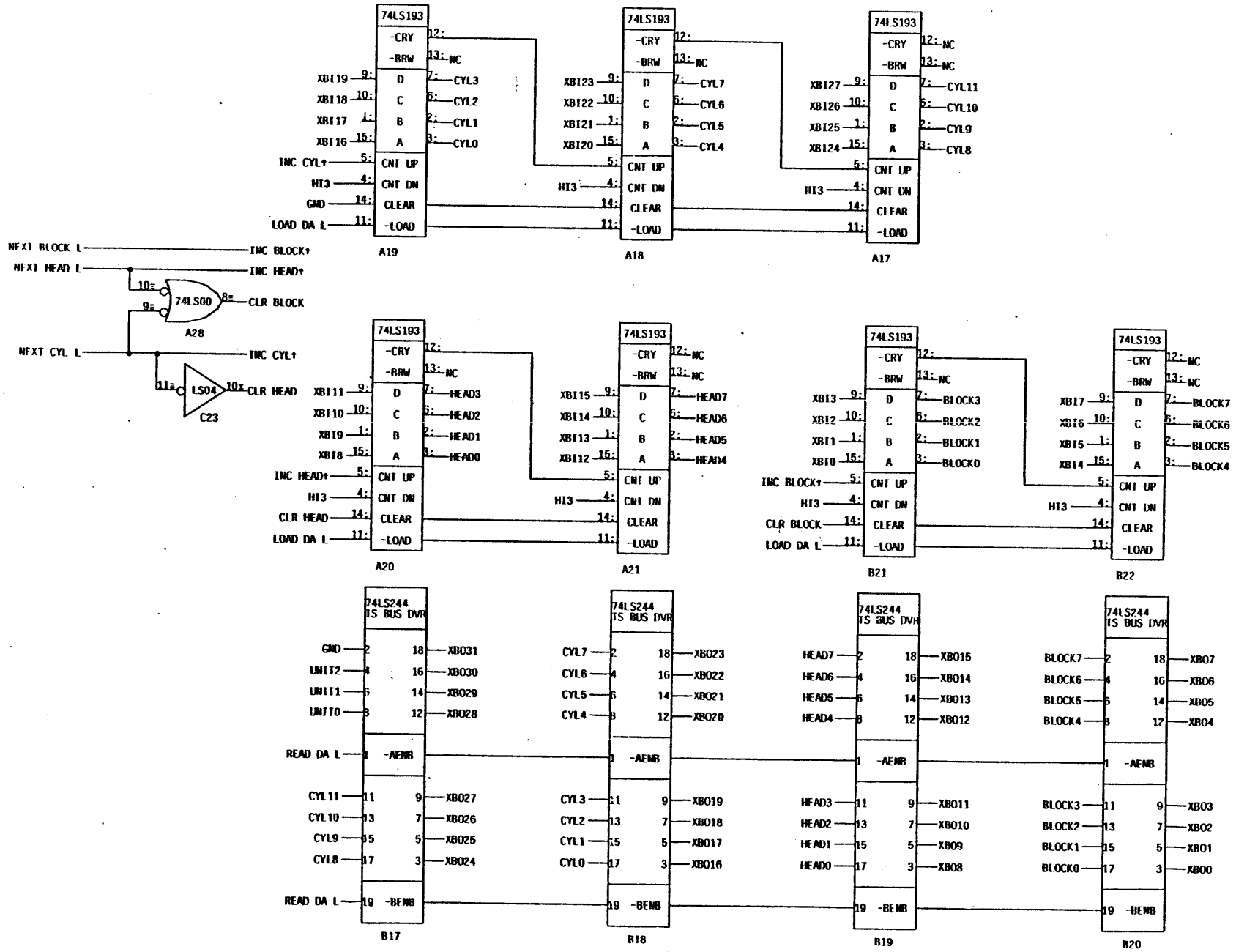




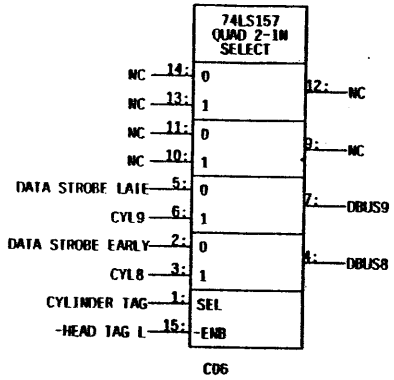


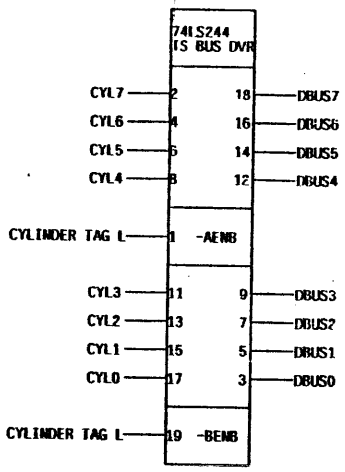


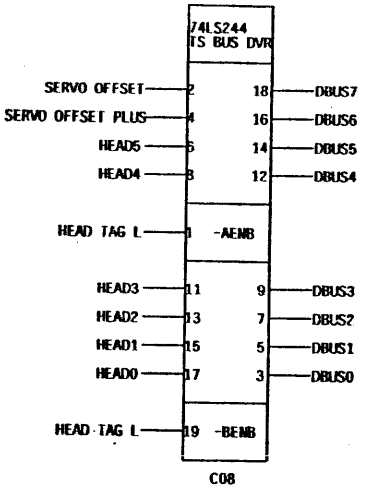


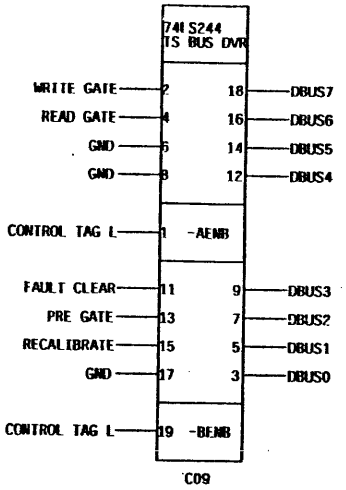


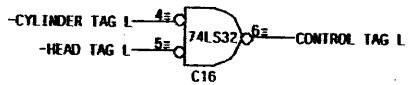
DISK CONTROL	DISK ADDRESS	30-SEP-1978 01:36	AI: CADRDC; DCDA

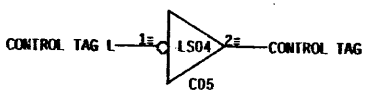

74LS157
QUAD 2-IN
SELECT
NC 14:
NC 13:
NC 11:
NC 10:
DATA STROBE LATE 5:
CYL9 6:
DATA STROBE EARLY 2:
CYL8 3:
CYLINDER TAG 1:
-HEAD TAG L 15:
0
1
SEL
-ENB
12: NC
9: NC
7: DBUS9
4: DBUS8
C06

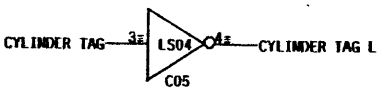

74LS244
TS BUS DVR
CYL7 2
CYL6 4
CYL5 6
CYL4 8
CYLINDER TAG L 1
-AENB
CYL3 11
CYL2 13
CYL1 15
CYL0 17
CYLINDER TAG L 19
-BENB
18 DBUS7
16 DBUS6
14 DBUS5
12 DBUS4
9 DBUS3
7 DBUS2
5 DBUS1
3 DBUS0
C07

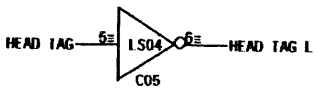

74LS244
TS BUS DVR
SERVO OFFSET 2
SERVO OFFSET PLUS 4
HEAD5 6
HEAD4 8
HEAD TAG L 1
-AENB
HEAD3 11
HEAD2 13
HEAD1 15
HEAD0 17
HEAD TAG L 19
-BENB
18 DBUS7
16 DBUS6
14 DBUS5
12 DBUS4
9 DBUS3
7 DBUS2
5 DBUS1
3 DBUS0
C08

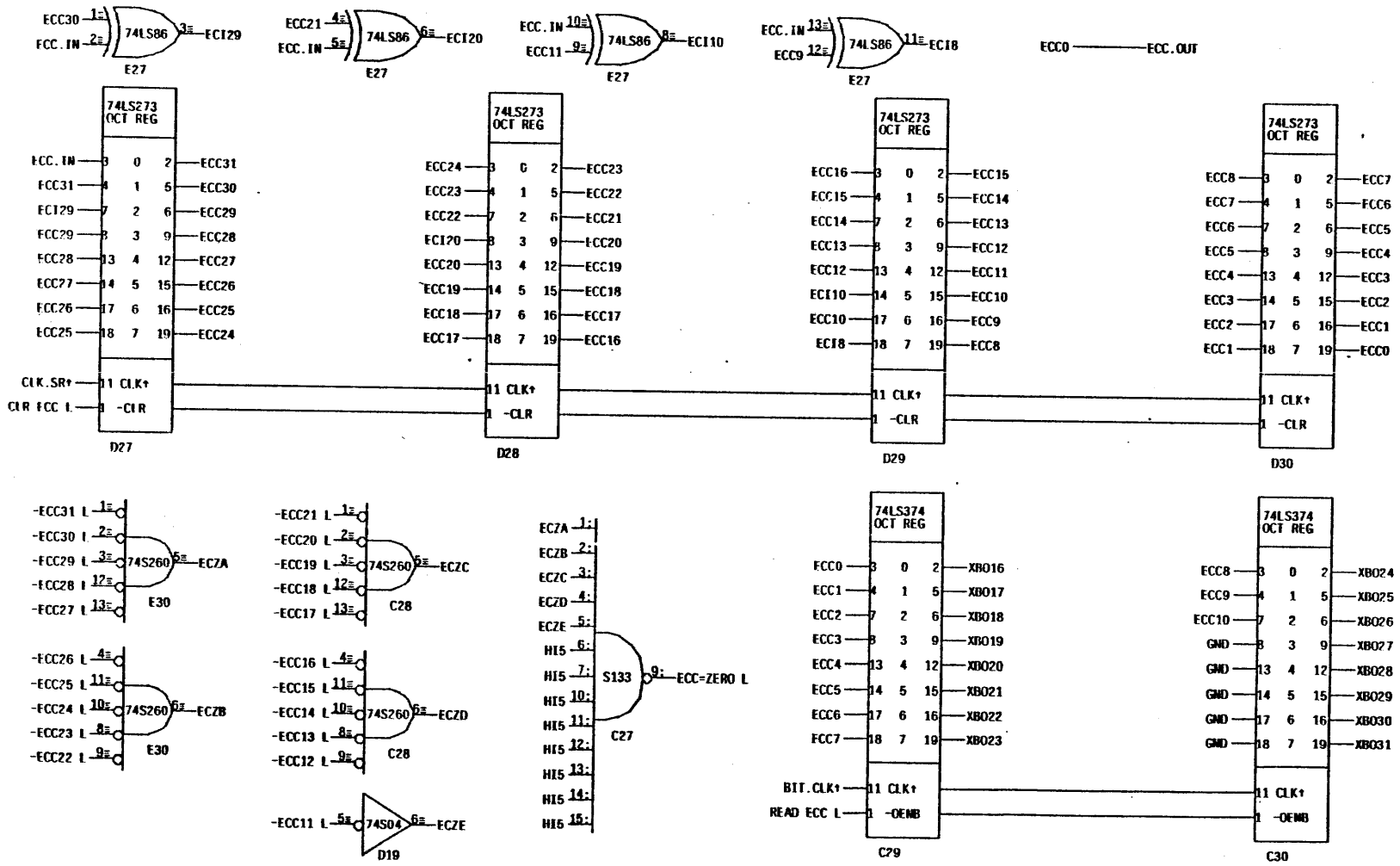

74LS244
TS BUS DVR
WRITE GATE 2
READ GATE 4
GND 6
GND 8
CONTROL TAG L 1
-AENB
FAULT CLEAR 11
PRE GATE 13
RECALIBRATE 15
GND 17
CONTROL TAG L 19
-BENB
18 DBUS7
16 DBUS6
14 DBUS5
12 DBUS4
9 DBUS3
7 DBUS2
5 DBUS1
3 DBUS0
C09


-CYLINDER TAG L 4
-HEAD TAG L 5
74LS32
6 CONTROL TAG L
C16

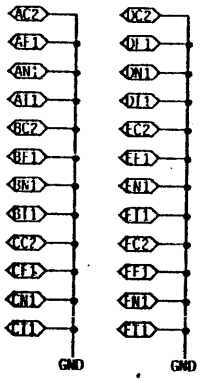

CONTROL TAG L 1
LS04
2 CONTROL TAG
C05


CYLINDER TAG 3
LS04
4 CYLINDER TAG L
C05


HEAD TAG 5
LS04
6 HEAD TAG L
C05


ECC30
ECC.IN
74LS86
ECI29
E27
ECC21
ECC.IN
74LS86
ECI20
E27
ECC.IN
ECC11
74LS86
ECI10
E27
ECC.IN
ECC9
74LS86
ECI8
E27
ECC0
ECC.OUT
74LS273 OCT REG
ECC.IN
ECC31
ECI29
ECC29
ECC28
ECC27
ECC26
ECC25
CLK.SR↑
CLR ECC L
ECC31
ECC30
ECC29
ECC28
ECC27
ECC26
ECC25
ECC24
D27
74LS273 OCT REG
ECC24
ECC23
ECC22
ECI20
ECC20
ECC19
ECC18
ECC17
CLK↑
-CLR
ECC23
ECC22
ECC21
ECC20
ECC19
ECC18
ECC17
ECC16
D28
74LS273 OCT REG
ECC16
ECC15
ECC14
ECC13
ECC12
ECI10
ECC10
ECI8
CLK↑
-CLR
ECC15
ECC14
ECC13
ECC12
ECC11
ECC10
ECC9
ECC8
D29
74LS273 OCT REG
ECC8
ECC7
ECC6
ECC5
ECC4
ECC3
ECC2
ECC1
CLK↑
-CLR
ECC7
ECC6
ECC5
ECC4
ECC3
ECC2
ECC1
ECC0
D30
-ECC31 L
-ECC30 L
-ECC29 L
-ECC28 L
-ECC27 L
74S260
ECZA
E30
-ECC26 L
-ECC25 L
-ECC24 L
-ECC23 L
-ECC22 L
74S260
ECZB
E30
-ECC21 L
-ECC20 L
-ECC19 L
-ECC18 L
-ECC17 L
74S260
ECZC
C28
-ECC16 L
-ECC15 L
-ECC14 L
-ECC13 L
-ECC12 L
74S260
ECZD
C28
-ECC11 L
74S04
ECZE
D19
ECZA
ECZB
ECZC
ECZD
ECZE
HI5
HI5
HI5
HI5
HI5
HI5
HI5
HI5
S133
ECC=ZERO L
C27
74LS374 OCT REG
ECC0
ECC1
ECC2
ECC3
ECC4
ECC5
ECC6
ECC7
BIT.CLK↑
READ ECC L
CLK↑
-OEMB
XB016
XB017
XB018
XB019
XB020
XB021
XB022
XB023
C29
74LS374 OCT REG
ECC8
ECC9
ECC10
GND
GND
GND
GND
GND
CLK↑
-OEMB
XB024
XB025
XB026
XB027
XB028
XB029
XB030
XB031
C30

GROUNDS



JUMPERS FOR 1-BOARD VERSION:

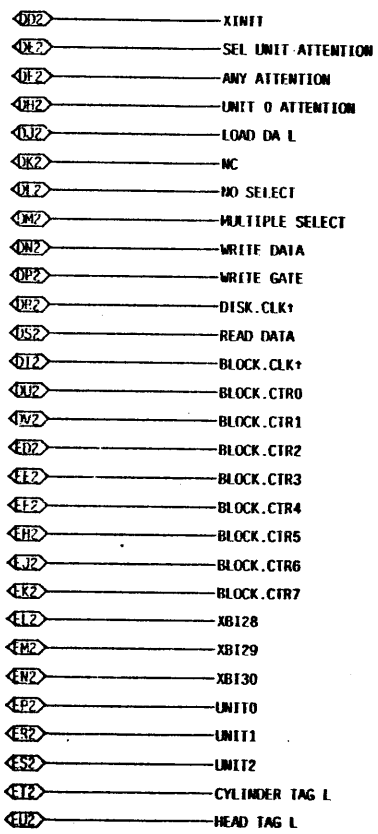
DE2 - DF2 - DH2
DN1 - DM2
ET1 - EP2 - ER2 - ES2

OMITTED DIPS IN 2-BOARD VERSION:

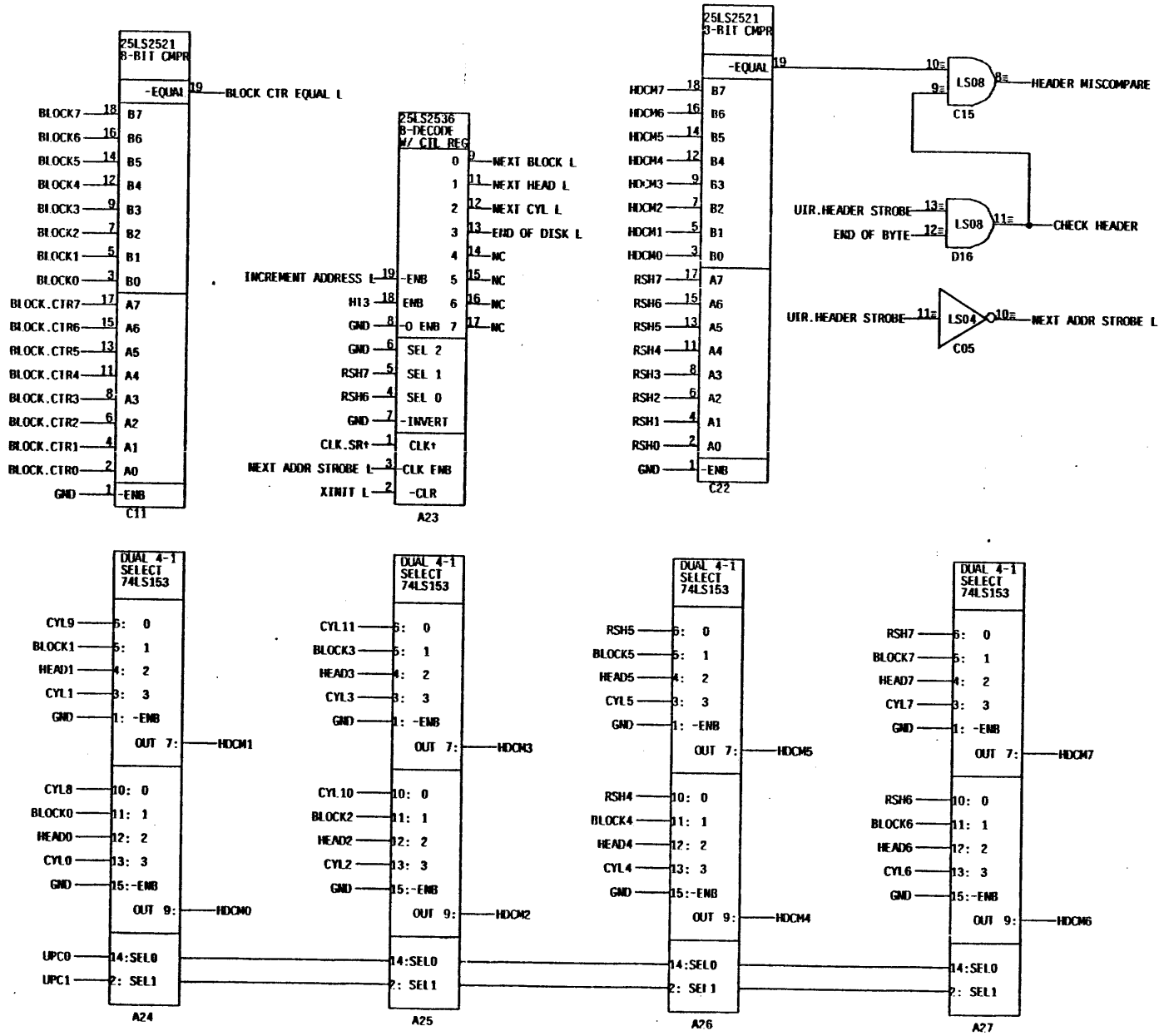
A7 A8 A9
A10 B7 B8

BE CERTAIN TO EDIT THE
RAY FILE FOR UNDEDICATED
GROUND PINS ON J1, J3

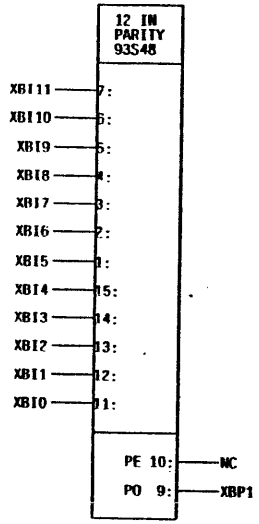
TO DISK MUX BOARD

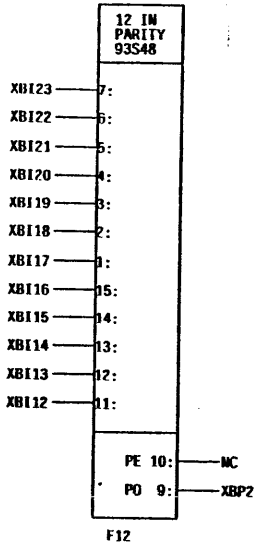


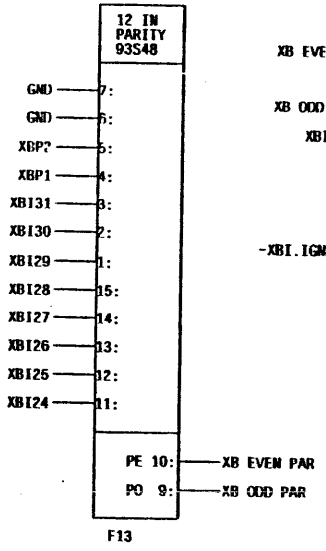
DISK CONTROL	EDGE CONNECTIONS	10-JUN-1979 20:33	AI: CADRDC; DCEDGE

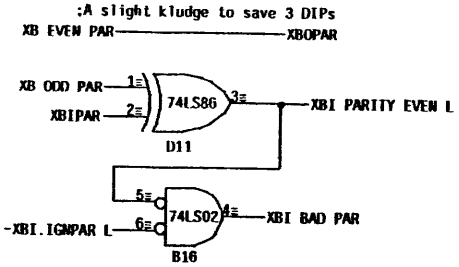


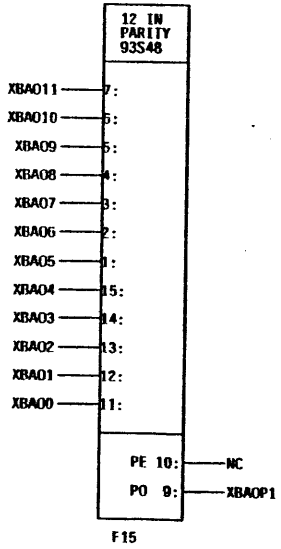
DISK CONTROL	HEADER COMPARE	10-JUN-1979 20:34	AI: CADRDC; DCHDCM

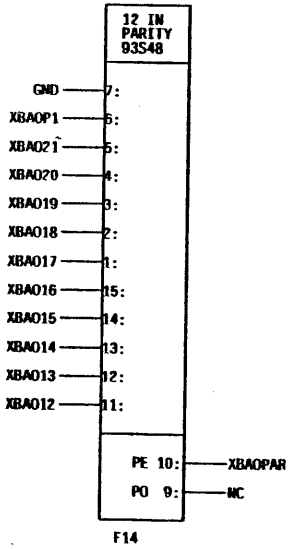

12 IN PARITY 93S48
XBI11 7:
XBI10 6:
XBI9 5:
XBI8 4:
XBI7 3:
XBI6 2:
XBI5 1:
XBI4 15:
XBI3 14:
XBI2 13:
XBI1 12:
XBI0 11:
PE 10: NC
PO 9: XBP1
F11

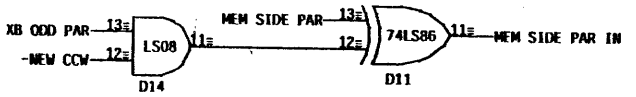

12 IN PARITY 93S48
XBI23 7:
XBI22 6:
XBI21 5:
XBI20 4:
XBI19 3:
XBI18 2:
XBI17 1:
XBI16 15:
XBI15 14:
XBI14 13:
XBI13 12:
XBI12 11:
PE 10: NC
PO 9: XBP2
F12

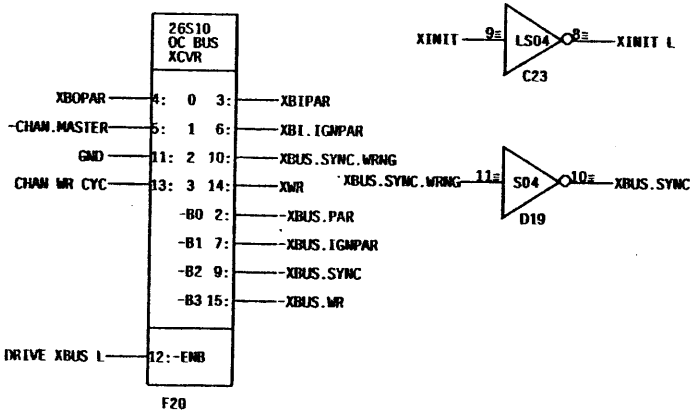

12 IN PARITY 93S48
GND 7:
GND 6:
XBP? 5:
XBP1 4:
XBI31 3:
XBI30 2:
XBI29 1:
XBI28 15:
XBI27 14:
XBI26 13:
XBI25 12:
XBI24 11:
PE 10: XB EVEN PAR
PO 9: XB ODD PAR
F13

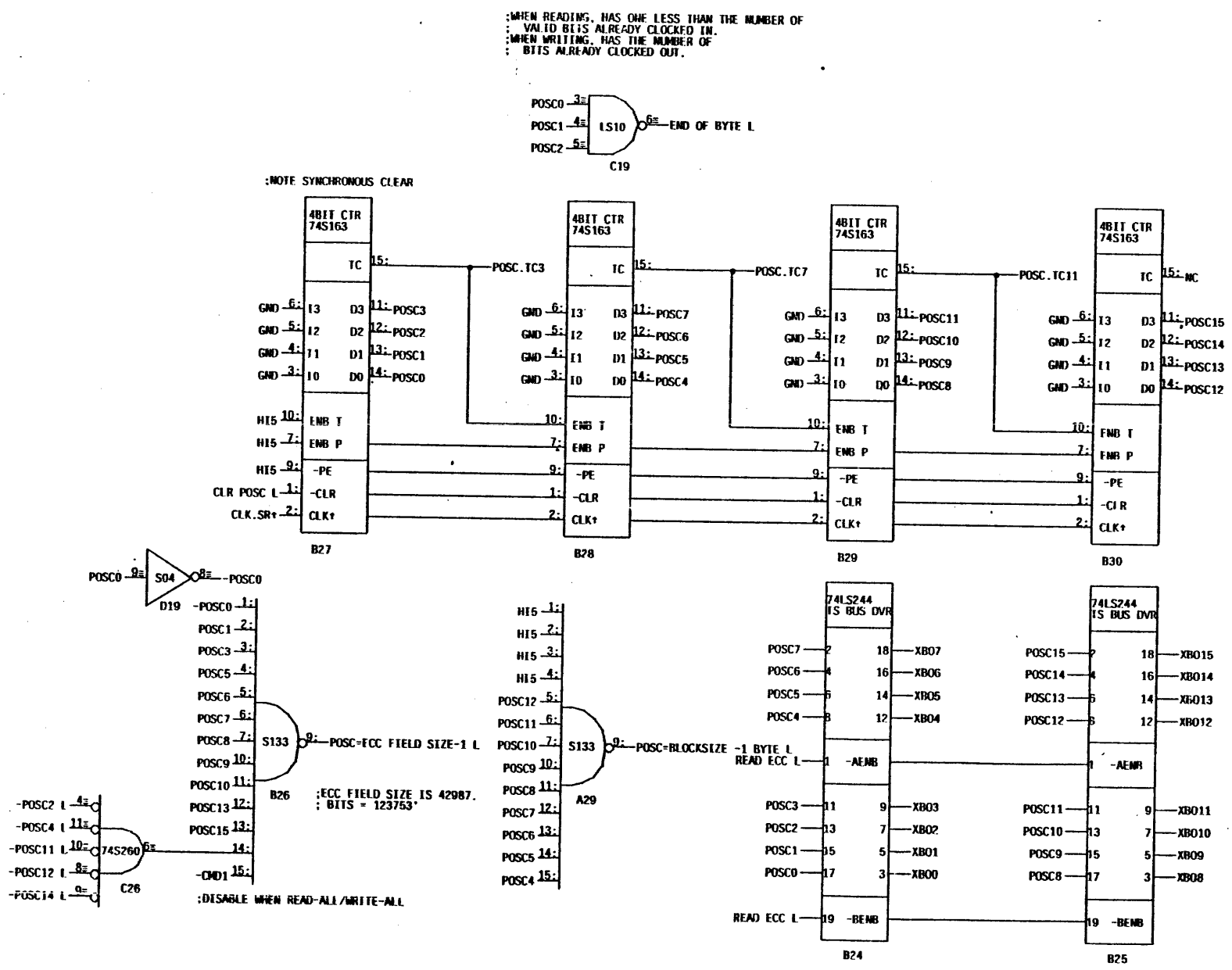

:A slight kludge to save 3 DIPs
XB EVEN PAR
XBOPAR
XB ODD PAR
XBIPAR
74LS86
D11
XBI PARITY EVEN L
-XBI.IGNPAR L
74LS02
B16
XBI BAD PAR

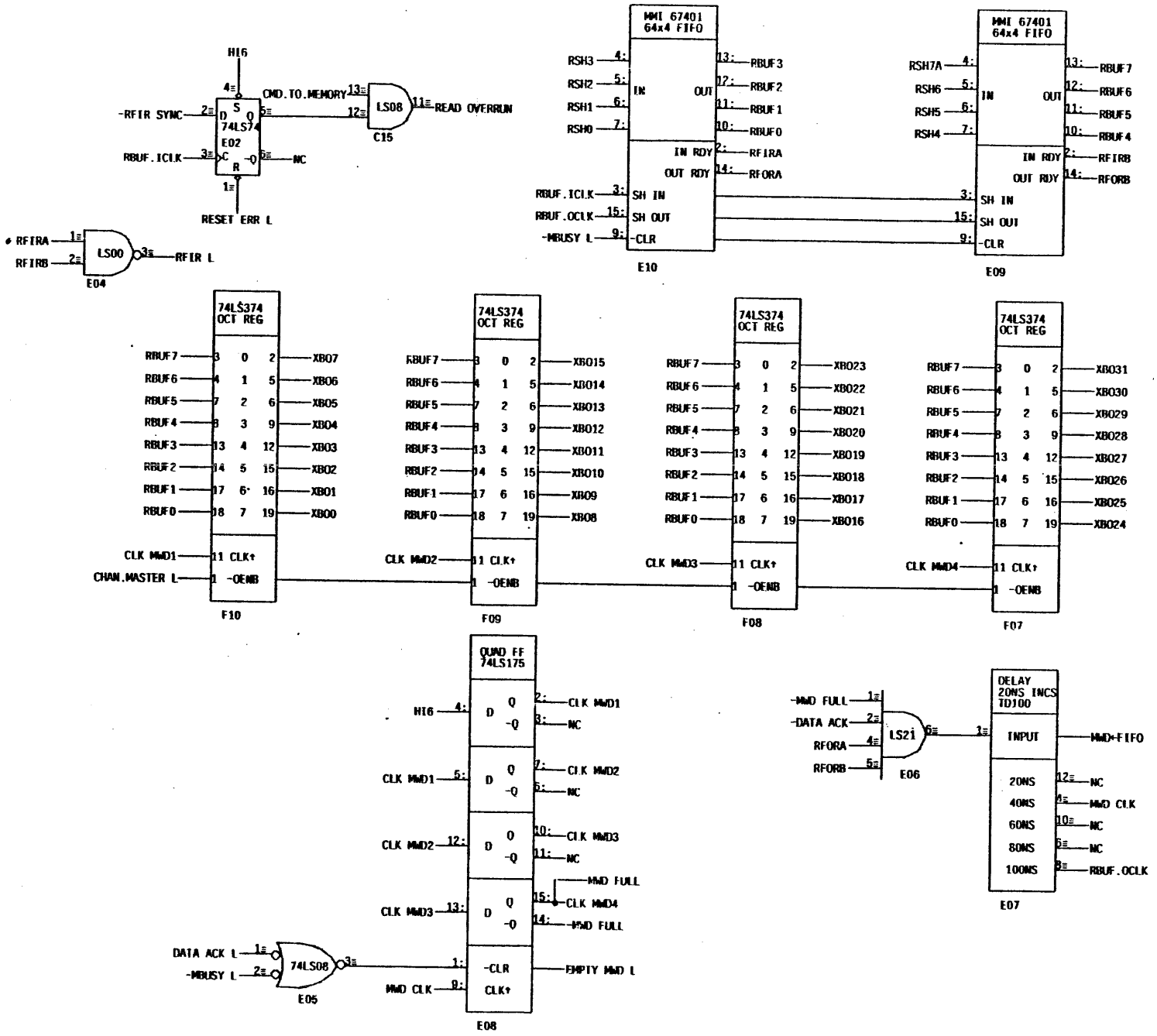

12 IN PARITY 93S48
XBA011 7:
XBA010 6:
XBA09 5:
XBA08 4:
XBA07 3:
XBA06 2:
XBA05 1:
XBA04 15:
XBA03 14:
XBA02 13:
XBA01 12:
XBA00 11:
PE 10: NC
PO 9: XBAOP1
F15


12 IN PARITY 93S48
GND 7:
XBAOP1 6:
XBA021 5:
XBA020 4:
XBA019 3:
XBA018 2:
XBA017 1:
XBA016 15:
XBA015 14:
XBA014 13:
XBA013 12:
XBA012 11:
PE 10: XBAOPAR
PO 9: NC
F14

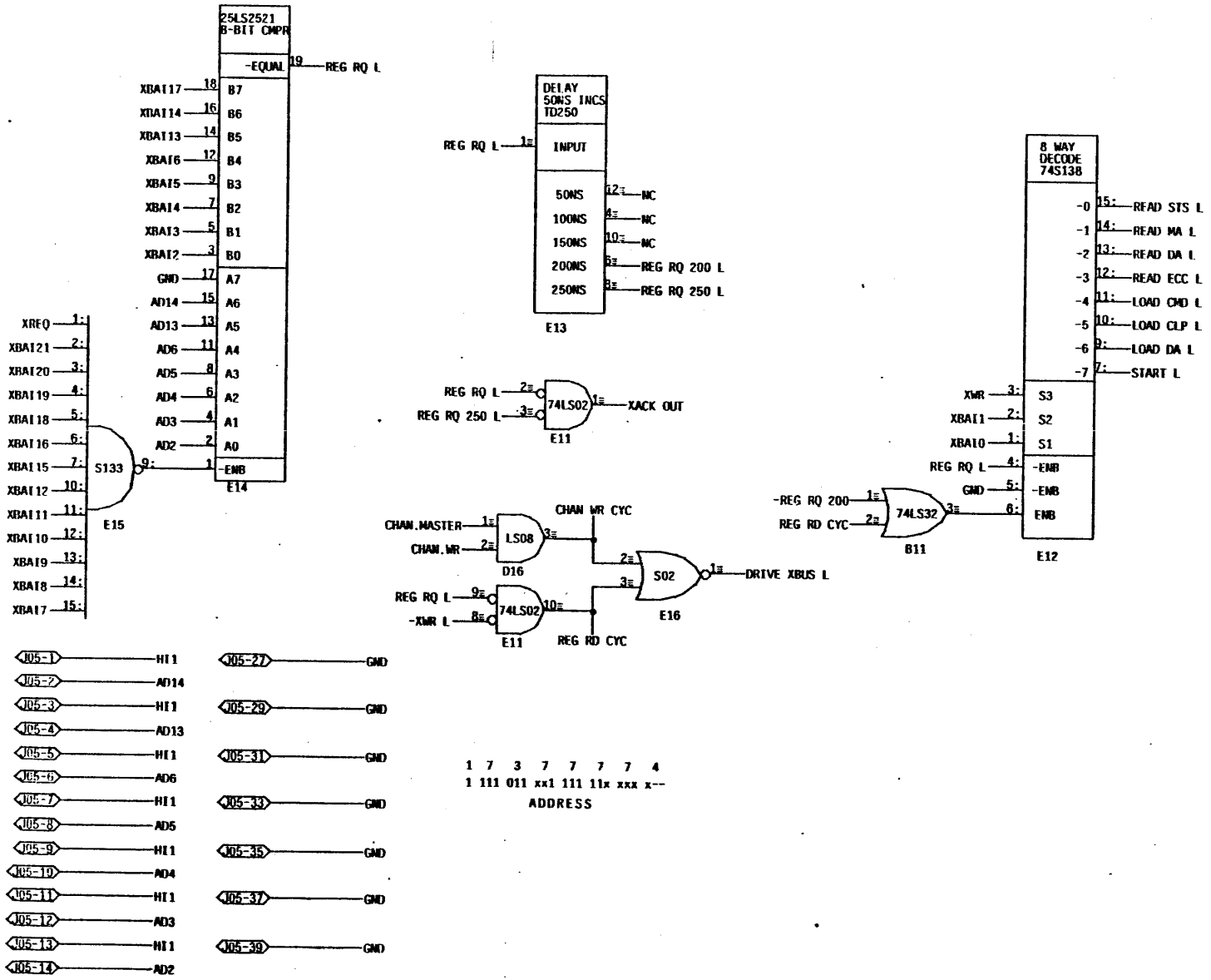

XB ODD PAR
-MEM CCW
LS08
D14
MEM SIDE PAR
74LS86
D11
MEM SIDE PAR IN


26S10 OC BUS XCVR
XBOPAR 4: 0 3: XBIPAR
-CHAN.MASTER 5: 1 6: XBI.IGNPAR
GND 11: 2 10: XBUS.SYNC.WRNG
CHAN WR CYC 13: 3 14: XWR
-B0 2: -XBUS.PAR
-B1 7: -XBUS.IGNPAR
-B2 9: -XBUS.SYNC
-B3 15: -XBUS.WR
DRIVE XBUS L 12:-ENB
F20
XINIT
LS04
C23
XINIT L
XBUS.SYNC.WRNG
S04
D19
XBUS.SYNC

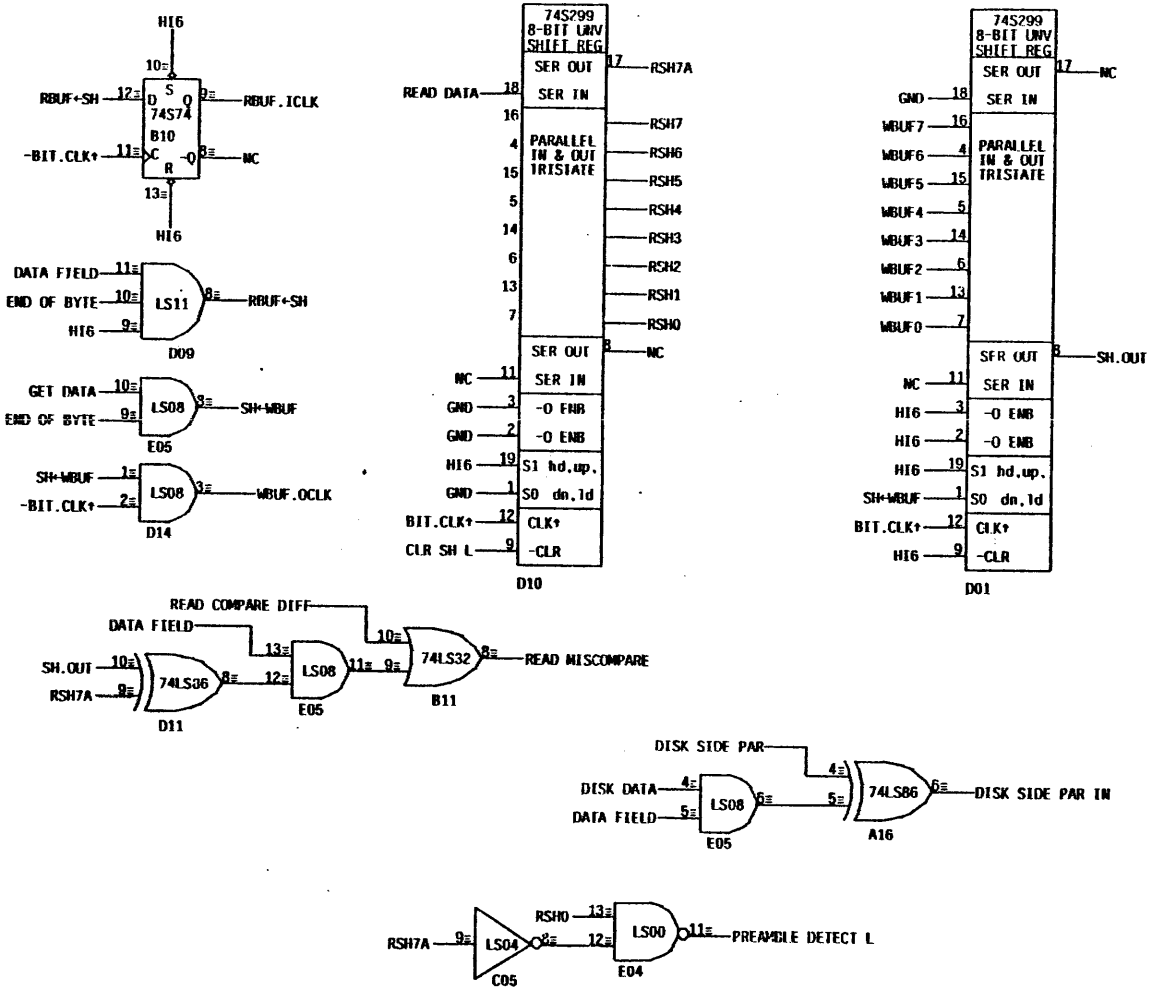

;WHEN READING, HAS ONE LESS THAN THE NUMBER OF
; VALID BITS ALREADY CLOCKED IN.
;WHEN WRITING, HAS THE NUMBER OF
; BITS ALREADY CLOCKED OUT.
POSC0
POSC1
POSC2
LS10
END OF BYTE L
C19
;NOTE SYNCHRONOUS CLEAR
4BIT CTR 74S163
TC
POSC.TC3
POSC.TC7
POSC.TC11
NC
GND
I3
I2
I1
I0
D3
D2
D1
D0
POSC3
POSC2
POSC1
POSC0
POSC7
POSC6
POSC5
POSC4
POSC11
POSC10
POSC9
POSC8
POSC15
POSC14
POSC13
POSC12
HI5
ENB T
ENB P
-PE
CLR POSC L
-CLR
CLK.SR↑
CLK↑
B27
B28
B29
B30
POSC0
S04
-POSC0
D19
-POSC0
POSC1
POSC3
POSC5
POSC6
POSC7
POSC8
POSC9
POSC10
POSC13
POSC15
-CMD1
S133
POSC=ECC FIELD SIZE-1 L
B26
;ECC FIELD SIZE IS 42987.
; BITS = 123753*
-POSC2 L
-POSC4 L
-POSC11 L
-POSC12 L
-POSC14 L
74S260
C26
;DISABLE WHEN READ-ALL/WRITE-ALL
HI5
POSC12
POSC11
POSC10
POSC9
POSC8
POSC7
POSC6
POSC5
POSC4
S133
POSC=BLOCKSIZE -1 BYTE L
A29
74LS244
IS BUS DVR
POSC7
POSC6
POSC5
POSC4
POSC3
POSC2
POSC1
POSC0
XB07
XB06
XB05
XB04
XB03
XB02
XB01
XB00
READ ECC L
-AENB
-BENB
B24
POSC15
POSC14
POSC13
POSC12
POSC11
POSC10
POSC9
POSC8
XB015
XB014
XB013
XB012
XB011
XB010
XB09
XB08
B25

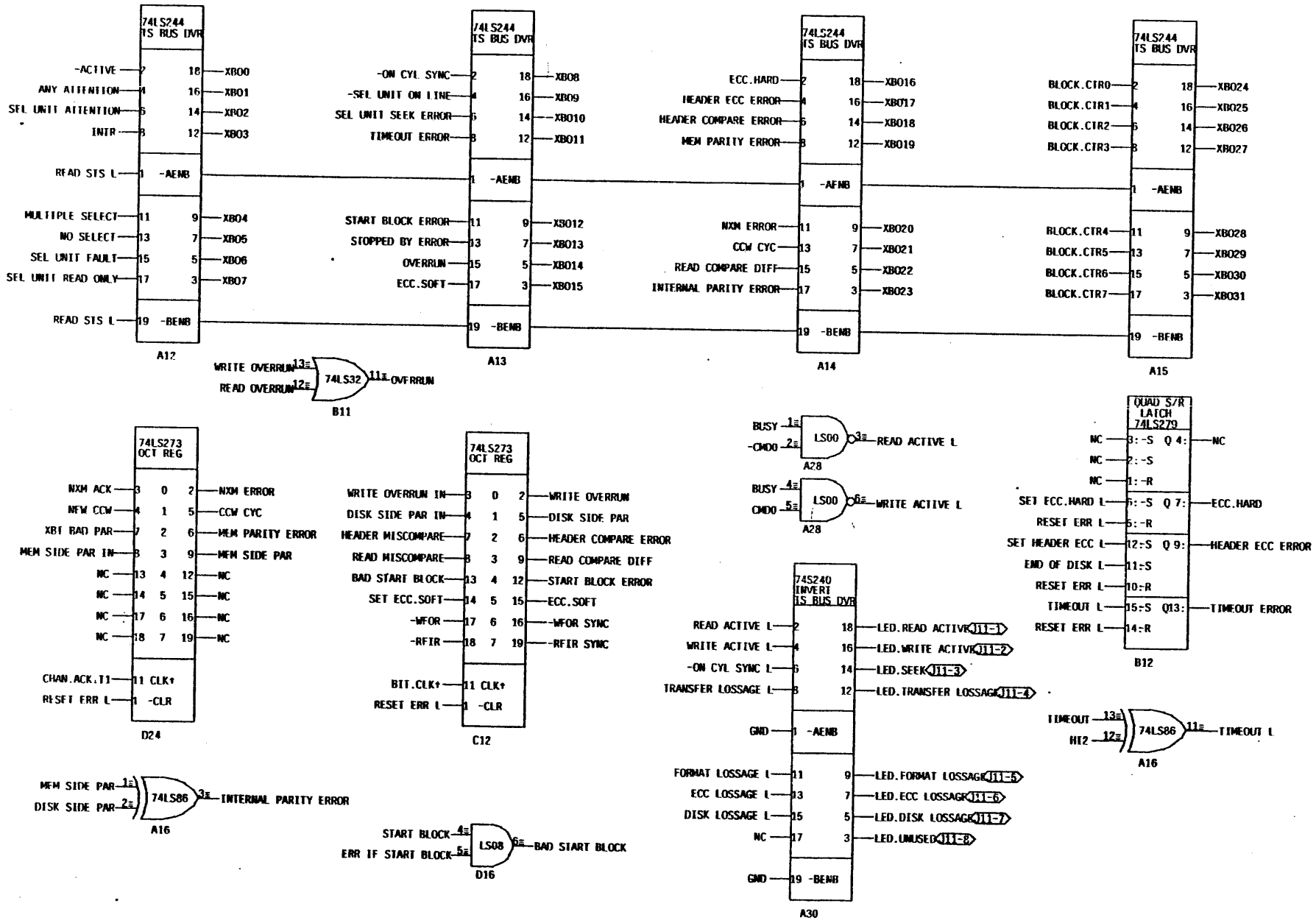


DISK CONTROL	READ BUFFER	30-SEP-1978 04:07	AI: CADRDC; DCRBUF

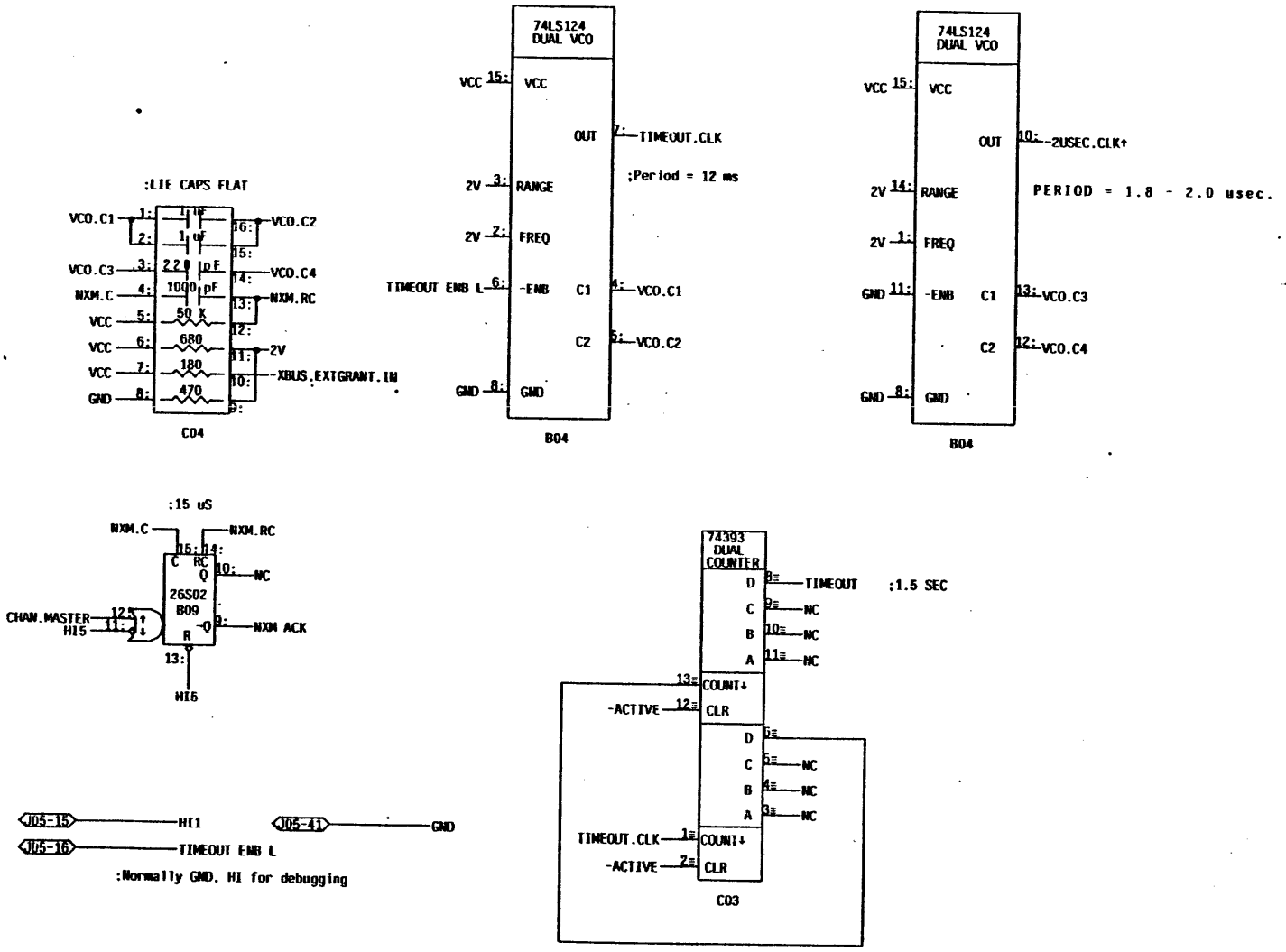


DISK CONTROL	REGISTER ADDRESSING	8-OCT-1978 16:56	AI: CADRDC; DCREG

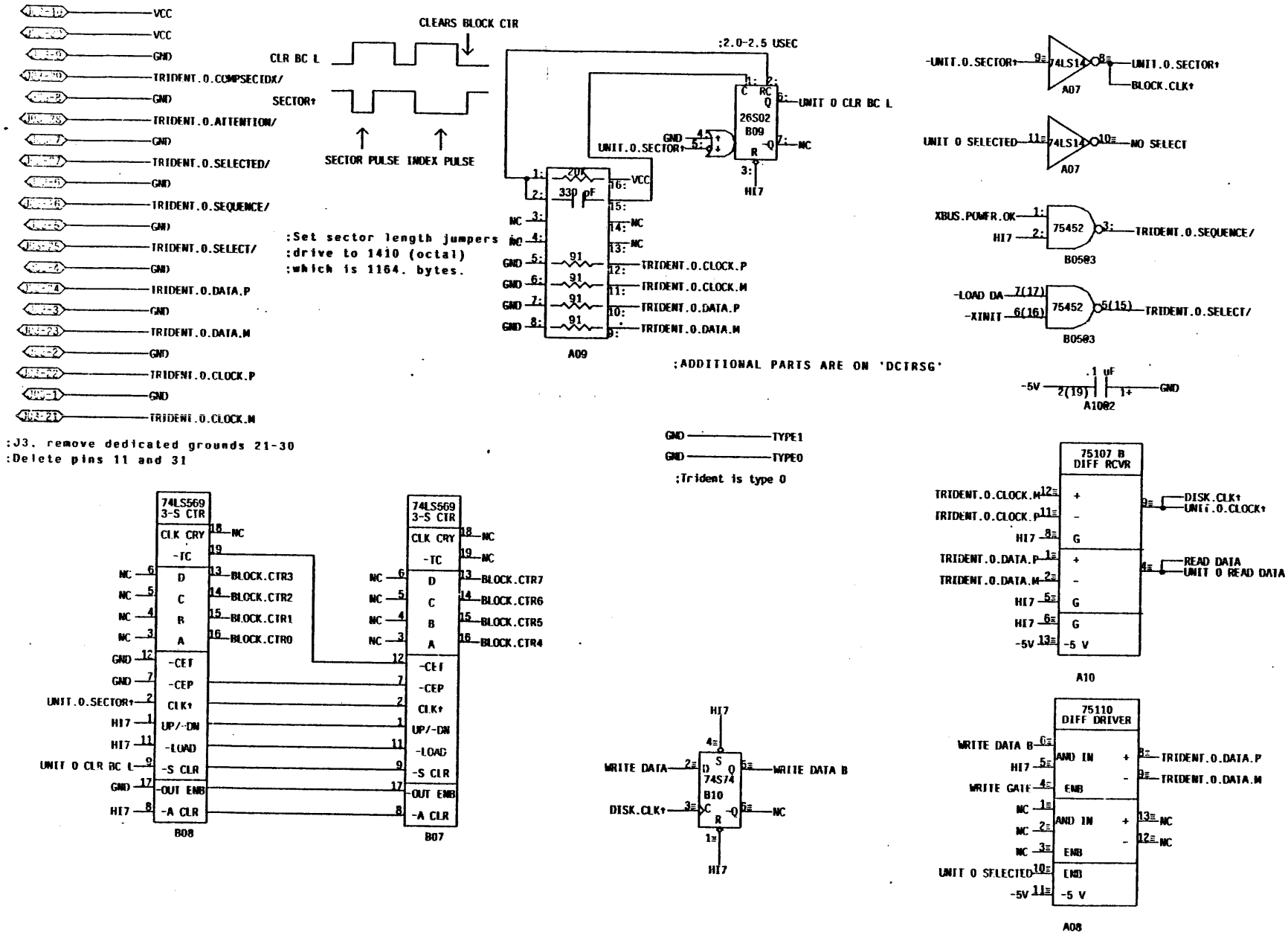

HI6
10
RBUF+SH
12
S
D
Q
74S74
B10
C
R
Q
9
RBUF.ICLK
-BIT.CLK↑
11
8
NC
13
HI6
DATA FIELD
11
END OF BYTE
10
LS11
8
RBUF+SH
HI6
9
D09
GET DATA
10
END OF BYTE
9
LS08
8
SH+WBUF
E05
SH+WBUF
1
-BIT.CLK↑
2
LS08
3
WBUF.OCLK
D14
74S299
8-BIT UNV
SHIFT REG
SER OUT
17
RSH7A
READ DATA
18
SER IN
16
RSH7
4
RSH6
PARALLEL
IN & OUT
TRISTATE
15
RSH5
5
RSH4
14
RSH3
6
RSH2
13
RSH1
7
RSH0
SER OUT
8
NC
NC
11
SER IN
GND
3
-O ENB
GND
2
-O ENB
HI6
19
S1 hd,up,
GND
1
S0 dn,ld
BIT.CLK↑
12
CLK↑
CLR SH L
9
-CLR
D10
74S299
8-BIT UNV
SHIFT REG
SER OUT
17
NC
GND
18
SER IN
WBUF7
16
WBUF6
4
PARALLEL
IN & OUT
TRISTATE
WBUF5
15
WBUF4
5
WBUF3
14
WBUF2
6
WBUF1
13
WBUF0
7
SER OUT
8
SH.OUT
NC
11
SER IN
HI6
3
-O ENB
HI6
2
-O ENB
HI6
19
S1 hd,up,
SH+WBUF
1
S0 dn,ld
BIT.CLK↑
12
CLK↑
HI6
9
-CLR
D01
READ COMPARE DIFF
DATA FIELD
13
10
SH.OUT
10
74LS36
8
LS08
11
9
74LS32
8
READ MISCOMPARE
RSH7A
9
12
D11
E05
B11
DISK SIDE PAR
4
DISK DATA
4
LS08
6
5
74LS86
6
DISK SIDE PAR IN
DATA FIELD
5
E05
A16
RSH0
13
RSH7A
9
LS04
8
LS00
11
PREAMBLE DETECT L
12
C05
E04



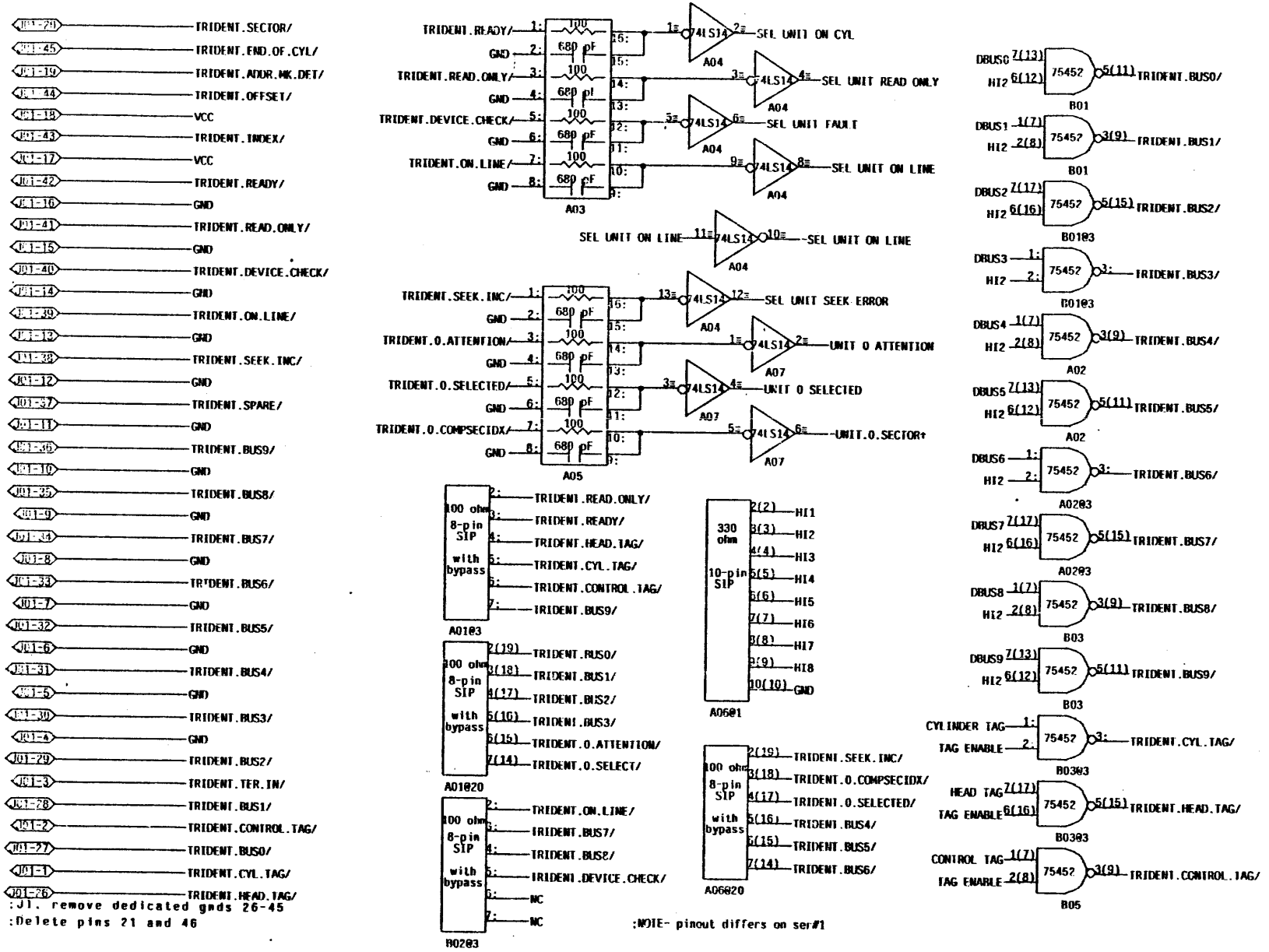
DISK CONTROL	STATUS	5-FEB-1980 01:50	AI: CADRDC; DCSTS



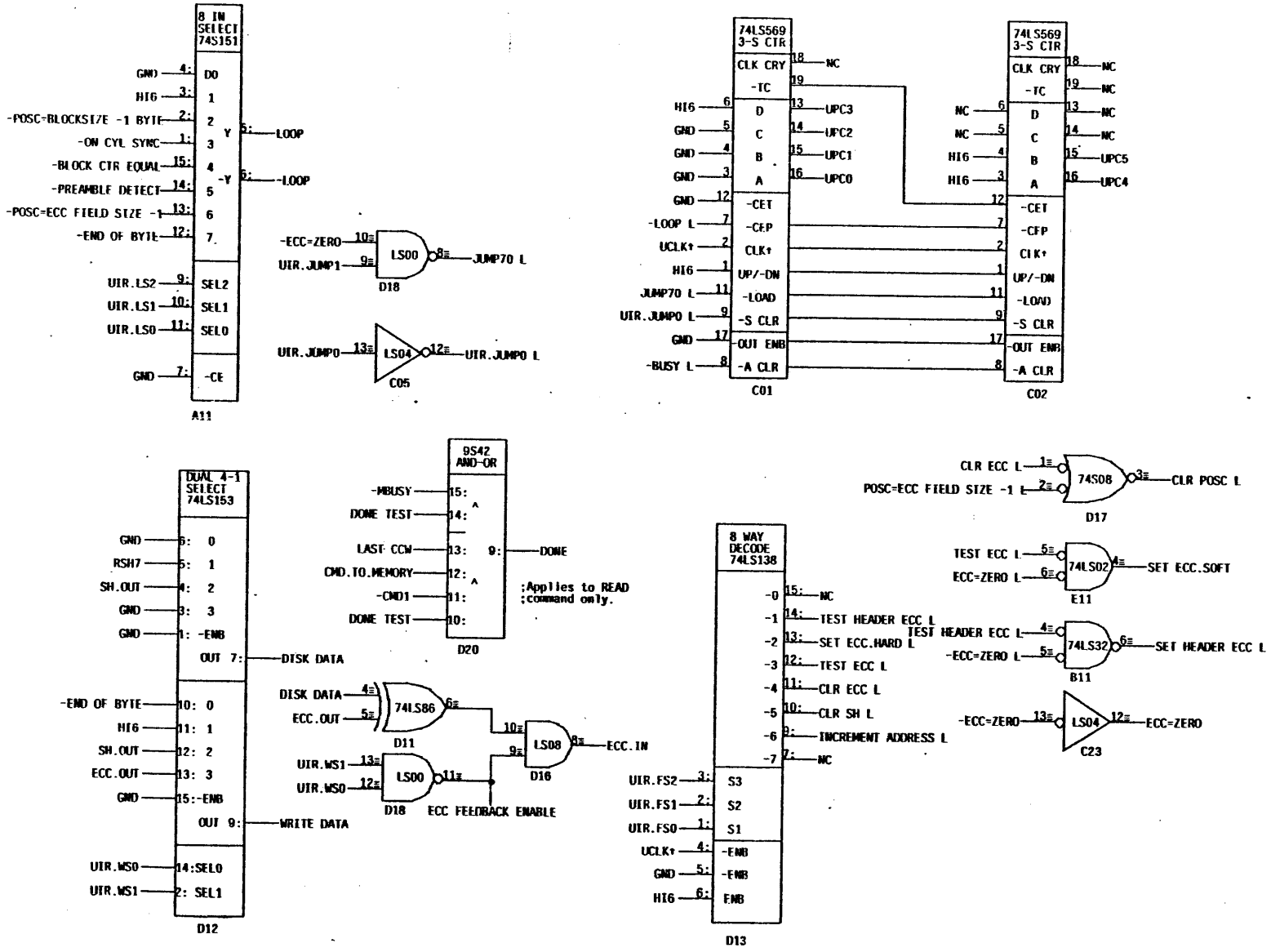
DISK CONTROL	TIMEOUT	7-OCT-1980 22:12	AI: CADRDC; DCTMOT



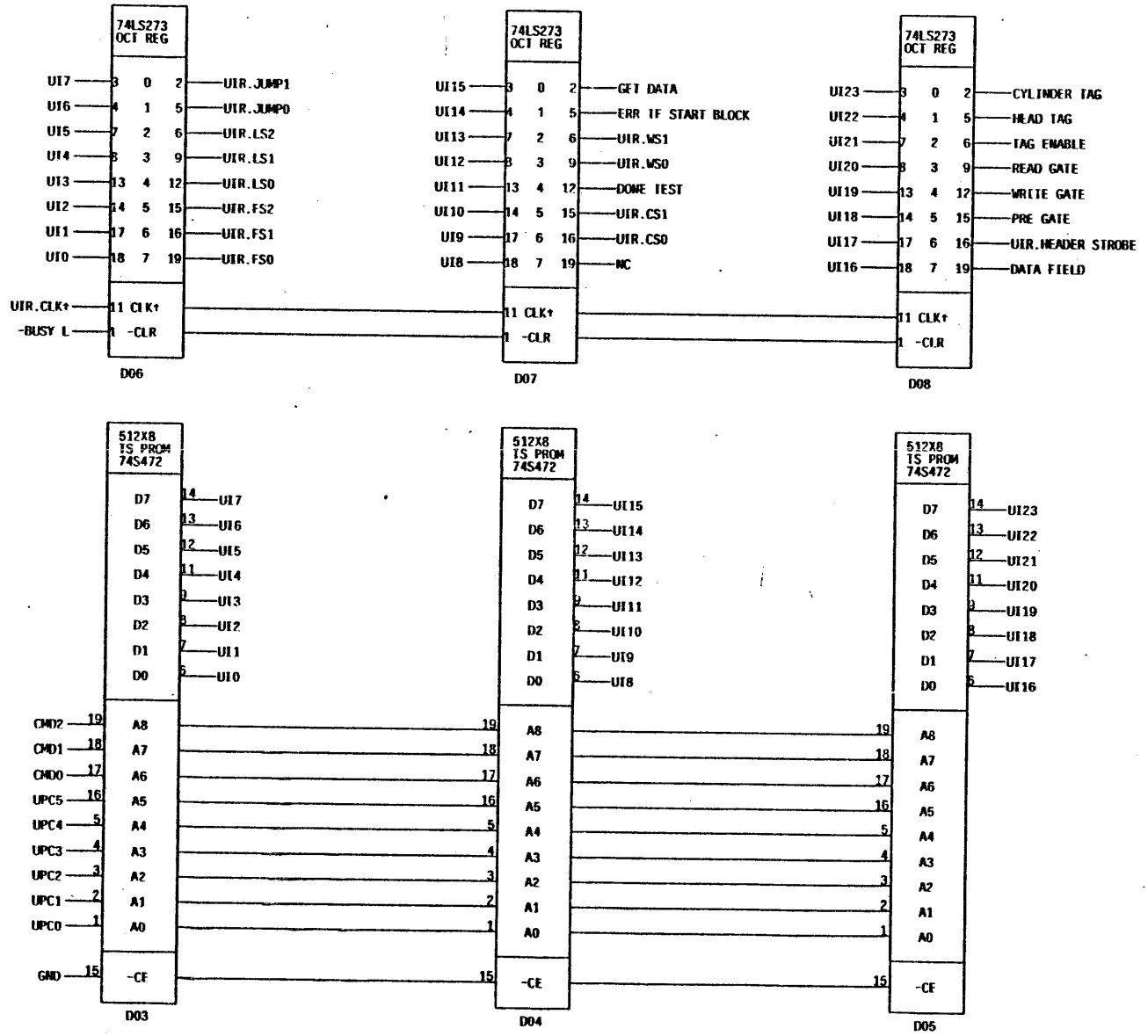
DISK CONTROL	SINGLE TRIDENT	10-JUN-1979 21:54	AI: CADRDC; DCTRID

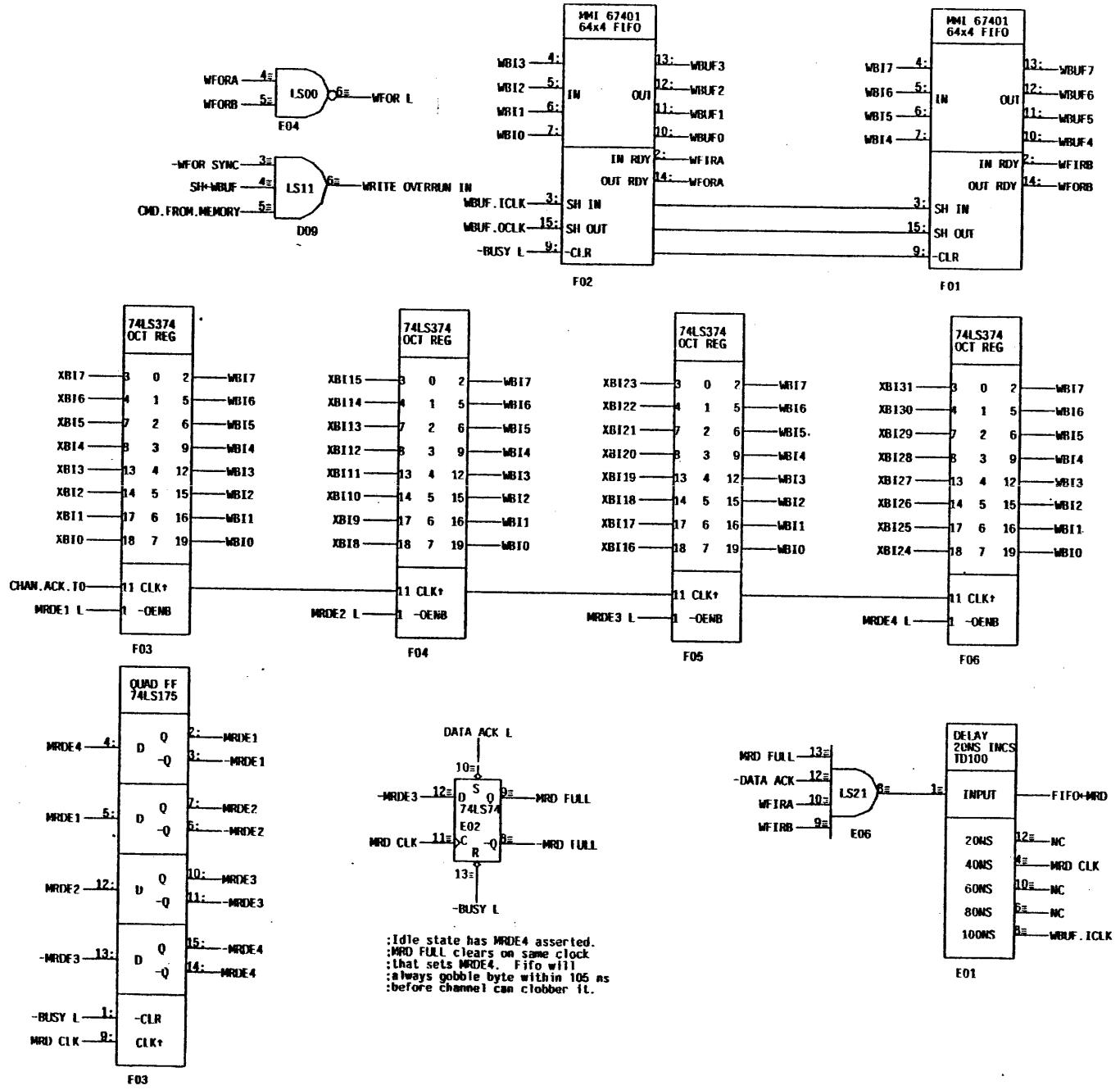


DISK CONTROL	TRIDENT SIGNAL CABLE	30-JUL-1979 02:11	AI: CADRDC; DCTRSG

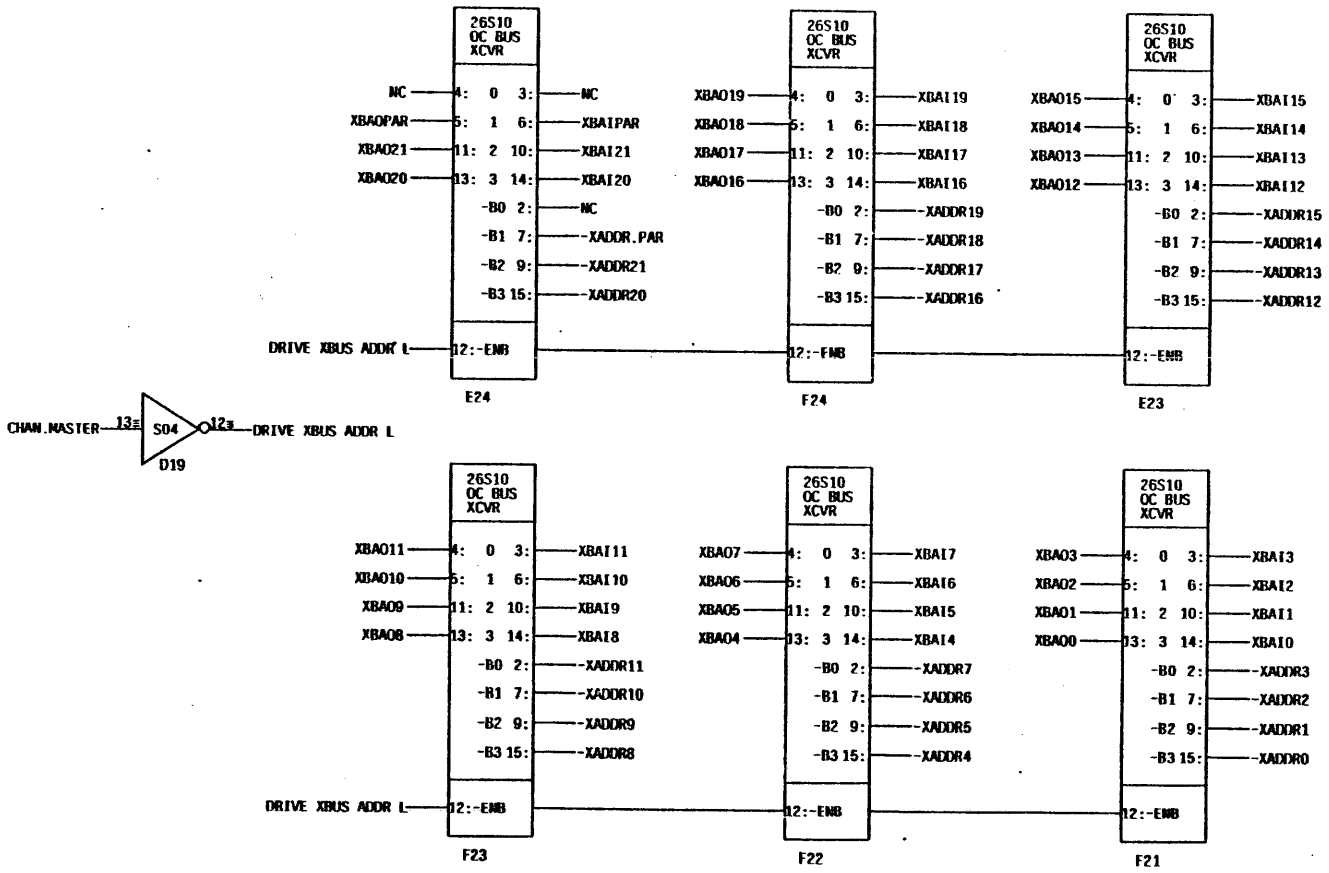


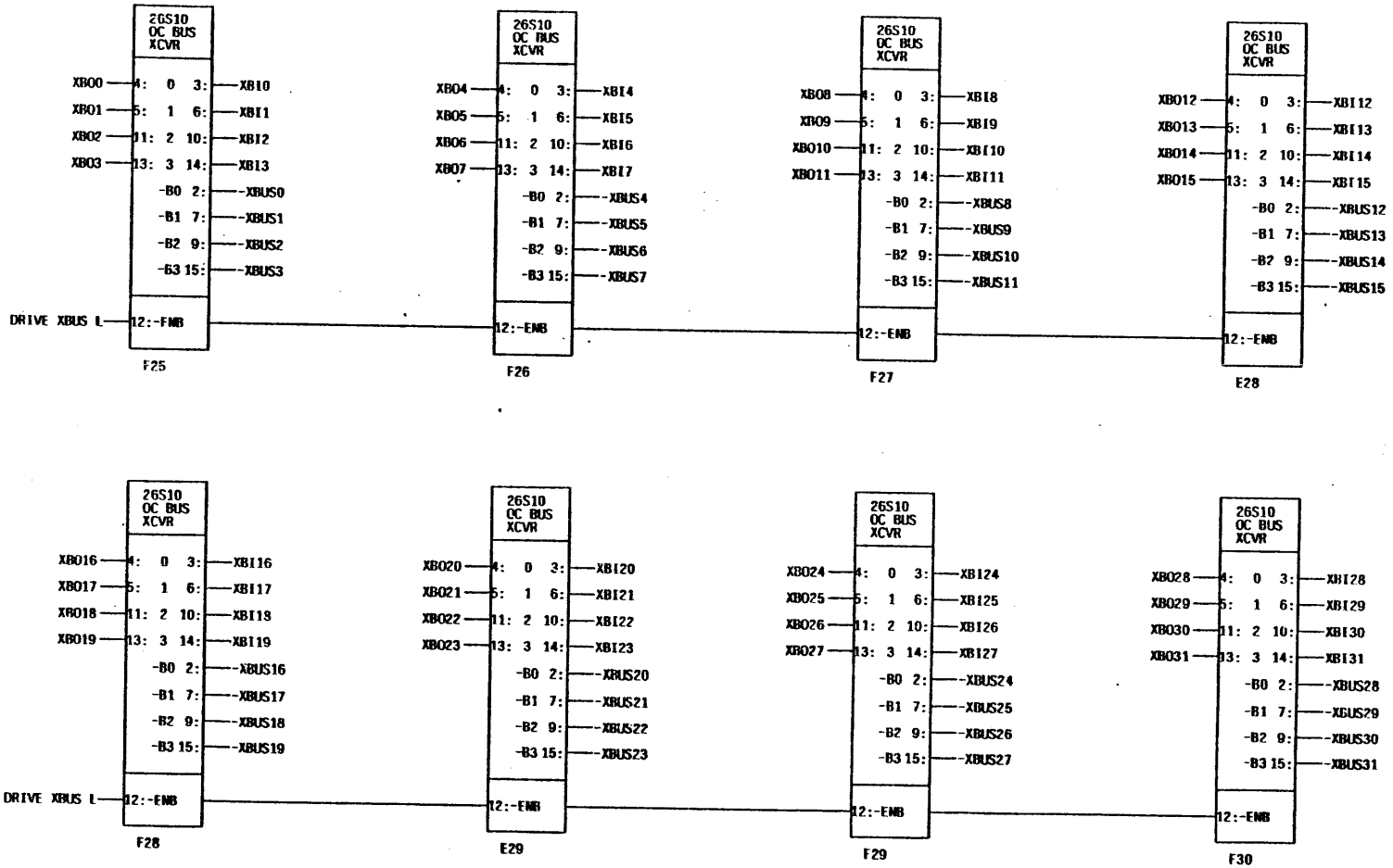
DISK CONTROL	MICROCODE CONTROL	10-JUN-1979 20:40	AI: CADRDC; DCUC

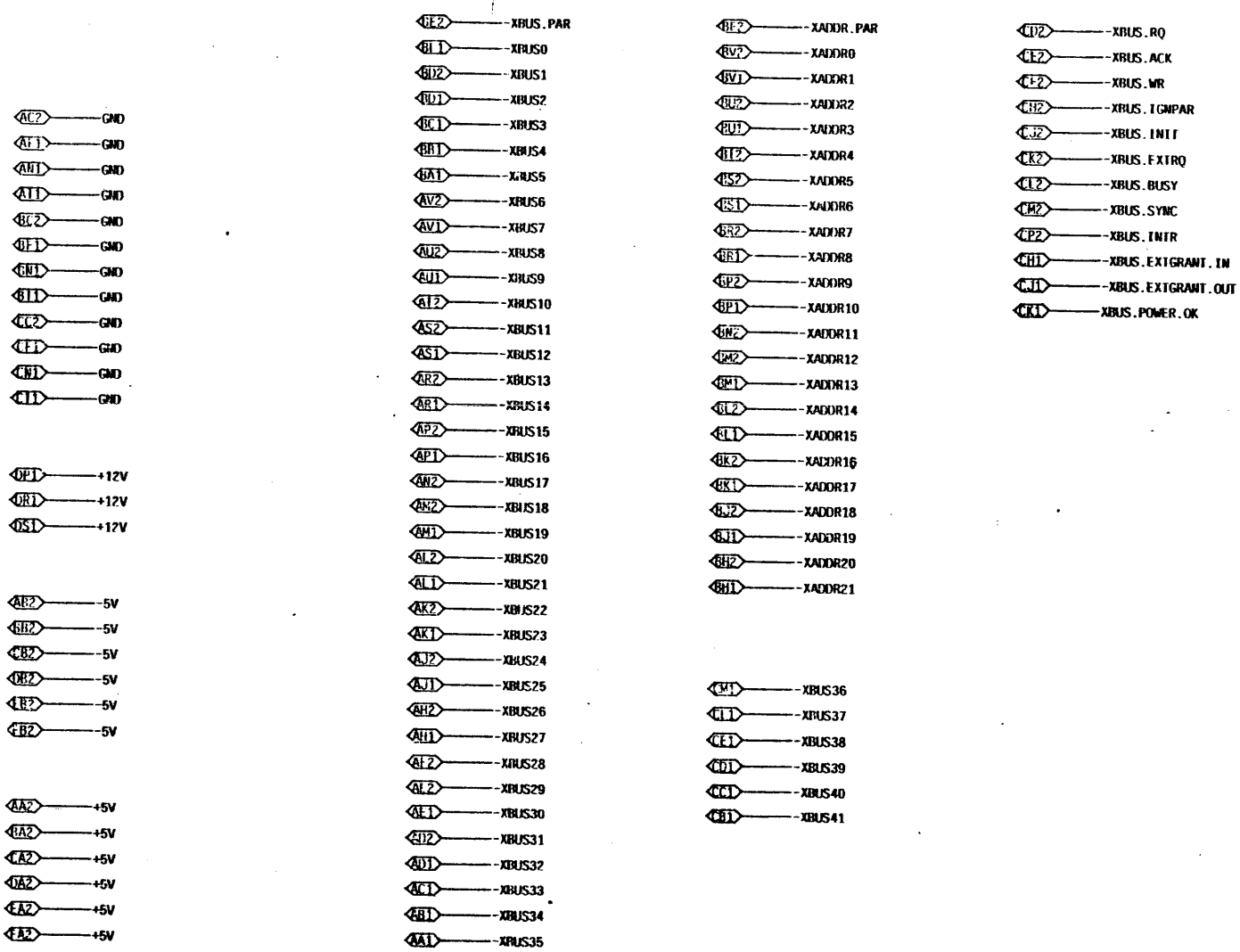

74LS273
OCT REG
UI7
UI6
UI5
UI4
UI3
UI2
UI1
UI0
UIR.JUMP1
UIR.JUMP0
UIR.LS2
UIR.LS1
UIR.LS0
UIR.FS2
UIR.FS1
UIR.FS0
UIR.CLK↑
-BUSY L
CLK↑
-CLR
D06
UI15
UI14
UI13
UI12
UI11
UI10
UI9
UI8
GET DATA
ERR IF START BLOCK
UIR.WS1
UIR.WS0
DONE TEST
UIR.CS1
UIR.CS0
NC
D07
UI23
UI22
UI21
UI20
UI19
UI18
UI17
UI16
CYLINDER TAG
HEAD TAG
TAG ENABLE
READ GATE
WRITE GATE
PRE GATE
UIR.HEADER STROBE
DATA FIELD
D08
512X8
TS PROM
74S472
D7
D6
D5
D4
D3
D2
D1
D0
A8
A7
A6
A5
A4
A3
A2
A1
A0
-CE
CMD2
CMD1
CMD0
UPC5
UPC4
UPC3
UPC2
UPC1
UPC0
GND
D03
D04
D05

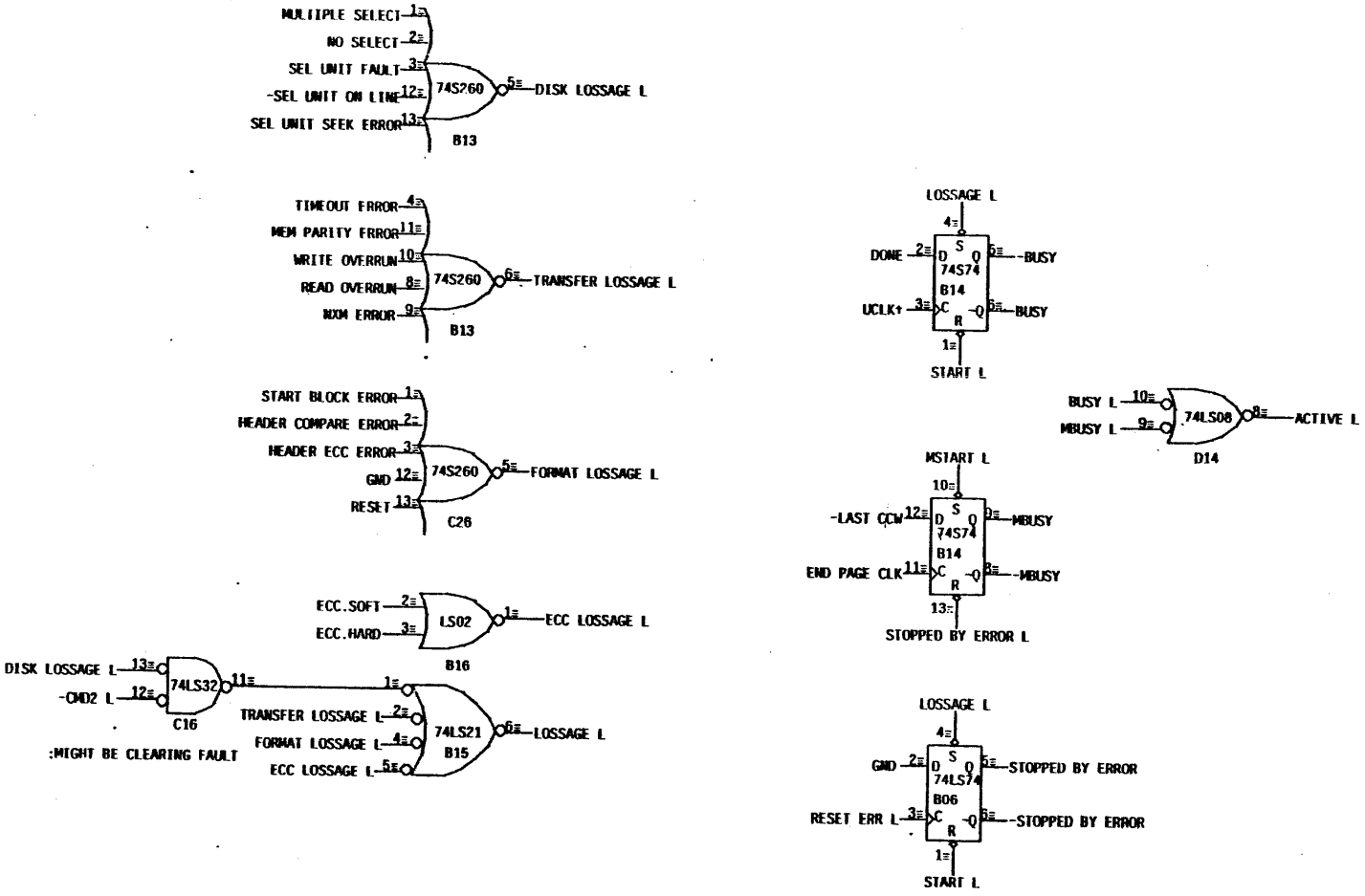


DISK CONTROL	WRITE BUFFER	30-SEP-1978 02:27	AI: CADRDC; DCWBUF

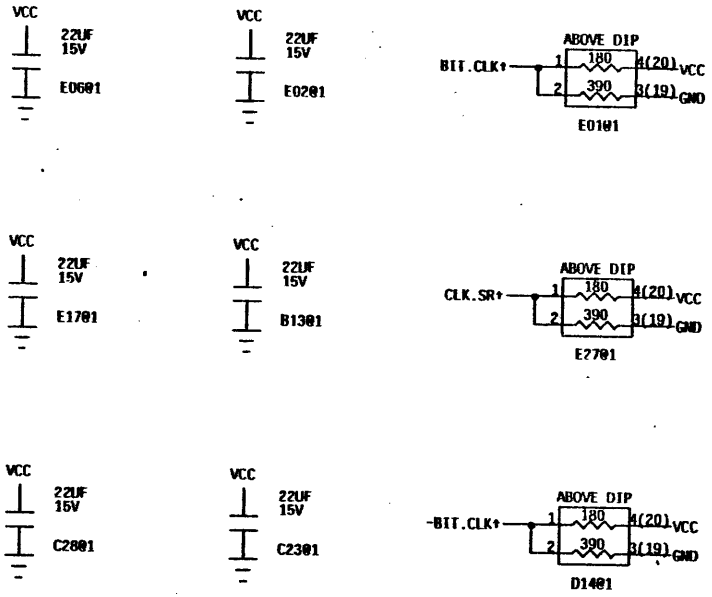

26S10
OC BUS
XCVR
NC
XBAOPAR
XBAO21
XBAO20
4: 0 3:
5: 1 6:
11: 2 10:
13: 3 14:
-B0 2:
-B1 7:
-B2 9:
-B3 15:
12:-ENB
NC
XBAIPAR
XBAI21
XBAI20
NC
-XADDR.PAR
-XADDR21
-XADDR20
DRIVE XBUS ADDR L
E24
XBAO19
XBAO18
XBAO17
XBAO16
XBAI19
XBAI18
XBAI17
XBAI16
-XADDR19
-XADDR18
-XADDR17
-XADDR16
F24
XBAO15
XBAO14
XBAO13
XBAO12
XBAI15
XBAI14
XBAI13
XBAI12
-XADDR15
-XADDR14
-XADDR13
-XADDR12
E23
CHAN.MASTER
13
S04
12
DRIVE XBUS ADDR L
D19
XBAO11
XBAO10
XBAO9
XBAO8
XBAI11
XBAI10
XBAI9
XBAI8
-XADDR11
-XADDR10
-XADDR9
-XADDR8
F23
XBAO7
XBAO6
XBAO5
XBAO4
XBAI7
XBAI6
XBAI5
XBAI4
-XADDR7
-XADDR6
-XADDR5
-XADDR4
F22
XBAO3
XBAO2
XBAO1
XBAO0
XBAI3
XBAI2
XBAI1
XBAI0
-XADDR3
-XADDR2
-XADDR1
-XADDR0
F21

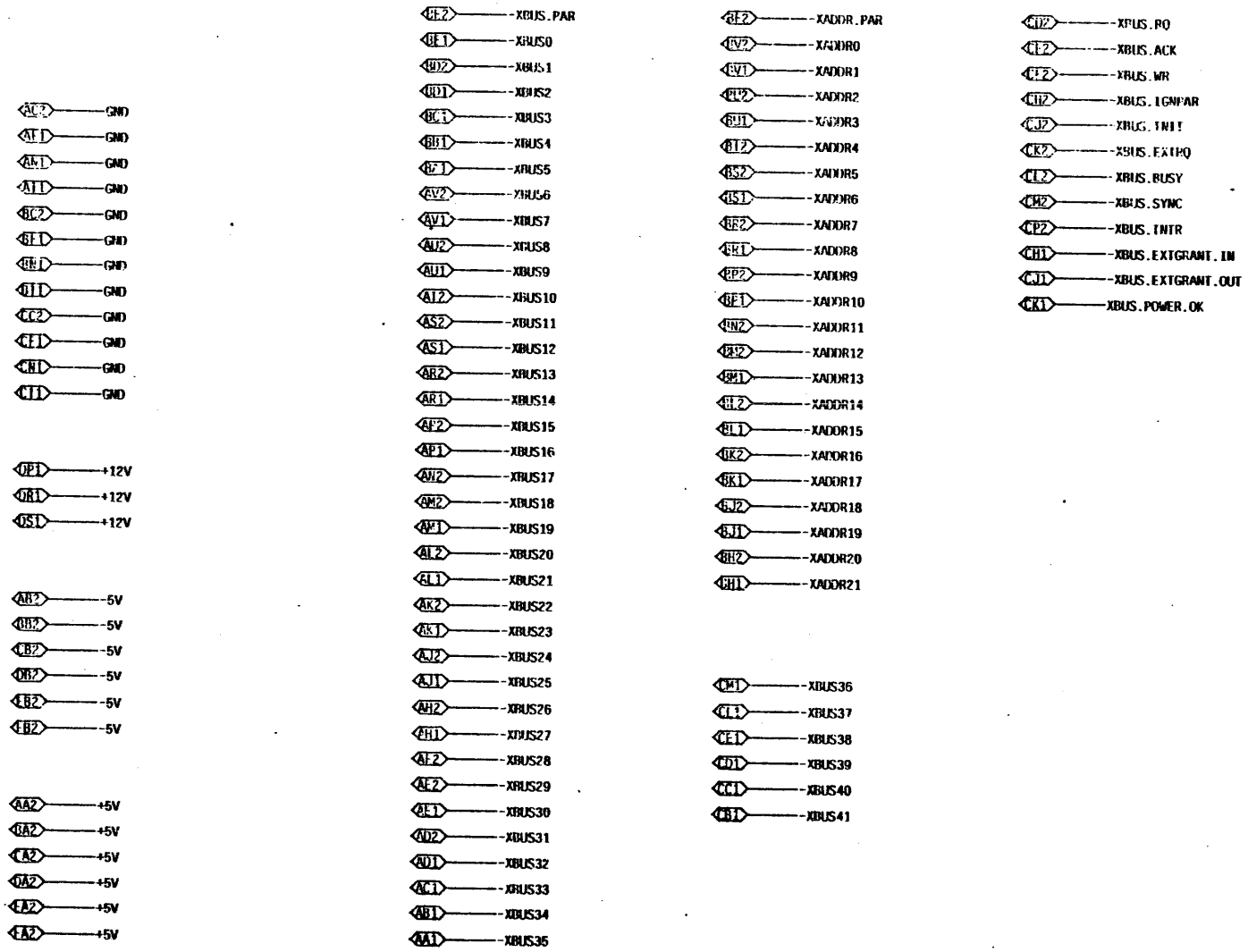

26S10
OC BUS
XCVR
XBO0
XBO1
XBO2
XBO3
4: 0 3:
5: 1 6:
11: 2 10:
13: 3 14:
-B0 2:
-B1 7:
-B2 9:
-B3 15:
XBI0
XBI1
XBI2
XBI3
-XBUS0
-XBUS1
-XBUS2
-XBUS3
DRIVE XBUS L
12:-ENB
F25
XBO4
XBO5
XBO6
XBO7
XBI4
XBI5
XBI6
XBI7
-XBUS4
-XBUS5
-XBUS6
-XBUS7
F26
XBO8
XBO9
XBO10
XBO11
XBI8
XBI9
XBI10
XBI11
-XBUS8
-XBUS9
-XBUS10
-XBUS11
F27
XBO12
XBO13
XBO14
XBO15
XBI12
XBI13
XBI14
XBI15
-XBUS12
-XBUS13
-XBUS14
-XBUS15
E28
XBO16
XBO17
XBO18
XBO19
XBI16
XBI17
XBI18
XBI19
-XBUS16
-XBUS17
-XBUS18
-XBUS19
F28
XBO20
XBO21
XBO22
XBO23
XBI20
XBI21
XBI22
XBI23
-XBUS20
-XBUS21
-XBUS22
-XBUS23
E29
XBO24
XBO25
XBO26
XBO27
XBI24
XBI25
XBI26
XBI27
-XBUS24
-XBUS25
-XBUS26
-XBUS27
F29
XBO28
XBO29
XBO30
XBO31
XBI28
XBI29
XBI30
XBI31
-XBUS28
-XBUS29
-XBUS30
-XBUS31
F30


AC2 GND
AF1 GND
AM1 GND
AT1 GND
BC2 GND
BF1 GND
BN1 GND
BT1 GND
CC2 GND
CF1 GND
CN1 GND
CT1 GND
DP1 +12V
DR1 +12V
DS1 +12V
AB2 -5V
BH2 -5V
CB2 -5V
DB2 -5V
EB2 -5V
FB2 -5V
AA2 +5V
BA2 +5V
CA2 +5V
DA2 +5V
EA2 +5V
FA2 +5V
GE2 -XBUS.PAR
BL1 -XBUS0
BU2 -XBUS1
BU1 -XBUS2
BC1 -XBUS3
BA1 -XBUS4
BA1 -XBUS5
AV2 -XBUS6
AV1 -XBUS7
AU2 -XBUS8
AU1 -XBUS9
AT2 -XBUS10
AS2 -XBUS11
AS1 -XBUS12
AR2 -XBUS13
AR1 -XBUS14
AP2 -XBUS15
AP1 -XBUS16
AN2 -XBUS17
AM2 -XBUS18
AM1 -XBUS19
AL2 -XBUS20
AL1 -XBUS21
AK2 -XBUS22
AK1 -XBUS23
AJ2 -XBUS24
AJ1 -XBUS25
AH2 -XBUS26
AH1 -XBUS27
AF2 -XBUS28
AL2 -XBUS29
AE1 -XBUS30
AU2 -XBUS31
AU1 -XBUS32
AC1 -XBUS33
AB1 -XBUS34
AA1 -XBUS35
BE2 -XADDR.PAR
BV2 -XADDR0
BV1 -XADDR1
BU2 -XADDR2
BU1 -XADDR3
BT2 -XADDR4
BS2 -XADDR5
BS1 -XADDR6
BR2 -XADDR7
BR1 -XADDR8
BP2 -XADDR9
BP1 -XADDR10
BN2 -XADDR11
BM2 -XADDR12
BM1 -XADDR13
BL2 -XADDR14
BL1 -XADDR15
BK2 -XADDR16
BK1 -XADDR17
BJ2 -XADDR18
BJ1 -XADDR19
BH2 -XADDR20
BH1 -XADDR21
CM1 -XBUS36
CL1 -XBUS37
CE1 -XBUS38
CD1 -XBUS39
CC1 -XBUS40
CB1 -XBUS41
CD2 -XBUS.RQ
CE2 -XBUS.ACK
CF2 -XBUS.WR
CH2 -XBUS.IGNPAR
CJ2 -XBUS.INIT
CK2 -XBUS.EXTRQ
CL2 -XBUS.BUSY
CM2 -XBUS.SYNC
CP2 -XBUS.INTR
CH1 -XBUS.EXTGRANT.IN
CJ1 -XBUS.EXTGRANT.OUT
CK1 -XBUS.POWER.OK



DISK CONTROL	BUSY, LOSSAGE	7-OCT-1980 21:32	AI: CADRDC; DCBUSY


VCC
22UF
15V
E0601
VCC
22UF
15V
E0201
ABOVE DIP
BIT.CLK↑
180
390
4(20)VCC
3(19)GND
E0101
VCC
22UF
15V
E1701
VCC
22UF
15V
B1301
ABOVE DIP
CLK.SR↑
180
390
4(20)VCC
3(19)GND
E2701
VCC
22UF
15V
C2801
VCC
22UF
15V
C2301
ABOVE DIP
-BIT.CLK↑
180
390
4(20)VCC
3(19)GND
D1401



XBUS	BACKPLANE CONNECTIONS	19-DEC-1979 00:54	AI: CADRDC; XBUS