

PDP-11 Unibus Chaosnet Interface CHAOS;UBCHNI UML 17-DEC-80 1800
 ***** DIP MAP *****

DM8838 QUBXCV x	74LS74 QADTIM xx	74LS193 QADTIM x	74LS193 QADTIM x	74LS174 LMUCON x	74LS193 QADTIM x
F20	E20	D20	C20	B20	A20
DM8836 QUBXCV x	74LS193 QADTIM x	74LS244 LMDATP x	74LS133 LMUCON x	74LS164 LMTURN x	74LS193 LMTURN x
F19	E19	D19	C19	B19	A19
DM8838 QUBXCV x	74LS244 LMDATP x	74LS244 LMDATP x	74LS138 LMUCON x	74LS164 LMTURN x	74LS193 LMTURN x
F18	E18	D18	C18	B18	A18
DM8838 QUBXCV x	74LS244 LMDATP x	74LS244 LMDATP x	74LS244 LMDATP x	74S04 QUBINT xoooo	74LS193 LMTURN x
F17	E17	D17	C17	B17	A17
74S38 QUBINT xxxx	25LS2521 QADADR x	74LS244 LMDATP x	74LS244 LMDATP x	74LS02 QUBINT xxxx	74LS161 LMTURN x
F16	E16	D16	C16	B16	A16
74S38 QUBINT xxx	25LS2521 QADADR x	74S32 LMRCLL xxxx	74S00 LMTBFC xxxx	74S74 LMMODU xx	74100 QUBINT x
F15	E15	D15	C15	B15	A15
74S175 QUBINT x	DUMMY QUBINT x	74S112 LMTURN xx	74S00 LMTBFC xxxx	74S04 LMTBFC xxxxxx	74LS163 QADTIM x
F14	E14	D14	C14	B14	A14
DUMMY QUBINT x	74S04 QADADR xxxxxx	74S112 LMTBFC xx	25LS193 LMTBUF x	74 165 LMTBUF x	74S37 QADADR xxox
F13	E13	D13	C13	B13	A13
74S00 QUBINT xxxx	74LS163 QADTIM x	DUMMY LMMYNN x	25LS193 LMTBUF x	74 165 LMTBUF x	74260 QADADR x
F12	E12	D12	C12	B12	A12
74LS10 QUBINT xxx	74LS02 QADADR xxox	P STP100 LMMYNN x	25LS193 LMTBUF x	74100 LMDETC x	7425 LMDETC x
F11	E11	D11	C11	B11	A11
DM8838 QUBINT x	74S08 LMRCLL xxxx	DUMMY LMMYNN x	2147 LMTBUF x	74S00 LMTBFC xxxx	74S288 LMMODU x
F10	E10	D10	C10	B10	A10

PDP-11 Unibus Chaosnet Interface CHAOS;UBCHNI UML 17-DEC-80 1801
 ***** DIP MAP *****

DM8837A QUBXCV x	DUMMY QADADR x	74 279 LMRCTL OXOX	9401 LMTBUF x	74S04 LMDETC xxxxxx	74S112 LMMODU xx
F09	E09	D09	C09	B09	A09
DM8837A QUBXCV x	74S74 QADADR xx	74S74 LMRCTL xx	74S51 LMTBUF xx	74S02 LMTBFC xxxx	74S374 LMMODU x
F08	E08	D08	C08	B08	A08
DM8837A QUBXCV x	PULLUP-D QADADR x	74S00 LMRBUF xxxx	9401 LMRBUF x	74LS164 LMRBUF x	74LS164 LMRBUF x
F07	E07	D07	C07	B07	A07
DM8837A QUBXCV x	74S251 LMMYNM x	26LS193 LMRBUF x	74S74 LMRCLK xx	74LS161 LMRCLK x	74S112 LMTCLK xx
F06	E06	D06	C06	B06	A06
74S251 LMMYNM x	74S51 LMRBUF xx	26LS193 LMRBUF x	74S37 LMRBUF xxxx	74LS161 LMRCLK x	EXAR-CL LMTCLK x
F05	E05	D05	C05	B05	A05
74LS161 LMMYNM x	74S00 LMUCON xxxx	26LS193 LMRBUF x	2147 LMRBUF x	TD100 LMDLTC x	26S02 LMRCTL xx
F04	E04	D04	C04	B04	A04
74LS161 LMMYNM x	74S00 LMRCTL xxxx	74S04 LMTCLK xxxxxx	TD250 LMRCLK x	74S163 LMTCLK x	DUMMY LMLNDR x
F03	E03	D03	C03	B03	A03
74LS161 LMMYNM x	74S158 LMLNDR x	74S10 LMMODU xxx	74S08 LMRBUF xxxx	74S74 LMDETC xx	26LS31 LMLNDR xxxx
F02	E02	D02	C02	B02	A02
74S11 LMMODU xxx	74S174 LMMYNM x	74S287 LMMYNM x	74S74 LMDETC xx	74S04 LMRCLK xxxxxx	26LS33 LMLNDR xxxx
F01	E01	D01	C01	B01	A01

PDP-11 Unibus Channel Interface CHAOS:UBCHNI UML 17-DEC-80 1803
***** EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *****

-J01-

-J02-

-J03-

-J04-

01	01 GND	# 01	01
02	02 INTERFERE+	02	02
03	03 INTERFERE-	# 03	03
04	04 GND	04	04
05	05 RCVR.DATA+	05	05
06	06 RCVR.DATA-	06	06
07	07 GND	# 07	07
08	08 TRANS.DATA+	08	08
09	09 TRANS.DATA-	# 09	09
10	10 GND	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
15	15	15	15
16	16	16	16
17	17	17	17
18	18	18	18
19	19	19	19
20	20	20	20
21	21	21	21
22	22	22	22
23	23	23	23
24	24	24	24
25	25	25	25
26	26 GND	# 26	26
27	27 GND	# 27	27
28	28 GND	# 28	28
29	29 GND	# 29	29
30	30 GND	# 30	30
31	31 GND	# 31	31
32	32 GND	# 32	32
33	33 GND	# 33	33
34	34 GND	# 34	34
35	35 GND	# 35	35
36	36	36	36
37	37	37	37
38	38	38	38
39	39	39	39
40	40	40	40
41	41		
42	42		
43	43		
44	44		
45	45		
46	46		
47	47		
48	48		
49	49		
50	50		

PDP-11 Unibus Chaosnet Interface

CHAOS:UBCHNI UML

17-DEC-80 1803

***** EDGE CONNECTIONS Flags: (# Output, @ Terminator, ---- Dedicated ground, ++++ Dedicated power) *****

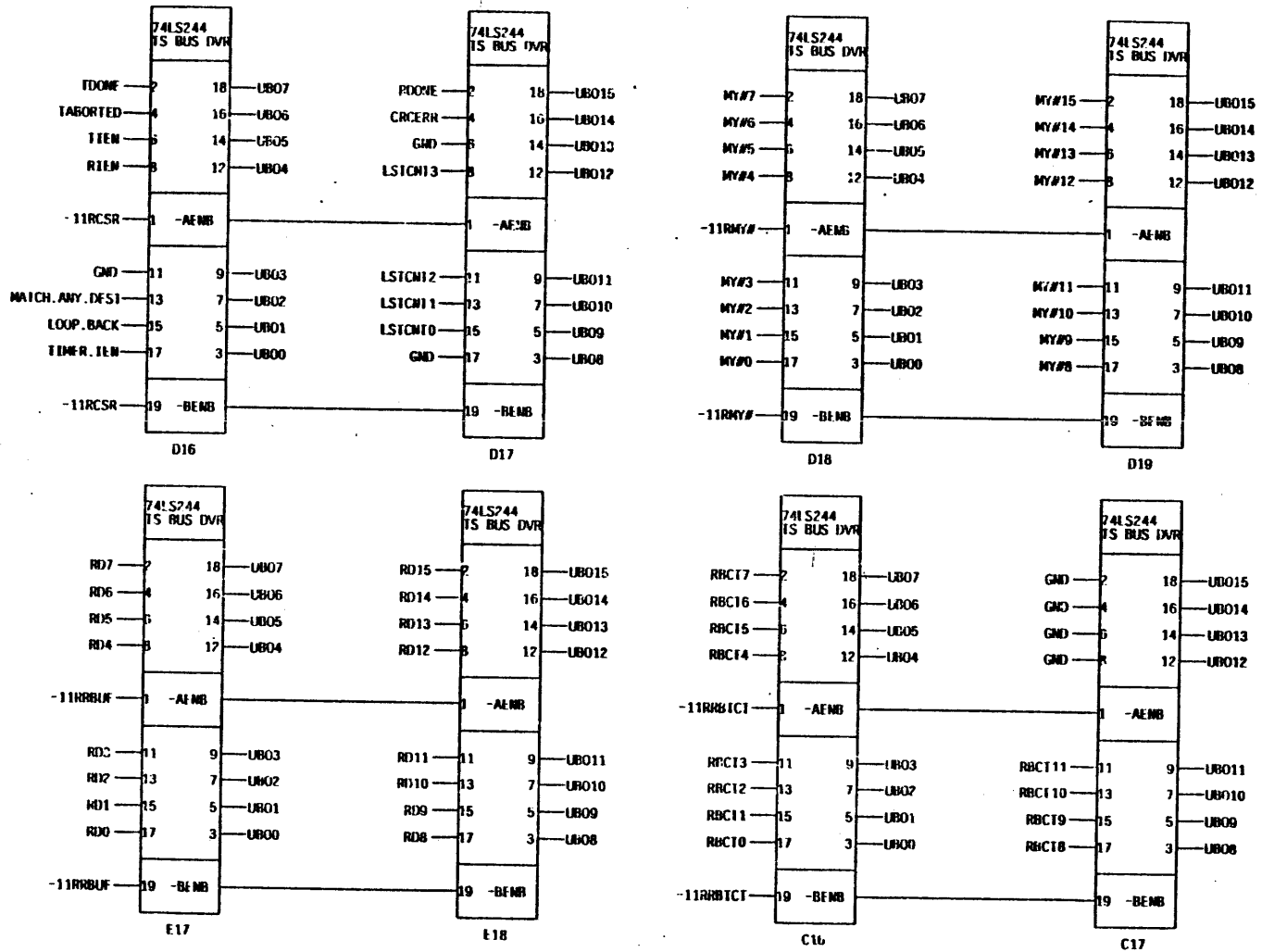
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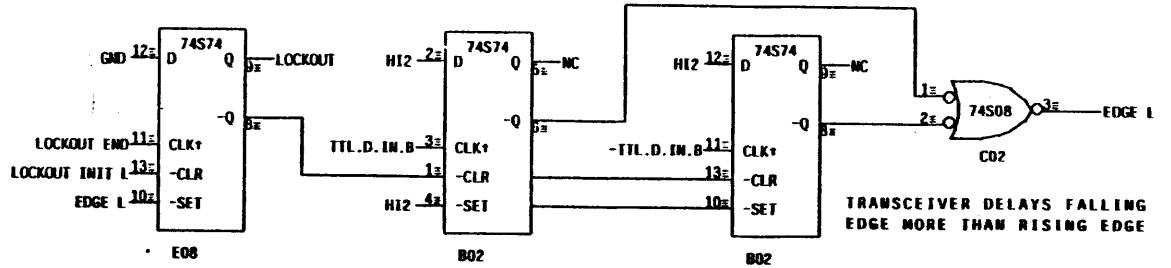
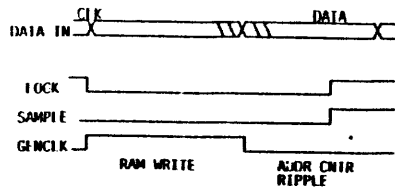
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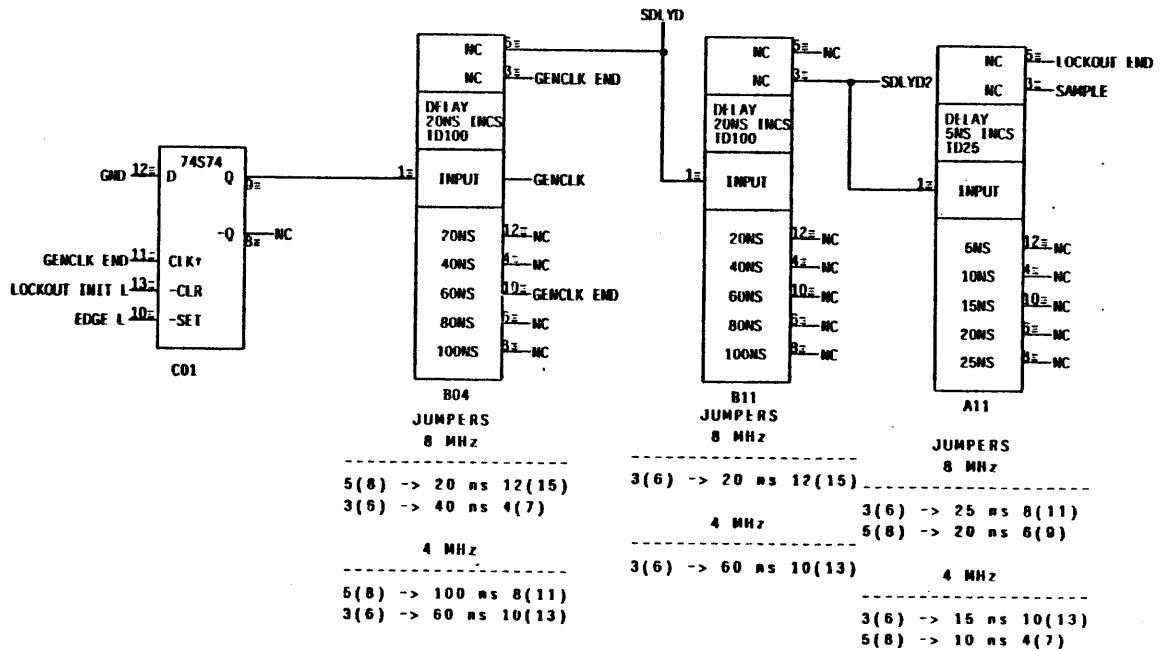
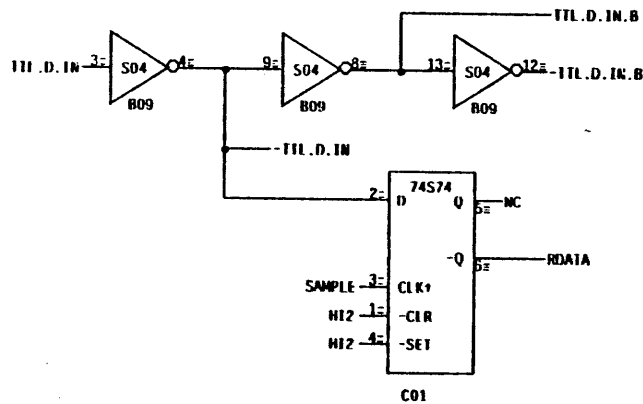
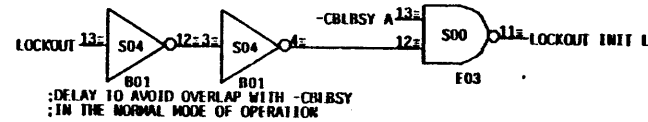
-J08-

01	01	01	01
02	02	02	02
03	03	03	03
04	04	04	04
05	05	05	05
06	06	06	06
07	07	07	07
08	08	08	08
09	09	09	09
10	10	10	10
11	11	11	11
12	12	12	12
13	13	13	13
14	14	14	14
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36	36	36	36
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38	38	38	38
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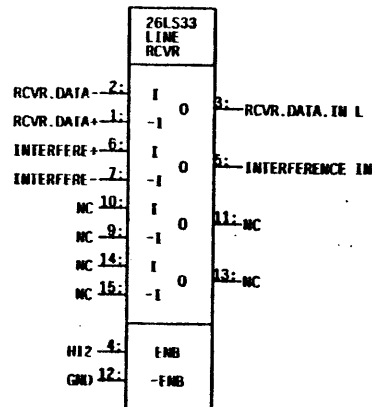




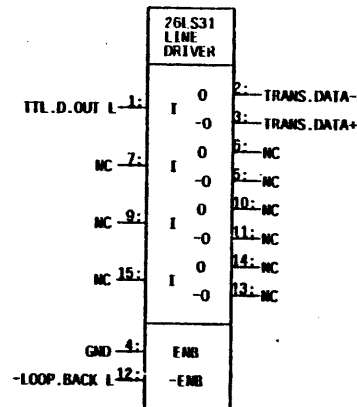
SAMPLE should be timed to occur in the middle of the data part of the cycle. Normally, this will be .75 of the cycle time less 15-25 ns. LOCKOUT END should be 5 ns earlier.



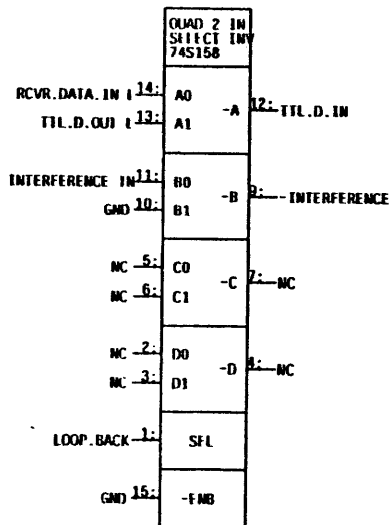
:26LS32



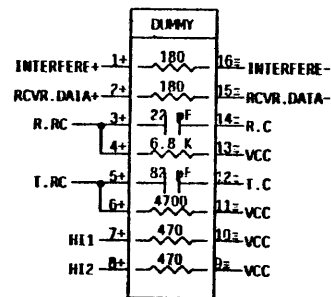
A01



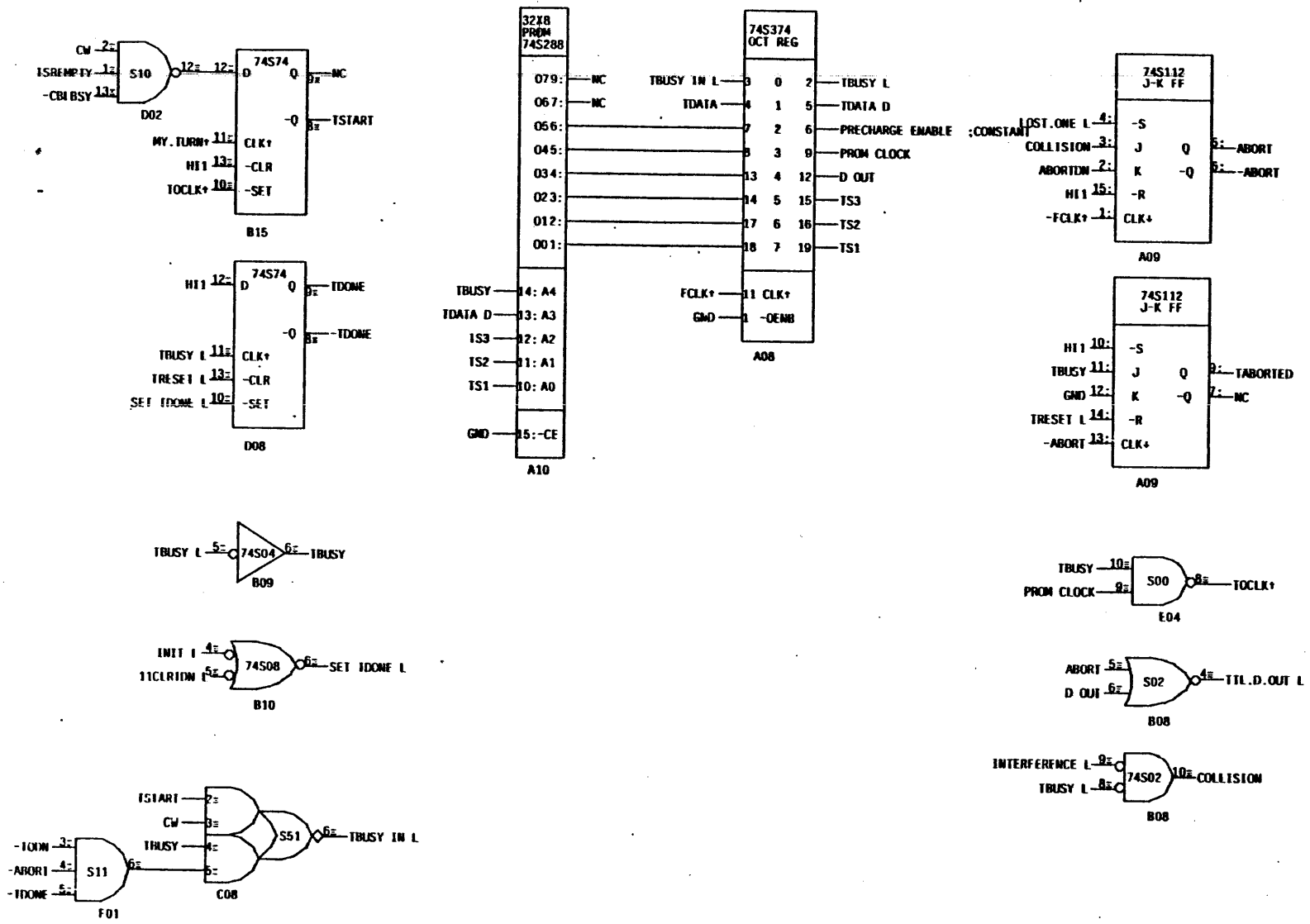
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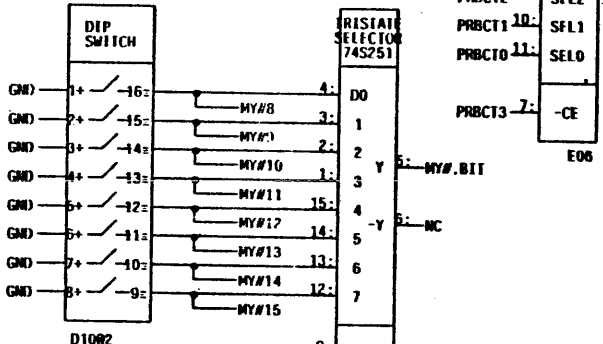
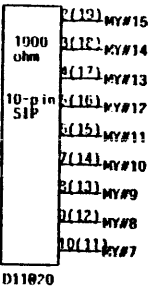
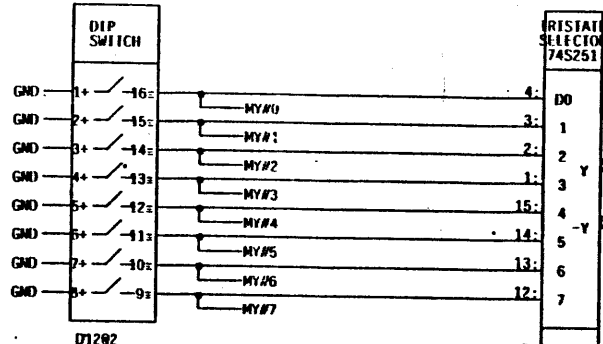
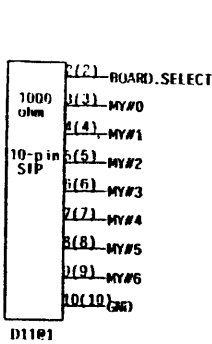


E02

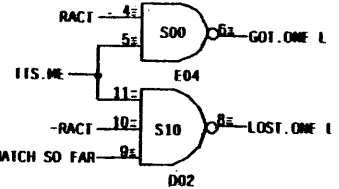
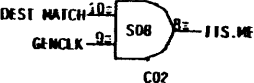
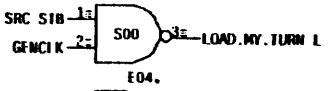
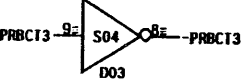
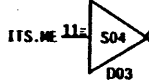
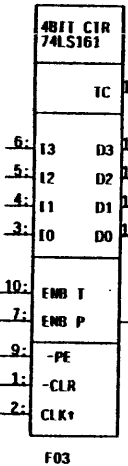
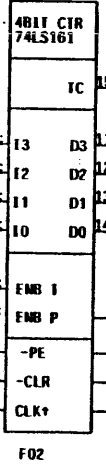
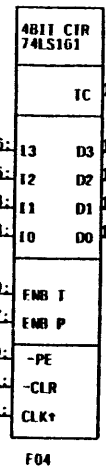
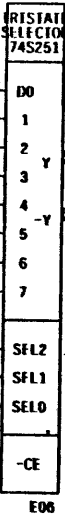
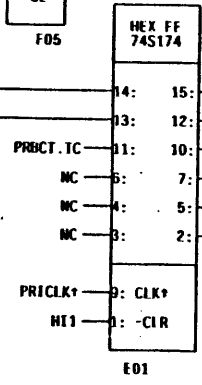
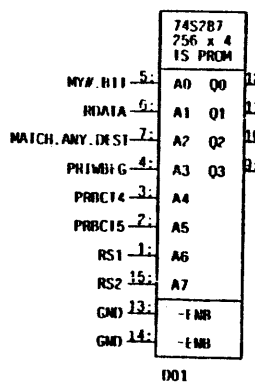


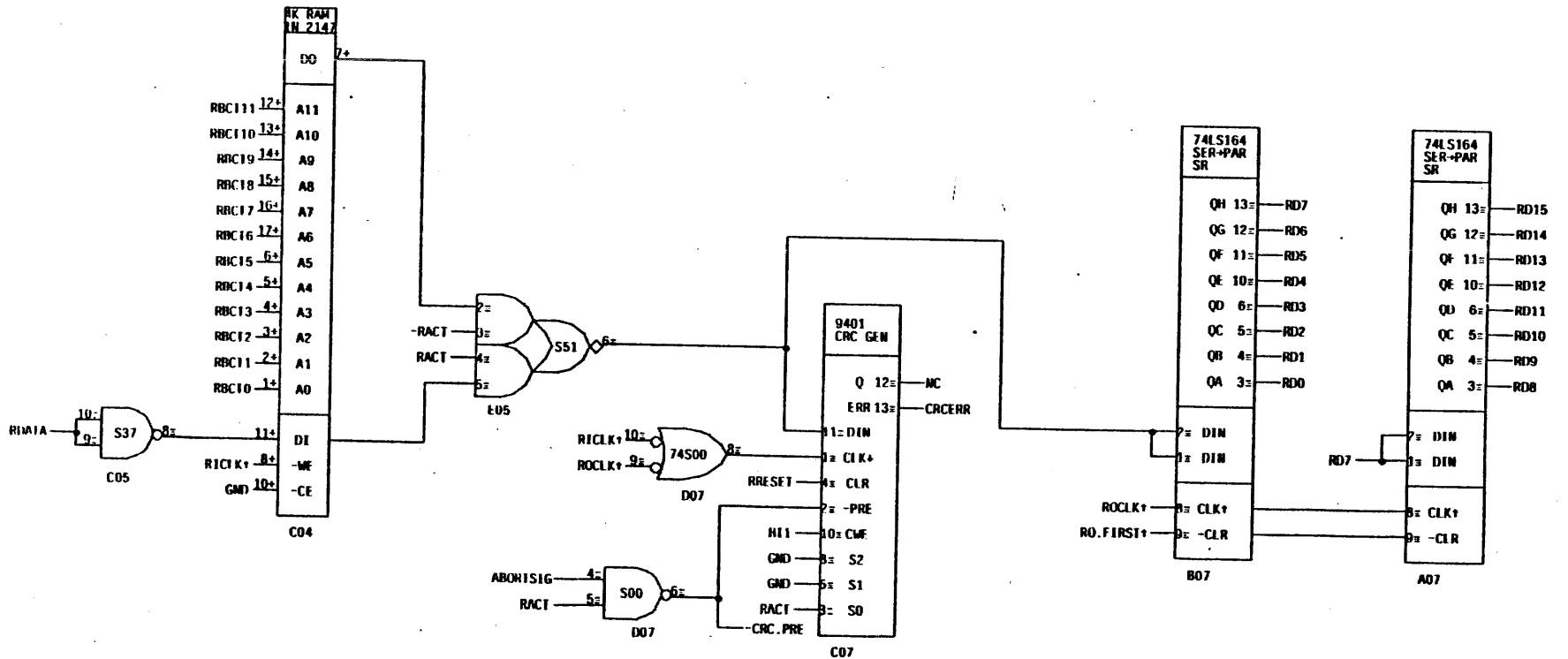
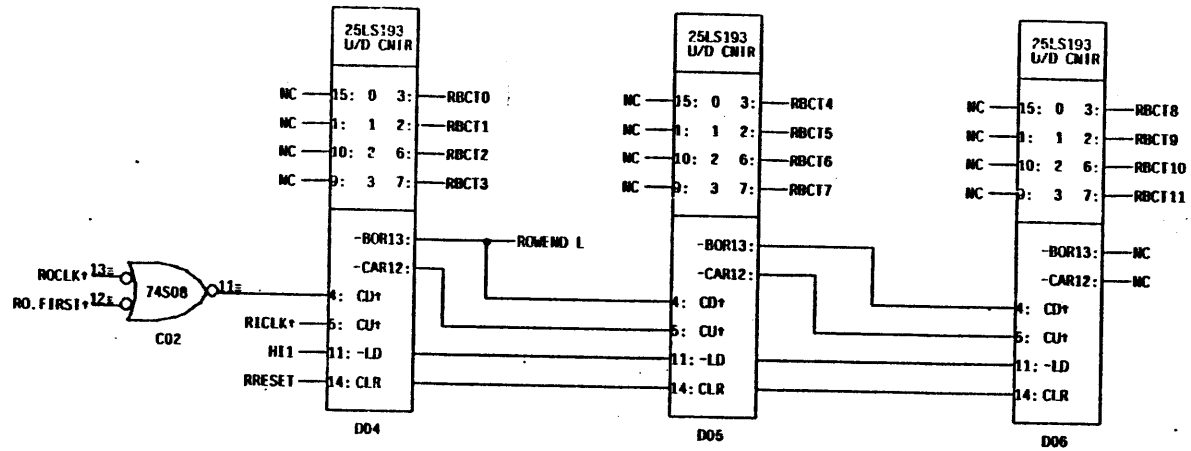
A0302

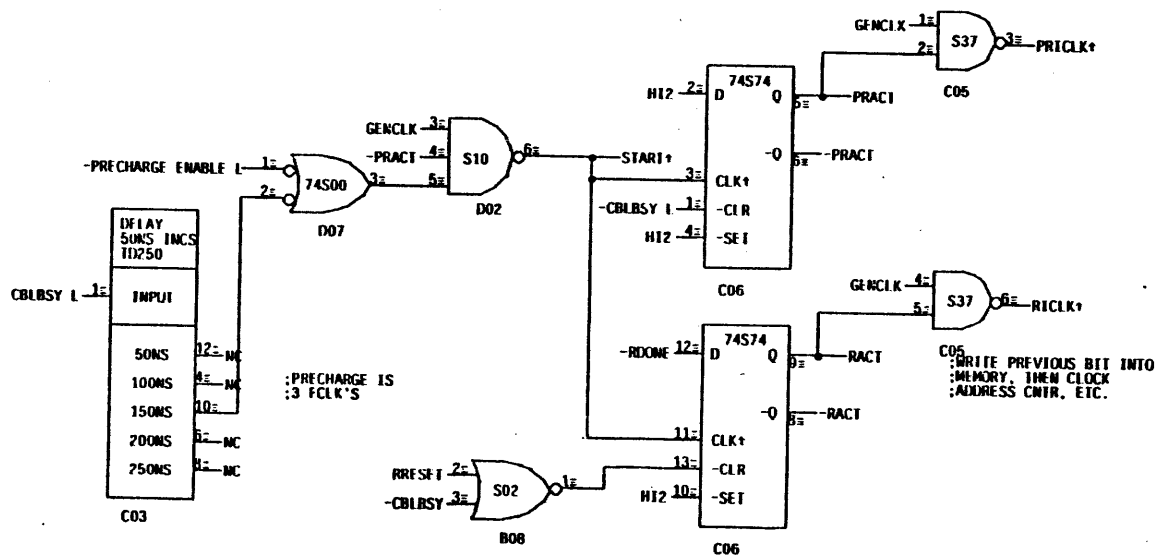
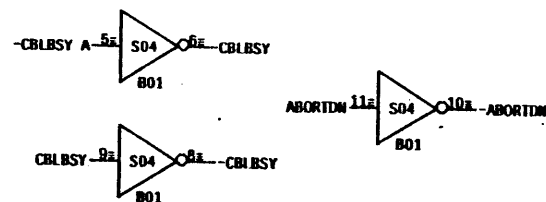
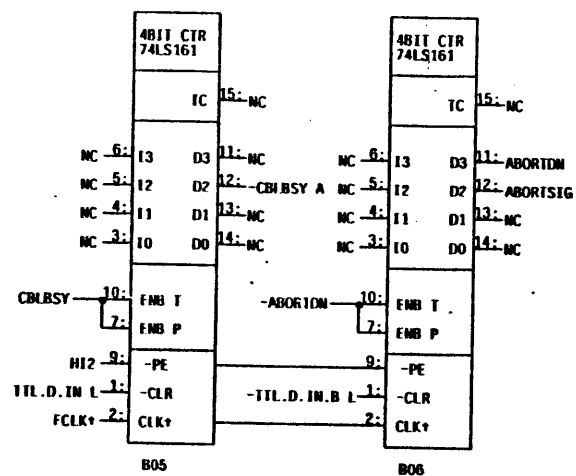


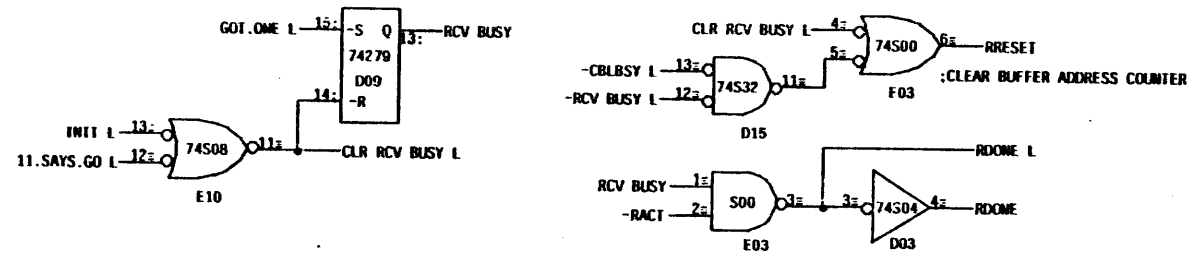
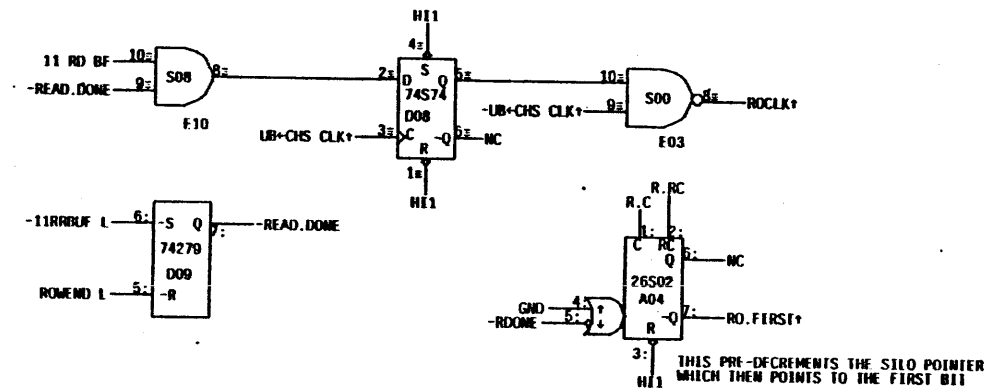


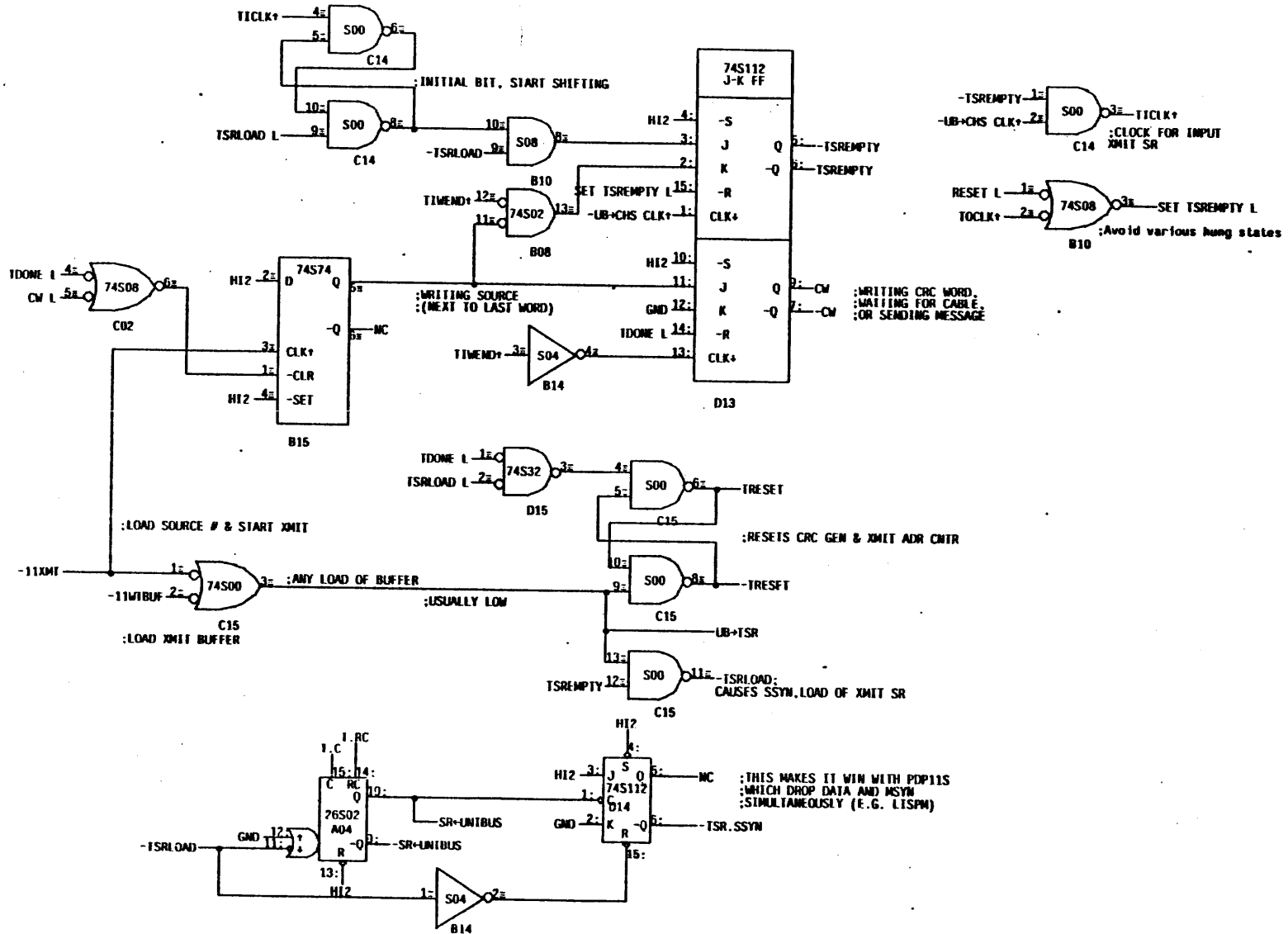
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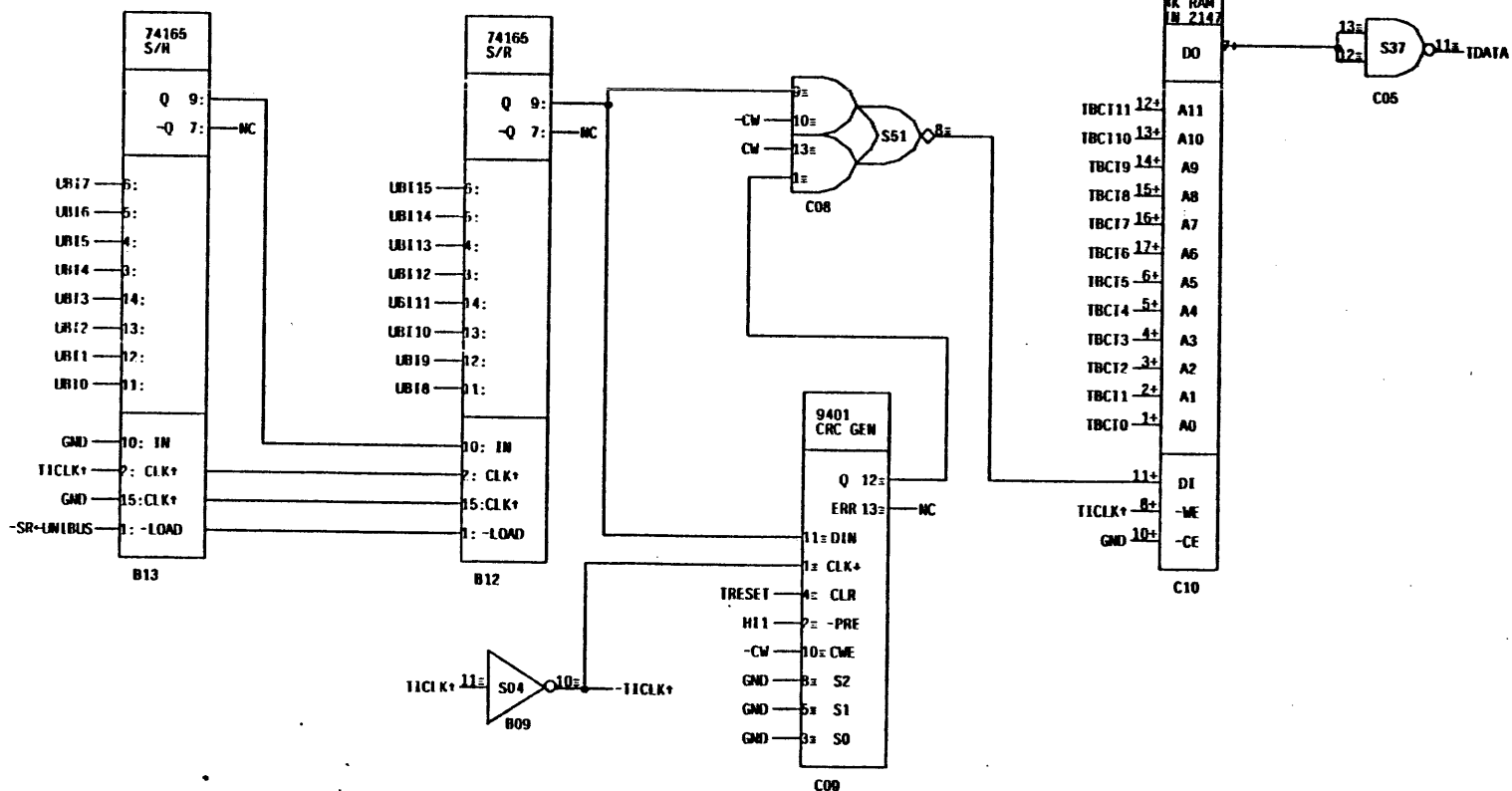
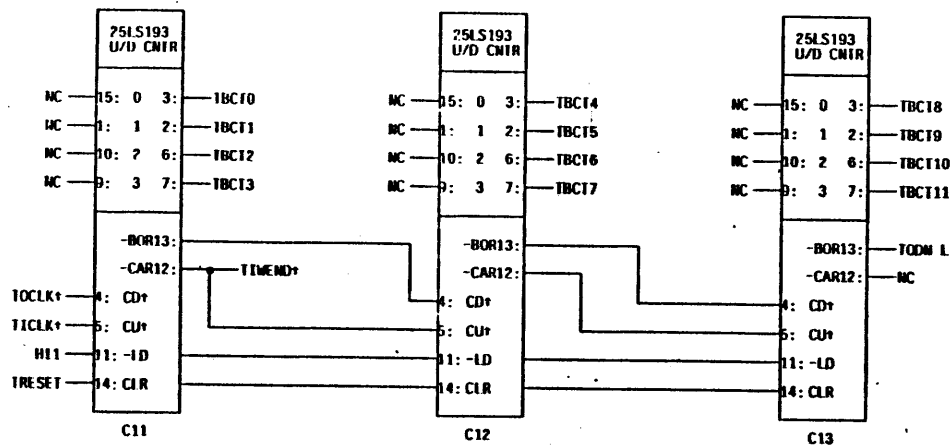


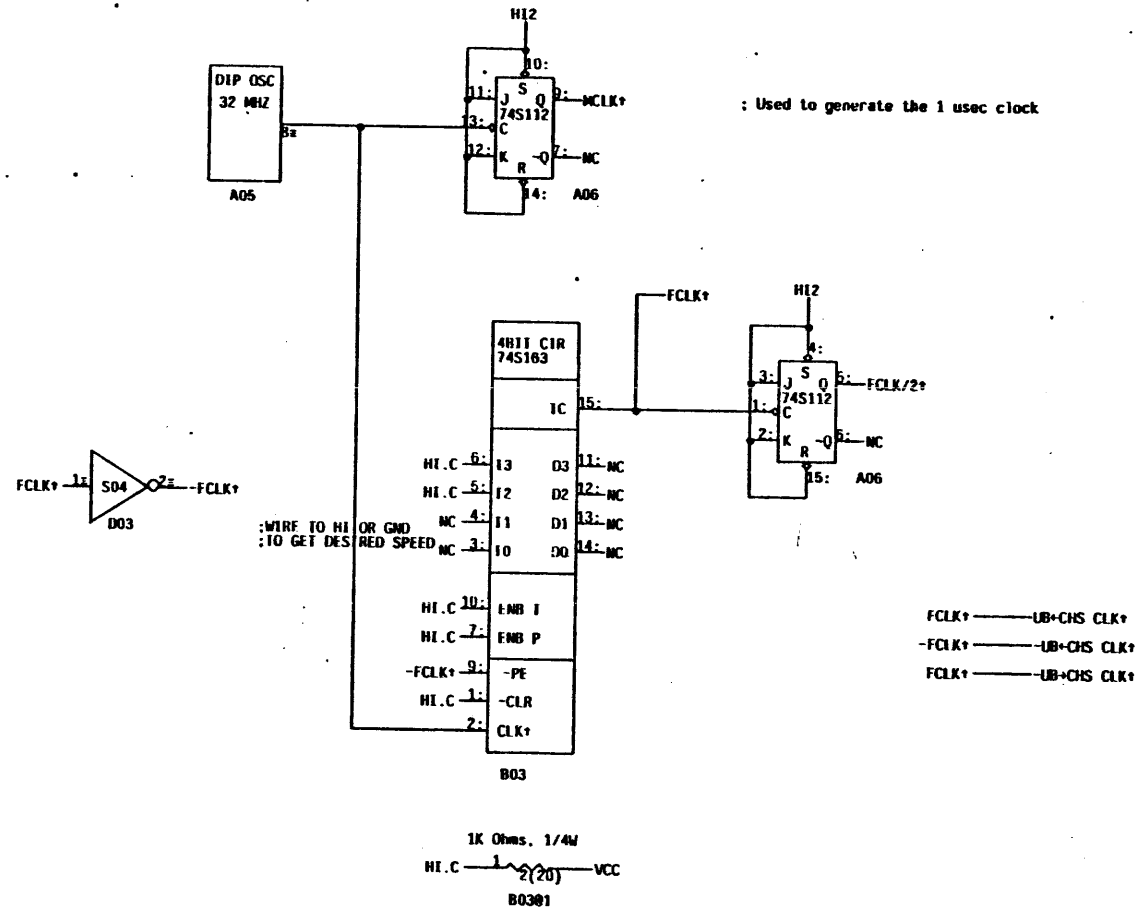




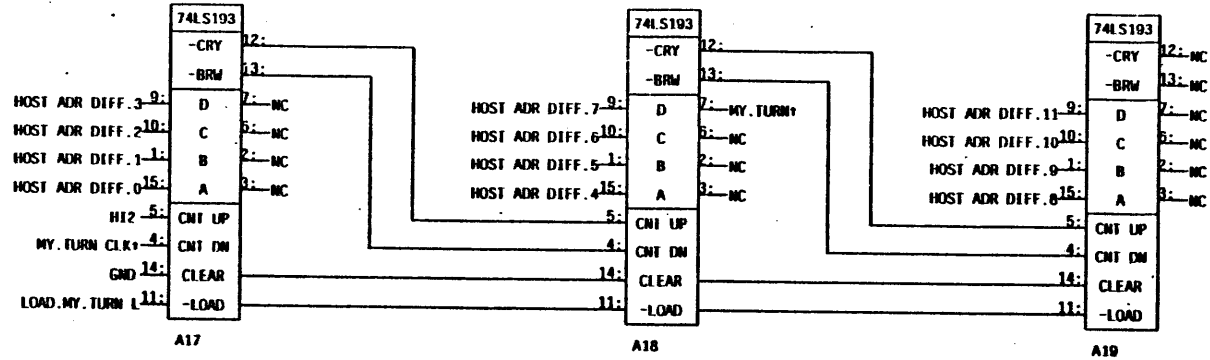




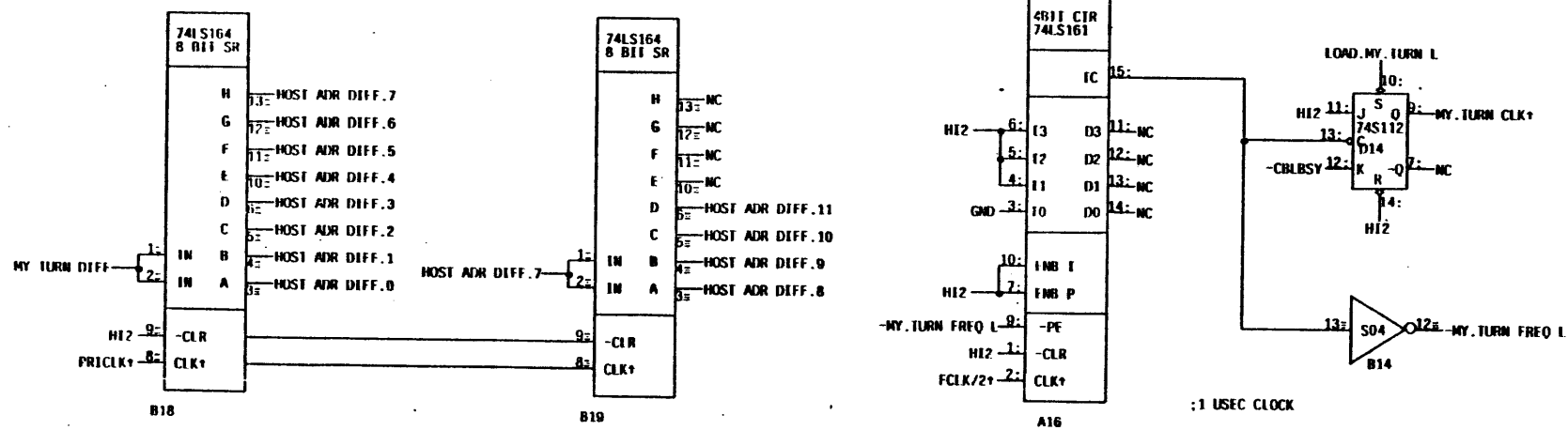




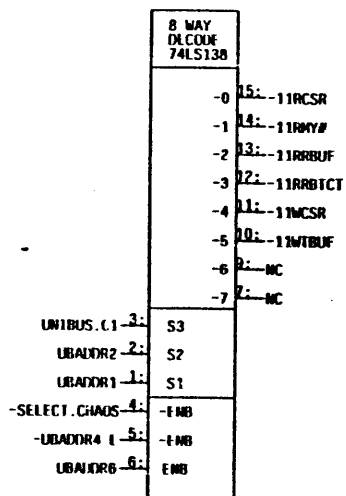
"My Turn" Counter



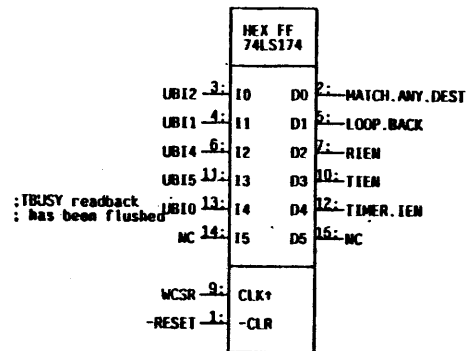
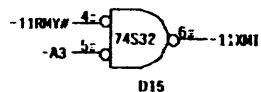
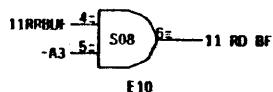
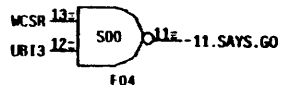
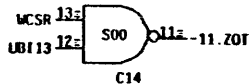
:DEFAULT IS MYTURN.MOD 2+7 OR 64 USECS



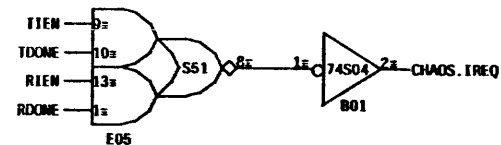
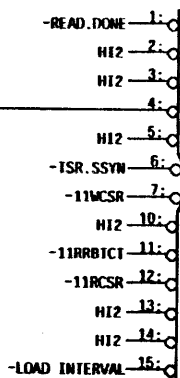
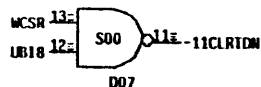
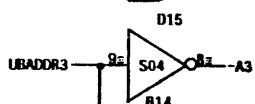
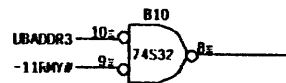
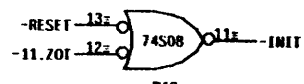
:1 USEC CLOCK

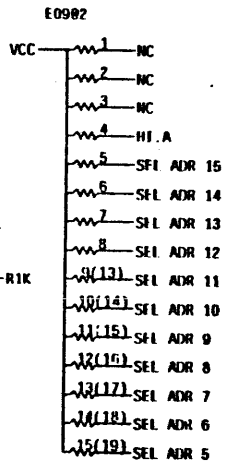
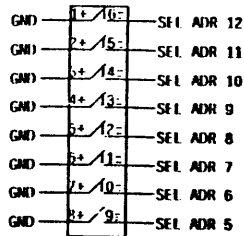


C18



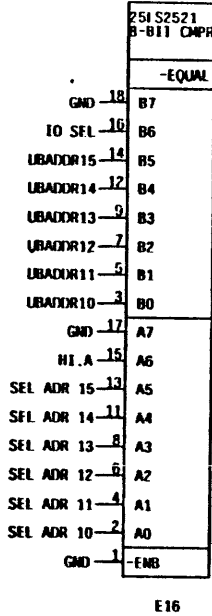
:TRISY readback
: has been flushed



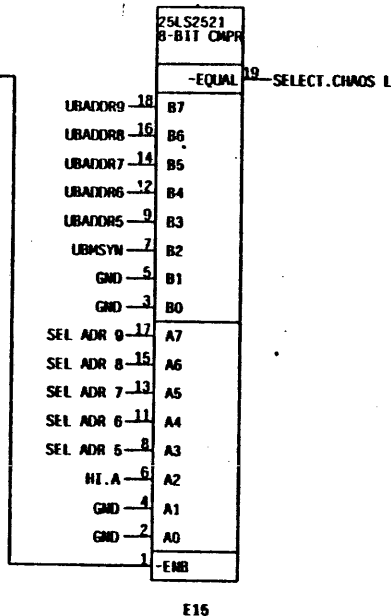


898-1-R1K

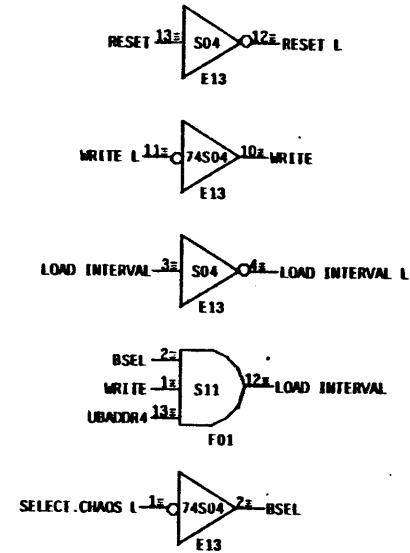
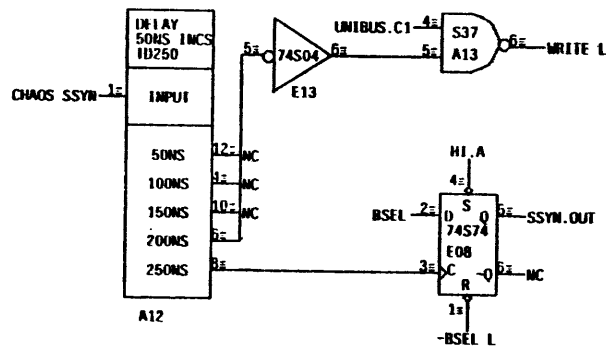
E0701



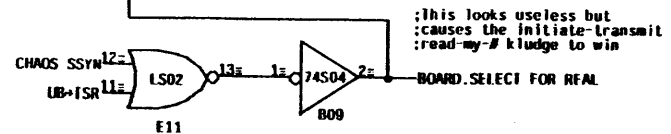
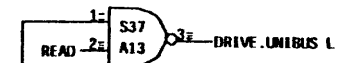
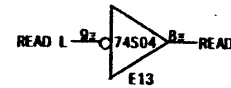
E16

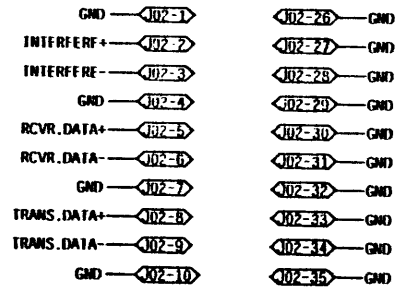


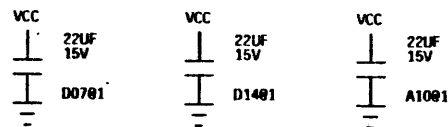
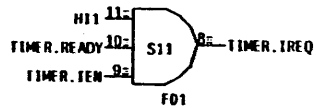
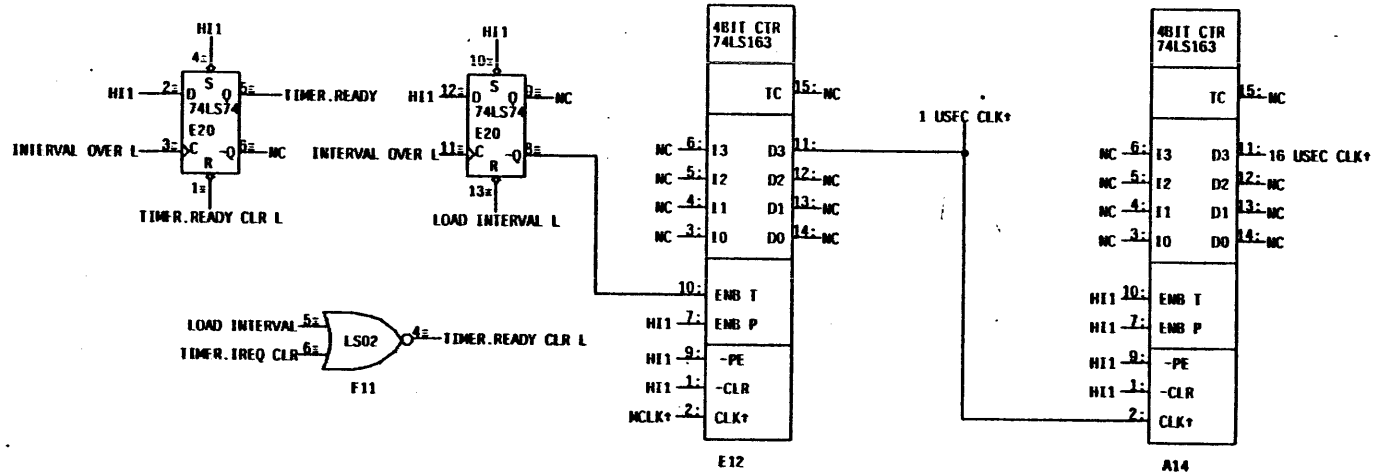
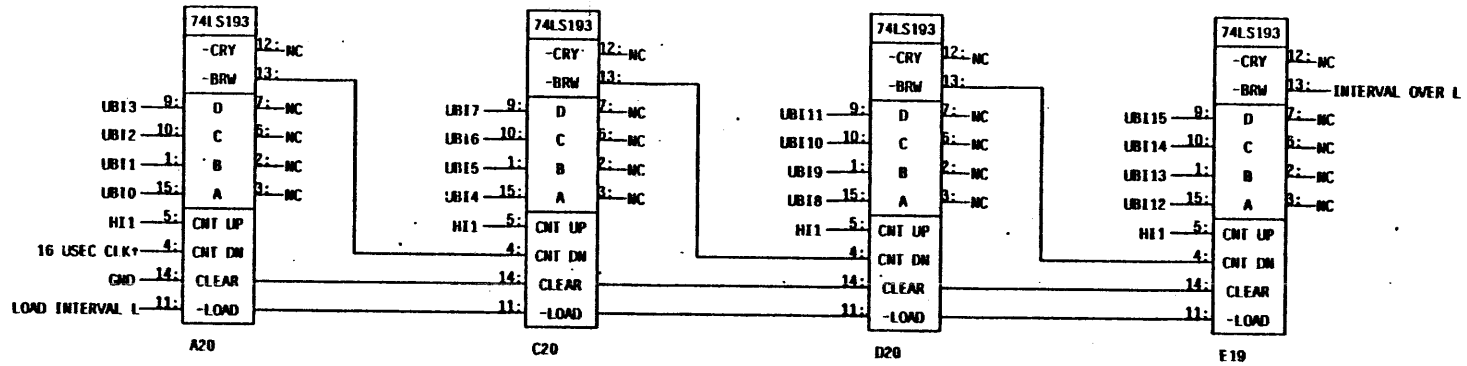
E15



UNIBUS.C1 READ







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 <A11> — B001°

<A11> — MPG. IN°
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 <B2> — BG5. IN°
 <B2> — BG5. OUT°
 <S2> — BG4. IN°
 <B2> — BG4. OUT°
 <D11> — BBSY°
 <A11> — NPR°
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 <D12> — SACK°

