Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

SUBJECT: DESCRIPTION OF MEMORY TEST SETUP VI

To: N. H. Taylor

From: E. A. Guditz

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Approved: W. N. Papian

Abstract: Memory Test Setup VI is an assembly of Burroughs' test equipment designed to simulate computer operation of magnetic-core memories. It makes possible the dynamic testing and evaluation of both single memory planes and completed memories of sizes up to 64x64 registers and word lengths of approximately 20 digits.

Drawing SD 47148 is a block diagram of Memory Test Setup VI. It has letter and number coordinates on the left and upper edges respectively. These facilitate locating the numbered blocks. The drawing consists of ten basic parts: pulse generation and distribution logic, the address counter, cycle timing circuit, buffer storage, display circuit, alarm circuit, address skip circuit, pattern generating circuit, pattern checking circuit, and automatic rewriting circuit.

## PULSE GENERATION AND DISTRIBUTION LOGIC

The pulse generation and distribution elements are located in the area B-1 of the block diagram. They consist of multivibrator pulse generator 1, channel selectors 2 and 3, gate and delay unit 5, low frequency multivibrator 4 and switch S1. Unless otherwise indicated, these logical blocks are standard Burroughs or Whirlwind equipment.

The operation of the pulse generating and distribution system is as follows: Multivibrator pulse generator 1 puts out continuous 0.1 μ sec pulses at a 30 KC rate. These pulses are sent into channel selectors 2 and 3 from which they are distributed to the rest of the system. Gate and delay unit 5 delays one of these pulses to provide a delayed scope sync pulse. Low frequency multivibrator 4 provides pulses to the system at a much slower rate than those which come from multivibrator 1. These pulses, however, go only to the X address counter. Switch S1 provides a selection of either high frequency pulses from multivibrator pulse generator 1 or low frequency pulses from low frequency multivibrator 4.



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## THE ADDRESS COUNTER AND MEMORY ADDRESS REGISTER

The address system consists of the address counter which is shown at the extreme right of the diagram, pulse mixer 12 which is located at A-4, delay unit 10 (B-3), delay unit 11 (C-3), delay unit 9 (D-3), channel selector 32 which is located at K-5, and the memory address register (MAR) which is located at E-6 and E-8. The addressing with this system is usually done sequentially. The pulses which index the counter come from multivibrator pulse generator 1 in the pulse generating circuit via channel selector 3, switch S1, gate tube 6 which is normally on, channel selector 13, delay unit 10, delay unit 11, mixer 12 and switch S3. Switch S3 permits the adding of these clock pulses to either the first or second half (X or Y) of the address counter. In normal operation these pulses are added to the first half of the address counter. This address counter is a conventional binary counter consisting of flipflops and gate tubes. Each stage has an extra gate tube which is used for reading out of the counter in parallel.

The sequence of operations in the address system is as follows: First, the MAR is cleared by a pulse from channel selector 13, output 2. Next, a pulse from delay unit 10 is applied to the control grids of the readout gate tubes and the contents of the counter is read out in parallel to the memory address register flipflops. Since some of the pattern generating operations depend on the number held in the counter, the next counting pulse is not added to the counter until after all reading and writing operations are completed in the memory. The pulse, which increases the number in the counter by one, comes from delay unit 11. The timing of this pulse can be quite critical under certain operating conditions. The memory address register selects the coordinate driving line (via the crystal matrix) in memory. There will be times when the contents of the memory address register and the memory address counter differ by a count of one. This will be true at the time just prior to the clearing of the memory address register by a clock pulse from multivibrator pulse generator 1. It should be noted that the memory address counter is added to sequentially until it holds a full count at which time the process is repeated while the memory address register is always restored to the cleared position before each address is selected.

## THE CYCLE TIMING CIRCUIT

The cycle timing circuitry consists of a group of delay units located on the diagram about the point H-4. The function of these units is to deliver pulses at the proper times to generate the memory cycle pattern shown in the attached Timing Chart. As will be seen in the chart, the currents necessary for the proper operation of memory are "read" and "write" currents, an "inhibit" current and a "post-write disturb" current. The units which produce these driving currents are basically gated amplifiers which are excited by the output waveform of flipflops. The actions of these flipflops are controlled by initiating and terminating pulses provided by the delay units in the cycle timing circuit. The first current to be produced in time is the read current. It is important that this read current does not occur before the desired memory core address has been selected. The required delay is effected by delay units 15 and 113. The pulse which enters delay unit 17 initiates the read current in memory; delay unit 22 terminates the read current in memory. It will be noted here, in tracing a clock pulse from multivibrator pulse generator 1 through channel selector 2, mixer 14, delay unit 15, and delay unit 113, that the pulse next goes to gate tube 114. The reason for this gate tube will be explained in the section on skip circuitry. Referring to the timing chart, it will be seen that the inhibit current, when required, is turned on slightly before the write current. It will also be seen that the inhibit current remains on slightly longer than the write current. It is not absolutely necessary that this condition prevail; it is done here merely for the sake of safety.

The next pulse in the cycle, for initiating the inhibit current should it be desired, is generated at the output of delay unit 16. This delay unit determines the time which will exist between the end of the read current pulse in memory and the beginning of the inhibit pulse. The basic waveform which ultimately becomes an inhibit pulse is generated differently from that for the read and write pulses, by a single-shot multivibrator in a standard Burroughs gate and delay unit (25). The termination of the inhibition pulse is determined by the setting of this gate and delay unit.

Delay unit 19 determines the length of time which shall occur between the beginning of the inhibit pulse and the beginning of the write pulse. The input to delay unit 18 is the pulse which initiates the write current and the output of delay unit 23 terminates the write current. The setting of these two delays (18 and 23) determine the length of the write pulse.

Under certain conditions it is desirable to include in the memory cycle a post-write disturb pulse. Delay unit 24 determines how long after the completion of an inhibit pulse the post-write disturb pulse shall occur. The length of the post-write disturb pulse in this set-up is automatically the same as the length of an inhibit pulse because it is the same unit which produces both.

As shown in the cycle timing chart, when we have produced this series of current pulses at the prescribed lengths, we have used up less

than half of the 33 microseconds existing between clock pulses. For simple modes of operation, the remaining time in this interval is simply a wait period during which no actual work is performed in memory. However, more complicated modes of operation call for the use of a double read-write cycle. To produce the intermediate clock pulse for this double read-write cycle, delay unit 21 is used. Switch SØ, when placed in the up position, causes this to happen along with several other things. Switch SØ is located at K-3 on the block diagram. It is the left-most pole on this switch which causes the output of delay unit 21 to be fed back into mixer 14 thereby repeating the sequence of events of the first read-write cycle. This is explained more fully in the section on the "Complemented Mode of Operation."

There is one other pulse which is important to the read-write cycle; this is the strobe pulse which must occur during the read operation at a time determined by delay units 41 and 37.

## BUFFER STORAGE

The buffer storage circuit is located at H-1 on the block diagram. It consists of flipflop 26, switch $S_4$, gate tube 20 and flipflop 27 with its input gate tubes.

Reading out of the memory destroys the information it contains. Should we desire to retain the information indefinitely, it must be temporarily stored somewhere in order that we may read it back into memory again. To do this, the output of the sensing amplifier is fed indirectly into the buffer storage flipflop 26. This flipflop controls gate tube 20 which in turn controls the pulse which excites the digit-plane driver.

Buffer storage flipflop 26 is initially cleared by a clock pulse from delay unit 28 via mixer 29. A ONE output from memory results in a pulse out of the sensing amplifier which sets flipflop 26 to a ONE position. Gate tube 20 remains off and prevents the occurrence of an inhibit pulse. This is as it should be since an inhibit pulse is not needed in order to write a ONE into memory. A ZERO out of memory results in no pulse from the sensing amplifier and flipflop 26 remains in the ZERO position. In this case gate tube 20 is on and a pulse gets through to excite the digit-plane driver and produce an inhibit current pulse in memory. The type of operation just described is referred to as the static mode of operation because the same bit of information which is read out of a core at a given address in memory is put back into that same core.

In contrast to the static mode of operation, a cyclic mode is possible. This involves the use of flipflop 27 and its input gate tube. It will be noted that switch $S_4$ permits gate tube 20 to be tied to either the ZERO side of flipflop 26 or flipflop 27. For the static mode of operation, gate tube 20 is connected to flipflop 26. For the cyclic mode of operation, gate tube 20 is connected to flipflop 27. Operation in the cyclic mode is as follows: A clock pulse is applied to the control grid of the input gate tube of flipflop 27. This reads the information contained in flipflop 26 into flipflop 27. Next a pulse from delay unit 28 via mixer 29 clears flipflop 26. Flipflop 26 is now ready to receive information from the next readout operation. Assume that a ONE is read out during the next read operation and sets flipflop 26 to the ONE position. When the write operation occurs for this read-write cycle it will be noted that what gets read back into memory is the information contained in flipflop 27, to which gate tube 20 is attached. This means that it is the information from the previous read-write cycle which gets read back into memory. With sequential addressing, the information from the preceeding core in the sequence gets read into the currently addressed core. The result of this kind of operation is to cause the information to precess through the memory. This is clearly seen when a displayed pattern consists of all ZEROs except for a single core which contains a ONE. Push button pulse generator 31 and switch $S_5$ are used to insert a single ONE into a field of ZEROs for this mode of operation.

## DISPLAY INTENSIFICATION CIRCUIT

The display circuit is located on the drawing at L-1. It consists of the display scope intensification flipflop 33, gate and delay unit 34, flipflop 35 and gate tube 36.

The operation of the display intensification circuit is as follows: The readout of a ONE from memory results in a pulse which sets flipflop 33 into the ONE position, at the same time triggering gate and delay unit 34. This pulse comes through gate tube 36 which is normally on. The output of gate and delay unit 34 sets flipflop 33 back to the ZERO position. The ZERO side output plate voltage of flipflop 33 is applied to the cathode of the display oscilloscope where it performs Z-axis modulation. The result of reading a ONE out of memory is to intensify the spot on the display scope which corresponds to the selected core address.

Flipflop 35 and gate tube 36 are used for the special case of the complemented pairs-checkerboard pattern. As mentioned in the section on cycle timing there is a double readout during this mode of operation. Since every readout affects the intensification circuit, we must provide for gating off the second readout pulse. Gate tube 36 does this. The operation is as follows: Flipflop 35 is initially set in the ZERO position by a pulse from channel selector 2, output 2. This leaves gate tube 36 on during the first read operation. When a double read-write cycle is ordered, a pulse from delay unit 21 via switch SØ (position ONE) sets flipflop 35 into the ONE position thereby turning off gate tube 36. By this action, we cause the pairs-checkerboard pattern to be displayed only as a result of the first readout pulse. If this were not done the displayed pattern would be getting complemented continually and would be unintelligible.

## THE SKIP CIRCUIT

The skip circuit is located on the drawing at C-4. It consists of gate tubes 116, 117, 118, 119, 120 and 121; buffer amplifier 122, flip-flop 115 and gate tube 114.

It is often desirable to know if the operating margins of a memory plane would be significantly improved if the core causing the failure could be disregarded. The skip circuit permits taking four sets of failure points. Gate tubes 116, 117 and 118 are associated with X addresses. Gate tubes 119, 120 and 121 are associated with Y addresses. The output of delay unit 15 in the cycle timing group is applied to the input of the X skip gate tubes. The outputs of each of the three X skip gate tubes are applied to one of the Y skip gate tubes. The three outputs of these being fed into buffer amplifier 122. The output of buffer amplifier 122 is fed into the ZERO input of flipflop 115. Gate tube 114 normally passes the pulse which ultimately initiates the read-write cycle. The nature of the skipping action is to cause this read-write cycle to be omitted at a particular address or addresses.

The skip circuit is used in the following manner: Should it be desirable to skip an address in memory, the suppressor lead from gate tube 116 is applied to the control grid of the 5998 driving tube for that X address. Likewise, the suppressor lead for gate tube 119 is applied to the control grid of the 5998 driving tube for the Y-address. When an output occurs from delay unit 15, the pulse will get through gate tube 116 and will also get through gate tube 119. It will pass through buffer amplifier 122 and set flipflop 115 into the ZERO position thereby turning off gate tube 114. This will prevent the occurrence of a read-write cycle at that address. After the read-write cycle is over and it is time to add 1 to the address counter, the same pulse from delay unit 11 sets flipflop 115 back into the ONE position turning on gate tube 114. Under these conditions another set of operation of failure points may be recorded. This action can be extended to include skipping a total of three addresses in memory.

## ALARM CIRCUIT

The alarm circuit is located at Q-1. It consists of alarm flipflop 89, alarm pulse gate tube 87, switch S9, gate and delay unit 111 and alarm panel 86.

A pulse which occurs at the end of the write operation and comes from delay unit 23 is applied to the control grid of alarm gate tube 87. This gate tube will be on upon the occurrence of an error in memory. When switch S9 is closed, this alarm pulse triggers gate and delay unit 111 which in turn triggers alarm panel 86, causing a lamp to light and a bell to ring.

## PATTERN GENERATING CIRCUIT

Pairs-Checkerboard Generator

This circuit is located on the drawing at R-3. It consists of the pattern generating flipflop 84, gate tube 110, and gate tubes 82 and 83 in conjunction with the $2^0$ flipflop of the X and Y address counters. These are flipflops 43 and 49 respectively.

The action of the pairs-checkerboard pattern generator is as follows: Consider the memory addressed to core 0,0. Flipflops 43 and 49 are set in the ZERO position. Gate tube 82 is off and gate tube 83 is on. Assume flipflop 84 would be in the ZERO position. The system controls are set up to force the pairs-checkerboard pattern into memory. This means that the digit-plane driver is under control of gate tube 110 which in turn is controlled by flipflop 84. The control is such that when flipflop 84 holds a ZERO, a ZERO is ordered written into memory and when flipflop 84 holds a ONE, a ONE is ordered written into memory. For the selected address (0,0) a ZERO will be written into memory. Upon the occurrence of the next clock pulse, gate tube 82 being on, flipflop 84 is complemented by that clock pulse. Flipflop 43 is now in the ONE position which turns off gate tube 82. We now address to core 1,0. Flipflop 84 is in the ONE position, therefore, a ONE will be written into core 1,0. When the next clock pulse comes along it finds gate tube 82 off. Flipflop 84 remains in the ONE position. The address counter is added to, however, and we find we have addressed to core 2,0. Since flipflop 84 is in the ONE position we again write a ONE and flipflop 43 is back into the ZERO position thereby turning on gate tube 82 again. The next clock pulse finds gate tube 82 on and complements flipflop 84 back to the ZERO position. We are now addressed to core 3,0. Flipflop 84 contains a ZERO so we write a ZERO into core 3,0. The next clock pulse comes along and finds gate tube 82 off again. It addressed the counter to core 4,0, however, since flipflop 84 still contains a ZERO we write a ZERO into core 4,0. This action produces the familiar 011001100, etc. grouping of the pairs-checkerboard pattern.

When we reach the end of the Y0 line, we are addressed to core 63,0. Flipflop 84 is in the ZERO position and we have written a ZERO into core 63,0. The flipflops in the X counter are all in the ONE position. The next clock pulse to come along will restore the X flipflops to the ZERO position at the same time producing an end-carry pulse which will add ONE to the Y counter. This will cause us to be addressed to core 0,1. In order to continue generating the pairs-checkerboard pattern, we must write a ONE in core 0,1. Flipflop 84, however, was in the ZERO position prior to advancing from core 63,0 to core 0,1. Since flipflop 43 of the X counter was in the ONE position at that time, gate tube 82 was off and the clock pulse which caused us to change address did not get through to complement flipflop 84. Since we want to write a ONE in core 0,1, we must have some means for complementing flipflop 84 at this time. For this, we use the end-carry pulse from the X counter via channel selector 79 (output 2). This pulse is fed into gate tube 83 which at that time is on since flipflop 49 contains a ZERO. As we scan across the line Y1, the pattern generating action is exactly the same as it was for line Y0.

When we get to the end of line Y1 (core 63,1), we find flipflop 84 in the ONE position and we have written a ONE in core 63,1. The flipflop of the X counter once again contains all ONEs; also flipflop 49 of the Y counter contains a ONE since we are addressed to line Y1. The next clock pulse to come along will address us to core 0,2. Since flipflop 49 is on a ONE, and gate tube 83 is off, the X end-carry will not get through to complement flipflop 84 and flipflop 84 will remain in the ONE position thereby writing a ONE in core 0,2. The pattern generating action for line Y2 is exactly the same as the line Y1. At the end of line Y2 when we are changing address from core 63,2 to 0,3, we find flipflop 49 in the ZERO position with gate tube 83 on and in this case the X end-carry pulse gets through to complement flipflop 84 and we write a ZERO in core 0,2. Thus, it can be seen that the familiar 011001100, etc., pattern is being produced along the Y coordinate also. This action progresses automatically until we have scanned a complete frame and are addressed to core 63,63. We are now ready to address core 0,0 again. When we are addressed to core 63,63, flipflop 84 is in the ZERO position and we have just written a ZERO in core 63,63, the next clock pulse will select address 0,0. Since flipflop 43 was in the ONE position, gate tube 82 was off; also gate tube 83 was off because flipflop 49 was also in the ONE position. Thus no pulse gets through to complement flipflop 84. So, we are in a position to start rastering through the memory again exactly as before.

The pattern just described is what is known as a pairs-checkerboard with ZEROs in the corners. This resulted from the assumption that flipflop 84 was in the ZERO position at the start of pattern generation. Had it been in the ONE position, a pairs-checkerboard pattern with ONEs in the corner would have resulted. Either of these patterns may be selected by pushing the push button on push button pulse generator 31. This inserts a complement pulse into flipflop 84 which accomplishes this selection. Switch S13 must be in the top position for the generation of the pairs-checkerboard pattern.

Quadrant Checkerboard Pattern Generator

The quadrant checkerboard pattern resulted from the design of a new sense winding which runs parallel to the coordinate driving lines instead of diagonal to these wires. This pattern produces the same cancellation of half-select signals for the new parallel sense winding as the pairs-checkerboard pattern does for the old diagonal sense winding.

To generate the quadrant checkerboard pattern, switch S13 must be in the bottom position. As in the case for generating the pairs-checkerboard pattern, when flipflop 84 is in the ZERO position, a ZERO will be written into memory and when flipflop 84 is in the ONE position, a ONE will be written into memory. Gate tube 110, being controlled by flipflop 84, determines the excitation to the digit-plane driver. Pattern generation is as follows: Consider the memory addressed to core 0,0. Assume flipflop 84 to be in the ZERO position. Since switch S13 is in the bottom position, the pulses which will complement flipflop 84 will come from counter gate tube 59 and counter gate tube 65 of the X and Y address counters respectively. These gate tubes are in the $2^4$ position in each of

these counters. This means that every 32nd counting pulse will be available to complement flipflop 84. Since we have started to write ZEROs along line Y0, we will continue to write ZEROs until we have addressed to wure 31,0 and completed operation on that core. In changing address from core 31,0 to core 32,0, a pulse will come out of gate tube 59 and complement flipflop 84. From core 32,0 to 63,0 inclusively, ONEs will be written. At the time of the X end-carry pulse, flipflop 84 is complemented back to the ZERO position by a pulse from gate tube 59. Action in scanning lines Y1 through Y31 inclusively is exactly the same as that for line Y0. In changing address from line Y31 to line Y32, we have in addition to the X end-carry pulse from gate tube 59 a pulse from gate tube 65 which again complements flipflop 84. Now we start scanning line Y32 with flipflop 84 in the ONE position and write ONEs until we get to address X32 at which time the pulse from gate tube 59 complements flipflop 84 back to the ZERO position and we finish the line by writing ZEROs. This action continues through the remainder of the Y addresses up to and including core 63,63. In addressing from core 63,63 to core 0,0, flipflop 84 is first complemented by the X end-carry pulse from gate tube 59 and then by the Y end-carry pulse from gate tube 65. Thus we again start scanning line Y0 with flipflop 84 in the proper position to write ZEROs again.

This action results in the generation of a pattern in which quadrants 1 and 3 hold ZEROs and quadrants 2 and 4 hold ONEs. Should the complement of this pattern be desired it is only necessary that flipflop 84 be in the ONE position when scanning is begun. This is accomplished by pushing the button on push-button pulse generator 31.

## The Complemented Mode of Operation

This mode of operation resulted from attempts to produce a so-called "worst" pattern. It was found, in the case of the pairs-checkerboard pattern, that the most deleterious effect on the output signal from a selected core occurred when the information read out of that core was the complement of the pairs-checkerboard value for that core (E-488, E. A. Guditz, October 14, 1952). In order to observe the effects of such a condition, it was necessary to design some additional logic. This resulted in what is known as the "double read-write cyle." The memory operation for this mode of operation is as follows: A core is selected and the information readout into the buffer storage flipflop. A pulse from the system complements the buffer storage flipflop prior to the write operation. Thus the complement of the information read out is rewritten. While still addressed to this core, another read-write cycle takes place. It is during this second readout operation that the core output is evaluated. Again the buffer storage flipflop is complemented by a pulse from the system and original information written back into the core. Thus the pattern remains unchanged.

Several changes from normal operation are required to produce the double read-write cycle. These changes are accomplished by throwing switch SØ. Considering the switch positions left to right, it will be seen that the first switch position causes the output of delay unit 21 to be admitted to mixer 14 and produce a double read-write cycle. The second

section of switch SØ admits a pulse from the output of delay unit 23 into the ZERO side input of buffer storage flipflop 26 in order to prepare this flipflop for the second read output. The third section of switch SØ admits the system pulse which will complement buffer storage flipflop 26 via mixer 30. The fourth section of switch SØ causes the output of the sensing amplifier (via buffer amplifier 93-4) to be applied to the complement input of buffer storage flipflop rather than the ONE side input. These four changes satisfy the conditions necessary for the complemented mode of operation.

## AUTOMATIC PATTERN CHECKING CIRCUIT

The automatic pattern checking circuit is located at the area S-2 on the drawing. It consists of switch S8, mixer 94, alarm flipflop 89, gate tubes 91 and 92 and a checkerboard pattern generating flipflop 84. This pattern checking logic is designed to check patterns of all ONEs, all ZEROs and the checkerboard and complemented checkerboard patterns. Logic could be designed to check any pattern as long as it is known what the sequence of ONEs and ZEROs out of memory will be when the pattern is scanned. What this logic does is provide a complementing pulse to flipflop 89 every time a pulse is properly expected out of the sensing amplifier.

The action of the circuit is as follows: In checking a pattern of all ONEs, switch S8 is put into the B position as shown on the drawing. The alarm flipflop 89 is initially cleared by a clock pulse from channel selector 2. For a pattern of all ONEs, we know that there should be a pulse coming out of the sensing amplifier for every readout operation. Therefore, we take a system pulse which occurs, in time, prior to the read operation and we apply it to the complement input of flipflop 89 via mixer 94. This is the pulse which comes into switch S8 on cable 172. This pulse puts flipflop 89 into the ONE position turning on gate tube 87. When the read operation occurs, a pulse should come out of the sensing amplifier via buffer amplifier 93-5 (L11), go through switch S7 which is in the upper position, mixer 94, and complement flipflop 89 back to the ZERO position. When a pulse from delay unit 23 at the end of the write operation gets through control grids of gate tube 87 it finds the gate tube off and does not get through to cause an alarm. Should, however, a ONE pulse fail to come out of the sensing amplifier, flipflop 89 would have remained in the ONE position, gate tube 87 would have been on and an alarm pulse would have gotten through to indicate the absence of a ONE readout.

To check a pattern of all ZEROs, switch S8 is placed in the neutral position. Flipflop 89 is again initially cleared. For a pattern of all ZEROs, we should expect no pulses to come out of the sensing amplifier during the read operation. For this check we do not supply any pulses from the system to complement flipflop 89. Therefore, at the time of the readout operation flipflop 89 could be in the ZERO position and should remain in the ZERO position. If, however, a ONE pulse comes out of the sensing amplifier, flipflop 89 would be set to the ONE position turning on gate tube 87 and causing an alarm when the alarm pulse comes along at the end of write time.

Checking the pairs-checkerboard pattern is basically the same kind of action as goes on for the patterns of ONEs and ZEROs. The only difference being that in this case we electronically select the pulses from the system which will complement flipflop 89. Since we already have a flipflop which is capable of generating the pairs-checkerboard pattern, it is a simple matter to let this flipflop continue to operate while the memory is remembering and to use it instead for checking purposes. For this use we add a gate tube on the ONE side of the flipflop. Whenever a ONE is being read out of memory, flipflop 84 will be in the ONE position.

Whenever a ZERO is being read out of memory it will be in the ZERO position. Prior to the read operation, gate tube 91 will supply a pulse via switch S8, which is in position T, and mixer 94 to the complement input of flip-flop 89. When a ZERO is being read out of memory, there will be no pulse into the complement input of flipflop 89. The checking action is exactly the same as for the cases of all ONEs and all ZEROs.

The action of this circuit in checking the complemented pairs-checkerboard pattern is a bit more complicated. For this operation, switch S8 is placed again in the neutral position. Another gate tube (92) is added on the ZERO side of flipflop 84. Switch S7 is placed in the B position. Flipflop 90 and gate tube 88 is essentially a divider circuit so that only the pulse which comes out of the sensing amplifier during the second read operation can be used for checking purposes. Note that flipflop 90 is always put in the ZERO position by a pulse from delay unit 16 which occurs before the read operation. Only if a double read-write cycle is called for does a pulse from delay unit 21 via switch SØ cause flipflop 90 to be set to the ONE position thereby turning on gate tube 88. Also for this complemented checkerboard pattern check, switch S12 must be placed in the B position thereby providing an alarm pulse from an alternate source which occurs only for the second half of the double read-write cycle. Since the information which comes out of memory during the second read operation of a double read-write cycle is the complement of that occuring during the first read-write cycle, we use the pulses out of gate tube 92 to complement the alarm flipflop 89. The checking action from here on is exactly the same as is the case of the pairs-checkerboard pattern.

To summarize this latter case, the difference between checking the pairs-checkerboard pattern and the complemented pairs-checkerboard patterns lies in gating out the sensing amplifier output during the first read operation, providing a checking or alarm pulse during only the second read-write cycle, and utilizing a gate tube on the ZERO side of pattern generating flipflop 84 instead of a gate tube on the ONE side.

## AUTOMATIC PATTERN REWRITING LOGIC

This circuit is located at N-10 on the diagram. It consists of flipflop 99, gate tubes 98 and 97 and 96, switch S11, flipflop 101, gate tube 100, flipflop 104, gate tubes 102 and 103 and switch S10.

Consider first the automatic rewriting of a pattern of ONEs. For normal operation the sensing amplifier will be putting out pulses for every address. Should an error occur the automatic checking logic will cause an alarm pulse to set flipflop 99 to the ONE position. If switch S11 is closed the strobe pulse will bypass the sensing amplifier via gate tube 97 and switch S11 and set up flipflop storage to a ONE position, thereby ordering the rewrite of a ONE. This rewriting process continues until the second Y end-carry. By this time the raster has been completely rewritten at least once, and the pattern should be restored. Flipflop 101 and gate tube 100 are a scale of two divider circuit for the counting of this second end-carry. The second Y end-carry clears flipflop 99 thereby restoring control of rewriting to the sensing amplifier. This takes care of rewriting ONEs.

In considering the rewriting of ZEROs it will be noted that gate tube 96 is in series with the output of the sensing amplifier. Consider a pattern of all ZEROs in the memory plane. Since gate tube 96 is tied to the ZERO side of flipflop 99 it is on during normal operation. Should a ONE pulse come out of the sensing amplifier the automatic checking logic will cause an alarm pulse to set flipflop 99 to the ONE position. This then turns off gate tube 96 and forces a pattern of ZEROs to be written into the plane. This action likewise continues until the second end-carry occurs and resets flipflop 99 to a ZERO, thereby turning on gate tube 96 again and restoring control of rewriting to the sensing amplifier again. This takes care of rewriting ZEROs.

Consider now the rewriting of the pairs-checkerboard pattern. Gate tube 103 is in series with gate tube 20. This gate tube is on during normal operation. Gate tube 102 is in series with gate tube 110 on the ZERO side of flipflop 84. On the occurrence of an alarm pulse during operation of the pairs-checkerboard pattern, flipflop 104 is set in the ONE position, thereby giving rewriting control to flipflop 84 via gate tube 102. This action likewise continues until the second Y end-carry has occurred at which time flipflop 104 is restored to the ZERO position and rewriting control is returned to buffer storage via gate tube 103. Switch S10 must be closed for this latter mode of operation. Also, switch S11 must be open for both the ZERO and the checkerboard modes of rewriting.

The checking action for the quadrant checkerboard pattern is the same as for the pairs-checkerboard pattern because flipflop 84 generates both patterns. Switch S11 must be open for the quadrant checkerboard mode of operation.

Signed E. A. Guditz
E. A. Guditz

EAG:jd

cc: Group 62 Memory Section Staff
Group 63 Leader and Section Chiefs
W. Wittenberg - IBM
H. Hample - IBM
F. Hadley - IBM
J. Piro
S. DiFazio
W. Canty - IBM

Attach: SD-48544G
SD-47148

UNIT LOCATION CHART
(For use with SD-47148)

| Unit | Rack |
|---|---|
| 1 | 3-B1 |
| 2 | 2-D1 |
| 3 | 2-C1 |
| 4 | 3-A1 |
| 5 | 3-E1 |
| 6 | 2-A2 |
| 7 | 2-B2 |
| 8 | 2-C2 |
| 9 | 2-D3 |
| 10 | 2-B3 |
| 11 | 2-C3 |
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