Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MTC ACCUMULATOR TEST

To: Norman H. Taylor

From: Harlan E. Anderson

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Abstract: A high speed self checking test was used to test the MTC accumulator. Every gate tube and buffer tube was tested at a time when it should pass a pulse and at a time when it should not pass a pulse. Marginal checking of this test indicated that the accumulator had satisfactory margins throughout.

Description of Test

The accumulator test consisted of the following steps:

1. The partial-sum flip-flops and carry flip-flops were cleared.

2. All 1's were added into the partial sum.

3. All 1's were added in again, thereby creating a carry in each digit.

4. The command carry was performed next.

5. At this point the partial sum has all 1's. 1×2^{-15} is added to the partial sum thus sending a high-speed carry the full length of the register.

6. The partial-sum and carry flip-flops were cleared.

7. The number 0.101 010 101 010 101 was added in.

8. This was cycled right 3 times.

9. The same number was added again.

10. Step 5 was repeated.

If the accumulator responded properly, it continued running at high speed through the same test.

If any part of the accumulator failed to respond properly, the test would stop and an alarm would occur.

Results

During this test, the screens of the gate tubes were marginally checked separately and simultaneously. When checked simultaneously, the screen grid of all gate tubes could be reduced from +90 volts to +52 volts before an error occurred. The screens of all flip-flops could be varied from +55 volts to -45 volts before an error occurred.

All pulse amplitudes, durations, rise times, and general appearances were checked and found to be excellent.

Signed _____Harlan E. Anderson_____
                          Harlan E. Anderson

Approved _____Kenneth W Olsen_____
                          Kenneth Olsen

Approved _____
                          Norman H. Taylor

HEA:jrt