6D-2631

TX-2 CIRCUITRY HANDBOOK*

A discussion of the
circuitry used in the
Lincoln TX-2 Computer.

Jonathan R. Fadiman**

1 October, 1958

* The research reported in this document was supported jointly by the Army, Navy, and Air Force under contract with the Massachusetts Institute of Technology.

** Lincoln Laboratory, Massachusetts Institute of Technology.

ACKNOWLEDGEMENT

I am indebted to Mr. Ben Gurley for his many suggestions and valuable aid in the preparation of this paper and for the section on the display system; to Mr. Frank Hazel for his assistance in editing; to Mr. Arthur Grennel for the block schematic drawings in the reference manual; to Mrs. Madeline Higgins for the typing; and to many other members of Group 63 for their suggestions and corrections.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

LIST OF ILLUSTRATIONS (Cont'd)

PART I

INTRODUCTION

This handbook is a discussion of the transistor circuitry used in the Lincoln TX-2 computer. The circuitry itself, the operation, and the use of all of the TX-2 plug-in units are explained. These units include all those used in the central machine, index memory, display system, toggle switch storage system, input-output units, and control. Part I describes the general methods by which transistor circuitry is used to implement the logic of the computer.

Part II gives a detailed description of each of the plug-in units used in TX-2. Each plug-in unit is assigned a serial number, which is mentioned in the text where the unit is discussed. This number is indicated by the color code on the handle of the unit itself (the colors are read from outside to inside).

Part III, the reference manual, lists the serial numbers of each of the units in order. Each left-hand page carries a circuit diagram of the unit; on the facing page is a block schematic diagram and a few salient facts about the unit. The user will find it advantageous to refer to the reference manual in connection with his study of the circuit discussed.

In order to avoid needless duplication, numerous references are made in the text of this handbook to M-notes issued by Division 6, which contain information pertinent to the TX-2 circuitry. Of special importance is 6M-4968, "The Lincoln TX-2 Computer," by W.A. Clark et al, issued April 1st, 1957. It contains a logic outline of the computer, a discussion of the input-output system, a discussion of the memories and memory circuitry, and a general outline of the central computer circuitry. It is recommended that 6M-4968 be read in conjunction with this handbook, although it must be remembered that the M-note was written before the actual construction of the machine, and thus there are many details which have been changed.

At the end of this handbook is included a list of M-notes pertaining to TX-0 (a small general purpose transistor computer constructed as a precursor to TX-2), TX-2 itself, and surface barrier transistors in general. The specifications of the various types of surface barrier transistors used in TX-2 are also given.

TX-2 is an experimental research machine; frequent additions and modifications will be made as more knowledge is gained from the construction and operation of the computer. These changes will be incorporated in new pages punched for easy insertion in this handbook.

GENERAL DISCUSSION

In TX-2 there are two logic levels of information: ground and -3 volts. Timing pulses are negative, with an amplitude of from 2.5 to 3 volts and a width of from 80 to 100 mμsec. The principal supply voltages used for the surface barrier transistor (SBT) circuitry are -3, -10, and +10 volts. The +10 volts on some of the lines can be varied from 0 to +20 volts for marginal checking. In addition there is a -30 volt supply used for input-output devices, driving relays, etc.

The L-5122 and L-5134 SBT's are used for high speed work. AND and OR gates are formed from inverter or emitter follower combinations. Timing pulses, generated by vacuum tube circuits, are stepped down by pulse transformers to 3 volt, 0.1 μsec negative pulses which are used in the computer. These pulses are gated by the register driver circuit. The cascode configuration is used as a power amplifier to obtain fast rise and fall times. There is a high speed flip-flop capable of 5 mcps operation, and a much simpler dual flip-flop for low speed work to 800 kcps.

A standard set of symbols shown in Figure 1 is used for all TX-2 block schematic drawings, and for all drawings in this handbook. Figure 2 is a system schematic drawing of TX-2, showing the principal registers and information paths.

PACKAGING

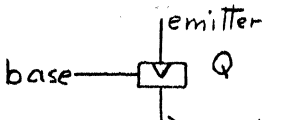
All TX-2 circuitry is packaged in plug-in units each measuring approximately 1 by 2 by 6 inches long, and containing from 4 to 14 transistors and associated resistors and condensers. (For the central computer there is an average of 8 transistors per PIU.) In general there are two etched wired cards per plug-in unit; these are connected by wires to an 18-pin plug and mounted in a steel frame to prevent flexing. The components are mounted on the etched cards by hand-soldering either to solid turret lugs or small eyelets. Pictures of two typical plug-in units (one using turret lugs and the other using eyelets) are shown in Figure 3.

TRANSISTORS

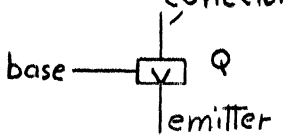
The high speed logic circuitry for TX-2 is based on the use of Philco surface barrier transistors for which the specifications are given in an appendix to this handbook. Also in the appendix is a transistor nomenclature reference which lists the transistor manufacturer and the experimental type designations plus the EIA or MIL designations which may have since been assigned. With certain exceptions that will be noted later, all inverters and emitter followers are L-5122 (2N240) transistors. Micro-alloy L-5134 (2N393) transistors are used where a high current gain at relatively high current levels (10 - 70 ma) is required. Thus the L-5134 is used as the power output stage of the high speed flip-flop, in the inverting cascode and cable driver, as the pulse gating transistor in the register driver, and in some input-output circuitry. There are a few places in the machine where a very high frequency, high current transistor is needed, and here the Philco micro-alloy diffused-base transistor 2N501 (previously known as the L-5409) is used. For a detailed discussion of the L-5122 parameters, refer to 6M-4955 by D. J. Eckl, for some notes on the L-5134 transistor refer to 6M-5193 by J. W. Langford, and for some notes on the 2N501 refer to 6M-5856 by J. W. Langford.

TX-2 BLOCK SYMBOLS

PNP Transistor

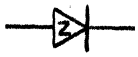


NPN Transistor



Diode (Ge or Si)

Zener Diode



Double Anode Diode

-3 Volt Level

Ground Level

Non Standard Level

Negative 0.1 μsec. Pulse

Positive Pulse: Input to Flip-Flop

+30 Volt Supply

+10 Volt Supply

Ground

-3 Volt Supply

-10 Volt Supply

-30 Volt Supply

Figure 1.

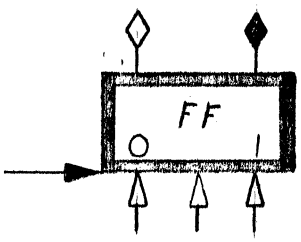
SA-87034 (Sheet 1 of 2)

TX-2 BLOCK SYMBOLS (Cont.)

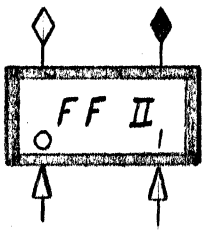
Non Standard Positive Voltage Supply

Non Standard Negative Voltage Supply

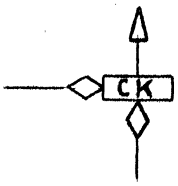
High Speed Flip-Flop



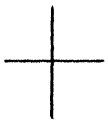
Dual Flip-Flop Mod II (1 FF)



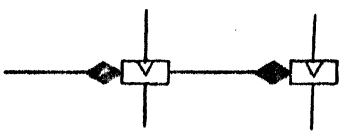
Capacitor-Diode Gate



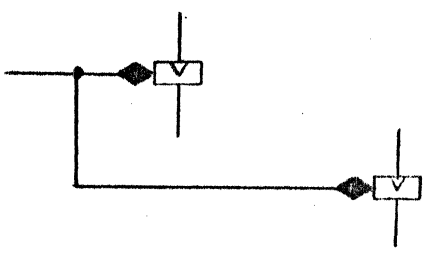
No Connection



Connection



is equivalent to:



SA-87034 (Sheet 2 of 2)

SA-87034 (Sheet 2 of 2)

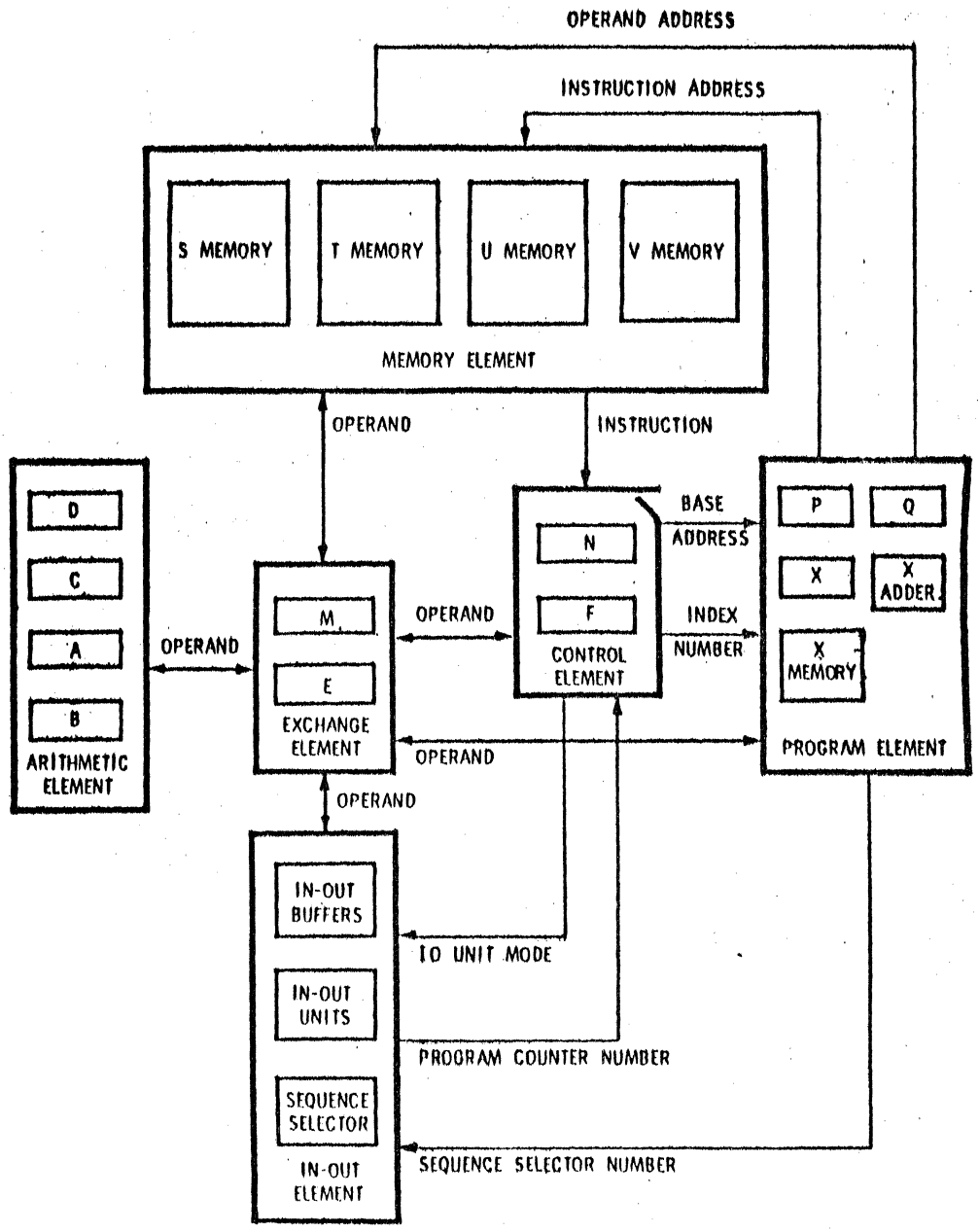


FIG. 2
TX-2 System Schematic

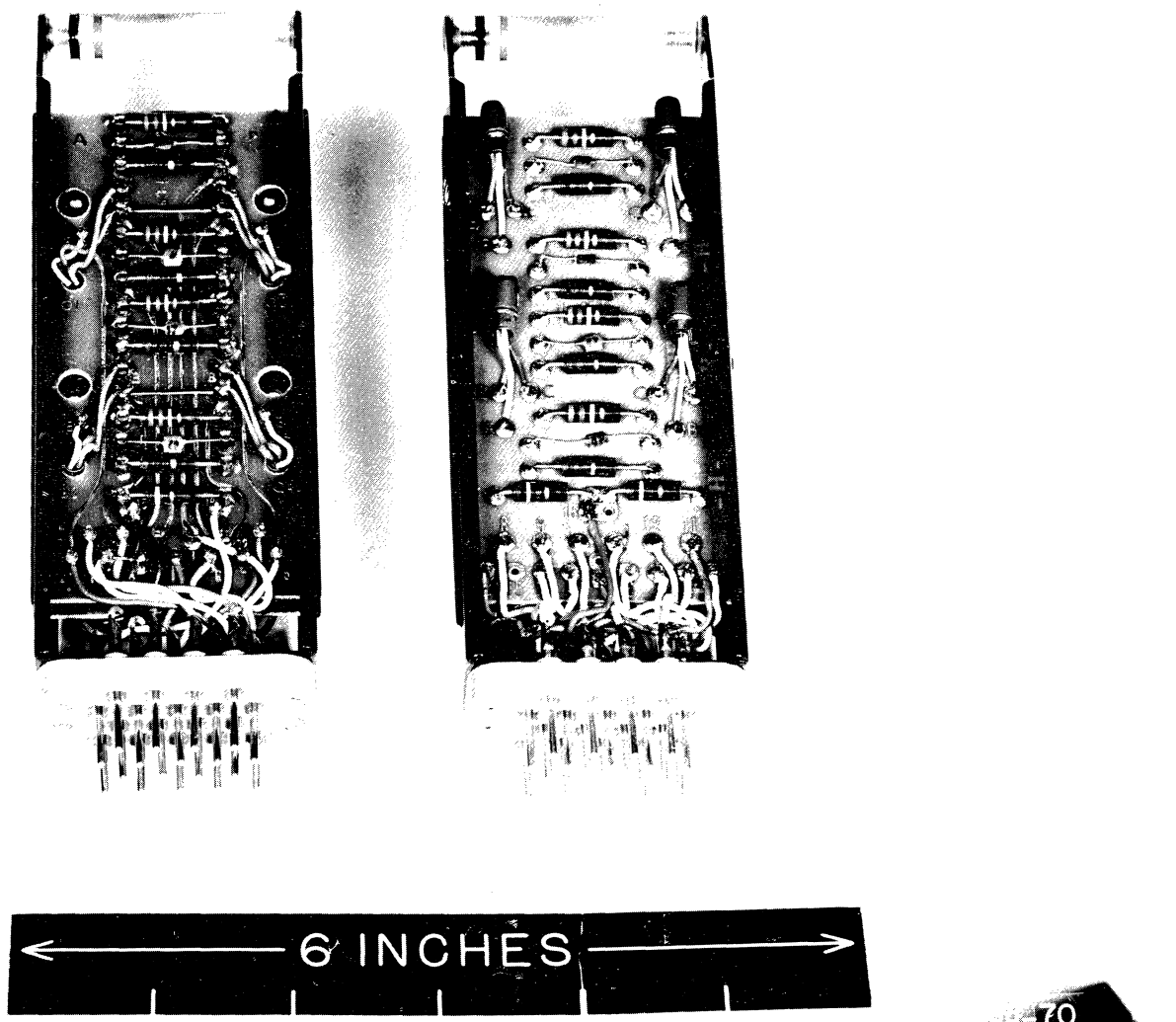


FIG. 3

LOGIC

All the high speed logic for TX-2 is performed with transistors by what might be termed "level logic". The AND and OR functions are obtained by mixing and gating levels; never is one pulse used to gate another. The levels are generated by flip-flops, which are set, cleared, or complemented by pulses arriving at a basic synchronous clock rate. The levels are transmitted throughout the computer by means of open wire or twisted pair wire depending upon the length of line. The necessary logic operations are performed with these levels which may be used to gate pulses on or off through register driver circuits. The pulses coming out of register driver circuits are sent directly to flip-flops. They may be gated by other levels at the input to each flip-flop, and, by means of transistors a number of pulses may be mixed at this point. In the TX-2 system pulses can be gated only twice: once at the register driver and once at the flip-flop itself. Therefore when many consecutive stages of logic are to be performed, they must make use of levels rather than pulses.

Logic levels at ground and -3 volt potentials are used to convey information. In TX-2 a flip-flop is said to be set to the ONE state when the ONE output is at -3 volts. Therefore if one wishes a -3 volt level to be the result of setting a flip-flop, one connects the output wire to the ONE output; conversely, a ground level results if this wire is connected to the ZERO output.

The AND and OR gates that perform level logic in TX-2 are formed from either emitter followers in parallel or inverters in series and/or parallel. The AND gate for ground level in, ground level out, is formed by connecting emitter followers in parallel as shown in Figure 4A. An inverting AND gate for ground level in, -3 level out, is formed by connecting inverters in parallel as shown in Figure 4B. An inverting OR gate for ground level in, -3 level out, is formed by connecting inverters in series as shown in Figure 4C. The polarity of the input signal determines whether a given gate is AND or OR. Thus, in order to specify the logic function of any particular circuit configuration, it is necessary to specify the polarity of either the input or the output.

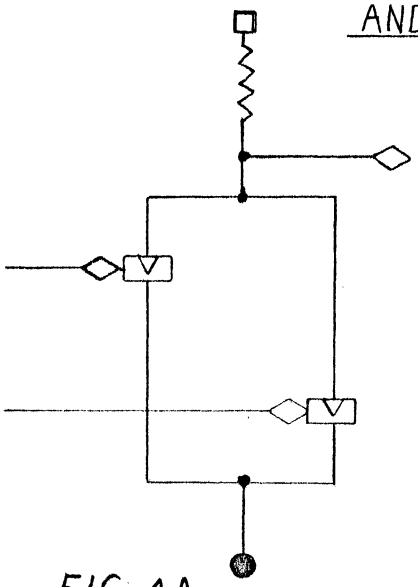


FIG. 4A

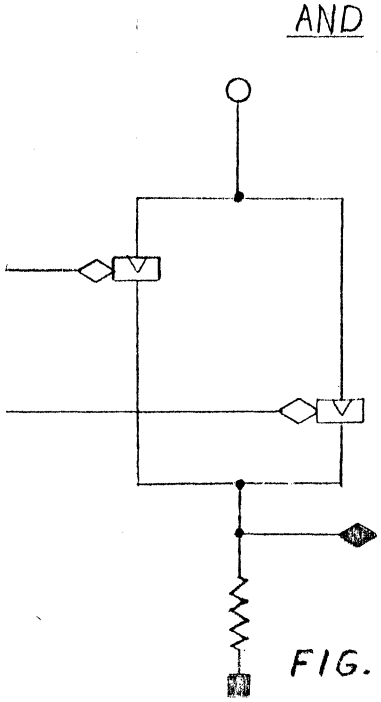


FIG. 4B

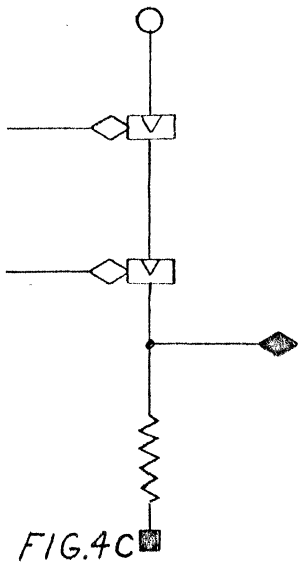


FIG. 4C

SA-87035

Only two L-5122 inverters can be connected in series for two reasons: 1) the 0.15 volt drop across one saturated transistor is multiplied by the number (n) of inverters in series and the output then becomes 0.15n volts below the required ground level; and 2) the collector current I_c of the transistor Q_1 nearest ground is equal to $\frac{E_s}{R_L} + I_{b_2} + I_{b_3}$ etc. where E_s is the supply voltage, R_L is the load resistance, and I_{b_2}, I_{b_3} etc. are the base currents of all transistors between Q_1 and the supply voltage. Thus the transistor nearest ground will tend to come out of saturation if there are many transistors below it. The number of inverters that may be placed in parallel is limited by the delay which can be tolerated. The fall transition time (measured at the 10% points from the point at which the input starts up from -3 volts to the point at which the output returns to -3 volts) is shown as a function of the number of inverters in parallel in Figure 5. (The input rise time is about 20 mμsec.)

When emitter followers are placed in parallel to form an AND gate, the transition delay time is considerably less than that of inverters. The rise transition time, as a function of the number of emitter followers in parallel, is shown in Figure 6. The rise transition time is measured at the 10% point near the ground level.

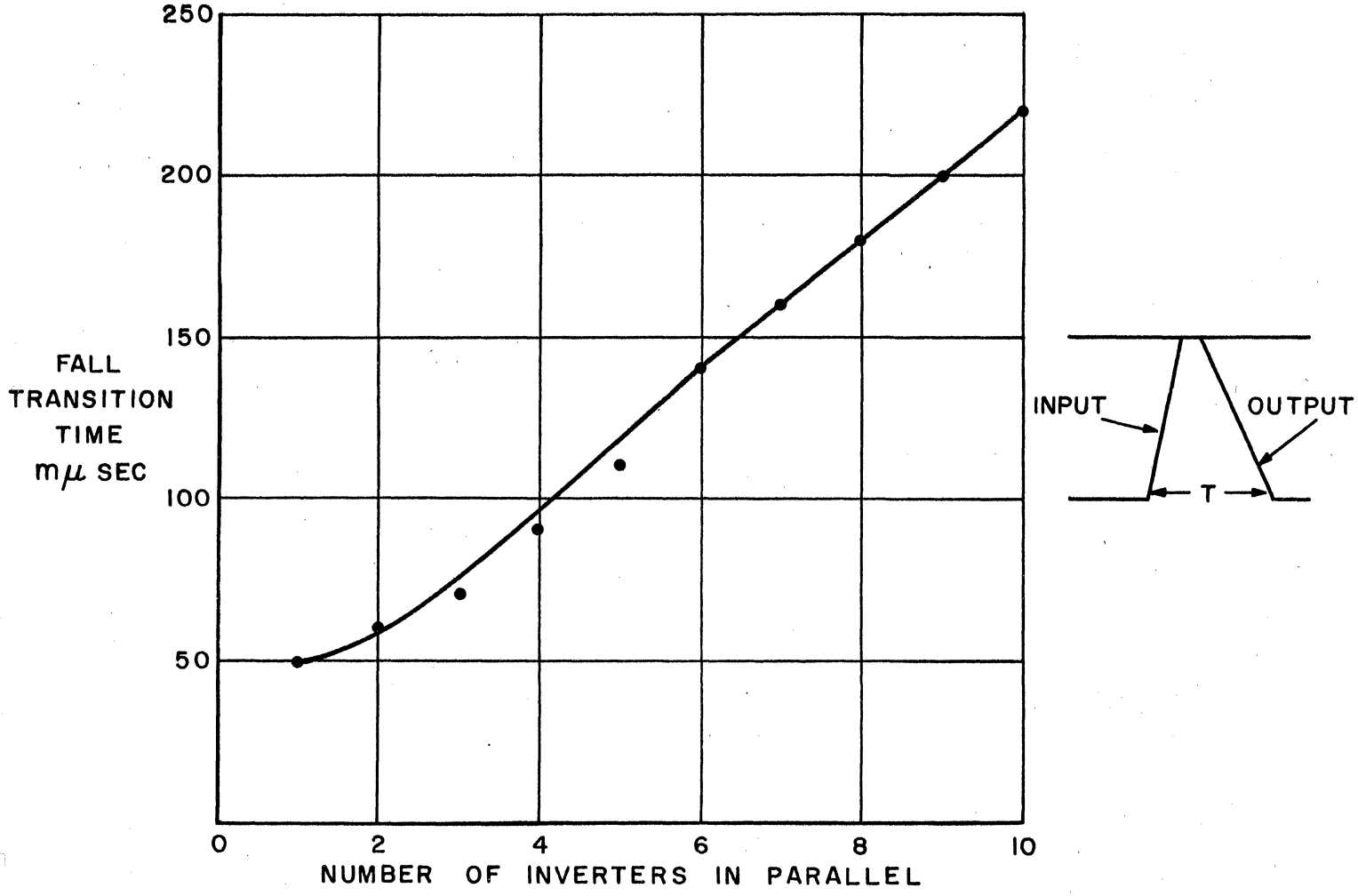


FIG. 5

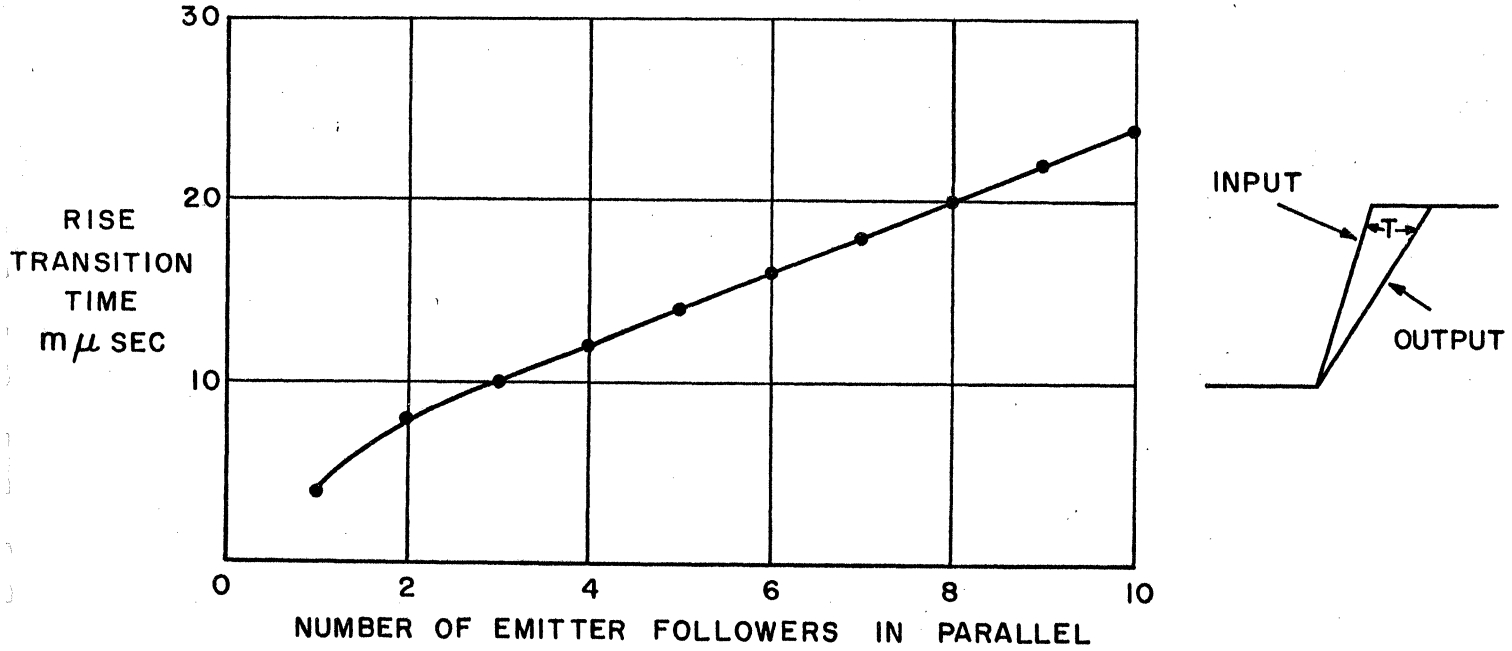


FIG. 6

TRANSITION TIMES vs NUMBER OF TRANSISTORS IN PARALLEL

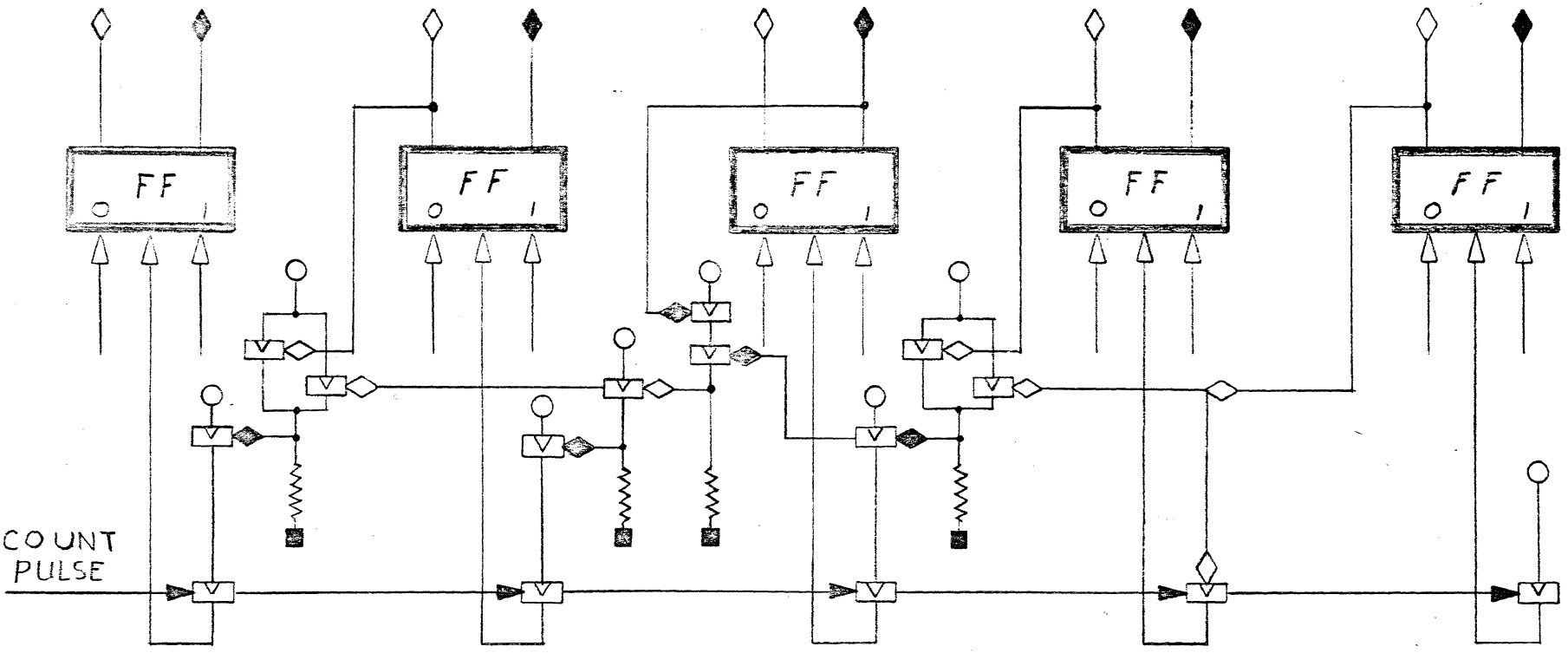
A-11960

PART II - CIRCUIT DETAILS

CENTRAL COMPUTER

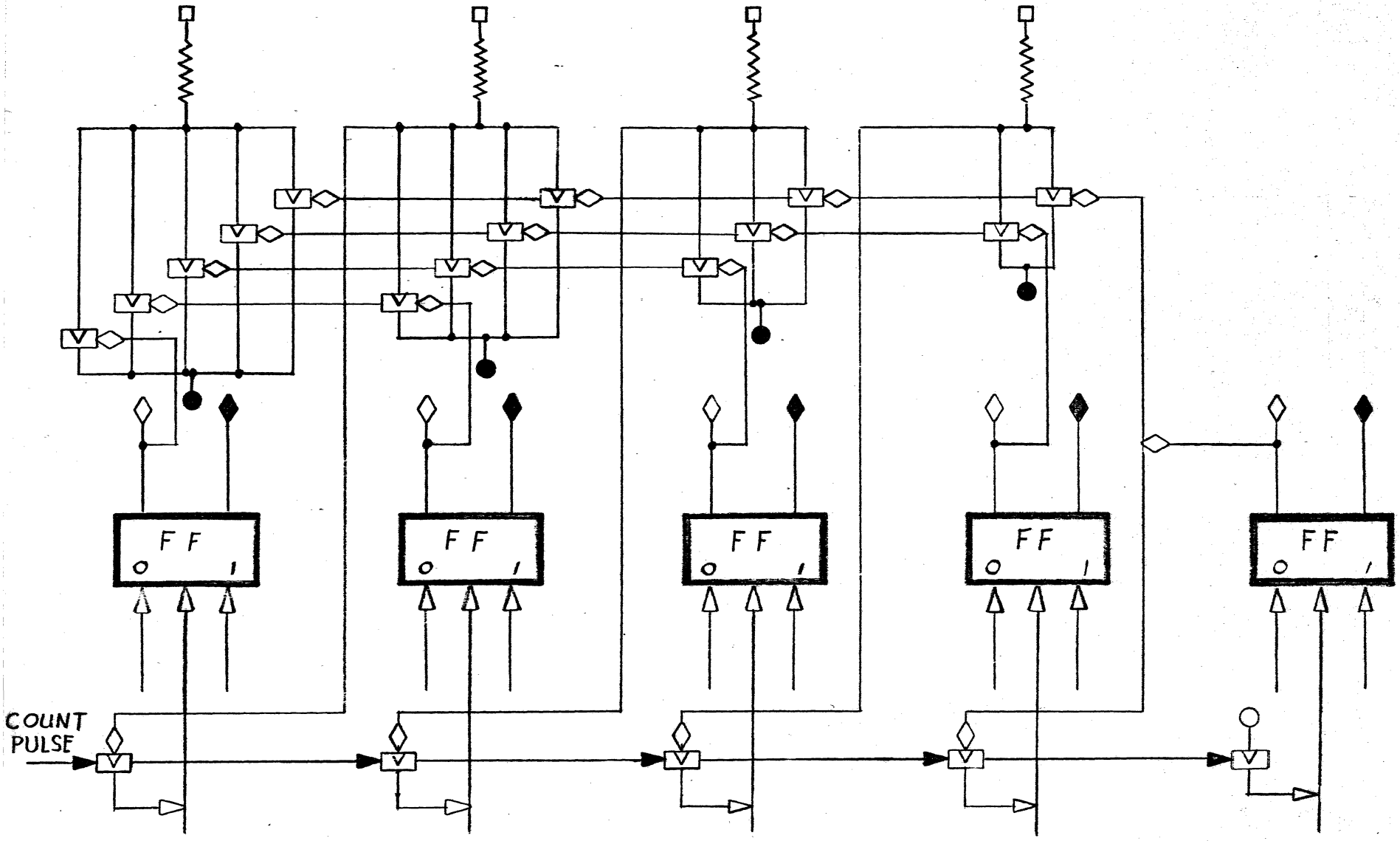
Counting Circuits for TX-2 logic are formed by flip-flops and inverters as shown by the block diagram, Figure 7. Each count pulse is separated by 0.4 μsec to compensate for the delay imposed by the flip-flop and the inverters.

If a faster counting rate is required, emitter follower circuits (Figure 8) are used which need only 0.2 μsec between each count pulse. These circuits, however, use more transistors, and so complicate counters containing a large number of digits.



5 STAGE COUNTER USING INVERTERS

FIG. 7



5 STAGE COUNTER USING EMITTER FOLLOWERS

FIG. 8

Inverter In the circuit shown in Figure 9A the values of load resistance (R_1), input resistance (R_2), and positive bias resistance (R_3) are chosen to give maximum tolerance to signal variations, noise voltages, and transistor parameter variations consistent with the necessary driving capabilities. The result is a circuit for which the maximum output current at -3 volts is 2.9 ma; minimum input current is 1.0 ma (1.2 ma at -3 volts); positive bias current from +10 volt is .15 ma, which gives a positive bias of .31 volts above ground. All of the inverters work from a -10 volt supply.

The actual voltage at the collector, however, is never allowed to exceed -5 volts; it is clamped to -3 by an emitter follower, or by a voltage divider to ground formed by the input resistance to an inverter following it. However if the inverter is accidentally unloaded it will not be damaged. The minimum punch-through voltage (emitter-to-collector voltage) of the L-5122 and L-5134 is 6 volts. If the transistor were to punch through at this voltage, the power dissipation would be only 10 mw -- not enough to damage the transistor. The value of the capacitor (C_1) is chosen so that with a 3 volt input signal, the capacitor will store a charge at least as large as that contributed by the hole storage of a transistor with the maximum allowable hole storage coefficient. Thus sufficient overdrive is provided for minimum rise and fall transition times. A single inverter provides enough current to drive either two other inverters, three emitter followers, or one inverter and one emitter follower. The d-c transfer characteristic of the TX-2 inverter circuit is shown in Figure 10.

The following plug-in units consist of L-5122 inverters such as are described above:

Inverter P-6 (No. 02)
Inverter S-8 (No. 03)
Inverter P-5 (No. 04)
Inverter S-6 (No. 05)
Inverter P-8 (No. 24)
Inverter S-8R (No. 32)
Inverter P-10 (No. 33) (Two transistors nearest ground are L-5134)
Parity Circuit (No. 34) (Also contains 2 emitter followers)
Inverter S-8RA (No. 46) (Contains 3 L-5134 and 1 2N501)

INVERTER

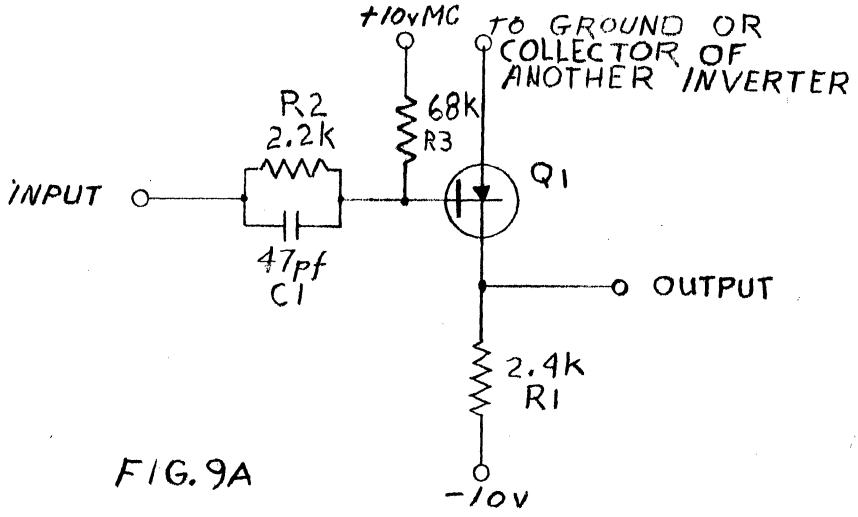


FIG. 9A

EMITTER FOLLOWER

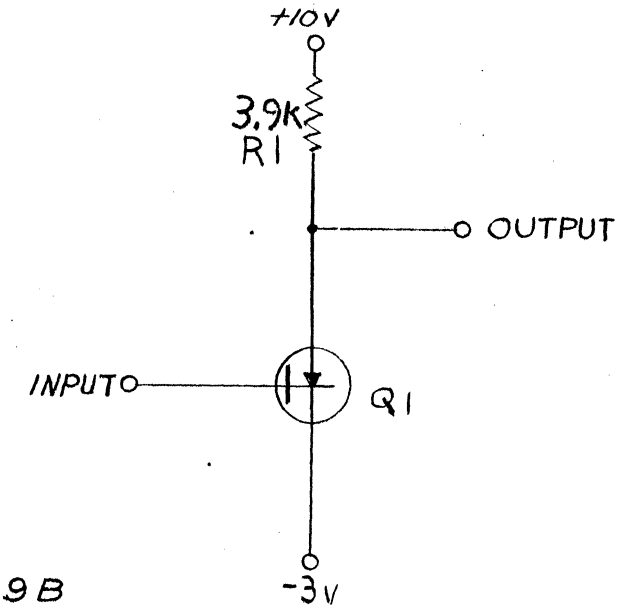


FIG. 9B

SA-87038

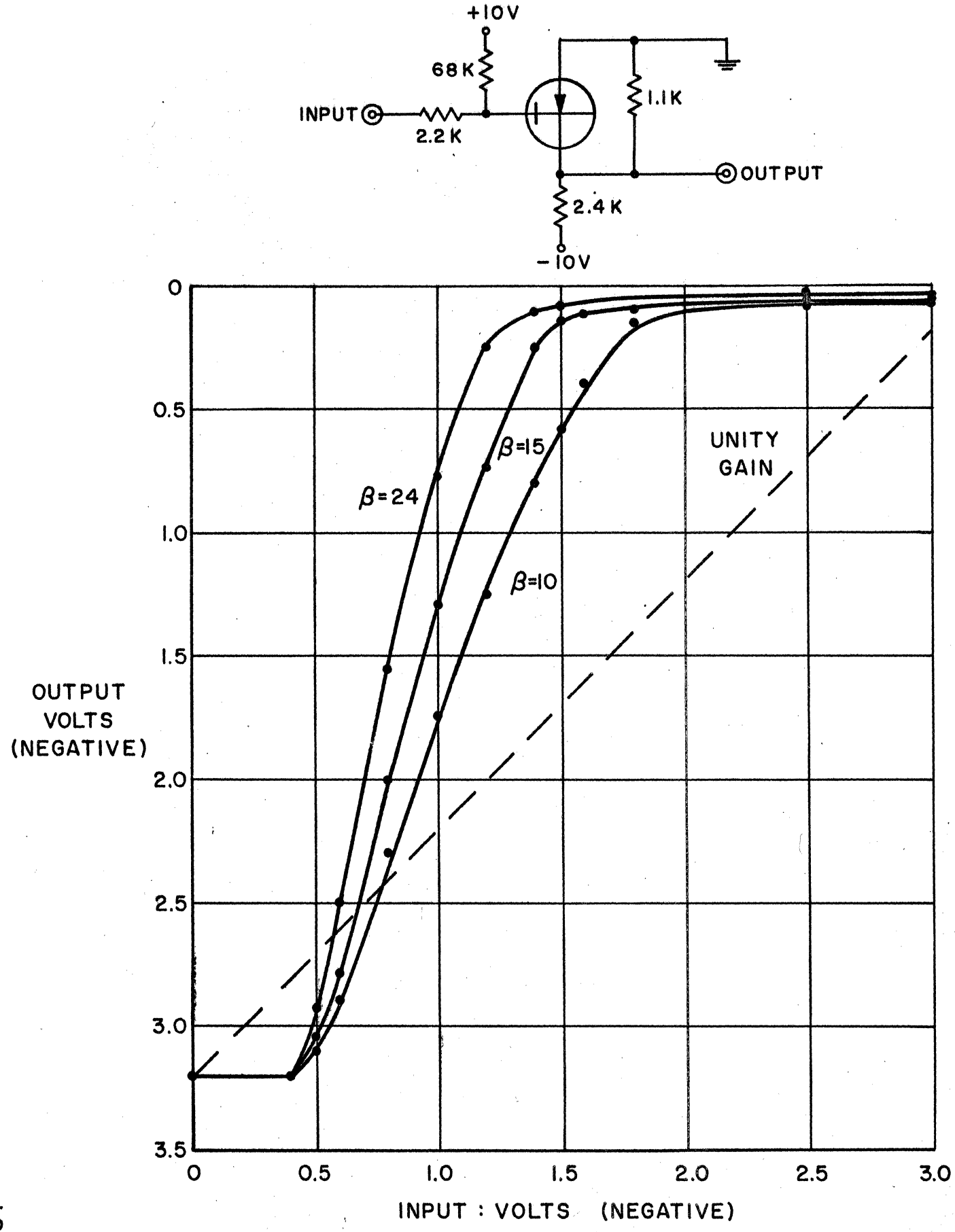


FIG. 10

TRANSFER CHARACTERISTIC TX-2 INVERTER

A-84967

Emitter Follower The circuit shown in Figure 9B is used as a logic element and as a current amplifier. An emitter follower may be driven from an inverter, in which case it is kept in saturation when turned on since its base is returned to -10 volts through the load resistance of the previous inverter. An emitter follower may also be driven from a cascode circuit or from another emitter follower. In these cases, the base is returned to -3 volts through the very low resistance of a saturated transistor. One emitter follower may drive another only if the first is driven by an inverter, and is thus saturated from -10 volts. Usually the emitter is returned to +10 volts through a 3.9K resistance to limit the total emitter current to 10 ma. Thus the maximum output current is 6.7 ma. If a larger reverse current from +10 volts is needed (as when driving several inverter bases as fast as possible, or when driving the emitter of a pulsed transistor) the load resistance may be decreased to 2K (or two 3.9K resistors in parallel) provided there are at least two emitter followers in parallel in the same unit to share the dissipation in the "off" condition. In this case the output current is limited to 3.5 ma. Therefore one emitter follower will drive a maximum of 3 inverter bases if sufficient time is available or 5 emitter follower bases if the current limitation is observed.

The following plug-in units consist of L-5122 emitter followers such as are described above:

Emitter Follower 8	(No. 06)	
Emitter Follower 4	(No. 07)	
Address Decoder	(No. 13)	(Contains 12 emitter followers and 4 sets of output diodes.)
Emitter Follower 9	(No. 35)	
Time Level Decoder	(No. 37)	(Contains 5 emitter followers and 2 cascode circuits.)

Cascode and Cable Driver (No. 08) The circuit shown in Figure 38 (in Reference Manual) is used in TX-2 as a power amplifier to provide fast rise and fall times and to supply a large amount of current in both the ground and -3 volt states. Consequently it is used as the output stage of the high speed flip-flop, as a power amplifier for driving a large number of bases, and as a cable driver. The input signal is applied simultaneously to the bases of the inverters, Q_1 and Q_2. The output of the inverter Q_1 drives the base of Q_3. Therefore the inputs to Q_2 and Q_3 are always opposite in phase so that in the steady state only one transistor is conducting. Q_3 acts as an emitter follower which provides the driving current in the -3 state, and pulls the output quickly down to -3 volts. Q_2 acts as an inverter which provides the driving current in the ground state, and pulls the output quickly up to ground. Thus, the circuit exploits the fast fall time of the emitter follower, the fast rise time of the inverter, and makes the total current available to the load since none is required in load resistances.

The TX-2 plug-in unit contains four independent inverting cascode circuits. A level input is required which swings from ground to at least -2.5 volts. The input transition times must be less than 0.2 μsec; the required input current is 2.4 ma at -3 volts. The maximum output current of 30 ma at -3 volts and 20 ma at ground is sufficient to drive 20 bases (either inverter bases or emitter followers) and one pulsed emitter from the direct output (pin H, etc.). The delay contributed by the cascode circuit is approximately 30 mμsec.

The same cascode unit is used to drive video cables from pin M, etc. through the 82 ohm resistor included in the unit to properly terminate the driven end of the cable. A series termination is possible because, unlike the emitter follower or inverter, the cascode circuit looks like a very low impedance (less than 10 ohms) when driving in either direction. Therefore reflections are completely absorbed at the input end of the cable and no termination is used at the output end. Each cascode cable driver circuit will drive one 93 ohm RG62/U cable or one twisted pair line. (Two lines may be driven by adding another 82 ohm resistor on the

back panel.) The maximum output current available at the end of the cable is 4 ma in either direction.

93 ohm cable is used in TX-2 to drive voltage levels to and from memory, input-output units, etc. Twisted pair wire (No. 22 stranded, Teflon insulated, twisted 2 turns per inch) is used to drive voltage levels over long distances within the central computer.

Timing Pulses TX-2 uses a vacuum tube clock to produce timing pulses at a 2.5 mcps basic clock rate. Two pulse outputs are available from the 2.5 mcps generator; one (β phase) is delayed 0.2 μsec from the other (α phase). The α and β pulses differ only in their reference to some arbitrary zero starting time. By means of this system, one event can occur at an interval of 0.2 μsec after another despite the fact that the maximum prf of the pulse transformers and amplifiers is only 2.5 mcps. For example, a flip-flop can be set on an α pulse and sampled 0.2 μsec later on a β pulse.

Each pulse output phase of the clock is fed to a shaper and then to a shaper amplifier which driver 10 vacuum tube driver amplifiers (No. 64).* The output of each of these is a 40 volt positive pulse which, in turn, drives 5 buffer amplifiers (No. 67). Negative 30 volt (variable 25-35), 0.1 μsec pulses from the buffer amplifiers are transferred to the computer frame over 93 ohm RG62/U coaxial cable. Each buffer amplifier drives one cable. At the end of each cable a non-inverting 7:1 pulse transformer provides -3 volt pulses for the transistor register drivers. Pulse transformer units (No. 36) are plug-in packages containing two pulse transformers and the proper termination for the cable. The transformer is wound on a Ferramic H toroidal core,** with a primary winding of 14 turns of No. 30 wire, and a secondary of 2 turns of No. 22 wire close-wound over the primary. Across the secondary a resistive load of 2.5 ohms properly terminates the cable and transformer. The maximum additional load on any one transformer is 10 ohms; this is equivalent to 4 fully loaded register drivers on at the same time.

* The tubes used are Sylvania, type 6888.

** General Ceramics F-625 (.375 O.D.)

Register Driver (No. 09) The circuit shown in Figure 40 (in Reference Manual) is a gate which passes clock pulses only when both level inputs are at ground. The register driver incorporates no pulse gain; it is merely a pulse switch. The TX-2 plug-in unit contains three such gates, two of which have a common pulse input. There are four transistors to each gate. Q_1 and Q_2 form a level AND gate that allows a pulse to pass only if there is a ground level at the inputs to both their bases. If there is a -3 volt level at either input, there will be no pulse output. In operation, the pulse input is applied to the collector of Q_3. Provided that Q_1 and Q_2 are held off by ground level inputs, the base of Q_3 will be saturated from the -10 volt supply. Thus an output pulse will appear from the emitter of Q_3. This transistor is an L-5134 used to carry the large pulse current necessary to drive a register. Q_4 is used when driving large amounts of capacity to pull the output up to ground at the conclusion of the pulse.

The 70 ma maximum output pulse current from the register driver is capable of driving a maximum of 20 bases (active or inactive). The input pulse current required is equal to the output current. A minimum input pulse of 3 volts is required by a fully loaded register driver. The maximum voltage drop across the driver is 0.5 volts. The required set-up time is 20 m_{μ}sec. The level input current required into each base is 2.13 ma at -3 volts, and 0.6 ma at ground. The input level is specified at ground or a minimum of -2.5 volts. If this level input is driven from a cable or twisted pair line, one cable may drive either one or two register drivers.

High Speed Flip-Flop (No. 01) uses RC coupling between inverters, and a cascode output. Q_1 and Q_2 are normally conducting pulse amplifiers which are cut off by a positive input pulse (going up to ground) at the "zero" or "one" input. Q_3 and Q_4 are the flip-flop transistors themselves which are RC coupled in the normal manner. A positive input pulse cuts off Q_1 or Q_2, opens the emitter circuit of Q_3 or Q_4, and changes the state of the flip-flop. Q_5 and Q_6 are amplifiers which are used to saturate the emitter followers of the output cascodes. Q_7 and Q_8, and Q_9 and Q_{10} form the cascode circuits on the "one" and "zero" sides respectively. These four transistors are L-5134's, used to carry the heavy output current required of the flip-flop. Q_{13} and Q_{14} are steering gate transistors which are wired internally to the flip-flop. In order to set, clear, or complement the flip-flop, one of the points "ONE IN", "ZERO IN", or "COMP. IN" is brought up to ground by a circuit such as the one shown in Figure 11A. Alternately, the circuit in Figure 11B may be used, if the ground level is supplied by a cascode circuit. A maximum of one pulse transistor and two level transistors may be used in series for input gating to the flip-flop. (The steering gate transistor or the cascode transistor which provides the ground level is considered as a level transistor.) A maximum of 15 pulse transistors may be connected in parallel to any of the flip-flop inputs. Q_{12} is an ungated clear input which is internally wired. A 2.5 volt negative pulse is applied at the "CLEAR IN".

The maximum usable prf of this flip-flop is 5 mcps and it has a nominal logic delay of 0.1 μsec. The maximum total transition time of fully loaded flip-flop is less than 0.2 μsec. The maximum output current is 30 ma at -3 volt, and 9 ma at ground. Thus the flip-flop will drive 20 bases in the -3 state, and will carry a maximum of 3 base currents plus one pulse current in the ground state. Plots of the output voltage vs. load current for a transistor meeting minimum specifications are given in Figure 12, and plots of the rise and fall transition times vs. the number of loads being driven are given in Figure 13. Plots of transition times vs. pulse amplitude are shown in Figure 14 and those of pulse amplitude vs. prf in Figure 15.

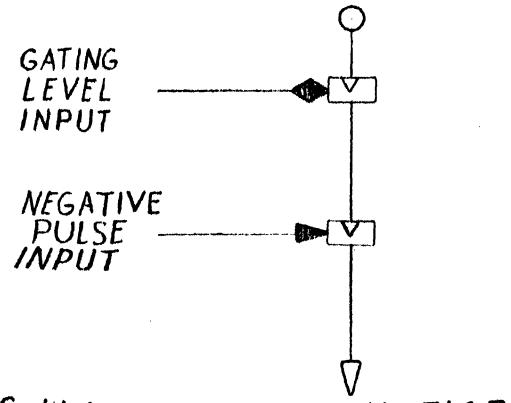


FIG. 11A

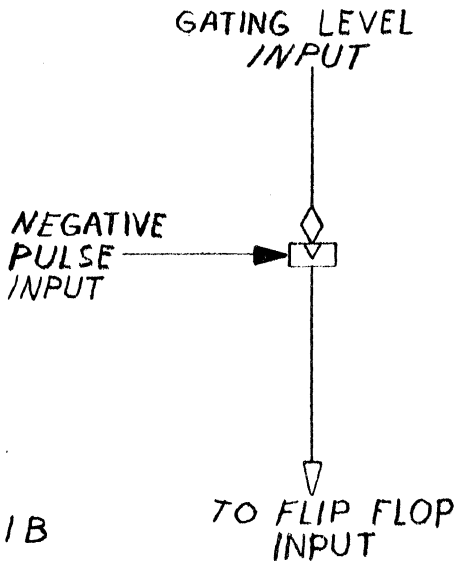


FIG. 11B

SA-87039

The input to the pulse gates to the flip-flop must be a negative pulse with a minimum amplitude of 2.5 volts, and a width of from 0.07 to 0.12 μsec for complement. The input pulse current into the base is approximately 2.5 ma. The flip-flop may be set or cleared with a 3 volt negative level, provided the level returns to its original ground state before the flip-flop is again changed.

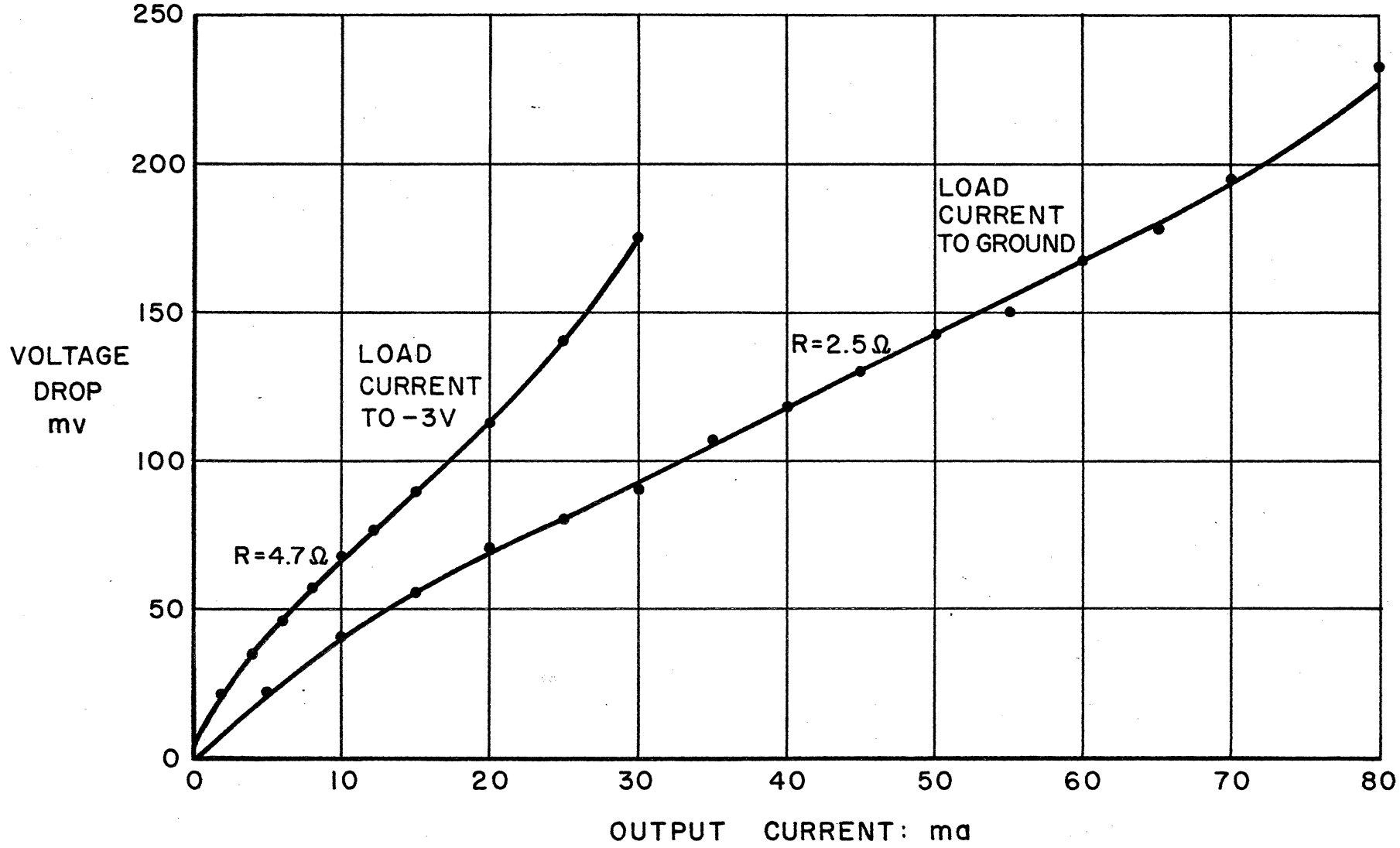


FIG. 12

HIGH SPEED FLIP-FLOP

VOLTAGE DROP ACROSS FLIP-FLOP CASCODE vs LOAD CURRENT

(MINIMUM β TRANSISTOR)

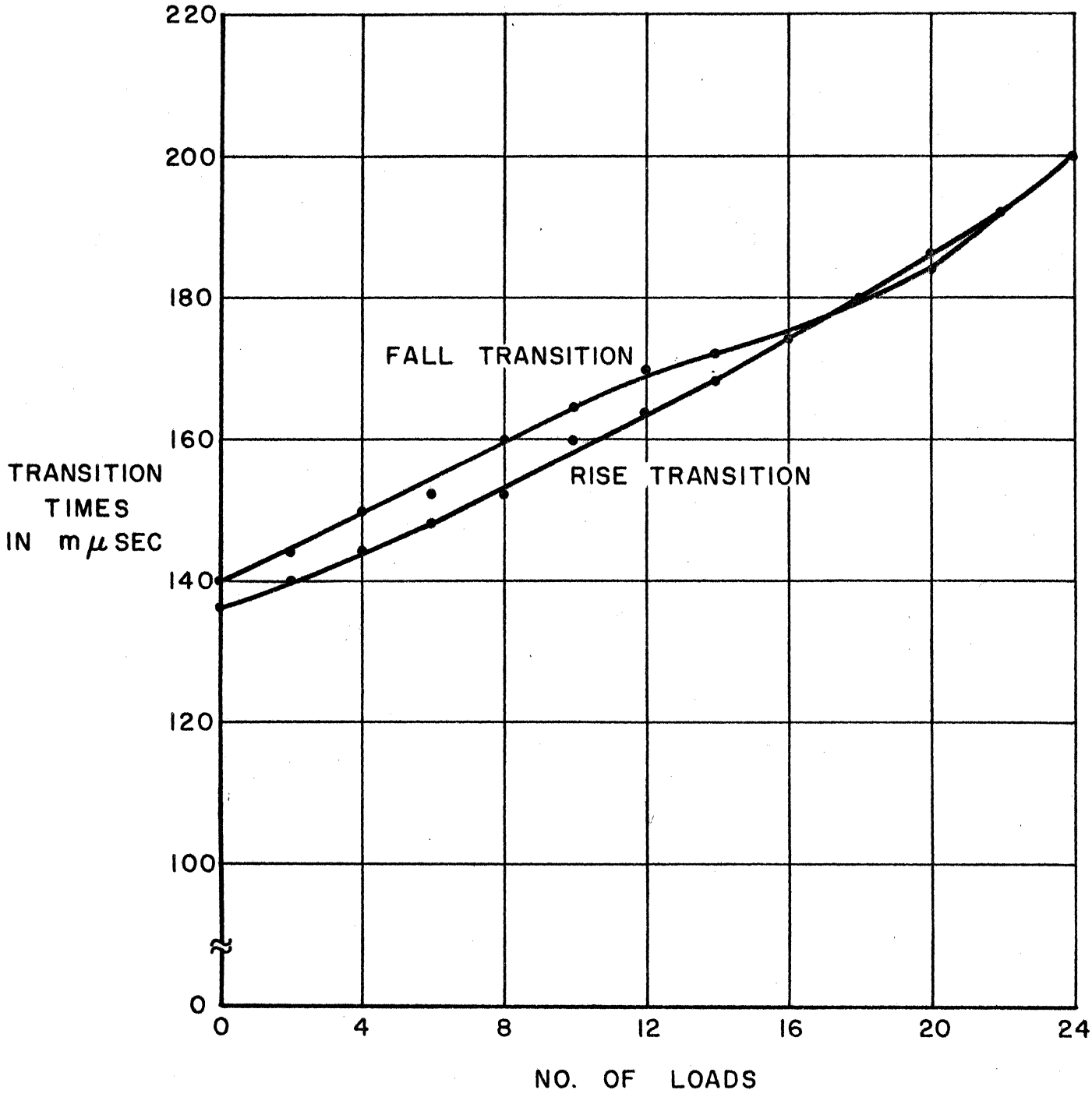


FIG. 13

HIGH SPEED FLIP-FLOP

TRANSITION TIMES vs NUMBER OF INVERTER BASES BEING DRIVEN

A-84969

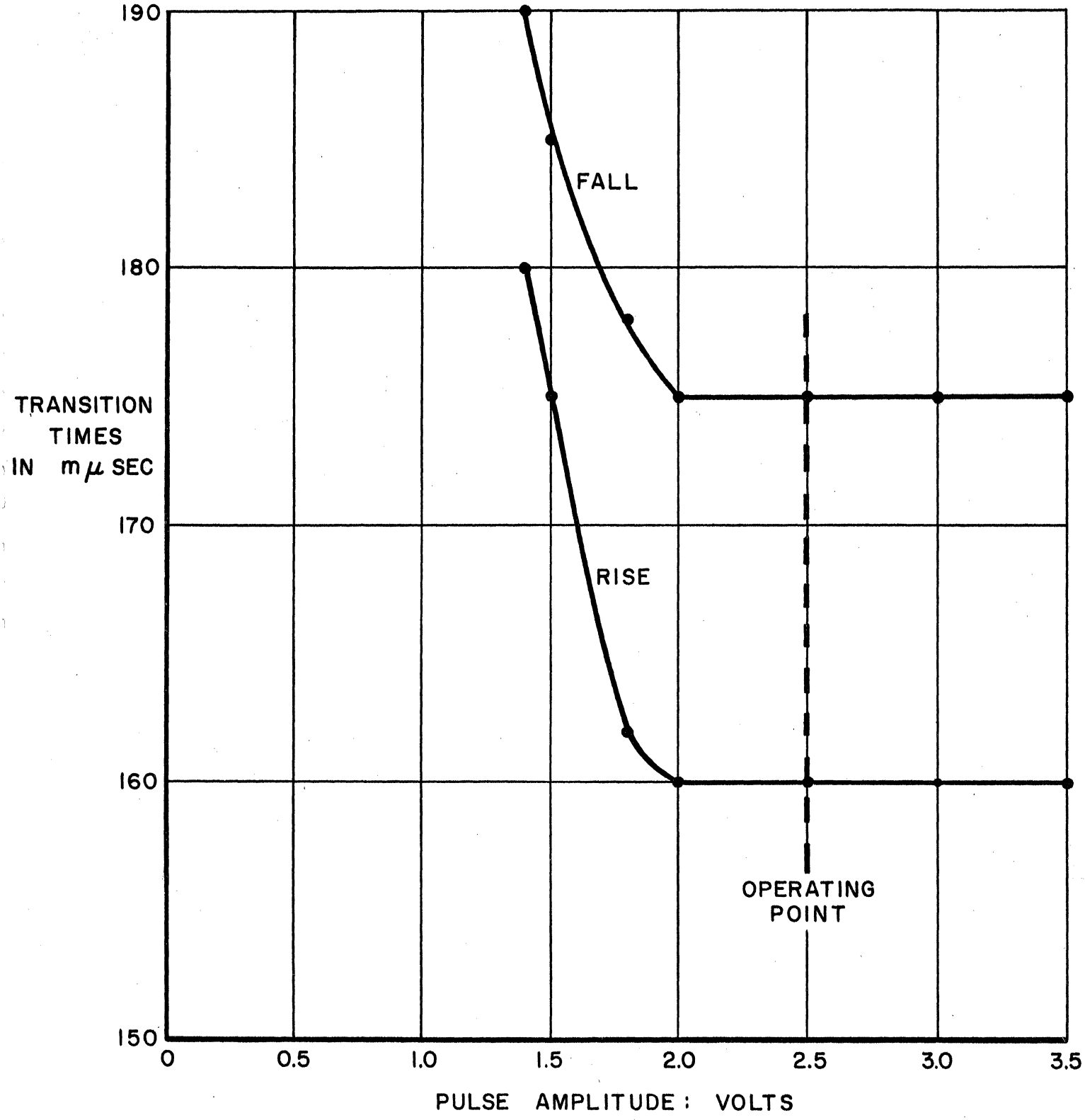


FIG. 14

HIGH SPEED FLIP-FLOP

TRANSITION TIMES vs PULSE AMPLITUDE TO COMPLEMENT

A-84971

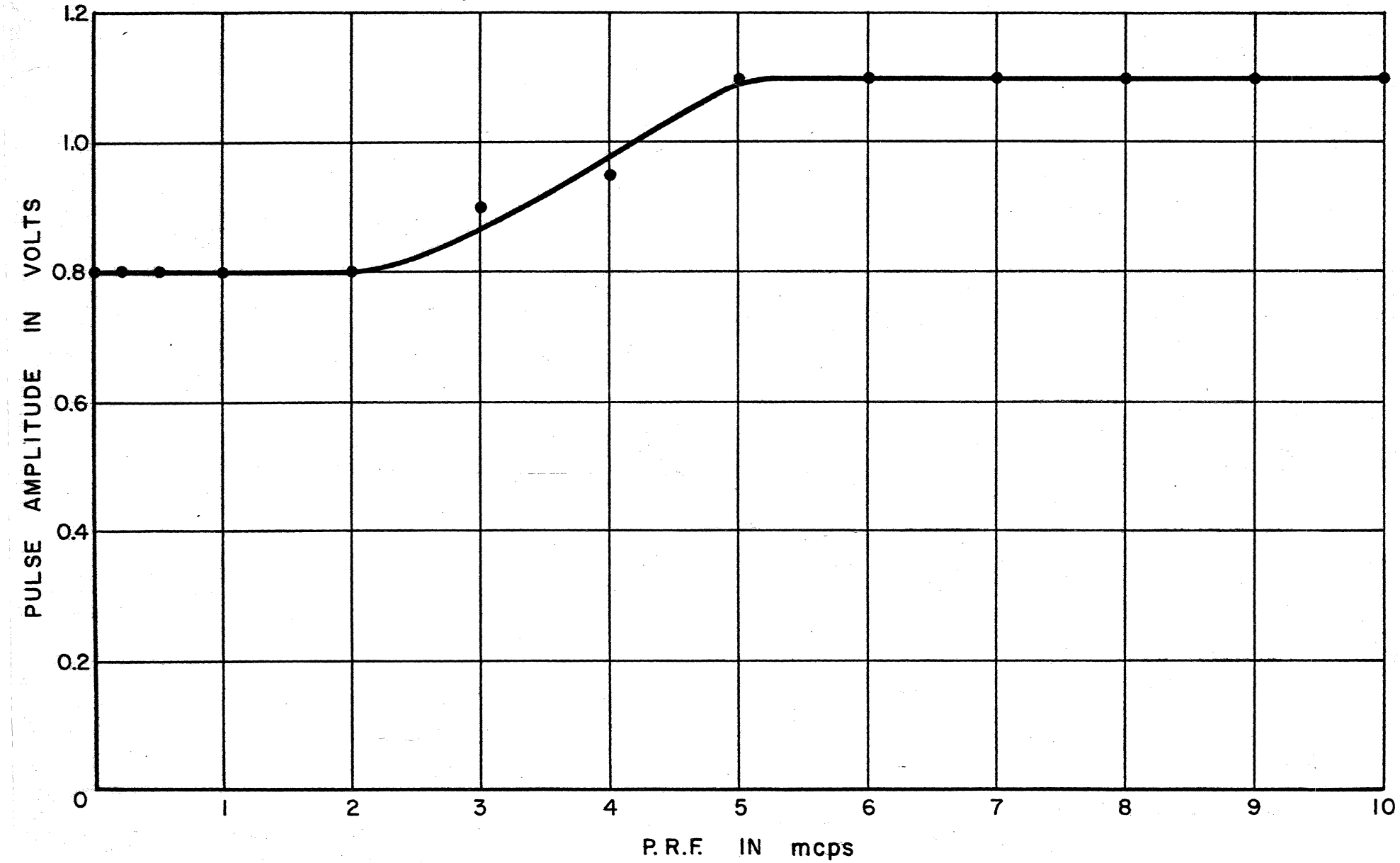


FIG. 15

HIGH SPEED FLIP-FLOP

MINIMUM AMPLITUDE TO COMPLEMENT VS P.R.F.

Marginal checking of all the high speed circuitry in TX-2 is done by varying the +10 voltage on the base of the inverter transistors. Increasing this positive bias effectively reduces the negative base current and tends to make the transistor come out of saturation. Reducing the positive bias supply tends to allow the transistor to conduct when it should be held off, and increases the fall transition time. Emitter followers are not directly marginal checked. The flip-flop has two marginal checking lines, so that when one line is varied and the other is held at fixed +10 volts the flip-flop becomes unbalanced and will fail at a certain point. The minimum acceptance margin on inverters is $\pm$10 volts either side of the +10 volt supply. The minimum margin on flip-flops is -8 and +10V, and that on register drivers is -5 and +10V.

Marginal checking curves for the following circuit parameters appear in Figures 16 and 17:

Voltage Margins vs. pulse amplitude.

Voltage Margins vs. prf.

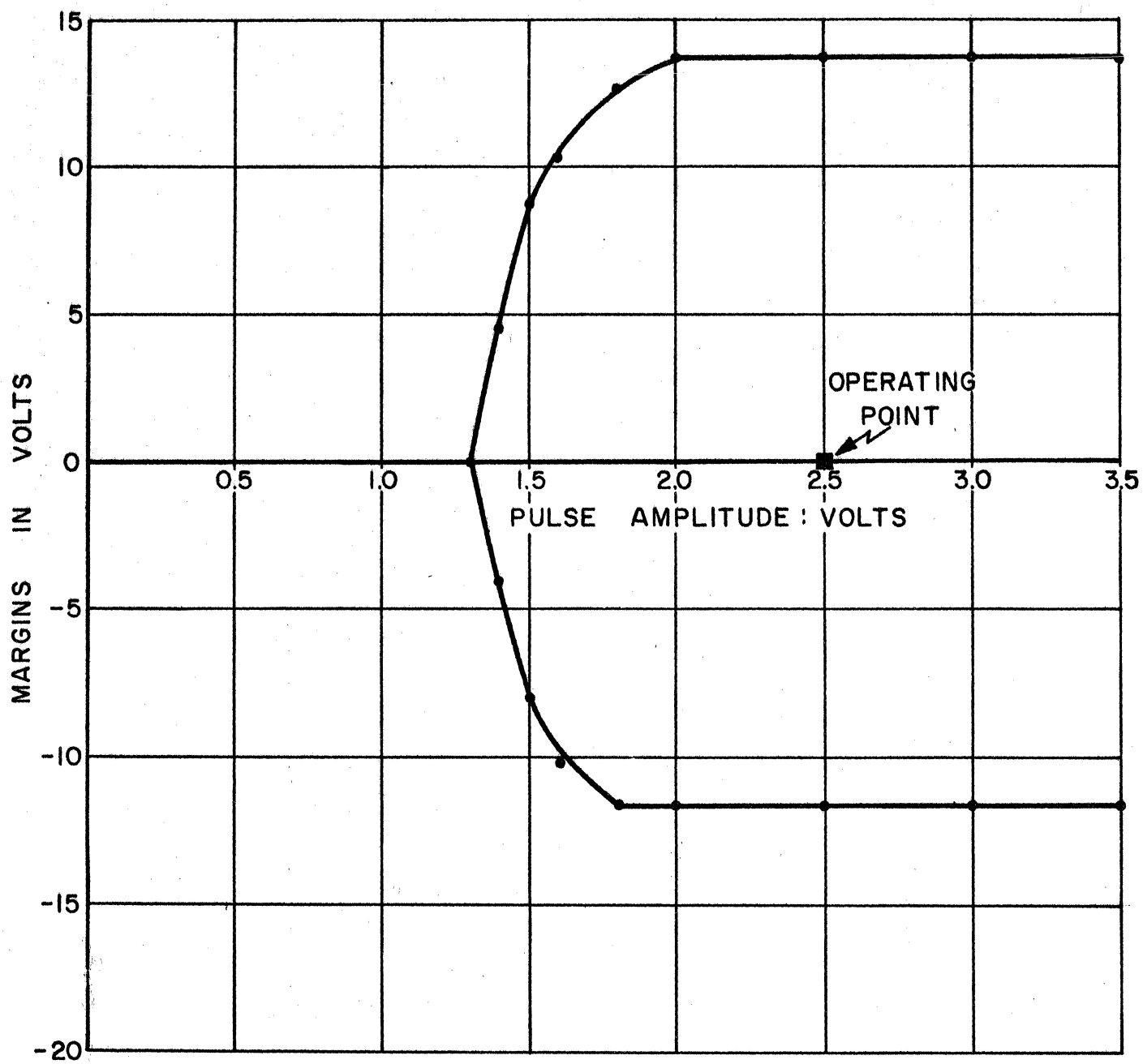


FIG. 16

HIGH SPEED FLIP-FLOP

MARGINS vs MINIMUM PULSE AMPLITUDE TO COMPLEMENT

A-84970

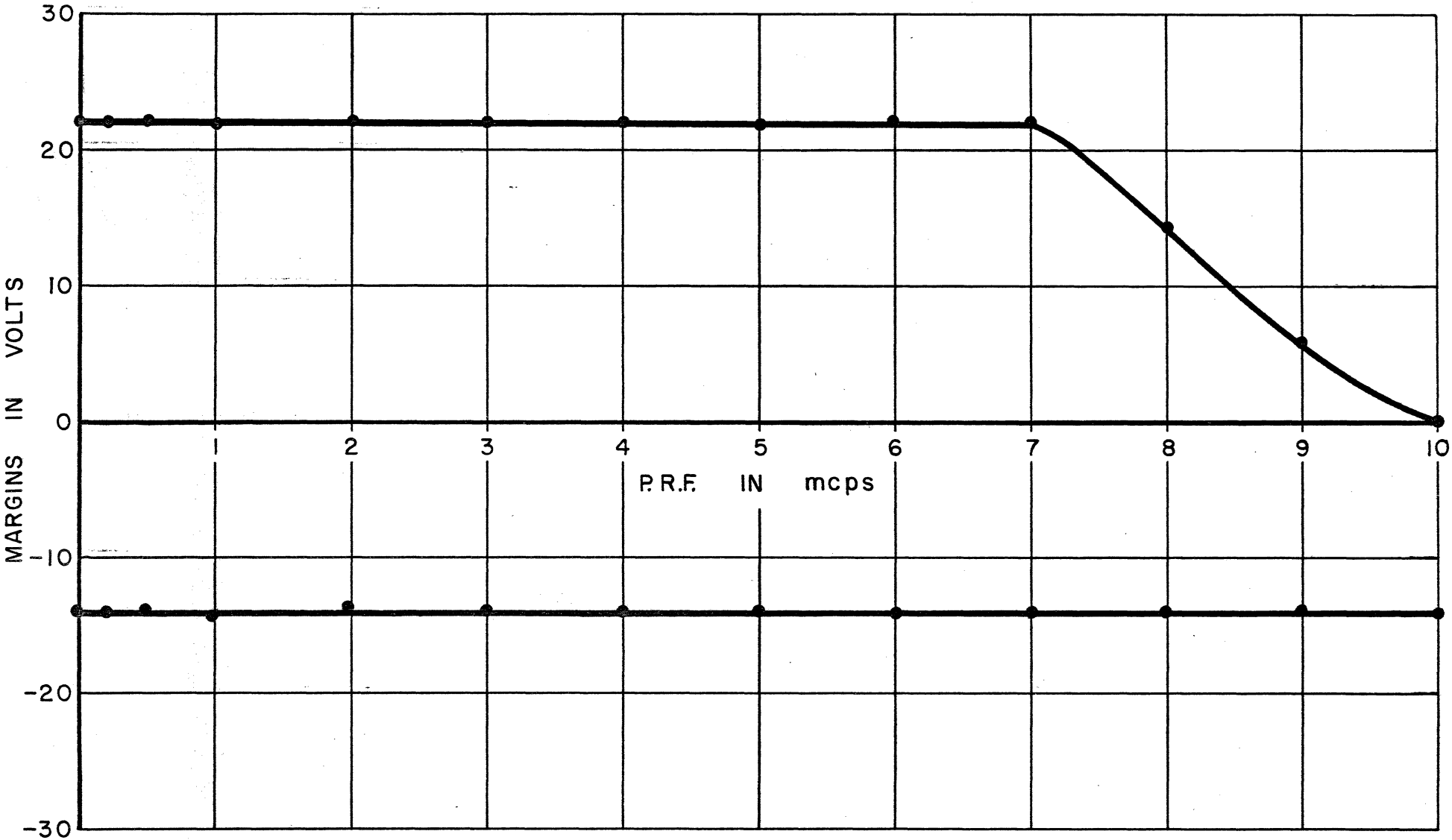


FIG. 17

HIGH SPEED FLIP-FLOP

MARGINS vs P.R.F.

S-8RA (No. 46) is a special plug-in unit used only in the carry circuit in the X-adder. In logic and lay-out it is identical to the S-8R, which consists of 8 inverters and two load resistances. However, in the S-8RA, Q_1, Q_2, and Q_3 are replaced by L-5134 transistors. Q_4 is a type 2N501, the high frequency Philco micro-alloy diffused-base transistor. R_9 is a 1000 ohm load resistor for these transistors. The A version reduces the delay time of the conventional carry circuit which caused poor margins and slowed up the operation of the X-memory. The A circuit is faster in two ways: Q_4 is the only transistor which is actually in the carry chain, and the fast response time of the 2N501 saves a considerable amount of delay time over 18 digits. By increasing the load current from 4.2 ma to 10 ma, it is possible to charge the stray capacitance faster, and to further reduce the delay. The result is that the carry time for the X-adder circuit is 0.42 μsec for 18 digits, which is about 23 mμsec per stage.

Power Protector (No. 22) prevents either over-voltage or the wrong polarity voltage from being applied to the transistors through the voltage distribution system. The power protector unit is connected between the appropriate voltage line and ground. If the voltage on this line exceeds the specified limit, the Zener diode will conduct and cause the power transistor* to conduct heavily. So much current will be conducted through this transistor that the circuit breaker on the line will trip and remove all power from the computer.

Specifications

Nominal Supply	Protection Limits
-3 volts:	at -4.0 volts, current less than 50 ma
	at -5.5 volts, current greater than 10 amps
	at +2.0 volts, current greater than 10 amps
-10 volts:	at -11 volts, current less than 50 ma
	at -15 volts, current greater than 10 amps
	at +2 volts, current greater than 10 amps
+10 volts:	at +11 volts, current less than 50 ma
	at +15 volts, current greater than 10 amps
	at -2 volts, current greater than 10 amps

* Delco 2N174

Variable Delay Units. A .1 μsec negative pulse applied to the variable delay unit (No. 23) will provide a -3 volt output level for a period continuously variable from .3 μsec to 2.2 sec. Five coarse ranges are obtained by prewiring the socket for the unit, and fine adjustments are made with the potentiometer* within the unit. The maximum output currents are 15 ma at -3 volts, and 6 ma at ground. The end of the delay can be made to occur synchronously with a clock pulse by the use of an added inverter P-5 unit (No. 04). With the variable delay auxiliary unit (No. 51), it is possible for the output of a decoder network to choose any one of four values of delay within any one particular range. It is possible to obtain a delay which will last for a given time after the last of a series of input pulses if two variable delay units are used along with the variable delay coupling unit (No. 49). (The same coupling unit may also be used when triggering one variable delay unit from another.) The input to the delay unit may be a negative 2.5 volt, 0.1 μsec pulse, or a negative-going level which is at least 20% shorter than the maximum desired delay time. An input pulse current of approximately 2.5 ma is required for triggering.

For normal asynchronous operation, pin J is connected to pin D, and pin N is connected to pin L. The capacitance is selected according to the delay range desired. The delays available, the proper pin connections, and the necessary recovery time (constant for any given capacitance) are given below:

* Bourns TrimR, 132-7-E100,000

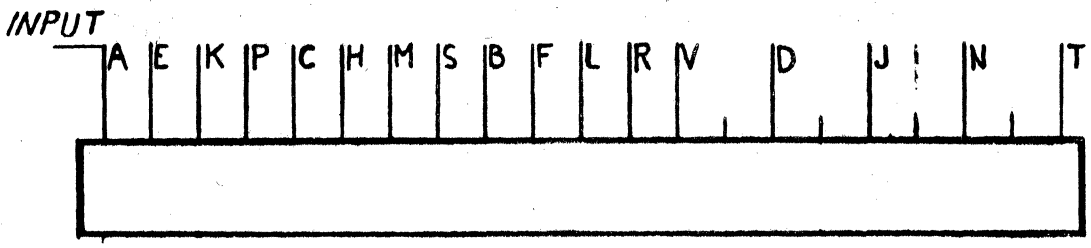
VARIABLE DELAY UNIT (Cont.)

Pos.	Capacitance μfd.	Pin Connection	Minimum Delay	Maximum Delay	Recovery Time
1	.00047	N-L	0.3 μsec	6.0 μsec	0.2 μsec
2	.01	N-L-F	1.7 μsec	110 μsec	0.5 μsec
3	.22	N-L-H	34 μsec	2.4 msec	5.0 μsec
4	6.8	N-L-M	1.0 msec	80 msec	130 μsec
5	180	N-L-R	26 msec	2.2 sec	8 msec

For $t > .5$ μseconds the delay as a function of capacitance is given approximately by $.14C < t < 12C$, where C is the capacitance in μfd. and t is the length of delay in milliseconds. For longer delays than are available from the capacitances within the unit, added capacitance may be connected between pin L and the -3 volt supply.

The operation and uses of the variable delay unit (No. 23), variable delay auxiliary unit (No. 51), and variable delay coupling unit (No. 49) are completely described in 6M-5216, S1; the original design of the delay unit is described in 6M-5216.

Delay Lines. Three separate delay lines are used in TX-2 for memory control timing. One is a .15 μsec, 50 ohm line, (No. 57) used for controlling the timing of the strobe pulses for the S-memory. This is a 20 section line using coils* and separate capacitors. Either end of the delay line can be used as the input. Reference to the figure below will show that any delay between 0 and .15 μsec can be obtained in steps of 7.5 mμsec. The end of the delay line should be terminated with 50 ohms; no termination is used at any of the taps. The maximum load at any tap is one inverter base.



The second, the inhibit level delay line (No. 48), is used to control the timing of the inhibit levels for the S-memory, and is also a 20 section tapped line. However, certain capacitors have values which compensate for the stray capacitance of the computer wiring at the output taps. Consequently this is a special delay line which can be used only for the stated purpose. The nominal total delay time of this line is .15 μsec; the taps are 7.5 mμsec apart; the nominal impedance level is 220 ohms. Consequently the end of the line should be terminated with 220 ohms.

* Coils manufactured by R.D. Brew Company

The third is a .4 μsec, 75 ohm delay line (No. 58), used to control the timing of the pulses for the memory control flip-flops. This is a 40 section line using capacitors and Brew coils. Any delay between 0 and .4 μsec can be obtained in steps of 20 mμsec, depending on the selected output tap and on the end which is used for the input. The line should be terminated with 75 ohms.

Gated Pulse Amplifier (No. 56) is a two-stage transformer-coupled amplifier for 0.1 μsec 3 volt negative pulses. In TX-2 this unit is used primarily for amplification after a pulse has gone through a delay line. The input transistor is an L-5122 and may be gated in series at the emitter or in parallel at the collector by conventional TX-2 circuitry. The output 2N501 transistor is capable of driving 10 bases and a 100 ohm termination with a 3 volt pulse. The input looks like a single pulsed base. The maximum prf of this pulse amplifier is 2.5 mcps. The transfer characteristics, and a full description of the design and use of this circuit are given in 6M-5590.

INDEX MEMORY

A complete description of the index memory (X-memory) is given in 6M-4968, "The Lincoln TX-2 Computer". At the time that these circuits were designed, the only high speed transistor available was the L-5122,* with its low current gain and 6 volt emitter-collector voltage limit. For higher voltages, the best choice was the 2N123** which has an 8 mcps alpha cut-off. The index memory circuits have since been redesigned to use the better transistors which have recently become available. Fewer transistors and lower driving currents are needed for these new circuits. These faster circuits also eliminate vacuum tubes and their associated power supplies. The memory cycle time has been decreased from 4.0 μsec to 3.6 μsec, and the access time has been decreased from 0.8 μsec to 0.6 μsec.

The L-5134* has approximately the speed of the L-5122, but has a much higher current gain at high collector current levels. The 2N501* has a 15 volt emitter-collector voltage limit, is considerably faster than the L-5122, and has a 35 mw maximum dissipation limit. The L-5432* is essentially equivalent to the type 2N501, except that it has a 30 volt rating and 150 mw dissipation limit. The 2N580*** transistor is somewhat faster and has a considerably higher current gain at high currents than the original type 2N123.

The read driver (No. 19) has undergone significant change. The present circuit consists of two L-5432 transistors. These transistors are used because they are fast and have a high beta at pulse currents of over 100 ma. Even when operated at conservative loads they have sufficient voltage and power capabilities to drive the memory. A ground level at the input causes a READ pulse by cutting off Q_1, which saturates Q_2. Q_2 is an emitter follower which, when saturated, passes the 117 ma negative READ pulse.

* Philco

** General Electric

*** RCA

INDEX MEMORY (Cont.)

The write driver (No. 21) has been changed by replacing the 2N123 transistors with types 2N501 and L-5134 to save 0.4 μsec in the WRITE time.

Important changes have also been made in the read amplifier and digit driver (No. 16). The first two transistors of the read amplifier part (i.e., the sense amplifier) were changed from L-5122 to L-5134. The digit driver part, which previously consisted of two 2N123 transistors, is now made up of two NPN type 2N635* transistors. These transistors provide a faster digit driver than that of the original system and one that incorporates more current gain.

In the select circuit first level (No. 17) and the select circuit second level (No. 18) all L-5122 inverters have been replaced by L-5134 inverters, and the 2N123 transistors have been replaced by the 2N580 type which are somewhat faster and have largercurrent gain. These changes have reduced the driving current requirements and increased the operating margins of the system with respect to both current drive and timing.

* General Electric

DISPLAY SYSTEM

General

The display decoder (digital-to-analog converter) PIU's are used as part of a high speed electrostatic display system. While the two stage decoder (No. 26), four stage decoder (No. 27), and focus decoder (No. 29), PIU's may have fairly general use, the position decoder (No. 28) (more properly the decoder position stage), the decoder gain section (No. 30), and the decoder power unit (No. 31) are quite specialized and can be explained best with reference to the decoder schematic shown in Figure 18.

Figure 19 outlines the general principles of the display position decoder. Each bit of the decoder requires a switch in series with a current source adjusted to a negative power of two corresponding to its digit significance. Since the one's complement number system is used, the sign bit is adjusted to equal the sum of the currents in all the other stages.

To illustrate, a given positive number set into the switches causes an unbalance in the currents flowing to the "one" and "zero" outputs. The equivalent negative number is obtained by reversing all switches, i.e., by complementing the input. The new current unbalance is the same except that the signal previously flowing through the "one" output now appears at the "zero" output and vice versa. Since the deflection plates of the cathode ray tube sense the difference signal, the deflection for the negative number is equal in magnitude to, but opposite in direction to that of the positive number.

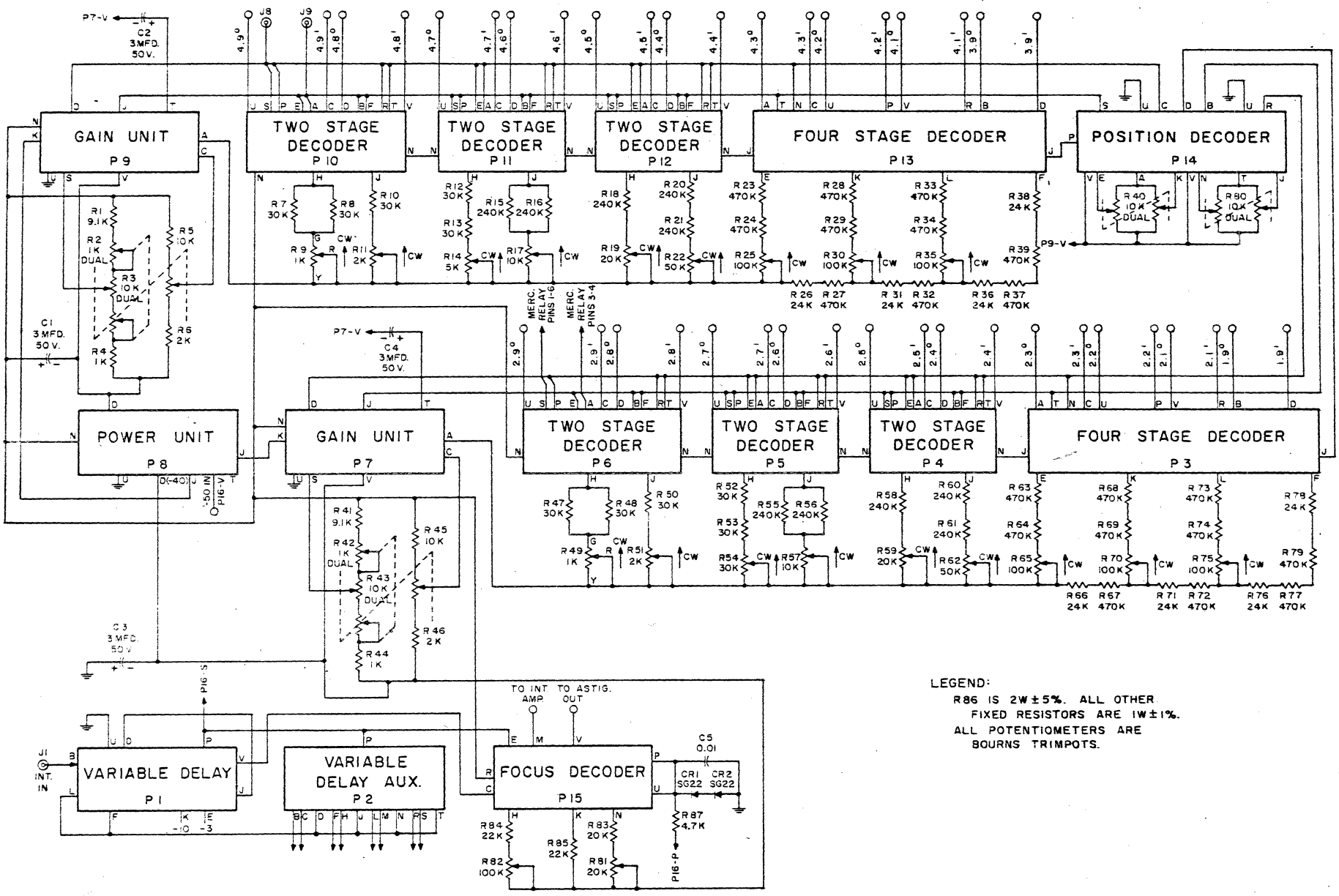


FIG. 18

SCHEMATIC – DISPLAY DECODER TX-2

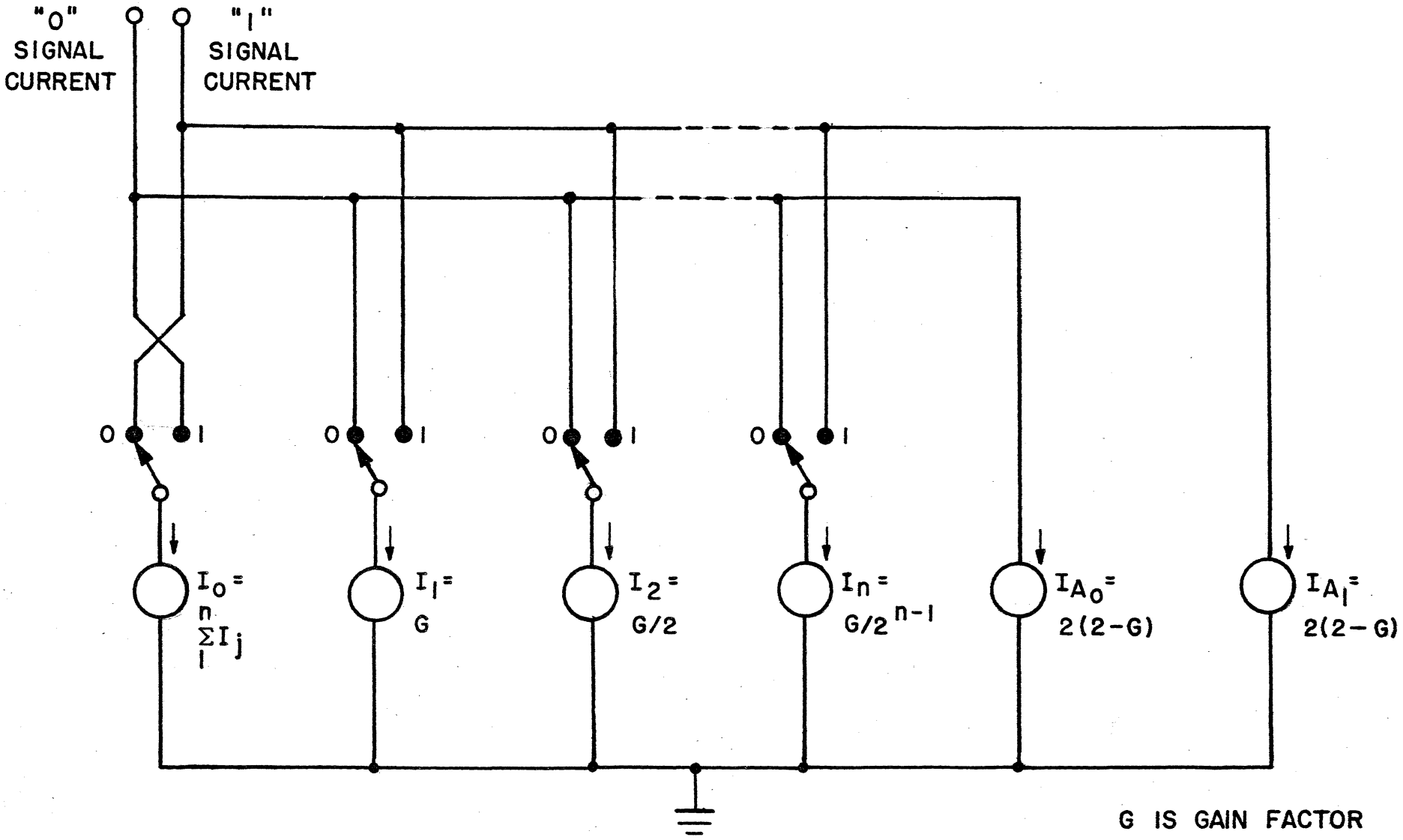


FIG. 19

WEIGHTED CURRENT DECODER

The two stages at the right of Figure 20 [included in the decoder gain section PIU (No. 30)] have no switches. They set the lower voltage point of the deflection amplifier. If they were not present, an amplifier with minimum signal would tend to go to zero volts and, of course, saturate. These switchless stages also help provide a satisfactory gain control. Any gain control which changes either the total current of all current sources or the gain of the amplifier itself also shifts the average or common mode voltage of the deflection plates, and destroys the astigmatism adjustment. Any maladjustment of the astigmatism setting in turn degrades the spot size. To circumvent this problem, gain reduction is accomplished by reducing the current in the digit sources and increasing, by the same amount, the current in the non-digit sources. Thus, a constant total current flowing to the amplifiers is maintained.

The power for the decoder is separate from the d-c supplies for the central computer to prevent modulation of the decoder by the computer program. A constant — voltage transformer eliminates the effects of variations in the a-c input and maintains a stable -50 volt supply to the decoder. Since the decoder load does not vary, no load regulation is required. The actual voltages used by the decoder are obtained by special internal supplies in the decoder power and gain PIU's.

Four Stage Decoder (No. 27). Each stage of the decoder consists of a current source transistor in series with a two-position switch. The current through any one stage is determined largely by the emitter current at pins E,K,L or F. This is determined, in turn, largely by an external resistance, by the PD reference voltage, and by the output of the decoder gain section (No. 30). The voltage difference between these two supplies is variable from about 15 to 30 volts. The current out of the first stage current source, I_{cs}, will then be

$$\left(\frac{15}{R_e}\right)\left(\bar{\alpha}_3 \text{ min.}\right) < I_{cs} < \left(\frac{30}{R_e}\right)\left(\bar{\alpha}_3 \text{ max.}\right) .$$

R_e is the external resistor, $\bar{\alpha}_3$ is the average or d-c common-base current gain of Q_3, and subscripts min and max refer to lowest end-of-life conditions and highest initial values respectively.

If pin A is at ground and pin C is at -3 volts, the "0" output current signal will be

$$\bar{\alpha}_1 I_{cs} + I_{eo_2}$$

and the "1" output current from this stage will be I_{co_2}.

If pin C is set to ground and pin A to -3 volts, the current "0" output will be

$$\bar{\alpha}_2 I_{cs} + I_{eo_1}.$$

and the "1" output current will be I_{co_1}.

Since the display tube is primarily sensitive to difference signals, the differential change in current as the A-C pin terminal pair input is complemented is

$$(\bar{\alpha}_1 - \bar{\alpha}_2)\ I_{cs} + I_{eo_2} - I_{eo_1} + I_{co_2} - I_{co_1}.$$

Two Stage Decoder (No. 26) This circuit is used in the first six bits of each axis of the position decoder.

Buffer FF signals are connected to pins U and C (D and V in the second stage). The PD reference voltage is connected to pin N; pins S and P (B and F) are jumped as are E and A (R and T); the stage current is established by a resistor from pin H (J) to the decoder supply voltage output of the decoder gain section PIU.

The 100 ohm resistors in series with each collector have a dual use. They damp any resonant circuits and thus prevent oscillations and they monitor leakage currents and gains of the individual transistors.

The use of two transistors at each point of the circuit can be illustrated by discussing the current transfer of the current source of stage 1 (transistors Q_5 and Q_6). The signal into the current source is the emitter current I_{in} of Q_6 which divides between the collector and base of Q_6. $\bar{\alpha}_6$ of the current is collector output current, and $1 - \bar{\alpha}_6$ of the input current appears as Q_6 base current and thus as Q_5 emitter current.

$$I_e = I_c + I_b$$

$$I_c = \bar{\alpha}\, I_e$$

$$\therefore\ I_b = I_e\ (1 - \bar{\alpha})$$

This Q_5 emitter current also divides and thus the Q_5 collector current, which is now equal to I_{in} $(1 - \bar{\alpha}_6)$ $\bar{\alpha}_5$, is recovered as output current to the emitters of the switch. This is added to the collector current, $\bar{\alpha}_6$ I_{in}, coming directly from Q_6. Therefore the current transfer ratio is:

$$\bar{\alpha}_6 + \bar{\alpha}_5 (1 - \bar{\alpha}_6).$$

If both Q_6 and Q_5 have $\bar{\alpha}$'s of 0.98, then the transfer ratio of the pair would be 0.9996. The current transfer ratio of the switch (Q_1 and Q_2; Q_3 and Q_4) is a similar expression.

The silicon diodes in this decoder stage are used primarily to reduce leakage currents by insuring that each emitter-base diode of the off side of the switch is reverse biased. They also aid slightly in decreasing the transition time of the switch.

Focus Decoder (No. 29) contains four pairs of NPN transistors. It is a simple decoder of relatively low accuracy, suitable for such digital-to-analogue conversion purposes as driving an audio amplifier from the outputs of a flip-flop register, etc. It is used in the high speed display system for driving the intensity amplifier and the astigmatism control circuit.

Position Decoder PIU (No. 28) forms the position control stages for the X and the Y decoders. The bases of Q_6 and Q_7 are connected to the taps of a dual ganged potentiometer connected to provide opposite variations as the control is varied. This potentiometer is supplied with the PD reference voltage through an emitter follower, Q_5, and is returned to -40 volts. Thus, if the control is started with pin E at the PD reference voltage and pin K at -40 volts, Q_1 emitter current will be zero and Q_2 emitter current will be approximately 0.25 ma. As the control is varied, the "0" out current will linearly increase and the "1" out current will linearly decrease until the "0" out is now 0.25 ma and the "1" out is 0 ma. The total current is constant at all times and so the

astigmatism is not disrupted. Also, the central position of the display is unaffected by the gain control.

Decoder Gain Section PIU (No. 30) contains two series regulated power supplies (Q_1, Q_2 and Q_5; Q_3, Q_4 and Q_6) and two switchless decoder stages. The use of these latter circuits is explained in the section dealing with the general principles of the decoder.

Supply voltages for pins C and S can be varied by the gain control -- a cross-coupled dual potentiometer located between the -40 volt supply and the PD reference voltage. Thus, as the voltage at C increases by one volt, the voltage at S decreases by one volt.

Q_1 and Q_2 form a difference amplifier. Q_2 modulates the base current of Q_5 and thus varies the current available to the load connected to pin A (the other terminal of the load is, and must be, connected to a more positive potential). The feedback to the base of Q_1 strives to maintain the voltage difference between A and C constant and ideally zero. The circuit is stabilized by two external capacitors -- one between pin A and -40 volts, the other between pin T and ground.

The connection to the -45 volt point provides reverse bias for the series regulator transistor and helps establish the proper operating point for the difference amplifier.

Decoder Power Unit PIU (No. 31) supplies -40 volts, the position decoder reference voltage, and -45 volt bias for the gain section power supplies from the -50 volt regulated supply.

The -40 volt supply is obtained from an emitter follower, Q_3, whose base is held at -40 volts by two double-anode Zener diodes* in series. A constant current is supplied to these diodes by Q_4 and its associated 5.4 volt Zener diode.**

The PD reference voltage supplies the bases of all the decoder current sources and, therefore, must be regulated with respect to the -40 supply rather than ground. Five 6.2 volt double-anode Zener reference diodes*** are supplied with a constant current by Q_2. The output is from an emitter follower, Q_1. The variations of the Q_1 emitter-base voltage with temperature will partially compensate for similar variations in the decoder current source transistors.

Low impedance of these voltages at higher frequencies is insured by by-passing the -40 volt supply to ground and the PD reference to the -40 volt supply.

* Hoffman, type 1N229, purchased to 20 volt ±5% specification.

** Texas Instrument, type 651C9, 5.4 volt ±5%.

*** Hoffman, type 1N429A, 6.2 volt ±5%.

INPUT-OUTPUT

Toggle Switch Storage Three different plug-in units are used in the toggle switch storage system:

TSS resistor driver (No. 39)
TSS 25 volt power supply unit (No. 41)
TSS digit detector unit (No. 40)

A complete description of the design and operation of the TX-2 toggle switch storage system is given in 6M-5661. Brief descriptions of each of its units are given below.

The TSS resistor driver (No. 39) includes two circuits, each of which uses a L-5122 inverter to drive another inverter combination of an L-5134 and a 2N123 in series. These, in turn, drive a GA-52830* emitter follower. An input current of 1.2 ma at -3 volts is required to produce an output which swings from ground to -25 volts in phase with the input. The maximum output current is 125 ma at -25 volts and 6 ma at ground. Transition times are about 1 μsec.

The TSS 25 volt power supply unit (No. 41) consists of a single H-6** emitter follower which obtains its collector voltage from the -30 volt computer supply. The base of the H-6 is biased at -25 volts and the output is taken from the emitter.

The TSS digit detector unit (No. 40) contains six separate detector circuits, each consisting of a single L-5122 inverter with a Stabistor voltage dropping diode (TS320G) in the base circuit instead of the usual resistor and capacitor. The input current required is 1 ma and the maximum output current is 2.9 ma at -3 volts. The transition times are about 0.5 μsec.

* Western Electric
** Minneapolis Honeywell

Schmidt Trigger, Mod II (No. 53) This circuit provides an output between ground and -3 volts that is independent of the rise and fall times of the input. The output level is inverted with respect to the input. The circuit triggers when a rising input reaches -0.9 volts, and the output falls in less than 0.15 μsec. It also triggers when a falling input reaches -2.2 volts, and the output then rises in less than 0.1 μsec.

There are two identical circuits per plug-in unit, with independent inputs and outputs. Each circuit consists of the trigger circuit itself made up of two NPN 2N357* transistors, and an L-5134 inverter amplifier. With the required input current of 0.5 ma, the maximum output current from the inverter is 15 ma at both ground and -3 volts. This is enough to drive a cable through the 82 ohm series resistance which is provided. A filter network with a time constant of 2.2 millisec is also available within the unit. For the first circuit, filtering is obtained by feeding the signal into pin S, and connecting pin R to the normal input at pin T. The normal output is obtained from pin V, and the cable driver output from pin N. The filtering for the second circuit is similar.

* General Transistor

PETR Amplifier (No. 54) amplifies the signal from the photo diode* in the photo-electric tape reader. A negative input signal is required, and the sensitivity can be adjusted by varying the 500K Trimpot** potentiometer included in the unit. The output is a signal which swings from ground to -3 volts in phase with the input. The maximum output current is 2 ma in the ground state and 3 ma at -3 volts. The maximum transition time for both rise and fall is 5 μsec. There are two identical amplifier circuits per plug-in unit, with independent inputs and outputs.

* Sylvania 1N77B.

** Bourns Trimpot, 120-15-500,000

Solenoid Driver (No. 38) and Electric Typewriter Circuitry The power to drive the solenoids in the IBM Electric Typewriter for TX-2 output is obtained from H-6 transistors. The solenoid driver unit contains two 2N241 inverters, each of which drives one H-6 inverter. Load resistors for the H-6 inverters are external to the unit and are connected to -30 volts. (The coil of a solenoid itself may constitute the load resistance.) The driver unit supplies a 600 ma output at a swing of ground to -30 volts from a 2 ma input swinging from ground to -3 volts. A ground level input energizes the solenoids.

The Four H-6 Unit (No. 42) contains only four H-6 transistors mounted on a heat sink with the emitter, base, and collector of each transistor brought out to separate pins. The specifications of the unit are equivalent to those of the transistor itself. The maximum collector current is 2 amps; the maximum collector-emitter voltage is 60 volts; the minimum end-of-life β is 25. Thus the input current must be equal to at least the output current divided by 25. The maximum power dissipation of the unit is not specified, but the collector junction temperature must be held to less than 80 degrees C.

The Typewriter Diode Unit (No. 44) is used for level mixing. Each unit contains two groups of 8 1N537 silicon diodes* with the cathodes within each group connected. All anodes are brought out to separate pins. The maximum current through any one diode is 750 ma, and the peak inverse voltage is 100 volts.

* General Electric

Lamp Lighter (No. 68) is an amplifier to supply current to light the 30 volt lamps on the console. This unit is identical in lay-out and pin connections to the solenoid driver (No. 38) but uses different transistors and different component values. There are two lamp lighter circuits per plug-in unit.

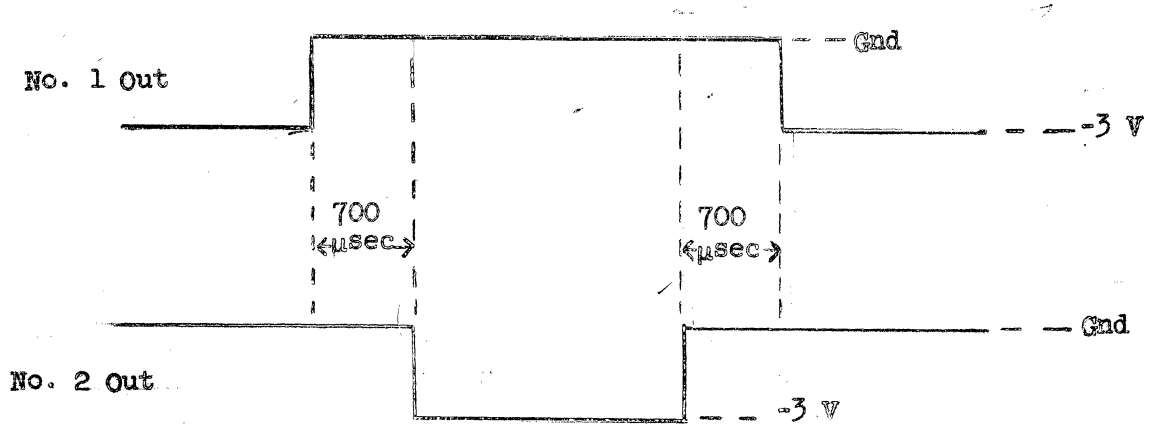
A ground level is required at the input to light the lamp; a -3 volt input level will keep the lamp off. The input current required is 0.65 ma at -3 volts and the maximum output current is 100 ma at -30 volts. The lamp is connected directly between the output and the -30 volt supply.

Mercury Relay Signal Generator (No. 50) provides several output signals under control of a single push button. From "Level Gate No. 1 Out" a level is obtained which goes from -3 volts up to ground, remains at ground as long as the button is pushed, and then returns to -3 volts.

From "Level Gate No. 2 Out", the level goes from ground to -3 volts, remains negative as long as the button is pushed, then returns to ground. The maximum level current available is 15 ma at -3 volts. For driving short lines (less than 3 feet), the level output may be taken directly from pins M or C to drive an open wire. For longer lines, a coax cable or twisted pair line should be used and the output obtained through the 82 ohm series terminating resistor from pins L or B.

From "Pulse Gate Out", a 0.1 μsec 3 volt negative pulse is obtained when the button is pushed. The pulse current is sufficient to drive a 100 ohm cable which can, in turn, drive two transistor bases. The same considerations relative to the length of line to be driven apply to pulses as well as levels. Pulse driving lines, however, must be terminated with 100 ohms for proper formation of the pulse.

It should be noted that the mercury relay contacts are of the make-before-break type. Consequently there will be a time at the beginning and end of the output level when the signal at both level output gates will be at ground. This length of time is approximately 700 μsec. Thus the level output wave-forms look like this:



The mercury relay* and the push button and associated resistor and capacitor decoupling must be mounted externally to the plug-in unit. It is essential that the decoupling shown in the circuit diagram (Figure 104 in Reference Manual) be mounted at the push button. Its purpose is to filter out the contact bounce of the push button by inserting a low-pass filter between the button and the mercury relay coil.

*Clare HG 1012

.1 μsec Pulse Former (No. 55) generates a 0.1 μsec 3 volt negative pulse from either a rising or falling input swinging between ground and -3 volts with a transition time of less than 0.2 μsec.

The pulse former requires a rising input of at least 2.4 ma at pin D to cut off Q_1 and Q_4 simultaneously. A falling input would be applied to pin N (pin J connected to Pin D) to go through the inverter Q_5, which, because of its gain, requires an input of only 1.2 ma. In either case, the output of the emitter of Q_3 is driven immediately down to -3 volts. The negative waveform travels down the lumped-constant 0.1 μsec delay line and causes Q_2 to conduct 0.1 μsec after the input is applied. When Q_2 conducts, the base of Q_3 goes back to ground and the output rises to ground. The resultant 30 ma 0.1 μsec negative pulse is enough to drive a terminated 100 ohm cable or twisted pair line.

Input Mixer (No. 45) and Input Mixer Amplifier (No. 52) The Input Mixer will mix two levels from input-output equipment in the in-out frame. There are four separate circuits per plug-in unit and each circuit has two inputs and two outputs. Each circuit consists of two pairs of transistors: the first is a PNP inverter (Q_1) in parallel with an NPN emitter follower (Q_2) with the output at pin A, and the second consists of two NPN emitter followers (Q_3 and Q_4) with the output at pin C. The input to the circuit is at pin H, and the gating input is at pin M. With pin M at -3 volts, the desired negative output appears at pin A if the input at pin H is at ground, and at pin C if the input at pin H is at -3 volts. If pin M is at ground, both outputs are at ground regardless of the input at pin H. The possibilities are summarized below:

Input Pin H	Gate Pin M	Out 1 Pin A	Out 2 Pin C
-3 v	-3 v	Gnd	negative
Gnd	-3 v	negative	Gnd
-3 v	Gnd	Gnd	Gnd
Gnd	Gnd	Gnd	Gnd

The operation of the other 3 circuits is similar. Pin M is the common gating point for inputs at pin H and pin S; pin L is the common gating point for inputs at pin N and pin F.

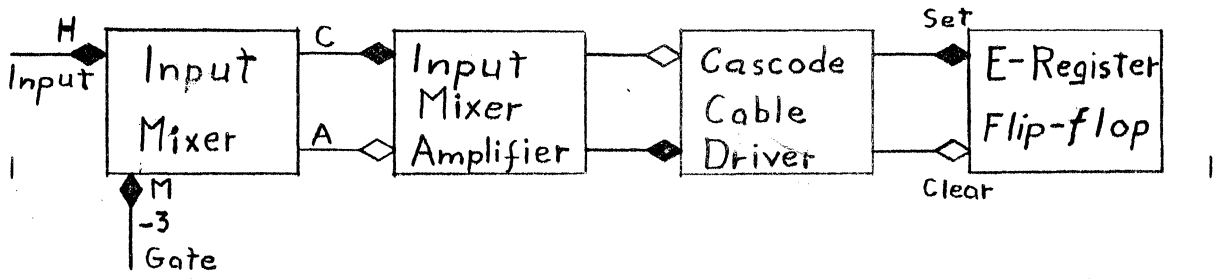
The input current required at pin H is 1.2 ma at -3 volts, and 0.5 ma at ground. The gating input current required at pin M is 2 ma. The negative output current available is 3 ma.

Input Mixer (No. 45) and Input Mixer Amplifier (No. 52) (Cont.)

The negative output signals from a number of input mixers are mixed and fed into the input mixer amplifier which contains four separate transistor inverters with a diode input for each. The input current needed for each inverter is 2 ma at -3 volts, and 1 ma at ground. The maximum output current of the input mixer amplifier is 3.6 ma at -3 volts.

When the amplifier is used in the computer, the output signal is fed through a cascode cable driver which reinverts it, and sends it out over a cable to a flip-flop in the E register of the central computer. The signal which originally came from pin C of the input mixer is used to gate a base input to the SET side of the flip-flop; the signal which originally came from pin A gates the CLEAR side of the same flip-flop. Thus, provided that the gating input at pin M of the mixer is at -3 volts, the flip-flop will be either set or cleared depending on the input at pin H. If the gating input at pin M is at ground the state of the flip-flop will not be changed.

A block diagram of this system is shown below:



IN-OUT LOGIC CIRCUITS

Introduction

The logic units to be discussed in the following part of this handbook are used in connection with the input-output equipment. The basic inverter circuitry is all a-c coupled, instead of being d-c coupled as is the high speed logic circuitry previously discussed. It is the rising transition from -3 volts up to ground which does the work. L-5134 transistors are used throughout, and the inverter output swing is clamped to -3 volts by a diode* and to ground by the transistor itself. The circuitry is designed to operate at a maximum speed of 800 kcps -- a much lower prf than that of the central computer. The time constants are such that 1.2 μsec is needed between one event and the next. Diode mixing is by capacitor-diode gates which provide logic OR gates when their outputs are in parallel.

*Clevite: CTP-592

The Capacitor-Diode Gate (No. 63) (CK) is used to form a positive pulse from a waveform which is rising from -3 volts up to ground. The required input can have a maximum rise time of 0.2 μsec. Peak input currents of 2 ma in the transition toward ground and 1 ma in the transition toward -3 volts are required. The set-up time for the gating input is 1.2 μsec. The gate is so biased that the output pulse goes from -0.6 volts up to about +2 volts with a width of approximately 0.3 μsec. Up to 10 gates may be connected in parallel to form an OR circuit. Plug-in unit No. 63 contains six such gates, with independent inputs and outputs, except that two outputs are connected in parallel at pin A. For the first circuit, the input is at pin B and the output is at pin A. Pin C is a gating point; a ground input gates the pulse on, and a -3 volt input of 1 ma prevents the pulse from being formed. The positive pulse is used to cut off the base of a transistor which is normally biased on from a negative supply. The other five circuits are similar.

.3 μsec Pulse Former Mod II (No. 60) forms a positive or negative 3 volt pulse (ground to -3 volts or -3 volts to ground) from a positive-going wave front. The negative pulse is used to trigger the variable delay unit and the high speed flip-flop; the positive pulse is used for triggering a capacitor-diode gate or the low speed dual flip-flop.

This pulse former unit consists of a capacitor-diode gate and two clamped L-5134 inverters in series. A negative pulse output is obtained from the first inverter (Q_1), the positive output from the second (Q_3). There are two identical circuits per plug-in unit with separate inputs and outputs. For the first circuit the input is at pin D, the gating point is at pin F, the negative pulse output is at pins B and V, and the positive pulse output is at pin H. Pin J is the point at which other capacitor-diode gates may be connected to form an OR circuit.

The input specifications and conditions for gating are the same as for the capacitor-diode gate (No. 63). The maximum negative pulse output current is 3 ma at -3 volts, and the maximum positive pulse output is 6.5 ma at -3 volts and 10 ma at ground. Depending on the width of the input pulse the output pulse width may vary from 0.3 to 0.4 μsec, and the rise and fall times are less than 0.2 μsec.

Output Distributor (No. 59) and Output Mixer (No. 65) These plug-in units each contain 4 L-5134 clamped inverters for logic operations associated with the in-out equipment, and to drive 93 ohm cables or twisted pair lines to and from the in-out frame. Each emitter is brought out separately so that it can be gated on by a ground level at the emitter. Each transistor of the output distributor has a load resistance plus an 82 ohm series terminating resistance for driving cables. The base inputs to Q_1 and Q_2 are common at pin A, and the inputs to Q_3 and Q_4 are common at pin B. The output mixer has all four inputs and outputs at separate pins; the one load resistor and one cable driving resistor are brought out to separate pins. Thus transistors in the output mixer may be placed in parallel with those in the output distributor.

Both distributor and mixer units require an input current of 2.2 ma at -3 volts, and 0.4 ma at ground. Output voltage levels of these units are clamped at ground and -3 volts. The maximum output current available is 2.9 ma at -3 volts, and 15 ma at ground. Thus, when driving a cable or twisted pair line through the 82 ohm resistance, the rise time at the end of the cable will be equal to the rise time of the current through the transistor (about 30 mμsec), but the fall time will be long because of the limited current available in the -3 direction. When driving RG62/U 93 ohm cable, the fall time will be approximately equal to 16 mμsec per foot of cable or a minimum of 30 mμsec.

Line Driver (No. 66) is similar to the output distributor and output mixer in that it contains four L-5134 clamped inverters, and is used in association with the in-out equipment. However, its primary use is for driving RG62/U coaxial cable or twisted pair lines. Its input and output pin connections are identical to those of the cascode and cable driver (No. 08), with four separate inputs, four direct outputs, and four outputs through 82 ohm series terminating resistances.

The input current required is 2.2 ma at -3 volts, and 0.4 ma at ground. The maximum output current available is 7 ma at -3 volts, and 10 ma at ground. Each line driver transistor will drive one cable, with a rise time of about 30 mμsec and a fall time of about 8 mμsec per foot of cable (minimum of 30 mμsec).

Dual Flip-Flop Mod II (No. 61) provides logic levels of ground and -3 volts. Every plug-in unit contains two independent flip-flops, each of which has two L-5134 RC coupled inverters (Q_1 and Q_2), two capacitor-diode gates, and two additional transistors (Q_3 and Q_4) to drive an indicator light.

Because of the 1.2 μsec set-up time of the capacitor-diode gates, the maximum prf of this flip-flop is 800 kcps. The unit may be set and cleared internally but external logic delay provided by capacitor-diode gates is required for complementing. The proper connections for complementing the flip-flop are shown in Figure 20. The output voltage is clamped at ground and at -3 volts. The maximum output current is 6.5 ma at -3 volts and 5 ma at ground.

The inputs at pin B "SET IN," and pin D "CLEAR IN," set and clear the flip-flop from a level which is rising from -3 volts to ground. These inputs are similar to those of the capacitor-diode gate except that they cannot be gated. The flip-flop may also be triggered from 0.1 μsec pulses applied through the conventional L-5122 two transistor gate, using an external 10K resistor to -10 volts and a clamp diode (CTP-592) to -3 volts. The collector of the gate is connected to pins B or D for setting or clearing. This circuit will be less sensitive than that of the high speed flip-flop and will require a minimum trigger pulse of about 2 volts.

Plots of voltage margins vs. prf and voltage margins vs. rise time of the input waveform are given in Figures 21 and 22.

Up to 10 capacitor-diode gates (No. 63) may be connected in parallel at pins A ("ONE IN") and C ("ZERO IN") as an OR gate to set or clear the flip-flop.

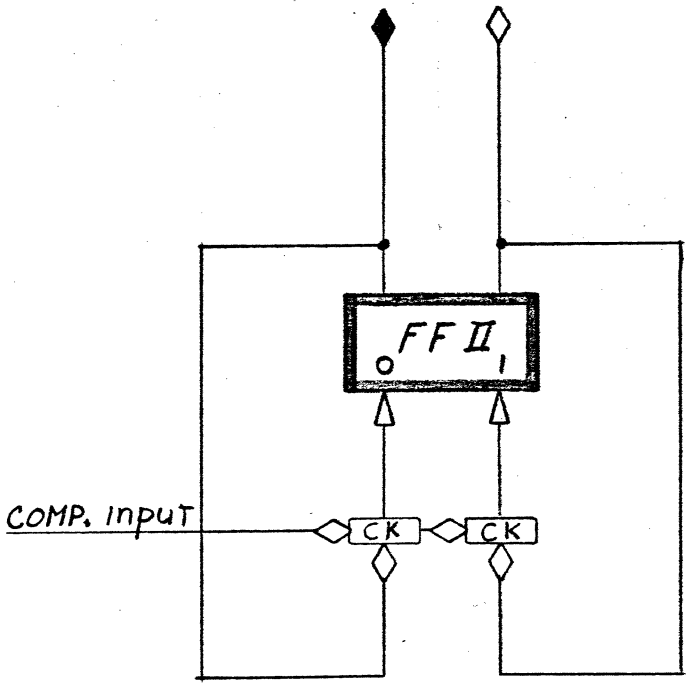


FIG. 20

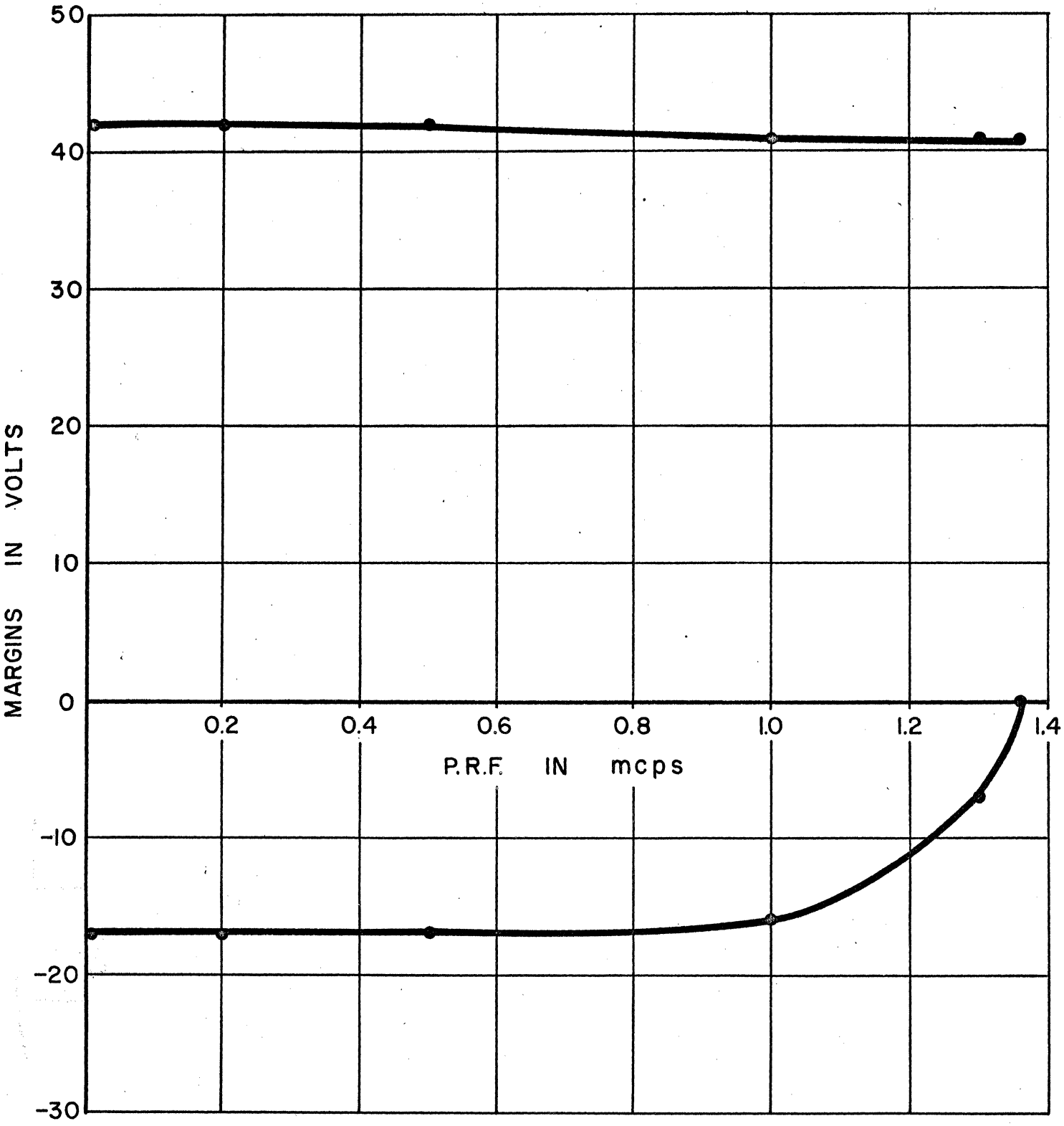


FIG. 21

DUAL FLIP-FLOP, MOD. II

MARGINS vs P.R.F.

A-84974

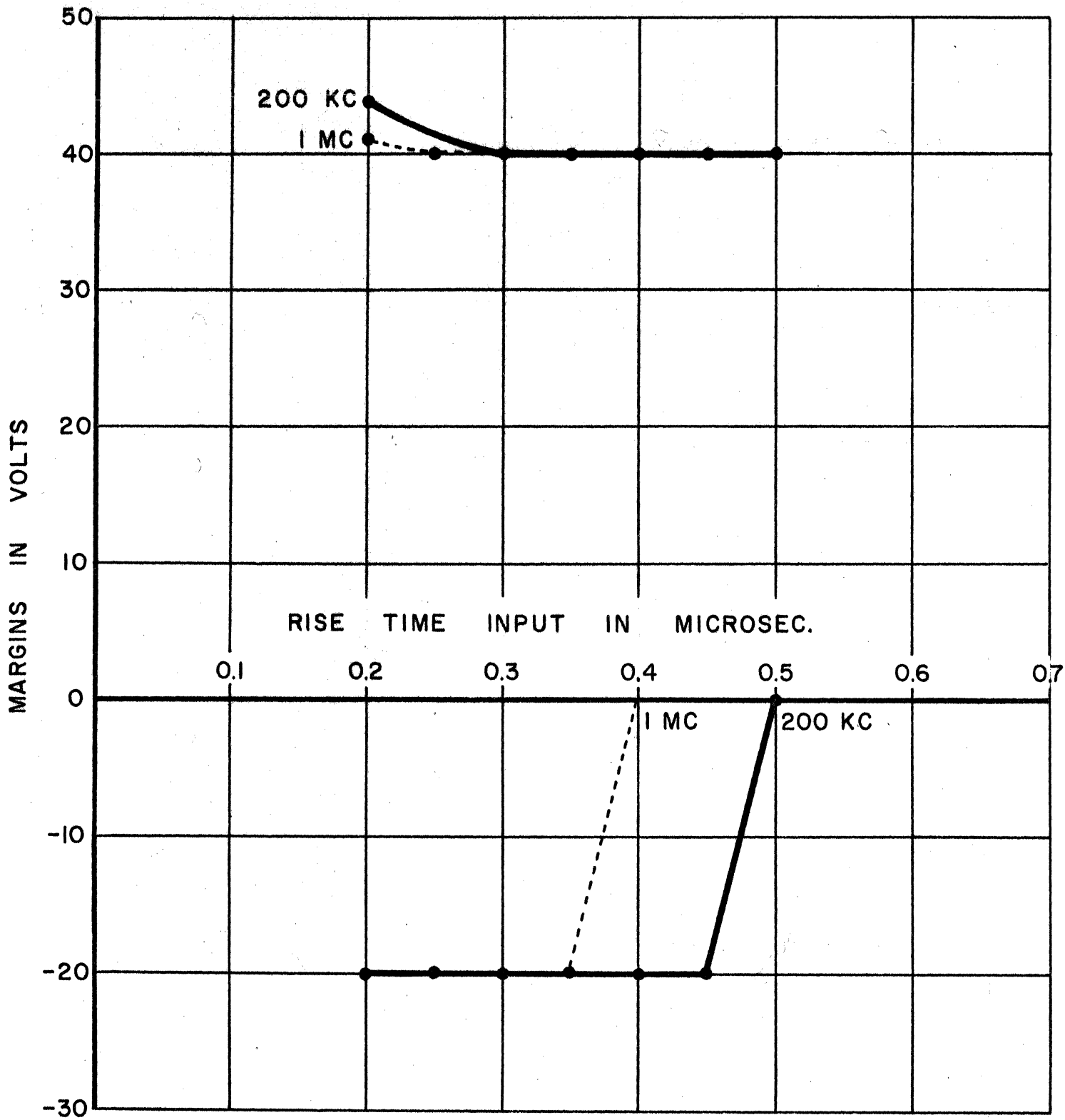


FIG. 22

DUAL FLIP-FLOP, MOD. II

MARGINS vs RISE TIME OF INPUT

A-84975

Synchronizer (No. 62) consists of one dual flip-flop Mod II (No. 61) to which is added two diodes and a resistor. Thus the synchronizer unit includes two flip-flops, four capacitor-diode gates, two mixing diodes, and a bias resistor. It synchronizes with the central computer clock asynchronous pulses or levels from in-out equipment.

In normal operation, pin J (the ZERO output of the second FF) is connected to pin N, the common gating point for the ZERO inputs. The asynchronous input comes in to pin V of the capacitor-diode gate which can be gated at pin T. The synchronous clock pulse input consists of positive levels (-3 volts up to ground) 0.4 μsec wide occurring every 1.6 μsec. The clock pulse input at pin D is applied in common to the CLEAR and SET inputs of the 2nd FF and to the CLEAR input of the 1st FF. The output of the synchronizer is usually taken from pin R, the ONE output of the 1st FF.

At the beginning of the operation both flip-flops are in the ZERO state. The asynchronous level or pulse from the in-out device sets the 1st FF to a ONE and the output at pin R goes from ground down to -3 volts. The next clock pulse sets the 2nd FF to a ONE because the capacitor-diode gates on the ZERO input sides are both gated off.

The following clock pulse clears both flip-flops to a ZERO since the ZERO input gates are now gated on by the ground level from pin J. Thus on the second clock pulse, the synchronizer output at pin R goes from -3 volts up to ground. It is this positive-going transition that is used as the synchronous output.

The input and output specifications for this unit are the same as those of the dual flip-flop Mod II (No. 61).

Relay Unit (No. 69) consists of two double-pole double-throw relays* each of which can switch a maximum of 2 amps. Each relay draws 16.5 ma through its 1825 ohm coil resistance at nominal -30 volt operation. The actual voltage required to pull in any of these relays is a maximum of -20 volts and any of them will drop out at no less than 3.5 volts.

*Clare, Type F, No. RP 7638

REFERENCE MANUAL

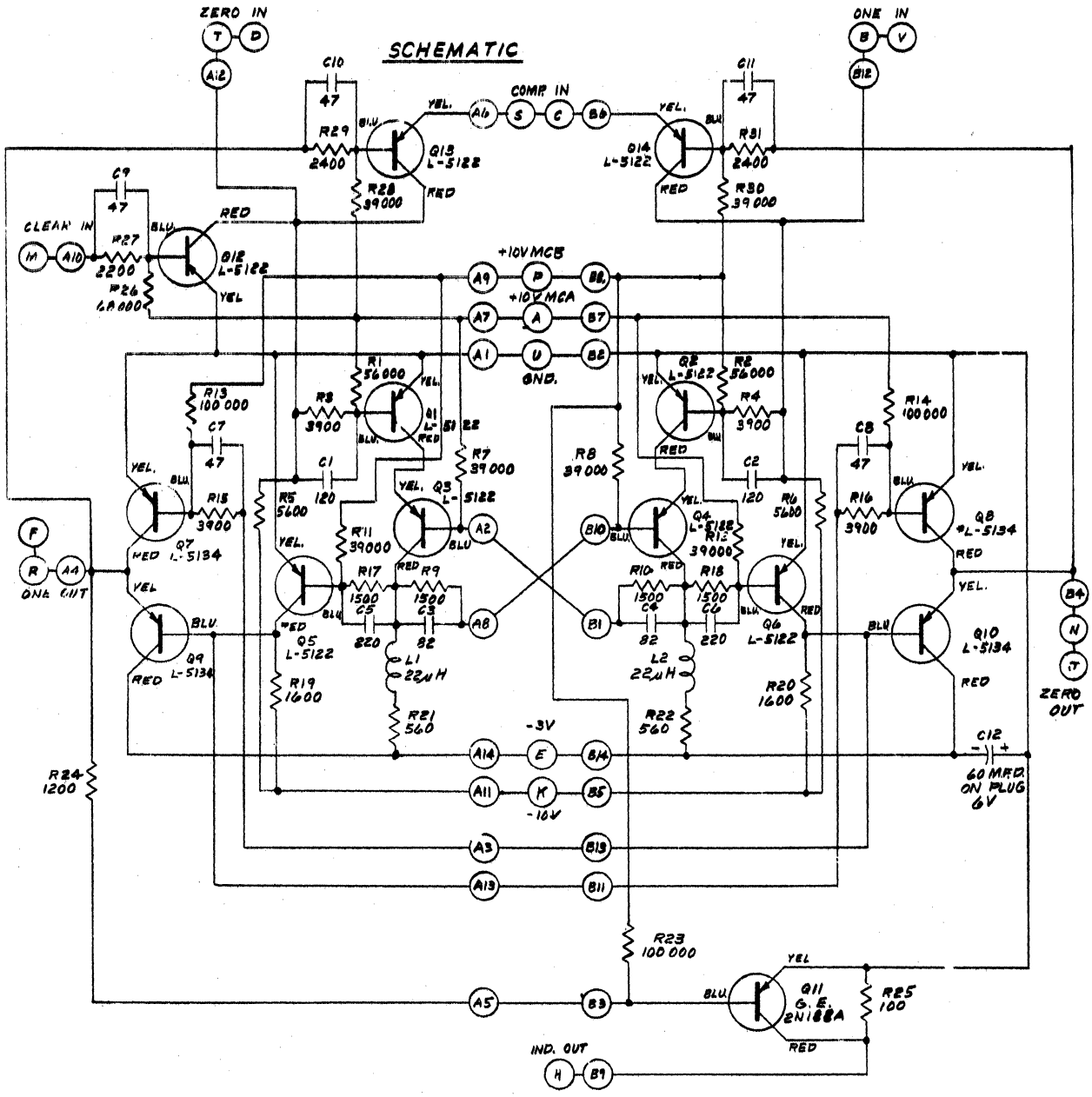


FIG. 23

HIGH - SPEED FLIP - FLOP

D-84997
"A" RED

HIGH SPEED FLIP-FLOP

Handle Color: Black Brown

Drawing Number: D-66439 (lug); D-84997 (eyelet)

PW Number: 63-580 (lug); 63-1067 (eyelet)

Transistors:* 9 L-5122; 4 L-5134; 1 2N188A

Power Supply Voltages: +10 MCA; +10 MCB; -3; -10

Use: Bistable device to provide logic levels of ground or -3 volts

Remarks: May be set, cleared, or complemented
Maximum prf: 5 mcps
Cascode output provides 30 ma output current

*All transistor type numbers are identified with manufacturer in appendix

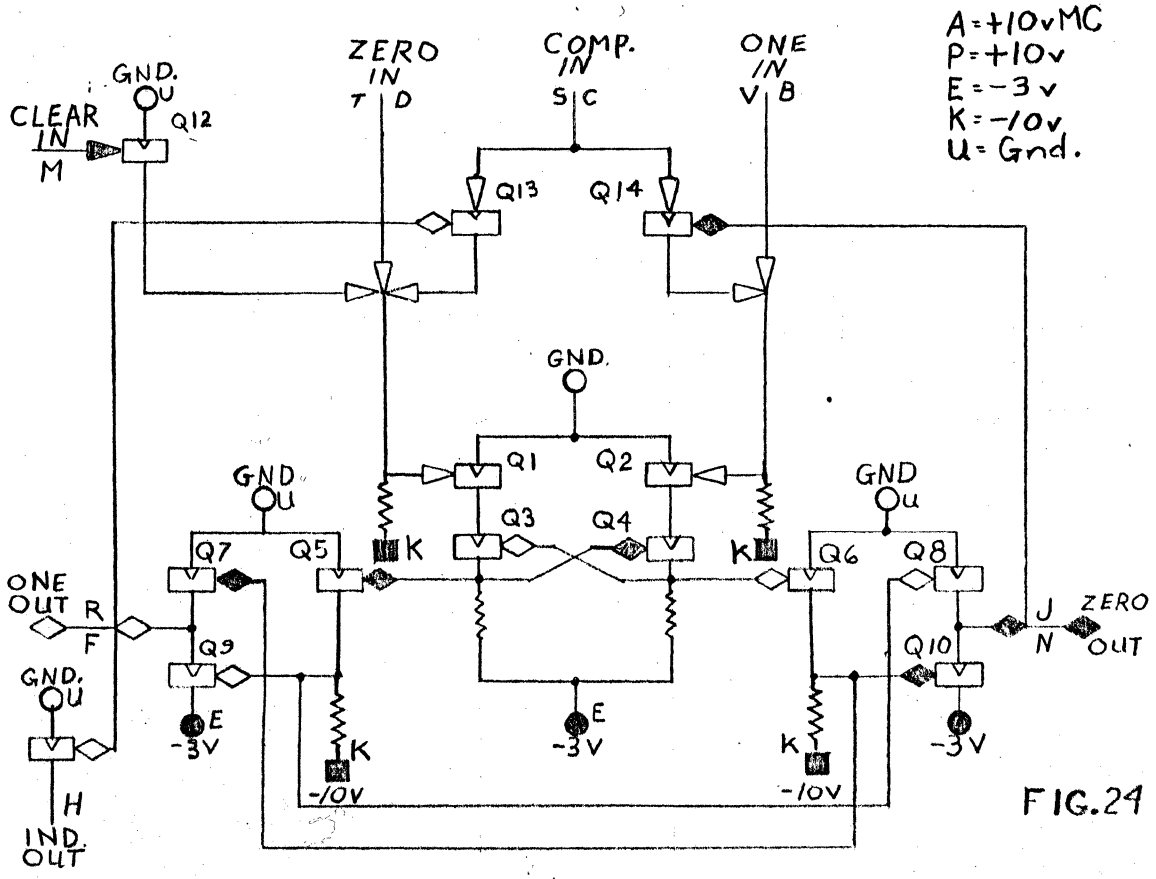
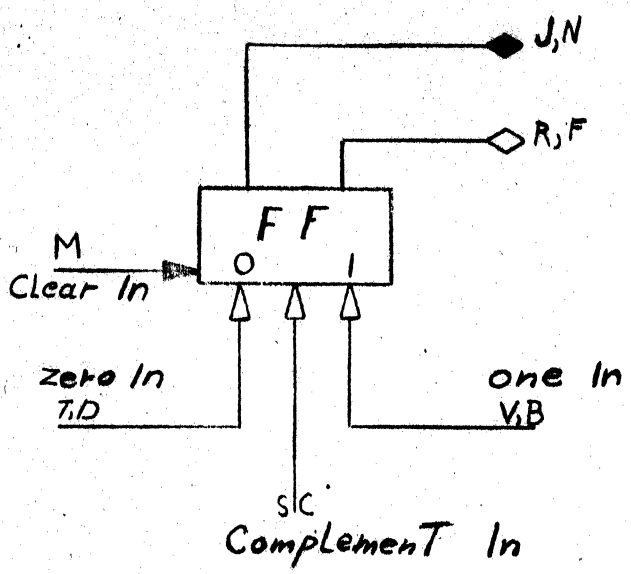


FIG.24

HIGH SPEED FLIP-FLOP

Block Symbol



A = +10v MC
P = +10v
E = -3v
K = -10v
U Gnd.

FIG. 25

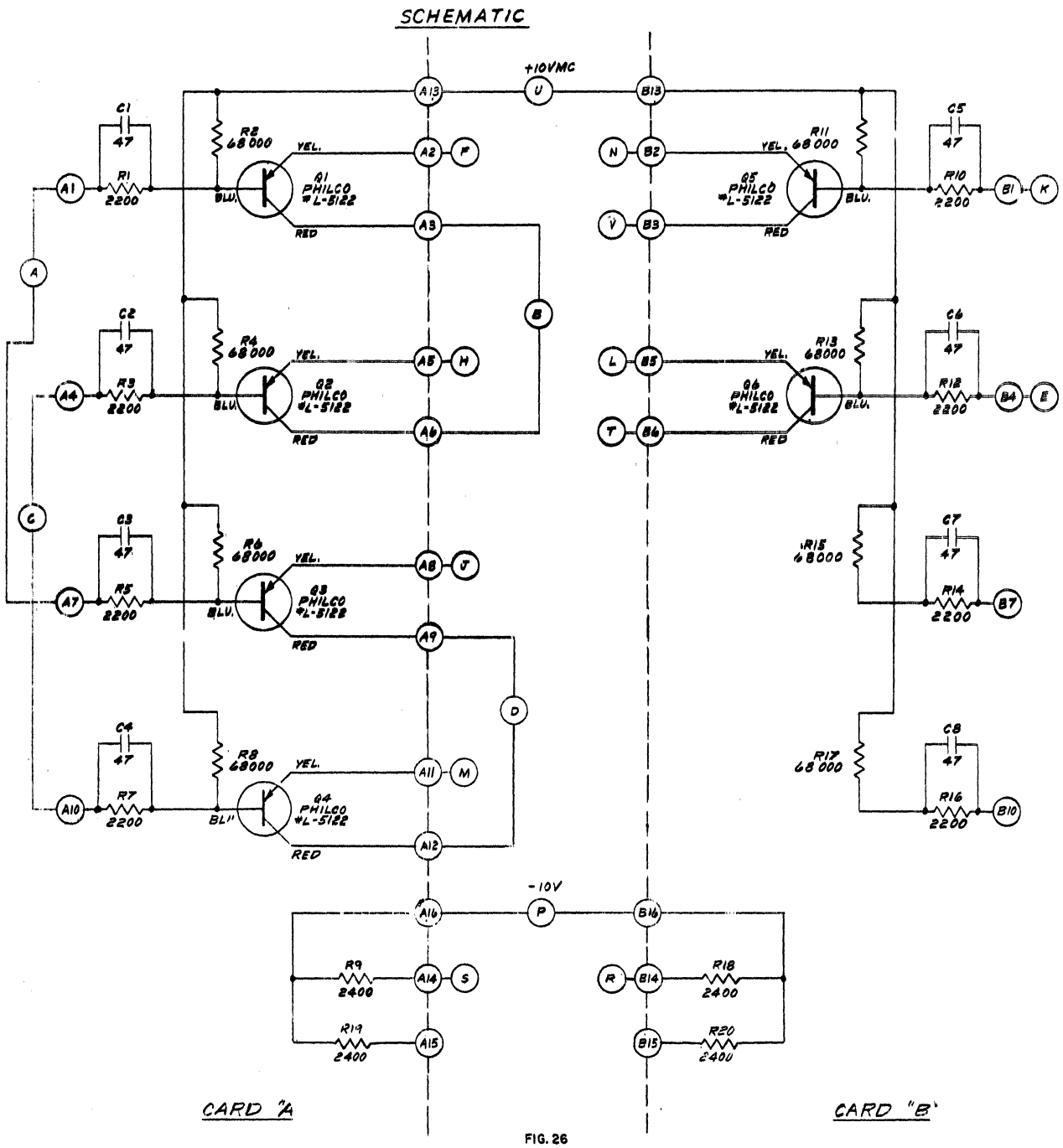


FIG. 26
PARALLEL (6) INVERTER

INVERTER P-6

Handle Color: Black Red

Drawing Number: D-67285 (lug); D-86866 (eyelet)

PW Number: 63-582 (lug); 63-1023 (eyelet)

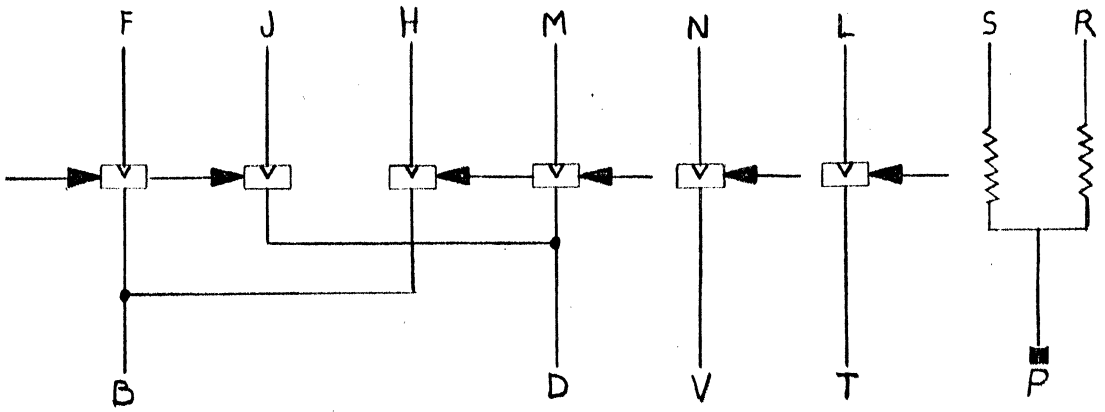
Transistors:* 6 L-5122

Power Supply Voltages: +10 MC; -10

Use: Inverters for logic and gating. Contains 2 load resistors

Remarks:

*All transistor type numbers are identified with manufacturer in appendix



U = +10V MC.
P = -10V

FIG. 27

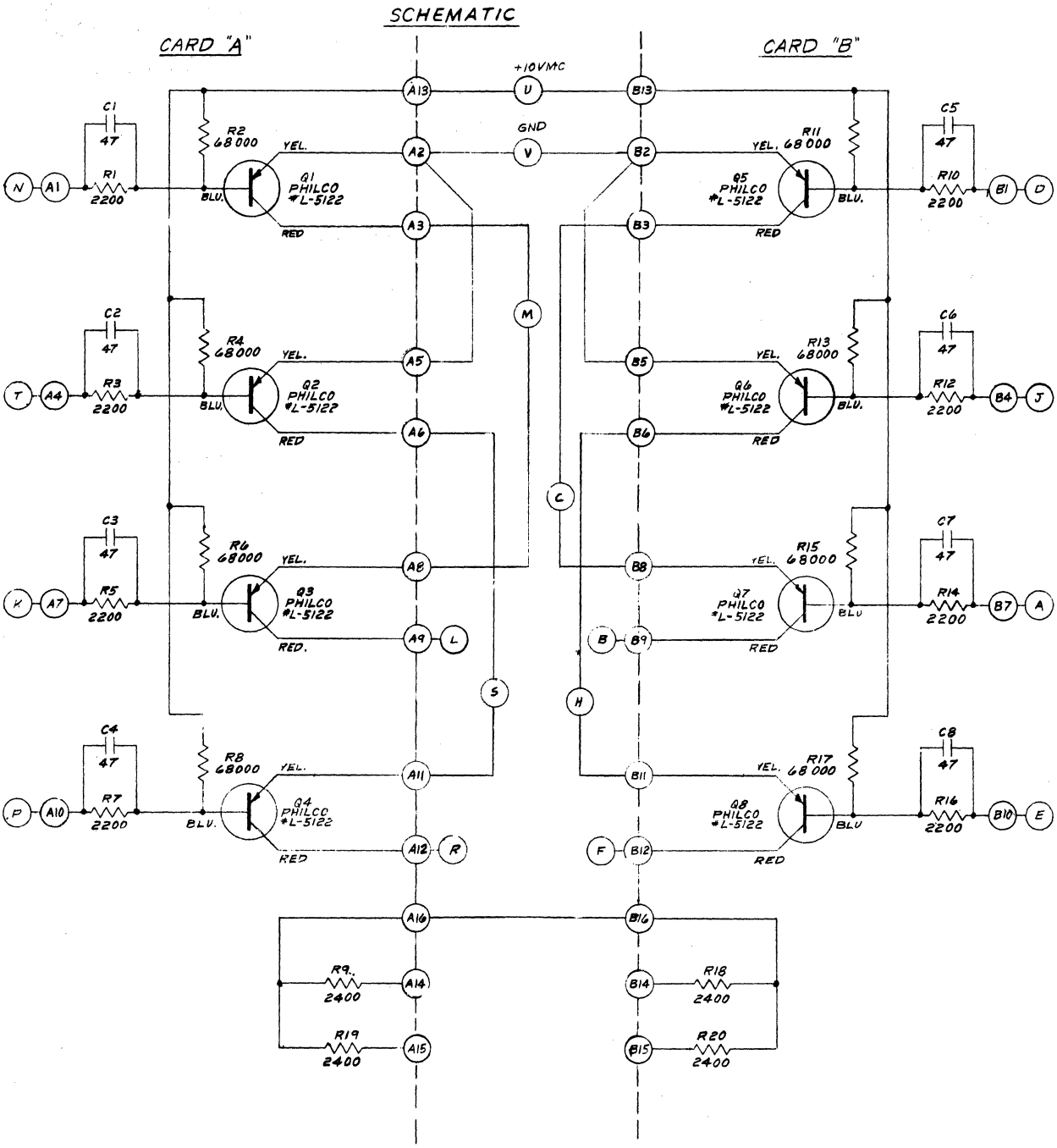


FIG. 28

SERIES (8) INVERTER

D-86867
"N" RED.

INVERTER S-8

Handle Color: Black Orange

Drawing Number: D-80129 (lug); D-86867 (eyelet)

PW Number: 63-582 (lug); 63-1023 (eyelet)

Transistors:* 8 L-5122

Power Supply Voltages: +10 MC

Use: Inverters for logic and gating

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

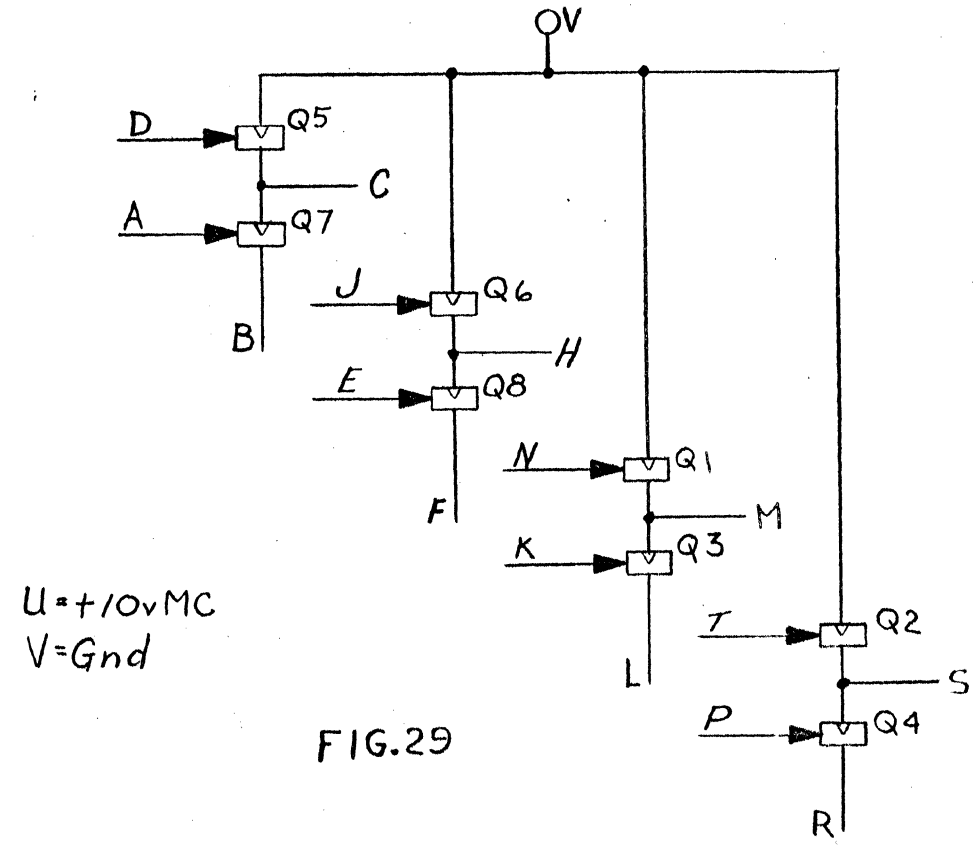


FIG.29

SCHEMATIC

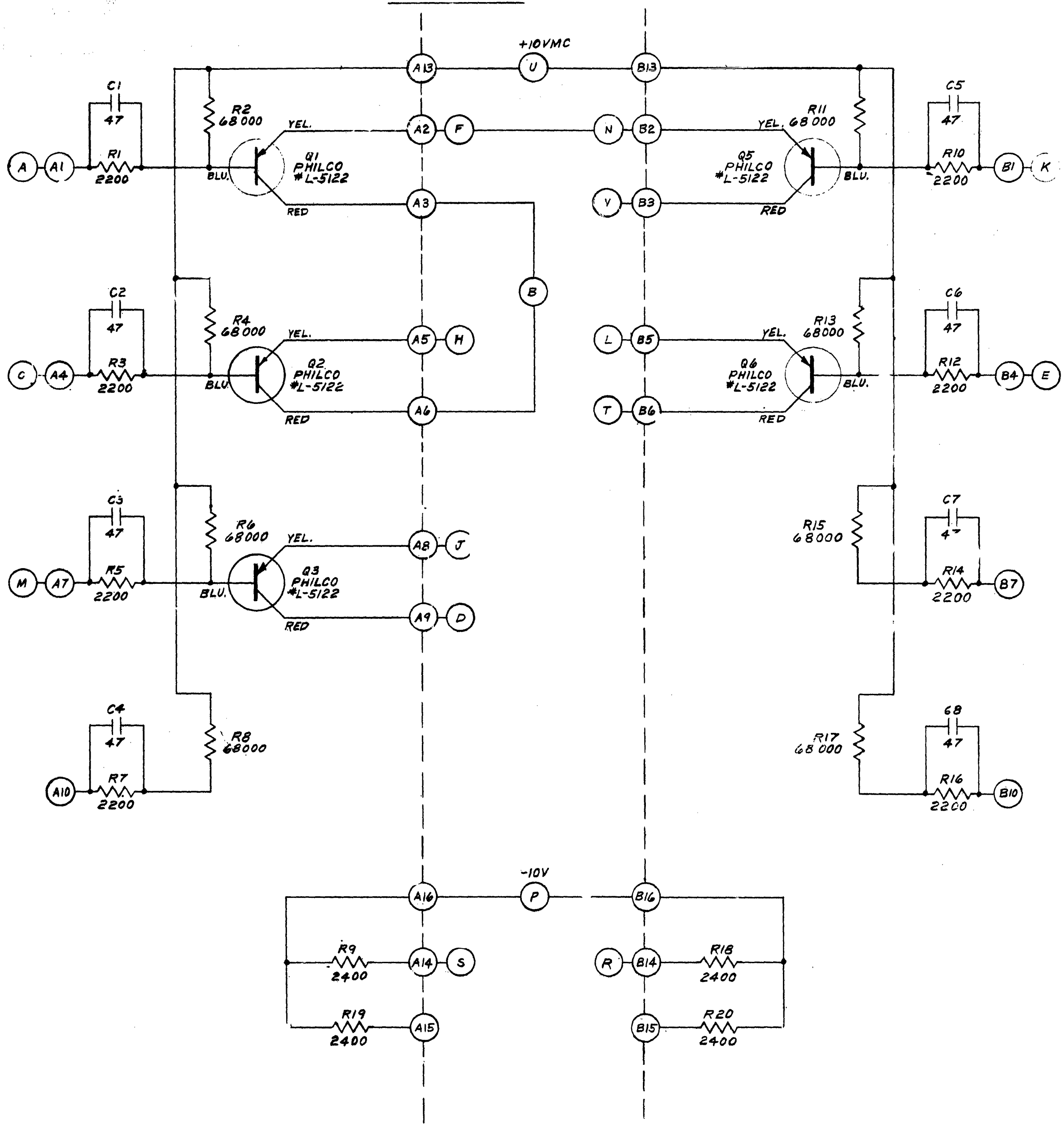


FIG. 30

PARALLEL (5) INVERTER

INVERTER P-5

Handle Color: Black Yellow

Drawing Number: D-67255 (lug); D-86518 (eyelet)

PW Number: 63-582 (lug); 63-1023 (eyelet)

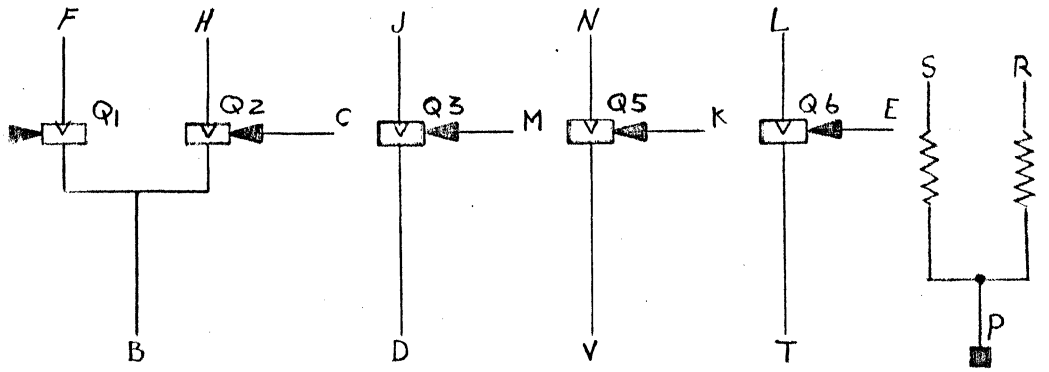
Transistors:* 5 L-5122

Power Supply Voltages: +10 MC; -10

Use: Inverters for logic and gating. Contains 2 load resistors.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix



U = +10V M.C.
P = -10V

FIG. 31

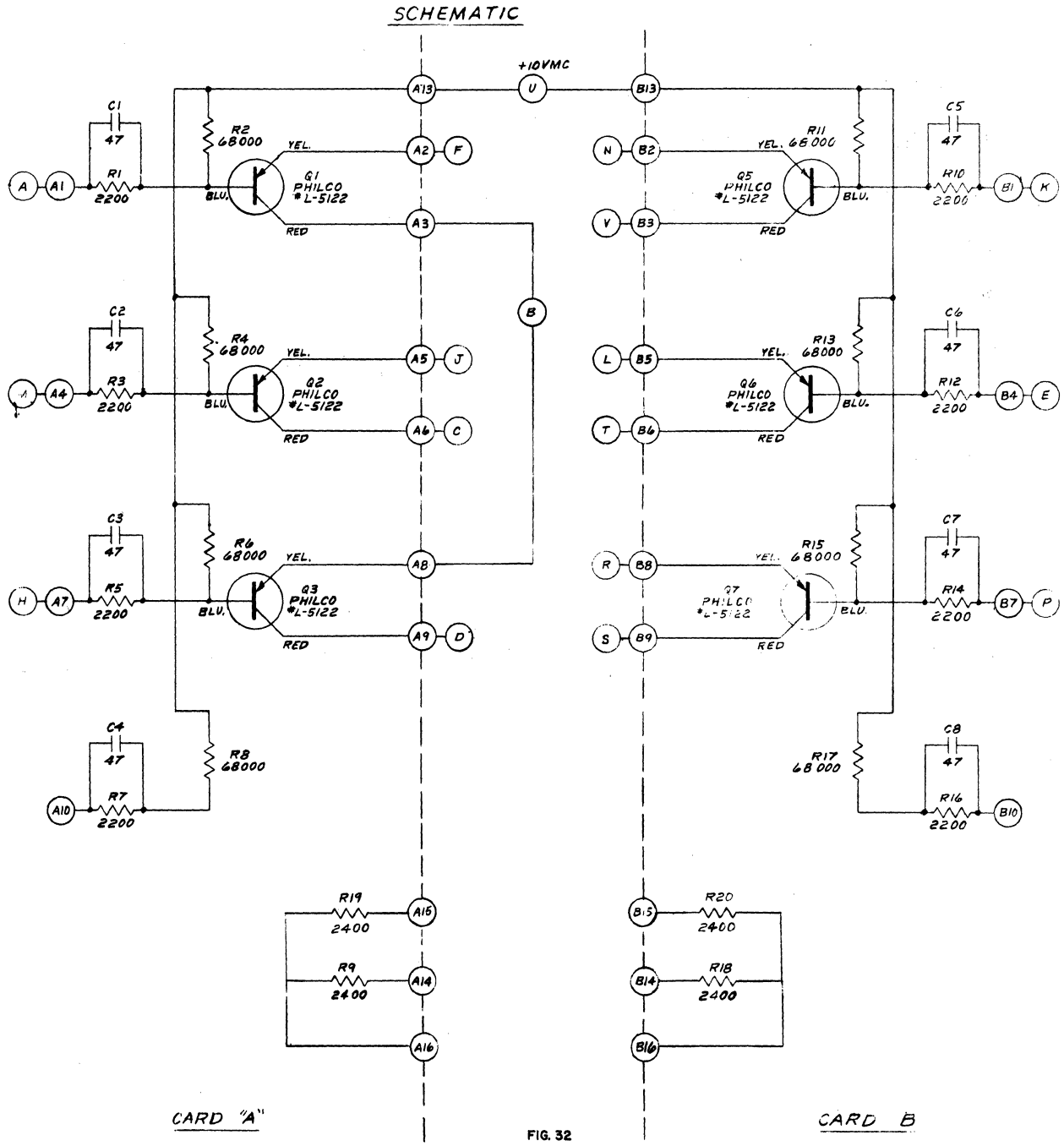


FIG. 32

SERIES (6) INVERTER

D-28665
11-RED

INVERTER S-6

Handle Color: Black Green

Drawing Number: D-67254 (lug); D-86865 (eyelet)

FW Number: 63-582 (lug); 63-1023 (eyelet)

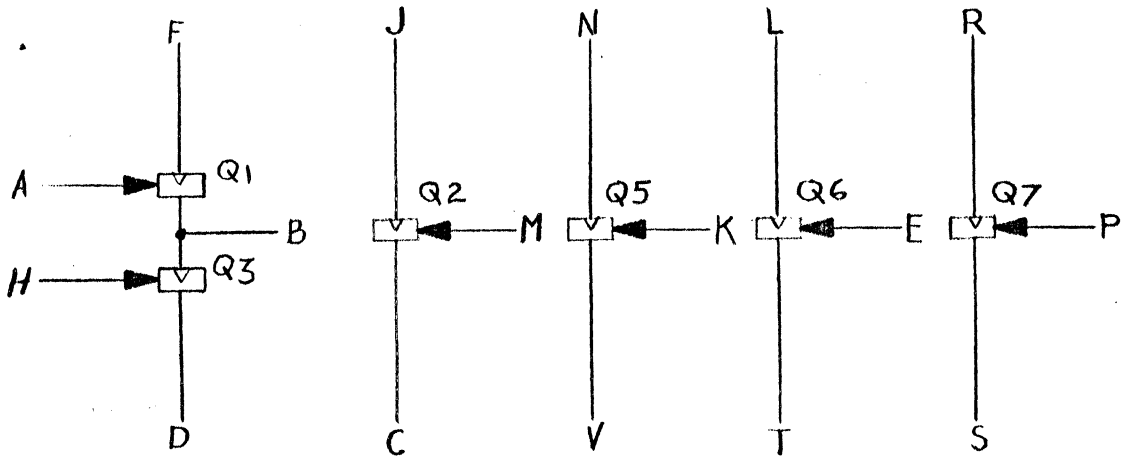
Transistors:* 6 L-5122

Power Supply Voltages: +10 MC

Use: Inverters for logic and gating

Remarks:

*All transistor type numbers are identified with manufacturer in appendix



U = +10v MC

FIG. 33

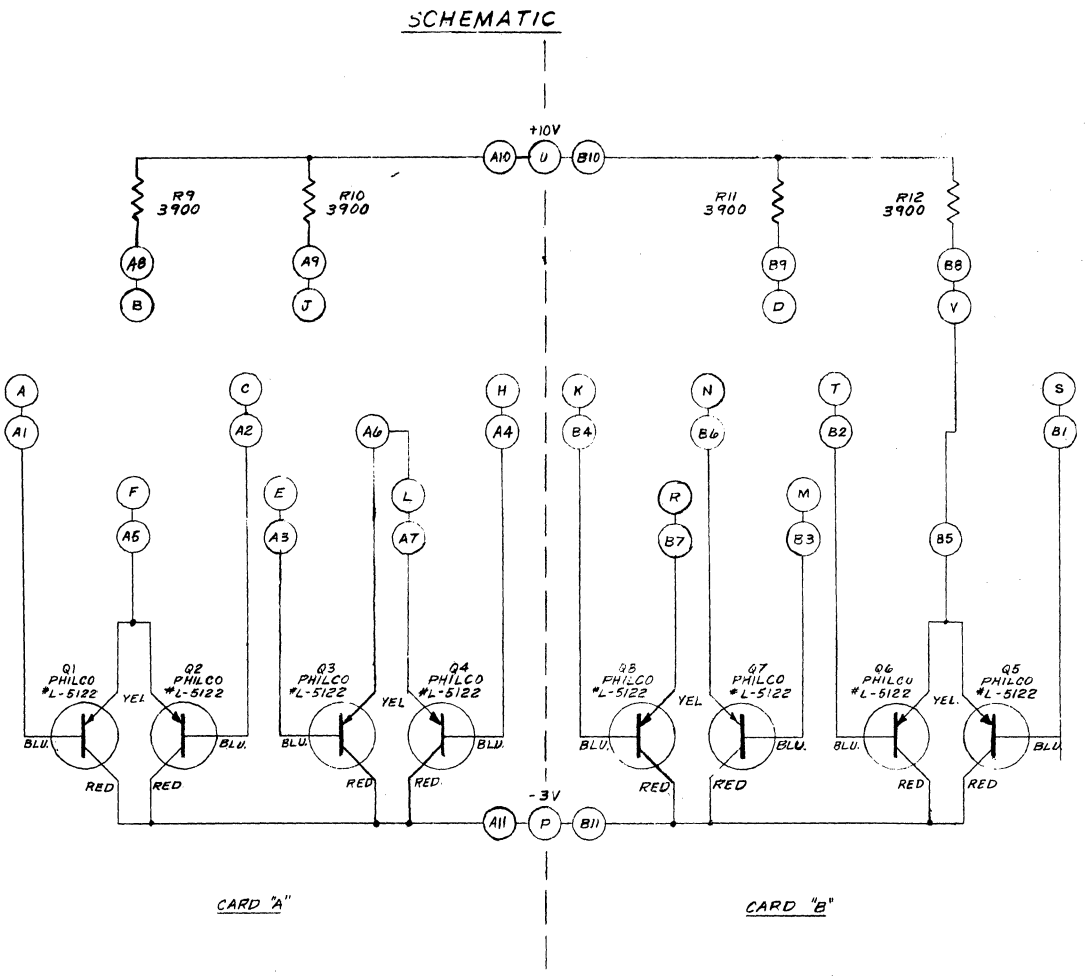


FIG. 34

(8) TRANSISTOR EMITTER FOLLOWER

P-86827
#-RED.

EMITTER FOLLOWER 8

Handle Color: Black Blue

Drawing Number: D-67273 (lug); D-86827 (eyelet)

PW Number: 63-581 (lug); 63-1021 (eyelet)

Transistors:* 8 L-5122

Power Supply Voltages: +10

Use: Emitter followers for logic and current amplification. Contains 4 load resistances

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

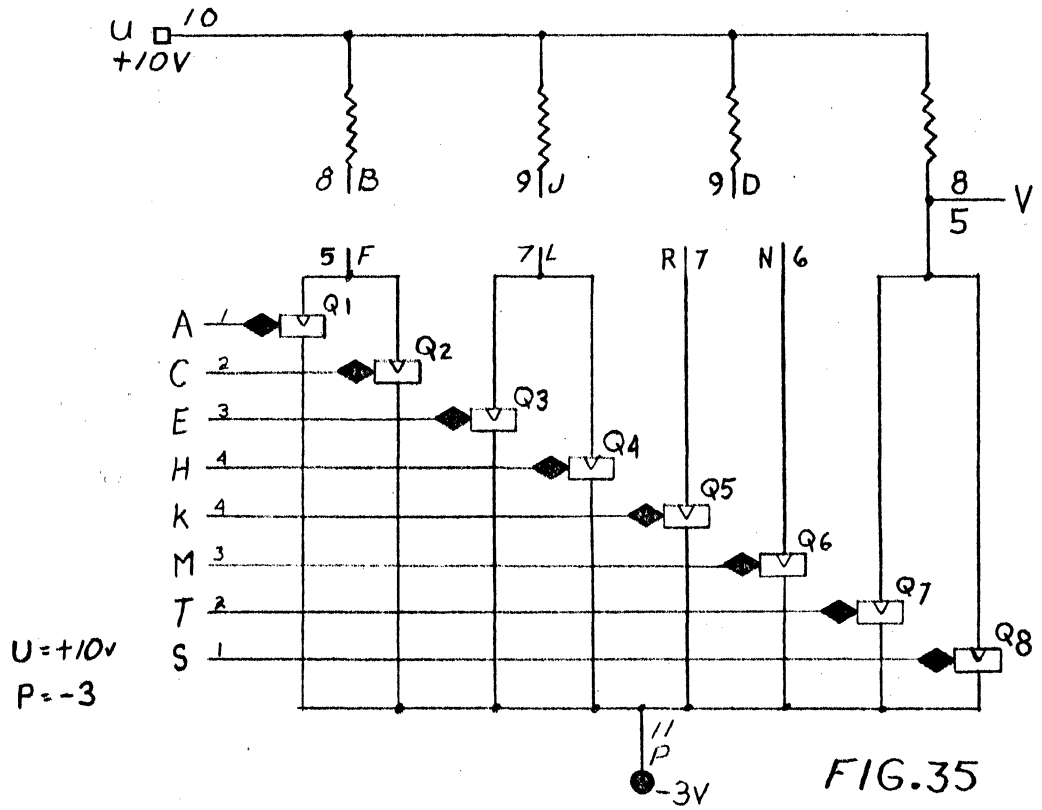


FIG.35

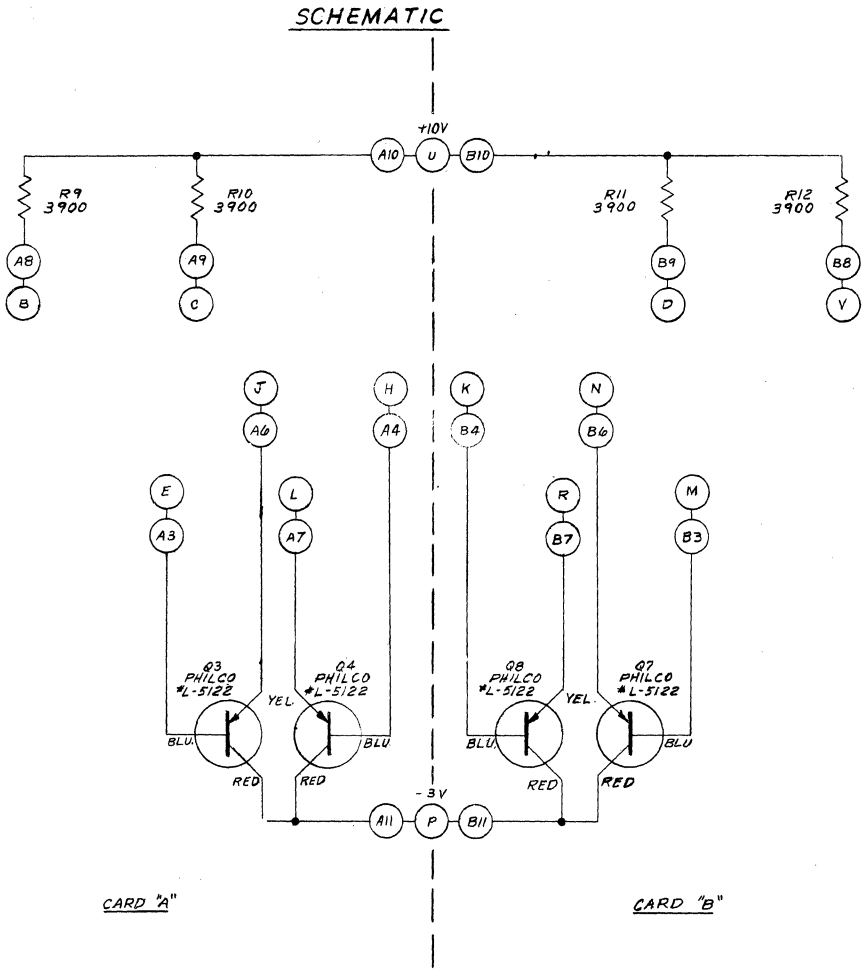


FIG. 36

(4) TRANSISTOR EMITTER FOLLOWER

D-66826
"A" ED.

EMITTER FOLLOWER 4

Handle Color: Black Violet

Drawing Number: D-67272 (lug); D-86826 (eyelet)

PW Number: 63-581 (lug); 63-1021 (eyelet)

Transistors:* 4 L-5122

Power Supply Voltages: +10

Use: Emitter followers for logic and current amplification. Contains 4 load resistances

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

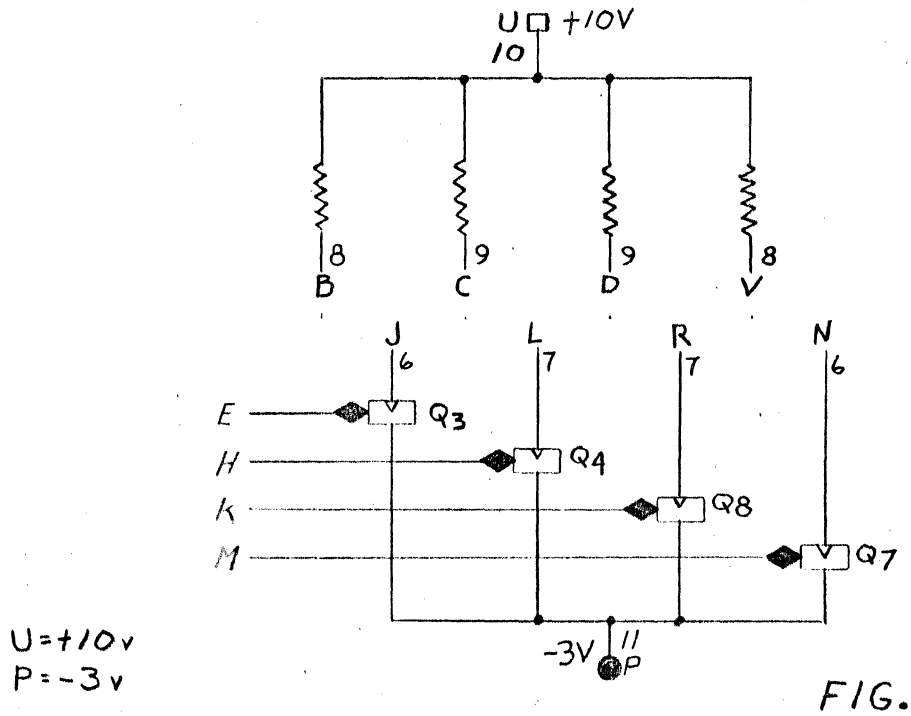


FIG.37

SCHEMATIC

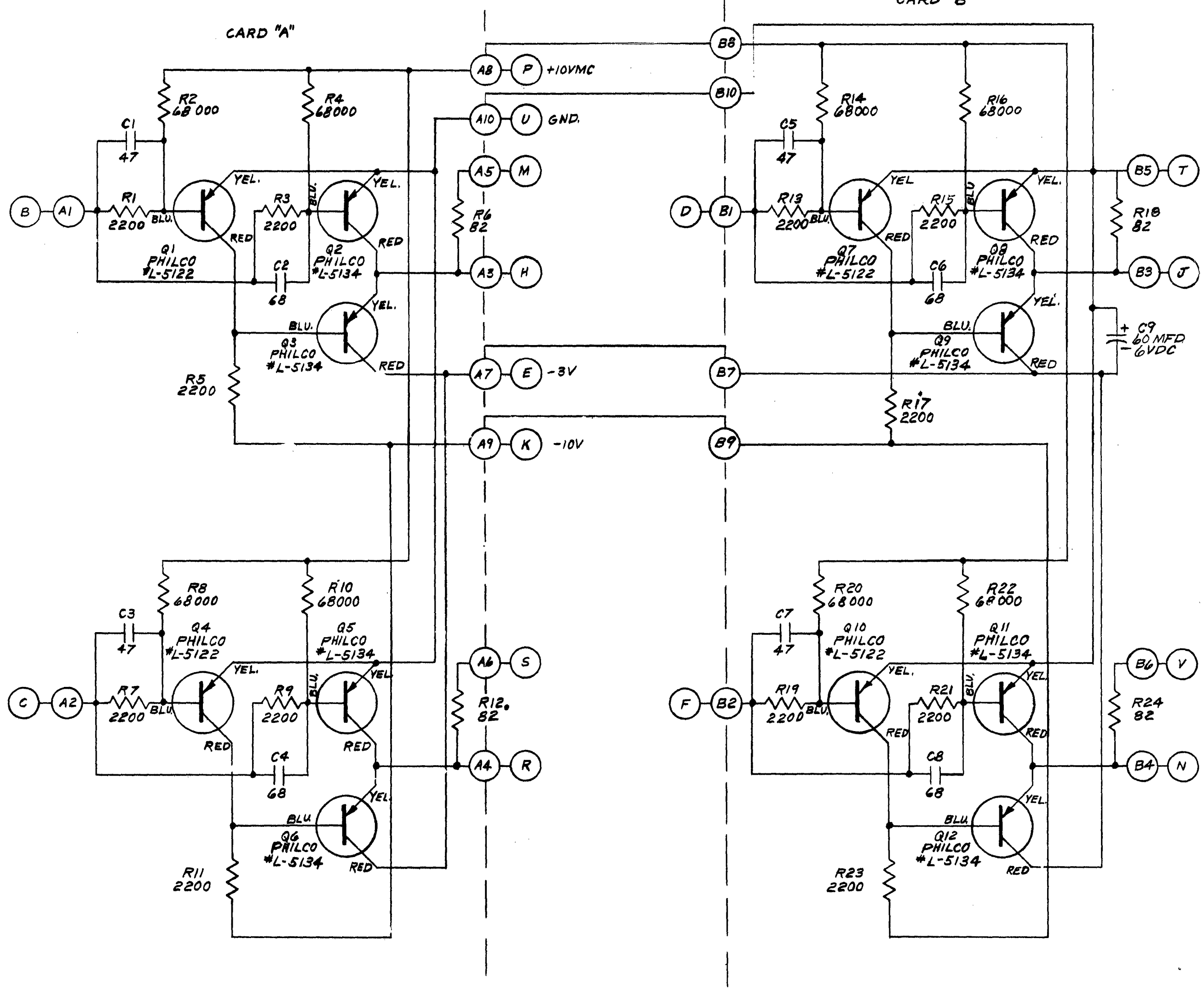


FIG. 38
CASCODE AND CABLE DRIVER

D-86555 "A" REQ

CASCODE AND CABLE DRIVER

Handle Color: Black Grey

Drawing Number: D-67159 (lug); D-86555 (eyelet)

PW Number: 63-514 (lug); 63-1022 (eyelet)

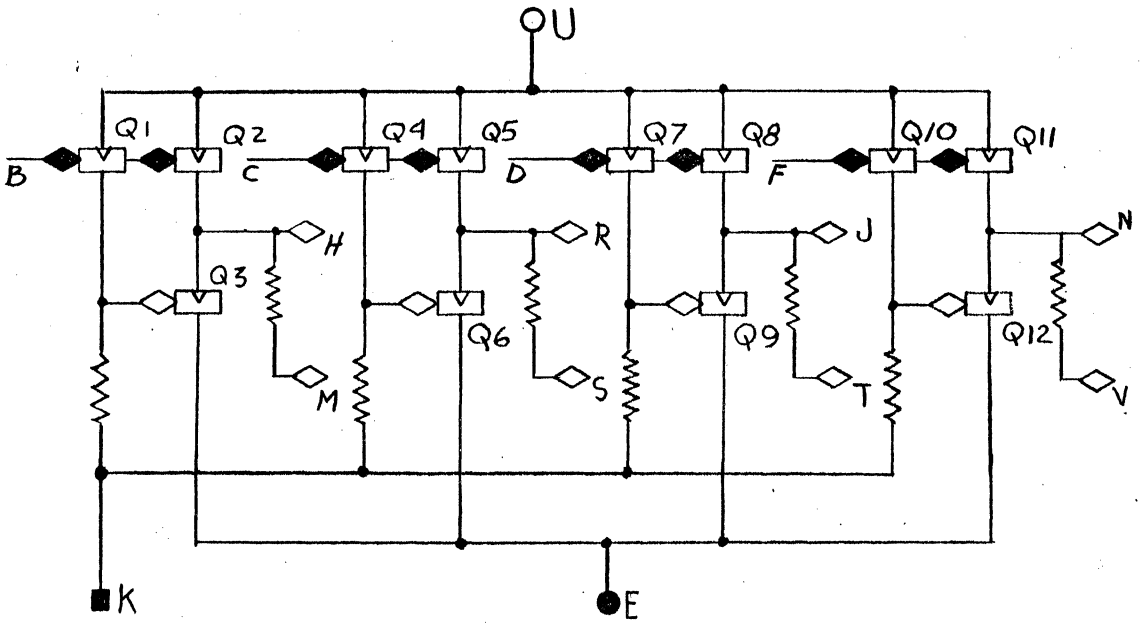
Transistors:* 4 L-5122; 8 L-5134

Power Supply Voltages: +10 MC; -3; -10

Use: Inverting power amplifier, and cable driver for 93 ohm cable and twisted pair wire.

Remarks: 4 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix



P=+10vMC
K=-10v
E=-3v
U=Gnd

FIG. 39

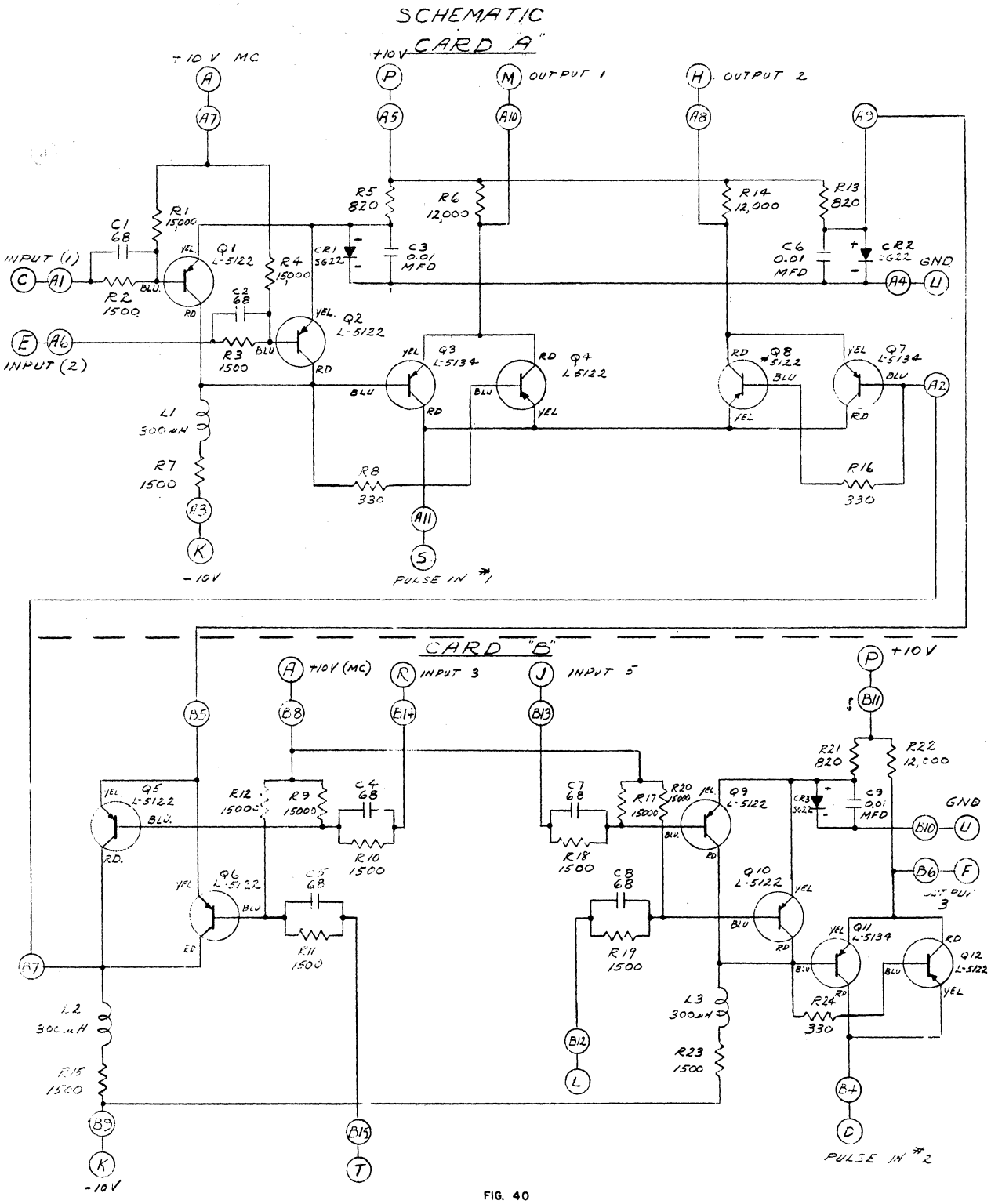


FIG. 40
REGISTER DRIVER

D-84924
"A"-REV.

REGISTER DRIVER

Handle Color: Black White

Drawing Number: D-67976 (lug); D-84924 (eyelet)

PW Number: 63-624 (lug); 63-1027 (eyelet)

Transistors:* 9 L-5122; 3 L-5134

Power Supply Voltages: +10 MC; +10; -10

Use: Pulse gate for driving register of pulsed bases

Remarks: 3 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

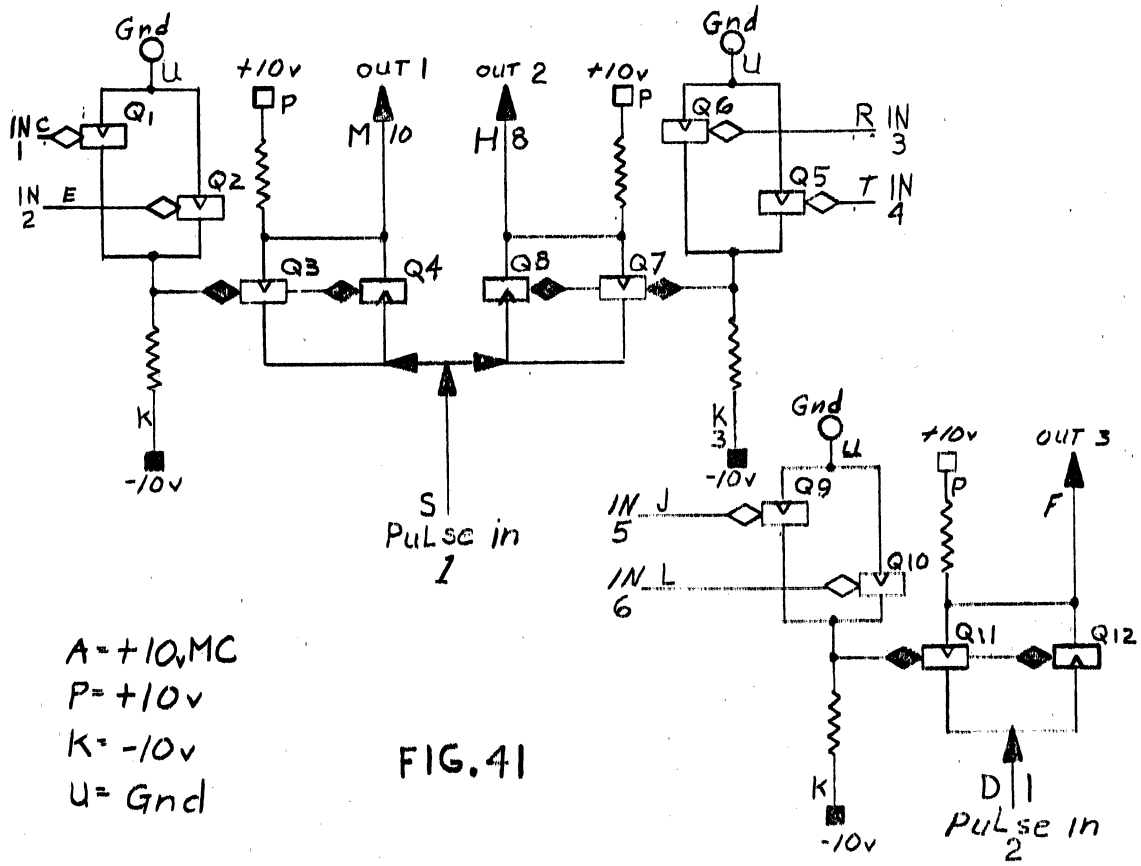


FIG. 41

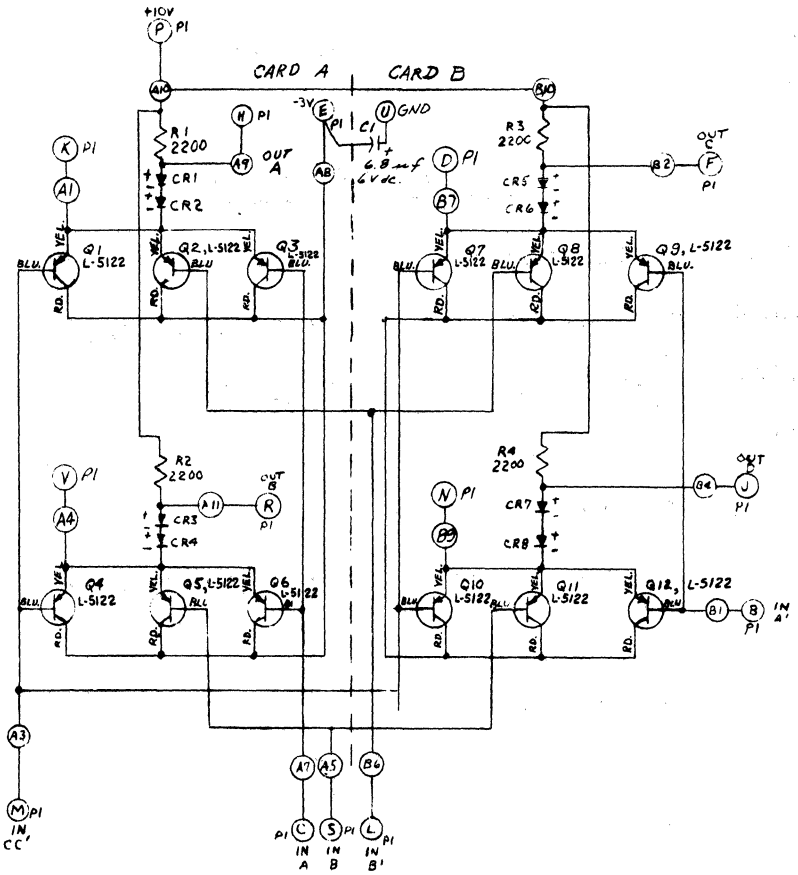


FIG. 42

ADDRESS DECODER

ADDRESS DECODER

Handle Color: Brown Orange

Drawing Number: D-67141

PW Number: 63-606

Transistors:* 12 L-5122

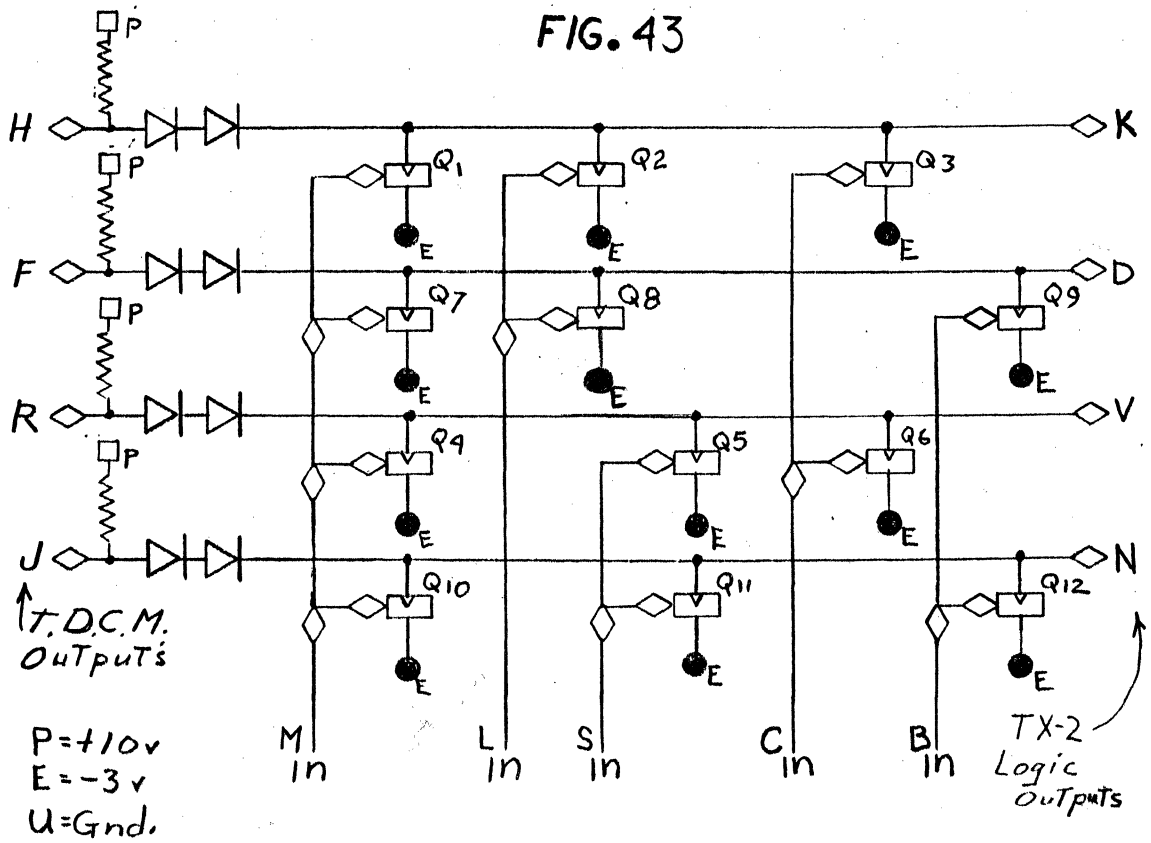
Power Supply Voltages: +10;MC -3

Use: Address Decoder in TDCM and S memory and emitter follower logic

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG. 43



D-87626
A-REDUCTION

SCHEMATIC

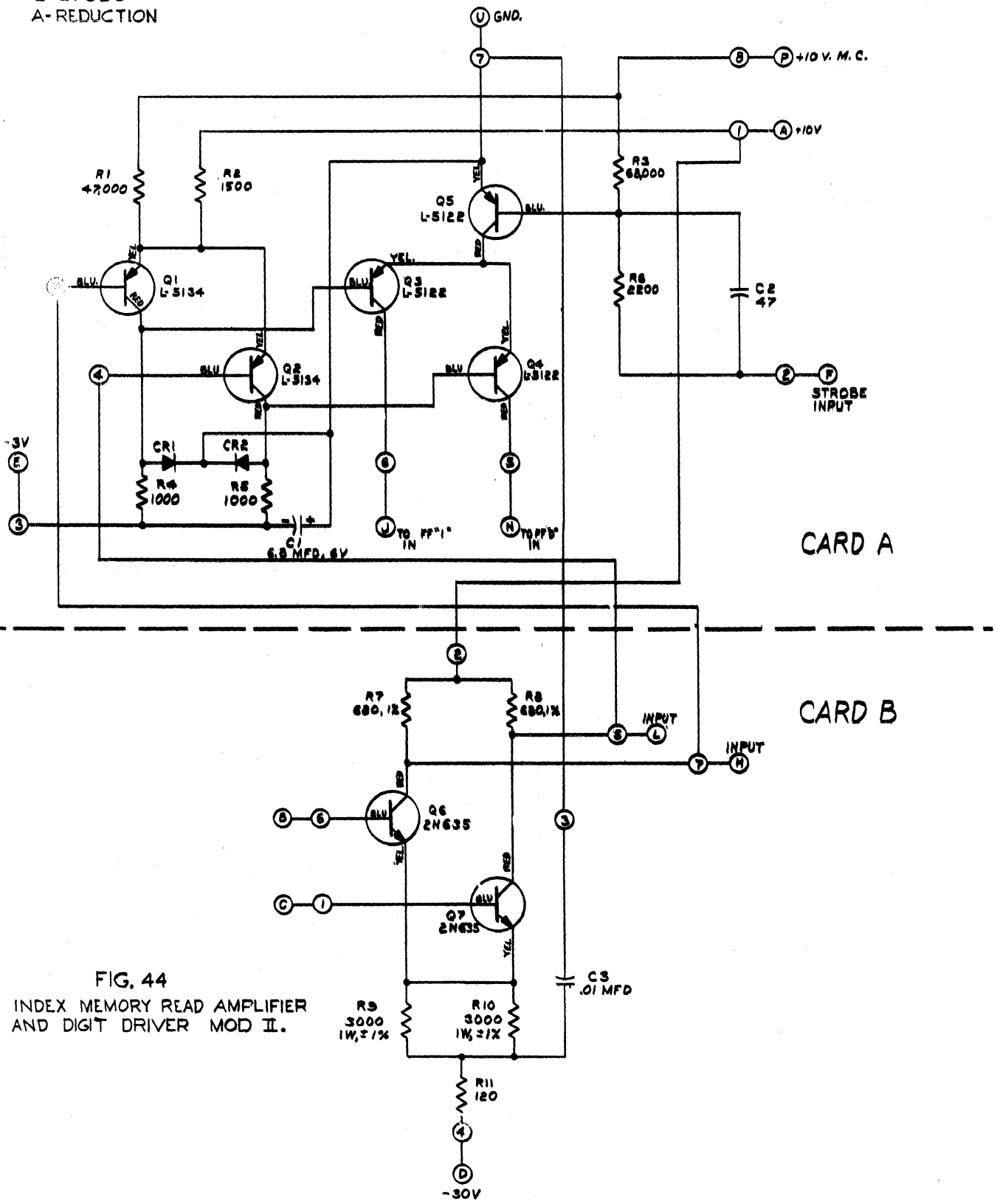


FIG. 44
INDEX MEMORY READ AMPLIFIER AND DIGIT DRIVER MOD II.

READ AMPLIFIER AND DIGIT DRIVER MOD II

Handle Color: Brown Blue

Drawing Number: D-87626

PW Number: 63-1121

Transistors:* 3 L-5122; 2 L-5134; 2 2N635

Power Supply Voltages: +10 MC; +10; -3; -10; -30

Use: Sense amplifier and digit line driver for Index Memory

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

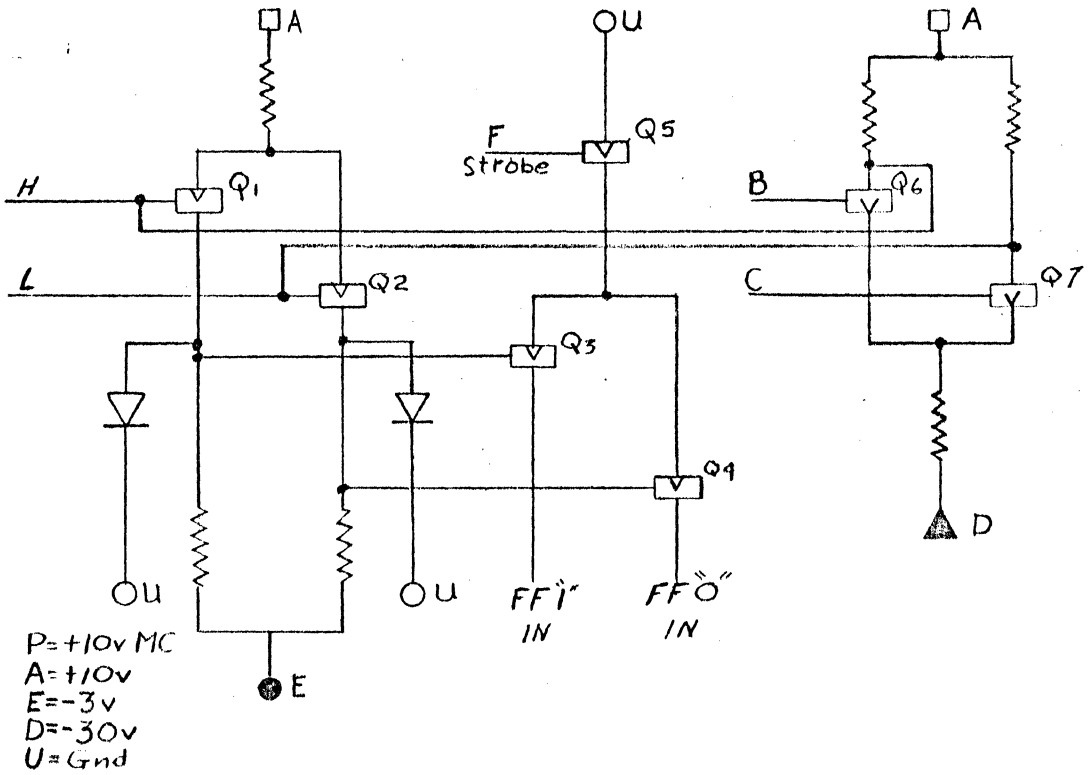


FIG. 45

D-67511
A - REDUCTION

SCHEMATIC

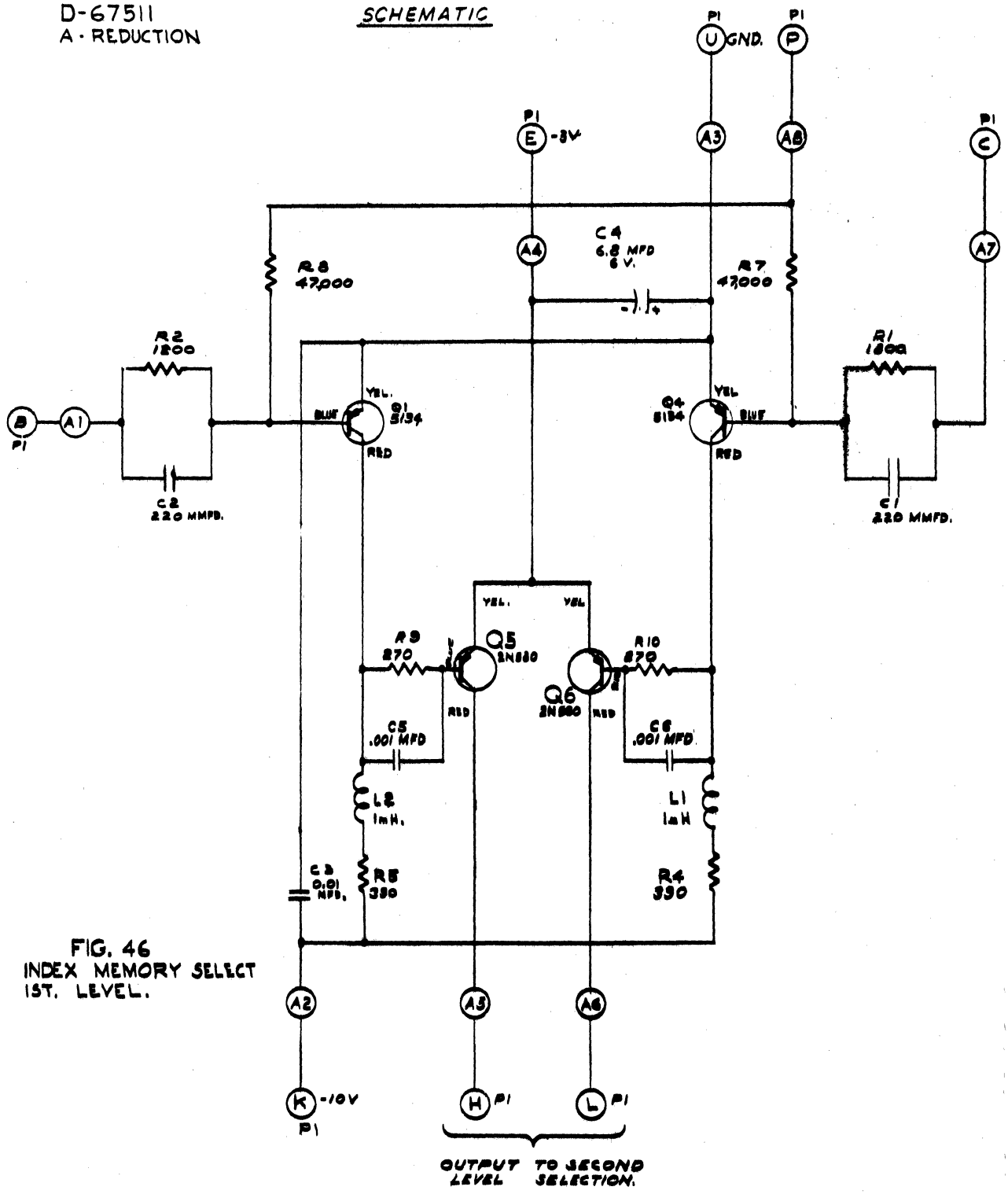


FIG. 46
INDEX MEMORY SELECT
1ST. LEVEL.

SELECT CIRCUIT 1ST LEVEL

Handle Color: Brown Violet

Drawing Number: D-67511

PW Number: 63-595

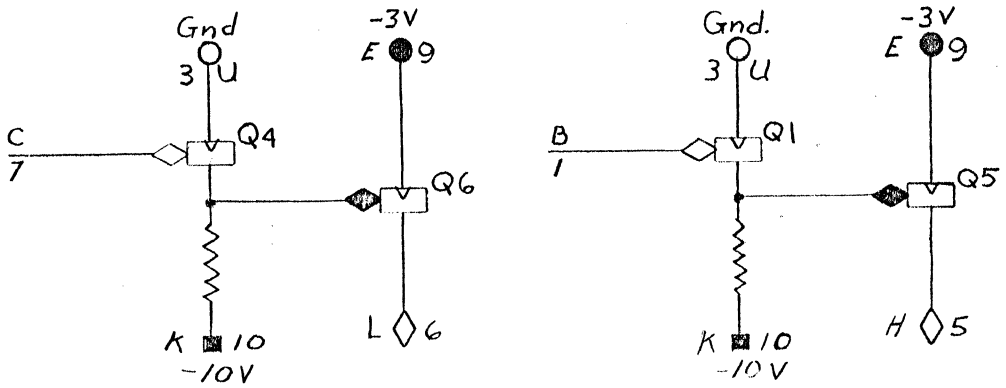
Transistors:* 2 L-5134; 2 2N580

Power Supply Voltages: +10 MC; -3; -10

Use: First level selection circuit for Index Memory

Remarks:

*All transistor type numbers are identified with manufacturer in appendix



P = +10v MC
E = -3v
K = -10v
U = Gnd.

FIG. 47

D-67572
A- REDUCTION.

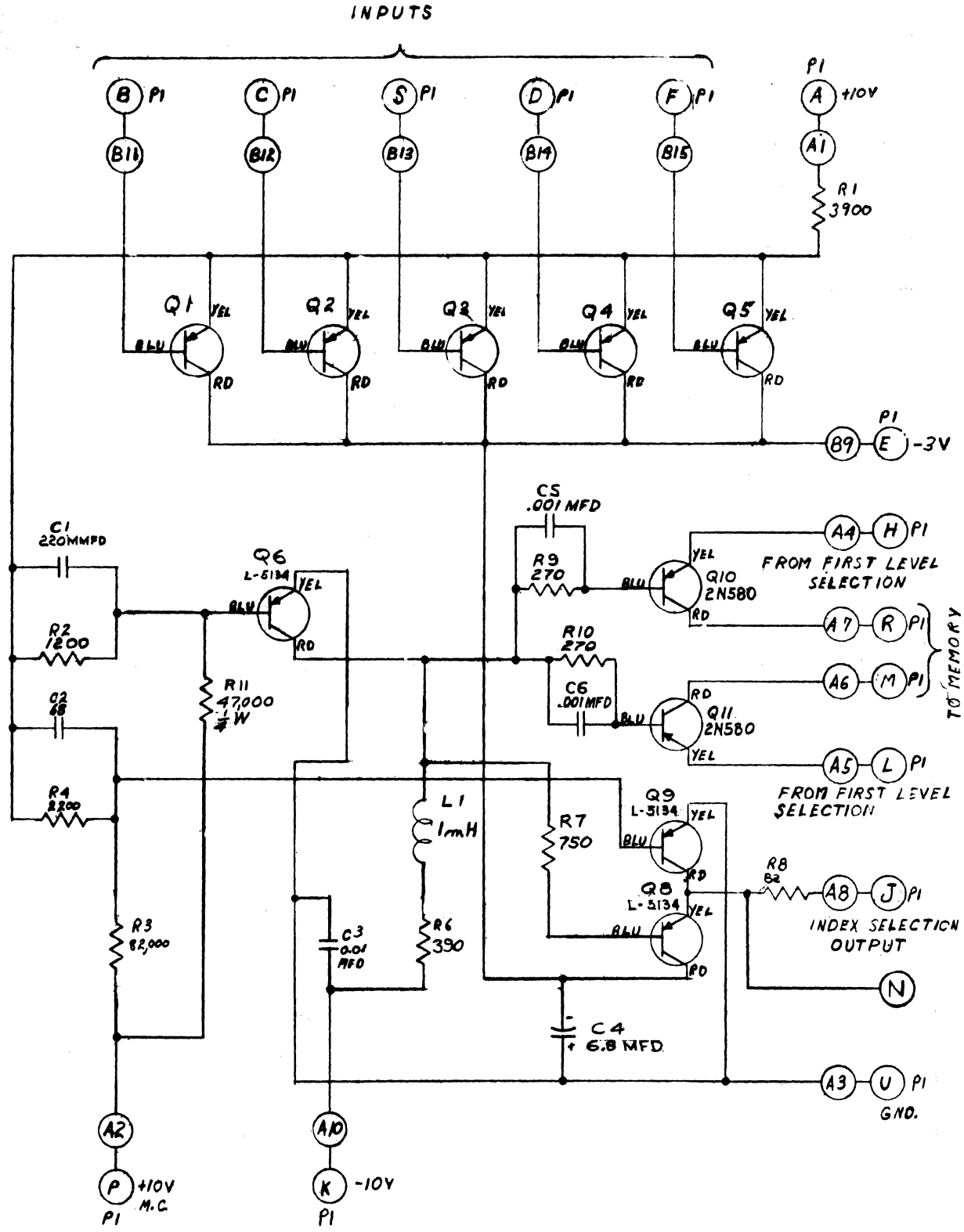


FIG. 48
INDEX MEMORY SELECT,
SECOND LEVEL.

SELECT CIRCUIT 2ND LEVEL

Handle Color: Brown Grey

Drawing Number: D-67572

PW Number: 63-605

Transistors:* 5 L-5122; 3 L-5134; 2 2N580

Power Supply Voltages: +10 MC; +10; -3; -10

Use: Second level selection circuit for Index Memory

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

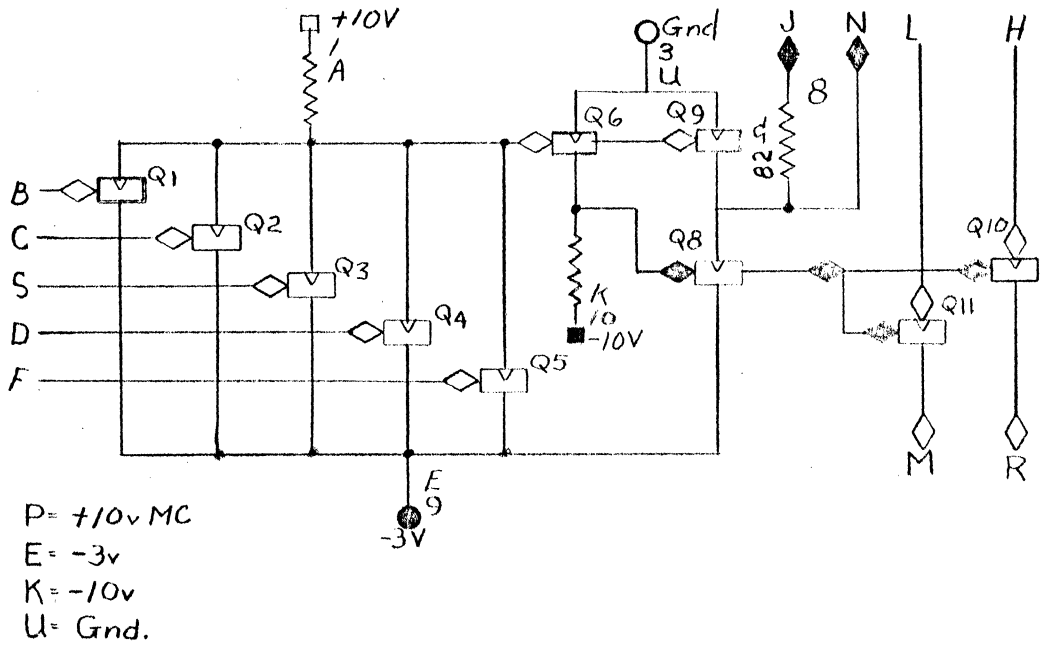


FIG. 49

D-80635
A- REDUCTION.

SCHEMATIC

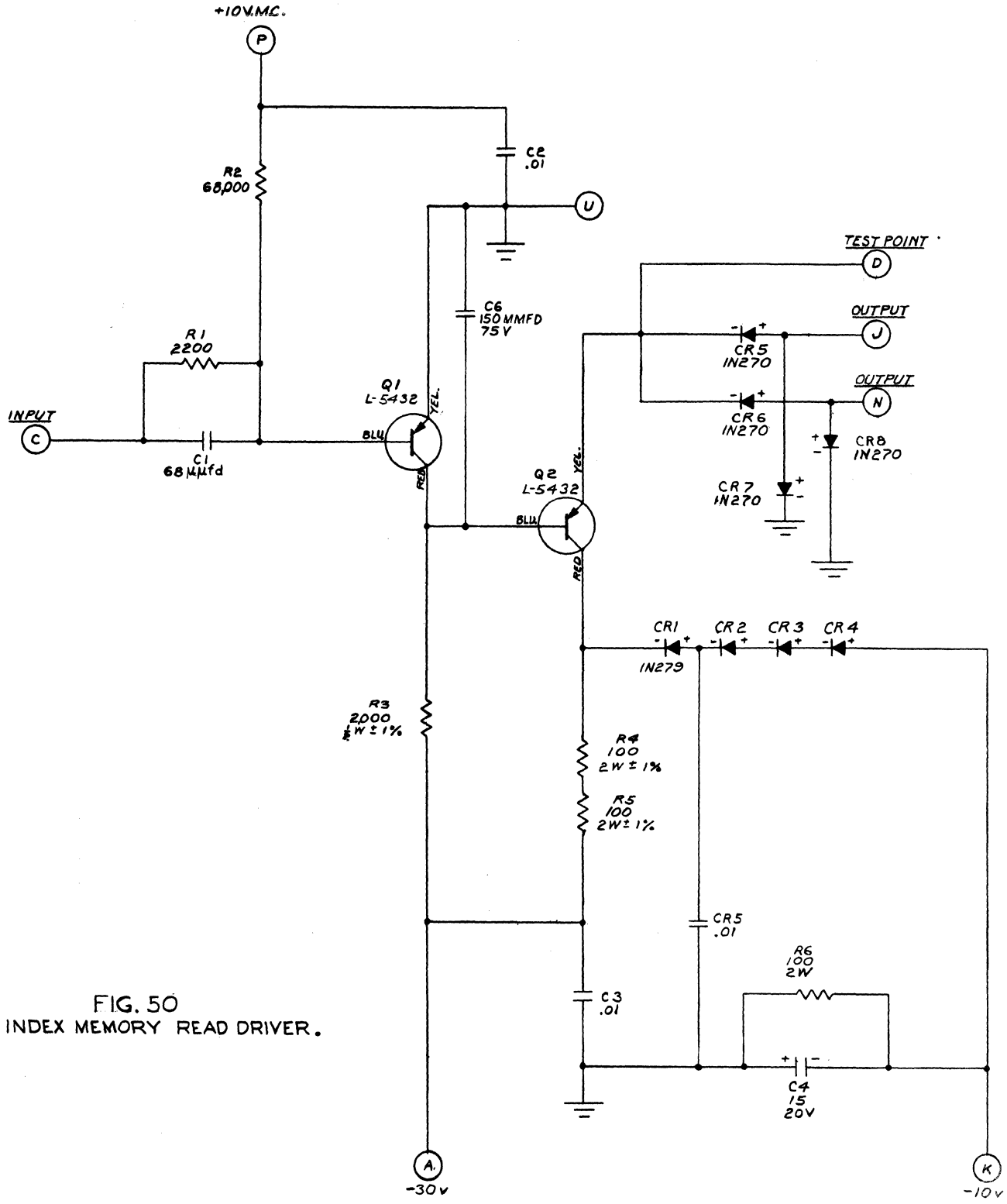


FIG. 50
INDEX MEMORY READ DRIVER.

READ DRIVER

Handle Color: Brown White

Drawing Number: D-80635

PW Number: 63-956

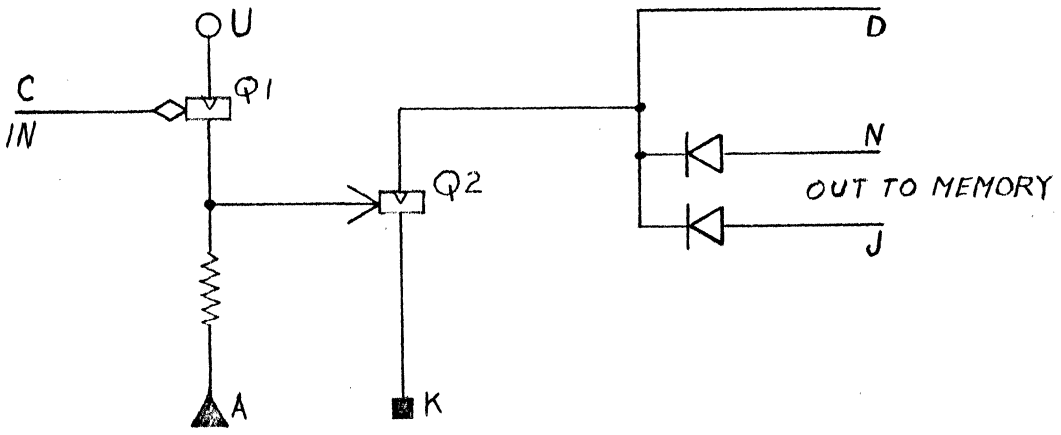
Transistors:* 2 L-5432

Power Supply Voltages: +10 MC; -10; -30

Use: Read Driver for Index Memory

Remarks:

*All transistor type numbers are identified with manufacturer in appendix



P=+10vMC
K=-10v
A=-30v
U=Gnd.

FIG. 51

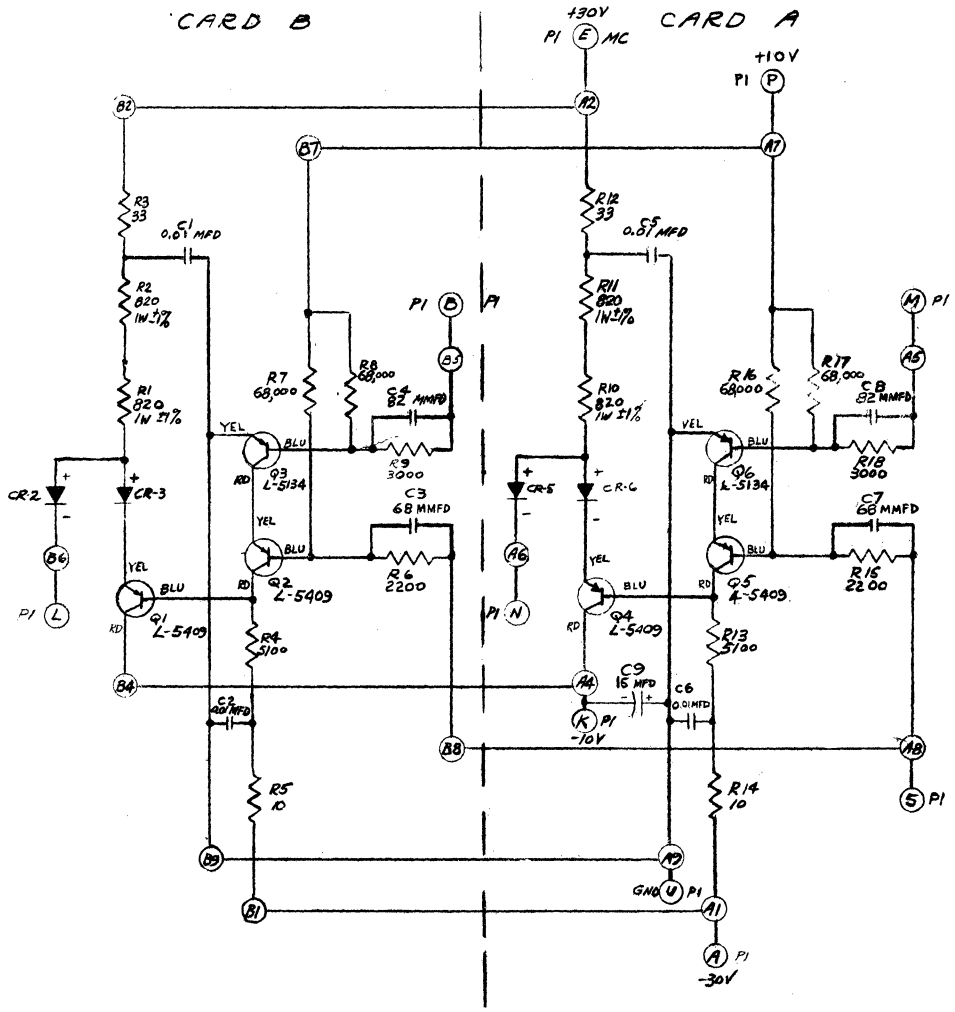


FIG. 52

INDEX MEMORY WRITE DRIVE

D-67513
"A" SERIES

WRITE DRIVER

Handle Color: Red Brown

Drawing Number: D-67573

PW Number: 63-597

Transistors:* 2 L-5134; 4 2N501

Power Supply Voltages: +30 MC; +10 MC; -30

Use: Write Driver for Index Memory

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

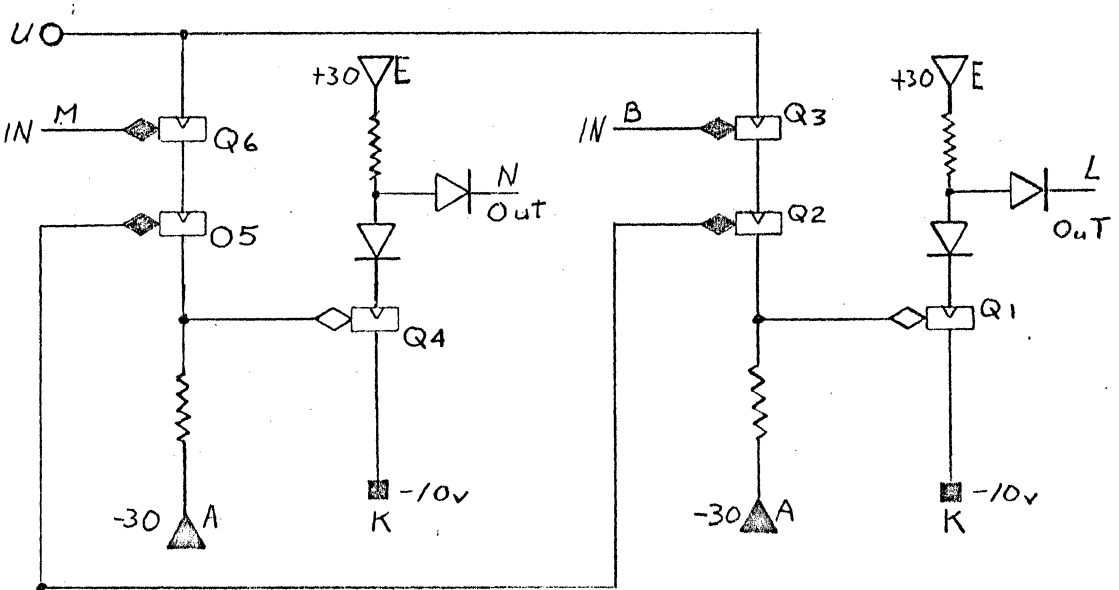


FIG. 53

SCHEMATIC

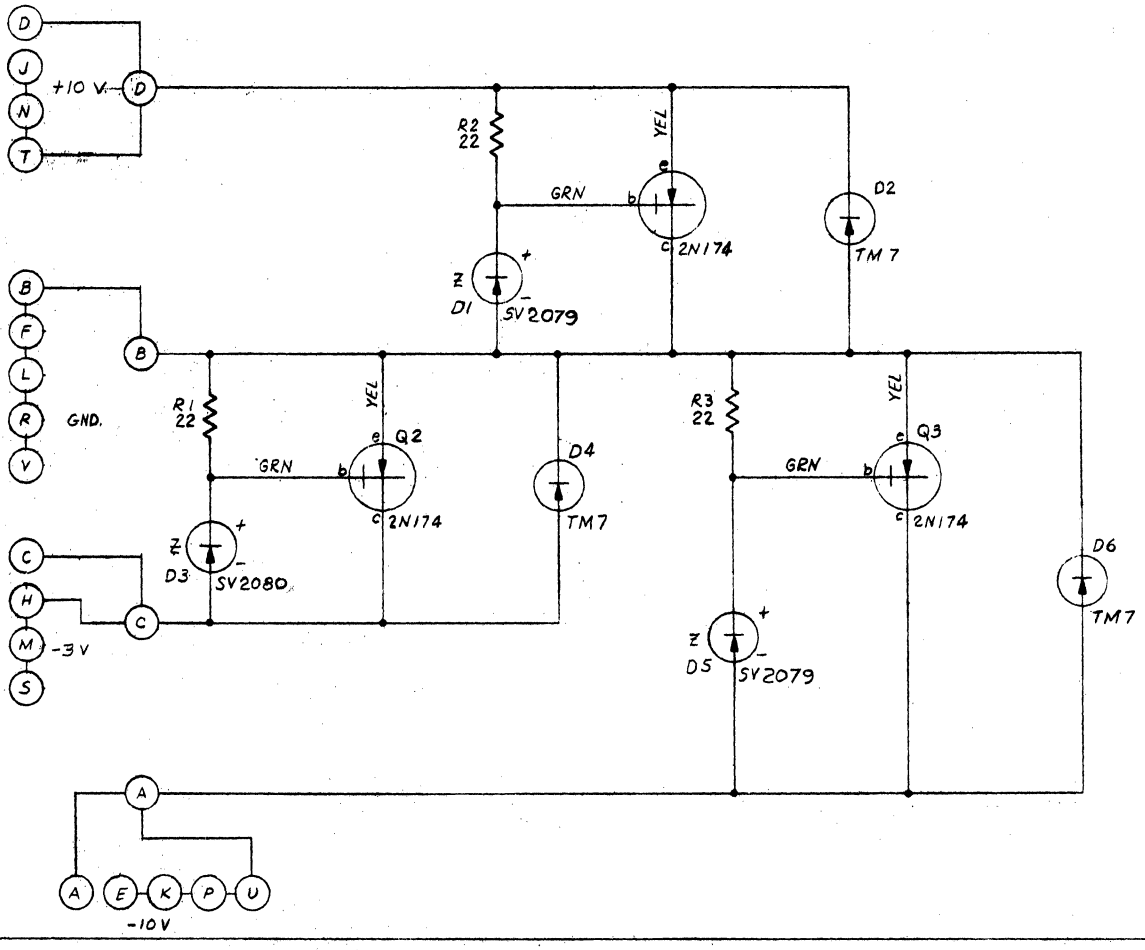


FIG. 54
POWER PROTECTOR

D-88400
"D" REG.

NO. 22

POWER PROTECTOR

Handle Color: Red Red

Drawing Number: D-82709

PW Number: 63-829

Transistors:* 3 2N174

Power Supply Voltages: +10; -3; -10

Use: Provides protection against over voltage on computer

Remarks: Also contains 6 Transitron Diodes -
3 TM7, 2 SV2079 Zener, 1 SV2080 Zener

*All transistor type numbers are identified with manufacturer in appendix

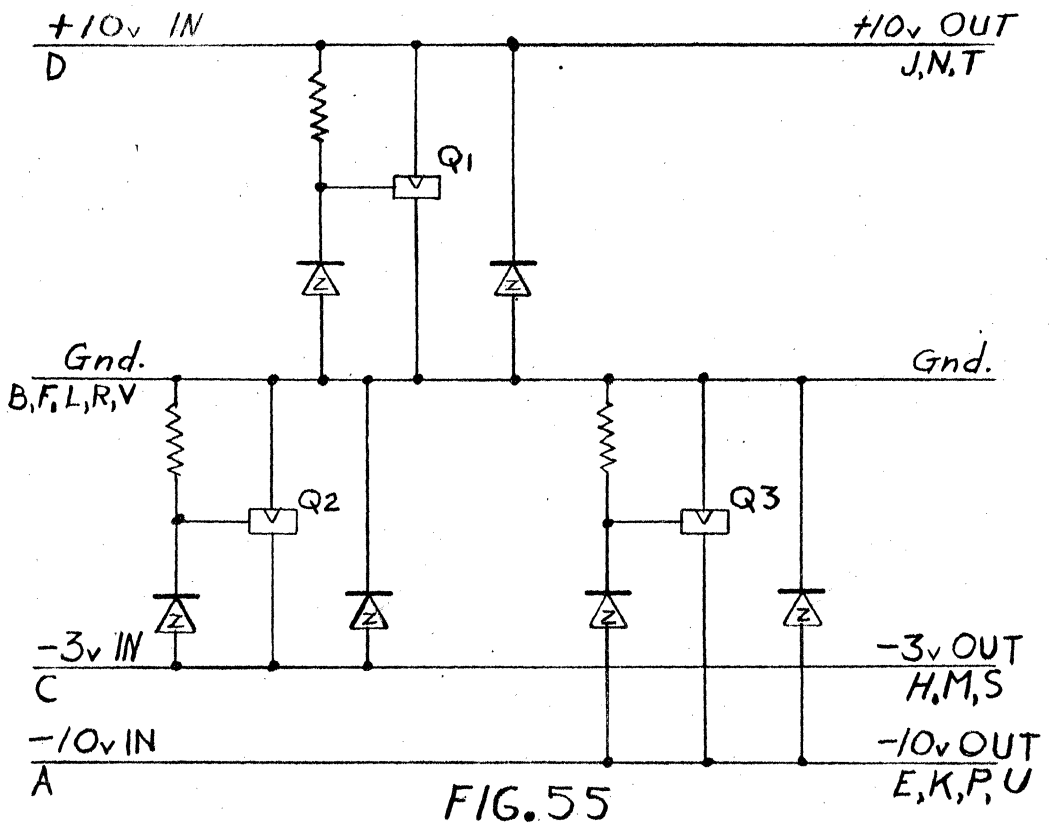


FIG. 55

SCHEMATIC

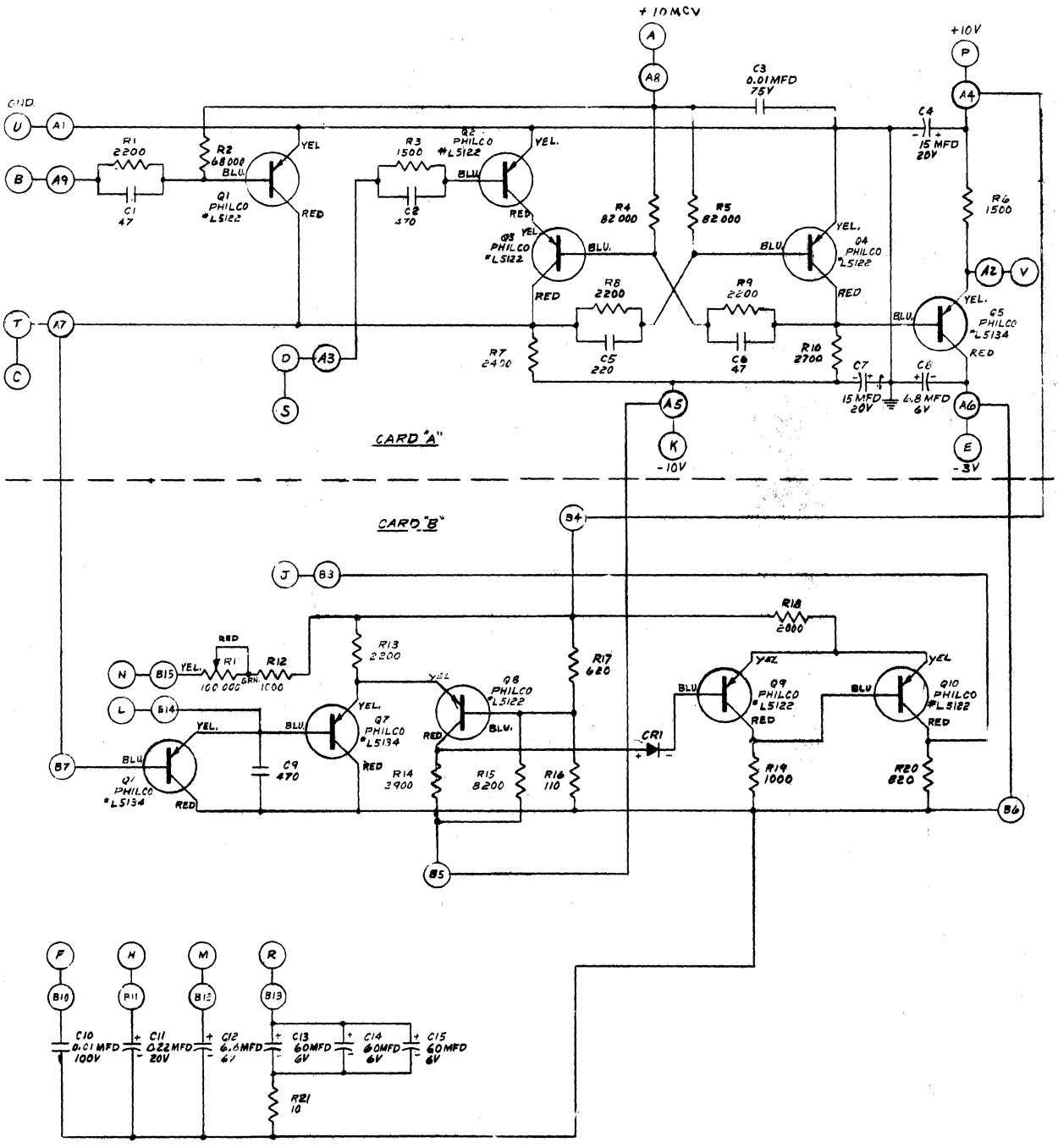


FIG. 56
VARIABLE DELAY UNIT

D-84175
"A" RED

NO. 23

VARIABLE DELAY UNIT

Handle Color: Red Orange

Drawing Number: D-84175

PW Number: 63-942

Transistors:* 7 L-5122; 3 L-5134

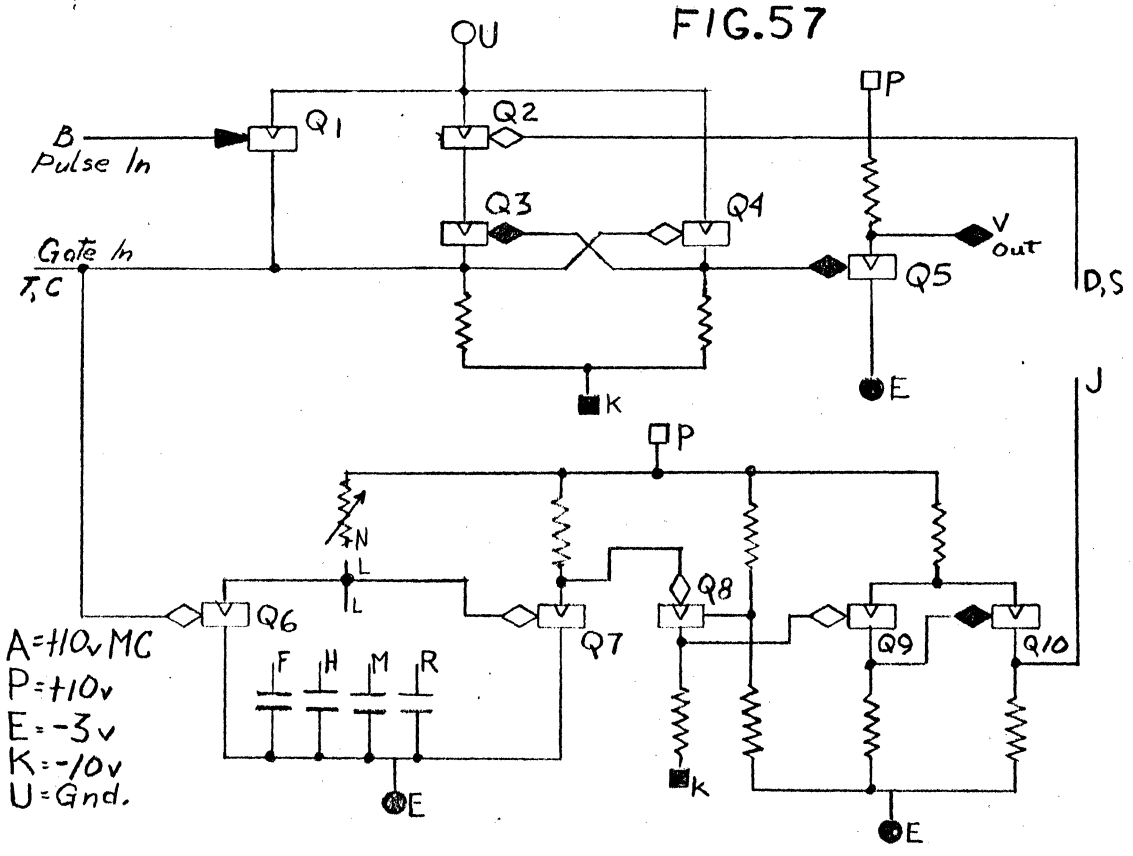
Power Supply Voltages: +10 MC; +10; -3; -10

Use: Provides delayed level. Duration of -3 volt level variable from .3 μsec to 2.2 sec.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG.57



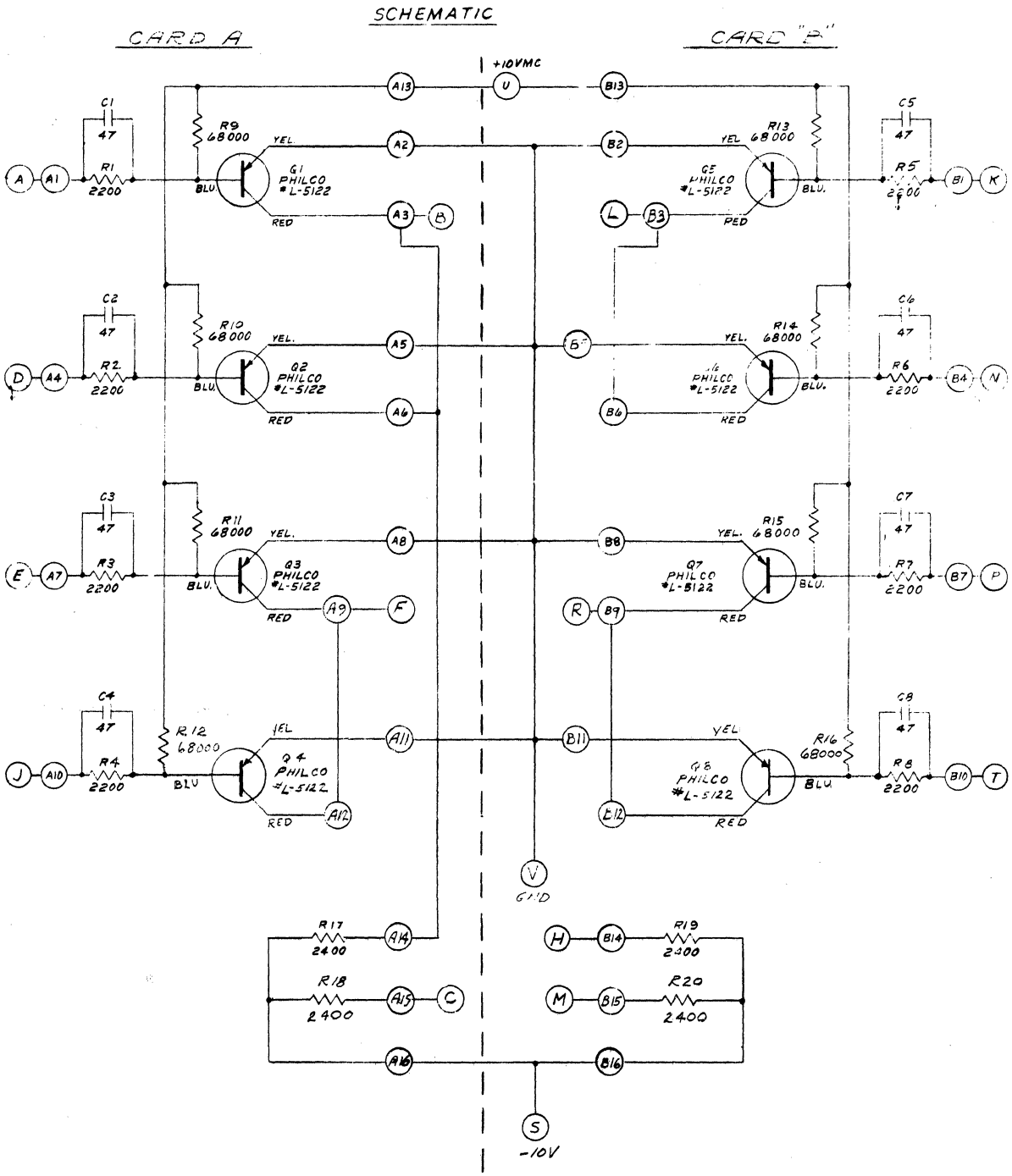


FIG. 58

PARALLEL (8) NVERTER

D-86886
"A" RED

NO. 24

INVERTER P-8

Handle Color: Red Yellow

Drawing Number: D-86886

PW Number: 63-1023

Transistors:* 8 L-5122

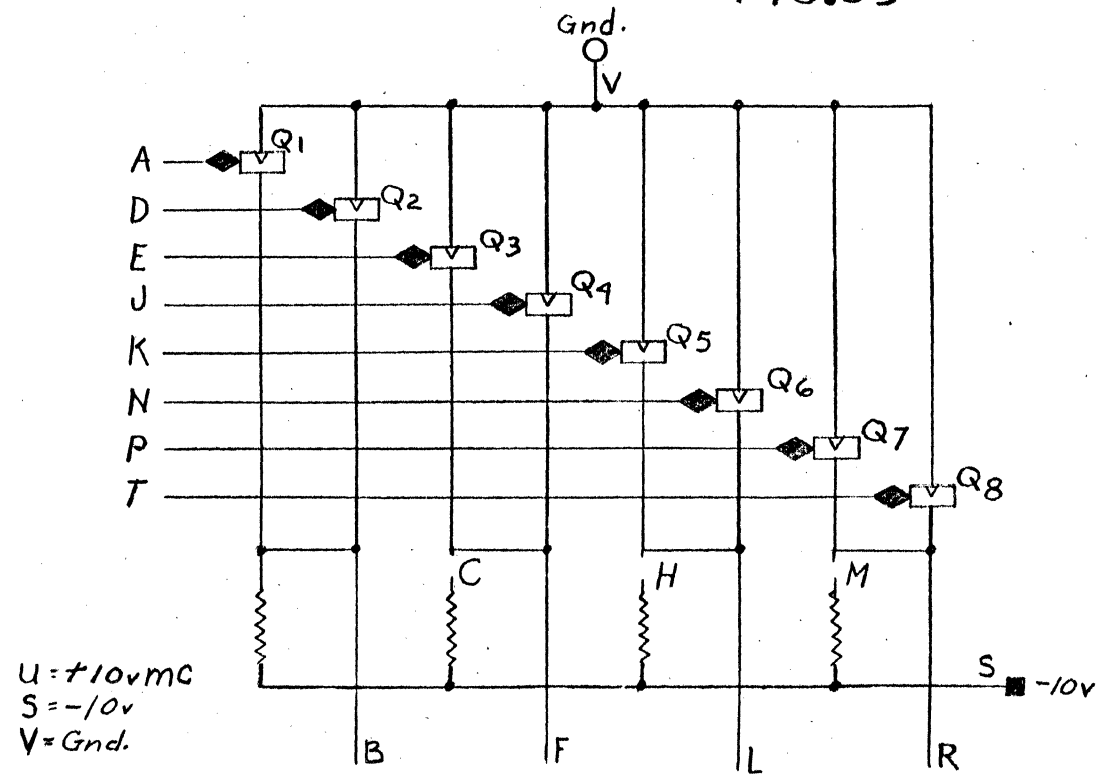
Power Supply Voltages: +10 MC; -10

Use: Inverters for logic and gating. Contains 4 load resistors.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG.59



SCHEMATIC:

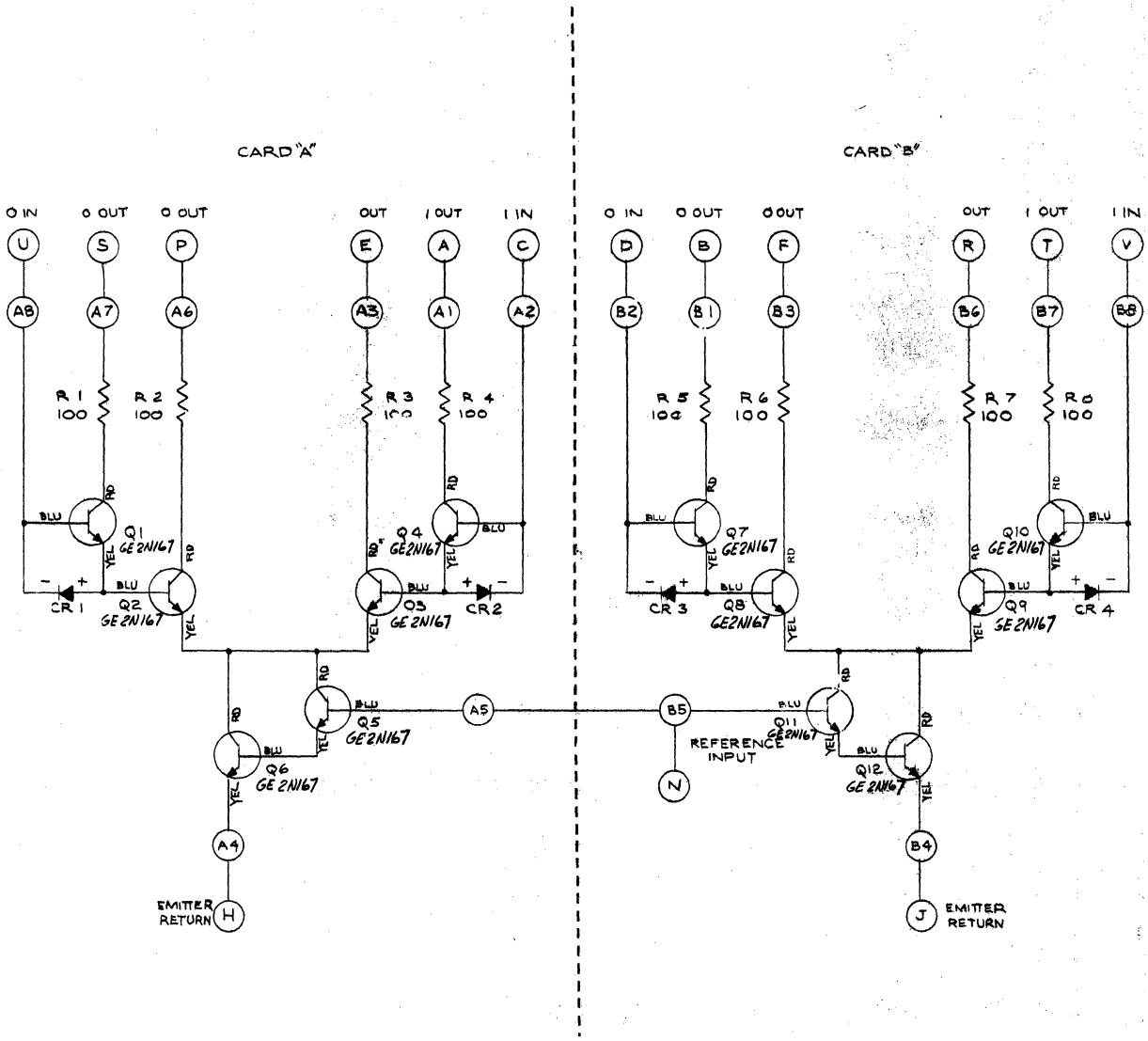


FIG. 60
TWO STAGE DECODER

D-68017
"A" - RED

NO. 26

TWO STAGE DECODER

Handle Color: Red Blue

Drawing Number: D-68017

PW Number: 63-623

Transistors:* 12 2N167

Power Supply Voltages:

Use: Decoder for high speed display
Used for first 6 bits of position decoder.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

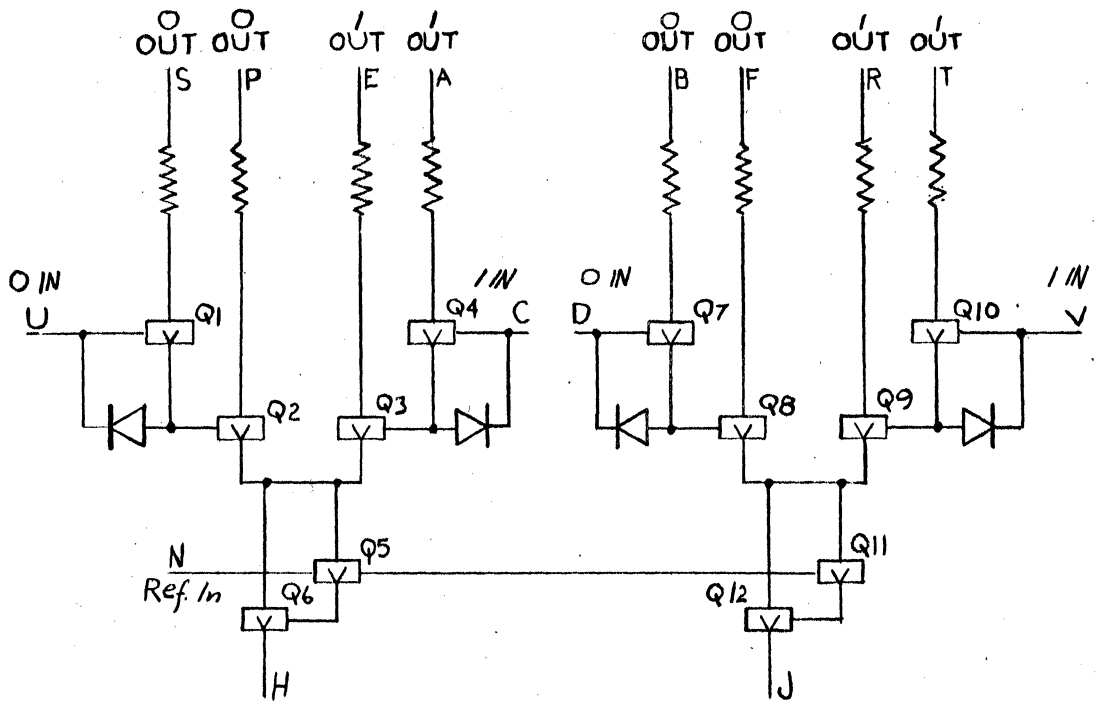


FIG. 61

SCHEMATIC

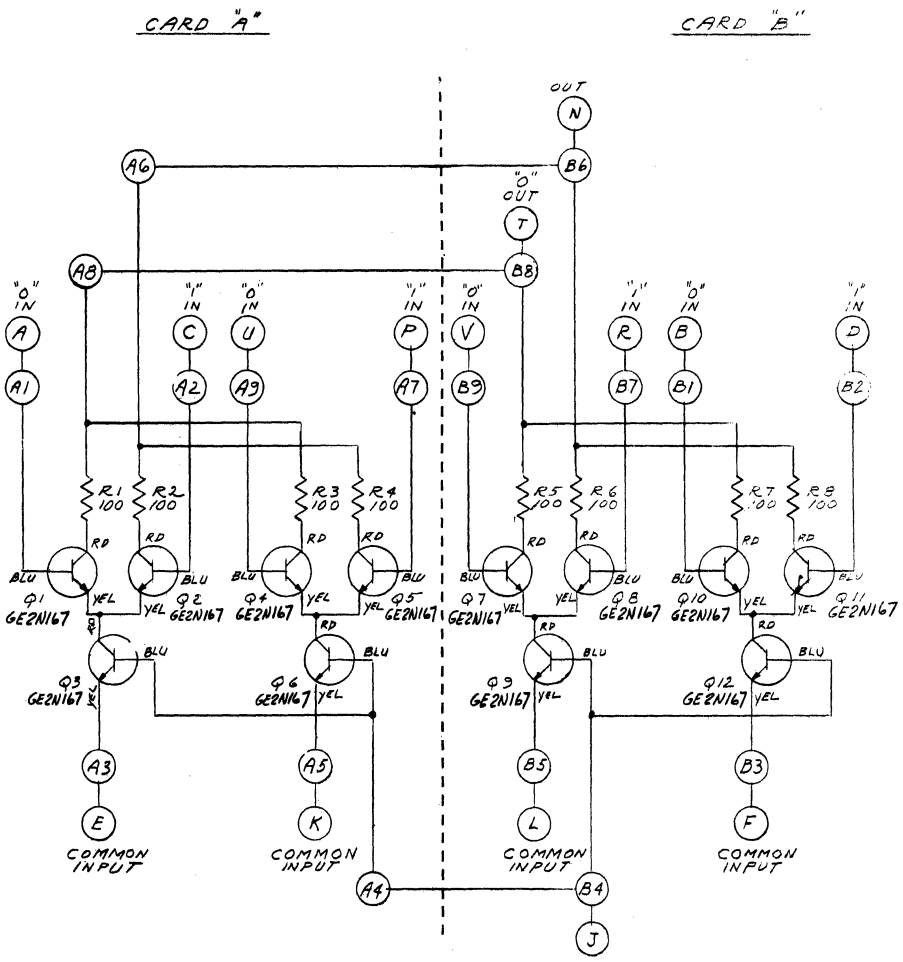


FIG. 62

FOUR STAGE DECODER

D-67993
"A"-RED

NO. 27

FOUR STAGE DECODER

Handle Color: Red Violet

Drawing Number: D-67993

PW Number: 63-621

Transistors:* 12 2N167

Power Supply Voltages:

Use: Decoder for high speed display

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

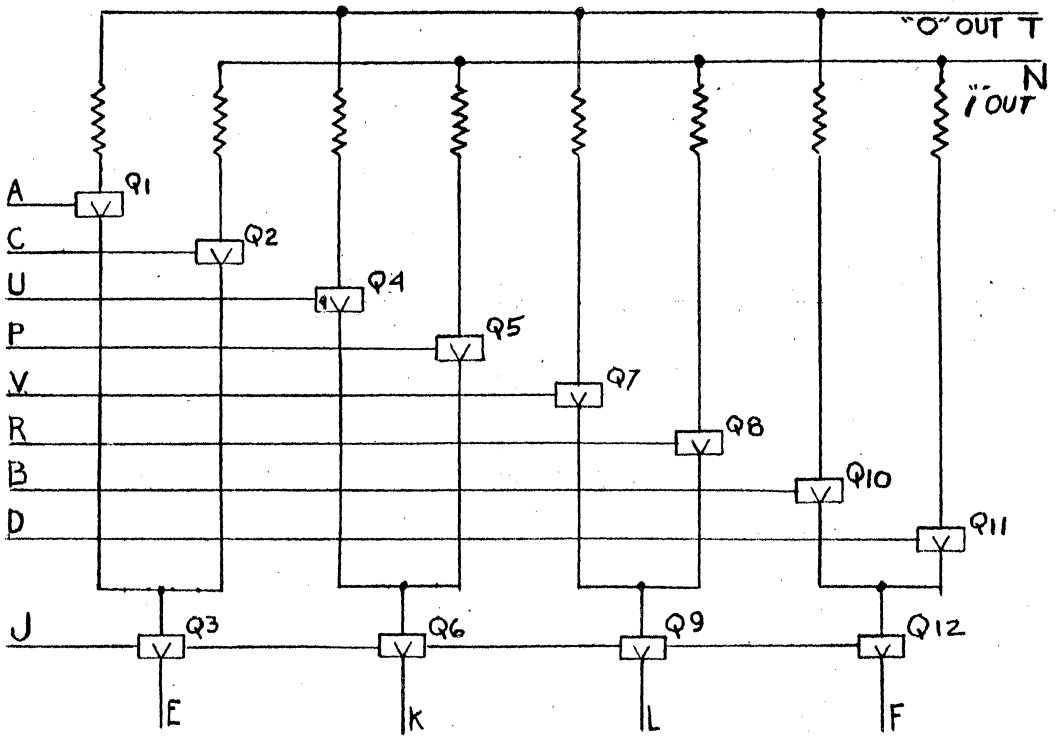


FIG. 63

SCHEMATIC:

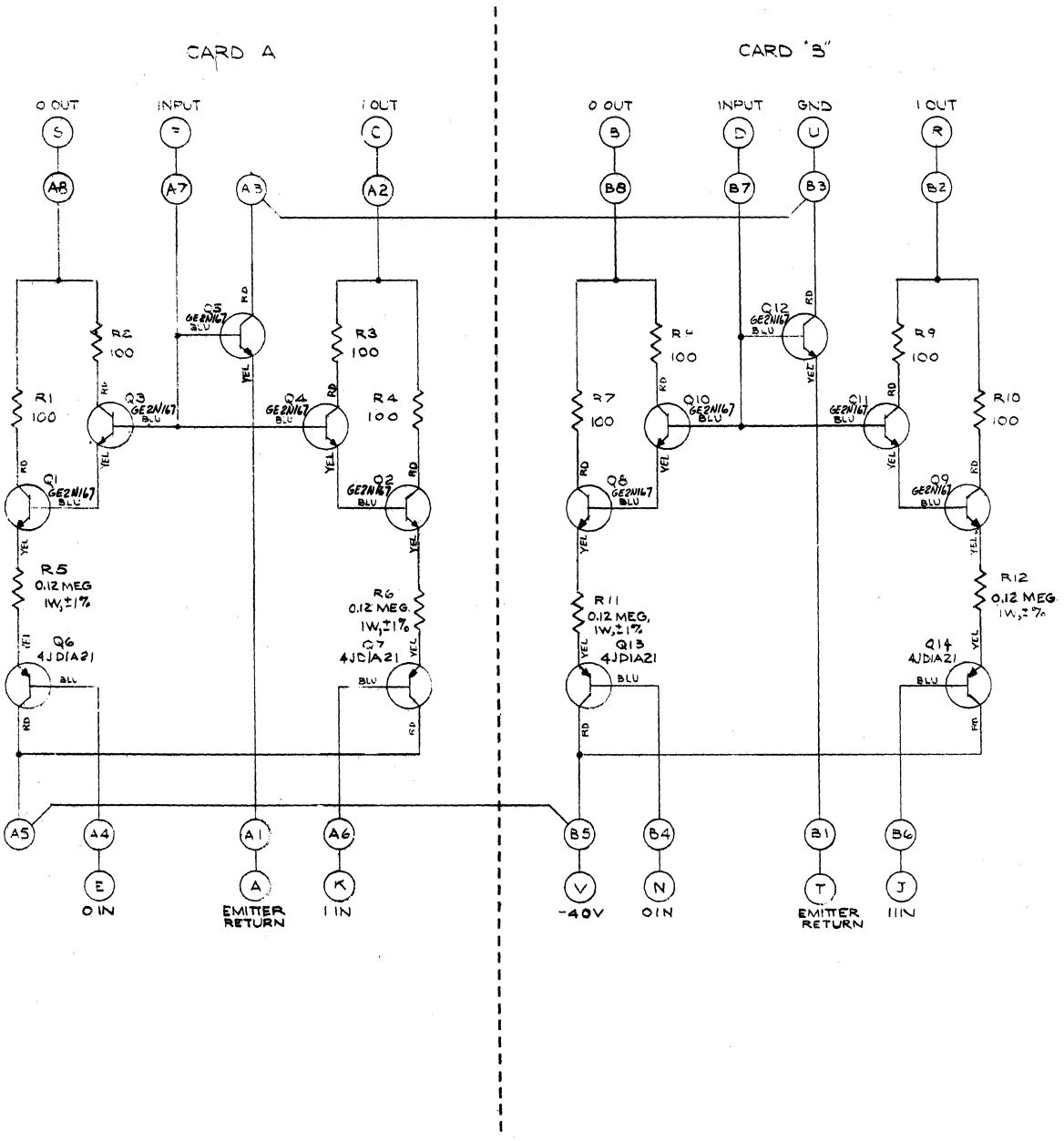


FIG. 64

POSITION DECODER

D-67844
"A"-RED

6D-2631

NO. 28

POSITION DECODER

Handle Color: Red Grey

Drawing Number: D-67844

PW Number: 63-618

Transistors:* 4 4JD1A21; 10 2N167

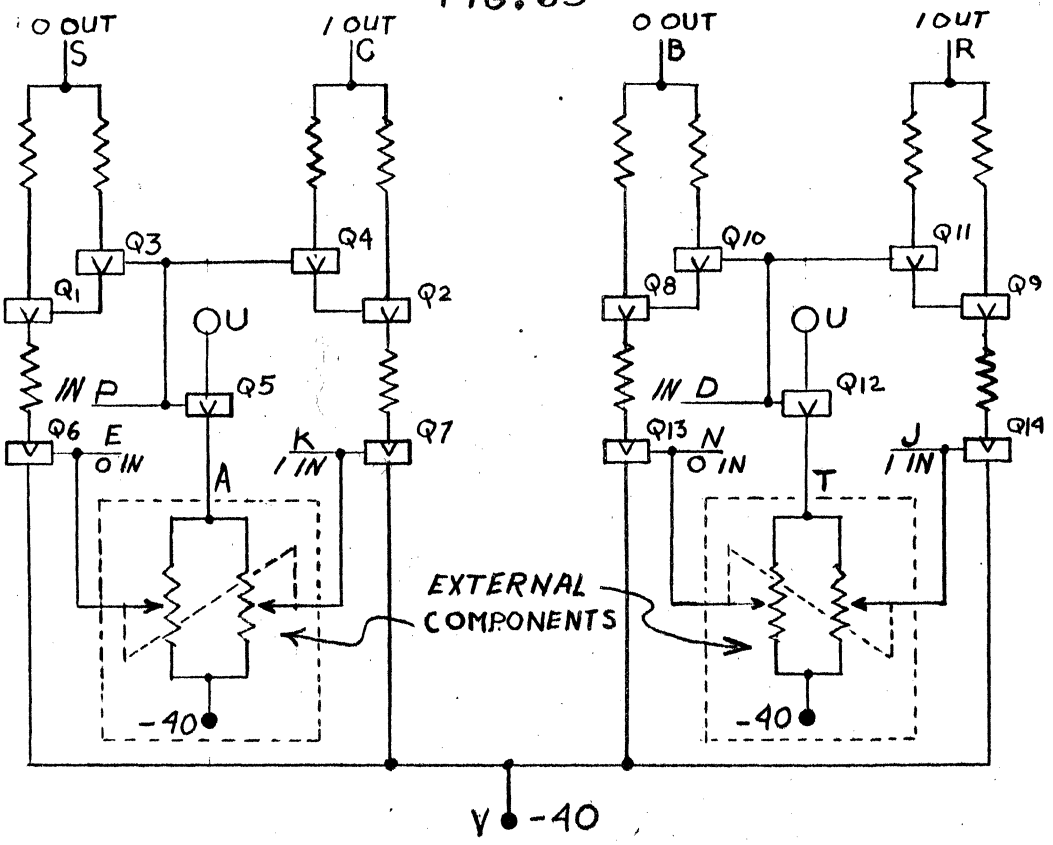
Power Supply Voltages: -40

Use: Position control stages for X and Y decoders of high speed display

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG. 65



SCHEMATIC:

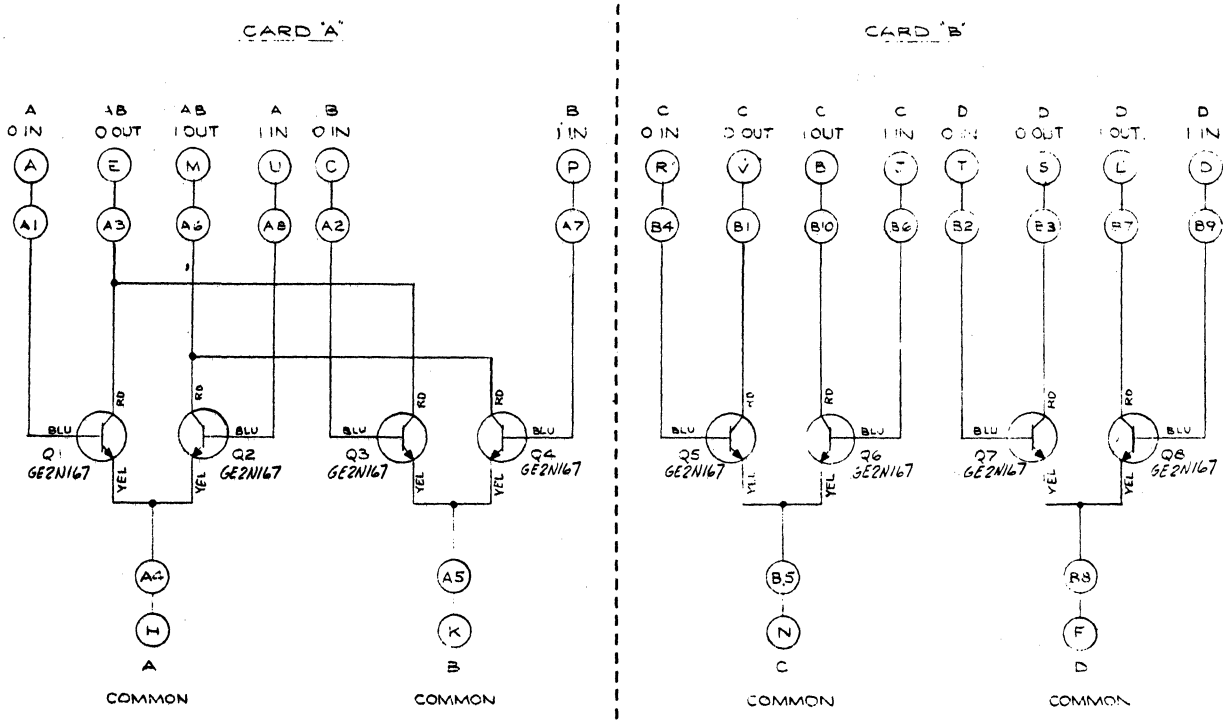


FIG. 66

FOCUS DECODER

D-67904
"A" - RED

FOCUS DECODER

Handle Color: Red White

Drawing Number: D-67904

PW Number: 63-620

Transistors:* 8 2N167

Power Supply Voltages:

Use: Used for intensity and astigmatism control for high speed display

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

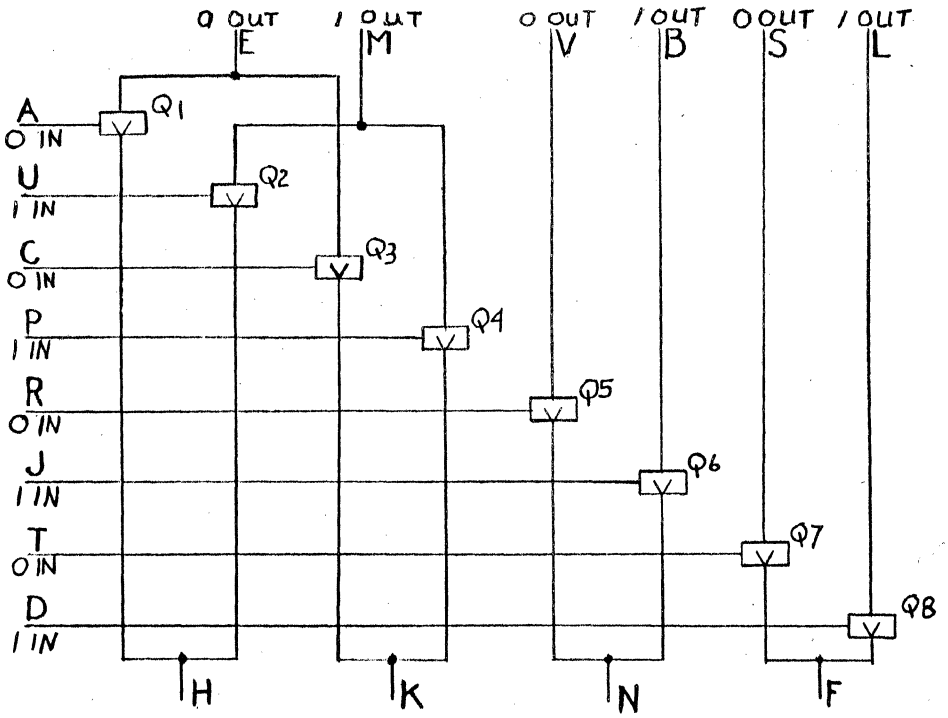


FIG. 67

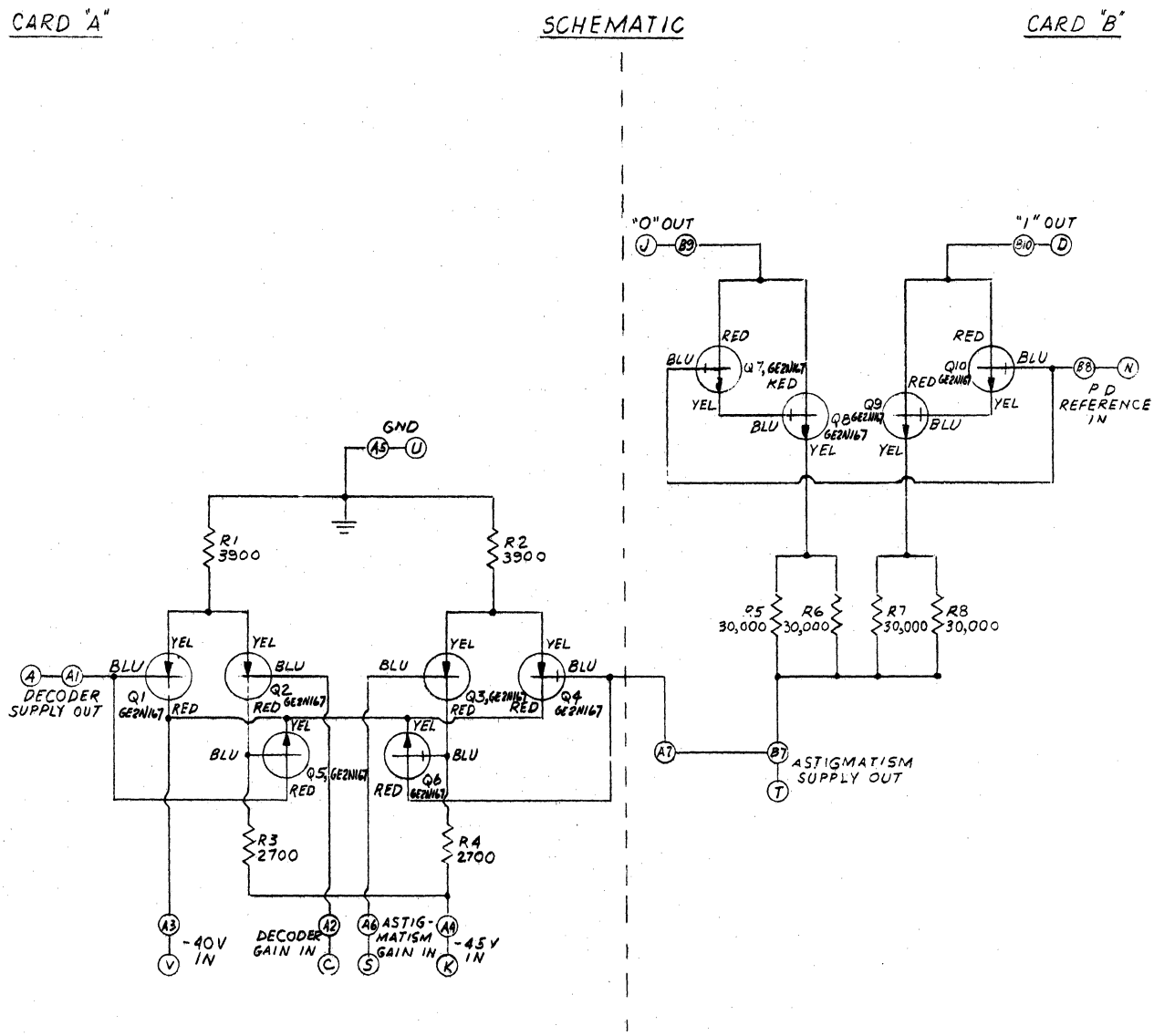


FIG. 68

DECODER GAIN SECTION

D-69151
"A"-RED

DECODER GAIN SECTION

Handle Color: Orange Black

Drawing Number: D-69151

PW Number: 63-664

Transistors:* 4 4JD1A21; 2 GT-901; 4 2N167

Power Supply Voltages: -40; -45 (both obtained from decoder power unit)

Use: Amplifier for decoder and astigmatism control for high speed display. Contains 2 series regulated power supplies and 2 decoder stages.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

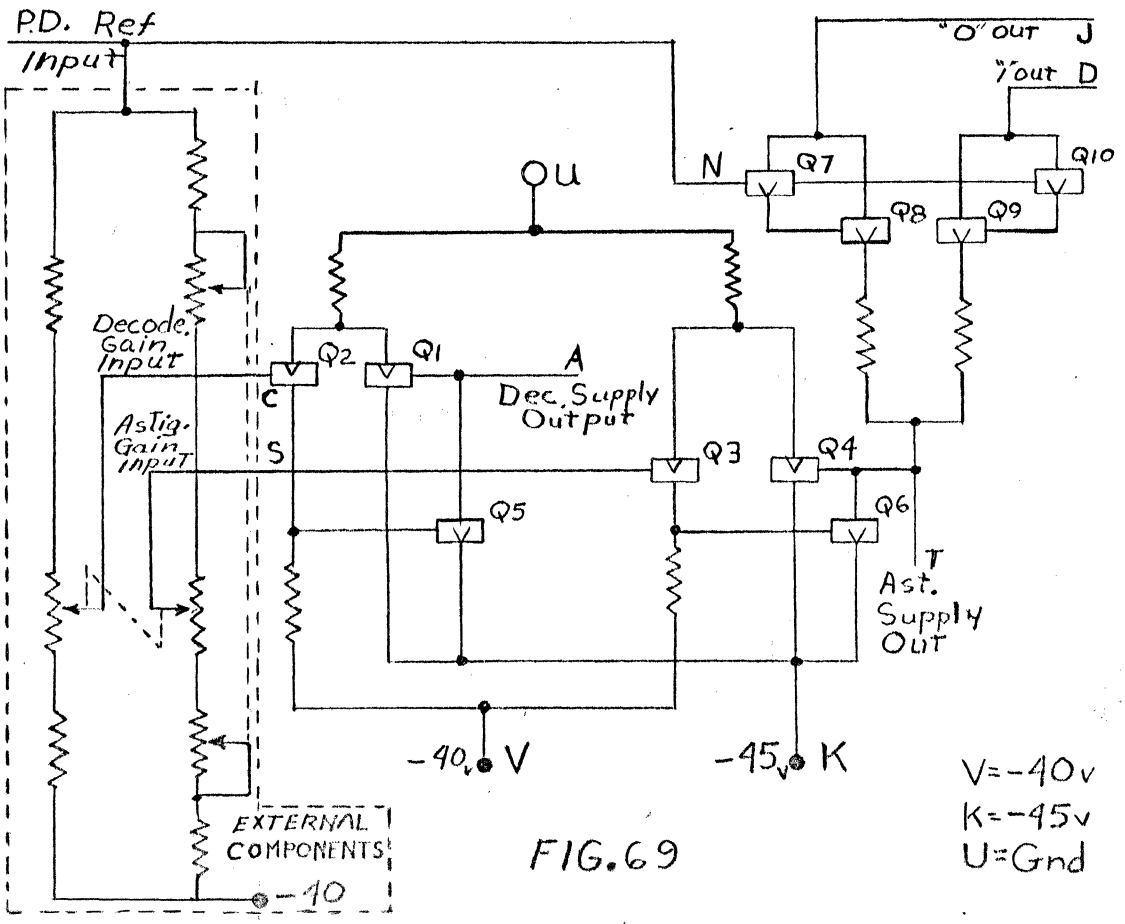


FIG. 69

SCHEMATIC

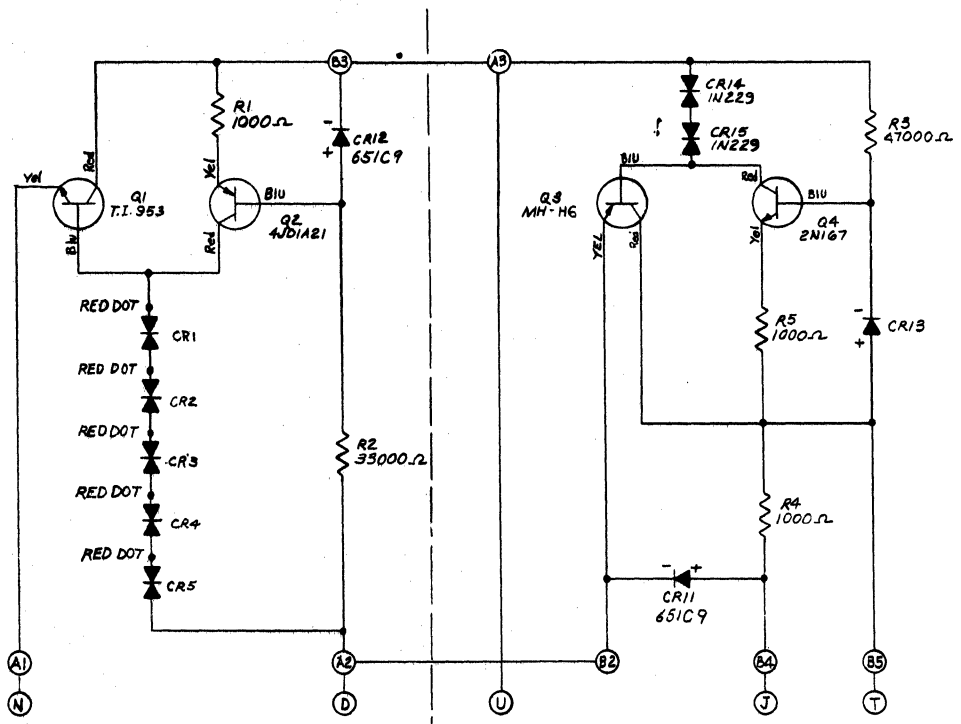


FIG. 70
DECODER POWER UNIT

0-6J152
"A" REQ.

NO. 31

DECODER POWER UNIT

Handle Color: Orange Brown

Drawing Number: D-69152

PW Number: 63-670

Transistors:* 1 4JD1A21; 1 GT-901; 1 2N167; 1 GA-52830

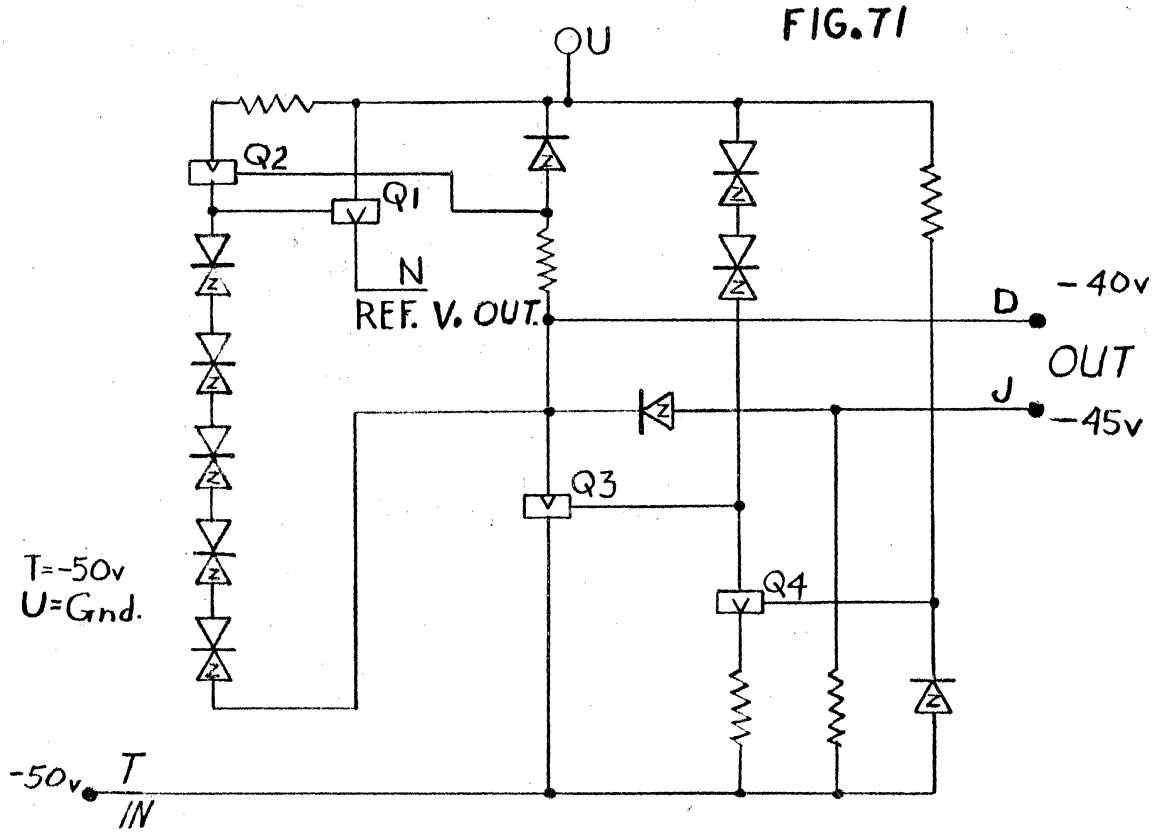
Power Supply Voltages: -50

Use: Provides -40 volts, -45 volts, and position decoder reference for decoder gain section (No. 30).

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG. 71



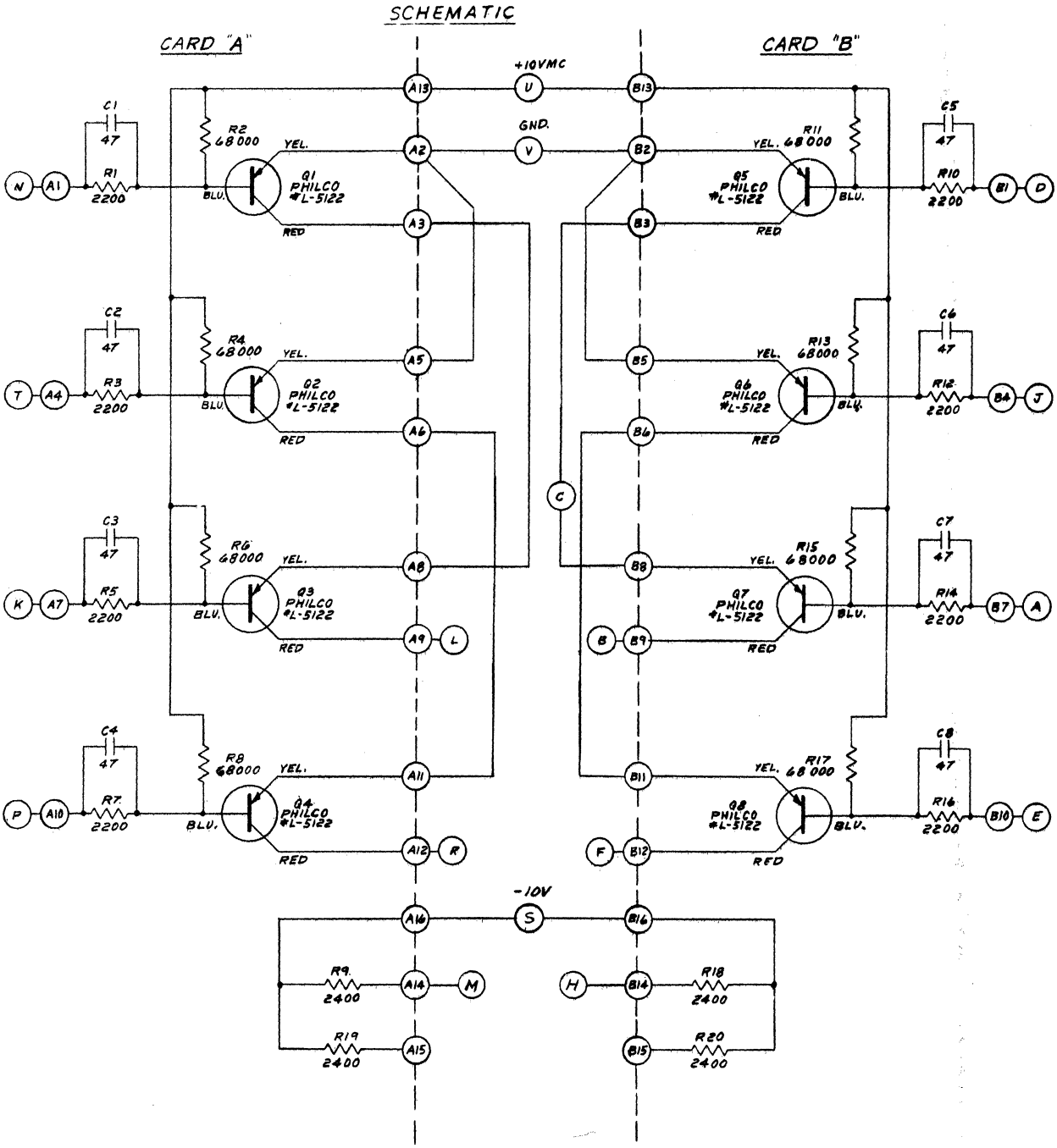


FIG. 72

SERIES (8R) INVERTER

D-86868
"A" RED

NO. 32

INVERTER S-8R

Handle Color: Orange Red

Drawing Number: D-80130 (lug); D-86868 (eyelet)

PW Number: 63-582 (lug); 63-1023 (eyelet)

Transistors:* 8 L-5122

Power Supply Voltages: +10 MC; -10

Use: Inverters for logic and gating. Contains 2 load resistors.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

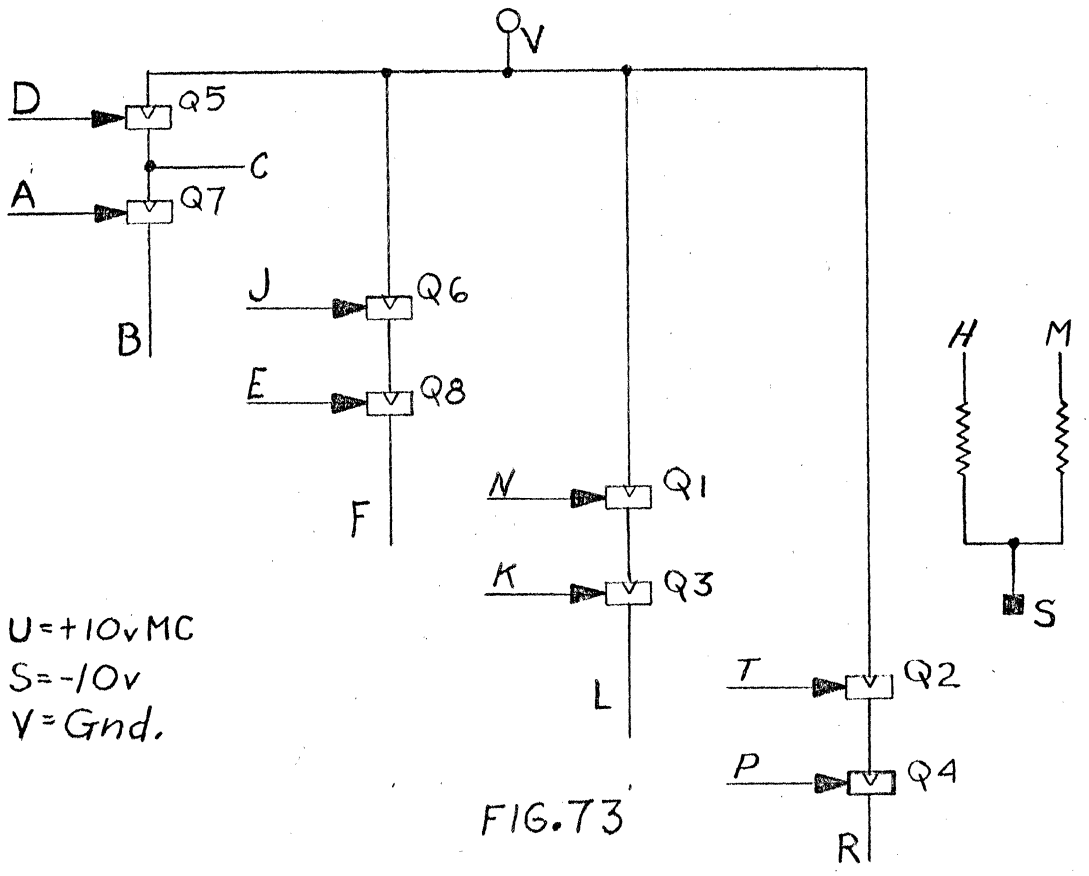


FIG. 73

SCHEMATIC:

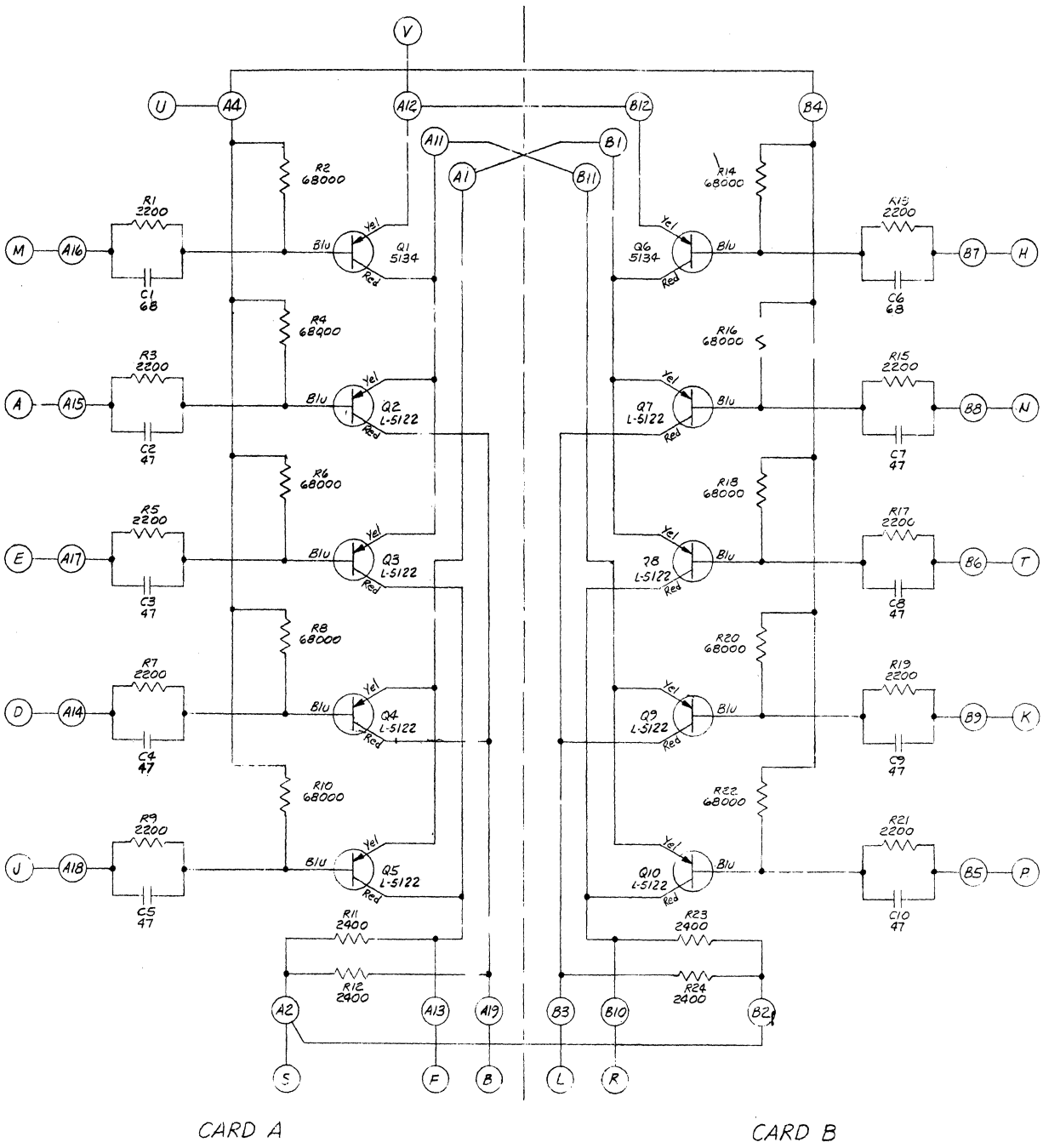


FIG. 74

PARALLEL (10) INVERTER MEMORY SELECTOR

D-81274
"A"-RED

NO. 33

INVERTER P-10

Handle Color: Orange Orange

Drawing Number: D-81274

PW Number: 63-782

Transistors:* 8 L-5122; 2 L-5134

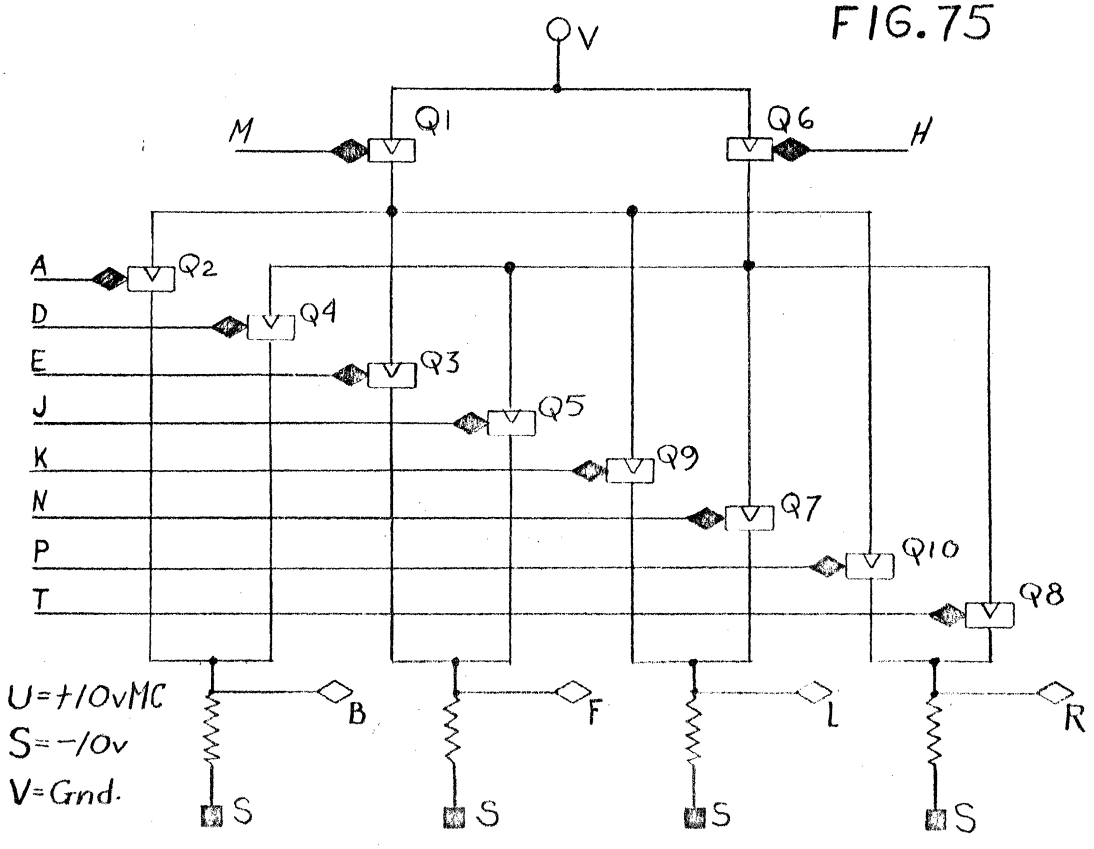
Power Supply Voltages: +10 MC; -10

Use: Inverters for logic and gating. Used as memory selector for S memory. Contains 4 load resistors.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG. 75



CARD A

SCHEMATIC:

CARD B

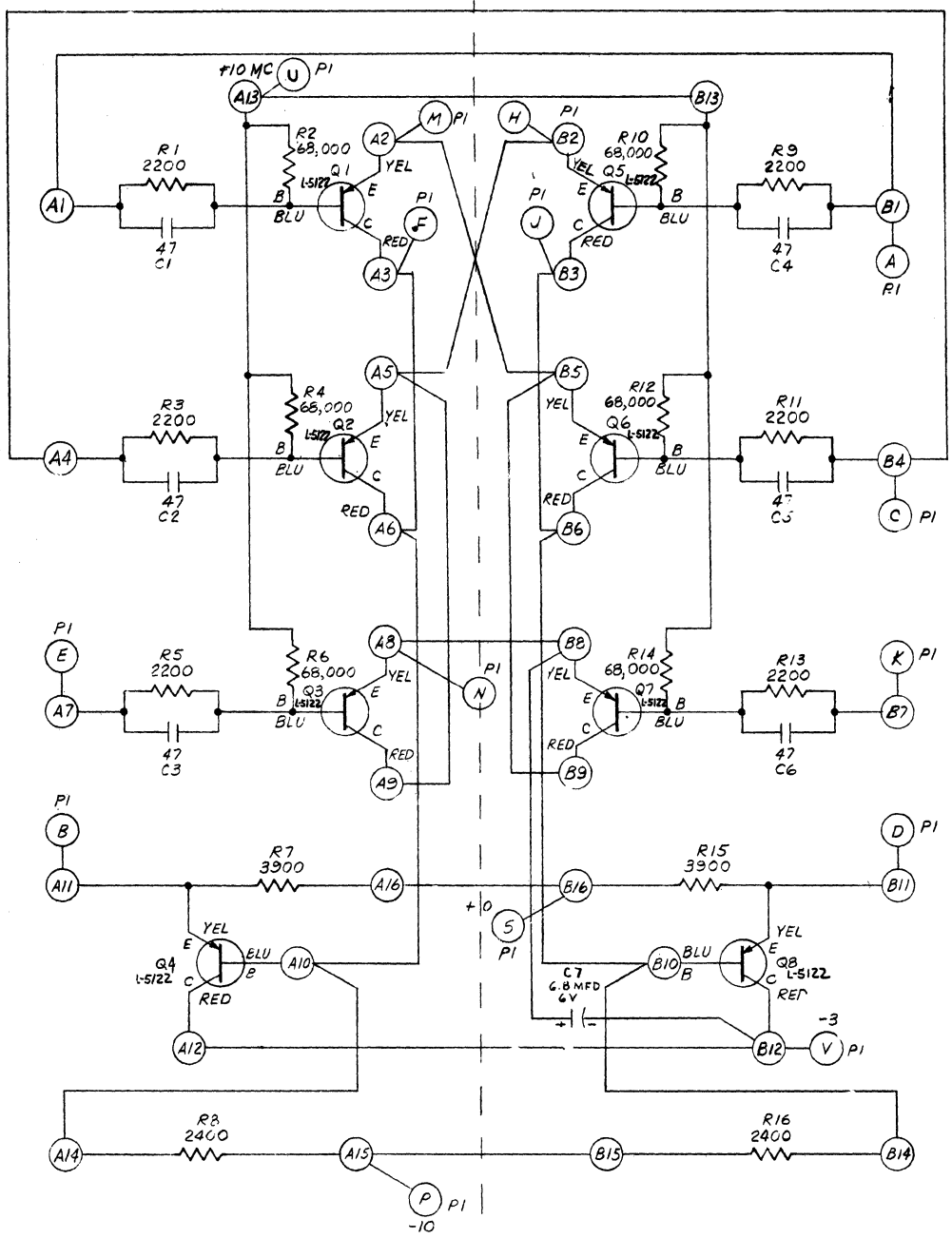


FIG. 76

PARITY CIRCUIT

D-81271
"A"-RED

PARITY CIRCUIT

Handle Color: Orange Yellow

Drawing Number: D-81271

PW Number: 63-786

Transistors:* 8 L-5122

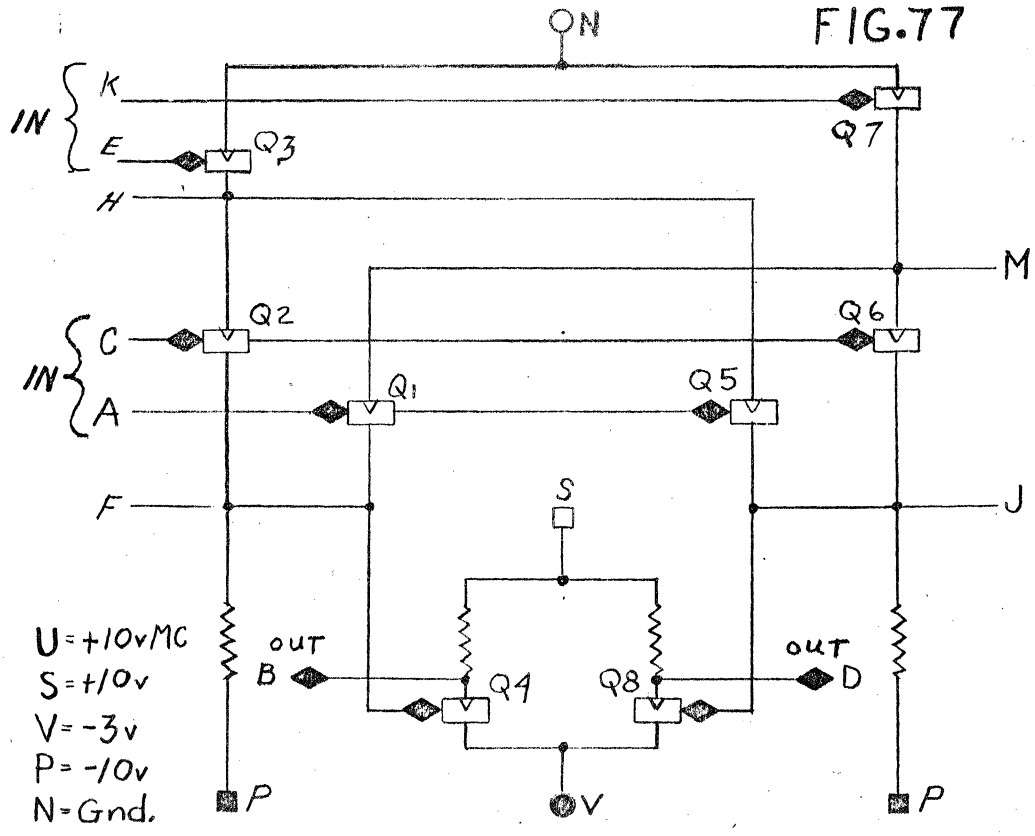
Power Supply Voltages: +10 MC; +10; -3; -10

Use: 6 inverters are 2 emitter followers used in M and N register parity circuits. Contains 2 load resistors for inverters, and 2 for emitter followers.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG.77



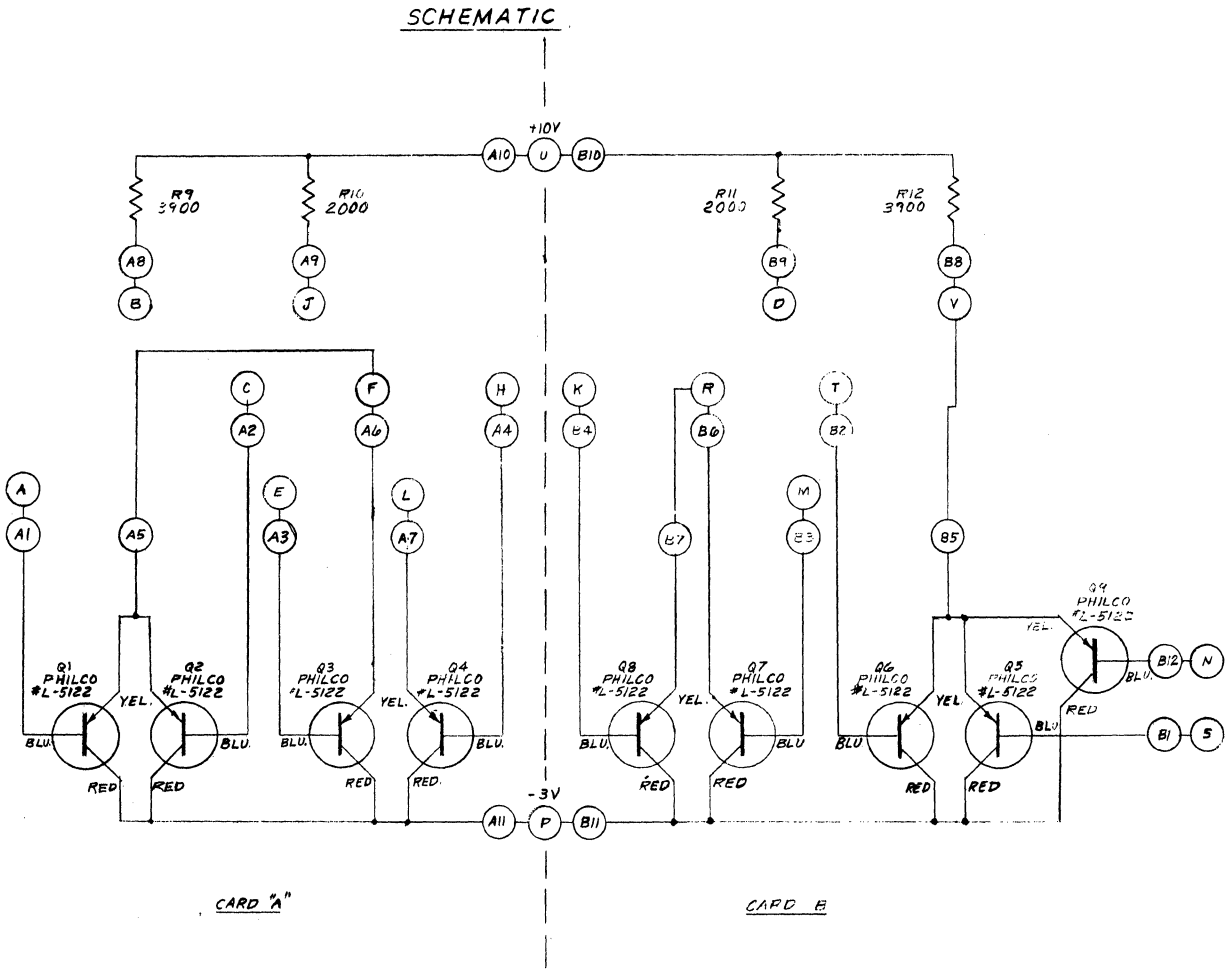


FIG. 78

(9) TRANSISTOR EMITTER FOLLOWER

D-86828
"A" RED

EMITTER FOLLOWER 9

Handle Color: Orange Green

Drawing Number: D-84151 (lug); D-86828 (eyelet)

PW Number: 63-581 (lug); 63-1021 (eyelet)

Transistors:* 9 L-5122

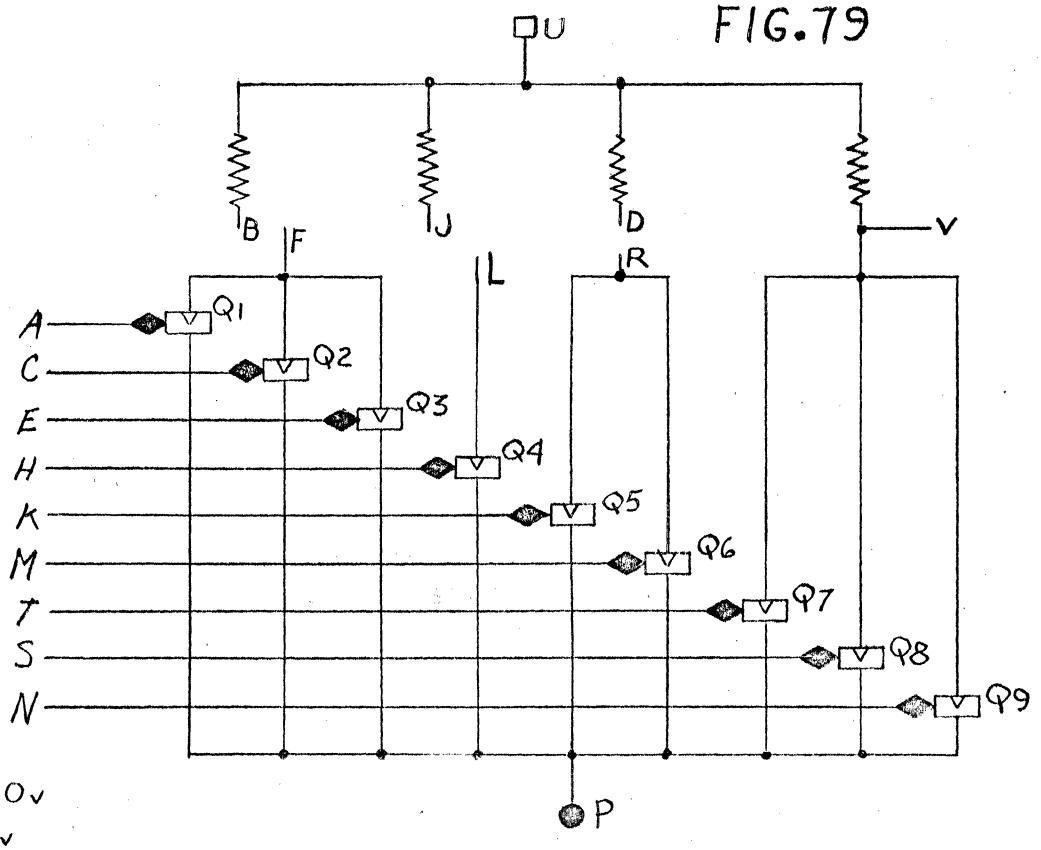
Power Supply Voltages: +10; -3

Use: Emitter followers for logic and current amplification. Contains 4 load resistors.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG. 79



SCHEMATIC:

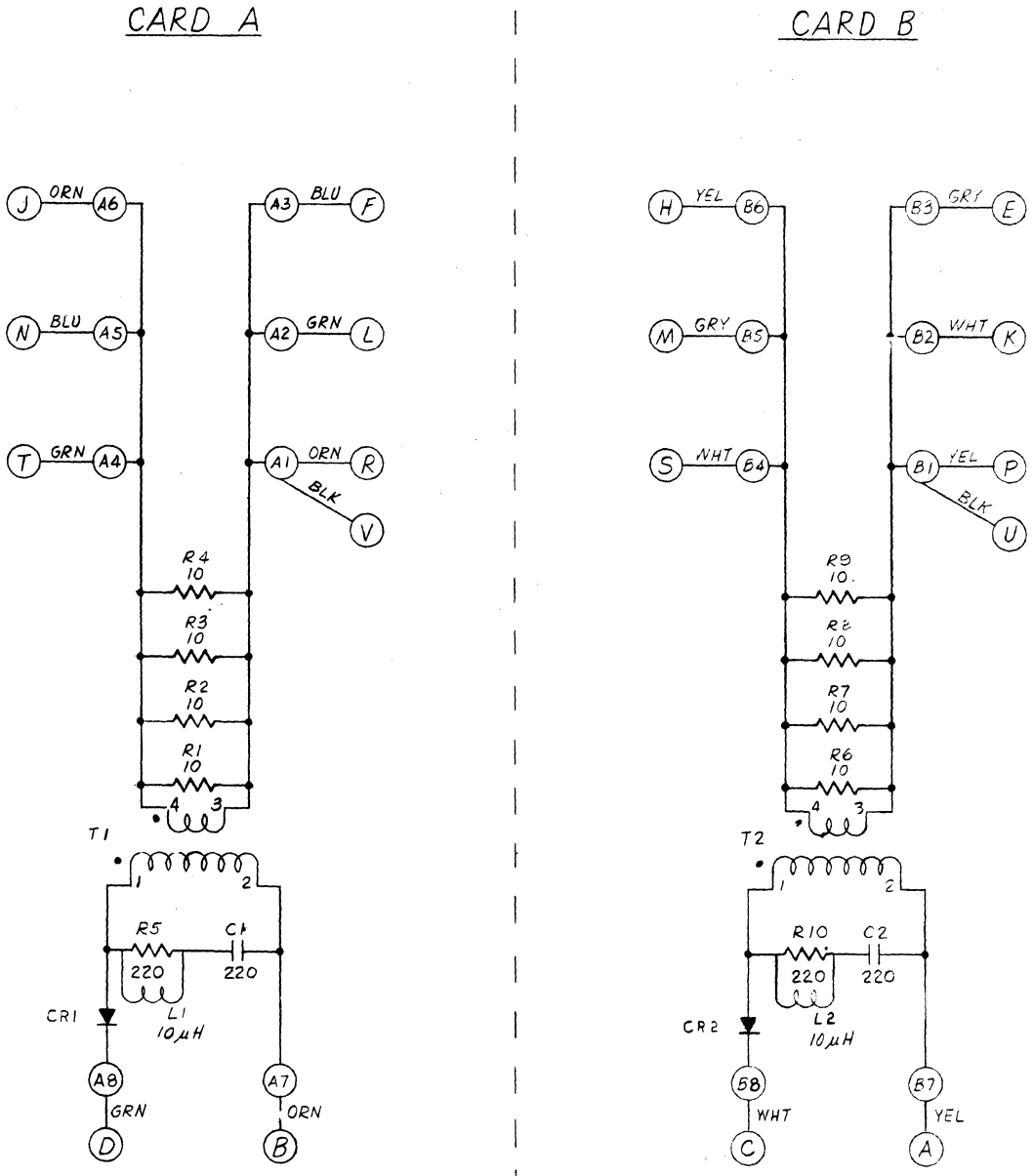


FIG. 80

PULSE TRANSFORMER

D-82342
"A"-RED

PULSE TRANSFORMER

Handle Color: Orange Blue

Drawing Number: D-82342

PW Number: 63-841

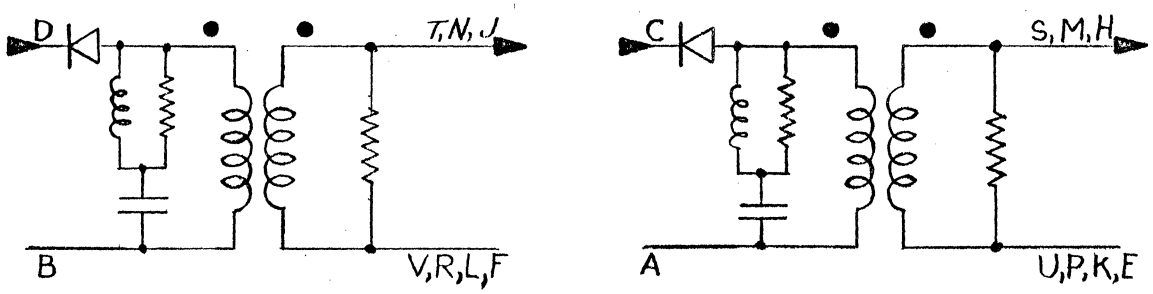
Transistors:*

Power Supply Voltages:

Use: Input: 30 volt 0.1 μsec negative pulse from vacuum tube clock.
Output: 3 volt 0.1 μsec negative pulse to transistor register drivers.

Remarks: Contains two pulse transformers and terminations per PIU.

*All transistor type numbers are identified with manufacturer in appendix



U
V = Gnd.

FIG. 81

SCHEMATIC:

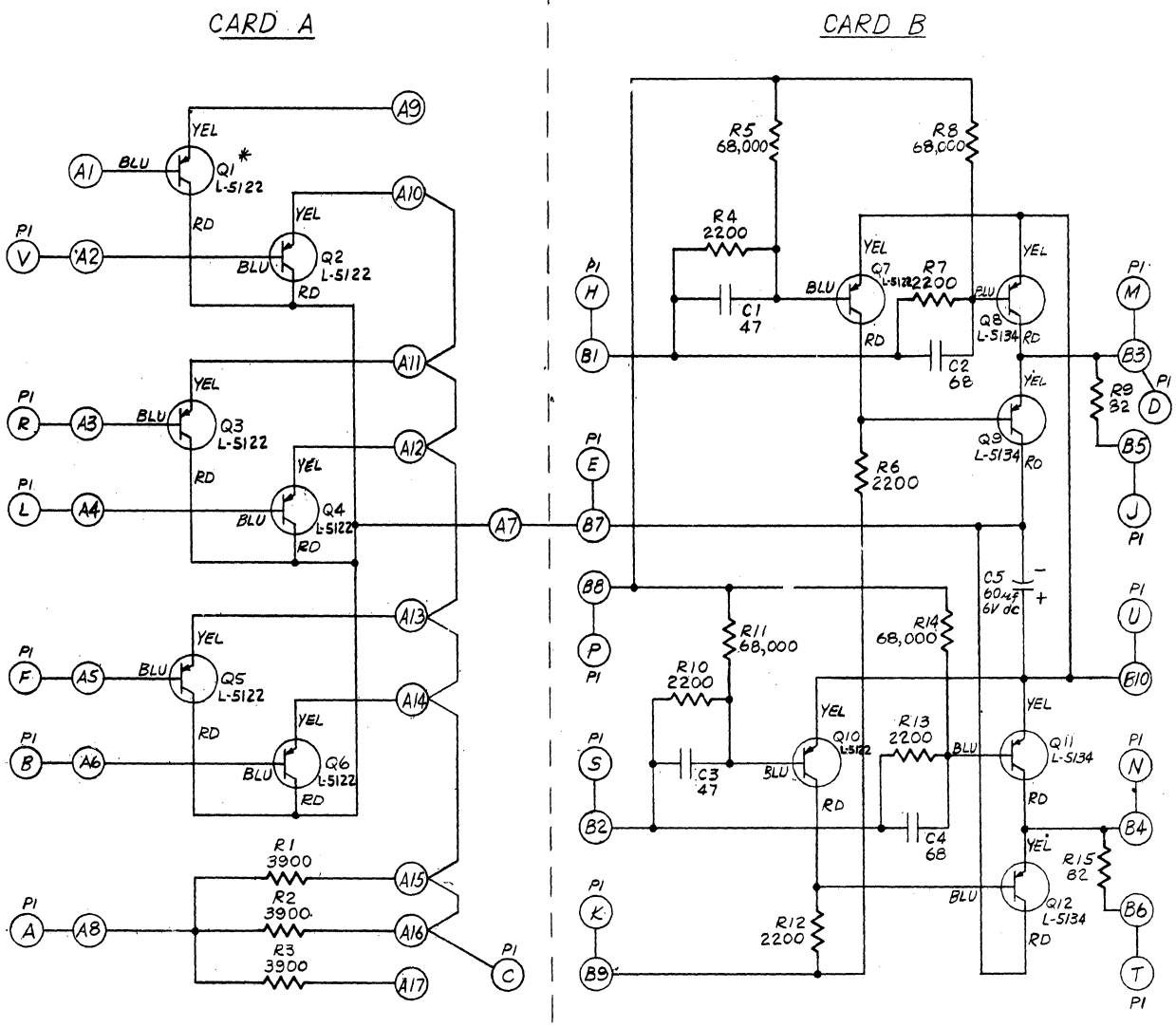


FIG. 82

TIME LEVEL DECODER

D - 82308
"A" REV

TIME LEVEL DECODER

Handle Color: Orange Violet

Drawing Number: D-82908

PW Number: 63-871; 63-514

Transistors:* 7 L-5122; 4 L-5134

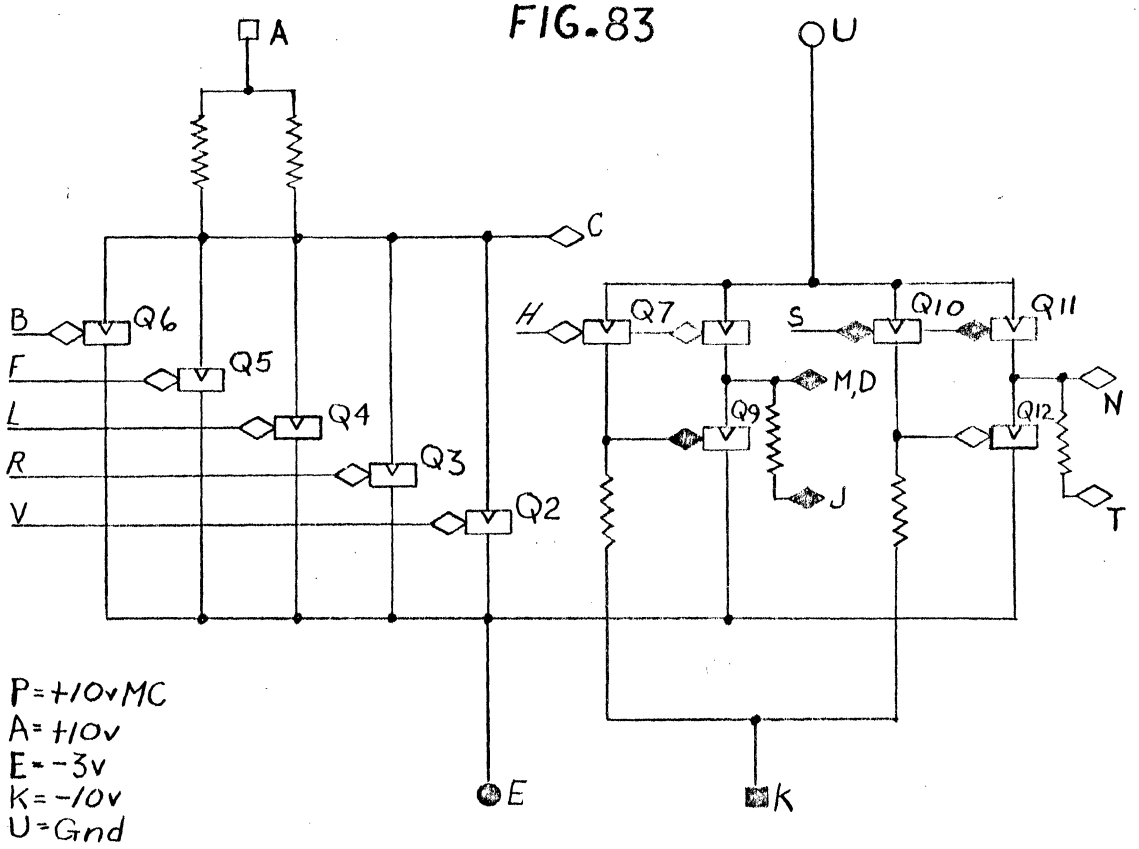
Power Supply Voltages: +10 MC; +10; -3; -10

Use: 5-way emitter follower AND circuit used as decoder followed by 2 Cascode circuits.

Remarks: Both ground and -3 volt outputs are obtainable.

*All transistor type numbers are identified with manufacturer in appendix

FIG. 83



SCHEMATIC
CARD-A

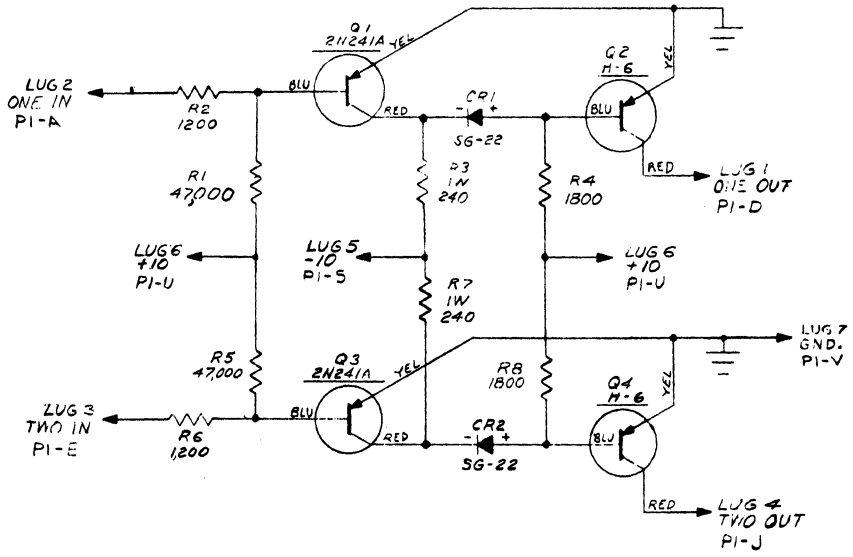


FIG. 84

SOLENOID DRIVER

D-84655
"A" REV

NO. 38

SOLENOID DRIVER

Handle Color: Orange Grey

Drawing Number: D-84655

PW Number: 61-874

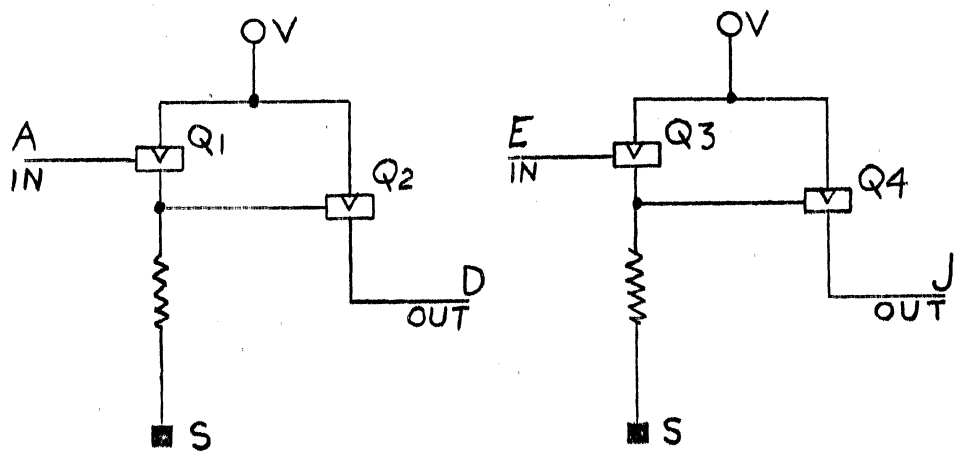
Transistors:* 2 2N241A; 2 H-6 (2N539)

Power Supply Voltages: +10; -10

Use: Power amplifier to drive solenoids in electric typewriter

Remarks: Maximum output current: 600 ma
Maximum output voltage: 30 volts

*All transistor type numbers are identified with manufacturer in appendix



U=+10v
S=-10v
V=Gnd.

FIG. 85

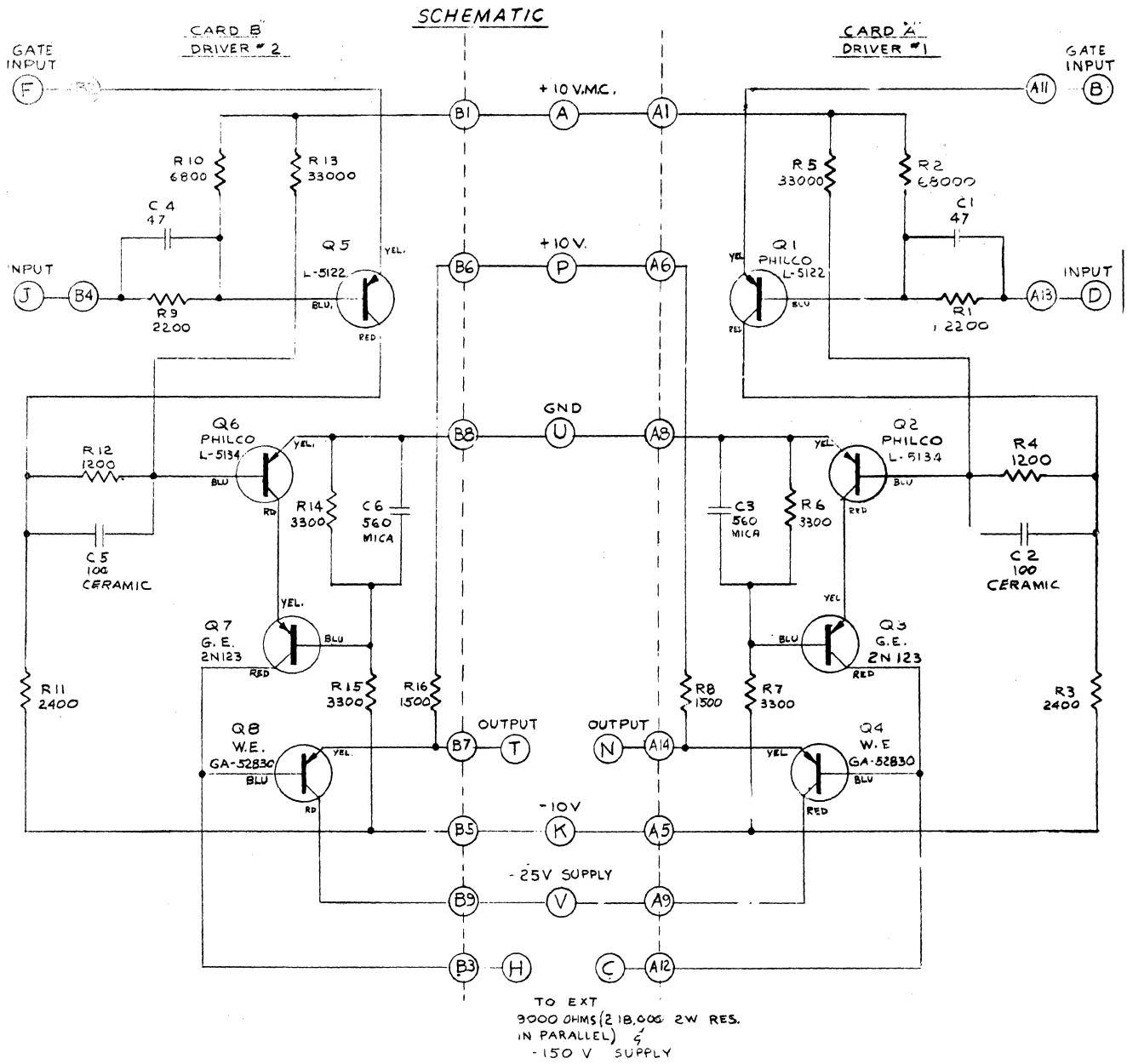


FIG. 86

TOGGLE SWITCH STORAGE RESISTOR DRIVER

D-82581
"A" - RED

NO. 39

TSS RESISTOR DRIVER

Handle Color: Orange White

Drawing Number: D-82581

PW Number: 63-883

Transistors:* 2 L-5122; 2 L-5134; 2 2N123; 2 GA-52830

Power Supply Voltages: +10 MC; +10; -10; -25 (From TSS Power Unit)

Use: Provides drive current for resistor decoder network of toggle switch storage.

Remarks: Requires external 9000 ohm resistor connected to -150 volt power supply. 2 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

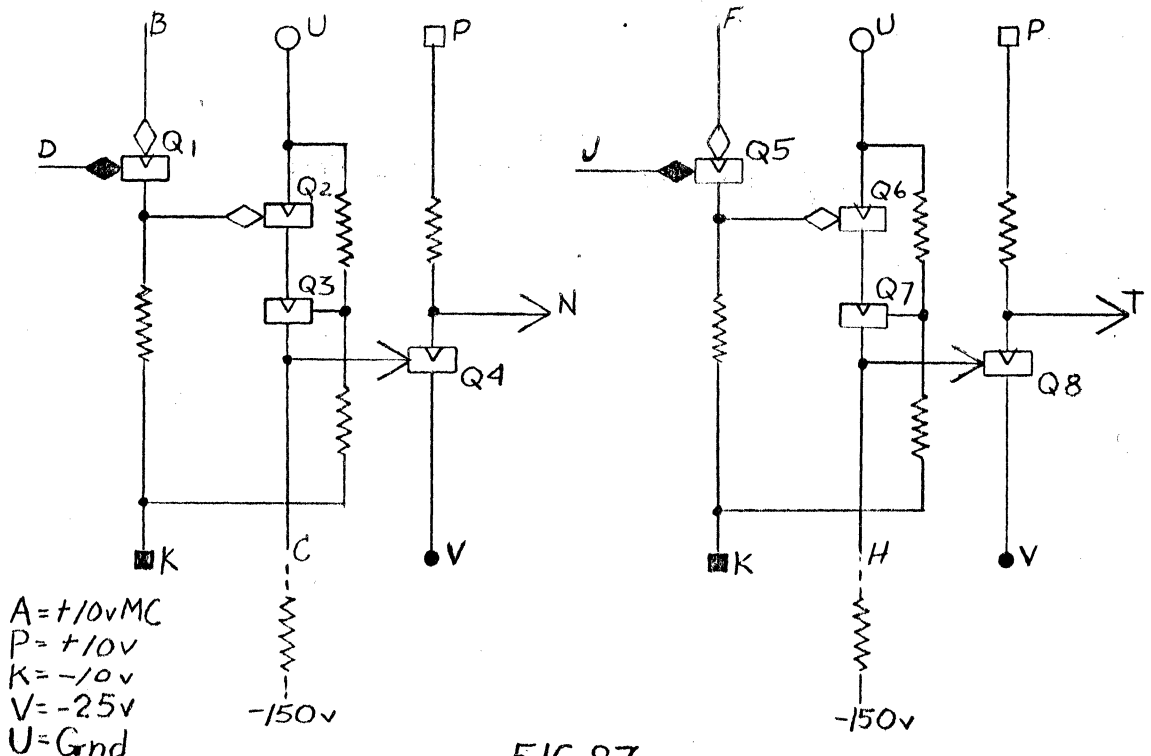


FIG.87

SCHEMATIC

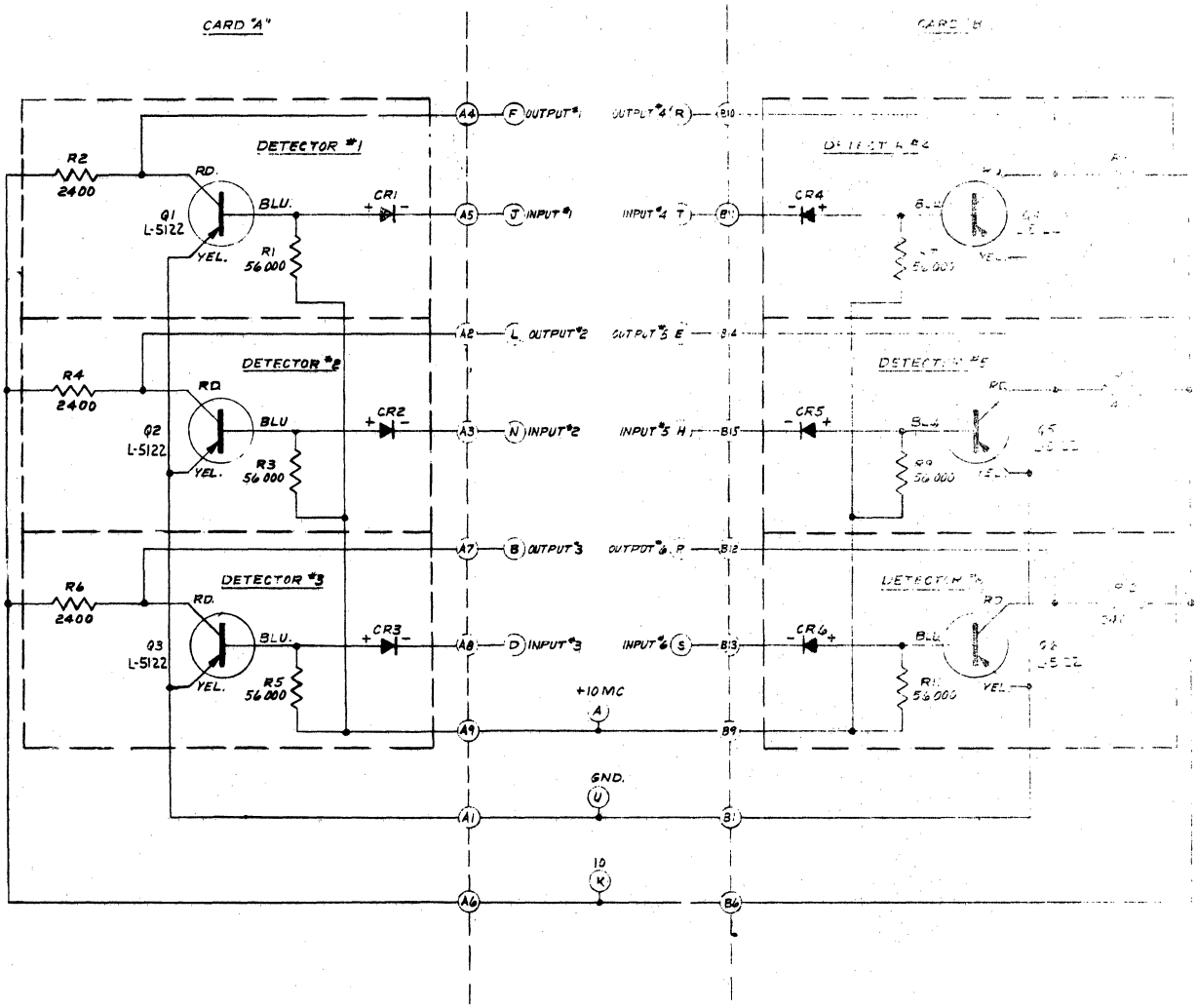


FIG. 88

TOGGLE SWITCH STORAGE DIGIT DETECTOR

D-83557
"A" Pen.

TSS DIGIT DETECTOR

Handle Color: Yellow Black

Drawing Number: D-82557

PW Number: 63-886

Transistors:* 6 L-5122

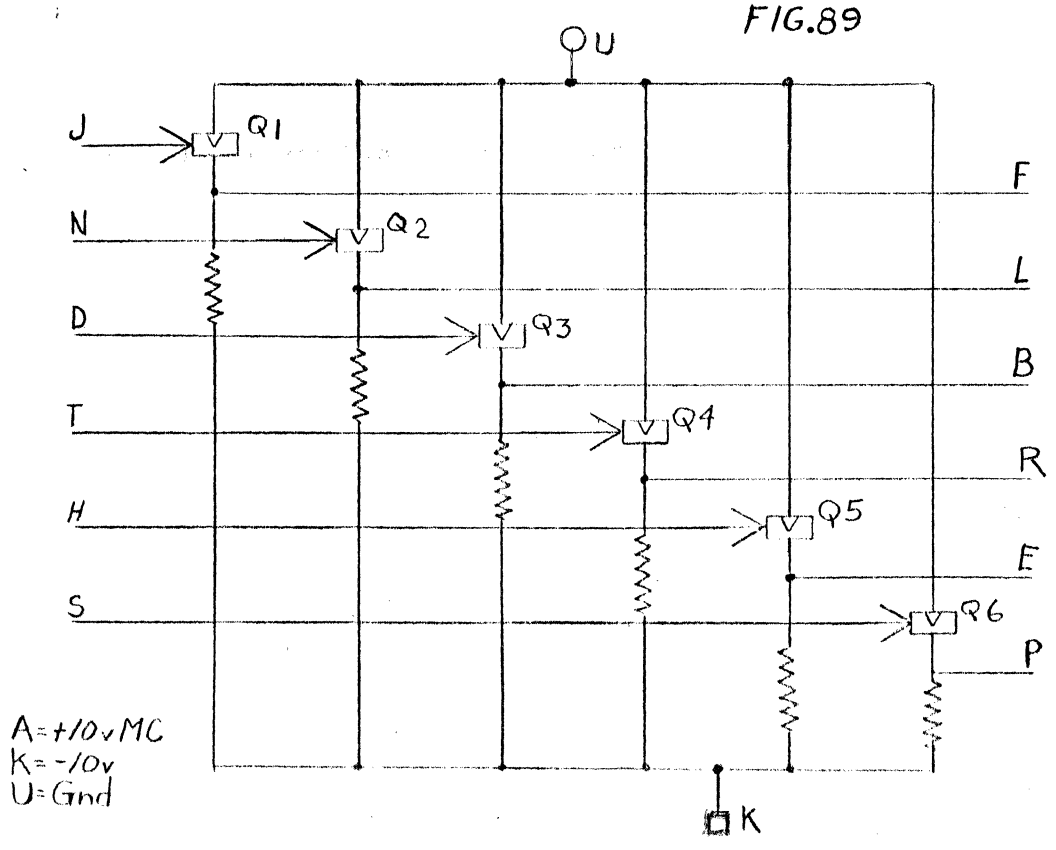
Power Supply Voltages: +10 MC; -10

Use: Detects selected digits in toggle switch storage.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG.89



SCHEMATIC

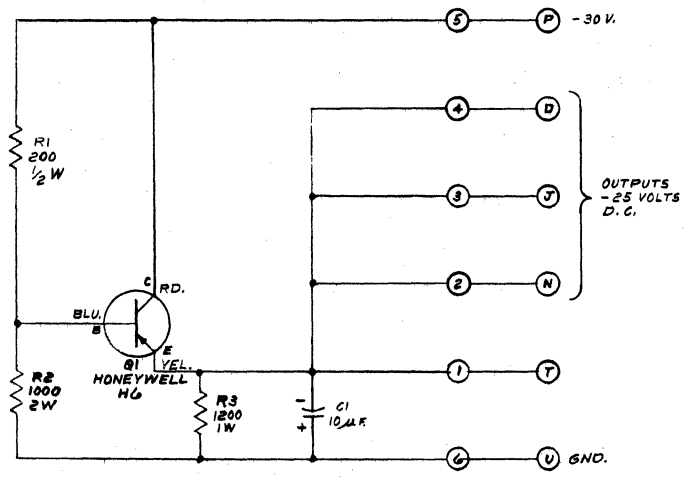


FIG. 90

TOGGLE SWITCH STORAGE 25V . POWER SUPPLY

D-8269
1/4" RED

NO. 41

TSS POWER UNIT

Handle Color: Yellow Brown

Drawing Number: D-82691

PW Number: 63-884

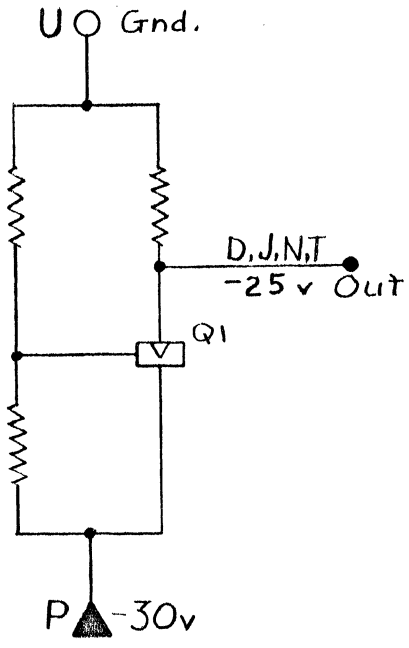
Transistors:* 1 H-6 (2N539)

Power Supply Voltages: -30

Use: Provides -25 volts for TSS resistor driver (No. 39)

Remarks:

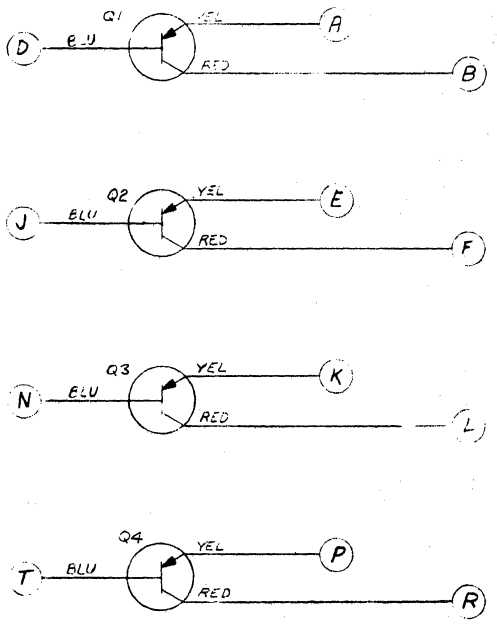
*All transistor type numbers are identified with manufacturer in appendix



P=-30v.

FIG. 91

SCHEMATIC



NOTE:
TRANSISTORS ARE MINNEAPOLIS HONNEYWELL H-6

FIG. 92
FOUR H-6

D-84761
"A" REQ.

NO. 42

FOUR H-6

Handle Color: Yellow Red

Drawing Number: D-84761

PW Number:

Transistors:* 4 H-6 (2N539)

Power Supply Voltages:

Use: Power Amplifier. Used in electric typewriter circuitry

Remarks: Maximum collector current per transistor: 2 amps
Maximum collector-emitter voltage: 60 volts

*All transistor type numbers are identified with manufacturer in appendix

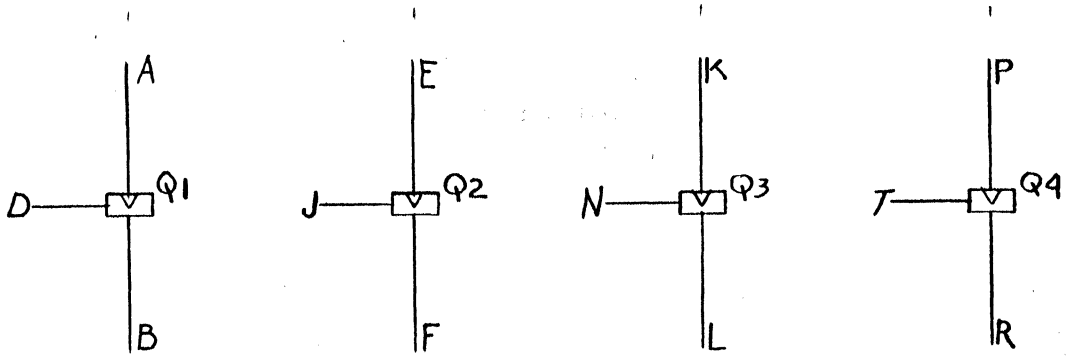
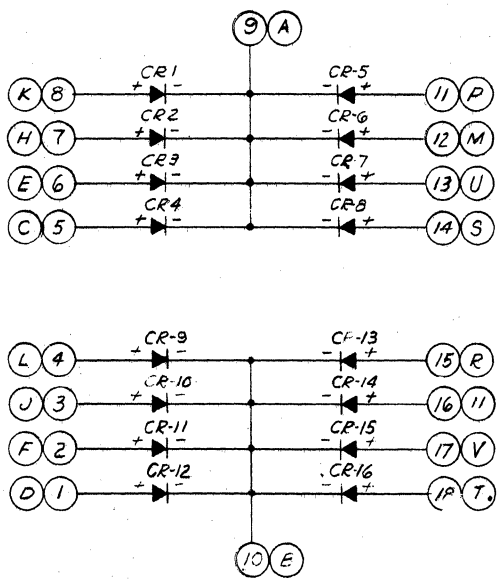


FIG. 93

SCHEMATIC



NOTES:
1. ALL DIODES ARE TYPE IN537 (SILICON) G.E.

FIG. 94

TYPEWRITER DIODE

D-85686
"A"-RED

NO. 44

TYPEWRITER DIODE

Handle Color: Yellow Yellow

Drawing Number: D-85686

PW Number: 63-924

Transistors:*

Power Supply Voltages:

Use: Contains 16 GE Silicon 1N537 diodes used in electric typewriter circuitry.

Remarks: Maximum current 750 ma PIV = 100 volts

*All transistor type numbers are identified with manufacturer in appendix

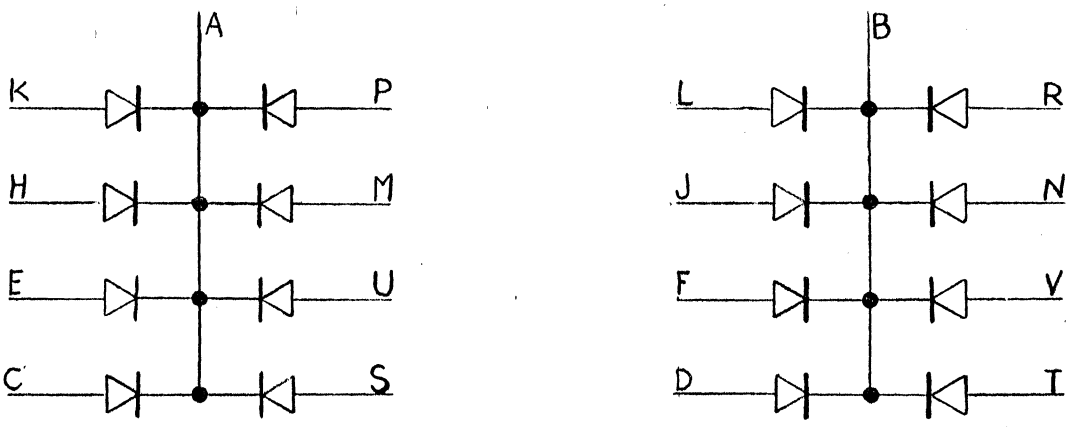


FIG. 95

SCHEMATIC

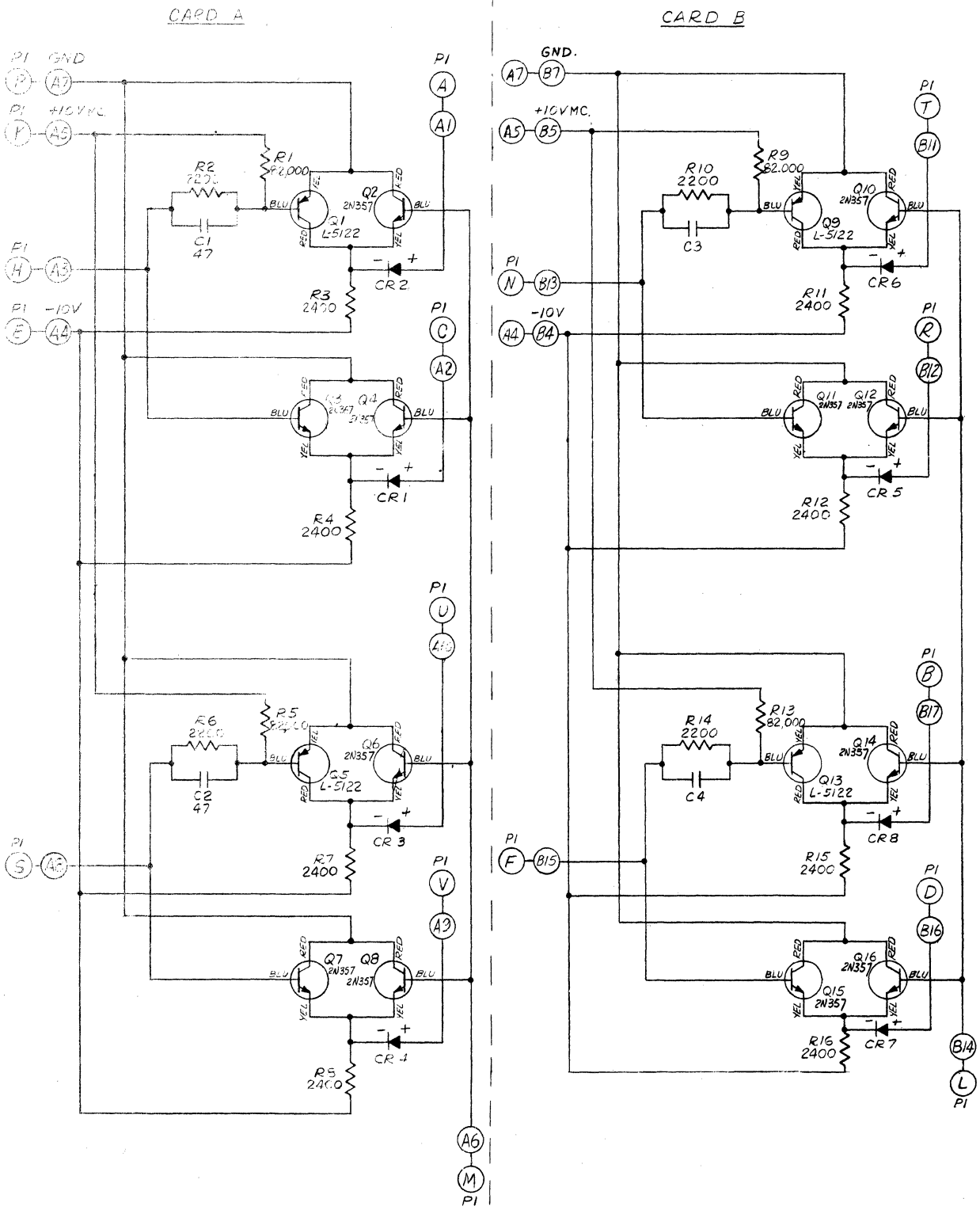


FIG. 96

INPUT MIXER

D-85545
"A" RED

INPUT MIXER

Handle Color: Yellow Green

Drawing Number: D-85545

PW Number: 63-953

Transistors:* 4 L-5122; 12 2N357

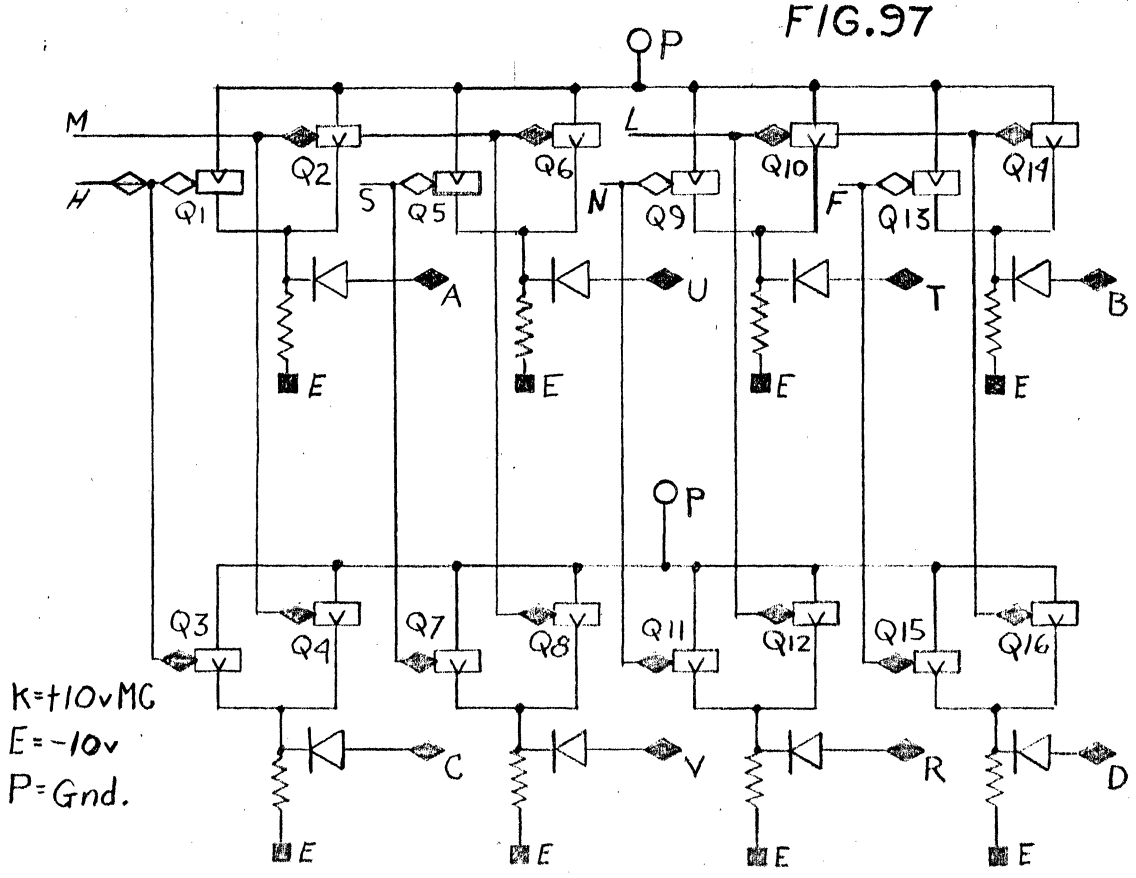
Power Supply Voltages: +10 MC; -10

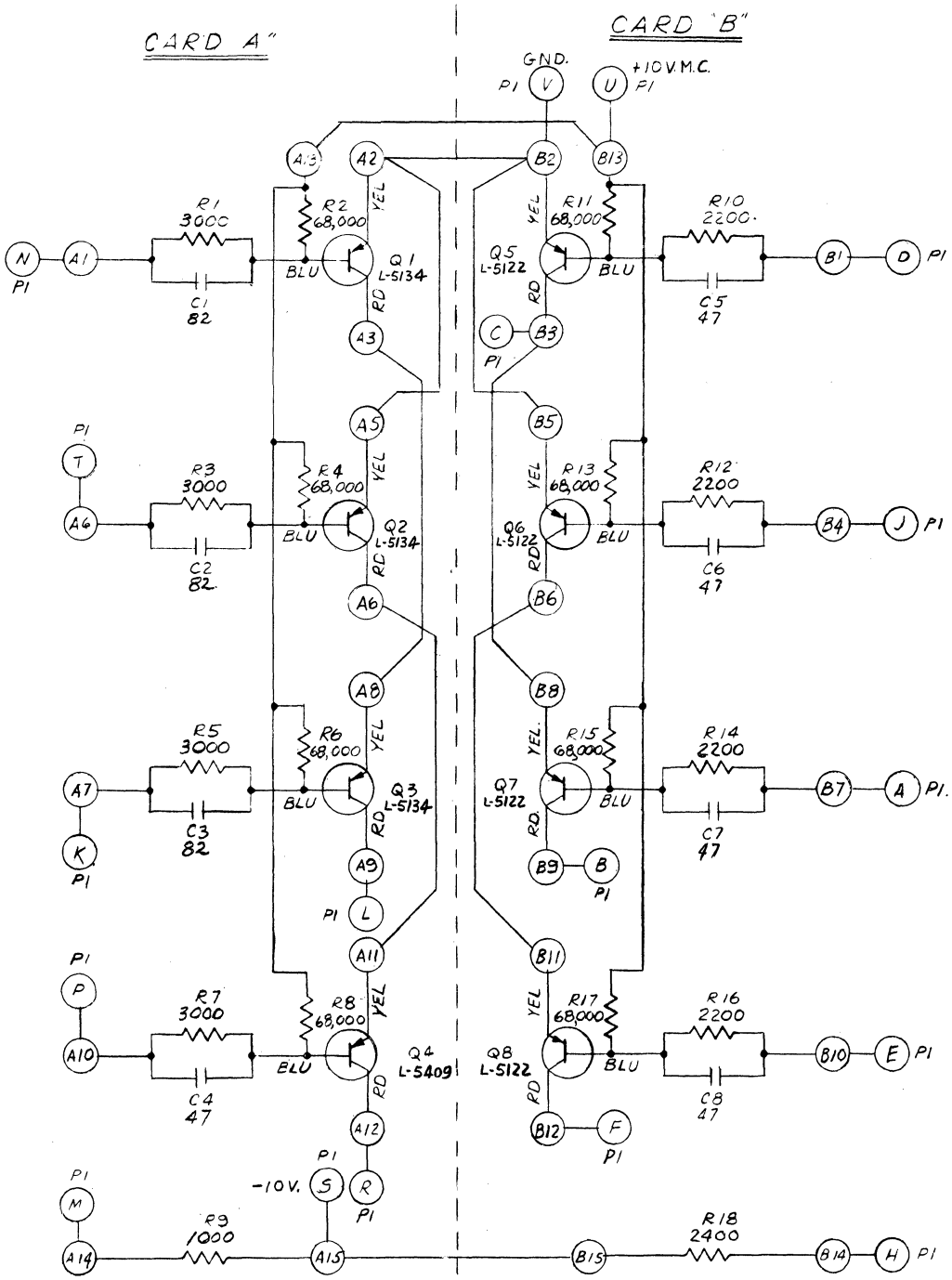
Use: Mix input levels for input-output equipment in in-out frame

Remarks: 4 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

FIG. 97





D-85386
"A"-RED

FIG. 98

SERIES (8R-A) INVERTER

INVERTER S-8RA

Handle Color: Yellow Blue

Drawing Number: D-85386

PW Number: 63-582

Transistors:* 4 L-5122; 3 L-5134; 1 2N501

Power Supply Voltages: +10 MC; -10V

Use: Inverters used in X-Adder carry circuit to provide fast carry time

Remarks: This is similar to unit 32, the inverter S-8R, with different transistors and load resistors.

*All transistor type numbers are identified with manufacturer in appendix

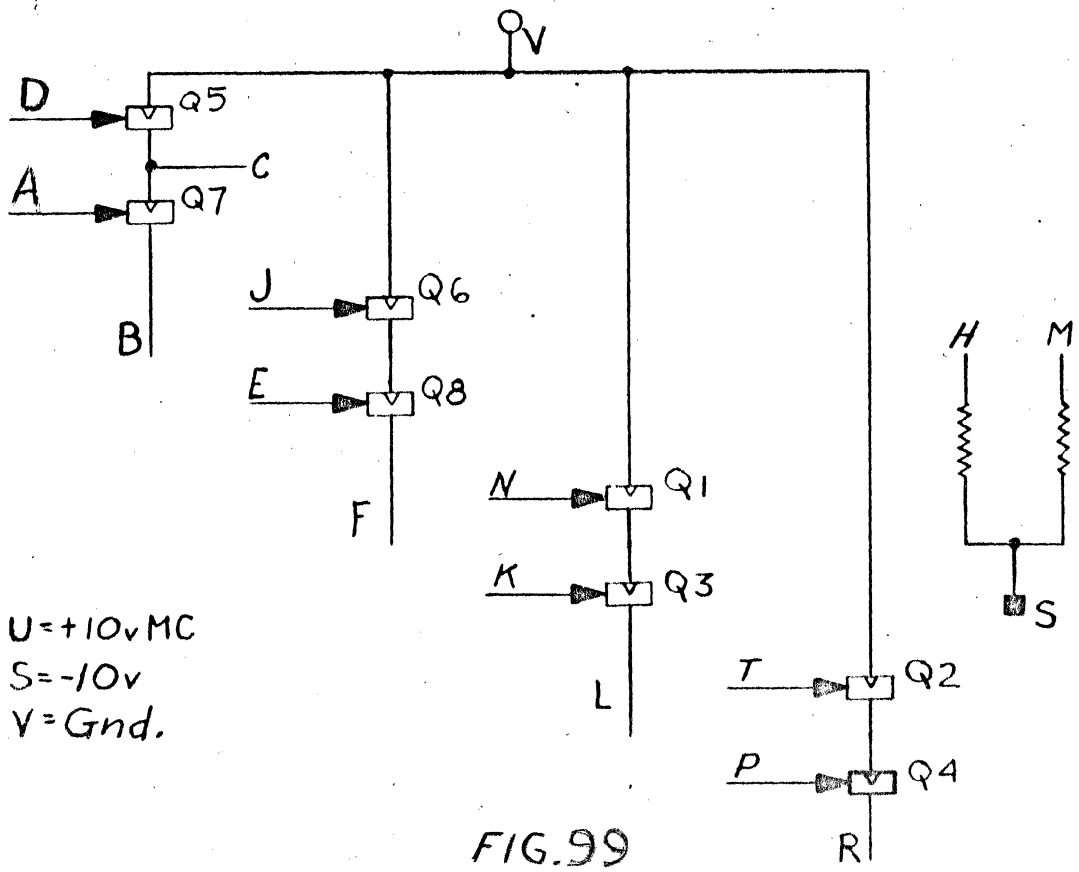


FIG. 99

SCHEMATIC

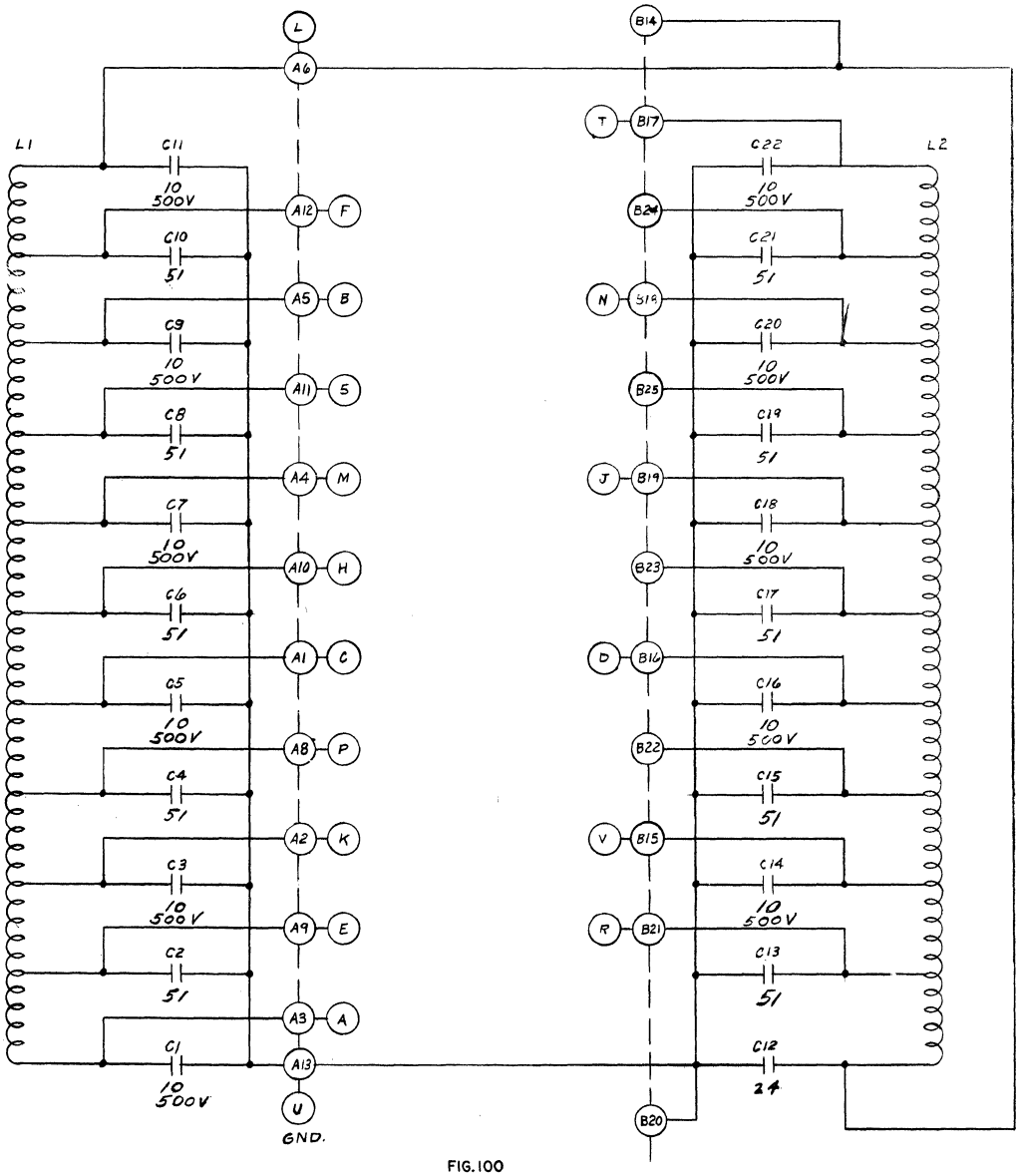


FIG. 100

INHIBIT LEVEL DELAY LINE

D-84806
4-1-60

NO. 48

INHIBIT LEVEL DELAY LINE

Handle Color: Yellow Grey

Drawing Number: D-84995

PW Number: 63-964

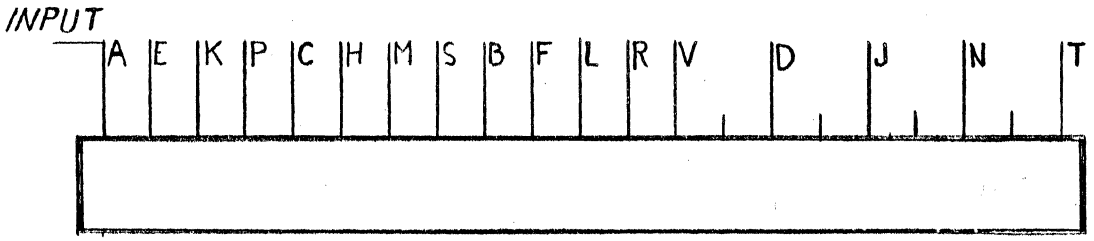
Transistors:*

Power Supply Voltages:

Use: Controls timing of Inhibit levels in S memory. Taps at 7.5 mμsec intervals

Remarks: Nominal total delay: .15 μsec
Terminate end with 220 ohm resistor

*All transistor type numbers are identified with manufacturer in appendix



U=Gnd

FIG. 101

SCHEMATIC

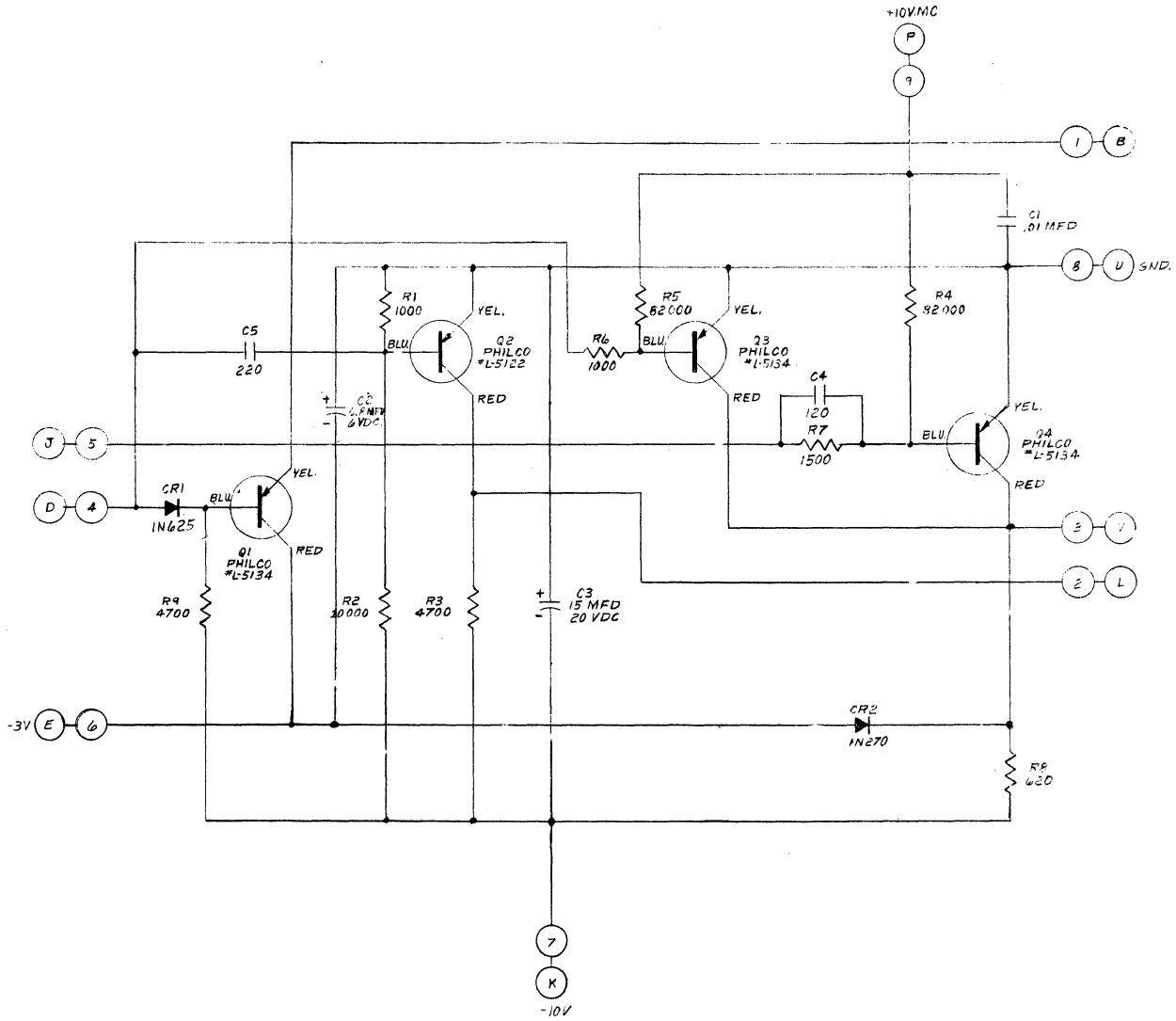


FIG. 102

VARIABLE DELAY COUPLING UNIT

D-80513
"A"-RED

NO. 49

VARIABLE DELAY COUPLING UNIT

Handle Color: Yellow White

Drawing Number: D-80513

PW Number: 63-976

Transistors:* 1 L-5122; 3 L-5134

Power Supply Voltages: +10 MC; -3; -10

Use: Used to couple one variable delay unit (No. 23) to another so as to provide a delay which will last for a given time after the last of a series of pulses.

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

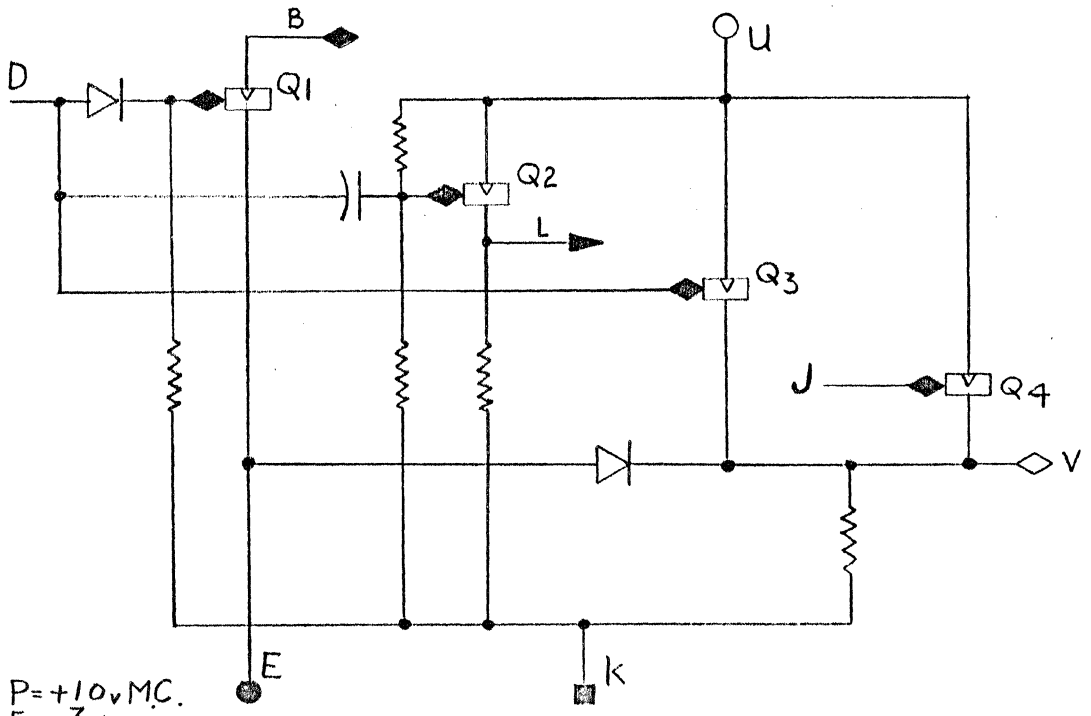


FIG. 103

SCHEMATIC

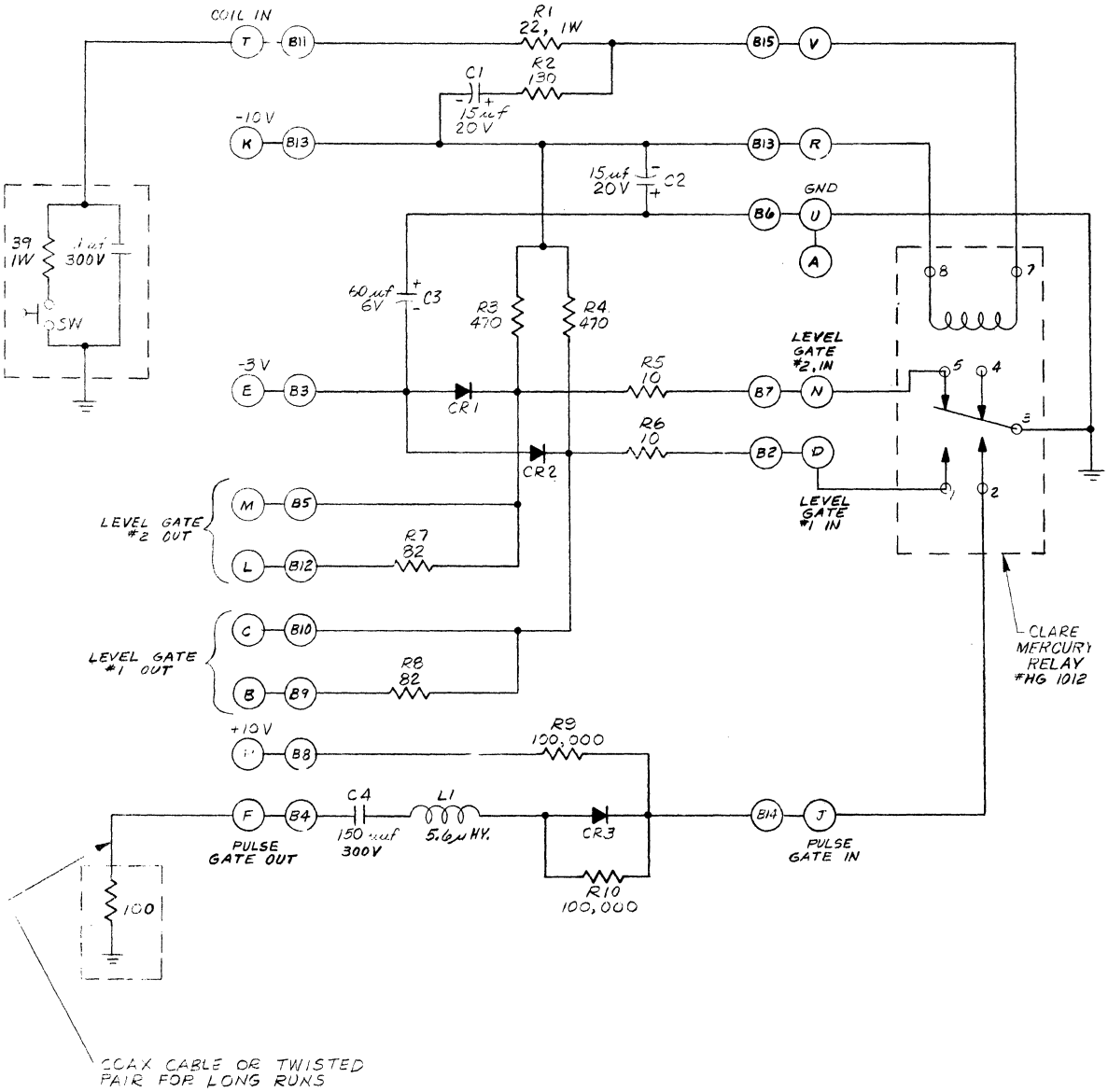


FIG. 104

MERCURY RELAY SIGNAL GENERATOR

D-85700
"A" REV.

MERCURY RELAY SIGNAL GENERATOR

Handle Color: Green Black

Drawing Number: D-80700

PW Number: 60-982

Transistors:*

Power Supply Voltages: +10; -3; -10

Use: Provides 3 volt negative pulse, or ground level, or 3 volt negative level upon application of push button.

Remarks: Requires externally mounted Clare HG1012 Mercury Relay, and push button.

*All transistor type numbers are identified with manufacturer in appendix

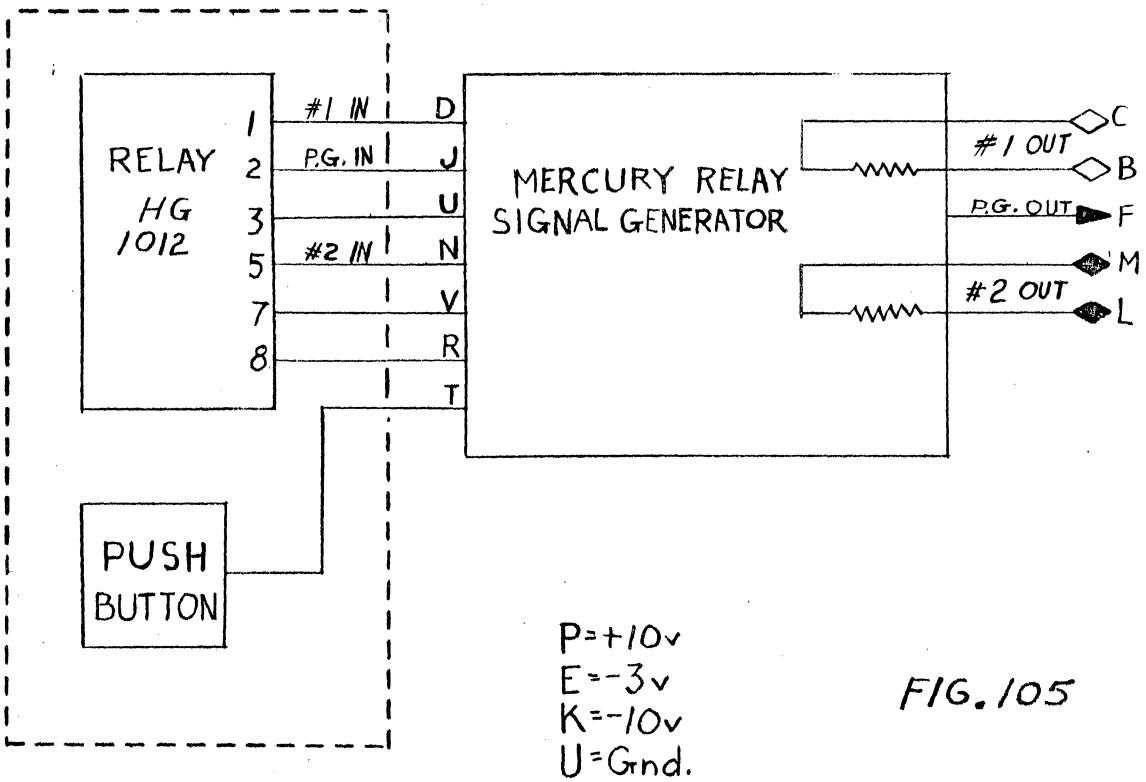


FIG. 105

SCHEMATIC

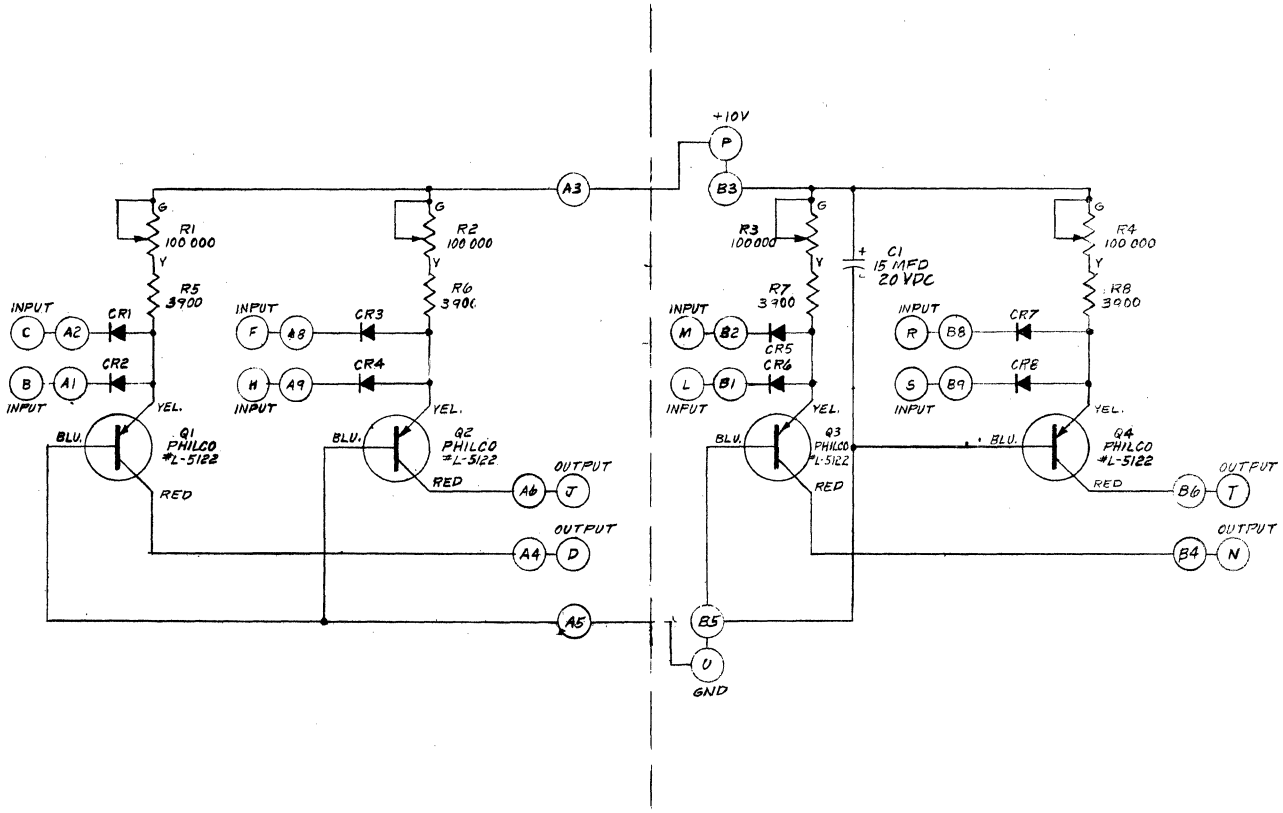


FIG. 106

VARIABLE DELAY AUXILIARY UNIT

D-85673
"A"-RED

NO. 51

VARIABLE DELAY AUXILIARY UNIT

Handle Color: Green Brown

Drawing Number: D-85673

PW Number: 63-974

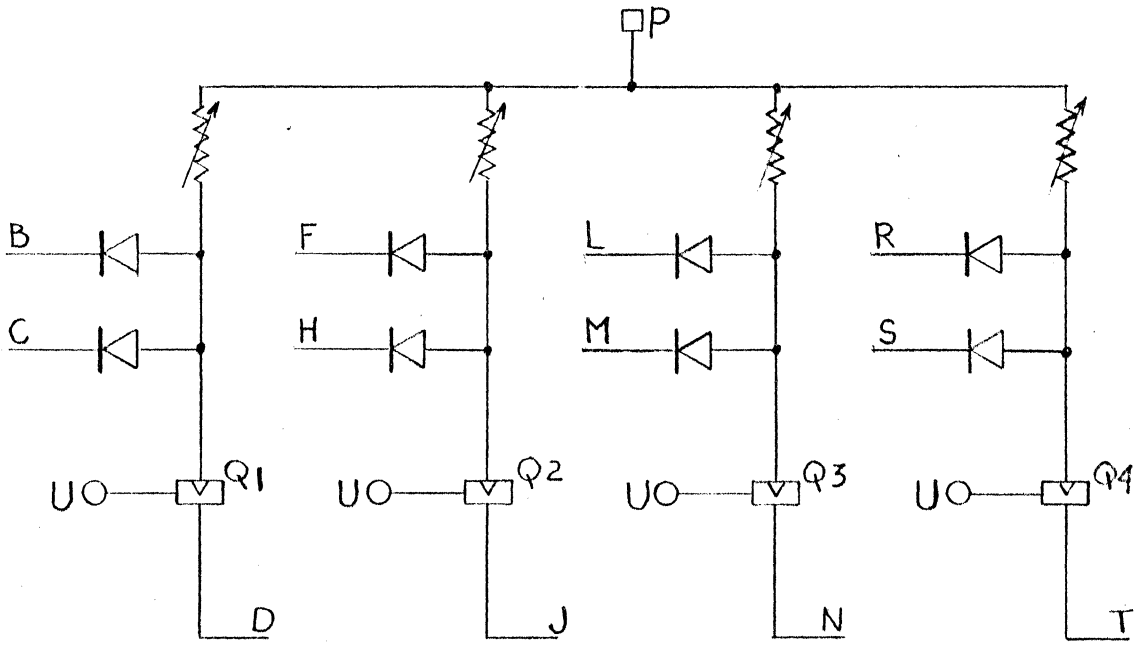
Transistors:* 4 L-5122

Power Supply Voltages: +10

Use: Provides a switch under computer control to switch among any of four values of delay

Remarks: Used with variable delay unit (No. 23)

*All transistor type numbers are identified with manufacturer in appendix



P = +10v
U = Gnd.

FIG. 107

SCHEMATIC

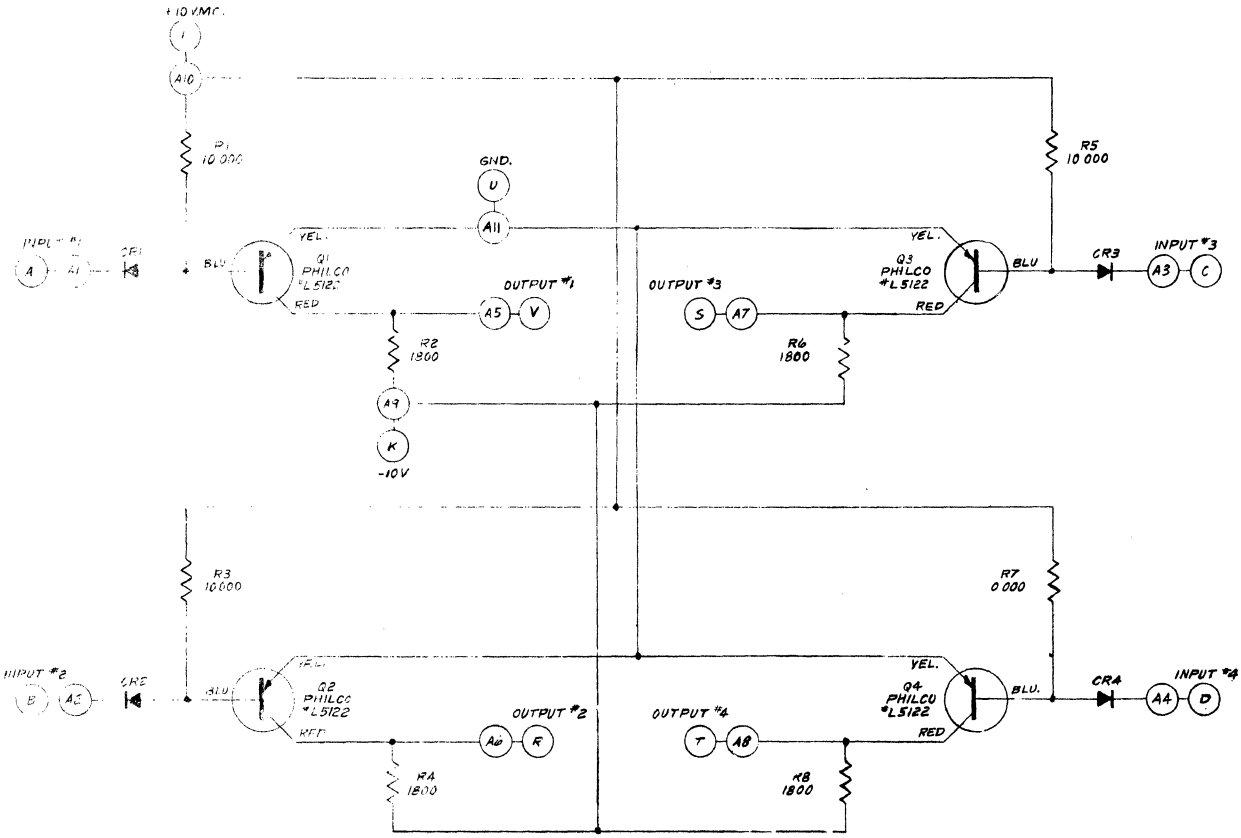


FIG. 108

INPUT MIXER AMPLIFIER

D-85744
"A"-2ED.

INPUT MIXER AMPLIFIER

Handle Color: Green Red

Drawing Number: D-85744

PW Number: 63-988

Transistors:* 4 L-5122

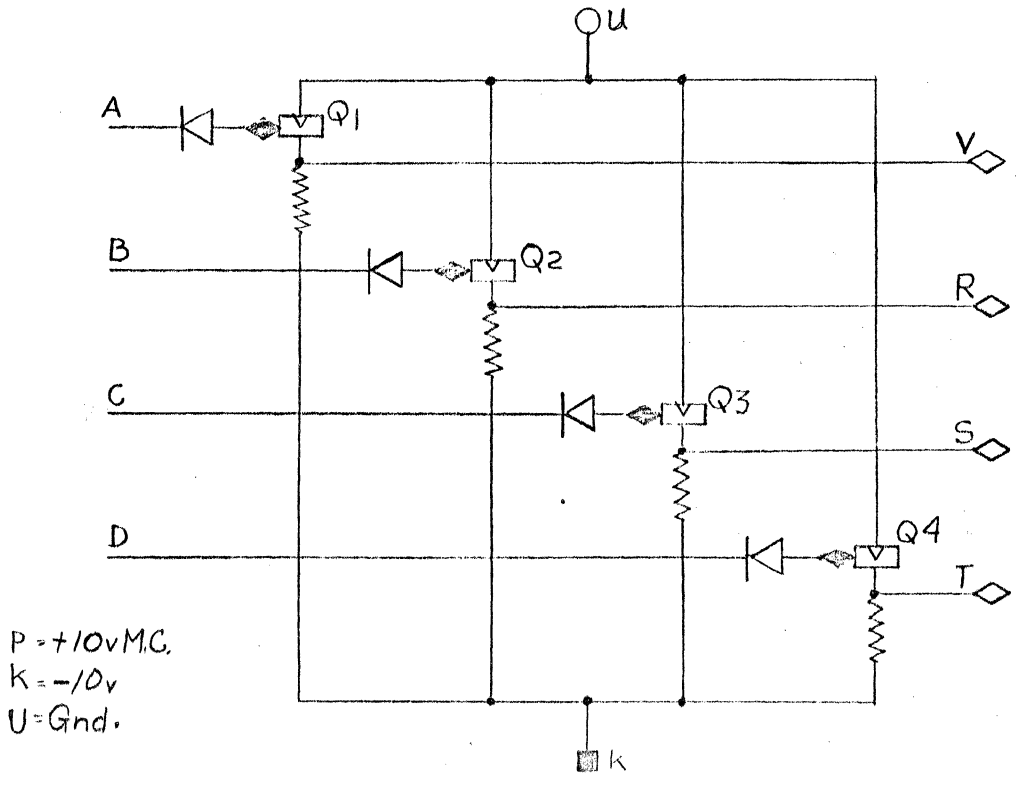
Power Supply Voltages: +10 MC; -10

Use: Inverting amplifier for levels coming from input mixer (No. 45)

Remarks: 4 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

FIG. 109



D-87685
A- REDUCTION.

SCHEMATIC

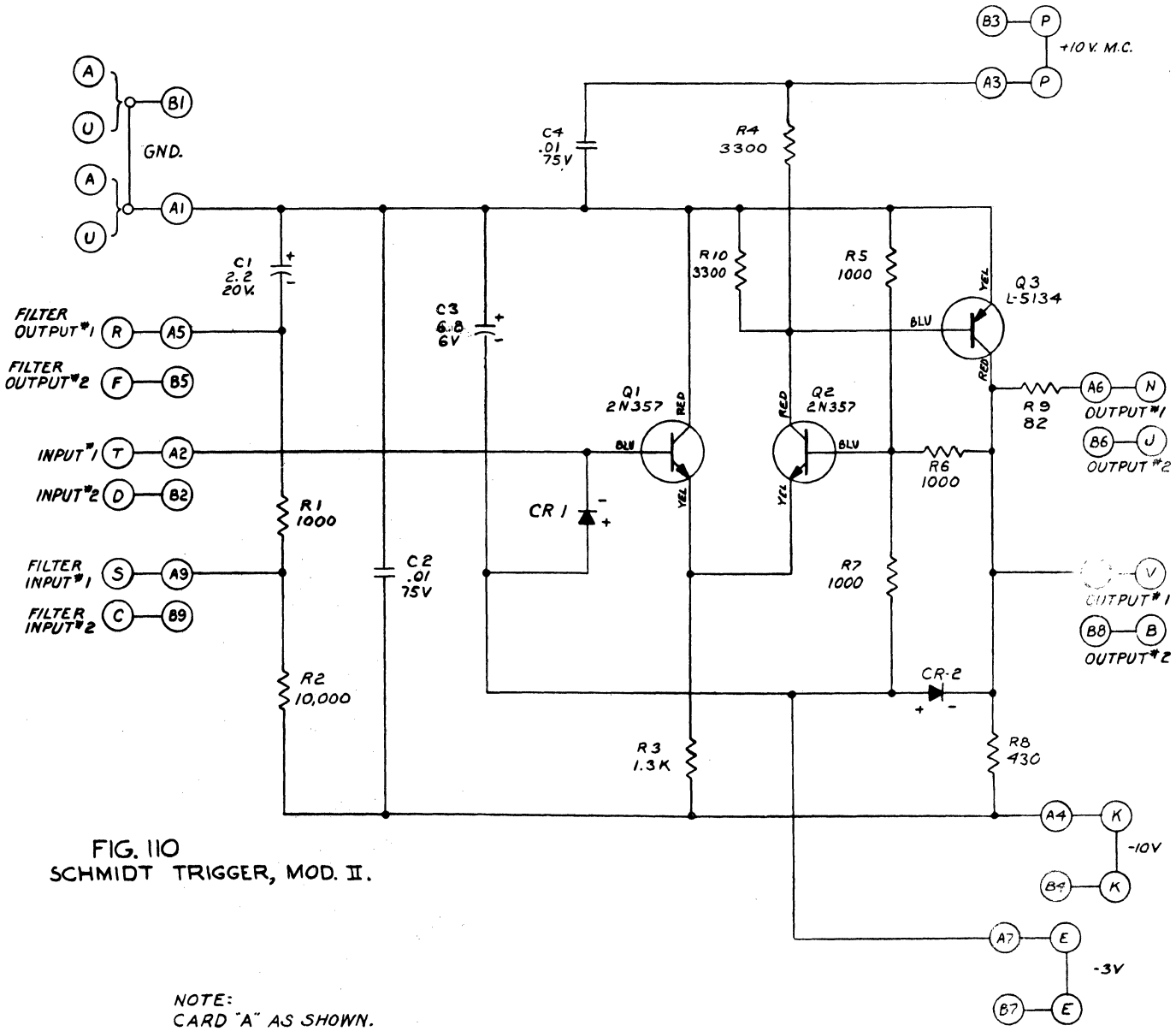


FIG. 110
SCHMIDT TRIGGER, MOD. II.

NOTE:
CARD "A" AS SHOWN.
CARD "B" SAME AS CARD "A"

NO. 53

SCHMIDT TRIGGER MOD II

Handle Color: Green Orange

Drawing Number: D-87685

PW Number: 63-1105

Transistors:* 2 L-5134; 4 2N357

Power Supply Voltages: 10; -3; -10

Use: Inverting circuit providing fast transition times between ground and -3 volts independent of input transition times

Remarks: Trigger points: -0.9 volts, -2.2 volts
2 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

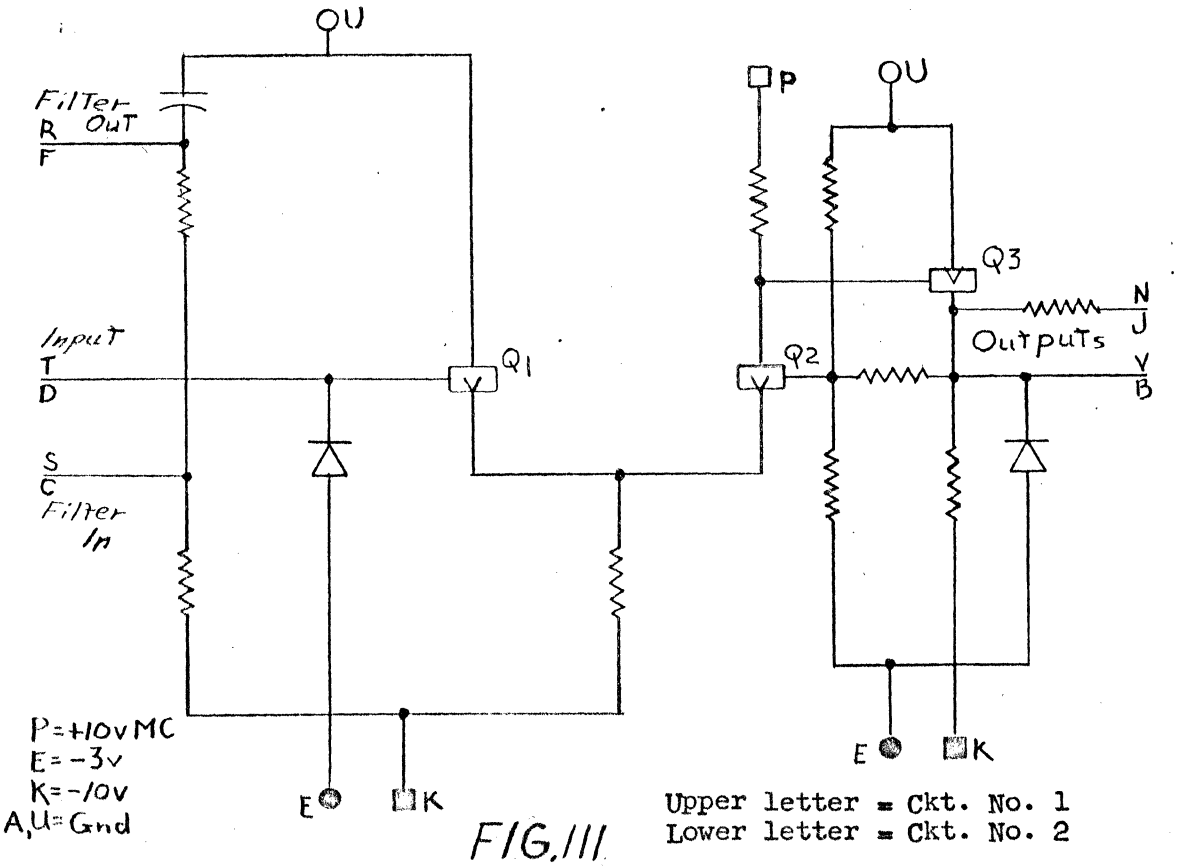


FIG. III

D-80515
A-REDUCTION.

SCHEMATIC

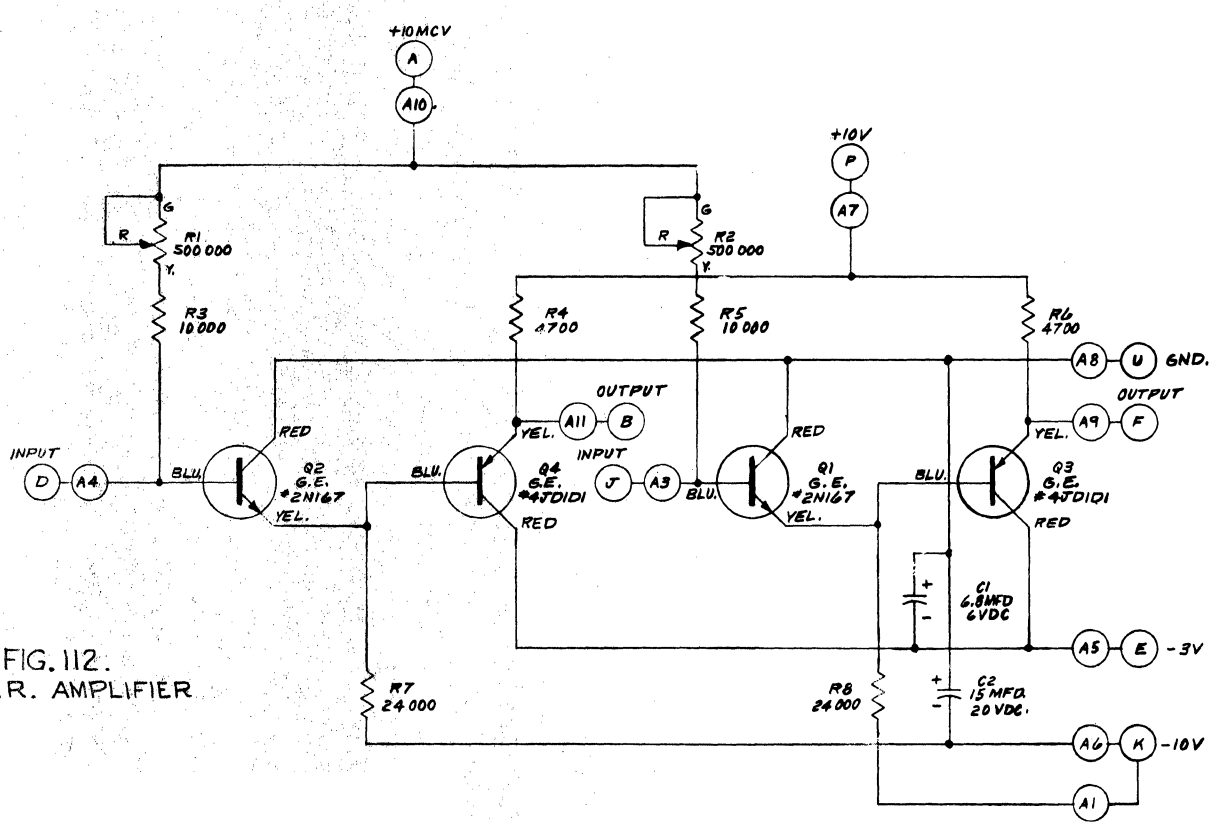


FIG. 112.
P.E.T.R. AMPLIFIER

NO. 54

PETR AMPLIFIER

Handle Color: Green Yellow

Drawing Number: D-80515

PW Number: 63-987

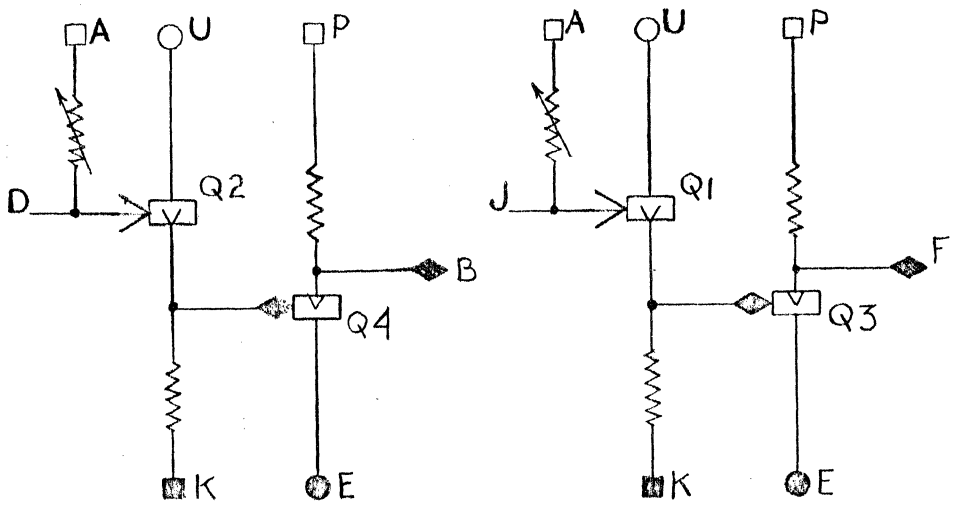
Transistors:* 2 4JD1D1; 2 2N167

Power Supply Voltages: +10 MC; +10; -3; -10

Use: Emitter follower type amplifier for current supplied by photo diode. Used in Photo-electric Tape Reader circuit.

Remarks: 2 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix



A = +10v MC.
P = +10v
E = -3v
K = -10v
U = Gnd.

FIG. 113

SCHEMATIC

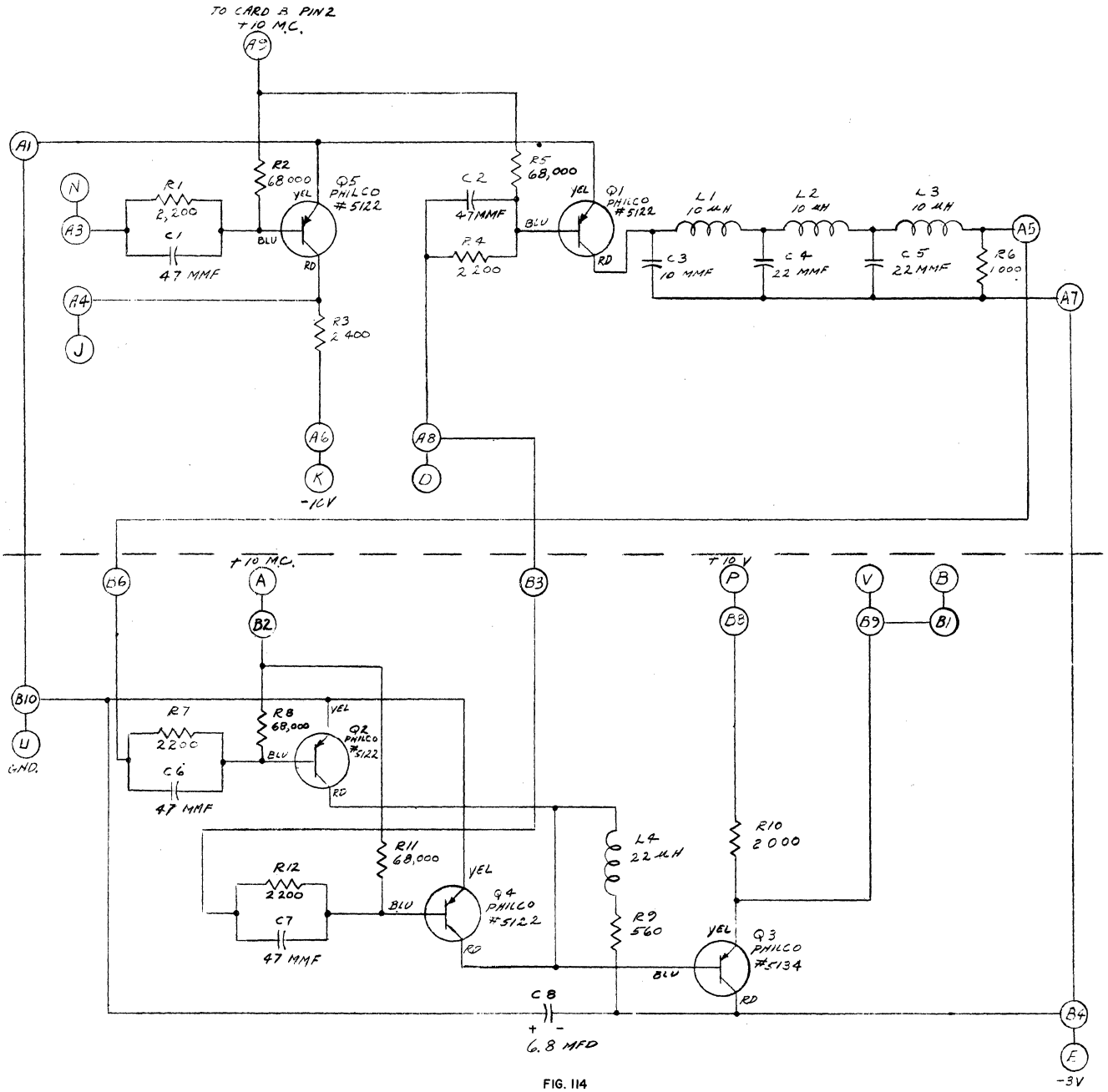


FIG. 114

0.1 μ SEC. PULSE FORMER

D-80514
"A" RED

.1 μSEC PULSE FORMER

Handle Color: Green Green

Drawing Number: D-80514

PW Number: 63-986

Transistors:* 4 L-5122; 1 L-5134

Power Supply Voltages: +10 MC; +10; -3; -10

Use: Form .1 μsec 3 volt negative pulse from rising or falling level

Remarks: Maximum output pulse current: 30 ma

*All transistor type numbers are identified with manufacturer in appendix

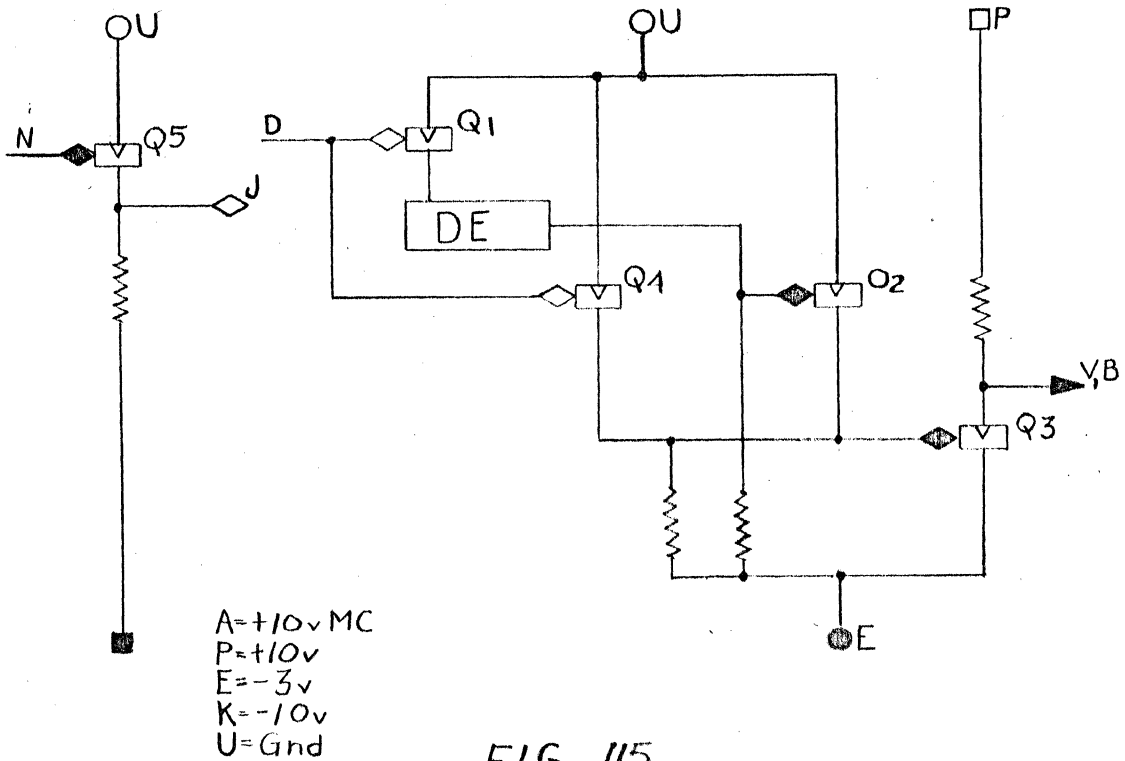


FIG. 115

SCHEMATIC

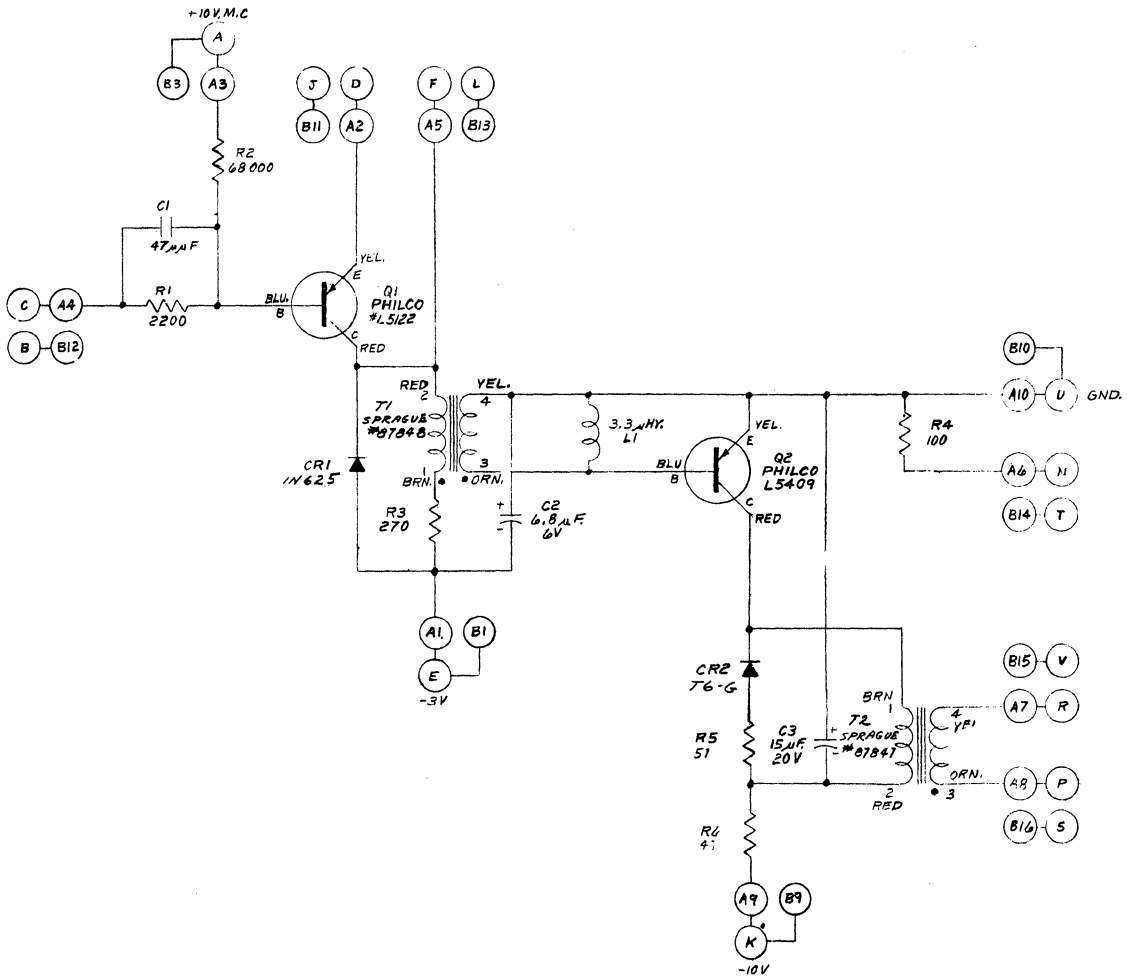


FIG. 116

GATED PULSE AMPLIFIER

D-85748
"A": RED.

NO. 56

GATED PULSE AMPLIFIER

Handle Color: Green Blue

Drawing Number: D-85748

PW Number: 63-961

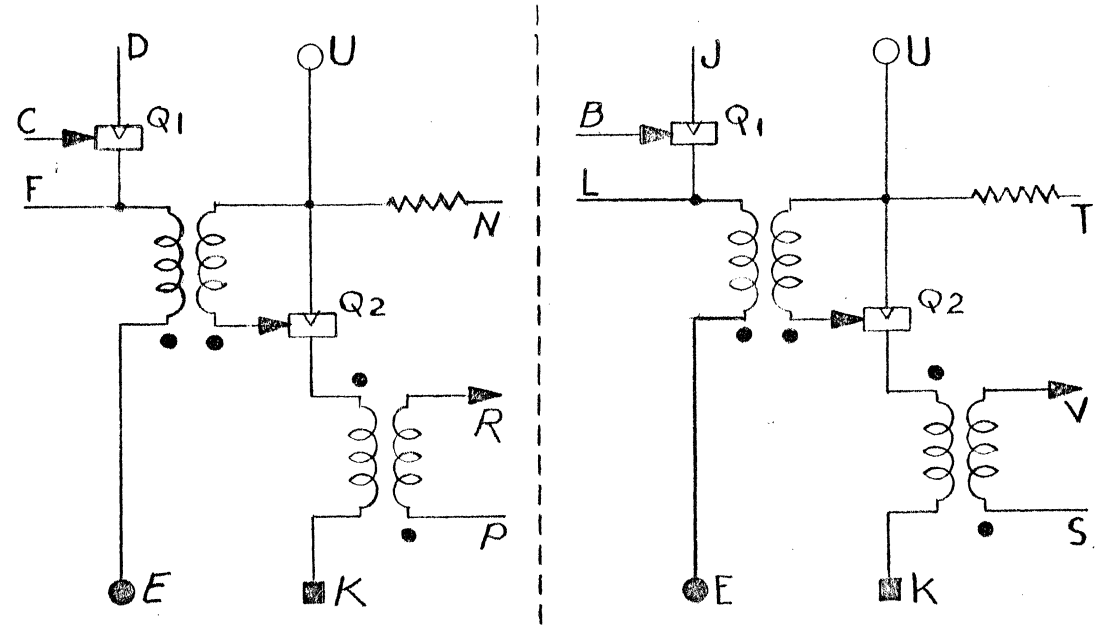
Transistors:* 2 L-5122; 2 2N501

Power Supply Voltages: +10 MC; -3; -10

Use: Pulse amplifier for .1 μsec 3 volt negative pulses. Used in in-out equipment, and for amplification after pulse has gone through a delay line.

Remarks: 2 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix



A=+10v MC.
E=-3v
K=-10v
U=Gnd.

CARD A CARD B

FIG. 117

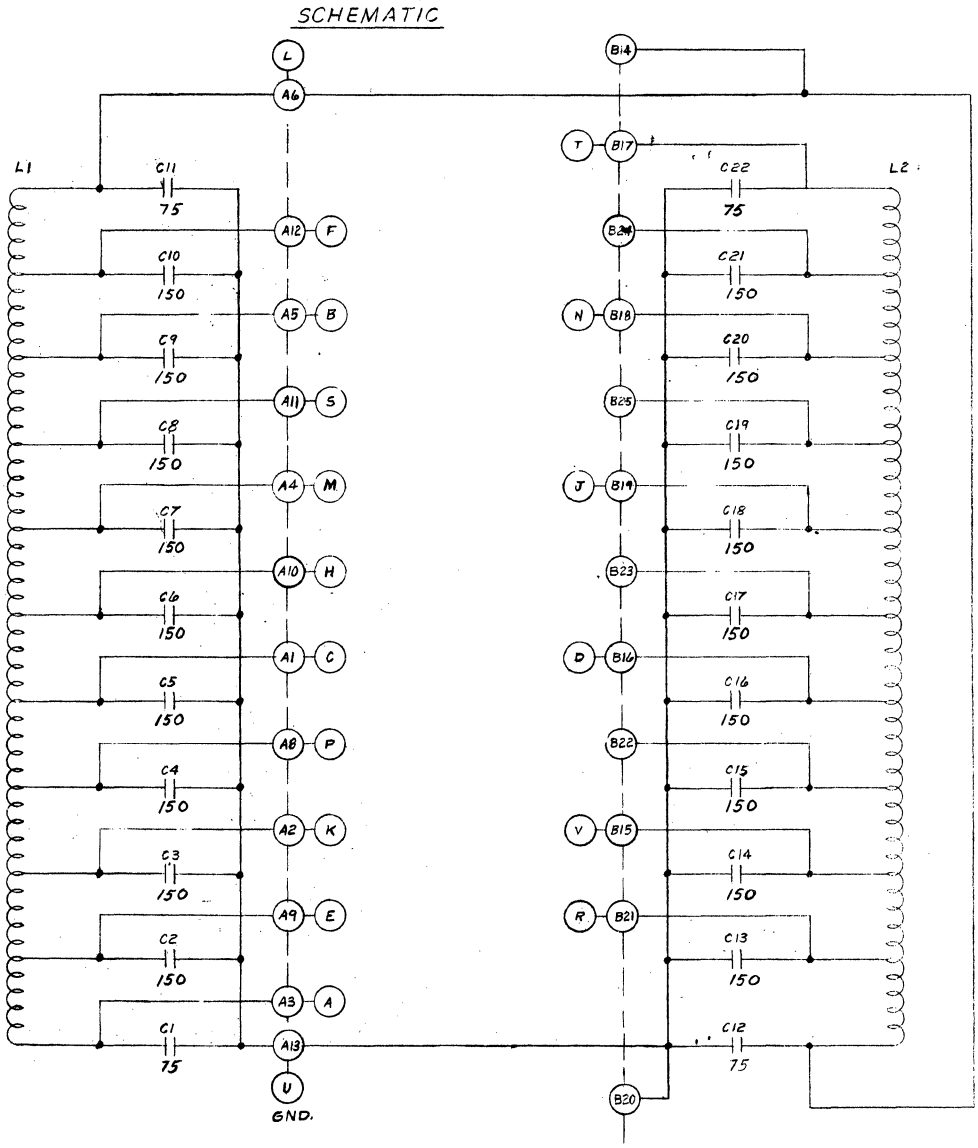


FIG. 118

0.15 μSEC, 50 OHM DELAY LINE

D-85568
4-12-61 REP.

NO. 57

.15 μSEC 50 OHM DELAY LINE

Handle Color: Green Violet

Drawing Number: D-85568

PW Number: 63-964

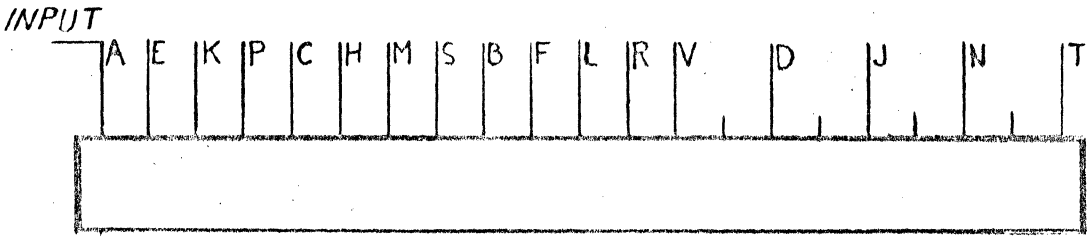
Transistors:*

Power Supply Voltages:

Use: Controls timing of Strobe pulses for S memory. Taps at 7.5 mμsec intervals.

Remarks: Terminate end with 51 ohm resistor.

*All transistor type numbers are identified with manufacturer in appendix



U-Cond

FIG. 119

SCHEMATIC

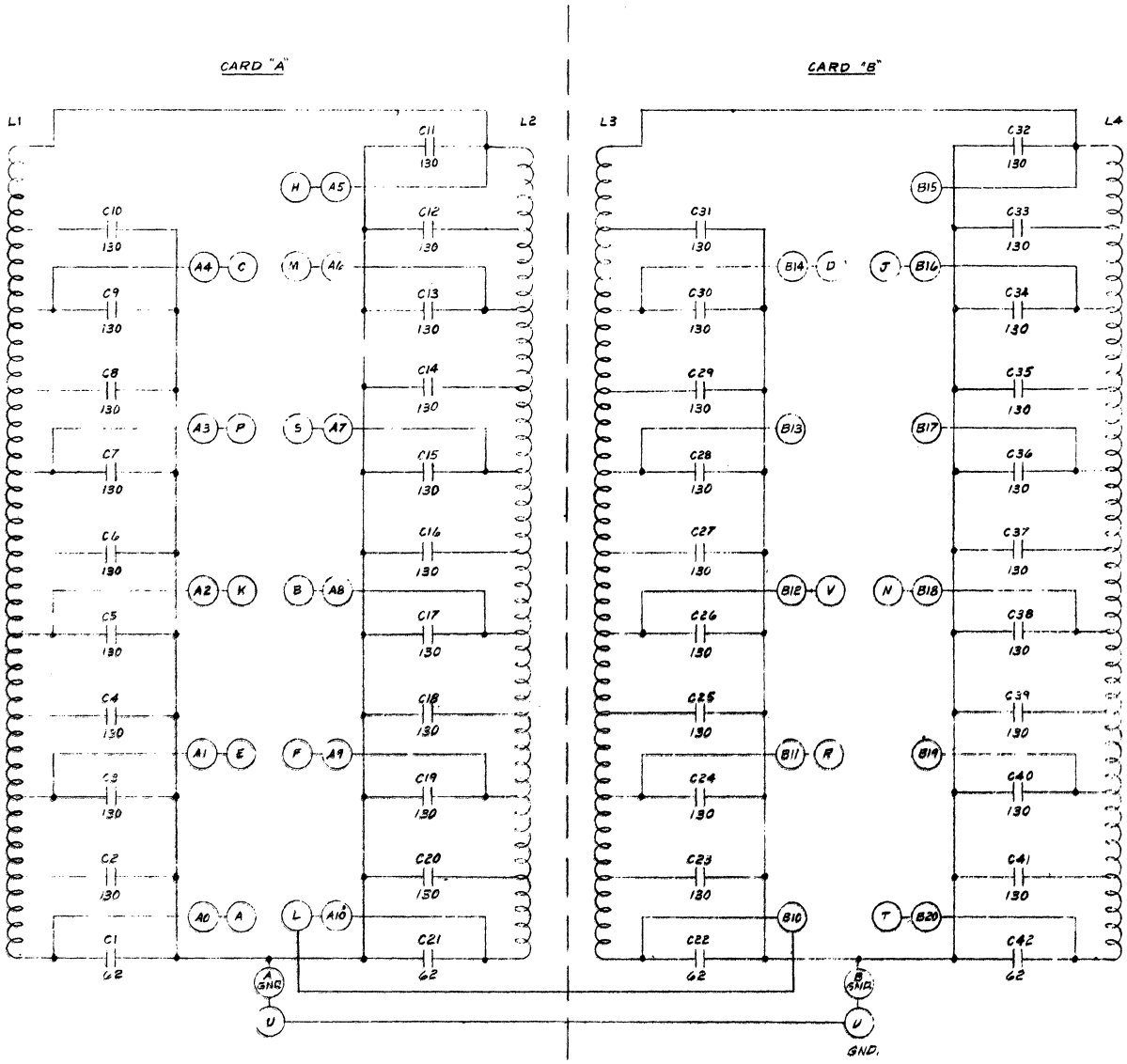


FIG. 120

0.4 μ SEC, 75 OHM DELAY LINE

NO. 58

.4 μSEC 75 OHM DELAY LINE

Handle Color: Green Grey

Drawing Number: D-85746

PW Number: 63-1002

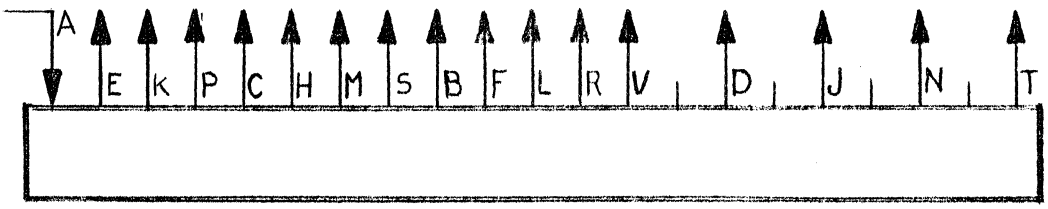
Transistors:*

Power Supply Voltages:

Use: Controls timing of pulses for memory control flip-flops. Taps at 20 mμsec intervals.

Remarks: Terminate end with 75 ohm resistor

*All transistor type numbers are identified with manufacturer in appendix



U=Gnd.

FIG. 121

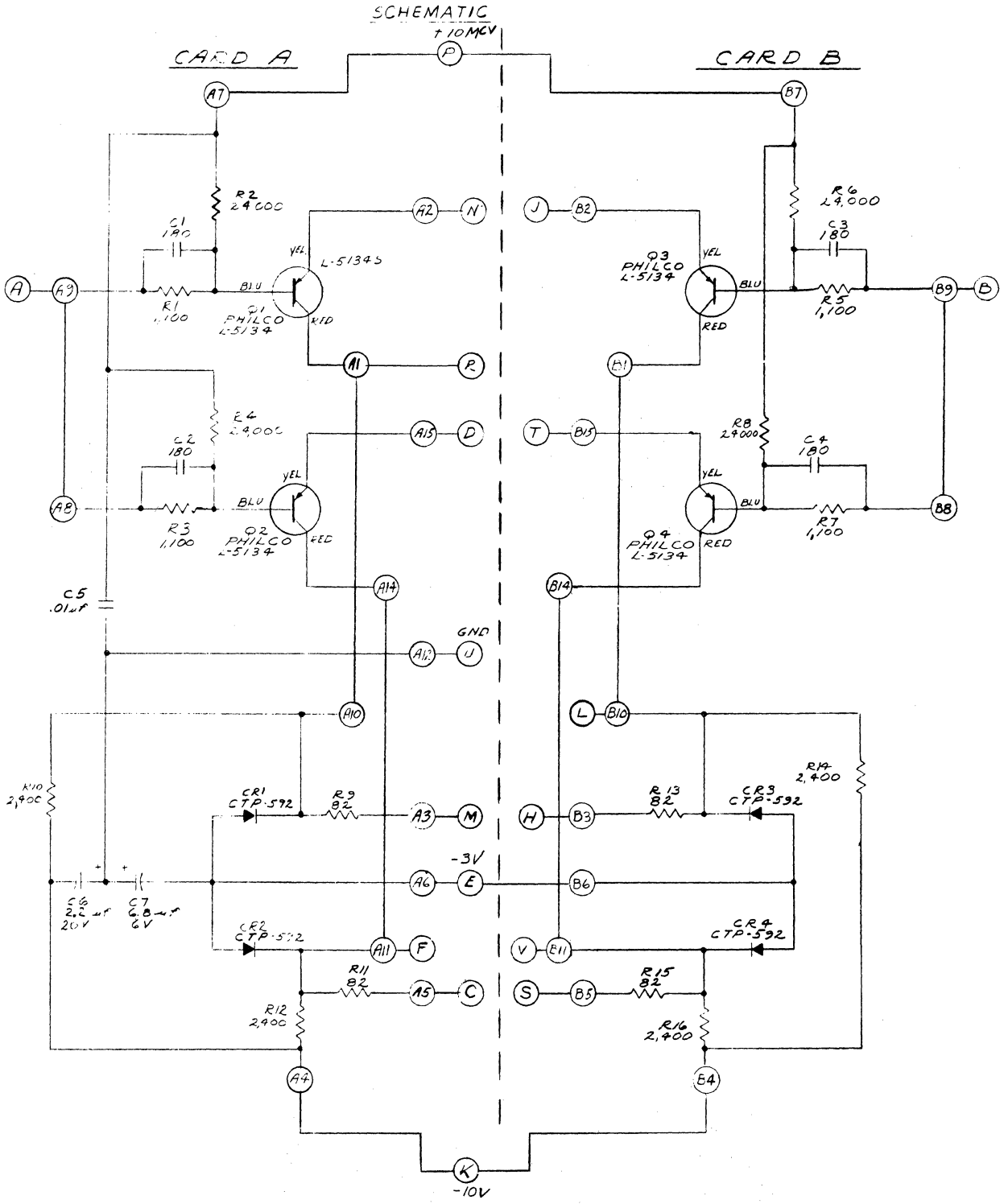


FIG. 122

OUTPUT DISTRIBUTOR

D-85745
"A" RED

NO. 59

OUTPUT DISTRIBUTOR

Handle Color: Green White

Drawing Number: D-85745

PW Number: 63-1000

Transistors:* 4 L-5134

Power Supply Voltages: +10 MC; -3; -10

Use: 4 clamped inverters with 4 load resistors and outputs for driving bases and for driving cables

Remarks: Used in in-out equipment

*All transistor type numbers are identified with manufacturer in appendix

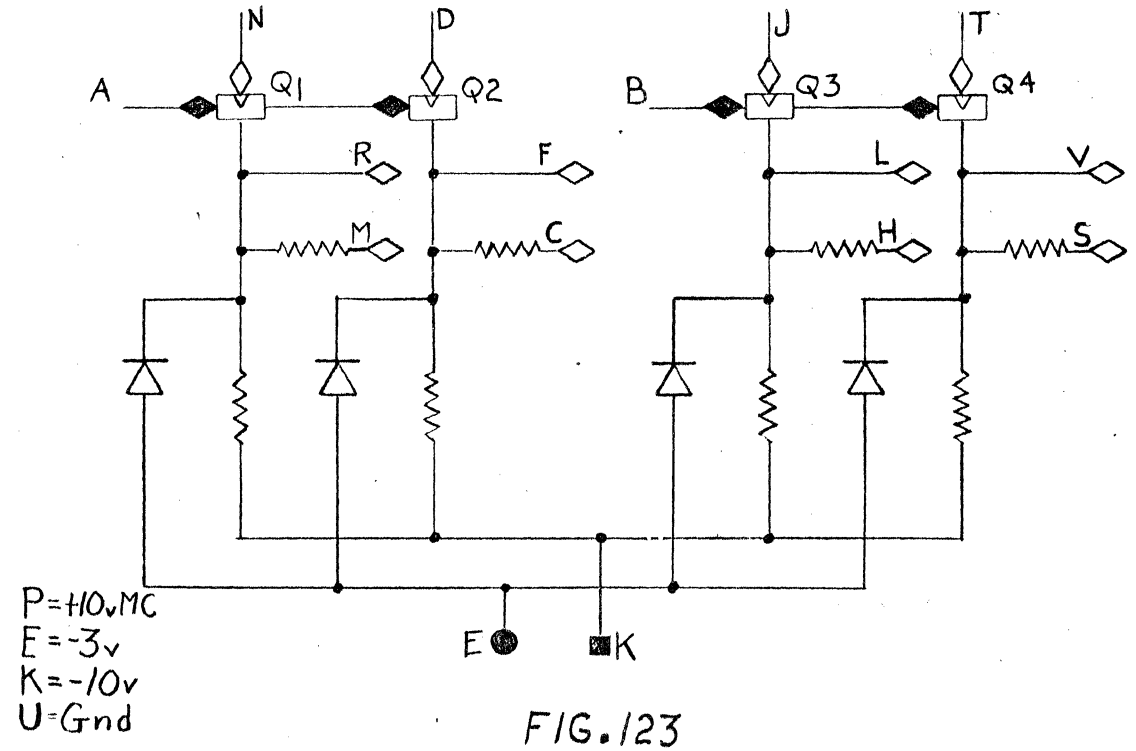


FIG. 123

D-87522
A- REDUCTION.

SCHEMATIC

CARD A

CARD B

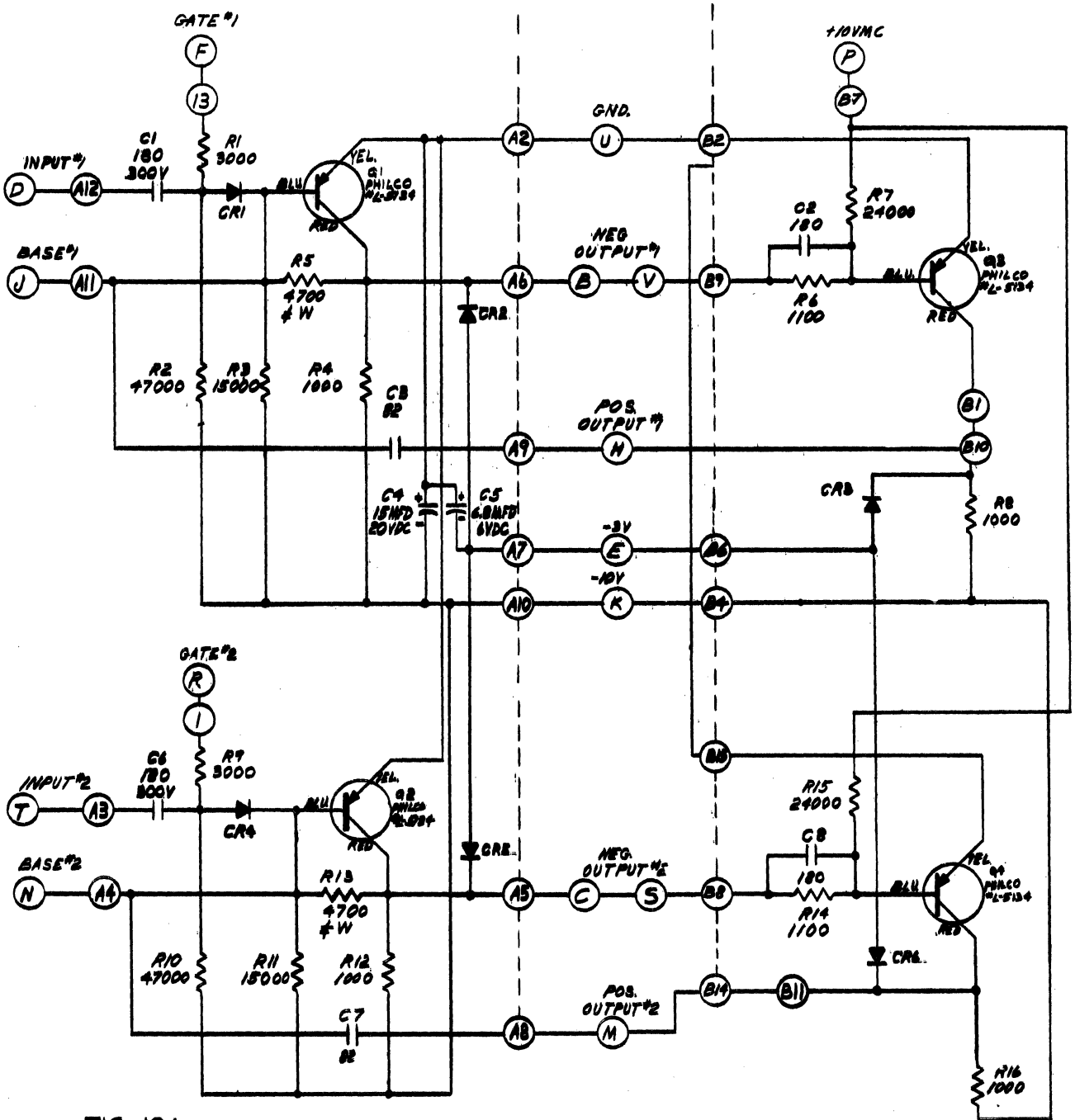


FIG. 124

.3 μ SEC. PULSE FORMER, MOD II.

.3 μSEC PULSE FORMER MOD II

Handle Color: Blue Black

Drawing Number: D-87522

PW Number: 63-1001; 63-1000

Transistors:* 4 L-5134

Power Supply Voltages: +10 MC; -3; -10

Use: a-c coupled clamped inverters for forming .3 μsec 3 volt positive or negative pulses from wave form rising from -3 volts to ground

Remarks: 2 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

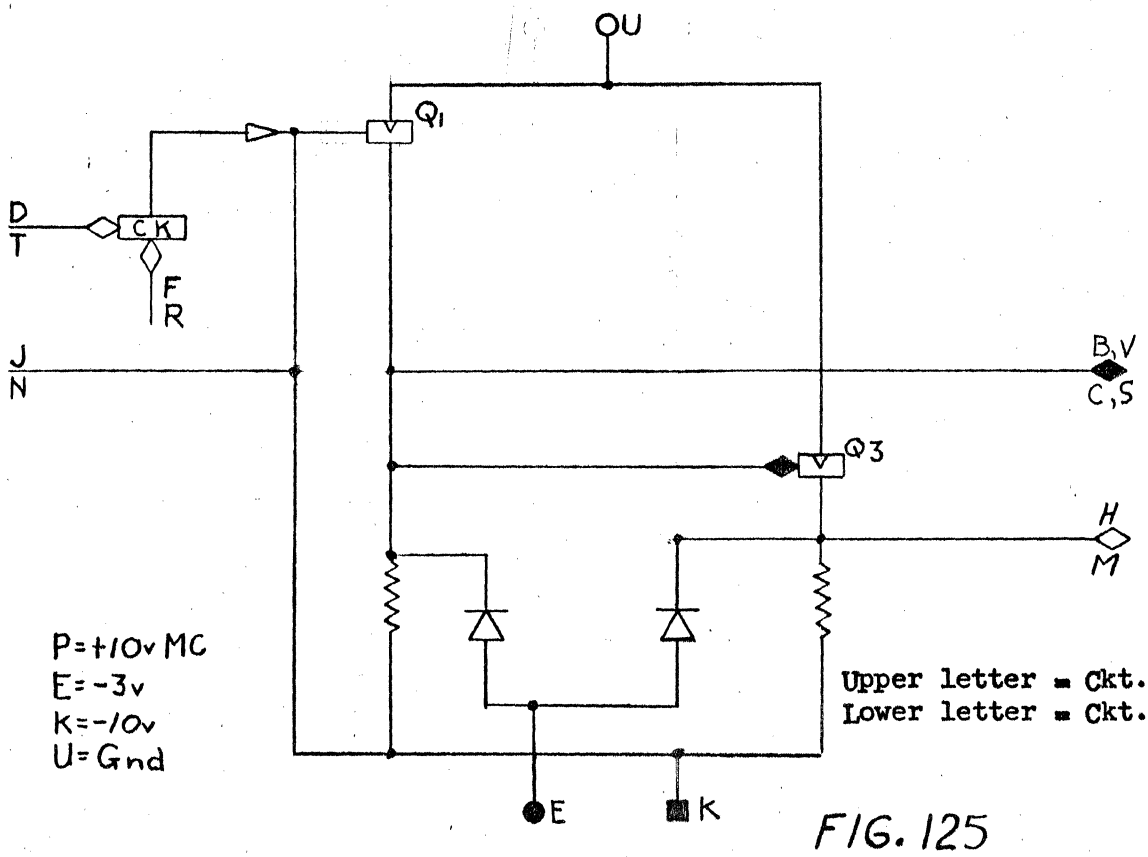


FIG. 125

SCHEMATIC

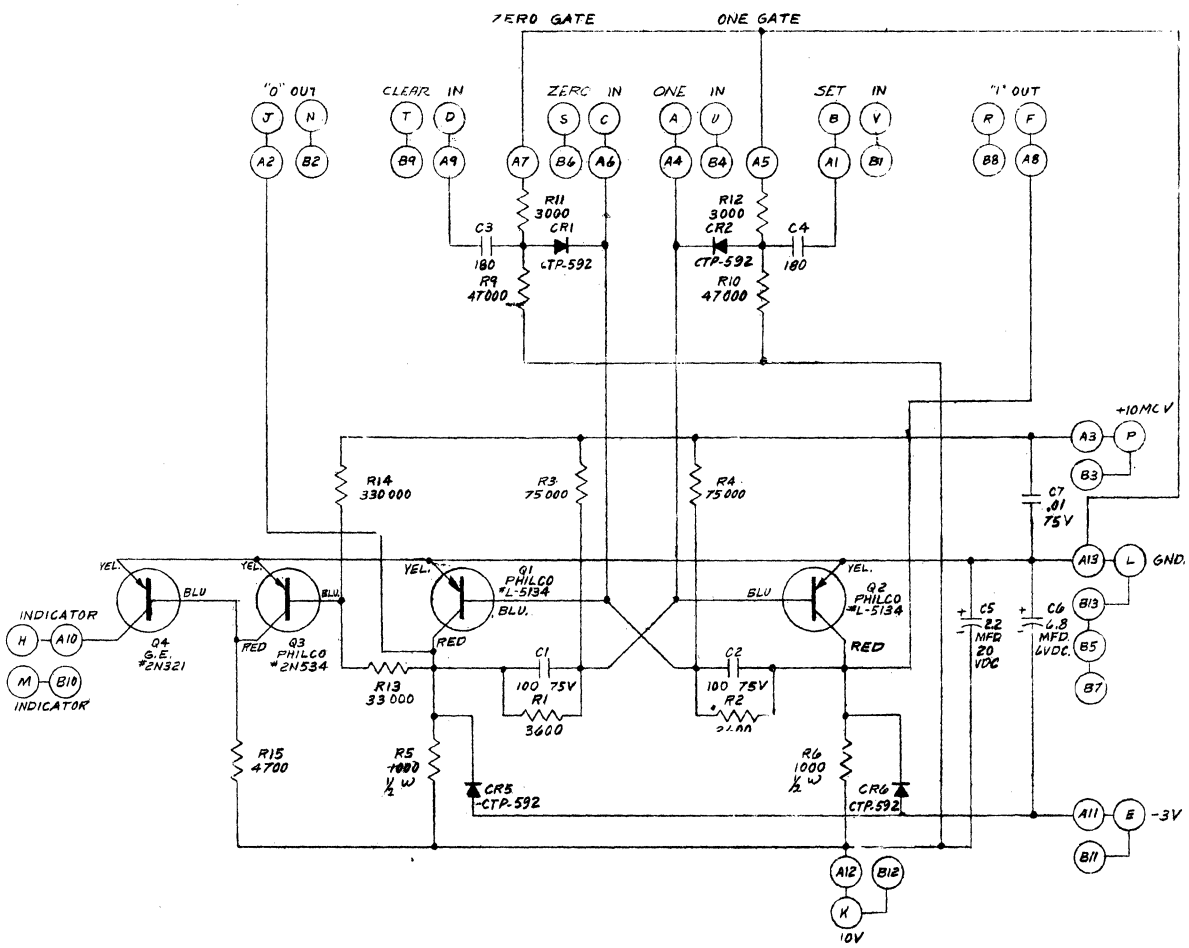


FIG. 126

DUAL FLIP-FLOP MOD II

D-85749
"A", RED

DUAL FLIP-FLOP MOD II

Handle Color: Blue Brown

Drawing Number: D-85749

PW Number: 63-999

Transistors:* 4 L-5134; 2 2N534; 2 2N321

Power Supply Voltages: +10 MC; -3; -10

Use: Bistable device to provide logic levels of ground or -3 volts. Used in in-out equipment

Remarks: May be set or cleared
Maximum prf: 800 kcps
Clamped output provides 6.5 ma output current

2 circuits per PIU

*All transistor type numbers are identified with manufacturer in appendix

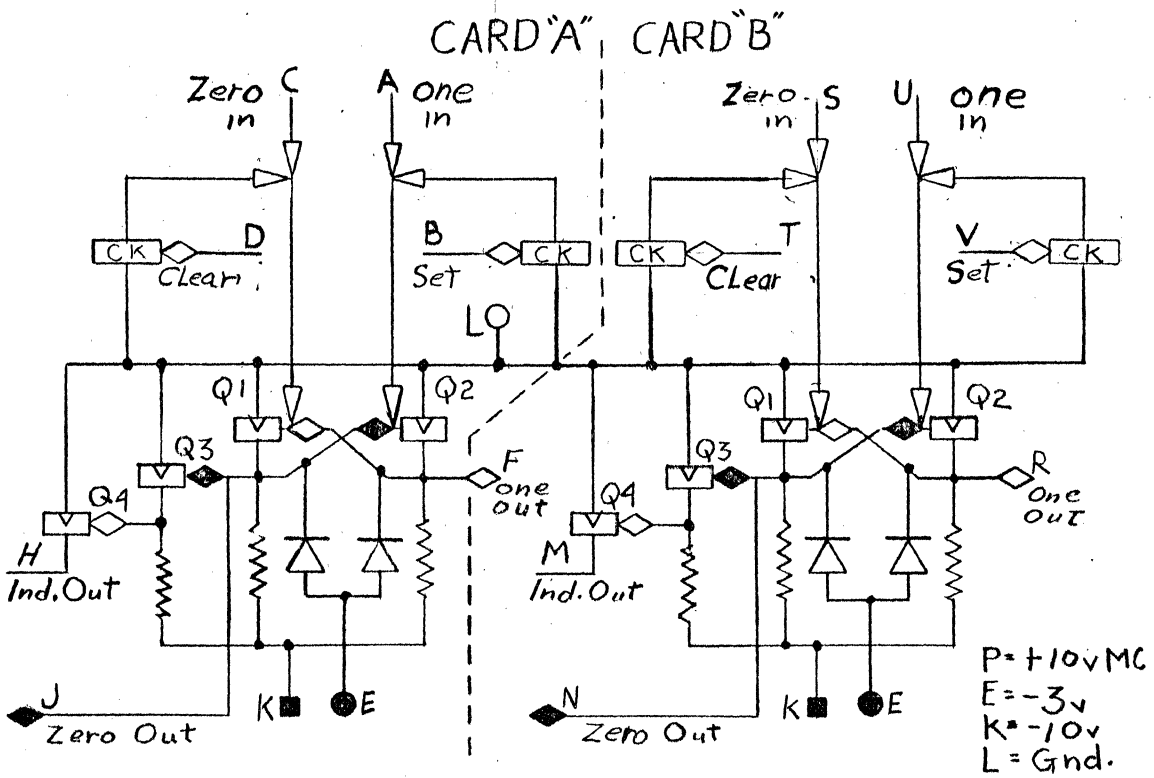


FIG. 127

DUAL FLIP-FLOP MOD II

Block Symbol

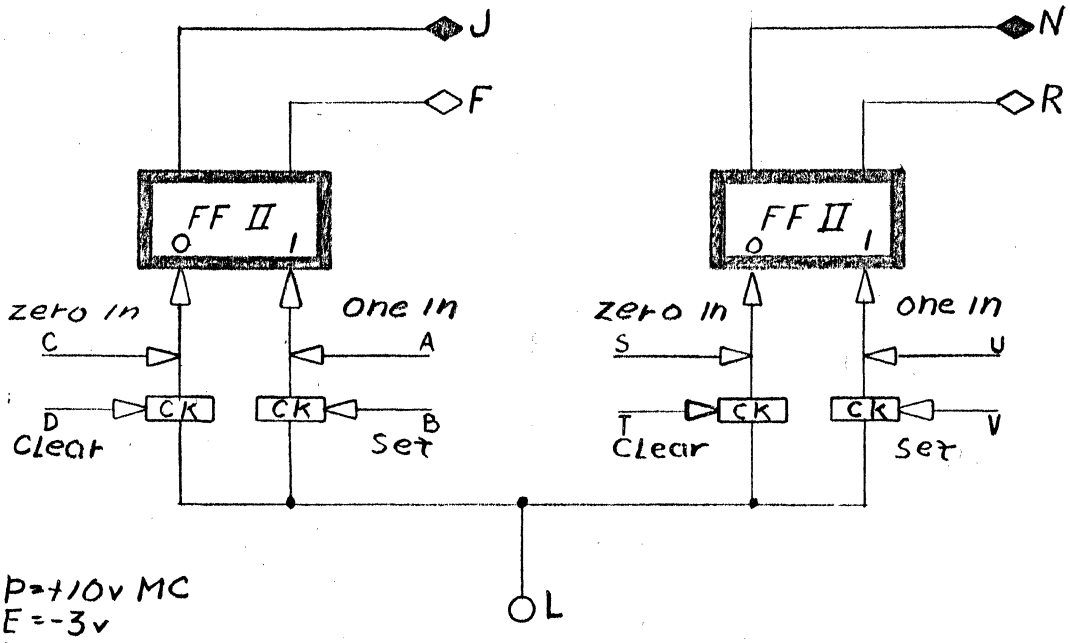


FIG.128

SCHEMATIC

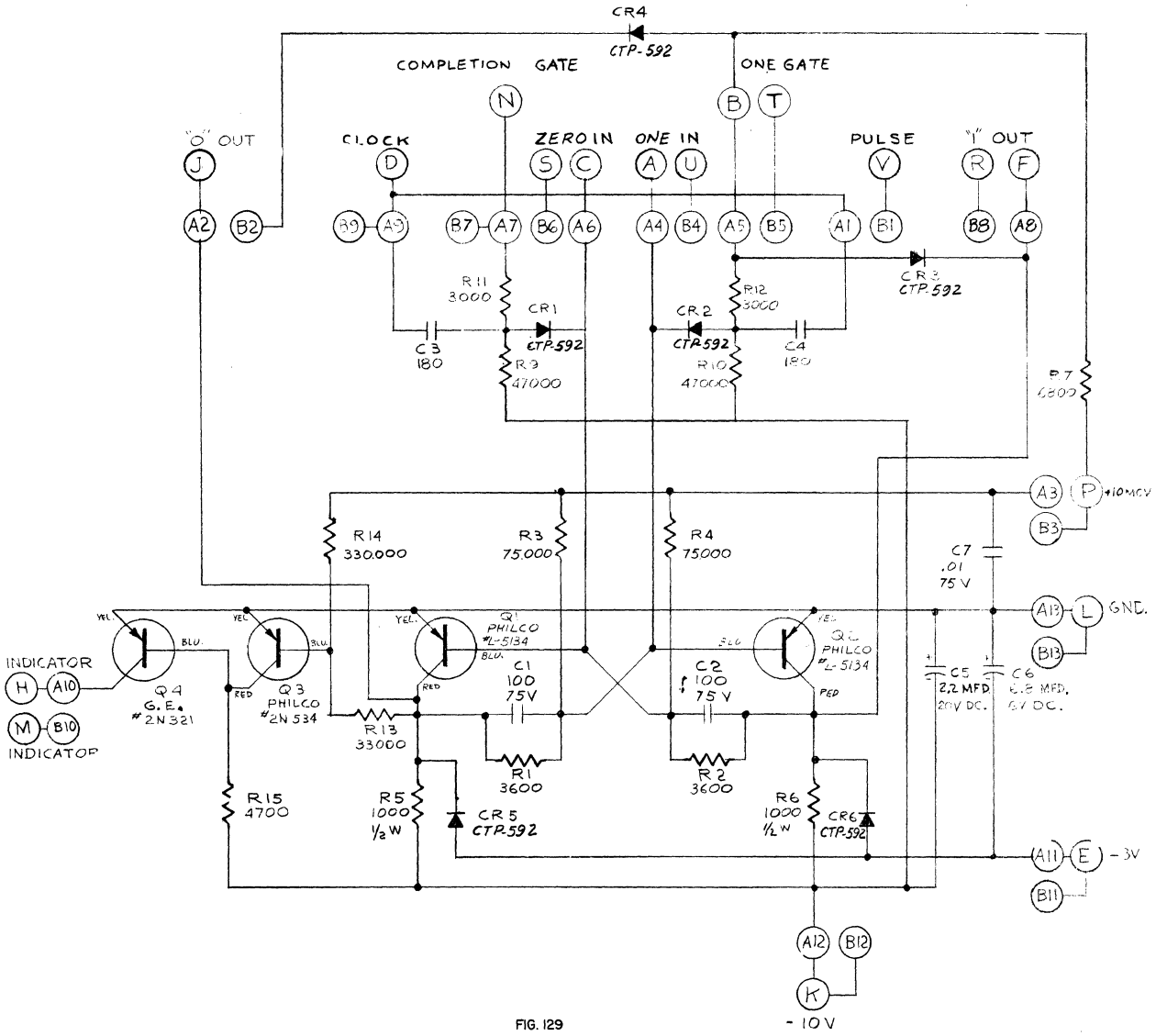


FIG. 129
SYNCHRONIZER

D-85888
"A" RED

NO. 62

SYNCHRONIZER

Handle Color: Blue Red

Drawing Number: D-85888

PW Number: 63-999

Transistors:* 4 L-5134; 2 2N534; 2 2N321

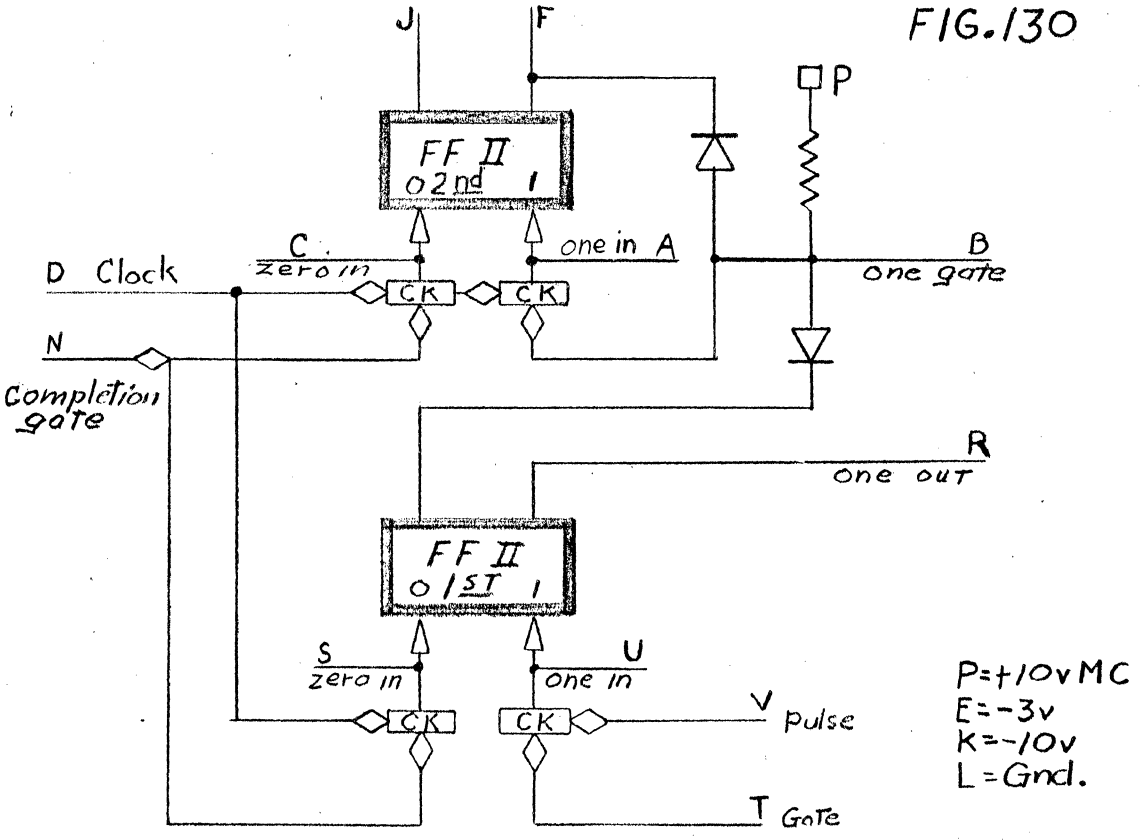
Power Supply Voltages: +10 MC; -3; -10

Use: Contains 1 complete dual flip-flop Mod II (No. 61)
Used for synchronizing circuit in in-out equipment

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

FIG. 130



SCHEMATIC

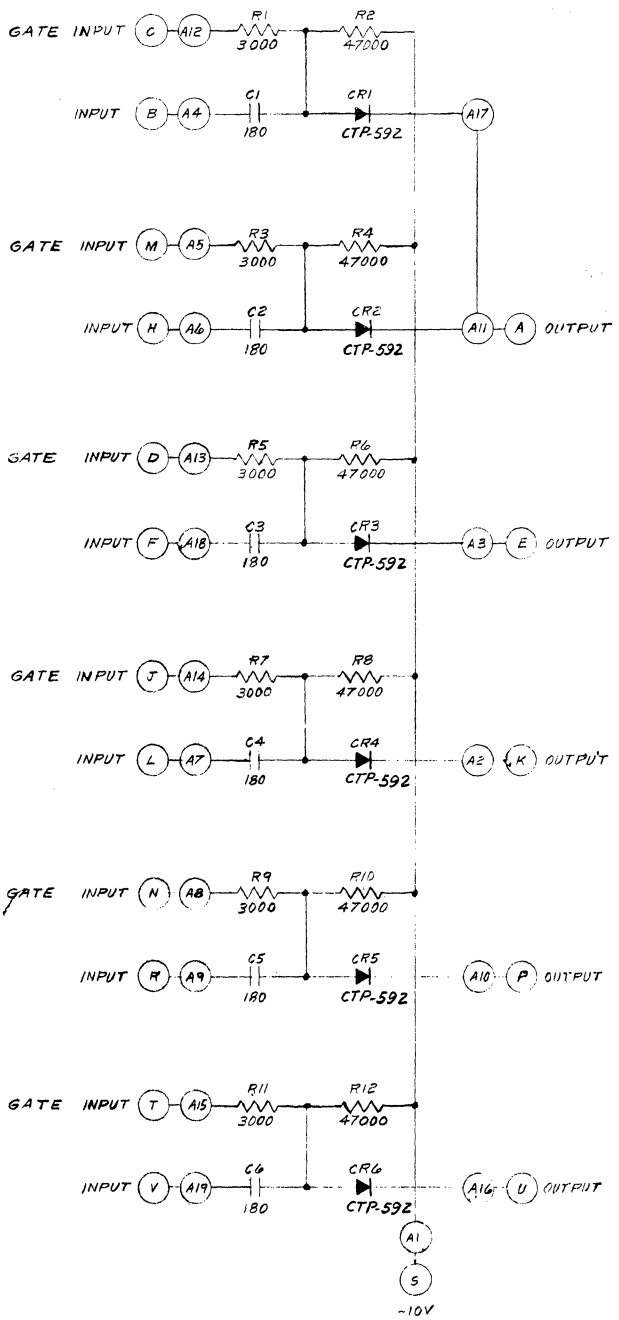


FIG. 131

CAPACITOR-DIODE GATE

D-85747
"A" REV.

NO. 63

CAPACITOR DIODE GATE (CK)

Handle Color: Blue Orange

Drawing Number: D-85747

PW Number: 63-1006

Transistors:*

Power Supply Voltages: -10

Use: Contains 6 capacitor diode gates. Can be used for mixing and gating of levels rising from -3 volts to ground. Output is positive pulse for use in in-out equipment

Remarks:

*All transistor type numbers are identified with manufacturer in appendix

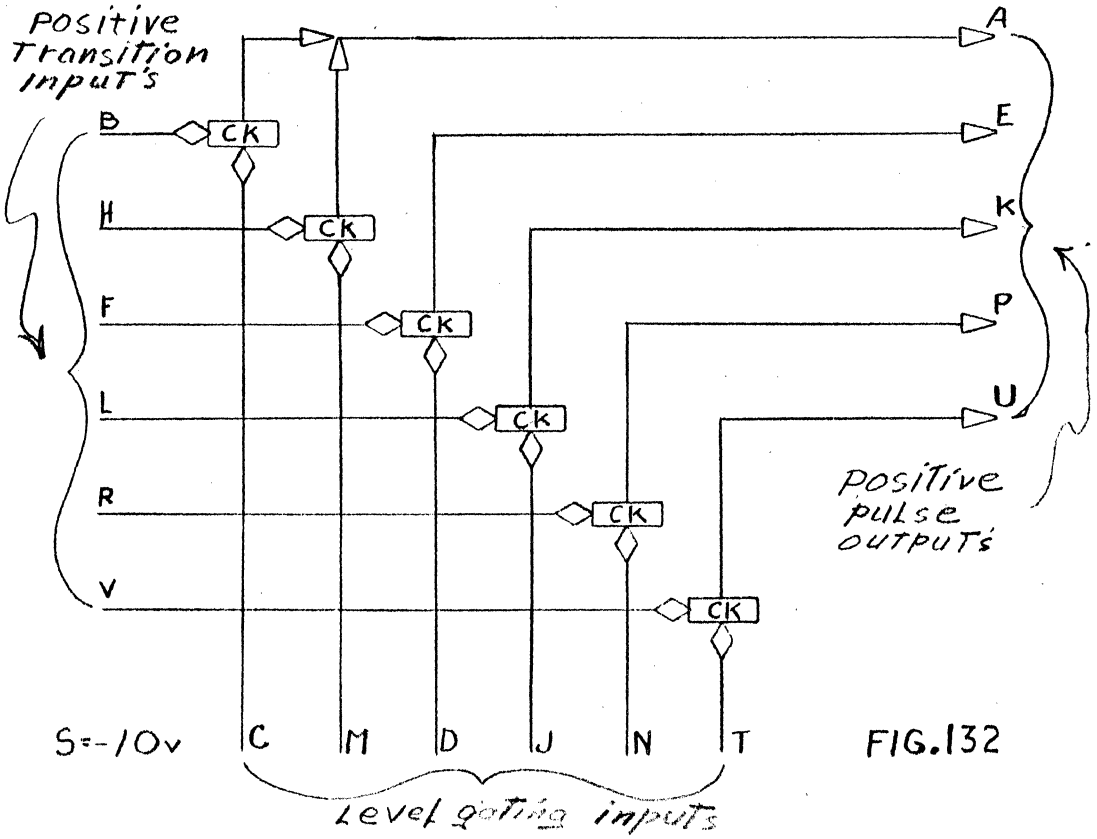


FIG. 132

SCHEMATIC

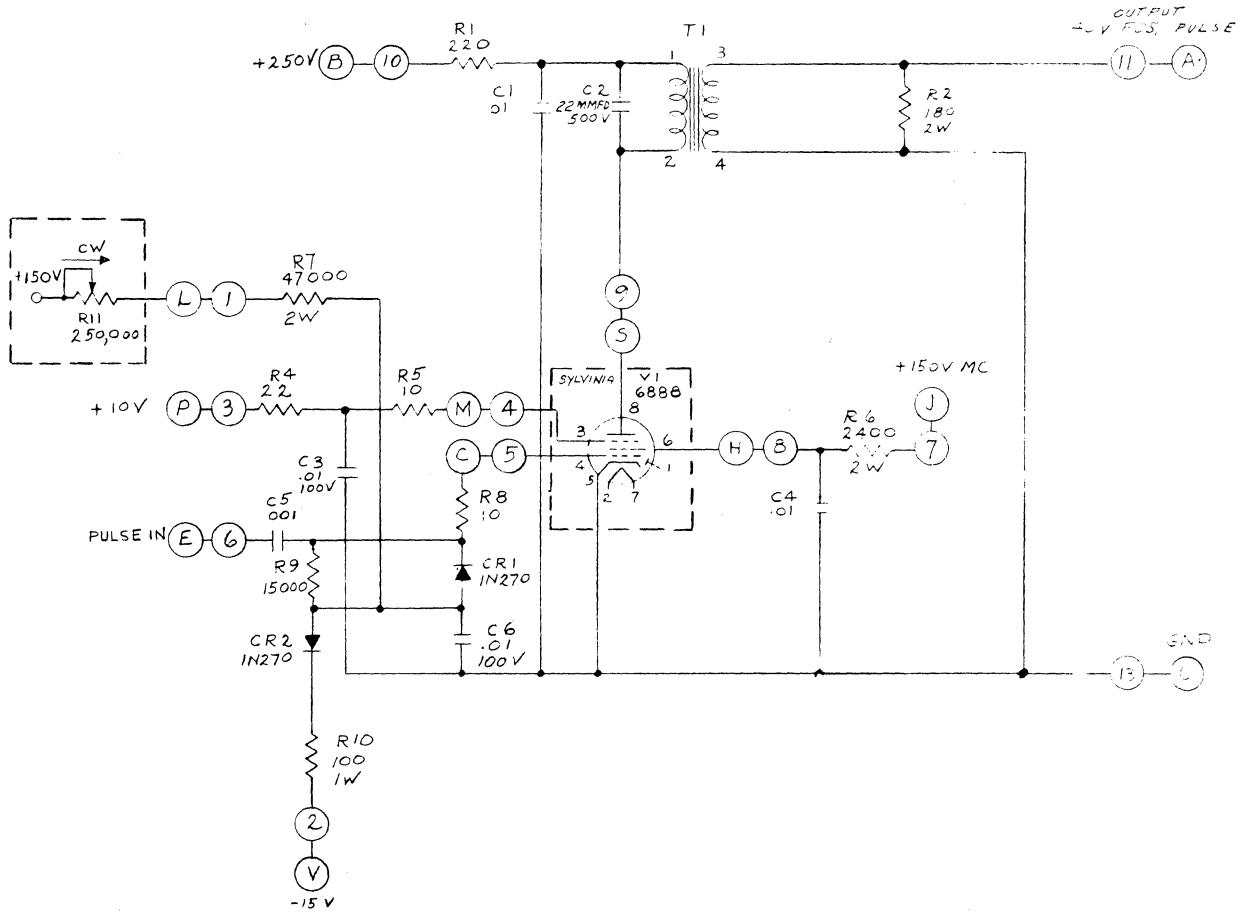


FIG. 133

VT DRIVER AMPLIFIER

D-85751
"A" RED

NO. 64

VT DRIVER AMPLIFIER

Handle Color: Blue Yellow

Drawing Number: D-85751

PW Number: 63-1013

Transistors:*

Power Supply Voltages: +250; +150 MC; +10; -15

Use: Amplification of 30 volt clock pulses. Positive output pulse feeds VT buffer amplifier (No. 67)

Remarks: Sylvania 6888 vacuum tube and 250K potentiometer mounted external to unit

*All transistor type numbers are identified with manufacturer in appendix

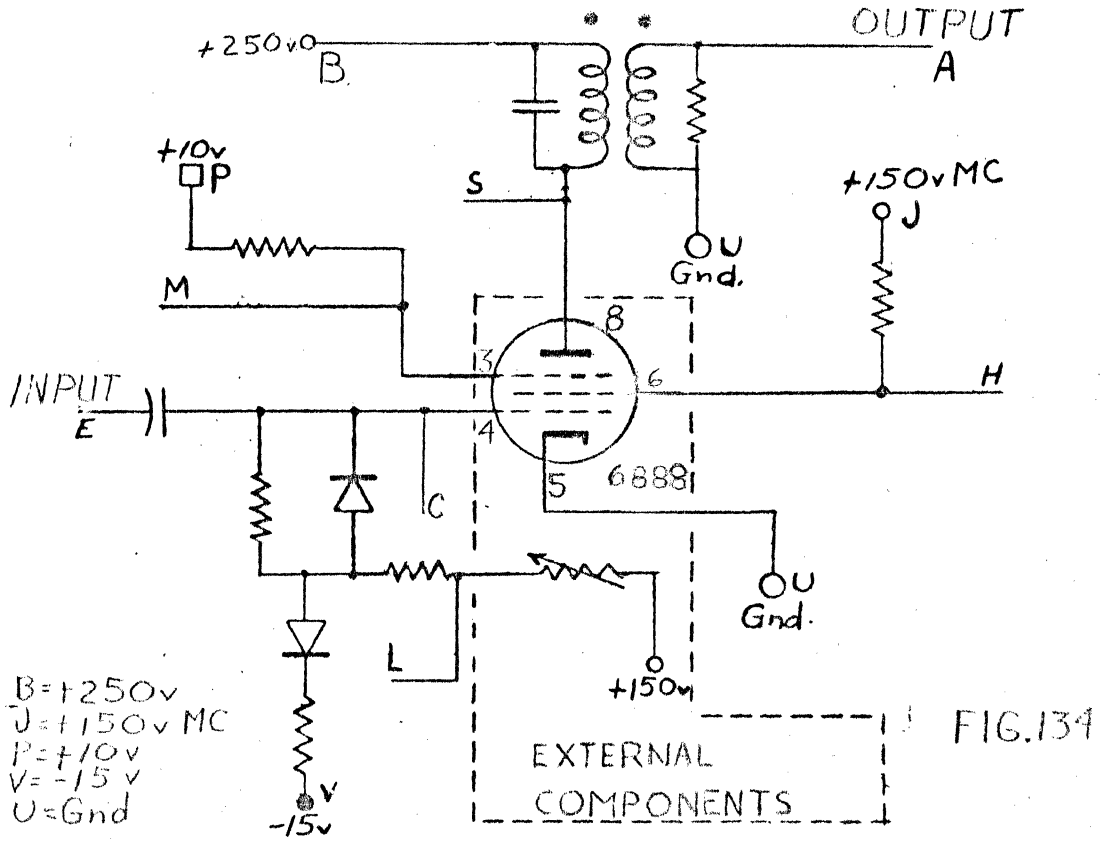
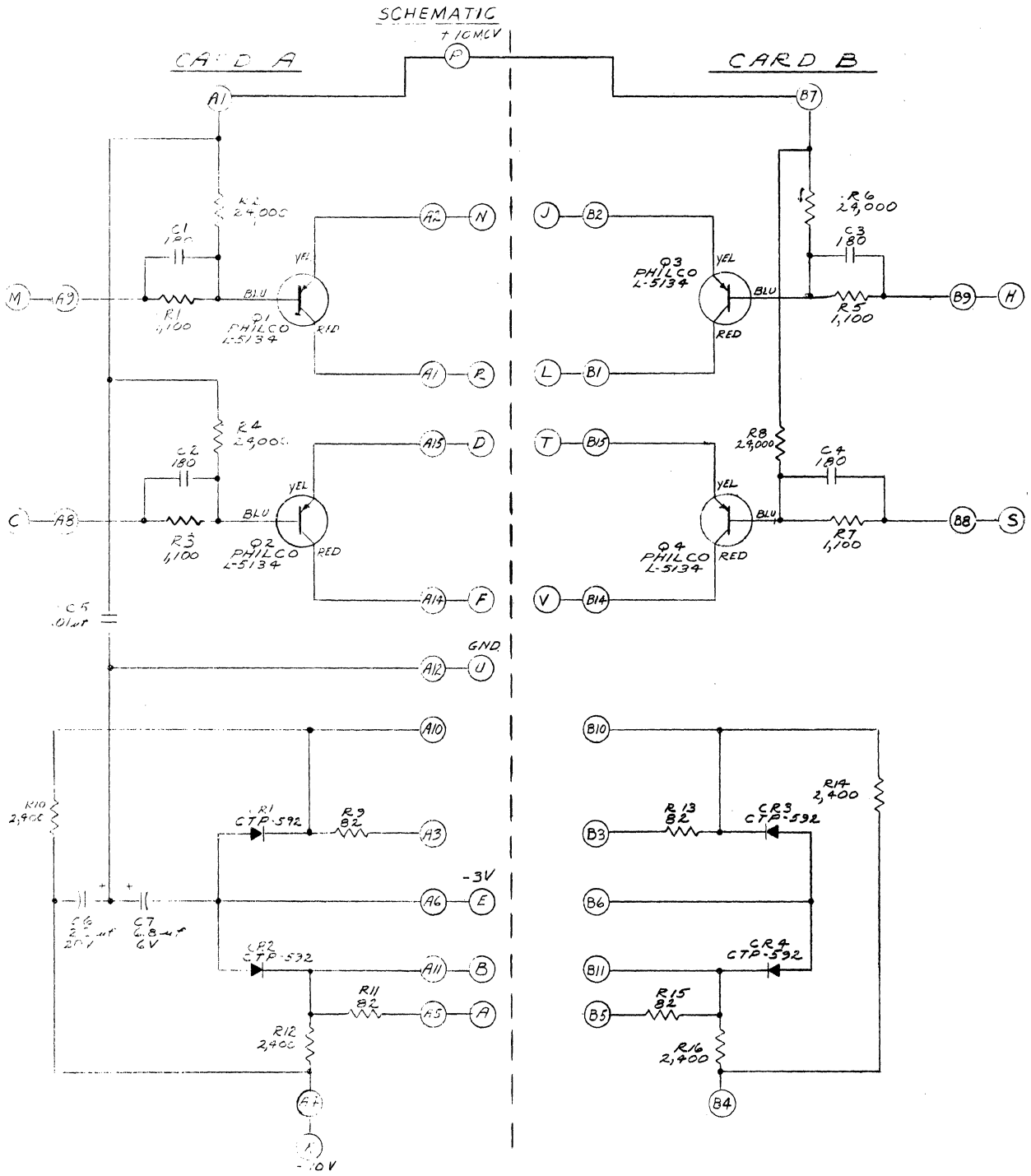


FIG. 134



D-86317
"A"-RED

FIG. 135
OUTPUT MIXER

NO. 65

OUTPUT MIXER

Handle Color: Blue Green

Drawing Number: D-86317

PW Number: 63-1000

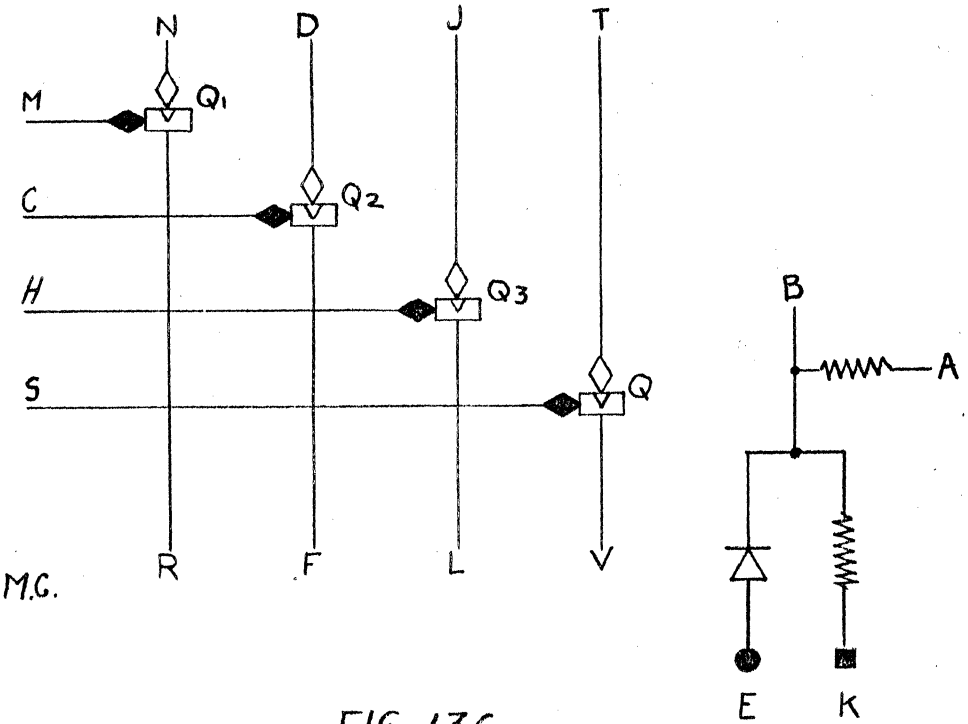
Transistors:* 4 L-5134

Power Supply Voltages: +10 MC; -3; -10

Use: 4 clamped inverters with one load resistor and one output for driving bases or driving cables. Used in in-out equipment

Remarks:

*All transistor type numbers are identified with manufacturer in appendix



P=+10v M.C.
E=-3v
K=-10v
U=Gnd

FIG. 136

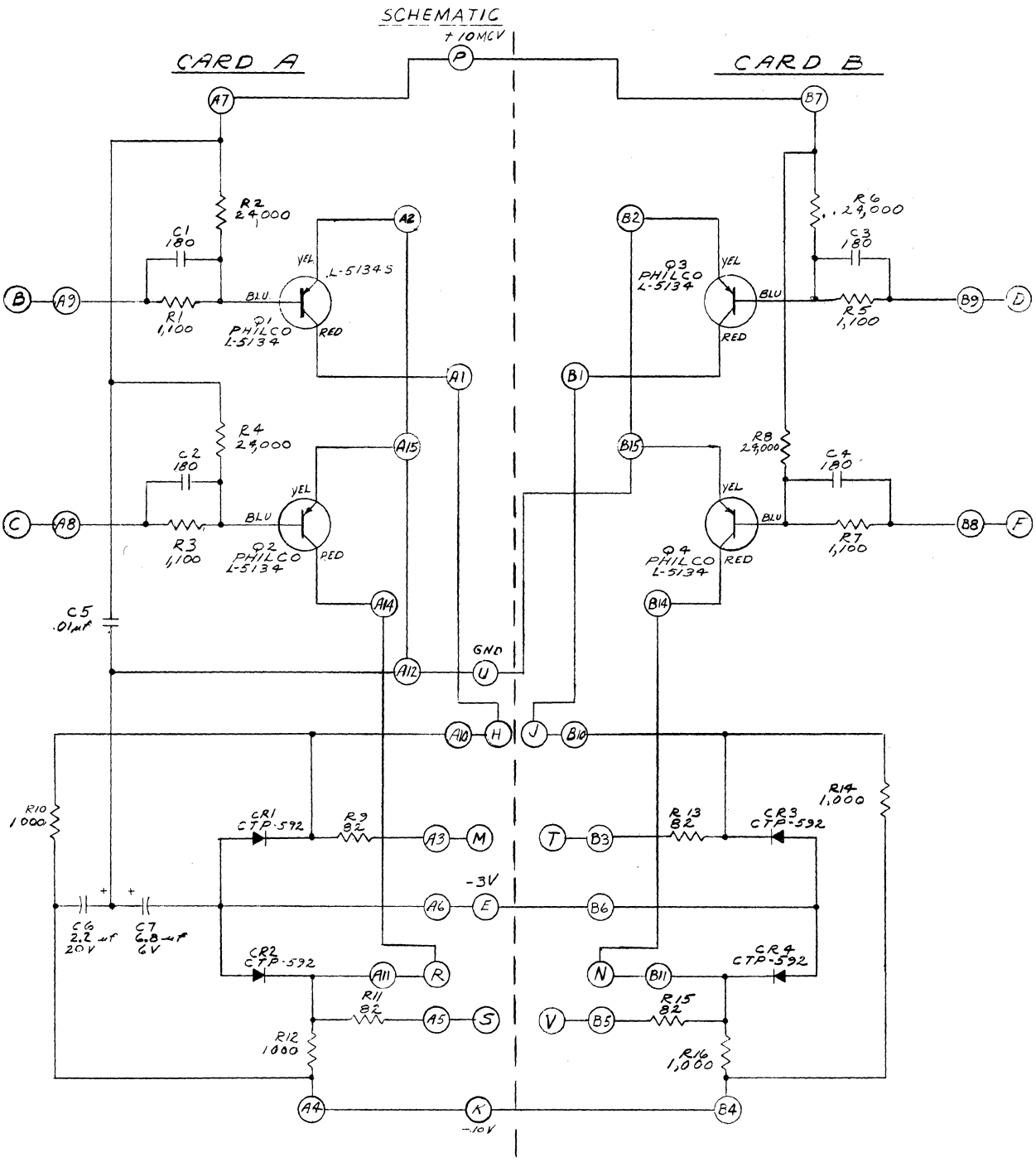


FIG. 137

LINE DRIVER

D-86893
"A" RED

NO. 66

LINE DRIVER

Handle Color: Blue Blue

Drawing Number: D-86893

PW Number: 63-1000

Transistors:* 4 L-5134

Power Supply Voltages: +10 MC; -3; -10

Use: 4 clamped inverters with 4 load resistors and outputs for driving bases and for driving cables and twisted pair lines.

Remarks: Used in in-out equipment primarily for driving cables

*All transistor type numbers are identified with manufacturer in appendix

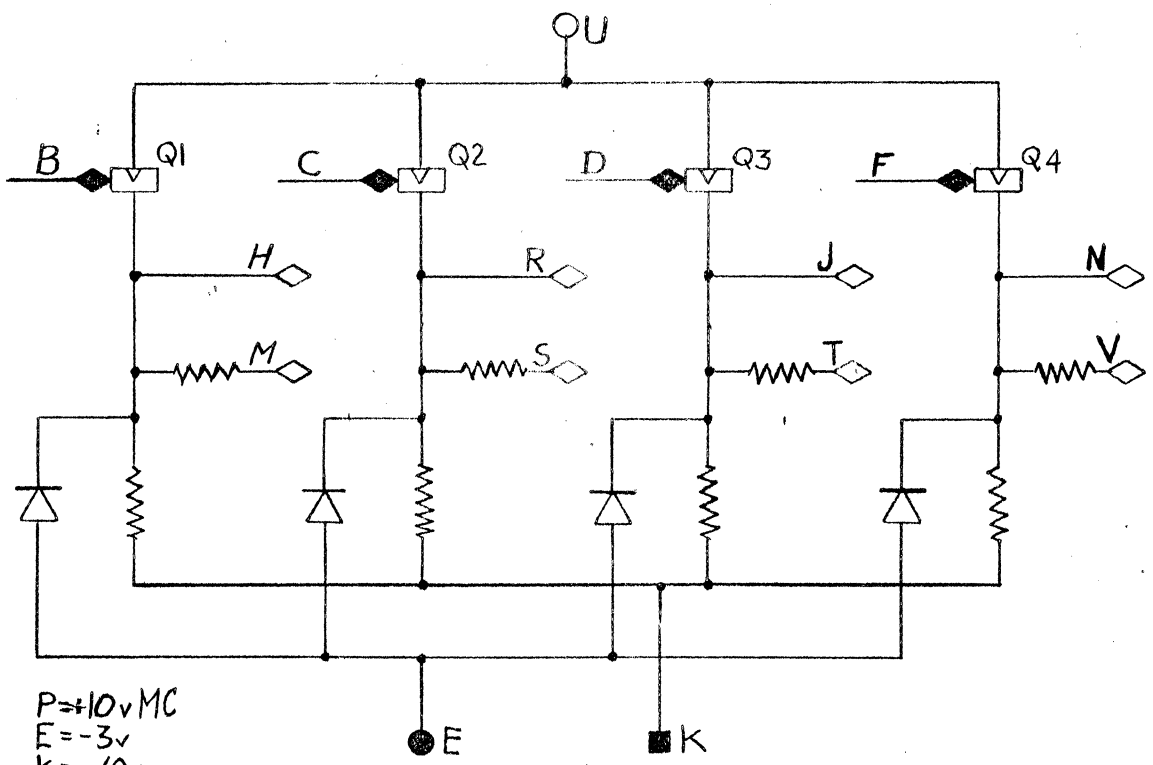


FIG. 138

SCHEMATIC

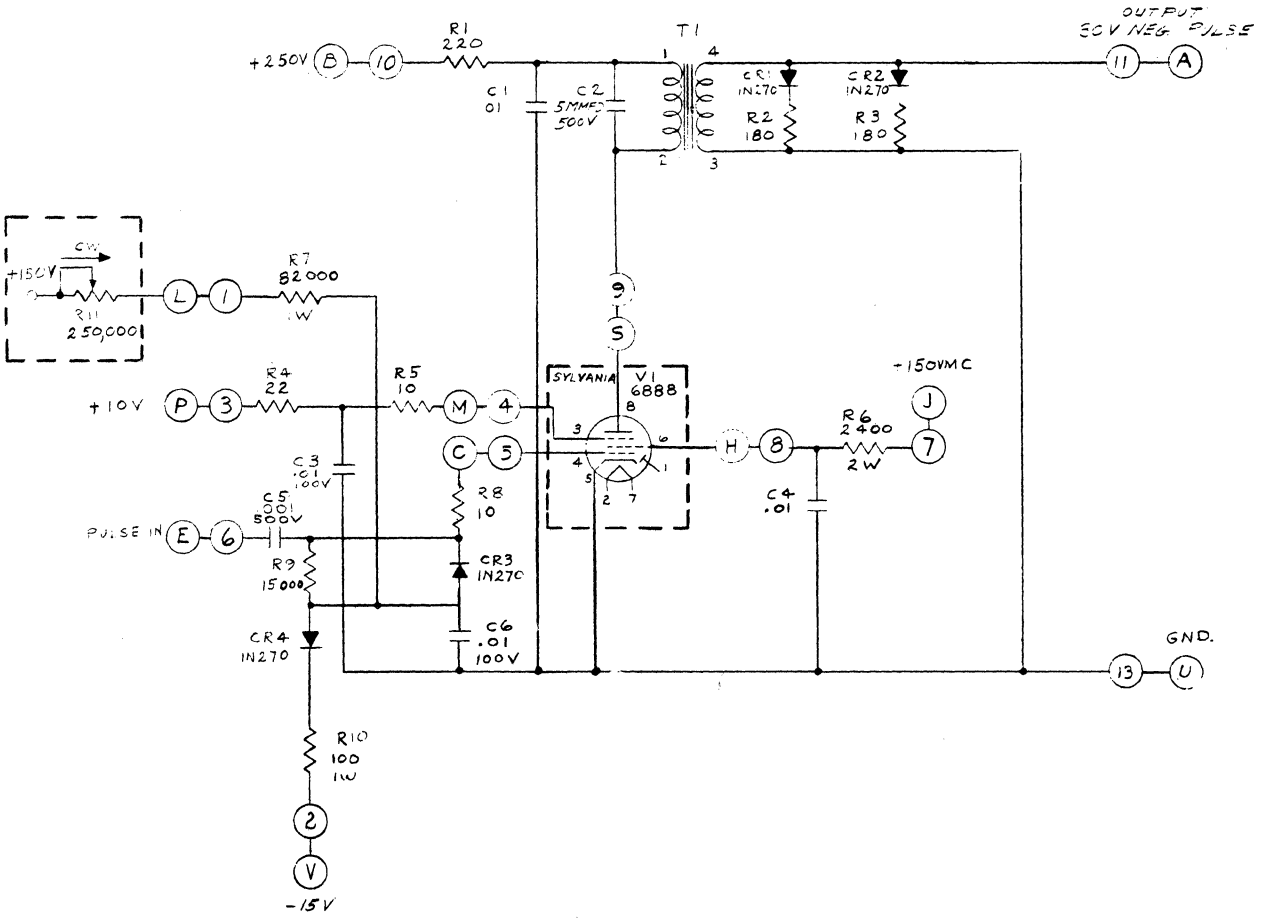


FIG. 139
VT BUFFER AMPLIFIER

D-84996
A RED

NO. 67

VT BUFFER AMPLIFIER

Handle Color: Blue Violet

Drawing Number: D-84996

PW Number: 63-1014

Transistors:*

Power Supply Voltages: +250; +150 MC; +10; -15

Use: Provides 30 volt negative pulses for driving 93 ohm cable to pulse transformers in computer

Remarks: Sylvania 6888 vacuum tube and 250K potentiometer mounted external to unit

*All transistor type numbers are identified with manufacturer in appendix

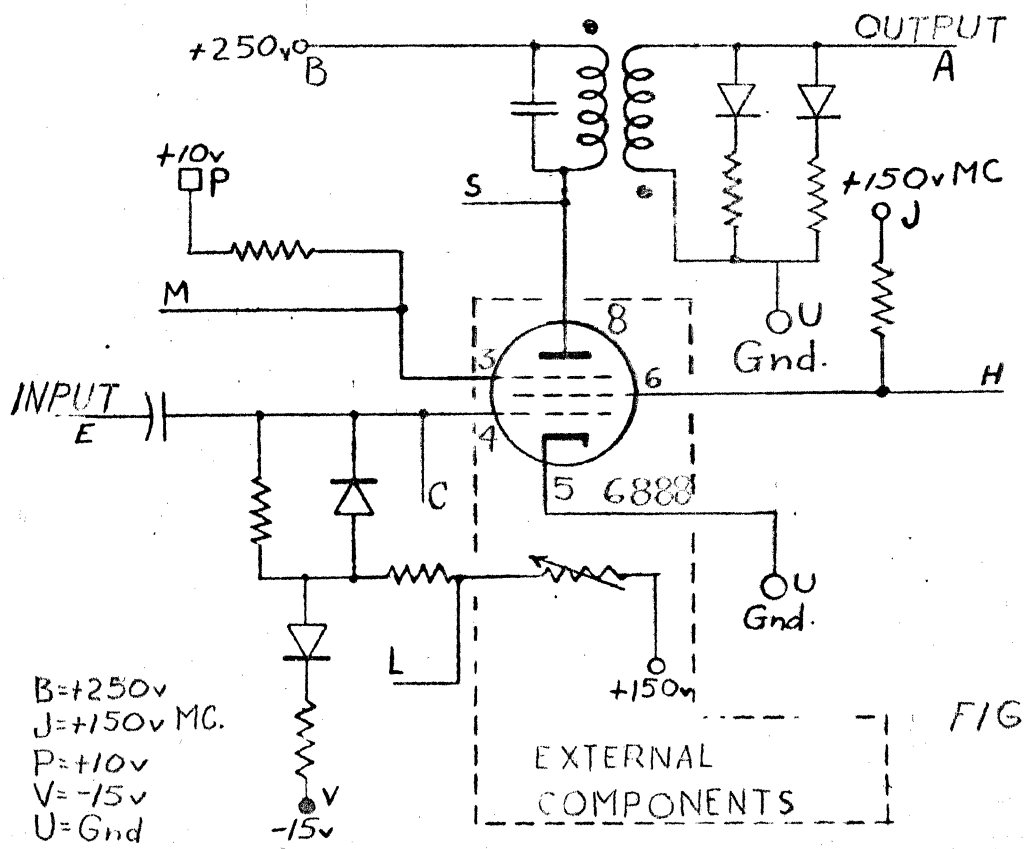


FIG. 190

SCHEMATIC
CARD-A

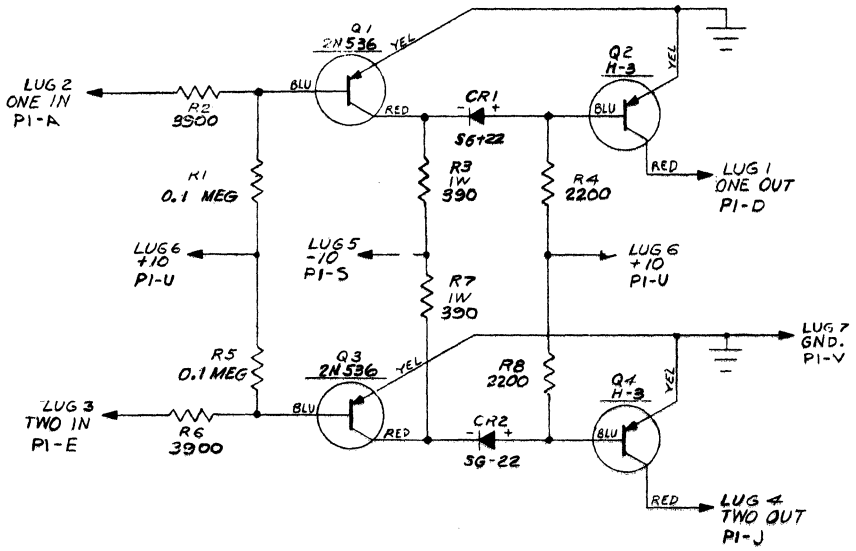


FIG. 141
LAMP LIGHTER

D-87007
"A" RED

NO. 68

LAMP LIGHTER

Handle Color: Blue Grey

Drawing Number: D-87007

PW Number: 61-874

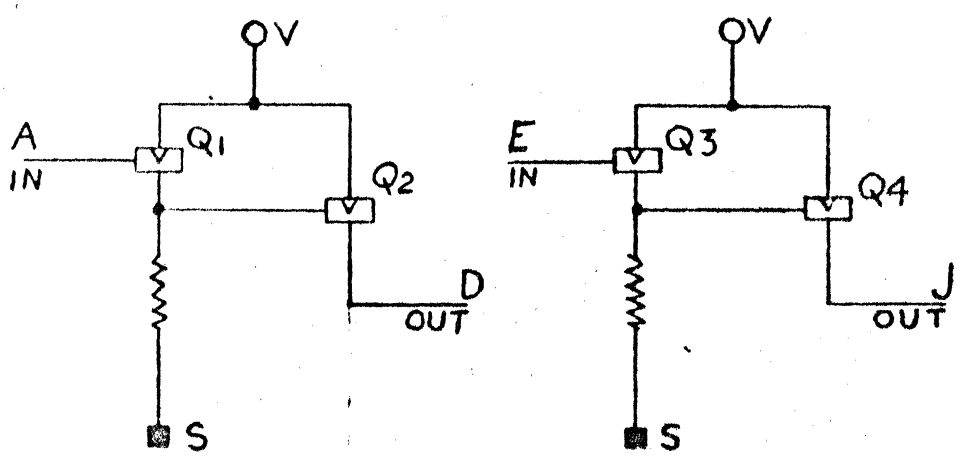
Transistors:* 2 2N536; 2 H-3

Power Supply Voltages: +10; -10

Use: Used to light 30 volt bulbs

Remarks: Maximum output current: 100 ma
Maximum output voltage: 30 volts

*All transistor type numbers are identified with manufacturer in appendix



U=+10v
S=-10v
V=Gnd.

FIG. 142

D-87655
A-REDUCTION.

SCHEMATIC

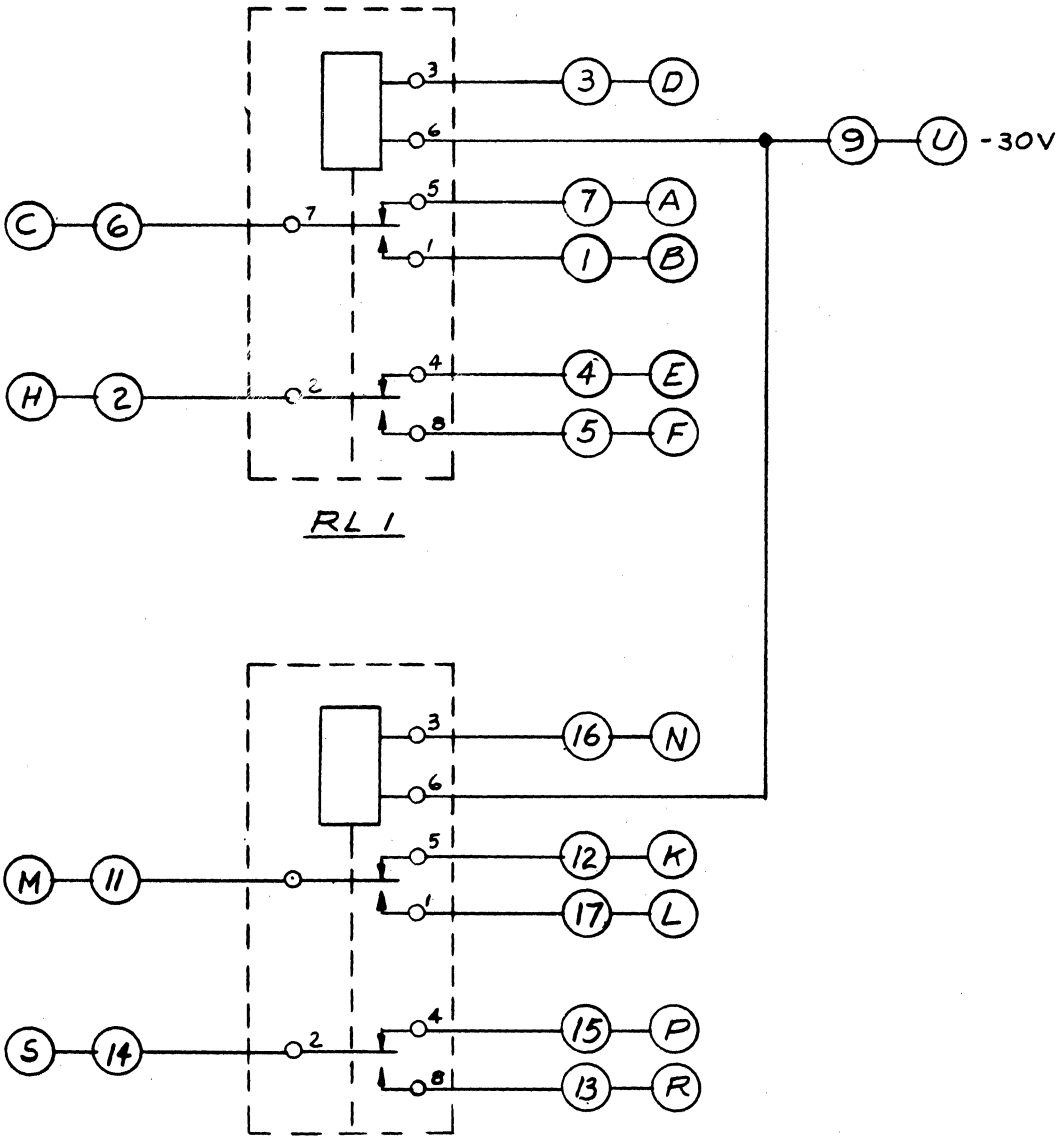


FIG. 143
RELAY UNIT.

RELAY UNIT

Handle Color: Blue White

Drawing Number: D-87655

PW Number: 63-1061

Transistors:*

Power Supply Voltages: -30

Use: Contacts will switch 2 amps with 30 volt input on coil

Remarks: Contains two double-pole double-throw relays, Clare, Type F, No. RP7638

*All transistor type numbers are identified with manufacturer in appendix

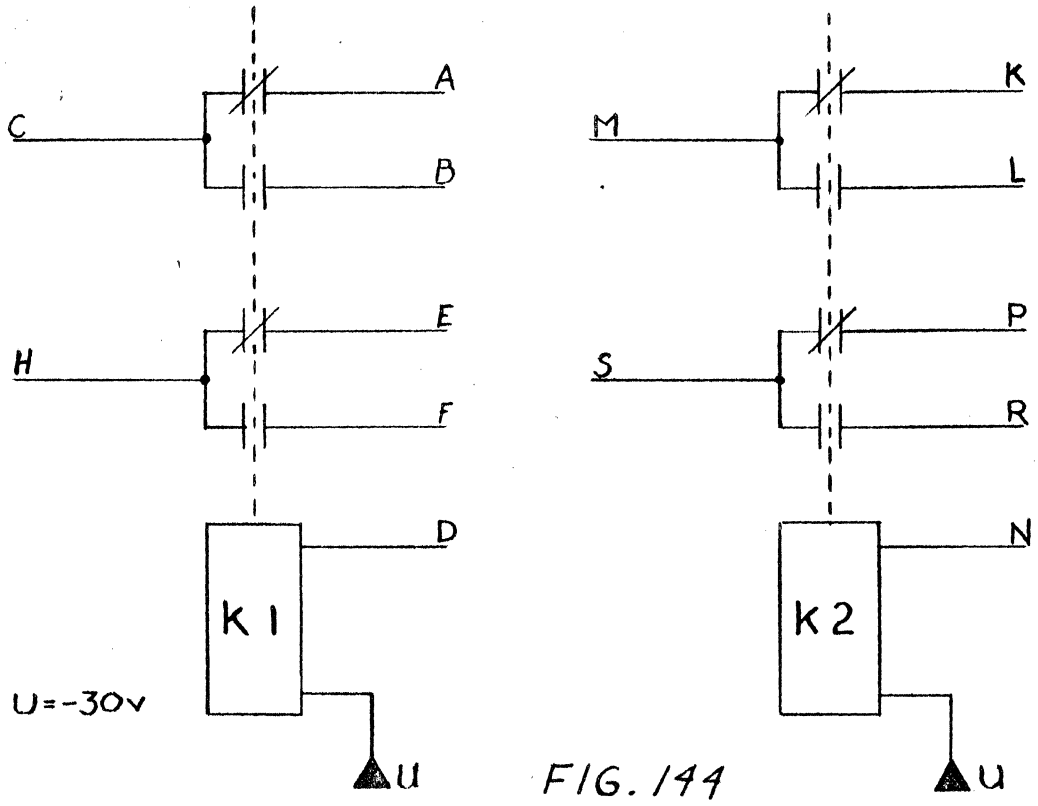


FIG. 144

APPENDIX

LIST OF TRANSISTORS USED IN TX-2 CIRCUITRY

Type Number As Listed in Text	Manufacturer	Equivalent Number	Remarks
GA-52830	Western Electric		PNP Core Switch
GT-901	Sylvania		NPN Core Switch
H-3	Minneapolis Honeywell		PNP Power
H-6	Minneapolis Honeywell	2N539	PNP Power
L-5122	Philco and Sprague	2N240 (Similar)	PNP SBT
L-5134	Philco and Sprague	2N393 (Similar)	PNP Micro-alloy SBT
L-5409	Philco	2N501	PNP Micro-alloy diffused-base transistor - Very high speed switch.
L-5432	Philco		PNP Micro-alloy diffused-base transistor - High voltage, high power 2N501.
2N123	General Electric		PNP Medium Speed
2N167	General Electric		NPN Audio, Grown Junction
2N174	Delco		PNP Power
2N188A	General Electric		PNP Audio

LIST OF TRANSISTORS USED IN TX-2 CIRCUITRY (Cont'd)

Type Number As Listed in Text	Manufacturer	Equivalent Number	Remarks
2N241A	General Electric		PNP Audio
2N321	General Electric		PNP Audio
2N357	General Transistor		NPN Medium Speed
2N396	General Electric	4JD1D1	PNP Medium Speed
2N534	Philco		PNP Audio, Miniature
2N536	Philco		PNP Audio, Miniature
2N580	RCA		PNP Medium Speed
2N635	General Electric		NPN Medium Speed
4JD1A21	General Electric	2N43 (Similar)	PNP Audio

SURFACE BARRIER TRANSISTOR SPECIFICATIONS

Philco: L-5122 T-1071 Sprague: S-5122 Similar to type: 2N240

Maximum dissipation at 40°C: 10 mw

Maximum collector voltage, V_{CB}: -6 volts

Maximum collector current: -15 ma

Minimum h_{fe} (Small signal β) (I_c = -.5 ma, V_{CE} = -3 v): 16

Minimum DC β (I_b = -.6 ma, V_{CE} = -.15 v): 8.33 for Philco units
10.0 for Sprague units

Minimum Grounded-Emitter Unity Gain Frequency, f_T (I_c = -.5 ma, V_{CE} = -3 v): 30 mc

Maximum Hole Storage Coefficient, K_s': 105 μμcoul/ma

Maximum I_{co} (V_{cb} = -5 v): 3 μamps

Maximum I_{eo} (V_{cb} = -5 v): 3 μamps

Philco: L-5134 T-1301 Sprague: S-5134 Similar to type: 2N393

Maximum dissipation at 40°C: 35 mw

Maximum collector voltage, V_{CB}: -6 volts

Maximum collector current: -50 ma

Minimum h_{fe} (Small signal β) (I_c = -.5 ma, V_{CE} = -3 v): 40

Minimum DC β (I_b = -.5 ma, V_{CE} = -.15 v): 30

Minimum DC β (I_c = -50 ma, V_{CE} = -1.0 v): 20

Minimum Grounded-Emitter Unity Gain Grequency, f_T, (I_c = -.5 ma, V_{CE} = -3 v): 30 mc

Maximum Hole Storage Coefficient, K_s': 160 μμcoul/ma

Maximum I_{co} (V_{cb} = -5 v): 5 μamps

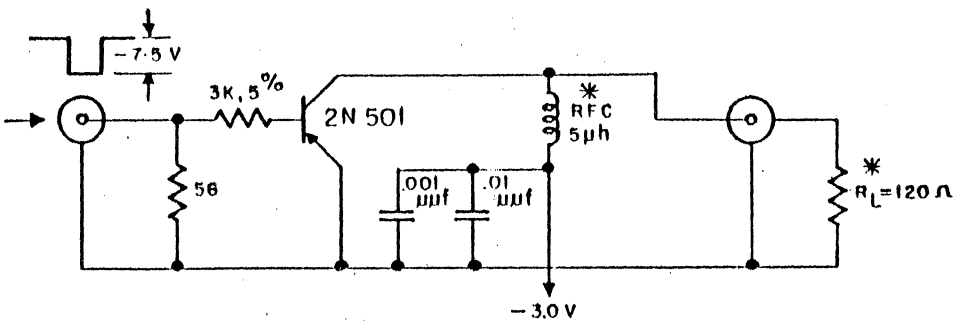
Maximum I_{eo} (V_{cb} = -5 v): 10 μamps

SURFACE BARRIER TRANSISTOR SPECIFICATIONS (Cont'd)

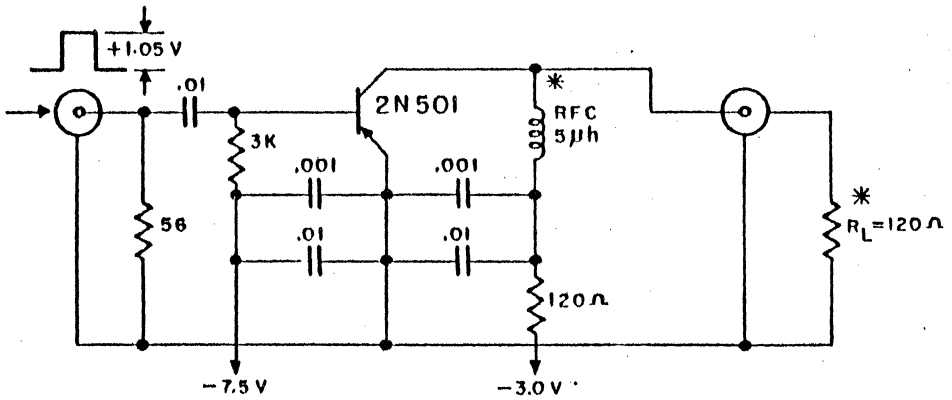
Philco: 2N501
L-5409

Maximum dissipation at 40°C:	35 mw
Maximum collector voltage, V_{CB}:	-15 volts
Maximum collector current:	-50 ma
Maximum emitter voltage, V_{EB}:	2 volts
Minimum DC β (I_c = -10 ma, V_{CE} = -.5 v):	20
Minimum DC β (I_c = -50 ma, V_{CE} = -.5 v):	20
Maximum rise time:*	18 mμsec
Maximum storage time:*	12 mμsec
Maximum fall time:*	10 mμsec
I_{co} (V_{CB} = -5 v):	5 μamps

*NOTE: These times are measured in Philco Test Circuits described in the Philco specification sheet for the 2N501 and shown below. These times do not necessarily coincide with those in TX-2 circuitry.



RISE TIME TEST CIRCUIT



DELAY AND FALL TIME TEST CIRCUIT

LIST OF M-NOTES PERTAINING TO TX-0, TX-2, AND SURFACE BARRIER TRANSISTORS

Number	Title	Author	Date
6M-3649	Typical SBT Static Characteristics	E.U. Cohler	5/31/55
6M-3830	Positive Bias as Applied to Surface-Barrier Transistor Switching Circuits	K.H. Konkle E.U. Cohler	8/12/55
6M-4521	A LaPlace Transform Anaylsis of Pulse Beta	R.C. Johnston	8/21/57
6M-4521, S-1	A LaPlace Transform Analysis of Pulse Beta	R.C. Johnston	9/12/57
6M-4561	TX-0 Circuitry	J.R. Fadiman	10/22/56
6M-4571	Transistor Logic in TX-0	R.C. Jeffrey	9/5/56
6M-4789	A Functional Description of the TX-0 Computer	J.T. Gilmore H.P. Peterson	11/20/56
6M-4955	Parameter Distributions for the Philco L-5122 Surface-Barrier Transistor	D.J. Eckl	3/19/57
6M-4968	The Lincoln TX-2 Computer	W.A. Clark et al.	4/1/57
6M-5097	TX-0 Direct Input Utility System	J.T. Gilmore	4/10/57
6M-5193	Inverters and Flip-Flops using L-5134 Transistors	J.W. Langford	8/28/57
6M-5199	A Two Transistor Flip-Flop for the TX-2 Computer	R.A. Hughes	9/3/57
6M-5216	A Transistorized Variable Delay Unit	L. Kleinrock	9/12/57

LIST OF M-NOTES (Cont'd)

Number	Title	Author	Date
6M-5216, S-1	A Transistorized Variable Delay Unit	J.R. Fadiman	1/20/58
6M-5590	TX-2 Gated Pulse Amplifier	L. Neumann	3/13/58
6M-5661	Toggle-Switch Storage System, TX-2	L. Neumann	4/21/58
6M-5701	A Computer-Integrated, Rapid Access, Magnetic Tape System with Fixed Address	R.L. Best T.C. Stockebrand	5/16/58
6M-5780	Some Examples of TX-2 Programming	H.P. Peterson	7/23/58
6M-5856	Some Applications of 2N501 Transistors to Switching Circuits	J.W. Langford	8/29/58