DIVISION 6

LINCOLN LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASSACHUSETTS

Report 6R-215

STANDARD TEST EQUIPMENT

Reprinted 1 December 1957

Report by
Div. 6 Test Equipment Committee

2. The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19 (122)-458.

PREFACE

This report describes the Division 6 Standard Test Equipment, composed of Whirlwind Units, Burroughs Pulse Control Equipment, Plug-In Units (vacuum tube), and Digital Equipment Corp. Building Blocks (transistorized).

The test equipment units have been designed with a maximum of flexibility to be used as building blocks for test systems ranging in complexity from very simple setups requiring one or two panels to very extensive setups requiring several racks of equipment.

The equipment described in this report will be supplemented from time to time as needs for other units develop.

The Test Equipment Committee has endeavored to provide the engineer with a line of standard test equipment which would relieve him of the time consuming and diversionary task of designing his own test equipment. The standard test equipment is thus a powerful tool which permits the engineers of this laboratory to perform tests which would otherwise require a very long time or not be undertaken at all.

Division 6 Test Equipment Committee

rjm

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STANDARD TEST EQUIPMENT

INTRODUCTION

DEFINITION

The term "standard test equipment" is applied to any unit which has been approved by the Test Equipment Committee for quantity purchase or production.

Standard test equipment may be one of four types: Whirlwind units, Burroughs units, plug-in units, and Digital Equipment Corp. Building Blocks. Whirlwind and plug-in units are assembled in either the Laboratory's shop or in the shop of a contractor, Burroughs units are built by the Burroughs Adding Machine Co. and its subsidiary the Control Instrument Co., Inc., and the Digital Equipment Corp. builds the DEC Building Blocks.

TYPICAL USES OF STANDARD TEST EQUIPMENT:

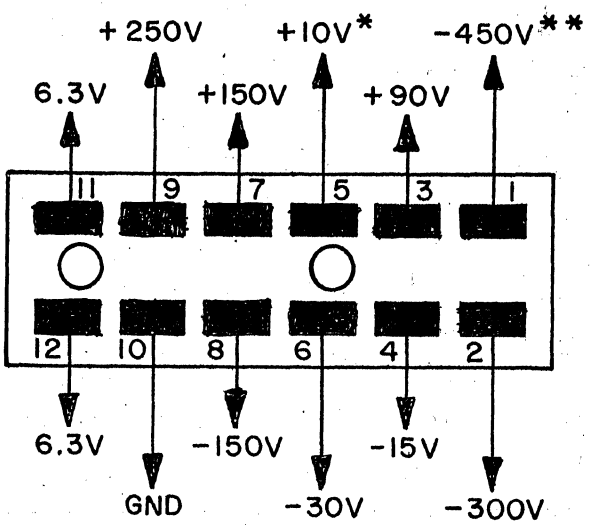
The equipment described in the following sections has been assembled as building blocks to perform numerous tasks. During computer design, this method is extremely valuable in examining the behavior of basic circuits such as flip flops and gates under system conditions. Even more important is its use in testing and simulating large computer elements (storage, arithmetic registers, and arithmetic control). This application alone has saved many months in computer installation by permitting testing of one element before an associated element was completed.

LABORATORY POWER SUPPLY:

Most laboratory work benches are equipped with centrally mounted power box which supplies the following voltages:

DC Voltages		
Positive	Negative	AC Filament Voltages
10 (Lexington only)		
90	-15	
120 (Barta Bldg. only)	-30	6.3
150	-150	
250	-300	

The front panel of the box has four outlets for Jones 12-pin cable connectors. All boxes have an on-off switch and green indicator lights for the 6.3V AC. The older boxes, most of which are located in the Barta Building, have an on-off switch and a red indicator light for the DC voltages. The newer boxes have an on-off switch for all the DC voltages except -450. (For safety reasons, -450V had its own switch; the supply has since been disconnected.) Indicator lights for each of the negative voltages are correspondingly marked. The drawing reproduced below, which specifies the voltages at the twelve terminals, is attached to the conduit under each box.



* Except Barta Building, where Pin 5 carries +120V.
** The -450V supply is disconnected.

Heinemann circuit breakers capable of switching in 1 millisecond are used in all the DC lines; they are located in nearby wall-mounted circuit breaker boxes. One such box can supply power to as many as six bench power boxes.

Benches are supplied with 115V AC through the circuit breaker in the AC power box located at the end of the bench. Numerous AC outlets are provided by the terminal strip along the shelf at the top of each bench and by a short terminal strip or electrical outlet box on the lower side of the bench top. The DC power box is supplied with 6.3V AC by a bench-mounted transformer, the primary of which is connected to the AC power box.

When racks of vacuum-tube equipment are used, power should be supplied through the rack power-control unit described in Section 6, below.

The DEC plug-in units differ from the others in that they do not use the central lab power supply. The special DEC power supply is described in Section 30, below, along with the rest of this line of equipment.

SPECIFICATION SHEETS:

A photograph of each unit is followed by its general description and specifications, including circuitry, controls, and power requirements. The last item on the sheet lists all the pertinent references on the unit for those who may be interested.

Immediately following the specification sheet is an A-size reduction of the unit's circuit schematic.

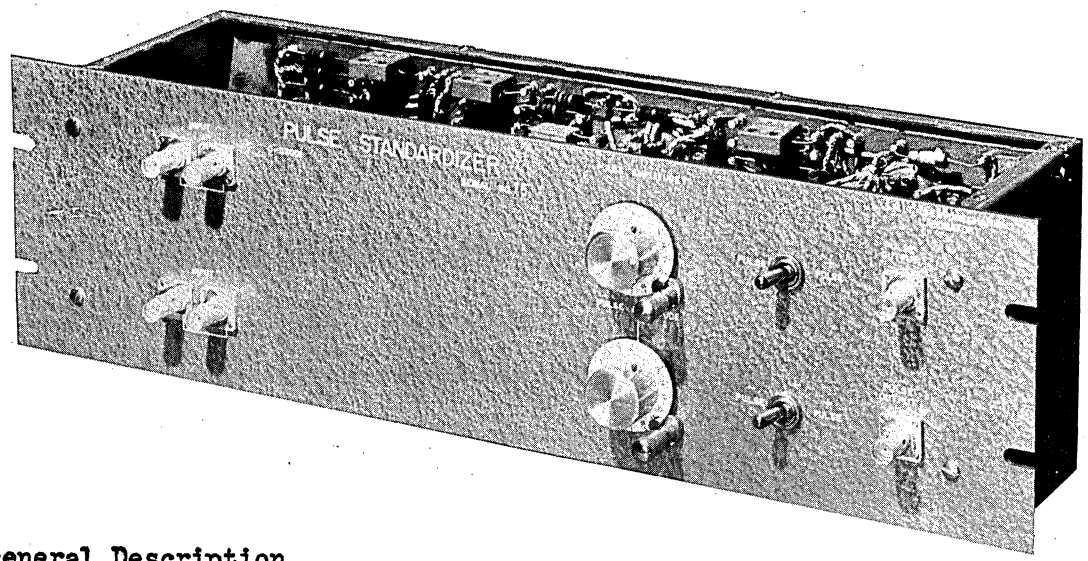
Similar units have been put in the same section, Whirlwind units always preceding Burroughs' units. Names conform to standard Laboratory nomenclature. The type numbers appear with the Burroughs' units. The letter "W" following a Burroughs-type number indicates that the unit so labeled is built according to Division 6 specifications and requires the voltages listed above. However, several hundred Burroughs' units were delivered before the letter "W" was added to the type number. Test equipment built by Burroughs for other users than Division 6, Lincoln Laboratory, likewise has no "W" following the type number and differs in requiring such power-supply voltages as +105 volts and -400 volts.

As other units are acquired, specification sheets will be prepared and distributed to holders of this book.

Division 6 Test Equipment Committee

rjm

PULSE STANDARDIZER



General Description

The pulse standardizer is used to convert positive pulses of different amplitudes and shapes to standard 0.1-μsec half-sine-wave pulses whose amplitude and shape are independent of the input amplitude and shape. It is used to provide standard pulses for test equipment, computer components, and for making measurements on basic circuits. The unit is constructed in duplicate on a single panel and chassis.

Specifications

Dimensions: 4-1/2 x 5-1/2 x 19 inches.

Circuits:
5687/2 buffer amplifier
5687/2 inverter
6AG7 RLC peaker
6AG7 buffer amplifier

Input (each unit): 2 parallel jacks. Input pulse must be positive, but amplitude may vary from 12 v min. to 50 v max. Resolution time: 0.45 μsec.

Output (each unit): Standard 0.1-μsec pulse. Polarity reversible. Amplitude range 12 to 35 volts, controlled by potentiometer in final buffer. Bus-driver crystal rectifier in output.

Minimum Delay (through each unit): 0.1 μsec

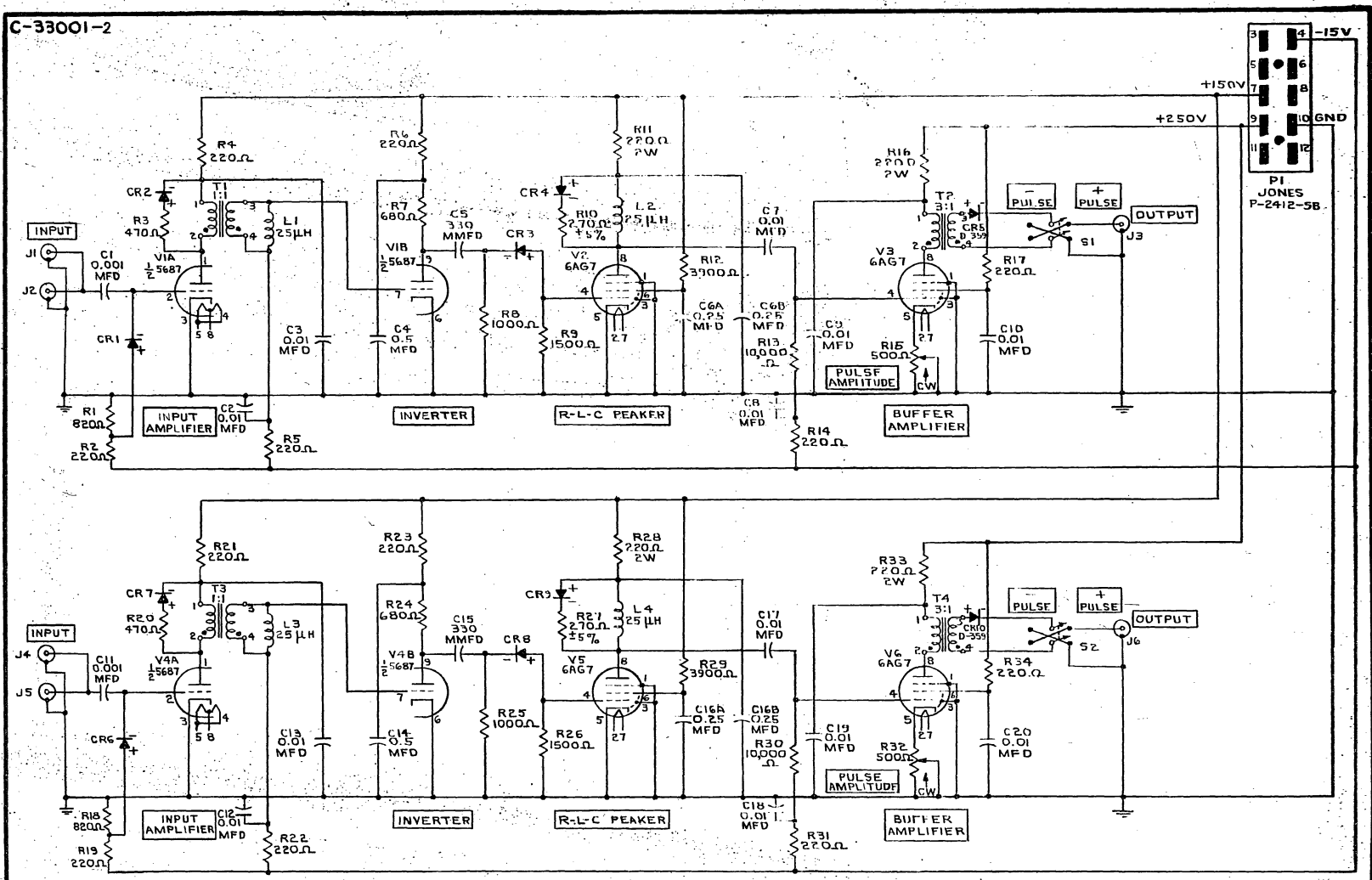
Power Requirements (both units):

Voltages	Currents	
	No Sig.	1-mc pulse
+250 v d.c.	1.75 ma	25 ma
+150 v d.c.	105.0 ma	175 ma
- 15 v d.c.	30 ma	30 ma
6.3 v a.c.	4.4 amp	4.4 amp

References

Circuit Schematic: C-33001

C-33001-2



DRAWING REFERENCES:
PHENOLIC PANEL ASSEMBLY: SC-40078.

FOR SPECIFICATION OF COMPONENTS,
SEE PL-33001.

NOTES:
1. RESISTORS ARE 1W, ±10%.
2. VIDEO CONNECTORS ARE UG-290/U.
3. CRYSTAL RECTIFIERS ARE 1N34'S OR D-357'S.
4. CAPACITORS ARE MICA, ±10%, EXCEPT C6A, C6B AND C16A AND C16B; WHICH ARE OIL-FILLED DUAL BATHTUBS.

APPROVED BY: DATE: THIS IS A GRADE 2 DRAWING OF HIGHEST GRADE APPROVED BELOW.
GRADE 1 - FOR REFERENCE ONLY
GRADE 2 - PRELIMINARY DESIGN
GRADE 3 - FINAL DESIGN
11/15/48

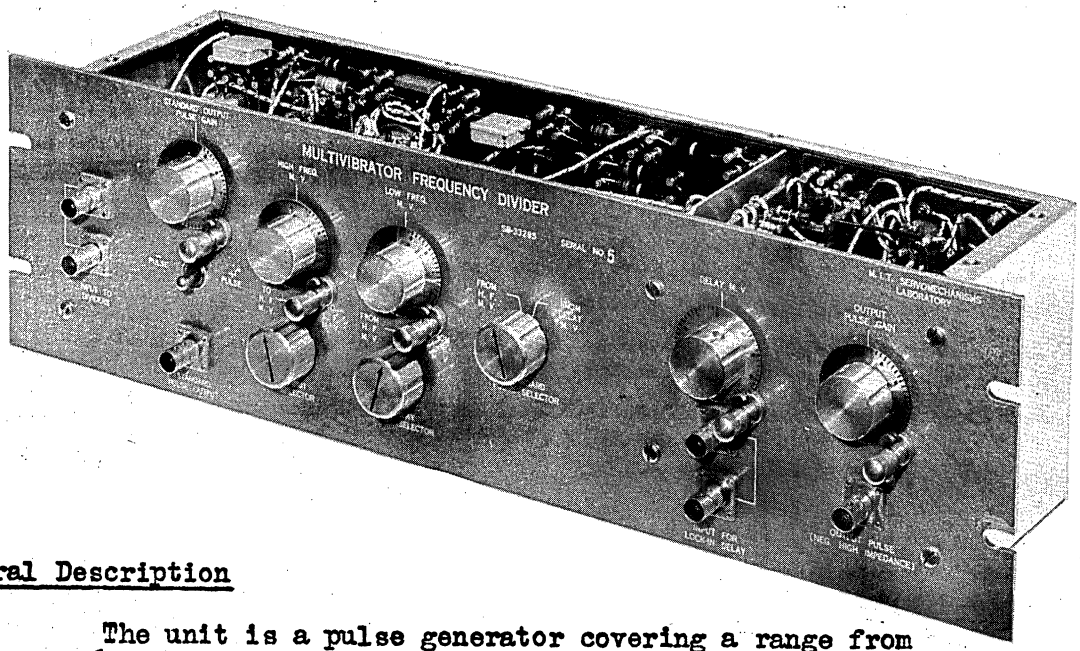
SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC, PULSE STANDARDIZER

SCALE: —
DR. D.C.S. 9-30-48
ENG. HR Nov 15 48
CK. TC 11/15/48
APP.

C-33001-2
B-REDUCTION

MULTIVIBRATOR FREQUENCY DIVIDER



General Description

The unit is a pulse generator covering a range from 200 kc to 60 cps and which may be synchronized with any frequency equal to or greater than the output frequency. Two output pulses are provided: one a standard 0.1-μsec pulse, the other a high-impedance negative pulse used to trigger a synchroscope.

Specifications

Dimensions: 5 1/4 x 6 x 19 inches, for rack mounting.

Circuits:
2 input pulse amplifiers (each 1/2 5687).
High-freq. multivibrator (5687).
Low-freq. multivibrator (2C51).
Pulse generator for 0.1-μsec pulses (1/2 5687).
Delay multivibrator (5687).
Output amplifier for 0.1-μsec pulses (6AG7).
Output amplifier for high-impedance pulses (1/2 5687).

Input to Dividers: Input pulses - positive, 0.1 μsec or longer.
Pulse amplitude - 15 v min.
PRF - 60 cps to approx. 5 mc.
Multivibrator ranges overlap between 2.5-3 kc.

Input to Lock-in Delay: For synchronized delay, positive pulses may be fed to this input. These are amplified and fed to the delay multivibrator.

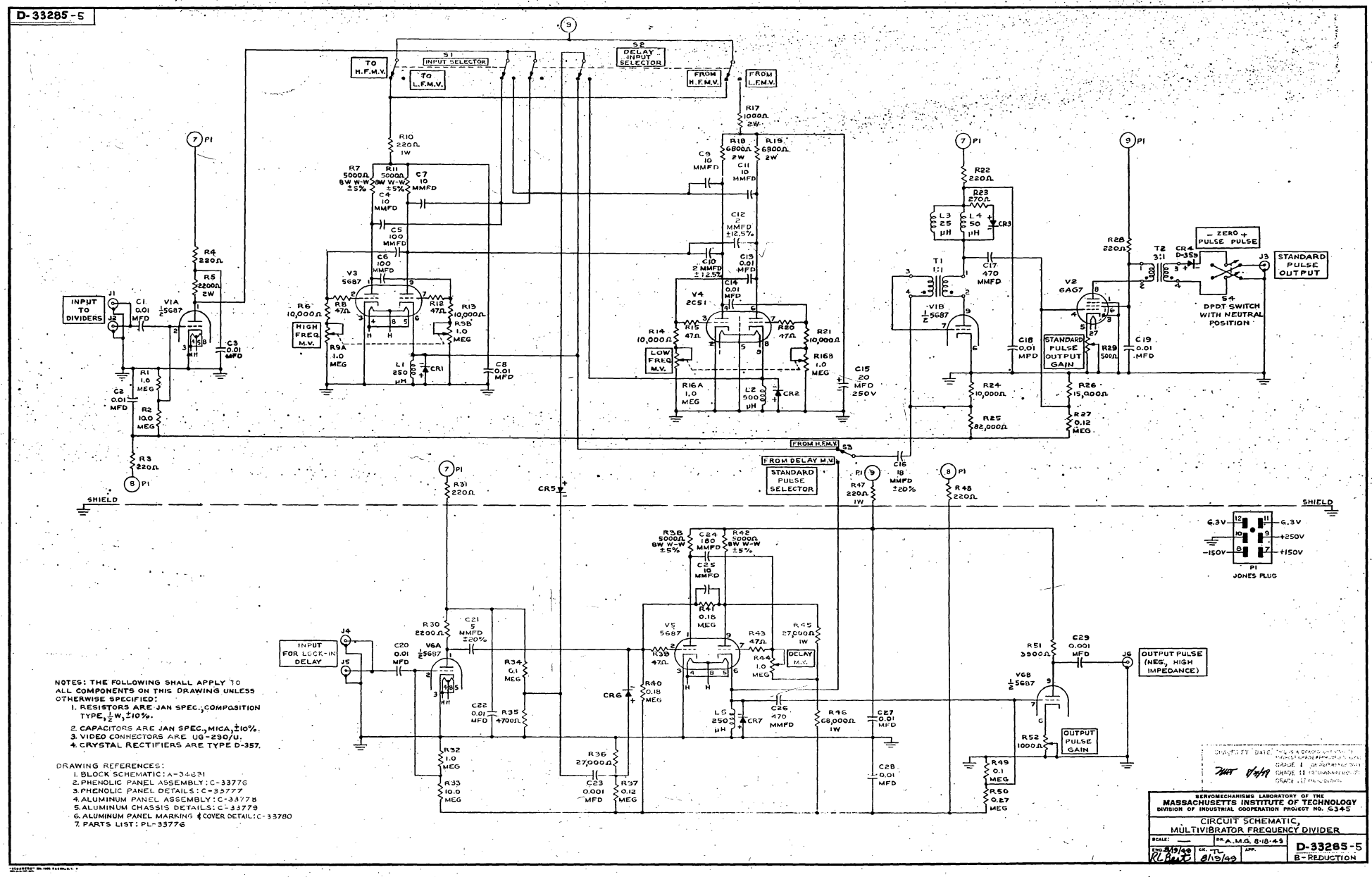
Standard Pulse Output: 0.1-μsec half-sine-wave pulses, polarity reversible; amplitude adjustable up to 25 v when output feeds a 93-ohm terminated line.

Output Pulse (Neg. High Impedance): 0.2-μsec leading edge, amplitude adjustable up to 100 volts. Will drive an unterminated 93-ohm line of reasonable length. Occurs at the end of a delay interval variable from 5 to 100 μsec.

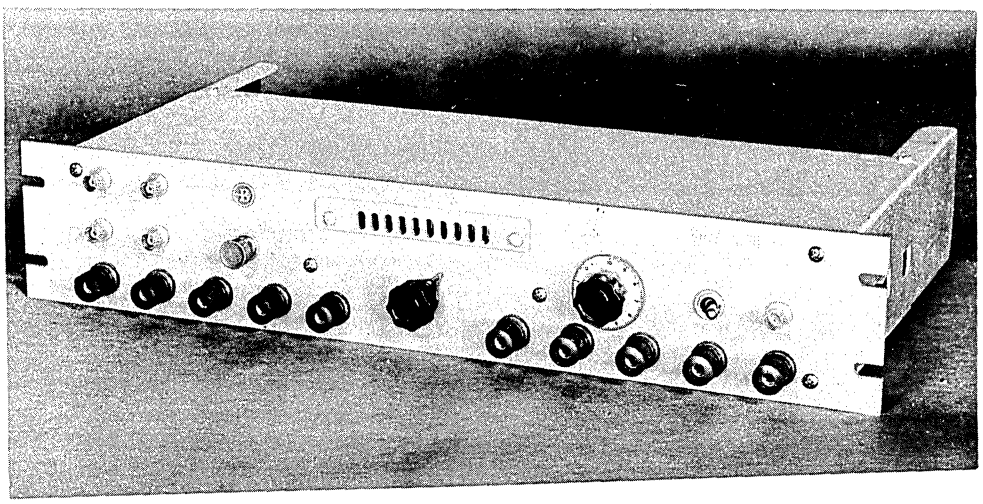
Power Requirements:
+250 v d.c. at 115 ma
+150 v d.c. at 6.4 ma
-150 v d.c. at 8.4 ma
6.3 v a.c. at 4.5 amp

References

Engineering Note:	E-281
Circuit Schematic:	D-33285
Photograph:	F-1301


D-33285-5
S1
INPUT SELECTOR
TO H.F.M.V.
TO L.F.M.V.
S2
DELAY INPUT SELECTOR
FROM H.F.M.V.
FROM L.F.M.V.
INPUT TO DIVIDERS
J1
C1 0.01 MFD
V1A 1/2 5687
R1 1.0 MEG
C2 0.01 MFD
R2 10.0 MEG
C3 0.01 MFD
R3 220Ω
R4 220Ω
R5 2200Ω 2W
HIGH FREQ. M.V.
R6 10,000Ω
R7 5000Ω 8W W-W ±5%
R8 47Ω
R9A 1.0 MEG
R9B 1.0 MEG
R10 220Ω 1W
R11 5000Ω 8W W-W ±5%
C4 10 MMFD
C5 100 MMFD
C6 100 MMFD
C7 10 MMFD
V3 5687
R12 47Ω
R13 10,000Ω
L1 250 μH
CR1
C8 0.01 MFD
LOW FREQ. M.V.
R14 10,000Ω
R15 47Ω
R16A 1.0 MEG
R16B 1.0 MEG
V4 2C51
R17 1000Ω 2W
R18 6800Ω 2W
R19 6800Ω 2W
C9 10 MMFD
C11 10 MMFD
C12 2 MMFD ±12.5%
C10 2 MMFD ±12.5%
C13 0.01 MFD
C14 0.01 MFD
R20 47Ω
R21 10,000Ω
R16B 1.0 MEG
L2 5000 μH
CR2
C15 20 MFD 250V
R22 220Ω
R23 270Ω
L3 25 μH
L4 50 μH
CR3
T1 1:1
C17 470 MMFD
V1B 1/2 5687
C18 0.01 MFD
R24 10,000Ω
R25 82,000Ω
V2 6AG7
STANDARD PULSE OUTPUT GAIN
R26 15,000Ω
R27 0.12 MEG
R28 220Ω
R29 500Ω
C19 0.01 MFD
T2 3:1
CR4 D-355
- ZERO + PULSE PULSE
J3
STANDARD PULSE OUTPUT
S4
DPDT SWITCH WITH NEUTRAL POSITION
FROM H.F.M.V.
S3
FROM DELAY M.V.
STANDARD PULSE SELECTOR
C16 18 MMFD ±20%
R47 220Ω 1W
R48 220Ω
CR5
R31 220Ω
SHIELD
6.3V
+250V
+150V
-150V
P1
JONES PLUG
R38 5000Ω 8W W-W ±5%
C24 180 MMFD
R42 5000Ω 8W W-W ±5%
C25 10 MMFD
R41 0.18 MEG
R43 47Ω
R45 27,000Ω 1W
R44 1.0 MEG
DELAY M.V.
INPUT FOR LOCK-IN DELAY
J4
J5
C20 0.01 MFD
V6A 1/2 5687
R30 2200Ω
C21 5 MMFD ±20%
R34 0.1 MEG
C22 0.01 MFD
R35 4700Ω
R32 1.0 MEG
R33 10.0 MEG
V5 5687
R39 47Ω
CR6
R40 0.18 MEG
L5 250 μH
CR7
C26 470 MMFD
R46 68,000Ω 1W
C27 0.01 MFD
R36 27,000Ω
C23 0.001 MFD
R37 0.12 MEG
C28 0.01 MFD
R51 3900Ω
C29 0.001 MFD
J6
OUTPUT PULSE (NEG., HIGH IMPEDANCE)
V6B 1/2 5687
R52 1000Ω
OUTPUT PULSE GAIN
R49 0.1 MEG
R50 0.27 MEG
NOTES: THE FOLLOWING SHALL APPLY TO ALL COMPONENTS ON THIS DRAWING UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE JAN SPEC., COMPOSITION TYPE, 1/2 W, ±10%.
2. CAPACITORS ARE JAN SPEC., MICA, ±10%.
3. VIDEO CONNECTORS ARE UG-290/U.
4. CRYSTAL RECTIFIERS ARE TYPE D-357.
DRAWING REFERENCES:
1. BLOCK SCHEMATIC: A-34631
2. PHENOLIC PANEL ASSEMBLY: C-33776
3. PHENOLIC PANEL DETAILS: C-33777
4. ALUMINUM PANEL ASSEMBLY: C-33778
5. ALUMINUM CHASSIS DETAILS: C-33779
6. ALUMINUM PANEL MARKING & COVER DETAIL: C-33780
7. PARTS LIST: PL-33776
SERVOMECHANISMS LABORATORY OF THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345
CIRCUIT SCHEMATIC, MULTIVIBRATOR FREQUENCY DIVIDER
SCALE: —
DR. A.M.G. 8-18-49
CK. TL 8/15/49
APP.
ENG. 8/19/49 RLB
D-33285-5
B-REDUCTION

Burroughs'
PULSE COUNTER TYPE 1750B



General Description

This unit is a pulse counter with a counting rate -- pushbutton to 500 KC. It has both a manual and electronic reset. Each count is represented visually by means of a neon indicator as well as electronically in the form of a DC signal. A pulse is generated at the count corresponding to the position of the scale switch (1-10). This pulse may be connected to the reset input clearing the counter every time it counts up to the scale number.

Specifications:

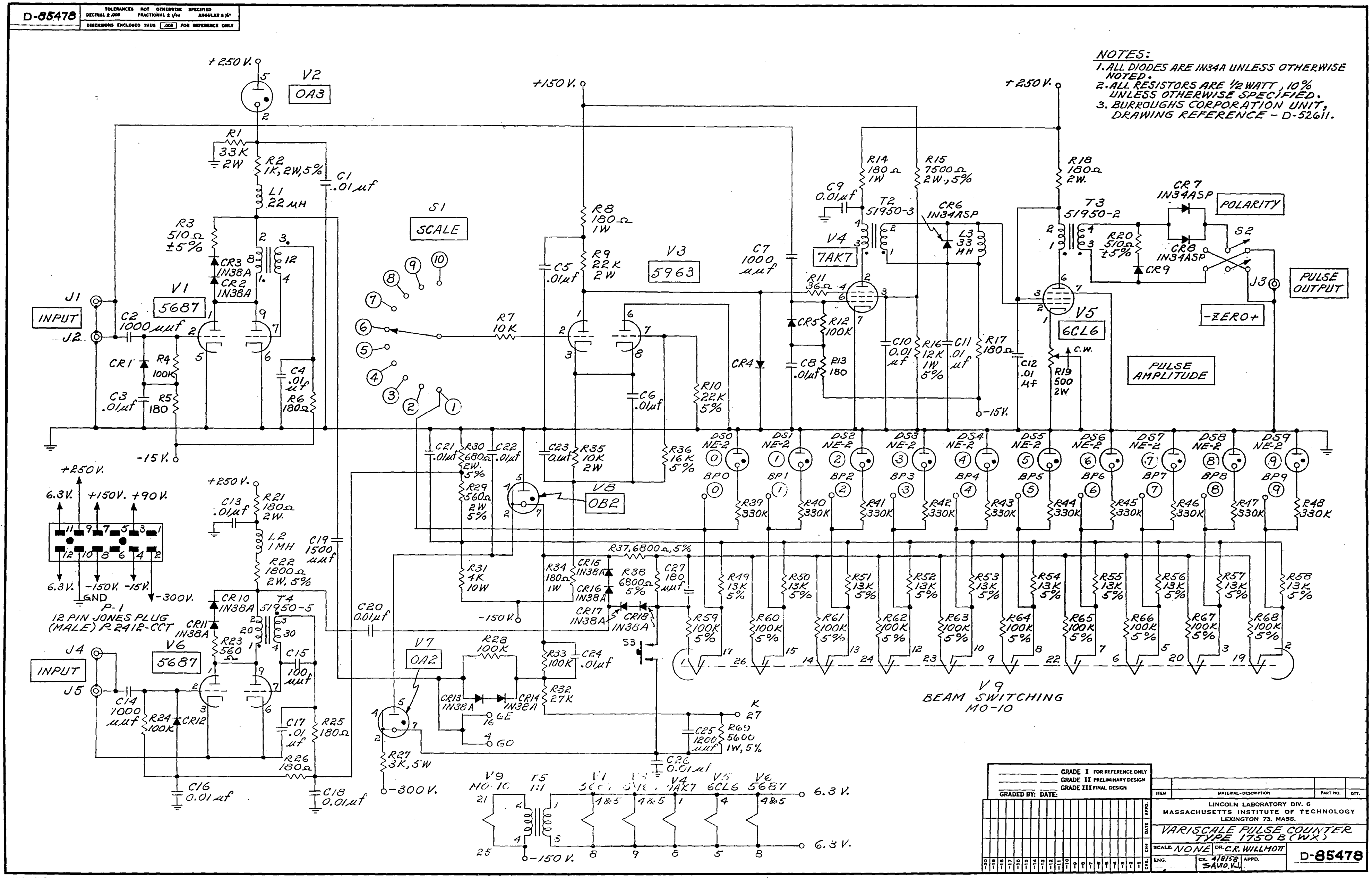
Dimensions: Panel 3 1/2 in. x 19 in., depth 10 in.

Inputs:
Count input 0.1 usec positive half sinewave 15-30 volts
Reset input 0.1 usec positive half sinewave 15-30 volts
Reset time: 10 usec

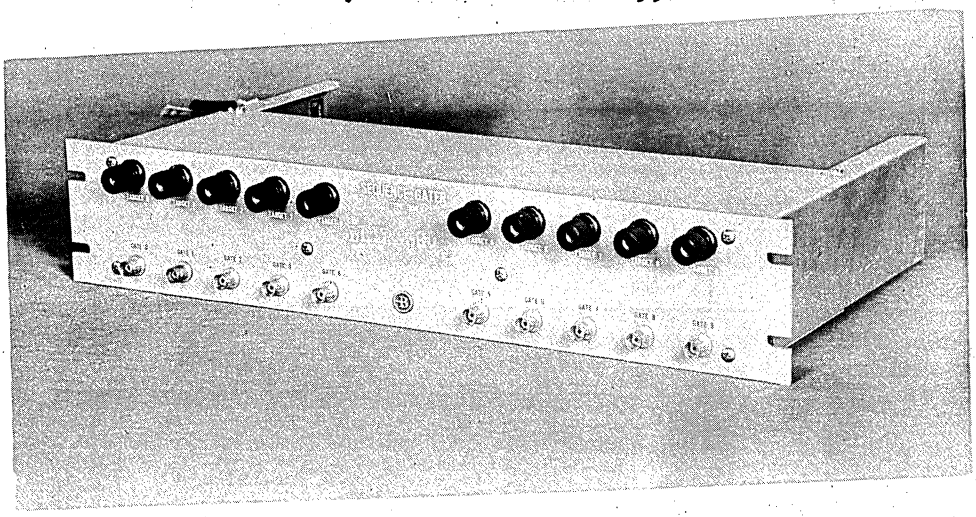
Outputs:
Pulse 0.1 usec half sinewave ±30 volts (adjustable)
D.C. -90 V from target on which beam is formed
-60 V from the other nine targets
Sequence gater can be used with this unit to convert stated values to standard Burroughs' level, zero or -15 volts.

Controls:
Manual reset pushbutton
Scale factor switch

Power:	+250 VDC	23 ma.
	+150 VDC	16 ma.
	-15 VDC	-6 ma.
	-150 VDC	39 ma.
	-300 VDC	14 ma.
	6.3 VAC	3.85 amps
Tube Complement:	2 5689	1 6700
	1 5963	1 0A2
	1 7AK7	1 0B2
	1 6CL6	1 0A3
References:	Circuit Schematic	D-85478


D-85478
TOLERANCES NOT OTHERWISE SPECIFIED
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY
NOTES:
1. ALL DIODES ARE IN34A UNLESS OTHERWISE NOTED.
2. ALL RESISTORS ARE 1/2 WATT, 10% UNLESS OTHERWISE SPECIFIED.
3. BURROUGHS CORPORATION UNIT, DRAWING REFERENCE - D-52611.
+250 V.
V2
OA3
+150 V.
V3
5963
V4
7AK7
V5
6CL6
V1
5687
V6
5687
V7
OA2
V8
OB2
S1
SCALE
INPUT
J1
J2
J3
J4
J5
POLARITY
S2
PULSE OUTPUT
-ZERO+
PULSE AMPLITUDE
V9
BEAM SWITCHING
MO-10
P-1
12 PIN JONES PLUG (MALE) P-2412-CCT
-15V.
-150 V.
-300 V.
6.3 V.
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:
ITEM
MATERIAL - DESCRIPTION
PART NO.
QTY.
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.
VARISCALE PULSE COUNTER
TYPE 1750 B (WX)
SCALE: NONE
DR. C.R. WILLMOTT
ENG.
CK. 4/8/58 SAVIO, V.J.
APPD.
D-85478

Burroughs'
SEQUENCE GATER TYPE 1950



General Description

This unit accepts DC levels from the target outputs of the Pulse Counter, Type 1750B, and converts them to the standard DC voltage used in the Burroughs Pulse control line (zero and -15 volts).

Specifications:

Dimensions: 5 1/2 in. x 19 in., depth 10 in.

Inputs:
- Frequency: Pushbutton to 500 KC
- DC levels
  - Gate on: -90 VDC
  - Gate off: -60 VDC
- Number of Inputs: 10

Outputs:
- Number of outputs: 10
- DC levels
  - Unloaded
    - Gate on: 0 volts (ground)
    - Gate off: -30 volts
  - Loaded with 1800 ohms and 100 mmf
    - Gate on: 0 volts (ground)
    - Gate off: -15 volts
- Transient response
  - Unloaded
    - Rise time 0.2 usec
    - Fall time 0.4 usec
  - Loaded with 1800 ohms and 100 mmf
    - Rise time 0.4 usec
    - Fall time 0.8 usec

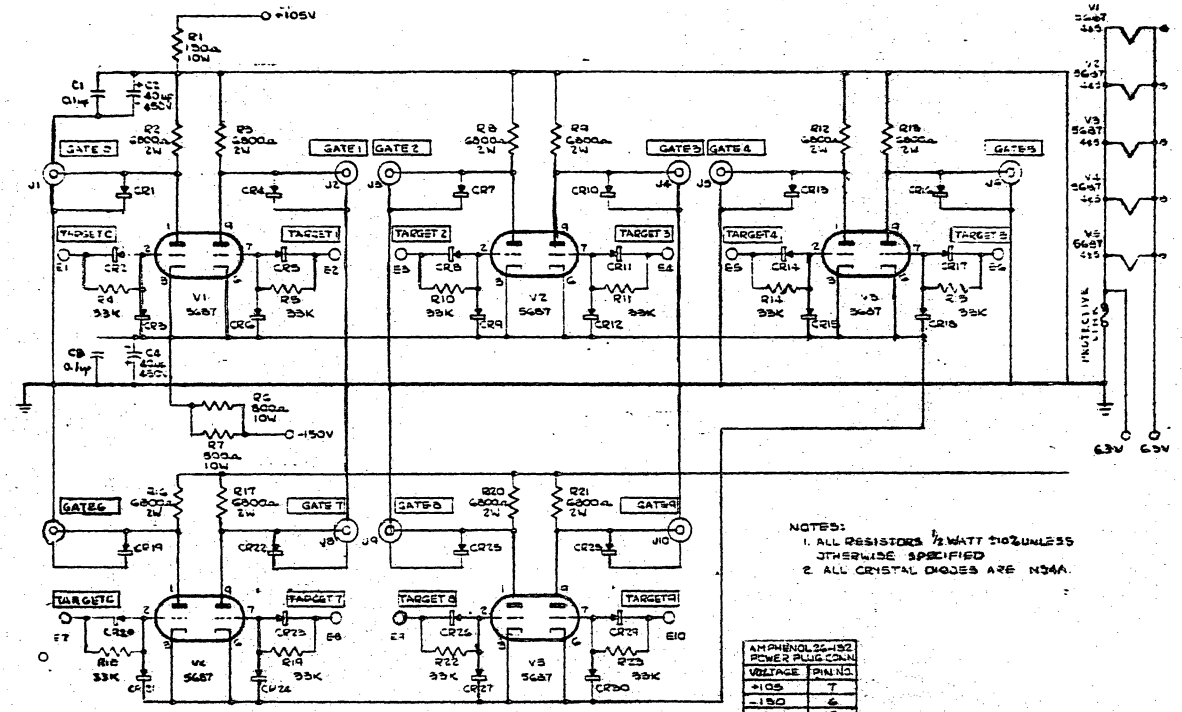
Circuit: 5 5687's used as voltage amplifiers

Power Consumption: -150 VDC 160 ma

References: Circuit Schematic B-80501

B-80501

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY



NOTES:
1. ALL RESISTORS ½ WATT ±10% UNLESS OTHERWISE SPECIFIED
2. ALL CRYSTAL DIODES ARE N34A.

AMPHENOL 26-132 POWER PLUG CONN.	
VOLTAGE	PIN NO.
+105	7
-150	6
63	13
63 & GND	15
GND	14

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
-13			
-12			
-11			
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2			
-1			

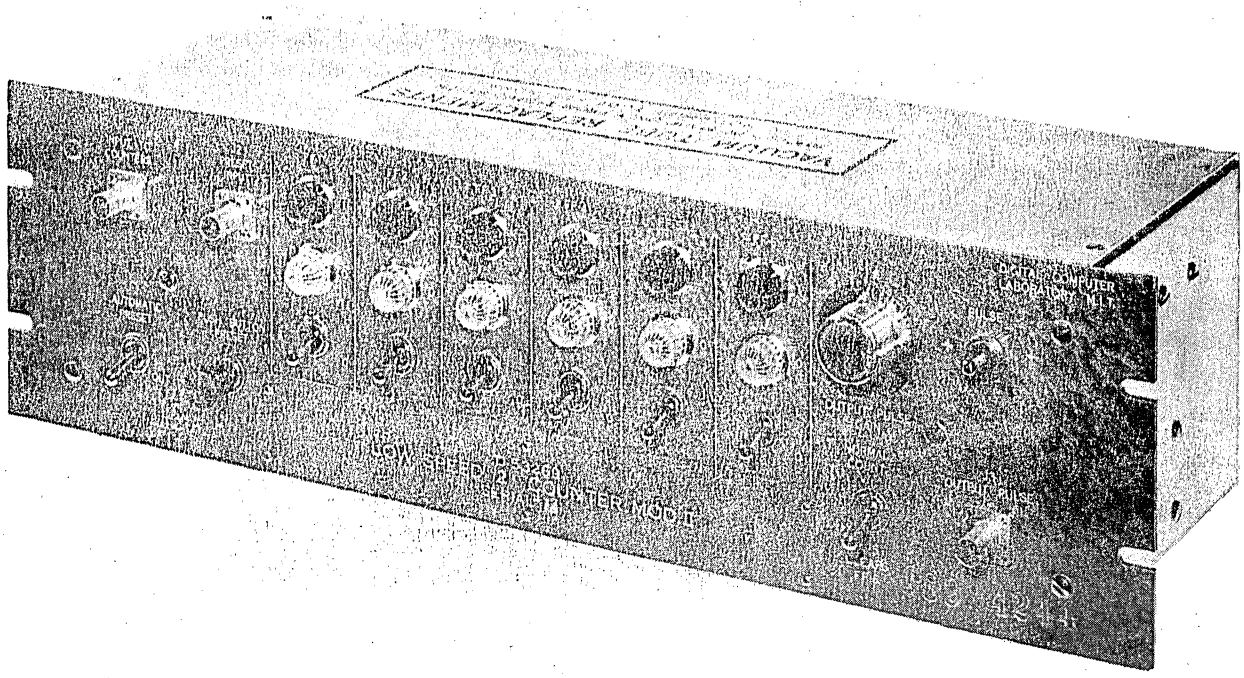
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC, SEQUENCE GATER TYPE 1950A
(C-51993 BURROUGHS CORPORATION)

SCALE ~ DR. JOAN S. ALLEN 1-31-58
ENG. CK. APPD.

B-80501

LOW-SPEED 2^6 Counter, Mod. II



General Description

The low-speed 2^6 counter, Mod. II, is a compact, flexible device with a counting rate of 200 kilocycles and below. This unit, like the Mod. I described in this Section, uses 6 plug-in binary scalers which may be preset to produce an end carry after any desired count up to 64. A single-pulse output for each preset input pulse may be obtained after any given count by switching in a special circuit between the fifth and sixth plug-in units: if the sixth unit is preset to a 1, the carry from the fifth unit will clear the sixth and produce a single pulse. Any carry thereafter from the fifth unit will keep the sixth unit cleared, producing no further outputs until the unit is again preset.

Specifications

Dimensions: Panel, 5-1/2 x 19 inches
Depth 9 inches

Circuits: 2C51 trigger circuit
2C51 preset circuit
6 - GE 4SN1A3 binary scalers (plug-in)
2C51 output-pulse generator
6AN5 buffer amplifier
12 neon bulb flip-flop indicators

Input: To counters and preset:

Random 0.1-μsec half-sine wave pulse
Minimum pulse amplitude, +12 volts
Maximum prf, 200 kilocycles

Output: 0.1-μsec half-sine wave pulse, variable, polarity reversible.

Delay through unit:

3.9 μsec with all flip-flops preset to 1.

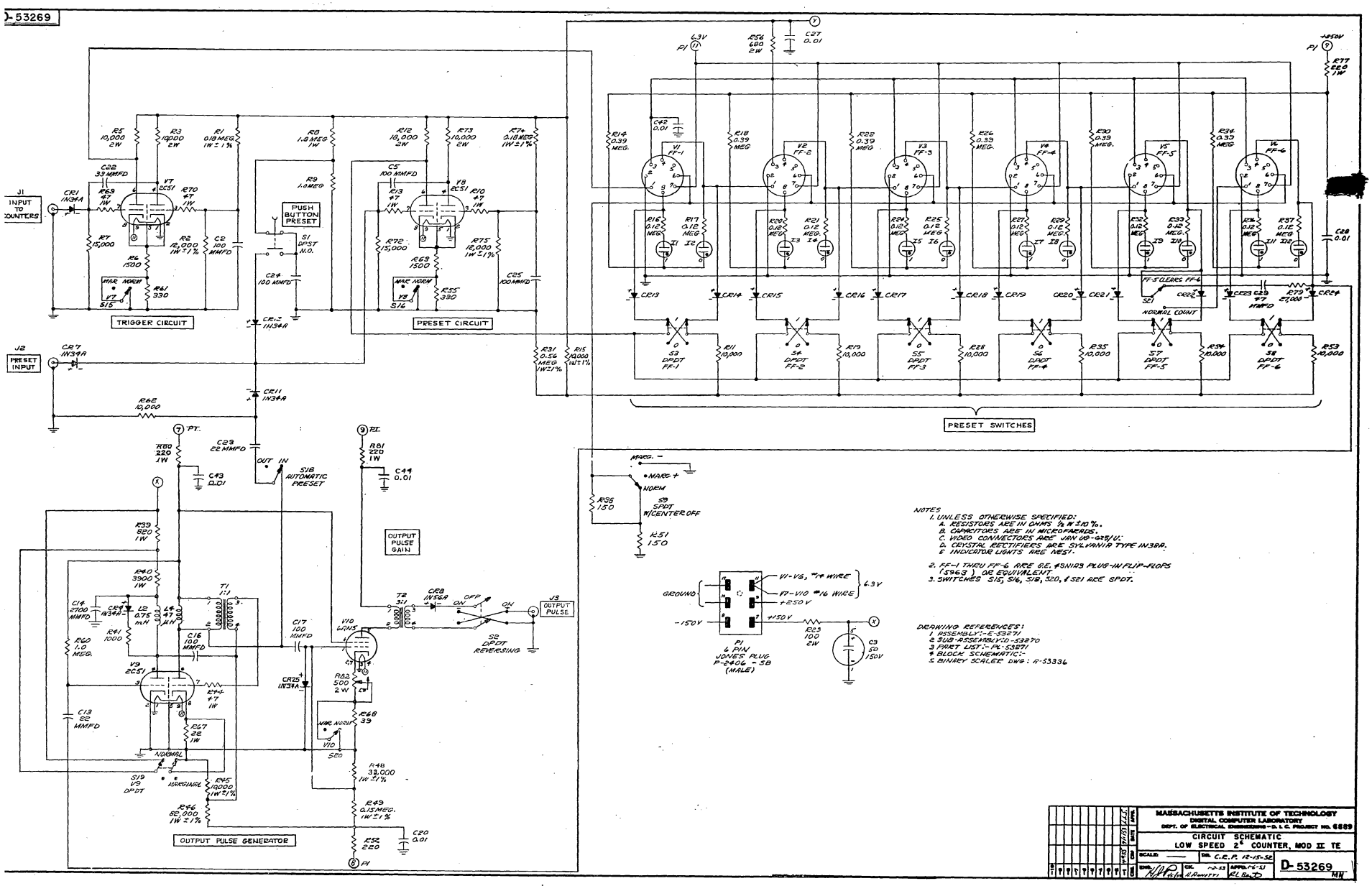
Power Requirements:

+250 volts DC	2 ma
+150 volts DC	70 ma
-150 volts DC	3 ma
6.3 volts AC	4.05 amp

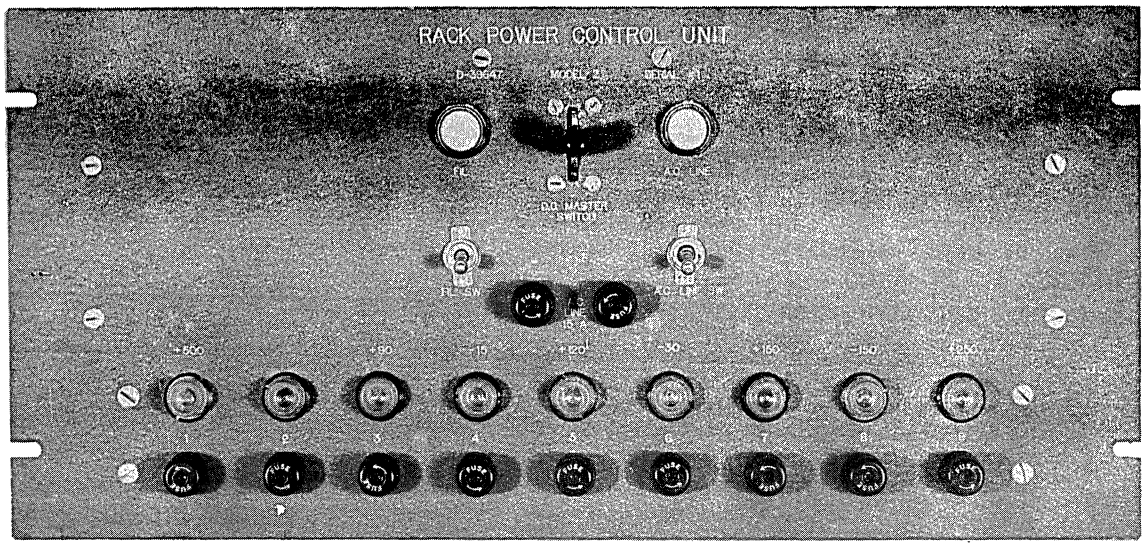
References

Circuit Schematics D-53269
A-53336 (Plug-in Unit)

Engineering Note E-521


D-53269
J1 INPUT TO COUNTERS
J2 PRESET INPUT
TRIGGER CIRCUIT
PRESET CIRCUIT
PUSH BUTTON PRESET
PRESET SWITCHES
OUTPUT PULSE GAIN
OUTPUT PULSE GENERATOR
AUTOMATIC PRESET
OUTPUT PULSE
P1 6 PIN JONES PLUG P-2606 - SB (MALE)
NOTES
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS ½ W ±10 %.
B. CAPACITORS ARE IN MICROFARADS.
C. VIDEO CONNECTORS ARE JAN UG-625/U.
D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N38A.
E. INDICATOR LIGHTS ARE NE51.
2. FF-1 THRU FF-6 ARE G.E. #5N1103 PLUG-IN FLIP-FLOPS (5963) OR EQUIVALENT.
3. SWITCHES S15, S16, S18, S20, & S21 ARE SPDT.
DRAWING REFERENCES:
1. ASSEMBLY:- E-53271
2. SUB-ASSEMBLY:D-53270
3. PARTS LIST:- PK-53271
4. BLOCK SCHEMATIC:-
5. BINARY SCALER DWG: A-53336
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING - D. L. C. PROJECT NO. 6869
CIRCUIT SCHEMATIC
LOW SPEED 2⁶ COUNTER, MOD II TE
SCALE: —
DR. C.E.P. 12-15-52
CK. 1-2-53
APPD. 1-2-53
D-53269 MN

RACK POWER CONTROL UNIT
(Model 2)



General Description

This unit provides 6.3 v a-c and a convenient means for switching all d-c power from the central supply to equipment mounted on a standard 19-inch relay rack. When fused properly, it prevents local short circuits or overloads from tripping the main circuit breakers, thereby allowing other racks to continue drawing power. In addition, the equipment has a time-delay relay which acts as a current-surge suppressor by shorting out series resistors in the +250 and +150 lines.

Specifications

Dimensions: 8 3/4 x 10 x 19 inches.

Input (rear chassis): D-C input from bench power box through a 12-pin male Jones plug.
115-v, 60-cycle input through a flush motor plug.

Output (rear chassis): Standard d-c voltages (central power supply) to 4 female 12-pin Jones plugs.
6.3 v a-c (40 amp) from 2 filament transformers (primaries tapped). Output from one through the 4 Jones plugs; output from the second (with center taps) brought out to 2 terminal strips.
4 115-v a-c outlets on top rear of chassis.

Auxiliary Power: Filament Power Panel (Sect. 2) may be plugged into the 115-v a-c outlet marked "AUX. FIL" if additional filament power is needed.
+500 v may be fed into the unit through the Jones-plug input or a uhf coaxial jack (J2).

Maximum Loads: 2 amp for d-c voltages
15 amp for 115 v a-c
80 amp for 6.3 v a-c
(80 amp additional with Fil. Power Panel)

Fusing (front panel):

(1) D-C Voltages - 3AG fuses up to 2 amp.
(2) 115v a-c - 4AG fuses, 15 amp, on both sides of line.

Controls (front panel):

(1) Multi-contact D-C MASTER SWITCH.
(2) Toggle Switch for a-c input, A-C LINE.
(3) FIL. SWITCH, toggle switch controlling primary power to both fil. transformers and to 115-v a-c outlet, AUX. FIL.
(4) Current-surge suppressor. Time-delay relay, energized by d-c master switch, cuts out series resistors in +250 and +150 lines. Optimum delay - 8 seconds.

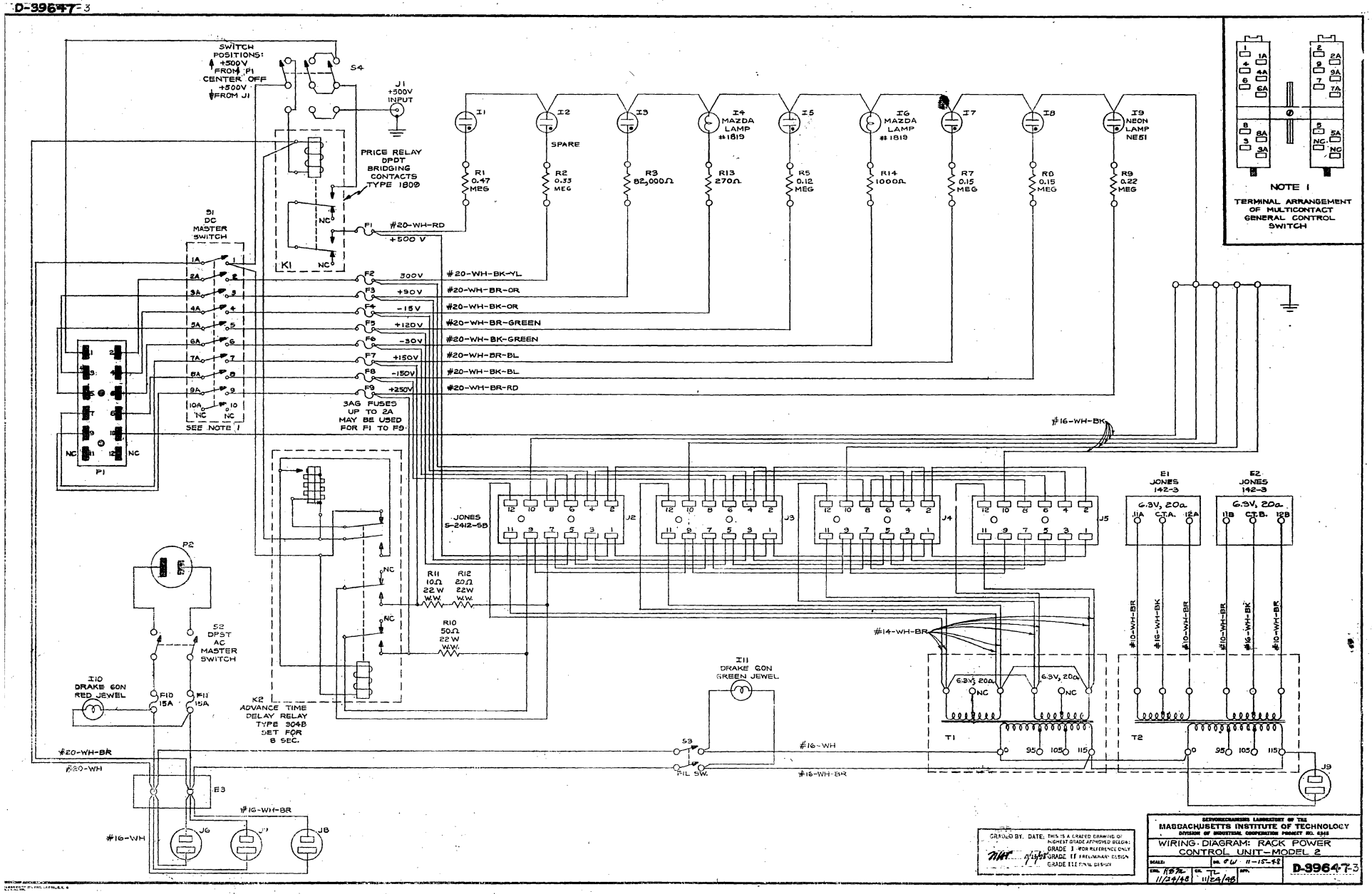
Indicators (front panel):

A-C line - Drake 60N Red Jewel
Fil. - Drake 60N Green Jewel
D-C (all) - NE51 neon lamps except -15 v, -30 v which use incandescent lamps.

References

Engineering Note	E-118
Circuit Schematic	D-39647

D-39647-3



GRADED BY: DATE: THIS IS A CRAFTED DRAWING OF HIGHEST GRADE APPROVED BELOW:
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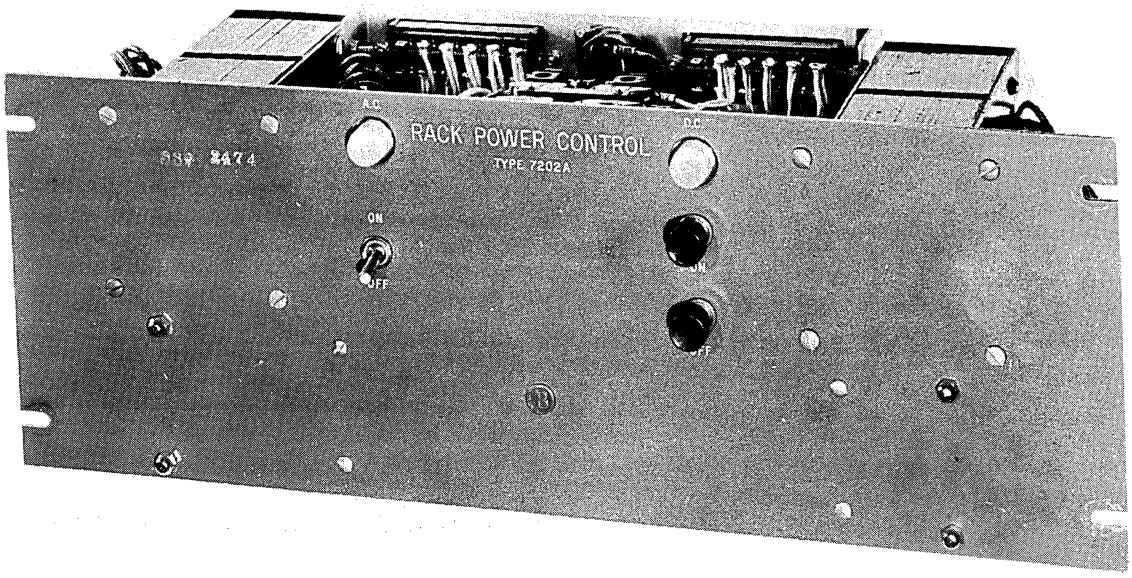
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

WIRING DIAGRAM: RACK POWER CONTROL UNIT—MODEL 2

SCALE: | DR. GV 11-15-48 | CH. TL 11/29/48 | APP. | D-39647-3

Burroughs'
RACK POWER CONTROL
(Type 7202 AW, Models I & II)



General Description

The Rack Power Control is the switch and fuse box for a rack of test equipment; it also is a 50-amp, 6.3-v filament supply. A toggle switch connects the a-c input and permits the ON push button to control the d-c voltages. In Model I, the ON button immediately connects the d-c voltages. In Model II, the ON button immediately connects all the d-c voltages except +150 volts and +250 volts where it leaves series resistors for a period of approximately 8 seconds. In either Model I or Model II, failure of any fuse disconnects all the d-c voltages.

Specifications

Dimensions: 7 x 19 inches, depth 9 inches

Input (at rear of chassis): apply Laboratory d-c power supply to 12-pin, male Jones plug and 115-v, 60-cycle AC to male line plug.

Output (at rear of chassis): the lower, 12-pin Jones plug is in parallel with input. The two upper, 12-pin Jones plugs provide standard d-c voltages from the Rack Power Control. The female, a-c line plug is in parallel with male line plug. Transformer terminals furnish four 12.5-amp filament supplies, the voltage of which may be changed by moving the input connection among the eight taps on each transformer.

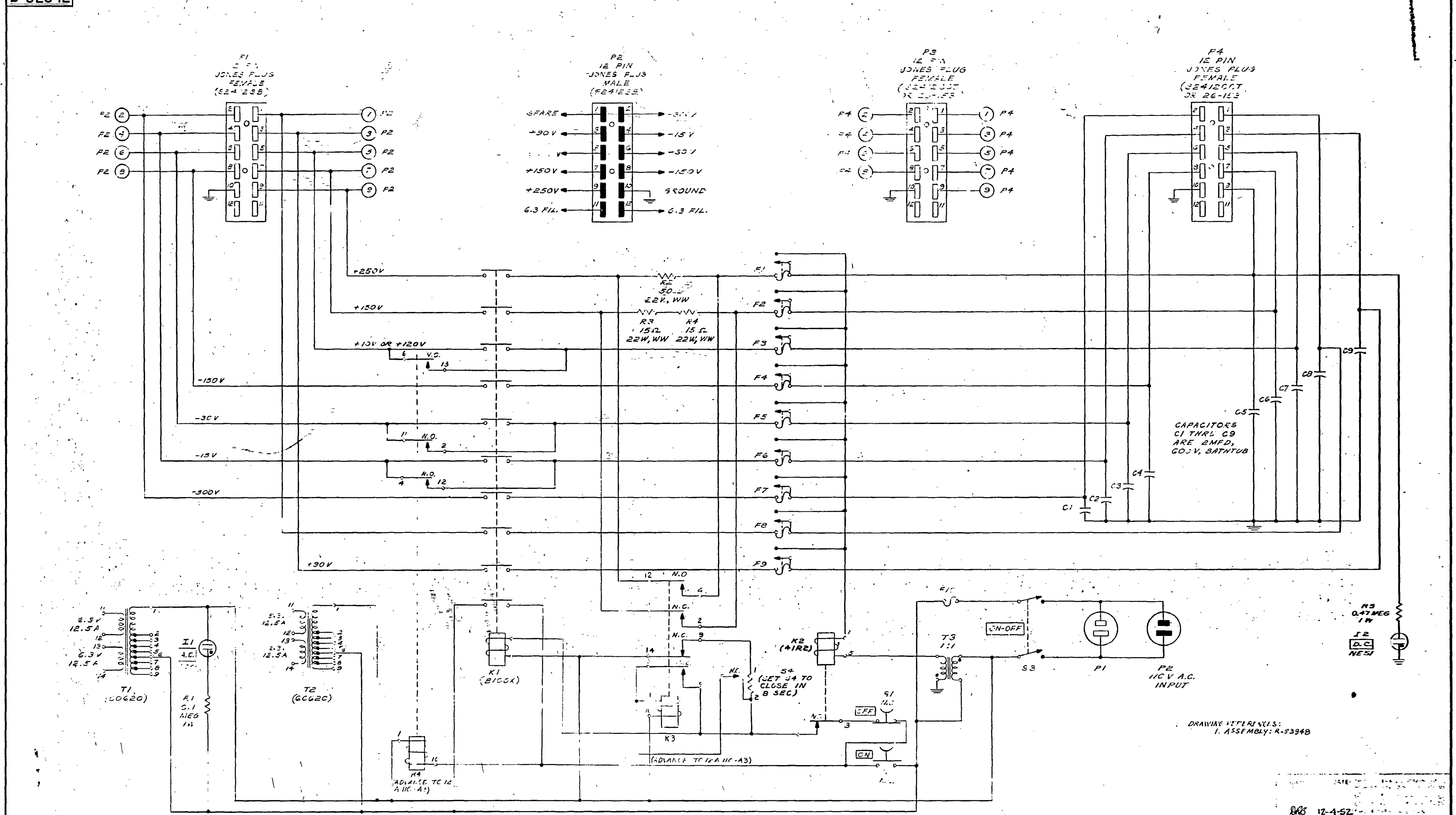
Maximum Loads: 2 amp for d-c voltages
5 amp for 115-v AC
50 amp for 6.3-v AC

Fuses: d-c voltages -- Grasshopper 2 amp
115-v AC -- Fusetron FNM 5

Reference

Circuit Schematic D-52642 (Model II)
D-55393 (Model I)

D-52642



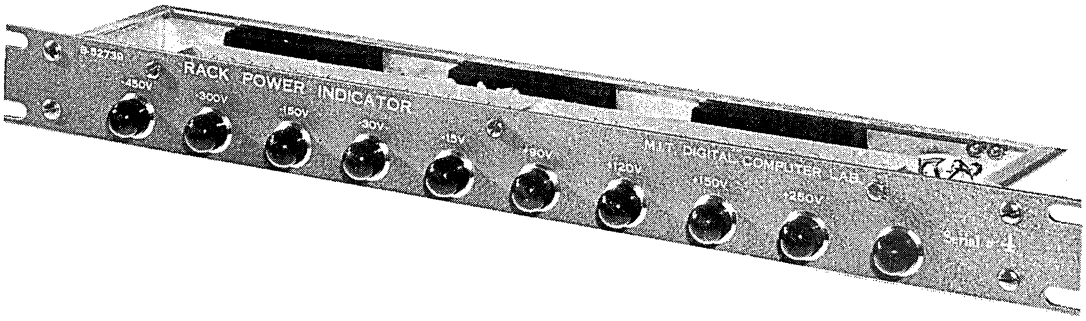
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING—D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC,
RACK POWER CONTROL, TYPE 7202AW, MODEL II

SCALE: ——— DR. brm 9-30-52

D-52642

RACK POWER-INDICATOR PANEL



General Description

This unit is an indicator of Laboratory voltages. When connected to the output of a Burroughs Rack Power Control or to the rack power strip, the panel indicates by the glow of its lamps which power-supply lines are continuous from the source. Each of the nine labelled indicator lamps is connected between a d-c voltage and ground. A tenth lamp is connected to a two-terminal Jones strip where another voltage may be applied.

Specifications

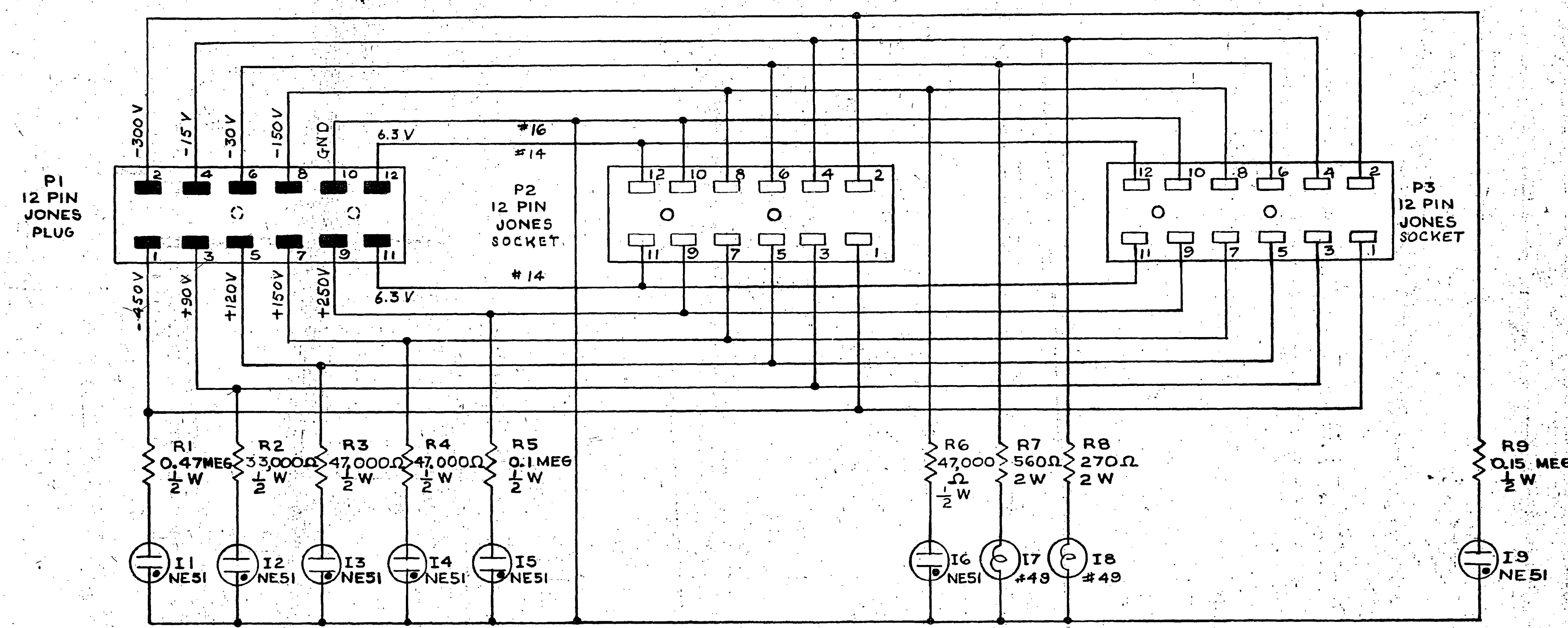
Dimensions: 1-3/4 x 19 inches, depth 4 inches

Lamps: NE 51 across all d-c voltages except -15 and -30
No 49 across -15 and -30 volts

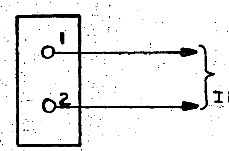
References

Circuit Schematic B-52739

B-52739



NOTE:
UNLESS OTHERWISE SPECIFIED
WIRE SIZE SHALL BE #20.



E1
2 TERMINAL
JONES STRIP
140-2

DRAWING REFERENCES:
1. ASSEMBLY: D-52767
2. PARTS LIST: PL-52767

DRAWN BY | DATE — THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
DRC 10-23-52 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
1	4102	10/30/52	[illegible]
2	4631	1-29-53	[illegible]

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DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

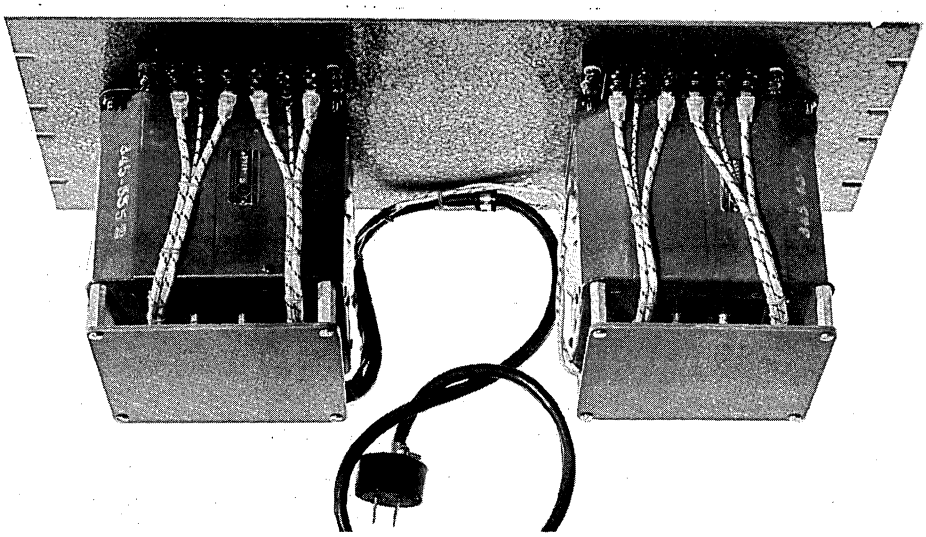
CIRCUIT SCHEMATIC
RACK POWER INDICATOR PANEL

SCALE:
DR. CS 10-9-52
ENG. 10-14-52 RBP
CK. 10-14-52 R. B. [illegible]
APPD. [illegible] 10/21/52

B-52739

K+E ALBANENE TRACING PAPER

FILAMENT POWER PANEL
(Models 1, 2, & 3)



General Description

This unit is used to supply auxiliary filament power when the amount from the rack power-control unit is inadequate for test setups. It consists of two 40-amp filament transformers mounted on the rear of a panel. Models 1 and 2 have no indicator lamp, fuse, or switch. Model 1 has eight center-tapped secondaries; Model 2 has four center-tapped secondaries. Model 3 has indicator lamp, fuse, and switch and four center-tapped secondaries. On the primaries of models 2 and 3 are taps for input voltages of either 95, 105, or 115 volts.

Specifications

Construction: Panel for rack mounting.

Dimensions: 8-3/4 x 19 inches.

Transformers: Two 40-amp, 6.3-v a-c filament transformers. Each transformer of Model 1 has four center-tapped 10-amp secondaries; those of models 2 and 3 have two center-tapped 20-amp secondaries.

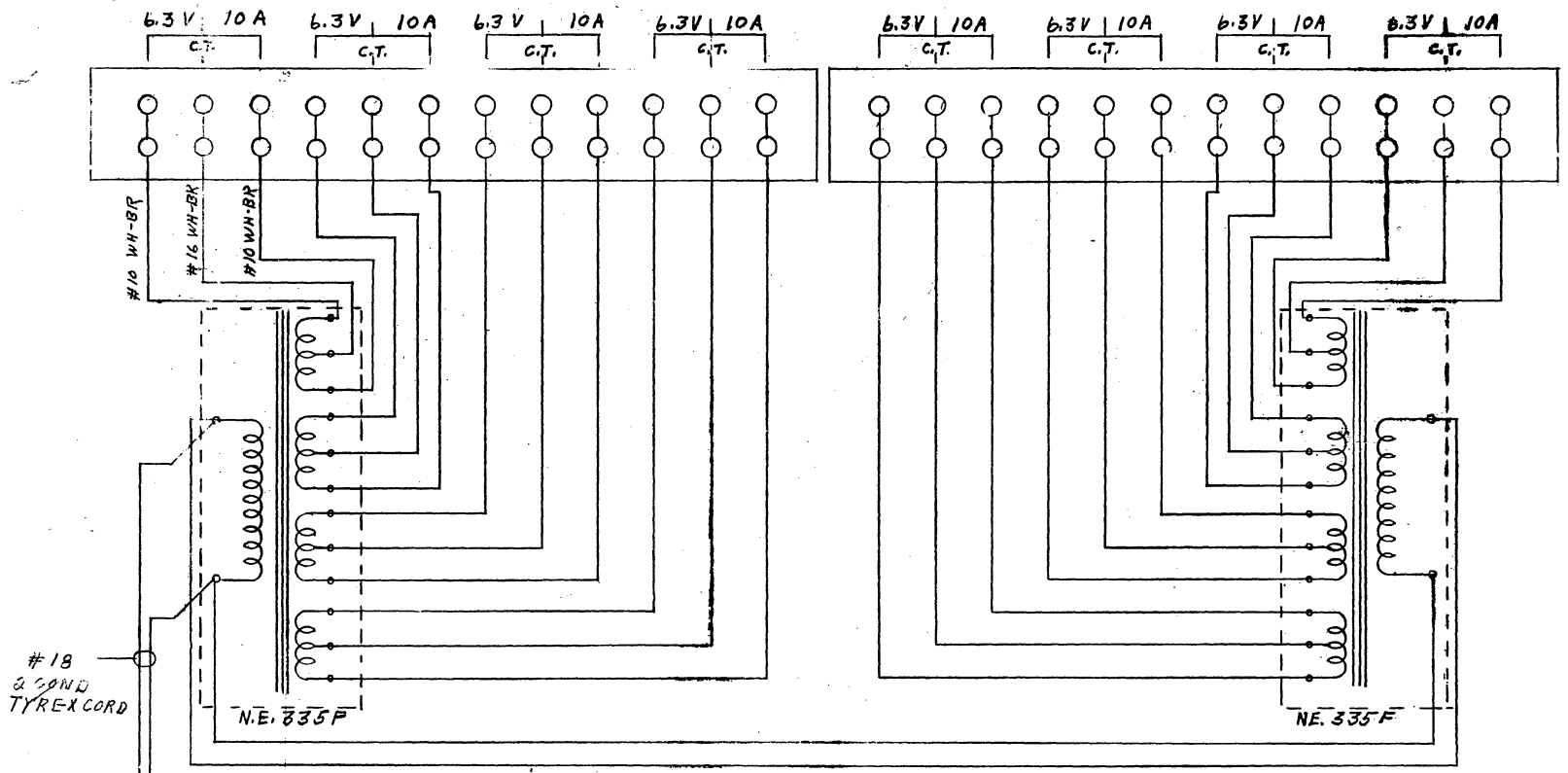
Input: 115-v AC primary power from AUX. FIL. outlet on rack power-control unit, controlled by filament switch.

Output: Secondaries with center taps brought to Jones terminal strips on rear of panel. May be used in parallel to obtain more than 20 amp on one line.

References

Circuit Schematic B-38759 (Model 1)
B-40127 (Model 2)
Engineering Note E-117 (Model 1)

SB-39759



HUBBEL. LUG
#9753

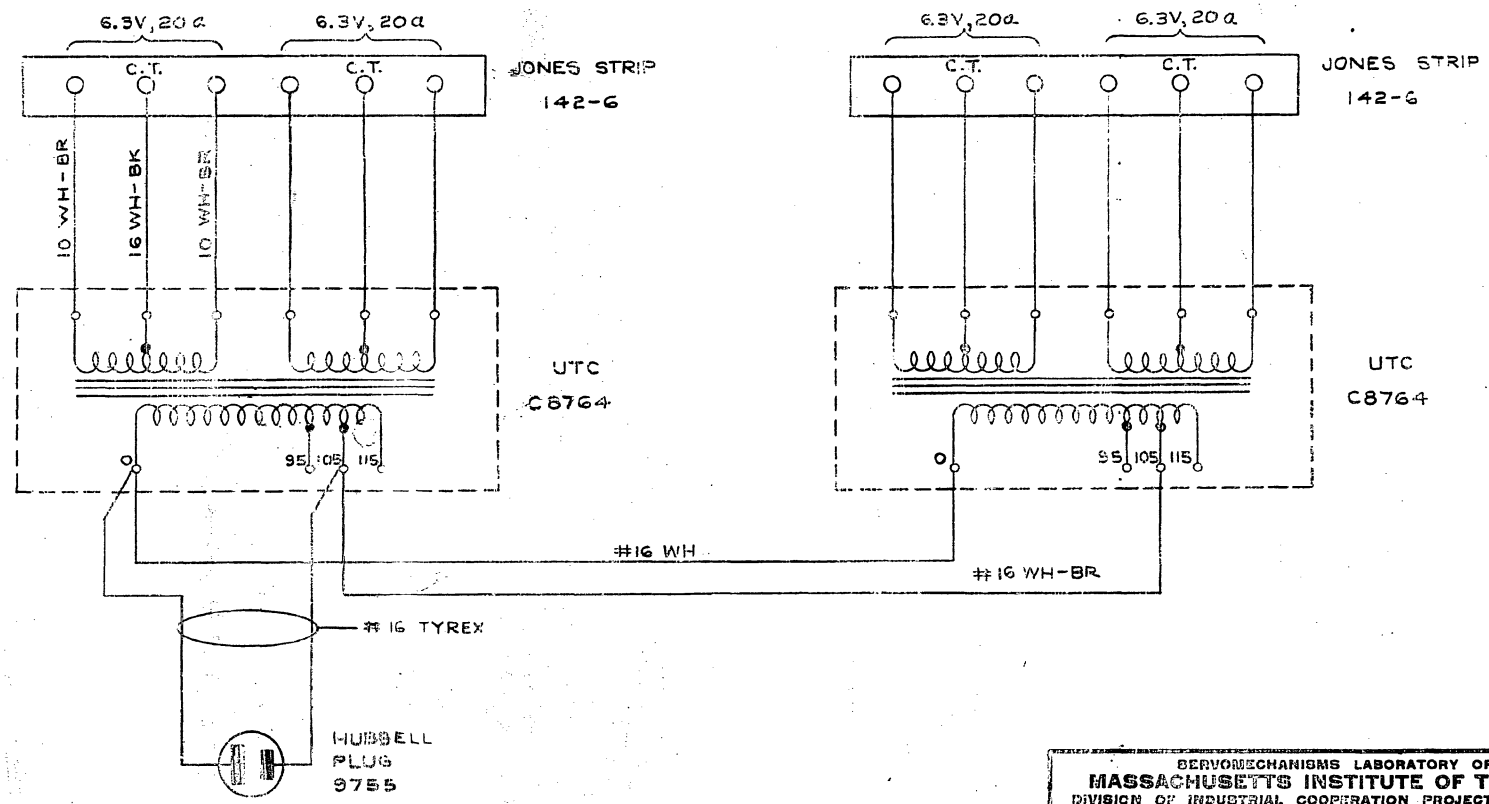
115 V 60~
INPUT

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

FILAMENT POWER PANEL

SCALE: ~	DR. RHM 4/26/48	SB-39759
ENG. RHM	CK.	APP.

B-40127-1



SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

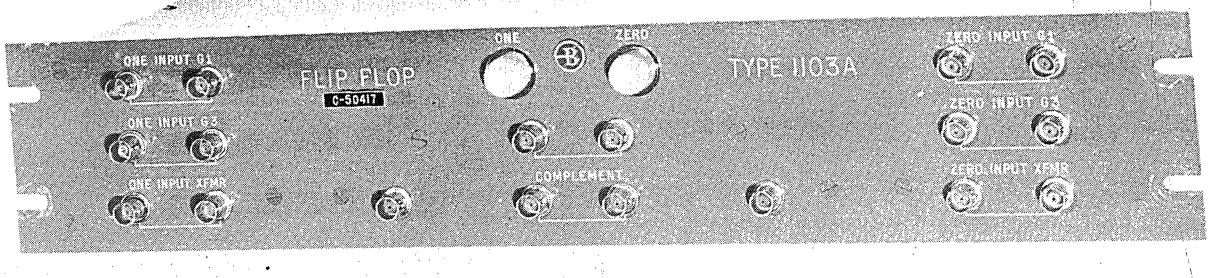
CIRCUIT SCHEMATIC,
FILAMENT-POWER PANEL, MODEL 2

SCALE:	DR. M.M. 9-23-48	B-40127-1
ENG. R.H.M. 9/28/48	CK. TL 9/28/48	APP.

"ALBANENE" NO. 1001. H&G CO. N. Y. U.S.A.
PAT. U.S.A. PAT. OFF.

9L

Burroughs' FLIP-FLOP (Type 1103 A or AW)



General Description

This unit uses the same 7AD7 flip-flop, d-c coupled to its load, that is used in the D-C In-Out Register in Whirlwind. The two stable states of the flip-flop are 0 and -15 volts. The equipment is meant to drive gate tube panels, crystal gate panels, and similar loads up to 100 mmf with 1/4-μsec rise time

"ONE" and "ZERO" inputs may pass through an input transformer or through a gate tube. In order that a pulse pass either of the Read-In gate tubes their G3 input must be zero or positive. If a terminator is put in this jack the gate will always be open; if it is 15 or more volts negative it will be closed. There is also a complement-input that has a 0.05-μsec delay included so that the flip-flop may be used for counting. It will operate up to 4 megacycles, and will resolve pulses 0.25 μsec apart. Two indicator lights show the position of the flip-flop.

Specifications

Construction:	Panel and chassis
Dimensions:	3-1/2 x 19 inches Depth 10 inches

Circuit: 2 - 7AD7's FF
7AK7 "Zero" input trigger
7AK7 "ONE" input trigger
7AD7 Complement trigger

Input: ONE AND ZERO INPUTS

Read-In Gate Tubes: (G3) to No. 3 grids of gate tubes. 0 or positive voltage for gate to be open; 15 or more volts negative for gate to be closed.
(G1) to No. 1 grids of gate tubes. Positive, 0.1-μsec pulse of at least 15 volts.

Direct to FF: (XFMR) through transformer to one side of FF. Positive, 0.1-μsec pulse of at least 15 volts

COMPLEMENT INPUT

To trigger tube. Positive 0.1-μsec pulse of at least 15 volts delayed 0.05 μsec.

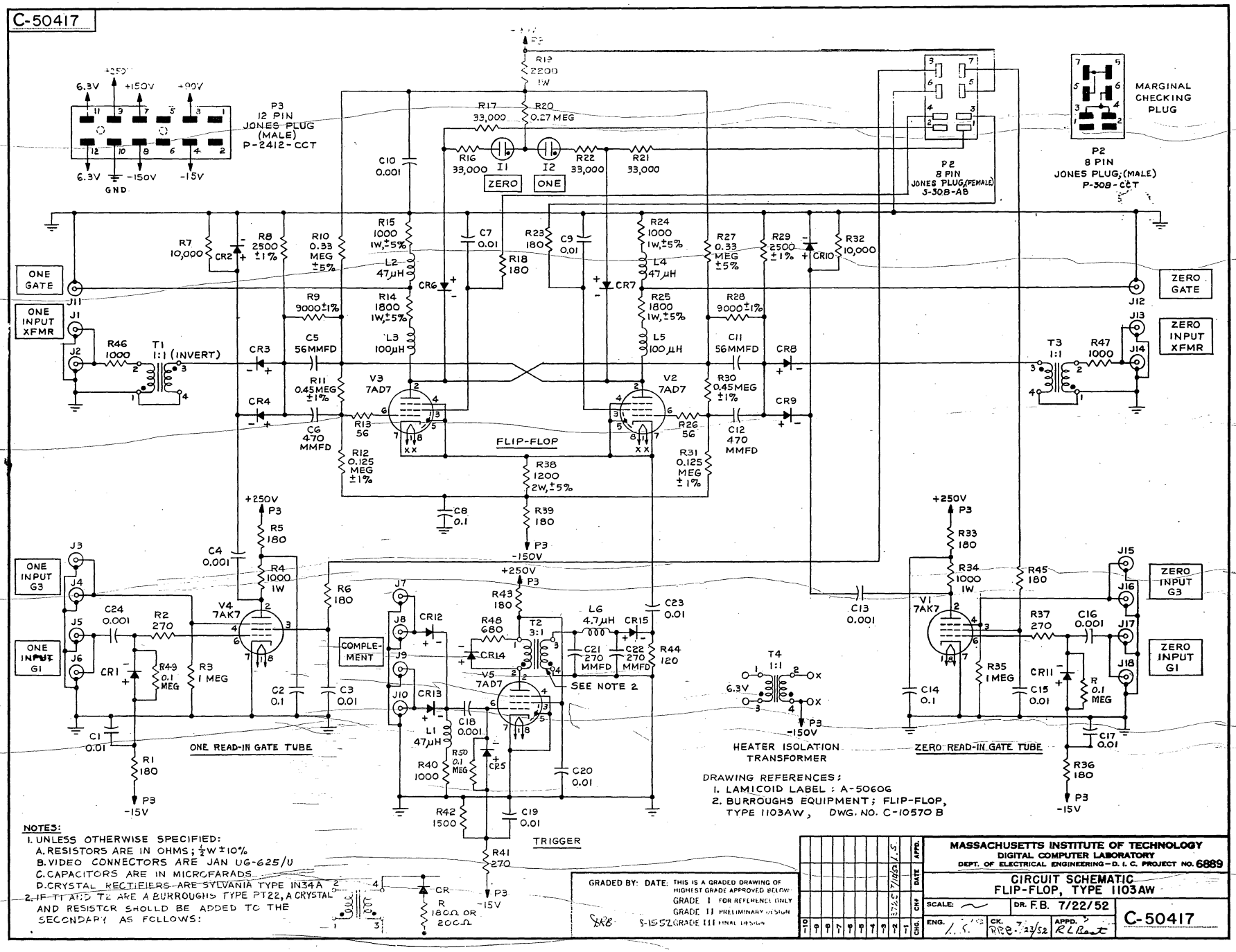
Output: 0 or -15 volts depending on position of FF; interval impedance is 1000 ohms, and should not be loaded by more than 100 mmf capacitance.

Power Requirements:

+250 volts d-c	10 ma
+ 90 volts d-c	3 ma
- 15 volts d-c	10 ma
-150 volts d-c	30 ma
6.3 volts a-c	3.4 amps

References

Circuit Schematic	C-50417
Engineering Note	E-434
Photograph	P-1554



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; ½W ±10%
   B. VIDEO CONNECTORS ARE JAN UG-625/U
   C. CAPACITORS ARE IN MICROFARADS
   D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
2. IF T1 AND T2 ARE A BURROUGHS TYPE PT22, A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:

DRAWING REFERENCES:
1. LAMICOID LABEL : A-50606
2. BURROUGHS EQUIPMENT; FLIP-FLOP, TYPE 1103AW, DWG. NO. C-10570 B

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW
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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
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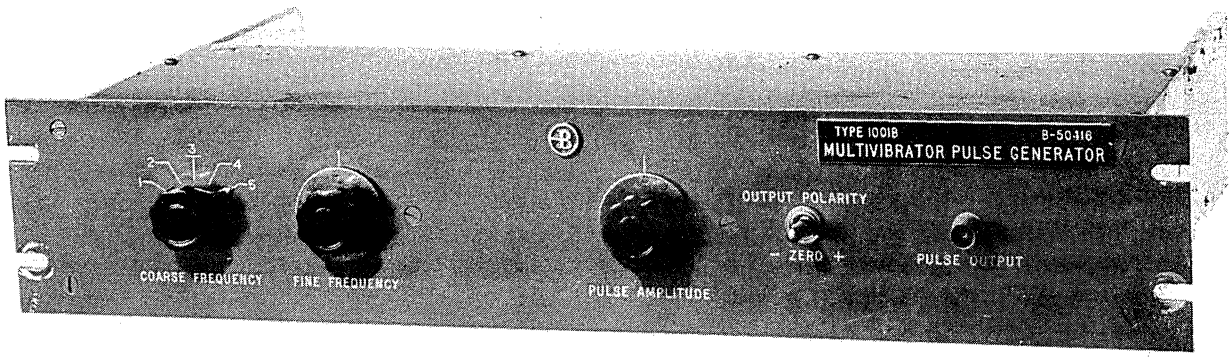
CIRCUIT SCHEMATIC
FLIP-FLOP, TYPE 1103AW

SCALE: DR. F.B. 7/22/52
ENG. CK. RRB 7/23/52 APPD. RLBest

C-50417

Burroughs'
MULTIVIBRATOR PULSE GENERATOR
(Type 1001 B or BW)



General Description

This unit generates either positive or negative 0.1-μsec pulses at frequencies continuously variable from 15 to 650,000 cycles per second, in five overlapping bands.

A symmetrical multivibrator is used to control the frequency, but there is no provision for synchronizing it with an external higher-frequency signal.

Specifications

Construction: Panel and chassis

Dimensions: 3-1/2 x 19 inches
Depth 10 inches

Circuit: 5687 Multivibrator
5687 Pulse Standardizer
6AG7 Buffer Amplifier

Output: The pulse output jack provides standard 0.1-μsec half-sine-wave pulses of reversible polarity at amplitudes from 10 to 32 volts not affected by changes in frequency.

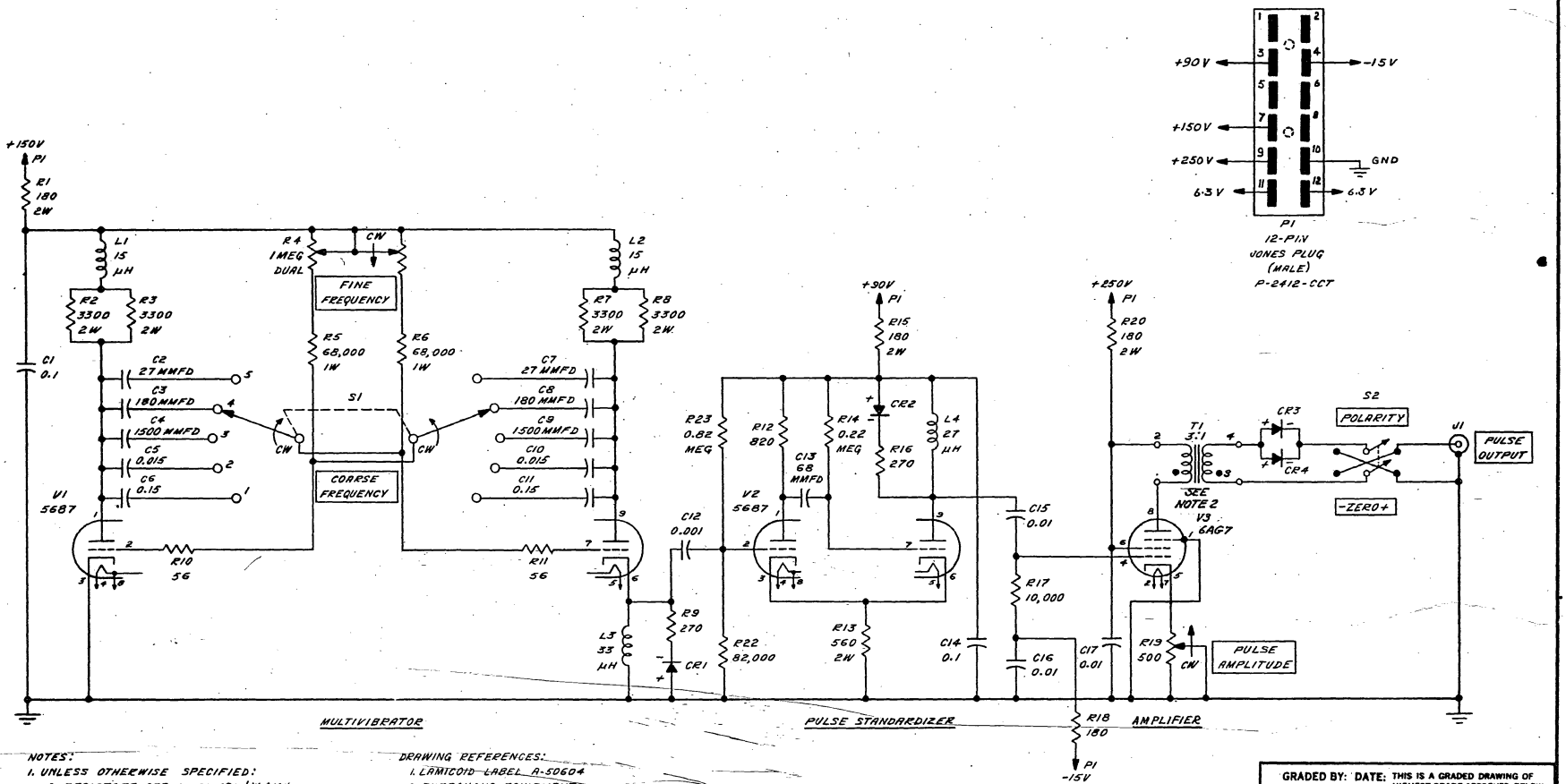
Power Requirements:

+250 volts d-c	8 ma
+150 volts d-c	57 ma
+90 volts d-c	40 ma
15 volts d-c	1 ma
6.3 volts a-c	2.5 amp

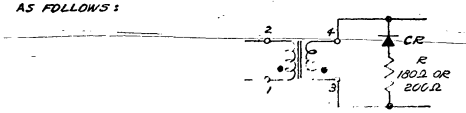
References

Circuit Schematic	C-50416
Engineering Note	E-434
Photograph	F-1552

C-50416



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; ½W, ±10%
   B. CAPACITORS ARE IN MICROFARADS
   C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
   D. VIDEO CONNECTORS ARE JAN UG-625/U
2. IF T1 IS A BURROUGHS TYPE PT22, A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:



DRAWING REFERENCES:
1. LAMICOID LABEL A-50604
2. BURROUGHS EQUIPMENT; PULSE GENERATOR, TYPE 1001BW DWG # B-10565B

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GRADE III FINAL DESIGN
RCB 5-15-52

NO.	DATE	CHK.	APPD.
3124	7-1-52		

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DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

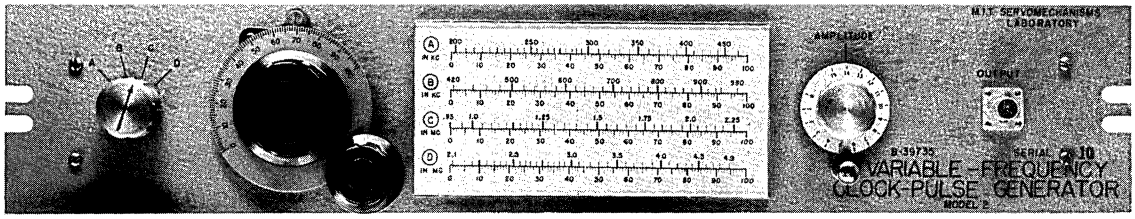
CIRCUIT SCHEMATIC,
MULTIVIBRATOR PULSE GENERATOR, TYPE 1001BW

SCALE: —— DR. A. S. 7-1-52

ENG. R.L.S. CK. APPD. R.L.B.-C.

C-50416

VARIABLE-FREQUENCY CLOCK-PULSE GENERATOR
(Model 2)



General Description

This unit is a primary pulse source for test setups of gate tubes, flip-flops, matrices, bus drivers, control-line drivers, and other components. It is also a basic building block for complete systems and special tests, providing standard output pulses 0.1 microsecond long at a 93-ohm impedance level with frequencies variable from 0.2 to 4.9 megacycles.

Specifications

Construction: Panel and chassis for standard rack mounting.

Dimensions: $3\frac{1}{2}$ x $5\frac{1}{2}$ x 19 inches.

Circuits: 6SN7 cathode-coupled oscillator.
6AG7 inverter.
6L6 R-L-C peaker.
6L6 buffer amplifier.

Output: 0.1-μsec half-sine-wave positive pulses at 93-ohm impedance level.

Amplitude Control: 0 to 40 volts, control linear but not calibrated.

Frequency Range: 0.2 to 4.9 megacycles in 4 bands. Calibration chart on front panel.

Frequency Stability: 20 parts in 1,000,000.

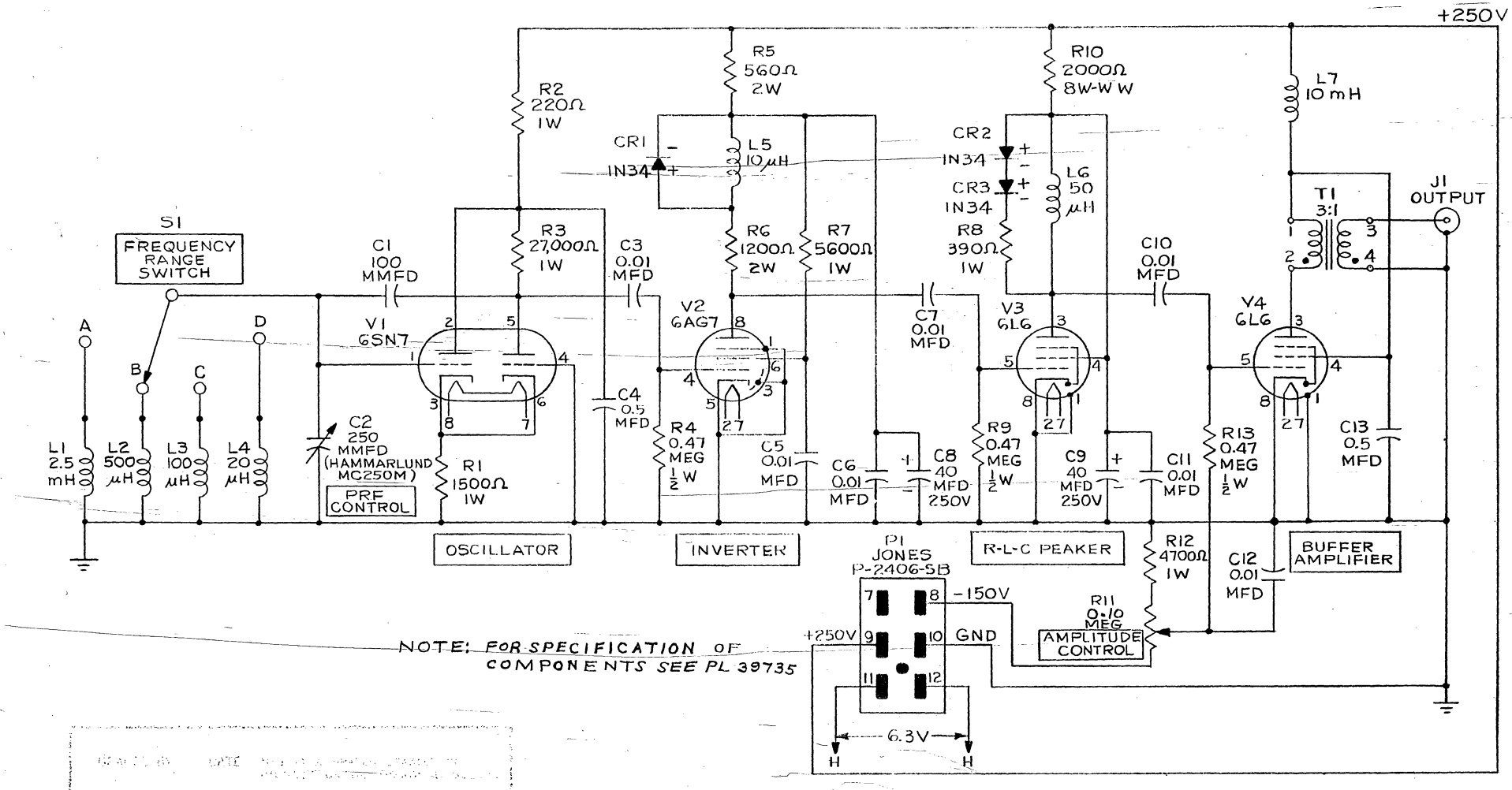
Power Requirements: (standard laboratory power supply)

+250 v, 130 ma (maximum)
-150 v, 1.3 ma
6.3 v a-c, 3.05 amp

References

Circuit Schematic: B-39735-1
Instruction Booklet: Report R-144
Specification of Components: PL 39735

B-39735-3



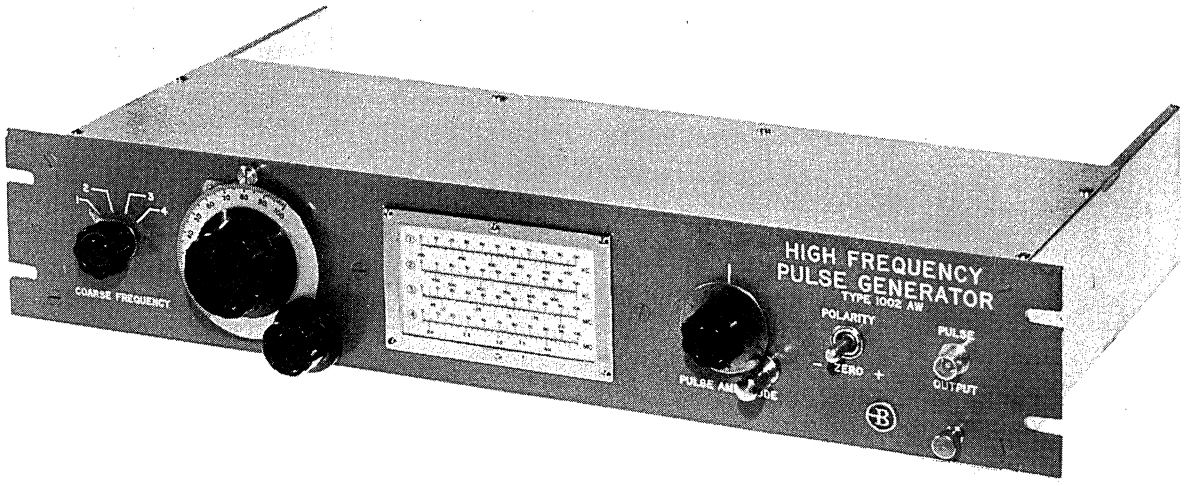
NOTE: FOR SPECIFICATION OF COMPONENTS SEE PL 39735

MHT 1/1/48

VARIABLE-FREQUENCY CLOCK-PULSE GENERATOR MODEL 2

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D.I.C. NO. 6345	DR. F. B. 5-13-48	CK. TL 5/19/48
ENG. HL	B-39735-3	

Burroughs'
HIGH-FREQUENCY PULSE GENERATOR
(Type 1002 AW)



General Description

This unit generates 0.1-μsec pulses at frequencies continuously variable from 0.2 megacycle to 4.5 megacycles in four overlapping bands. A calibrated, L-C controlled, sine-wave oscillator controls the frequency which is within ±8 percent of the value indicated on the calibration chart.

Specifications

Construction: Panel and chassis

Dimensions: 3-1/2 x 19 inches
Depth 10 inches

Controls: Coarse frequency
Fine frequency
Output pulse amplitude
Output pulse polarity

Frequency Range:

Coarse Frequency Setting	Approximate Range
1	200-450 kc
2	430-970 kc
3	0.93-2.1 mc
4	2-4.5 mc

Output: The pulse output jack provides pulses from a transformer-coupled output circuit designed to match the characteristic 93-ohm impedance of coaxial cable. The output pulse polarity is reversible by means of a three-position switch. With the switch in the "ZERO" position the output jack is disconnected from the output circuit. The output amplitude can be varied from 10 to 32 volts and is affected by frequency changes only in the ranges above 2 megacycles.

The duration of the pulses varies with the frequency from a width of 0.14 μsec at the lowest frequency to 0.08 μsec at the highest frequency

Circuit:
6SN7 Oscillator
6AG7 Shaper
6AG7 Peaker
6BF5 Output amplifier

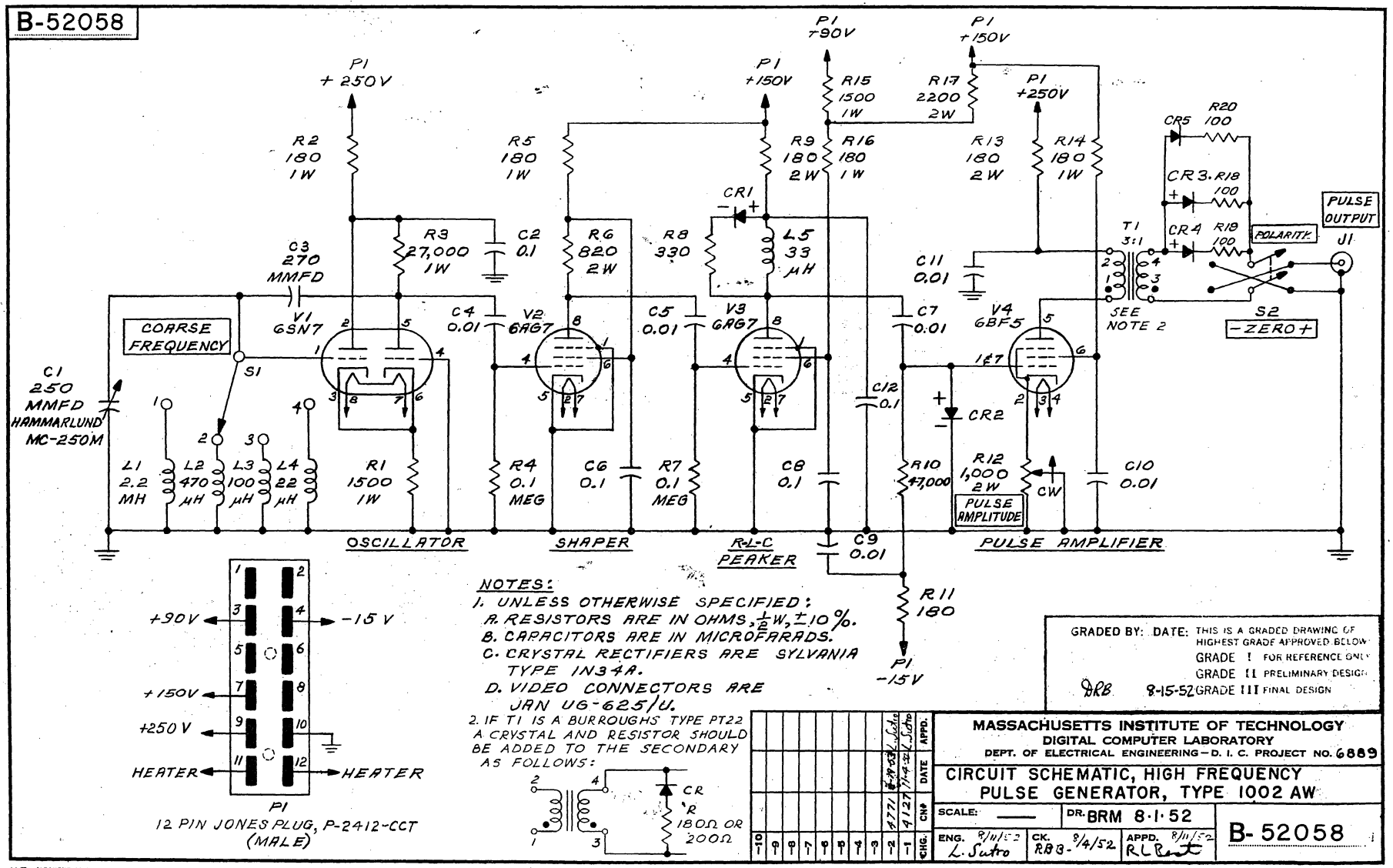
Power Requirements:

+ 250 volts d-c	47 ma
+ 90 volts d-c	36 ma
- 15 volts d-c	0.5 ma
6.3 volts a-c	3.1 amp

References

Circuit Schematic C-52058

B-52058



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTORS ARE IN OHMS, ½W, ±10%.
   - B. CAPACITORS ARE IN MICROFARADS.
   - C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
   - D. VIDEO CONNECTORS ARE JAN UG-625/U.
2. IF T1 IS A BURROUGHS TYPE PT22 A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:

GRADED BY: DRB DATE: 8-15-52

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GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

CHG.	DATE	APPD.
-10		
-9		
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-2	4/7/53	L. Sutro
-1	4/27/54	L. Sutro

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

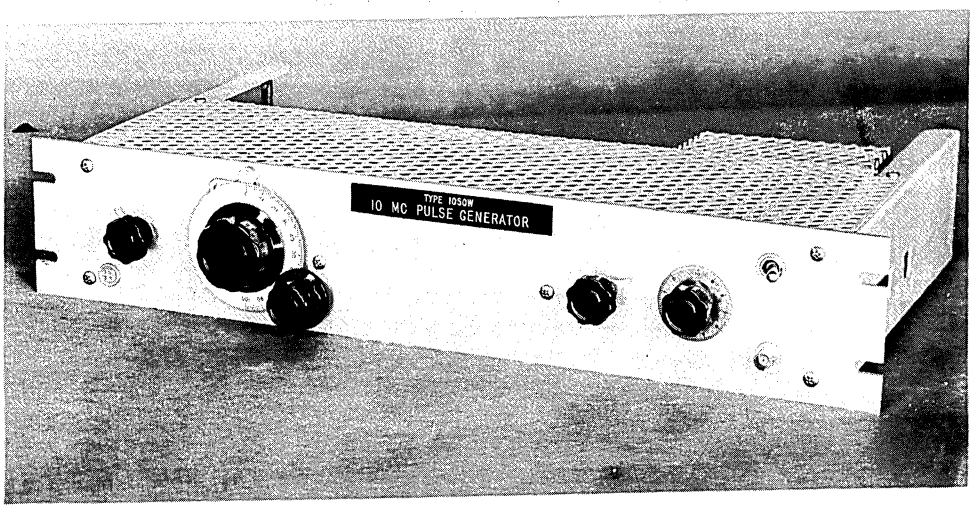
CIRCUIT SCHEMATIC, HIGH FREQUENCY PULSE GENERATOR, TYPE 1002 AW

SCALE: —— DR. BRM 8-1-52

ENG. 9/11/52 L. Sutro | CK. RBG 9/4/52 | APPD. 8/11/52 RLR

B-52058

Burroughs'
10 MC PULSE GENERATOR TYPE 1050 W



General Description

This unit produces half sinewave variable-width voltage pulses at frequencies continuously variable from 1.6 to 10.4 megacycles in four overlapping bands. Power supply unit, type 9802 (3 1/2 in. panel) can be used to power this generator.

Specifications:

Dimensions: 3 1/2 in. x 19 in., depth 10 in.

Output Signal: Amplitude adjustable from 1 volt to 30 volts.
Polarity -- Positive or negative
Pulse width (5 available) 30, 40, 50, 60 & 70 millimicroseconds tolerance ±10%

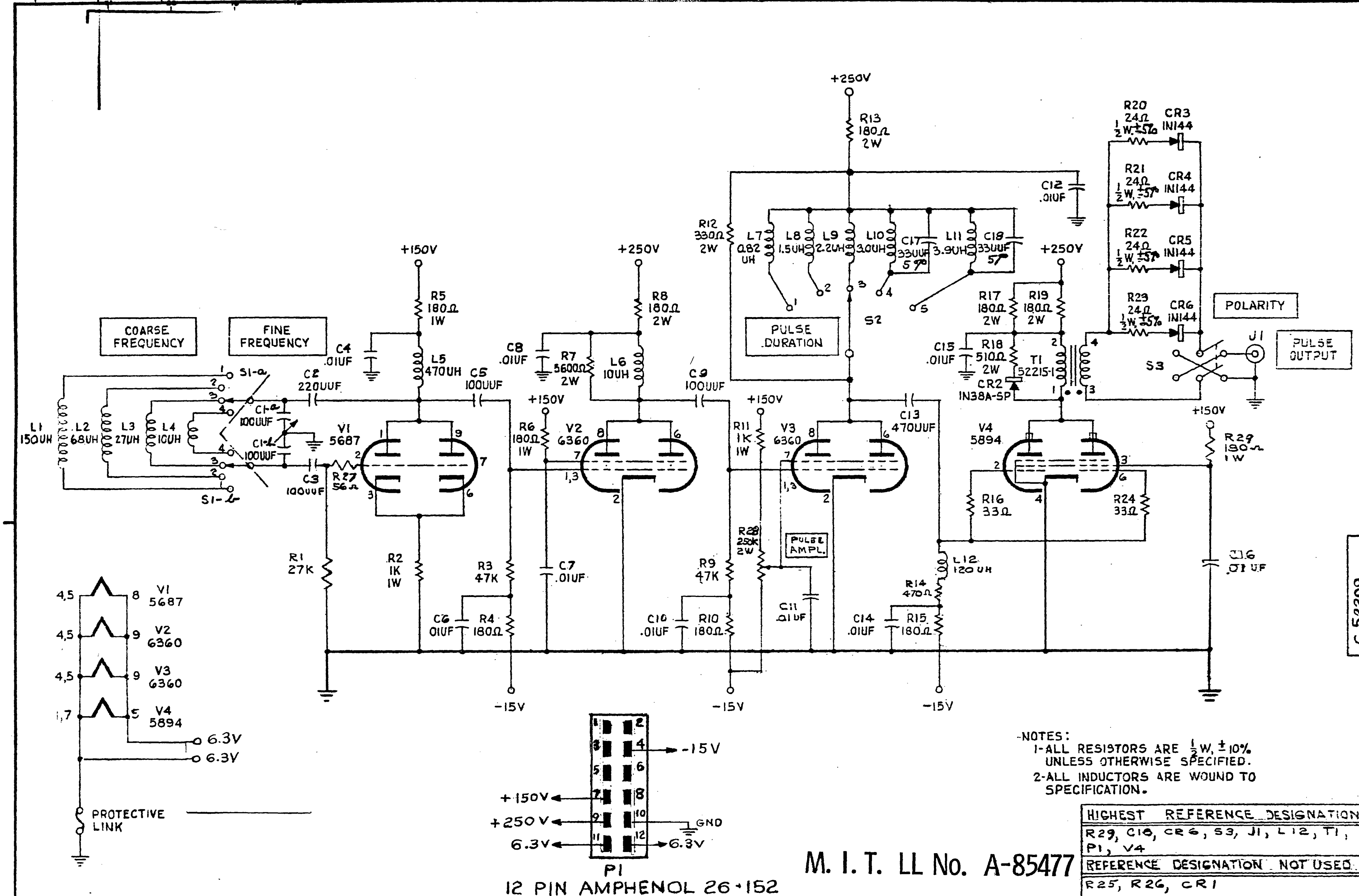
Controls:
Band frequency
Fine frequency
Output pulse amplitude
Pulse width control
Output pulse polarity

Power Requirements:

Voltage	Max Current
+250 VDC	250 MA
+150 VDC	40 MA
-15 VDC	-7 MA
6.3 VAC	4.34 amps

Circuit:
1 5787 oscillator
2 6360 pulse shapers
1 5894 output buffer

References: Circuit Schematic C-85477



+250V
R13 180Ω 2W
C12 .01UF
R12 330Ω 2W
L7 0.82 UH
L8 1.5UH
L9 2.2UH
L10 3.0UH
C17 33UUF 5%
L11 3.9UH
C18 33UUF 5%
S2
PULSE DURATION
COARSE FREQUENCY
FINE FREQUENCY
+150V
R5 180Ω 1W
L5 470UH
C4 .01UF
C5 100UUF
C2 220UUF
S1-a
S1-b
C1-a 100UUF
C1-b 100UUF
L1 150UH
L2 68UH
L3 27UH
L4 10UH
V1 5687
C3 100UUF
R27 56Ω
R1 27K
R2 1K 1W
R3 47K
C6 .01UF
R4 180Ω
C8 .01UF
R7 5600Ω 2W
L6 10UH
R8 180Ω 2W
C9 100UUF
R6 180Ω 1W
V2 6360
C7 .01UF
C10 .01UF
R10 180Ω
R9 47K
R11 1K 1W
V3 6360
R28 250K 2W
PULSE AMPL.
C11 .01UF
C13 470UUF
L12 120 UH
R14 470Ω
C14 .01UF
R15 180Ω
-15V
R17 180Ω 2W
R19 180Ω 2W
C15 .01UF
R18 510Ω 2W
T1 52215-1
CR2 1N38A-SP
V4 5894
R16 33Ω
R24 33Ω
R29 180Ω 1W
C16 .01 UF
R20 24Ω ½W, ±5%
CR3 1N144
R21 24Ω ½W, ±5%
CR4 1N144
R22 24Ω ½W, ±5%
CR5 1N144
R23 24Ω ½W, ±5%
CR6 1N144
POLARITY
S3
J1
PULSE OUTPUT
4,5 8 V1 5687
4,5 9 V2 6360
4,5 9 V3 6360
1,7 5 V4 5894
6.3V
6.3V
PROTECTIVE LINK
+150V
+250V
6.3V
-15V
GND
6.3V
P1
12 PIN AMPHENOL 26-152
C-52209

NOTES:
1-ALL RESISTORS ARE ½W, ±10% UNLESS OTHERWISE SPECIFIED.
2-ALL INDUCTORS ARE WOUND TO SPECIFICATION.

HIGHEST REFERENCE DESIGNATION
R29, C18, CR6, S3, J1, L12, T1, P1, V4
REFERENCE DESIGNATION NOT USED
R25, R26, CR1

M. I. T. LL No. A-85477

REVISIONS
A C-479 ... 10-19-55
B C-487 Balke - 1-19-56 ... 1-23-56
C C-495 ... 2-17-56

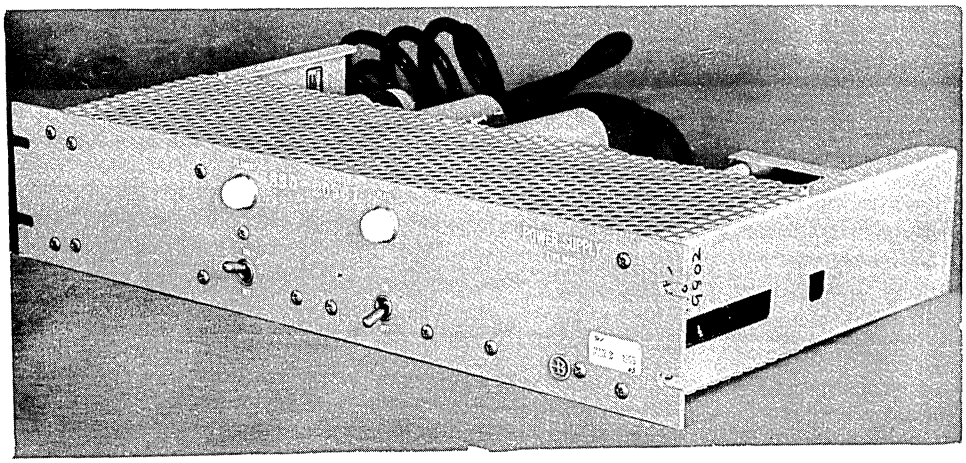
BURROUGHS CORPORATION
ELECTRONIC INSTRUMENTS DIVISION, PHILA., PENNA.

SCHEMATIC
TYPE 1050
PULSE GENERATOR

Unless otherwise specified— Tolerances after Machining: Fract. ±1/64, Dec. ±.005, Ang. ±1/2°; Surface Finish 125

DRAWN SURKIN 9-14-55
CHECKED ... 9-21-55
APPROVED ... 9-21-55
TYPE NO. 1050
PROJ. NO. EP-D-94
DRAWING NO. C-52209

Burroughs' POWER SUPPLY (Type 9802A)

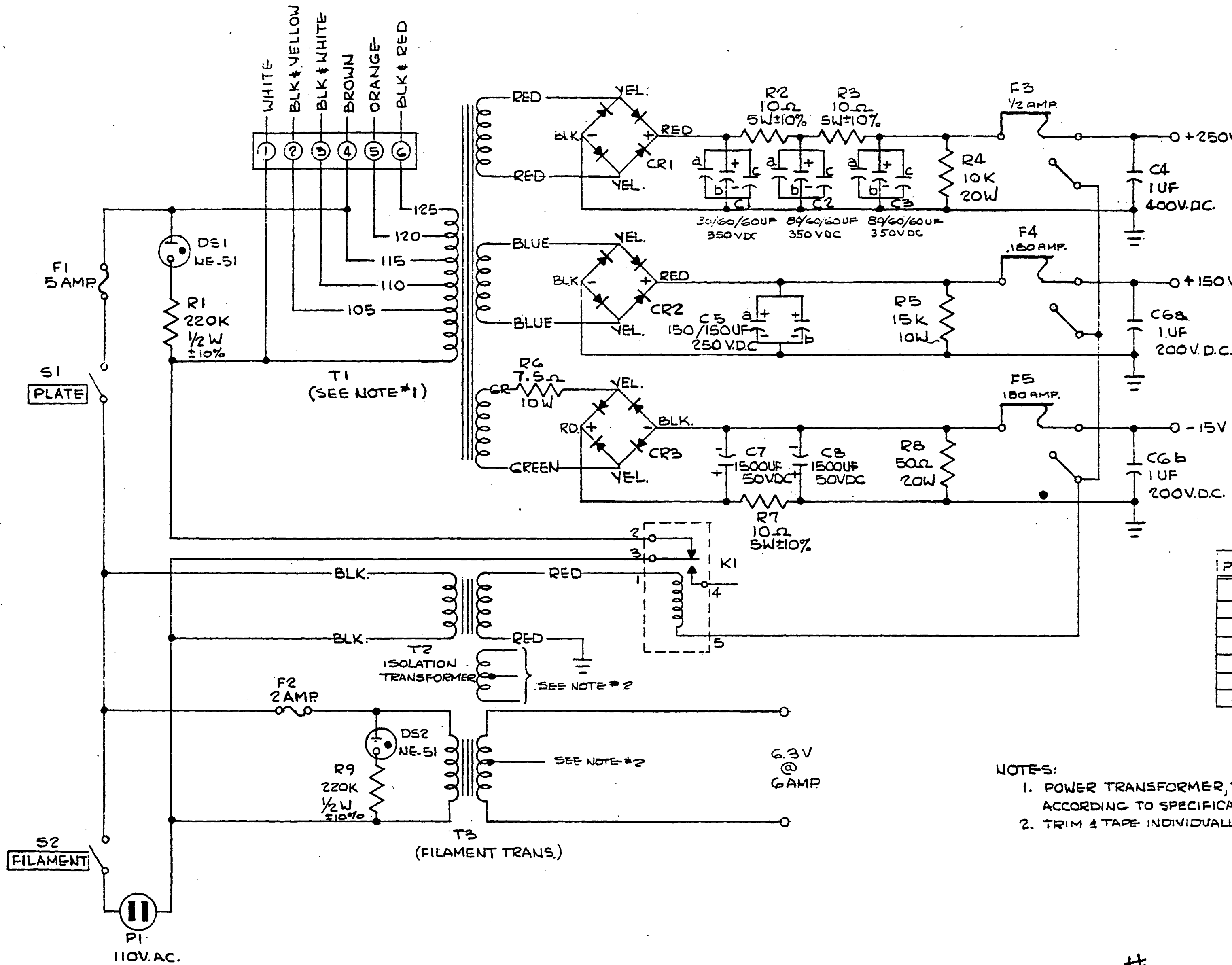


General Description:

This is a power supply designed specifically for use with the Burroughs' Type 1750 BW clock-pulse generator. Comparison of the capabilities of this supply with the requirements of other Burroughts' units will show that this supply can be used to power some other units also.

Specifications:

Dimensions:	3-1/2 in. x 19 in., depth 10 in.	
Inputs:	110 volts, 60 cycles a.c.	
Outputs:	+250 vdc	350 ma.
	+150 vdc	55 ma.
	-15 vdc	-10 ma.
	6.3 vac	4.3 amp
Controls:	Filament power switch. Plate power switch.	
Circuit:	3 full wave semiconductor rectifiers. Grasshopper fuses are used in the dc outputs so that blowing of any fuse will dump the plate supply voltage.	
Power:	110 volts ac.	
References:	Circuit schematic #A-85852	



WHITE
BLK & YELLOW
BLK & WHITE
BROWN
ORANGE
BLK & RED
125
120
115
110
105
F1
5 AMP.
DS1
NE-51
R1
220K
1/2 W
±10%
S1
PLATE
T1
(SEE NOTE #1)
RED
YEL.
BLK
RED
CR1
R2
10 Ω
5W±10%
R3
10 Ω
5W±10%
C1
C2
C3
30/60/60UF
350VDC
80/60/60UF
350VDC
80/60/60UF
350VDC
R4
10K
20W
F3
1/2 AMP.
C4
1UF
400V.DC.
+250V
BLUE
CR2
C5
150/150UF
250 V.D.C
R5
15K
10W
F4
.180 AMP.
C6a
1UF
200V.D.C.
+150V
R6
7.5 Ω
10W
GR
RD
GREEN
BLK.
CR3
C7
1500UF
50VDC
C8
1500UF
50VDC
R7
10 Ω
5W±10%
R8
50 Ω
20W
F5
.180 AMP.
C6b
1UF
200V.D.C.
-15V
K1
BLK.
RED
T2
ISOLATION
TRANSFORMER
SEE NOTE #2
F2
2 AMP.
DS2
NE-51
R9
220K
1/2 W
±10%
SEE NOTE #2
6.3V
@
6 AMP.
T3
(FILAMENT TRANS.)
S2
FILAMENT
P1
110V.AC.

X-1

POWER SOCKET CONNS	
VOLTAGES	PIN NO'S
+ 250	3
+ 150	5
- 15	2
6.3 V.A.C	13
GND	14
6.3 V.A.C	15

NOTES:

1. POWER TRANSFORMER, T1, TO BE SUPPLIED ACCORDING TO SPECIFICATION SP-1031.
2. TRIM & TAPE INDIVIDUALLY LEADS INDICATED.

MIT # A-85852

C-52271

REVISIONS

RELEASED FOR MANUFACTURE
DATE: 12-14-55
BY: J.J. O'B

A C-455 Read 12-16-55 adams 12-21-55

PART NO.	NEXT ASSEMBLY

Unless otherwise specified—Tolerances after Machining

Fract.	Dec.	Ang.	Surface Finish not to exceed
±1/64	±.005	±1/2°	125

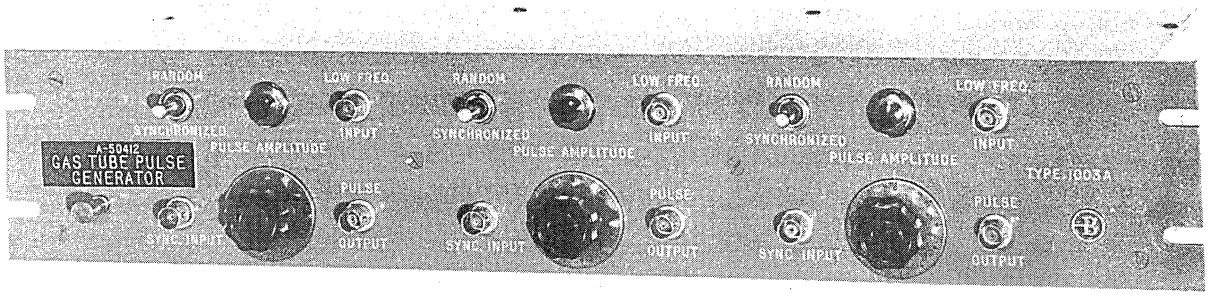
SCALE — DATE
DRAWN BALKE 11/5/55
CHECKED adams 12/14/55
APPROVED [illegible] 12/12/55

BURROUGHS CORPORATION
ELECTRONIC INSTRUMENTS DIVISION, PHILA., PENNA.

SCHEMATIC
POWER SUPPLY
TYPE 9802 A

MATERIAL —
FINISH —
TYPE NO. 9802A
PROJ. NO. E.P.D-119
DRAWING NO. C-52271

Burroughs'
GAS TUBE PULSE GENERATOR
(Type 1003 A or AW)



General Description

This unit generates 0.1-μsec positive pulses. Pulses may be generated in three different ways: (1) by push button, (2) by the coincidence of a positive synchronizing pulse with pushing a button, and (3) by the action of a positive pulse alone, with no push button. Input pulses must be at least 1.2-μsec duration, and of at least 20 volts amplitude. For the second mode of operation, these pulses are fed in the "sync input" jack; for the third mode of operation they are fed in the "low frequency input" jack. The upper frequency limit is 2000 cycles. Three identical units are mounted on one 3-1/2 x 19-inch panel.

Specifications

Construction:	Panel and chassis
Dimensions:	3-1/2 x 19 inches Depth 10 inches
Circuit:	2D21 Trigger Tube 2D21 Pulse Generator

Controls: The circuit is so designed that only one pulse is generated for each push-button depression.

A selector switch with "Random" and "Synchronized" positions permits generation of an output pulse by depressing the push button in "Random" position or in "Synchronized" position provided a sync pulse is received at the sync input jack during the time the button is depressed. The output pulse is fired four μsec after the positive rise of the sync pulse.

The output pulse amplitude may be varied from 0 to 35 volts.

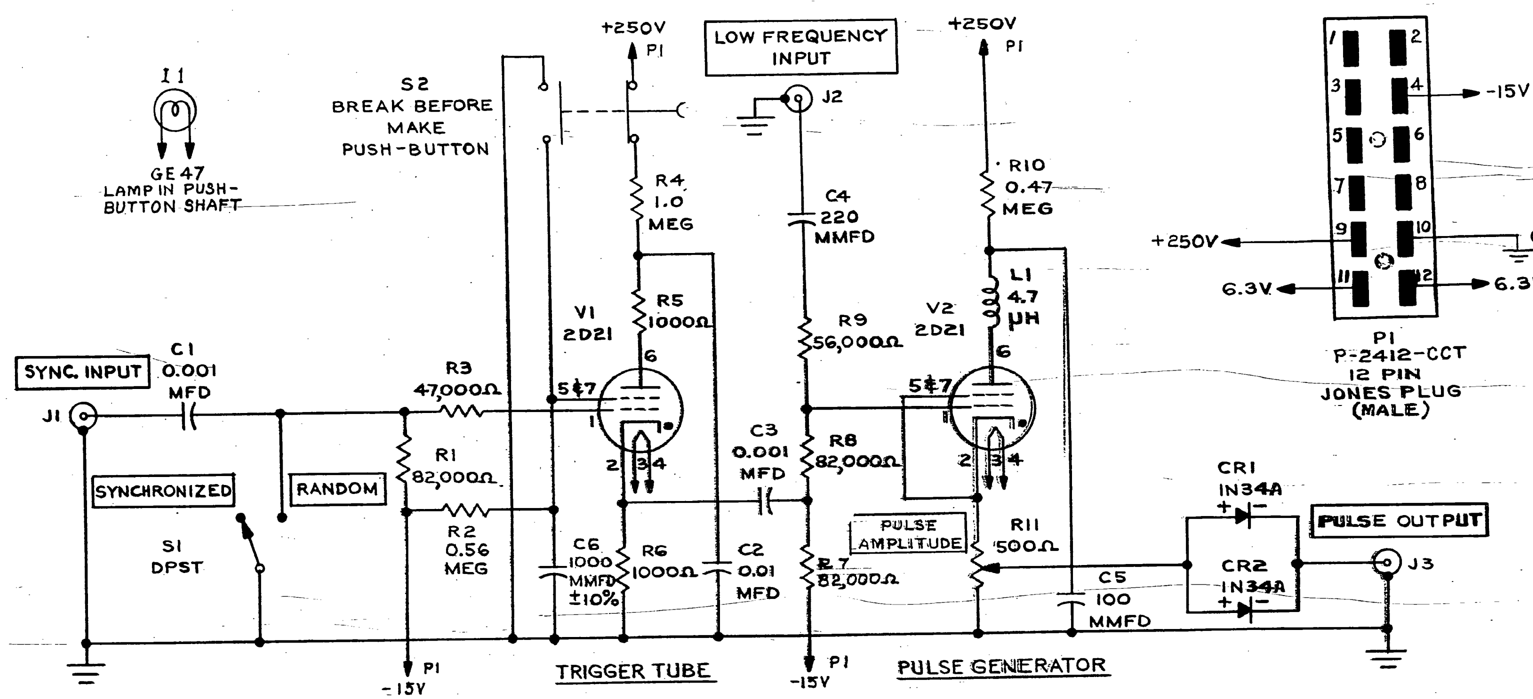
Power Requirements:

+150 volts d-c	0.3 ma
- 15 volts d-c	0.6 ma (surge)
6.3 volts a-c	3.6 amps

References

Circuit Schematic	B-50412
Engineering Note	E-434
Photograph	F-1553

B-50412



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE ½W, ±10%.
   B. VIDEO CONNECTORS ARE JAN. UG-625/U
2. THREE IDENTICAL CIRCUITS SIMILAR TO THE ABOVE ARE LOCATED ON PANEL.

DRAWING REFERENCES:
1. BURROUGHS EQUIP., PULSE GENERATOR, TYPE 1003AW: A-10563 B
2. LAMICOID LABEL: A-50613

GRADED BY:	DATE:	THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
		GRADE I FOR REFERENCE ONLY
		GRADE II PRELIMINARY DESIGN
JRB	8-15-52	GRADE III FINAL DESIGN

CHG.	1	2	3	4	5	6	7	8	9	10
CH#		3720								
DATE		6-26-52								
APPD.		L.S.								

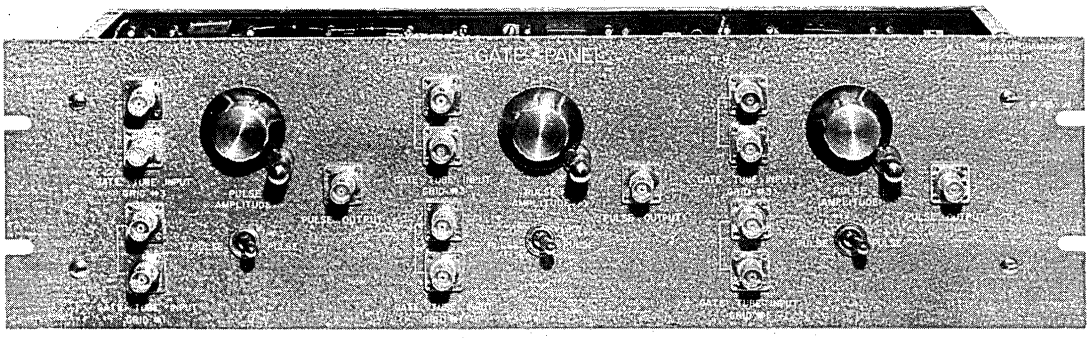
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING—D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC,
GAS TUBE PULSE GENERATOR, TYPE 1003 AW

SCALE: ——— DR. A.M.G. 6-26-52
ENG. 7-21-52 L.L.S. CK. 7/14/52 RBB. APPD. 8/11/52 R L Best

B-50412

GATE PANEL



General Description

The gate panel consists of three independent gate tubes and associated buffer amplifiers. The No. 3 grid of each gate tube is connected to paired jacks on the front panel so that externally generated gates can be utilized. The No. 1 grids also have paired input jacks for pulses to be gated. The polarity and amplitude of the output pulse can be selected by panel controls.

The gate panel was designed to provide auxiliary gate-tube circuits for the register panel (a-c or d-c). In applications where steady-state gate pulses are used, the gates can be obtained from the gate and delay unit.

Specifications

Construction: Panel and chassis for standard rack mounting.

Dimensions: 5 x $5\frac{1}{2}$ x 19 inches.

Circuits: 3 7AK7 gate tubes.
3 7AD7 buffer amplifiers.

Input: External gates
Paired input jacks to the No. 3 grid of each 7AK7.
0.1-microfarad coupling condenser extends lower repetition frequency range of gate.
Switch for selecting input from a-c or d-c register panel.

Pulses to be gated
Paired input jacks to No. 1 grid of gate tube.
Input pulse must be positive.

Input Amplitudes:
Min. 14 v, (to obtain specified output amplitude range) max. 35 v.

Output: Gated pulses
Each gate tube has a single output jack.
Polarity reversible.
Amplitude control in cathode of 7AD7, 6 to 23 volts.

Minimum Delay: (all sections) 0.06 μsec.

Resolution Time: (all sections) 0.33 μsec.

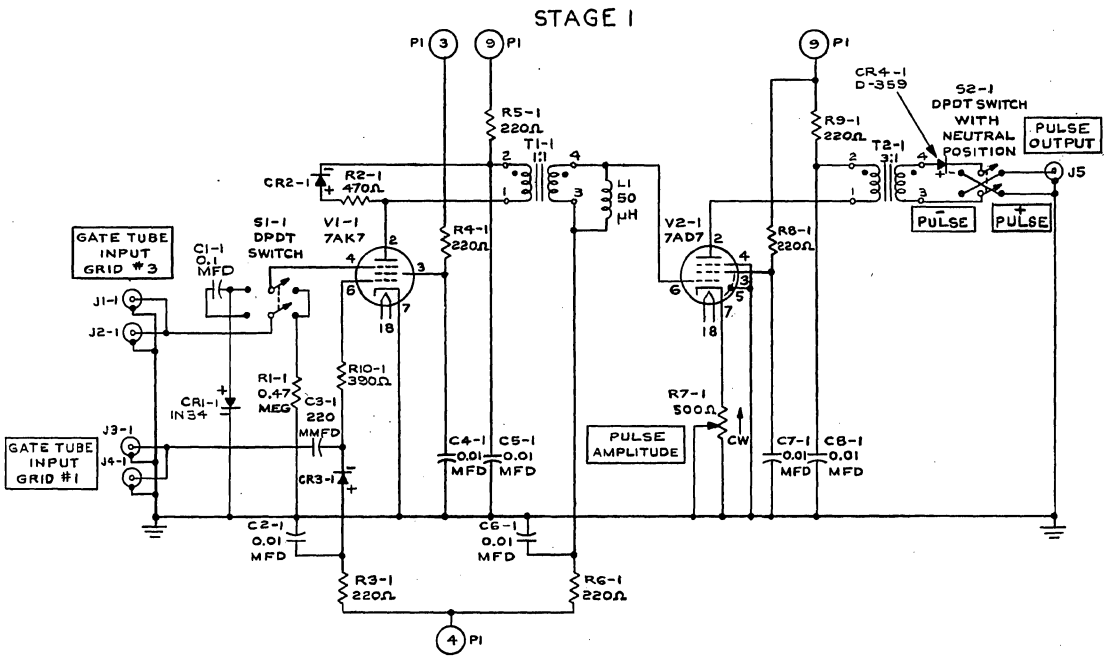
Power Requirements (all sections):

Voltages	Current with no signal	Current with 1-mc clock pulses
+250 v	1.2 ma	17.0 ma
+150 v	1.5 ma	6.1 ma
+ 90 v	0.5 ma	8.3 ma
- 15 v	0	2.2 ma
6.3 v a-c	4.2 amp	4.2 amp

References

Circuit Schematic: C-32496
Instruction Booklet: Report R-151

C-32496-3



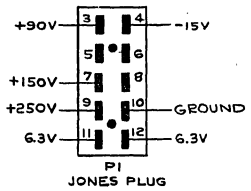
STAGE 2

STAGE 3

NOTES:

THE FOLLOWING SHALL APPLY TO ALL COMPONENTS ON THIS DRAWING UNLESS OTHERWISE SPECIFIED:

1. STAGES 2 AND 3 ARE IDENTICAL WITH STAGE 1 EXCEPT FOR DASH NUMBERS OF COMPONENTS. FOR INSTANCE, THE CHOKE IN STAGE 3 IS L1-3.
2. RESISTORS ARE JAN SPEC., COMPOSITION TYPE, 1W, ±10%.
3. CAPACITORS ARE JAN SPEC., MICA, ±10%.
4. VIDEO CONNECTORS ARE UG-290U.
5. CRYSTAL RECTIFIERS ARE TYPE D-357.



DRAWING REFERENCE:
TERMINAL BOARD AND PANEL WIRING DIAGRAM: SC-40037.

GRADED BY DATE

GRADE I
GRADE II PRELIMINARY DESIGN
GRADE III

DRN A.M.G. 8-22-49
CK'D 8/23/49
APP'D

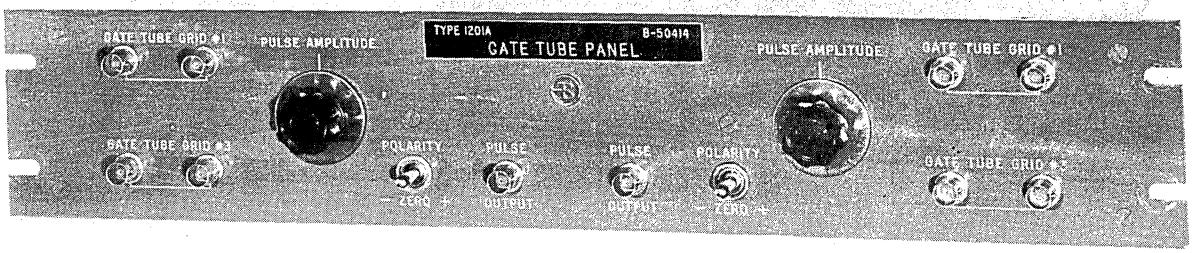
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC, GATE PANEL

C-32496-3

B-REDUCTION

Burroughs'
GATE TUBE PANEL
(Type 1201 A or AW)



General Description

This unit consists of two independent sections mounted on one panel. Each section consists of a 7AK7 gate tube followed by a pulse standardizer which puts out 0.1-μsec pulses.

Specifications

Construction: Panel and chassis

Dimensions: 3-1/2 x 19 inches
Depth 10 inches

Circuit (each section):

7AK7 Gate Tube
6AG7 Peaker
6AG7 Pulse Amplifier

Controls: Output pulse amplitude may be varied from 10 to 32 volts; polarity may be reversed.

Input: No. 1 grid: Pulse to be gated is coupled to No. 1 grid of gate tube through a capacitor and crystal clamp circuit connected to -15 volts. Input pulse must be positive 0.1 μsec long, with an amplitude of at least 13 volts.

No. 3 grid: D-C level must be at more than -15 volts to hold the gate tube off; at ground to hold it on.

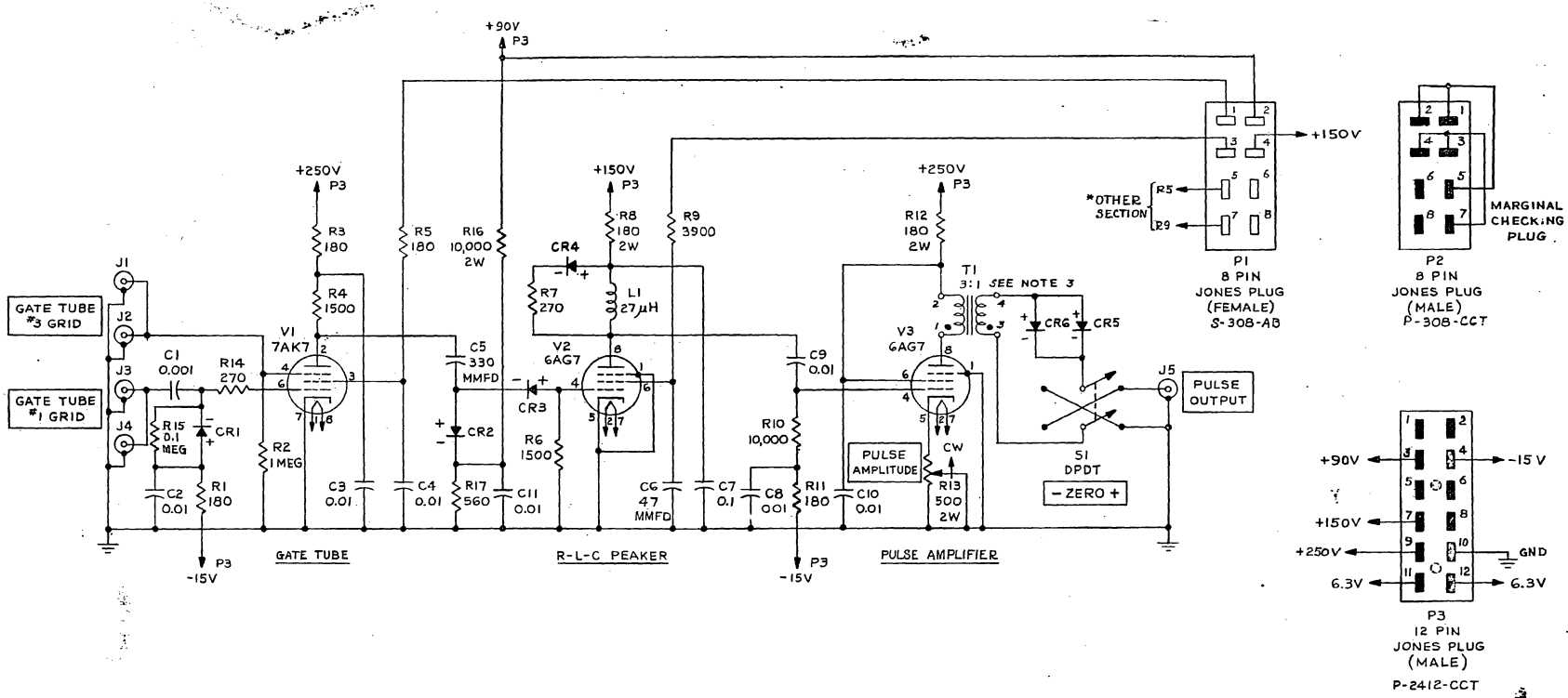
Power Requirements:

+250 volts d-c	60 ma
+150 volts d-c	70 ma
+120 volts d-c	30 ma
+90 volts d-c	20 ma
-15 volts d-c	7 ma
6.3 volts a-c	4.2 amps

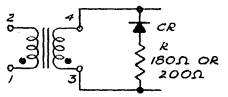
References

Circuit Schematic	C-50414
Engineering Note	E-434
Photograph	F-1555

C- 50414



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, ½W, ±10%.
   B. CAPACITORS ARE IN MICROFARADS.
   C. VIDEO CONNECTORS ARE JAN UG-625/U
   D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
* 2. TWO SECTIONS TO BE MADE FOR EACH PANEL
3. IF T1 IS A BURROUGHS TYPE P22 A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:



DRAWING REFERENCES:
1. LAMICOID LABEL: A-50600
2. BURROUGHS EQUIPMENT; COINCIDENCE DETECTOR TYPE 1201AW; B-10567A
3. ASSEMBLY & PL: R-53323

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:

GRADE I FOR REFERENCE ONLY

GRADE II PRELIMINARY DESIGN

DRB 8-15-52 GRADE III FINAL DESIGN

CHG.	DATE	APPD.
-10		
-9		
-7		
-5		
-4	4-29-52	L.S.
-3	4-30-52	L.S.
-2	5-22-52	L.S.
-1	7/11/52	L.S.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC
GATE TUBE PANEL, TYPE 1201AW

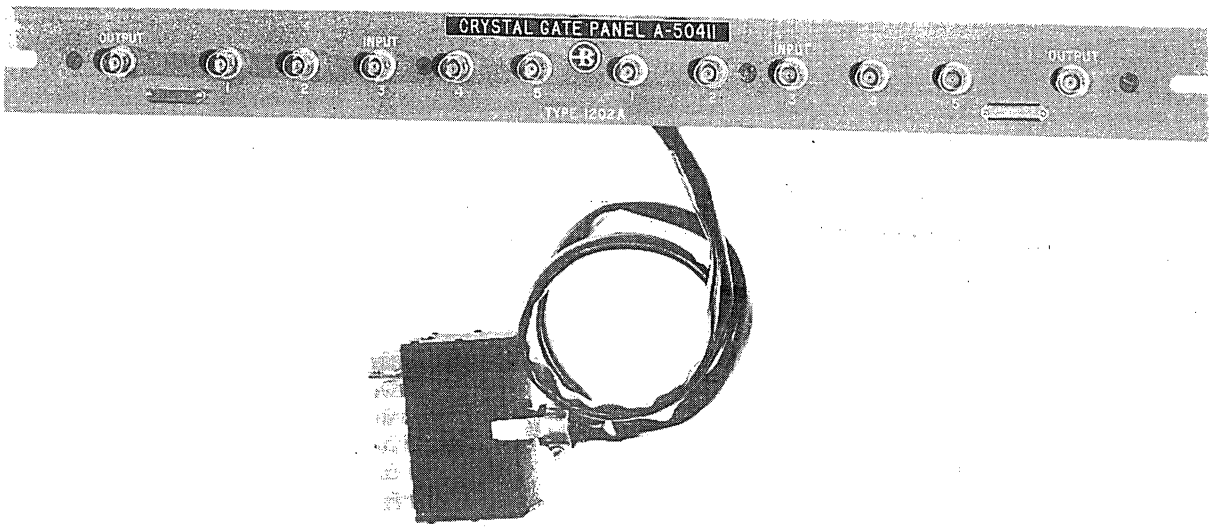
SCALE: ~ DR. F.B. July 1 '52

ENG. 7/14/52 L.L.S. CK. 7/14/52 R.B.B. APPD. 8/11/52 E.L. Ragan

C- 50414

MIN

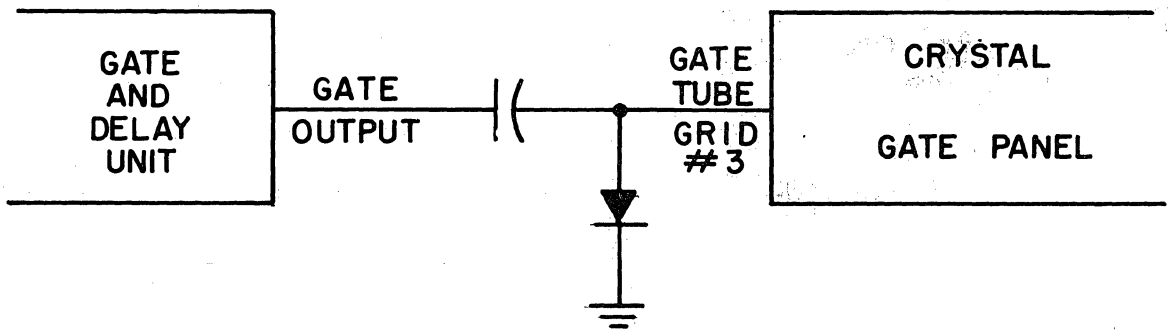
Burroughs'
CRYSTAL GATE PANEL
(Type 1202 A or AW)



General Description

Two identical units occupy one 1-3/4-inch panel, each having five inputs and one output. They are meant to be operated from d-c coupled gates which run between two voltage levels, the lower of which should be -15 or more, and the upper of which should be zero or positive. The output assumes a voltage equal to the most negative input; it will be zero or positive only if all the inputs are zero or positive.

The output of a Burroughs' Flip-Flop, a D-C Register Panel, or a Burroughs' Gate and Delayed-Pulse Generator may be connected directly to this input. However, a Whirlwind Gate and Delay Unit may not be connected directly to this jack, since the d-c level of the output of the Whirlwind Gate and Delay Unit is about +30 volts. The only way in which this unit may be used with the Whirlwind Gate and Delay Unit is if the gate duty cycle is greater than 0.05. Connections would be made as shown below.



The time constant of the coupling capacitor and a resistance of 15,000 ohms should be at least five times the maximum interval between gates,

Specifications

Construction: Panel and chassis

Dimensions: 1-3/4 x 19 inches
Depth 2 inches

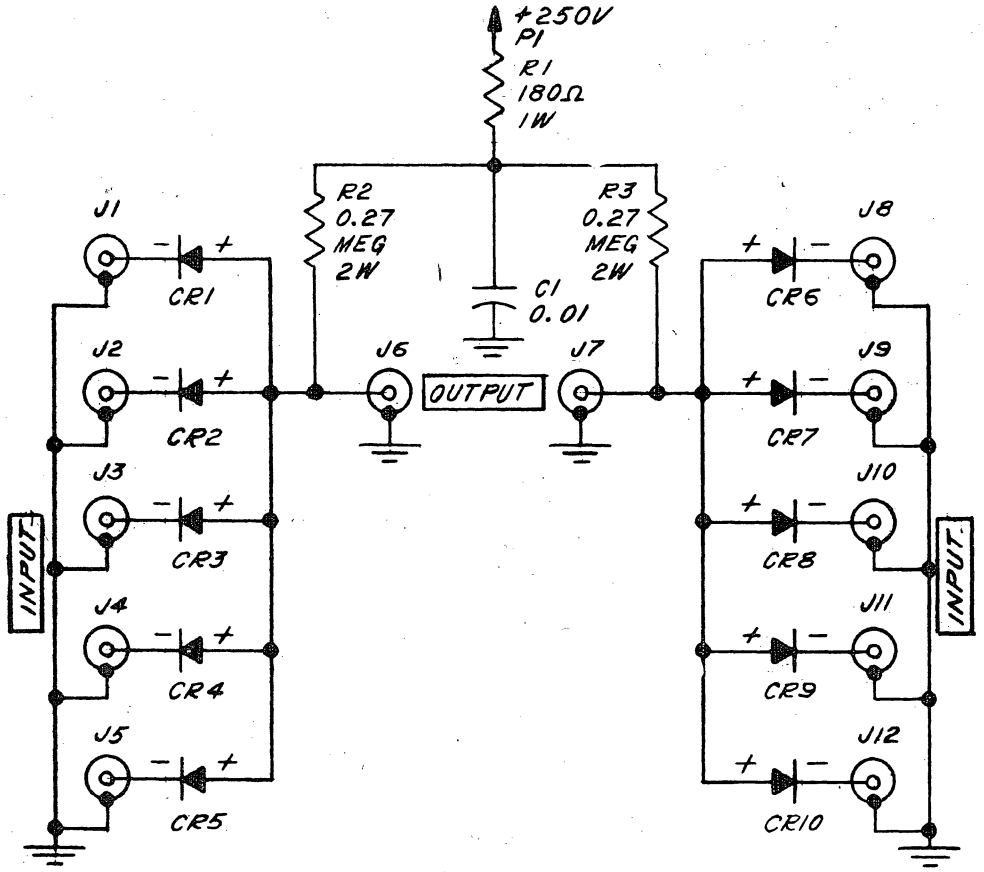
Power Requirements:

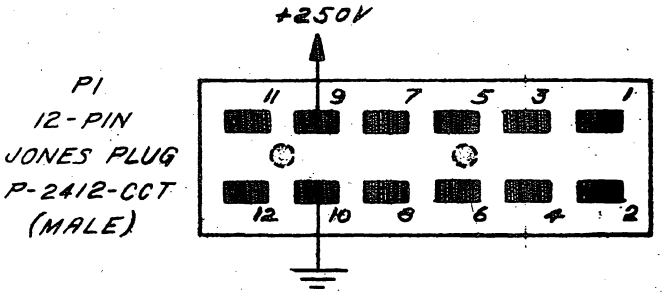
+250 volts d-c 1 ma
for each section

References

Circuit Schematic	A-50411
Engineering Note	E-434
Photograph	F-1556

A-50411





DRAWING REFERENCES:
1. LAMICOID LABEL A-50615
2. BURROUGHS EQUIPMENT:
COINCIDENCE DETECTOR,
TYPE 1202A (WW)
DWG. # A-10560A

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:

GRADE I FOR REFERENCE ONLY

GRADE II PRELIMINARY DESIGN

DRB 8-15-52 GRADE III FINAL DESIGN

NOTES:
1. VIDEO CONNECTORS ARE JAN UG-625/U
2. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2	3719	7-3-52	L.S.
-1			

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

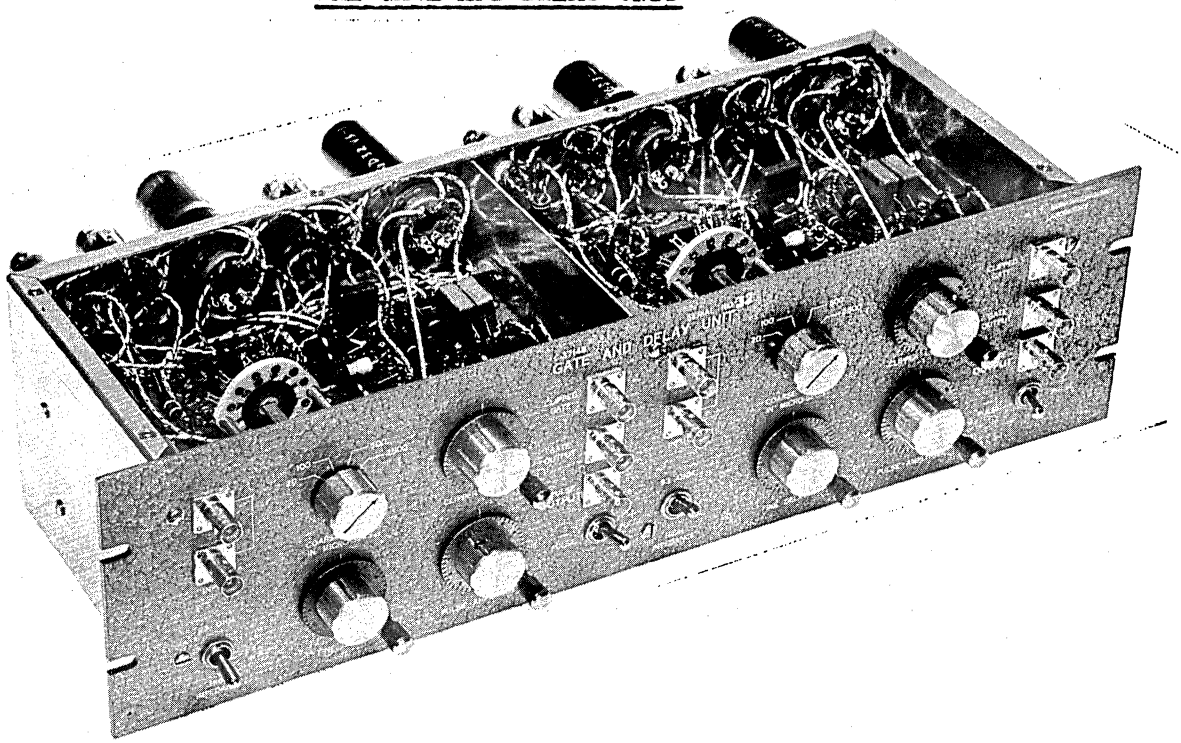
CIRCUIT SCHEMATIC,
CRYSTAL GATE PANEL, TYPE 1202AW

SCALE: —— DR. A. S. 7-3-52

ENG. 7/21/52 L. L. S. CK. 7-14-52 RBB APPD. 8/11/52 R L Best

A-50411

THE GATE AND DELAY UNIT



General Description

The purpose of the gate and delay unit is to provide a test equipment building block which can supply a gate pulse, a delayed pulse, or both, to external test blocks or complete systems.

Specifications

Dimensions: length - 19 inches
width - 5 1/2 inches
depth - 6 1/4 inches

Circuits (duplicate sections): 6AK5 trigger tube.
1/2 5687 delay multivibrator.
6L6 cathode follower.
6L6 R-L-C peaker.
6L6 buffer amplifier

Input (each section): 0.1-μsec half-sine-wave positive pulses of at least 20 volts amplitude.

Output (each section): Unclipped gate:
Amplitude +40 volts.
Rise time 0.2 μsec.
Fall time 0.1 μsec.

Clipped gate -
Rise time 0.3 μsec.
Fall time 0.1 μsec.
Gate length continuously variable from 0.5 μsec to 2500 μsec in four overlapping ranges.

Delayed (output) pulse:
0.1-μsec half-sine-wave pulse across a 93-ohm impedance.
Pulse amplitude is continuously variable from 0 to approximately 40 volts.
Polarity reversible.
Delay time equal to gate length.

Resolution Time: For coarse delay setting of 10 μsec: 1 μsec.
50 μsec: 2 μsec.
450 μsec: 10 μsec.
2500 μsec: 70 μsec.

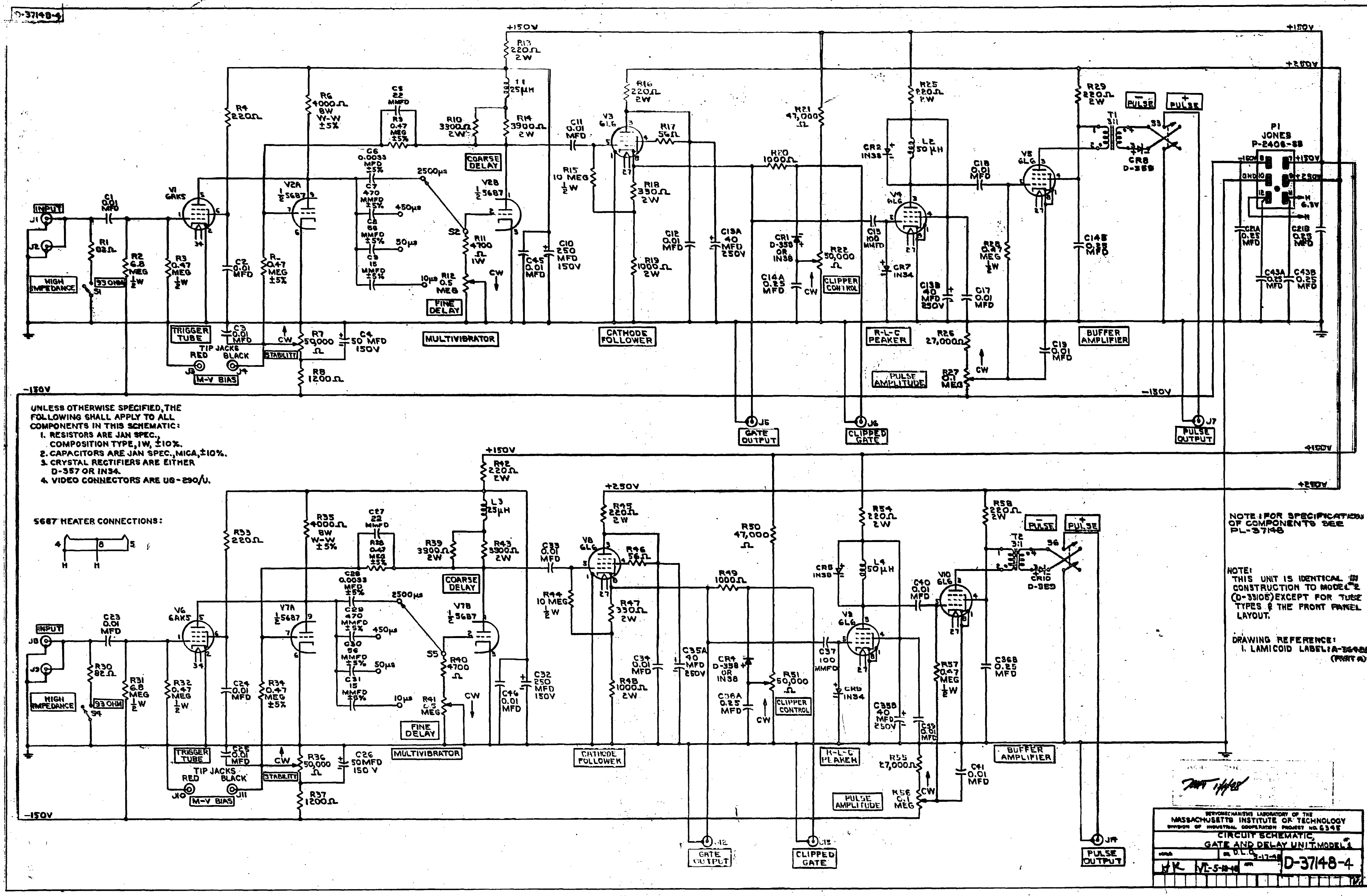
Power Requirements: (both sections)

Voltages	Currents	
	No Sig.	4-kc Signal
+250 v d.c.	115 ma	110 ma
+150 v d.c.	220 ma	195 ma
-150 v d.c.	8.5 ma	8.5 ma
6.3 v a.c.	7.55 amp	7.55 amp

Voltage Regulation: The voltages of the multivibrator are filtered sufficiently to allow operation with an unregulated power supply which is reasonably stable.
Any low-frequency variations, of the order of 5 cps, in the power supply will change the delay time of the unit.

References

Engineering Note: E-121
Circuit Schematic: D-37148
Photograph: F-679


D-37148-4
UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS IN THIS SCHEMATIC:
1. RESISTORS ARE JAN SPEC., COMPOSITION TYPE, 1W, ±10%.
2. CAPACITORS ARE JAN SPEC., MICA, ±10%.
3. CRYSTAL RECTIFIERS ARE EITHER D-357 OR IN34.
4. VIDEO CONNECTORS ARE UG-290/U.
5687 HEATER CONNECTIONS:
NOTE: FOR SPECIFICATIONS OF COMPONENTS SEE PL-37148
NOTE: THIS UNIT IS IDENTICAL IN CONSTRUCTION TO MODEL 2 (D-33105) EXCEPT FOR TUBE TYPES & THE FRONT PANEL LAYOUT.
DRAWING REFERENCE:
1. LAMICOID LABEL: A-36488 (PART A)
INPUT
HIGH IMPEDANCE
93 OHM
TRIGGER TUBE
TIP JACKS
RED
BLACK
M-V BIAS
STABILITY
MULTIVIBRATOR
COARSE DELAY
FINE DELAY
CATHODE FOLLOWER
CLIPPER CONTROL
R-L-C PEAKER
PULSE AMPLITUDE
BUFFER AMPLIFIER
GATE OUTPUT
CLIPPED GATE
PULSE OUTPUT
- PULSE
+ PULSE
P1 JONES P-2406-SB
+150V
+250V
-150V
6.3V
SERVOMECHANISMS LABORATORY OF THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345
CIRCUIT SCHEMATIC, GATE AND DELAY UNIT, MODEL 3
D-37148-4

GATE AND DELAY UNIT
Model 2

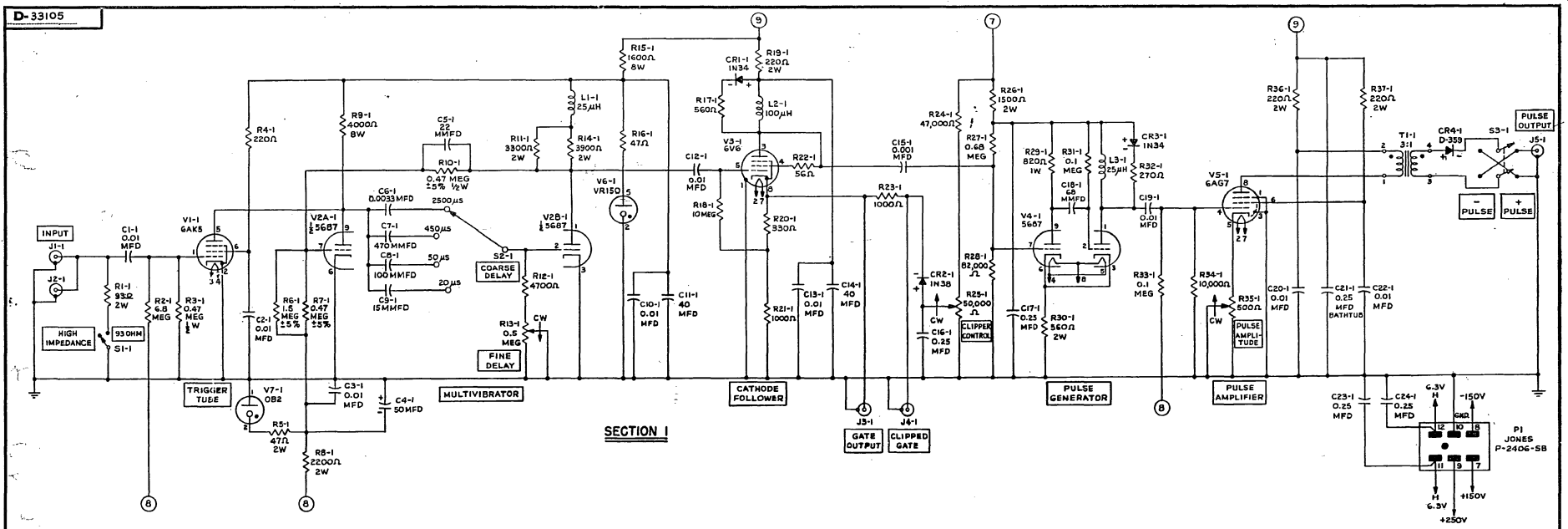
This unit differs from Model 1 only in its tube complement:

6AK5	Trigger Tube
5687	Multivibrator
6V6	Cathode Follower
5687	Pulse Generator
6AG7	Output pulse Amplifier

Reference

Circuit Schematic D-33105

D-33105



SECTION 1

SECTION 2

NOTES:

1. STAGE 1 AND STAGE 2 ARE IDENTICAL EXCEPT FOR DASH NUMBERS OF COMPONENTS. FOR EXAMPLE: THE JACK IN STAGE 2 IS J1-2.
2. UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS IN THIS SCHEMATIC:
   1. RESISTORS ARE JAN SPEC., COMPOSITION TYPE, 1W, ±10%.
   2. CAPACITORS ARE JAN SPEC., MICA, ±10%.
   3. VIDEO CONNECTORS ARE UG-290/U.
3. FOR FURTHER SPECIFICATION OF COMPONENTS SEE PL-33105.
4.  5687 HEATER CONNECTIONS.

DRAWING REFERENCES:

1. REAR PANEL WIRING DIAGRAM: SC-33100
2. PANEL & COVER LAYOUT: SC-33101
3. TERMINAL BOARD WIRING DIAGRAM: SC-33102
4. TERMINAL BOARD TEMPLATE: SC-33103
5. PANEL LETTERING TEMPLATE: SC-33104

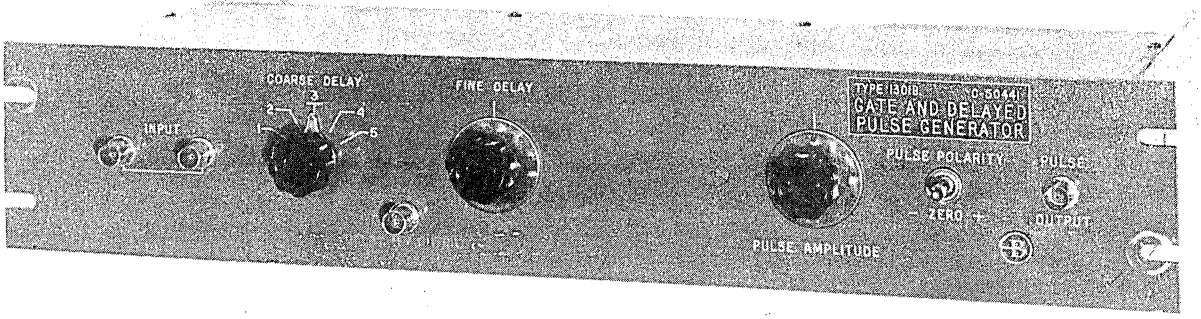
GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW.
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
1/6/51

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

CIRCUIT SCHEMATIC
GATE AND DELAY UNIT, MODEL 2

SCALE: NONE | DR. F.B. JAN. 5 '51 | CK. 1-9-51 | APP. | D-33105 | B-REDUCTION

Burroughs'
GATE AND DELAYED-PULSE GENERATOR
(Type 1301 B or BW)



General Description

This unit consists of a gate generator designed to be triggered by 0.1-μsec pulses. The gate output is d-c coupled, swings between approximately -20 and +5 volts, and may be varied from 1 to 80,000 μsec in length in five overlapping ranges. The gate output impedance is less than 1000 ohms, and the rise time less than 1/4 μsec. A 0.1-μsec positive or negative pulse is generated at the end of the gate, so that it is in effect the input pulse delayed by the length of the gate.

Specifications

Construction: Panel and chassis

Dimensions: 3-1/2 x 19 inches
Depth 10 inches

Controls: Coarse delay
Fine delay
Output pulse amplitude
Output pulse polarity

Input: (Two jacks in parallel)

Positive 0.1-μsec pulses having a minimum amplitude of about 13 volts.

Pulse Output: The output amplitude is variable from 10 to 32 volts and polarity is reversible.

Delay MV Output: During the delay interval the output is approximately +15 volts. During standby it is approximately -20 volts. Rise time when driving 100μμf is less than 0.1 μsec.

Coarse Delay Setting	Delay Range (μsec)
1	1-22
2	10-250
3	90-2000
4	850-17,000
5	9000-80,000

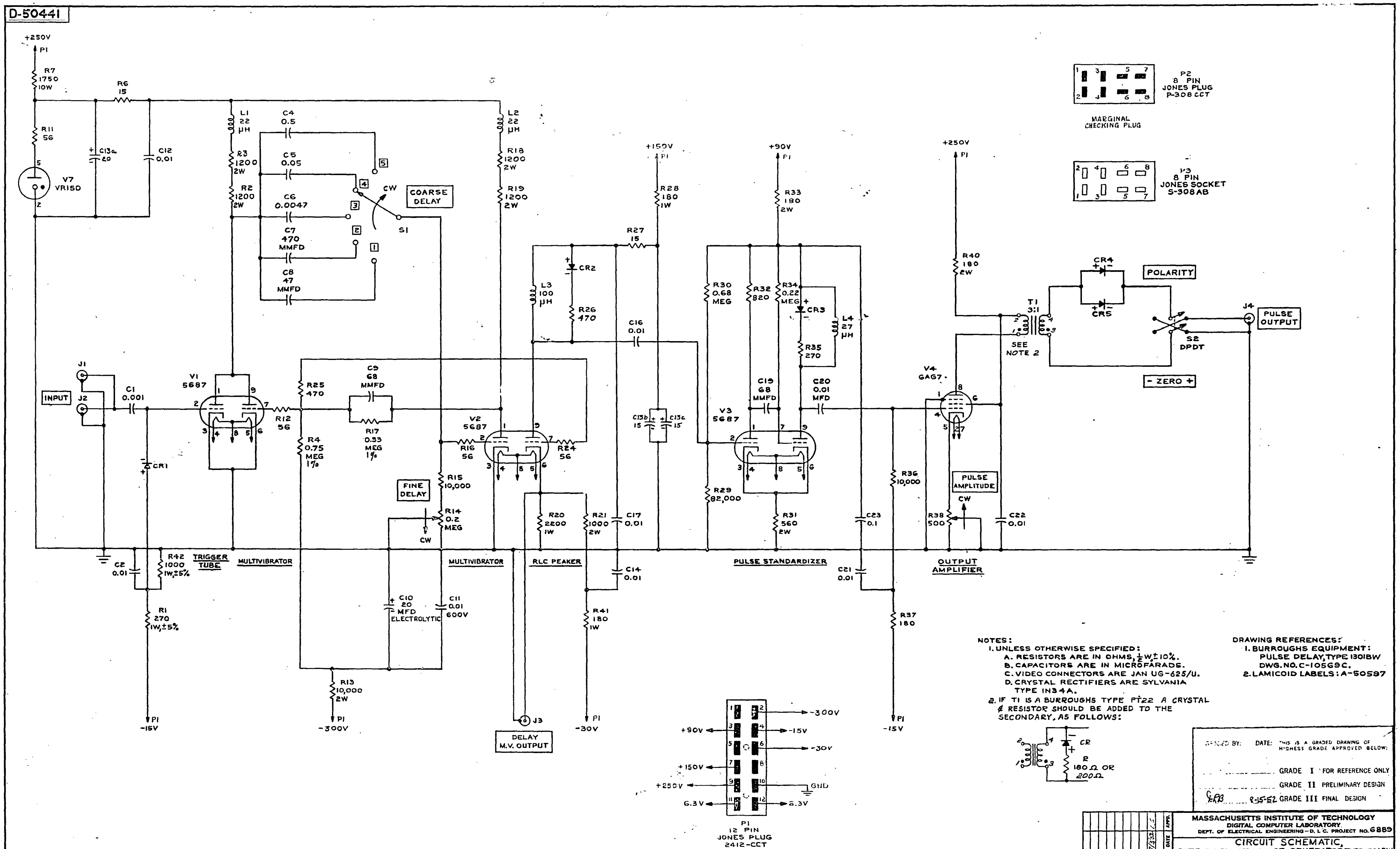
Circuit:
1/2 5687 Trigger tube
5687 Multivibrator
1/2 5687 Peaker and cathode follower
5687 Pulse standardizer
6AG7 Output amplifier
VR150 Voltage regulator for +250v

Power Requirements:

+250 volts d-c	60 ma
+150 volts d-c	18 ma
+ 90 volts d-c	40 ma
- 15 volts d-c	1 ma
- 30 volts d-c	30 ma
-300 volts d-c	0.5 ma
6.3 volts a-c	3.35 amp

References

Circuit Schematic	D-50441
Engineering Note	E-434
Photograph	F-1557



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, ½W, ±10%.
   B. CAPACITORS ARE IN MICROFARADS.
   C. VIDEO CONNECTORS ARE JAN UG-625/U.
   D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE IN34A.
2. IF T1 IS A BURROUGHS TYPE PT22 A CRYSTAL & RESISTOR SHOULD BE ADDED TO THE SECONDARY, AS FOLLOWS:

DRAWING REFERENCES:
1. BURROUGHS EQUIPMENT: PULSE DELAY, TYPE 1301BW DWG. NO. C-10569C.
2. LAMICOID LABELS: A-50597

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
RRB 8-15-52 GRADE III FINAL DESIGN

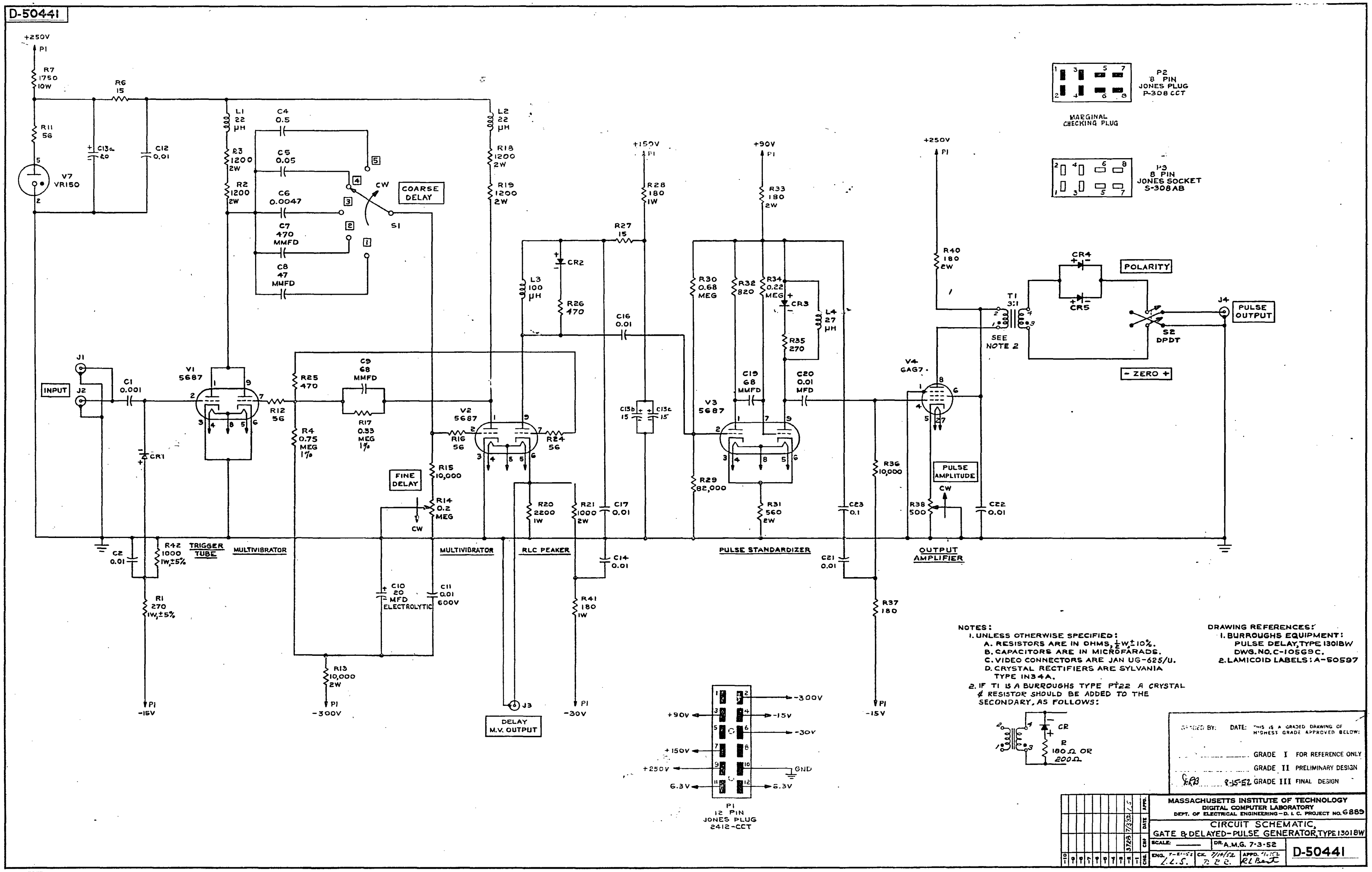
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO. 6889

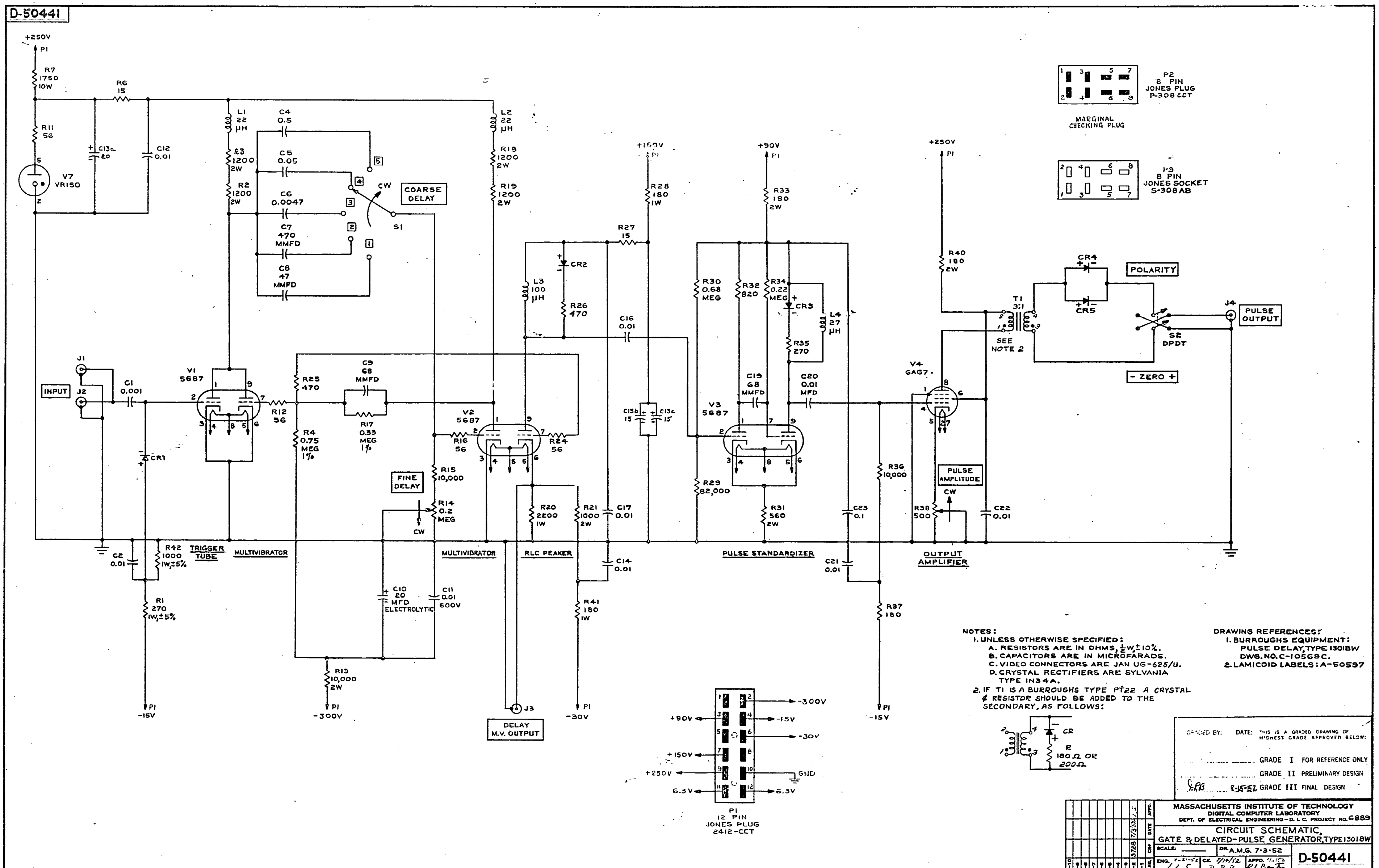
CIRCUIT SCHEMATIC,
GATE & DELAYED-PULSE GENERATOR, TYPE 1301BW

SCALE: ——— DR. A.M.G. 7-3-52
ENG. 7-21-52 L.L.S. CK. 7/14/52 R.E.C. APPD. 7/1/52 RL Best

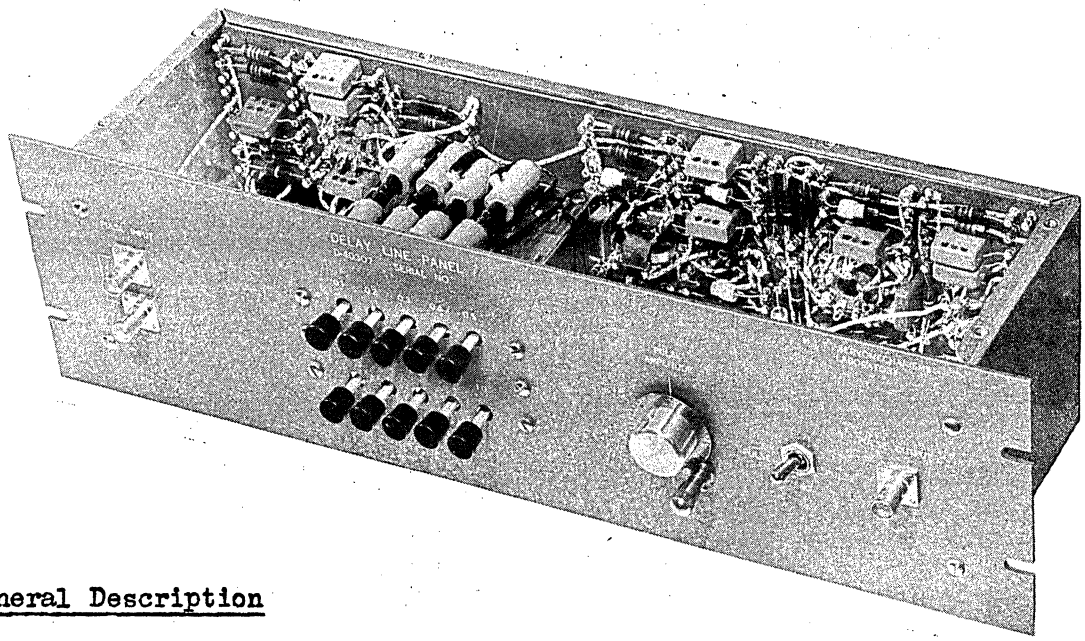
D-50441

CHG. 1 | CK# 3728 | DATE 7/3/52 | APPD. L.S.


D-50441
+250V P1
R7 1750 10W
R6 15
R11 56
V7 VR150
C13a 20
C12 0.01
L1 22 μH
R3 1200 2W
R2 1200 2W
C4 0.5
C5 0.05
C6 0.0047
C7 470 MMFD
C8 47 MMFD
COARSE DELAY
CW
S1
L2 22 μH
R18 1200 2W
R19 1200 2W
+150V P1
R28 180 1W
R27 15
CR2
L3 100 μH
R26 470
C16 0.01
+90V P1
R33 180 2W
R30 0.68 MEG
R32 820
R34 0.22 MEG
CR3
L4 27 μH
R35 270
+250V P1
R40 180 2W
T1 3:1
SEE NOTE 2
CR4
CR5
POLARITY
S2 DPDT
J4
PULSE OUTPUT
- ZERO +
P2 8 PIN JONES PLUG P-308 CCT
MARGINAL CHECKING PLUG
P3 8 PIN JONES SOCKET S-308 AB
J1
J2
INPUT
C1 0.001
V1 5687
R12 56
R25 470
C9 68 MMFD
R17 0.33 MEG 1%
R4 0.75 MEG 1%
V2 5687
R16 56
R24 56
C13b 15
C13c 15
V3 5687
C19 68 MMFD
C20 0.01 MFD
V4 6AG7
CR1
FINE DELAY
R15 10,000
R14 0.2 MEG
CW
R20 2200 1W
R21 1000 2W
C17 0.01
R29 82,000
R31 560 2W
R36 10,000
C23 0.1
PULSE AMPLITUDE
R38 500
C22 0.01
C2 0.01
R42 1000 1W,±5%
TRIGGER TUBE
MULTIVIBRATOR
MULTIVIBRATOR
RLC PEAKER
PULSE STANDARDIZER
OUTPUT AMPLIFIER
C14 0.01
C21 0.01
R1 270 1W,±5%
C10 20 MFD ELECTROLYTIC
C11 0.01 600V
R41 180 1W
R37 180
R13 10,000 2W
P1 -15V
P1 -300V
J3
DELAY M.V. OUTPUT
P1 -30V
P1 -15V
-300V
+90V
-15V
-30V
+150V
+250V
GND
6.3V
6.3V
P1 12 PIN JONES PLUG 2412-CCT
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, 1/2W, ±10%.
B. CAPACITORS ARE IN MICROFARADS.
C. VIDEO CONNECTORS ARE JAN UG-625/U.
D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE IN34A.
2. IF T1 IS A BURROUGHS TYPE PT22 A CRYSTAL & RESISTOR SHOULD BE ADDED TO THE SECONDARY, AS FOLLOWS:
CR
R 180 Ω OR 200 Ω
DRAWING REFERENCES:
1. BURROUGHS EQUIPMENT: PULSE DELAY, TYPE 1301BW DWG. NO. C-10569C.
2. LAMICOID LABELS: A-50597
GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
8-15-52 GRADE III FINAL DESIGN
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING—D. I. C. PROJECT NO. 6889
CIRCUIT SCHEMATIC,
GATE & DELAYED-PULSE GENERATOR, TYPE 1301BW
SCALE:
DR. A.M.G. 7-3-52
ENG. 7-21-52 L.L.S.
CK. 7/14/52
APPD. R L Best
D-50441


D-50441
INPUT
TRIGGER TUBE
MULTIVIBRATOR
RLC PEAKER
PULSE STANDARDIZER
OUTPUT AMPLIFIER
COARSE DELAY
FINE DELAY
PULSE AMPLITUDE
POLARITY
- ZERO +
PULSE OUTPUT
DELAY M.V. OUTPUT
P2 8 PIN JONES PLUG P-308 CCT
MARGINAL CHECKING PLUG
J3 8 PIN JONES SOCKET S-308AB
P1 12 PIN JONES PLUG 2412-CCT
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, ½W ±10%.
B. CAPACITORS ARE IN MICROFARADS.
C. VIDEO CONNECTORS ARE JAN UG-625/U.
D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE IN34A.
2. IF T1 IS A BURROUGHS TYPE PT22 A CRYSTAL & RESISTOR SHOULD BE ADDED TO THE SECONDARY, AS FOLLOWS:
DRAWING REFERENCES:
1. BURROUGHS EQUIPMENT: PULSE DELAY, TYPE 1301BW DWG. NO. C-10569C.
2. LAMICOID LABELS: A-50597
GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
8-15-52
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO. 6889
CIRCUIT SCHEMATIC,
GATE & DELAYED-PULSE GENERATOR, TYPE 13018W
DR. A.M.G. 7-3-52
D-50441

DELAY LINE PANEL



General Description

The delay line panel is used to delay 0.1-microsecond pulses, in steps of 0.1 microsecond, up to a maximum of 1 microsecond. External terminals are provided for adding extra delay lines.

Specifications

Dimensions: 4 1/2 x 5 1/2 x 19 inches.

Delay: 9 delay lines, each 0.1 μsec.
Inherent delay of unit 0.1 μsec.
Terminals on rear of chassis for additional delay lines.

Circuits: 6AG7 input buffer amplifier.
9 delay lines, each 0.1 μsec 1100 ohms, can be switched in series.
1/2 5687 buffer amplifier.
1/2 5687 inverter.
6AG7 R-L-C peaker.
6AG7 output buffer amplifier.

Input: Positive 0.1-μsec half-sine-wave pulse.
Minimum pulse amplitude 8 volts.
Resolution time of equipment 0.45 μsec.

Output: 0.1-μsec pulses, polarity reversible, amplitude variable up to 36 volts with a 15-volt input pulse. Output circuit is transformer coupled to match 93 ohms.

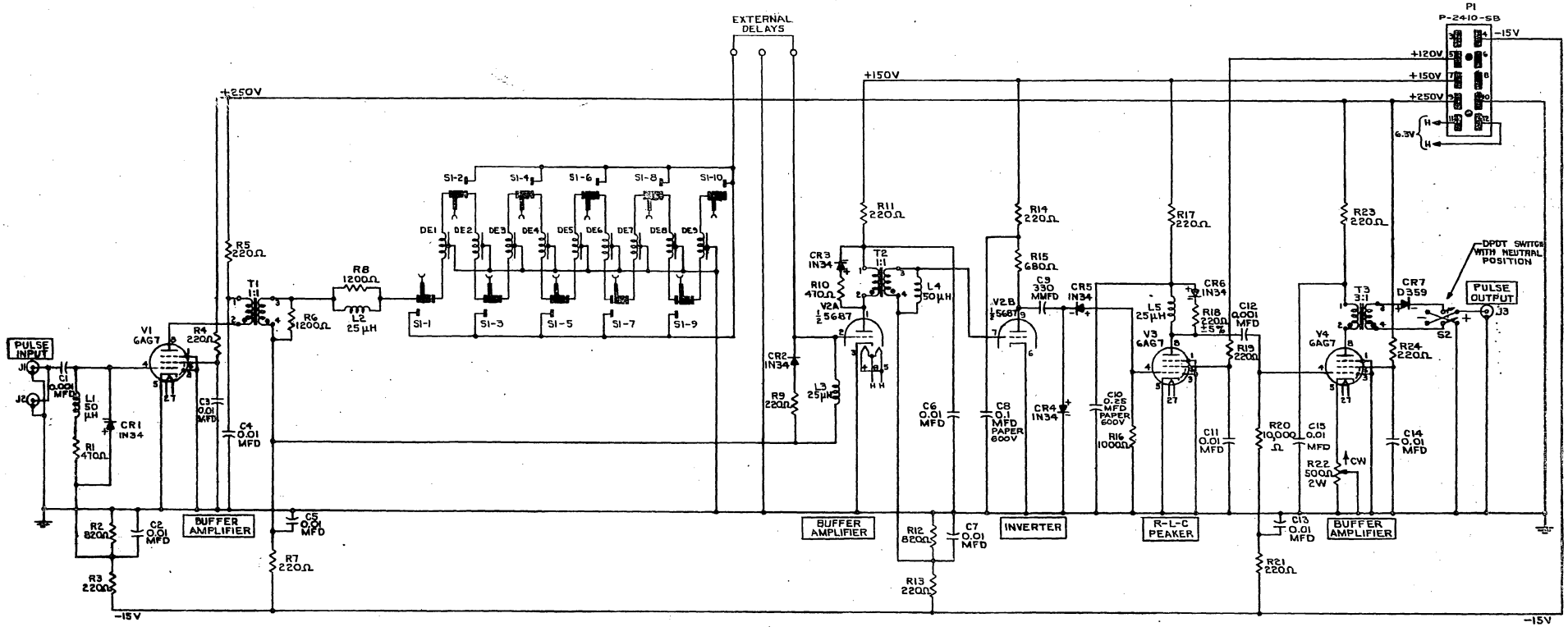
Power Requirements:

Voltages	Currents	
	No Sig.	1-mc input
- 15 v d.c.	28 ma	25 ma
+120 v d.c.	11 ma	11 ma
+150 v d.c.	46 ma	62 ma
+250 v d.c.	9 ma	29 ma
6.3 v a.c.	2.85 amp	2.85 amp

References

Photograph: F-689
Circuit Schematic: D-40307

D-40307-3



NOTES:

UNLESS OTHERWISE SPECIFIED, THE FOLLOWING SHALL APPLY TO ALL COMPONENTS IN THIS SCHEMATIC:

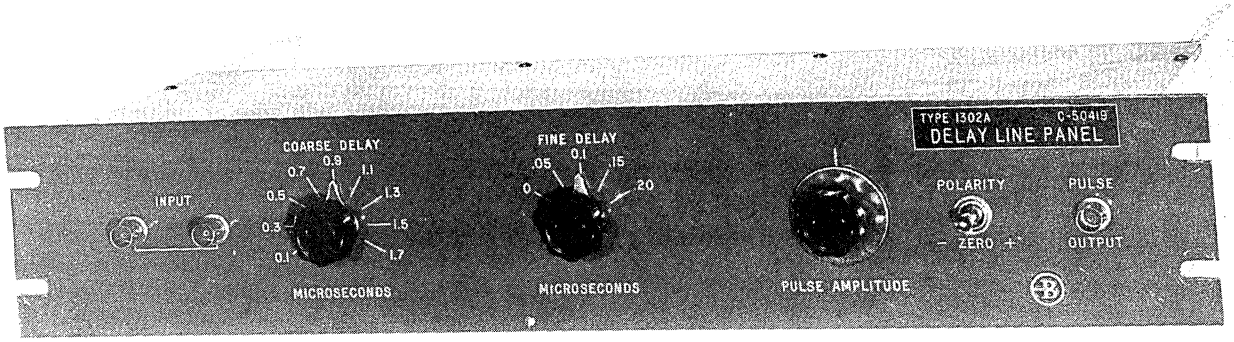
1. ALL RESISTORS ARE JAN SPEC. COMPOSITION, TYPE, 1W, ±10%.
2. ALL CAPACITORS ARE JAN SPEC, MICA, ±10%.
3. ALL VIDEO CONNECTORS ARE UG-290/U.
4. ALL DELAY LINES ARE 0.1 µSEC, 1100Ω.

DRAWING REFERENCES:

1. ASSEMBLY: C-33202
2. AL. PANEL: C-33200
3. AL. CHASSIS: C-33201
4. PHENOLIC PANEL: C-33203
5. SWITCH ASSEMBLY: C-36094

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
RADIATION LABORATORY
CIRCUIT SCHEMATIC, DELAY-LINE PANEL
D.L.S. 12-10-47
D-40307-3

Burroughs'
DELAY LINE PANEL
(Type 1302 A or AW)



General Description

This unit delays 0.1-μsec pulses by means of a tapped delay line in 0.05-μsec steps from 0.1 to 1.9 μsec. It is designed to receive 0.1-μsec pulses with a minimum amplitude of 13 volts. The output pulse polarity is reversible and its amplitude may be varied from 10 to 32 volts.

Specifications

Construction:	Panel and chassis
Dimensions:	3-1/2 x 19 inches Depth 10 inches
Circuit:	6AG7 Input amplifier 6AG7 Amplifier 6AG7 Inverter 6AG7 Peaker 6AG7 Buffer amplifier

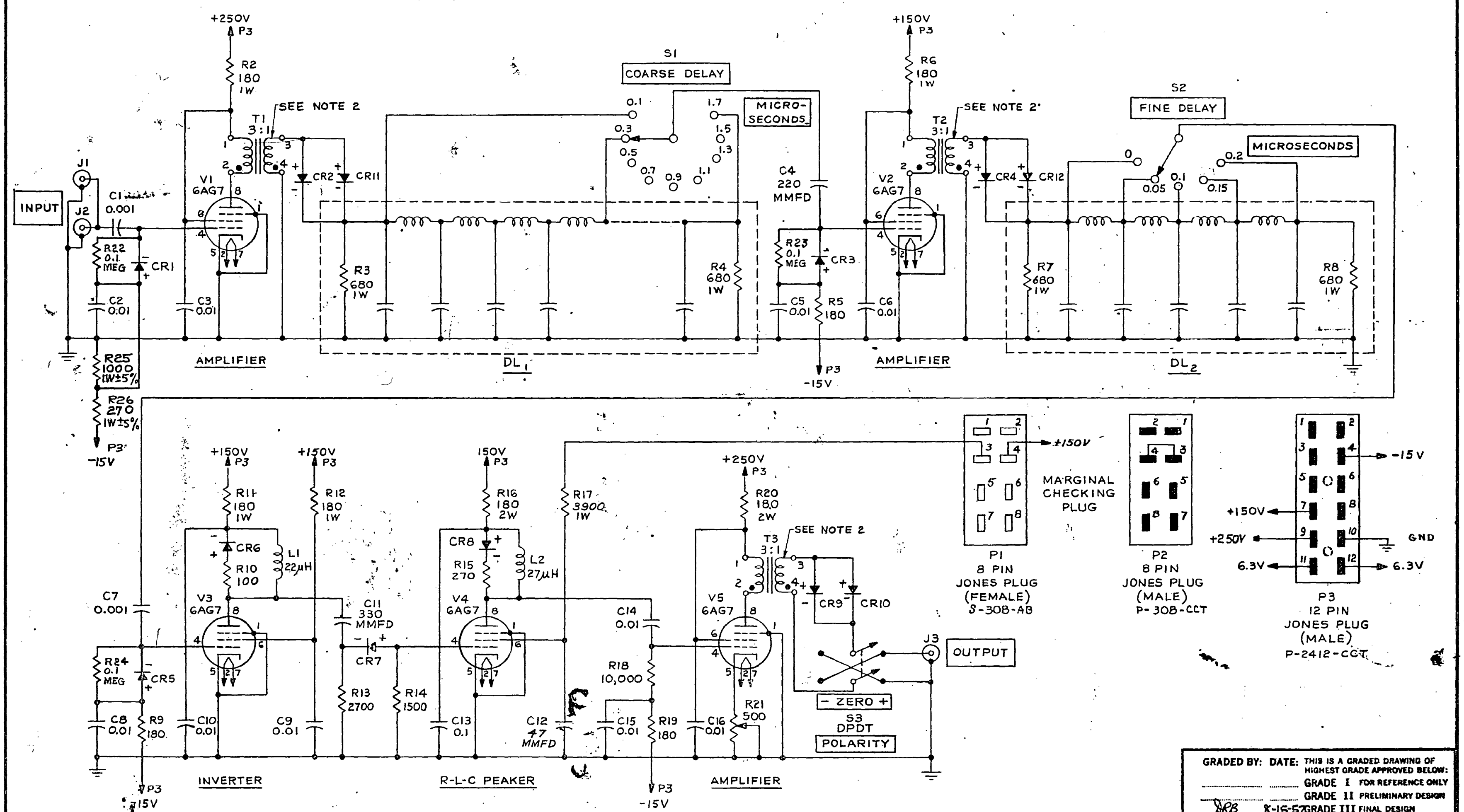
Power Requirements:

+250 volts d-c	69 ma
+150 volts d-c	112 ma
+120 volts d-c	20 ma
- 15 volts d-c	12 ma
6.3 volts a-c	3.25 amps

References

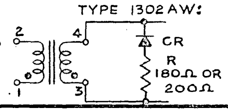
Circuit Schematic	C-50419-1
Engineering Note	E-434
Photograph	F-1558

C- 50419


INPUT
J1
J2
C1 0.001
R22 0.1 MEG
CR1
C2 0.01
R25 1000 1W±5%
R26 270 1W±5%
P3 -15V
+250V P3
R2 180 1W
SEE NOTE 2
T1 3:1
V1 6AG7
C3 0.01
CR2
CR11
AMPLIFIER
S1
COARSE DELAY
MICRO-SECONDS
R3 680 1W
R4 680 1W
DL1
C4 220 MMFD
R23 0.1 MEG
CR3
C5 0.01
R5 180
P3 -15V
+150V P3
R6 180 1W
SEE NOTE 2
T2 3:1
V2 6AG7
C6 0.01
CR4
CR12
AMPLIFIER
S2
FINE DELAY
MICROSECONDS
R7 680 1W
R8 680 1W
DL2
+150V P3
R11 180 1W
CR6
R10 100
L1 22μH
+150V P3
R12 180 1W
C7 0.001
V3 6AG7
R24 0.1 MEG
CR5
C8 0.01
R9 180
C10 0.01
C9 0.01
P3 -15V
INVERTER
C11 330 MMFD
CR7
R13 2700
R14 1500
150V P3
R16 180 2W
CR8
R15 270
L2 27μH
V4 6AG7
C13 0.1
R17 3900 1W
C12 47 MMFD
R-L-C PEAKER
C14 0.01
R18 10,000
C15 0.01
R19 180
P3 -15V
+250V P3
R20 180 2W
SEE NOTE 2
T3 3:1
V5 6AG7
C16 0.01
R21 500
CR9
CR10
AMPLIFIER
- ZERO +
S3 DPDT
POLARITY
J3
OUTPUT
+150V
MARGINAL CHECKING PLUG
P1 8 PIN JONES PLUG (FEMALE) S-308-AB
P2 8 PIN JONES PLUG (MALE) P-308-CCT
-15V
+150V
GND
+250V
6.3V
6.3V
P3 12 PIN JONES PLUG (MALE) P-2412-CCT

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
DRB 8-15-52 GRADE III FINAL DESIGN

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, ½W, ±10%
   B. CAPACITORS ARE IN MICROFARADS.
   C. VIDEO CONNECTORS ARE JAN. UG-625/U
   D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE IN34A
2. IF T1, T2, AND T3 ARE A BURROUGHS TYPE PT 22, A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:



DRAWING REFERENCES:
1. LAMICOID LABEL: A-50605
2. BURROUGHS EQUIPMENT; PULSE DELAY, TYPE 1302AW: C-10568B

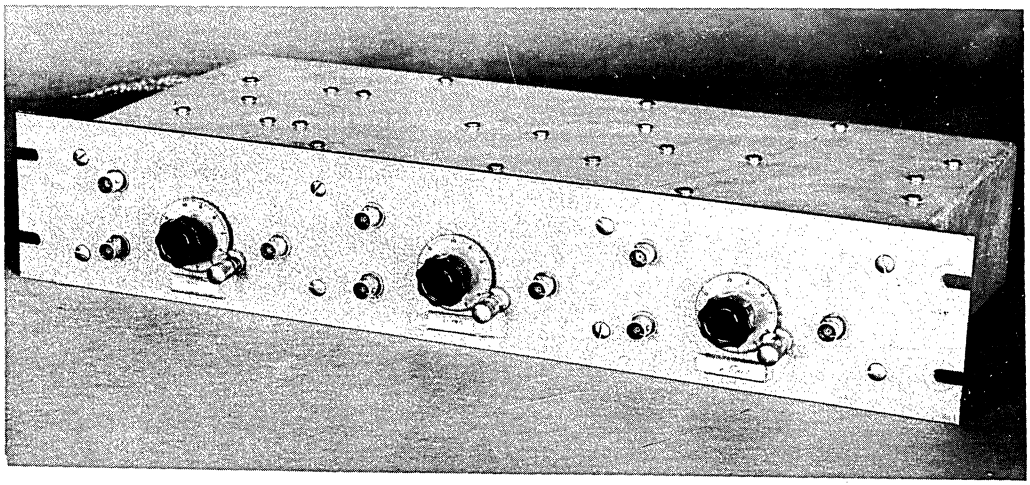
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING—D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC,
DELAY LINE PANEL, TYPE 1302AW

SCALE: —— DR. F. B. JUNE 27 '52
ENG. 7/21/52 L.L.S. CK. 7/14/52 R.B.B. APPD. 8/11/52 RLBest

C- 50419

THREE CHANNEL DELAY PANEL



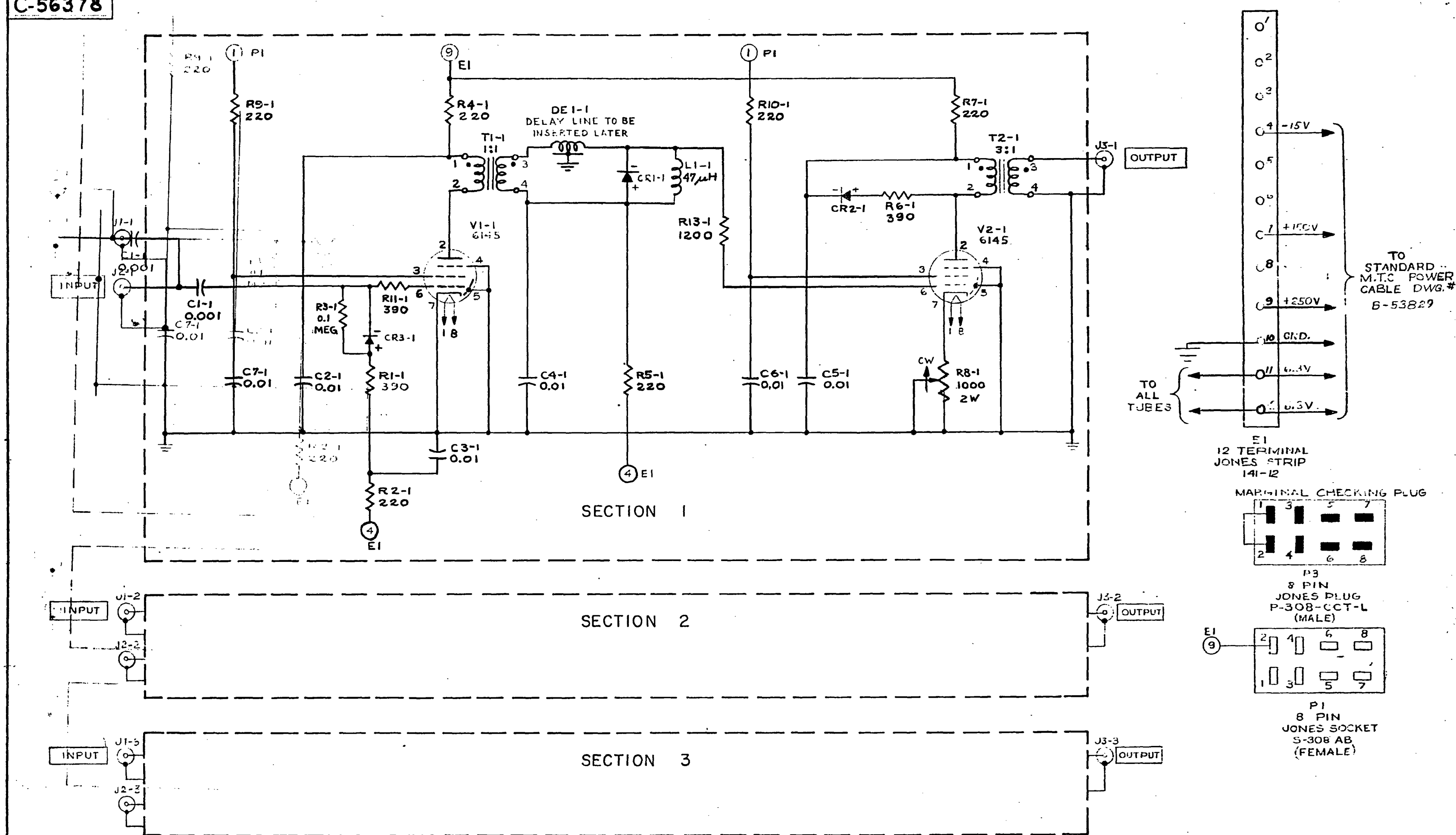
General Description

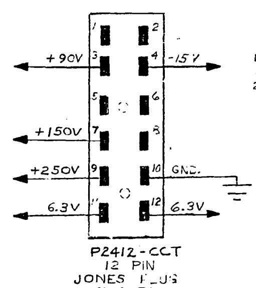
This unit contains 3 identical pulse delay circuits, each consisting of a delay line (whose length may be chosen by the user to be between 0.1 and 2.0 usec) with an input and an output buffer amplifier. A variety of suitable delay lines are available at test equipment headquarters.

Specifications:

Dimensions:	3 1/2 x 19, depth 10 1/2 in.
Inputs:	Positive 0.1-usec. Pulses 15 to 40 volts in amplitude up to 4 mc; one input for each channel.
Outputs:	Positive 0.1-usec pulses variable in amplitude between 5 and 30 volts up to 2 mc (gain becomes less at higher prf); one output for each channel.
Controls:	One gain control for each channel.
Circuit:	3 6145 input buffer amplifiers 3 6145 output buffer amplifiers
Power:	+250 vdc 30 ma/mc/channel } at 30 volt input -15 vdc 0.6 ma/mc/channel } and output 93-ohm loads. 6.3 vac 3.6 amps
References:	Circuit Schematic C-56378

C-56378


SECTION 1
SECTION 2
SECTION 3
INPUT
OUTPUT
DE1-1 DELAY LINE TO BE INSERTED LATER
T1-1 1:1
T2-1 3:1
V1-1 6145
V2-1 6145
R9-1 220
R4-1 220
R10-1 220
R7-1 220
R13-1 1200
R6-1 390
R11-1 390
R3-1 0.1 MEG
R1-1 390
R2-1 220
R5-1 220
R8-1 1000 2W
C1-1 0.001
C7-1 0.01
C2-1 0.01
C3-1 0.01
C4-1 0.01
C6-1 0.01
C5-1 0.01
L1-1 47μH
CR1-1
CR2-1
CR3-1
TO STANDARD M.T.C POWER CABLE DWG.# B-53829
TO ALL TUBES
E1 12 TERMINAL JONES STRIP 141-12
MARGINAL CHECKING PLUG
P3 8 PIN JONES PLUG P-308-CCT-L (MALE)
P1 8 PIN JONES SOCKET S-308 AB (FEMALE)



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A RESISTORS ARE IN OHMS, ½W ±10%
   - B. CAPACITORS ARE IN MICROFARADS.
   - C. VIDEO CONNECTORS ARE JAN UG 625/U
   - D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. STAGES 2 & 3 ARE IDENTICAL WITH STAGE 1, EXCEPT FOR COMPONENT NUMBER SUFFIXES. FOR EXAMPLE, THE TUBE V1-1 6145 IN STAGE 1 IS V1-3, 6145 IN STAGE 3.
3. VALUE OF DELAY LINES WILL BE DETERMINED WHEN UNIT IS USED.

DRAWING REFERENCES:
1. ASSEMBLY: D-56379
2. PARTS LIST: PL-[illegible]

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN

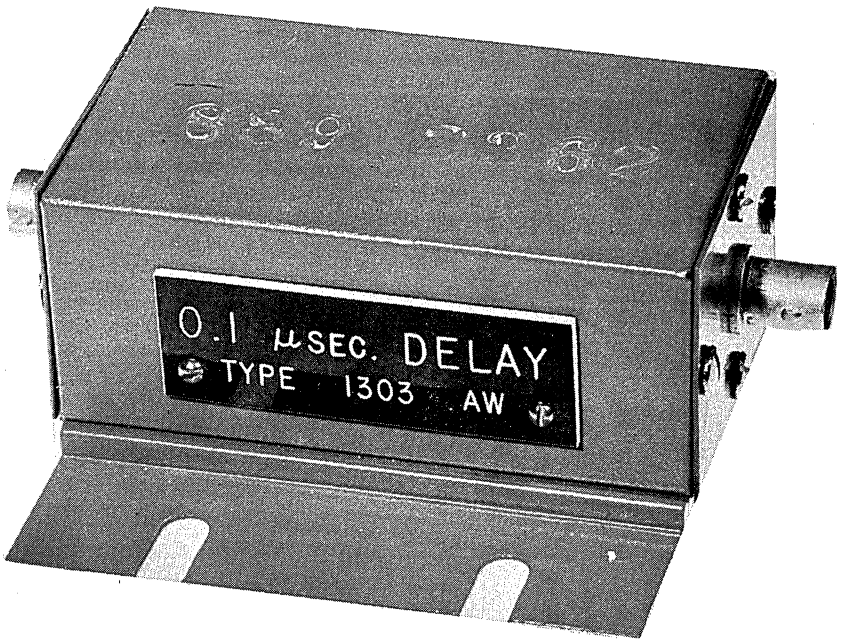
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING—D. I. C. PROJECT NO. 6689

CIRCUIT SCHEMATIC,
THREE CHANNEL DELAY PANEL, TE

SCALE: | DR | ENG. L Sulro | CK | APPD. L Sulro

C-56378

Burroughs'
0.1-μSEC DELAY
(Type 1303 AW)



General Description

This unit provides a fixed delay of 0.1 μsec, with a signal attenuation of less than 5%. The balanced system network has an impedance of 93 ohms and permits either jack to be used as input or output. The unit can resolve 0.1-μsec pulses having a period of 0.3 μsec.

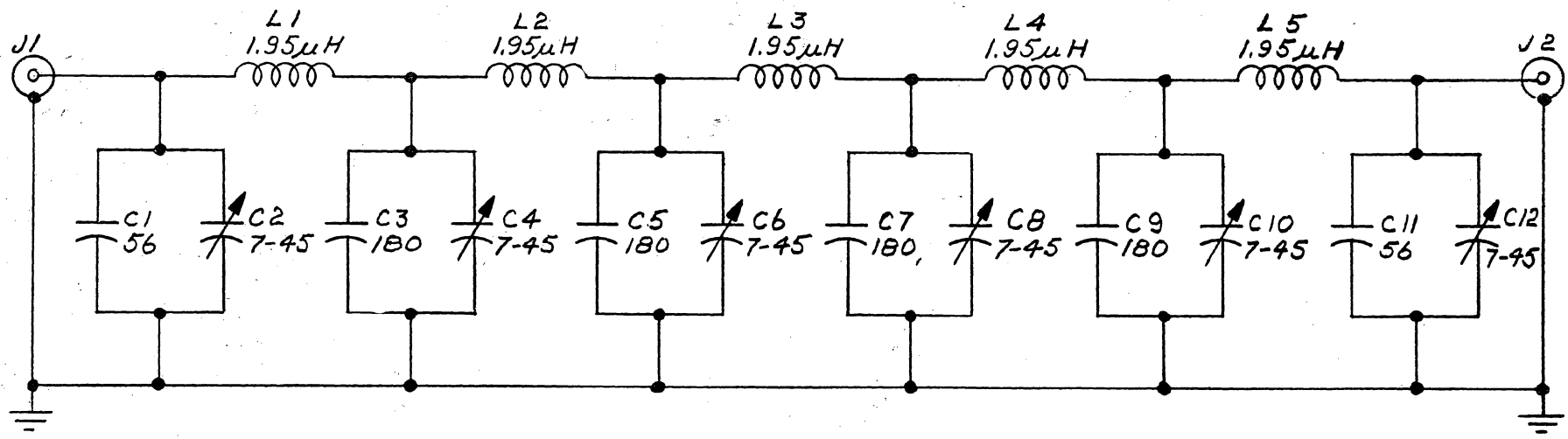
Specifications

Construction:	Metal box with mounting flange
Dimensions:	4-1/2 x 3 x 1-3/4 inches overall, including a 3-1/2 x 1 inch mounting flange
Power Requirements:	None

References

Circuit Schematic A-52057

A-52057



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. CAPACITORS ARE IN MICROMICROFARADS.
   B. VIDEO CONNECTORS ARE JAN UG-625/U.

DRAWING REFERENCES:

1. BURROUGHS EQUIPMENT: PULSE DELAY, TYPE 1303AW, DWG. NO. A-11719-A.
2. LAMICOID LABEL: A-53668

GRADED BY. DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
DRB 8-15-52 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
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-3			
-2			
-1	4627	1-28-53	L. Sutro

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC, 0.1 μ sec DELAY, TYPE 1303 AW.

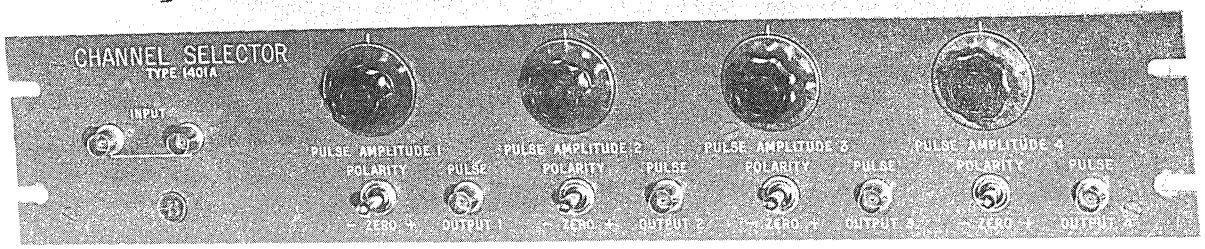
SCALE: _____ DR. R.B.B. 8-7-52

ENG. 2/11/52 L. Sutro | CK. W Cook 8-11-52 | APPD. 8/11/52 RL Best

A-52057 MN

K-E ALBANENE 1961

Burroughs'
CHANNEL SELECTOR
(Type 1401 A)



General Description

This unit accepts a 0.1-μsec pulse at its input, standardizes it, and feeds it to four buffer amplifiers which drive four output jacks. Each output has its own gain control and 3-position selection switch. The center position of the switch (ZERO) disconnects the jack from the output circuit; the two outside positions reverse the polarity of the output pulse. The inherent delay is 0.08 μsec, and resolution time is less than 0.5 μsec.

Specifications

Construction: Panel and chassis

Dimensions: 3-1/2 x 19 inches
Depth 10 inches

Circuit: 6AG7 Inverter
6AG7 Peaker
6AG7 Buffer Amplifier
4 - 6AG7's Output Amplifiers

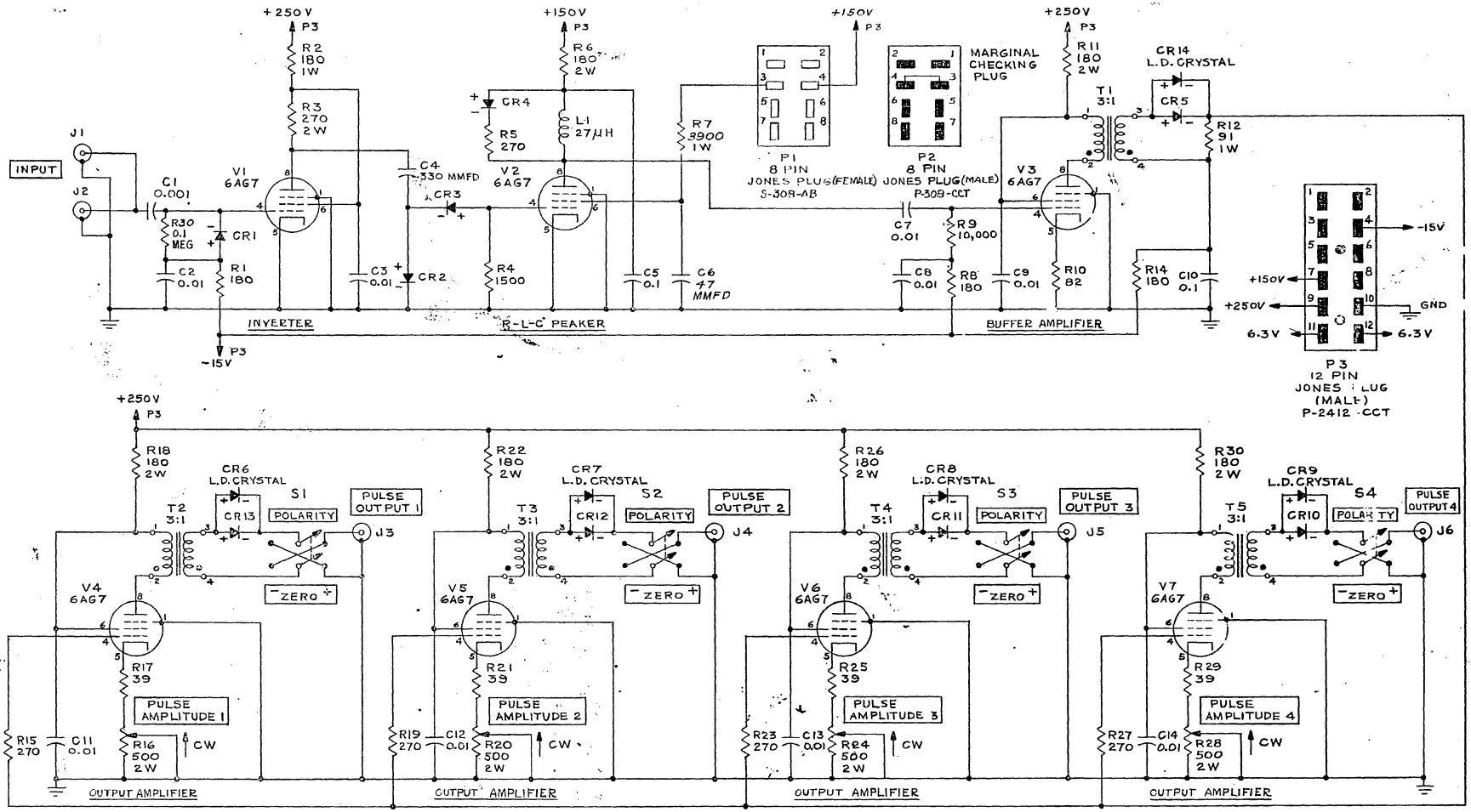
Power Requirements:

+250 volts d-c	120 ma
+150 volts d-c	44 ma
+120 volts d-c	15 ma
- 15 volts d-c	5.8 ma
6.3 volts a-c	4.55 amps

References

Circuit Schematic C-50415
Engineering Note E-434
Photograph F-1559

C-50415



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, ½W ±10%
   B. CAPACITORS ARE IN MICROFARADS
   C. VIDEO CONNECTORS ARE JAN UG-625/U
   D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A

DRAWING REFERENCES:
1. BURROUGHS EQUIPMENT: CHANNEL SELECTOR, TYPE 1401A DWG. NO. B-10564 B
2. LAMICOID LABEL A-50599

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
8-15-52 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-10	4610	7-7-52	
-9	3723	7-7-52	

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DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

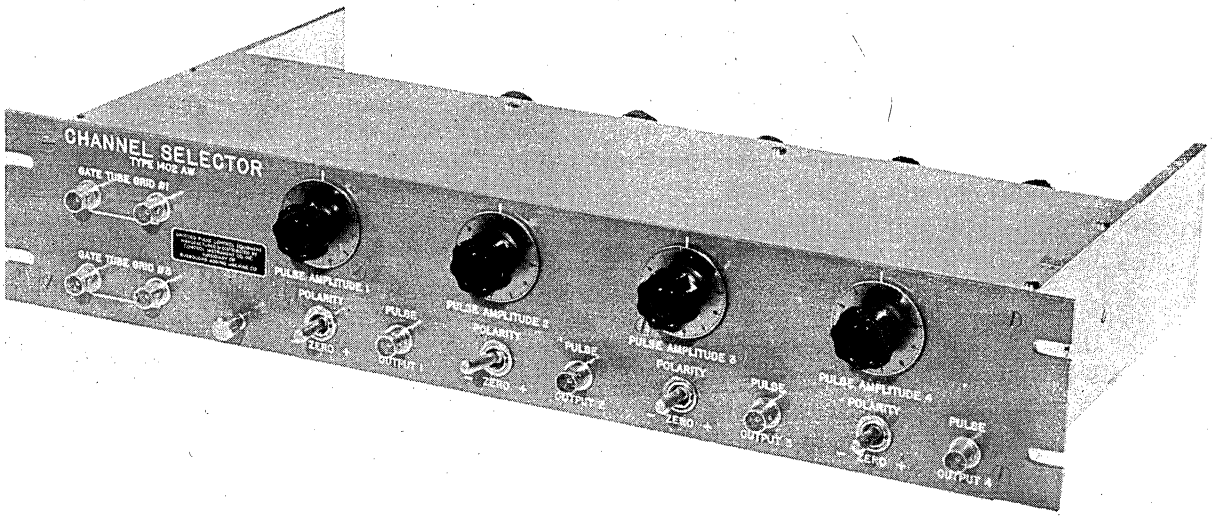
CIRCUIT SCHEMATIC
CHANNEL SELECTOR, TYPE 1401A

SCALE: —— DR. R.B. 7-7-52

ENG. 7/21/52 L.L.S. CK. 7/14/52 R.B.B. APPD. 8/11/52 R.L.B.

C-50415

Burroughs'
GATED CHANNEL SELECTOR
(Type 1402 AW)



General Description

The first stage of the Gated Channel Selector is a read-in gate tube which will pass 0.1-μsec pulses at its #1 grid input (G1) only when a gating voltage is applied simultaneously to its #3 grid input (G3). After this initial stage the operation is as described for Channel Selector Type 1401 A.

Specifications

Construction:	Panel and chassis	
Dimensions:	3-1/2 x 19 inches Depth 10 inches	
Circuit:	7AK7	Gate Tube
	6AG7	Peaker
	6AG7	Buffer Amplifier
	4 - 6AG7's	Output Amplifier

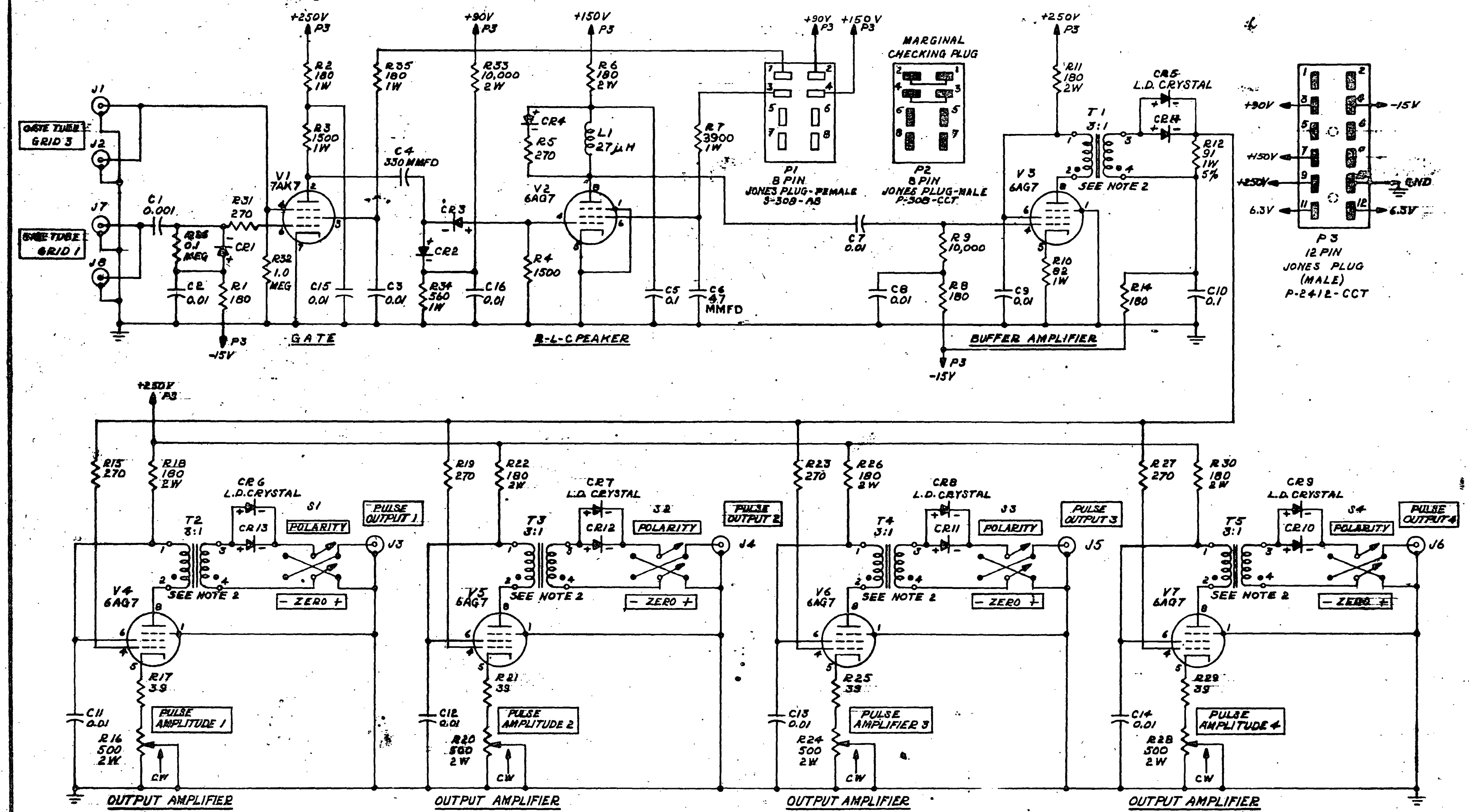
Power Requirements:

+250 volts d-c	120 ma
+150 volts d-c	44 ma
+120 volts d-c	15 ma
+ 90 volts d-c	2 ma
- 15 volts d-c	5.8 ma
-150 volts d-c	
6.3 volts a-c	4.55 amp

References

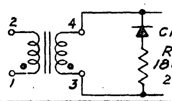
Circuit Schematic C-52059

C-52059



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTORS ARE IN OHMS, ½W, 10%.
   - B. CAPACITORS ARE IN MICROFARADS.
   - C. VIDEO CONNECTORS ARE JAN UG-625/U.
   - D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE IN34A.
2. IF T1 THRU T5 ARE A BURROUGHS TYPE PT22, A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:



DRAWING REFERENCES:

1. BURROUGHS EQUIPMENT: CHANNEL SELECTOR, TYPE 1402AW : DWG. NO. B-11725-A.
2. ASSEMBLY & PL : R-53325

GRADED BY: RRB DATE: 8-15-52 — THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW: GRADE I FOR REFERENCE ONLY; GRADE II PRELIMINARY DESIGN; GRADE III FINAL DESIGN

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DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

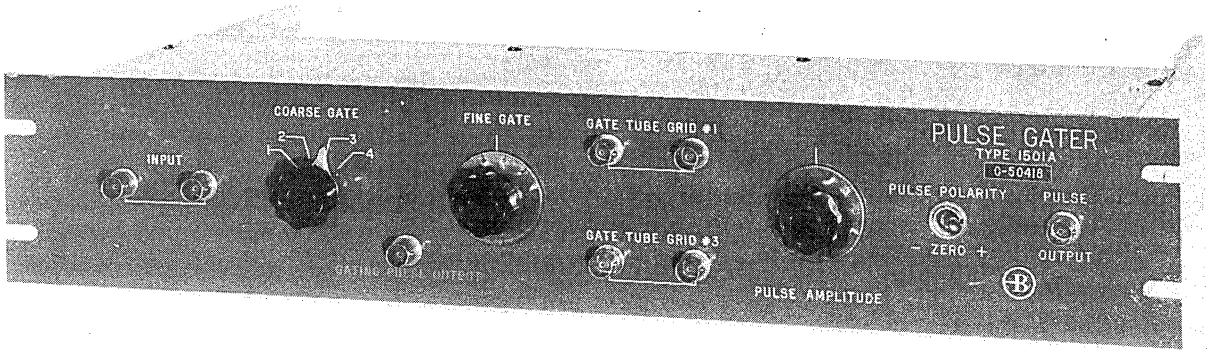
CIRCUIT SCHEMATIC, GATED CHANNEL SELECTOR, TYPE 1402 AW

SCALE: — DR. R.B.B. 8-6-52

ENG. 8/12/52 L. Sutro | CK. 8/11/52 | APPD. 8/12/52 RL Best

C-52059

Burroughs' PULSE GATER (Type 1501 A or AW)



General Description

The pulse gater consists of a gate generator and a gate tube circuit mounted on one 3-1/2-inch panel. Either section may be used independently of the other.

The gate may be varied from 0.3 to 5000 μsec in four overlapping ranges, is d-c coupled to its output jack, and swings from -30 volts in stand-by to 0 volts during the gate. Although the gate generator has neither the stability nor the low output impedance of the Gate and Delayed-Pulse Generator (Type 1302 AW), it is adequate for generating chains of pulses when connected to the gate tube circuit. The gate tube circuit is identical with those described for the Gate Tube Panel (Type 1201 AW).

Specifications

Construction: Panel and chassis

Dimensions: 3-1/2 x 19 inches
Depth 10 inches

Circuit: 12AV7 Multivibrator
7AK7 Gate Tube
6AG7 Pooker
6AG7 Buffer Amplifier

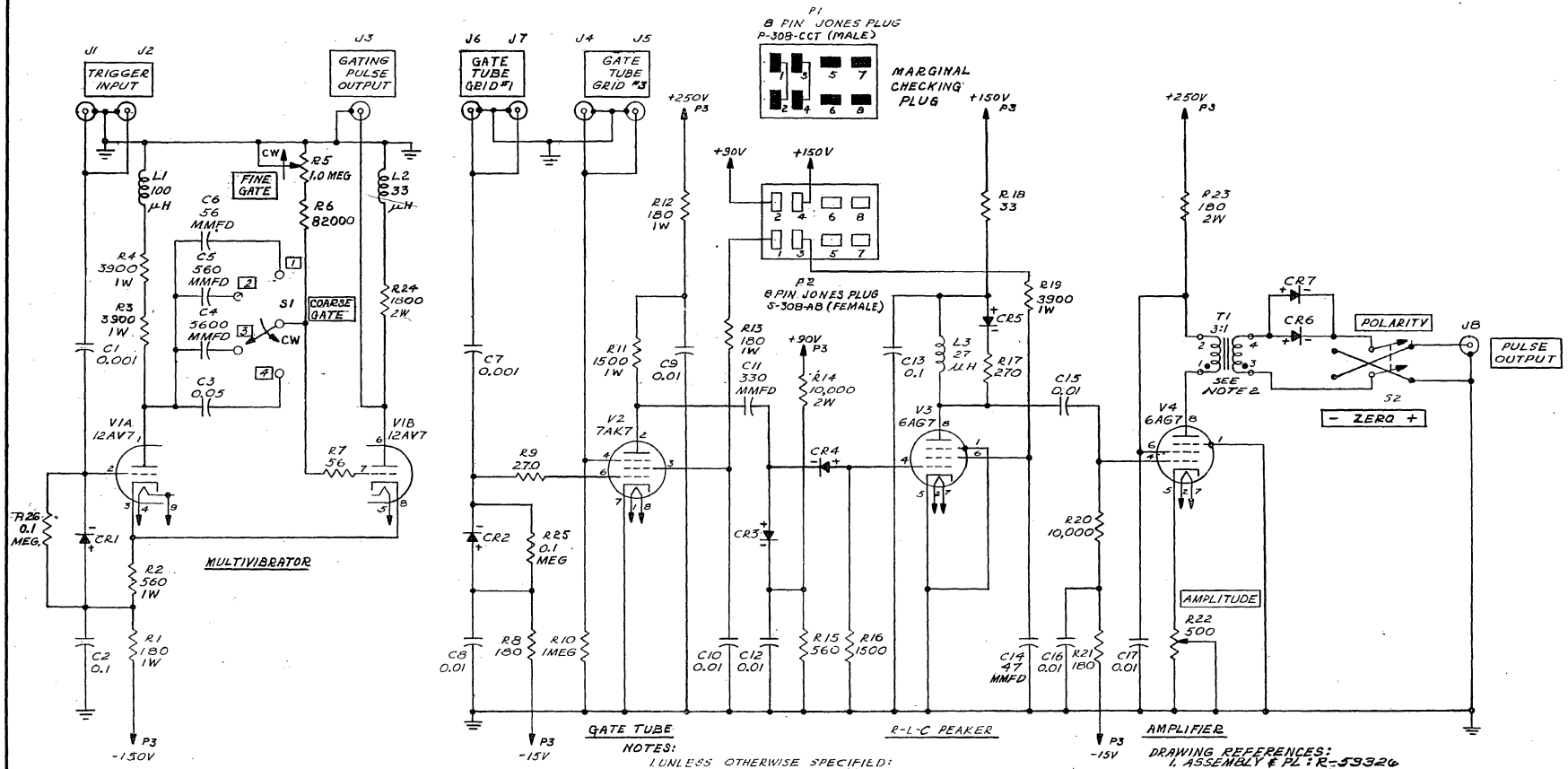
Power Requirements:

+250 volts d-c	30 ma
+150 volts d-c	35 ma
+120 volts d-c	15 ma
+ 90 volts d-c	10 ma
- 15 volts d-c	3.5 ma
-150 volts d-c	20 ma
6.3 volts a-c	3.55 amps

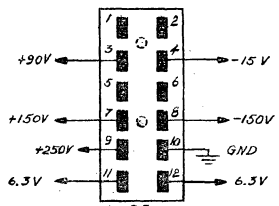
References:

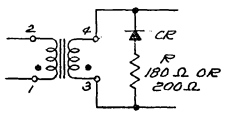
Circuit Schematic	C-50418
Engineering Note	E-434
Photograph	P-1560

C-50418



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS; ½W, ±10%.
B. CAPACITORS ARE IN MICROFARADS.
C. VIDLO CONNECTORS ARE JAN UG-625/U.
D. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. IF T1 IS A BURROUGHS TYPE PT 22, A CRYSTAL AND RESISTOR SHOULD BE ADDED TO THE SECONDARY AS FOLLOWS:





DRAWING REFERENCES:
1. ASSEMBLY & PL: R-53326
2. LAMICOID LABEL: A-50607
3. BURROUGHS EQUIPMENT; PULSEGATER TYPE 1501A (WW) DWG. NO. C-10566A

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
_____ _____ GRADE I FOR REFERENCE ONLY
_____ _____ GRADE II PRELIMINARY DESIGN
JWB 8-15-52 GRADE III FINAL DESIGN

CHK	DATE	APPD.
-10		
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-3	4612 7-28-52	J.W.F.
-2	4002 8-25-52	J.S.M.
-1	3726 6-25-52	L.S.

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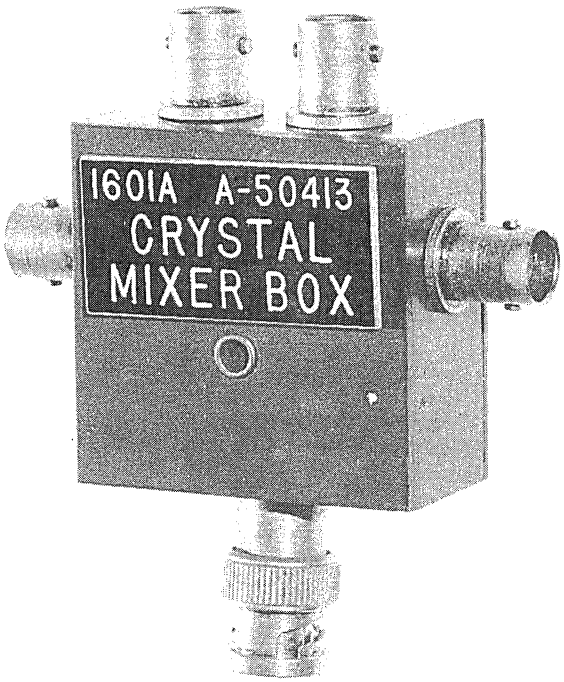
CIRCUIT SCHEMATIC,
PULSE GATER, TYPE 1501AW

SCALE: ____ DR. J.B.N. 6-25-52

ENG. 7/2/52 L.L.S. CK. R.I.B. 8-4/21/52 APPD. 8/11/52 R.L.R. Jr.

C-50418

Burroughs'
CRYSTAL MIXER BOX
(Type 1601 A or AW)



General Description

The crystal mixer box has four input jacks which feed a common output through crystal diodes. It is designed for mixing positive pulses. The unit can resolve 0.1-μsec pulses having periods of 0.5 μsec when the load is no greater than 50 mmf.

Specifications

Construction: Independent box not mounted

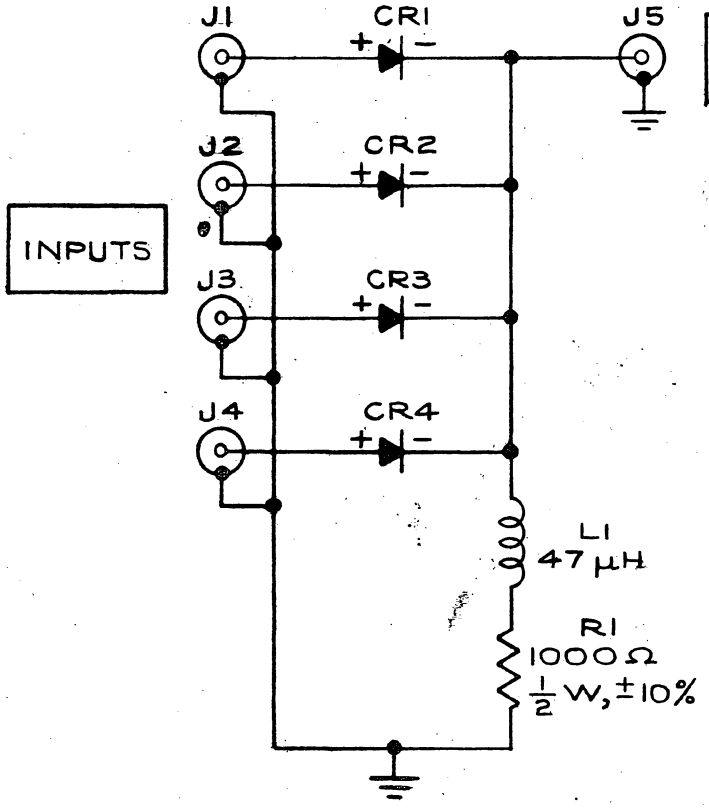
Dimensions: 2-1/2 x 2-1/2 x 1 inch overall

Power Requirements: None

References

Circuit Schematic A-50413
Engineering Note E-434
Photograph F-1561

A-50413



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. VIDEO CONNECTORS ARE JAN UG-625/U
   B. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.

DRAWING REFERENCES:
1. BURROUGHS EQUIPMENT; MIXER, TYPE 1601A(WW) DWG. NO. A-10561A
2. LAMICOID LABEL: A-50614.

GRADED BY:	DATE:	THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
		GRADE I FOR REFERENCE ONLY
		GRADE II PRELIMINARY DESIGN
[illegible]	8-5-52	GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
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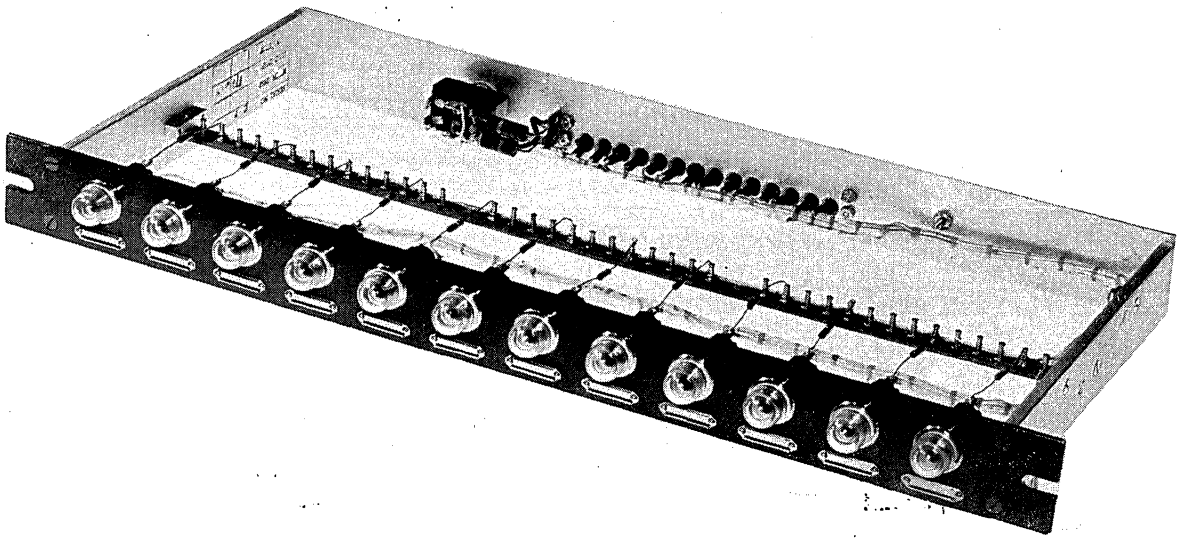
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC,
CRYSTAL MIXER BOX, TYPE 1601AW

SCALE: ——	DR. M.M. 7-7-52	
ENG. 7/21/52 L.L.S.	CK. R.B.B. 7-7-52	APPD. 8/11/52 R L Best

A-50413

Burroughs'
REMOTE INDICATOR
(Type 8201 AW)



General Description

This unit is designed to provide a centralized remote monitoring point for FF's. The position of each FF can be visually determined by observing whether the lamp connected to it is on or off.

Twelve NE51 neon lamps are mounted on the panel. Either one or two lamps may be used per FF at operator's choice. A switch permits selection of either +90 or +250 volts. +90 is used with Flip-Flop (1103 A) when lights are being driven by the flip-flop; +250 is used when lights are being driven by the D-C coupled Register Panel.

Specifications

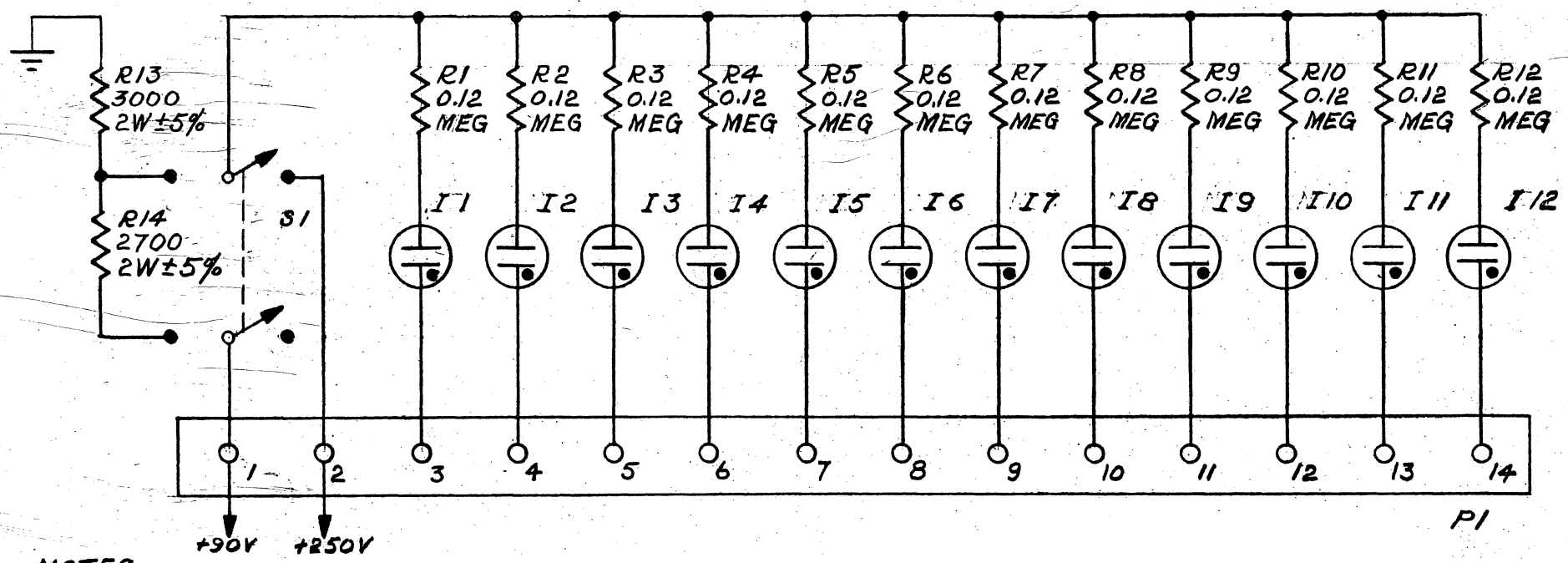
Construction:	Panel and chassis
Dimensions:	1-3/4 x 19 inches Depth 9 inches

References

Circuit Schematic A-52056

A-52056

P



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS, ½W, ±10%
   B. VIDEO CONNECTORS ARE JAN UG-625/U
2. I1 THRU I12 ARE NE51, NEON PILOT LAMPS

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:

.... GRADE I FOR REFERENCE ONLY

.... GRADE II PRELIMINARY DESIGN

RRB 8-15-52 GRADE III FINAL DESIGN

DRAWING REFERENCES:

1. BURROUGHS EQUIPMENT: REMOTE INDICATOR PANEL, TYPE 8201AW, DWG. #A-11736-A.

CHG.	CN#	DATE	APPD.
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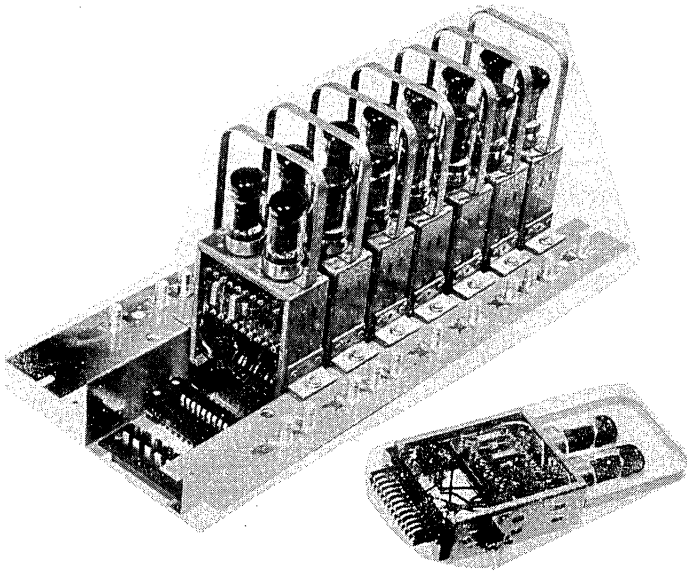
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC, REMOTE INDICATOR PANEL, TYPE 8201AW

SCALE: ———	DR. R.B.B. 8-7-52	
ENG. 8/11/52 L. Sutro	CK. W Cook 8-11-52	APPD. 8/11/52 RL Best

A-52056 P

PLUG-IN UNITS
and
PLUG-IN-UNIT MOUNTING PANEL



PLUG-IN UNITS

General Description

This Section presents descriptions, data, and circuit schematics of plug-in-type test equipment. Plug-in units contain the essential elements of the larger units of test equipment presented in other sections of this Report. Units of this type are intended for semipermanent systems of test equipment in which pulse standardizers and adjustments of amplitude and polarity are not needed. Blank chassis are available for the construction of nonstandard plug-in units.

Specifications

Construction: Plug-in chassis

Dimensions: 3-3/4 x 1-5/8 inches
Depth 9-1/4 inches

PLUG-IN-UNIT MOUNTING PANEL

General Description

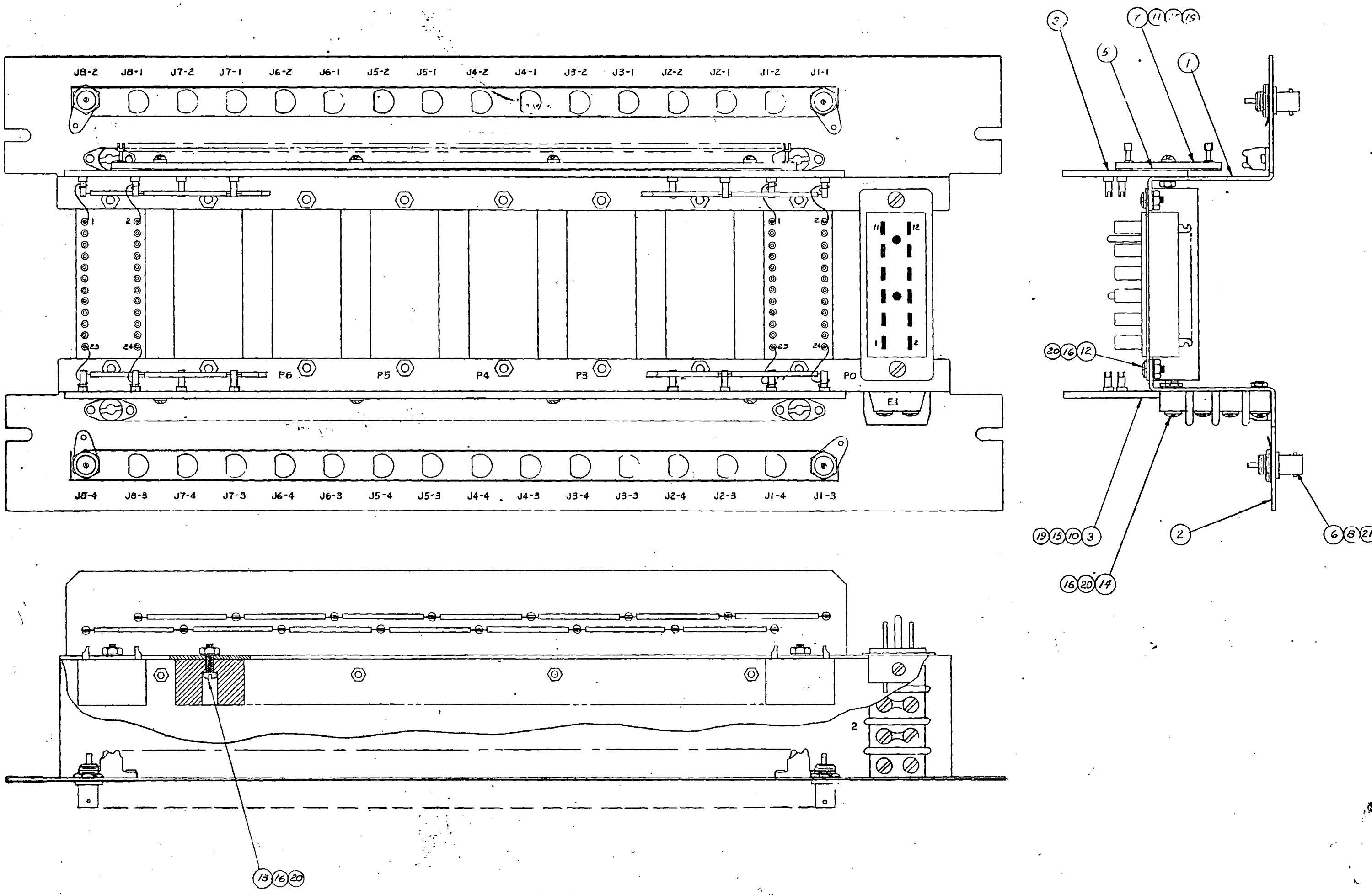
The mounting panel contains eight 24-pin connectors which support plug-in units. The following voltages are wired to these connectors: 6.3 AC, -15, -150, ground, +90, and +250. On the face of the panel are 32 BNC connectors. On the top surface, at the back of the panel, is a phenolic strip with 70 lugs on which a passive network can be assembled.

Specifications

Construction: Two pieces of sheet metal held together by the eight connectors and a Jones plug

Dimensions: 8-1/2 x 19 inches
Depth 4 inches

D-51029



DRAWING REFERENCES:
1. CIRCUIT SCHEMATIC: C-51028
2. PARTS LIST: PL-51029

CHG.	DATE	APPR.	
4581	1/23/53		
9959	9/20/5?		
3705	7/26/52		

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DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO. 6889

ASSEMBLY, PLUG-IN UNIT
MOUNTING PANEL, TEST EQUIPMENT

SCALE: FULL | DR. 3-13-52 | ENG. 3/11/52 | CK. 3-28-52 | APPD. 3-31-52

D-51029

Plug-In
GATE-TUBE UNIT, MOD II
(GT-GT)

General Description

This unit consists of two independent gate-tube circuits mounted on a single plug-in chassis. V1, the read-out gate tube, has a transformer output to provide positive or negative pulses for the transfer of information from a flip-flop into a bus or other low-impedance load. V2, the read-in gate tube, uses capacitive coupling to provide only negative pulses for the transfer of information into a flip-flop or other high-impedance load. Prf sensitivity of the latter circuit is negligible up to about 2 mc.

Specifications

Input: Positive standard pulses of 15-v to 30-v amplitude; d-c levels of 0 volts or positive to turn the gate "on", -15 volts or more negative to turn the gate "off."

Output: With the suppressor at 0 volts, V1 gives positive or negative pulses of about 7 volts into a 100-ohm line; V2 gives pulses of about 12-v amplitude into the grid of a flip-flop tube. More output will be realized if the suppressor is held positive with respect to ground.

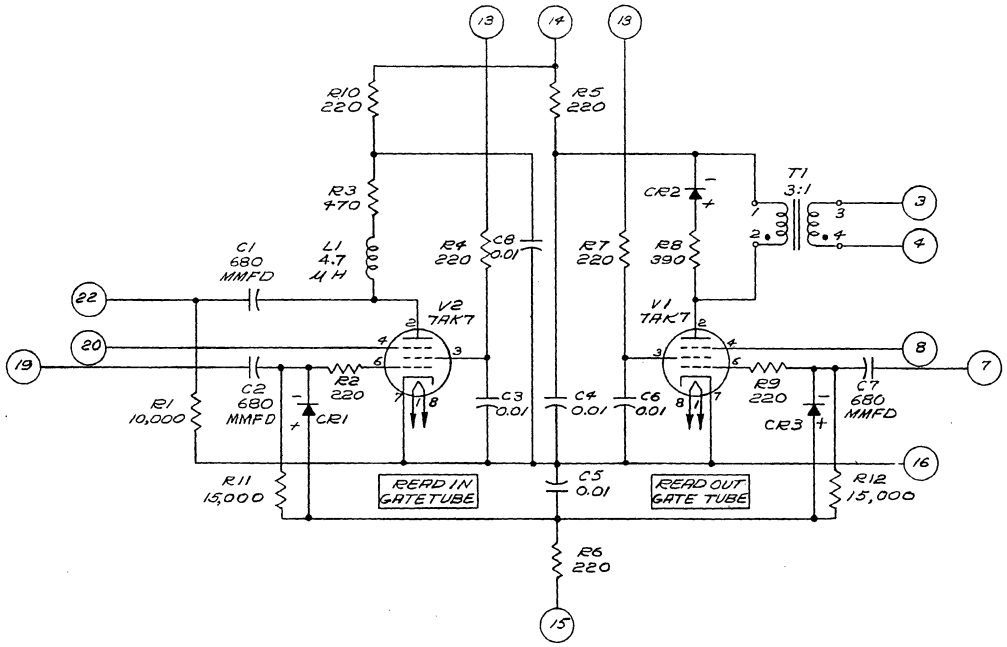
Power Requirements:

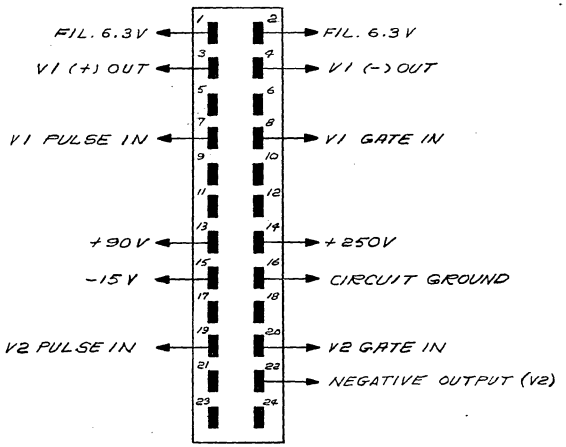
Voltage	Current to One Tube
+250-v DC	approx. 0.2 ma plus 6 ma per mc of prf
+ 90-v DC	approx. 5 ma per mc of prf
- 15-v DC	approx. -1 ma per mc of prf
6.3-v AC	1.6 amp

References

Circuit Schematic: C-50950
Engineering Notes: E-104
E-144

C-50950





P1
RADIO TERMINAL CONNECTOR
#6824-15
CANNON ELECTRIC CO.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; JAN SPEC., COMPOSITION TYPE, ½ W, ±10 %.
   B. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
   C. ALL 0.01 MFD CAPACITORS ARE CERAMIC DISC, 600V.
   D. ALL OTHER CAPACITORS ARE MMFD; JAN SPEC., MICA ±10 %.

DRAWING REFERENCES:
1. BLOCK DIAGRAM:
2. BLOCK SCHEMATIC:
3. ASSEMBLY: C-51023
4. PARTS LIST: PL-51023

		MASSACHUSETTS INSTITUTE OF TECHNOLOGY DIGITAL COMPUTER LABORATORY DEPT. OF ELECTRICAL ENGINEERING – D. I. C. PROJECT NO. 6889	
		CIRCUIT SCHEMATIC PLUG-IN GATE TUBE UNIT, MOD II, WWI	
		SCALE NONE	DR CRD – 3/6/52
		ENG	CK APPD
			C-50950

Plug-In
DUAL BUFFER AMPLIFIER, MOD II
(BA-BA)

General Description

This unit comprises two identical, independent, point-to-point amplifiers mounted on one standard plug-in chassis. Each amplifier can be driven without pulse droop by standard pulses at prf's up to 1 mc; from 1 mc to 2 mc, the amplifier is usable but increasingly prf sensitive with about 5-v droop in a series of pulses at 2 mc. Each amplifier provides transformer output and therefore provides positive or negative pulses depending upon which output terminal is grounded. Nonstandard pulses of sufficient amplitude will be amplified and partially reshaped to approximate a standard pulse out.

Specifications

Input: Positive pulses of 15-v to 30-v amplitude.

Output: Positive or negative pulses of 15-v to 35-v amplitude into 100 ohms. Any input pulses exceeding 30 volts will overdrive the amplifier to give a slightly distorted pulse out with about 35-v major amplitude.

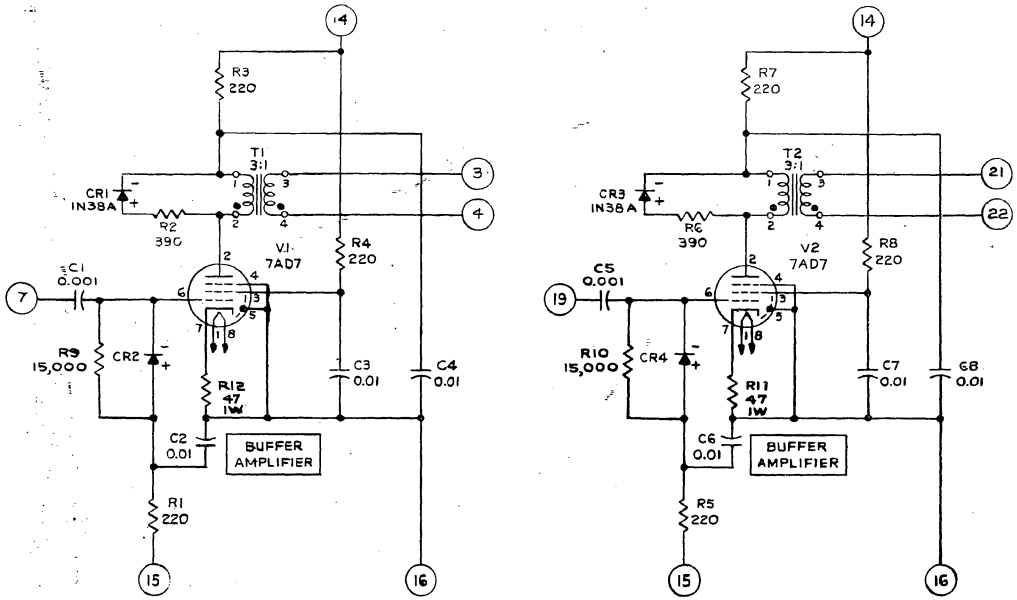
Power Requirements:

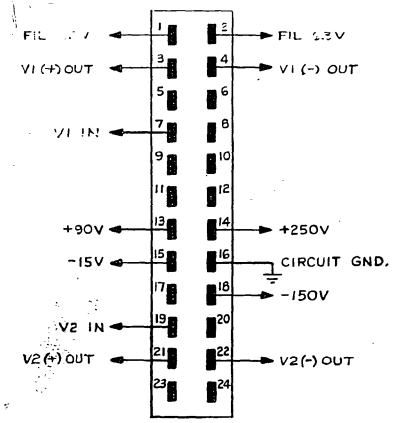
Voltage	Current to One Tube
+250-v DC	approx. 2.4 ma plus 30 ma per mc of prf
- 15-v DC	approx. -2 ma per mc of prf
6.3-v AC	1.2 amp

References

Circuit Schematic: C-50826

C-50826





P1
RADIO TERMINAL
CONNECTOR
#16824-15
CANNON ELEC. CO.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS ; JAN SPEC. COMPOSITION TYPE, $\frac{1}{2}$W, $\pm$10%
   B. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
   C. ALL 0.01 MFD CAPACITORS ARE CERAMIC DISC, 600V
   D. ALL OTHER CAPACITORS ARE MFD ; JAN. SPEC., MICA, $\pm$10%

DRAWING REFERENCES:

1. ASSEMBLY: C-50830
2. BLOCK SCHEMATIC:
3. PARTS LIST: PL-50830

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW
GRADE 1 FOR REFERENCE ONLY
GRADE 2
GRADE 3
SHD 3/4/52

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING PROJECT NO 6889

CIRCUIT SCHEMATIC
PLUG-IN DUAL BUFFER AMPLIFIER, MC I, II, WWI
F.B. Feb 7 '52
C-50826

aw 2/26/52

Plug-In
GATE-BUFFER AMPLIFIER, MOD II
(GT-BA)

General Description

This unit consists of a buffer amplifier fed from a gate-tube circuit. The gate is controlled by a d-c voltage level, such as a flip-flop output. When open, the gate passes pulses to the buffer amplifier which insures output pulses of good shape and amplitude at a 100-ohm impedance level. A separate input is provided to the buffer amplifier so that it may be used independently. The entire circuit may be driven without pulse droop at prf's up to 2 mc; from 1 mc to 2 mc it is usable but increasingly prf sensitive with about 5-v droop at 2 mc. The transformer output provides positive or negative pulses depending upon which output terminal is grounded.

Specifications

Input: Positive standard pulses of 15-v to 30-v amplitude; d-c levels of 0 volts to turn the gate tube "on" and -15 volts to turn it "off," or gate pulses of the same amplitude.

Output: Positive or negative pulses of 17-v to 35-v amplitude at a 100-ohm level.

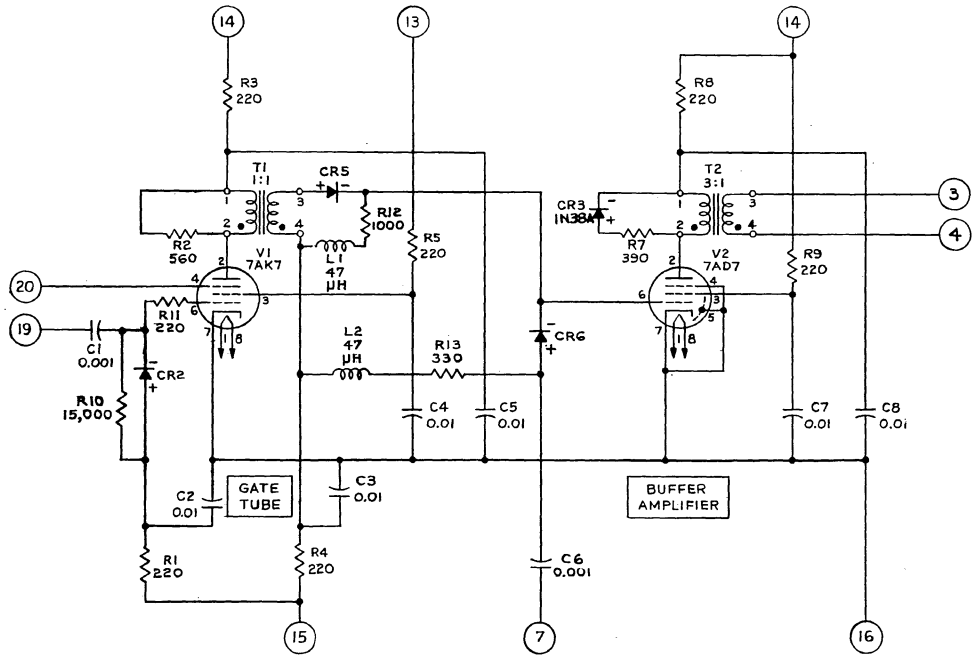
Power Requirements:

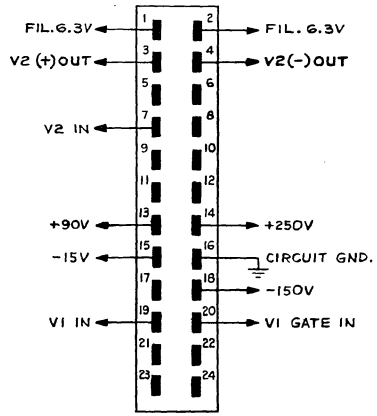
Voltage	Current
+250-v DC	approx. 2.6 ma plus 30 ma per mc of prf
+ 90-v DC	approx. 5 ma per mc of prf
- 15-v DC	approx. -2 ma per mc of prf
6.3-v AC	1.4 amp

References

Circuit Schematic: C-50827

C-50827





P1
RADIO TERMINAL
CONNECTOR
#16824-15
CANNON ELEC. CO.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. RESISTORS ARE IN OHMS; JAN SPEC. COMPOSITION TYPE, $\frac{1}{2}$W, ±10%
   - B. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
   - C. ALL 0.01 MFD CAPACITORS ARE CERAMIC DISC, 600V
   - D. ALL OTHER CAPACITORS ARE MFD; JAN SPEC., MICA, ±10%

DRAWING REFERENCES:

1. ASSEMBLY: C-50831
2. BLOCK SCHEMATIC:
3. PARTS LIST: PL-50831

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
SWD 3/4/52 GRADE III FINAL DESIGN

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING - D.S.L. PROJECT NO. 6889

CIRCUIT SCHEMATIC
PLUG-IN GATE-BUFFER AMPLIFIER, MCRII, WWI

F.B. Feb. 6 '52 C-50827

GW 7/26/52 2-26-52 3-4-52

Plug-In
D-C FLIP-FLOP
(FF)

General Description

The circuit of this plug-in Flip-Flop is essentially the same as that of the Burroughs Flip-Flop, Type 1103 AW (see Sect. 9, above), without the trigger amplifier and two read-in gate tubes. The unit is intended to drive gate tubes, crystal gates, and similar loads. It is set or cleared by negative pulses applied to the "one" or "zero" control grids, respectively; it is triggered by negative pulses applied simultaneously to the control grids of both sides or by positive pulses applied to the common cathode. Triggering can be achieved reliably at prf's of up to about 4 mc.

Specifications

Input: Negative pulses of over 6-v amplitude for "set" or "clear"; positive or negative pulses of over 6-v amplitude for "complement." In either case, ripple or overshoot should be less than .3 volts.

Output: The "one" and "zero" outputs yield either of two d-c levels intended to be applied to a high-impedance load which may consist of the grids of 1 to 3 gate tubes. The two levels are 0 and -18 volts. Rise and fall trigger time are approximately 0.2 μsec.

Other outputs provide two d-c voltage levels to control neon indicator lights, to control plug-in switch units, and to operate typewriter equipment.

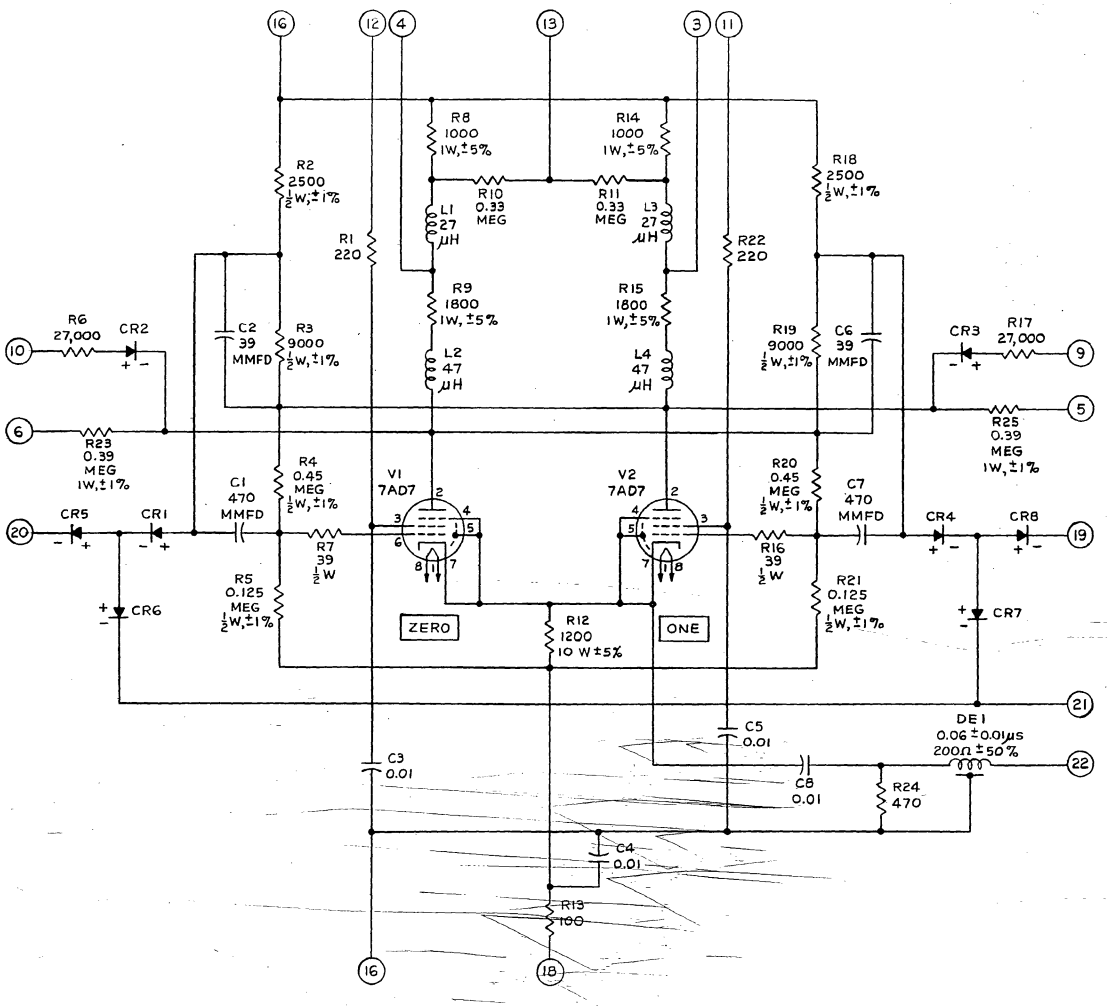
Power Requirements:

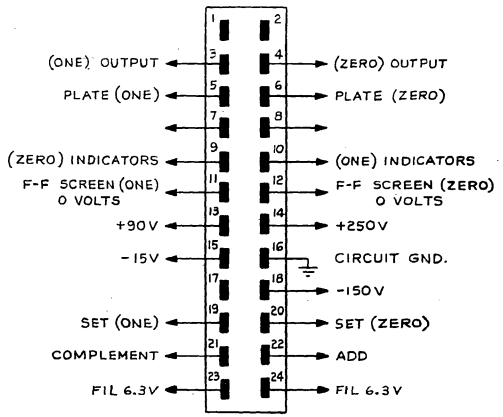
+90-v DC	0.7 ma
-150-v DC	30 ma
6.3-v AC	1.2 ma

References

Engineering Notes	E-168
	E-493
Circuit Schematic	C-50825

C-50825





P1
RADIO TERMINAL CONNECTOR
#16824-15
CANNON ELEC. CO

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; JAN SPEC. COMPOSITION TYPE, ½W, ±10%
   B. RESISTORS R2 THRU R5, AND R18 THRU R21 ARE CONTINENTAL CARBON "NOBLELOY" NF ½ OR THE EQUIV.
   C. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A
   D. ALL 0.01 MFD CAPACITORS ARE CERAMIC DISC, 600V
   E. ALL OTHER CAPACITORS ARE MFD; JAN SPEC., MICA, ±10%
2. FOR FURTHER SPECIFICATION OF SPECIAL DELAY LINE (DE1) SEE ASSEMBLY DRAWING D-51068

DRAWING REFERENCES:
1. ASSEMBLY: C-50838
2. BLOCK SCHEMATIC:
3. BLOCK DIAGRAM:
4. PARTS LIST: PL-50838

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW.
GRADE I FOR REFERENCE ONLY
GRADE II
GRADE III
4/22/52

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D.C.L. PROJECT NO 6889

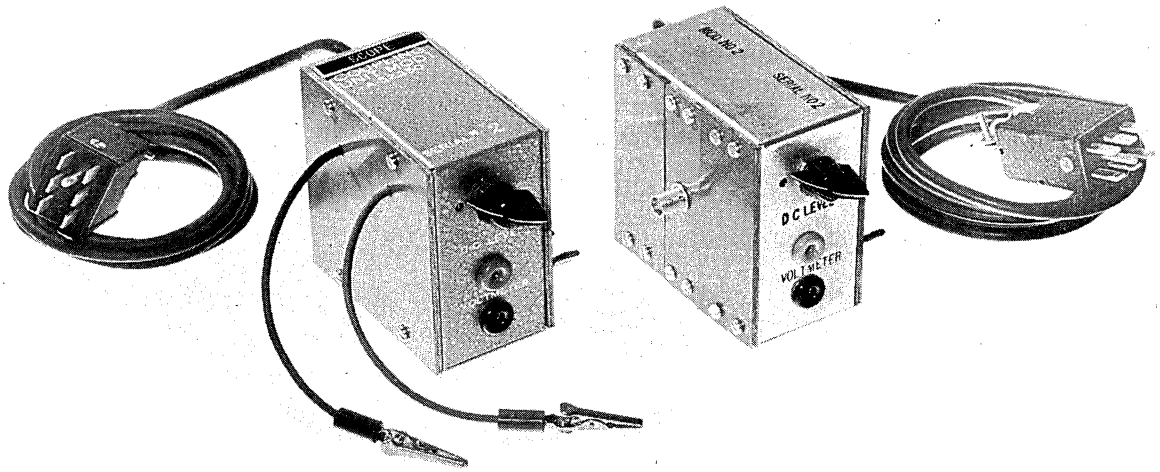
CIRCUIT SCHEMATIC
PLUG-IN D-C FLIP-FLOP, MOD. II, WWI

F.B. Apr 8 '52

C-50825

4/22/52

SCOPE COUPLING UNIT
(Models I & II)



General Description

The scope coupling unit is used to couple signals directly to the vertical-deflection plates of the Tektronix 514D scope. Because of the scope amplifier's pass-band limits, this unit is used to best advantage in observing fast rise-time pulses such as the standard 0.1-μsec pulse. It is also used to check on the presence of high-frequency parasitic oscillations. While both models are the same except for input (see below), Model I is preferable to Model II since it provides less capacitive loading.

Specifications

Dimensions: 4 x 4 x 2-1/4 inches.

Circuit: Vertical-positioning-control coupling circuit.

Input: The input on both models may be direct-coupled since there are internal series capacitors. Models I and II differ only in the mechanical arrangement of the input, which in Model I is through a pair of short clip leads while Model II uses a 3/8-inch BNC connector. Signals lower than 1 or 2 volts cannot be observed with either model.

Output: The output goes directly to the plates of the CRT through vertical-deflection-plate banana plugs on the side of the scope. Two banana jacks permit a voltmeter to be plugged in.

Control: The control knob changes the level of the trace on the scope. Signal amplitude is measured by turning the control to its extreme CCW position and applying a signal. The sweep is then lifted (by use of the control) to the observed position of the top of the signal on the scope face. A voltmeter plugged into the banana jacks indicates the amplitude of the signal.

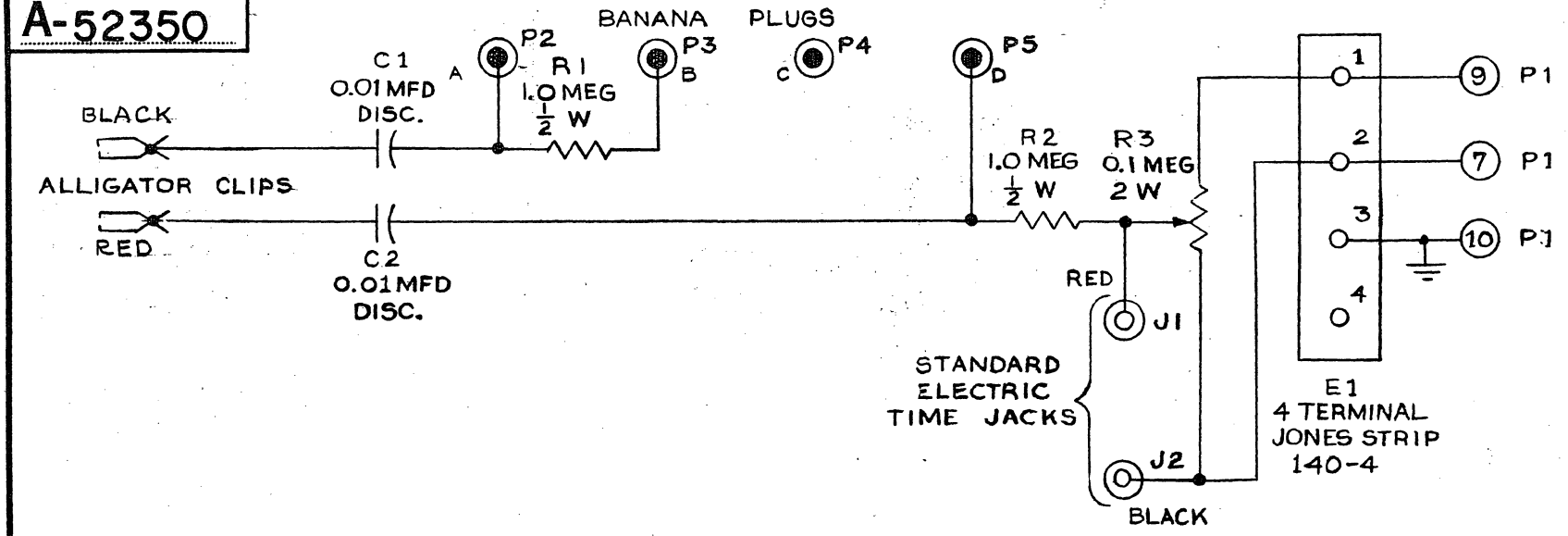
Power Requirements:

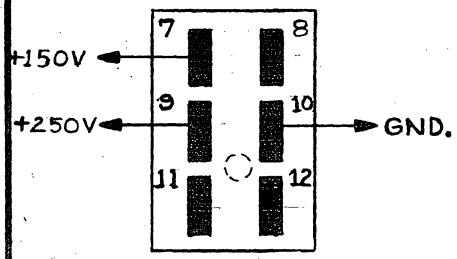
+250-volts DC	1 ma
+150-volts DC	1 ma

References

Circuit Schematic	A-52350
Memorandum	M-1604
Photograph	F-1821

A-52350





P 1
6 PIN
JONES PLUG

DRAWING REFERENCES
1. ASSEMBLY: C-52552
2. PARTS LIST: PL-52552

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:

GRADE I FOR REFERENCE ONLY

GRADE II PRELIMINARY DESIGN

DRB 10-23-52 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
-10			
-9			
-8			
-7			
-6			
-5			
-4			
-3			
-2	4456	12/31/51	Chm B
-1	4181	11/14/52	Chm D

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO.

CIRCUIT SCHEMATIC
SCOPE COUPLING UNIT, MOD. I TE

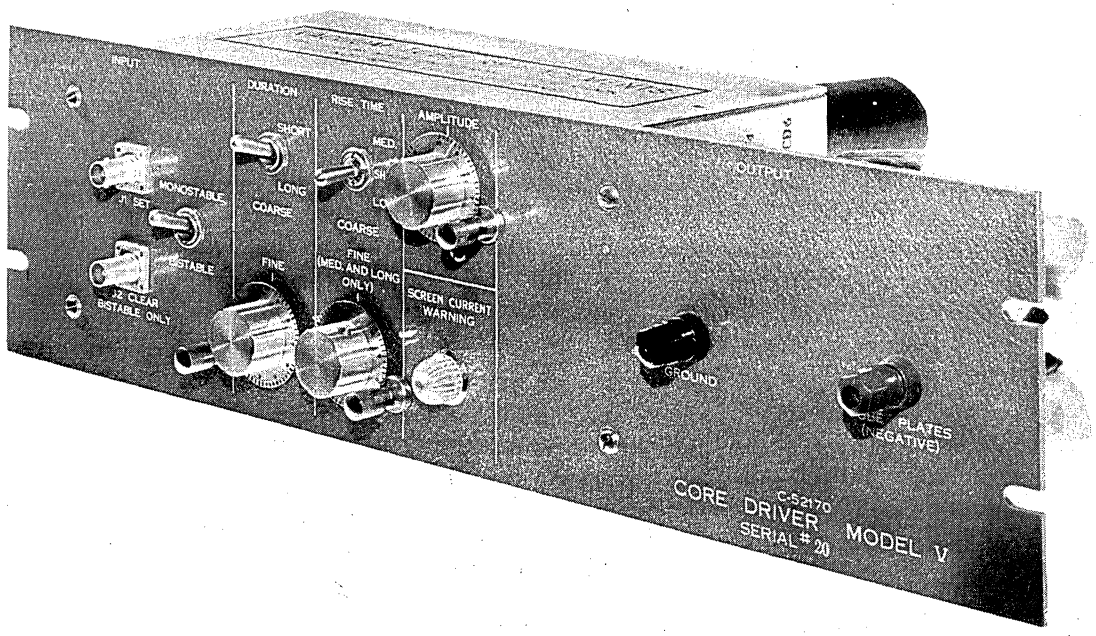
SCALE: —— DR. CMS 9-29-52

ENG. HP 9/31/52 CK. RBB 10/1/52 APPD. RLBeat

A-52350

Whirlwind
CORE DRIVER,MOD.V identical to
CORE DRIVER,MOD.VI identical to

Burroughs
CURRENT-PULSE GENERATOR (NEGATIVE)
CURRENT-PULSE GENERATOR (POSITIVE)



General Description

The Model V and Model VI core drivers deliver rectangular-wave current pulses of variable amplitude, rise time, and duration. These units were designed principally to test cores and drive core setups. Model V supplies negative-going pulses, whereas Model VI supplies positive-going pulses; both are from a ground level.

Specifications

Dimensions: 5-1/4 x 5 x 19 inches.

Circuits: Monobistable multivibrator (5965).
Amplifier (1/2, 5687).
Cathode follower (1/2, 5687).
Current amplifier (4, 6CD6's).

Input: Standard 0.1-μsec pulses, negative, 13-30 volts (J1-set or J1-set and J2-clear).

Output:

Shape -- rectangular.
Amplitude -- variable from 0 to greater than 1.6 amp.
Regulation and back voltage -- back voltage may be up to 100 volts. For Mod. V, this causes a drop in current of approximately 10%; for Mod. VI, a drop of approximately 70%.
Rise time -- less than 0.15 μsec and 0.2 to 1.0 μsec in two overlapping ranges.
Duration -- 1-40 μsec in two overlapping ranges (monostable); 0.6-40 (bistable).

Duty Factor:

Limited by multivibrator to no more than:
40% in monostable
75% in bistable
Limited by dissipation in output tubes to no more than:
20% at 2.0-amp output
25% at 1.6-amp output
40% at 1.0-amp output
50% at 0.8-amp output
75% at 0.53-amp output

Resolution Time: 0.5 μsec at maximum-output amplitude. (May be complemented in "bistable" from 12.5 kilocycles to 2 megacycles connecting J1 and J2 together.)

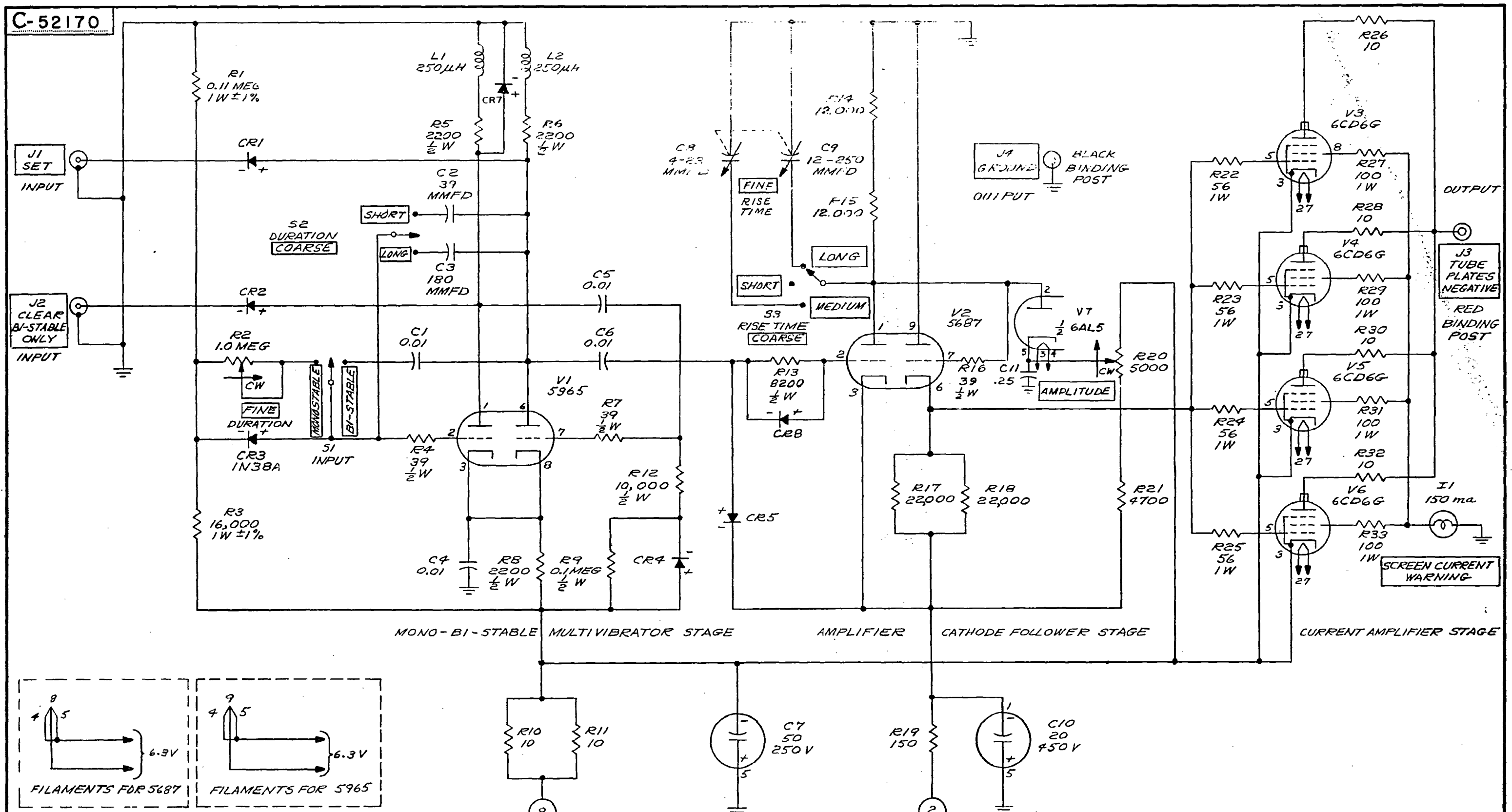
Power Requirements:

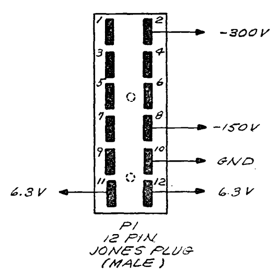
Voltage	Model V	Model VI
+150-v DC		0.03-2.03 amp
-150-v DC	0.03-2.03 amp	0.04 amp
-300-v DC	0.04 amp	
6.3-v AC	10.6 amp	10.6 amp

References

Circuit Schematics C-52170
C-52643
Engineering Note E-523

C-52170





NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; 2W.
   B. RESISTORS ARE ±10%.
   C. CAPACITORS ARE IN MICROFARADS.
   D. VIDEO CONNECTORS J1 & J2 ARE JAN UG-290/U
   E. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. USE SEPARATE FILAMENT SUPPLY OR ISOLATION TRANSFORMER
3. CONNECT SHAFTS OF C8 & C9 TOGETHER WITH SLEEVE. CONNECT FRAMES TOGETHER FOR RIGIDITY.
4. THIS DRAWING IS SIMILAR TO C-52643 (CORE DRIVER MOD VI) ~ EXCEPT OUTPUT & SUPPLY VOLTAGES.
5. TITLE OF IDENTICAL ALTERNATE UNIT IS "CURRENT-PULSE GENERATOR (NEGATIVE)."

DRAWING REFERENCES:
1. ASSEMBLY: D-52622
2. PARTS LIST: PL-52622

FIG. 1

GRADED BY DATE. THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
DRB 10-9-52 GRADE II PRELIMINARY DESIGN
DRB 1-5-53 GRADE III FINAL DESIGN

CHG.	CN#	DATE	APPD.
1	4066	11/20/52	
2	1331		
3	4717		
4	5178	5-15-53	

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING—D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC, CORE DRIVER-MOD V, TE

SCALE: — | DR. CRD 9/25/52 | ENG. 9/29/52 | CK. 9/29/52 | APPD. 9/29/52

C-52170

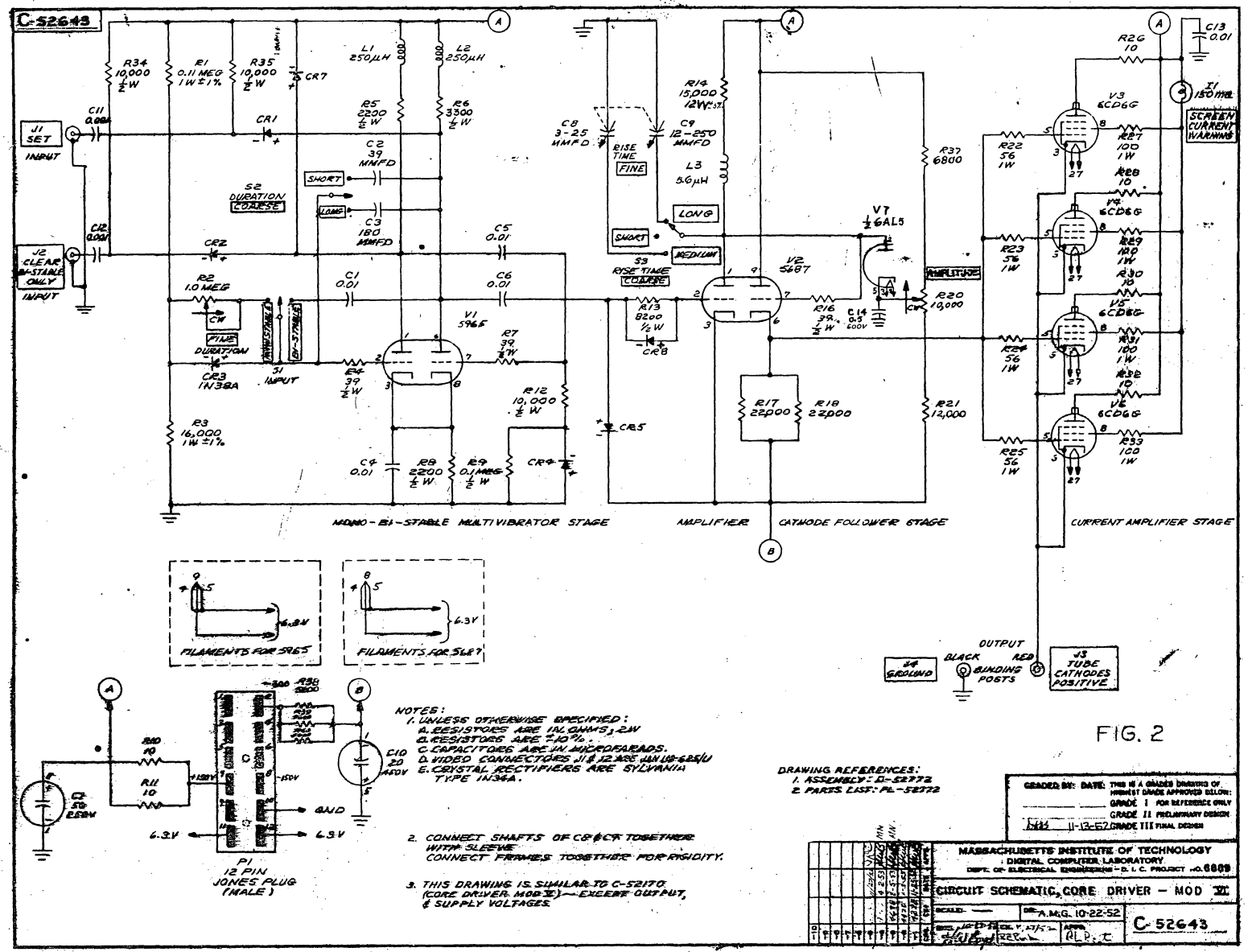
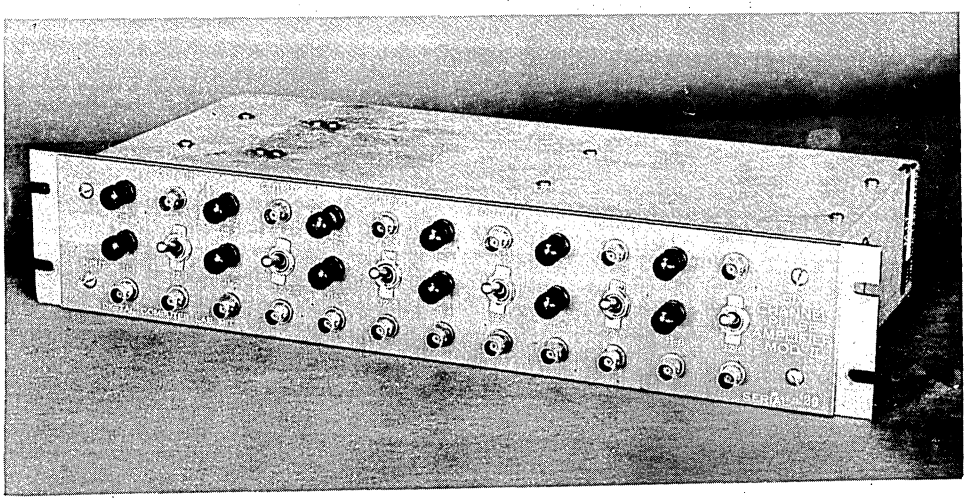

C-52643
J1 SET INPUT
J2 CLEAR (BI-STABLE ONLY) INPUT
S2 DURATION COARSE
SHORT
LONG
FINE
MEDIUM
S3 RISE TIME COARSE
R34 10,000 ½W
R1 0.11 MEG 1W ±1%
R35 10,000 ½W
CR7
L1 250μH
L2 250μH
C11 0.001
CR1
R5 2200 ½W
R6 3300 ½W
C2 39 MMFD
C3 180 MMFD
C12 0.001
CR2
C5 0.01
C1 0.01
C6 0.01
R2 1.0 MEG
CW
FINE
DURATION
CR3 IN38A
BI-STABLE
J3 INPUT
V1 5965
R4 39 ½W
R7 39 ½W
R12 10,000 ½W
R3 16,000 1W ±1%
C4 0.01
R8 2200 ½W
R9 0.1 MEG ½W
CR4
C8 3-25 MMFD
C9 12-250 MMFD
R14 15,000 12W
L3 5.6μH
CR8
R13 8200 ½W
CR5
V2 5687
R16 39 ½W
C14 0.5 600V
V7 ½ 6AL5
R17 22,000
R18 22,000
R37 6800
R20 10,000
AMPLITUDE
R21 12,000
R26 10
C13 0.01
I1 150 MA
SCREEN CURRENT WARNING
V3 6CD6G
V4 6CD6G
V5 6CD6G
V6 6CD6G
R22 56 1W
R23 56 1W
R24 56 1W
R25 56 1W
R27 100 1W
R28 10
R29 100 1W
R30 10
R31 100 1W
R32 10
R33 100 1W
MONO-BI-STABLE MULTIVIBRATOR STAGE
AMPLIFIER
CATHODE FOLLOWER STAGE
CURRENT AMPLIFIER STAGE
FILAMENTS FOR 5965
FILAMENTS FOR 5687
J4 GROUND
OUTPUT
BLACK
RED
BINDING POSTS
J3 TUBE CATHODES POSITIVE
R10 10
R11 10
C7 50 250V
C10 20 450V
GND
6.3V
P1 12 PIN JONES PLUG (MALE)
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. RESISTORS ARE IN OHMS, 2W
B. RESISTORS ARE ±10%.
C. CAPACITORS ARE IN MICROFARADS.
D. VIDEO CONNECTORS #1 & 12 ARE MIL-C-625A/U
E. CRYSTAL RECTIFIERS ARE SYLVANIA TYPE 1N34A.
2. CONNECT SHAFTS OF C8 & C9 TOGETHER WITH SLEEVE
CONNECT FRAMES TOGETHER FOR RIGIDITY.
3. THIS DRAWING IS SIMILAR TO C-52170 (CORE DRIVER MOD IX) EXCEPT OUTPUT, & SUPPLY VOLTAGES
DRAWING REFERENCES:
1. ASSEMBLY: D-52772
2. PARTS LIST: PL-52772
GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
11-13-52 GRADE III FINAL DESIGN
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING - D. I. C. PROJECT NO. 6606
CIRCUIT SCHEMATIC, CORE DRIVER - MOD XI
SCALE: —
DR. A.M.G. 10-22-52
APPR. A.L.P.
C-52643

FIG. 2

6 CHANNEL PULSE AMPLIFIER MOD I



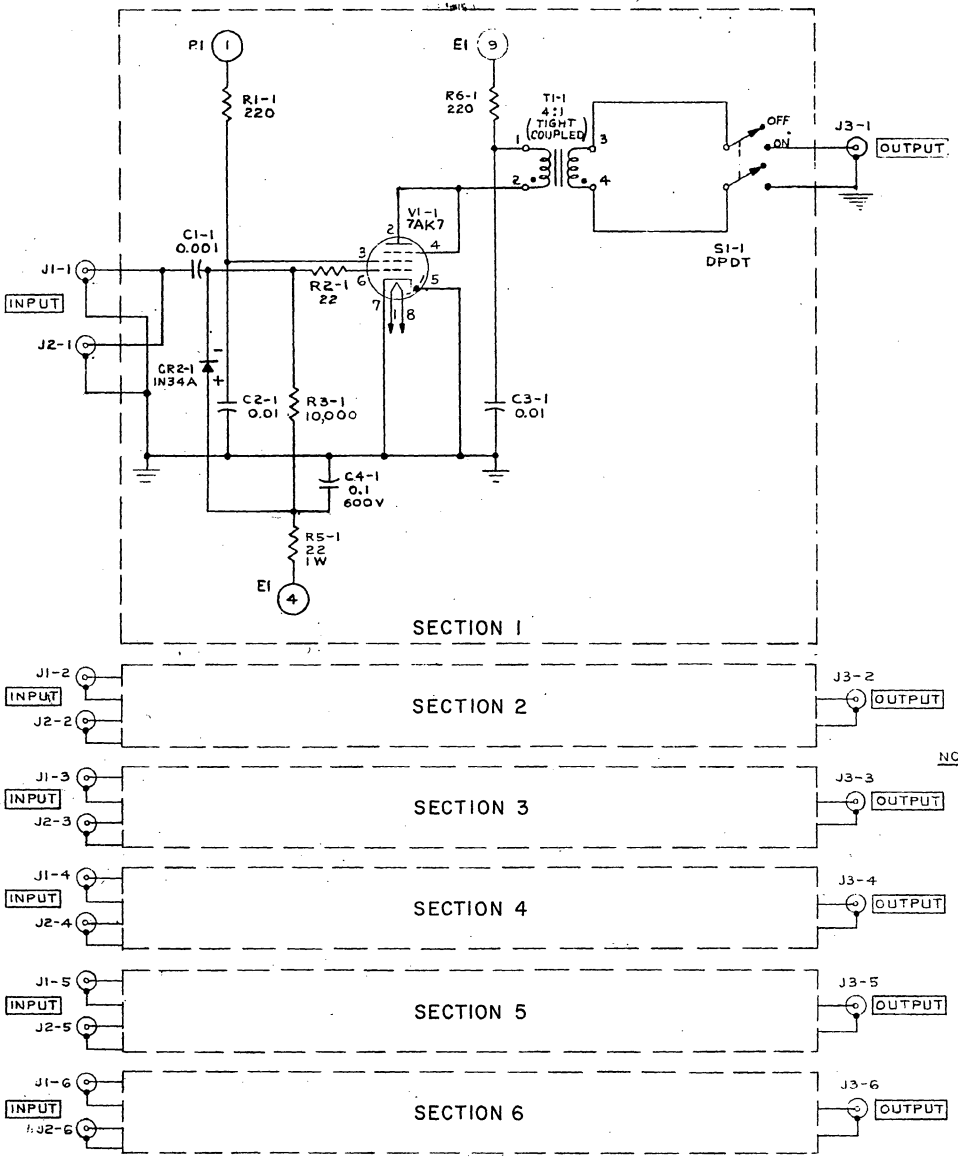
General Description

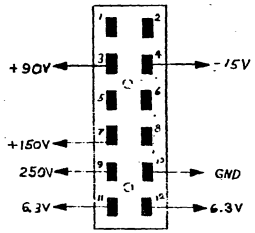
This unit consists of 6 identical pulse amplifiers, each of which accepts an input pulse at any dc level and generates an output pulse. The shield of the input and output (co-ax connectors) are grounded.

Specifications:

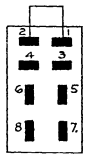
Dimensions:	3 1/2 in. x 19 in., depth 10 1/2 in.
Inputs:	Positive 0.1 - usec pulses 15 to 40 volts in amplitude, up to 5 mc.
Outputs:	Positive 0.1 - usec pulses 15 to 50 volts in amplitude (depends on input amplitude, prf, and load) up to 5 mc. Gain becomes poorer above 1 mc.
Controls:	An on-off switch for each of the 6 outputs.
Circuit:	7AK7 pulse amplifier
Power:	+250 vdc 10 ma/mc/ channel +90 vdc 0.5 ma/mc/ channel -15 vdc 1 ma/mc/ channel 6.3 vac 4.8 amps
References:	Circuit Schematic C-58285

C-58285

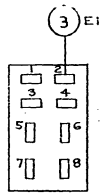




P2412-CCT
12 PIN
JONES PLUG
(MALE)



P2
8 PIN
JONES PLUG
P-308-CCT
(MALE)



P1
8 PIN
JONES SOCKET
S-308-AB
(FEMALE)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; $\frac{1}{2}$ W, ± 5 %.
   B. CAPACITORS ARE IN MICROFARADS.
   C. VIDEO CONNECTORS ARE UG-625/U.
2. SECTIONS 2 THRU 6 ARE IDENTICAL WITH SECTION 1, EXCEPT FOR COMPONENT NUMBER SUFFIXES. FOR EXAMPLE, THE TUBE V1-1 7AK7 IN SECTION 1 IS V1-3, 7AK7 IN STAGE 3.
3. NO LOAD TERMINATION ≈ 50Ω

DRAWING REFERENCES:

1. ASSEMBLY : D-58288
2. BLOCK SCHEMATIC:
3. PARTS LIST: PL-58288

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN.
3-26-54

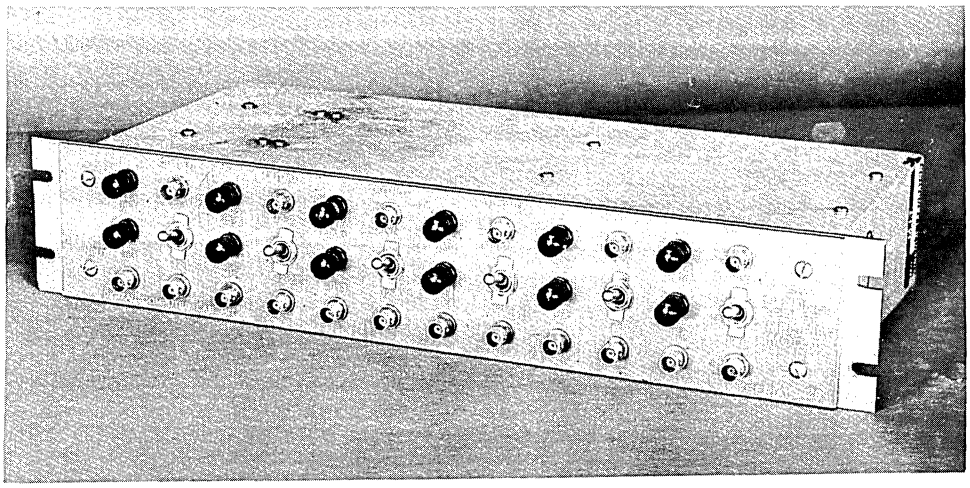
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC, SIX CHANNEL PULSE AMPLIFIER PANEL, TE

SCALE: —— DR. A.S. 3-22-54 ENG. 3/23/54 CK. APPD.

C-58285

6 CHANNEL PULSE AMPLIFIER MOD II



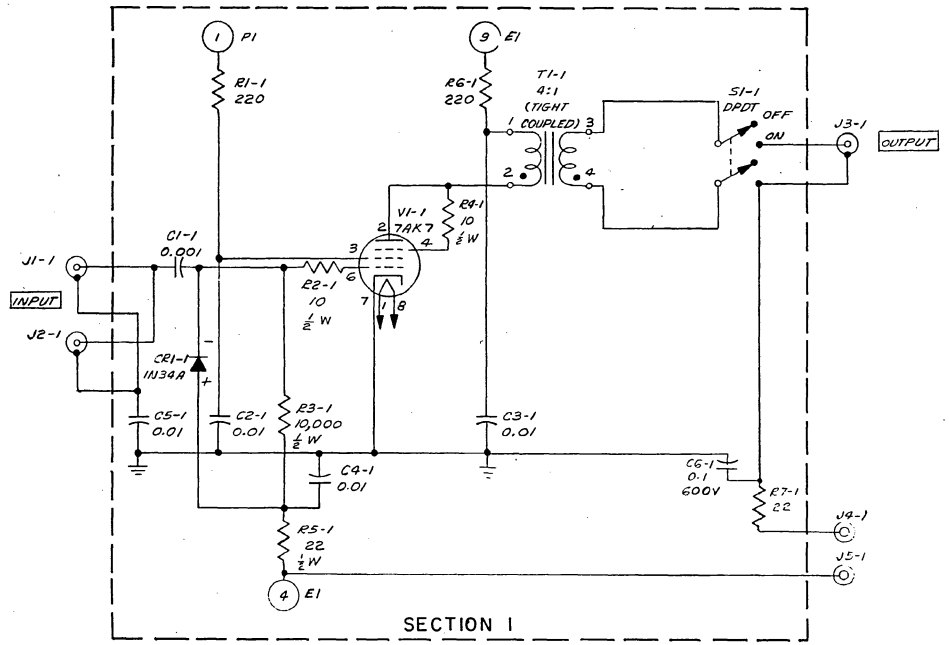
General Description

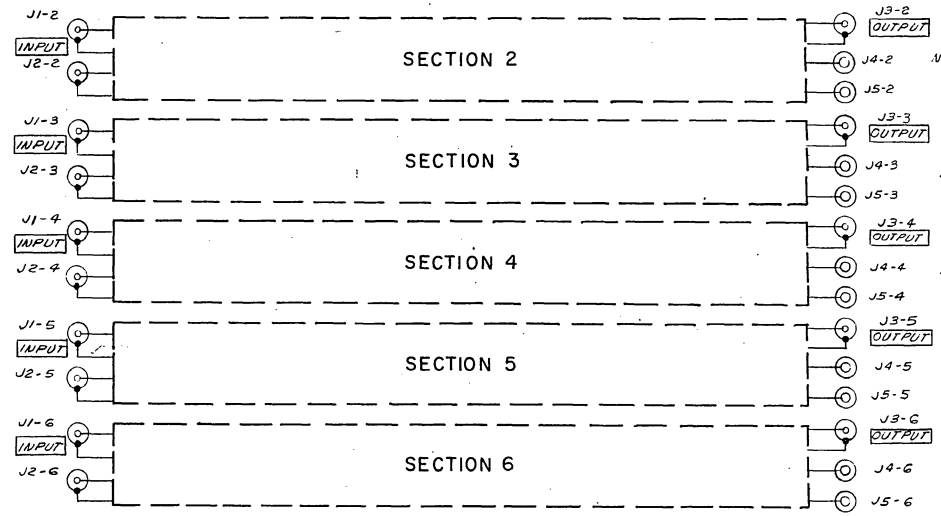
This unit consists of 6 identical pulse amplifiers, each of which accepts an input pulse at any dc level and generates an output pulse at a dc level of zero or -15 volts. The shield of the input (co-ax connectors) (J1 and 2) which may be at any dc level are bypassed to ground through a capacitor; the shield of the output jack (J3) is brought out to J4. J5 is -15 volts; the output may be placed at a dc level of -15 by a jumper between J4 and J5. This unit was designed to match pulse test equipment to the XD-1 computer, where pulse lines are at a level of -15 volts.

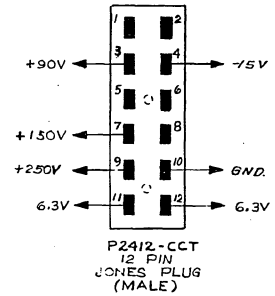
Specifications:

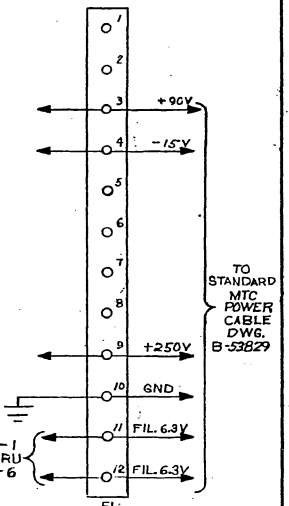
Dimensions:	3 1/2 in. x 19 in., depth 10 1/2 in.
Inputs:	Positive 0.1 -usec pulses 15 to 40 volts in amplitude, up to 5 mc.
Outputs:	Positive 0.1 -usec pulses 15 to 50 volts in amplitude (depends on input amplitude, prf, and load) up to 5 mc. Gain becomes poorer above 1 mc. DC level of output pulse may be modified from the front panel.
Controls:	An on-off switch for each of the 6 outputs.
Circuit:	6 7AK7 pulse amplifiers
Power:	+250 vdc 10 ma/mc/ channel +90 vdc 0.5 ma/mc/ channel -15 vdc -1 ma/mc/ channel 6.3 vac 4.8 amps
References:	Circuit Schematic C-58678

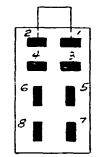
C-58678

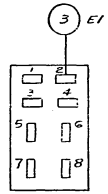












NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS; 1W ± 5%.
   B. CAPACITORS ARE IN MICROFARADS.
   C. VIDEO CONNECTORS ARE UG-625/U.
2. SECTIONS 2 THRU 6 ARE IDENTICAL WITH SECTION 1, EXCEPT FOR COMPONENT NUMBER SUFFIXES. FOR EXAMPLE, THE TUBE V1-1 7AK7 IN SECTION 1 IS V1-3 7AK7 IN STAGE 3.
3. NO LOAD TERMINATION ≈ 50Ω.

DRAWING REFERENCES:
1. ASSEMBLY: D-53679
2. PARTS LIST: PL-53679

GRADED BY: DATE: THIS IS A GRADED DRAWING OF HIGHEST GRADE APPROVED BELOW:
GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
5-11-54 GRADE III FINAL DESIGN

CHG.	CHK	DATE	APPD.
10			
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2	7256	1-30-54	
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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIGITAL COMPUTER LABORATORY
DEPT. OF ELECTRICAL ENGINEERING — D. I. C. PROJECT NO. 6889

CIRCUIT SCHEMATIC,
SIX CHANNEL PULSE AMPLIFIER PANEL MOD II, TE

SCALE: —— DR. BP 4-28-54

ENG. 4-[illegible]-54 CK. 4/27/54 APPD. 5-14-54 RLE

C-58678

DIGITAL EQUIPMENT CORPORATION

BUILDING BLOCKS

I. Introduction To DEC BUILDING BLOCKS

DEC Building Blocks are a coordinated set of packaged basic digital circuits. They are primarily planned to be assembled in temporary or semi-permanent systems for laboratory and production testing. They are designed so as to take full advantage of the characteristics of transistor circuitry.

Test pattern generation, checking, counting, shifting, adding and general logic and memory functions are ideally performed by DEC Building Blocks. DEC Building Blocks are fast in operation, small in size, easy to use, and consume little power.

In most systems the blocks will operate at 5 megapulses per second. The signals are readily adapted to other types of digital circuits. To prevent accidental electrical damage, the units have been designed so that terminals may be grounded without harm to the unit.

These units are completely enclosed in rugged aluminum cases (approximately 6-1/2 x 4-1/2 x 1-3/4) so that they will withstand the rough handling received by laboratory equipment. Nine such units can be mounted in a 5-1/4 x 19 inch rack mounting panel. The standard DEC power supplies also mount directly in a 19 inch rack. Small numbers of the building block units can be conveniently used right on a lab bench. The power comes in the rear of each unit and the signal terminals are graphic diagramed on the front panel. Logical connections are made with patch cords which have miniature stacking banana connectors.

II. Logical Operations with DEC BUILDING BLOCKS

In DEC Building Blocks logical operations are performed by combinations of saturable transistor inverters. The user can consider these as simple switches that are either open or closed. In the graphic symbology used in DEC Building Blocks, a negative level on A, the input or base of figure 1 will "Short" the output x to ground while a ground level in will open the gate and the output will be -3 volts.

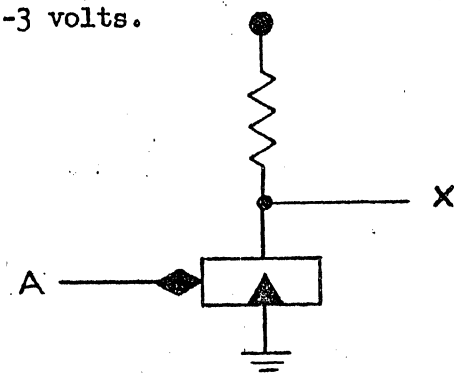


FIG. 1

If two transistors are connected in series as in Figure 2, both A and B need to be negative to "Short" the output to ground, thus an "and" gate is formed for negative levels or an "or" gate for ground levels.

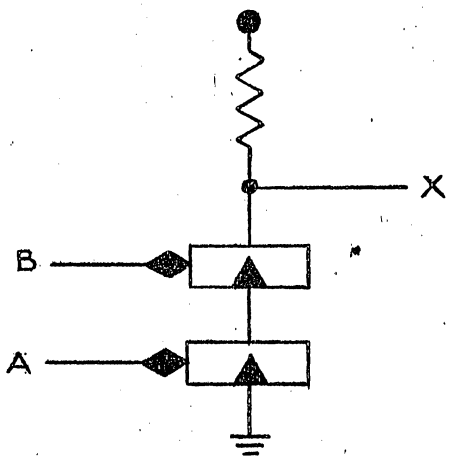


FIG. 2

If two or more transistors are connected in parallel as in Figure 3, any one will short the output to ground and an "or" gate is formed for negative signals or an "and" gate for positive signals. More complex logical functions are generated by series parallel combinations.

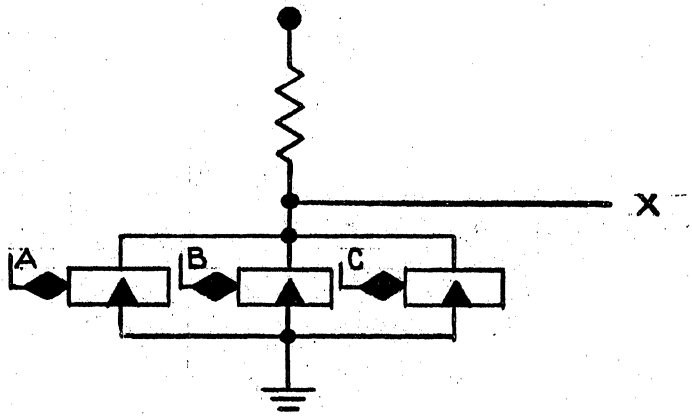
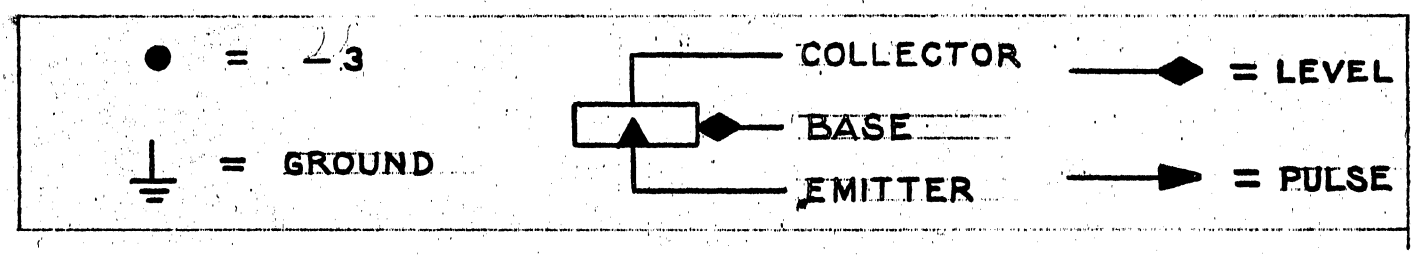


FIG. 3



The DEC flip-flops are set by "shorting" the appropriate input to ground with a pulsed transistor as in Figure 4. If the ground is replaced by another gate or a network of gates the flip-flop is only set if there is a "shorted" path through the network to ground. Pulses are used only in the gate nearest the flip-flop.

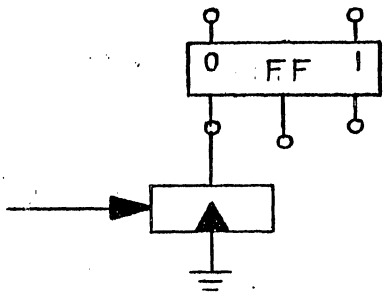


FIG. 4

The output stages of the flip-flop are low impedance inverters and can be included as part of logic net works. For example information can be shifted from one flip-flop to another by using just the 2 gates included with each flip-flop connected as in Figure 5.

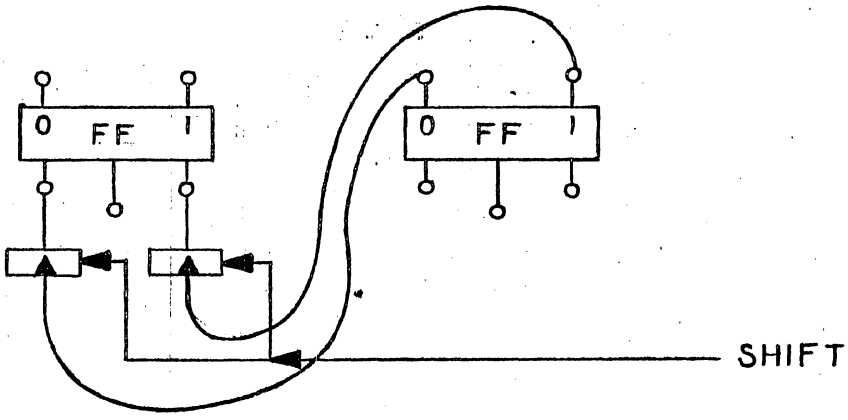


FIG. 5

Logical operations are usually performed by combinations of D.C. gates. Pulses are normally used to read the results into flip-flops. The terminal labeled P above the center of the flip-flop will deliver a standard 2.5 volt negative signal every time the flip-flop complement input terminal is pulsed. This signal is very useful in binary counter applications.

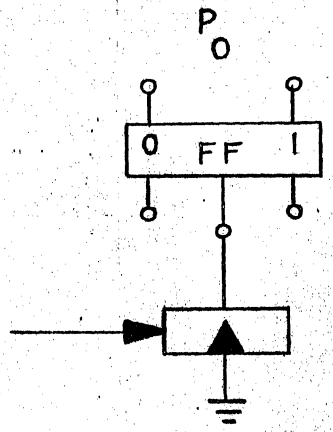


FIG. 6

A simple counter is illustrated in Figure 7. The pulse from jack P of #A will complement the next flip-flop when A holds a "1". When a flip-flop is in the "1" state the "1" output is at -3 and the "0" is at ground.

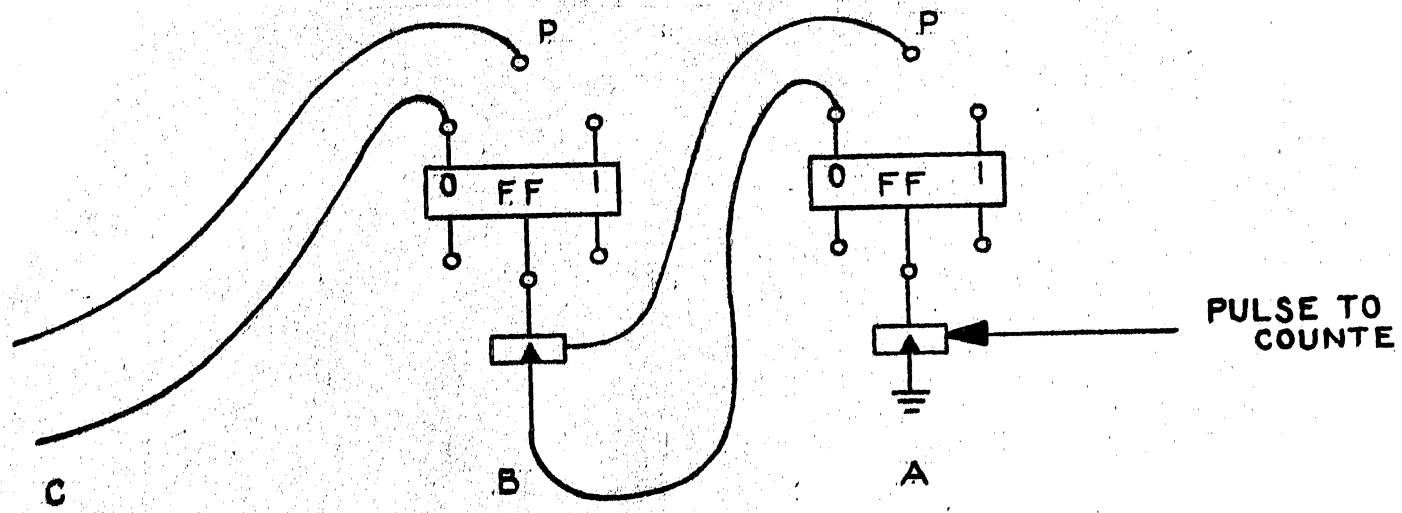


FIG. 7

In DEC Building Blocks the standard levels are ground and -3 volts (-3 to -3.5 volts measured). The pulses are -2.5 volts (from ground) in amplitude and no more than 70 millimicroseconds in duration. No more than three D.C. gates are put in series including the flip-flop output amplifier transistor when it is used. A pulsed gate can be used as a fourth gate in a series chain.

The catalog of transistor connections gives several examples of useful logical connections.*

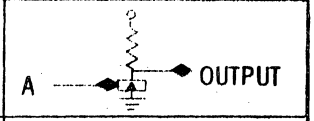
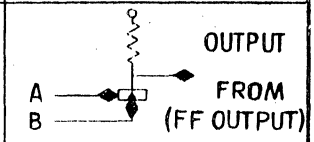
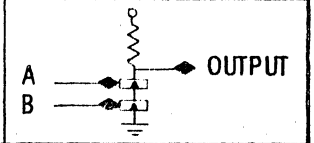
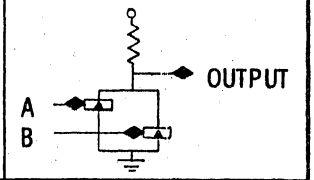
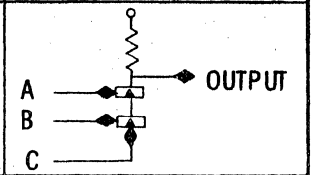
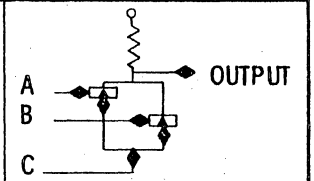
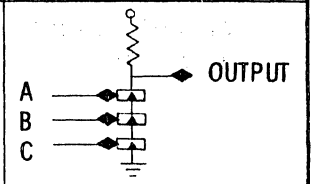
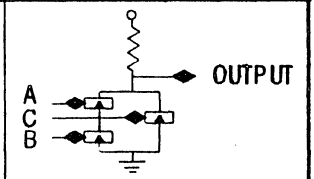
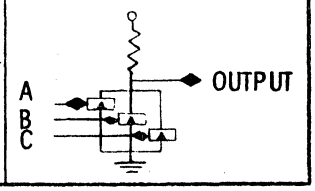
III. Marginal Checking of DEC BUILDING BLOCKS

Facility for marginal checking has been included in the DEC Building Blocks so that deteriorating components may be located before failure and, perhaps more significantly, to pinpoint noise or poor layout that is not serious enough to cause failure but that would limit the reliability of the system.

Marginal checking is accomplished by varying the + 10 volt supplies. This supply develops the bias on the inverters and, in general, if it is increased, low gain transistors will be made to fail. If it is decreased, it will allow any noise to cause failure.

There are two + 10 volt power terminals (+ 10a and + 10b) on each unit. Normally they are both set at + 10 volt but during marginal checking they are varied one at a time to detect failure points. In the standard DEC power supply + 10a and + 10b are connected to two variable voltage supplies so that marginal checking is convenient at any time. If marginal checking is not required, + 10a and + 10b may both be connected to the same power supply.

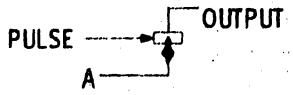
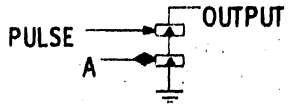
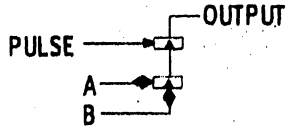
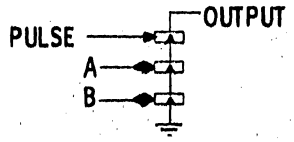
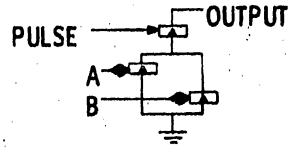
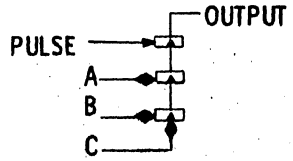
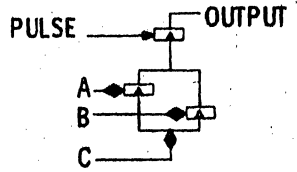
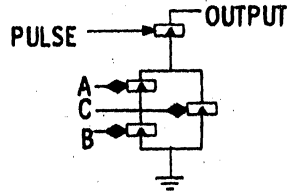
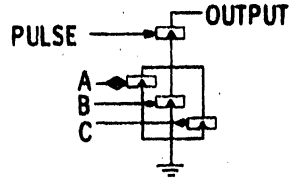
*See Catalog on the following pages.

NO. OF INPUT LEVELS	NO. OF TRAN-SISTORS	LOGIC		CONNECTION
		FOR ⏚ AT OUTPUT	FOR ● AT OUTPUT	
1	1	A= ●	A = ⏚	
2	1	A= ● AND B= ⏚	A= ⏚ OR B= ●	
2	2	A= ● AND B= ●	A= ⏚ OR B= ⏚	
2	2	A= ● OR B= ●	A= ⏚ & B= ⏚	
3	2	A= ● AND B= ● AND C = ⏚	A= ⏚ OR B= ⏚ OR C= ●	
3	2	(A= ● OR B=●) AND C= ⏚	(A= ⏚ AND B= ⏚) OR C = ●	
3	3	A= ● AND B=● AND C= ●	A= ⏚ OR B= ⏚ OR C= ⏚	
3	3	(A= ● AND B= ●) OR C= ●	(A= ⏚ OR B= ⏚) AND C= ⏚	
3	3	A= ● OR B= ● OR C= ●	A= ⏚ AND B= ⏚ AND C= ⏚	

B - 80561

CATALOG OF TRANSISTOR CONNECTIONS

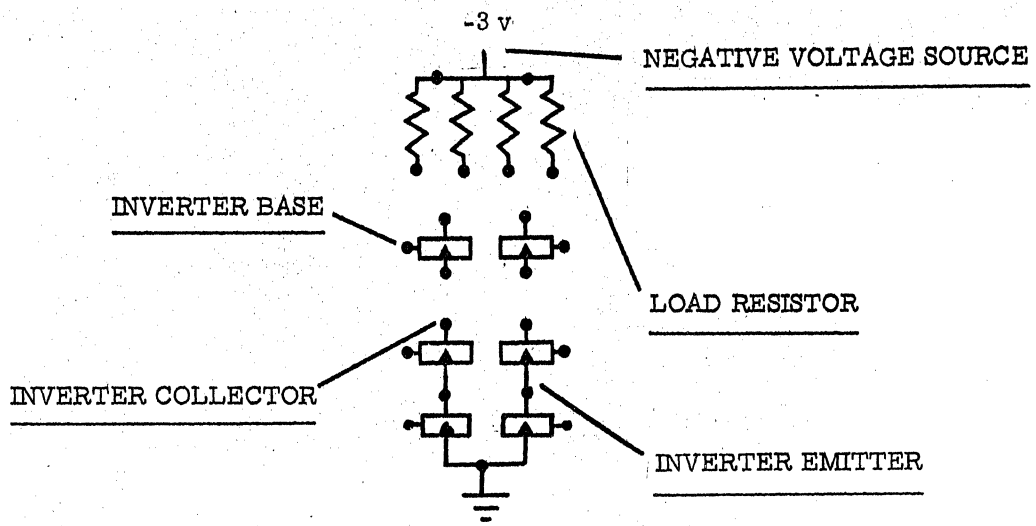
TABLE I LEVEL OUTPUTS

NO. OF INPUT LEVELS	NO. OF TRAN-SISTORS	LOGIC FOR PULSE TO BE PASSED	CONNECTION
1	1	A = ⏚	
1	2	A = ●	
2	2	A = ● AND B = ⏚	
2	3	A = ● AND B = ●	
2	3	A = ● OR B = ●	
3	3	A = ● AND B = ● AND C = ⏚	
3	3	(A = ● OR B = ●) AND C = ⏚	
3	4	(A = ● AND B = ●) OR C = ●	
3	4	A = ● OR B = ● OR C = ●	

CATALOG OF TRANSISTOR CONNECTIONS
TABLE 2 PULSE OUTPUTS

BUILDING BLOCKS

Inverter 101 INSTRUCTIONS



INVERTER 101

The basic circuit used in doing logical operations with DEC Building Block Test Equipment is the transistor inverter. A PNP transistor is the main element of the inverter. In the notation of DEC for the inverter, the base is at the side of the rectangle, the emitter is at the bottom and the collector is at the top.

The Inverter 101 package contains six identical transistor inverters and four identical load resistors which are diode clamped at -3v.

The inverter acts like a switch, i.e. when the base is negative with respect to the emitter a "simple switch" between the emitter and collector is closed thus allowing current to flow. When the base is at the same or positive potential with respect to the emitter, there is no emitter to collector current.

The transistor inverter is used as either a Level Gate or a Pulse Gate. The load resistors can be used with Level Gates. When the inverters are used as Pulse Gates, the unit being pulsed replaces the load resistor. Pulses are applied only to the base of an inverter. See Section 30, pages 7 and 8.

The delay through a transistor depends on the capacitive loading and under typical conditions is approximately 20 millimicroseconds. Since each transistor is an amplifier, Level Gate Logic can be cascaded (collector to base) an indefinite number of stages without losing signal amplitude. The signal delays must be taken into consideration when a large number of stages are cascaded.

Not more than three transistors can be placed in series for Level Gate Logic, i.e. emitter to collector. When a Flip Flop 201 drives an emitter, the built in output inverter amplifier of the Flip Flop must be counted as one of the three transistors. A fourth transistor can be used in series as a Pulse Gate.

The output (collector) of a Level Gate can drive (1) four bases of transistor inverters and (2) one emitter of a Level Gate or any number of emitters of Pulse Gates providing only one is pulsed at a time. The output (collector) of a Pulse Gate can drive one input to a pulsed unit.

Both polarities of logic can be utilized to make negative "or" s, negative "and" s, positive "or" s and positive "and" s.

The built in Pulse Gate inputs to the Flip Flop 201, Delay 301 Pulse Amplifier 601 and Tube Pulser 650 are all similiar to the inverters contained in Inverter Model 101. The built in inverter output amplifier of the Flip Flop 201 and Diode 110 are also similiar to the inverters contained in Inverter 101.

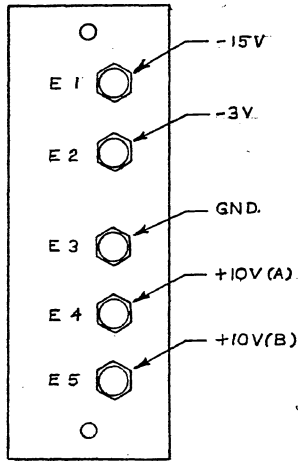
The maximum power requirements of the Inverter 101 package are:

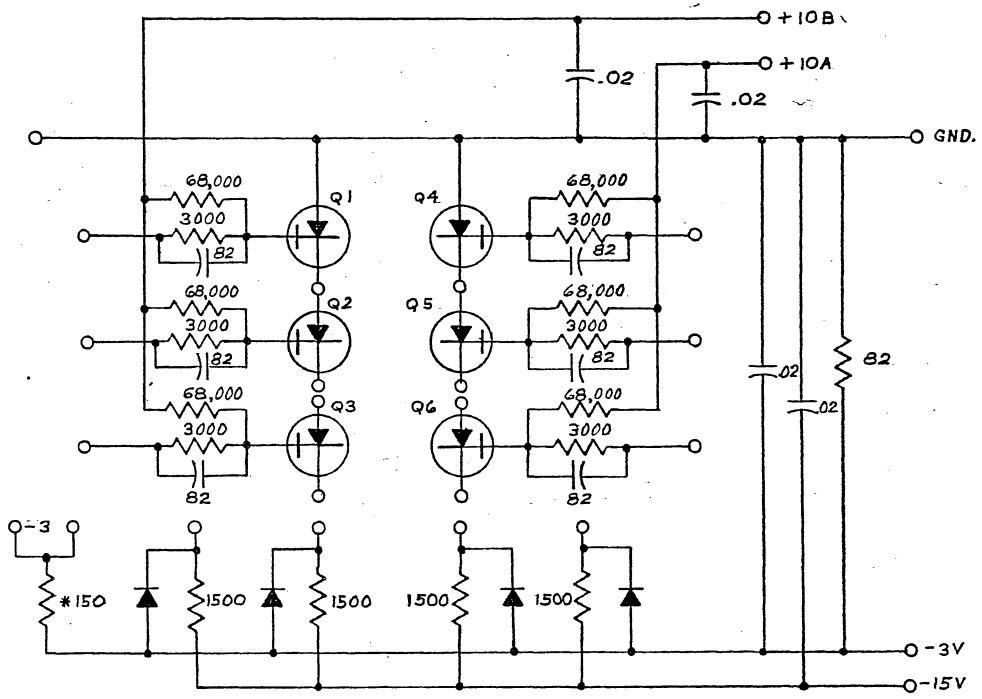
-3 volts	34 milliamperes
-15 volts	40 milliamperes
+10 volts	0.1 milliamperes

CIRCUIT SCHEMATIC: B-80563

B-80563

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY





(* RESISTOR NOT INCLUDED IN FIRST UNIT)

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS.
   B. CAPACITORS < 1 IN MICROFARADS.
   C. CAPACITORS > 1 IN MICROMICROFARADS
   D. DIODES ARE T1-G.
   E. TRANSISTORS ARE 2N 393

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC INVERTER 101 (B-00000-2 DIGITAL EQUIPMENT CORP.)

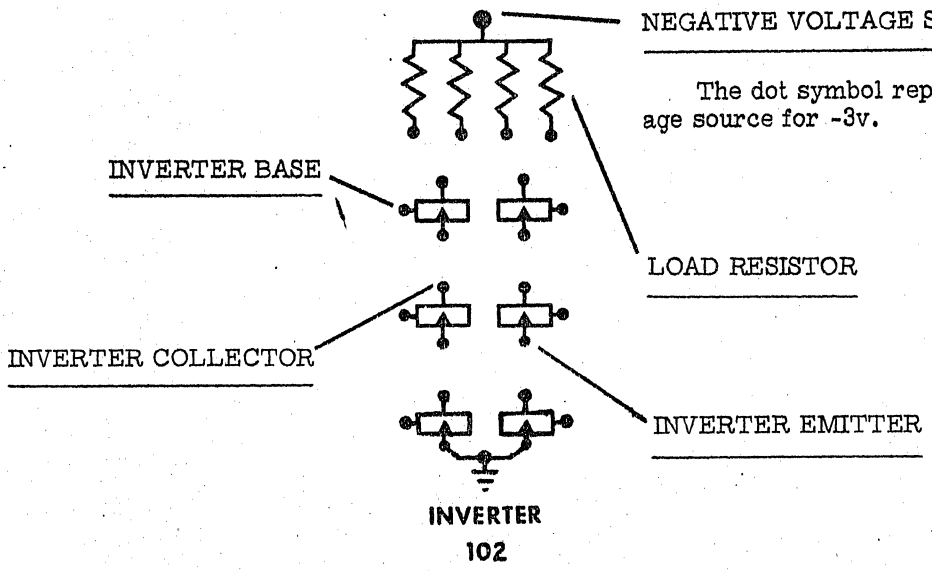
SCALE: —— DR. JAK 1-30-58

ENG. CK. APPD. 7-9-58

B-80563

CHG.	CN#	DATE	APPD.
-1	~	7-9-58	
-2			
-3			
-4			
-5			
-6			
-7			
-8			
-9			
-10			
-11			
-12			
-13			
-14			
-15			
-16			
-17			
-18			
-19			
-20			

Inverter 102 INSTRUCTIONS



The basic circuit used in doing logical operations with DEC Building Block Test Equipment is the transistor inverter. A PNP transistor is the main element of the inverter. In the notation of DEC for the inverter, the base is at the side of the rectangle, the emitter is at the bottom and the collector is at the top.

The Inverter 102 package contains six identical transistor inverters and four identical load resistors which are diode clamped at -3v.

The inverter acts like a switch, i.e. when the base is negative with respect to the emitter a "simple switch" between the emitter and collector is closed thus allowing current to flow. When the base is at the same or positive potential with respect to the emitter, there is no emitter to collector current.

The transistor inverter is used as either a Level Gate or a Pulse Gate. The load resistors can be used with Level Gates. When the inverters are used as Pulse Gates, the unit being pulsed replaces the load resistor. Pulses are applied only to the base of an inverter. See Section 30, pages 7 and 8.

The delay through a transistor depends on the capacitive loading and under typical conditions is approximately 20 millimicroseconds. Since each transistor is an amplifier, Level Gate Logic can be cascaded (collector to base) an indefinite number of stages without losing signal amplitude. The signal delays must be taken into consideration when a large number of stages are cascaded.

Not more than three transistors can be placed in series for Level Gate Logic, i.e. emitter to collector. When a Flip Flop 201 drives an emitter, the built in output inverter amplifier of the Flip Flop must be counted as one of the three transistors. A fourth transistor can be used in series as a Pulse Gate.

The output (collector) of a Level Gate can drive (1) four bases of transistor inverters and (2) one emitter of a Level Gate or any number of emitters of Pulse Gates providing only one is pulsed at a time. The output (collector of a Pulse Gate can drive one input to a pulsed unit.

Both polarities of logic can be utilized to make negative "or" s, negative "and" s, positive "or" s and positive "and" s.

The built in Pulse Gate inputs to the Flip Flop 201, Delay 301 Pulse Amplifier 601 and Tube Pulser 650 are all similiar to the inverters contained in Inverter Model 102. The built in inverter output amplifier of the Flip Flop 201 and Diode 110 are also similiar to the inverters contained in Inverter 102.

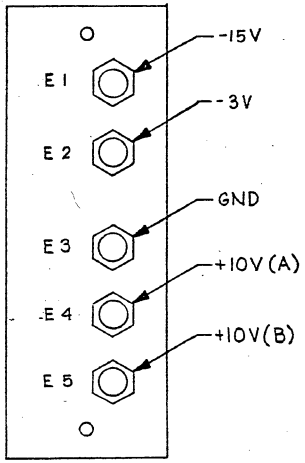
The maximum power requirements of the Inverter 102 package are:

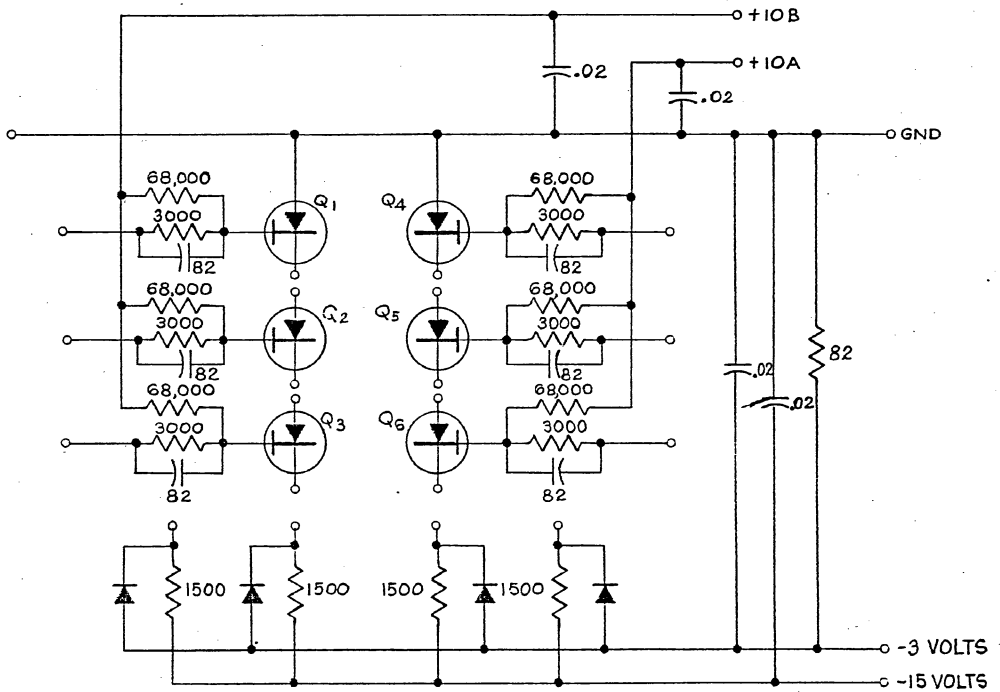
-3 volts	34 milliamperes
-15 volts	40 milliamperes
+10 volts	0.1 milliamperes

CIRCUIT SCHEMATIC : B-87305

B-87305

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY





NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS.
   B. CAPACITOR <1 IN MFD, >1 IN MMFD.
   C. DIODES ARE T1-G.
   D. TRANSISTORS ARE 2N393.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	CN#	DATE	APPD.
-1	1	9/23/59	[illegible]
-2			
-3			
-4			
-5			
-6			
-7			
-8			
-9			
-10			
-11			
-12			
-13			
-14			
-15			
-16			
-17			
-18			
-19			
-20			

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

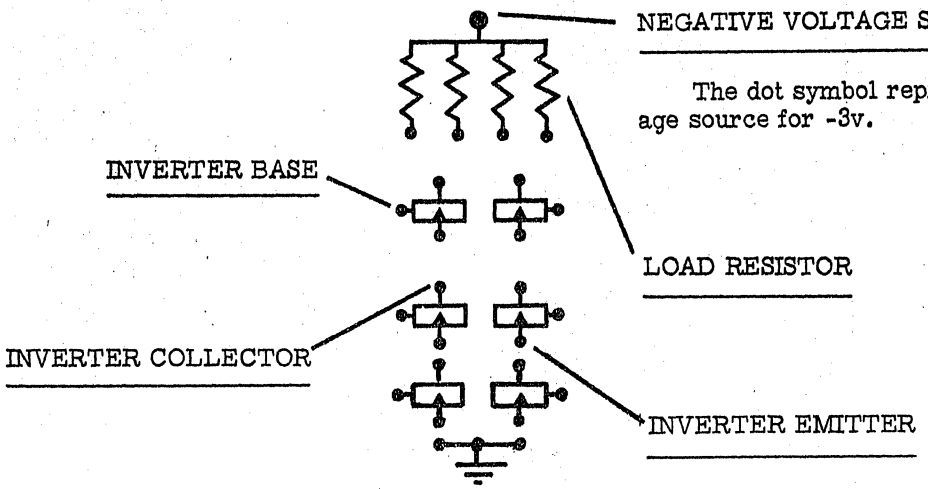
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73. MASS.

CIRCUIT SCHEMATIC INVERTER 102
(DIGITAL EQUIPMENT CORP.)

SCALE: _____ DR. S.A.R. 7/11/58
ENG. CK. APPD. 7-16-59

B- 87305

Inverter 103 INSTRUCTIONS



INVERTER 103

The basic circuit used in doing logical operations with DEC Building Block Test Equipment is the transistor inverter. A PNP transistor is the main element of the inverter. In the notation of DEC for the inverter, the base is at the side of the rectangle, the emitter is at the bottom and the collector is at the top.

The Inverter 103 package contains six identical transistor inverters and four identical load resistors which are diode clamped at -3v.

The inverter acts like a switch, i.e. when the base is negative with respect to the emitter a "simple switch between the emitter and collector is closed thus allowing current to flow. When the base is at the same or positive potential with respect to the emitter, there is no emitter to collector current.

The transistor inverter is used as either a Level Gate or a Pulse Gate. The load resistors can be used with Level Gates. When the inverters are used as Pulse Gates, the unit being pulsed replaces the load resistor. Pulses are applied only to the base of an inverter. See Section 30, pages 7 and 8.

The delay through a transistor depends on the capacitive loading and under typical conditions is approximately 20 millimicroseconds. Since each transistor is an amplifier, Level Gate Logic can be cascaded (collector to base) an indefinite number of stages without losing signal amplitude. The signal delays must be taken into consideration when a large number of stages are cascaded.

Not more than three transistors can be placed in series for Level Gate Logic, i.e. emitter to collector. When a Flip Flop 201 drives an emitter, the built in output inverter amplifier of the Flip Flop must be counted as one of the three transistors. A fourth transistor can be used in series as a Pulse Gate.

The output (collector) of a Level Gate can drive (1) four bases of transistor inverters and (2) one emitter of a Level Gate or any number of emitters of Pulse Gates providing only one is pulsed at a time. The output (collector) of a Pulse Gate can drive one input to a pulsed unit.

Both polarities of logic can be utilized to make negative "or" s, negative "and" s, positive "or" s and positive "and" s.

The built in Pulse Gate inputs to the Flip Flop 201, Delay 301 Pulse Amplifier 601 and Tube Pulser 650 are all similiar to the inverters contained in Inverter Model 103. The built in inverter output amplifier of the Flip Flop 201 and Diode 110 are also similiar to the inverters contained in Inverter 103.

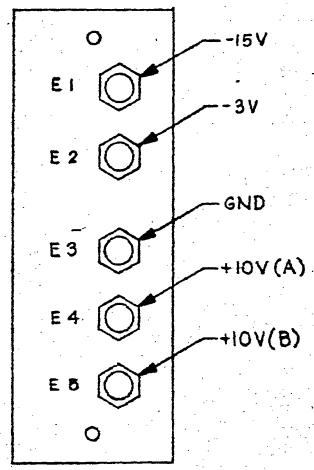
The maximum power requirements of the Inverter 103 package are:

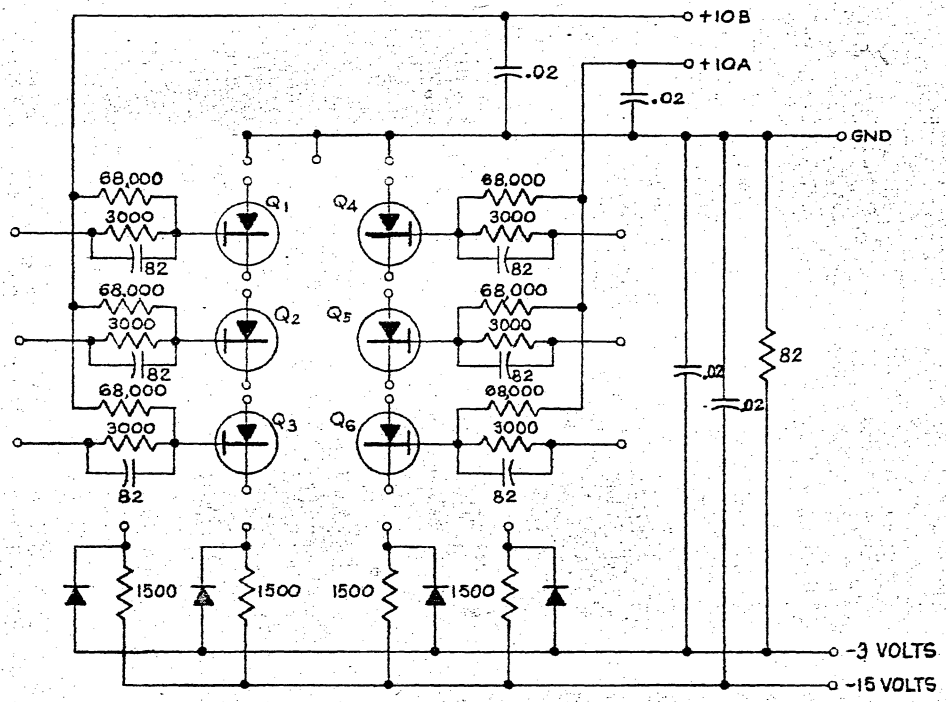
-3 volts	34 milliamperes
-15 volts	40 milliamperes
+10 volts	0.1 milliamperes

CIRCUIT SCHEMATIC: B-87656

B-87656

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY





NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS.
   B. CAPACITOR <1 IN MFD, >1 IN MMFD.
   C. DIODES ARE T1-G.
   D. TRANSISTORS ARE 2N393.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC INVERTER 103
(DIGITAL EQUIPMENT CORP.)

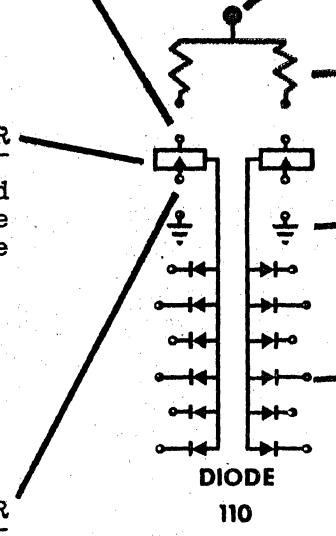
SCALE: DR. J.L.L. 9/23/58

ENG. 9/20/58 RLB CK. APPD. RLB

B-87656

CHG.	CN#	DATE	APPD.
-1	1	10/1/58	RLB

Diode 110 INSTRUCTIONS



INVERTER COLLECTOR

See Inverter 102 Instruction Sheet

NEGATIVE VOLTAGE SOURCE

The dot symbol represents a voltage source for -3v.

LOAD RESISTOR

INVERTER

The inverter is like those included in Model 102 Inverter except that the base is permanently tied to the diode gate.

GROUND TERMINAL

LEVEL INPUT TERMINALS

The six diode input terminals are for use with level signals such as tho(from the outputs from flip-flops, inverters, delays. Other DC signals that switch between ground and -3v can also be used.

INVERTER EMITTER

See Inverter 102 Instruction Sheet.

The Diode Model 110 package contains two 6 input diode "or" gates for negative levels each with an inverter amplifier. The user is reminded that an "or" circuit for negative signals is by definition and "and" circuit for positive signals. Since all DEC flip-flops have both polarities available and convenient inverters are available for all other logical signals, the Diode Model 110 can be used for either "and" or "or" type of logic.

The Diode unit is for use only with levels. When it is desired to read the logical result from a diode unit into a flip-flop, pulse delay, or any other unit requiring a pulse input, the emitter of the Diode inverter is grounded and the collector is connected to the emitter of an inverter used as a pulse gate. If the logical polarity is incorrect for this type connection, the collector of the Diode inverter is connected to the load resistor and to the base of a transistor inverter whose collector is connected to the emitter of a pulse gate.

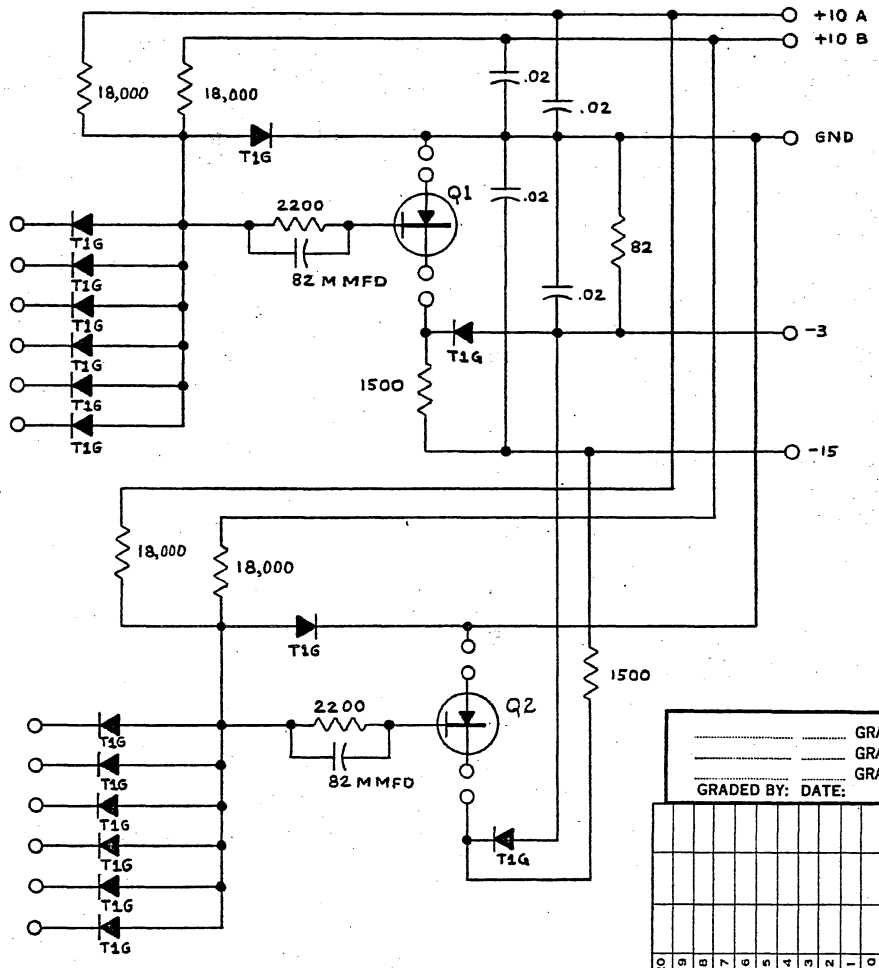
The power requirements of the Diode 110 are:

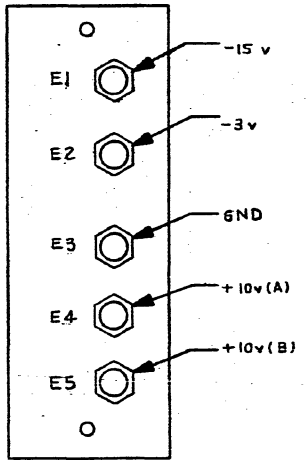
-3 volts	34 milliamperes
-15 volts	20 milliamperes
+10 volts	2.2 milliamperes

CIRCUIT SCHEMATIC : B-80565

B-80565

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY





NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS
   B. CAPACITORS ARE IN MICROFARADS.
   C. TRANSISTORS ARE 2N393.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	CN#	DATE	APPD.
-20 to -2			
-1	—	7.5.58	RLB

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC, DIODE UNIT 110
(8-00003 DIGITAL EQUIPMENT CORPORATION)

SCALE: | DR. B. TIBBETTS 12-1-58 | ENG. | CK. | APPD. 7-16-58 RLBeet

B-80565

BUILDING BLOCKS

Flip Flop 201 INSTRUCTIONS

INDICATOR

When FF is in a "one" state, the indicator bulb will be on.

ZERO OUTPUT TERMINAL

When FF is in a "one" state, this terminal will be at ground level.

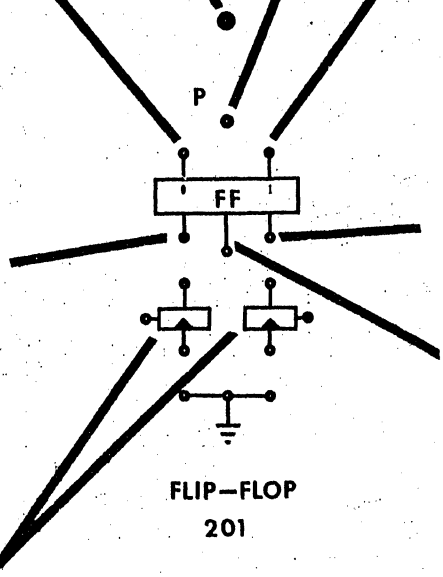
When FF is in a "zero" state, this terminal will be at -3v nominal voltage. This terminal can drive (1) ten bases of transistor gates and (2) two emitters of Level Gates or any number of emitters of Pulse Gates providing only one is pulsed at a time.

ZERO INPUT TERMINAL

The zero input terminal is pulsed whenever it is desired to place the FF in a "zero" state. The signal driving this terminal must come from the collector of a transistor gate. Each logical source of pulses must have its own transistor gate. Collectors of the transistor gates are tied in parallel when used in this mode.

INVERTERS

See Inverter 102 Instruction Sheet. Normally the inverters on this model are used as Pulse Gates.



FLIP—FLOP
201

"P" PULSE

The complement input terminal is transformer coupled to the "P" Pulse terminal so that when the complement input to the FF is pulsed, a standard -2.5v, 70 millimicrosecond pulse capable of driving one transistor base will appear on this terminal.

ONE OUTPUT TERMINAL

When FF is in a "one" state, this terminal will be at -3v nominal voltage.

When FF is in a "zero" state, this terminal will be at ground level. This terminal can drive (1) ten bases of transistor gates or any number of emitters of Level Gates or any number of emitters of Pulse Gates providing only one is pulsed at a time.

ONE INPUT TERMINAL

Similar to zero input terminal.

COMPLEMENT INPUT TERMINAL

Every time the complement input terminal is pulsed, the FF will go to the opposite state from what it held before the pulse. Input to this terminal must come from the collector of a transistor gate. Each logical source of pulses must have its own transistor gate. Collectors of the transistor gates are tied in parallel when used in this mode. Successive complement pulses must be at least 200 millimicroseconds apart for reliable operation.

The Flip-Flop Model 201 is basically a four transistor static flip-flop with built-in output amplifiers, indicator, source of counting carry pulses (P Pulse), complement input and two transistor gates. It has sufficient built-in gating to be used as one digit of a shift register, or one digit of a binary counter. It can also be used for all general type logical operations. It has a built-in delay of about 90 millimicroseconds, so that its output terminal can be sensed at the same instant that the input terminal is being pulsed.

The output voltage swing is diode clamped at -3v, to provide a constant output voltage independent of loading within the above specifications.

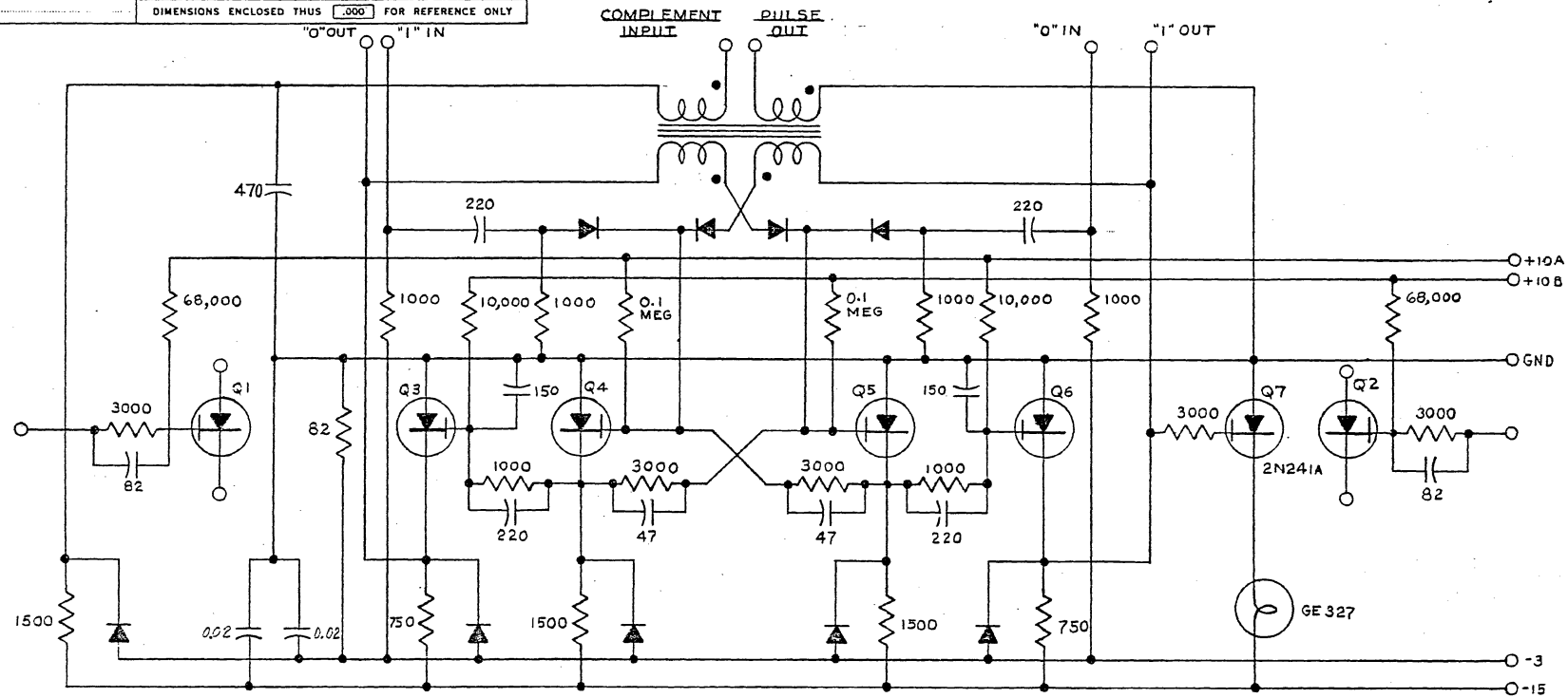
The power requirements of the Flip-Flop 201 are:

-3 volts	20 milliamperes
-15 volts	84 milliamperes
+10 volts	3 milliamperes

CIRCUIT SCHEMATIC: B-80564

B-80564

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS
   B. CAPACITORS < 1 IN MICROFARADS
   C. CAPACITORS > 1 IN MICROMICROFARADS
   D. DIODES ARE T1-G
   E. TRANSISTORS ARE 2N393

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC, FLIP-FLOP 201
(DIGITAL EQUIPMENT CORPORATION B-00001)

SCALE: _____ DR. BJ LOFGREN 1-30-58

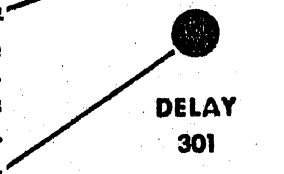
ENG. CK. APPD.

B-80564

CHG.	DATE	APPD.
-1	7.5.58	

BUILDING BLOCKS

Delay 301 INSTRUCTIONS



EXTERNAL PULSE GATE TERMINAL

Additional pulse gate collectors can be connected to this terminal to accomplish pulse mixing.

PULSE GATE BASE

Standard pulses are applied to this input terminal.

PULSE GATE EMITTER

Gating levels can be applied to this terminal. See Inverter 103 Instruction Sheet and Section 30, pages 7 and 8.

GROUND TERMINAL

EXTERNAL CAPACITOR TERMINAL

Longer delays than listed in table may be accomplished by connecting additional external capacitance between this point and the scale selection terminal.

POTENTIOMETER

The potentiometer provides continuous control over the length of the delay intervals.

LEVEL OUTPUT TERMINAL

When the input is pulsed, the level output at this terminal goes from ground to -3 volts for the duration of the delay. This level output can drive (1) 8 bases of transistor inverters and (2) one emitter of a level gate or any number of emitters of pulse gates providing only one is pulsed at a time.

PULSE OUTPUT TERMINAL

At the end of the negative level interval (above), a standard DEC pulse is produced at this terminal. This output will drive 10 pulse gates. Output impedance is 22 ohms.* (see footnote.)

SCALE SELECTION TERMINAL

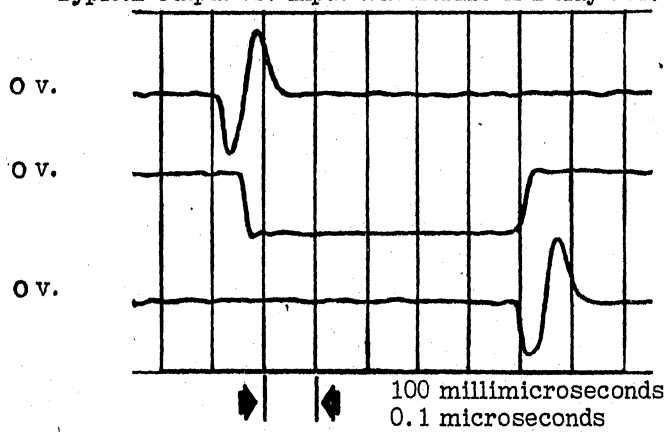
Capacitors are connected to this point (A internally connected as shown) to obtain delay intervals listed below:

CAPACITOR	MIN. DELAY	MAX. DELAY
A	0.2	2.5
B	2.2	34.
C	32.	550.

(delays in microseconds)

The Delay Model 301 package contains a monostable multivibrator circuit (one shot) and a pulse gate. The unit serves a dual purpose: 1.) to delay a standard pulse, and 2.) to produce a negative gating signal (a negative level for a predetermined interval). See typical waveforms below.

Typical Output vs. Input Waveforms of Delay 301.



Standard -2.5 volt DEC pulse. (at pulse gate base) — INPUT

Continuously variable -3v. delay — LEVEL OUTPUT

Standard -2.5 volt delayed pulse — PULSE OUTPUT

Long term variations in the selected delay time will not be greater than 10%. For accurate and stable delays, the recovery time (from end of one delay until beginning of next delay) should be of the same magnitude as the delay.

The power requirements of the Delay 301 are:

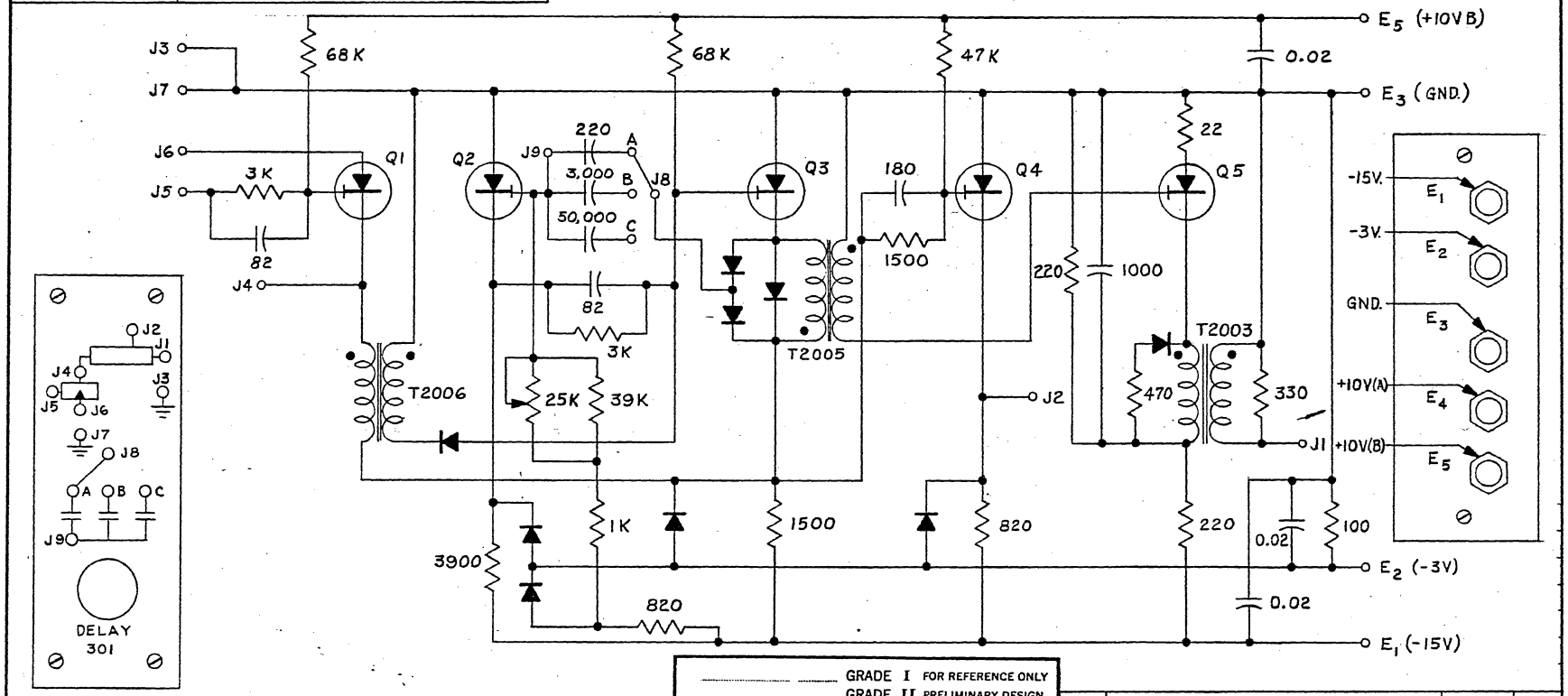
-3 volts	12 milliamperes
-15 volts	80 milliamperes
+10 volts	0.5 milliamperes

*Output impedance is defined as the terminating resistance which will halve the open circuit output voltage.

CIRCUIT SCHEMATIC: B-87306

B-87306

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS.
   B. CAPACITOR < 1 IN MFD, > 1 IN MMFD.
   C. DIODES ARE T1-G
   D. TRANSISTORS ARE 2N393.
   E. Q5 SELECTED TO HAVE < 15V PUNCH THRU.

CHG.	-20	-19	-18	-17	-16	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1
CN#																				
DATE																				
APPD.																				

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

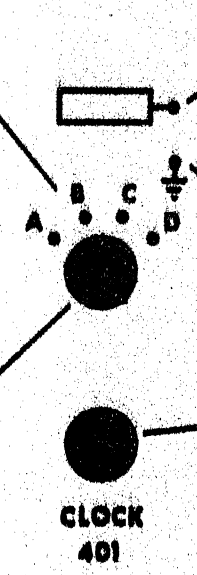
CIRCUIT SCHEMATIC, DELAY 301
(DIGITAL EQUIPMENT CORPORATION - B-00037)

SCALE: —— DR. JRK 7-21-58
ENG. CK. APPD. 7-22-58 RLB

B-87306

BUILDING BLOCKS

Clock 401 INSTRUCTIONS



FREQUENCY SCALES

The following pulse repetition frequencies are obtained:

Scale	Min. f	Max. f
A	500 cps.	5 kc.
B	5 kc.	50 kc.
C	50 kc.	500 kc.
D	500 kc.	5 mc.

Lower frequencies may be obtained by adding a capacitor internally in parallel with the capacitor for scale A.

SCALE SELECT

This control knob selects the four frequency ranges.

CLOCK PULSE OUTPUT TERMINAL

A standard -2.5 volt, 70 millimicrosecond DEC pulse is produced at this terminal. This pulse source can drive 10 units of load (10 pulse gate bases.)

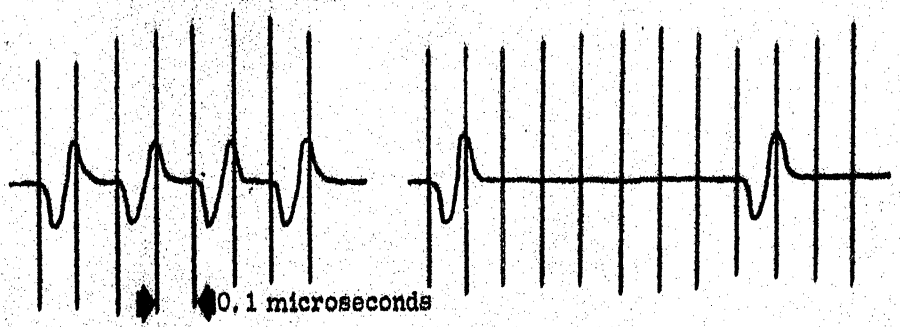
GROUND TERMINAL

POTENTIOMETER

This potentiometer provides continuous fine control over the frequency interval selected by the scale select knob.

The Clock Model 401 package contains a high stability multivibrator type variable frequency oscillator. The Clock is normally used as the generator of the standard DEC pulses. For a source of DEC Pulses synchronized to an external signal the Pulse Generator Model 410 should be used. Complete freedom for synchronous or asychronous operation is available with the Clock and Pulse Generator Model 410 as choices for sources of standardized pulses.

Typical selected frequency Clock 401 outputs:



Frequency setting is limited only by the fine control potentiometer. An Allen-Bradley composition potentiometer is used.

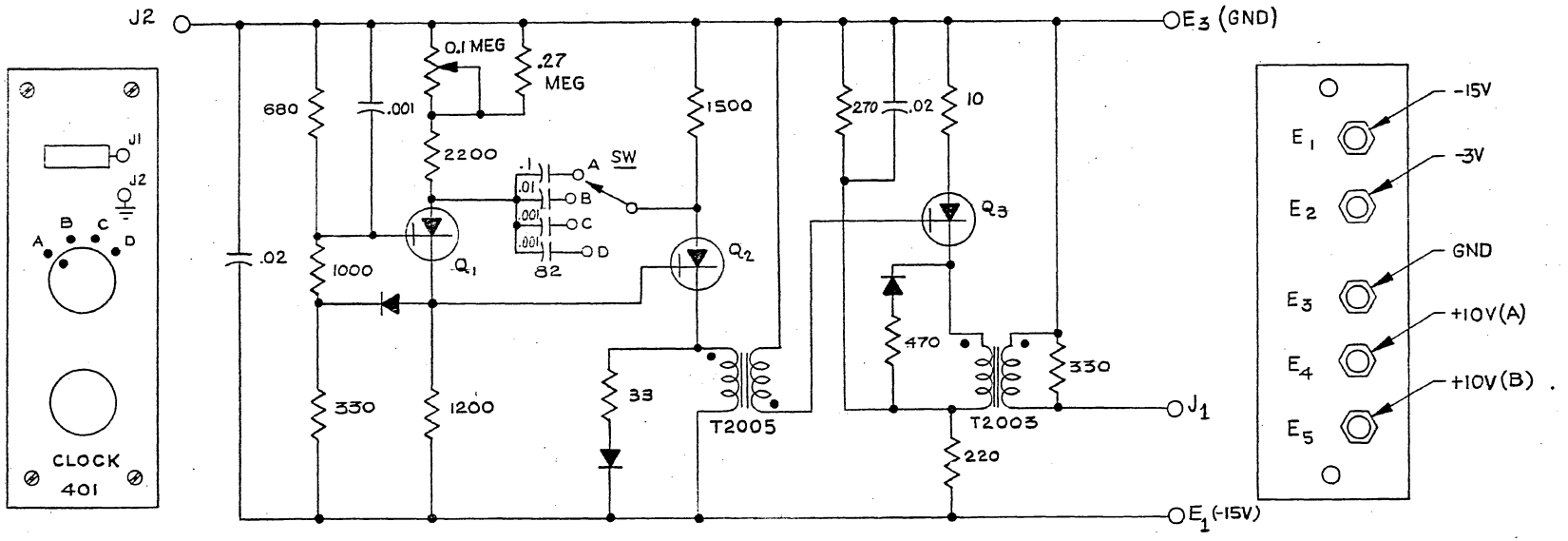
The power requirements of the Clock 401 are:

-3 volts	0 milliamperes
-15 volts	54 milliamperes
+10 volts	0 milliamperes

CIRCUIT SCHEMATIC: B-87307

B-87307

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS
   B. CAPACITORS ARE <1 IN MFD, >1 IN MMFD
   C. DIODES ARE T1-G
   D. TRANSISTORS ARE 2N393
   E. Q3 SHALL BE SELECTED TO HAVE >THAN 15V PUNCH THRU.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL-DESCRIPTION	PART NO.	QTY.

CHG.	-20	-19	-18	-17	-16	-15	-14	-13	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	DATE	APPD.
CH#																						

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC CLOCK MODEL 401
(B-00035-1 DIGITAL EQUIPMENT CORPORATION)

SCALE: — DR. H. FEWTRELL-7/14/58
ENG. CK. 7/14/58 WJS APPD. 7-15-58

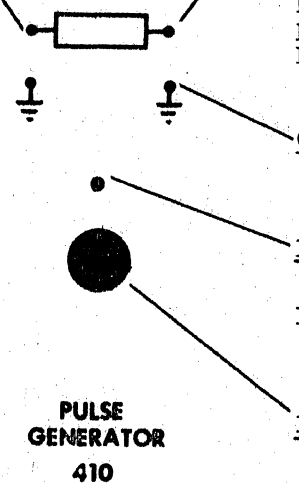
B-87307

BUILDING BLOCKS

Pulse Generator 410
INSTRUCTIONS

PULSE GENERATOR INPUT TERMINAL

When the input voltage goes more negative than -2.5 volts after having been more positive than -1.0 volts, a DEC Standard Pulse is produced at the output. The input is a D.C. connection, thus eliminating fall time as a characteristic of the incoming signal. Input impedance is 3000 ohms. Input signal should stay between limits of +10 volts and -10 volts.



OUTPUT TERMINAL

The output of the Pulse Generator is a DEC Standard Pulse (-2.5 volts, 70 millimicrosecond). The minimum time between pulses is limited to 1 microsecond. This pulse source can drive 10 units of load (10 DEC Pulse Gate bases).

GROUND TERMINAL

PUSH BUTTON SIGNAL

Can be connected to Pulse Generator Input Terminal for Manual operation.

PUSH BUTTON

Each time the button is firmly depressed, a Push Button Signal which meets the Pulse Generator input requirements is generated by an integrating circuit.

The Pulse Generator Model 410 is basically a Schmitt circuit with built in protection against generation of multiple pulses when the input signal is near -2.5 volts. This built in protection requires the input to go above -1.0 volt before the next pulse can be generated. It is used to provide signal compatibility between DEC Standard Signals and other types which meet the input requirement above. It is used for manual control of digital test sets or for providing synchronization with an external signal.

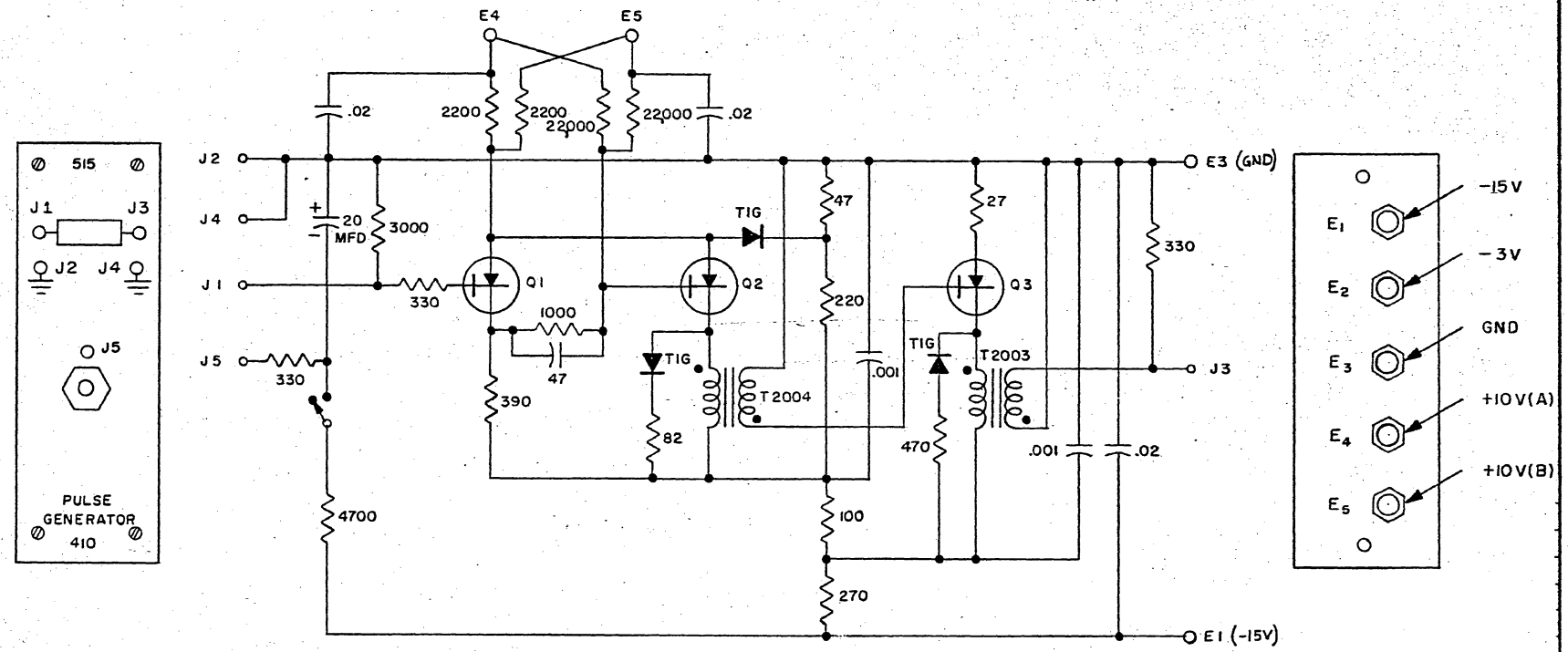
The power requirements of the Pulse Generator 410 are:

-3 volts	0 milliamperes
-15 volts	40 milliamperes
+10 volts	0.2 milliamperes

CIRCUIT SCHEMATIC: B-87308

B-87308

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A RESISTORS ARE IN OHMS
   - B CAPACITOR <1 IN MFD, >1 IN MMFD
   - C TRANSISTORS ARE 2N393
   - D Q 3 SELECTED TO HAVE <15 V PUNCH THRU.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	CN#	DATE	APPD.
-20 -19 -18 -17 -16 -15 -14 -13 -12 -11 -10 -9 -8 -7 -6 -5 -4 -3 -2 -1			

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

PULSE GENERATOR 410 CS (B-00026)

SCALE: _____ DR. BT 7-16-58 B-87308

ENG. CK. APPD. 7-16-58 R L B

BUILDING BLOCKS

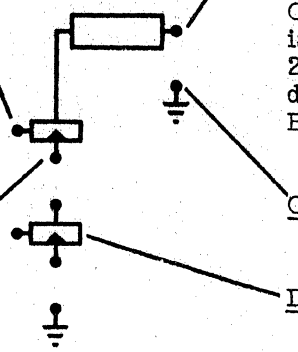
Pulse Amplifier 601 INSTRUCTIONS

PULSE GATE BASE

The input pulse must be negative and have a minimum amplitude of -2.0 volts and a maximum amplitude of -5.0 volts and should approach the general rise and fall time characteristics of DEC Standard Pulses. Input pulses of less than -0.5 volts will not generate an output pulse.

PULSE OUTPUT TERMINAL

A DEC Standard Pulse (-2.5 volts, 70 millimicroseconds) is produced at this terminal, everytime the signal on the Pulse Gate Base meets the input requirement. It is delayed from the input pulse by less than 20 millimicroseconds. This pulse can drive 16 units of Load (16 DEC Pulse Gate Bases).



GROUND TERMINAL

PULSE GATE EMITTER

Gating levels can be applied to this terminal. If no gating is used, this terminal must be grounded. See Inverter 103 Instruction Sheet.

INVERTER

This is a general purpose inverter similiar to those in Model 103. It is normally used here for making multiple level input gates for the pulse input. For details, see instruction sheet for Model 103.

PULSE AMPLIFIER 601

The Pulse Amplifier Model 601 is intended for use in standardizing DEC Pulses in amplitude and width. It has two inverters for gating the input included in the unit, one of which is permanently connected to the Pulse Amplifier. The output is used on the input Pulse Gate Bases of units such as the Delay 301, Flip Flop 201, Tube Pulser 650, or Pulse Amplifier 601. It is useful as a register driver for clearing, resetting or shifting a group of flip flops simultaneously.

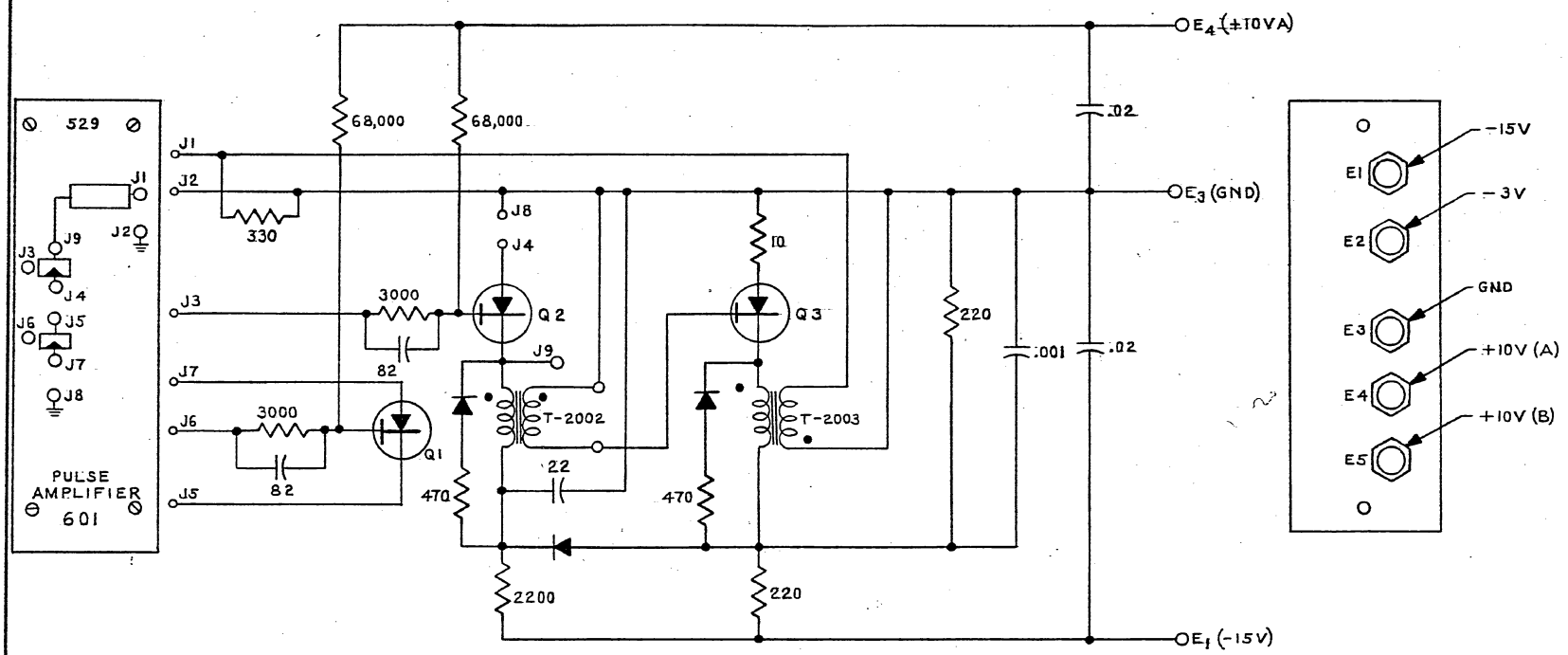
The power requirements of the Pulse Amplifier 601 are:

-3 volts	0 milliamperes
-15 volts	40 milliamperes
+10 volts	0.5 milliamperes

CIRCUIT SCHEMATIC: B-80566

B-80566

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS.
   B. CAPACITORS <1 IN MFD, >1 IN MMFD.
   C. DIODES ARE T1-G
   D. Q2 & Q3 ARE SELECTED TO HAVE >THAN 15V PUNCH THRU.
   E. TRANSISTORS ARE 2N393.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
-19			
-18			
-17			
-16			
-15			
-14			
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-1			

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CS, PULSE AMPLIFIER 601
(DIGITAL EQUIPMENT CORP. B-00004)

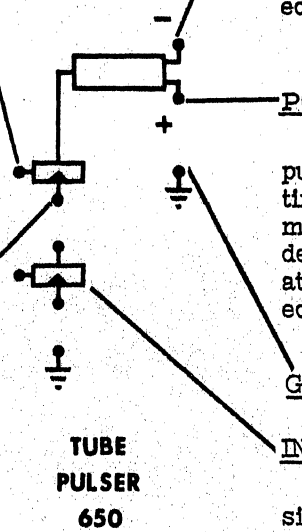
SCALE: —— DR. JLOFGREN-1-29-58

ENG. CK. APPD. 2-16-58 RLB

B-80566

BUILDING BLOCKS

Tube Pulser 650
INSTRUCTIONS



PULSE GATE BASE

The input pulse must be negative and have a minimum amplitude of -2.0 volts and a maximum amplitude of -5.0 volts and should approach the general rise and fall time characteristics of DEC Standard Pulses. Input pulses of less than 0.5 volts will not generate an output pulse. The upper pulse repetition frequency of this unit is 1 megacycle.

PULSE GATE EMITTER

Gating levels can be applied to this terminal. If gating is not used, this terminal must be grounded. See Inverter 103 Instruction Sheet.

NEGATIVE PULSE OUTPUT

A negative 15 volt, 0.1 microsecond pulse is produced at this terminal everytime the signal on the Pulse Gate Base meets the input requirement. When it is desired to use this negative pulse, the Positive Pulse Output terminal must be grounded.

POSITIVE PULSE OUTPUT

A positive 15 volt, 0.1 microsecond pulse is produced at this terminal everytime the signal on the Pulse Gate Base meets the input requirement. When it is desired to use this positive pulse, the Negative Pulse Output terminal must be grounded.

GROUND TERMINAL

INVERTER

This is a general purpose inverter similar to those in Model 103. It is normally used here for making multiple level input gates for the pulse input. For details, see instruction sheet for Model 103.

The Tube Pulser Model 650 contains a power amplifier and two inverters for gating the input, one of which is permanently connected to the Tube Pulser. It is useful in providing signal compatibility between DEC Standard Pulses and other types of digital circuits requiring larger signals, such as vacuum tube circuits. Either negative or positive pulses are available.

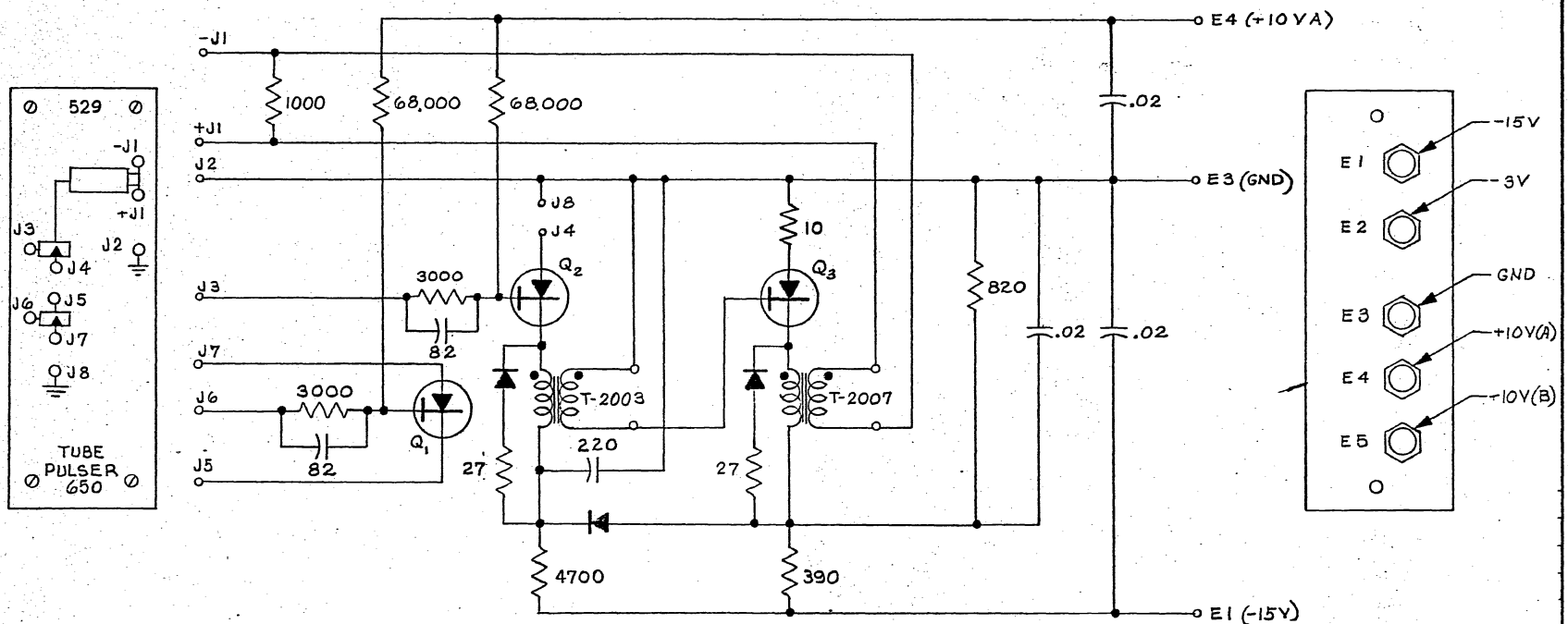
The power requirements are:

-3 volts	0 milliamperes
-15 volts	17 milliamperes
+10 volts	0.2 milliamperes

CIRCUIT SCHEMATIC: B-87309

B-87309

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS.
   B. CAPACITOR <1 IN MFD, >1 IN MMFD.
   C. DIODES ARE T1-G.
   D. TRANSISTORS ARE 2N393.
   E. Q_2 & Q_3 ARE SELECTED TO HAVE > 15 V PUNCH THRU.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	CN#	DATE	APPD.
-1	1	7/21/59	L.L.E.
-2 to -20			

ITEM	MATERIAL-DESCRIPTION	PART NO.	QTY.

LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

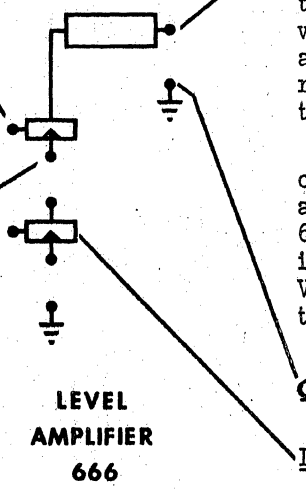
CIRCUIT SCHEMATIC TUBE PULSER 650
(DIGITAL EQUIPMENT CORPORATION B-00055)

SCALE: ——— DR. S.A.R. 7/14/59
ENG. CK. APPD. 7-16-59 L L Ellis

B-87309

BUILDING BLOCKS

Level Amplifier 666
INSTRUCTIONS



LEVEL GATE BASE

Standard DEC Levels (ground and -3 volts) are applied to this terminal from outputs such as Flip-Flop 201, Inverter 103 when used as a Level Gate, Delay 301, (Level Output), Diode 110. See Inverter 103 Instruction Sheet.

LEVEL GATE EMITTER

Same as above. This terminal must be at ground level if the Level Gate Base is to have any effect.

LEVEL OUTPUT TERMINAL

When the input base is at -3 volts and the input emitter is at ground, the output will be at ground. When the input base is at ground, the output will be at -15 volts regardless of the state of the input emitter.

Output impedance of this unit is 1500 ohms. Unloaded rise and fall times are approximately 20 millimicroseconds and 60 millimicroseconds respectively. Delay is approximately 40 millimicroseconds. When output is loaded with 47 mmf, the fall time becomes 130 millimicroseconds.

GROUND TERMINAL

INVERTER

This is a general purpose inverter similar to those in Model 103. It is normally used here for making multiple level input gates. For details, see instruction sheet for Model 103.

The Level Amplifier Model 666 contains an amplifier for converting 3 volt digital signals (0 to -3 volts) to 15 volt digital signals (0 to -15 volts). It has two inverters for gating the input, one of which is permanently connected to the Level Amplifier. It is useful in providing signal compatibility between DEC Standard Pulses and other types of digital circuits requiring larger signals, such as vacuum tube circuits.

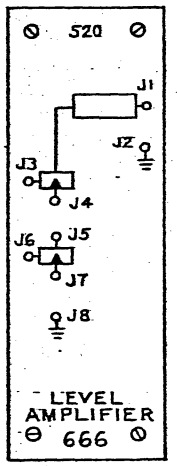
The power requirements are:

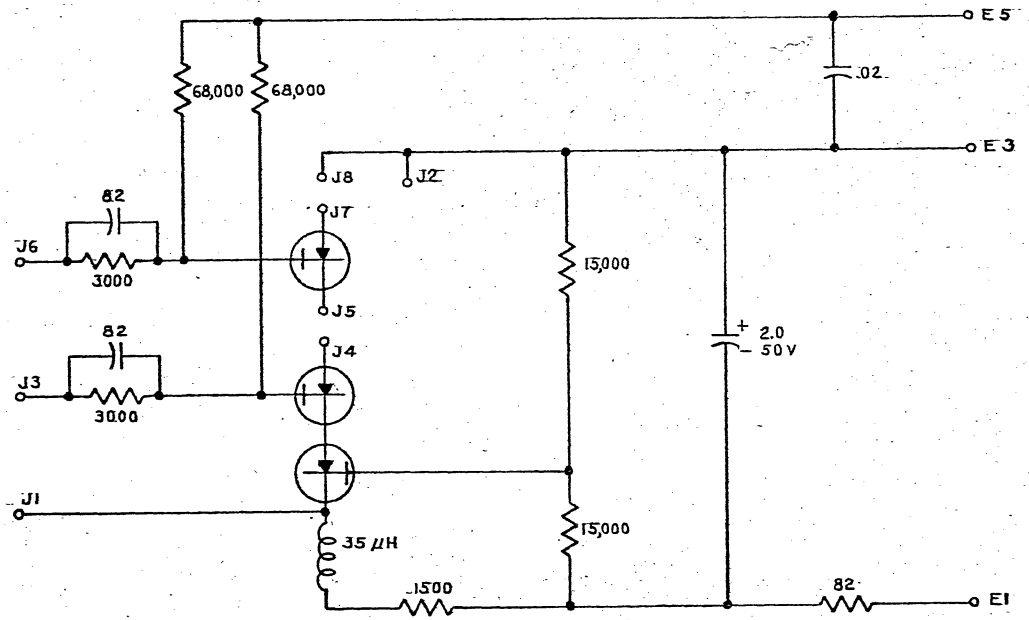
-3 volts	0 milliamperes
-15 volts	10 milliamperes
+10 volts	0.02 milliamperes

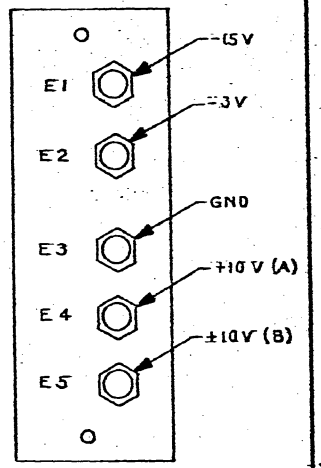
CIRCUIT SCHEMATIC: B-87310

B-87310

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS [.000] FOR REFERENCE ONLY







NOTES

1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS
   B. CAPACITOR <1 IN MFD, >1 IN MMFD
   C. TRANSISTORS ARE 2N393.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.
-			

CHG.	CN#	DATE	APPD.
-20			
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LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

LEVEL AMPLIFIER 666 C.S.
(DIGITAL EQUIPMENT CORP. B-00025)

SCALE: DR. J. LOFGREN 7-15-58
ENG. CK. APPD. 7-15-58 R.L. Reed

B-87310

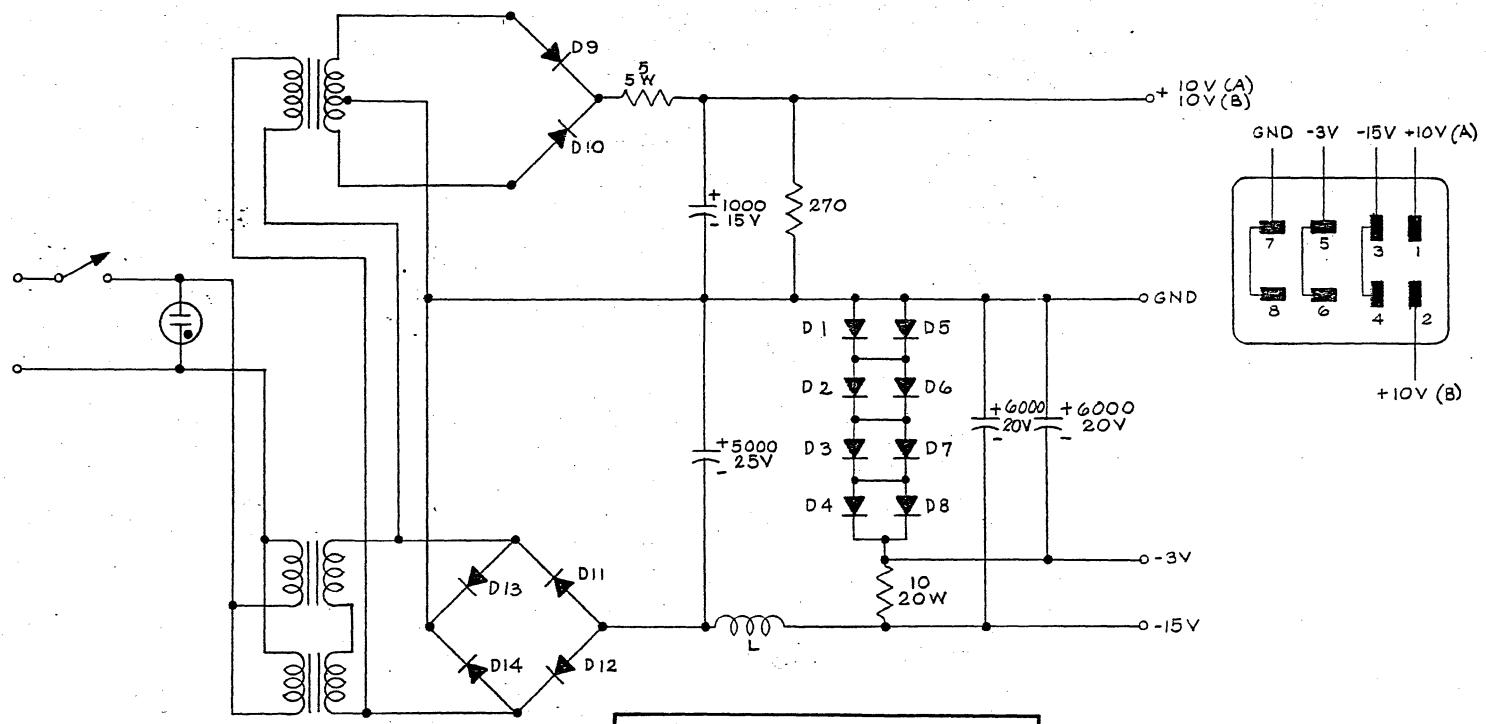
The power supply generates all voltages needed to operate the DEC building blocks. The capacity of the supply varies with serial and type number as below:

Model No.	Serial No.	V (volts)	I (amps)
720	1-535	+10	0.09
		-3	0.8
		-15	3.0
720	536 and up	+10	0.09
		-3	0.8
		-15	4.5
721	all	+10	0.09
		-3	1.2
		-15	4.5

Circuit Schematic of Type 720: B-87311

B-87311

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED
   A. RESISTORS ARE IN OHMS.
   B. CAPACITORS ARE IN MFDS.
   C. DIODES D1 THRU D4 & D11 THRU D14 ARE — 341-A,
      D5 THRU D8 ARE — 305-A,
      D9 & D10 ARE — 320-A.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

CHG.	CN#	DATE	APPD.
-20			
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LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC POWER SUPPLY MODEL 720
(DIGITAL EQUIPMENT CORPORATION B-00040)

SCALE: _____ DR. S. A. R. 7/14/58

ENG. CK. APPD. R.L.B.

B-87311

BUILDING BLOCKS

Relay 801 INSTRUCTIONS

RELAY COMMON CONTACT (J2)

This is the pole of a single pole double throw relay which has contacts rated at 2 amperes.

RELAY NORMALLY CLOSED CONTACT (J1)

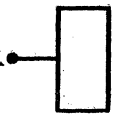
When the input level is at ground (or absent), a closed path exists between this terminal and J2.

LEVEL INPUT TERMINAL

The input to this terminal is a DEC Standard Level (ground or -3 volts). This input represents the equivalent load of 1 inverter base. If other input signals are used, they should stay between limits of +5 volts and -10 volts.

RELAY NORMALLY OPEN CONTACT (J3)

When the input level is at -3 volts, a closed path exists between this terminal and J2.



RELAY 801

The Relay 801 package contains a relay driver amplifier and a single pole double throw relay. The purpose of this unit is to enable DEC Building Blocks circuitry to drive electromechanical units requiring power beyond the driving capabilities of regular transistor circuitry.

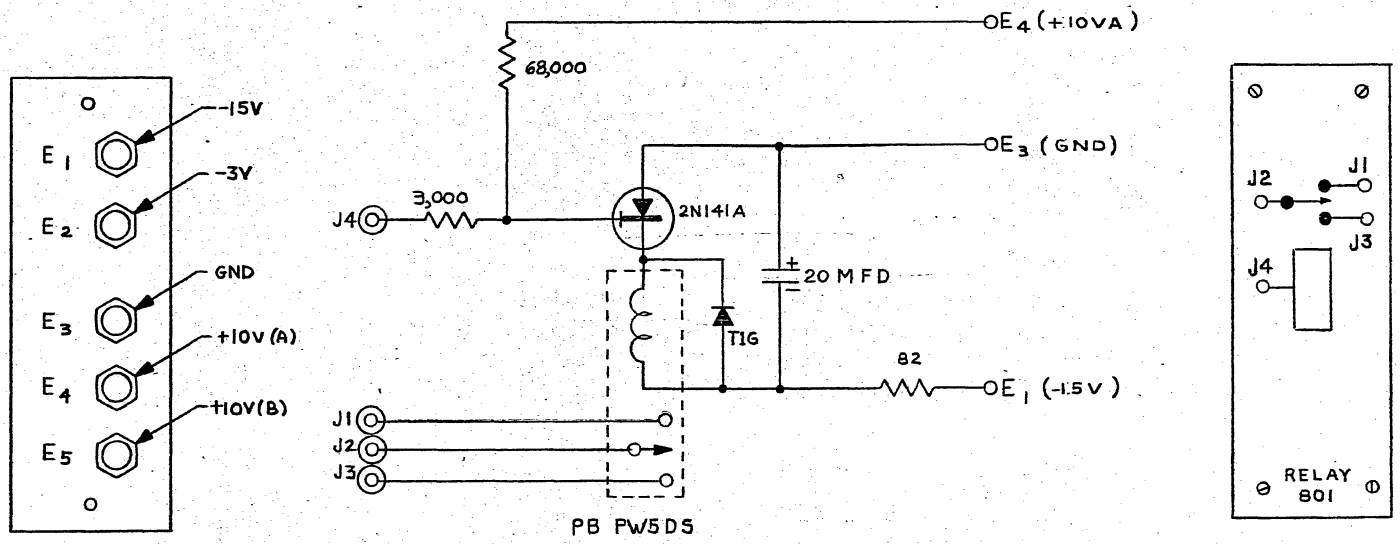
The Relay 801 maximum power requirements are:

-3 volts	0 milliamperes
-15 volts	19 milliamperes
+10 volts	.02 milliamperes

CIRCUIT SCHEMATIC: B-87312

B-87312

TOLERANCES NOT OTHERWISE SPECIFIED
DECIMAL ± .005 FRACTIONAL ± 1/64 ANGULAR ± ½°
DIMENSIONS ENCLOSED THUS .000 FOR REFERENCE ONLY



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. RESISTORS ARE IN OHMS.

GRADE I FOR REFERENCE ONLY
GRADE II PRELIMINARY DESIGN
GRADE III FINAL DESIGN
GRADED BY: DATE:

CHG.	APPD.	DATE	CN#
-20			
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-3			
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-1			

ITEM	MATERIAL - DESCRIPTION	PART NO.	QTY.

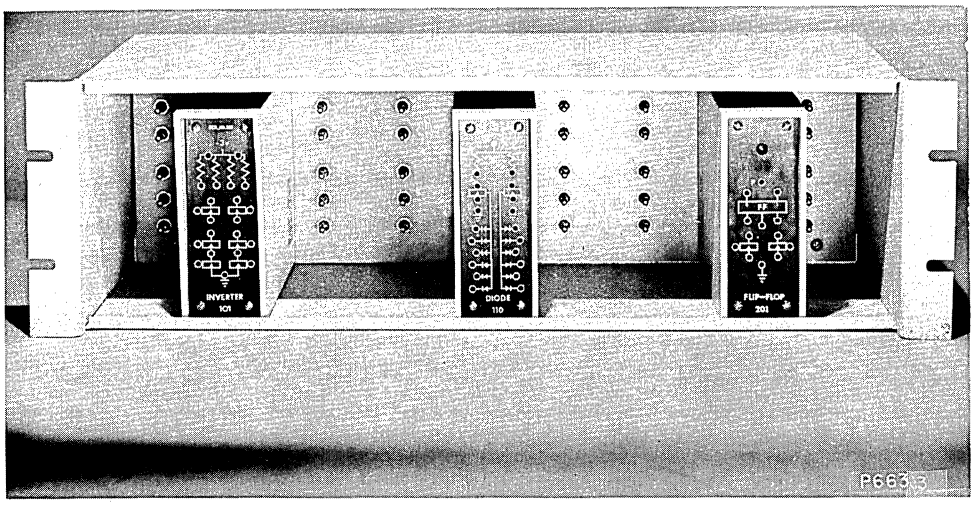
LINCOLN LABORATORY DIV. 6
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON 73, MASS.

CIRCUIT SCHEMATIC, RELAY UNIT 801
(B-00005 DIGITAL EQUIPMENT CORPORATION)

SCALE: DR: J. ALLEN 7-14-58
ENG. CK. APPD. 7-16-58 R.L.B.J.

B-87312

MOUNTING PANEL
901



Description:

The mounting panel is 5-3/16" x 8-5/8" and mounts in a standard 19" relay rack. It will hold nine DEC Building Blocks and has all of the necessary plugs for bringing power to the units. Each voltage is filtered within the panel to prevent noise transients.