PDP-1 COMPUTER
ELECTRICAL ENGINEERING DEPARTMENT
M.I.T.
CAMBRIDGE 39, MASSACHUSETTS

PDP-12

PDP-1 MAGNETIC DRUM STORAGE

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The PDP-1 computer is now equipped with a high-speed magnetic drum storage. The drum is divided into 22_{10} fields of 4096 words each. Words are transferred between the drum and the core memory under automatic control. Because the drum runs at 30 revolutions per second, each word on the drum is available once every 33-1/3 milliseconds; but when a drum operation has begun, words are transferred at a rate of 8.16 microseconds each. In a single operation, information can be written on the drum, read from the drum, or both simultaneously.

Each field has a five-bit address and each word in a given field has a twelve-bit address. By use of the instructions below, the programmer specifies a drum field, an initial word address, an initial core memory address, the number of words to be transferred, and whether the operation is to write on the drum, read from the drum, or swap the contents of core memory with the contents of the drum.

The following instructions have been added to the PDP-1:

dia (iot 60) [drum initial address] Causes the $C(IO)_{1-5}$ to be sent to the drum write field buffer. These bits specify which field of the drum will be written on during the next dcc instruction; or, if $C(IO)_{1-5}=0$, that no write operation is to occur. The $C(IO)_{6-17}$ are sent to the drum initial address register to specify the first drum address to be transferred.

dba (iot 61) [drum break on address] Causes the $C(IO)_{6-17}$ to be sent to the drum initial address register. When the current drum address becomes equal to the contents of the initial address register, a sequence break request is indicated.

Bit 5 of the status word is set by the break, and is cleared by the next dcc instruction.

dcc (iot 62) [drum count and commence] Causes the $C(IO)_{1-5}$ to be sent to the drum read field buffer. These bits specify which field will be read; or, if $C(IO)_{1-5}=0$, that no read operation is to occur. The $C(AC)_{6-17}$ specify the first core memory address of the data to be transferred. The $C(IO)_{6-17}$ specify the number of words to be transferred. If the $C(IO)_{6-17}=0$, 4096 words are transferred. While the dcc instruction is being executed, the computer stops and the drum system takes full control of the core memory. Successive words are transferred from sequential locations until the operation is complete. If no errors occurred during the drum operation, the instruction following the dcc will be skipped. The C(AC) and C(IO) are lost during this operation. If both the read field and write field are non-zero (both reading and writing operations are specified) the contents of memory are written on the write field; then the read field data are read into memory. The read field must not equal the write field.

In order to avoid passing a given drum address, and hence losing 33 milliseconds, the dcc instruction must be given at least 250 microseconds before the drum address reaches the initial address.

dra (iot 63) [drum read address] Causes the current drum address to be read into IO_{6-17}. The parity error flag is read into IO_0; the write error flag is read into IO_1; and the timing error flag is read into IO_2. Two cycles elapse before this information is placed in the IO.

The various error conditions are as follows:

Read Error: When a word is written on the drum, its parity is generated and is also written on the drum. Whenever this word is read off the drum, a new parity is generated and is checked against the parity just read. A mismatch sets the read error flip flop.

Selection Error: A 5-bit address can specify 32 drum fields out of which 23 are legal and 9 and illegal. Field 0 means no selection, fields 1 through 22 are legal fields and fields 23 through 32 are illegal fields. A selection error flip flop will be set if a user selects an illegal field.

Timing Error: This error monitors the drum clock circuit malfunctions. The timing error flip flop will be set when (1) the time period between consecutive clock pulses is not equal to ~ 8.2 μs, (2) number of clock pulses available on drum is not equal to 4096 and (3) the reference index pulse is lost.

Alan Kotok, David Gross and
Gary Wang

Approved J. Dennis

J. B. Dennis