

**VME10  
SYSTEM  
CONTROL  
MODULE**

**VME/10  
Microcomputer System  
System Control Module  
User's Manual**



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VME/10  
MICROCOMPUTER SYSTEM  
SYSTEM CONTROL MODULE  
USER'S MANUAL

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First Edition

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## PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (\*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (\*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

Refer to the VME/10 Microcomputer System Equipment Manual, publication number M68KVSEM, for all external signal and power wiring information to the System Control Module (SCM).

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## CHAPTER 1

### GENERAL INFORMATION

#### 1.1 INTRODUCTION

This manual provides general information and hardware configuration, functional description, and support information for the System Control Module (SCM).

#### 1.2 SPECIFICATIONS

The SCM specifications (which are subject to change without notice) are given in Table 1-1.

TABLE 1-1. SCM Specifications

CHARACTERISTICS	SPECIFICATIONS
Microprocessor	MC68010
Power requirements (for board components only)	+5 Vdc, 15 A (max.) +12 Vdc, 0.48 A (max) -12 Vdc, 0.024 A (max.)
ROM/PROM/EPROM	Two sockets for 16K or 32K bytes (for bootload, etc.).
Dynamic RAM	384K bytes (used for system RAM and graphics) dual ported (to onboard MPU, to VMEbus).
Character generator RAM	2K byte static RAM (used to define character fonts).
Attribute generator RAM	2K byte static RAM (used to define cursors, underline character, inverse video character, and inverse video screen).
Character/display RAM	2K word static RAM (optionally 4K words) (used to call the character wanted from the character generator RAM and to define its associated attribute).
Interrupt handler	22 sources of interrupts to the MC68010.
CRT controller	MC68A45 (used by software to define the video screen).
Time-of-day clock	MC146818 (has real time clock plus 50 bytes of general purpose RAM.) Battery backed up allowing up to five days data retention on power down if batteries are charged.
I/O Channel interface	I/O Channel master interface.

TABLE 1-1. SCM Specifications (cont'd)

CHARACTERISTICS	SPECIFICATIONS
VMEbus interface:	
Address and data bus interface	Interfaces onboard data and address buses to VMEbus data and address buses and controls handshaking between the two.
Interrupter	7-level VMEbus interrupter (level is software programmable).
Requester	Software selectable to release on request, release when done, release on BCLR*, or release never.
Arbiter	Full VMEbus arbiter arbitrates all four levels.
Keyboard interface	MC2661B (uses RS-422 type buffers to serial bus).
Reset	Connector provided for RESET switch, power-on-reset circuit on board.
Software abort	Connector provided for Software ABORT switch.
Keyboard lock	Connector provided for KYBD LOCK key switch.
Operating temperature	0° to 70° C.
Storage temperature	-40° to 85° C.
Relative humidity	0% to 90% noncondensing.
Physical characteristics:	
Height	12 in. (304.8 mm)
Width	16.5 in. (419.1 mm)
Thickness	0.60 in. (152.4 mm)



### 1.3 GENERAL DESCRIPTION

The SCM is an advanced VMEbus-compatible microcomputer module which is used for system requirements of the VME/10.

When installed in its chassis and provided with power, peripherals, and a program, the SCM makes a complete MC68010 system.

The SCM contains an MC68010, a battery backed up time-of-day clock, a keyboard interface, an I/O Channel interface, a VMEbus interface, a color or monochrome video interface, and an operator panel interface. The I/O interface is used for such functions as floppy or Winchester disk controllers, serial ports, and parallel ports. The VMEbus interface is used for such functions as multiprocessors, RAM boards, or ROM boards.

# **HDWE CONFIG.**

## CHAPTER 2

### HARDWARE CONFIGURATION

#### 2.1 INTRODUCTION

This chapter provides hardware configuration information for the SCM.

#### 2.2 HARDWARE CONFIGURATION

Figure 2-1 illustrates the location of the headers, sockets, and connectors. The VME/10 is shipped with factory-installed jumper configurations for normal development system operation. A list of the headers is shown below:

- a. Status bits select (J2)
- b. ROM type select (J9)
- c. MPU clock frequency select (J10)
- d. I/O Channel enable select (J11)
- e. Time-of-day clock power source select (J15)

##### 2.2.1 Status Bits Select Header (J2)

Bits 5, 6, and 7 of the status register may individually set as a 1 or as a 0 by the jumpers on header J2. Bit 5 is used by TEnbug to bypass the power-up test. Bit 7 is used to select color or monochrome display. Bit 6 is user-defined. As shown in Figure 2-2, the VME/10 is shipped with the jumpers positioned for all ones.

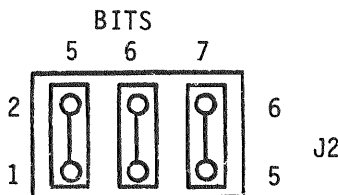


FIGURE 2-2. Status Bits Select Header (J2)

##### 2.2.2 ROM Type Select Header (J9)

Header J9 must be configured to allow operation with the type of ROM/EPROM device used in sockets U239 and U251. Figure 2-3 shows the factory configuration for MCM68366 ROM devices in U239 and U251. Table 2-1 lists the devices which may be used.

#### NOTE

Any device used must have an access time shorter than or equal to the MPU clock speed.

450 nanoseconds = 8 MHz  
350 nanoseconds = 10 MHz

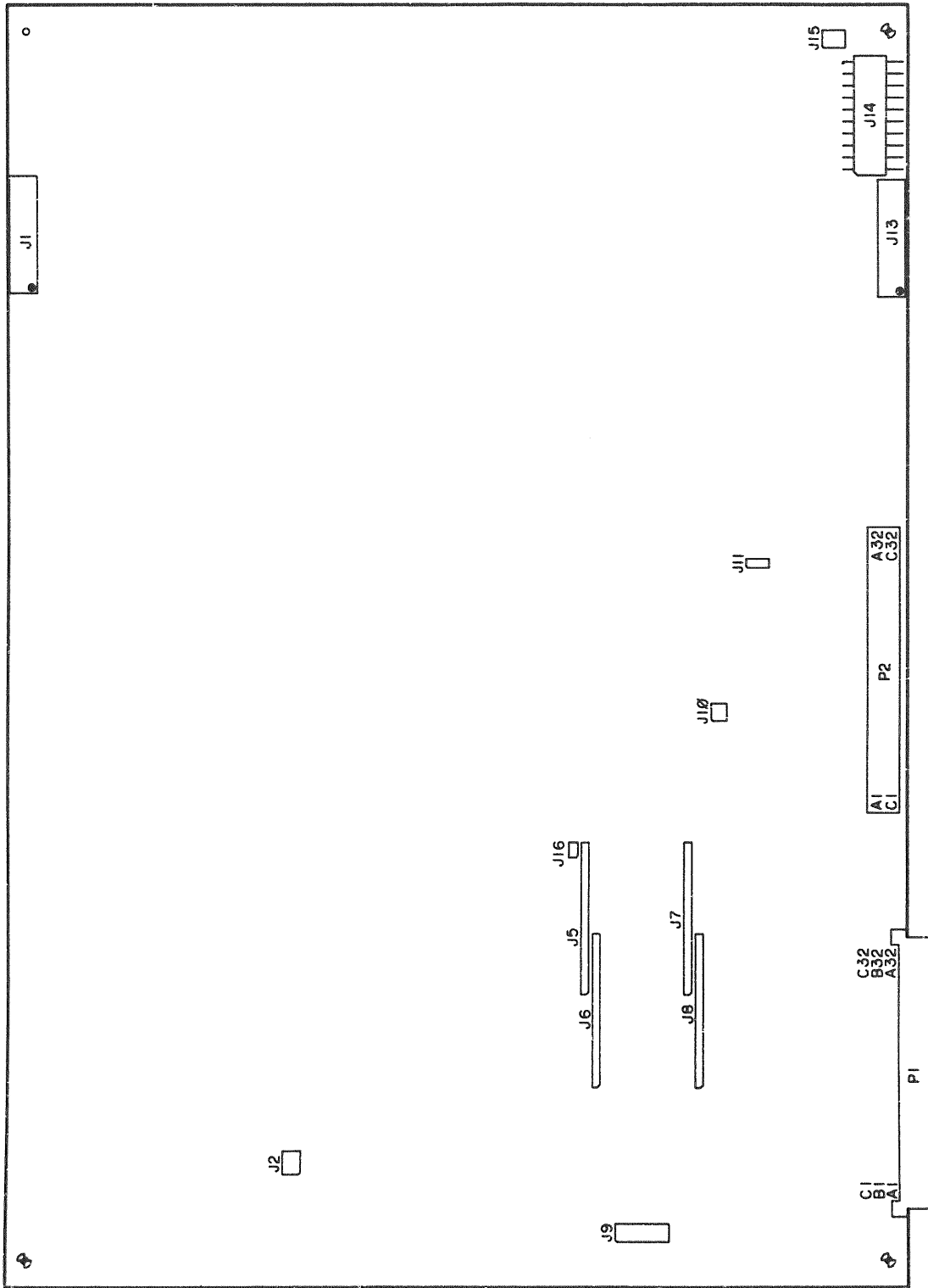


FIGURE 2-1. SCM Option Locations

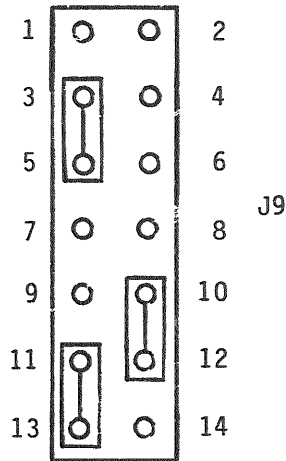


FIGURE 2-3. ROM Type Select Header (J9)

TABLE 2-1. ROM and EPROM Devices

PART NUMBER	TYPE	SIZE	JUMPERS
<u>MOTOROLA</u>			
MCM68364	ROM	8K x 8	3-5, 10-12, 11-13
MCM68365	ROM	8K x 8	3-5, 10-12, 11-13
MCM68366	ROM	8K x 8	3-5, 10-12, 11-13
MCM68764	EPROM	8K x 8	3-5, 10-12, 11-13
MCM68766	EPROM	8K x 8	3-5, 10-12, 11-13
<u>MOSTEK</u>			
MK276X	EPROM	8K x 8	9-10, 11-12, 13-14
MK37000	ROM	8K x 8	9-10, 11-12, 13-14
<u>TEXAS INSTRUMENTS</u>			
TMS4764	ROM	8K x 8	3-5, 10-12, 11-13
TMS2564	EPROM	8K x 8	3-5, 4-14(1), 7-9, 10-12, 11-13
<u>INTEL</u>			
I2764	EPROM	8K x 8	5-7, 9-10, 11-12, 13-14
I27128	EPROM	16K x 8	1-2, 5-7, 9-10, 11-12, 13-14

NOTE: Wirewrap or other method of jumpering.

The sockets U239 and U251 are connected to accommodate either a 24-pin or a 28-pin device. Refer to Figure 2-4. If the device has 28 pins, orient device pin 1 with socket pin 1 and insert. If the device has 24 pins, orient device pin 1 with socket pin 3 and insert.

Device containing even data must be in socket U239 and device containing odd data must be in socket U251.

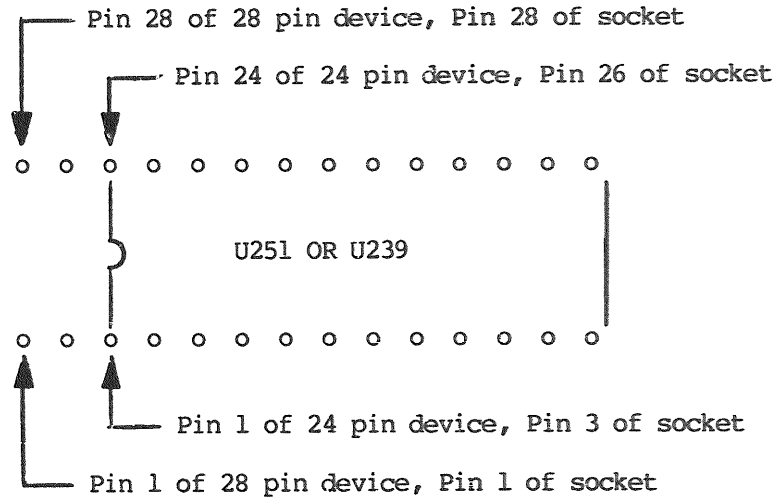


FIGURE 2-4. Socket Layout

### 2.2.3 MPU Clock Frequency Select Header (J10)

Header J10 is provided as a means of matching the module clock speed to the MC68010 clock frequency. Figure 2-5 shows the factory configuration which matches the 10 MHz MC68010 provided in the VME/10. The jumper positioned between pins 3 and 4 would match an 8 MHz MC68010.

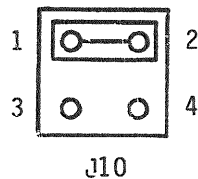


FIGURE 2-5. MPU Clock Frequency Select Header (J10)

#### 2.2.4 I/O Channel Enable Select Header (J11)

The SCM may be enabled as I/O Channel master. To enable, the jumper should be positioned between pins 1 and 2 as shown in Figure 2-6 (as shipped).

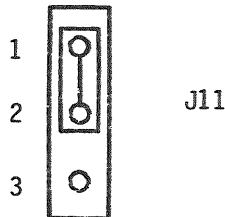


FIGURE 2-6. I/O Channel Enable Select Header (J11)

#### 2.2.5 Time-of-Day Clock Power Source Select Header (J15)

The time-of-day clock may be powered in three different ways. Figure 2-7 shows the factory configuration for header J15. See Table 2-2 for three methods.

TABLE 2-2. Power Source Methods

POWER SOURCE	BACKUP POWER	JUMPERS
+12V	BATTERY	1-3, 2-4
+12V	NONE	2-4
+5V STBY	+5V STBY	4-6

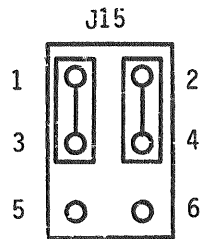


FIGURE 2-7. Time-of-Day Clock Power Source Select Header (J15)

#### 2.2.6 Factory Use Only Headers

Headers J3 and J4 are not used. Header J16 is for factory use only and has no user value.



**FUNCT.**  
**DESCR.**

## CHAPTER 3

### FUNCTIONAL DESCRIPTION

#### 3.1 INTRODUCTION

This chapter provides a general description of the overall microcomputer and detailed descriptions of internal modules and various modes of operation. For further details, consult the schematics in Chapter 4.

#### 3.2 GENERAL DESCRIPTION

The SCM is a complete microcomputer system. The module contains memory, input/output, and numerous control functions. The SCM can be used for system requirements ranging from single board applications through complex multiprocessor systems. Its shared RAM facilitates intercommunication between multiple microprocessors.

The ROM sockets (U239, U251) on the SCM may be configured to accommodate 8K- or 16K-byte devices. When either the 8K or 16K device is used, it repeats itself in the address space provided in the memory map.

The RAM is accessible to the onboard MPU. The RAM is also accessible to offboard devices via the VMEbus. The address of the dual ported RAM on the VMEbus port is factory configured as locations \$D00000-\$D5FFFF. However, these addresses are firmware configurable on any 512K-byte boundary.

There are several modes of protection for the VMEbus port of the dual ported RAM. It can be configured to be:

- private onboard RAM
- shared read/write RAM
- shared read only RAM
- shared programmable write protect RAM

Private RAM is not accessible from the VMEbus. When RAM is configured as programmable write protect RAM, the onboard MPU may write protect it under software control via the Write Protect Circuit (WPCT\*) bit in control register 2. Programmable write protect permits initial system load via bootstrap from VMEbus resources, followed by software write protect so that the system may operate with write protected memory. The SCM is configured with shared programmable write protect RAM.

The VMEbus interface is incorporated in the SCM to allow its use in a system requiring additional offboard resources. The VMEbus is characterized by asynchronous bidirectional operation and supports Direct Memory Address (DMA) and multiprocessor system operation. The VMEbus interface supports the full 16-megabyte range of the MC68010 MPU. VMEbus data, address, and control lines are available on P1.

The MPU, RAM, ROM, keyboard interface, I/O Channel slave boards, time-of-day clock, status register, and control registers are interconnected via local busing. The local bus allows the SCM processor to continue operating at full speed onboard while other VMEbus masters operate simultaneously.

The MPU gains access to the VMEbus when becoming VMEbus master via a bus request. The priority of the SCM bus request is software programmable to one of the four available levels, using the status and control registers.

Bus requests may be made by the indirect (software transparent) method and by the direct method by specific request through the status and control registers.

Indirect request -- When the program attempts to access an offboard memory location while the board is not the bus master, the memory decode logic automatically initiates a bus request at the software programmed level. When the memory access is complete, VMEbus mastership is either released immediately or it is held onto until another board on the VMEbus requests VMEbus mastership. The decision on how to release bus mastership and how to obtain it is software programmable in the control registers. The indirect methods of requesting VMEbus mastership are software transparent. In addition, they allow multiple processor boards to cycle-steal bus resources following each bus access cycle.

Direct request -- A bus request can be initiated through the status and control registers under direct program control. When using the direct request method, bus mastership is retained by the board until released under program control via the status and control registers. This method permits block transfers to be performed by the SCM to and from the VMEbus at maximum speed. The block transfer can be interrupted by another board of higher priority bus request if the SCM control registers are set up to allow that interruption.

The VMEbus interrupter logic permits the MPU to place an interrupt request on one of the seven VMEbus interrupt request lines. The interrupt request is placed using the status and control registers. The interrupter allows the SCM to interrupt another VMEbus card.

The SCM interrupt handler may be software configured to respond to any subset of the seven VMEbus interrupt request lines. This allows several boards with like interrupt handlers to respond to different interrupts from the VMEbus.

The SCM can be software configured to monitor the AC power fail (ACFAIL\*) line on the VMEbus. This allows user-provided power-down and power-up firmware routines to perform system-wide activities, such as storing critical data in nonvolatile RAM in the event of a power-down condition.

The SCM is designed as a system controller, which means it can provide the following system management and control functions:

- a. VMEbus arbitration - The system controller accepts bus requests from the VMEbus potential masters on four bus request priority levels, and issues a bus grant to the highest priority requester when appropriate.
- b. System clock - A 16-MHz TTL clock signal is provided to other VMEbus devices to facilitate their counting and synchronizing tasks.

- c. Reset - The SCM's power-on-reset and its switch reset drive the System Reset (SYSRESET\*) line on the VMEbus.
- d. Bus time-out - Generates a Bus Error (BERR\*) on the VMEbus when a nonexistent device is addressed on the bus. This function is software selectable as ON or OFF.

Because the SCM is always the system controller, care must be taken to ensure that no other boards on the VMEbus are configured as the system controller.

In addition to the VMEbus functions already mentioned, a major function of the SCM is that of being a video monitor controller. The video controller is capable of controlling either a monochrome monitor with seven gray scales or a color monitor. There are three options of the video control section. They are explained as follows:

- a. An 80-character by 25-character display with no graphics.
- b. An 800-pixel by 600 (or 300) pixel graphics display with no characters.
- c. An 80-character by 25-character display ORed with an 800-pixel by 600 (or 300) pixel graphics display.

Associated with each character is an attribute byte that defines it as blanked, underlined, inverse video, blinking, red, green, and/or blue.

Each graphic pixel has three bits associated with it in memory. Each bit in memory represents red, green, or blue pigment of the pixel or a gray scale on the monochrome display. Each pigment of the pixel is in a different plane of the memory. The planes can be addressed individually 8/16 bits at a time, or the three bits associated with a pixel can all be addressed at once.

The memory map of the SCM depends on the size RAM with which it is populated. Figures 3-1, 3-2, 3-3, and 3-4 show these memory maps.

ADDRESS	High Resolution Graphics
\$000000	System RAM after unswap goes from 0 to 1
\$00FFFF	System ROM after power on reset (see control reg. section)
\$010000	System RAM
\$02FFFF	
\$030000	High Resolution Graphics RAM
\$05FFFF	
\$060000	
\$17FFFF	Reserved for RAM Expansion
\$180000	VMEbus
\$DFFFFF	
\$E00000	Graphics - Pixel Access Addressing Block
\$EFFFFFF	
\$F00000	System ROM after unswap bit goes from 0 to 1
\$FOFFFF	System RAM after power on reset (see control reg. section)
\$F10000	SCM I/O (see Figure 3-4)
\$F1BFFF	
\$F1C000	Lower Data Byte (D00-D07) - I/O Channel
\$F1DFFF	Upper Data Byte (D08-D15) - Illegal
\$F1E000	VMEbus
\$FFFFFF	

FIGURE 3-1. SCM Memory Map, High Resolution Graphics

ADDRESS	Normal Resolution Graphics
\$000000	System RAM after unswap goes from 0 to 1
\$00FFFF	System ROM after power on reset (see control reg. section)
\$010000	System RAM
\$047FFF	
\$048000	Normal Resolution Graphics RAM
\$05FFFF	
\$060000	Reserved for RAM Expansion
\$17FFFF	
\$180000	VMEbus
\$DFFFFF	
\$E00000	Graphics - Pixel Access Addressing Block
\$EFFFFFF	
\$F00000	System ROM after unswap bit goes from 0 to 1
\$FOFFFF	System RAM after power on reset (see control reg. section)
\$F10000	SCM I/O (see Figure 3-4)
\$F1BFFF	
\$F1C000	Lower Data Byte (D00-D07) - I/O Channel
\$F1DFFF	Upper Data Byte (D08-D15) - Illegal
\$F1E000	VMEbus
\$FFFFFF	

FIGURE 3-2. SCM Memory Map, Normal Resolution Graphics

ADDRESS	No Graphics
\$000000	System RAM after unswap goes from 0 to 1
\$00FFFF	System ROM after power on reset (see control reg. section)
\$010000	
	System RAM
\$05FFFF	
\$060000	Reserved for RAM Expansion
\$17FFFF	
\$180000	
\$DFFFFF	VMEbus
\$E00000	Graphics - Pixel Access Addressing Block
\$EFFFFFF	
\$F00000	System ROM after unswap bit goes from 0 to 1
\$FOFFFF	System RAM after power on reset (see control reg. section)
\$F10000	
\$F1BFFF	SCM I/O (see Figure 3-4)
\$F1C000	Lower Data Byte (D00-D07) - I/O Channel
\$F1DFFF	Upper Data Byte (D08-D15) - Illegal
\$F1E000	
\$FFFFFF	VMEbus

FIGURE 3-3. SCM Memory Map, No Graphics

ADDRESS	D15-D08 UPPER DATA	D07-D00 LOWER DATA
\$F10000 \$F13FFF	ILLEGAL	
\$F14000 \$F14FFF	ILLEGAL	CHARACTER GENERATOR RAM
\$F15000 \$F15FFF		ATTRIBUTE GENERATOR RAM
\$F16000 \$F16FFF	ILLEGAL	
\$F17000 \$F18FFF	DISPLAY AND ATTRIBUTE RAM	
\$F19000 \$F19EFF	ILLEGAL	
\$F19F00	VERTICAL GRAPHICS CURSOR REGISTER	
\$F19F02	HORIZONTAL GRAPHICS CURSOR REGISTER	
\$F19F05	ILLEGAL	CONTROL REGISTER 0
\$F19F07	ILLEGAL	CONTROL REGISTER 1
\$F19F09	ILLEGAL	CONTROL REGISTER 2
\$F19F0B	ILLEGAL	CONTROL REGISTER 3
\$F19F0D	ILLEGAL	CONTROL REGISTER 4
\$F19F0F	ILLEGAL	CONTROL REGISTER 5
\$F19F11	ILLEGAL	CONTROL REGISTER 6
\$F19F13	ILLEGAL	GRAPHICS OFFSET REGISTER
\$F19F20 \$F19F7F	RESERVED	
\$F19F85	ILLEGAL	STATUS REGISTER
\$F19FA0 \$F1A01F	RESERVED	

FIGURE 3-4. SCM I/O Memory Map (Sheet 1 of 2)



ADDRESS	D15-D08 UPPER DATA	D07-D00 LOWER DATA
\$F1A021 \$F1A023	ILLEGAL	MC68A45 ADDRESS REGISTER MC68A45 INTERNAL REGISTER FILE
\$F1A025 \$F1A02F	ILLEGAL	
\$F1A031 \$F1A033 \$F1A035 \$F1A037	ILLEGAL	MC2661 TX/RX DATA REGISTERS MC2661 STATUS REGISTER MC2661 MODE 1 AND MODE 2 REGISTERS MC2661 COMMAND REGISTER
\$F1A039 \$F1A07F	ILLEGAL	
\$F1A081 \$F1A083 \$F1A085 \$F1A087 \$F1A089 \$F1A08B \$F1A08D \$F1A08F \$F1A091 \$F1A093 \$F1A095 \$F1A097 \$F1A099 \$F1A09B		MC146818 SECONDS REGISTER MC146818 SECONDS ALARM REGISTER MC146818 MINUTES REGISTER MC146818 MINUTES ALARM REGISTER MC146818 HOURS REGISTER MC146818 HOURS ALARM REGISTER MC146818 DAY OF THE WEEK REGISTER MC146818 DAY OF THE MONTH REGISTER MC146818 MONTH REGISTER MC146818 YEAR REGISTER MC146818 REGISTER A MC146818 REGISTER B MC146818 REGISTER C MC146818 REGISTER D
\$F1A09D \$F1A0FF	ILLEGAL	BATTERY BACKED UP RAM TIME OF DAY CLOCK (MC146818)
\$F1A100 \$F1A7FF	ILLEGAL	
\$F1A800 \$F1AFFF	DMA/MMU	
\$F1B000 \$F1BFFF	ILLEGAL	

FIGURE 3-4. SCM I/O Memory Map (Sheet 2 of 2)

### 3.3 DETAILED DESCRIPTION

Figure 3-5 shows a block diagram for the SCM.

#### PROCESSOR

The processor section of the SCM consists of the MC68010 MPU and the required support hardware, including the clock generator and reset logic. Also included with the processor is a set of four sockets used to route all of the signal pins plus extra power, grounds, and spares up to a daughter board. The daughter board includes an MC68010 processor.

A 10-MHz MPU is supplied as standard on the SCM.

#### ROM/EPROM

The two 28-pin ROM/EPROM sockets are provided for custom applications. Header J9 configures both sockets for 8K- or 16K-byte devices. The sockets are decoded for map locations \$F00000-\$FOFFFF. If either the 8K or 16K device is used, it appears repeatedly in the 64K-byte space.

Any time the SCM goes through a full reset condition, a map swap occurs. This swap results in ROM/EPROM being mapped at locations \$000000-\$00FFFF, and the RAM that was in that position being mapped at \$F00000-\$FOFFFF. This causes all of the exception table of the MPU (including the reset vectors) to be in ROM after a full reset condition occurs. After the SCM is in the swapped state, it can be unswapped by setting the unswap bit in control register 1. There is a reset condition which does not cause a memory map swap to occur. This partial reset is accomplished by the operator pushing the reset switch which would normally be on a front panel. These two choices of reset facilitate development where it is desired to use a program in RAM to emulate a reset condition in a target system.

A write to ROM always results in a bus error exception being executed in the MPU.

#### RAM

384K bytes of video and general purpose RAM is supplied on the SCM. The RAM may be accessed by the MPU or by a VMEbus device; both the MPU and the VMEbus device use the SCM local bus to access the RAM. Any time a VMEbus device tries to access the SCM RAM, if it is a valid cycle, a request is made to the onboard MPU to remove itself from the local bus to allow the VMEbus device to use the local bus to access SCM RAM. The onboard MPU waits until it finishes its current cycle before granting the local bus to the VMEbus device. There is one exception to this -- any time the onboard MPU is executing a cycle that is requesting mastership of the VMEbus, if a VMEbus device requests the local bus, it is granted the VMEbus immediately without the processor finishing its current cycle. After the VMEbus device access cycle of the SCM RAM completes, the processor continues the cycle that it was executing. It should be noted that all of the above arbitration is transparent to software; however, the programmer should keep in mind that VMEbus device accesses of the SCM RAM detain the onboard MPU while the accesses take place.

\* USABLE AS SYSTEM  
DRAM IF GRAPHICS  
DRAM NOT TO BE USED

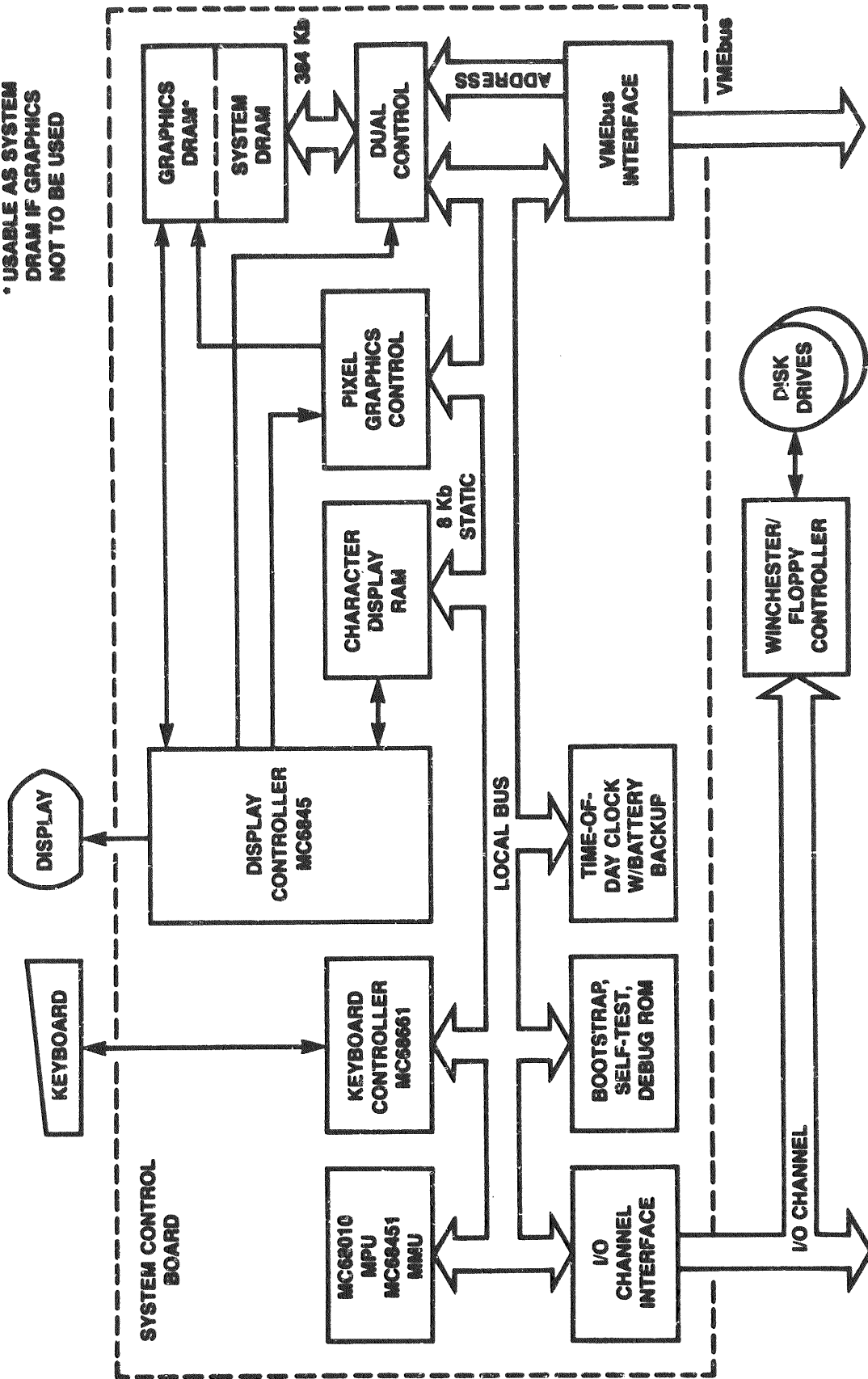


FIGURE 3-5. SCM Block Diagram

## RAM AS VIEWED FROM THE ONBOARD MPU (IN THE NORMAL UNSWAPPED POSITION)

If no graphics are being used, all of the RAM on the SCM is available as system RAM. In this mode, RAM appears at locations \$000000-\$05FFFF.

If graphics are being used and the SCM is in the normal resolution graphics mode, system RAM appears at locations \$000000-\$047FFF, and graphics RAM appears at locations \$048000-\$05FFFF.

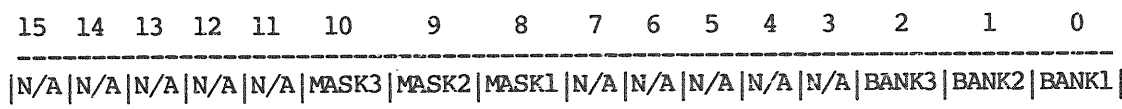
If graphics is being used and the SCM is in the high resolution graphics mode, system RAM appears at locations \$000000-\$02FFFF, and graphics RAM appears at locations \$030000-\$05FFFF. Note that any time the SCM switches from low resolution to high resolution, all of the system RAM is moved around. Therefore, any program or variables that were stored in system RAM prior to the switch is lost. The same occurs when switching from high resolution to low resolution.

Another area of the memory map allows the onboard MPU to access the graphics RAM in the pixel mode. In order to understand the pixel mode, a discussion of the graphics RAM is in order.

The graphics RAM is divided into three banks. Each bank is a color for color monitors, and each bank is an intensity for monochrome monitors. The graphics RAM block in the memory map is organized so that the first third of the graphics RAM locations is bank 3, the second third of the graphics RAM locations is bank 2, and the last third of the graphics RAM locations is bank 1. This allows the MPU to change 8 or 16 pixels on the screen at a time in one bank (color/intensity). For example, if the monitor is a color monitor and bank 3 is green, bank 2 is blue and bank 1 is red. When all of the graphics RAM is zeroed, the screen is blank. If the MPU now sequentially fills the graphics RAM from lowest address to highest address with \$FFFF'S, using word writes, the screen fills with red from top to bottom, 16 pixels at a time, until bank 2 is all \$F'S. Then the screen fills with cyan (green and blue mixed) from top to bottom, 16 pixels at a time, until bank 2 is all \$F'S. Then the screen fills with white (red, green, and blue mixed) from top to bottom, 16 pixels at a time, until bank 1 is all \$FF'S.

The graphics RAM is accessible in another mode called the pixel access mode. In the pixel access mode, the processor has the ability to change one pixel at a time (in one memory cycle) in all three banks. In this mode, the processor uses only word accesses. The lower three bits of a pixel access word affect the three banks of the pixel, where bit 0 is bank 1, bit 1 is bank 2, and bit 2 is bank 3. Bits 3-7 and 11-15 have no function, and bits 8-10 are mask bits. Bit 8, when low, disallows any effect by bit 0 on bank 1 of the pixel accessed. Bit 9, when low, disallows any effect by bit 1 on bank 2 of the pixel accessed. Bit 10, when low, disallows any effect by bit 2 on bank 3 of the pixel accessed. Each of bits 8-10 has no effect on its corresponding bank bit when high.

The organization of the pixel access word is as shown in the following figure.



For example: If all of the graphics RAM is zeroed, the screen is blank. Assume the same conditions as in the example above. If the MPU writes \$0707 starting at the lowest address of the pixel access block of the memory map to the highest address, the screen fills with white one pixel at a time from top to bottom.

The pixel access block appears at locations \$E00000 through \$E7FFFF in low resolution graphics mode, and at locations \$E00000 through \$EFFFFFF in high resolution graphics mode.

Locations \$000-\$3FF are predefined by the MPU as exception vectors.

#### RAM AS VIEWED FROM THE VMEbus

Except for the RAM that is swapped with ROM if the SCM memory map is swapped, all of the RAM is accessible from the VMEbus. However, it is accessible only in the byte or word access mode and not in the pixel access mode. The base address of the RAM from the VMEbus is firmware configurable. The factory configuration in firmware places the address as locations \$D00000-\$D5FFFF.

In addition to configuring the address at which the SCM RAM responds to VMEbus access cycles, the same decode PROM decodes the address modifier lines (AM0-AM5) and the WRITE\* line from the VMEbus and the [WPTCT\*] line from control register 2. This allows resource protection from the VMEbus. The PROM is factory-programmed to allow accesses when the address modifier code is supervisory (data or program) only if the WPTCT\* bit is high, or if the WPTCT\* bit is low but the cycle is a read rather than a write.

The VMEbus address decode PROM program used in U298 is as follows:

INPUTS TO DECODE PROM (384K BYTE)													OUTPUT- VALID
A23	A22	A21	A20	A19	AM5	AM4	AM3	AM2	AM1	AM0	WRITE*	WPTCT*	ADDRESS*
1	1	0	1	0	1	1	1	1	1	0	1	0	0
1	1	0	1	0	1	1	1	1	0	1	1	0	0
1	1	0	1	0	1	1	1	1	1	0	X	1	0
1	1	0	1	0	1	1	1	1	0	1	X	1	0
ALL OTHER COMBINATIONS OF ADDRESSES AND ADDRESS MODIFIERS													1

NOTE: 0 = Low logic level  
1 = High logic level

Note that the SCM cannot access its own dual port memory from the VMEbus side. Any time such an attempt is made, the BERR\* line is driven true on the VMEbus, which causes the bus error signal line to the SCM MPU to be driven true.

The access time of the SCM RAM from the VMEbus is typically 1950 nanoseconds.

## SCM CONTROL AND STATUS REGISTERS

The SCM has seven control registers and one status register. The individual addresses of these registers are listed in the memory maps. Control registers 0, 2-7 are cleared to 0 by any of the reset conditions occurring. Control register 1 is cleared to 0 only by the power-on-reset condition occurring. All of the control registers are writable by the MPU when it is in the supervisory state. Only control registers 0 and 1 are writable by the MPU when it is in the user state. All of the control registers are readable by the MPU in any state. However, the data read is not reliable unless each control register has been written to by the processor at least once since the last reset condition occurred. The bit definitions of the control registers are as follows:

### CONTROL REGISTER 0 (ADDRESS \$F19F05)

7	6	5	4	3	2	1	0
-----							
CDIS3	CDIS2	CDIS1	CURBK	DUTYCYCLE	IVS	TIMIMSK*	DMAIMSK*
-----							

- CDIS3-CDIS1 Each of these three bits is used to disable a color bank from being displayed to the monitor (this affects character mode only). CDIS3 disables color one when high and enables it when low. CDIS2 disables color two when high and enables it when low. CDIS1 disables color three when high and enables it when low.
- CURBK Cursor blink causes the character cursor to blink on and off when it is high. When it is low, it has no effect on the character cursor.
- DUTYCYCLE When high, this bit corrects the BX syndrome by not displaying every other dot on each line. This prevents horizontal lines, such as those in the uppercase letter B, from standing out more than nonhorizontal lines such as those in the letter X. When DUTYCYCLE is low, it has no effect on the display.
- IVS Invert video screen performs the function of inverting all characters on the screen when it is high. When it is low, all characters are normal.
- TIMIMSK\* When low, this bit inhibits interrupts caused by the real-time clock (MC146818) IRQ\* signal line being low. When high, this bit performs no masking function. Note that further masking of this interrupt is provided in the MC146818.
- DMAIMSK\* When low, this bit inhibits interrupts caused by the DMAIRQ\* signal line being low. When high, this bit performs no masking function.

CONTROL REGISTER 1 (ADDRESS \$F19F07)

7	6	5	4	3	2	1	0
IG	S1	S0	HIGH RES	GRE2	GRE1	GRE0	UNSWAP

IG When no graphics are being used, this bit may be set high to speed up accesses to the system RAM.

S1,S0 These bits select one of four optional character cursors which are user-definable. See attribute RAM description.

HIGH RES This bit also drastically affects the SCM system RAM mapping (see Figure 3-2).

GRE2,GRE1,GRE0 These bits are used to control color for color monitors and gray scales for monochrome monitors. When a color monitor is used, GRE2 enables color 2 (blue) when high, GRE1 enables color 1 (red) when high, and GRE0 enables color 3 (green) when high. When a monochrome monitor is used, the gray scales are controlled by these three bits as follows:

GRE2	GRE1	GRE0	GRAY SCALE
0	0	0	OFF
0	0	1	LOWEST INTENSITY
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	HIGHEST INTENSITY

UNSWAP Whenever a power-on-reset (or SCM reset and abort switch reset) condition occurs, the memory map of the SCM is swapped so that ROM appears at locations 0-\$7FFF; the system RAM which would normally appear at those locations (0-\$FFFF) appears where ROM would normally appear (locations \$F00000-\$FOFFFF).

These sections of RAM and ROM may be restored to their normal positions by setting the UNSWAP bit to a 1. After this action occurs (that of transitioning UNSWAP from 0 to 1), this bit has no more ability to affect the memory map. Clearing UNSWAP to a zero again does not cause RAM and ROM to swap out of their normal positions in the memory map. The only conditions that swap RAM and ROM out of their normal positions are the reset conditions mentioned above.



CONTROL REGISTER 2 (ADDRESS \$F19F09)

7	6	5	4	3	2	1	0
-----							
RXRDYMSK* SYSEMSK* WPTCT* KBDRST* VMEAVMSK* BCLRMSK* TXRDYMSK* MMUIMSK*							
-----							

- RXRDYMSK\*** When low, this bit inhibits interrupts caused by the EPCI RXRDY\* signal line being low. When this bit is high, it performs no masking function.
- SYSEMSK\*** When low, this bit inhibits interrupts caused by the SYSFAIL signal on the VMEbus being low. When high, this bit does no masking.
- WPTCT\*** When low, this bit disallows all writes to SCM RAM by other VMEbus devices; when it is high, it does not.
- KBDRST\*** Keyboard reset when low sends a reset out from the keyboard interface. It also continually resets the MC2661. When high, this bit performs no function.
- VMEAVMSK\*** When low, this bit inhibits interrupts caused by the VMEbus becoming available.
- BCLRMSK\*** When low, this bit inhibits interrupts caused by the BCLR\* line on the VMEbus being low when the SCM requester is holding the VMEbus in the release never mode (see requester description). When high, this bit does no masking.
- TXRDYMSK\*** When low, this bit inhibits interrupts caused by the EPCI TXRDY\* signal line being low. When high, this bit does no masking.
- MMUIMSK\*** When low, this bit inhibits interrupts caused by the MMUIRQ\* signal line being low. When this bit is high, it performs no masking function. The MMUIRQ\* signal comes only from the daughter board capable of driving that line.

CONTROL REGISTER 3 (ADDRESS F19F08)

7	6	5	4	3	2	1	0
IRQ7MSK*	IRQ6MSK*	IRQ5MSK*	IRQ4MSK*	IRQ3MSK*	IRQ2MSK*	IRQ1MSK*	VBIAMSK*

- IRQ7MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ7\* on the VMEbus being low. This bit performs no masking function when it is high.
- IRQ6MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ6\* on the VMEbus being low. This bit performs no masking function when it is high.
- IRQ5MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ5\* on the VMEbus being low. This bit performs no masking function when it is high.
- IRQ4MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ4\* on the VMEbus being low. This bit performs no masking function when it is high.
- IRQ3MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ3\* on the VMEbus being low. This bit performs no masking function when it is high.
- IRQ2MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ2\* on the VMEbus being low. This bit performs no masking function when it is high.
- IRQ1MSK\*      When low, this bit inhibits interrupts to the SCM processor caused by IRQ1\* on the VMEbus being low. This bit performs no masking function when it is high.
- VBIAMSK\*      When low, this bit inhibits interrupts to the SCM processor caused by an interrupt acknowledge cycle having occurred for the interrupt request initiated by the SCM interrupter.

CONTROL REGISTER 4 (ADDRESS \$F19F0D)

7	6	5	4	3	2	1	0
IDC7	IDC6	IDC5	IDC4	IDC3	IDC2	IDC1	IDC0

This register is the vector register. During an interrupt acknowledge cycle on the VMEbus, if the SCM initiated the interrupt request that is being acknowledged, the contents of this register are driven onto the VMEbus data lines as follows:

IDC7 drives D07  
IDC6 drives D06  
IDC5 drives D05  
IDC4 drives D04  
IDC3 drives D03  
IDC2 drives D02  
IDC1 drives D01  
IDC0 drives D00

CONTROL REGISTER 5 (ADDRESS \$F19F0F)

7	6	5	4	3	2	1	0
BRDFAIL*	AMA	VMETOEN	LTOEN	BRC1	BRC0	BRL1*	BRL0*

**BRDFAIL\*** When low, this bit causes the SYSFAIL\* signal line on the VMEbus to be low, indicating a board failure. When high, this bit does not drive the SYSFAIL\* signal line low.

**AMA** This bit may be used to alter the way that the address modifier lines are driven by the SCM during accesses by it to the VMEbus. The effect of AMA on the address lines is programmable in a PROM.

**VMETOEN** When high, this bit enables the VMEbus time-out circuitry to operate (causes BERR\* to go low if DS0\* or DS1\* is low for 64 microseconds or longer). When low, it disables the VMEbus time-out circuitry.

**LTOEN** When high, this bit enables the local resource time-out circuitry to operate (if [UDS\*] or [LDS\*] is low for 64 microseconds or longer, it causes [BERR\*] to the processor to go low). When low, it disables the VMEbus time-out circuitry.

**BRC1, BRC0** These two bits control the operating mode of the requester. The bit to mode correspondence is as follows:

BRC1	BRC0	MODE
0	0	RELEASE ON REQUEST
0	1	RELEASE ON BUS CLEAR
1	0	RELEASE WHEN DONE
1	1	RELEASE NEVER

For further details, see the requester section.

**BRL1\*, BRL0\*** These two bits control the level at which the requester operates. This level should be set one time only, immediately after a reset condition. For further details on how to set the requester level, see the requester section.

CONTROL REGISTER 6 (ADDRESS \$F19F11)

7	6	5	4	3	2	1	0
IMASK*	INT4MSK*	INT3MSK*	INT2MSK*	INT1MSK*	IL2	IL1	ILO

- IMASK\* When low, this bit inhibits all interrupts to the SCM processor under all conditions. When high, this bit masks no interrupts.
- INT4MSK\* When low, this bit inhibits interrupts to the SCM processor caused by the I/O Channel interrupt signal line INT4\* being low. When this bit is high, it provides no masking function.
- INT3MSK\* When low, this bit inhibits interrupts to the SCM processor caused by the I/O Channel interrupt signal line INT3\* being low. When this bit is high, it provides no masking function.
- INT2MSK\* When low, this bit inhibits interrupts to the SCM processor caused by the I/O Channel interrupt signal line INT2\* being low. When this bit is high, it provides no masking function.
- INT1MSK\* When low, this bit inhibits interrupts to the SCM processor caused by the I/O Channel interrupt signal line INT1\* being low. When this bit is high, it provides no masking function.
- IL2,IL1,ILO These three bits are used to generate interrupts onto the VMEbus. For further details, see the interrupter section.

## STATUS REGISTER

The status register monitors several signal lines on the SCM. The bit definitions of the status register are as follows:

### STATUS REGISTER (ADDRESS \$F19F85)

7	6	5	4	3	2	1	0
-----							
SWITCH2	SWITCH1	SWITCH0	KYBDLOCK*	IOCHEN	SYSFAIL	VBIACK*	VMEAV
-----							

- SWITCH2** This bit is low when J2 pins 5-6 are connected; it is high when they are not. This bit is used to bypass the POR diagnostics.
- SWITCH1** This bit is low when J2 pins 3-4 are connected; it is high when they are not. This bit is used only as a general purpose switch.
- SWITCH0** This bit is low when J2 pins 1-2 are connected. Pins 1-2 must be connected.
- KYBDLOCK\*** When this bit is low, the keyboard lock switch is in the lock position. The software should respond accordingly to this condition. When this bit is high, the keyboard lock switch is in the unlock position.
- IOCHEN** When this bit is high, the SCM is the I/O Channel master.
- SYSFAIL** When this bit is high, the "SYSFAIL\*" signal line on the VMEbus is being driven low. When this bit is low, the "SYSFAIL\*" signal line is not being driven low.
- VBIACK\*** When this bit is low, it indicates that the interrupt being generated by the board interrupter has been acknowledged. When this bit is high, it indicates that either the board interrupter is not generating an interrupt onto the VMEbus or that it is generating an interrupt onto the VMEbus which has not yet been acknowledged.
- VMEAV** When this bit is low, it indicates that the SCM does not have mastership of the VMEbus. When this bit is high, it indicates that this board does have mastership of the VMEbus.

## GENERATING VMEbus INTERRUPTS

The SCM has an interrupter module which is capable of generating interrupts onto the VMEbus. The level that it interrupts onto the VMEbus is software programmable and the status ID byte that it passes during the interrupt acknowledge cycle is software programmable. The following is the required sequence in order to use the interrupter module to interrupt onto the VMEbus:

- a. Make sure that the interrupt bits (bits 0-2) of control register 6 are cleared to zero.
- b. Initialize the status ID byte (control register 4) to the desired value. The interrupt handler on the VMEbus normally shifts the status ID byte left twice and uses the result as the address in its exception table for handling the VMEbus interrupt.
- c. Set the interrupt bits (bits 0-2) to the desired interrupt level. This causes the appropriate IRQ to be generated on the VMEbus. The bit level to interrupt level correspondence is as follows:

BIT 2	BIT 1	BIT 0	IRQ
0	0	0	NONE
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

- d. Wait for the VMEbus interrupt acknowledged bit (bit 1 of the status register) to become a 0, indicating that the interrupt has been acknowledged.
- e. Clear the interrupt bits (bits 0-2) of control register 6 to zero.

Note that it is possible to set up the interrupt acknowledged condition to cause a level 1 interrupt to the processor. If this option is used, it is important to account for the fact that the VMEAV\* interrupt has the same level and shares the same exception table location as does [VBIACK\*]. See the interrupt handler section.

## INTERRUPTING THE ONBOARD MPU

There are 22 sources of interrupts on the SCM. Each one is capable of interrupting the MPU on one of seven levels (1-7). All of the interrupt sources have an assigned distinct priority. For example, if three interrupt sources occur on the same level at the same time, they are serviced in the order of their priority. The interrupt sources, their levels, and their priorities are as follows:

LEVEL	PRIORITY WITHIN LEVEL		
	LOWEST	MEDIUM	HIGHEST
7	IRQ7* (from VMEbus)	ACEPTL*	SOFTWARE ABORT
6	IRQ6* (from VMEbus)	I/O CHNL INT4*	SYSTEM FAIL
5	IRQ5* (from VMEbus)	I/O CHNL INT3*	TIME-OF-DAY INTERRUPT
4	IRQ4* (from VMEbus)	I/O CHNL INT2*	MMU INTERRUPT
3	IRQ3* (from VMEbus)	RXRDY INT	TXRDY INT
2	IRQ2* (from VMEbus)	I/O CHNL INT1*	DMA INTERRUPT
1	IRQ1* (from VMEbus)	BUS CLEAR INT	VMEbus AVAILABLE (OR VMEbus INTERRUPT ACKNOWLEDGED)



Each interrupt source (except for those from the VMEbus) is serviced through a different vector in the MC68010 exception table. The interrupt source to exception table correspondence is as follows:

INTERRUPT SOURCE	EXCEPTION TABLE ADDRESS
IRQ1*	VECTOR PASSED BY INTERRUPTING BOARD DURING INTERRUPT ACKNOWLEDGE CYCLE, SHIFTED LEFT TWICE
BUS CLEAR INTERRUPT	\$100
VMEbus AVAILABLE OR INTERRUPT ACKNOWLEDGED	\$120
IRQ2*	SAME AS IRQ1*
I/O CHANNEL INT1*	\$104
DMA INTERRUPT	\$124
IRQ3*	SAME AS IRQ1*
RXRDY* INTERRUPT	\$108
TXRDY* INTERRUPT	\$128
IRQ4*	SAME AS IRQ1*
I/O CHANNEL INT2*	\$10C
MMU INTERRUPT	\$12C
IRQ5*	SAME AS IRQ1*
I/O CHANNEL INT3*	\$110
TIME-OF-DAY INTERRUPT	\$130
IRQ6*	SAME AS IRQ1*
I/O CHANNEL INT4*	\$114
SYSTEM FAIL	\$134
IRQ7*	SAME AS IRQ1*
ACFAIL*	\$118
SOFTWARE ABORT	\$138

All of the interrupt sources are maskable by several different methods. The first method of masking interrupts is via bit 7 of control register 6. The name of this bit is IMASK\*. When this bit is low, it masks all interrupts; when it is high, it does not mask any interrupt. From a reset condition, this bit comes up low, masking all interrupts. Another method of masking interrupts is that of using the mask bit associated with each interrupt. The interrupts and their corresponding mask bits are listed in the table below. Each of these bits masks its corresponding interrupt when it is low but does not when it is high. All of these mask bits come up masking at reset time.

INTERRUPT SOURCE	CORRESPONDING MASK BIT	
	CONTROL REGISTER #	BIT NUMBER
IRQ1*	3	1
BUS CLEAR INTERRUPT	2	2
VMEBUS AVAILABLE	2	3
INTERRUPT ACKNOWLEDGED	3	0
IRQ2*	3	2
I/O CHANNEL INT1*	6	3
DMA INTERRUPT	0	0
IRQ3*	3	3
RXRDY* INTERRUPT	2	7
TXRDY* INTERRUPT	2	1
IRQ4*	3	4
I/O CHANNEL INT2*	6	4
MMU INTERRUPT	2	0
IRQ5*	3	5
I/O CHANNEL INT3*	6	5
TIME-OF-DAY INTERRUPT	0	1
IRQ6*	3	6
I/O CHANNEL INT4*	6	6
SYSTEM FAIL	2	6
IRQ7*	3	7
ACFAIL*	NO MASK EXISTS FOR THIS INTERRUPT	
SOFTWARE ABORT	NO MASK EXISTS FOR THIS INTERRUPT	

The third method of masking interrupts is that of using the internal mask bits of the MPU status register (see MC68010 data sheet for further details).

## KEYBOARD INTERFACE

The keyboard interface consists of an MC2661 Enhanced Programmable Communications Interface (EPCI). The EPCI interfaces the half duplex serial data bus (from the keyboard) to the processor lower data bus. The serial bus uses RS-422 type drivers and receivers, allowing multiple peripherals to be connected to the serial bus for communication with the SCM. (The serial bus is not fully RS-422 compatible.) Do not use the MOVEP instruction with the EPCI.

For the keyboard interface to operate properly, the EPCI should be programmed as follows:

### EPCI INITIALIZATION

- a. Reset the serial bus and the EPCI by clearing KYBDRST\* (bit 1 of control register 0) to zero. (This happens automatically during any of the SCM reset conditions except for software reset.) Then set KYBDRST\* to a 1, which removes the reset.

- b. Move the hexadecimal value \$5E into the mode 1 register (location \$F1A035) -- i.e., MOVE.B #5E,\$F1A035

This causes the following:

- STOP BIT LENGTH = 1
- PARITY = ODD,ENABLED
- CHARACTER LENGTH = 8
- MODE = ASYNCHRONOUS
- BAUD RATE FACTOR = 16X

- c. Move the hexadecimal value \$7B into the mode 2 register (location \$F1A035) -- i.e., MOVE.B #7B,\$F1A035

This causes the following:

- TXC = INTERNAL
- RXC = INTERNAL
- DIVISOR = 128 (FOR 512 BAUD)

- d. Move the hexadecimal value \$15 into the command register (location \$F1A037) -- i.e., MOVE.B #15,\$F1A037

This causes the following:

- OPERATING MODE = NORMAL
- RTS\* = HIGH
- ERROR FLAGS = CLEARED
- SEND NO BREAK
- RECEIVER = ENABLED
- DTR\* = HIGH
- TRANSMITTER = ENABLED

## EPCI OPERATION AFTER INITIALIZATION

a. To transmit a command to a peripheral on the serial bus, perform the following:

1. Write the command byte into location \$F1A031.
2. Do not send another command to a peripheral until the peripheral responding to the current command has finished sending back its response character, unless the character sent was a deselect. If the character was a deselect, then no ACK/NACK is sent by the peripheral. After a deselect, the next character can be loaded for transmission when TXRDY\* goes low (bit 0 of location \$F1A033 goes high).

b. To receive a character back from the peripheral, perform the following:

1. Wait for bit 1 of location \$F1A033 to go to 1.
2. The character may now be read from location \$F1A031.

c. To interrupt the MPU upon the receipt of a character from the serial bus, perform the following:

1. Clear bit 7 of control register 2 to 0 to inhibit RXRDY\* interrupts.
2. Initialize location \$108 with the address of the interrupt service routine.
3. Ensure that bit 7 of control register 6 is set to 1 (IMASK\* does no masking).
4. Lower the processor interrupt mask to level 2.
5. Set bit 7 of control register 2 to a 1 (enables RXRDY\* interrupts).

To avoid interrupting the processor upon receipt of a character from the serial bus, execute only step 1 above.

d. To interrupt the MPU when another character may be loaded for transmission from the EPCI (TXRDY\* goes low):

1. Clear bit 1 of control register 2 to 0 to inhibit RXRDY\* interrupts.
2. Initialize location \$128 with the address of the interrupt service routine.
3. Ensure that bit 7 of control register 6 is set to 1 (IMASK\* does no masking).
4. Lower the processor interrupt mask to level 2.
5. Set bit 1 of control register 2 to a 1 (enables TXRDY\* interrupts).

To avoid interrupting the processor when TXRDY\* goes low, execute only step 1 above.

- e. To transmit a command to a peripheral on the serial bus, perform the following:
1. Write the command byte into location \$F1A031.
  2. Do not send another command to a peripheral until the peripheral responding to the current command has finished sending back its response character.
- f. To receive a character back from the peripheral, perform the following:
1. Wait for bit 1 of location \$F1A033 to go to 1.
  2. The character may now be read from location \$F1A031.
- g. The following bits may be used to determine which, if any, errors occurred in the reception of a character.
1. Bit 5 of location \$F1A033 signals that a framing error occurred, when it is high.
  2. Bit 4 of location \$F1A033 signals that an overrun error occurred, when it is high.
  3. Bit 3 of location \$F1A033 signals that a parity error occurred, when it is high.
  4. All of the above error flags are cleared when bit 4 of location \$F1A037 is set to 1 or when KYBDRST\* is asserted. In addition, the parity error flag is cleared on the reception of the next good character after the parity error flag was set.

- NOTES:
- 1) Location \$F1A031 contains both a read only register and a write only register.
  - 2) Location \$F1A033 is a read only register.
  - 3) Location \$F1A035 contains two registers, mode 1 and mode 2. Mode 1 is accessed by the first MPU access of location \$F1A035 after the EPCI is reset. Mode 2 is accessed by the next MPU access of location \$F1A035, mode 1 by the next, mode 2 by the next, and so forth.
  - 4) Location \$F1A037 is a read/write register as are the mode 1 and mode 2 registers.

## I/O CHANNEL INTERFACE

The SCM has an I/O Channel interface for communication with I/O Channel modules. The memory map of the SCM is organized such that the I/O Channel appears only on the lower data lines (D0-D7) of the MPU. When J11 pins 1-2 are connected, the SCM is the I/O Channel master. INT1\*-INT4\* from the I/O Channel are brought in as interrupts to the MPU by the interrupt handler. The RST\* line on the I/O Channel is driven low by any of the reset conditions on the SCM, and it is driven low when an MPU reset instruction is executed. For more details on the I/O Channel, refer to the I/O Channel Specification Manual.

## BATTERY BACKED UP TIME-OF-DAY CLOCK

The SCM is equipped with a battery backed up time-of-day clock. The operation of the clock is described in the MCI46818 data sheet. Because of the battery backup feature of the clock, it is recommended that the board not be left for more than five days without recharging the backup batteries. Charging the batteries is accomplished by applying power to the SCM. A charge time of 14 hours is necessary to fully charge the backup batteries. When power is turned off to the SCM, the backup batteries, if fully charged, maintain the proper voltage to the MCI46818 to ensure no data loss for about five days. If the power is left off longer than five days, data may be lost in the MCI46818. The power sense bit in the MCI46818 may be used to detect if voltage to the power pins of the MCI46818 ever dropped low enough to allow loss of data. The addresses of the individual registers within the MCI46818 are listed in the memory map section. The IRQ line from the MCI46818 causes a level 1 interrupt to the processor if that interrupt is not masked.

## VMEbus COMPATABILITY

VMEbus compatibility is provided by the following:

- . VMEbus interface
- . VMEbus arbiter
- . VMEbus requester

### VMEbus Interface

The VMEbus interface provides the data path from the onboard MPU via the local bus to the VMEbus. The interface does not become active until VMEbus mastership has been obtained. If this condition is not met, the output buffers to the VMEbus remain in a high impedance state.

During VMEbus access cycles, the VMEC1 drives the address modifier lines (AM0-AM5), depending on the processor function code lines as follows:

INPUTS				OUTPUTS						ADDRESS MODIFIER
AMA	FC2	FC1	FC0	AM5	AM4	AM3	AM2	AM1	AM0	CODE DESCRIPTION
X	0	0	1	1	(1)	1	0	0	1	Standard non-privileged data
X	0	1	0	1	(1)	1	0	1	0	Standard non-privileged prog
X	1	0	1	1	(1)	1	1	0	1	Standard supervisory data
X	1	1	0	1	(1)	1	1	1	0	Standard supervisory prog
X	1	1	1	X	X	X	X	X	X	Interrupt acknowledge cycle

NOTE 1: 1 for address \$000000-\$EFFFFFFF

0 for address \$F00000-\$FFFFFFF

## VMEbus Arbiter

The arbiter on the SCM is a full arbiter (i.e., it arbitrates all four levels of bus requests). Its operation is transparent to software and it has no software or hardware options. Care must be taken to ensure that no other boards on the VMEbus have an arbiter operating when placed on the same bus as the SCM.

## VMEbus Requester

The VMEbus requester is used to gain access to resources on the VMEbus. Most of the operation of the requester is transparent to software. However, there are several options available to the user, and some initialization is required before the requester may be used.

The level on which the requester operates is a function which should be initialized only one time -- after reset. The following procedure performs the necessary initialization.

When the SCM goes through a reset sequence, the requester is at a level 3 (highest priority). To change the level at which the requester operates, execute the following.

- a. Set bits 2 and 3 of control register 5 to 1's (this will initiate a block transfer request).
- b. Wait for bit 0 of the status register to become a 1 (indicating that the SCM is now VMEbus master).
- c. Change bits 0 and 1 of control register 5 from 00 (level 3) to the desired request level. The bit value to level chosen is as follows:

### CONTROL REGISTER 5

BIT 1	BIT 0	LEVEL
0	0	3
0	1	2
1	0	1
1	1	0

- d. Set bits 2 and 3 of control register 5 to the desired mode of operation (see following explanation).



The VMEbus requester is capable of operating in one of four modes. The mode is determined by bits 2 and 3 of control register 5. The bit values and corresponding modes of operation are as follows:

CONTROL REGISTER 5

BIT 3	BIT 2	MODE OF OPERATION	DESCRIPTION
0	0	RELEASE ON REQUEST	In this mode the requester requests mastership of the VMEbus any time the processor initiates an access cycle to a VMEbus device (provided the SCM is not a current VMEbus master). The requester does not relinquish VMEbus mastership until some other device on the VMEbus requests mastership or until bits 2 and 3 change to a mode that causes the SCM to give up VMEbus mastership.
1	0	RELEASE WHEN DONE	In this mode the requester requests mastership of the VMEbus any time the processor initiates an access cycle to a VMEbus device. The requester relinquishes mastership of the VMEbus when it finishes its current VMEbus cycle. If the processor changes from a mode that is maintaining bus mastership to this mode, it gives up bus mastership immediately.
0	1	RELEASE ON BUS CLEAR	In this mode the requester requests mastership of the VMEbus any time the processor initiates an access cycle to a VMEbus device (provided the SCM is not a current VMEbus master). The requester does not relinquish VMEbus mastership until some other device on the VMEbus, which is of a higher priority, requests mastership of the bus or until bits 2 and 3 change to a mode that causes the SCM to give up VMEbus mastership.
1	1	RELEASE NEVER	In this mode the requester immediately requests mastership of the VMEbus. The processor can determine whether or not VMEbus mastership has been obtained by checking bit 0 of the status register (VMEAV). If VMEAV = 1, mastership has been obtained; if it is a 0, it has not. In addition to being a status bit, VMEAV is an interrupt source (see interrupt handler). After mastership is obtained, it is not relinquished until bits 2 and 3 change to a value that causes the SCM to give up VMEbus mastership.

NOTE: All of the release modes of the requester require one processor cycle to occur after the release condition is detected before the actual release of BBSY\* occurs.

## SCM RESET CIRCUITRY

There are four sources for resetting the SCM. They are as follows:

- a. **SYSRESET\*** - If some device external to the SCM drives the **SYSRESET\*** line on the VMEbus low, all of the resettable devices are initialized on the SCM. However, this has no effect on the swapping function of the SCM memory map, nor does it pull the **RESET** line to the MC68A45 or control register 1.
- b. **SCM RESET SWITCH** - If only the **SCM RESET** switch is pushed, it has the same effect on the SCM as does **SYSRESET\***. This condition also causes the **SYSRESET\*** line on the VMEbus to be driven low.
- c. **POWER-ON-RESET** - At power-on time, the **SCM power-on-reset** circuit does the same thing as the **SCM RESET** switch. It also causes the **SCM** memory map to switch so that **ROM** appears at locations \$0-\$FFFF and the **RAM** that is normally at \$0-\$FFFF appears at locations \$F00000-\$F0FFFF. In addition, **RESET** is sent to the MC68A45 and to control register 1.
- d. **POWER-DOWN-RESET** - If there is a device that drives the **ACFAIL\*** line to low (from bus connector or on power connector) when ac power fails, the **SCM power-down-reset** circuit drives the **SYSRESET\*** line on the VMEbus to low within 2.5 ms of **ACFAIL\*** going low. It does not release **SYSRESET\*** until **ACFAIL\*** goes back to a high.
- e. **SCM ABORT AND RESET SWITCHES** - An imitation of power-on-reset can be obtained by the following sequence:
  1. Press and hold the **SCM RESET** switch.
  2. Press the **SCM ABORT** switch.
  3. Release the **SCM ABORT** switch.
  4. Release the **SCM RESET** switch.

If the MC68010 reset instruction is executed, the only result is that the I/O Channel line **RST\*** is driven low, resetting the resettable devices on the I/O Channel.

If bit 1 of control register 1 (**KBDRST\***) is cleared to a zero either because of any of the five resets mentioned above or because of software, all of the devices on the serial bus are reset along with the MC2661 in the keyboard interface section of this board. This reset condition remains until **KBDRST\*** is set to a 1.

## SCM SOFTWARE ABORT

The **SCM** has a software **ABORT** switch which, when depressed, causes a level 7 interrupt request to the **SCM** processor (provided the **IMASK\*** bit is high). It is then up to the software to handle the interrupt so as to obtain the desired software abort function.

## SCM LOCAL RESOURCE TIME-OUT GENERATOR

When the MPU begins an access cycle, the Local Resource Time-out Generator (LRTG) begins counting. If a device responds and the cycle is completed before 64 microseconds expire, the LRTG stops counting and resets itself. If no device responds causing the cycle to not complete before 64 microseconds expire, the LRTG drives the MPU BERR\* line to low, causing a bus error exception. If the access cycle is to the VMEbus, the timer functions only to ensure that VMEbus mastership is obtained within 64 microseconds. After VMEbus mastership is obtained, access cycles to the VMEbus do not activate the LRTG. The LRTG is enabled when the [LTOEN] bit (bit 4) of control register 5 is high; it is disabled when that same bit is low.

## VMEbus TIME-OUT GENERATOR

The VMEbus Time-out Generator (VMETG) is a general-purpose watchdog timer for the VMEbus. When any VMEbus master (including the SCM) begins a VMEbus cycle by driving either DS0\* or DS1\* low, and if no device responds allowing that data strobe to go high within 64 microseconds, the VMETG drives the BERR\* signal line on the VMEbus low until the data strobe returns to a high. The VMETG is enabled when the [VMETO] bit (bit 5) of control register 5 is high; it is disabled when that same bit is low.

## THE DISPLAY SECTION

### a. THE CHARACTER DISPLAY

#### 1. The MC6845

The following is the list of register options supporting the MC6845. To select the register, write the register number into location \$F1A021. After doing this, the specified register can be written into at location \$F1A023.

NOTE: This cannot be accomplished in TENbug because TENbug changes the register being addressed each time it updates the cursor.

REGISTER	NORMAL	HIGH
0	62	62
1	50	50
2	56	56
3	11	11
4	19	19
5	03	02
6	19	19
7	19	19
8	00	03
9	0B	16

## 2. Color (Intensity) Enables

The character color (intensity) enables are three bits located in the attribute portion of each character word.

The color (intensity) enables for the screen are located in control register zero, located at address \$F19F05 bits 5, 6, and 7.

Example 1: The three character color (intensity) bits could be used to draw pictures with seven gray scales on a monochrome display.

Example 2: The three screen color (intensity) enables could be used to allow the operator to select the color (intensity) of his screen from the keyboard.

## 3. Inverse Video Screen

To display dark characters on a light background set bit 2 in control register 0 at location \$F19F05.

## 4. Cursor Controls

To make the cursor blink, set bit 4 in register 0 located at \$F19F05.

Four different cursors are available to the user and are individually selected by bits 5 and 6 in register 1 located at \$F19F07.

## 5. Display RAM

The display RAM consists of 2K words of memory, each of which contains character and attribute information. The even location contains the character and one software bit. The odd location contains the attribute for that character.

```
-----  
| 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 |  
-----
```

Bits 0-6	Displayable characters (see character generator)
Bit 7	Software attribute
Bits 8-10	Color (intensity) attribute
Bit 12	Underline
Bit 11	Inverse video attribute
Bit 13	Blink attribute
Bit 14	Display enable attribute
Bit 15	Software attribute

NOTE: Software attribute bits are used by TENbug and VERSAdos.

## 6. Character Generator RAM

The character generator RAM begins at location F14001 and ends at location F14FFE (only the odd locations are used). Each character takes up 16 consecutive bytes in the RAM with the first byte corresponding to the first line of the character displayed on the screen.

## 7. Attribute Generator RAM

The attribute generator RAM is located at \$F15001 in the memory map and gives the user the flexibility of redefining the attribute byte. It is a 2K byte static RAM and it exclusive ORs its data with the character generator as defined below:

Bit 7	XOR	CG Bit 6	Displayed Bit 2
Bit 6	XOR	CG Bit 5	Displayed Bit 3
Bit 5	XOR	CG Bit 4	Displayed Bit 4
Bit 4	XOR	CG Bit 3	Displayed Bit 5
Bit 3	XOR	CG Bit 2	Displayed Bit 6
Bit 2	XOR	CG Bit 1	Displayed Bit 7
Bit 1	XOR	CG Bit 0,7	Displayed Bits 1,8
Bit 0			Displayed Bits 0,9

The characters in the attribute generator RAM are 32 bytes in length and are defined as follows:

Character Rows 0-32	MPU ADR A1-A5	Rows 1-32 of the video character
D11-D12 (see display and attribute RAM)	MPU ADR A6-A7	Define underline and inverse video
Cursor Enable	MPU ADR A8	Defines these characters; as cursors
Cursor Style Selects	MPU ADR A9-A10	Selects different cursor styles
Inverse Video Screen Select	MPU ADR A11	Selects inverse video screen

Examples: The attribute generator is used for inverse video screen, inverse video characters underlining, and cursor generation.

### b. THE GRAPHICS DISPLAY

#### 1. Graphics Enable Bits

The graphics display is enabled by bits 1, 2, and 3 in control register 1 located at \$F19F07. These bits correspond to the color (intensity) screen bits of the character display.

#### 2. Normal Access

The normal access mode of the graphics section is utilized by word or by byte reads and writes. The color (intensity) planes are located at \$300000, \$400000, and \$500000. The first word in each plane corresponds to the first 16 pixels displayed in the upper left hand corner of the display.

### 3. Pixel Access

The pixel access mode of the graphics section is utilized by word reads and writes only. The pixel access area starts at \$E00000 and each word corresponds to a dot on the screen. Bits 0, 1, and 2 provide the color (intensity) control for each dot of the graphics display. Bits 8, 9, and 10 are mask bits that inhibit the write logic on individual planes when doing a pixel write.

### 4. Graphics Offset Register

If normal resolution is to be used, the graphics offset register (\$F19F13) should be set to 0 and if high resolution is to be used, the graphics offset register should be set to \$32.

### 5. Vertical Graphics Cursor

The vertical graphics cursor is setup to display a vertical line on the screen when the dot count in the register plus the dot count on the screen reaches \$XFFF.

Example: Load \$XFFF into the vertical graphics cursor register to display an inverse video vertical line on the first line of the display. To move the line right one dot on the display, load the vertical graphics cursor register with \$XFFE.

### 6. Horizontal Graphics Cursor

The horizontal graphics cursor is setup to display a horizontal line on the screen when the line count in the register plus the line count on the screen reaches \$XFFF.

Example: Load \$XFFF into the horizontal graphics cursor register to display an inverse video horizontal line on the first line of the display. To move the line down one dot on the display, load the vertical graphics cursor register with \$XFFE.

#### NOTE

When the CRTIC and the graphics offset register are loaded for high resolution, two lines are displayed for the horizontal graphics cursor and the cursor is moved down two lines each time the horizontal graphics cursor register is decremented.

### c. 50% DUTY CYCLE

1. The 50% duty cycle is located in control register 0 bit 3. When bit 3 is set, each dot on the display lasts only half as long. This solves the B-X problem on monochrome displays. The bit should be zeroed on color displays in order to achieve a suitable brightness level.

## CHAPTER 4

### SUPPORT INFORMATION

#### 4.1 INTRODUCTION

This chapter provides the interconnection signals, parts lists with parts location illustrations, and schematic diagrams of modules.

#### 4.2 INTERCONNECT SIGNALS

The daughter board is mounted on top of and connects directly to the SCM module. The connection is made through headers J1-J8 on the daughter board and headers J5-J8 on the SCM module. The SCM interconnects through cables with J1, P2, J12, J13 and J14. P1 connects directly to connector XJ1 on the VME backplane. The connector functions are listed below:

- J1 - Keyboard, ABORT switch, RESET switch, and KYBD LOCK
- P1, P2 - VME backplane
- J5, J6, J7, J8 - Daughter board
- J12 - Battery backup
- J13 - Video (monitor)
- J14 - Power Supply

##### 4.2.1 Connector J1 Interconnect Signals

The signals at connector J1 on the SCM are shown as well as connector P1 on the front panel cable from KYBD LOCK, RESET, ABORT, switches and the keyboard connector. Table 4-1 lists each pin connection, signal mnemonic, and signal characteristic for the connectors.

TABLE 4-1. Connector J1 Interconnect Signals

PIN NUMBER		SIGNAL	SIGNAL NAME AND DESCRIPTION
P1	J1	MNEMONIC	
2	1	GND	GROUND
Not Used			
1	2	ABRT*	ABORT - when the front panel ABORT switch is depressed the ABRT* signal goes low causing the software operation to halt.
4	3	NABRT*	NOT ABORT - an active low signal from the ABORT switch which indicates a normal unabort condition.
3	4	NRST*	NOT RESET - an active low signal from the RESET switch which indicates a normal set condition.
Not Used			
6	5	GND	GROUND
5	6	RST*	RESET - when the front panel RESET switch is depressed the RST* signal goes low causing a reset condition to occur.
8	7	KYBD LOCK*	KEYBOARD LOCK - when the KYBD LOCK key switch is in the lock position the keyboard is ignored by the system, and ABORT and RESET is disabled.
10	8	GND	GROUND - keyboard ground
7	9	GND	GROUND - ABORT, RESET, and KYBD LOCK switches ground.
9	10	+12VDC	+12 Vdc Power - used by keyboard circuits.
12	11	RST+	RESET POSITIVE - this signal together with RST- signal is a differential pair that resets the keyboard.
11	12	RST-	RESET NEGATIVE - this signal together with RST+ signal is a differential pair that resets the keyboard.
14	13	D+	DATA POSITIVE - this signal together with D- is a differential pair that carries data between the Enhanced Programmable Communications Interface (EPCI) and the devices it controls.
13	14	D-	DATA NEGATIVE - this signal together with D+ is a differential pair that carries data between the EPCI and the devices it controls.



#### 4.2.2 Connector P1 Interconnect Signals

The signals at connector P1 on the SCM are the same pin-for-pin as the signals at connector XJ1 on the VME backplane. Table 4-2 lists each pin connection, signal mnemonic, and signal characteristics for the connector.

TABLE 4-2. Connector P1 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1	D00	DATA BUS (bit 0) - one of three-state bidirectional data lines that provide the data path between the SCM and the VME backplane.
A2	D01	DATA BUS (bit 1) - same as D00 on pin A1.
A3	D02	DATA BUS (bit 2) - same as D00 on pin A1.
A4	D03	DATA BUS (bit 3) - same as D00 on pin A1.
A5	D04	DATA BUS (bit 4) - same as D00 on pin A1.
A6	D05	DATA BUS (bit 5) - same as D00 on pin A1.
A7	D06	DATA BUS (bit 6) - same as D00 on pin A1.
A8	D07	DATA BUS (bit 7) - same as D00 on pin A1.
A9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - a constant 16 MHz clock signal generated on the SCM.
A11	GND	GROUND
A12	DS1*	DATA STROBE 1 - three-state driven signal that indicates data lines D08-D15 are valid on a write cycle. When low, DS1 indicates D08-D15 are driven by a slave on a read cycle. SCM drives DS1* as a master and receives it as a slave.
A13	DS0*	DATA STROBE 0 - three-state driven signal that indicates data lines D00-D07 are valid on a write cycle. When low, DS0* indicates D00-D07 are driven by a slave on a read cycle. SCM drives DS0* as a master and receives it as a slave.
A14	WRITE*	WRITE - three-state driven signal indicating the flow of data. A high level indicates a read from slave to master. A low level indicates a write from master to slave. SCM drives this line as master and receives it as a slave.
A15	GND	GROUND

TABLE 4-2. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. SCM receives this signal as a master and drives it as a slave.
A17	GND	GROUND
A18	AS*	ADDRESS STROBE - an active low signal that indicates valid address, valid address modifiers, etc., are on the VMEbus. SCM drives this signal as master and receives it as a slave.
A19	GND	GROUND
A20	IACK*	INTERRUPT ACKNOWLEDGE - three-state driven signal, when low, indicates that the VMEbus cycle is an IACK* cycle. SCM drives this signal as master and receives it as slave.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - this line is part of the interrupt acknowledge daisy chain. When IACKIN* goes low at the input to a module on the VMEbus, and if the module interrupt is being acknowledged, then the module intercepts the interrupt by not issuing an IACKOUT* signal. If the interrupt acknowledge is not for the module, then the module issues an IACKOUT* signal to the next module in the daisy chain. The SCM is at the head of the daisy chain and uses IACK* as IACKIN* and drives pin A21 as IACKOUT*.
A22		Not used.
A23	AM4	ADDRESS MODIFIER (bit 4) - one of five three-state driven address modifier lines which affect the devices and how the devices are accessed during VMEbus cycle. SCM drives these lines as master and receives as slave.
A24	A07	ADDRESS BUS (bit 7) - one of 23 three-state driven address lines that specify a memory address. SCM drives these lines as master and receives as slave.
A25	A06	ADDRESS BUS (bit 6) - same as A07 on pin A24.
A26	A05	ADDRESS BUS (bit 5) - same as A07 on pin A24.
A27	A04	ADDRESS BUS (bit 4) - same as A07 on pin A24.
A28	A03	ADDRESS BUS (bit 3) - same as A07 on pin A24.
A29	A02	ADDRESS BUS (bit 2) - same as A07 on pin A24.

TABLE 4-2. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A30	A01	ADDRESS BUS (bit 1) - same as A07 on pin A24.
A31	-12V	-12 Vdc Power - used by the VMEbus modules.
A32	+5V	+5 Vdc Power - used by the VMEbus modules.
B1	BBSY*	BUS BUSY - open-collector driven active low signal used in arbitrating the VMEbus.
B2	BCLR*	BUS CLEAR - driven by the SCM arbiter when a module with a higher priority than the SCM requests the bus.
B3	ACFAIL*	AC FAILURE - an input signal that indicates that the AC input to the power supply is no longer provided.
B4	BG0IN*	BUS GRANT IN (level 0) - SCM requester three-state driven signal to the first module in the daisy chain if the SCM arbiter grants the VMEbus on this level. The SCM drives BG0IN* as its bus grant out and does not connect to BG0OUT* on the VMEbus.
B5		Not used.
B6	BG1IN*	BUS GRANT IN (level 1) - same as BG0IN* on pin B4.
B7		Not used.
B8	BG2IN*	BUS GRANT IN (level 2) - same as BG0IN* on pin B4.
B9		Not used.
B10	BG3IN*	BUS GRANT IN (level 3) - same as BG0IN* on pin B4.
B11		Not used.
B12	BR0*	BUS REQUEST (level 0) - open-collector driven active low signal generated by the requester requiring access to the VMEbus on this level.
B13	BR1*	BUS REQUEST (level 1) - same as BR0* on pin B12.
B14	BR2*	BUS REQUEST (level 2) - same as BR0* on pin B12.
B15	BR3*	BUS REQUEST (level 3) - same as BR0* on pin B12.
B16	AM0	ADDRESS MODIFIER (bit 0) - same as AM4 on pin A23.
B17	AM1	ADDRESS MODIFIER (bit 1) - same as AM4 on pin A23.
B18	AM2	ADDRESS MODIFIER (bit 2) - same as AM4 on pin A23.
B19	AM3	ADDRESS MODIFIER (bit 3) - same as AM4 on pin A23.

TABLE 4-2. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B20	GND	GROUND
B21,B22		Not used.
B23	GND	GROUND
B24	IRQ7*	INTERRUPT REQUEST (level 7) - open-collector driven signal, generated by the interrupter, which carries priority level interrupt requests.
B25	IRQ6*	INTERRUPT REQUEST (level 6) - same as IRQ7* on pin B24.
B26	IRQ5*	INTERRUPT REQUEST (level 5) - same as IRQ7* on pin B24.
B27	IRQ4*	INTERRUPT REQUEST (level 4) - same as IRQ7* on pin B24.
B28	IRQ3*	INTERRUPT REQUEST (level 3) - same as IRQ7* on pin B24.
B29	IRQ2*	INTERRUPT REQUEST (level 2) - same as IRQ7* on pin B24.
B30	IRQ1*	INTERRUPT REQUEST (level 1) - same as IRQ7* on pin B24.
B31	+5V STDBY	+5 Vdc Standby Power - used by devices on the SCM requiring battery backup (e.g., time-of-day clock).
B32	+5V	+5 Vdc Power - used by the VMEmodules.
C1	D08	DATA BUS (bit 8) - same as D00 on pin A1.
C2	D09	DATA BUS (bit 9) - same as D00 on pin A1.
C3	D10	DATA BUS (bit 10) - same as D00 on pin A1.
C4	D11	DATA BUS (bit 11) - same as D00 on pin A1.
C5	D12	DATA BUS (bit 12) - same as D00 on pin A1.
C6	D13	DATA BUS (bit 13) - same as D00 on pin A1.
C7	D14	DATA BUS (bit 14) - same as D00 on pin A1.
C8	D15	DATA BUS (bit 15) - same as D00 on pin A1.
C9	GND	GROUND
C10	SYSFAIL*	SYSTEM FAIL - open-collector driven low level signal that indicates a failure has occurred in the system.

TABLE 4-2. Connector P1 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C11	BERR*	BUS ERROR - open-collector driven low level signal that indicates an error has occurred on the VMEbus. If the SCM is master when a bus error occurs, the MC68010 goes through a bus error exception. The SCM has a VMEbus timer which, if enabled, drives BERR* low if DS0* or DS1 if low for more than 64 microseconds.
C12	SYSRESET*	SYSTEM RESET - open-collector driven active low signal used to reset the modules on the VMEbus. It is driven by the SCM during any SCM reset conditions.
C13	LWORD*	LONGWORD - a three-state driven active low signal that indicates the data transfer is 32 bits. The SCM does not respond to this signal.
C14	AM5	ADDRESS MODIFIER (bit 5) - same as AM4 on pin A23.
C15	A23	ADDRESS BUS (bit 23) - same as A07 on pin A24.
C16	A22	ADDRESS BUS (bit 22) - same as A07 on pin A24.
C17	A21	ADDRESS BUS (bit 21) - same as A07 on pin A24.
C18	A20	ADDRESS BUS (bit 20) - same as A07 on pin A24.
C19	A19	ADDRESS BUS (bit 19) - same as A07 on pin A24.
C20	A18	ADDRESS BUS (bit 18) - same as A07 on pin A24.
C21	A17	ADDRESS BUS (bit 17) - same as A07 on pin A24.
C22	A16	ADDRESS BUS (bit 16) - same as A07 on pin A24.
C23	A15	ADDRESS BUS (bit 15) - same as A07 on pin A24.
C24	A14	ADDRESS BUS (bit 14) - same as A07 on pin A24.
C25	A13	ADDRESS BUS (bit 13) - same as A07 on pin A24.
C26	A12	ADDRESS BUS (bit 12) - same as A07 on pin A24.
C27	A11	ADDRESS BUS (bit 11) - same as A07 on pin A24.
C28	A10	ADDRESS BUS (bit 10) - same as A07 on pin A24.
C29	A09	ADDRESS BUS (bit 9) - same as A07 on pin A24.
C30	A08	ADDRESS BUS (bit 8) - same as A07 on pin A24.
C31	+12V	+12 Vdc Power - used by the VMEbus modules.
C32	+5V	+5 Vdc Power - used by the VMEbus modules.

### 4.2.3 Connector P2 Interconnect Signals

The signals at connector P2 on the SCM are the same pin-for-pin as the signals at connector XJ15 on the I/O Channel bus. Table 4-3 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 4-3. Connector P2 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A10	GND	GROUND
A11	A11	ADDRESS BUS (bit 11) - one of twelve output lines used to selectively address the I/O modules. Matches MC68010 MPU address line A12.
A12	A10	ADDRESS BUS (bit 10) - same as A11 on pin A11 except matches MPU address line A11.
A13	A8	ADDRESS BUS (bit 8) - same as A11 on pin A11 except matches MPU address line A9.
A14	A6	ADDRESS BUS (bit 6) - same as A11 on pin A11 except matches MPU address line A7.
A15	A4	ADDRESS BUS (bit 4) - same as A11 on pin A11 except matches MPU address line A5.
A16	A2	ADDRESS BUS (bit 2) - same as A11 on pin A11 except matches MPU address line A3.
A17-A19	GND	GROUND
A20	D7	DATA BUS (bit 7) - one of eight bidirectional data lines used to transfer data between the SCM and the I/O Channel bus.
A21	D6	DATA BUS (bit 6) - same as D7 on pin A20.
A22	D4	DATA BUS (bit 5) - same as D7 on pin A20.
A23	D2	DATA BUS (bit 2) - same as D7 on pin A20.
A24,A25	GND	GROUND
A26	-12V	-12 Vdc Power - used by I/O Channel modules.
A27		Not used.
A28	+12V	+12 Vdc Power - used by I/O Channel modules.
A29,A30	+5V	+5 Vdc Power - used by I/O Channel modules.
A31,A32	GND	GROUND

TABLE 4-3. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C1	INT4*	INTERRUPT REQUEST (level 4) - one of four active low signals used by the I/O Channel slave modules to interrupt the SCM.
C2	INT3*	INTERRUPT REQUEST (level 3) - same as INT4* on pin C1.
C3	INT2*	INTERRUPT REQUEST (level 2) - same as INT4* on pin C1.
C4	INT1*	INTERRUPT REQUEST (level 1) - same as INT4* on pin C1.
C5	IORES*	INPUT/OUTPUT RESET - active low signal generated by the SCM or the MPU reset instruction. This output signal resets I/O Channel modules.
C6	XACK*	TRANSFER ACKNOWLEDGE - active low input signal from I/O Channel bus that indicates write data has been latched or read data is available.
C7	CLK	CLOCK - free-running 4 MHz clock signal output to the I/O Channel modules for internal synchronization and timing.
C8,C9, C10		Not used.
C11	GND	GROUND
C12	A9	ADDRESS BUS (bit 9) - same as A11 on pin A11.
C13	A7	ADDRESS BUS (bit 7) - same as A11 on pin A11.
C14	A5	ADDRESS BUS (bit 5) - same as A11 on pin A11.
C15	A3	ADDRESS BUS (bit 3) - same as A11 on pin A11.
C16	A1	ADDRESS BUS (bit 1) - same as A11 on pin A11.
C17	A0	ADDRESS BUS (bit 0) - same as A11 on pin A11.
C18	STB*	STROBE - a high-to-low transition of this output signal indicates the start of a write cycle. A low-to-high transition indicates the end of the cycle.
C19	WT*	WRITE - when low, this output signal indicates a write cycle to the I/O Channel. When high, this signal indicates a read cycle.
C20	GND	GROUND
C21	D5	DATA BUS (bit 5) - same as D7 on pin A20.

TABLE 4-3. Connector P2 Interconnect Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C22	D3	DATA BUS (bit 3) - same as D7 on pin A20.
C23	D1	DATA BUS (bit 1) - same as D7 on pin A20.
C24	D0	DATA BUS (bit 0) - same as D7 on pin A20.
C25	GND	GROUND
C26	-12V	-12 Vdc Power -- used by I/O Channel modules.
C27		Not used.
C28	+12V	+12 Vdc Power -- used by I/O Channel modules.
C29,C30	+5V	+5 Vdc Power - used by I/O Channel modules.
C31,C32	GND	GROUND

#### 4.2.4 Headers J5-J8 Interconnect Signals

The signals at headers J5-J8 on the SCM are the same as the signals at headers J1-J8 on the daughter board. Table 4-4 lists each pin connection, signal mnemonic, and signal characteristic for the SCM headers and the daughter board headers.



TABLE 4-4. Headers J5-J8 Interconnect Signals

HEADER AND PIN NUMBER	DAUGHTER BOARD	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
J5-1	J1-1	PAS*	PROCESSOR ADDRESS STROBE - active low indicates there is a valid address on the address bus.
J5-2	J1-2	PUDS*	PROCESSOR UPPER DATA STROBE - this signal controls the flow of data on the data bus. When PWRITE* line is high, the processor reads from the data bus. When the PWRITE* line is low, the processor writes to the data bus.
J5-3	J1-3	PLDS*	PROCESSOR LOWER DATA STROBE - this signal controls the flow of data on the data bus. When PWRITE* line is high, the processor reads from the data bus. When the PWRITE* line is low, the processor writes to the data bus.
J5-4	J1-4	PWRITE*	PROCESSOR WRITE - this signal defines the data bus transfer as a read or write cycle. This signal works in conjunction with PUDS* and PLDS*.
J5-5	J1-5		Not used.
J5-6	J1-6	PDTACK*	PROCESSOR DATA TRANSFER ACKNOWLEDGE - this signal indicates that the data transfer is completed. When the processor recognizes PDTACK* during a read cycle, data is latched one clock cycle later and the bus cycle is terminated. When PDTACK* is recognized during a write cycle, the bus cycle is terminated.
J5-7	J1-7	BG*	BUS GRANT - this signal indicates to all other potential bus master devices that bus control is to be released at the end of the current bus cycle.
J5-8	J1-8	BGACK*	BUS GRANT ACKNOWLEDGE - this signal indicates that some other device has become the bus master.
J5-9	J1-9		Not used.
J5-10	J1-10	PRST*	PROCESSOR RESET - this bidirectional signal line acts to reset the processor in response to an external reset signal. An internal reset (result of a reset instruction) causes all external devices to be reset and the internal state of the processor is not affected.

TABLE 4-4. Headers J5-J8 Interconnect Signals (cont'd)

HEADER AND PIN NUMBER		SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
SCM	DAUGHTER BOARD		
J5-11	J2-1	VMA*	VALID MEMORY ADDRESS - this signal is used to indicate to M6800 peripheral devices that a valid address is on the address bus and the processor is synchronized to enable the E signal. This signal only responds to the VPA* signal.
J5-12	J2-2	E	ENABLE - this signal is the standard enable signal common to all M6800 type peripheral devices. The period for this signal is ten MC68010 clock periods. E is a free-running clock and runs regardless of the state of the bus on the MPU.
J5-13	J2-3	VPA*	VALID PERIPHERAL ADDRESS - this signal indicates that the device addressed is an M6800 family device and that data transfer should be synchronized with the E signal.
J5-14	J2-4	PBERR*	PROCESSOR BUS ERROR - this signal informs the processor that an error has occurred with the cycle currently being executed.
J5-15	J2-5	IPL2*	INTERRUPT CONTROL (level 2) - one of three signals that indicate the encoded parity level of the device requesting an interrupt.
J5-16	J2-6	IPL1*	INTERRUPT CONTROL (level 1) - same as IPL2* on SCM J5-15.
J5-17	J2-7	IPL0*	INTERRUPT CONTROL (level 0) - same as IPL2* on SCM J5-15.
J5-18	J2-8	FC2	FUNCTION CODE (level 2) - one of three signals that indicate the state (user or supervisor) and the cycle type currently being executed.
J5-19	J2-9	FC1	FUNCTION CODE (level 1) - same as FC2 on SCM J5-18.
J5-20	J2-10	DMA/MMU*	DIRECT MEMORY ACCESS/MEMORY MANAGEMENT UNIT - this signal indicates memory access to the MMU.
J6-1	J3-1	PD05	PROCESSOR DATA BUS (bit 5) - one of 16 bidirectional signal lines that transmit and accept data in either word or byte length.
J6-2	J3-2	PD06	PROCESSOR DATA BUS (bit 6) - same as PD05 on SCM J6-1.

TABLE 4-4. Headers J5-J8 Interconnect Signals (cont'd)

HEADER AND PIN NUMBER	DAUGHTER BOARD	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
J6-3	J3-3	PD07	PROCESSOR DATA BUS (bit 7) - same as PD05 on SCM J6-1.
J6-4	J3-4	PD08	PROCESSOR DATA BUS (bit 8) - same as PD05 on SCM J6-1.
J6-5	J3-5	PD09	PROCESSOR DATA BUS (bit 9) - same as PD05 on SCM J6-1.
J6-6	J3-6	PD10	PROCESSOR DATA BUS (bit 10) - same as PD05 on SCM J6-1.
J6-7	J3-7	PD11	PROCESSOR DATA BUS (bit 11) - same as PD05 on SCM J6-1.
J6-8	J3-8	PD12	PROCESSOR DATA BUS (bit 12) - same as PD05 on SCM J6-1.
J6-9	J3-9	PD13	PROCESSOR DATA BUS (bit 13) - same as PD05 on SCM J6-1.
J6-10	J3-10	PD14	PROCESSOR DATA BUS (bit 14) - same as PD05 on SCM J6-1.
J6-11	J4-1	PD15	PROCESSOR DATA BUS (bit 15) - same as PD05 on SCM J6-1.
J6-12 through J6-J17	J4-2 through J4-7	GND	GROUND
J6-18, J6-19	J4-8, J4-9		Not connected.
J6-20	J4-10	MMUIRQ*	MEMORY MANAGEMENT UNIT INTERRUPT REQUEST - this signal indicates an interrupt request from the MMU.
J7-1	J5-1	BR*	BUS REQUEST - this signal indicates to the processor that some other device desires to become the bus master.
J7-2	J5-2	+5V	+5 Vdc Power - used by the logic circuits on the daughter board.
J7-3	J5-3	MPUCLK	MICROPROCESSOR UNIT CLOCK - a TTL-compatible signal that is used by the MCU for the development of internal clocks needed by the processor.

TABLE 4-4. Headers J5-J8 Interconnect Signals (cont'd)

HEADER AND PIN NUMBER	DAUGHTER BOARD	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
J7-4	J5-4	HALT*	HALT - when this bidirectional line is driven by an external device, it causes the processor to stop at the completion of the current bus cycle. When the processor is halted using this input, all control signals are inactive and all three-state lines are in the high impedance state.
J7-5	J5-5	PA15	PROCESSOR ADDRESS BUS (bit 15) - one of 23 unidirectional signal lines capable of addressing 8 megawords of data, providing the address for bus operation during all cycles.
J7-6	J5-6	PA14	PROCESSOR ADDRESS BUS (bit 14) - same as PA15 on SCM J7-5.
J7-7	J5-7	PA13	PROCESSOR ADDRESS BUS (bit 13) - same as PA15 on SCM J7-5.
J7-8	J5-8	PA12	PROCESSOR ADDRESS BUS (bit 12) - same as PA15 on SCM J7-5.
J7-9	J5-9	PA11	PROCESSOR ADDRESS BUS (bit 11) - same as PA15 on SCM J7-5.
J7-10	J5-10	PA10	PROCESSOR ADDRESS BUS (bit 10) - same as PA15 on SCM J7-5.
J7-11	J6-1	PA09	PROCESSOR ADDRESS BUS (bit 9) - same as PA15 on SCM J7-5.
J7-12	J6-2	PA08	PROCESSOR ADDRESS BUS (bit 8) - same as PA15 on SCM J7-5.
J7-13	J6-3	PA07	PROCESSOR ADDRESS BUS (bit 7) - same as PA15 on SCM J7-5.
J7-14	J6-4	PA06	PROCESSOR ADDRESS BUS (bit 6) - same as PA15 on SCM J7-5.
J7-15	J6-5	PA05	PROCESSOR ADDRESS BUS (bit 5) - same as PA15 on SCM J7-5.
J7-16	J6-6	FC0	FUNCTION CODE (level 0) - same as FC2 on SCM J5-18.
J7-17	J6-7	PA01	PROCESSOR ADDRESS BUS (bit 1) - same as PA15 on SCM J7-5.
J7-18	J6-8	PA02	PROCESSOR ADDRESS BUS (bit 2) - same as PA15 on SCM J7-5.
J7-19	J6-9	PA03	PROCESSOR ADDRESS BUS (bit 3) - same as PA15 on SCM J7-5.

TABLE 4-4. Headers J5-J8 Interconnect Signals (cont'd)

HEADER AND PIN NUMBER		SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
SCM	DAUGHTER BOARD		
J7-20	J6-10	PA04	PROCESSOR ADDRESS BUS (bit 4) - same as PA15 on SCM J7-5.
J8-1	J7-1	PD04	PROCESSOR DATA BUS (bit 4) - same as PD05 on SCM J6-1.
J8-2	J7-2	PD03	PROCESSOR DATA BUS (bit 3) - same as PD05 on SCM J6-1.
J8-3	J7-3	PD02	PROCESSOR DATA BUS (bit 2) - same as PD05 on SCM J6-1.
J8-4	J7-4	PD01	PROCESSOR DATA BUS (bit 1) - same as PD05 on SCM J6-1.
J8-5	J7-5	PD00	PROCESSOR DATA BUS (bit 0) - same as PD05 on SCM J6-1.
J8-6	J7-6	PA23	PROCESSOR ADDRESS BUS (bit 23) - same as PA15 on SCM J7-5.
J8-7	J7-7	PA22	PROCESSOR ADDRESS BUS (bit 22) - same as PA15 on SCM J7-5.
J8-8	J7-8	PA21	PROCESSOR ADDRESS BUS (bit 21) - same as PA15 on SCM J7-5.
J8-9	J7-9	PA20	PROCESSOR ADDRESS BUS (bit 20) - same as PA15 on SCM J7-5.
J8-10	J7-10	PA19	PROCESSOR ADDRESS BUS (bit 19) - same as PA15 on SCM J7-5.
J8-11	J8-1	PA18	PROCESSOR ADDRESS BUS (bit 18) - same as PA15 on SCM J7-5.
J8-12	J8-2	PA17	PROCESSOR ADDRESS BUS (bit 17) - same as PA15 on SCM J7-5.
J8-13	J8-3	PA16	PROCESSOR ADDRESS BUS (bit 16) - same as PA15 on SCM J7-5.
J8-14 through J8-18	J8-4 through J8-8	+5V	+5 Vdc Power - used by the logic circuits on the daughter board.
J8-19	J8-9		Not used.
J8-20	J8-10	DMAIRQ*	DIRECT MEMORY ACCESS INTERRUPT REQUEST - this signal indicates an interrupt to a DMA operation.

#### 4.2.5 Connector J12 Interconnect Signals

Connector J12 interconnects with the battery backup input and the ACFAIL source on the power supply. The battery backup keeps the time-of-day clock operating in case of AC power failure. Table 4-5 lists each pin connection, signal mnemonic, and signal characteristic for the connection.

TABLE 4-5. Connector J12 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	BATT	BATTERY - positive 4.8V-5.6V battery connection.
2	GND	GROUND - negative battery connection.
3	ACFAIL*	AC FAILURE - this low active signal from the power supply that indicates AC power source has failed.

#### 4.2.6 Connector J13 Interconnect Signals

Video connector J13 connects the SCM to a color or monochrome monitor. Table 4-6 lists each pin connection, signal mnemonic and signal characteristic for the connector.

TABLE 4-6. Connector J12 Interconnect Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1		Not used.
2	CVD2	COLOR VIDEO DATA 2 - this TTL positive true signal line supplies color data to the monitor.
3	CVD3	COLOR VIDEO DATA 3 - same as CVD2 on pin 2.
4	CVD4	COLOR VIDEO DATA 4 - same as CVD2 on pin 2.
5,6	GND	GROUND
7	HSYNC	HORIZONTAL SYNCHRONIZATION - this TTL positive true signal supplies horizontal synchronization to the monitor.
8	VSYNC	VERTICAL SYNCHRONIZATION - this TTL positive true signal supplies vertical synchronization to the monitor.
9,10	GND	GROUND
11	MVD	MONOCHROME VIDEO DATA - this positive true analog signal supplies monochrome data to the monitor.
12,13, 14		Not used.

#### 4.2.7 Connector J14 Power Connections

Table 4-7 lists each pin connection, signal mnemonic, and signal characteristic for the connector.

TABLE 4-7. Connector J14 Power Connections

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	-12V	-12 Vdc Power - used by the SCM logic circuits, VMEbus, and I/O Channel bus.
2,3,4	+5V	+5 Vdc Power - used by the SCM logic circuits, daughter board logic circuits, VMEbus and I/O Channel bus.
5	+12V	+12 Vdc Power - used by the SCM logic circuits, keyboard, and I/O Channel bus.
6		Not used.
7-10	GND	GROUND

#### 4.3 CALIBRATION

The real-time clock device is factory calibrated and normally does not need recalibration. However, if the clock device (U281) or any of the components in the clock circuitry are replaced, the following procedure should be adequate.

- a. Turn equipment power OFF.
- b. Connect a frequency counter to test point E1 (see Figure 2-1) with ground to E2.
- c. Turn equipment power ON.
- d. Adjust timer capacitor C60 to obtain frequency reading of 1.048575 MHz.
- e. Turn equipment power OFF and remove counter.

This completes the calibration of the real-time clock.

#### 4.4 PARTS LISTS

Table 4-8 lists the components of the SCM. Table 4-9 lists the components of the daughter board. The part locations are illustrated in Figure 4-1 and 4-2. These parts lists reflect the latest issue of hardware at the time of printing.

TABLE 4-8. SCM Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8145B01	Printed wiring board
CR1,CR2	48NW9616A03	Diode, 1N4148/1N914
CR3,CR4	48NW9607A01	Rectifier, 1N4001
C1,C12,C49, C80	23NW9618A22	Capacitor, electrolytic, 50 uF @ 16 Vdc
C2-C6,C10, C11,C13-48, C50-C57,C63, C65-C68,C70- C72,C75-C78, C83-C92	21SW992C017	Capacitor, fixed, ceramic, 0.022 uF @ 50 Vdc
C7	21NW9604A11	Capacitor, fixed, ceramic, 0.47 uF @ 50 Vdc
C8,C9	21NW9702A20	Capacitor, fixed, ceramic, 0.1 uF @ 50 Vdc
C58,C61,C62, C64,C69,C73, C79,C81,C82	21SW992C025	Capacitor, fixed, ceramic, 0.100 uF @ 50 Vdc
C59	21NW9629A18	Capacitor, fixed, mica, 56 pF @ 500 Vdc
C60	20NW9628A04	Capacitor, trimmer, 5.5-18 pF
C74	23NW9618A09	Capacitor, electrolytic, 100 uF @ 16 Vdc
DL1,DL8	01NW9804C34	Delay module, triple, 70 ns
DL2,DL4,DL9	01NW9804C33	Delay module, triple, 40 ns
DL3,DL5	01NW9804C10	Delay module, digital, 215 ns
DL6	01NW9804C15	Delay module, triple, 60 ns
DL7,DL10	01NW9804C32	Delay module, triple 30 ns
DL11	01NW9804B35	Delay module, digital, 100 ns
J1	28NW9802F80	Header, right angle, two row, 14-pin
J2,J15	28NW9802B21	Header, double row post, 6-pin
J3,J4		Not used
J5-J8	28NW9802F27	Header, single row, 20 position socket
J9	28NW9802C36	Header, double row post, 14-pin



TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
J10	28NW9802C29	Header, double row post, 4-pin
J11	28NW9802D04	Header, single row post, 3-pin
J12	28NW9802F16	Header, friction lock, 3-pin
J13	28NW9802E69	Connector, 14-pin
J14	28NW9802E68	Connector, 10-pin
J16	28NW9802D01	Header, double row post, 2-pin
P1	28NW9802E71	Connector, DIN, socket, 96-pin
P2	28NW9802E70	Connector, DIN, plug, 64-pin
Q1	48NW9610A13	Transistor, 2N2222
R1,R2,R23	06SW-124A49	Resistor, fixed, film, 1.0K ohm, 5%, 1/4W
R3,R4,R26	06SW-124B22	Resistor, fixed, film, 1.0 megohm, 5%, 1/4W
R5,R6,R15	06SW-124A65	Resistor, fixed, film, 4.7K ohm, 5%, 1/4W
R7,R8,R25, R60	06SW-124A73	Resistor, fixed, film, 10K ohm, 5%, 1/4W
R9		Not used
R10,R20	51NW9626A64	Resistor network 7/2.2K ohm
R11,R14,R48	51NW9626A45	Resistor network 9/2.2K ohm
R12	51NW9626A22	Resistor network 5/10K ohm
R13	51NW9626A61	Resistor network 9/1K ohm
R16,R27,R28	51NW9626A41	Resistor network 9/4.7K ohm
R17-R19,R21, R22,R32-R34, R39-R44,R46, R47,R56-R58	51NW9626A37	Resistor network, 9/10K ohm
R24	06SW-124B50	Resistor, fixed, film, 15 megohm, 5%, 1/4W
R29,R30		Not used
R31	06SW-125A27	Resistor, fixed, carbon, 120 ohm, 5%, 1/4W
R35,R61	06SW-124A37	Resistor, fixed, film, 330 ohm, 5%, 1/4W
R36	06SW-124A11	Resistor, fixed, film, 27 ohm, 5%, 1/4W

TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R37	06SW-124A35	Resistor, fixed, film, 270 ohm, 5%, 1/4W
R38		Not used
R45	51NW9626A76	Resistor network 6/330/470
R49	06SW-124A43	Resistor, fixed, film, 560 ohm, 5%, 1/4W
R50	06SW-124A51	Resistor, fixed, film, 1.2K ohm, 5%, 1//4W
R51	06SW-124A57	Resistor, fixed, film, 2.2K ohm, 5%, 1/4W
R52-R55, R62, R63	06SW-124A01	Resistor, fixed, film, 10 ohm, 5%, 1/4W
R59	06SW-124A61	Resistor, fixed, film, 3.3K ohm, 5%, 1/4W
U1		Not used
U2, U79, U84 U109, U157, U319	51NW9615J39	I.C. 74F74PC
U3, U59, U77, U91, U278-U280	51NW9615G43	I.C. SN74S64N
U4-U9, U19- U24, U36-U41, U53-U58, U71- U76, U85-U90, U103-U108, U118-U123	51NW9615J17	I.C. MCM6665AP-20
U10, U11		Not used
U12	51NW9615C21	I.C. SN74LS04N
U13	51NW9615J24	I.C. SN74S22N
U14, U78, U320, U322	51NW9615C56	I.C. SN74S08N
U15, U45, U81, U82, U124, U164, U237, U299	51NW9615C21	I.C. SN74LS04N
U16, U17, U42, U276	51NW9615C22	I.C. SN74LS08N
U18, U27	51NW9615J40	I.C. SN75176P
U25, U33, U178, U291	51NW9615E88	I.C. SN74LS10N

TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U26	51NW9615B65	I.C. MC1455P1
U28,U51, U274,U292	51NW9615C96	I.C. SN74S04N
U29	51NW9615G38	I.C. SN74LS38N
U30,U47,U273	51NW9615F38	I.C. SN74LS393N
U31,U50,U95, U99,U100	51NW9615F85	I.C. SN74S38N
U32,U141	51NW9615D27	I.C. SN74S32N
U34,U63,U140	51NW9615C20	I.C. SN74LS02N
U35,U111,U143	51NW9615F31	I.C. DM74S51N
U43,U65,U149, U249	51NW9615C24	I.C. SN74LS32N
U44,U98	51NW9615E94	I.C. SN74LS279N
U46,U49,U64, U92,U93,U142, U144	51NW9615C95	I.C. SN74S74N
U48,U62,U277, U302	51NW9615E91	I.C. SN74LS00N
U52,U317	51NW9615F06	I.C. SN74LS51N
U60,U69,U112, U304,U305, U318	51NW9615C94	I.C. SN74S00N
U61	51NW9615D90	I.C. SN74S11N
U66	51NW9615G34	I.C. SN74LS85N
U67	51NW9615D32	I.C. SN74S02N
U68,U247,U248	51NW9615F01	I.C. SN74LS86N
U70,U97	51NW9615C25	I.C. SN74LS74AN
U80	51NW9615C69	I.C. SN74LS138N
U83	51NW9615D26	I.C. 74S113N
U94,U275	51NW9615E27	I.C. 74S10PC
U96,U116	51NW9615F79	I.C. SN74S240N

TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U101	(see NOTE)	I.C. programmed
U102,U117	(see NOTE)	I.C. programmed
U110	51NW9615G74	I.C. SN74S174N
U113,U127, U128	51NW9615G16	I.C. SN74S175N
U114,U311- U314	51NW9615G07	I.C. SN74S244N
U115	(see NOTE)	I.C. programmed
U125	51NW9615C58	I.C. SN74S86N
U126	51NW9615H10	I.C. SN74LS390N
U129,U145, U160,U175, U186,U188, U189,U201,U215	51NW9615F52	I.C. SN74LS273N
U130	51NW9615E95	I.C. SN74LS240N
U131	51NW9615C34	I.C. SN74S138N
U132,U148, U202	51NW9615G10	I.C. SN74LS148N
U133,U203, U295,U296	51NW9615F77	I.C. SN74LS158N
U134-U139, U258,U259	51NW9615J37	I.C. SN74LS299N
U146	(see NOTE)	I.C. programmed
U147	51NW9615G06	I.C. SN74S85N
U150-U155	(see NOTE)	I.C. programmed
U156,U171, U172	51NW9615C30	I.C. SN74LS193N
U158	51NW9615D83	I.C. SN74S133N
U159,U173, U174	51NW9615G99	I.C. SN74S163N
U161	(see NOTE)	I.C. programmed
U162,U191	51NW9615E86	I.C. SN74LS151N

TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U163,U198	51NW9615C29	I.C. SN74LS174N
U165,U167, U169,U180, U182,U184	51NW9615J35	I.C. SN74LS251N
U166,U168, U170,U181, U183,U185	51NW9615J38	I.C. SN74LS646NT
U176	(see NOTE)	I.C. programmed
U177	(see NOTE)	I.C. programmed
U179,U266, U267	51NW9615D92	I.C. SN74S20N
U187	51NW9615J33	I.C. SN74ALS874NT
U190,U257, U293	51NW9615G57	I.C. SN74S374N
U192	(see NOTE)	I.C. programmed
U193,U208, U242,U285, U286	51NW9615E98	I.C. SN74LS373N
U194	51NW9615J41	I.C. HD68A45SP
U195,U199 U200,U206, U212,U220, U225,U235, U246	51NW9615C27	I.C. SN74LS157N
U196,U254, U294	51NW9615E99	I.C. SN74LS374N
U197,U209, U222,U232, U243,U255, U256,U264, U265	51NW9615F48	I.C. DM74S151N
U204	(see NOTE)	I.C. programmed
U205,U297	51NW9615G56	I.C. SN74S373N
U207,U241		Not used
U210,U211 U233,U234	51NW9615J36	I.C. SN74LS283N

TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U213,U214, U25J,U262	51NW9615H79	I.C. TMM2016P-1
U216	(see NOTE)	I.C. programmed
U217	51NW9615K88	I.C. MC68661PB
U218	(see NOTE)	I.C. programmed
U219	(see NOTE)	I.C. programmed
U221,U231, U270-U272, U288,J316	51NW9615F02	I.C. SN74LS244N
U223,U224, U244,U245	51NW9615C28	I.C. SN74LS161N
U226,U227, U300	51NW9615H11	I.C. SN74LS645N
U229,U240	51NW9615E84	I.C. SN74LS153N
U236	51NW9615J32	I.C. SN74ALS874NT
U238,U250	51NW9615G11	I.C. MCM21L14P20
U239	(see NOTE)	I.C. programmed
U251	(see NOTE)	I.C. programmed
U252		Not used
U253	51NW9615H57	I.C. SN74LS194AN
U260	51NW9615A03	I.C. MC14011CL
U261,U263		Not used
U268	51NW9615D01	I.C. MC14020BCP
U269	51NW9615C70	I.C. SN74LS139N
U281	51NW9615H35	I.C. MC146818P
U282,U283	51NW9615E96	I.C. SN74LS245N
U284	(see NOTE)	I.C. programmed
U287	(see NOTE)	I.C. programmed
U289,U290	51NW9615F41	I.C. DM74LS164N

TABLE 4-8. SCM Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U298	(see NOTE)	I.C. programmed
U301	51NW9615B01	I.C. SN7412N
U303	51NW9615D93	I.C. SN74S30N
U306-U308	51NW9615F21	I.C. SN74LS03N
U309,U310	51NW9615H89	I.C. SN74LS645-1N
U315	51NW9615E93	I.C. SN74LS14N
U321	51NW9615F30	I.C. DM74S05N
U323	51NW9615J42	I.C. LH0002CN
VR1	48NW9608A31	Diode, zener, 1N5339B, 5.6V
VR2	51NW9615J93	I.C. LM317LZ
Y1	48AW1014B15	Oscillator, crystal, 18.7 MHz
Y2	48AW1016B01	Oscillator, crystal, 16.0 MHz
Y3	48AW1068B03	Oscillator, crystal, 20.0 MHz
Y4	48AW4206B02	Oscillator, crystal, 4.194304 MHz
	09NW9811A86	Socket, DIL, 16-pin (use at U287)
	09NW9811A78	Socket, DIL, 20-pin (use at U298)
	09NW9811A16	Socket, DIL, 24-pin (use at U207, U241)
	09NW9811A64	Socket, DIL, 28-pin (use at U239, U251)
	09NN9811A34	Socket, DIL, 64-pin (use at U252)
	09NW9805B17	Jumper, shorting (use at J2, J10, J11, J15, J16)

NOTE: When ordering, use number labeled on part.

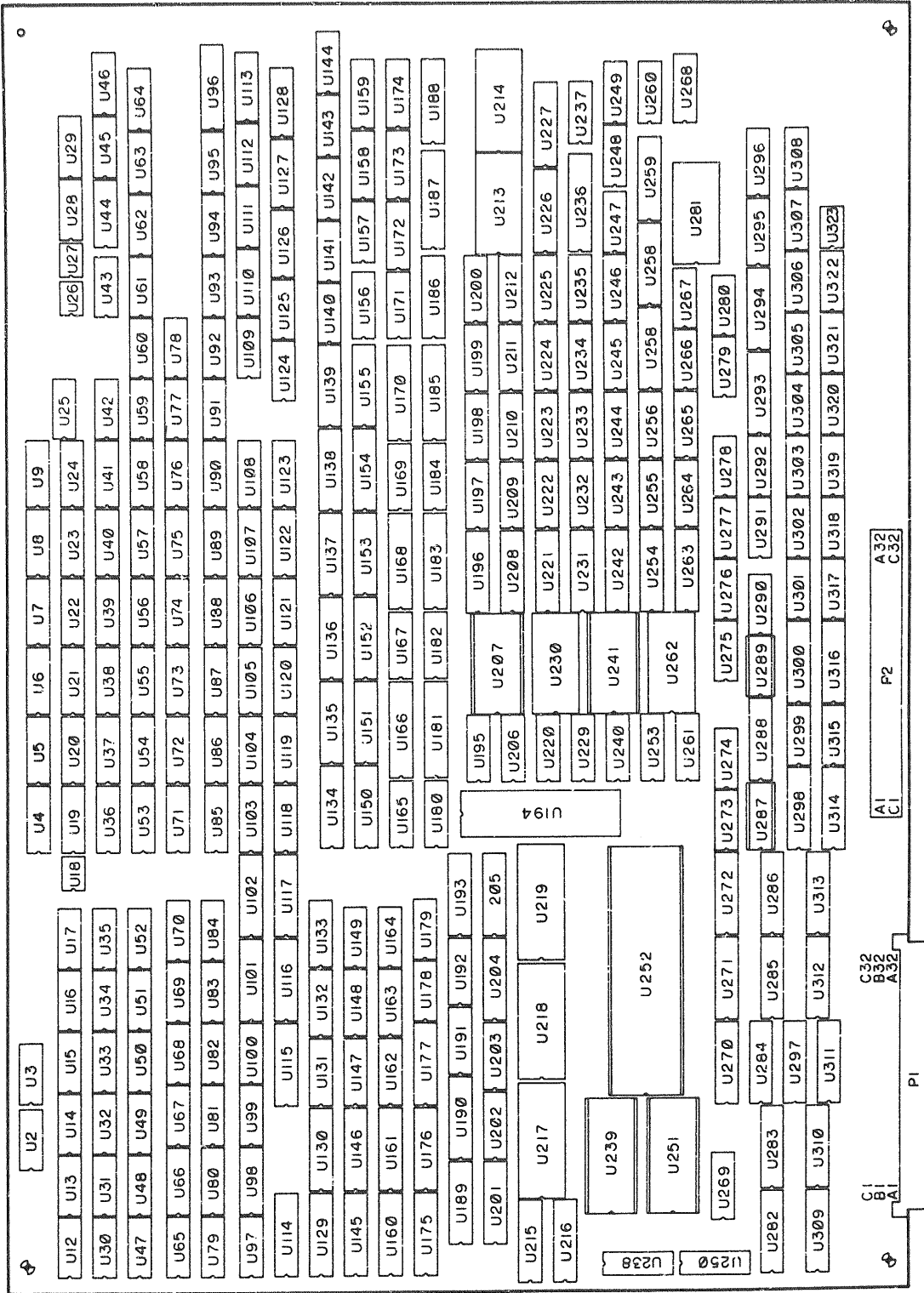


FIGURE 4-1. SCM Parts Location (sheet 1 of 2)



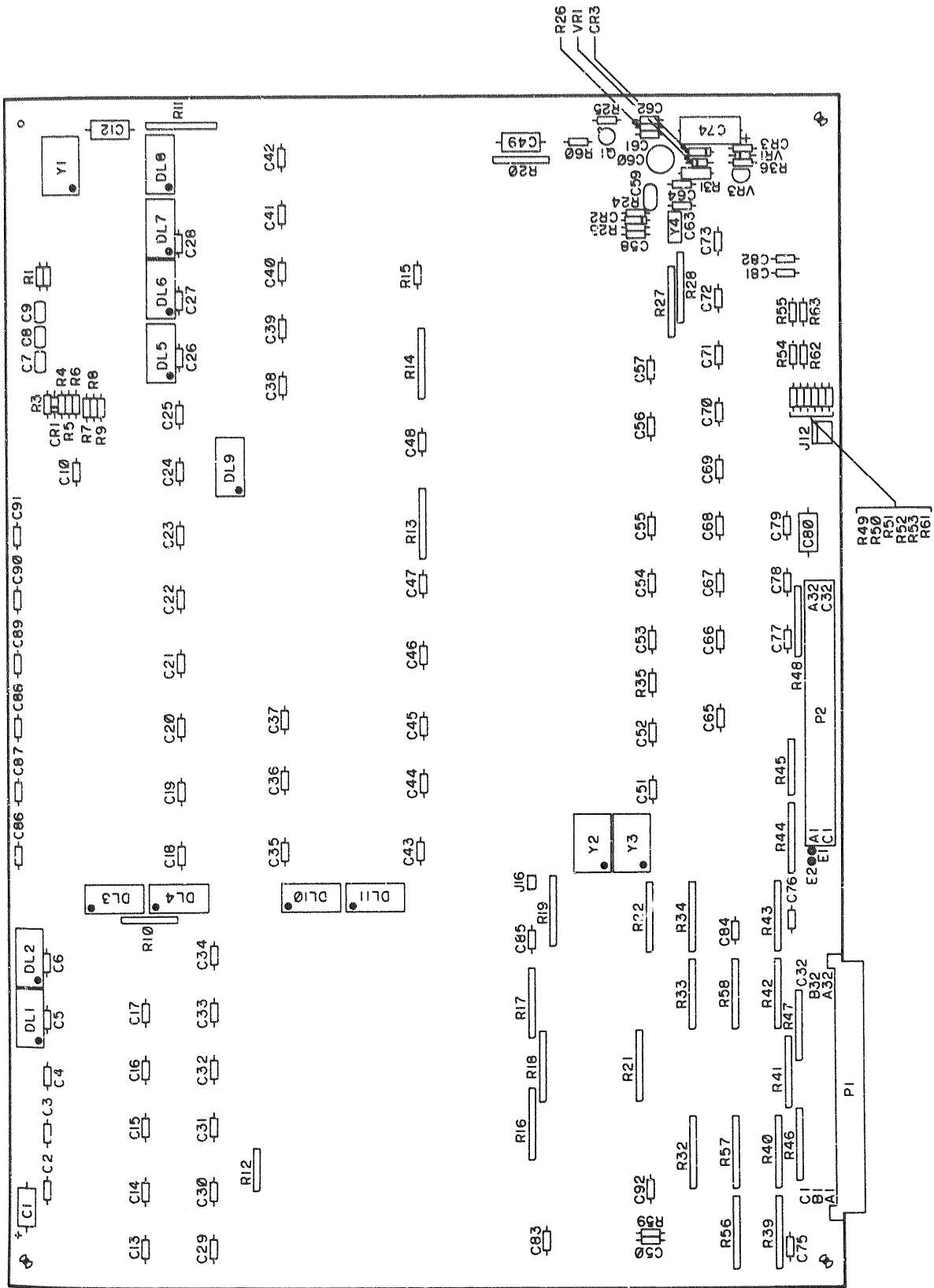


FIGURE 4-1. SCM Parts Location (sheet 2 of 2)

TABLE 4-9. Daughter Board Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8262B01	Printed wiring board
C1,C20	23NW9618A22	Capacitor, electrolytic, 50 uF @ 16 Vdc
C2-C19,C21-C28	21NW9632A03	Capacitor, fixed, ceramic, 0.1 uF @ 50 Vdc
DL1	01NW9804B33	Delay module, 250 ns
J1-J8	28NW9802D21	Header, single row post, 10-pin
R1,R4,R7	51NW9626A49	Resistor network, 7/10K ohm
R2,R3	51NW9626A47	Resistor network, 7/4.7K ohm
R5,R6,R8	51NW9626A37	Resistor network, 9/10K ohm
R9-R19		Not used
R20	06SW-124A17	Resistor, fixed, film, 47 ohm, 5%, 1/4W
U1	51NW9615C21	I.C. SN74LS04N
U2,U10	51NW9615D27	I.C. SN74S32N
U3	51NW9615M11	I.C. MC68010L10
U4	51NW9615M01	I.C. MC68451L10
U5-U7		Not used
U8	51NW9615G38	I.C. SN74LS38N
U9	51NW9615C24	I.C. SN74LS32N
U11	51NW9615C22	I.C. SN74LS08N
U12	51NW9615C69	I.C. SN74LS138N
U13		Not used
U14,U16	51NW9615H11	I.C. SN74LS645N
U15		Not used
U17-U19	51NW9615G56	I.C. SN74S373N
U20		Not used
	09NW9811A34	Socket, DIL, 64-pin (use at U3-U7)

#### 4.5 SCHEMATIC DIAGRAMS

Figures 4-3 and 4-4 illustrate the schematic diagrams for the SCM and the daughter board respectively.

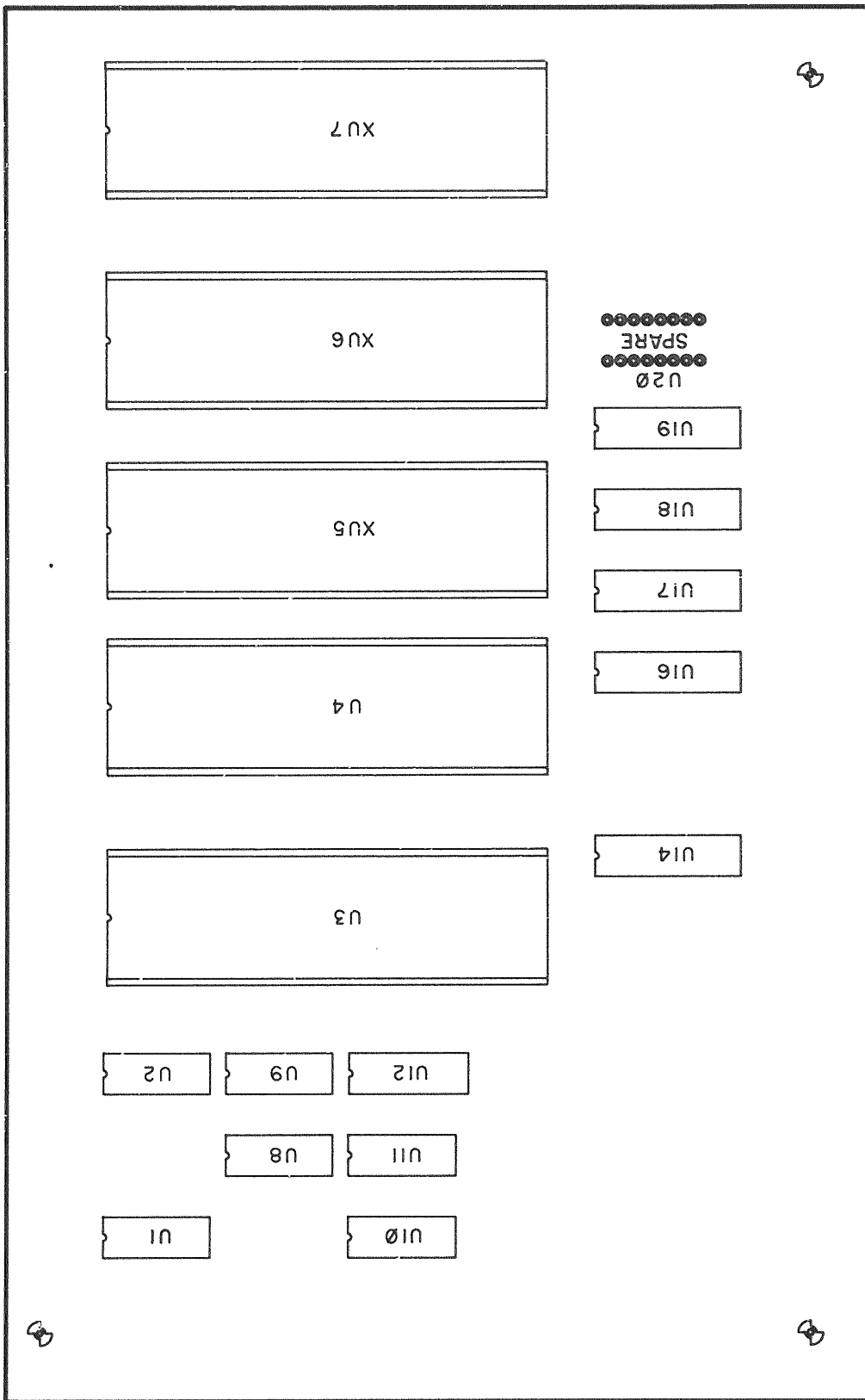


FIGURE 4-2. Daughter Board Parts Location (Sheet 1 of 2)

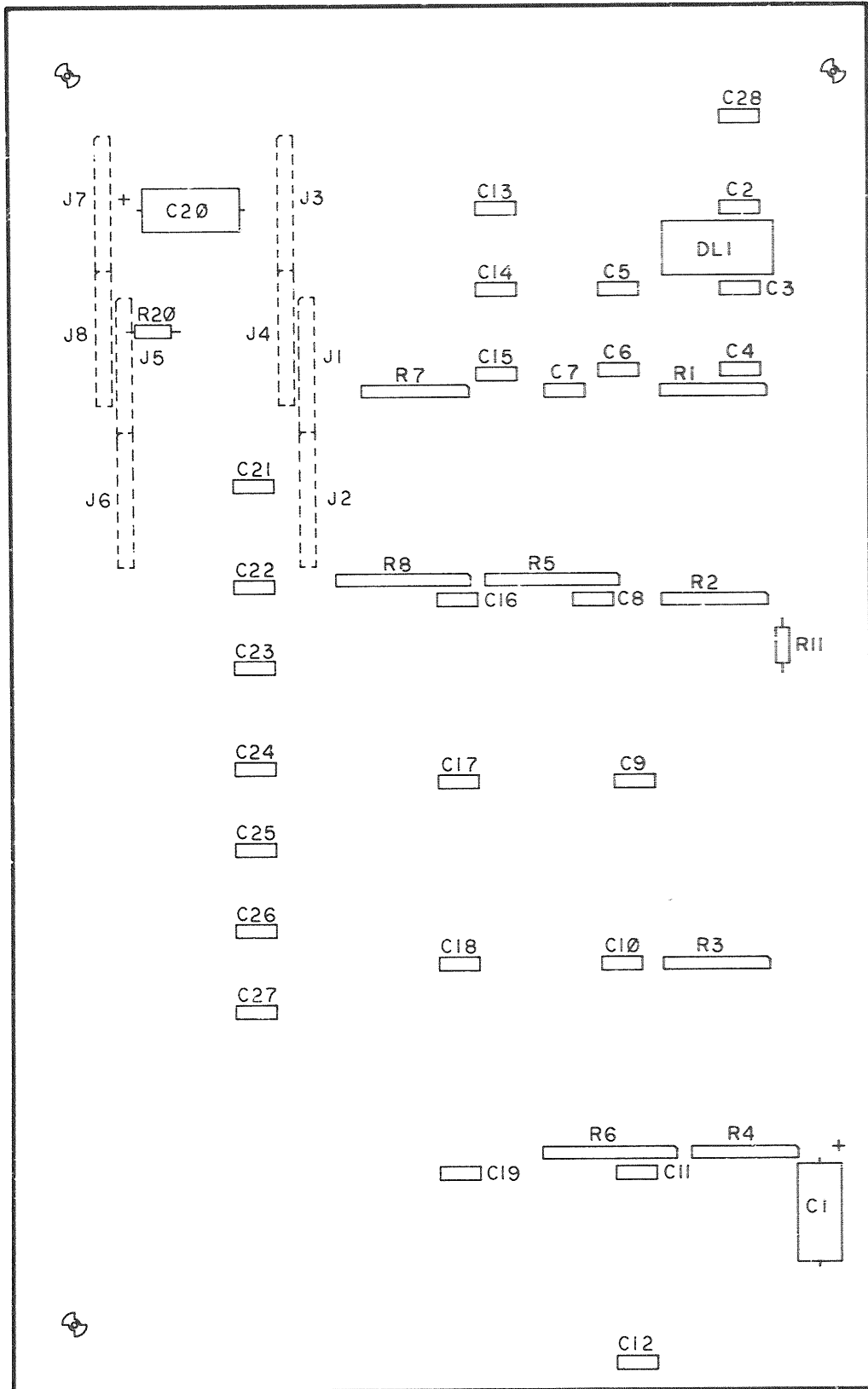


FIGURE 4-2. Daughter Board Parts Location (Sheet 2 of 2)

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3145B01.
2. UNLESS OTHERWISE SPECIFIED:  
ALL RESISTORS ARE IN OHMS,  $\pm 5\text{PCT.}$   
1/4 WATT.  
ALL CAPACITORS ARE IN UF.  
ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
- △ DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:  
\* DENOTES - ACTIVE LOW SIGNAL.  
() DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS. CURRENT REVISION.
- △ PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCE IS AS FOLLOWS:  
SHEET 6 A6 ZONE
- △ NUMBERS IN PARENTHESES ARE FOR 24 PIN DEVICES. REFER TO MANUFACTURER'S CATALOGUE FOR MNEMONICS.
- △ COMPONENTS NOT INSTALLED.

Y4	
VR3	
U323	U1,U228
RT1	
R63	R9
Q3	
P2	
J15	J4
E5	
DL11	
CR4	
C92	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	

TABLE 1

REF DES	TYPE △	GND	+5V	SH
DL1	70NS	7	14	16,27,28
DL2	40NS	7	14	31,32
DL3	215NS	7	14	14
DL4	40NS	7	14	7,11
DL5	215NS	7	14	12
DL6	60NS	7	14	23,31
DL7	30NS	7	14	31
DL8	70NS	7	14	28,31
DL9	42NS	7	14	12,25,29
DL10	30NS	7	14	14
DL11	80NS	7	14	25
U2	74F74	7	14	27
U3	74S64	7	14	26
U4	MSM37256	16	8	8
U5	MSM37256	16	8	5
U6	MSM37256	16	8	8
U7	MSM37256	16	8	9
U8	MSM37256	16	8	8
U9	MSM37256	16	8	9
U10	SPARE			3
U11	SPARE			3
U12	74LS04	7	14	20,22,33
U13	74S22	7	14	28,33
U14	74S08	7	14	10,25,26,29
U15	74LS04	7	14	14,32,33
U16	74LS08	7	14	32
U17	74LS08	7	14	7,14,27,33
U18	SN75176	5	8	22
U19	MSM37256	16	8	8
U20	MSM37256	16	8	9
U21	MSM37256	16	8	8
U22	MSM37256	16	8	9
U23	MSM37256	16	8	8
U24	MSM37256	16	8	9
U25	74LS10	7	14	8
U26	MC1455	1	8	23
U27	SN75176	5	8	22
U28	74S04	7	14	5,12,17,23,26,31
U29	74LS38	7	14	23,33
U30	74LS393	7	14	20
U31	74S38	7	14	3,20,32,34
U32	74S32	7	14	3,25,27,28
U33	74LS10	7	14	32,33
U34	74LS02	7	14	7,12,34
U35	74S51	7	14	20,28
U36	MSM37256	16	8	8
U37	MSM37256	16	8	9
U38	MSM37256	16	8	8
U39	MSM37256	16	8	9
U40	MSM37256	16	8	8
U41	MSM37256	16	8	9
U42	74LS08	7	14	9,17
U43	74LS32	7	14	12,23,28
U44	74LS279	8	16	23
U45	74LS04	7	14	23,28
U46	74S74	7	14	5
U47	74LS393	7	14	20
U48	74LS08	7	14	18,19,20
U49	74S74	7	14	14,29
U50	74S38	7	14	29
U51	74LS04	7	14	7,19,22,29
U52	74LS51	7	14	7

TABLE 1 (CONT)

REF DES	TYPE △	GND	+5V	SH
U53	MSM37256	16	8	8
U54	MSM37256	16	8	9
U55	MSM37256	16	8	8
U56	MSM37256	16	8	9
U57	MSM37256	16	8	8
U58	MSM37256	16	8	9
U59	74S64	7	14	12
U60	74S08	7	14	12
U61	74S11	7	14	12,31
U62	74LS08	7	14	14,17,31
U63	74LS02	7	14	23,2E
U64	74S74	7	14	5
U65	74LS32	7	14	25,31
U66	74LS05	8	16	31
U67	74S02	7	14	25,28,30,31
U68	74LS06	7	14	3,5,7,29
U69	74S08	7	14	11,25,29
U70	74LS74A	7	14	7
U71	MSM37256	16	8	8
U72	MSM37256	16	8	9
U73	MSM37256	16	8	8
U74	MSM37256	16	8	9
U75	MSM37256	16	8	8
U76	MSM37256	16	8	9
U77	74S64	7	14	12
U78	74S08	7	14	12
U79	74F74	7	14	31
U80	74LS139	8	16	31
U81	74LS04	7	14	31
U82	74LS04	7	14	7,17,28,31
U83	74S113	7	14	29
U84	74F74	7	14	32
U85	MSM37256	16	8	8
U86	MSM37256	16	8	9
U87	MSM37256	16	8	8
U88	MSM37256	16	8	9
U89	MSM37256	16	8	8
U90	MSM37256	16	8	9
U91	74S64	7	14	12
U92	74S74	7	14	12
U93	74S74	7	14	12
U94	74S10	7	14	3,12,28
U95	74S38	7	14	21,31
U96	74S248	10	20	5,28
U97	74LS74A	7	14	14,31
U98	74LS279	8	16	28,31
U99	74S38	7	14	31
U100	74S38	7	14	29,31
U101	PAL16L8	10	20	29
U102	PAL16L8	10	20	17
U103	MSM37256	16	8	8
U104	MSM37256	16	8	9
U105	MSM37256	16	8	8
U106	MSM37256	16	8	9
U107	MSM37256	16	8	8
U108	MSM37256	16	8	9
U109	74F74	7	14	12,14
U110	74S174	8	16	12
U111	74S51	7	14	31
U112	74S08	7	14	5,15,31

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FIGURE 4-3. SCM Schematic Diagram (Sheet 1 of 36)

TABLE 1 (CONT)

REF DES	TYPE	GND	+5V	SH
U113	74S175	8	16	5
U114	74S244	10	20	31
U115	PAL16L8	10	20	29
U116	74S240	10	20	29,30
U117	PAL16L8	10	20	17
U118	MSM37256	16	8	8
U119	MSM37256	16	8	9
U120	MSM37256	16	8	8
U121	MSM37256	16	8	9
U122	MSM37256	16	8	8
U123	MSM37256	16	8	9
U124	74LS04	7	14	17,31
U125	74S06	7	14	12,17
U126	74LS390	8	16	17
U127	74S175	8	16	5
U128	74S175	8	16	5
U129	74LS273	10	20	36
U130	74LS240	10	20	35
U131	74S130	8	16	30
U132	74LS148	8	16	30
U133	74LS150	8	16	11
U134	74S299	10	20	10
U135	74S299	10	20	10
U136	74S299	10	20	10
U137	74S299	10	20	10
U138	74S299	10	20	10
U139	74S299	10	20	10
U140	74LS02	7	14	13,17,20,31
U141	74S32	7	14	5,17,27,33
U142	74S74	7	14	5
U143	74S51	7	14	5
U144	74S74	7	14	5
U145	74LS273	10	20	36
U146	PAL12L6	10	20	32
U147	74S85	8	16	30
U148	74LS148	8	16	30
U149	74LS32	7	14	7,10,19
U150	PAL16L8	10	20	18
U151	PAL16L8	10	20	18
U152	PAL16L8	10	20	18
U153	PAL16L8	10	20	18
U154	PAL16L8	10	20	18
U155	PAL16L8	10	20	18
U156	74LS193	8	16	17
U157	74F74	7	14	5
U158	74S133	8	16	17
U159	74S163	8	16	17
U160	74LS273	10	20	36
U161	PAL12L6	10	20	32
U162	74LS151	8	16	32
U163	74LS174	8	16	30
U164	74LS04	7	14	17,18,26,30
U165	74LS251	8	16	18
U166	74LS646	12	24	11
U167	74LS251	8	16	18
U168	74LS646	12	24	11
U169	74LS251	8	16	18
U170	74LS646	12	24	11
U171	74LS193	8	16	17
U172	74LS193	8	16	17

TABLE 1 (CONT)

REF DES	TYPE	GND	+5V	SH
U173	74S163	8	16	17
U174	74S163	8	16	17
U175	74LS273	10	20	36
U176	PAL12L6	10	20	32
U177	PAL12L6	10	20	32
U178	74LS10	7	14	3,22
U179	74S20	7	14	14,19
U180	74LS251	8	16	18
U181	74LS646	12	24	11
U182	74LS251	8	16	18
U183	74LS646	12	24	11
U184	74LS251	8	16	18
U185	74LS646	12	24	11
U186	74LS273	10	20	17
U187	74ALS874	12	24	17
U188	74LS273	10	20	17
U189	74LS273	10	20	36
U190	74S374	10	20	32
U191	74LS151	8	16	32
U192	82S123	8	16	32
U193	74LS373	10	20	18
U194	MC68A45	1	20	6
U195	74LS157	8	16	6
U196	74LS374	10	20	14
U197	74S151	8	16	6
U198	74LS174	8	16	7
U199	74LS157	8	16	16
U200	74LS157	8	16	16
U201	74LS273	10	20	36
U202	74LS148	8	16	32
U203	74LS150	8	16	19
U204	PAL16L8	10	20	19
U205	74S373	10	20	6
U206	74LS157	8	16	6
U207	MK4802	12	24	13
U208	74LS373	10	20	14
U209	74S151	8	16	6
U210	74LS283	8	16	7
U211	74LS283	8	16	7
U212	74LS157	8	16	16
U213	TMM2016P1	12	24	16
U214	TMM2016P1	12	24	16
U215	74LS273	10	20	36
U216	PAL12L6	10	20	35
U217	MC2661	4	26	22
U218	82S100	14	28	19
U219	82S100	14	28	19
U220	74LS157	8	16	6
U221	74LS244	10	20	14
U222	74S151	8	16	6
U223	74LS161	8	16	7
U224	74LS161	8	16	7
U225	74LS157	8	16	16
U226	74LS645	10	20	16
U227	74LS645	10	20	16
U228	74LS153	8	16	13
U229	MK4802	12	24	13
U230	74LS244	10	20	14
U231	74S151	8	16	6
U232	74S151	8	16	6
U233	74LS283	8	16	7

TABLE 1 (CONT)

REF DES	TYPE	GND	+5V	+5BB	SH
U234	74LS283	8	16		7
U235	74LS157	8	16		16
U236	74ALS873	12	24		16
U237	74LS04	7	14		6,15
U238	MCM21L14	9	18		35
U239	(MCM68766)	12	24		33
U240	74LS153	8	16		13
U241	MK4802	12	24		13
U242	74LS373	10	20		14
U243	74S151	8	16		6
U244	74LS161	8	16		7
U245	74LS161	8	16		7
U246	74LS157	8	16		16
U247	74LS86	7	14		16
U248	74LS86	7	14		16
U249	74LS32	7	14		15,28
U250	MCM21L14	9	18		35
U251	(MCM68766)	12	24		33
U252	MC68010	16	14		24
U252	MC68010	53	49		24
U253	74LS194A	8	16		34
U254	74LS374	10	20		14
U255	74S151	8	16		6
U256	74S151	8	16		6
U257	74S374	10	20		15
U258	74LS299	10	20		15
U259	74LS299	10	20		15
U260	MCI40110	7		14	21
U261	SPARE				3
U262	MK4802	12	24		13
U263	SPARE				3
U264	74S151	8	16		6
U265	74S151	8	16		6
U266	74S20	7	14		15
U267	74S20	7	14		15
U268	MCI40200	8		16	21
U269	74LS139	8	16		35
U270	74LS244	10	20		25
U271	74LS244	10	20		25
U272	74LS244	10	20		25
U273	74LS393	7	14		23
U274	74S04	7	14		6,16,23,27
U275	74LS10	7	14		18,26,34
U276	74LS00	7	14		16,21
U277	74LS00	7	14		16,25
U278	74S64	7	14		15
U279	74S64	7	14		15
U280	74S64	7	14		15
U281	MC146818	12		24	21
U282	74LS245	10	20		26
U283	74LS245	10	20		26
U284	TRP18S22	10	20		25
U285	74LS373	10	20		25
U286	74LS373	10	20		25
U287	82S129	8	16		26
U288	74LS244	10	20		34
U289	74LS164	7	14		30
U290	74LS164	7	14		21
U291	74LS10	7	14		16,21
U292	74S04	7	14		15

TABLE 1 (CONT)

REF DES	TYPE	GND	+5V	SH
U293	74S374	10	20	15
U294	74LS374	10	20	21
U295	74LS150	8	16	21
U296	74LS150	8	16	21
U297	74S373	10	20	25
U298	PAL 5L2	10	20	27
U299	74LS04	7	14	3,16,21,34
U300	74LS64	10	20	34
U301	7412	7	14	21,33,34
U302	74S00	7	14	21,26,34
U303	74S00	7	14	15
U304	74S00	7	14	15
U305	74S00	7	14	15
U306	74LS03	7	14	21
U307	74LS03	7	14	21
U308	74LS03	7	14	21
U309	LS645	10	20	26
U310	LS645	10	20	26
U311	74S244	10	20	25
U312	74S244	10	20	25
U313	74S244	10	20	25
U314	74S244	10	20	26
U315	74LS14	7	14	32,34
U316	74LS244	10	20	34
U317	74LS51	7	14	26
U318	74S00	7	14	26,27
U319	74F74	7	14	27
U320	74S00	7	14	15,18
U321	74S00	7	14	15,33
U322	74S00	7	14	15,18,19
U323	LH0002C			19
Y1	K114B	7	14	5
Y2	K116A	7	14	23
Y3	K116A	7	14	23

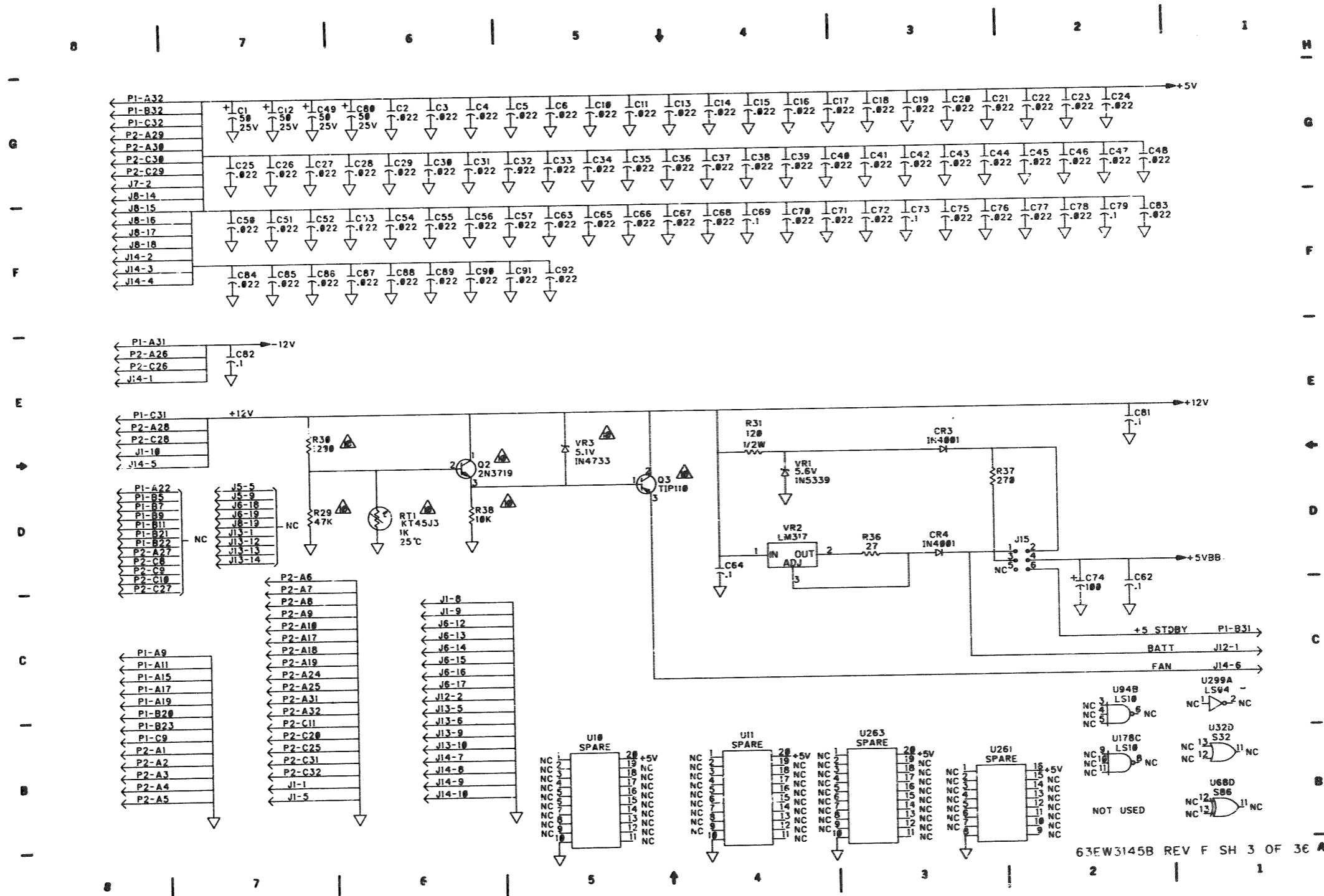


FIGURE 4-3. SCM Schematic Diagram (Sheet 3 of 36) 4-35/4-36

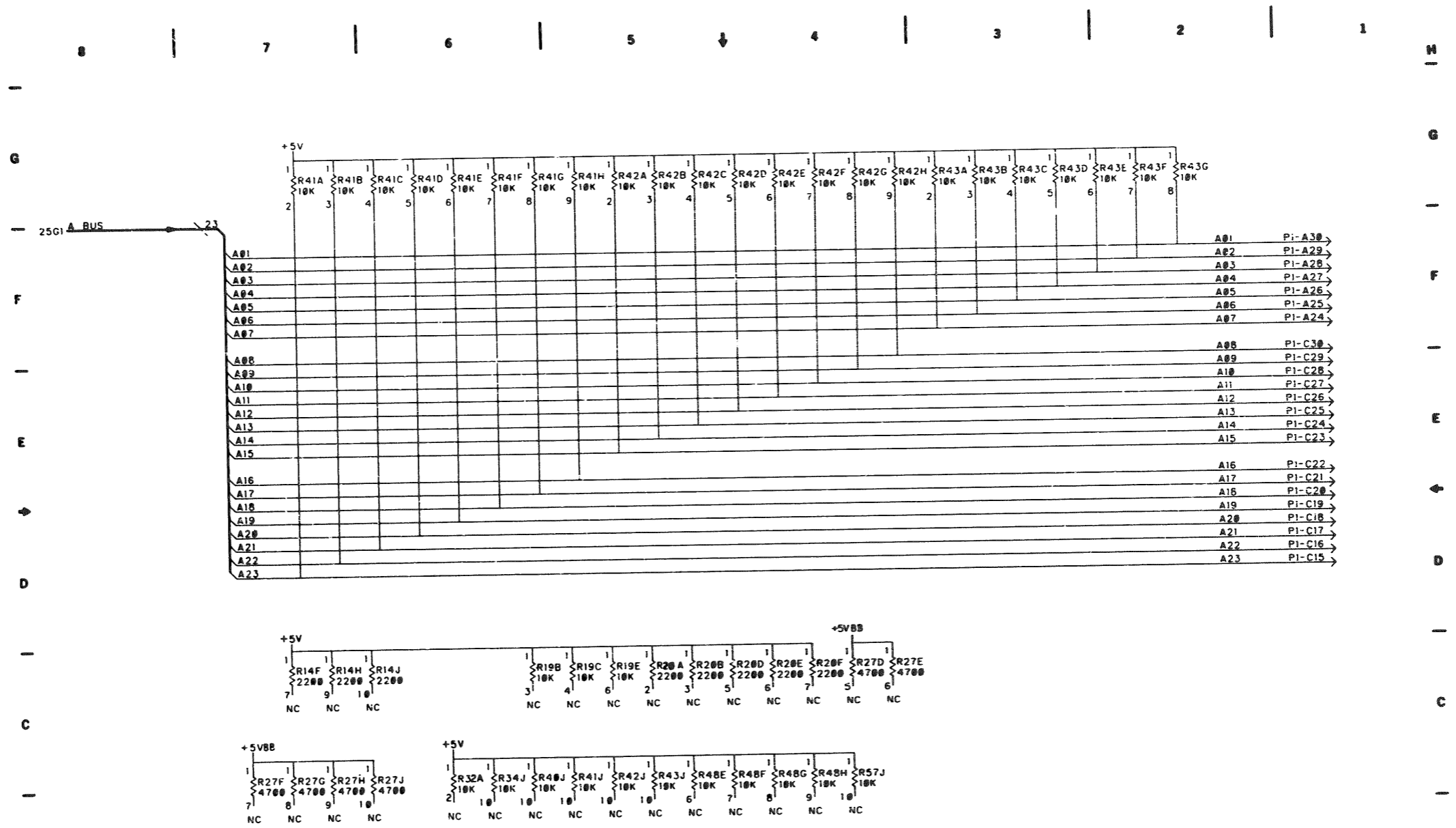


FIGURE 4-3. SCM Schematic Diagram (Sheet 4 of 36)



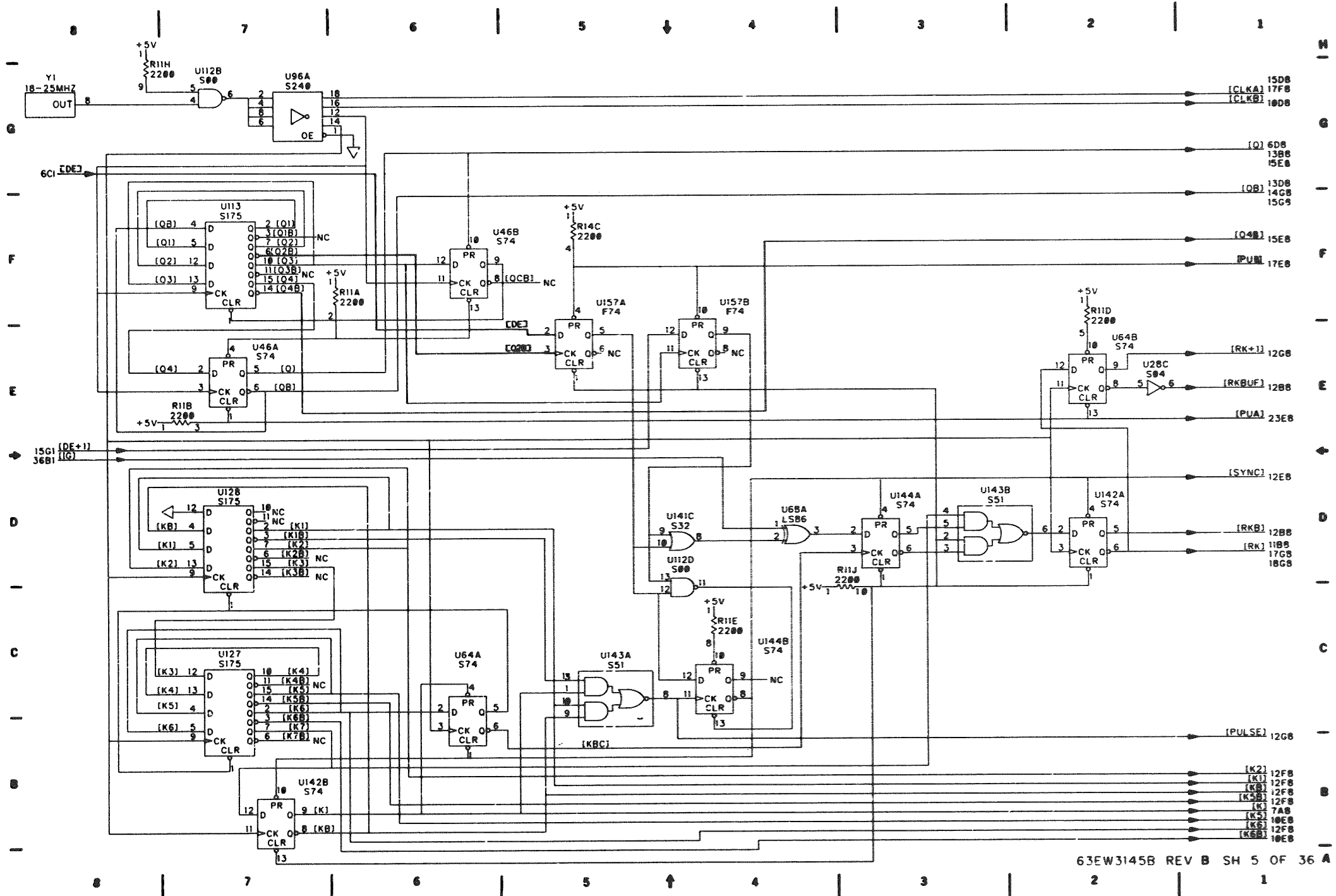
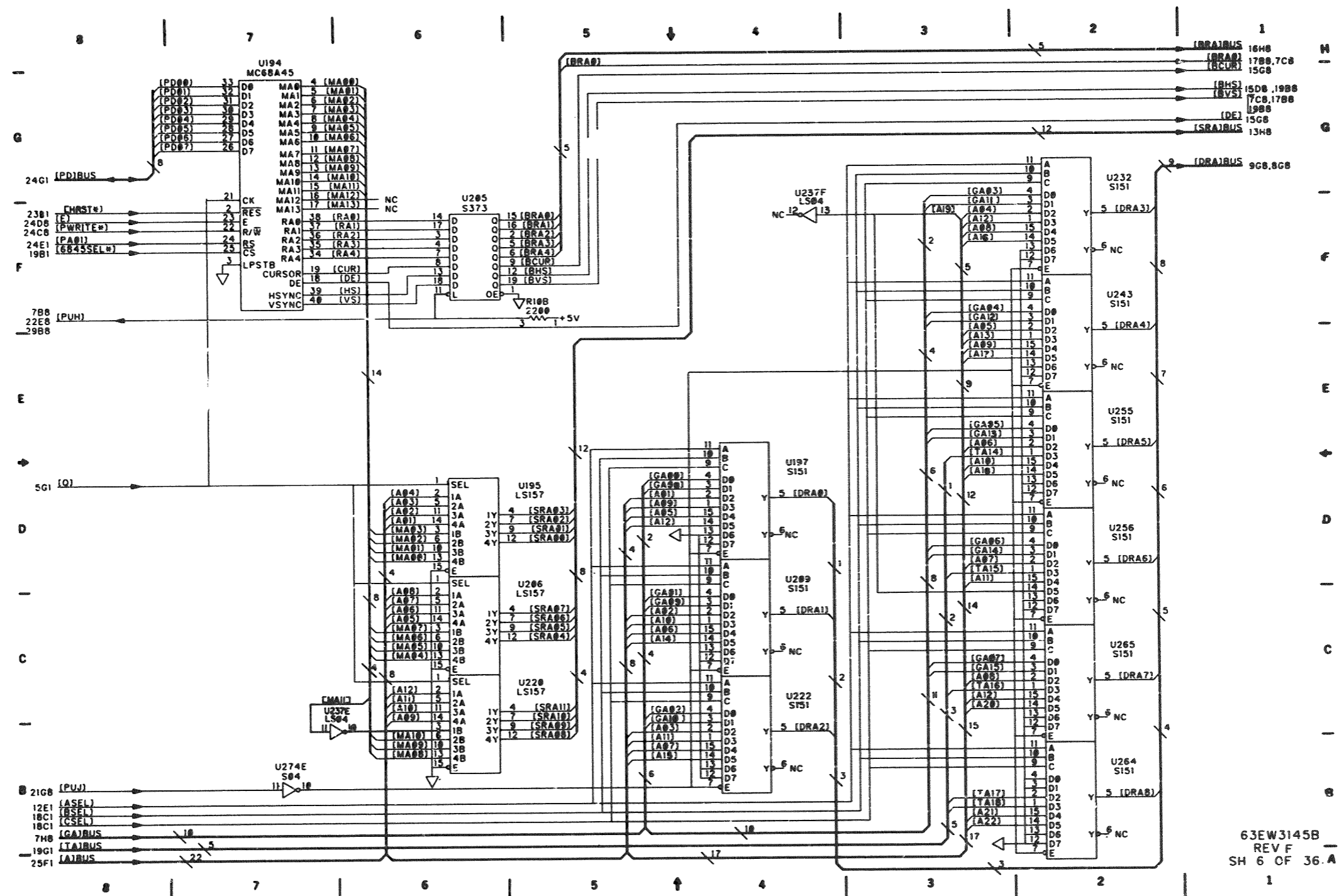


FIGURE 4-3. SOM Schematic Diagram (Sheet 5 of 36) 4-39/4-40



63EW3145B  
REV F  
SH 6 OF 36.A  
1

FIGURE 4-3. SCM Schematic Diagram (Sheet 6 of 36)

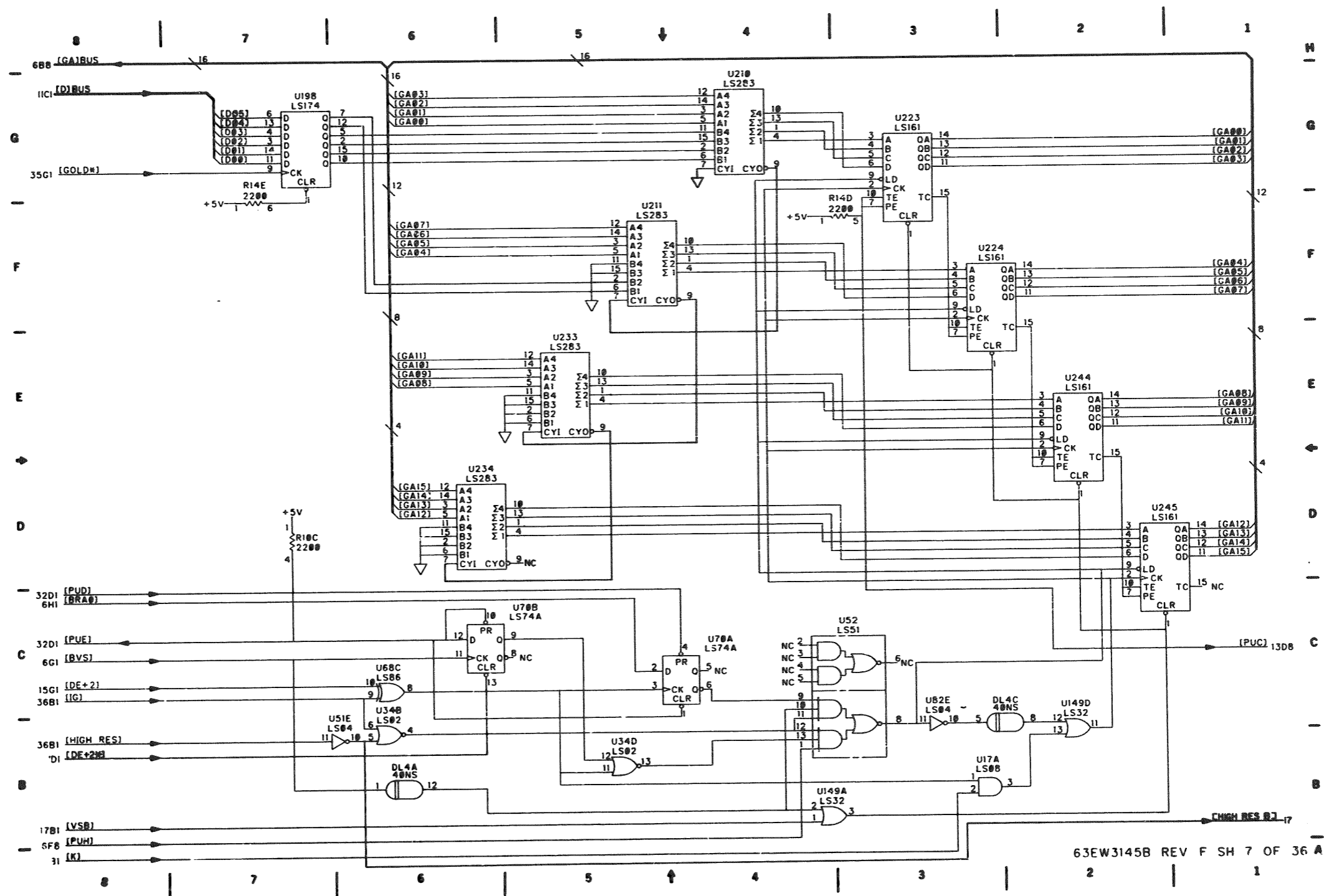


FIGURE 4-3. SCM Schematic Diagram (Sheet 7 of 36)

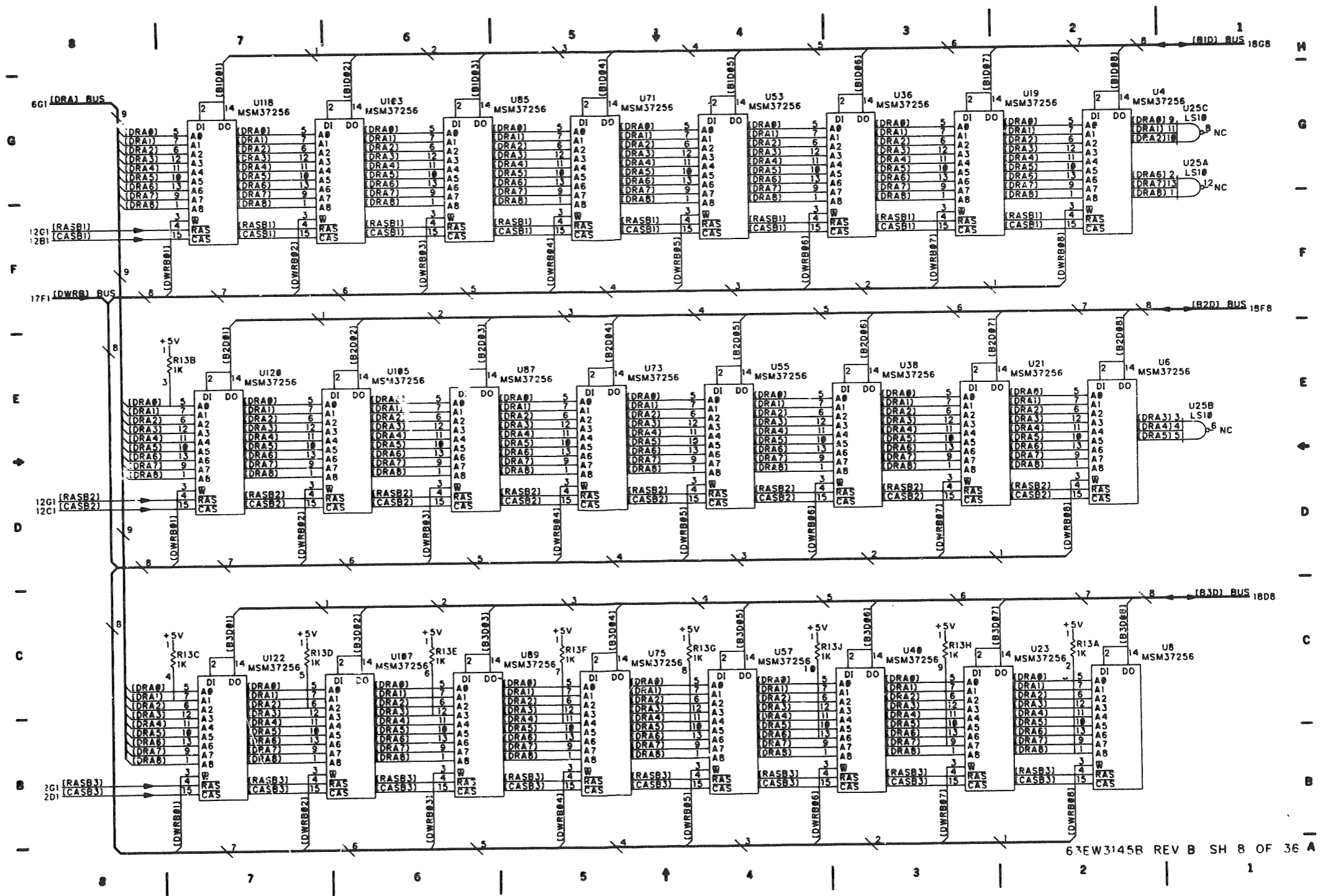


FIGURE 4-3. SCM Schematic Diagram (Sheet 8 of 36) 4-45/4-46

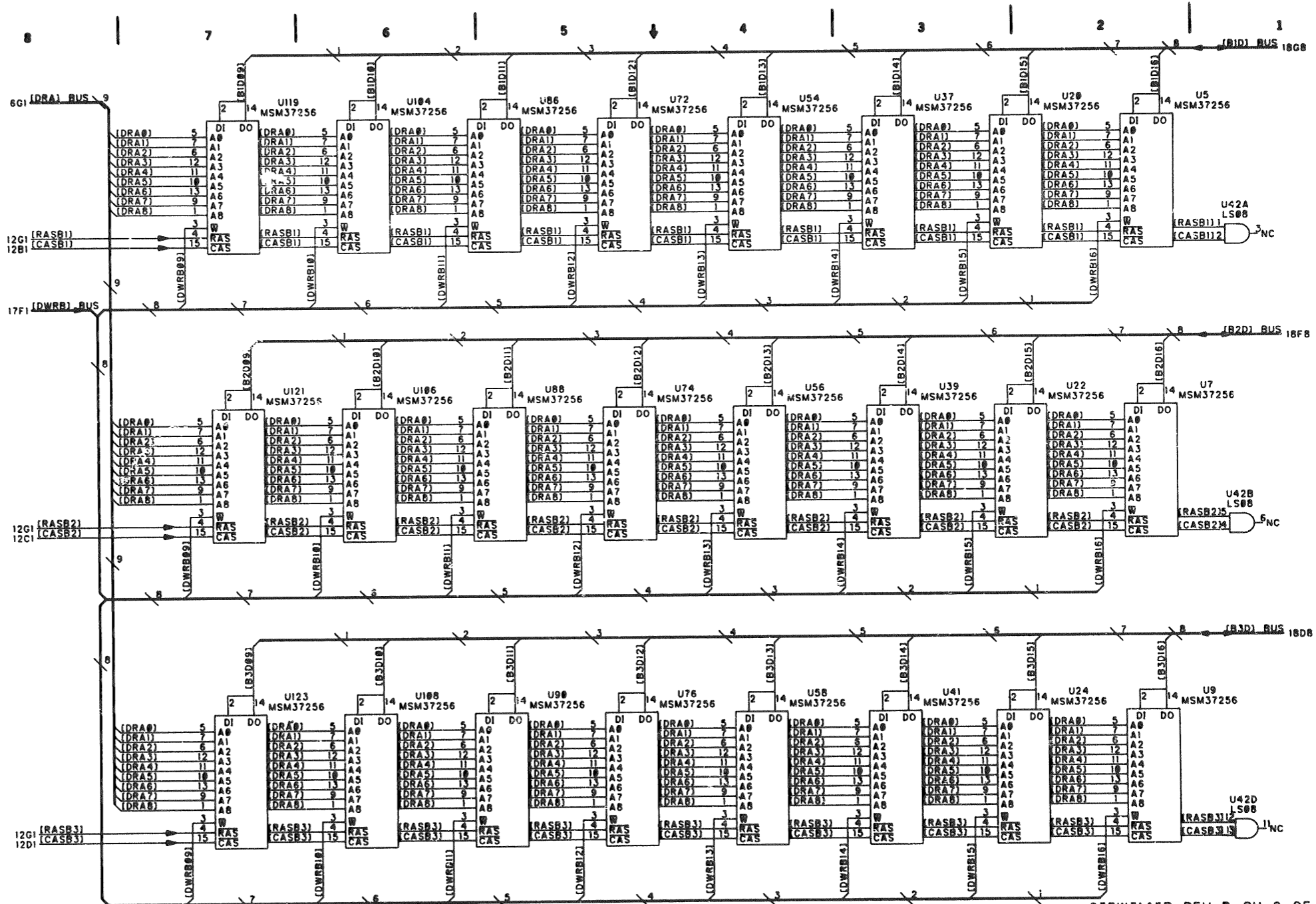


FIGURE 4-3. SCM Schematic Diagram (Sheet 9 of 36) 4-47/4-48

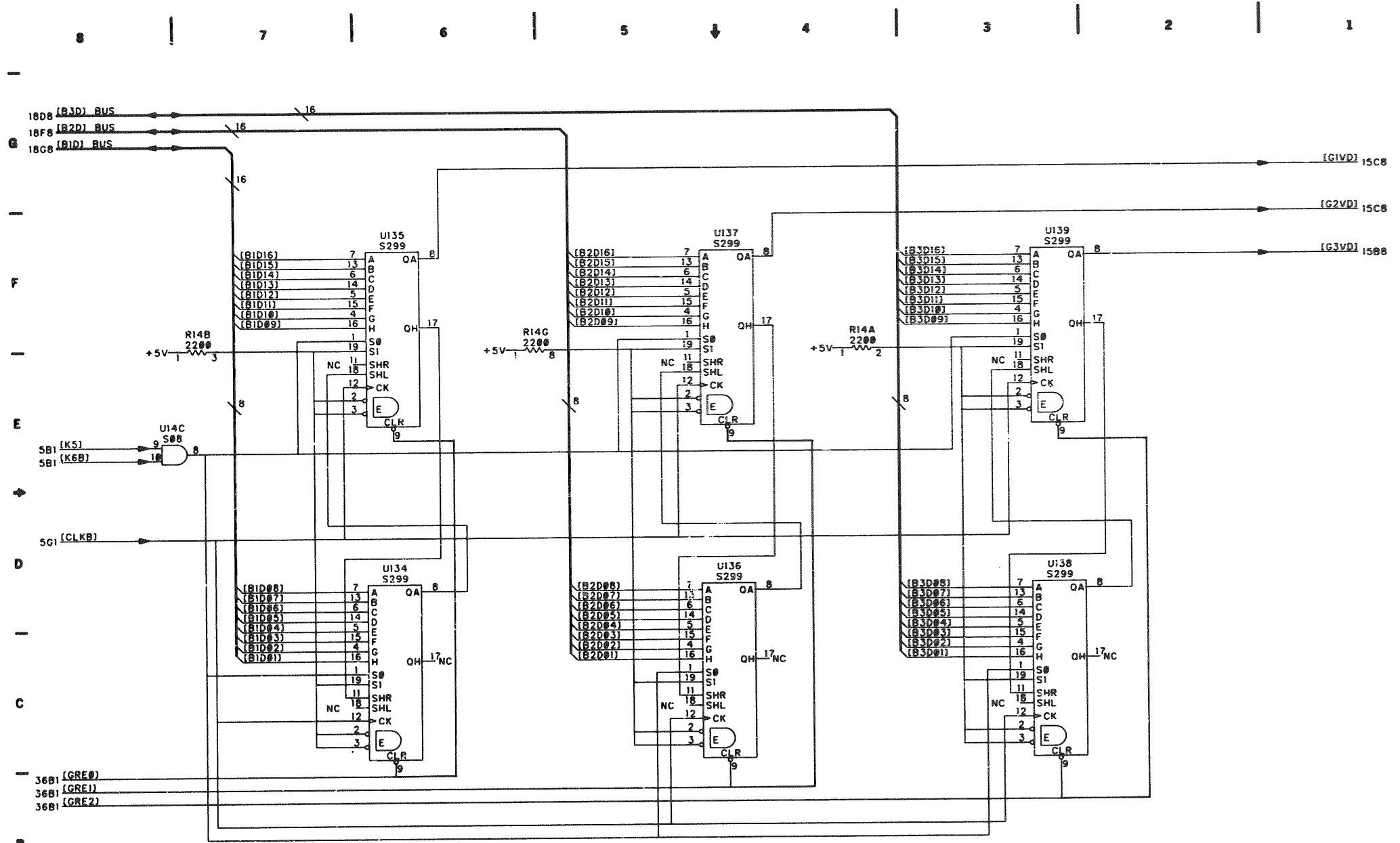
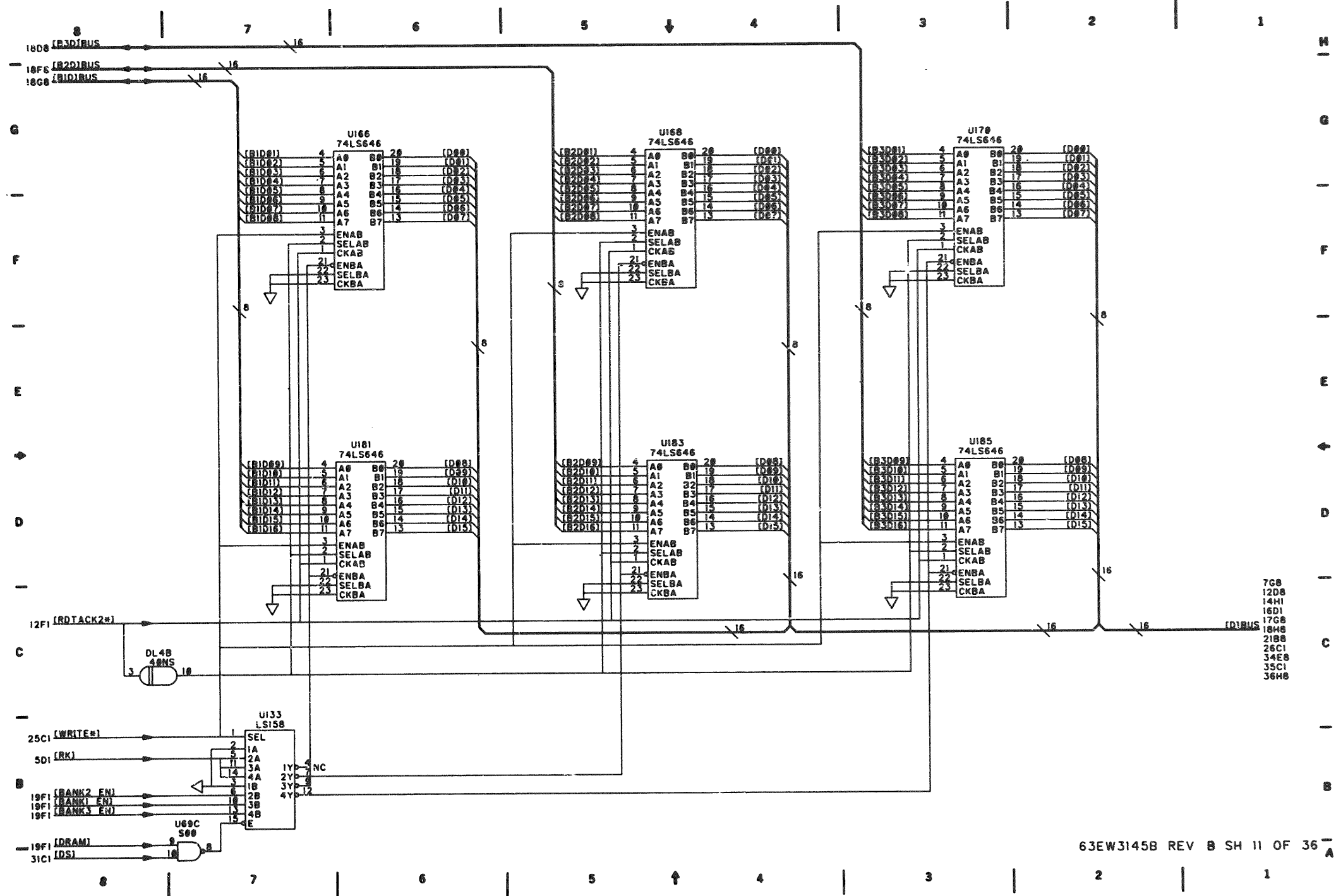
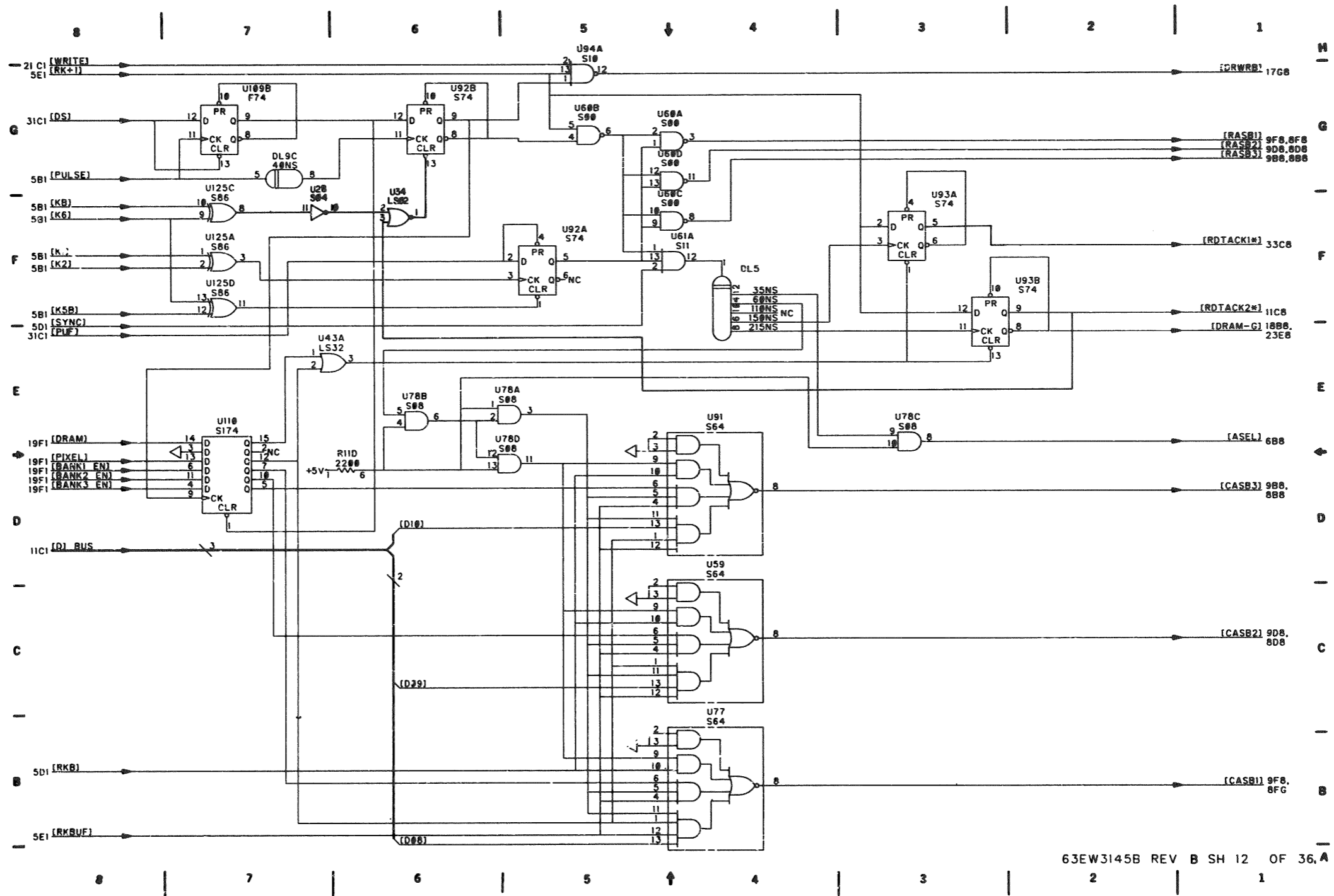


FIGURE 4-3. SCM Schematic Diagram (Sheet 10 of 36)



63EW3145B REV B SH 11 OF 36

FIGURE 4-3. SCM Schematic Diagram (Sheet 11 of 36)



63EW3145B REV B SH 12 OF 36, A

FIGURE 4-3. SCM Schematic Diagram (Sheet 12 of 36)



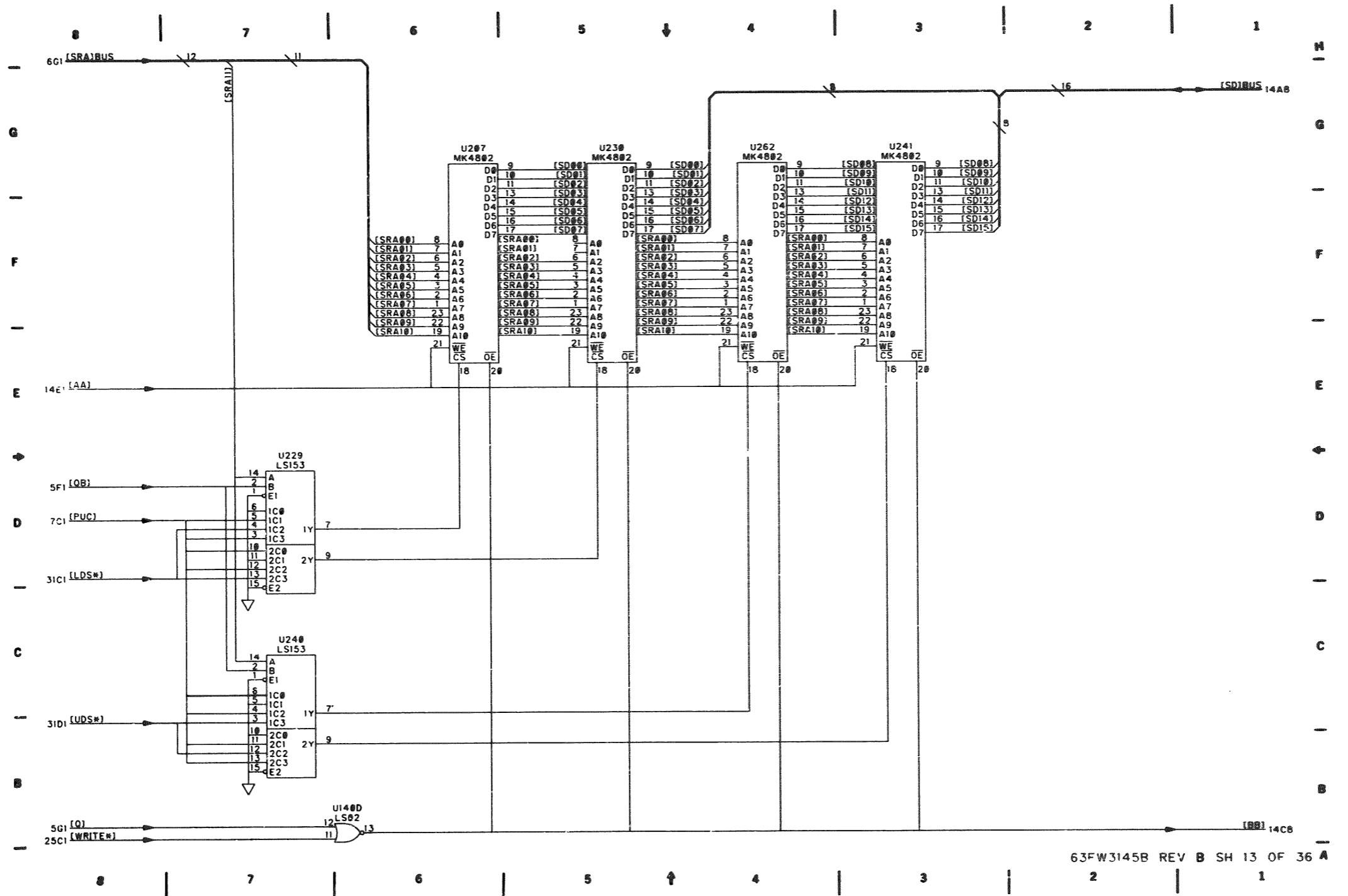


FIGURE 4-3. SCM Schematic Diagram (Sheet 13 of 36)

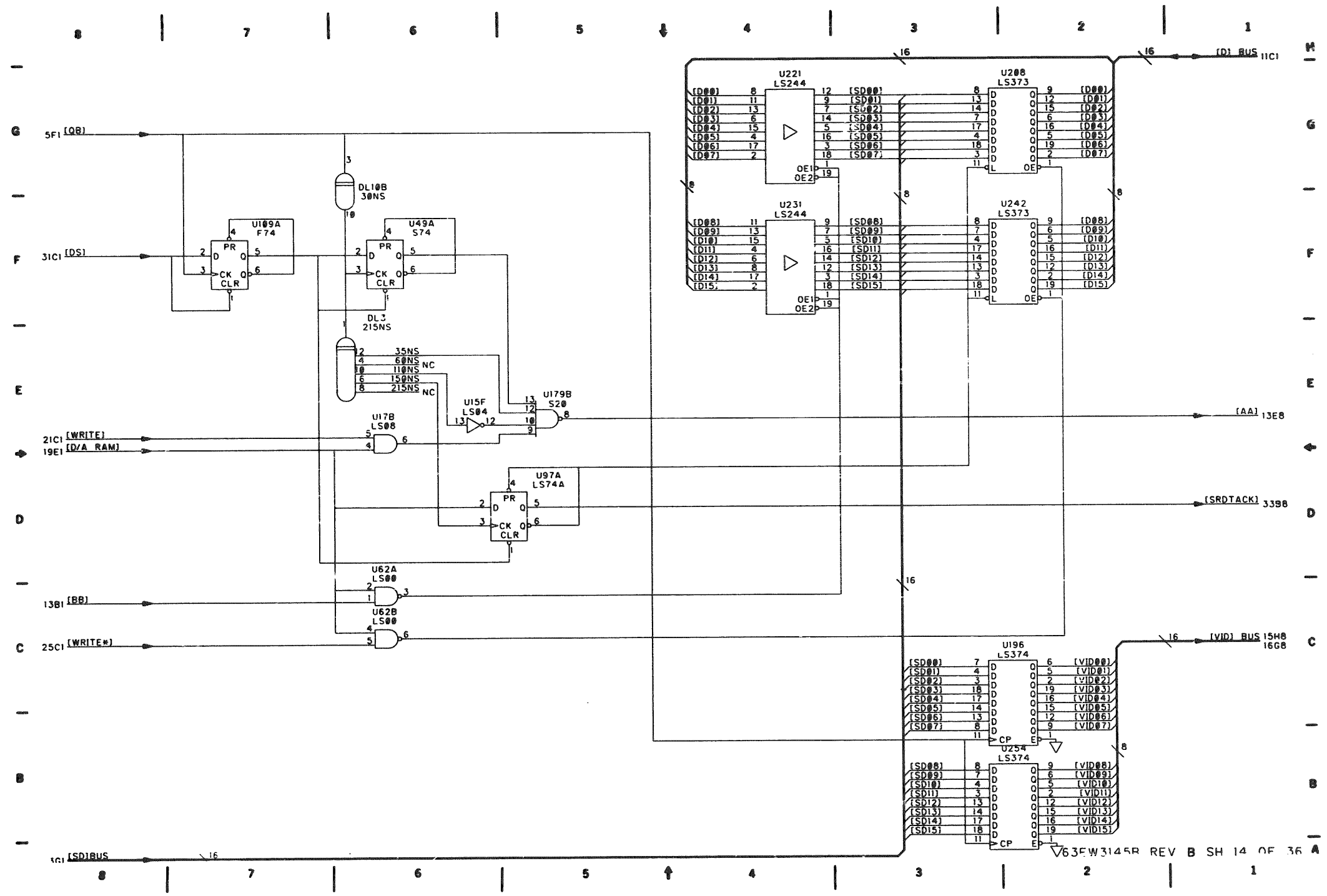


FIGURE 4-3. SOM Schematic Diagram (Sheet 14 of 36)

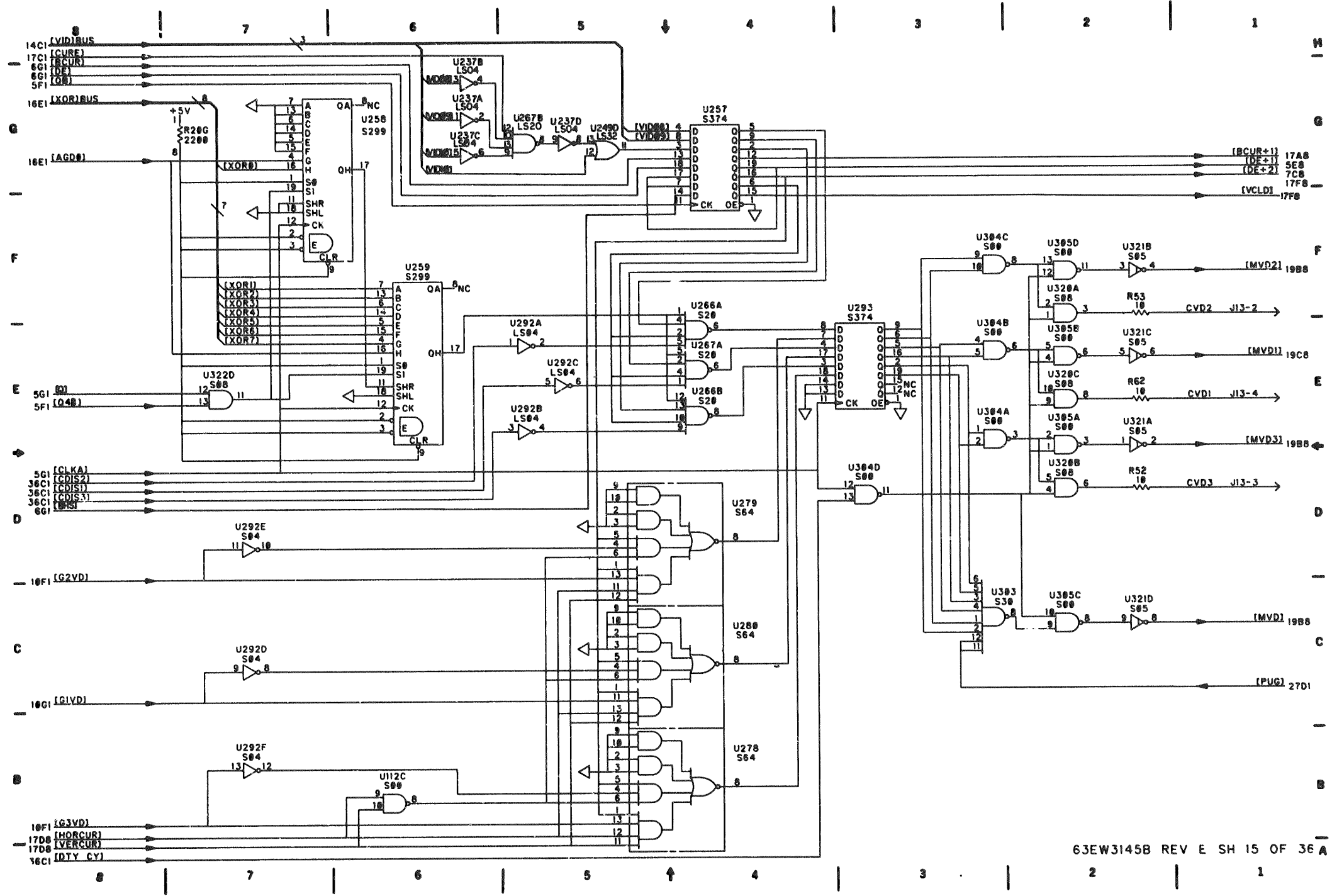
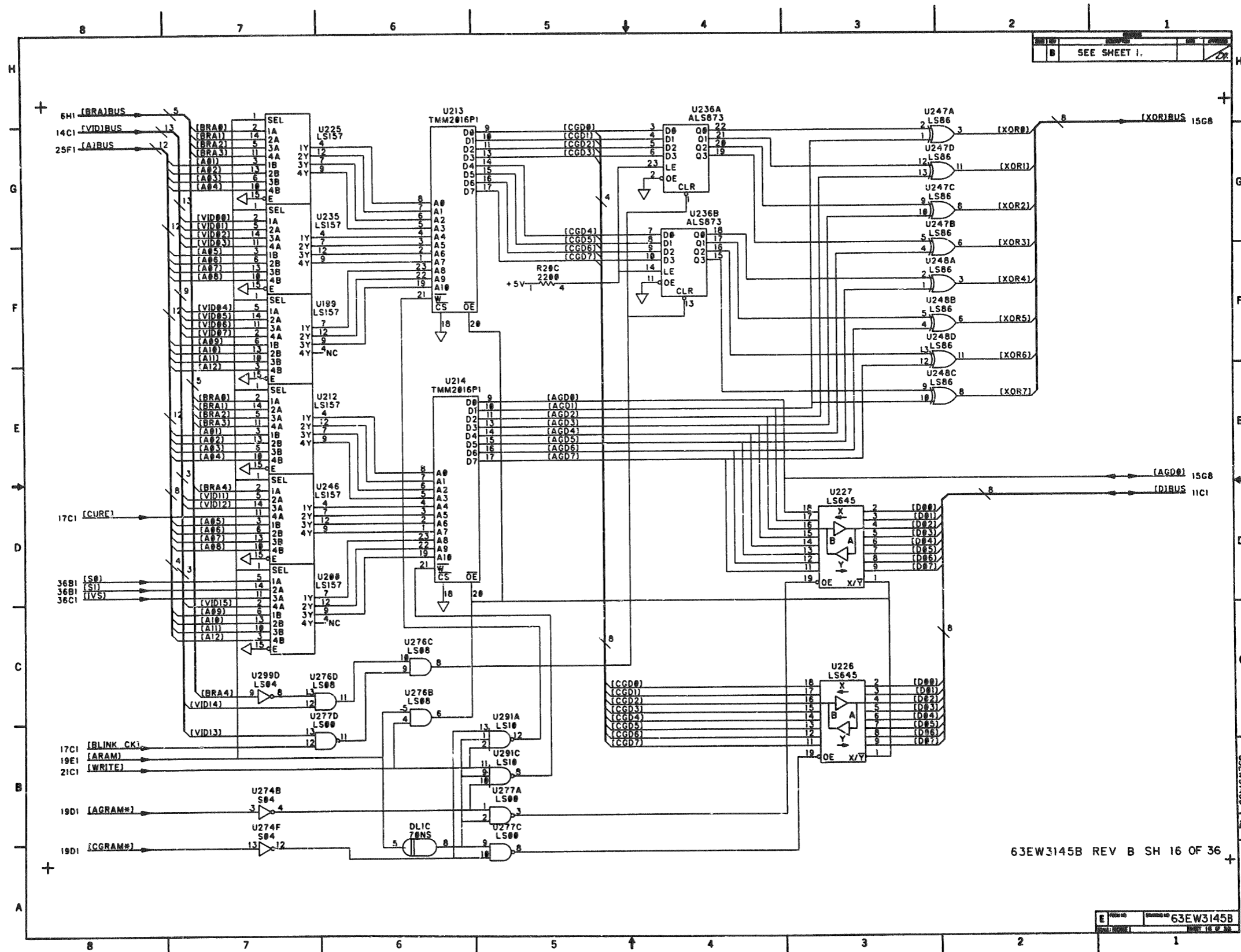


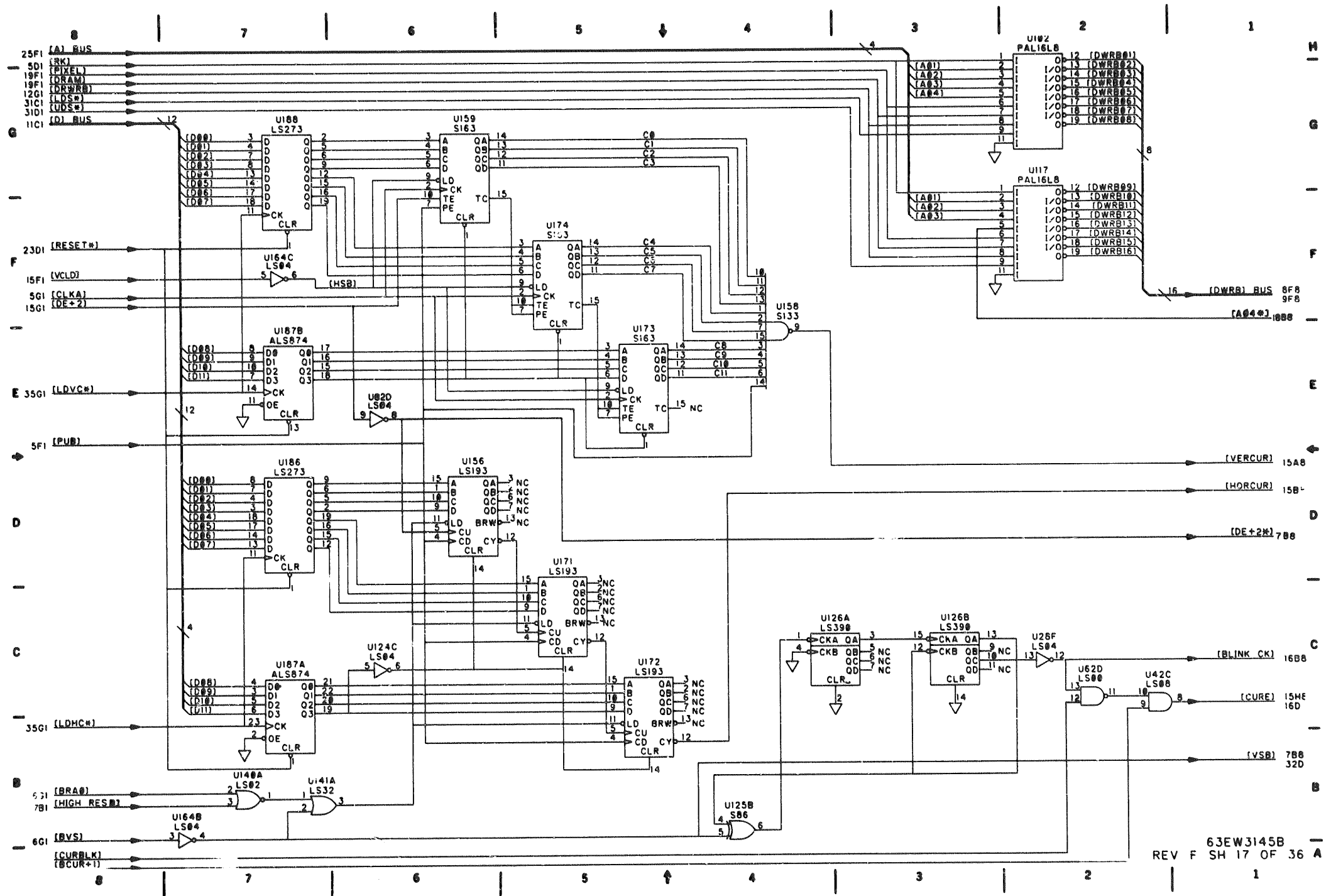
FIGURE 4-3. SCM Schematic Diagram (Sheet 15 of 36)



63EW3145B REV B SH 16 OF 36

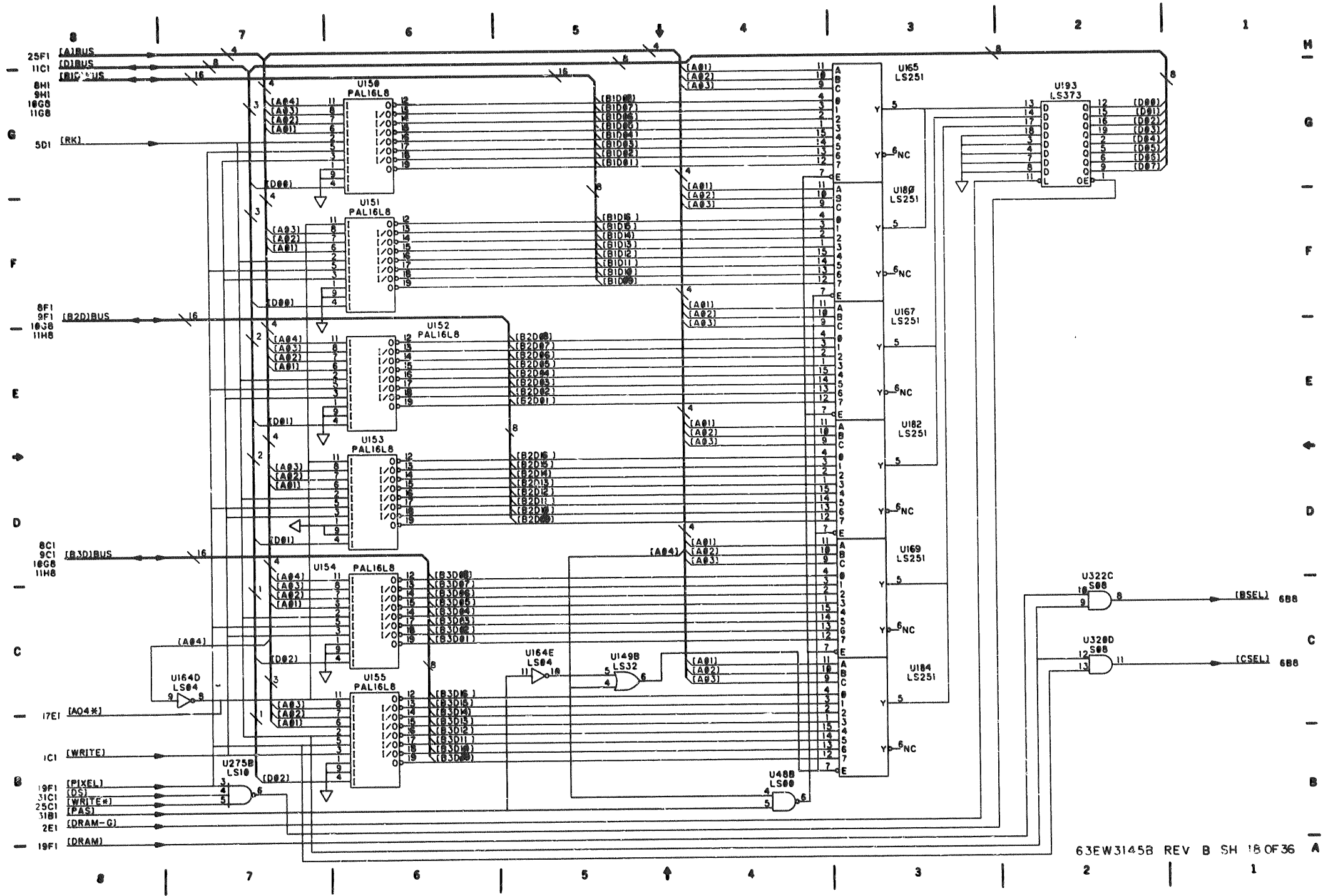
63EW3145B  
REV B SH 16 OF 36

FIGURE 4-3. SCM Schematic Diagram (Sheet 16 of 36)



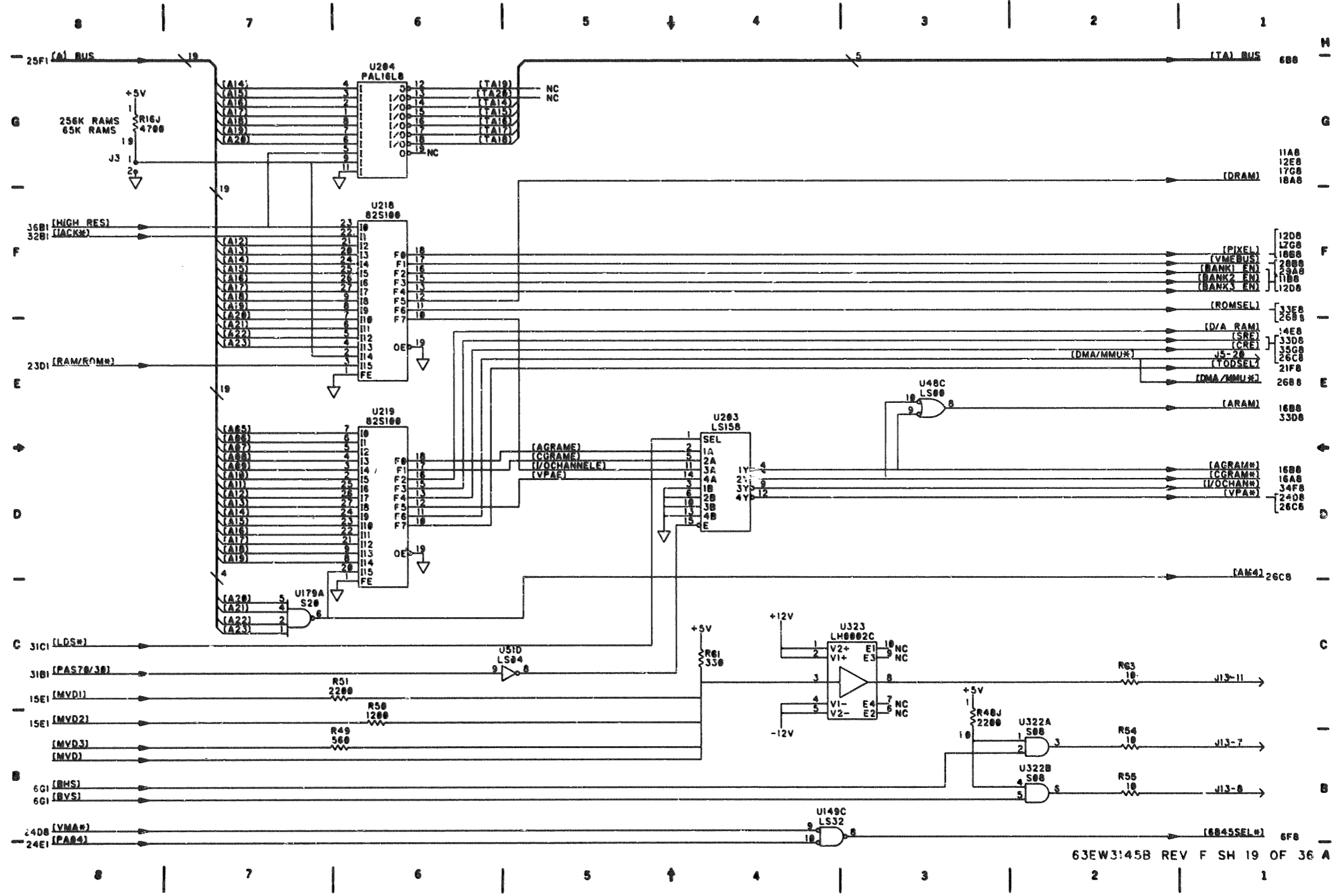
63EW3145B  
REV F SH 17 OF 36 A

FIGURE 4-3. SCM Schematic Diagram (Sheet 17 of 36) 4-63/4-64



63EW3145B REV B SH 18 OF 36

FIGURE 4-3. SCM Schematic Diagram (Sheet 18 of 36)



63EW3:45B REV F SH 19 OF 36 A

FIGURE 4-3. SQM Schematic Diagram (Sheet 19 of 36) 4-67/4-68

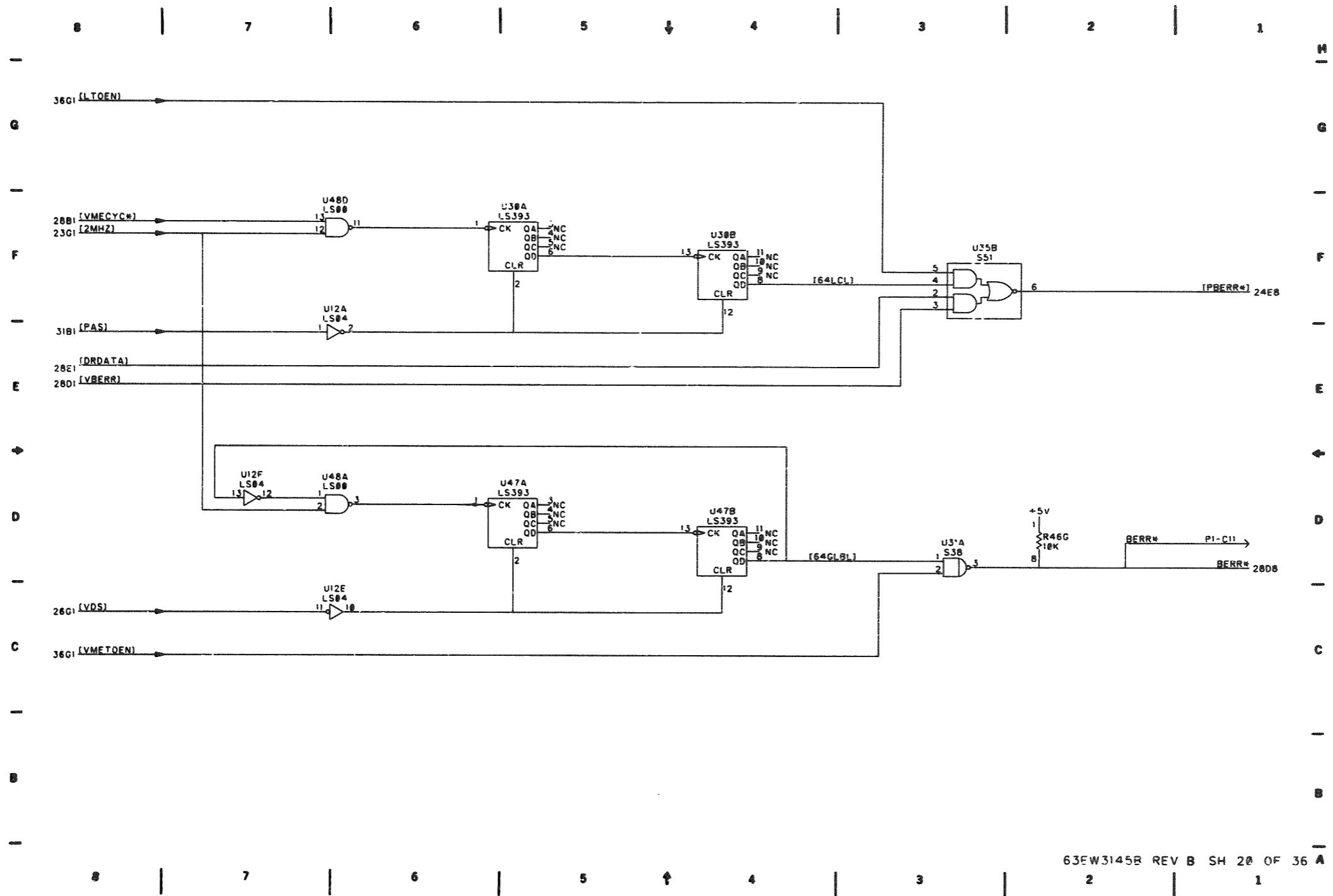


FIGURE 4-3. SCM Schematic Diagram (Sheet 20 of 36)



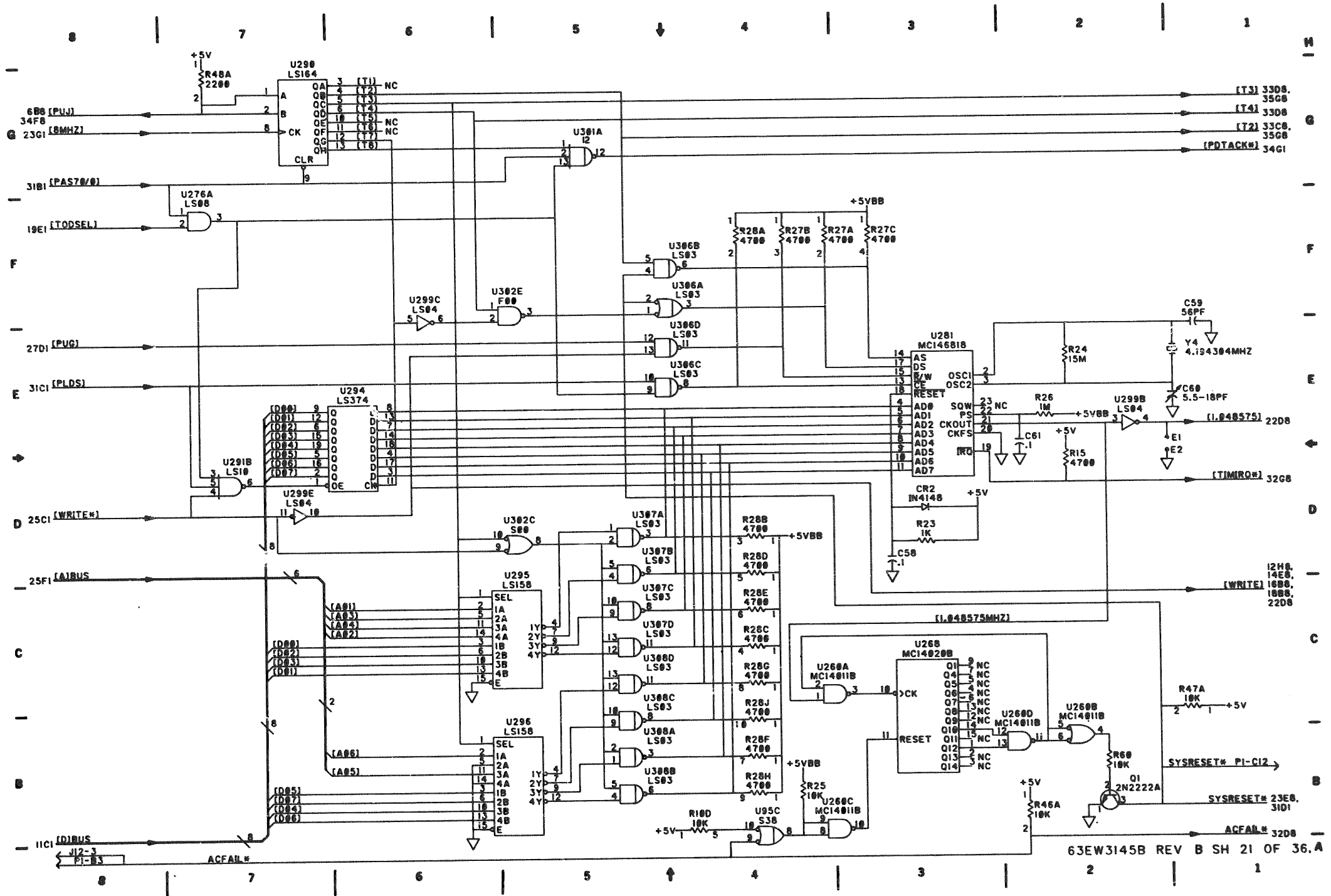


FIGURE 4-3. SCM Schematic Diagram (Sheet 21 of 36) 4-71/4-72

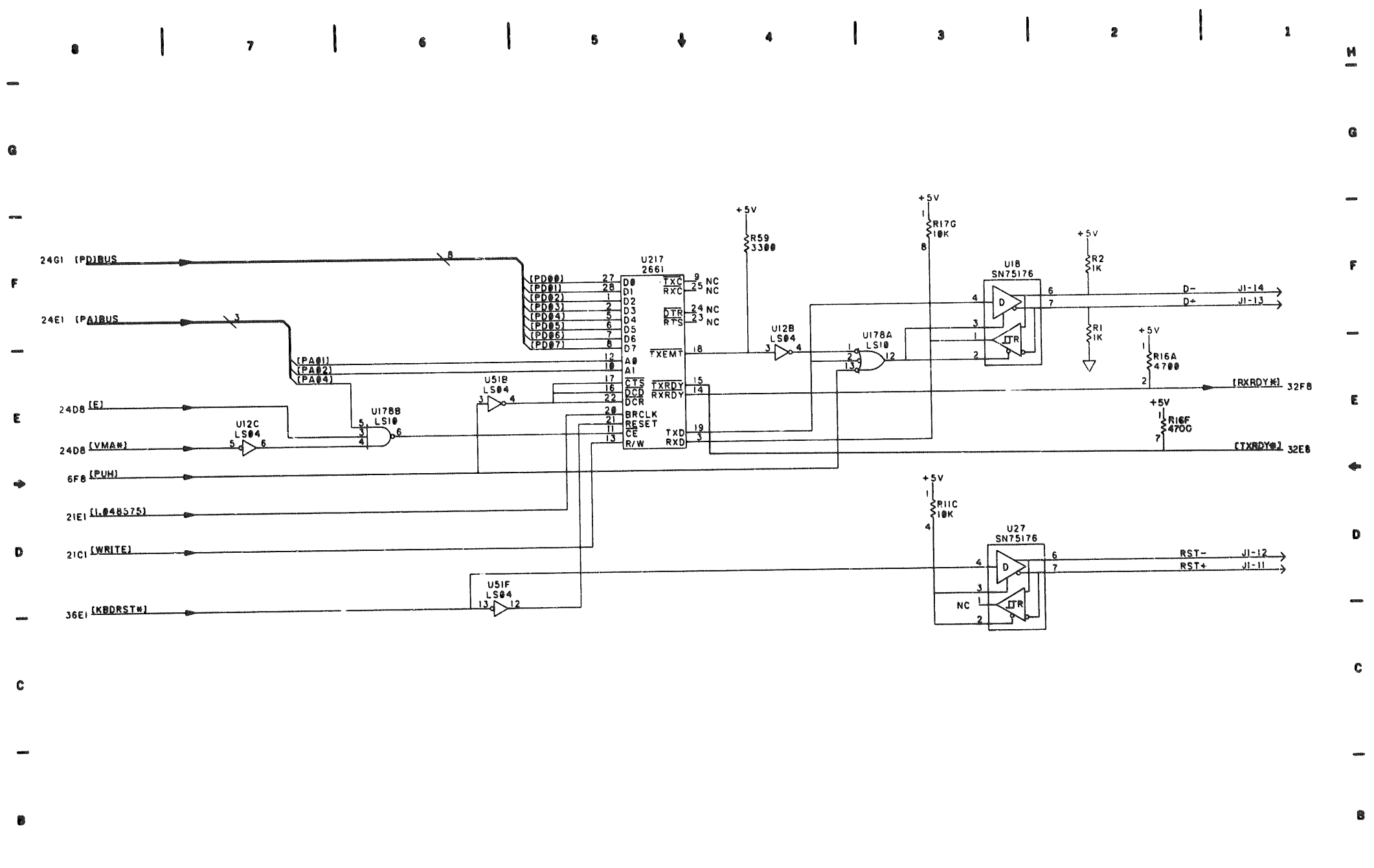
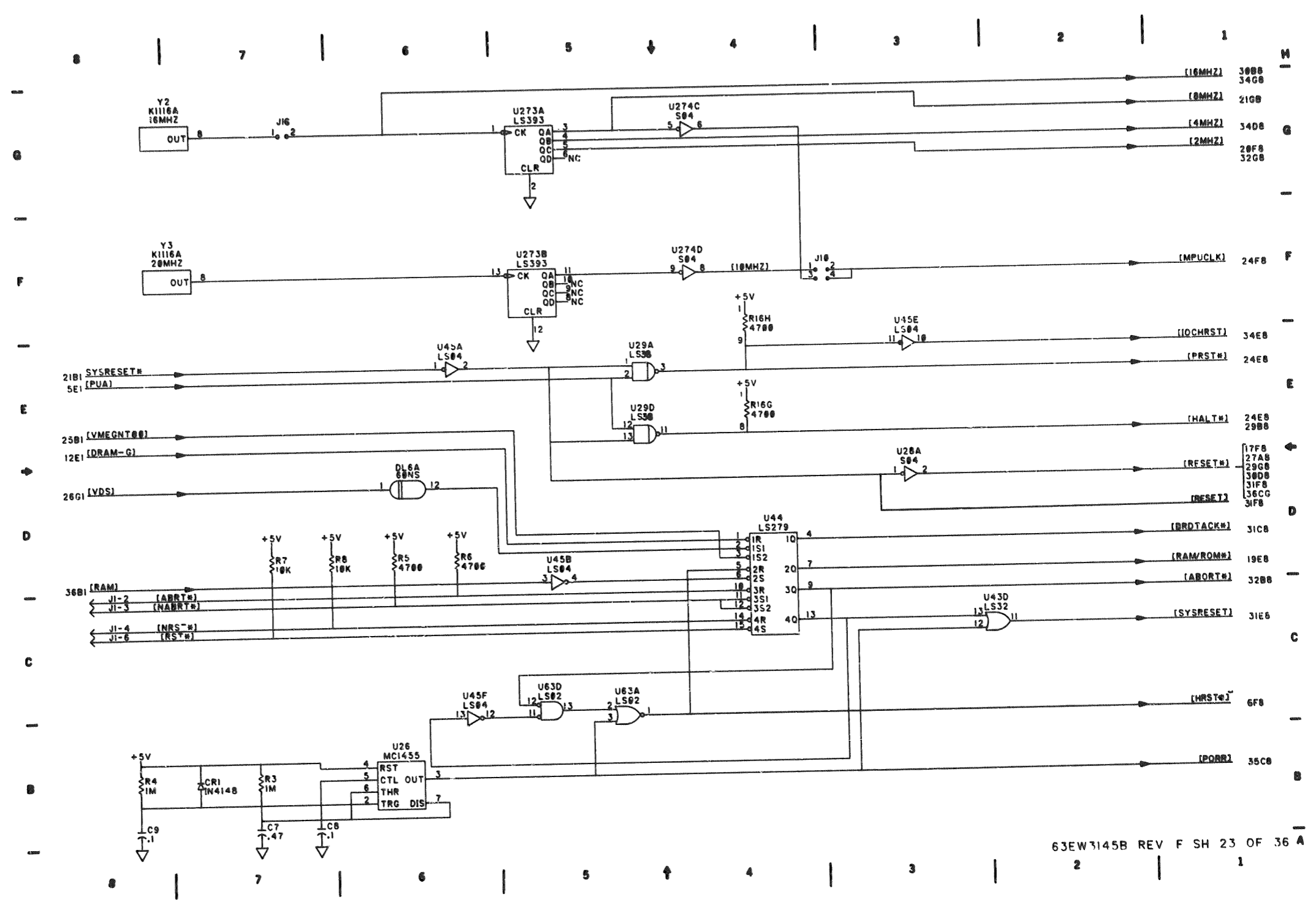


FIGURE 4-3. SCM Schematic Diagram (Sheet 22 of 36)



63EW3145B REV F SH 23 OF 36 A

FIGURE 4-3. SCM Schematic Diagram (Sheet 23 of 36)

4-75/4-76

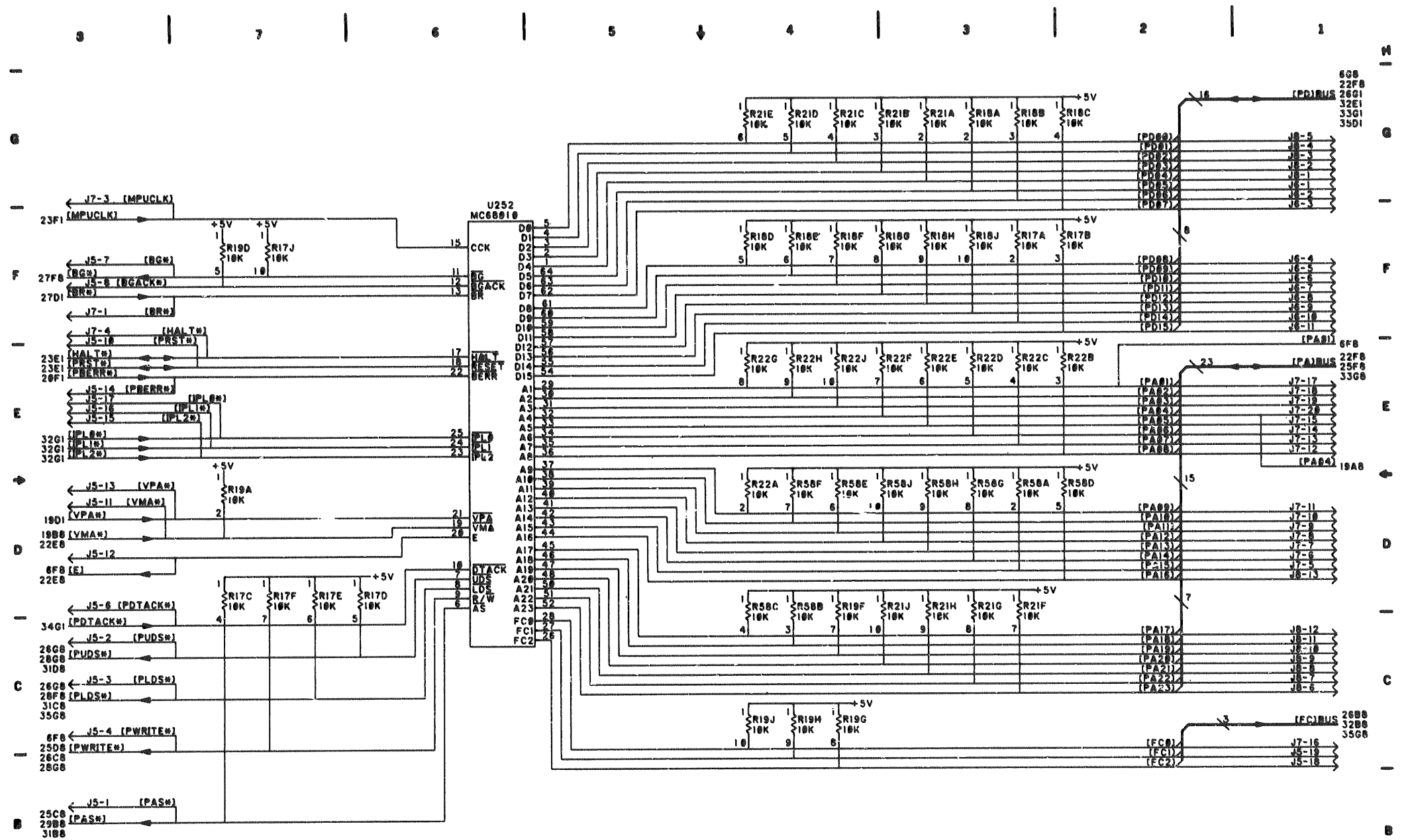
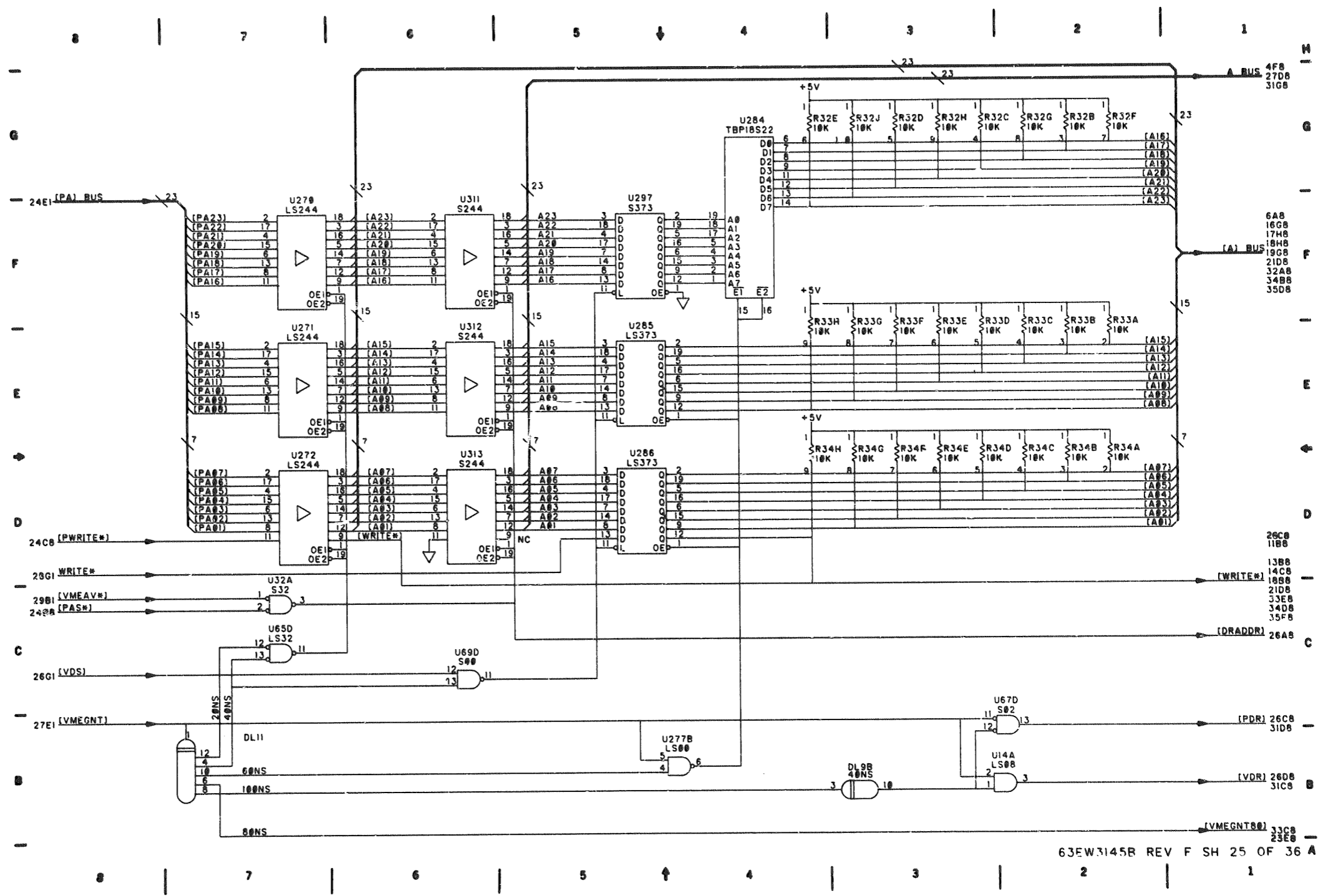


FIGURE 4-3. SCM Schematic Diagram (Sheet 24 of 36) 4-77/4-78



63EW3145B REV F SH 25 OF 36 A

FIGURE 4-3. SOM Schematic Diagram (Sheet 25 of 36) 4-79/4-80

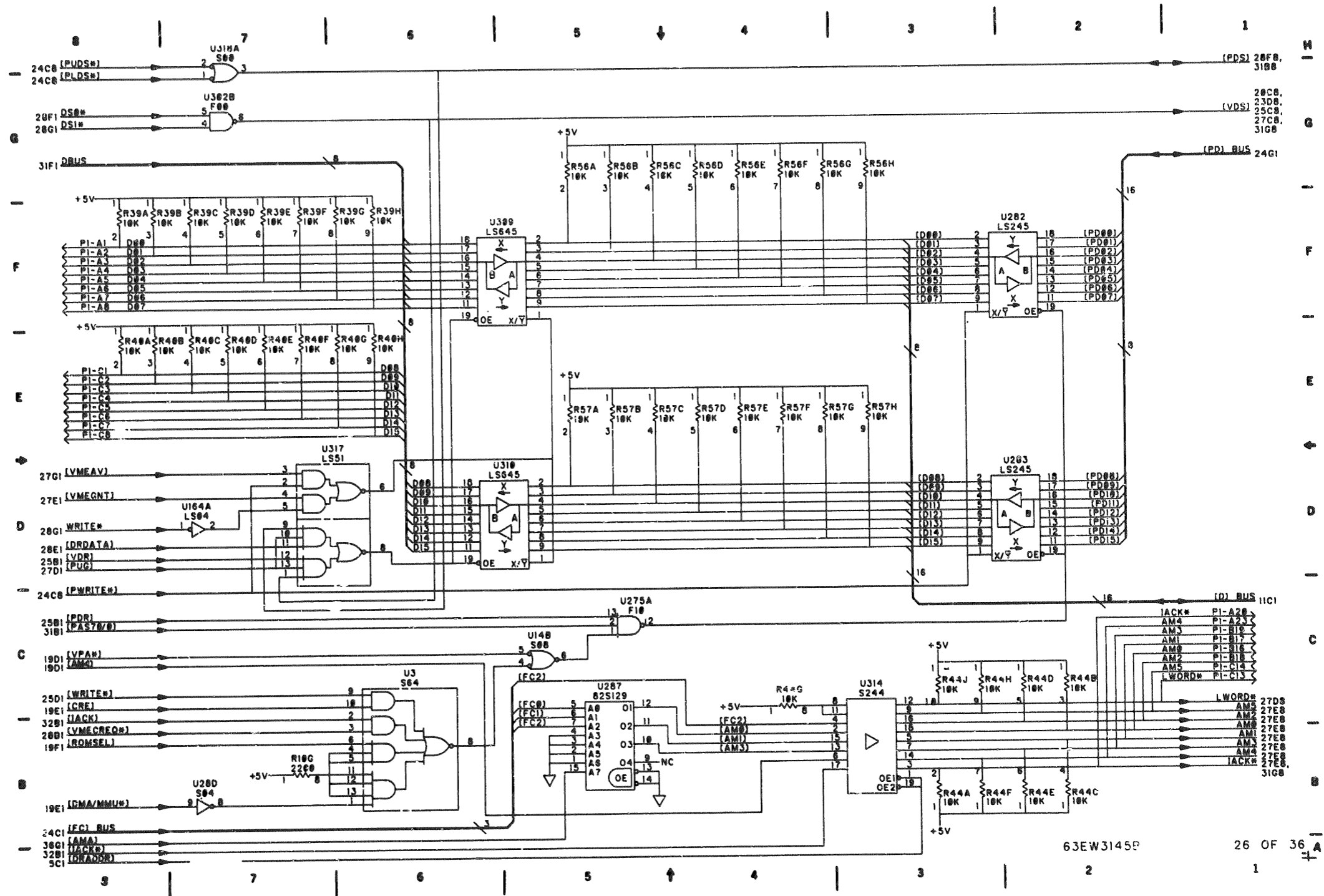
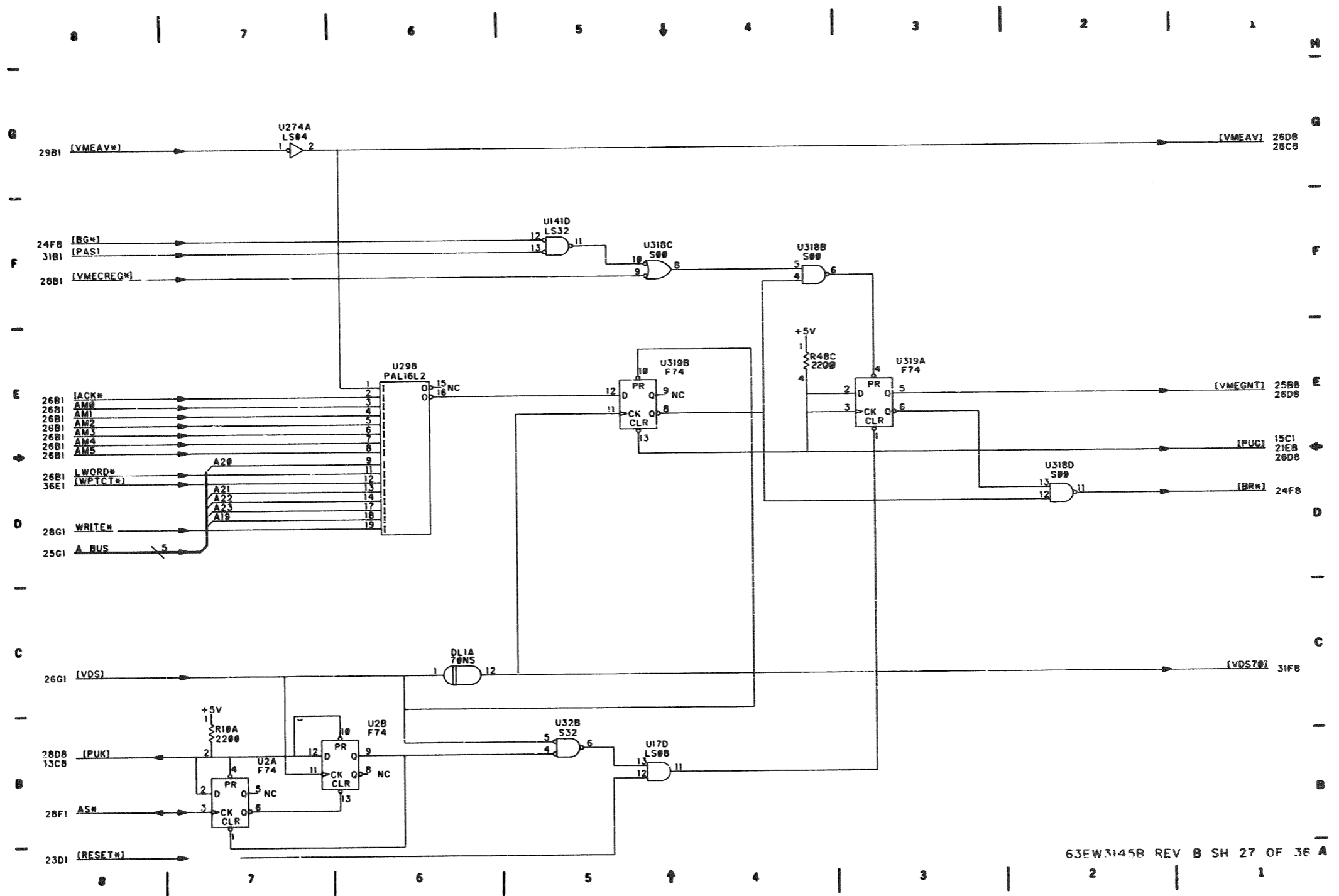
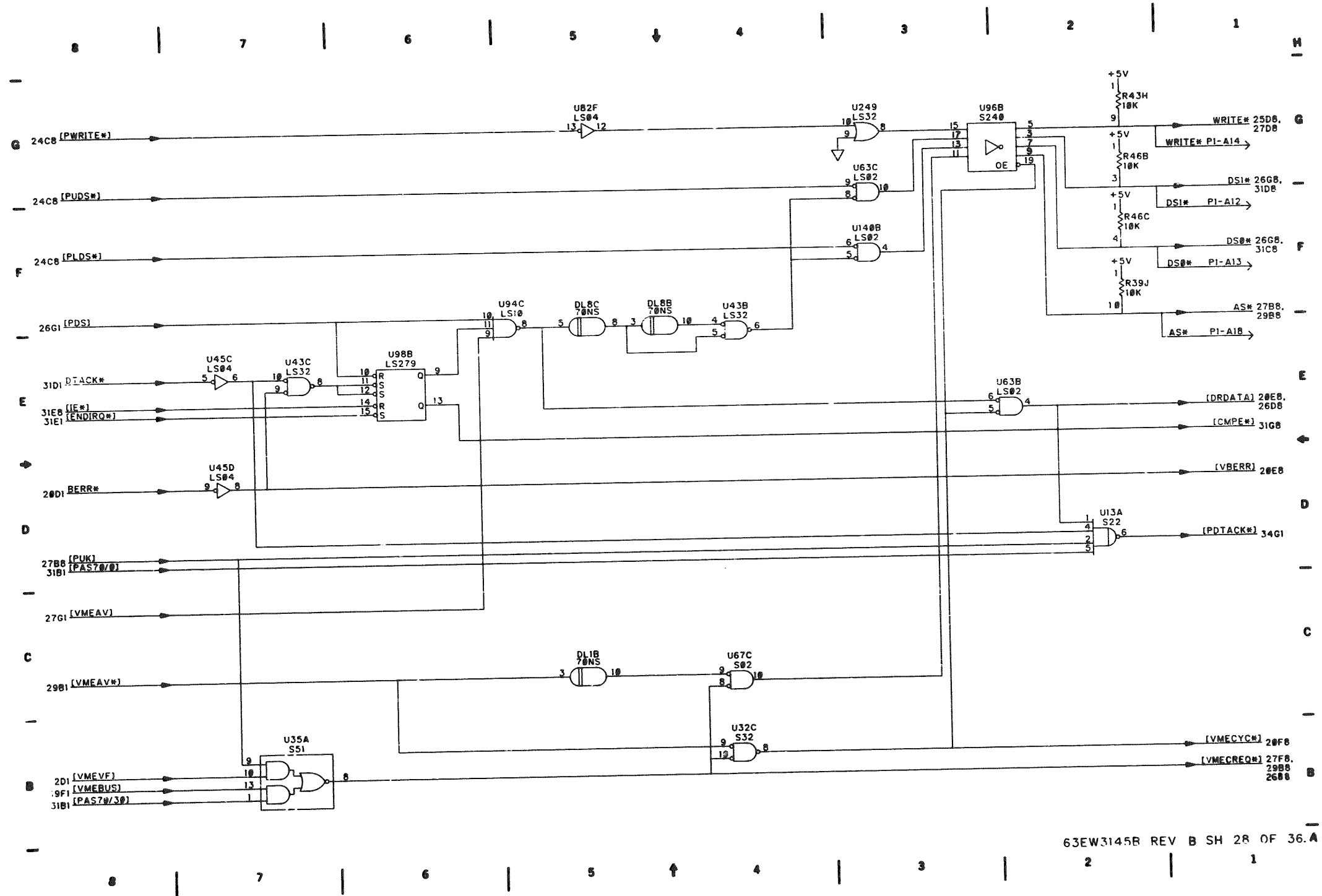


FIGURE 4-3. SOM Schematic Diagram (Sheet 26 of 36)



63EW3145B REV B SH 27 OF 36 A

FIGURE 4-3. SCM Schematic Diagram (Sheet 27 of 36) 4-83/4-84

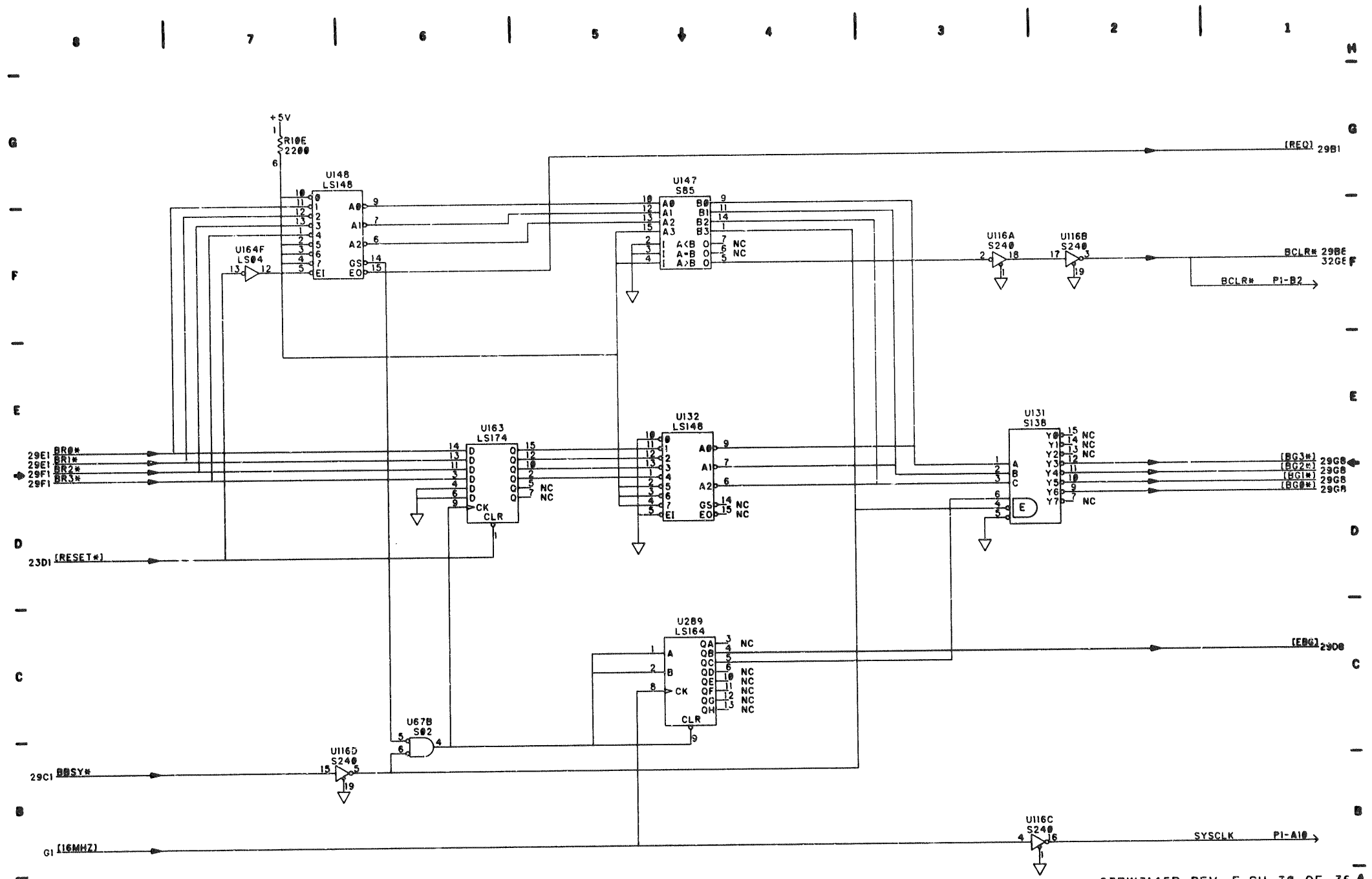


63EW3145R REV B SH 28 OF 36.A

FIGURE 4-3. SCM Schematic Diagram (Sheet 28 of 36)







63EW3145R REV F SH 30 OF 36.A

FIGURE 4-3. SCM Schematic Diagram (Sheet 30 of 36)

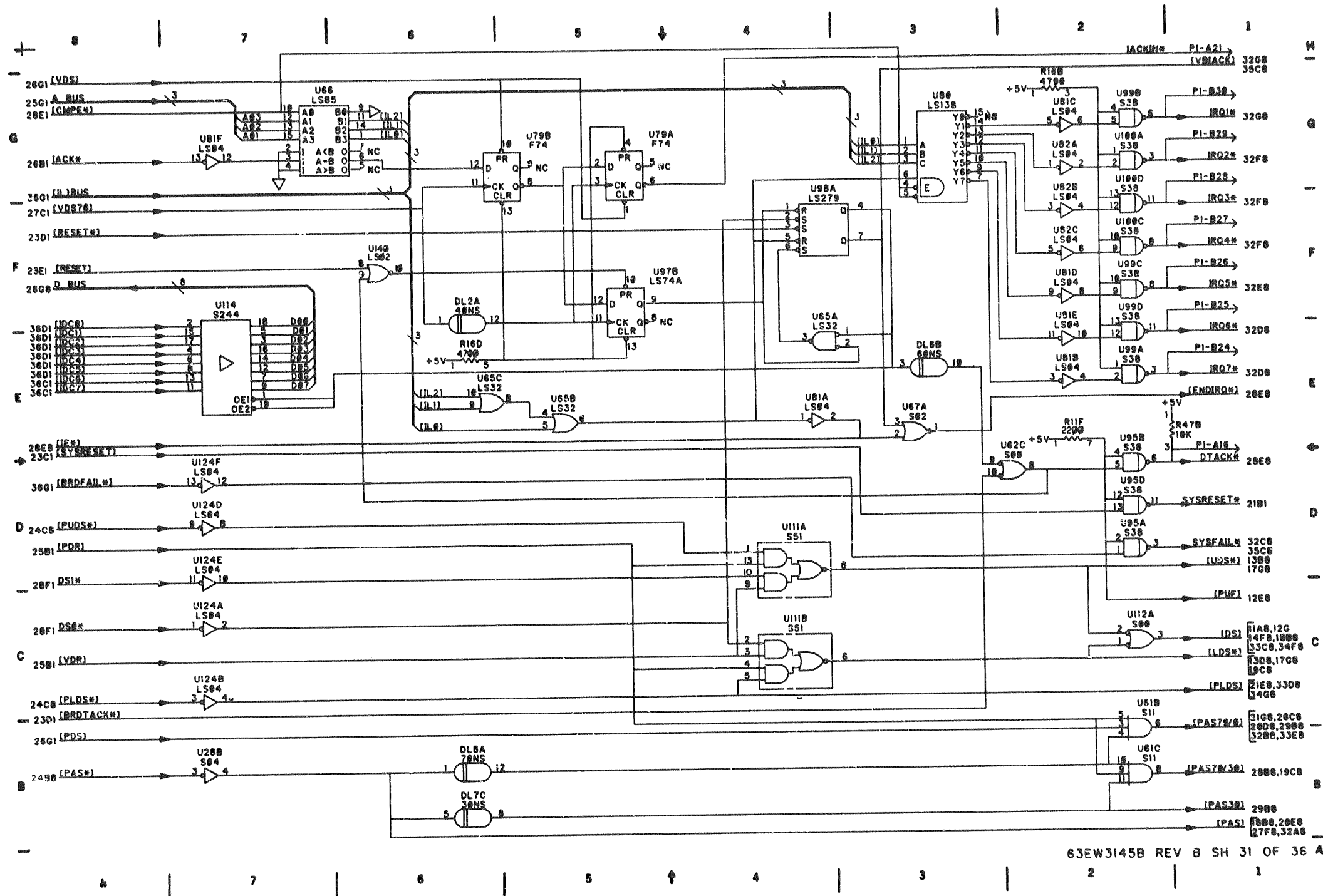


FIGURE 4-3. SCM Schematic Diagram (Sheet 31 of 36)

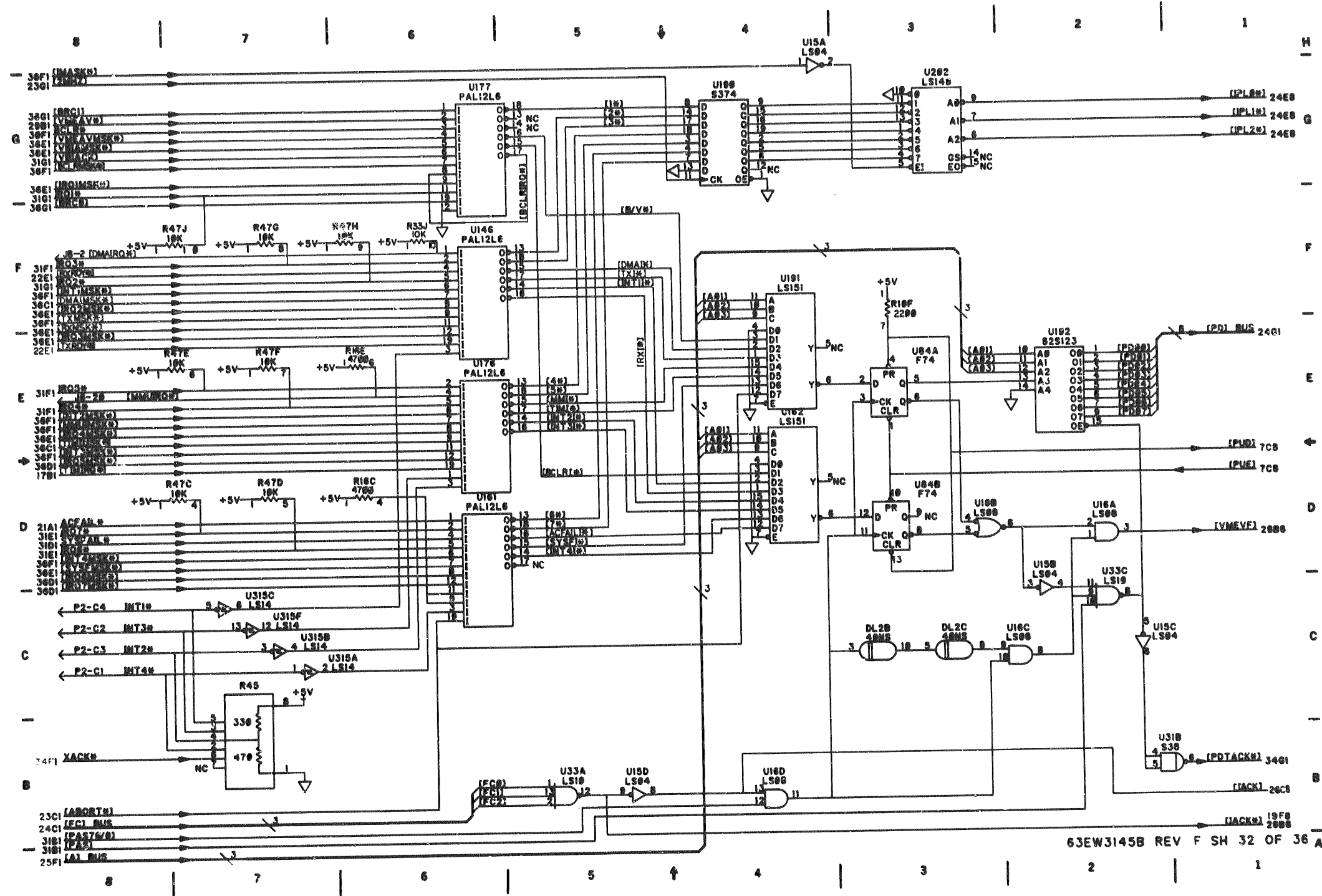


FIGURE 4-3. SCM Schematic Diagram (Sheet 32 of 36) 4-93/4-94

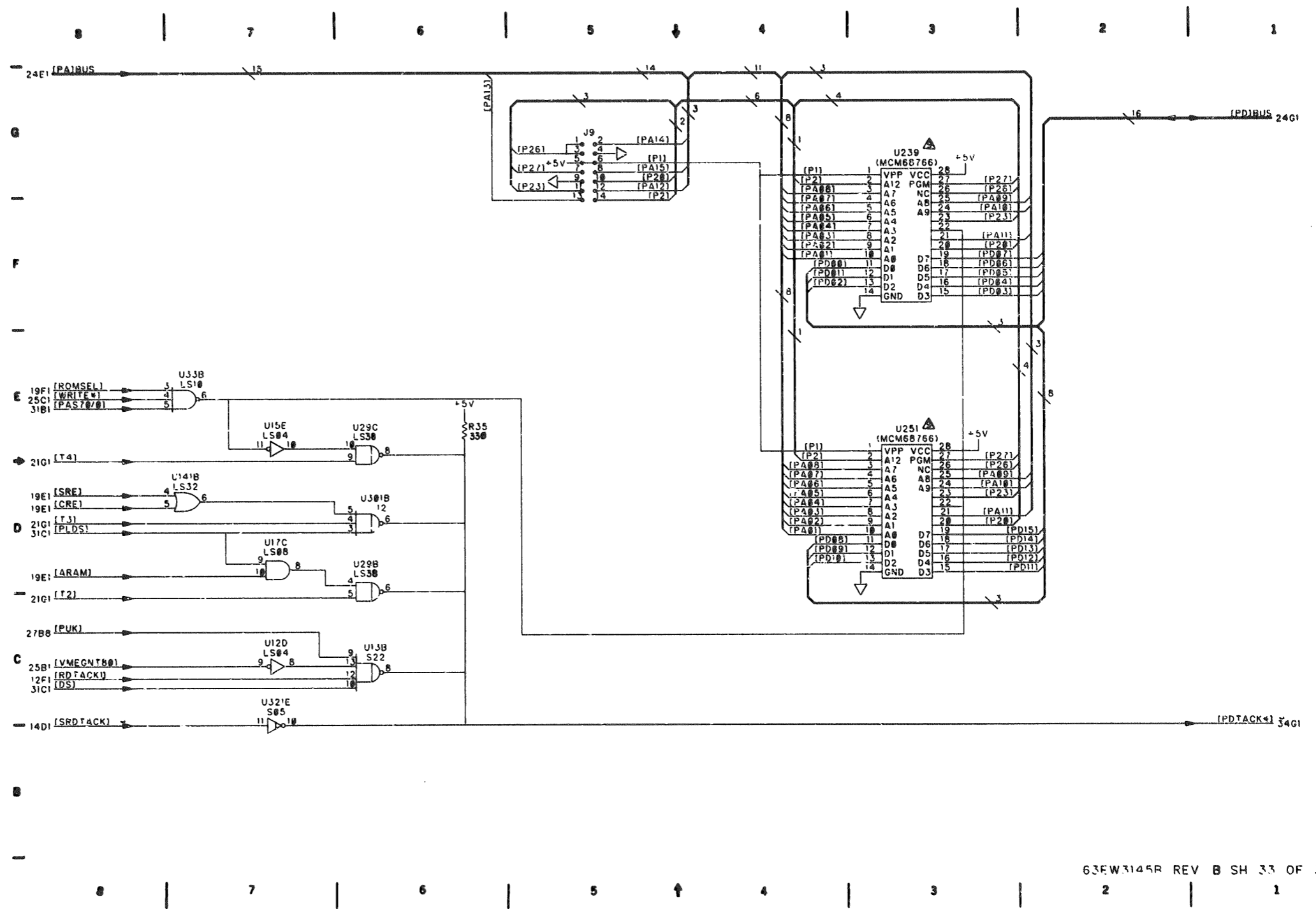


FIGURE 4-3. SCM Schematic Diagram (Sheet 33 of 36)

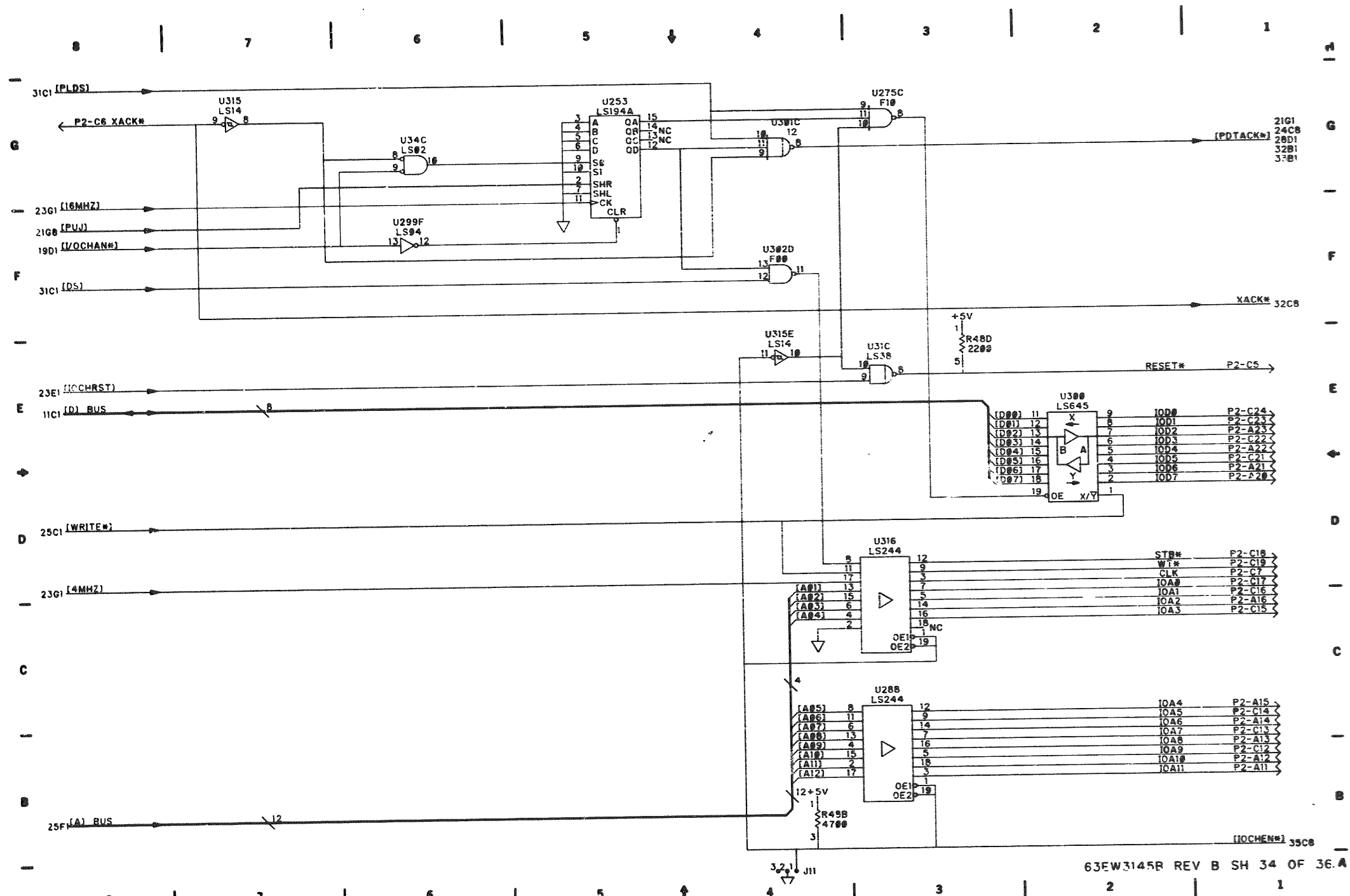
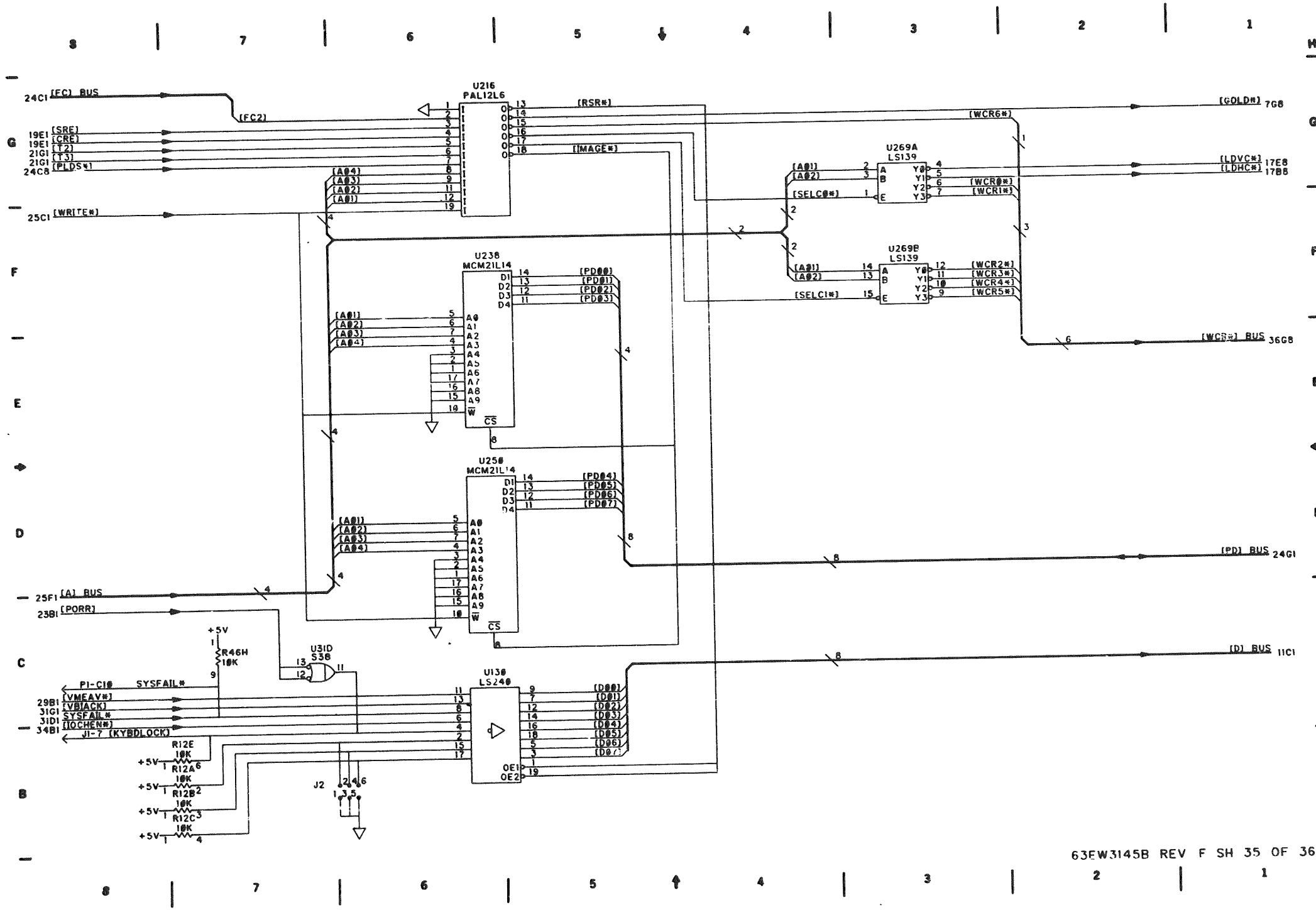


FIGURE 4-3. SCM Schematic Diagram (Sheet 34 of 36) 4-97/4-98



63EW3145B REV F SH 35 OF 36 A

FIGURE 4-3. SCM Schematic Diagram (Sheet 35 of 36)

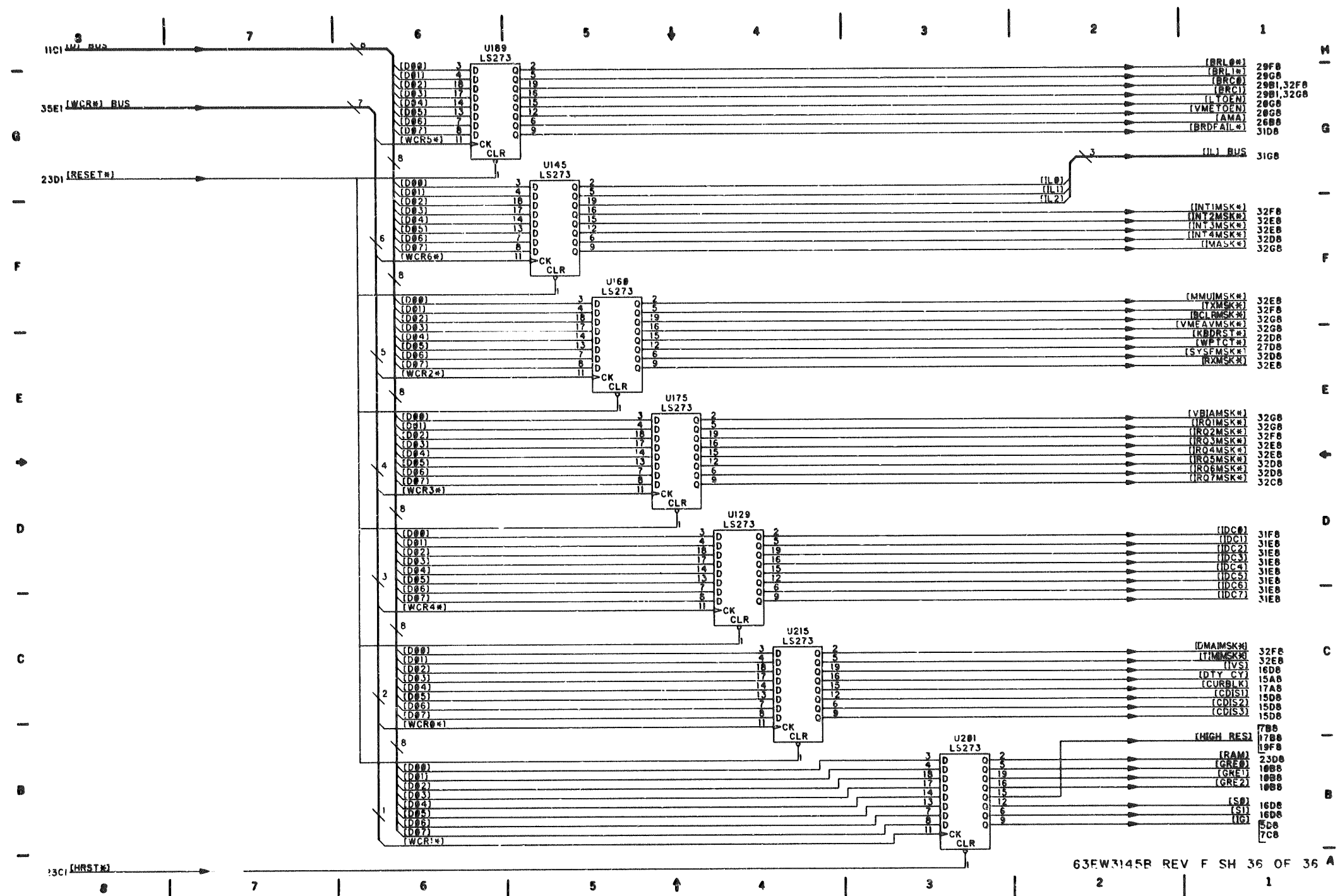


FIGURE 4-3. SCM Schematic Diagram (Sheet 36 of 36) 4-101/4-102

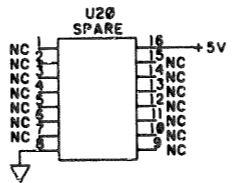
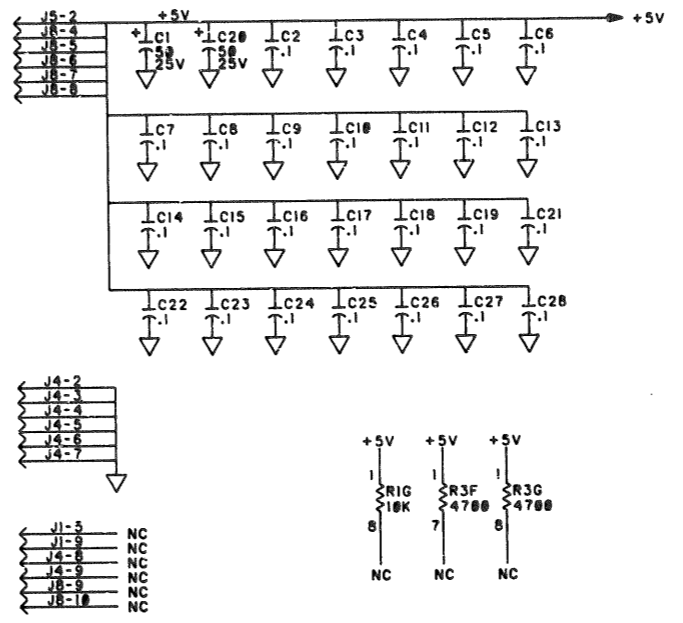


- NOTES:
- FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 61-W3262B01
  - UNLESS OTHERWISE SPECIFIED:  
ALL RESISTORS ARE IN OHMS,  $\pm 5\text{PCT.}$   
1/4 WATT.  
ALL CAPACITORS ARE IN UF.  
ALL VOLTAGES ARE DC.
  - INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
  - DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
  - SPECIAL SYMBOL USAGE:  
\* DENOTES - ACTIVE LOW SIGNAL.
  - INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
  - PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE 1.
  - CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:

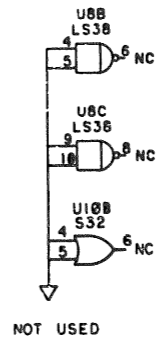
SHEET 8 A6 ZONE

TABLE 1

REF DES	TYPE	GND	+5V
DL1	DELAY	7	14
U1	74LS04	7	14
U2	74S32	7	14
U3	MC68010	53	14
U3	MC68010	16	49
U4	MC68451	41	56
U4	MC68451	8	25
U5	MC68451	41	56
U5	MC68451	0	25
U6	MC68451	41	56
U6	MC68451	8	25
U7	MC68451	41	56
U7	MC68451	8	25
U8	74LS30	7	14
U9	74LS32	7	14
U11	74LS00	7	14
U12	74LS138	8	16
U13	74LS645	10	20
U15	74LS645	10	20
U15	74LS645	10	20
U16	74LS645	10	20
U17	74S373	10	20
U18	74S373	10	20
U19	74S373	10	20

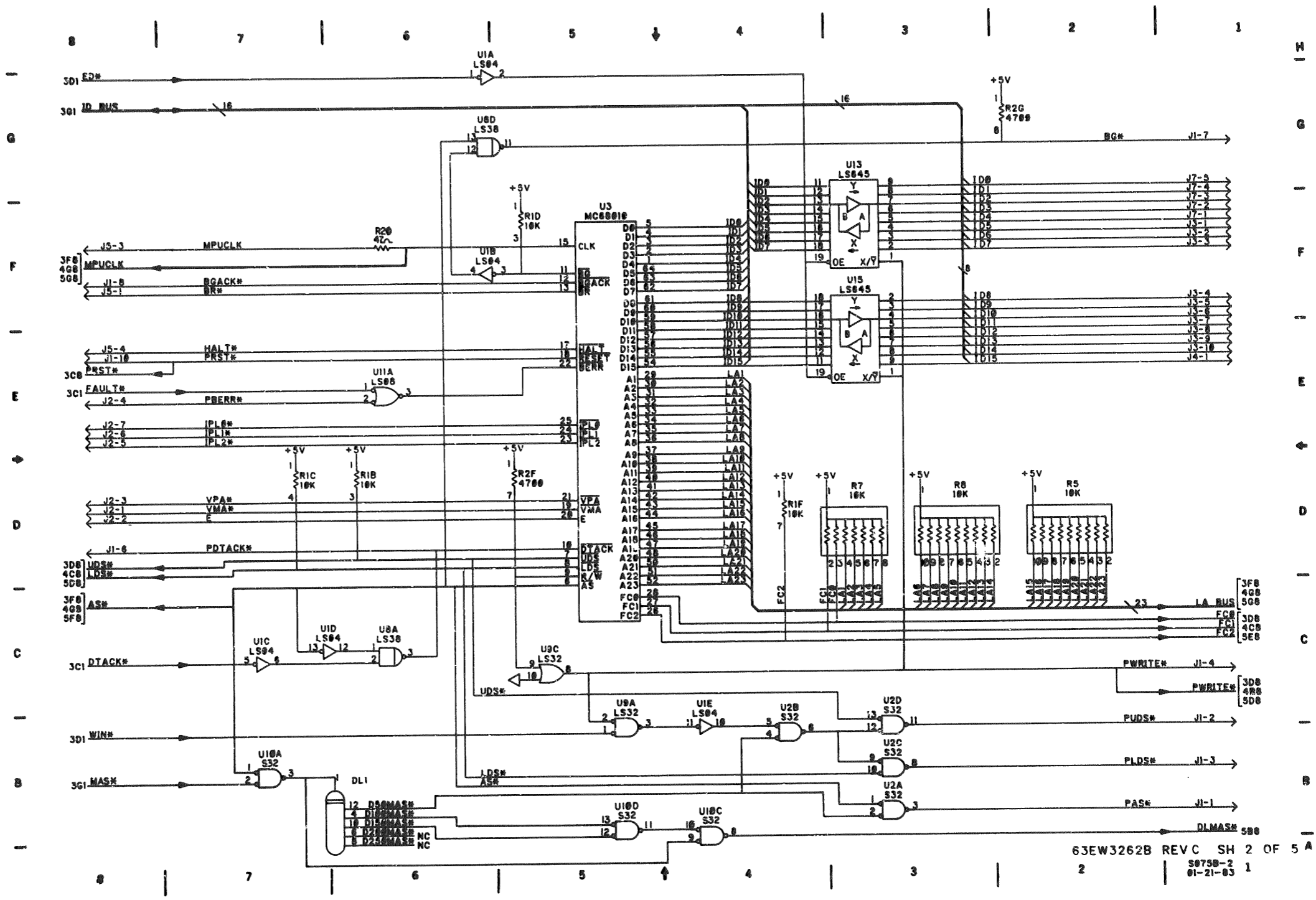


REFERENCE DESIGNATIONS	HIGHEST NUMBER USED
U20	
R20	R1-R9
J8	
DL1	
C27	
HIGHEST NUMBER USED	NOT USED



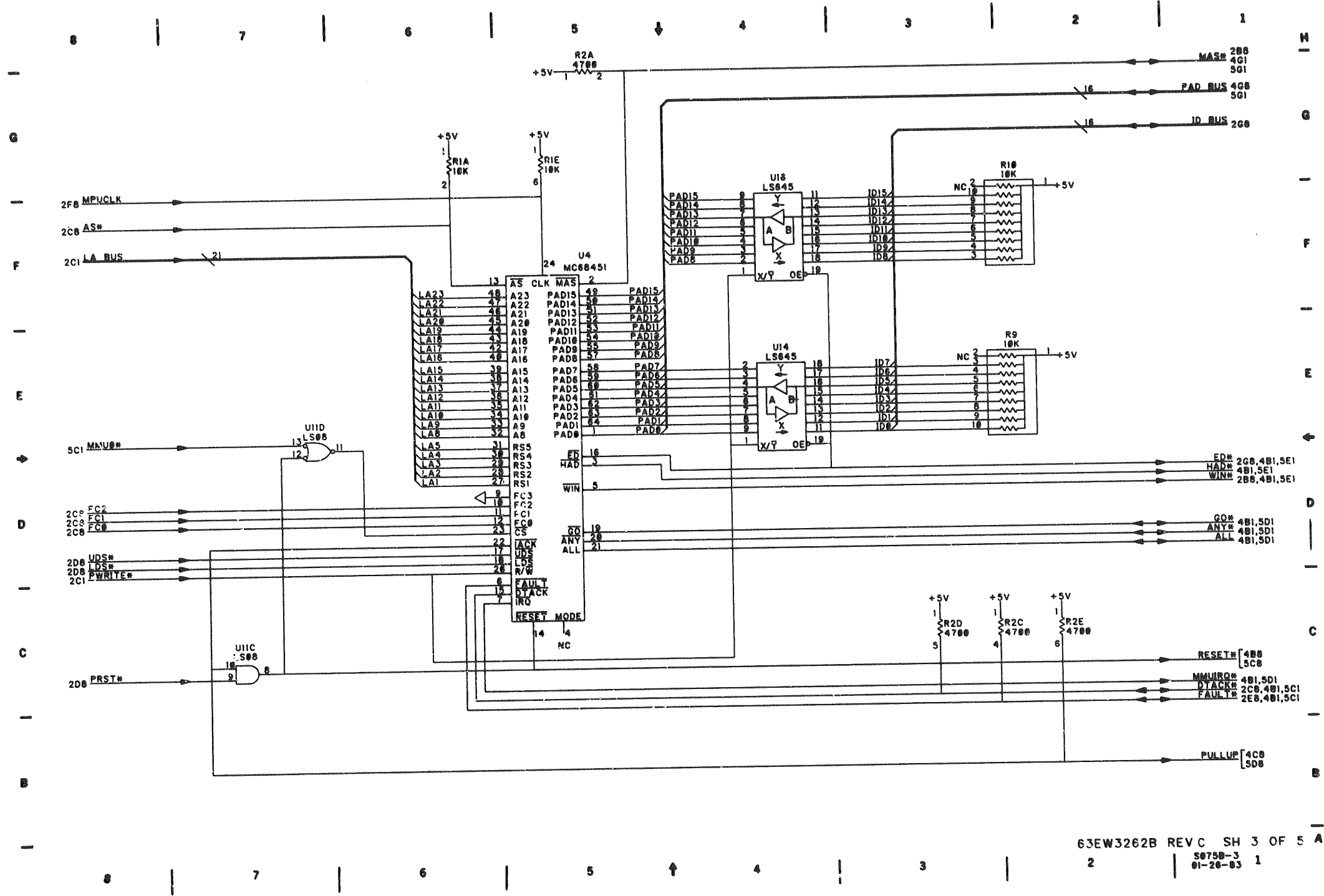
63EW3262B REV C SH 1 OF 5

FIGURE 4-4. Daughter Board Schematic Diagram (Sheet 1 of 5) 4-103/4-104



63EW3262B REV C SH 2 OF 5 A  
 2  
 50758-2  
 01-21-83 1

FIGURE 4-4. Daughter Board Schematic Diagram (Sheet 2 of 5) 4-105/4-106



63EW3262B REV C SH 3 OF 5 A  
 5075B-3  
 01-26-83 1

FIGURE 4-4. Daughter Board Schematic Diagram (Sheet 3 of 5) 4-107/4-108

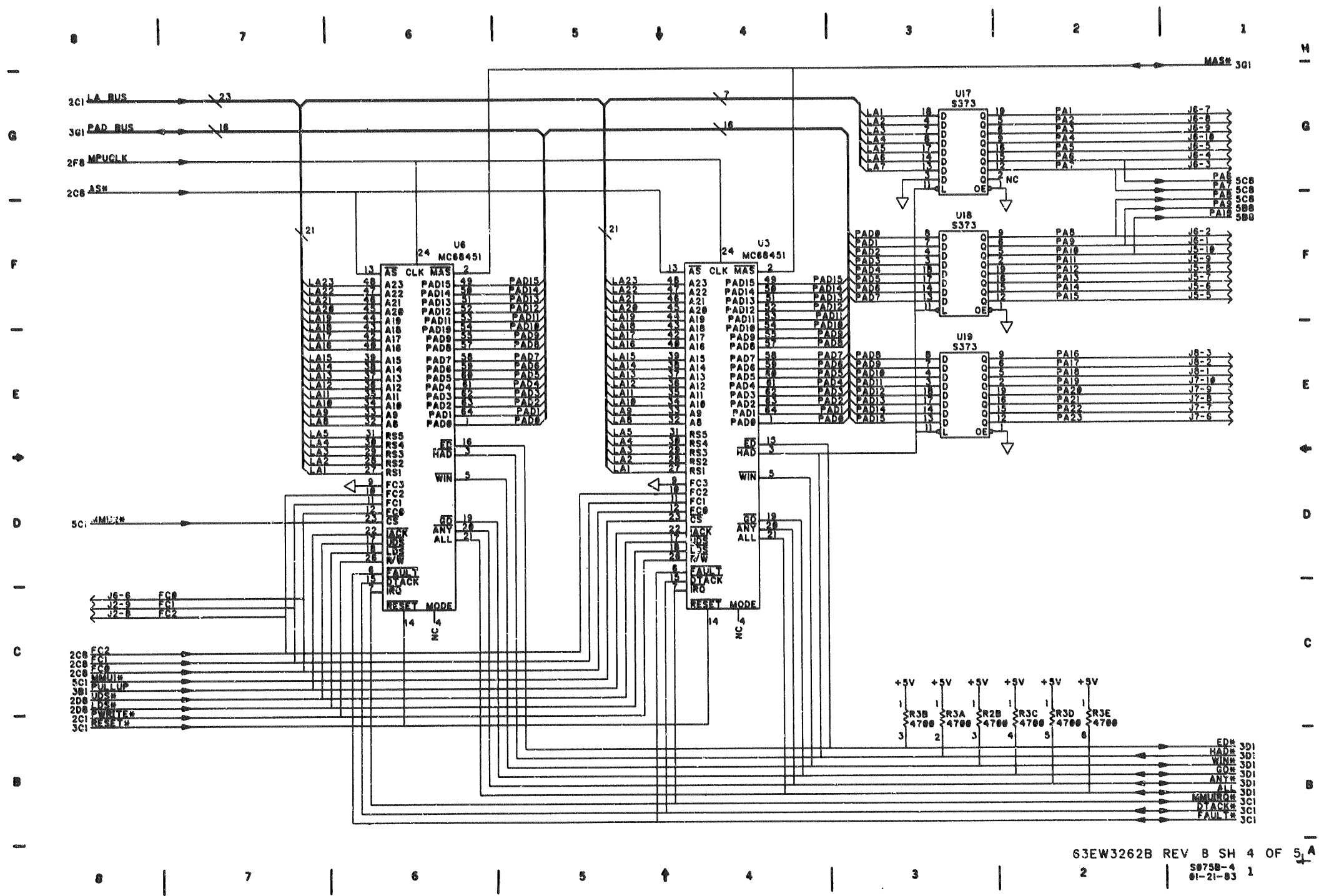
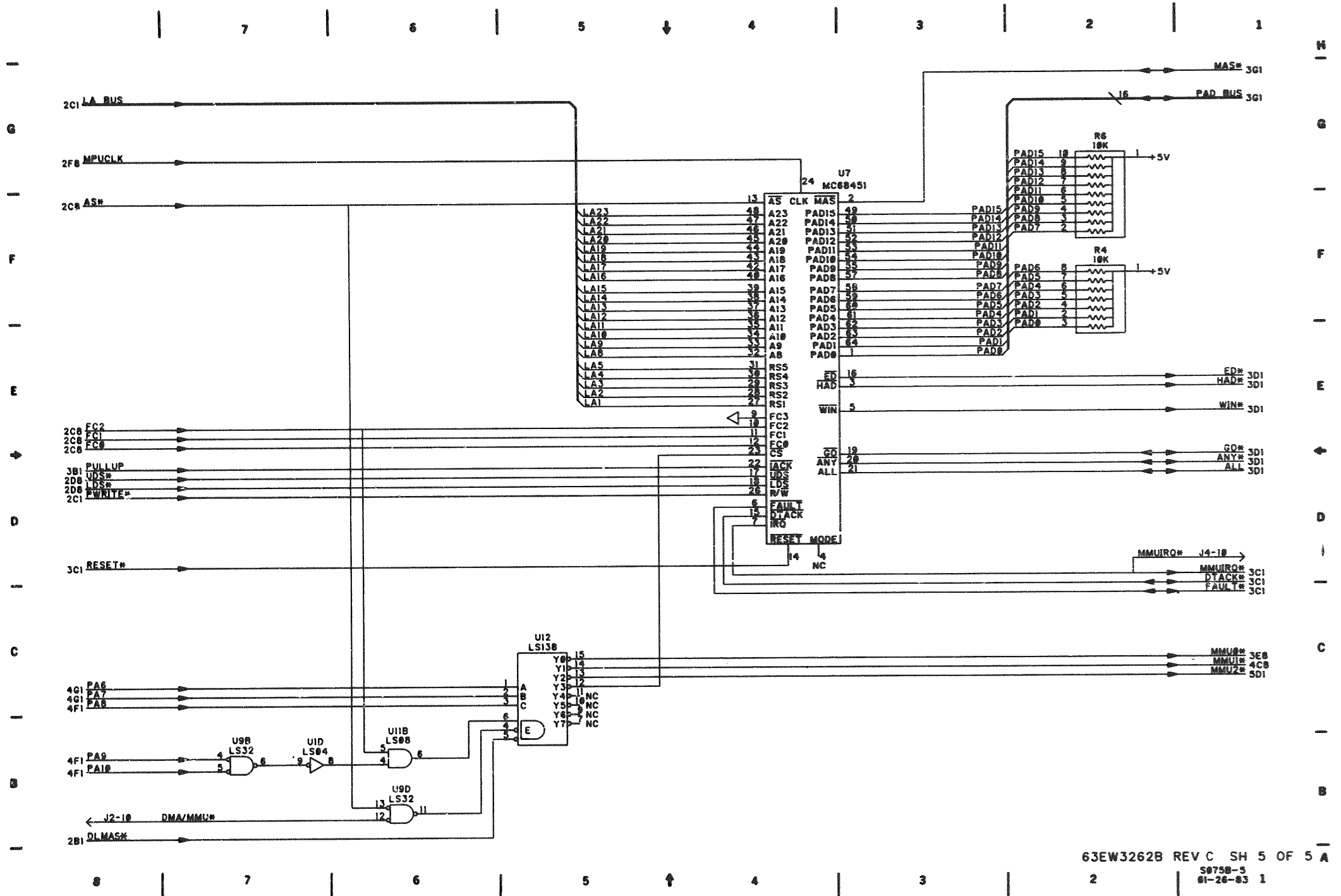


FIGURE 4-4. Daughter Board Schematic Diagram (Sheet 4 of 5) 4-109/4-110

63EW3262B REV B SH 4 OF 5  
 5075B-4  
 01-21-83



63EW3262B REV C SH 5 OF 5 A  
 58758-5  
 81-26-83 1

FIGURE 4-4. Daughter Board Schematic Diagram (Sheet 5 of 5) 4-111/4-112