NX-MLCP™
User's Manual

Preliminary
May 1985

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PERSONAL CAD SYSTEMS INC.

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PERSONAL CAD SYSTEMS

NX-MLCP USER'S MANUAL

PRELIMINARY

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INTRODUCTION

The P-CAD NX-MLCP Motorola(R) IC Interface program translates the netlist for a circuit created with PC-CAPS into a LOGCAP(TM) netlist format that is compatible with Motorola's special CAD systems.

This manual provides an overview of the NX-MLCP program. It describes the program inputs and outputs, explains the format of the LOGCAP netlist output, and provides operating instructions.

Refer to the PC-CAPS or PC-LOGS user manual for concepts not explained in this manual.

OVERVIEW

The input to the NX-MLCP interface program is a PC-NODES binary netlist output or PC-LINK single functional binary netlist output.

The output of the program is a LOGCAP component or cell netlist that describes the logic elements and their interconnections in the given circuit.

The program supports both ECL and CMOS design formats.

COMPONENT SYMBOLS

The NX-MLCP interface package includes special symbols which the designer needs to use to translate his schematic into a LOGCAP format. The special symbols include:

- o PADIN.SYM and PADOUT.SYM for circuit input and output pads
- o WAND2.SYM for a wired-AND with I/O pin or bidirectional pads (ECL format)
- o WOR2.SYM through WOR8.SYM for a wired-OR with from 2 to 8 inputs (ECL format)
- o TRIBUS2.SYM through TRIBUS16.SYM for a tri-state bus structure with from 2 to 16 inputs (CMOS format)

- o WIRED2.SYM through WIRED8.SYM for a wired function with from 2 to 8 inputs (CMOS format).

The NX-MLCP program describes these components in statements on the LOGCAP netlist.

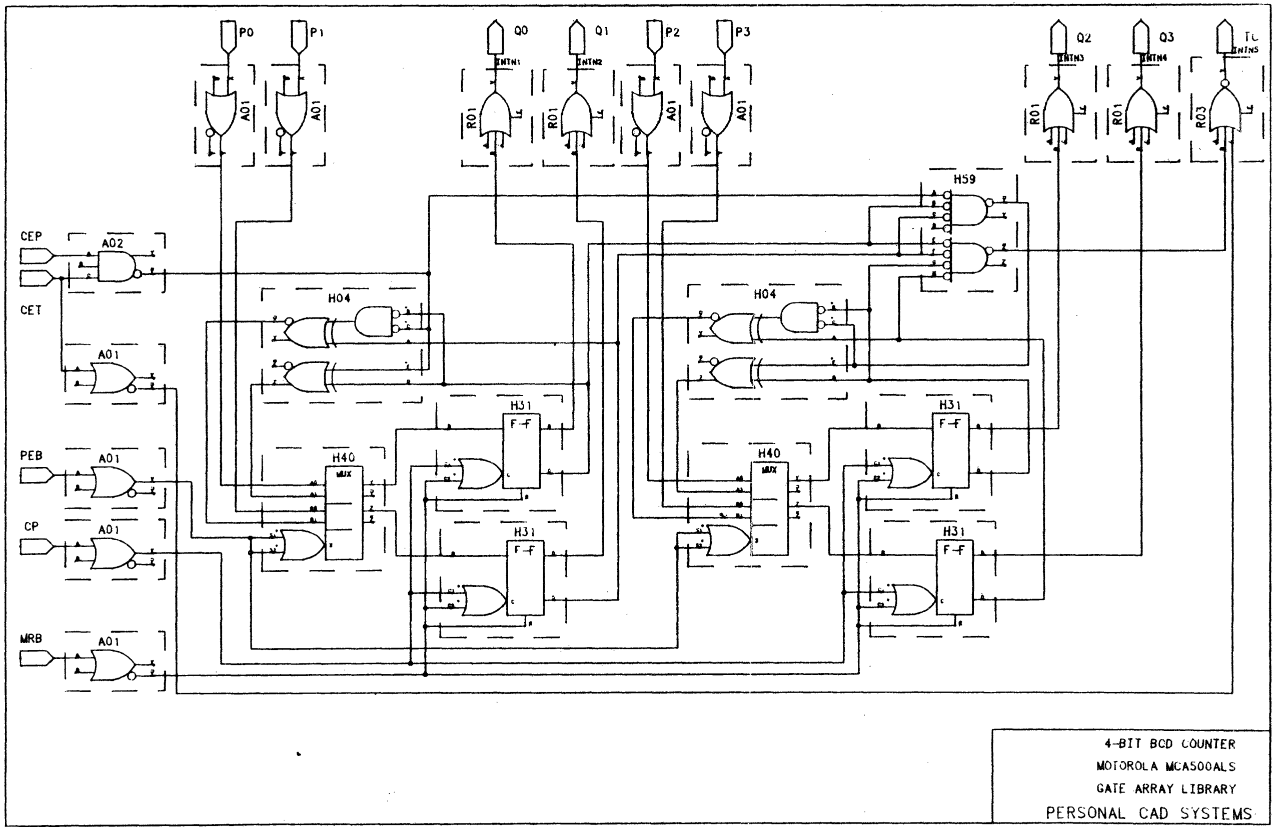
Refer to the appropriate Motorola documentation or consult Motorola technical support personnel for information on the use of these symbols in specific circuit designs.

LOGCAP STATEMENTS

The basic LOGCAP statements are:

- o $NETWORK for network identification
- o $INP and $OUT for circuit inputs and outputs
- o $AND, $OR, $TRIBUS, $WIRED, $SUBU, and $SUBU BOUT for macrocells and interconnects.

These statements are discussed in the following sections of the manual. An example of a schematic and the corresponding LOGCAP netlist output file is shown below.


P0
P1
Q0
Q1
P2
P3
Q2
Q3
TC
CEP
CET
PEB
CP
MRB
A02
A01
R01
R03
H04
H59
H31
H40
MUX
F-F
4-BIT BCD COUNTER
MOTOROLA MCA500ALS
GATE ARRAY LIBRARY
PERSONAL CAD SYSTEMS

```
$$***********************************************************************
$$                                                                      *
$$     Copyright  (C)  1985  -  Personal CAD Systems Inc.               *
$$                                                                      *
$$     Program  :   NX-LCP  VERSION 1.23                                *
$$     Date     :   Mar 07 1985                                         *
$$     Time     :   12:56:33 PM                                         *
$$     File In  :   MCACOUNT.NLT                                        *
$$     File Out :   MCACOUNT.LCP                                        *
$$     Format   :   LOGCAP LIST                                         *
$$                                                                      *
$$***********************************************************************

$NETWORK
$INP MRB CP PEB CEP CET P0 P1 P2 P3
$OUT Q0 Q1 Q2 Q3 TC
$SUBU A02
UN000013 UN0 / &
CEP CON1 CET
$SUBU R01
INTN1 / &
CON0 UN000000 CON0 CON1
$SUBU R01
INTN2 / &
CON0 UN000001 CON0 CON1
$SUBU R01
INTN4 / &
CON0 UN000025 CON0 CON1
$SUBU A01
UN000017 UN1 / &
CET CON0
$SUBU A01
UN2 UN000008 / &
PEB CON0
$SUBU A01
UN3 UN000010 / &
CP CON0
$SUBU A01
UN000011 UN4 / &
MRB CON0
$SUBU A01
UN5 UN000015 / &
P0 CON0
$SUBU A01
UN6 UN000016 / &
P1 CON0
```

```
$SUBU A01
UN7 UN000004 / &
P2 CON0
$SUBU A01
UN8 UN000002 / &
P3 CON0
$SUBU R01
INTN3 / &
CON0 UN000023 CON0 CON1
$SUBU R03
INTN5 / &
CON0 UN000024 UN000017 CON1
$SUBU H04
UN000014 UN9 UN000012 UN10 / &
UN000026 UN000013 UN000006 UN000026 UN000013
$SUBU H04
UN000005 UN11 UN000003 UN12 / &
UN000021 UN000020 UN000022 UN000021 UN000020
$SUBU H40
UN000009 UN13 UN14 UN000007 / &
UN000008 UN000008 UN000015 UN000012 UN000016 UN000014
$SUBU H40
UN000019 UN15 UN16 UN000018 / &
UN000008 UN000008 UN000004 UN000003 UN000002 UN000005
$SUBU H31
UN000000 UN000026 / &
UN000010 UN000011 UN000009 UN000011
$SUBU H31
UN000023 UN000021 / &
UN000010 UN000011 UN000019 UN000011
$SUBU H31
UN000025 UN000022 / &
UN000010 UN000011 UN000018 UN000011
$SUBU H31
UN000001 UN000006 / &
UN000010 UN000011 UN000007 UN000011
$SUBU H59
UN000020 UN17 UN18 UN000024 / &
UN000013 UN000026 UN000006 CON0 UN000026 UN000006 UN000021 UN000022
$SUBU BOUT
Q0 / &
INTN1
$SUBU BOUT
Q1 / &
INTN2
$SUBU BOUT
Q2 / &
INTN3
$SUBU BOUT
Q3 / &
INTN4
$SUBU BOUT
TC / &
INTN5
```

LOGCAP NETLIST FORMAT

Refer to the sample LOGCAP netlist for examples of the following statements.

NETWORK STATEMENT

$NETWORK is the first line in the LOGCAP netlist output. It denotes the type of file used to generate the LOGCAP netlist.

CIRCUIT INPUTS AND OUTPUTS

The program uses the PADIN.SYM and PADOUT.SYM components for the inputs and outputs of the circuit being modeled. Each of these components has input and output pins.

$INP Statement

A net connected to an output pin of a PADIN.SYM component is listed in the LOGCAP $INP statement as an input signal. This signal can be viewed as the input signal to the circuit from an external source.

The format of the $INP statement is:

```
$INP INPNNAM1 INPNNAM2 INPNNAM3
```

$OUT Statement

If the circuit is in ECL format, a net connected to the output pin of a PADOUT.SYM component is listed in the $OUT statement as an output signal. If the circuit is in CMOS format, a net connected to an input pin of a PADOUT.SYM component is listed as an output signal.

The LOGCAP output signal can be viewed as the output signal to the external environment.

The format of the $OUT statement is:

```
$OUT OUTNNAM1 OUTNNAM2 OUTNNAM3
```

MACROCELLS AND INTERCONNECTS

Macrocells and interconnects are modeled by $AND, $OR, $TRIBUS, $WIRED, and $SUBU statements in the LOGCAP netlist.

$AND Statement

The program prints an $AND statement for each WAND2.SYM component in the circuit. This symbol is only used in an ECL circuit to denote a Wired-AND component with an I/O pin or bidirectional pad with two inputs and one output.

The $AND statement lists the names of the nets tied to the input and output pins of the WAND2.SYM component and shows the number of inputs. The format of an $AND statement is:

```
$AND 0 0
OUTNNAME 2 INPNNAME INPNNAME
```

For example:

```
$AND 0 0
WIBIDIR1 2 BIDIR1I BIDIR1
```

$OR Statement

The program prints an $OR statement for each WOR.SYM component (Wired-OR) in the ECL circuit. The $OR statement lists the names of the nets tied to the input and output pins of the WOR.SYM component and shows the number of inputs. A WOR.SYM component has one output and from two to eight inputs.

The format of an $OR statement is:

```
$OR 0 0
OUTNNAME 2 INPNNAM1 INPNNAM2 ...
```

$TRIBUS Statement

A $TRIBUS statement is printed for each TRIBUS.SYM component (tri-state bus structure) in the CMOS circuit. This statement lists the names of the nets tied to the input and output pins of the TRIBUS.SYM component and shows the number of inputs.

A TRIBUS.SYM component has one output and from 2 to 16 inputs.

The format of a $TRIBUS statement is:

```
$TRIBUS 0 0
OUTNNAME 2 INPNNAM1 INPNNAM2 ...
```

$WIRED Statement

For each WIRED.SYM function in the CMOS circuit, the program prints a $WIRED statement. This statement lists the names of the nets connected to the input and output pins of the WIRED.SYM function and gives the number of inputs. A WIRED.SYM has one output and from two to eight inputs. The format of a $WIRED statement is:

```
$WIRED 0 0
OUTNAME 2 INPNNAM1 INPNNAM2 ...
```

$SUBU Statement

$SUBU statements give the definition names of the components (cells) in the circuit and the names of the nets tied to the component input and output pins.

The format of a $SUBU statement is:

```
$SUBU COMPDEFNAME
OUTNNAM1 OUTNNAM2 OUTNNAM3 / &
INPNNAM1 INPNNAM2 INPNNAM3
```

The nets tied to the output pins are listed first. A slash (/) separates the outputs from the inputs. An "&" indicates that the list is continued on the following line.

The symbol printed for an unused pin depends on the user's selection of ECL or CMOS cell type at the start of the program (see <u>OPERATION</u> in this manual).

If ECL cell type is selected, the program lists an unused output pin as "UN0", "UN1", etc. It lists an unused input pin as "CON0", with the following exceptions:

- o The program prints "CON1" if the component with the unused input pin has an attribute of FTYPE="INP".
- o The program prints "CON1" if the component has an attribute of FTYPE="OUT" and the unused pin is an enable pin named "E".

The following is an example of a $SUBU statement in a LOGCAP netlist:

```
$SUBU A02
UN000013 UNO / &
CEP CON1 CET
```

If CMOS cell type is selected, the program prints a "*" for each unused input and output pin.

$SUBU BOUT Statement

If the user's circuit is in ECL format, the program prints a $SUBU BOUT statement for each output signal listed in the LOGCAP $OUT statement. A $SUBU BOUT statement models the input and output signals of the PADOUT.SYM components.

The format of the $SUBU BOUT statement is:

```
$SUBU BOUT
OUTNNAME / INNNAME
```

DESIGNER NOTES

The NX-MLCP program allows the designer to use alternate symbols for components (cells) in an ECL circuit. Attributes of the form ALT = <filename> have been preassigned to the appropriate symbols, for example, M50 and M50A.

The P-CAD symbol libraries provided for CMOS designs allow the designer to group partial functions into a single cell. The attributes and grouping information are included in the component symbols. Use the PC-CAPS SCMD/PNUM command to assign reference designators and sections to the functions. See the PC-CAPS User's Manual for instructions.

OPERATION

To start the NX-MLCP program, type

NXMLCP

The program clears the screen and prompts for the name of the netlist input:

Net-List Filename :<Filename>.NLT

Enter the netlist filename and press [Return].

The program responds with the LOGCAP output filename:

<Filename>.LCP

Press [Return] to accept the output filename. The program will then prompt for the cell type:

Cell Type: ECL

Press [Return] to accept ECL, or use the space bar to select CMOS and press [Return].

After the cell type is entered, the program sets up the netlist database environment and generates the LOGCAP netlist output.

Program messages and errors are reported on the lower section of the screen. Use the escape key [ESC] to cancel the input or to exit from the program.