FAIRCHILD® F100K ECL COMPONENTS LIBRARY

Packaged Parts

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TRADEMARK

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OVERVIEW

The P-CAD/Fairchild® F100K ECL Packaged Parts Library consists of this manual and the Fairchild F100K ECL Packaged Parts diskette. The library has been developed jointly with Fairchild at the request of our users, and we welcome any suggestions for improvements or additions.

The library diskette contains the following files for use with the PC-CARDS printed circuit board (PCB) layout program:

- Component files
- Layer structure file, LAYS.PCB
- Standard-size drawing sheet files, ASIZE.PCB through ESIZE.PCB
- F100K.FIL and F100K.LIB files

  F100K.FIL is a sample text file used as input into PREPACK to create the binary file F100K.LIB that contains packaging information for PC-PACK. Both F100K.FIL and F100K.LIB contain all the components in the Fairchild F100K ECL Library. Normal usage is to extract only those components used in a design and put them in a new .FIL file for input to PREPACK.

- Padstack and special symbol files (<filename>.PS and <filename>.SSF)

  The padstacks and special symbol files are samples of what can be used in the PC-CARDS environment. Refer to the *PC-CARDS User's Manual* and the Padstacks section of this manual for more information on how to use padstacks and special symbol files.

FILE MANAGEMENT

The complete Fairchild F100K ECL Parts Library includes more than 250 KB of files. If you are loading the library onto the hard disk of your stand-alone computer, you should omit any of the components that you will not need in order to conserve disk space. This is especially important if you are using a 10 MB hard disk.

If your hard disk space is very limited, you can remove individual unneeded parts from the library. Each part is contained in a separate DOS file, and individual parts can be erased using the DOS erase command. Refer to your IBM DOS manual or the "DOS Reference" chapter in your *PC-CAPS* or *PC-CARDS User's Manuals* for instructions on listing and erasing files.

P-CAD recommends a specific directory structure for efficient system operation. Your library parts are normally placed in a specific subdirectory to make it easy to manage these files. The directory structure is described in your P-CAD *Installation Guide.*

CREATING A DESIGN

To use the library in a design, run PC-CARDS. Instructions are given in the "Using PC-CARDS" chapter of your *PC-CARDS User's Manual.* When the menu appears, select FILE/LOAD and load the layer structure. You can load LAYS.PCB or one of the standard-size drawing sheet files, ASIZE.PCB through ESIZE.PCB.

Layer Structure

One layer structure file, LAYS.PCB, is included with this library.

LAYS.PCB, shown in Table 1, is a standard P-CAD layer structure and is recommended when creating schematics.

Table 1. LAYS.PCB Layer Structure

Layer	Name	Pen	Status	Use
1	PADCOM	4	ON	Graphic component pads
2	FLCOMP	4	OFF	Flash component pads
3	PADSLD	8	OFF	Graphic solder pads
4	FLSOLD	8	OFF	Flash solder pads
5	PADINT	9	OFF	Graphic internal pads
6	FLINT	9	OFF	Flash internal pads
7	GNDCON	10	OFF	Graphic internal ground connections

Table 1 Continued

Layer	Name	Pen	Status	Use
8	FLGCON	10	OFF	Flash internal ground connections
9	CLEAR	7	OFF	Graphic universal clearance
10	FLCLER	7	OFF	Flash universal clearance
11	PWRCON	13	OFF	Graphic internal power connections
12	FLPCON	13	OFF	Flash internal power connections
13	SLDMSK	14	OFF	Graphic solder mask relief
14	FLSMSK	14	OFF	Flash solder mask
15	DRILL	15	OFF	Graphic drill template
16	FLDRLL	15	OFF	Flash drill template
17	PIN	4	ON	Graphic pin connections
18	BRDOUT	12	ON	Board outline
19	FLTARG	11	OFF	Flash alignment targets
20	SLKSCR	6	ON	Silkscreen paint
21	DEVICE	5	ON	Device names
22	ATTR	6	OFF	Attributes
23	REFDES	6	ON	Reference designators
24	COMP	1	ABL (A)	Component side traces
25	SOLDER	2	ABL	Solder side traces
26	INT1	3	OFF	Internal layer traces

Drawing Sheets

The standard-size drawing sheet files, ASIZE.PCB through ESIZE.PCB, were created using the LAYS.PCB layer structure. When loaded, they provide the correct layer structure for the library plus a standard-size drawing sheet border.

Components

When you have loaded the layer structure or drawing sheet file, you can enter the components, wires, text, instances, and net names. Complete instructions are given in the "Using PC-CARDS" chapter of your *PC-CARDS User's Manual.*

GENERAL INFORMATION

This library was created using the *Fairchild F100K ECL Data Book* and Fairchild's F100K ECL August 1986 Preliminary Data Sheet. IEEE representations of all the devices are included.

Although the Fairchild F100K components come in both DIP and flatpack packages, only the DIP packages are included in this library. P-CAD does not support surface mount technology at this time.

NAMING CONVENTIONS

In this library, all signal names are entered exactly as shown in the *Fairchild F100K ECL Data Book* and the Preliminary Data Sheet. Signal names for the parts are given in the Dip Pin Sequence List section of this manual.

FOOTPRINTS

The components in this library have been assigned footprint attributes on the ATTR layer for PC-PLACE. All DIP parts have the footprint attribute : FP=DIPxx where xx is the number of pins for that part.

PADSTACKS

The padstacks included in the Fairchild F100K library are the standard P-CAD padstacks. They are not complete enough to be used as is. The padstacks for pad types 11 through 14 (which are used for supply and reference voltages) do not have the appropriate layers defined for the different voltages required of 100K ECL. All of the padstacks require the addition of the appropriate layers required by your design. Refer to the *PC-CARDS User's Manual* for more information on how to use padstacks and special symbols files.

COMPONENT LIST BY SEQUENCE

The component filename consists of the component number plus the extension .PRT; for example, 100142D.PRT. "Plot Number" refers to the plots in the last section of this manual.

Component Number	Disk Number	Plot Number
100101D	1	1
100102D	1	1
100104D	1	1
100107D	1	1
100112D	1	1
100113D	1	1
100114D	1	1
100117D	1	1
100118D	1	1
100121D	1	1
100122D	1	1
100123D	1	1
100124D	1	1
100125D	1	1
100126D	1	1
100128D	1	1
100130D	1	1
100131D	1	1
100135D	1	1
100136D	1	1
100139D	1	1
100140D	1	1
100141D	1	1
100142D	1	1
100145D	1	1
100150D	1	1
100151D	1	1
100155D	1	2

Component Number	Disk Number	Plot Number
100156D	1	2
100158D	1	2
100160D	1	2
100163D	1	2
100164D	1	2
100165D	1	2
100166D	1	2
100170D	1	2
100171D	1	2
100175D	1	2
100179D	1	2
100180D	1	2
100181D	1	2
100182D	1	2
100183D	1	2
100241D	1	2
100413D	1	2

COMPONENT LIST BY FUNCTION

The components described below come only in DIP packaging. The filename for these components have a "D" suffix, such as 100101D.SYM, to indicate DIP packaging.

AND/NAND Gates

100104	Quint 2-input

Arithmetic Operators

100156	4-bit mask-merge/latch
100158	8-bit shift matrix
100160	Dual 9-bit parity checker/generator
100165	8-input priority encoder
100166	9-bit comparator
100179	Carry lookahead
100180	High speed 6-bit adder
100181	4-bit binary/BCD ALU
100182	9-bit Wallace tree adder
100183	2x8 decode multiplier

Buffers

100121	9-bit inverter
100122	9-bit buffer
100126	9-bit backplane driver
100413	16x8 FIFO memory buffer

Content Addressable Memory

100142	4x4-bit content addressable memory

Counters/Prescalers

100136	4-bit binary (count up/down)
100139	4-bit binary (async reset)
100140	4-bit decade (count down)

Demultiplexer/Decoders

100170	Universal (dual 1 of 4/single 1 of 8)

Exclusive OR/NOR Gates

100107	Quint EXCLUSIVE OR/NOR

Flip-Flops

100131	Triple D (async set/reset)
100135	Triple J-K (async set)
100151	Hex D (async reset)

Latches

100130	Triple D (async set/reset)
100150	Hex D (async reset)
100155	Quad 2-input MUX/latch (async reset)
100175	Quint latch 100K in/10K out

Line Bus Drivers/Transceivers/Receivers

100112	Quad line driver
100113	Quad line driver
100114	Quint differential line receiver
100123	Hex bus driver

Multiplexers

100155	Quad 2-input MUX/latch (async reset)
100163	Dual 8-input
100164	16-input MUX
100171	Triple 4-input (W/enable)

OR-AND/OR-AND-INVERT Gates

100117	Triple 2-wide OA/OAI
100118	5-wide 5,4,4,4,2 input OA/OAI

OR/NOR Gates

100101	Triple 5-input
100102	Quint 2-input

RAMS

100145	16x4-bit register file

Shift Registers

100136	4-bit bidirectional
100141	8-bit bidirectional
100241	8-bit bidirectional

Translators

100124	Hex TTL-100K ECL
100125	Hex 100K ECL-TTL
100128	Octal ECL/TTL bidirectional

DIP PIN SEQUENCE LIST

100101D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	D3 (C)	9	O' (B)	17	D1 (B)
2	D4 (C)	10	O' (A)	18	VEE
3	D5 (C)	11	O (A)	19	D2 (B)
4	O (C)	12	D1 (A)	20	D3 (B)
5	O' (C)	13	D2 (A)	21	D4 (B)
6	VCC	14	D3 (A)	22	D5 (B)
7	VCCA	15	D4 (A)	23	D1 (C)
8	O (B)	16	D5 (A)	24	D2 (C)

100102D: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	D2 (E)	9	O (C)	17	D2 (B)
2	O (E)	10	O (B)	18	VEE
3	O' (E)	11	O' (B)	19	E
4	O' (D)	12	O' (A)	20	D1 (C)
5	O (D)	13	O (A)	21	D2 (C)
6	VCC	14	D1 (A)	22	D1 (D)
7	VCCA	15	D2 (A)	23	D2 (D)
8	O' (C)	16	D1	24	D1 (E)

100104D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	OE	9 =	OC	17 =	D2B
2 =	OE'	10 =	OB'	18 =	VEE
3 =	OD	11 =	OB	19 =	D1C
4 =	OD'	12 =	OA'	20 =	D2C
5 =	F	13 =	OA	21 =	D2D
6 =	VCC	14 =	D1A	22 =	D1D
7 =	VCCA	15 =	D2A	23 =	D1E
8 =	OC'	16 =	D1B	24 =	D2E

100107D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	OE	9 =	OC	17 =	D2B
2 =	OE'	10 =	OB'	18 =	VEE
3 =	OD	11 =	OB	19 =	D1C
4 =	OD'	12 =	OA'	20 =	D2C
5 =	F	13 =	OA	21 =	D2D
6 =	VCC	14 =	D1A	22 =	D1D
7 =	VCCA	15 =	D2A	23 =	D1E
8 =	OC'	16 =	D1B	24 =	D2E

100112D: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1 =	O2' (D)	9 =	O2 (B)	17 =	D (B)
2 =	O2' (C)	10 =	O1' (B)	18 =	VEE
3 =	O1' (C)	11 =	O2' (B)	19 =	E
4 =	O2 (C)	12 =	O2' (A)	20 =	D (C)
5 =	O1 (C)	13 =	O1' (A)	21 =	D (D)
6 =	VCC	14 =	O2 (A)	22 =	O1 (D)
7 =	VCCA	15 =	O1 (A)	23 =	O2 (D)
8 =	O1 (B)	16 =	D (A)	24 =	O1' (D)

100113D: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1	O2' (D)	9	O2 (B)	17	D (B)
2	O2' (C)	10	O1' (B)	18	VEE
3	O1' (C)	11	O2' (B)	19	E
4	O2 (C)	12	O2' (A)	20	D (C)
5	O1 (C)	13	O1' (A)	21	D (D)
6	VCC	14	O2 (A)	22	O1 (D)
7	VCCA	15	O1 (A)	23	O2 (D)
8	O1 (B)	16	D (A)	24	O1' (D)

100114D: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1	D' (E)	9	O (C)	17	D' (B)
2	O' (E)	10	O' (B)	18	VEE
3	O (E)	11	O (B)	19	VBB
4	O' (D)	12	O' (A)	20	D (C)
5	O (D)	13	O (A)	21	D' (C)
6	VCC	14	D (A)	22	D (D)
7	VCCA	15	D' (A)	23	D' (D)
8	O' (C)	16	D (B)	24	D (E)

100117D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	D2 (C)	9	O' (B)	17	E (B)
2	D3 (C)	10	O' (A)	18	VEE
3	D4 (C)	11	O (A)	19	E (C)
4	O (C)	12	D1 (A)	20	D1 (B)
5	O' (C)	13	D2 (A)	21	D2 (B)
6	VCC	14	D3 (A)	22	D3 (B)
7	VCCA	15	D4 (A)	23	D4 (B)
8	O (B)	16	E (A)	24	D1 (C)

100118D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D2D	9	O	17	D3B
2	D3D	10	D1A	18	VEE
3	D4D	11	D2A	19	D4B
4	D1E	12	D3A	20	D1C
5	D2E	13	D4A	21	D2C
6	VCC	14	D5A	22	D3C
7	VCCA	15	D1B	23	D4C
8	O'	16	D2B	24	D1D

100121D: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA	9	O' (G)	17	D (G)
2	O' (C)	10	O' (F)	18	VEE
3	O' (B)	11	O' (E)	19	VCCA
4	O' (A)	12	O' (D)	20	D (H)
5	O' (I)	13	VCCA	21	D (I)
6	VCC	14	D (D)	22	D (A)
7	VCCA	15	D (E)	23	D (B)
8	O' (H)	16	D (F)	24	D (C)

100122D: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA	9	O (G)	17	D (G)
2	O (C)	10	O (F)	18	VEE
3	O (B)	11	O (E)	19	VCCA
4	O (A)	12	O (D)	20	D (H)
5	O (I)	13	VCCA	21	D (I)
6	VCC	14	D (D)	22	D (A)
7	VCCA	15	D (E)	23	D (B)
8	O (H)	16	D (F)	24	D (C)

100123D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA2 (C)	9	VCCA2 (A)	17	DE (B)
2	OA (C)	10	OB (A)	18	VEE
3	VCCA1 (C)	11	VCCA1 (B)	19	E
4	OB (B)	12	OA (B)	20	DE (C)
5	VCCA2 (B)	13	DA (B)	21	DB (C)
6	VCC	14	DB (A)	22	DA (C)
7	VCCA1 (A)	15	DA (A)	23	DB (B)
8	OA (A)	16	DE (A)	24	OB (C)

100124D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	O' (A)	9	O (D)	17	D (D)
2	O (B)	10	O' (D)	18	VEE
3	O' (B)	11	O' (E)	19	E
4	O' (C)	12	O (E)	20	VTTL
5	O (C)	13	O' (F)	21	D (A)
6	VCC	14	O (F)	22	D (B)
7	VCCA	15	D (F)	23	D (C)
8	VCCA	16	D (E)	24	O (A)

100125D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	O (F)	9	O (B)	17	VBB
2	O (E)	10	O (A)	18	VEE
3	O (D)	11	D' (A)	19	D (D)
4	VTTL	12	D (A)	20	D' (D)
5	VTTL	13	D' (B)	21	D (E)
6	VCC	14	D (B)	22	D' (E)
7	VCC	15	D' (C)	23	D (F)
8	O (C)	16	D (C)	24	D' (F)

100126D: Number of gates per package = 9

Pin	Signal	Pin	Signal	Pin	Signal
1	VCCA	9	O (G)	17	D (G)
2	O (C)	10	O (F)	18	VEE
3	O (B)	11	O (E)	19	VCCA
4	O (A)	12	O (D)	20	D (H)
5	O (I)	13	VCCA	21	D (I)
6	VCC	14	D (D)	22	D (A)
7	VCCA	15	D (E)	23	D (B)
8	O (H)	16	D (F)	24	D (C)

100128D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	E4	9	T7	17	LE
2	E5	10	T6	18	VEE
3	E6	11	T5	19	VCC
4	E7	12	T4	20	VTTL
5	OE	13	T3	21	E0
6	VCC	14	T2	22	E1
7	VCCA	15	T1	23	E2
8	DIR	16	T0	24	E3

100130D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	CD (C)	9	Q' (B)	17	EC'
2	E' (C)	10	Q' (A)	18	VEE
3	D (C)	11	Q (A)	19	MR
4	Q (C)	12	D (A)	20	SD (B)
5	Q' (C)	13	E' (A)	21	D (B)
6	VCC	14	CD (A)	22	E' (B)
7	VCCA	15	SD (A)	23	CD (B)
8	Q (B)	16	MS	24	SD (C)

100131D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	CD (C)	9	Q' (B)	17	CPC
2	CP (C)	10	Q' (A)	18	VEE
3	D (C)	11	Q (A)	19	MR
4	Q (C)	12	D (A)	20	SD (B)
5	Q' (C)	13	CP (A)	21	D (B)
6	VCC	14	CD (A)	22	CP (B)
7	VCCA	15	SD (A)	23	CD (B)
8	Q (B)	16	MS	24	SD (C)

100135D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1	S (C)	9	Q (B)	17	S (B)
2	J (C)	10	Q' (A)	18	VEE
3	K (C)	11	Q (A)	19	K (B)
4	Q' (C)	12	S (A)	20	J (B)
5	Q (C)	13	C (A)	21	CP (B)
6	VCC	14	CP (A)	22	C (B)
7	VCCA	15	J (A)	23	CP (C)
8	Q' (B)	16	K (A)	24	C (C)

100136D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	TC'	9	Q2'	17	CP
2	Q0	10	Q3'	18	VEE
3	Q0'	11	Q3	19	MR
4	Q1'	12	D3	20	S0
5	Q1	13	P3	21	S1
6	VCC	14	P2	22	S2
7	VCCA	15	P1	23	CEP'
8	Q2	16	P0	24	D0/CET

100139D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P0	9	PE1	17	CP
2	Q0'	10	TC15'	18	VEE
3	Q0	11	TC14	19	CEP
4	Q1'	12	Q2'	20	MR
5	Q1	13	Q2	21	CET
6	VCC	14	Q3'	22	P3
7	VCCA	15	Q3	23	P2
8	TC14'	16	PE2	24	P1

100140D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P0	9	PE1	17	CP
2	Q0'	10	TC0'	18	VEE
3	Q0	11	TC1	19	CEP
4	Q1'	12	Q2'	20	MR
5	Q1	13	Q2	21	CET
6	VCC	14	Q3'	22	P3
7	VCCA	15	Q3	23	P2
8	TC1'	16	PE2	24	P1

100141D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	D0	9	Q5	17	CP
2	Q0	10	Q6	18	VEE
3	Q1	11	Q7	19	S0
4	Q2	12	D7	20	S1
5	Q3	13	P7	21	P3
6	VCC	14	P6	22	P2
7	VCCA	15	P5	23	P1
8	Q4	16	P4	24	P0

100142D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	MK3	9	Q2	17	A2
2	M0	10	Q1	18	VEE
3	M1	11	Q0	19	WS
4	M2	12	MK1	20	A1
5	M3	13	D1	21	A0
6	VCC	14	MK0	22	D2
7	VCCA	15	D0	23	MK2
8	Q3	16	A3	24	D3

100145D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	AR2	9	Q3	17	WE2
2	AR1	10	D3	18	VEE
3	AR0	11	D2	19	MR
4	Q0	12	D1	20	AW0
5	Q1	13	D0	21	AW1
6	VCC	14	OE1	22	AW2
7	VCCA	15	OE2	23	AW3
8	Q2	16	WE1	24	AR3

100150D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	Q' (F)	9	Q (C)	17	D (D)
2	Q' (E)	10	Q' (B)	18	VEE
3	Q (E)	11	Q (B)	19	MR
4	Q' (D)	12	Q' (A)	20	EA'
5	Q (D)	13	Q (A)	21	EB'
6	VCC	14	D (A)	22	D (E)
7	VCCA	15	D (B)	23	D (F)
8	Q' (C)	16	D (C)	24	Q (F)

100151D: Number of gates per package = 6

Pin	Signal	Pin	Signal	Pin	Signal
1	Q' (F)	9	Q (C)	17	D (D)
2	Q' (E)	10	Q' (B)	18	VEE
3	Q (E)	11	Q (B)	19	MR
4	Q' (D)	12	Q' (A)	20	CPA
5	Q (D)	13	Q (A)	21	CPB
6	VCC	14	D (A)	22	D (E)
7	VCCA	15	D (B)	23	D (F)
8	Q' (C)	16	D (C)	24	Q (F)

100155D: Number of gates per package = 4

Pin	Signal	Pin	Signal	Pin	Signal
1	D1 (D)	9	Q (B)	17	S1
2	Q (D)	10	Q (A)	18	VEE
3	Q' (D)	11	Q' (A)	19	MR
4	Q' (C)	12	D0 (A)	20	E1'
5	Q (C)	13	D1 (A)	21	E2'
6	VCC	14	D0 (B)	22	D0 (C)
7	VCCA	15	D1 (B)	23	D1 (C)
8	Q' (B)	16	S0'	24	D0 (D)

100156D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	AM1	9	Q0	17	E'
2	A3	10	B0	18	VEE
3	B3	11	A0	19	AS0
4	Q3	12	B1	20	BS1
5	Q2	13	A1	21	AS1
6	VCC	14	B2	22	BM0
7	VCCA	15	A2	23	AM0
8	Q1	16	BS0	24	BM1

100158D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Z7	9	Z2	17	S1
2	Z6	10	Z1	18	VEE
3	Z5	11	Z0	19	M
4	Z4	12	D0	20	S2
5	VCCA	13	D1	21	D4
6	VCC	14	D2	22	D5
7	VCCA	15	D3	23	D6
8	Z3	16	S0	24	D7

100160D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I6B	9	IA	17	I7A
2	I7B	10	I0A	18	VEE
3	IB	11	I1A	19	I0B
4	ZB	12	I2A	20	I1B
5	C'	13	I3A	21	I2B
6	VCC	14	I4A	22	I3B
7	VCCA	15	I5A	23	I4B
8	ZA	16	I6A	24	I5B

100163D: Number of gates per package = 2

Pin	Signal	Pin	Signal	Pin	Signal
1	D3 (B)	9	D0 (A)	17	S0
2	D2 (B)	10	D1 (A)	18	VEE
3	D1 (B)	11	D2 (A)	19	S1
4	D0 (B)	12	D3 (A)	20	S2
5	Z (B)	13	D4 (A)	21	D7 (B)
6	VCC	14	D5 (A)	22	D6 (B)
7	VCCA	15	D6 (A)	23	D5 (B)
8	Z (A)	16	D7 (A)	24	D4 (B)

100164D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	I3	9	I8	17	S0
2	I4	10	I9	18	VEE
3	I5	11	I10	19	S1
4	I6	12	I11	20	S2
5	I7	13	I12	21	S3
6	VCC	14	I13	22	I0
7	VCCA	15	I14	23	I1
8	Z	16	I15	24	I2

100165D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Q0	9	Q2	17	OE'
2	Q0'	10	Q2'	18	VEE
3	Q1'	11	Q3'	19	E'
4	Q1	12	Q3	20	M
5	GS1	13	I7	21	I3
6	VCC	14	I6	22	I2
7	VCCA	15	I5	23	I1
8	GS2	16	I4	24	I0

100166D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	B2	9	A0	17	A8
2	B1	10	A1	18	VEE
3	B0	11	A2	19	B8
4	A<B	12	A3	20	B7
5	A=B	13	A4	21	B6
6	VCC	14	A5	22	B5
7	VCCA	15	A6	23	B4
8	A>B	16	A7	24	B3

100170D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	A1B	9 =	Z0	17 =	EB1
2 =	Z7	10 =	Z2	18 =	VEE
3 =	Z4	11 =	Z1	19 =	EB2
4 =	Z6	12 =	A0A	20 =	EA2
5 =	Z5	13 =	A1A	21 =	HA
6 =	VCC	14 =	M	22 =	HC
7 =	VCCA	15 =	A2A	23 =	HB
8 =	Z3	16 =	EA1	24 =	A0B

100171D: Number of gates per package = 3

Pin	Signal	Pin	Signal	Pin	Signal
1 =	I1 (C)	9 =	Z' (B)	17 =	S1
2 =	I2 (C)	10 =	Z' (A)	18 =	VEE
3 =	I3 (C)	11 =	Z (A)	19 =	E'
4 =	Z (C)	12 =	I0 (A)	20 =	I0 (B)
5 =	Z' (C)	13 =	I1 (A)	21 =	I1 (B)
6 =	VCC	14 =	I2 (A)	22 =	I2 (B)
7 =	VCCA	15 =	I3 (A)	23 =	I3 (B)
8 =	Z (B)	16 =	S0	24 =	I0 (C)

100175D: Number of gates per package = 5

Pin	Signal	Pin	Signal	Pin	Signal
1 =	VCCA	7 =	E2	12 =	D (E)
2 =	Q (A)	8 =	VEE	13 =	D (A)
3 =	Q (B)	9 =	D (B)	14 =	Q (D)
4 =	Q (C)	10 =	D (D)	15 =	Q (E)
5 =	D (C)	11 =	MR	16 =	VCC
6 =	E1				

100179D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	P1	9	CN+8	17	P6
2	G2	10	G3	18	VEE
3	P2	11	P3	19	CN
4	CN+2	12	G4	20	G7
5	CN+4	13	P4	21	P7
6	VCC	14	G5	22	G0
7	VCCA	15	P5	23	P0
8	CN+6	16	G6	24	G1

100180D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	A0	9	F5	17	A3
2	F0	10	P	18	VEE
3	F1	11	G	19	CN
4	F2	12	B5	20	B2
5	F3	13	A5	21	A2
6	VCC	14	B4	22	B1
7	VCCA	15	A4	23	A1
8	F4	16	B3	24	B0

100181D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	A0	9	P	17	S1
2	F0	10	G	18	VEE
3	F1	11	CN	19	E
4	F2	12	B0	20	S2
5	F3	13	B1	21	S3
6	VCC	14	B2	22	A3
7	VCCA	15	B3	23	A2
8	CN+4	16	S0	24	A1

100182D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D1	9 =	PC	17 =	D6
2 =	D0	10 =	PS	18 =	VEE
3 =	CON+2	11 =	CI3	19 =	D5
4 =	CO3	12 =	CI2	20 =	{n/c}
5 =	CO1	13 =	CI1	21 =	{n/c}
6 =	VCC	14 =	CIN-2	22 =	D4
7 =	VCCA	15 =	D8	23 =	D3
8 =	CO2	16 =	D7	24 =	D2

100183D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	B0	9 =	F5	17 =	B4
2 =	F0	10 =	F6	18 =	VEE
3 =	F1	11 =	F7	19 =	A2
4 =	F2	12 =	F8'	20 =	A1
5 =	F3	13 =	B8	21 =	A0
6 =	VCC	14 =	B7	22 =	B3
7 =	VCCA	15 =	B6	23 =	B2
8 =	F4	16 =	B5	24 =	B1

100241D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1 =	D0	9 =	Q5	17 =	CP
2 =	Q0	10 =	Q6	18 =	VEE
3 =	Q1	11 =	Q7	19 =	S0
4 =	Q2	12 =	D7	20 =	S1
5 =	Q3	13 =	P7	21 =	P3
6 =	VCC	14 =	P6	22 =	P2
7 =	VCCA	15 =	P5	23 =	P1
8 =	Q4	16 =	P4	24 =	P0

100413D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Q0	9	Q4	17	IR
2	Q1	10	Q5	18	VEE
3	Q2	11	Q6	19	MR
4	Q3	12	Q7	20	TI
5	OR	13	D7	21	D3
6	VCC	14	D6	22	D2
7	VCCA	15	D5	23	D1
8	TO	16	D4	24	D0

E100142D: Number of gates per package = 1

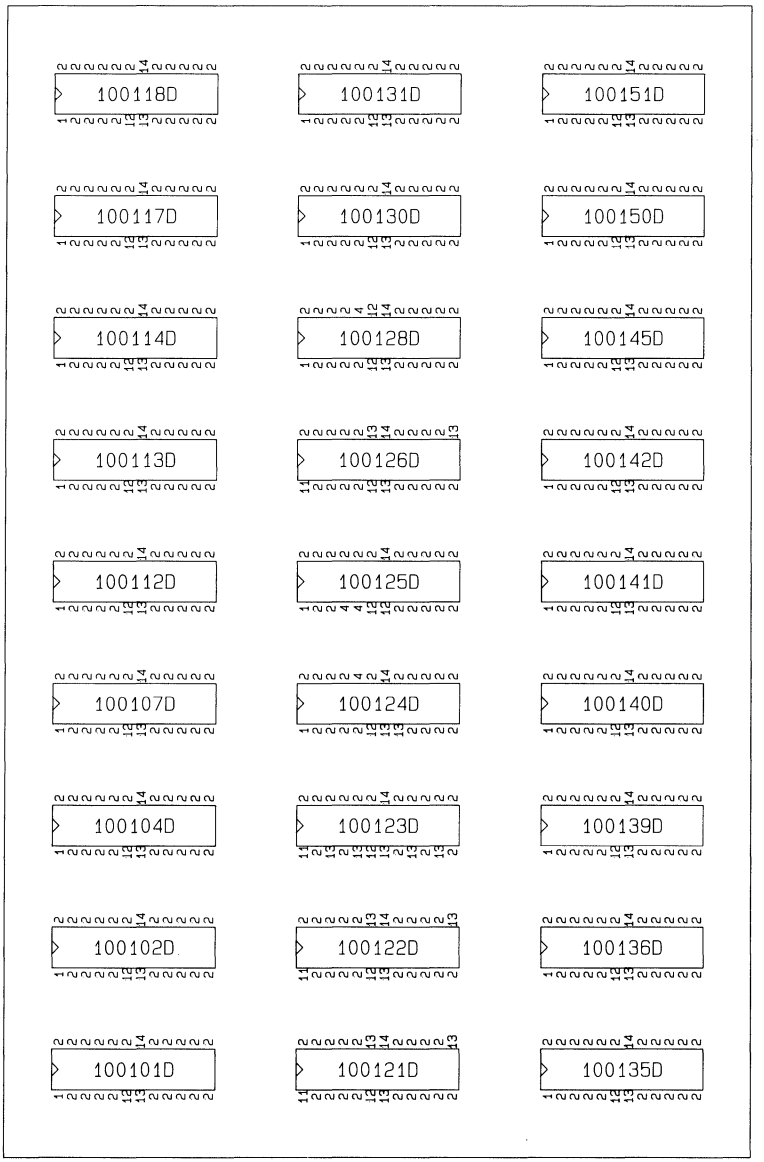
Pin	Signal	Pin	Signal	Pin	Signal
1	MK3	9	Q2	17	A2
2	M0	10	Q1	18	VEE
3	M1	11	Q0	19	WS
4	M2	12	MK1	20	A1
5	M3	13	D1	21	A0
6	VCC	14	MK0	22	D2
7	VCCA	15	D0	23	MK2
8	Q3	16	A3	24	D3

E100165D: Number of gates per package = 1

Pin	Signal	Pin	Signal	Pin	Signal
1	Q0	9	Q2	17	I6
2	Q0'	10	Q2'	18	VEE
3	Q1'	11	Q3'	19	I5
4	Q1	12	Q3	20	I7
5	GS1	13	M	21	I1
6	VCC	14	OE'	22	I2
7	VCCA	15	E'	23	I3
8	GS2	16	I0	24	I4

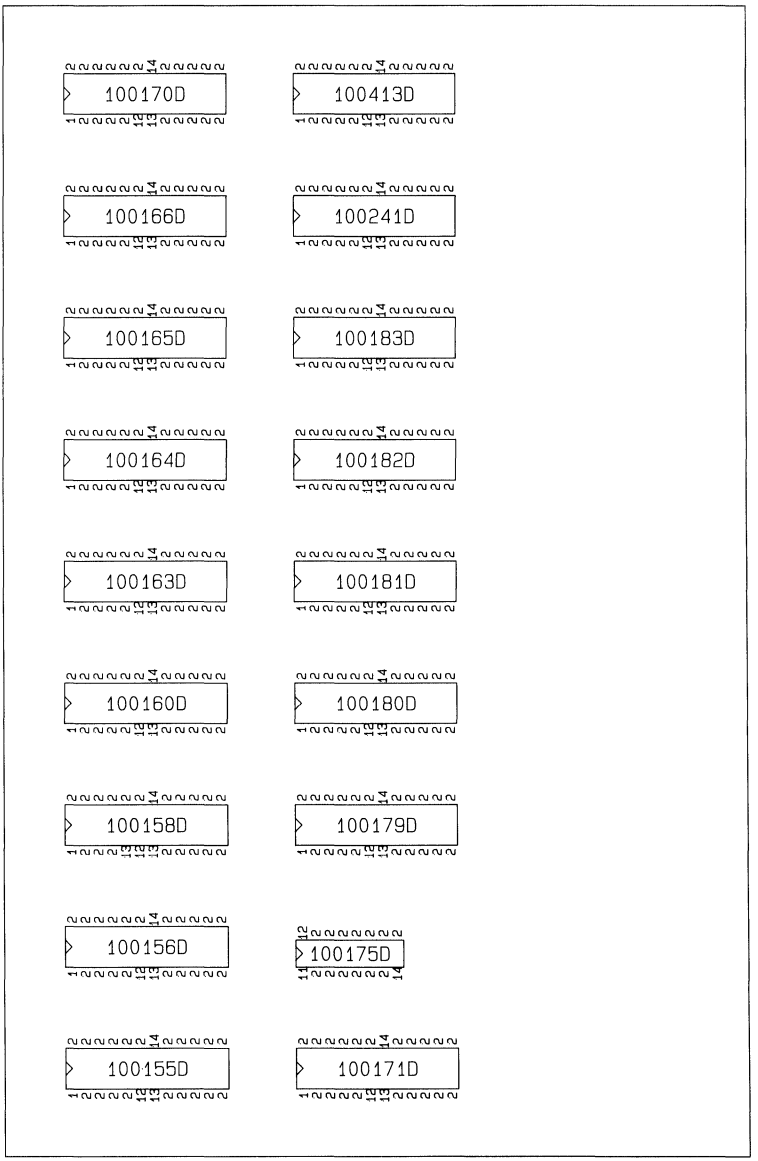
COMPONENT PLOTS

Plot 1



COMPONENT PLOTS

Plot 2



GERBER PHOTOPLOTTER APERTURE CHART

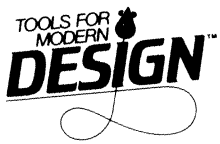
LAYER	TYPE 0 V50R28C.PS	TYPE 2 (N/C) 60R32C.PS	TYPE 3 (N/C) 60R32G.PS	TYPE 4 (N/C) 60R32P.PS
PADCOM	.050 Circle	.060 Circle	.060 Circle	.060 Circle
FLCOMP	Aperture 15	Aperture 9	Aperture 9	Aperture 9
PADSLD	.050 Circle	.060 Circle	.060 Circle	.060 Circle
FLSOLD	Aperture 15	Aperture 9	Aperture 9	Aperture 9
PADINT	.050 Circle	.060 Circle	.060 Circle	.060 Circle
FLINT	Aperture 15	Aperture 9	Aperture 9	Aperture 9
GNDCON	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X .100 Outer Diam	.020 Ring .060 Inner Diam
FLGCON	Aperture 8	Aperture 8	Aperture 22	Aperture 8
CLEAR	.100 Circle Solid Circle	.125 Circle Solid Circle	.125 Circle Solid Circle	.125 Circle Solid Circle
FLCLER	Aperture 20	Aperture 21	Aperture 21	Aperture 21
PWRCON	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X
FLPCON	Aperture 8	Aperture 8	Aperture 8	Aperture 22
SLDMSK	.060 Circle	.070 Circle	.070 Circle	.070 Circle
FLSMSK	Aperture 9	Aperture 11	Aperture 11	Aperture 11
DRILL	+28	+32	+32	+32
FLDRLL	Aperture 23 Text 28	Aperture 23 Text 32	Aperture 23 Text 32	Aperture 23 Text 32
PIN*	.050	.050	.050	.050

* The pin layer reflects connectivity (C) with a solid circle or no connectivity (N) with a hollow circle.

GERBER PHOTOPLOTTER APERTURE CHART (Continued)

LAYER	TYPE 1 (N/C) 60S32C.PS	TYPE 5 (N/C) 60S32P.PS	TYPE 6 (N/C) 60S32G.PS
PADCOM	.060 Square	.060 Square	.060 Square
FLCOMP	Aperture 10	Aperture 10	Aperture 10
PADSLD	.060 Square	.060 Square	.060 Square
FLSOLD	Aperture 10	Aperture 10	Aperture 10
PADINT	.060 Circle	.060 Circle	.060 Circle
FLINT	Aperture 9	Aperture 9	Aperture 9
GNDCON	.020 Ring .060 Inner Diam .100 Outer Diam	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X
FLGCON	Aperture 8	Aperture 8	Aperture 22
CLEAR	.125 Circle Solid Circle	.125 Circle Solid Circle	.125 Circle Solid Circle
FLCLER	Aperture 21	Aperture 21	Aperture 21
PWRCON	.020 Ring .060 Inner Diam .100 Outer Diam	Aperture 9 .025 Width X .100 Outer Diam	.020 Ring .060 Inner Diam
FLPCON	Aperture 8	Aperture 22	Aperture 8
SLDMSK	.070 Square	.070 Square	.070 Square
FLSMSK	Aperture 12	Aperture 12	Aperture 12
DRILL	+32	+32	+32
FLDRLL	Aperture 23 Text 32	Aperture 23 Text 32	Aperture 23 Text 32
PIN*	.050	.050	.050

* The pin layer reflects connectivity (C) with a solid circle or no connectivity (N) with a hollow circle.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