MODEL NO. BF649-30

SERIAL NO. 160708320

BUFFERED
PE FORMATTER
MODEL BF6X9

PERTEC

PERIPHERAL EQUIPMENT
DIVISION

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OPERATING AND SERVICE MANUAL NO. 101802

FOREWORD

This manual provides operating and service instructions for the Buffered PE Formatter, Model BF6X9 — 0.5K/1K/2K/4K, manufactured by PERTEC Peripheral Equipment Division, Chatsworth, California.

The content includes a detailed description, specifications, and installation instructions. Also included is the definition of interface functions with regard to timing, levels, and interrelationships. Section VII contains photo parts lists and schematics.

SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PERTEC agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact the following conveniently located regional service centers — our trained service staff will be pleased to assist you.

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PERTEC Service Center
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Encino, California 91316
Phone (213) 996-1333
TWX (910) 493-2075

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PERTEC Service Center
235 Bear Hill Road
Waltham, Massachusetts 02154
Phone (617) 890-6230
TWX (710) 324-1154

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PERTEC Service Center
6300 North River Road
O'Hare International Transportation Center
Rosemont, Illinois 60018
Phone (312) 696-2460
TWX (910) 253-5918

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PERTEC International
10 Portman Road
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SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the Buffered Phase Encoded Formatter, Model BF6X9, 0.5K/1K/2K/4K, manufactured by PERTEC Peripheral Equipment Division, Chatsworth, California.

1.2 PURPOSE OF EQUIPMENT

The Buffered Phase Encoded Formatter enables the asynchronous generation and reading of Phase Encoded (PE) ANSI and IBM compatible magnetic tapes when used in conjunction with PERTEC PE Magnetic Tape Transports. Data buffering, encoding, decoding, deskewing, error correction and tape motion control are provided by the formatter. The buffer portion of the formatter is 9 bits wide and may be one of four optional lengths. The ninth bit position may be used for flag data and is presented to the controller interface only. The buffer allows the data transfer to and from the customer's controller to be entirely asynchronous from 0 to 750 KHz.

Individual selection and operation with up to four *daisy-chained* PERTEC transports is provided. Normally, all transports attached to a formatter must be of the same speed. However, a dual speed option is available which allows the formatter to operate with any two different transport tape speeds. This option should be specified at the time of ordering.

The formatter section is capable of handling tape speeds in the range of 6.25 to 75.0 inches per second (ips).

The formatter operates directly from 100v ac to 250v ac, single phase, 48 to 400 Hz power. A tapped power transformer facilitates selection of the proper voltage.

1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

Two views of the Buffered PE Formatter are shown in Figure 1-1. The complete assembly is designed to be slide-mounted in a standard 19-inch EIA rack.

The formatter can be withdrawn from the rack to within three-quarters of its depth to facilitate servicing. The unit can be completely removed from the rack by increasing the withdrawing force.

The power supply and printed circuit boards are protected by a perforated panel which can be removed while the unit is extended. This provides access to the printed circuit boards from the top. A swing-down front panel (with cutouts to clear the power switch) provides access from the front.

A single operational control, the power switch, is located at the front of the power supply. Power is supplied through a 6-foot strain-relieved cord with a standard 3-pin plug.

Interface signals make connection to the formatter via edge connectors at the rear of the unit.

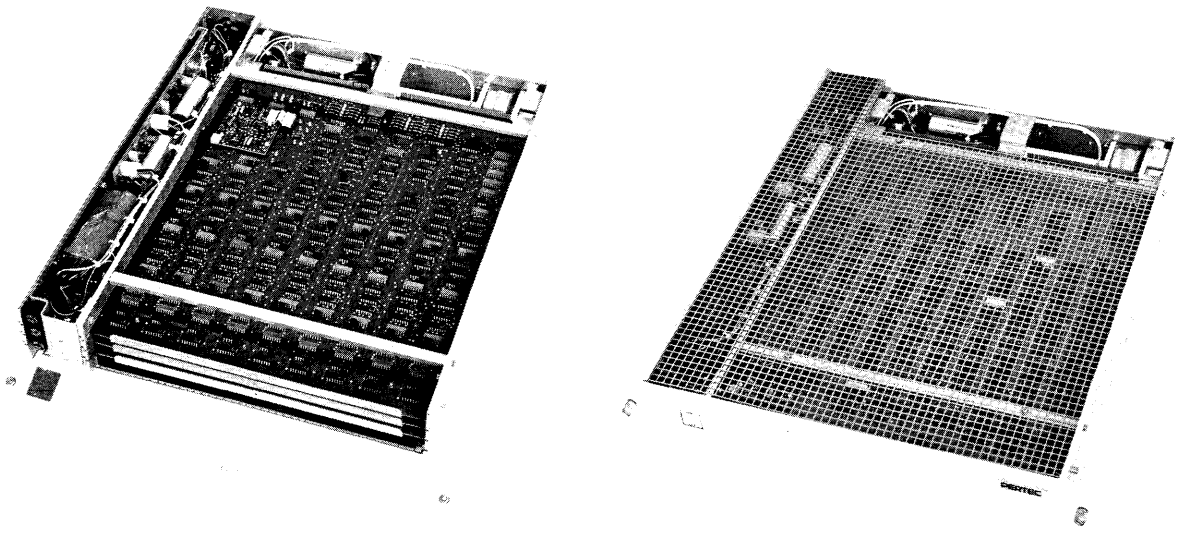


Figure 1-1. Buffered PE Formatter

1.4 FUNCTIONAL DESCRIPTION

The Buffered PE Formatter contains all logic and functions associated with the reading and writing of IBM and ANSI compatible 1600 cpi magnetic tape.

All logic for the generation of preamble, postamble, phase encoding data, and file mark patterns for recording onto magnetic tape is included in the formatter. Also, logic for the complete recovery of read data, including data decoding, buffering, error and file mark detection, and error correction logic is included.

Additionally, the formatter includes the following features.

(1) All timing necessary for the generation of IBM compatible IBGs and for correct head positioning between records.

(2) Compatibility with transports having either single- or dual-stack heads.

(3) Automatic recording of a Phase Mode identification burst prior to recording the first record on a tape.

(4) Automatic testing for the Phase Mode identification burst when reading the first record on a tape.

(5) Provision for fixed and variable length erase commands.

(6) Facility for generation of special commands for the editing of previously recorded tapes.

(7) Data buffering at optional lengths (512, 1024, 2048, or 4096) to be specified at time of order. Buffering can be performed either in a single- or split-buffer mode. Split, or double, buffering provides the customer with the option of continuous data flow at substantial throughput rates.

(8) Switch selectable error recovery attempts during read/write tape operation.

Two interfaces are provided, one to a controller and the other to the tape transports. Up to four transports may be daisy-chained on the transport interface. Figure 1-2 illustrates a typical system configuration.

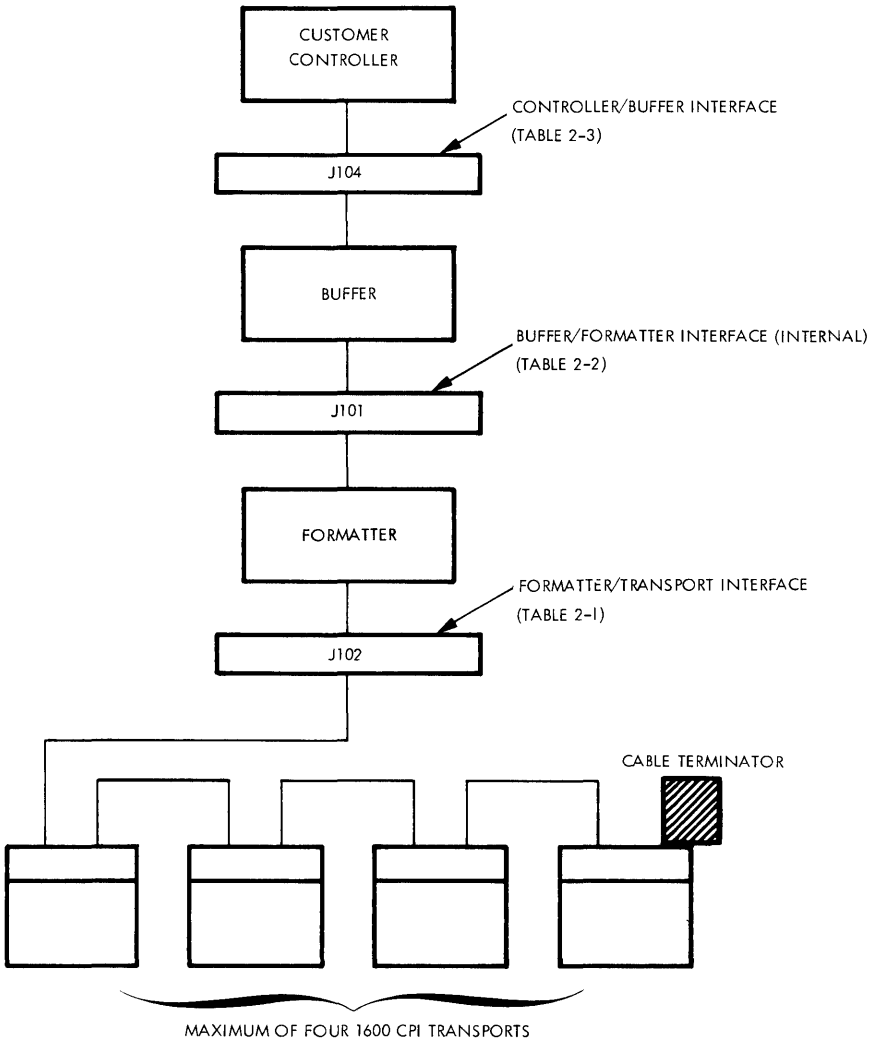


Figure 1-2. Typical System Configuration

1.5 MODEL DIFFERENCES

This manual covers the description of Models BF609, BF619, BF629, and BF649. The basic differences between the models are as follows.

(1) Model BF649 (Read After Write),
Model BF629 (Read/Write)

These models are similar except that Model BF649 is designed to operate with transports having a dual stack head, and BF629 is designed for use with transports having a single stack head. Both models consist of four basic sections: control logic, write logic, read logic, and buffer logic.

(2) Model BF619 (Read Only)

This model is used in Read Only applications, and consists of three basic sections: control logic, read logic, and buffer logic.

(3) Model BF609 (Write Only)

This model is used in Write Only applications, and consists of three basic sections: control logic, write logic, and buffer logic.

Each of the models described in Steps (1) through (3) can be configured to any of four optional buffer lengths. The length of the buffer can be 512, 1024, 2048 or 4096 and must be specified by the customer when the formatter is ordered.

1.6 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications are shown in Table 1-1.

1.6.1 INTERFACE SPECIFICATIONS

Levels: True = 0v (approximately)
False = +3v

Pulses: Levels as above. Minimum pulse width is 0.5 μsec. Edge transmission delay over 20 feet of cable is not greater than 100 nsec.

The interface circuits are designed so that a disconnected wire results in a false signal.

Figure 1-3 illustrates the configuration for which the transmitters and receivers have been designed.

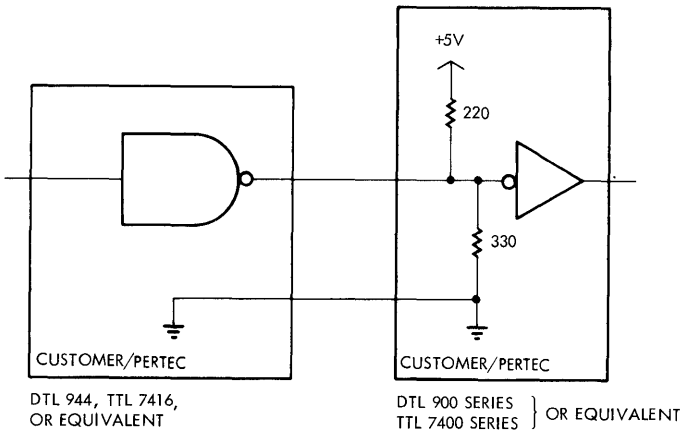


Figure 1-3. Interface Configuration

Table 1-1
Mechanical and Electrical Specifications

Buffer Lengths	512, 1024, 2048, or 4096*
Recording Mode (IBM and ANSI Compatible)	PE
Packing Density	1600 cpi
Number of Channels	9 (8 Data, 1 Parity)
Transport Tape Speed	6.25 to 75 ips (15.87 to 190.5 cm/s)
Data Rate Variation (Tracking Oscillator)	±10%
Preamble	41 Characters
Postamble	41 Characters
ID Burst (1600 frpi)	Channel P
Tape Mark (3200 frpi)	Channels P, 0, 2, 5, 6, and 7
Interblock Gap (IBG)	0.6 inch (15.24 mm) (nominal)
Parity	Odd
Dimensions	
Height	3.5 inches (8.89 cm)
Width	19.0 inches (48.26 cm)
Depth	20.0 inches (50.8 cm)
Weight	25 pounds (11.34 kg) (maximum)
Mounting — Standard 19-inch EIA Rack	—
Power	
Volts (ac)	100 — 250
Watts (maximum)	150
Frequency (Hz)	48 — 400
Electronics	All Silicon, DTL, TTL, MOS
Temperature	
Operating	2°C (35°F) to 50°C (122°F)
Non-Operating	—45°C (—50°F) to 71°C (160°F)
Altitude	
Operating	0 to 20,000 feet (0 to 6,096m)
Non-Operating	0 to 50,000 feet (0 to 15,240m)
Humidity (Operating)	10 to 95% (Without Condensation)
Error Retries (Switch Selectable)	0, 1, 2, 4, 8

*Optional Dual Buffer Lengths are 256, 512, 1024, 2048.

SECTION II
INSTALLATION

2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating the formatter, as well as the procedure for electrically connecting the formatter.

2.2 UNCRATING THE FORMATTER

The formatter is shipped in a protective container built to minimize the possibility of damage during shipping. The shipping container conforms to the National Safe Transit Committee Pre-Shipment Test Procedure.

The following procedure is used to uncrate the formatter unit.

(1) Place the shipping container in the position indicated on the container.

(2) Open the container by cutting the tape along the top joints of the container.

(3) Remove four 4-inch square polyurethane corner blocks.

(4) Remove the entire plywood shipping brace by lifting vertically.

(5) Place the formatter (contained within the shipping brace) on a flat surface and remove four 1/4-inch steel bolts.

(6) Remove the top plywood brace.

(7) Lift the formatter from remaining plywood brace and place on a flat surface.

(8) Remove the formatter from the plastic shipping bag.

(9) Remove the cable and the manual from the shipping carton.

Check the contents of the shipping container against the packing slip; investigate for possible damage. Notify the carrier immediately if any damage is noted.

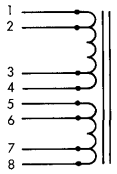
Access to the printed circuit boards is obtained by depressing the spring-loaded release button located on the right side of the formatter unit. The front panel, hinged at the bottom, will swing down to allow removal of the polyurethane foam pad placed inside the unit to prevent damage of the printed circuit boards during shipment.

Check the printed circuit boards and connectors for correct seating and installation.

Check that the identification label, located on the inside of the front panel, bears the correct model number and voltage requirement. If the actual line voltage at the installation site differs from that on the identification label, the power transformer taps should be changed as illustrated in Figure 2-1.

2.3 POWER CONNECTIONS

A fixed, strain-relieved power cord is supplied for plugging into a polarized 115v ac outlet. For other power sockets, the supplied plug must be removed and the correct plug installed.



LINE VOLTAGE	LINE INPUT	CONNECT
100	2 AND 7	2 AND 6, 3 AND 7
115	2 AND 8	2 AND 6, 4 AND 8
125	1 AND 8	1 AND 5, 4 AND 8
200	2 AND 7	3 AND 6
210	1 AND 7	3 AND 6
220	1 AND 7	3 AND 5
230	2 AND 8	4 AND 6
240	1 AND 8	4 AND 6
250	1 AND 8	4 AND 5

Figure 2-1. Transformer Primary Connections

2.4 RACK MOUNTING THE FORMATTER

The physical dimensions of the formatter, as illustrated in Figure 2-2, are such that it may be mounted in a standard 19-inch EIA rack; 3.5 inches of panel space is required. A depth of 20 inches behind the mounting surface is required.

To rack mount the formatter, proceed as follows.

(1) Install the two side rails on the formatter using ten No. 8 screws (five per side). Refer to Figure 2-2 for correct positioning.

(2) Install the two side rails in the EIA rack using eight No. 10 screws (four per rail). Refer to Figure 2-2 for correct positioning.

(3) Taking care to align the side guides with the side rails, slide the formatter unit into the rack.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT THE POWER CORD AND INTERFACE WIRING BUNDLES ARE NOT DAMAGED DURING THE RACK MOUNTING OPERATION.

(4) Tighten the two captive retaining screws on the front of the formatter.

2.5 INTERFACE CONNECTIONS

It is assumed that interconnection of PERTEC equipment and customer equipment uses a harness of individual twisted pairs, each with the following characteristics.

(1) Maximum length of 20 feet.

(2) Not less than one twist per inch.

(3) 22- or 24-gauge conductor with minimum insulation thickness of 0.01 inch.

Ensure that the ground side of each twisted pair is grounded within a few inches of the signal source and destination.

Included with the formatter is a single input/output cable, five feet in length, which will connect to a transport. This cable is terminated with a strain-relieved edge connector.

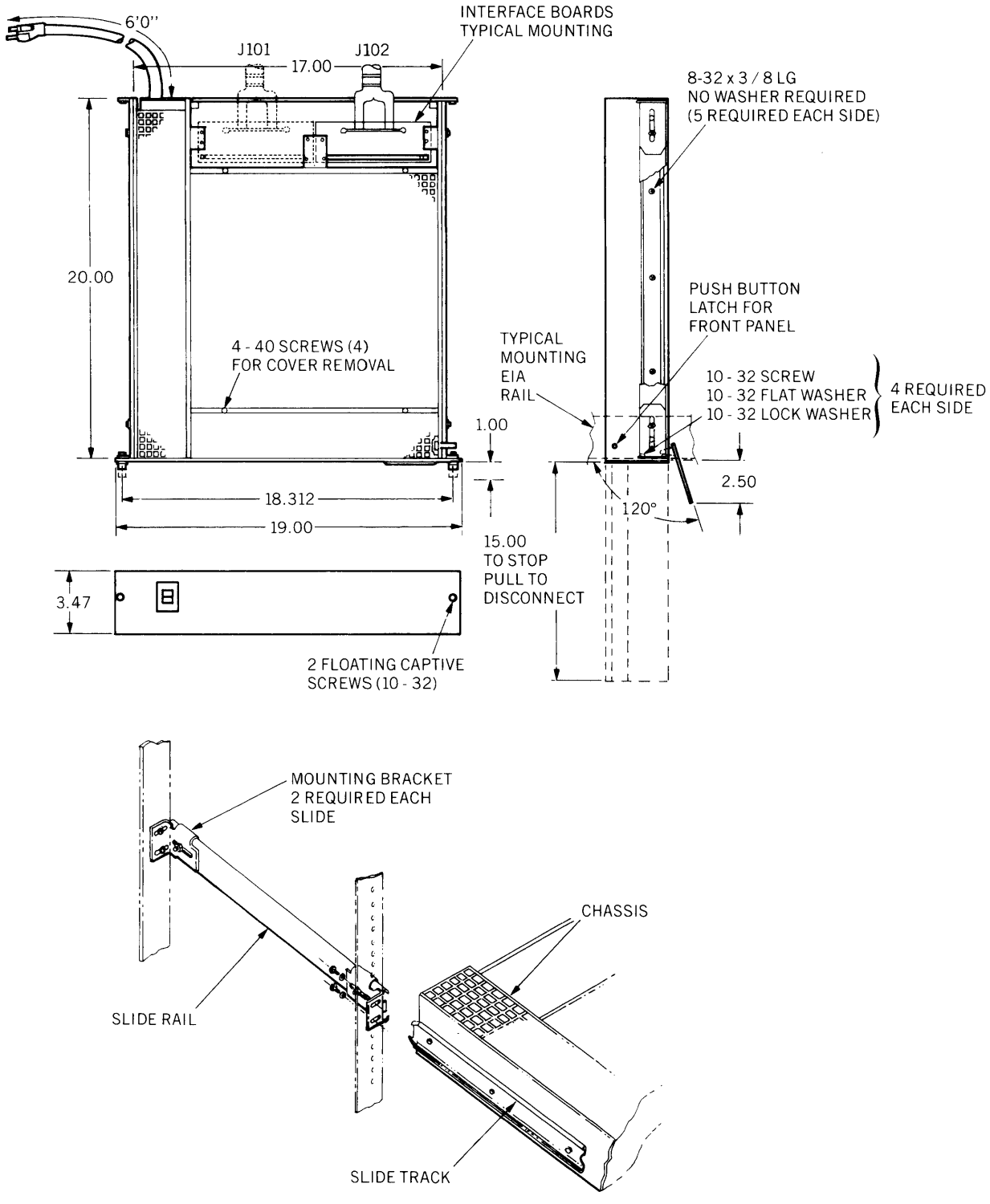


Figure 2-2. Rack Mounting the Buffered Formatter

The signal connector is a 100-pin 0.1-inch center edge connector with a cable terminating board attached. Tables 2-1 and 2-3 list the input/output pin connections. Table 2-2 lists the internal formatter interface between the buffer and the formatter.

NOTE

Pins on the 100-pin connectors are numbered A1 through A50, and B1 through B50, where pin A1 is opposite B1, etc. Due to the topology of the motherboard, pin connections on the four external interface connectors are reversed at the PCBA connectors.

Table 2-1

Interface Connections, Buffered Formatter/Transport

Connector (Reference Figure 2-2)	Live Pin	Gnd Pin	Signal*	Connector (Reference Figure 2-2)	Live Pin	Gnd Pin	Signal*
J102 Transport to Buffered Formatter	A1	A2	READ DATA STROBE (IRDS)**	J102 Buffered Formatter to Transport	B15	B14	WRITE DATA STROBE (IWDS)
	B1	B2	READ DATA PARITY (IRDP)		B16	B17	WRITE AMPLIFIER RESET (IWARS)
	B3	B2	READ DATA 0 (IRD0)		B18	B17	READ THRESHOLD Level 1 (IRTH1)
	A3	A2	READ DATA 1 (IRD1)		A18	A17	READ THRESHOLD Level 2 (IRTH2)
	A6	A5	READ DATA 2 (IRD2)		A21	A20	WRITE DATA PARITY (IWDP)
	B7	B8	READ DATA 3 (IRD3)		B22	B23	WRITE DATA 0 (IWD0)
	A7	A8	NRZI (INRZ)		A22	A23	WRITE DATA 1 (IWD1)
	B9	B8	7 TRACK (I7TR)**		B24	B23	WRITE DATA 2 (IWD2)
	A9	A8	SINGLE (ISGL)		A24	A23	WRITE DATA 3 (IWD3)
	B10	B11	SPEED (ISPEED)		B25	B26	WRITE DATA 4 (IWD4
	A10	A11	READ DATA 4 (IRD4)		A25	A26	WRITE DATA 5 (IWD5)
	B12	B11	READ DATA 5 (IRD5)		B27	B26	WRITE DATA 6 (IWD6)
	B13	B14	READ DATA 6 (IRD6)		A27	A26	WRITE DATA 7 (IWD7)
	A13	A14	READ DATA 7 (IRD7)		A28	A29	OVERWRITE (IOVW)
	A31	A32	DENSITY INDICATOR (IDDI) **		B30	B29	SYNCHRONOUS FORWARD Command (ISFC)
	B36	B35	ON-LINE (IONL)		A30	A29	DENSITY SELECT (IDDS)**
	A36	A35	REWIND (IRWD)		B31	B32	SYNCHRONOUS REVERSE Command (ISRC)
	B37	B38	IFPT		B33	B32	REWIND Command (IRWC)
	A37	A38	LOAD POINT (ILDP)		B34	B35	SET WRITE STATUS (ISWS)
	A39	A38	READY (IRDY)		A34	A35	OFF-LINE Command (IOFC)
	B40	B41	END OF TAPE (IEOT)		B42	B41	SELECT 0 (ISLT0)
					A42	A41	SELECT 1 (ISLT1)
					B43	B44	SELECT 2 (ISLT2)
					A43	A44	SELECT 3 (ISLT3)

*See Section III for definitions of interface functions.

**Not applicable to this formatter.

Table 2-2
Internal Connections, Formatter/Buffer

Connector (Reference Figure 2-2)	Live Pin	Gnd Pin	Signal*	Connector (Reference Figure 2-2)	Live Pin	Gnd Pin	Signal*
Buffer to Formatter	A1	A2	FORMATTER ADDRESS (IFAD)	Formatter to Buffer	A22	A23	FORMATTER BUSY (IFBY)
	B1	B2	TRANSPORT ADDRESS (ITAD0)		B22	B23	DATA BUSY (IDBY)
	A3	A2	TRANSPORT ADDRESS (ITAD1)		A24	A23	IDENTIFICATION (IDENT)
	B3	B2	INITIATE Command (IGO)		B24	B23	HARD ERROR (IHER)
	A4	A5	REVERSE/FORWARD (IREV)		A25	A26	CORRECTED ERROR (ICER)
	B4	B5	WRITE/READ (IWRT)		B25	B26	FILE MARK (IFMK)
	A6	A5	WRITE FILE MARK (IWFM)		A27	A26	READY (IRDY)
	B6	B5	EDIT (IEDIT)		B27	B26	ON-LINE (IONL)
	A7	A8	ERASE (IERASE)		A28	A29	REWINDING(IRWD)
	B7	B8	READ THRESHOLD Level 1 (ITHR1)		B28	A29	FILE PROTECT (IFPT)
	A9	A8	READ THRESHOLD Level 2 (ITHR2)		A30	A29	LOAD POINT (ILDP)
	B9	B8	DENSITY SELECT (IDEN)**		B30	B29	END OF TAPE (IEOT)
	A10	A11	PARITY SELECT (IPAR)**		B31	B32	NRZI (INRZ)
	B10	B11	LOAD AND ON-LINE (ILOL)		A33	A32	7 TRACK (I7TR)**
	A12	A11	REWIND (IREW)		B33	B32	SINGLE (ISGL)
	B12	B11	OFF-LINE (IOFL)		A34	A35	SPEED (ISPEED)
	A13	A14	LAST WORD (ILWD)		B34	B35	WRITE STROBE (IWSTR)
	B13	B14	FORMATTER ENABLE (IFEN)		A36	A35	READ STROBE (IRSTR)
	A16	A17	WRITE DATA 0 (IW0)		B36	B35	READ DATA PARITY (IRP)
	B16	B17	WRITE DATA 1 (IW1)		A37	A38	READ DATA 0 (IR0
	A18	A17	WRITE DATA 2 (IW2)		B37	B38	READ DATA 1 (IR1)
	B18	B17	WRITE DATA 3 (IW3)		A39	A38	READ DATA 2 (IR2)
	A19	A20	WRITE DATA 4 (IW4)		B39	B38	READ DATA 3 (IR3)
	B19	B20	WRITE DATA 5 (IW5)		A40	A41	READ DATA 4 (IR4)
	A21	A20	WRITE DATA 6 (IW6)		B40	B41	READ DATA 5 (IR5)
	B21	B20	WRITE DATA 7 (IW7)		A42	A41	READ DATA 6 (IR6)
					B42	B41	READ DATA 7 (IR7)

*See Section III for definitions of interface functions.
**Not applicable to this formatter.

Table 2-3
Interface Connections, Buffered Formatter/Controller

Connector (Reference Figure 2-2)	Live Pin	Gnd Pin	Signal*	Connector (Reference Figure 2-2)	Live Pin	Gnd Pin	Signal*
J104 Controller to Buffered Formatter Interface	A1	B2	LOAD ON-LINE (ILOL)	J104 Buffered Formatter to Controller	A23	B23	FORMATTER BUSY (IFBY)
	B1	B2	FORMATTER ADDRESS (IFAD0)		B25	B26	BUFFER A BUSY (IABSY)
	A2	B2	TRANSPORT ADDRESS (ITAD0)		A25	B26	BUFFER B BUSY (IBBSY)
	A3	B2	TRANSPORT ADDRESS (ITAD1)		B27	B26	BUFFER A OVERFLOW (IAOVFL)
	B3	B2	INITIATE Command (IGOI)		A27	B26	BUFFER B OVERFLOW (IBOVFL)
	B4	B5	REVERSE/FORWARD (IREVI)		A26	B26	DATA BUSY (IDBY)
	A4	B5	WRITE/READ (IWRTI)		B28	B29	IDENTIFICATION (IDENT)
	A5	B5	WRITE FILE MARK (IWFM)		A28	B29	HARD ERROR (IHER)
	B6	B5	EDIT (IEDIT)		A29	B29	CORRECTED ERROR (ICER) (PE Only)
	A6	B5	ERASE (IERASE)		A30	B29	FILE MARK (IFMK)
	B7	B8	THRESHOLD LEVEL 1 (ITHR1)		B30	B29	READY (IRDY)
	A7	B8	THRESHOLD LEVEL 2 (ITHR2)		B31	B32	ON-LINE (IONL)
	A8	B8	IDEN**		A31	B32	REWIND (IRWD)
	B9	B8	AUTOMATIC (IAUTO)		A32	B32	FILE PROTECT (IFPT)
	B10	B11	REWIND (IREW)		A33	B32	LOAD POINT (ILDP)
	A10	B11	OFF-LINE (IOFL)		B33	B32	END OF TAPE (IEOT)
	A11	B11	FORMATTER ENABLE (IFENI)		A34	B35	7 TRACK/9 TRACK (I7TRK)**
	B12	B11	END OF OPERATION (IEOO)		B34	B35	NRZI/PHASE ENCODED (INRZ)
	A12	B11	LAST WORD (ILWDI)		A35	B35	SINGLE STACK/DUAL STACK (ISGL)
	B13	B14	ANSWER STROBE (IANS)		A36	B35	HIGH SPEED/LOW SPEED (ISPEED)
	A13	B14	PARITY (or FLAG) (IWBP)		B36	B35	REQUEST DATA STROBE (IREQ)
	A14	B14	WRITE DATA 0 (IWB0)		A37	B38	READ DATA PARITY (IRBP)
	B15	B14	WRITE DATA 1 (IWB1)		A38	B38	READ DATA 0 (IRB0)
	A15	B14	WRITE DATA 2 (IWB2)		B39	B38	READ DATA 1 (IRB1)
	B16	B17	WRITE DATA 3 (IWB3)		A39	B38	READ DATA 2 (IRB2)
	A16	B17	WRITE DATA 4 (IWB4)		B40	B41	READ DATA 3 (IRB3)
	A17	B17	WRITE DATA 5 (IWB5)		A40	B41	READ DATA 4 (IRB4)
	B18	B17	WRITE DATA 6 (IWB6)		A41	B41	READ DATA 5 (IRB5)
	A18	B17	WRITE DATA 7 (IWB7)		B42	B41	READ DATA 6 (IRB6)
	B19	B20	BUFFER CONFIGURATION CONTROL 0 (IBCC0)		A42	B41	READ DATA 7 (IRB7)
	A19	B20	BUFFER CONFIGURATION CONTROL 1 (IBCC1)		B37	B38	BUFFER LAST WORD (IBLWD)
	B21	B20	BUFFER CONFIGURATION CONTROL 2 (IBCC2)				
	A21	B20	BUFFER CONFIGURATION CONTROL 3 (IBCC3)				
	B22	B23	COUNTER A INHIBIT (ICAI)				
	B24	B23	COUNTER B INHIBIT (ICBI)				

*See Section III for details of interface functions.
**Not applicable to this formatter.

SECTION III
OPERATION

3.1 INTRODUCTION

This section contains the functional specifications of the Buffered PE Formatter, a brief outline of the PE tape format, basic formatter operation, basic buffer operation, and a detailed definition of the various formatter interface lines.

3.2 CONTROLS AND INDICATORS

The Buffered PE Formatter utilizes a single operational control located on the front panel.

3.2.1 POWER

The ON/OFF switch is a rocker-type switch/indicator which connects line voltage to the power transformer. The indicator provides visual indication of the on/off status of the formatter.

When power is turned on, a reset signal is applied to all relevant flip-flops until the power supply voltages have been established.

When power is turned off or line voltage is lost, the formatter will reset all relevant flip-flops before the regulated power supplies decay, thus ensuring that no spurious signals are sent to the transports.

Three twist-lock fuses are provided adjacent to the power switch; a fourth fuse is located on the rear panel of the formatter. The front panel fuses consist of a 10-amp fast-blow fuse which protects the +5v circuits and two 1-amp fast-blow fuses which protect the +20v and —5v circuits. The rear panel fuse is a 2-amp slow-blow line fuse. Access to the front panel fuses is via the hinged front panel.

3.3 BASIC OPERATION

The Buffered PE Formatter is capable of executing the commands listed in Table 3-1. When a command is received from the customer's controller, the formatter goes *busy* and performs all control and timing functions necessary to execute the command. Any errors occurring during the command are reported to the controller. On completion of the command the formatter signals the controller and the controller is then free to issue a further command.

Two other command lines are provided which cause the transport to rewind, or to be switched off-line. These commands are routed directly to the selected transport and do not cause the formatter to go busy.

Note that for transports having a dual stack head, an automatic read-after-write data check is performed during each write command. Read-after-write errors are transmitted to the controller in the same manner as during read commands.

Figure 3-1 illustrates the 9-track PE tape format.

3.3.1 PREAMBLE

When writing, the formatter generates a preamble which precedes the data block. The preamble consists of 41 characters; the first 40 characters contain a zero (0) bit in each of

Table 3-1
Command Coding

	IAUTO	IREV	IWRT	IWFM	IEDIT	IERASE	ITHR1	ITHR2	IEOO	IBBC0	IBBC1	IBBC2	IBBC3
1. Read Tape Forward Into Buffer						A/R				A/R			
2. Read Tape Reverse Into Buffer		1											
3. Read Tape Reverse Edit Into Buffer		1			1								
4. Write Tape Forward From Buffer			1			A/R*							
5. Write Tape Forward Edit From Buffer			1		1								
6. Write File Mark Forward			1	1					Any Level				
7. Erase Variable Length Tape			1			1			A/R				
8. Erase Fixed Length Tape			1	1		1				Any Level			
9. Forward Space Tape						1	A/R						
10. Back Space Tape		1				1							
11. File Search Forward				1									
12. File Search Reverse		1		1									
13. Write Bufer From Controller			1					1		A/R			
14. Read Buffer To Controller								1					
15. Automatically Write Tape From Controller	1		1			A/R*			Any Level		1	Any Level	
16. Automatically Write Tape Continuous From Controller	1		1										
17. Automatically Read Tape To Controller	1					A/R							
18. Automatically Read Tape Continuously To Controller	1										1		

*As Required for Read-After-Write Units.

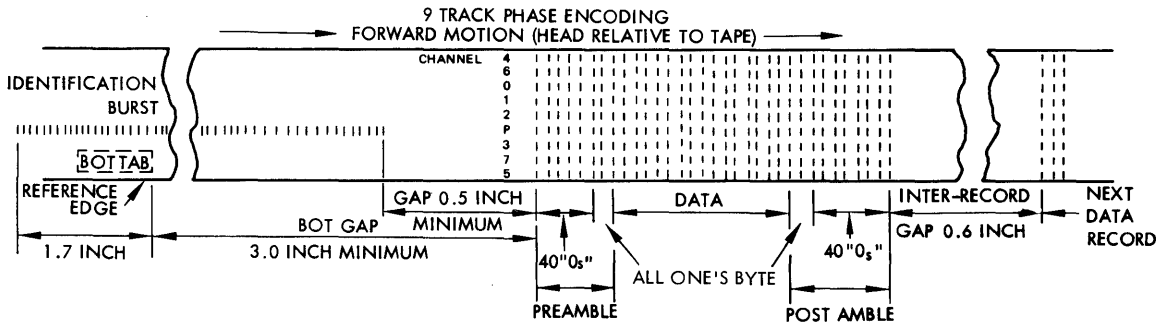


Figure 3-1. 9-Track PE Tape Format

the 9 tracks, and the subsequent single character contains a one (1) bit in each of the 9 tracks.

When performing a read operation, the formatter detects the preamble and separates it from the data block.

3.3.2 DATA

When writing, the buffer accepts asynchronous data, character by character, through a Request/Answer handshake circuit. The buffer then initiates the formatter which converts the data into a PE signal in which:

(1) A zero (0) bit is characterized by a transition in the middle of the bit cell away from the erase direction of magnetization.

(2) A one (1) bit is characterized by a transition in the middle of the bit cell toward the erase direction of magnetization.

When reading, the formatter accepts 9 channels of digital phase encoded data from the transport, and provides 4 bits of buffer per channel for the purpose of deskewing. The read logic assembles these data into parallel form, performs various error checks, and transmits the data to the buffer on 8 read data lines together with the strobe waveform. The buffer then offers the data asynchronously to the controller via the same Request/Answer handshake circuitry that wrote the data.

A tracking oscillator is provided in the formatter which can follow data rate variations of up to ±10 percent over 35 character periods. Data rate variation results from the Instantaneous Speed Variation (ISV) in the transport reading the tape, plus the ISV in the transport on which the tape was written.

3.3.3 POSTAMBLE

When writing, the formatter generates a postamble which follows the data and consists of 41 characters. The first character contains a one (1) bit in each of the 9 tracks; the subsequent 40 characters contain a zero (0) bit in each of the 9 tracks.

When performing a read operation, the formatter detects the postamble and separates it from the data block.

3.3.4 IDENTIFICATION BURST

When performing any write operation from BOT, the formatter automatically writes an IBM and ANSI compatible identification mark onto tape. This consists of a sequence of flux reversals at 1600 flux reversals per inch (frpi) in Channel P, with all other channels erased. A length of tape approximately 3 inches long is then erased before the first data record is written.

In the Read mode, the formatter samples the output of the parity channel as the BOT tab traverses the read head. If an identification burst is detected, the IDENT interface line is pulsed.

3.3.5 FILE MARK

When writing, the formatter generates a phase encoded tape mark consisting of 80 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4 are erased in the same direction as the IBG.

When reading, the formatter will recognize a file mark if it contains at least 64 flux reversals in Channels P, 0, and 5, or Channels 2, 6, and 7 with Channels 1, 3, and 4 dc-erased.

3.3.6 GAPS

The formatter provides the timing required to generate the following gaps.

(1) Interblock Gap (IBG)

- Nominal: 0.6 inch
- Minimum: 0.5 inch
- Maximum: 25 feet (depends upon number of consecutive erasures, no restrictions placed by the formatter to limit this distance).

(2) Initial Gap. When writing the first record from BOT, an ID burst is written followed by a gap of approximately 3 inches before the first data block.

When reading, the formatter can detect records written with an initial gap of 0.5 inch minimum between the end of the ID burst and the beginning of the first data block.

(3) File Mark Gap. A file mark is preceded by approximately 3.75 inches of tape with all tracks erased in the same direction as the IBG.

3.3.7 PARITY

During a write operation, the formatter generates odd parity derived from the data present on the 8 data channels. An option is provided (jumper selectable) whereby the parity bit can be supplied externally.

When reading, the formatter checks that the parity of the 9 channels is odd. An error is signaled when the parity check fails.

3.3.8 DROPOUT AND ERROR CORRECTION

The formatter provides single and multiple track dropout detection. When a single track dropout occurs, the formatter performs error correction by use of the parity circuits and the data on the other 8 channels. A status line to the buffer indicates when error correction is taking place within the formatter.

After a track has experienced a dropout, the output of that track will be ignored for the remainder of that record, and no attempt will be made by the formatter to re-synchronize the data on that track.

3.3.9 ERROR CHECKING

A switch is provided on the Buffer PCBA to enable the automatic rewrite or reread of erroneous records. When selected, error retry is attempted in both the split- and single-buffer modes and during both a Write Tape or Read Tape operation in either direction. In the event that an error is detected, the buffer logic causes the formatter to command the selected tape transport to backspace and reread or, when used with read-after-write tape drives, rewrite the affected record. A maximum of 8 (switch selectable) attempts at writing a record can be made before the buffer logic flags the interface that a hard error (IHERI) exists. In the event of an IHERI after the maximum number of attempts, the tape transport is commanded to advance to the next record and perform the next operation.

3.3.10 OPTIONS

The following features are available as options and must be specified at the time of ordering.

(1) Formatter address — 0 or 1.

(2) Internal or external Write Parity generation.

(3) Dual speed option.

(4) Buffer lengths of 512, 1024, 2048, or 4096 bits.

3.4 BUFFERED FORMATTER INTERFACING

There are two interfaces provided by the formatter, one from controller to formatter, and the other from formatter to transport. These interfaces are detailed in Tables 2-1 and 2-2.

The Buffered PE Formatter is designed so that up to four PERTEC PE transports can be daisy-chained on the formatter transport interface.

3.5 INTERFACE INPUTS (CONTROLLER TO BUFFERED FORMATTER)

All waveform names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the true level 0v and the false level +3v. All pulse widths at the interface must be a minimum of 0.5 μsec wide.

A disconnected interface line is interpreted as a logical false signal by the formatter logic.

3.5.1 FORMATTER ADDRESS (IFAD0)

The level on this line controls the selection of one of two possible formatters on the controller to buffer interface. The decoding of this address is performed on the specific formatter.

When selected, a buffered formatter is connected to the controller and all controller/buffered formatter interface lines are activated by enabling the buffer to formatter interface lines. The individual formatter address is determined by an address switch on the formatter PCBA.

NOTE

Descriptions of the controller/buffered formatter interface lines in the following paragraphs assume that the formatter is Selected [unless otherwise noted].

3.5.2 LOAD AND ON-LINE (ILOL) (OPTIONAL)

The Load and On-line interface line is routed through the buffered formatter interface to the applicable transport interface.

A true pulse on this line enables a remote Load sequence in the selected transport. A second pulse spaced a minimum of 1 second from initial pulse causes the transport to be placed On-line.

3.5.3 TRANSPORT ADDRESS (ITAD0, ITAD1)

The levels on these two lines determine which of the four possible transports is connected to the formatter. These lines are routed through the buffer and are decoded by the formatter; the code is then transmitted to the buffered formatter/transport interface. The following are levels and addresses associated with the selection of the transport by the formatter.

ITAD0	ITAD1	ADDR
0	0	ISLT0
0	1	ISLT1
1	0	ISLT2
1	1	ISLT3

When the buffer is not busy with a command, the state of these lines is not stored. Therefore, any formatter and any transport can be selected to inspect its status.

3.5.4 GO, INITIATE COMMAND, (IGOI)

This is a pulse which initiates the command specified by the command lines. The information on the command lines is loaded into the buffer control logic on the leading edge of the GO pulse. Simultaneously, the Buffer Busy signal (Paragraph 3.6.2) is set true and stays true until completion of the specific command.

3.5.5 COMMAND LINES

The levels on these lines (Paragraphs 3.5.7, 3.5.13, 3.5.17) specify a command to the buffer. The levels on the command lines are transferred to the formatter on the leading edge of the IGOI pulse. The levels must be held steady from 0.5 μsec before to 0.5 μsec after the trailing edge of GO.

Table 3-1 defines the command coding for various tape and buffer operations.

3.5.6 REVERSE/FORWARD (IREVI)

This is a level which, when true, specifies reverse tape motion and which, when false, specifies forward tape motion. This line must be held stable for the duration of the command.

3.5.7 WRITE/READ (IWRTI)

This is a level which, when true, specifies the Write mode of operation; when false, the Read mode of operation is specified.

3.5.8 WRITE FILE MARK (IWFM)

This is a level which, when true, and IWRTI (Paragraph 3.5.7) is true, causes a file mark to be written on tape; if IWRTI is false, the buffer searches for a file mark in the direction indicated by the IREVI line (Paragraph 3.5.6) and causes tape to stop on the first file mark encountered.

3.5.9 EDIT (IEDIT)

This is a level which, when true and IREVI is true, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When this level is true and IWRTI is true, the IOVW line is activated and the selected transport operates in the Edit mode.

3.5.10 ERASE (IERASE)

This is a level which, when true in conjunction with a true level on the IWRTI line, causes the formatter to execute a dummy WRITE command. The length of tape erased is determined by one of the following.

(1) If IWRTI, IERASE, and IWFM are true, 3.75 inches of tape will be erased.

(2) If IWRTI and IERASE are true, the buffered formatter transfers an erase variable command to the formatter and a length of tape, determined by the record length previously latched in the buffer, will be erased.

(3) If IWRTI is false and IERASE is true, the buffer will backspace or forwardspace the tape one record without a data transfer into or out of the buffer. There will be no erasure of tape in this condition.

3.5.11 READ THRESHOLD LEVEL 1 (ITHR1)

The levels on this line are utilized only in transports having a single stack head and specifies the operating level of the read threshold circuits. A true level specifies selection of the high read threshold level; a false level specifies the normal read threshold.

3.5.12 READ THRESHOLD LEVEL 2 (ITHR2)

The levels on this line are utilized in those transports having an extra low threshold capability. When true, the extra low threshold is specified; when false, the normal threshold is specified. The true level will normally be used only when it is required to recover data of very low amplitude.

3.5.13 AUTOMATIC (IAUTO)

This is a level which, when true, specifies an automatic read data transfer operation through the buffer. This line must be held true for the duration of the command.

3.5.14 REWIND (IREW)

This is a pulse which causes the Selected and On-line transport to rewind to the Load Point. Thus pulse is routed directly to the transport and does not cause the buffer to go busy.

3.5.15 OFF-LINE COMMAND (IOFL)

This is a pulse which, when true, causes the selected transport to revert to the Off-line mode. This pulse is routed directly to the transport and does not cause the buffer to go busy.

3.5.16 FORMATTER ENABLE (IFENI)

This is a level which, when false, causes the buffer control logic to revert to the quiescent state. This line may be used to disable the buffer if the controller power is lost, or to clear the buffer control logic (command register and sequence control) in case of an illegal command or unusual condition.

3.5.17 END OF OPERATION (IEOO)

This line is used as a command line to distinguish a straight buffer operation from a straight formatter operation, and to terminate automatic continuous buffer commands.

3.5.18 ANSWER STROBE (IANS)

This is a pulse which, when true, strobes data into the buffer during a write operation and accepts data from the buffer during a read operation. IANS is the answer (or handshake) to the IREQ line.

For a read buffer operation the data availability depends on IREQ (request) but the data will be held on the buffer output lines at least 500 nsec after IANS (answer) goes false.

For a write buffer operation, the controller must make data available at most 200 nsec after IANS goes true and hold the data on the buffer input lines at least 800 nsec after IANS goes true. The IANS line must be a minimum of 300 nsec wide.

3.5.19 LAST WORD (ILWDI)

This line is used to terminate the WRITE BUFFER sequence. ILWDI must be issued instead of IANS in response to the buffer's IREQ for data.

3.5.20 WRITE PARITY, WRITE DATA LINES (IWBP, IWB0 - IWB7)

These 9 lines transmit Write Data from the controller to the buffer. Upon receipt of an IREQ, the controller should set up the data on the IWB0 - IWB7, IWBP lines. Subsequent to setting the data on the lines, the controller issues an IANS and the buffer copies the data. This IREQ/IANS handshake continues until the controller terminates the dat transfer by issuing an ILWD instead of an IANS.

3.5.21 BUFFER CONFIGURATION CONTROL 0 (IBCC0)

The choice of source for input data to the buffer are chosen by the level on this line. Read data from tape via formatter, or write data from the controller, are routed to the desired half-buffer input according to the state of IBCC0. This line must be held true for the duration of the command.

(1) False — IRP, IR0 - IR7 to Buffer A; IWBP, IWB0 - IWB7 to Buffer B.

(2) True — IRP, IR0 - IR7 to Buffer B; IWBP, IWB0 - IWB7 to Buffer A.

3.5.22 BUFFER CONFIGURATION CONTROL 1 (IBCC1)

The level on this line configures the buffer to operate as a single buffer when false. When this level is true, the buffer is configured to operate as a split buffer (i.e., one-half single capacity). This line must be held true for the duration of the command.

3.5.23 BUFFER CONFIGURATION CONTROL 2, 3 (IBCC2, IBCC3)

The levels on these lines control the output data flow from the buffer. Specific coding necessary for desired data flow are as follows.

IBCC2	IBCC3	
False	False	Buffer A to IWP, IW0 - IW7 and IRBP, IRB0 - IRB7
False	True	Buffer A to IWP, IW0 - IW7, Buffer B to IRBP, IRB0 - IRB7
True	False	Buffer B to IWP, IW0 - IW7, Buffer A to IRBP, IRB0 - IRB7
True	True	Buffer B to IWP, IW0 - IW7 and IRBP, IRB0 - IRB7

3.5.24 COUNTER RESET INHIBIT (ICAI, ICBI)

The levels on these two lines are utilized to inhibit the normalizing of both counters associated with a particular half-buffer. ICAI is associated with Buffer Half A; ICBI is associated with Buffer Half B.

If the counters are inhibited, two consecutive records will be juxtaposed in the buffer as one long record. When a record has been written with the appropriate inhibit asserted, an IFENI will be required to reset the counter prior to writing a separate subsequent record.

3.6 INTERFACE OUTPUTS (BUFFERED FORMATTER TO CONTROLLER)

All waveform names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the true level 0v and the false level +3v. All pulse widths at the interface must be a minimum of 0.5 μsec wide.

3.6.1 FORMATTER BUSY (IFBY)

This is a level which is set true on the trailing edge of a IGO command when any command is issued to the formatter. It remains true until tape motion ceases after the execution of the command. This signal is routed from the formatter to the buffer/controller interface.

3.6.2 BUFFER BUSY (IABSY, IBBSY)

The levels on these two lines, when true, signify that the relevant buffer is busy and no new command can be executed until the existing command is completed. When, for example, IABSY goes false the controller can issue any new command relevant to the A-Buffer in the split-buffer mode. When the buffer is not split, the IABSY line signals the status of the entire (A + B) buffer.

3.6.3 BUFFER OVERFLOW INDICATORS (IAOVFL, IBOVFL)

The signals on these two lines are levels which, when true, indicate an overflow condition exists in the relevant buffer. This level is presented to the controller interface when the next data transfer will cause buffer overflow.

3.6.4 DATA BUSY (IDBY)

This is a level which goes true when the tape on the selected transport has reached operating speed, traversed the IBG, and the formatter is about to transfer data.

IDBY remains true until data transfer is completed and the appropriate post-record delay is completed. IDBY goes false as the capstan starts to decelerate the tape. To perform on-the-fly data transfers, the controller should issue the next command and IGOI pulse as soon as IDBY goes false. This line is routed internally to the buffer and is provided to the buffer/controller interface.

3.6.5 IDENTIFICATION (IDENT)

This is a level which is set true to identify Phase Encoded (PE) tapes. When reading forward off of the BOT, the formatter inspects the parity channel for the presence or absence of the identification burst which distinguishes PE tapes. If an identification burst is detected, this line is set true for a short period as the BOT tab passes over the read head.

3.6.6 HARD ERROR (IHERI)

This is a pulse or level which, when true, indicates that an uncorrectable read error has been detected by the formatter. This line is active during Read Forward, Read Reverse, and Read-After-Write (dual stack head) operation if one or more of the following occur.

(1) False preamble detection.

(2) False postamble detection.

(3) Multi-channel dropout.

(4) Parity error without associated channel dropout.

(5) When a given number of automatic retries are selected, the IHERI signal will not be asserted until these retries are exhausted.

When an error is detected while operating in a Read mode, IHERI will go true on completion of the tape operation after the selected number of retries and will be reset at the leading edge of the next BSY. For detected errors when operating in a Read-After-Write mode, IHERI will go true when the formatter detects an error and is reset at the beginning of the next tape operation or by clearing IFENI.

In the case of a vertical parity error, the formatter IHER line will be pulsed at the time the read data for the character in error is strobed into the buffer. The buffer will catch this signal and IHERI will be asserted after the complete record has been read.

All error information will be transferred to the controller prior to Data Busy (IDBY) going false.

3.6.7 CORRECTED ERROR (ICER)

This is a pulse which indicates that a single track dropout has been detected and that the formatter is performing error correction.

NOTE

When performing a Read-After-Write operation, the record should be rewritten if either an IHERI or ICER error is detected.

3.6.8 TRANSPORT STATUS AND CONFIGURATION (IRDY, INRZ, I7TRK, ISGL, ISPEED, IONL, IRWD, IFPT, IEOT, ILDP)

These lines indicate the status and configuration of the selected transport and are defined exactly the same as in the transport to buffered formatter interface inputs description except that they are gated with the formatter busy line IFBY.

- Status: IRDY, IONL, IRWD, IFPT, ILDP, IEOT
- Configuration: INRZ, I7TR, ISINGLE, ISPEED

3.6.9 FILE MARK (IFMK)

This is a pulse which indicates that the formatter read logic has detected a file mark. The IFMK line will go true upon detection of a file mark during any read forward or read reverse operation. IFMK data bytes are not loaded into the buffer and are not presented to the controller. Error conditions should be ignored when a file mark is detected.

3.6.10 REQUEST STROBE (IREQ)

This is a level which, when true, indicates to the controller that the buffer is ready to transfer data to or from the controller. In a write buffer transfer, the controller's response (IANS) to this request is used to copy the data into the buffer. In a read buffer transfer, the controller response (IANS) to this request is used to clock the buffer and ready the next data byte on the output lines.

3.6.11 BUFFER LAST WORD (IBLWD)

This is a signal which, when true, indicates to the controller that the buffer has transferred the last byte of valid data specified in the last command.

3.6.12 READ DATA LINES (IRBP, IRB0 - IRB7)

These 9 lines transmit read data from the buffer to the controller. Lines IRBP, IRB0 - IRB7 are used for 9-channel operation.

Each character is set up on the read data lines, IREQ is then set true. The controller, when ready to accept data, sets IANS true. The controller accepts the data, then resets the IANS line. The buffer then sets up the next character on the read data lines when IANS goes false.

3.7 INTERNAL INTERFACE — BUFFER TO FORMATTER

All waveform names are chosen to correspond to the logical true condition. All lines are low-true at the internal interface with the true level 0v and the false level + 3v.

All pulse widths at the interface must be a minimum of 1 μsec wide.

3.7.1 FORMATTER ADDRESS (IFAD)

The level on this line controls the selection of one of two possible formatter combinations on the controller to buffer interface. The decoding of this address is performed on the specific formatter section; in this system the PE Write PCBA performs the decoding.

When selected, a formatter is connected to the controller and all controller/buffered formatter interface lines are activated. The individual formatter address is determined by an address switch on the formatter PCBA.

NOTE

The descriptions of buffer/formatter interface lines in the following paragraphs assume that the formatter is selected, unless otherwise noted.

3.7.2 TRANSPORT ADDRESS (ITAD0, ITAD1)

The levels on these two lines determine which of the four possible transports is connected to the buffered formatter/transport interface. The lines are decoded by the formatter and transmitted to the buffered formatter/transport interface. The following are levels and addresses associated with the selection of the transport by the formatter.

ITAD0	ITAD1	IADDR
0	0	ISLT0
0	1	ISLT1
1	0	ISLT2
1	1	ISLT3

3.7.3 INITIATE COMMAND (IGO)

This is a pulse which initiates the command specified by the command lines (Paragraphs 3.7.4.1 through 3.7.4.7). The information on the command lines is copied into the corresponding formatter flip-flops on the trailing edge of the IGO pulse. If the formatter and the selected transport are ready the command is accepted by the formatter and the Formatter Busy (IFBY) line is set true.

3.7.4 COMMAND LINES

The levels on these lines specify a command to the formatter. The levels on the commands are transferred to the formatter on the trailing edge of the IGO pulse. The levels must be held steady from 0.5 μsec before to 0.5 μsec after the trailing edge of IGO.

The command lines are identified and functionally described in Paragraphs 3.7.4.1 through 3.7.4.7.

3.7.4.1 Reverse/Forward (IREV)

This is a level which, when true, specifies reverse tape motion and which, when false, specifies forward tape motion.

3.7.4.2 Write/Read (IWRT)

This is a level which, when true, specifies the Write mode of operation and which, when false, specifies the Read mode of operation. Therefore, this line should be held false for the duration of the command.

3.7.4.3 Write File Mark (IWFM)

This is a level which, when true and WRT/READ is also true, causes a file mark to be written onto tape.

3.7.4.4 EDIT (IEDIT)

This is a level which, when true and IREV is true, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When this level is true and IWRT is true, the IOVW line is activated and the selected transport operates in the Edit mode.

3.7.4.5 ERASE (IERASE)

If IERASE and IWRT are true, the formatter is conditioned to execute a dummy WRITE command. The formatter will go through all of the operations of a normal WRITE command, except that no data are recorded. A length of tape will be erased equivalent to the length of the dummy record (as defined by ILWD).

Alternatively, if IERASE, IWRT, and IWFM are true, the formatter will execute a dummy IWFM command. A fixed length of tape, approximately 3.5 inches, will be erased.

3.7.4.6 READ THRESHOLD LEVEL 1 (ITHR1)

The levels on this line are utilized in transports having a single stack head and specifies the operating level of the read threshold circuits. A true level specifies selection of the high read threshold; a false level specifies the normal read threshold.

3.7.4.7 READ THRESHOLD LEVEL 2 (ITHR2)

The levels on this line are utilized in those transports having an extra low read threshold capability.

When true, the extra low threshold is specified; when false, the normal threshold is specified. The true level will normally be used only when it is required to recover data of very low amplitude.

3.7.5 LOAD AND ON-LINE (ILOL) (OPTIONAL)

When used with T6000 and T8000A series transports this pulse, when true, enables a remote Load sequence. A second pulse on this line, spaced a minimum of 1 second from the initial pulse, causes the transport to be placed On-line. This line is not applicable for T9000 series transports.

This line is routed through the formatter to the buffered formatter transport interface.

3.7.6 REWIND COMMAND (IREW)

This is a pulse which causes the Selected and On-line transport to rewind to the Load Point. This pulse is routed directly to the transport and does not cause the formatter to become busy.

3.7.7 OFF-LINE COMMAND (IOFL)

This is a pulse which, when true, causes the selected transport to revert to the Off-line mode. This pulse is routed directly to the transport and does not cause the formatter to go busy.

3.7.8 FORMATTER ENABLE (IFEN)

This is a level which, when false, causes the formatter to revert to the quiescent state. This signal is not gated by IFAD (Paragraph 3.7.1); hence, the formatter connected to the interface will reset upon receipt of IFEN going false.

This line may be used to disable the formatter if the controller power is low, or to clear the formatter logic in the case of illegal commands or unusual conditions.

3.7.9 WRITE DATA LINES (IW0 - IW7, IWP)

These 8 lines (9 in the case of external parity option) transmit write data from the buffer to the formatter. In each case, IW7 corresponds to the least significant bit of the character.

3.8 INTERNAL INTERFACE — FORMATTER TO BUFFER

All waveform names are chosen to correspond to the logical true condition. All lines are low-true at the internal interface with the true level 0v and the false level + 3v.

All pulse widths at the interface must be a minimum of 1 μsec wide.

3.8.1 FORMATTER BUSY (IFBY)

This is a level which is set true on the trailing edge of an IGO command when any command is issued to the formatter. It remains true until tape motion ceases after the execution of the command.

3.8.2 DATA BUSY (IDBY)

This is a level which goes true when the tape on the selected transport has reached operating speed, traversed the IBG, and the formatter is about to look for a read signal from the tape.

IDBY remains true until data transfer is completed and the appropriate post-record delay is completed. IDBY goes false as the capstan starts to decelerate the tape.

3.8.3 IDENTIFICATION (IDENT)

This is a level which is set true to identify PE tapes. When reading forward off of the BOT, the formatter inspects the parity channel for the presence or absence of the identification burst which distinguishes PE tapes. If an identification burst is detected this line is set true for a short period as the BOT tab passes over the read head.

3.8.4 HARD ERROR (IHER)

This is a pulse or level which, when true, indicates that an uncorrectable read error has been detected by the formatter. This line is active during Read Forward, Read Reverse, and Read-After-Write (dual stack head) operation if one or more of the following occur.

(1) False preamble detection.

(2) False postamble detection.

(3) Multi-channel dropout.

(4) Parity error without associated channel dropout.

The formatter IHER line is presented only to the buffer interface.

3.8.5 CORRECTED ERROR (ICER)

This is a pulse which indicates that a single track dropout has been detected and that the formatter is performing error correction.

NOTE

When performing a Read-After-Write operation, the record should be rewritten if either a IHER or ICER error is detected.

3.8.6 FILE MARK (IFMK)

This is a pulse which indicates that the formatter read logic has detected a file mark. This may be during any read forward or read reverse operation or during a write file mark operation for a read-after-write transport.

3.8.7 READY (IRDY)

This is a level which is true only when the transport is ready to receive external commands. The following conditions must exist.

(1) All interlocks are made.

(2) Initial Load or Rewind sequence is complete.

(3) Transport is On-line.

(4) Transport is not rewinding.

3.8.8 ON-LINE (IONL)

This is a level which, when true, indicates that the selected transport is under remote control. This level is false when the transport is Off-line and cannot be operated remotely.

3.8.9 REWINDING (IRWD)

This is a level which is true when the selected transport is engaged in a rewind operation.

3.8.10 FILE PROTECT (IFPT)

This is a level which is true when the transport power is on, and a reel of tape without a write enable ring is mounted on the transport.

3.8.11 LOAD POINT (ILDP)

This is a level which is true when the BOT tab is located under the photo-tab sensor, interlocks are made, and the initial Load or Rewind sequence is completed in the selected transport. The ILDP level goes false when the tab leaves the photo-tab sensor.

3.8.12 END OF TAPE (IEOT)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor in the selected transport. This level is unstaticised, and transitions to and from the true state are not clean.

3.8.13 TRANSPORT FORMAT (INRZ)

This is an optional line which is employed in systems utilizing a mixture of PE and NRZI transports. When true, the levels indicate that the selected transport is of the NRZI type. When false, this level indicates that the selected transport is of the PE type.

When the level on this line is true, the command lines of a PE formatter are disabled. When the level is false, the command lines of a NRZI formatter are disabled.

3.8.14 TRACK CONFIGURATION (I7TRK)

This optional line is employed in systems utilizing a mixture of 7- and 9-channel transports. When true, this level indicates that a 7-channel transport has been selected. When false, this level indicates that a 9-channel transport has been selected.

3.8.15 HEAD CONFIGURATION (ISINGLE)

This is an optional line employed in systems utilizing mixed transports. When true, the level indicates that the selected transport has a single stack read/write head. When false, the level indicates that the selected transport has a dual stack read-after-write head.

The levels on this line condition the formatter to generate appropriate delays for the generation of the IRG and for head positioning.

3.8.16 TAPE SPEED (ISPEED)

This is an optional line which is used when it is desired to attach transports of two different tape speeds to a formatter.

When false, this line indicates the selected transport is high speed; when true, it indicates the selected transport is low speed.

3.8.17 WRITE STROBE (IWSTR)

The signals on this line consist of a pulse for each data character to be written on tape. IWSTR samples the write data lines IW0 - IW7 from the buffer and copies this information character-by-character into the formatter write logic.

3.8.18 READ STROBE (IRSTR)

The signals on this line consist of a pulse for each character of read information to be transmitted to the buffer and are used to sample the read data lines IR0 - IR7.

Individual IRSTR pulses will generally be equally spaced, although some variation may be present due to skew and bit crowding effects.

3.8.19 READ DATA LINES (IRP, IR0 - IR7)

These 8 lines are employed to transmit read data from the formatter to the buffer. Each character read from tape is sampled by IRSTR and strobed into the buffer.

3.9 INTERFACE OUTPUTS (BUFFERED FORMATTER TO TRANSPORT)

All waveform names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the true level 0v and the false level + 3v.

All pulse widths at the interface must be a minimum of 1 μsec wide.

3.9.1 WRITE DATA STROBE (IWDS)

This is a pulse with a frequency twice the frequency of the data transfer rate. The trailing edge of IWDS is utilized to copy the PE data appearing on IWDP, IWD0 - IWD7 into the selected transport write logic. The formatter logic holds the IWDP, IWD0 - IWD7 lines steady for the duration of IWDS.

3.9.2 WRITE AMPLIFIER RESET (IWARS)

A pulse immediately following the last character of the postamble is generated during all write operations. When in the Edit mode this pulse is utilized to control the early turn-off of write current in the selected transport.

3.9.3 READ THRESHOLD 1 (IRTH1)

The level on this line is the output of a flip-flop within the formatter which stores the condition of IRTH1 specified in the last command.

When this level is true, and the selected transport has a single stack head, the read electronics of the transport are conditioned to operate in the high Read Threshold mode. When false, the transport reverts to the normal Read Threshold.

3.9.4 READ THRESHOLD 2 (IRTH2)

The level on this line is the output of a flip-flop within the formatter which stores the condition of IRTH2 specified in the last command.

The output on this line is used only by those transports which have an extra low read threshold capability. When this level is true, the read electronics of the selected transport are conditioned to operate in the extra low Read Threshold mode. When false, the transport reverts to the normal Read Threshold.

3.9.5 WRITE DATA (IWDP, IWD0 - IWD7)

These 9 lines are utilized to transfer the PE data from the formatter to the selected transport. The information is copied on the trailing edge of each IWDS pulse into the selected transport write logic and written directly onto tape.

3.9.6 OVERWRITE (IOVW)

This is a level which, when true, causes special action in the write electronics of the selected transport to facilitate the editing of tapes. The line is the output of a flip-flop in the formatter logic which stores the condition IEDIT as specified in the last command.

3.9.7 SYNCHRONOUS FORWARD COMMAND (ISFC)

This is a level which, when true and the selected transport is Ready and On-line, causes the tape to move in the forward direction at the specified speed. When the level goes false, the tape decelerates to rest.

3.9.8 SYNCHRONOUS REVERSE COMMAND (ISRC)

This is a level which, when true and the selected transport is Ready and On-line, causes the tape to move in the reverse direction at the specified speed. When the level goes false, the tape decelerates to rest.

3.9.9 REWIND COMMAND (IRWC)

This is a pulse which, if the selected transport is Ready and On-line, causes the transport to rewind to BOT. The IRWC pulse is generated within the formatter by gating IREW with IFAD.

3.9.10 SET WRITE STATUS (ISWS)

The level on this line is the output of a flip-flop within the formatter which identifies the read/write status specified in the last command. The level on this line controls the selected transports' read/write electronics. Setting this level true causes the selected transport to enter the Write mode of operation. When the level on this line is false, the selected transport will enter the Read mode of operation.

Irrespective of the state of this line, the transport will be forced into the Read mode of operation under any one of the following conditions.

(1) An IRWC or IOFC is received.

(2) Interlock is lost.

(3) Transport is switched to the Off-line mode.

3.9.11 OFF-LINE COMMAND (IOFC)

This is a pulse which places the selected transport under local control. The IOFC pulse is generated by gating IOFL with IFAD. An OFF-LINE command can be given while a rewind is in progress provided IOFC is separated by at least 1 μsec from IRWC.

3.9.12 TRANSPORT SELECT LINES (ISLT0, 1, 2, 3)

The levels on these four lines are utilized to select one transport from the possible four. The levels are generated in the formatter by decoding address lines ITAD0 and ITAD1. Only one line can be true at a time. When formatter is not selected, transport 0 (ISLT0) is always selected.

When a transport is selected, all interface lines to and from the transport are activated and the transport is connected to the formatter.

3.10 INTERFACE INPUTS (TRANSPORT TO BUFFERED FORMATTER)

Waveform names correspond to the logical true condition. All interface lines are low-true at the interface with the true level 0v and the false level +3v.

All pulse widths at the interface must be a minimum of 1 μsec wide.

A disconnected interface line is interpreted as a logical false signal by the formatter logic.

3.10.1 READ DATA LINES (IRDP, IRD0 - IRD7)

These 9 read data lines are employed to transmit read data from the selected transport to the formatter. They are the outputs of 9 peak detectors, individually gated with the output of a threshold detector associated with each channel. The read signals are replicas of the PE waveforms used to drive the write amplifiers.

3.10.2 TRANSPORT FORMAT (INRZ)

This is an optional line which is employed in systems utilizing a mixture of PE and NRZI transports. When true, the level indicates that the selected transport is of the NRZI type; when false, this level indicates that the selected transport is of the PE type.

3.10.3 SINGLE/DUAL (ISGL) (HEAD CONFIGURATION) (OPTIONAL)

This is an optional line employed in systems utilizing mixed transports. When true, the level indicates that the selected transport has a single stack read/write head. When false, the level indicates that the selected transport has a dual stack read-after-write head.

The levels on this line condition the formatter to generate appropriate delays for the generation of the IRG and for head positioning.

3.10.4 SPEED (ISPEED) (TAPE SPEED) (OPTIONAL)

This is an optional line which is used when it is desired to attach transports of two different tape speeds to a formatter. When false, this line indicates the selected transport is high speed; when true, it indicates the selected transport is low speed.

This line controls a dual speed oscillator in the formatter logic which scales all formatter timing according to the tape speed.

3.10.5 ON-LINE (IONL)

This is a level which, when true, indicates that the selected transport is under remote control. This level is false when the transport is Off-line and cannot be operated remotely.

3.10.6 REWINDING (IRWD)

This is a level which is true when the selected transport is engaged in a rewind operation.

3.10.7 FILE PROTECT (IFPT)

This is a level which is true when the transport power is on, and a reel of tape without a write enable ring is mounted on the transport.

3.10.8 LOAD POINT (ILDP)

This is a level which is true when the BOT tab is located under the photo-tab sensor, interlocks are made, and the initial Load or Rewind sequence is completed. The ILDP level goes false when the tab leaves the photo-tab sensor.

3.10.9 END OF TAPE (IEOT)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor. This level is unstaticised, and transitions to and from the true state are not clean.

3.11 INTERNAL INTERFACE — FORMATTER TO FORMATTER

3.11.1 REVERSE/FORWARD (IREV)

The Reverse/Forward internal interface signal is used between the PE Write PCBA and the PE Read PCBA to signify the direction of the tape motion command.

This signal causes the data to be either inverted or not depending on whether the tape is moving forward or reverse direction.

3.11.2 READ GATE (IRGATE)

The READ GATE internal interface signal is used to enable the PE read recovery logic when reading a PE data record.

3.11.3 TEST ID (ITESTID)

An internal interface signal between the PE Write PCBA and PE Read PCBA that enables the test for PE identification. This signal is delayed from initial tape motion from BOT.

3.11.4 IDENTIFICATION GATE (IDG)

An internal interface signal between the PE Write PCBA and the PE Read PCBA that enables the read logic to test for the identification burst.

3.11.5 READ END (IREND)

The READ END signal is used between the PE Read PCBA and the PE Write PCBA to signify the end of data transfer from tape to formatter.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section describes the basic organization and operation of the Buffered PE Formatter. The formatter consists of the following major components.

(1) Basic chassis and chassis hardware
(2) Interconnect C Motherboard
(3) Power Supply Subassembly
(4) Buffer Assembly
(5) PE Write PCBA
(6) PE Read PCBA
(7) I/O cables and connector boards

The physical relationships of these major assemblies are illustrated in Figure 4-1.

4.2 ORGANIZATION OF THE FORMATTER

A highly modularized construction technique has been adopted with all major subassemblies and logic components interconnected by means of connectors mounted on a motherboard rather than the more conventional wiring techniques.

The PE Write PCBA, PE Read PCBA , and the Buffer PCBA contain all of the logic required to perform the various formatter and buffering functions listed in Table 3-1.

Each PCBA consists of a 14 X 16-1/2 inch processed board which mates to the Interconnect C Motherboard via two 100-pin edge connectors. The Read PCBA mounts in the top slot of the chassis assembly, mating with J1 and J2 of the motherboard. The Write PCBA mounts in the middle slot of the chassis assembly and mates with J4 and J3 of the motherboard. The Buffer PCBA mounts in the bottom slot of the chassis assembly, mating with J5 and J6 of the motherboard.

4.2.1 INTERCONNECT C MOTHERBOARD

The Interconnect C Motherboard, shown in Figure 4-2 (reference Schematic No. 103310), provides for the electrical connection between the three PCBAs and for the electrical interface to the customer, i.e., an interface to the customer's controller and an interface to the tape transports. Connection to the controller is made from motherboard socket J6 via J104. An Interface C board is provided to which the customer's controller interface can be wired. The relationship of the Interface C board and the motherboard is shown in Figure 4-1. Refer to Table 2-2 for Buffered Formatter/Controller interface pin identification which is used when wiring the Interface C board.

Similarly, the motherboard sockets associated with the transport interface (J2 and J4) are daisy-chained together and routed to edge connector J102. Connection between the formatter and the transport(s) is made by use of the Cable A assembly (or MTA Cable A assembly) which is shipped with the formatter.

NOTE

Pins on the 100-pin connectors are numbered A1 through A50, and B1 through B50, where pin A1 is opposite B1, etc. Due to the topology of the motherboard, pin connections on the four external interface connectors are reversed at the PCBA connectors.

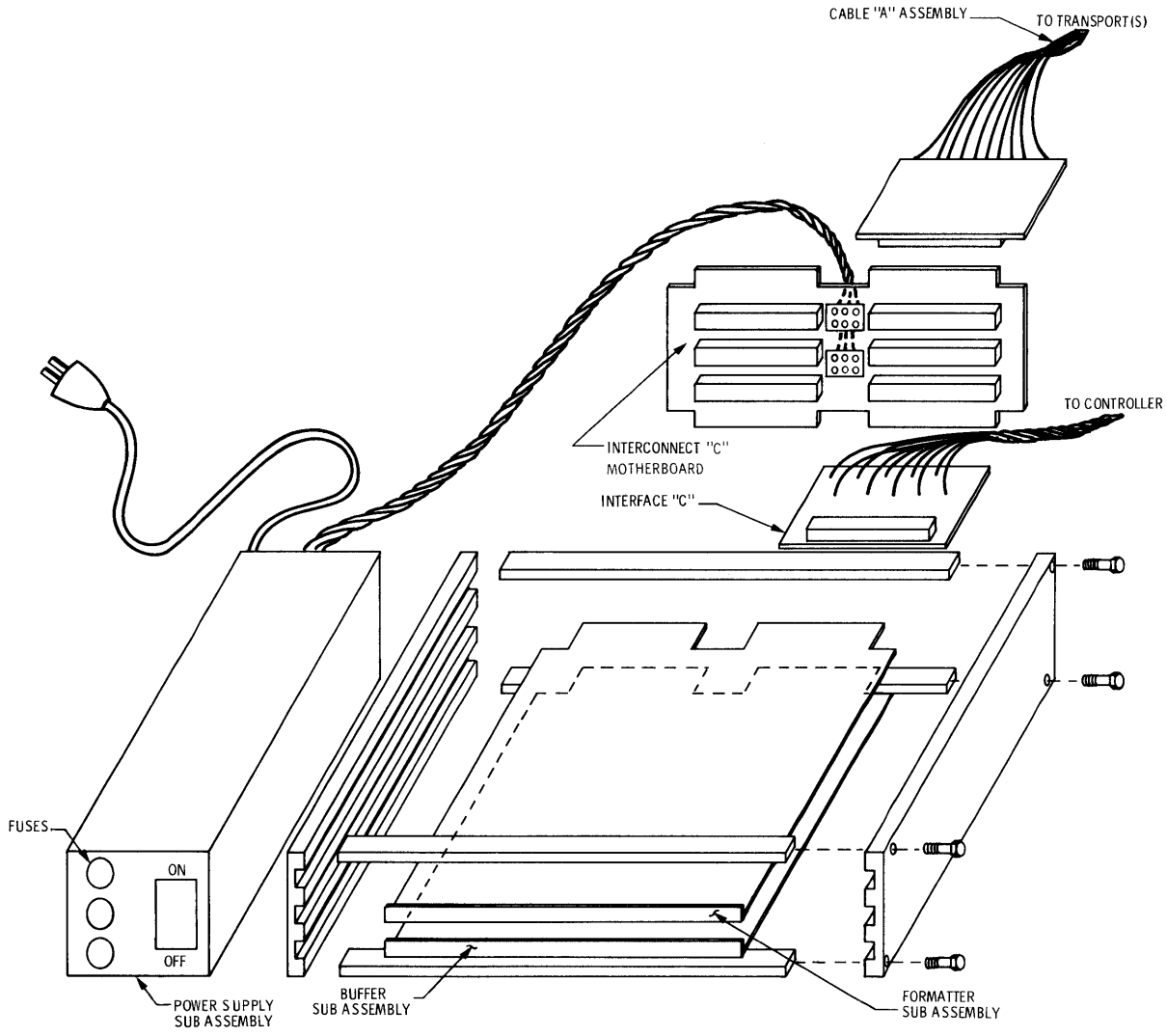


Figure 4-1. Relationship of Major Buffered Formatter Assemblies

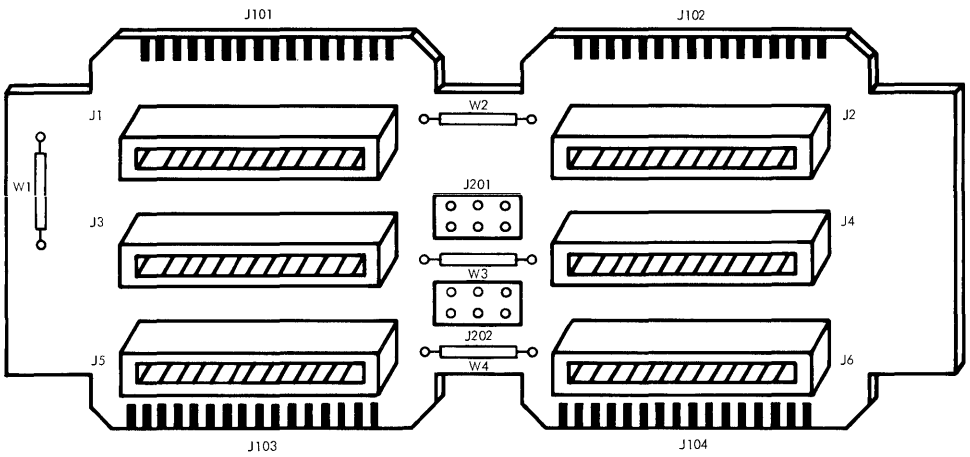


Figure 4-2. Interconnect C Motherboard

When making external connections, refer to Table 2-1 (transport interface). Definitions of the interface signals are contained in Section III.

It should be noted that the Interconnect C Motherboard does not have the etched interconnections between J4 and J6. The controller interfaces to the formatter PCBAs via J104.

DC power is delivered from the Power Supply Subassembly to the motherboard via connectors J201 and J202. The motherboard distributes power to each of the PCBA card slots through connectors J1 through J6.

4.2.2 POWER SUPPLY

Figure 4-3 is a block diagram of the power supply which is located along the left side of the main assembly. The transformer, fuses, rectifiers, and power cord, etc., are fastened directly to the power supply subassembly. The regulators, overcurrent detectors, overvoltage detectors, and the logic enable circuitry are located on a PCBA which is mounted on the power supply subassembly.

The power supply subassembly supplies +5v dc, +20v dc, and —5v dc, and a logic enable signal, PSEN, to the formatter logic. A switching regulator converts unregulated +15v to a +5v supply which is rated at 7 amps. A separate linear regulator converts unregulated +30v to a +19.5v supply which is rated at 1 amp. A linear regulator supplies —5v at 1 amp (maximum) to the buffer sense amplifiers.

NOTE

An overload condition will cause the +5v, +20v, or —5v supplies to be removed from their loads by the overcurrent detector. To reset the detector, ac power must be shut off for approximately 10 seconds.

The formatter logic is protected from excessive voltage by an overvoltage detector which shuts down the regulator if the supply voltage exceeds +7.5v on the +5v supply, or +22v on the +20v supply, or —7.5v on the —5v supply.

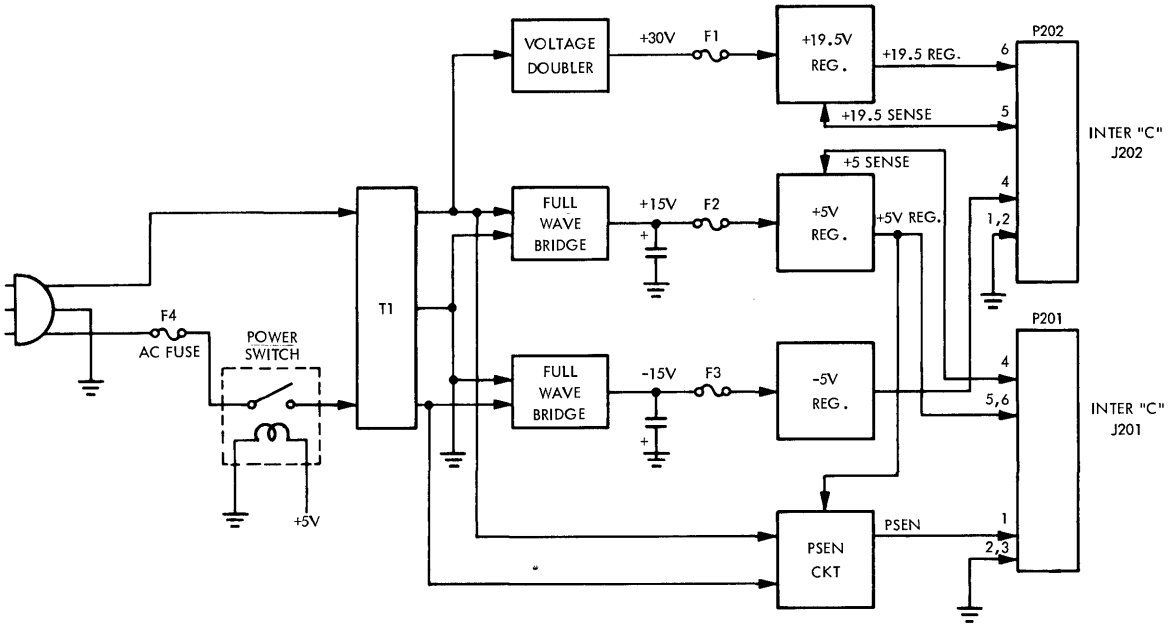


Figure 4-3. Power Supply Block Diagram

A reset signal, PSEN, is generated in the power supply and is used to clamp all formatter logic to the quiescent state while dc power is being established after switch-on. Similarly, when ac power is lost, PSEN clamps the formatter logic before there is a significant decay in the +5v supply, and prevents the writing or reading of spurious signals.

4.2.3 SYSTEM ORGANIZATION

Figure 4-4 is a diagram of the basic organization of the PE Formatter; Figure 4-5 is a diagram of the total Buffered PE Formatter system.

Two or three major logic assemblies are used in the Buffered PE Formatter. These are the PE Write PCBA, PE Read PCBA, and the Buffer PCBA. It is important to note that the addition of the Buffer assembly to the basic PE Formatter creates the Buffered Formatter. This is evident when Figures 4-4 and 4-5 are compared.

The descriptions contained in the following paragraphs describe the logic functions of each circuit board with direct reference made to internal interface between boards. This is done because the PE Write and the PE Read PCBA can operate alone as a PE Formatter without buffering, but the buffer assembly must be used in conjunction with the PE PCBAs to fulfill the requirements of the Buffered PE Formatter system.

4.2.4 BUFFER PCBA

The Buffer PCBA, in conjunction with the PE Write and PE Read PCBAs, performs the functions of a Buffered PE Formatter system. The following description of buffer operation is referenced to the logical discussion of the PE Write PCBA and PE Read PCBA.

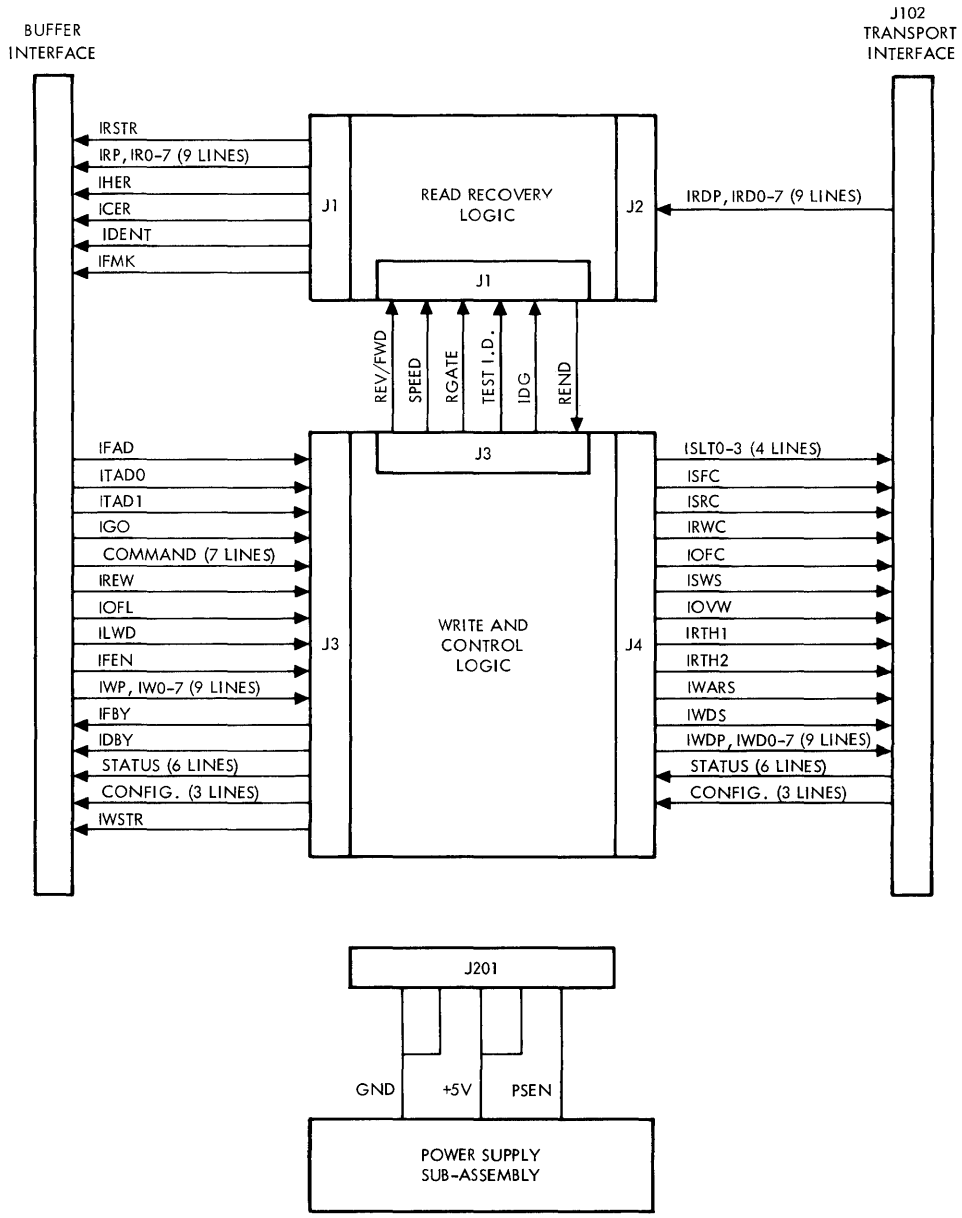


Figure 4-4. PE Formatter Logic Organization

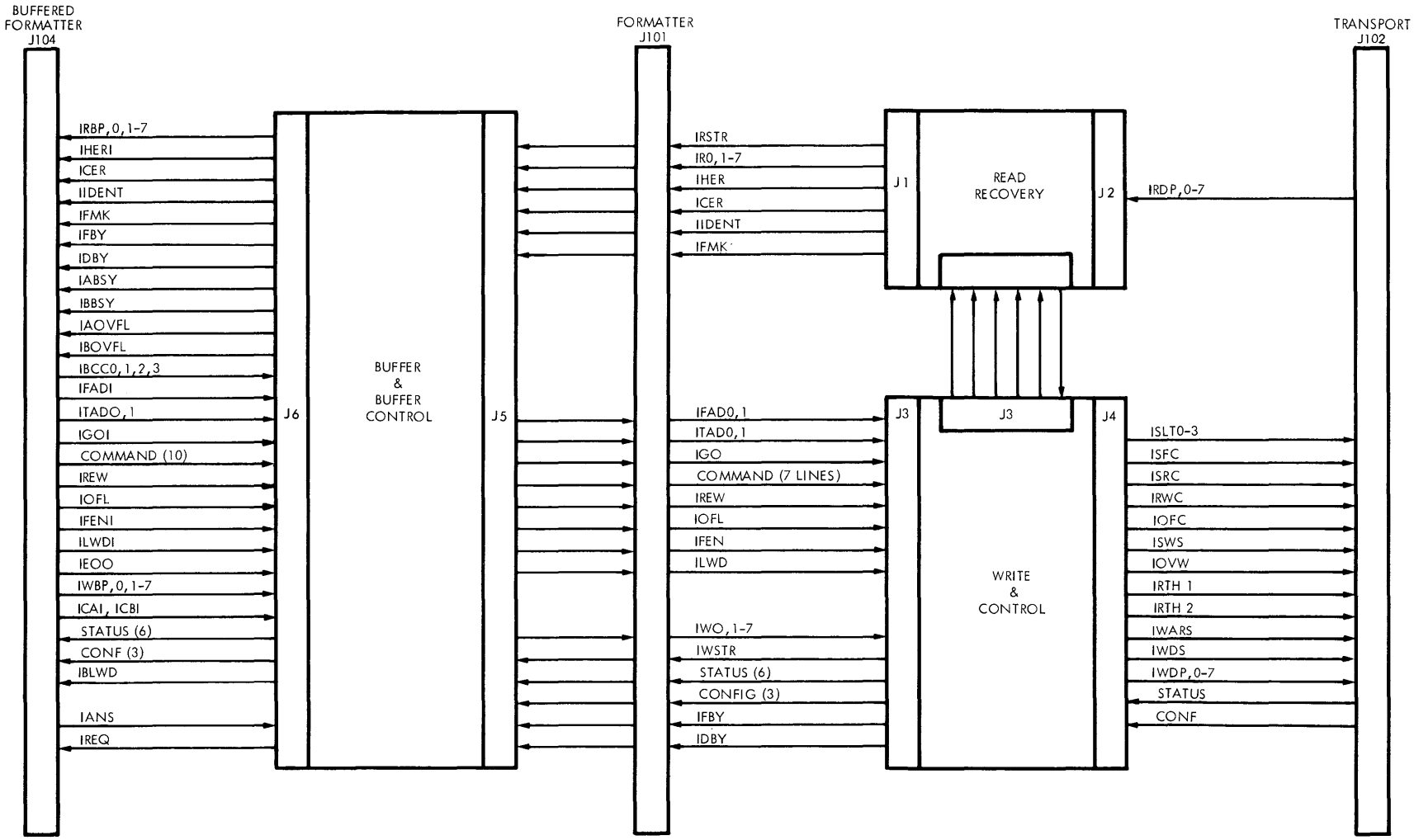


Figure 4-5. Buffered PE Formatter Logic Organization

The Buffer PCBA contains 165 integrated circuits (ICs), dependent on buffer size, employed in making a Buffered PE Formatter and in other buffered formatter applications. It contains the logic necessary to accept asynchronous data from the customer at any rate up to 750 kHz, provide buffer lengths to 4096 nine-bit characters, and pass these data on to the companion tape formatter at the synchronous rate of the addressed peripheral.

The Buffer PCBA is composed of five basic sections.

(1) Command register and command decoding circuitry.

(2) Memory (up to 4096 X 9).

(3) Data routing logic which controls data flow in and out of the buffer memory.

(4) Data reference counters that serve as end of memory reference and last valid data byte in memory reference.

(5) Control logic.

All buffer timing is controlled by a single fixed frequency (12 MHz) crystal oscillator. This single fixed frequency enables the internal buffer logic to be entirely synchronous.

Figure 4-6* is a simplified block diagram depicting the buffer organization and should be referenced for the following discussion.

4.2.4.1 Command Decoding

The buffer is capable of performing 18 different types of commands. These commands are listed in Table 3-1 and can be divided into four distinctive groups.

(1) Group 1 — Controller/Buffer Commands.

Two commands (Table 3-1, items 13 and 14) comprise this group. These commands involve asynchronous communication between the buffer and the controller and can be performed in either the Split or Single Buffer mode. The Write Buffer and Read Buffer from Controller commands can be performed simultaneously with a command in Group 2 when the buffer is split.

Paragraph 4.2.4.5 details the logic operation specified by the Group 1 commands.

(2) Group 2 — Buffer/Formatter Commands.

These commands (Table 3-1, items 1 through 5) involve synchronous communication between the buffer and the selected tape formatter. The commands in this group are the basic Read Tape and Write Tape commands. They are performed synchronously with the selected formatter through the use of the relevant IRSTR (Read Strobe) or IWSTR (Write Strobe). Commands in this group can be performed simultaneously with a command from Group 1 when the buffer is split.

Paragraph 4.2.4.6 details the logic operation specified by the Group 2 commands.

(3) Group 3 — Automatic Controller/Formatter Commands.

This group is comprised for four commands (Table 3-1, items 15 through 18). The commands involve the automatic transfer of data between formatter and controller. They are basically a sequence of two commands; one from Group 1 and the other from Group 2. The two automatic commands are performed when the buffer is configured as a single buffer. The two automatic continuous commands are basically the same except that the buffer is now split. A substantial through-put rate can be obtained in this mode. When operating in any of the automatic data transfer modes the Buffered Formatter is operating

*Foldout drawing, see end of this section.

in either an asynchronous load/synchronous Write mode, or a synchronous load/asynchronous Read mode.

These commands are executed with the coding listed in Table 3-1 and the command strobe pulse. They are terminated through the use of the IEOO (End of Operation) control line.

Paragraph 4.2.4.7 details the logic operation specified by the Group 3 commands.

(4) Group 4 — Controller/Formatter Commands.

These commands (Table 3-1, items 6 through 12) are controller to formatter commands that do not use the buffer control logic. The buffer monitors the operations specified and reports all error and status information to the controller. When Group 4 commands are being performed, the controller may still use the buffer for Group 1 commands, i.e., controller/buffer operations. The controller must wait for IFBY (Formatter Busy) interface line to go false before trying to initiate any Group 2 or Group 3 formatter commands.

Paragraph 4.2.4.8 details the logic operation specified by the Group 4 commands.

To initiate a command, the command lines are set up according to Table 3-1 and the IGOI line is pulsed. If the command is destined for a tape unit, the controller must set up the address of the desired unit before initiating the command and must hold the address for the duration of the operation. The buffer has one internal command register that is selectively loaded and cleared as a function of the command type.

The information on a command line is copied and decoded within 500 nanoseconds of the trailing edge of the IGOI pulse. The following restrictions apply to the execution of subsequent commands from the controller.

(1) If the buffer is operating in the Split-Buffer mode the controller may set up a new command and generate the IGOI pulse. If the first command was from Group 1, then a second command from Group 2 (and vice versa) is permissible.

(2) If the first command was from Group 3, no other commands are permissible until the completion of the operation.

(3) If the first command was from Group 4, then only commands from Group 1 are permissible.

4.2.4.2 Basic Memory Elements

The basic memory element of the buffer is a 1024-bit dynamic random access memory. The memory elements are constructed on a single monolithic chip using MOS P-Channel techniques. Three high speed clocks are required for operation. These clocks and all other inputs to the memory are driven by special MOS level shifters.

The following example illustrates how the basic memory elements can be connected in series to obtain the desired buffer length.

- 9 chips: 1024 X 9 Buffer
- 18 chips: 2048 X 9 Buffer
- 36 chips: 4096 X 9 Buffer

Figure 4-7 is a functional diagram of the basic memory element used in the buffer.

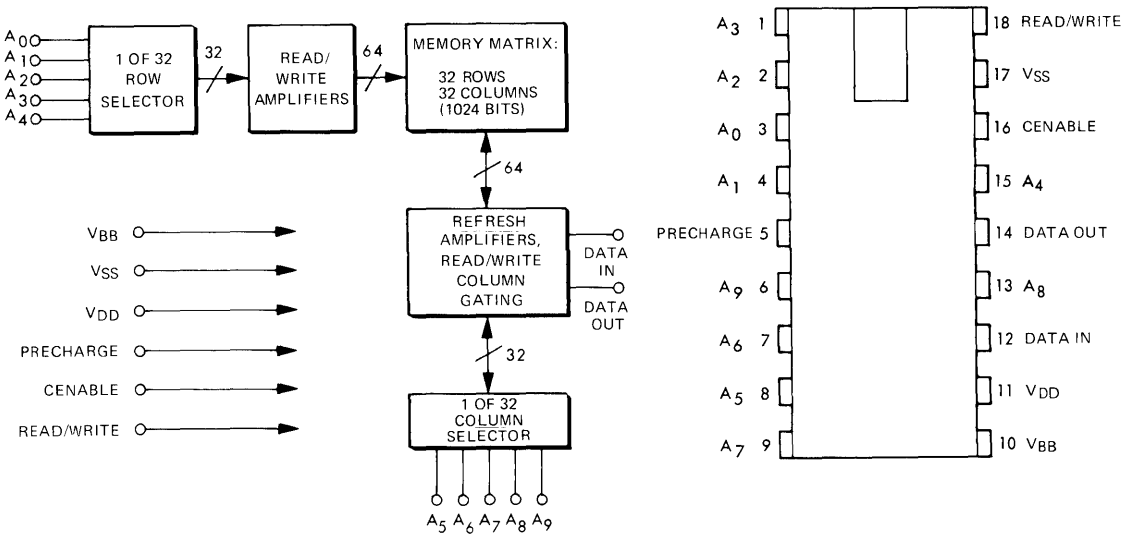


Figure 4-7. Basic Memory Element

4.2.4.3 Data Flow and Configuration Control

The basic data flow configuration lines and the basic manner in which data are referenced within the memory is described in the following paragraph. Figure 4-8 is a functional block diagram of the data flow through the buffer.

Data are presented to the buffer from either the controller or the selected tape formatter. If the buffer is split, data can be received from both sources simultaneously to opposite buffers. The input configuration control line IBCC0 determines these data paths (as shown in Figure 4-6). Configuration control line IBCC1 is used to split the buffer.

The output configuration control lines IBCC2, IBCC3 control the flow of data from the buffers to the two possible destinations. Data are transferred from the buffer by a read buffer command from Group 1, a write tape command from Group 2, or by the Group 3 automatic commands. IBCC2 directs the output of the buffers to the tape formatter write data inputs; IBCC3 directs the outputs of the buffers to the controller read data lines.

There are numerous data flow sequences which can be selected by discrete programming of configuration control lines IBCC0 - IBCC3. Figure 4-9 illustrates the data flow for these control lines and aids in tracking the data flow through the buffer for the desired configuration control. Two sources of data are represented: RT (Read Tape data information) and WB (Write Buffer data information). Two destinations are represented: WT (Write Tape data lines) and RB (Read Buffer data lines).

4.2.4.4 Reference Counter

When data are loaded into the buffer, a reference point must be established to identify the last valid data cell. Identical circuits are used for this purpose for each buffer half. The references are 13-bit circuits consisting of three 4-bit counter chips and a MSB flip-flop, three 4-bit parallel latches and a MSB flip-flop, and three 4-bit to 4-bit binary comparator chips and an exclusive OR gate. The B counter is preset as a function of the buffer length. Figure 4-10 is a simplified illustration of this preset condition.

Buffer overflow is determined by the MSB of the relevant counter length, dependent on buffer size. There are three overflow terms: ABOVFH (A Buffer Overflow), BBOVFH (B Buffer Overflow), and SBOVFH (Single Buffer Overflow). Figure 4-11 shows the relationship of the overflow terms to counter size.

When an operation is initiated (either loading or unloading the buffer) the reference counters increment once for each character transferred. When the operation is a load buffer (Write Buffer from Group 1 commands, or Read Tape from Group 2 commands) the counter increments for every character until the source of data gives an indication of the last data character to be loaded, i.e., ILWDI from the controller or IDBY from the read tape operation. At this time the state of the reference counter is loaded into a parallel latch giving the buffer a reference for the last valid data cell in memory. When this reference is latched, the control logic resets the counter to the preset condition unless the respective inhibit line is asserted (ICAI, ICBI).

For an unload buffer operation (Read Buffer to Controller from Group 1 commands, or Write Tape from Group 2 commands) the counter circuitry again increments once for every data byte transferred. Data are transferred until the reference counter compares to the latched counter that was set during the load buffer operation.

The comparison indicates that the buffer has reached the last valid data byte in memory and has transferred the contents of the record. At this time the buffer flags the condition to the user by setting Last Word (ILWD) to the formatter or Buffer Last Word (IBLWD) to the controller. When the transfer is complete the buffer control logic resets the counter to the preset state (Figure 4-10) if ICAI, ICBI are not asserted. Paragraphs 4.2.4.5 through 4.2.4.8 describe the logic flow of load buffer and unload buffer operations.

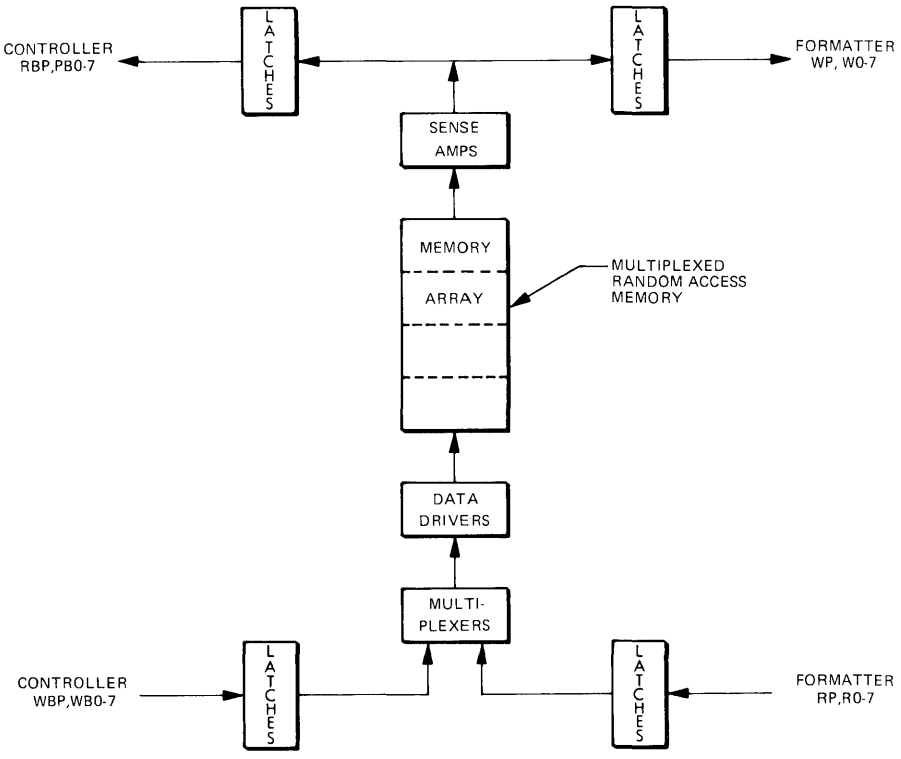
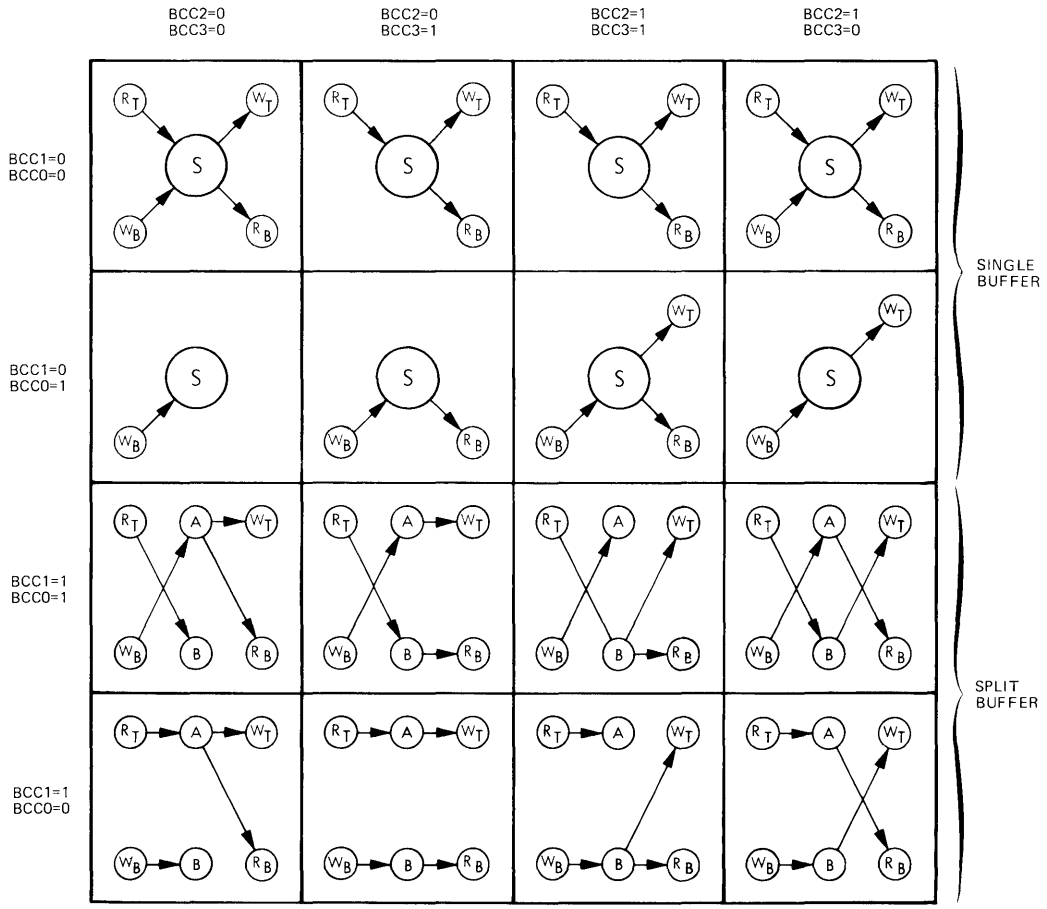


Figure 4-8. Basic Data Flow



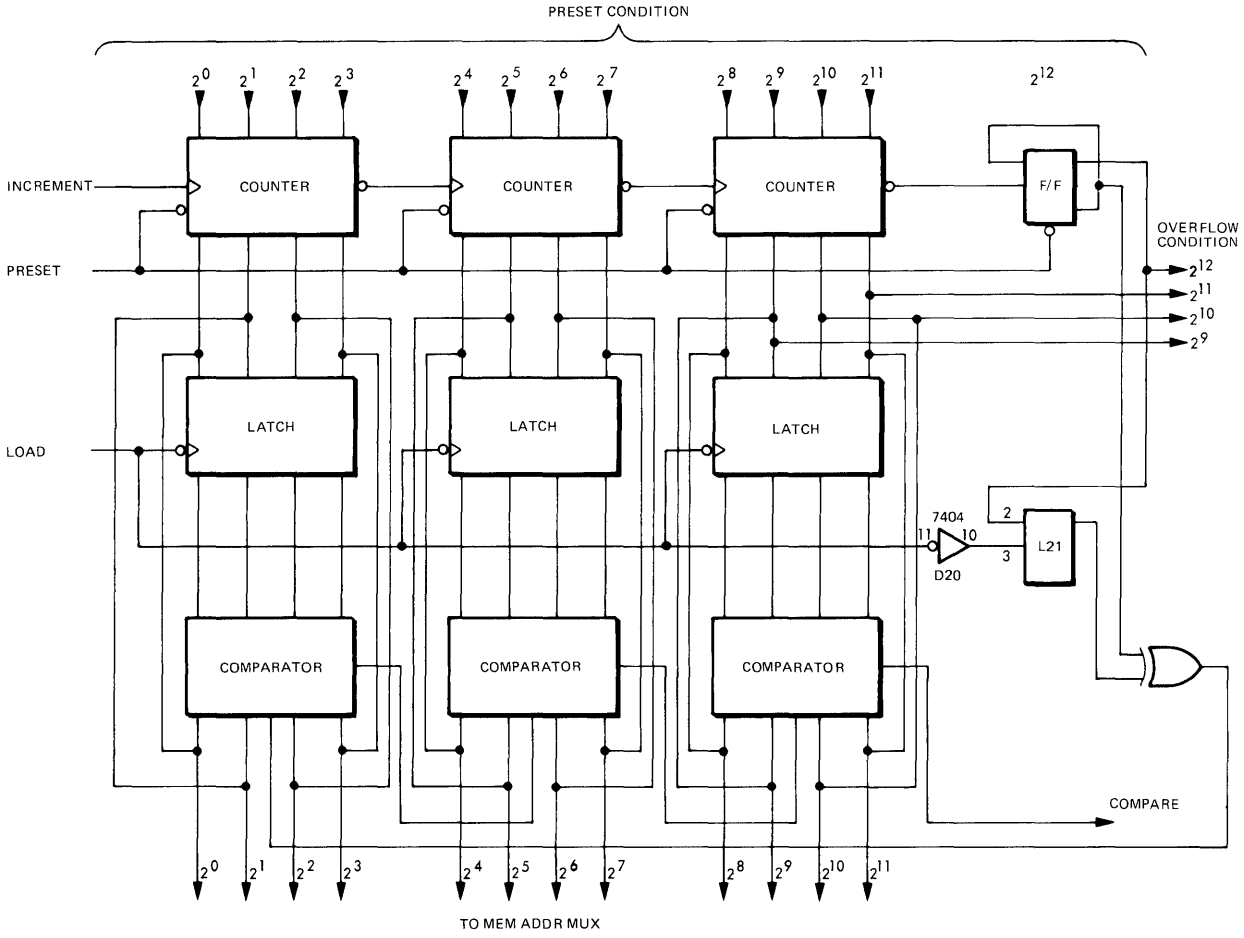
NOTE:

THE DIAGRAM SHOWN IN EACH STATE IS A PICTORIAL REPRESENTATION OF THE MEANINGFUL DATA FLOW FOR THE SPECIFIC STATE OF THE CONFIGURATION LINES.

LEGEND:

RT = READ TAPE
WT = WRITE TAPE
RB = READ BUFFER
WB = WRITE BUFFER
A = BUFFER A
B = BUFFER B
S = SINGLE BUFFER

Figure 4-9. Configuration Control



COUNTER POSITION	BUFFER CAPACITY							
	512		1024		2048		4096	
	A	B	A	B	A	B	A	B
2^0	0	0	0	0	0	0	0	0
2^1	0	0	0	0	0	0	0	0
2^2	0	0	0	0	0	0	0	0
2^3	0	0	0	0	0	0	0	0
2^4	0	0	0	0	0	0	0	0
2^5	0	0	0	0	0	0	0	0
2^6	0	0	0	0	0	0	0	0
2^7	0	0	0	0	0	0	0	0
2^8	0	1	0	0	0	0	0	0
2^9	0	0	0	1	0	0	0	0
2^{10}	0	0	0	0	0	1	0	0
2^{11}	0	0	0	0	0	0	0	1
2^{12}	0	0	0	0	0	0	0	0

Figure 4-10. Reference Counter Preset Conditions

BUFFER SIZE	OVERFLOW TERM		
	ABOVFH	BBOVFH	SBOVFH
512	2^8	2^8	2^9
1024	2^9	2^9	2^{10}
2048	2^{10}	2^{10}	2^{11}
4096	2^{11}	2^{11}	2^{12}

Figure 4-11. Overflow Conditions

4.2.4.5 Group 1 — Controller/Buffer Commands

Refer to Paragraph 4.2.4.1, Step (1), for definitions of the Group 1 commands. The two commands in this group (Write Buffer from Controller and Read Buffer to Controller) are truly asynchronous data transfer commands. The controller determines the transfer rate and the buffer limits the rate to a maximum of 750 kHz.

Figure 4-12 is a simplified timing diagram of the basic control of data during Group 1 Controller/Buffer commands and should be referred to for the following discussion.

The transfer of data between the controller and buffer is accomplished through a handshake circuit. Upon receipt of either Group 1 command, the buffer generates a request (IREQ) which indicates to the controller:

(1) If the command is a Write Buffer, the buffer is ready to accept the first data byte and, with each subsequent request, the buffer is ready for another data byte.

(2) If the command is a Read Buffer, the buffer has the first data byte ready and, with each subsequent request, another data byte.

The controller's answer (IANS) to this request sets the transfer rate and:

(1) Defines the time when the buffer should copy the data lines during a Write Buffer command.

(2) Acknowledges receipt of data from the buffer during a Read Buffer command.

The IREQ/IANS handshake continues until all data have been transferred for the particular record. The Write Buffer command is terminated by the ILWDI signal from the interface. The Read Buffer command is terminated by the internal signal COMPL which is the comparison of the relevant counter and latch circuits. At the end of the Read Buffer command the IBLWD line to the controller is pulsed.

The Read Buffer and Write Buffer Control sequences are generated by individual dedicated micro controllers. The command from the controller determines which sequence is to be performed.

Any length of record, up to the maximum length of the buffer, can be written by the preceding procedure. An attempt to write a record greater than the length of the buffer will be flagged as an overflow condition. The relevant overflow indication (IAOVFL, IBOVFL) will occur when the buffer is full, indicating that the next character will not be recorded. The controller should attempt at this time to reblock his data and rewrite the buffer. Certain automatic operations which prevent the loss of data and time are discussed later in this section.

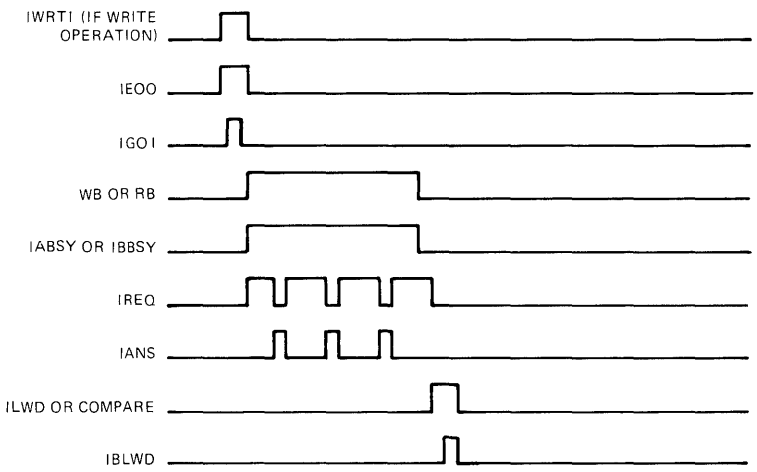


Figure 4-12. Controller/Buffer Commands

4.2.4.6 Group 2 — Buffer/Formatter Commands

The commands in the Group 2 Read Tape (Forward and Reverse) and Write Tape (Forward and Reverse) are the basic data flow commands between Buffer and Formatter. They are executed in much the same manner as the commands in Group 1 except that the transfer rate is determined by the tape transport. The buffer is capable of interfacing with all PERTEC PE Tape Transports from 6.25 ips (transfer rate of 1.25 kHz at 200 cpi) to 75 ips (60 kHz transfer rate at 800 cpi).

Figure 4-13 is a simplified timing diagram of the basic control of data during Group 2 Buffer/Formatter commands and should be referred to for the following discussion.

Upon receipt of any Group 2 command, the buffer goes busy and generates a tape formatter GO strobe. The response of the tape formatter to this strobe is described in detail in Paragraph 4.2.5 of this manual.

The execution of the commands from the buffer standpoint can be described basically as two commands, Write Tape or Read Tape, without regard to forward or reverse tape motion. If the command is a Write Tape command, the buffer generates a IGO strobe to the formatter and waits for write strobes (IWSTRs). Upon receipt of the first IWSTR (and each succeeding IWSTR) the buffer increments the appropriate reference counter and readies the next data byte from memory. The action continues at the synchronous rate of the tape transport until the end of the record contained in memory.

The end of record in memory is signaled by the NTLWD pulse; the occurrence of this pulse signifies that the reference counter state is equal to the reference latch state. From the discussion of Group 1 commands (Paragraph 4.2.4.5), it is recalled that the contents of the reference latch is the position of the last valid data cell in memory. Upon completion of the data transfer the relevant Buffer Busy drops and the counter is preset to its initial state.

If the command is a Read Tape command, the buffer generates an IGO strobe to the formatter and waits for read strobes (IRSTRs). Upon detection of the first IRSTR (and each

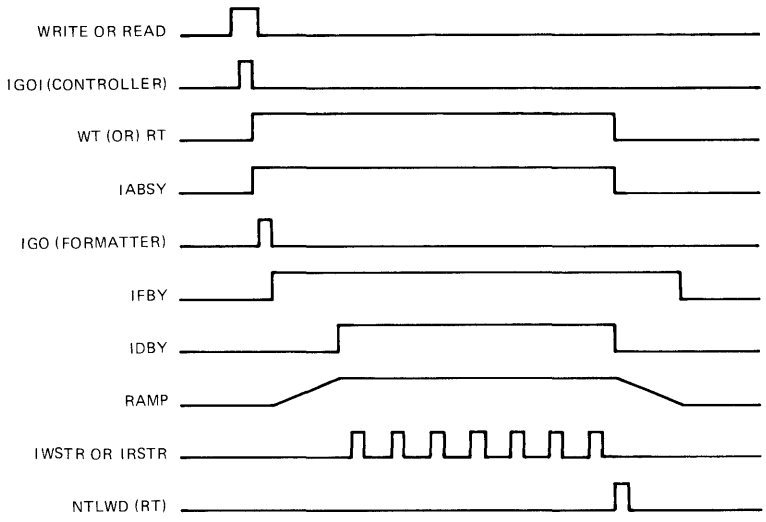


Figure 4-13. Buffer/Formatter Commands

succeeding IRSTR) the buffer copies the state of the input data lines (IRP, IR0 - IR7), increments its reference counter, and awaits the next read strobe. This process continues until the end of record is detected by the buffer (trailing edge of (IDBY) or a buffer overflow occurs internally.

Upon detection of the end of record, the relevant Buffer Busy signal drops and the counter is preset to its initial condition. If the controller attempts to load a record from tape greater in length than the buffer, the buffer will flag an overflow condition as soon as its last memory cell has been filled. There are certain buffer commands that allow the controller to read records from tape that are greater than the buffer length; they are described in Paragraph 4.2.4.7.

4.2.4.7 Group 3 — Automatic Commands

There are four automatic commands in Group 3. They entail the automatic transfer of data from formatter to controller and controller to formatter. These commands can be separated into two basic categories, Automatic Read and Automatic Write; each basic category uses a command type from Group 1 and Group 2. The Group 1 and Group 2 commands are performed automatically in sequence as follows.

(1) Automatic Write commands: Write Buffer, then Write Tape, etc.

(2) Automatic Read commands: Read Tape, then Read Buffer, etc.

This complete transfer is accomplished by the controller through a single command with the buffer generating the command and the IGO strobe for the second and all subsequent commands in the sequence. Both automatic commands can be performed continuously.

In the single-step or non-continuous mode of automatic transfer, the buffer is not split and single records less than or equal to the buffer length are automatically transferred through the buffer one at a time.

In the continuous mode of operation, the buffer is divided into two equal parts. For a continuous write command, data is transferred into the buffer at the desired rate. When one half of the buffer is full, the input data are automatically switched to the other half while the first half is automatically written onto tape. This mode of operation results in zero data loss. Maximum throughput can be configured by selection of buffer length and tape transport transfer rate as illustrated in Figure 4-14. For the continuous read operation, data is read from tape and loaded into the buffer. Data can be unloaded asynchronously from the first half of the buffer while the second half is being loaded from tape. The data transfer rate is determined by the user on a handshake basis. Unlimited block lengths can be transferred in these automatic continuous modes. Unblocked or extra long blocks of data on tape can be read successfully as long as the buffer is unloaded at a rate higher than the average system transfer rate.

In the automatic continuous modes, buffer input/output configuration control is determined by the buffer itself. The user has the option of splitting the buffer (IBCC1) to perform automatic continuous commands versus straight automatic commands.

Control for these commands is the same as for the individual commands that make up these automatic transfer operations. Input data are received via the same mechanisms that control the flow for the Group 1 and Group 2 commands.

4.2.4.8 Group 4 — Miscellaneous Commands

There are a number of commands that can be performed by the Buffered PE Formatter system that do not involve the buffer storage elements. These commands are decoded by the buffer and routed directly to the tape formatter for execution. These commands and their effect on formatter performance are as follows.

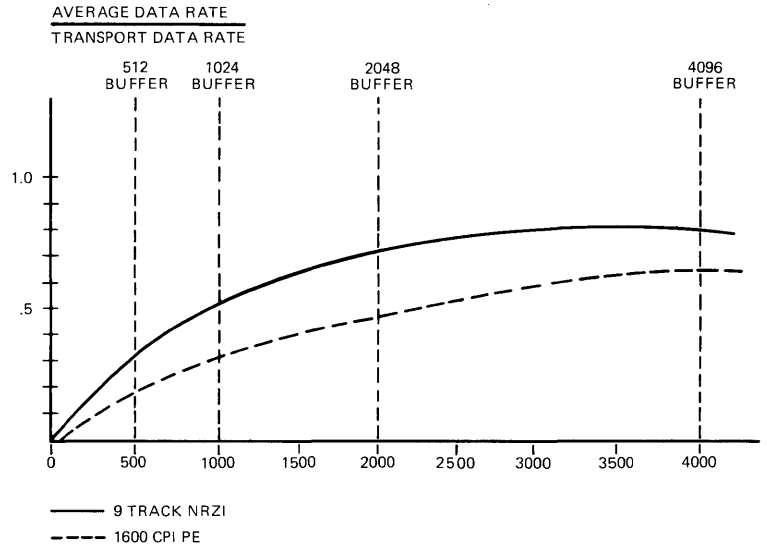


Figure 4-14. Buffered Formatter Transfer Function

(1) Backspace tape. Read reverse one record, buffer deactivated.

(2) Forward Space Tape. Read forward one record, buffer deactivated.

(3) File Search Forward. Read forward continuously, buffer deactivated, stop on file mark.

(4) File Search Reverse. Read reverse continuously, buffer deactivated, stop on file mark or BOT.

(5) Write File Mark. Write File Mark, buffer deactivated, file mark data generated by formatter.

(6) Erase Fixed Length. Dummy Write Tape, buffer deactivated, erase length of tape equal to file gap.

(7) Erase Variable Length. Dummy Write Tape, buffer deactivated, erase tape until length erased compares to length of previous record stored in the buffer.

In some cases the command coding specified in Table 3-1 differs from that required by the formatter for proper execution. The code conversion is performed by the buffer.

NOTE

When a command from Group 4 is being performed [Formatter Busy] only commands from Group 1 can be performed simultaneously; these are the commands described as Controller/Buffer type and entail transfer of data through the handshake circuit.

For a description of the logic operation of these miscellaneous commands, refer to the PE Formatter PCBA description in Paragraph 4.2.5.

4.2.4.9 Status, Configuration and Error Monitoring

There are a number of status, configuration and error monitoring signals and functions performed by the PE Formatter PCBA. These signals are routed through the Buffer PCBA and then sent to the controller.

Before issuing a tape command, the controller can address the particular peripheral in question and determine its type, configuration and readiness by reading these lines.

After issuing a tape command, numerous different error and status signals (IDENT, FMK, etc.) are generated by the formatter PCBA and routed to the controller via the Buffer PCBA. For a complete description of these signals, refer to the relevant group in Section III of this manual.

4.2.5 PE FORMATTER PCBAS

All logic necessary to perform the various formatter functions is contained on two IC logic assemblies; the PE Write PCBA and the PE Read PCBA.

The timing of all waveforms are controlled by an oscillator on each PCBA; on the Write PCBA it is a fixed frequency oscillator, on the Read PCBA it is a tracking oscillator.

The oscillator frequencies are initially adjusted according to tape speed. A simple change in oscillator frequency can therefore easily accommodate different tape speeds. Dual speed oscillators are available which allow transports of two different speeds to be attached to the same formatter.

The formatter logic must be conditioned according to the type of transport in use; this is accomplished by use of three configuration lines on the transport interface, as follows.

(1) INRZ. Distinguishes between NRZ and PE transports. This line must be held false when using the PE Formatter.

(2) ISINGLE. A true level indicates a single stack (read/write) transport; a false level indicates a dual stack (read-after-write) transport.

(3) ISPEED. For PE Formatters with a dual speed capability; this line selects one of two possible tape speeds.

When the formatter is dedicated to one type of transport the configuration lines are usually hardwired to the appropriate condition by jumper wires on the Formatter PCBAs.

Alternately, the configuration lines may be controlled by the output from the selected transport. This permits transports of different configurations to be daisy-chained onto the same formatter.

4.2.6 PE WRITE PCBA

The PE Write PCBA contains all logic necessary to perform all formatter functions except read recovery.

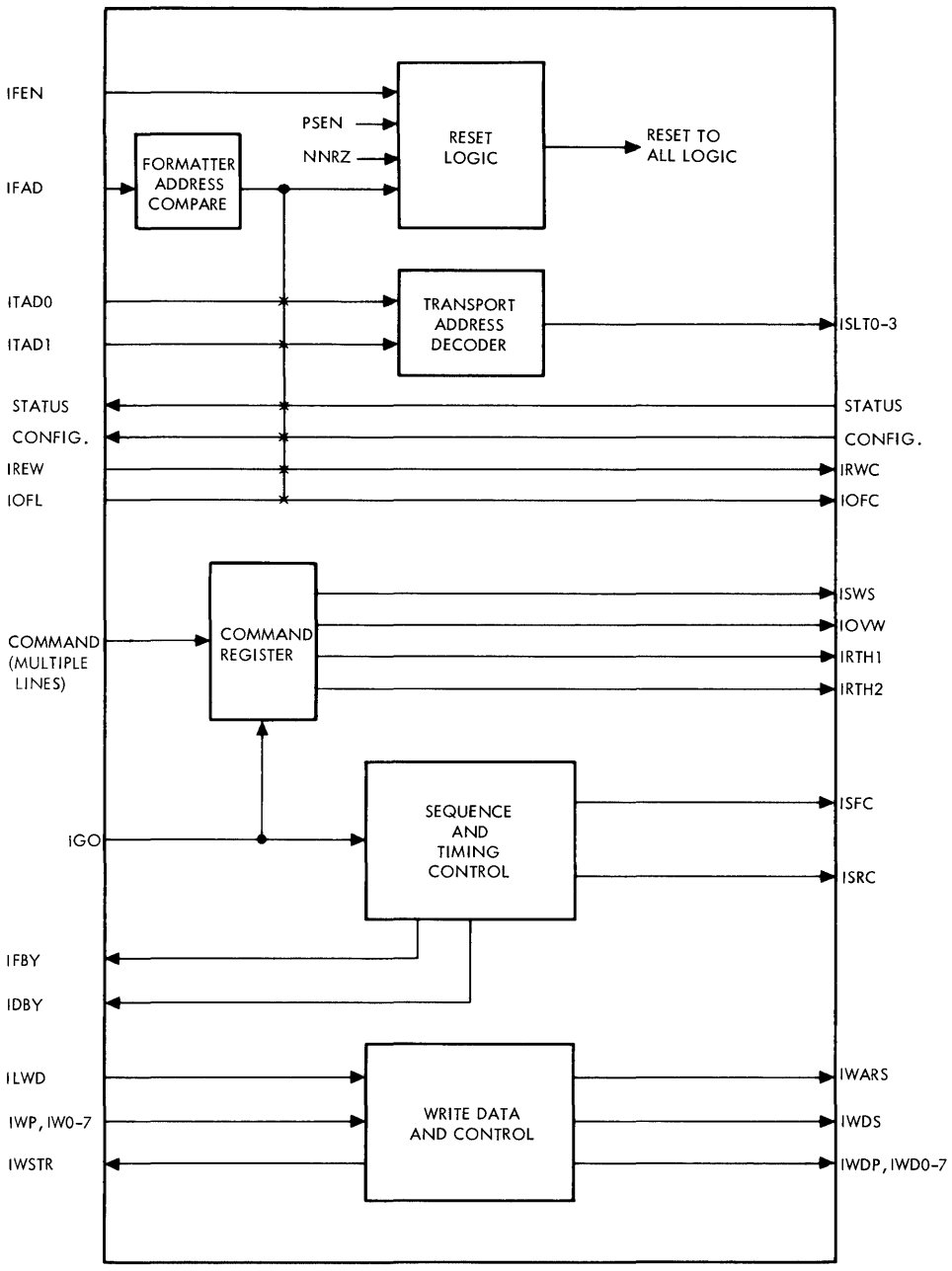
Formatter interface connections are illustrated in Figures 4-4 and 4-5. A simplified block diagram of the Write logic is shown in Figure 4-15 and should be referred to for the following discussion.

4.2.6.1 Control Logic

Performance of any formatter operation is dependent upon the formatter being selected by the controller. The formatter address is specified by the Formatter Address (IFAD) and a logic comparison is made against the position of an address switch on the PCBA. When a true comparison is made the formatter is connected to the buffer and controller interface.

When selected, the formatter will subsequently respond to controller commands provided no other reset condition exists. Transport address lines ITAD0 - ITAD1 are decoded and the selected transport is enabled. Status and configuration information from the selected transport will be routed to the controller via the formatter.

Note that REWIND and OFF-LINE commands (IREW and IOFL) are routed directly to the selected transport and are active any time the formatter is selected.



* INDICATES LINE IS GATED BY IFAD

Figure 4-15. Write Logic, Simplified Block Diagram

All other commands require that all inputs to the reset logic be true, i.e., the formatter is selected, power is established, no external reset from the controller is present, and the selected transport is compatible with the formatter.

To initiate a command, the command lines are set according to Table 3-1 and the IGOI line is pulsed. If no reset condition exists, the formatter is not busy, and the selected transport is ready, the command processed by the buffer is accepted by the formatter.

Information on the command lines will be copied and stored in a command register on the trailing edge of the IGO pulse from the buffer. FORMATTER BUSY (IFBY) will be set true and the formatter will begin the timing and sequencing required to execute the command.

At the end of a pre-record delay which allows the transport to ramp up to speed and traverse the IBG, DATA BUSY (IDBY) is set true and the read and/or write logic is activated. Data transfer will now occur between Controller/Buffered Formatter/Transport as specified by the command.

At the conclusion of the data transfer, a post-record delay is initiated which either assists in the generation of IBM-compatible gaps or optimizes head positioning within the gap. IDBY goes false at the end of the delay period and a stop command is given to the transport. IFBY will remain true while the transport is ramping down and will reset when the tape velocity reaches zero.

4.2.6.2 Command Separation

In most formatter applications it will be sufficient for the controller to inhibit execution of a new command until after the trailing edge of IFBY. This means that the transport will always ramp down to a halt between commands.

However, if maximum performance is required the formatter can be operated in the *On-The-Fly* mode. In this mode the controller is allowed to issue a new command any time after IDBY goes false provided the following conditions are met.

(1) The new command is in the same forward/reverse direction as the previous command. This ensures the integrity of the transport stop/start times and distance.

(2) The new command is in the same Read/Write mode as the previous one. This prevents the possibility of unerased areas of tape being left in the IBG.

The controller must furnish the logic necessary to detect the preceding conditions. *On-the-fly* operation results in a maximum time saving of one start/stop time per command (e.g., 30 msec per command at 12.5 ips).

4.2.6.3 Write Data and Control Logic

The write data and control logic on the PE Write PCBA controls the execution of all commands which involve the writing of data or erasing of data from tape, i.e., Write (normal), Write (edit), Write File Mark (IWFM), Erase (variable length) and Erase (fixed length).

Figure 4-16 illustrates the sequence of events in the execution of a typical write command. Note that the write logic is activated after tape has ramped up to speed and the correct IBG has been written.

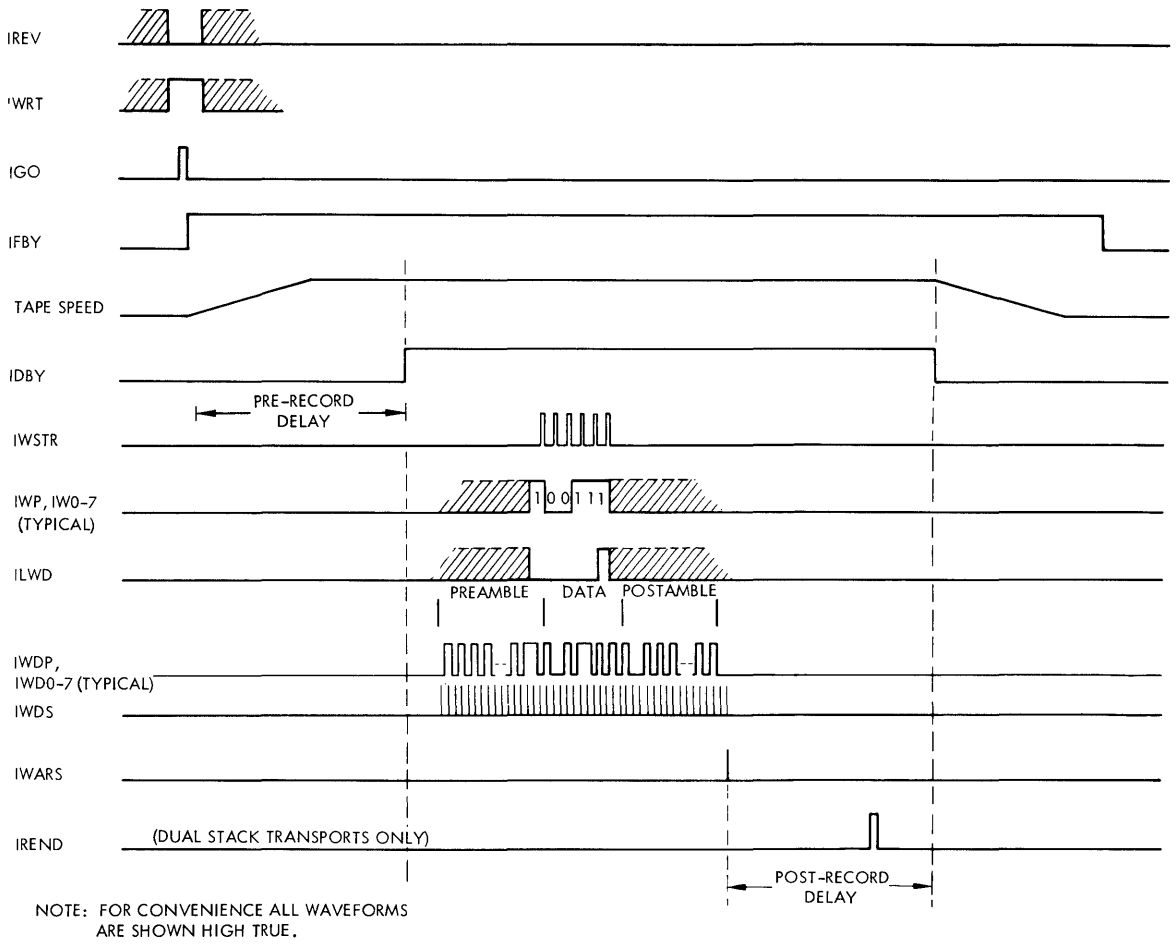


Figure 4-16. Phase Encoded Write Operation

4.2.6.4 Write (Norm), Write (Edit)

The Write (Norm) and Write (Edit) commands are executed in an identical manner by the write logic. In the case of a Write (Edit) operation the IEDIT command line is held true causing the IOVW flip-flop to set. Setting IOVW causes the write electronics in the selected transport to operate in the Edit mode.

When IDBY goes true (refer to Figure 4-16) the formatter write logic begins to generate a preamble data pattern consisting of four '0' bits followed by a '1' bit. This pattern is phase encoded, then written simultaneously onto the nine data channels on tape.

During the time period in which the last preamble bit (1) is being recorded, an IWSTR pulse is issued to the buffer.

On the trailing edge of IWSTR the data appearing on IWP, IW0 - IW7 is copied into the formatter, encoded and then written onto tape immediately following the preamble '1' bit.

The buffer/controller should use the trailing edge of the IWSTR pulse to set the next byte of data on IWP, IW0 - IW7. The formatter requires that the first bit be set up on the data lines before the first IWSTR is issued and that the subsequent bits are set up within one-half of a character period after the trailing edge of IWSTR.

The buffer will set ILWD true when the last data byte is set on IWP, IW0 - IW7. When the following IWSTR pulse occurs the formatter samples ILWD and will then enter a postamble sequence immediately following the writing of the last data byte.

The postamble pattern is a mirror image of the preamble and consists of a one bit followed by 40 zero bits. The postamble is phase encoded and written simultaneously on the nine tape tracks.

Shortly after the last postamble bit is recorded a Write Amplifier Reset (IWARS) pulse is issued by the formatter. The IWARS pulse is employed in some tape transport models to control write current turn-off at the end of an edit operation.

When operating with a transport utilizing a single stack head the post-record delay is initiated immediately after the last postamble bit is recorded.

The write sequence is terminated in a different manner when operating with a dual stack transport. The post-record delay is not initiated immediately after the last postamble bit is recorded. The delay is initiated after the transport's read electronics has completed read-after-write check on the data just recorded. An internal waveform, IREND, is utilized to indicate the end of a read-after-write operation.

Following the post-record delay, IDBY goes false and a stop command is given to the transport. Finally, IFBY is reset shortly after tape comes to rest.

4.2.6.5 Writing from BOT

The 1600 cpi PE format requires that tapes which are recorded in the PE mode be identified by a burst of alternate ones and zeros at the BOT marker. It is also required that the first record be written approximately 3 inches after the marker.

When writing from BOT the formatter generates an extra-long pre-record delay. In a suitable time interval during the delay, the PE identification burst is written consisting of a pattern of alternate ones and zeros (1 0 1 0 1 0 1 0) in the Parity channel. All other channels are erased.

Upon completion of the pre-record delay the tape is positioned approximately 3 inches past the BOT marker and the first record is now written in the normal manner.

4.2.6.6 Write File Mark

A file mark record consists of at least 80 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6 and 7. Channels 1, 3, and 4 are dc-erased. The file mark is separated from the preceding record by approximately 3.75 inches and from the following record by a nominal IBG (0.6 inch).

The formatter generates a long pre-record delay equivalent to a 3.75-inch IBG. The write logic then generates and encodes 40 preamble zero bits and records this onto Channels P, 0, 2, 5, 6, and 7. This pattern is equivalent to 80 flux reversals at 3200 frpi. The postamble one bit is not recorded.

At the completion of the write file mark operation the command is terminated in the same manner as other write operations.

4.2.6.7 Erase (Variable Length)

The Erase (Variable Length) is a dummy write command is is used to erase any desired length of tape. This operation is useful in applications which require the ability to erase individual records on a previously recorded tape.

In executing the Erase (Variable Length) command the formatter performs all operations of a normal write command except that the dummy data being transmitted from the controller to the formatter is not recorded. Therefore, a length of tape equivalent to the dummy record is erased. The ILWD signal determines record length in the manner previously described.

4.2.6.8 Erase (Fixed Length)

The Erase (Fixed Length) command is a dummy write file mark command. When executed, a fixed length of tape (approximately 3.75 inches) is erased.

4.2.7 PE READ PCBA

The PE Read PCBA, illustrated in Figure 4-17, contains the logic necessary to perform the formatter function of read recovery, including Read Forward, Read Reverse (Normal) and Read Reverse (Edit). It also performs simultaneous read-after-write data checks when transports having dual stack heads are utilized.

The read recovery logic is activated by the control waveform IRGATE from the PE Write PCBA. IRGATE goes true at the end of the pre-record delay. Upon reading a complete record, an IREND pulse is transmitted back to the PE Write PCBA which resets IRGATE. The resetting of IRGATE deactivates the PE Read PCBA.

4.2.7.1 Tracking Oscillator

The tracking oscillator is located on the PE Read PCBA. It compensates the read logic timing for instantaneous or average tape speed variations of both the transport which writes tape and the transport that performs the read function.

The tracking oscillator servos on one data channel such that its frequency is always a fixed multiple of the data rate. If a dropout occurs on the data channel the tracking function is automatically switched to another track.

4.2.7.2 Read Data Channel Logic

There are nine identical channels of read logic which operate independently of each other. Figure 4-18 illustrates a typical read data channel. Incoming data is routed to a circuit which either inverts the data or not, dependent on whether the transport is reading tape in the forward or reverse direction. The purpose of this is to ensure that any given flux transition on tape appears as the same change in signal polarity.

The remainder of the read recovery logic operates independently of tape direction.

The output of the inverter circuit is fed to a data decoder whose purpose is to distinguish each bit cell from the next and to decode the data contained within each cell.

Associated with the decoder is an envelope detector which continuously senses the presence (or absence) of data. A dropout detector monitors the data decoder during certain portions of each record and sets a flag if dropout occurs.

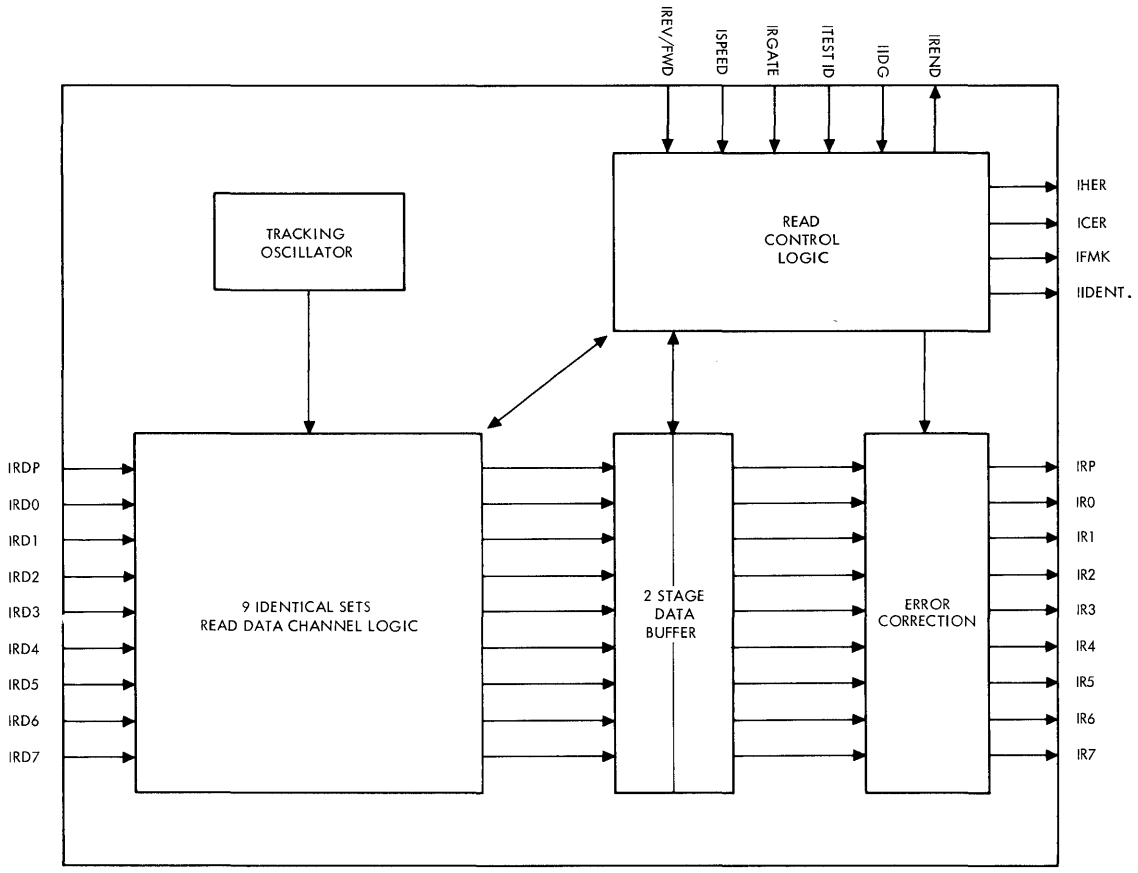


Figure 4-17. PE Read PCBA, Simplified Block Diagram

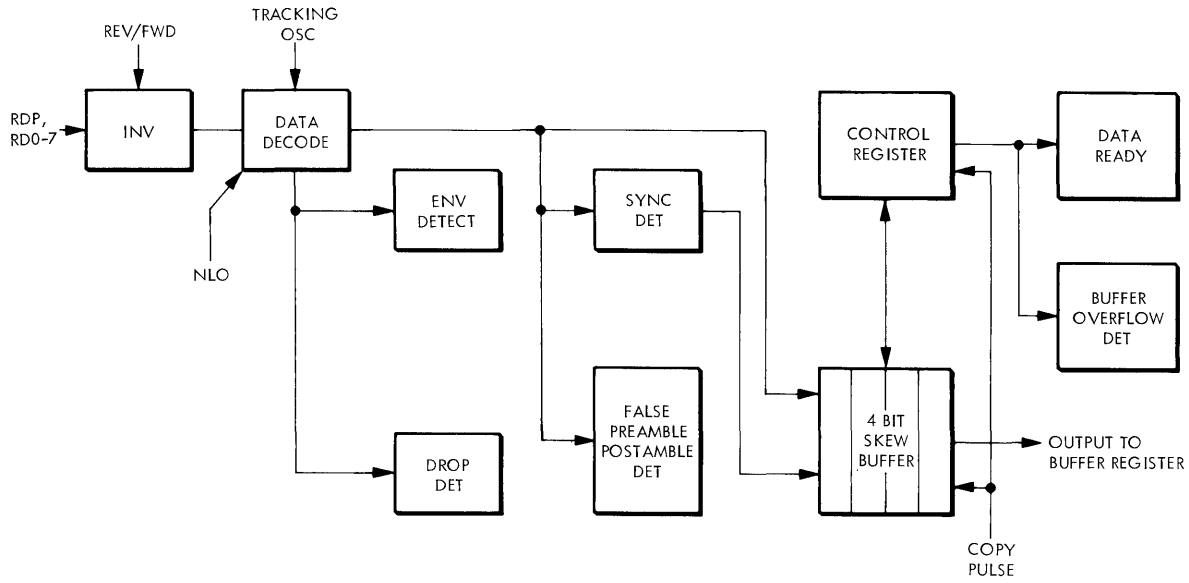


Figure 4-18. Read Data Channel Logic

The decoder is forced to lock onto the correct signal edge during the first period of the preamble by the NLO signal. During the same period the tracking oscillator will track onto the instantaneous data rate from its center frequency.

When lockon is achieved, NLO is released and the dropout detector is enabled. False preamble checks are now made and the logic then waits for the first one bit. When received, the one bit is interpreted as being the one bit written at the end of the preamble and will cause the SYNC flip-flop to set. All following bits until postamble detection will be interpreted as data bits.

The first data bit is copied into a 4-bit skew buffer. The control register simultaneously shifts left one place to record the occurrence. If this bit is still present when the second bit arrives, the second bit will be copied into the second position of the buffer. The amount of skew buffering actually used during a data transfer depends upon the combined write and read misalignments between the 9 channels and is typically less than half of the 4 bits provided for by the formatter. In the case of excessive skew a buffer overflow detection circuit will operate if the capacity of the skew buffer is exceeded.

A COPY pulse is issued when the read control logic detects that all 9 channels have a bit ready. This causes the first byte of data (now in parallel) to be copied into the first stage of the buffer and the contents of the first stage to be copied into the second stage, etc. Simultaneously, each of the skew buffers and control registers are shifted right one place to make room for new data.

4.2.7.3 Read Logic Control

The Read Logic Control circuits exercise overall control over the PE Read PCBA. Refer to Figure 4-17 for the following discussion.

4.2.7.4 Sequencing and Timing

This portion of the Read Logic Control circuits detect the presence of data from tape and supervises the sequence of events necessary to read a record. Functions include lock-on, timing for preamble and postamble tests, detection of data available in the skew buffers, postamble detection, and end-of-record detection (REND).

4.2.7.5 Error Detection

During a read operation a comprehensive set of tests are made to ensure that each record meets 1600 cpi format requirements and that the data is error free. These tests are as follows.

(1) Single channel dropout.

(2) Multi-channel dropout.

(3) False preamble detection.

(4) False postamble detection.

(5) Buffer overflow.

(6) Parity error without associated channel dropout.

In the case of a single channel dropout, error correction is performed automatically. Data from the channel suffering a dropout is discarded and replaced by regenerated data which has been computed on the basis of data on the other 8 channels together with the Parity circuits. Interface waveform CER indicates to the controller that error correction is taking place.

All other error conditions are not correctable and will result in a hard error indication (HER) to the controller. Note that for cases (2) through (5) transmission of data to the controller ceases immediately upon detection of the error. For case (6), data transmission will continue and each byte in error will be labeled by a pulse on HER at the time the corresponding RSTR is issued.

4.2.7.6 File Mark Detection

A test for file mark is made at the time lock-on is removed — approximately midway through the preamble. If the record contains data in Channels P, 0, and 5, or Channels 2, 6, and 7, with Channels 1, 3, and 4 erased, the record will be recognized as being a file mark. Interface line FMK indicates to the controller that a file mark has been detected.

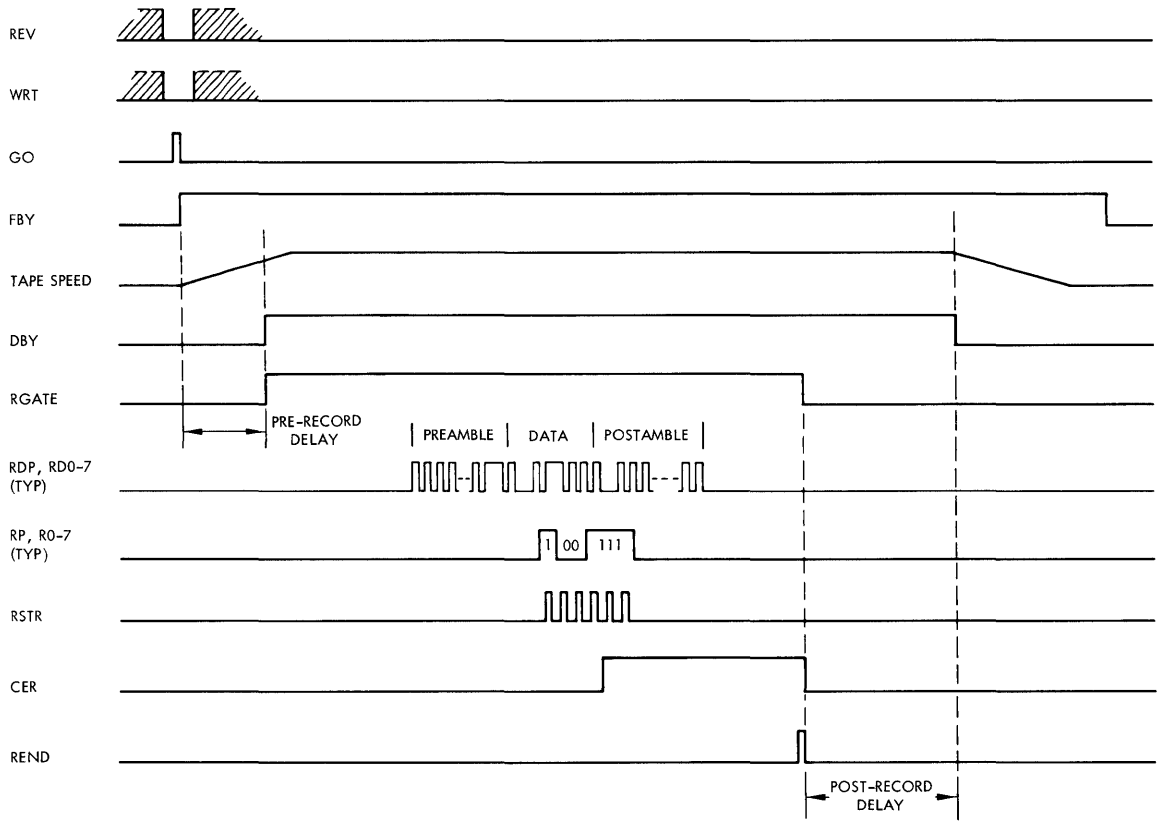
4.2.7.7 Ident Detection

When reading off BOT a test is automatically made to verify the presence or absence of a 1600 cpi identification burst at the BOT marker. As the BOT tab moves over the read head, a control signal (IDG) generated in the PE Write PCBA goes true and activates the envelope detector portion of the read data channels.

Shortly afterwards the TEST ID line is pulsed and samples the state of the envelope detectors. If Channel P contains data and all other channels are dc-erased, the IDENT interface line is pulsed. For transports having a dual stack head, IDENT detection is also operative when writing from BOT.

4.2.7.8 Read Waveforms

Waveforms for a typical Read operation are shown in Figure 4-19.



NOTE: FOR CONVENIENCE ALL WAVEFORMS ARE SHOWN HIGH TRUE.

Figure 4-19. PE Read Operation Illustrating Error Correction for Last Two Data Bytes

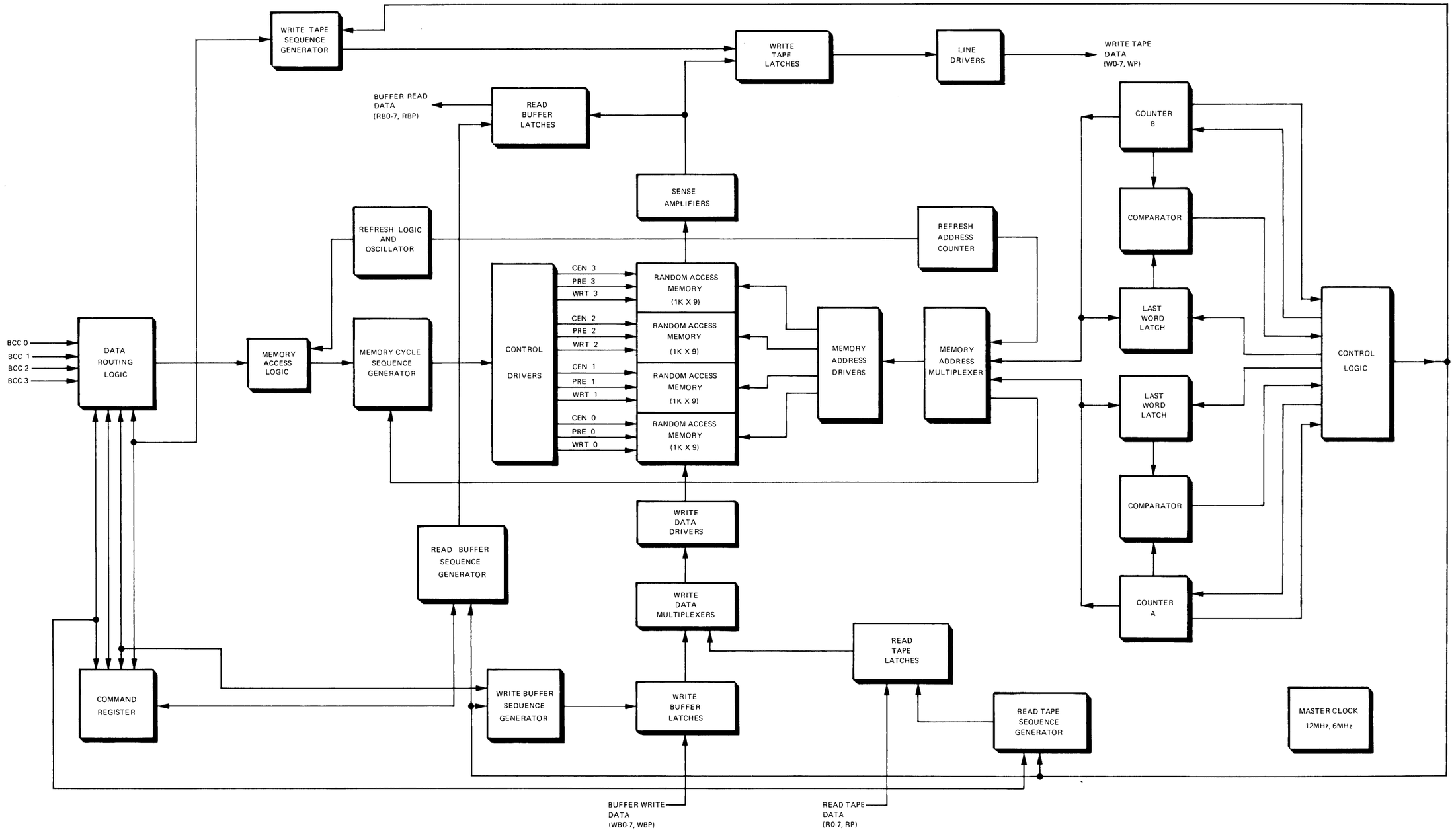


Figure 4-6. Buffer Organization, Simplified Control Block Diagram

SECTION V
DETAILED ELECTRICAL AND LOGIC DESCRIPTIONS

5.1 INTRODUCTION

This section contains the theory of operation of the printed circuit boards used in the formatter. Schematic and assembly drawings for each board are contained at the end of Section VII.

A better understanding of the logic used in the formatter can be gained when the operation of the various integrated circuit (IC) types is understood. Paragraphs 5.2 and 5.3 contain these descriptions and should be referred to in conjunction with the theory of operation for the individual PCBAs.

5.2 TYPICAL TTL PARAMETERS AND CIRCUITS

Figure 5-1 shows typical NAND and NOR TTL circuits used in PERTEC devices. Also shown are the electrical parameters and switching characteristics of these typical 7400 series TTL circuits. (Component values given in Figures 5-1 through 5-33 are nominal.)

5.2.1 2-INPUT NAND GATE (TYPE 7400)

Figure 5-2 shows the logic symbol and truth table for the Type 7400 2-input NAND gate. Typically, each IC of this type contains 4 gates.

5.2.2 2-INPUT NOR GATE (TYPE 7402)

Figure 5-3 shows the logic symbol and truth table for the Type 7402 2-input NOR gate. Typically, each IC of this type contains 4 gates.

5.2.3 INVERTER (TYPE 7404)

Figure 5-4 shows the logic and truth table for the Type 7404 inverter. Typically, each IC of this type contains 6 inverters.

5.2.4 3-INPUT NAND GATE (TYPE 7410)

Figure 5-5 shows the logic symbol and truth table for the Type 7410 3-input NAND gate. Typically, each IC of this type contains 3 gates.

5.2.5 INVERTER BUFFER/DRIVER (TYPE 7416)

The Type 7416 inverter buffer/driver is a monolithic TTL circuit which features high-voltage open-collector outputs for interfacing with high-level circuits. It can also be used as an inverter buffer for driving TTL inputs. The 7416, shown in Figure 5-6, has a minimum breakdown voltage of 15v and the maximum sink current is 40 ma. Typically, 6 inverters are packaged in this type IC.

5.2.6 2-INPUT NAND BUFFER (TYPE 7438)

The Type 7438 2-input NAND buffer is shown in Figure 5-7. This type buffer has an open-collector output and is typically packaged with 4 buffers per IC.

5.2.7 2-WIDE 2-INPUT AND-OR-INVERT GATE (TYPE 7450)

The logic, schematic, and truth table for the Type 7450 2-wide 2-input AND-OR-INVERT gate are shown in Figure 5-8. This type is normally packaged with 2 gates per IC.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(1)}$	LOGIC 1 INPUT VOLTAGE REQUIRED AT INPUT TERMINAL TO ENSURE LOGIC 0 LEVEL AT OUTPUT		2			V
$V_{IN(0)}$	LOGIC 0 INPUT VOLTAGE REQUIRED AT ANY INPUT TERMINAL TO ENSURE LOGIC 1 LEVEL AT OUTPUT				0.8	V
$V_{OUT(1)}$	LOGIC 1 OUTPUT VOLTAGE	V_{CC} = MIN. V_{IN} = 0.8V I_{LOAD} = −400μA	2.4	3.3		V
$V_{OUT(0)}$	LOGIC 0 OUTPUT VOLTAGE	V_{CC} = MIN. V_{IN} = 2V I_{SINK} = 16mA		0.22	0.4	V
$I_{IN(0)}$	LOGIC 0 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 0.4V			−1.6	mA
$I_{IN(1)}$	LOGIC 1 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 2.4V			40	μA
		V_{CC} = MAX. V_{IN} = 5.5V			1	mA

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PD0}	PROPAGATION DELAY TIME TO LOGIC 0 LEVEL	C_L = 15pF R_L = 400Ω		8	15	ns
T_{PD1}	PROPAGATION DELAY TIME TO LOGIC 1 LEVEL	C_L = 15pF R_L = 400Ω		12	22	ns

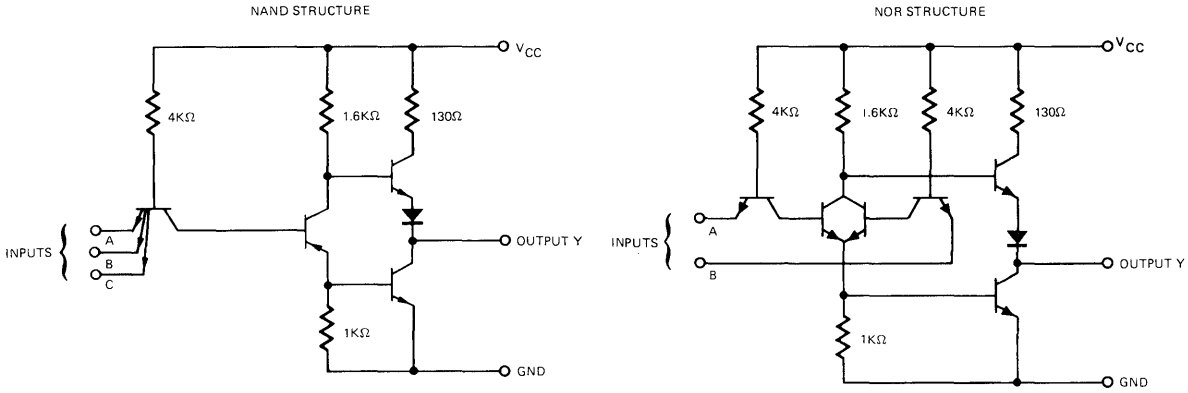
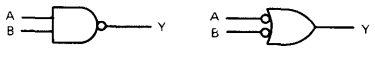
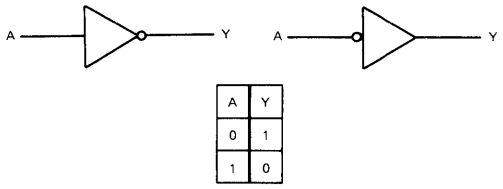


Figure 5-1. Typical TTL Parameters



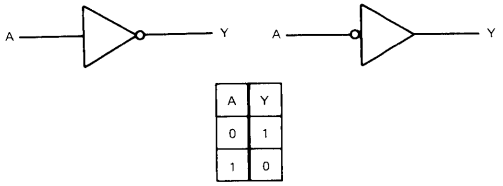
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5-2. 2-Input NAND Gate



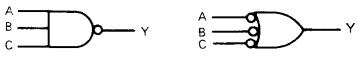
A	Y
0	1
1	0

Figure 5-3. 2-Input NOR Gate



A	Y
0	1
1	0

Figure 5-4. Inverter (Type 7404)



A	B	C	Y
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Figure 5-5. 3-Input NAND Gate

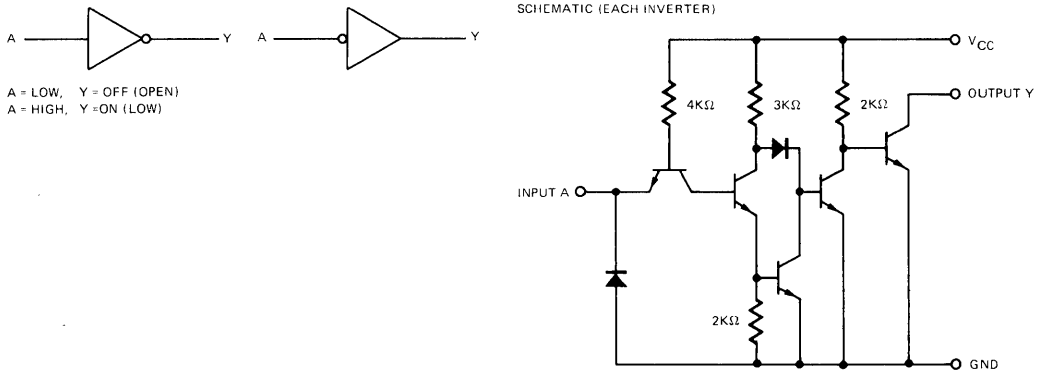
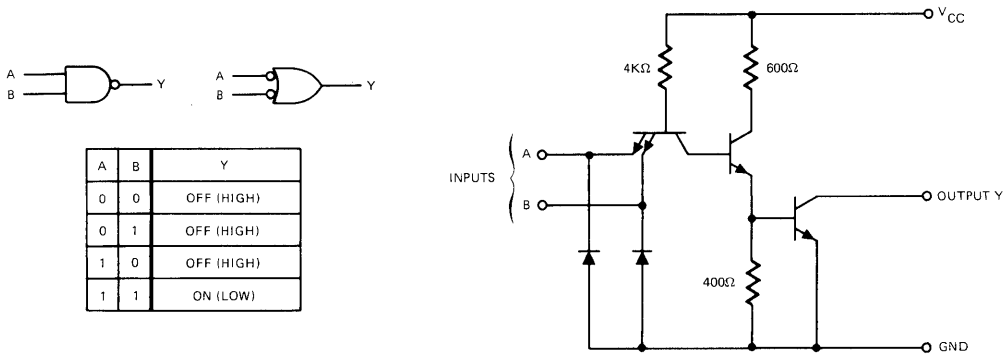
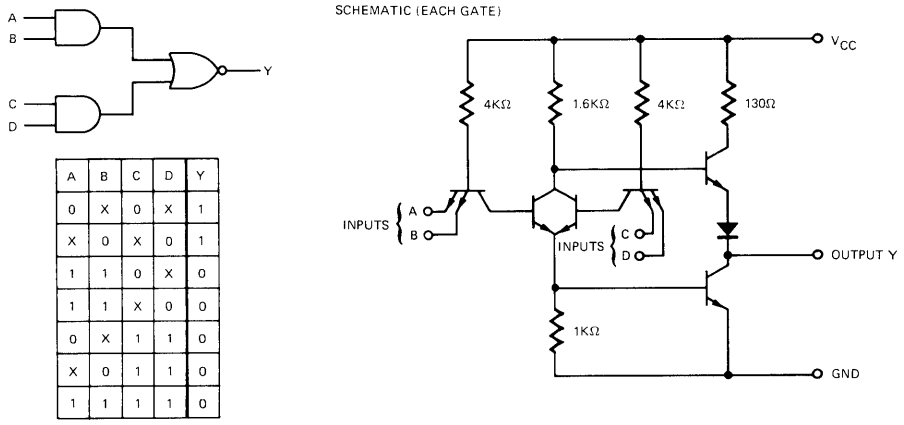


Figure 5-6. Inverter Buffer / Driver



A	B	Y
0	0	OFF (HIGH)
0	1	OFF (HIGH)
1	0	OFF (HIGH)
1	1	ON (LOW)

Figure 5-7. 2-Input NAND Buffer



A	B	C	D	Y
0	X	0	X	1
X	0	X	0	1
1	1	0	X	0
1	1	X	0	0
0	X	1	1	0
X	0	1	1	0
1	1	1	1	0

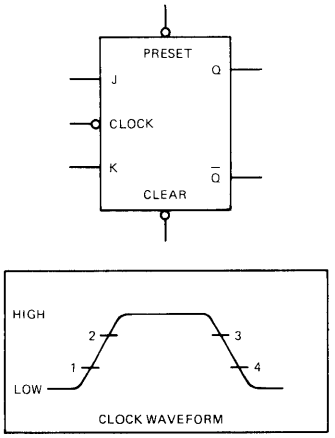
Figure 5-8. 2-Wide 2-Input AND-OR-INVERT Gate

5.2.8 J-K MASTER-SLAVE FLIP-FLOP (TYPE 7476)

The Type 7476 J-K Master Flip-Flop with preset and clear inputs is shown in Figure 5-9. Operation is based upon the master-slave principle with inputs to the master section controlled by the clock pulse. The clock also regulates the state of the coupling transistors which connect the master and slave sections.

Operationally, the slave section is isolated from the master section. Information is entered via the J and K inputs to the master section; the J and K inputs are then disabled. Information is then transferred from the master section to the slave section.

Two flip-flops are packaged in each IC of this type.



TRUTH TABLE (EACH FLIP-FLOP)		
T_n		T_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES: 1. T_n=BIT TIME BEFORE CLOCK PULSE.
2. T_{n+1}=BIT TIME AFTER CLOCK PLUSE.
3. POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGIC 1
LOW INPUT TO CLEAR SETS Q TO LOGIC 0
CLEAR AND PRESET ARE INDEPENDENT OF CLOCK.

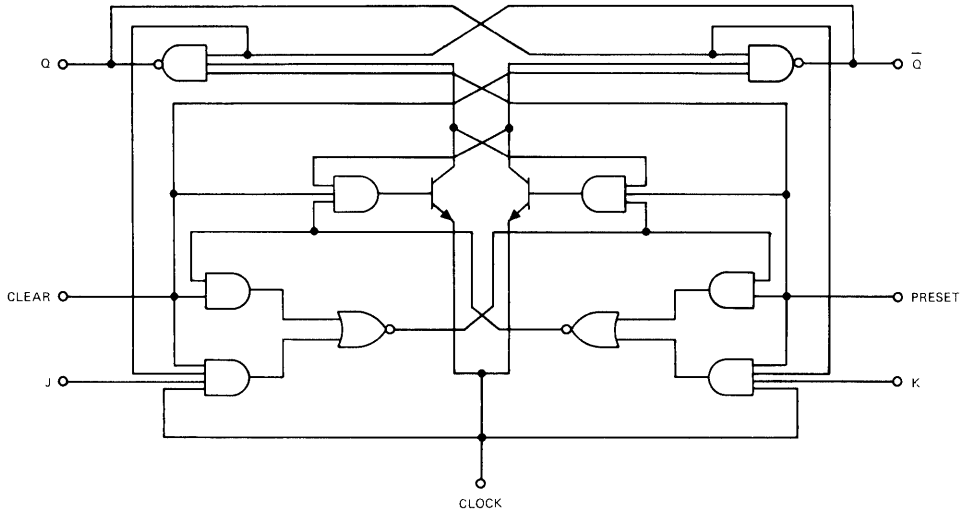


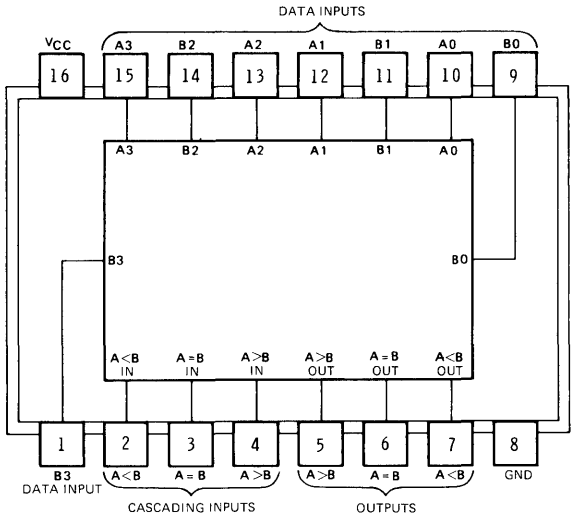
Figure 5-9. J-K Flip-Flop

5.2.9 4-BIT MAGNITUDE COMPARATOR (TYPE 7485)

Comparison of straight binary and straight BCD codes are performed by the Type 7485 4-bit magnitude comparator. The logic symbol and functional logic diagram are shown in Figures 5-10 and 5-11, respectively. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more significant bits. The stage handling the least significant bits must have a high-level voltage applied to the A = B input.

5.2.10 2-INPUT EXCLUSIVE-OR GATE (TYPE 7486)

Figure 5-12 shows the logic symbol and truth table for the Type 7486 2-input EXCLUSIVE-OR gate. Typically packaged 4 gates per IC, each gate utilizes TTL circuitry to perform the function $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output is a logic 1.



COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

Figure 5-10. 4-Bit Magnitude Comparator, Logic Symbol

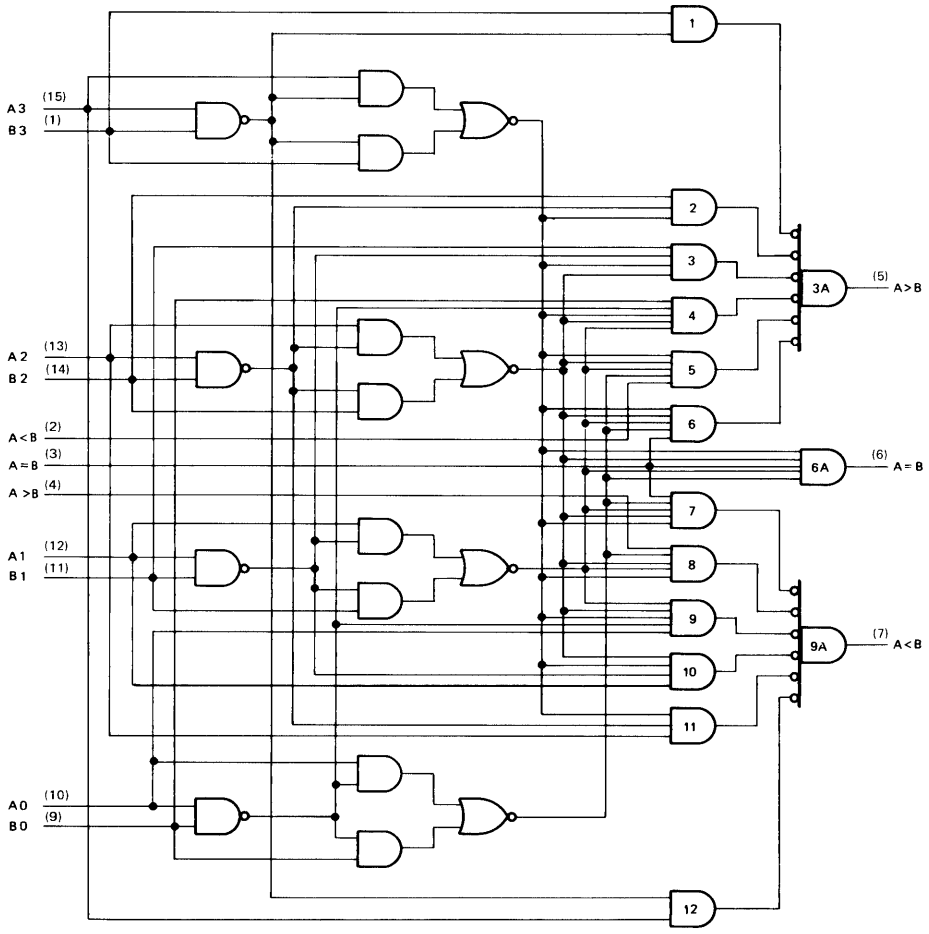


Figure 5-11. 4-Bit Magnitude Comparator, Logic Diagram

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

POSITIVE LOGIC: Y=A⊕B

Figure 5-12. EXCLUSIVE-OR Gate

5.2.11 5-BIT SHIFT REGISTER (TYPE 7496)

The logic symbol and functional block diagram for the Type 7496 5-bit shift register is shown in Figure 5-13. This register is typically contained on a single IC; it is made up of five R-S master-slave flip-flops connected to perform serial-to-parallel conversion of binary data. Since both inputs and outputs of all flip-flops are easily accessible, parallel-in/parallel-out or serial-in/serial-out operations may be performed.

Referring to Figure 5-13, all flip-flops may be simultaneously set to logic zero by the application of a logic zero voltage to the *clear* input. This condition may be applied independent of the state of the clock input.

The flip-flops in the shift register may be independently set to the logic one state by applying a logic one voltage to both the preset input of the specific flip-flop and the common preset input. The purpose of the preset-enable input is to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. The preset input is also independent of the state of the clock input or clear input.

Information is transferred to the output pin of the flip-flop when the clock input changes from a logic zero to a logic one.

The serial input to the shift register provides information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logic one and the preset input must be at a logic zero when clocking occurs.

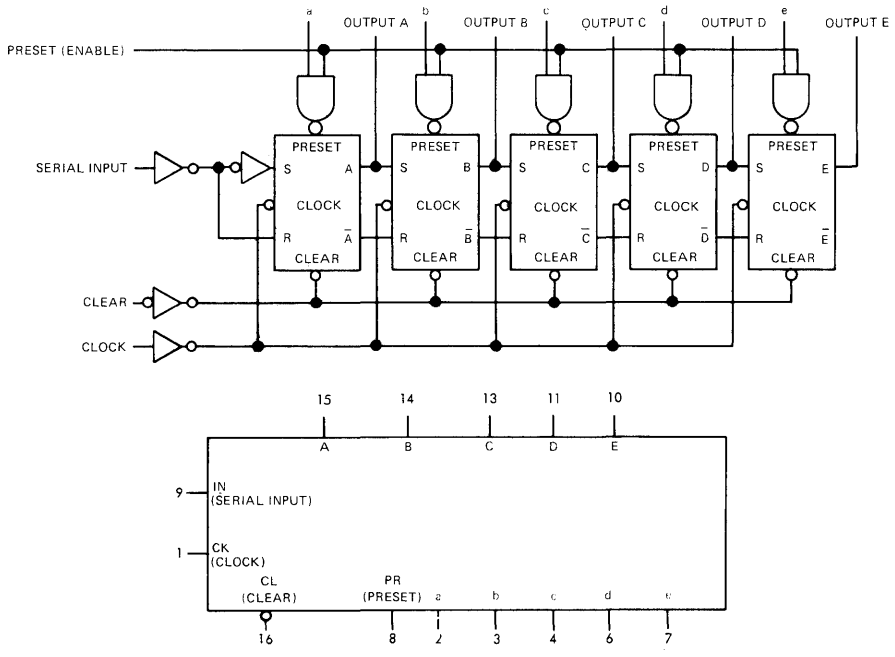


Figure 5-13. 5-Bit Shift Register

5.2.12 DATA SELECTOR MULTIPLEXER (TYPE 74151A)

The Type 74151A multiplexer chip contains the logic necessary to select one of eight data sources and provide both standard and inverted output. The logic symbol and functional block diagram are shown in Figure 5-14. Note that the strobe input must be at a low logic level to enable the device. A high level at the strobe forces the W output high and the Y output low.

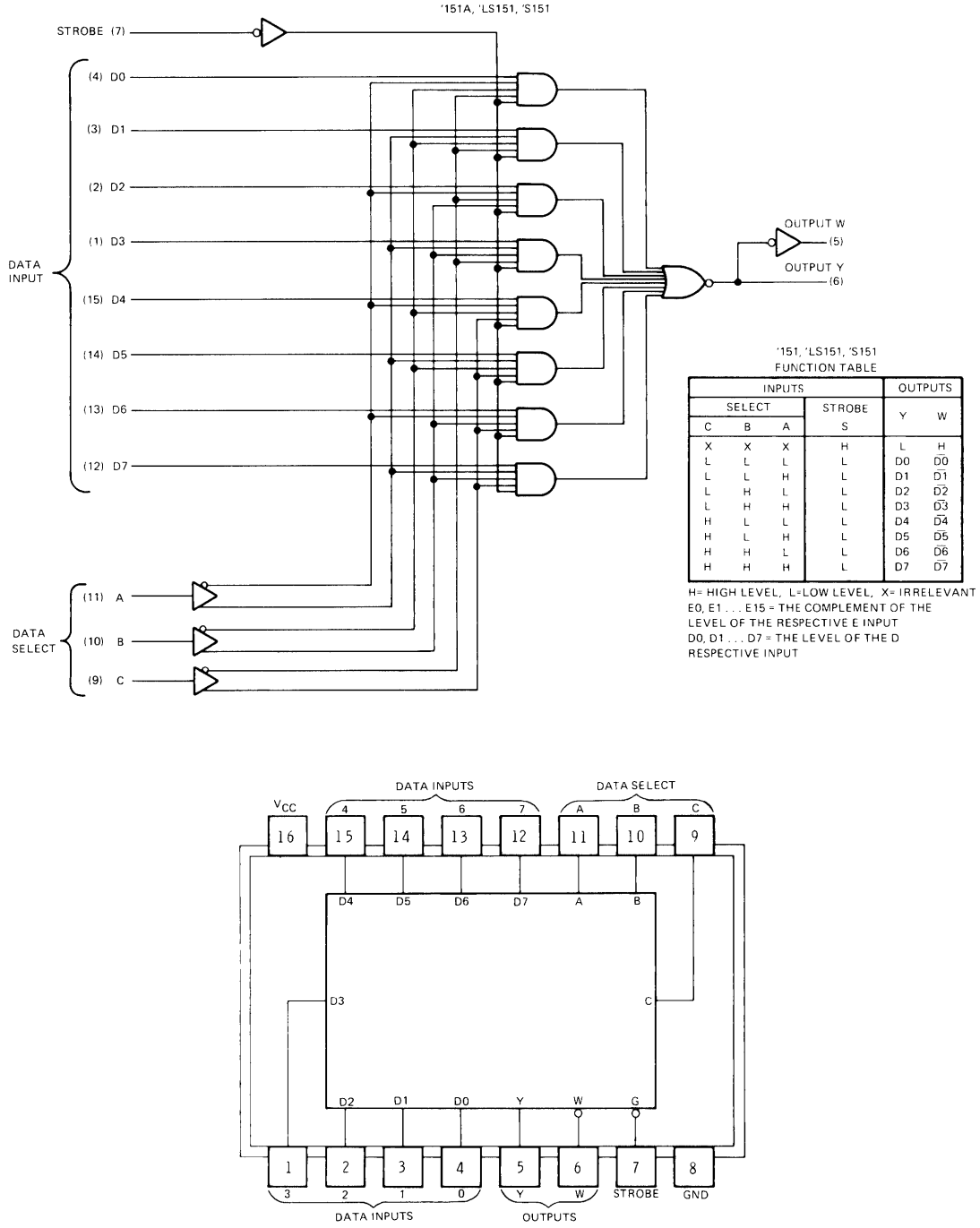
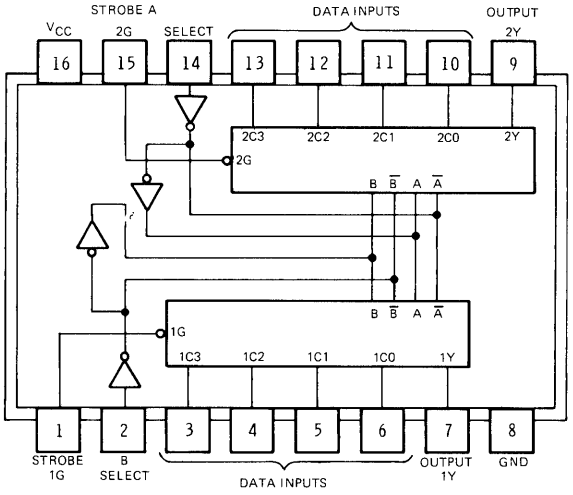


Figure 5-14. Data Selector Multiplexer

5.2.13 DUAL DATA SELECTOR/MULTIPLEXER (TYPE 74153)

The logic symbol and functional block diagram for the Type 74153 dual 4-line-to-1-line data selector/multiplexer are shown in Figure 5-15. Each chip contains the inverters and drivers necessary to supply fully complementary binary decoding data selection to the AND-OR invert gates. Note that separate strobe inputs are provided for each of the two 4-line sections.



SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

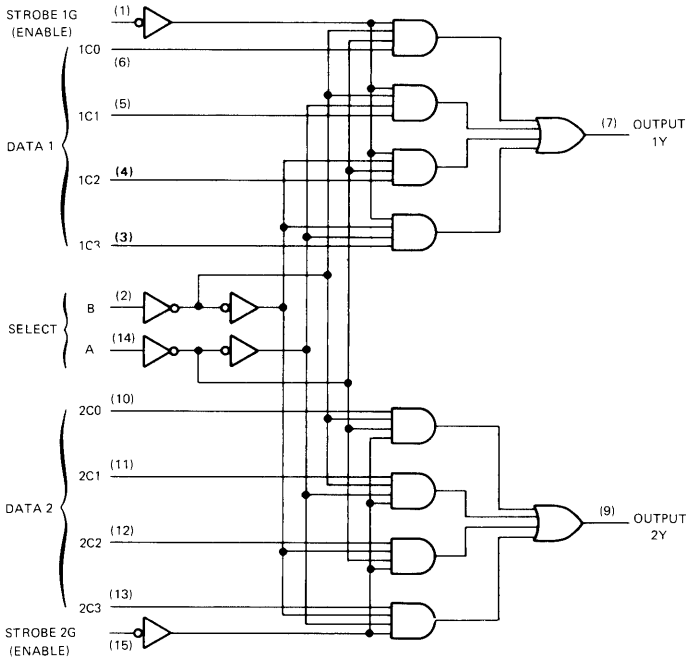


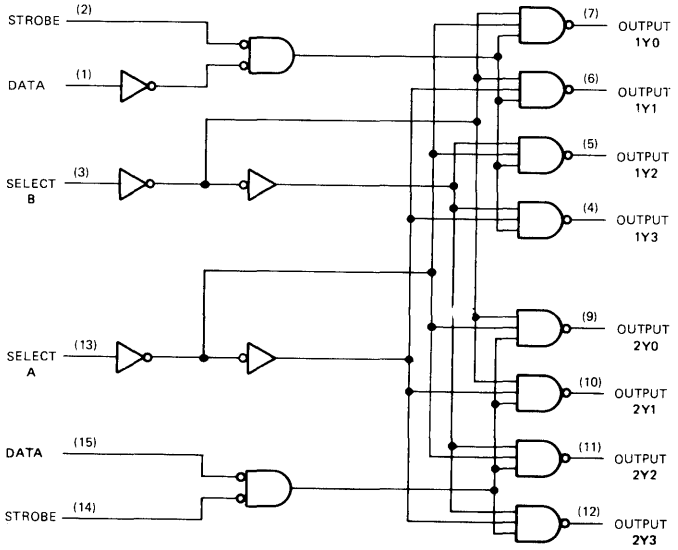
Figure 5-15. Dual Data Selector/Multiplexer

5.2.14 DUAL DECODER/DEMULTIPLEXER (TYPE 74155)

The Type 74155 dual 2-line-to-4-line decoder/demultiplexer is contained on a single chip. Figure 5-16 shows the logic symbol and functional logic diagram for the device.

Individual strobes and common binary address inputs are provided in this TTL package. When both sections are enabled by the strobes, the common binary address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes can be used to inhibit or activate each of the 4-bit sections as described.

Note that data applied to input 1-C is inverted at the output and that data applied to input 2-C is not inverted at the output.



INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

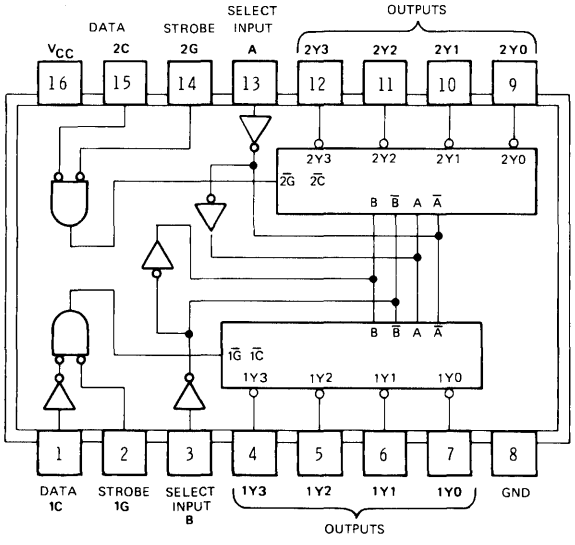
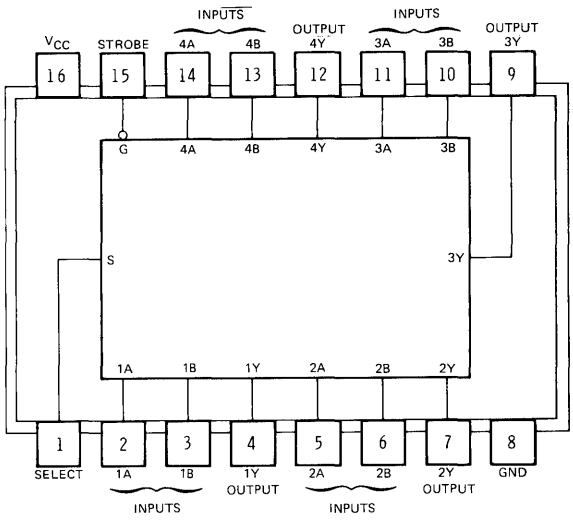


Figure 5-16. Dual Decoder/Demultiplexer

802B

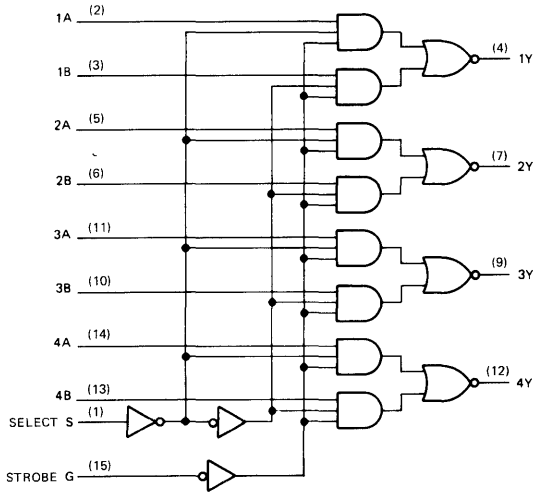
5.2.15 QUADRUPLE DATA SELECTOR/MULTIPLEXER (TYPE 74157)

The logic symbol and functional logic diagram for the quadruple 2-line-to-1-line data selector/multiplexer are shown in Figure 5-17. Contained on this chip are the inverters and drivers to supply full on-chip data selection to the four output gates. Note that a separate strobe input is provided. Functionally, a 4-bit word is selected from one of two sources and is routed to the four outputs.



INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	157	158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant



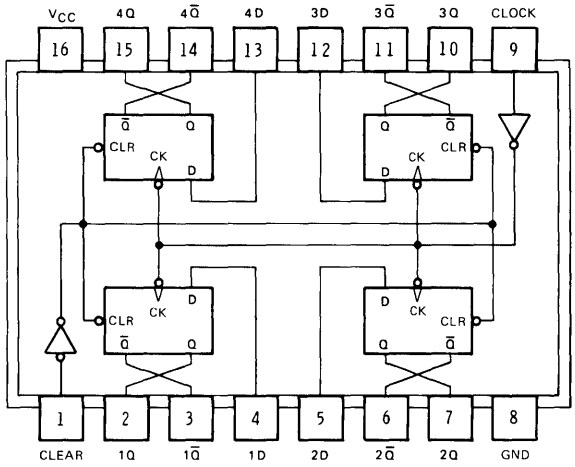
positive logic:

Low logic level at S selects A inputs.
High logic level at S selects B inputs.

Figure 5-17. Quadruple Data Selector/Multiplexer

5.2.16 HEX/QUADRUPLE D-TYPE FLIP-FLOP (TYPE 74175)

Four D-type flip-flops with clock and clear inputs are packaged on a single chip. These are positive-edge-triggered flip-flops utilizing TTL circuitry. The logic symbol and functional block diagram for the Type 74175 are shown in Figure 5-18.



FUNCTIONAL TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

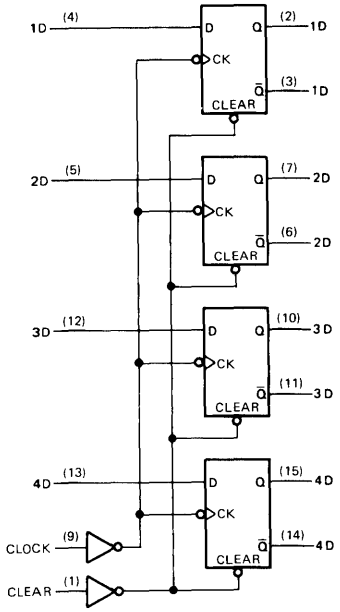


Figure 5-18. Hex/Quadruple D-Type Flip-Flop

Information at the D inputs which meet the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. With a high or low level at the clock input the D input signal has no effect at the output of the device.

5.2.17 SYNCHRONOUS 4-BIT COUNTER (TYPE 74161)

The logic symbol and functional block diagram of the Type 74161 synchronous 4-bit binary counter is shown in Figure 5-19. This counter is contained on a single IC.

The synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

The counters are fully programmable; that is, the outputs may be preset to either state. As presetting is synchronous, placing a low level on the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear function for the 74161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the state of the clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages.

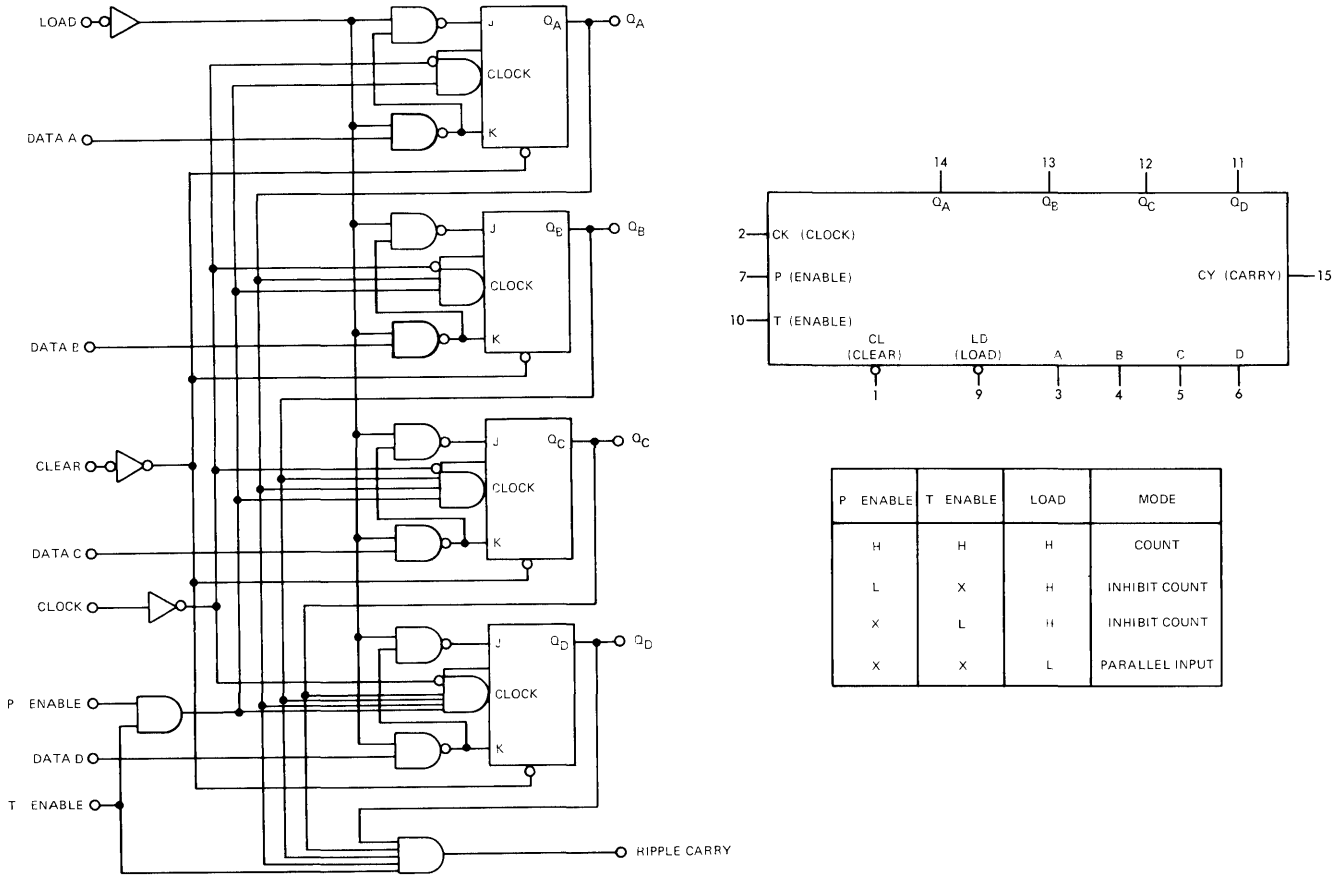
Typical clear, preset, count, and inhibit sequences for the Type 74161 counter are shown in Figure 5-20. The actual sequences illustrated are: clear outputs to zero; preset to binary 12; count to 13, 14, 15, 0, 1, and 2; inhibit.

5.2.18 DUAL LINE RECEIVER/SENSE AMPLIFIER (TYPE 75107)

The Type 75107 monolithic dual line receivers feature two independent channels, as shown in Figure 5-21. Each IC of this type contains the logic shown, a common current source, supply voltages, and ground. An individual receiver consists of a differential input stage which provides a high input impedance, a level-shifting stage, a second differential amplifier which enhances the common-mode rejection ratio, and a typical TTL output stage.

Two strobes are provided at the input of each gate. The receiver may be enabled or inhibited, respectively, when a logic 1 is applied to both strobes or a logic 0 is applied to either strobe. A strobe or gating input may be used on the output stage of either channel to hold the output at a logic 1 regardless of the input signal.

There are many applications for line receiver when used as differential comparators, such as voltage comparators, threshold detectors, controlled Schmitt triggers, and pulse width controls.



P ENABLE	T ENABLE	LOAD	MODE
H	H	H	COUNT
L	X	H	INHIBIT COUNT
X	L	H	INHIBIT COUNT
X	X	L	PARALLEL INPUT

Figure 5-19. Synchronous 4-Bit Counter

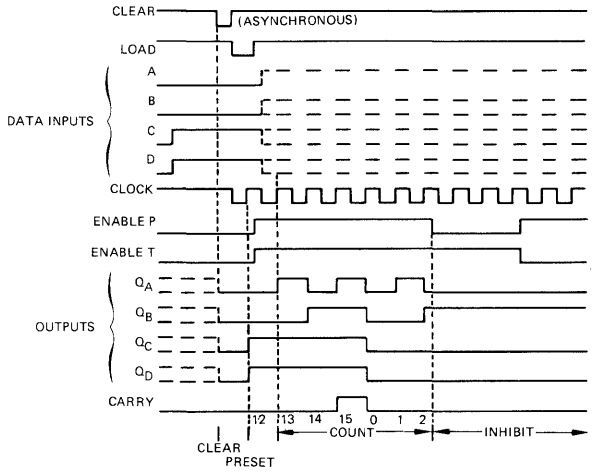


Figure 5-20. Clear, Preset, Count, and Inhibit Sequences for Type 74161 4-Bit Counter

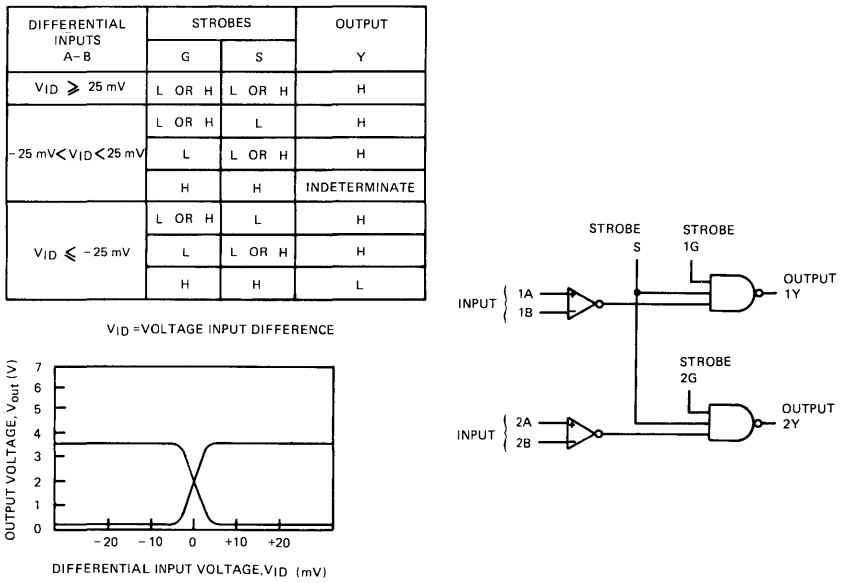


Figure 5-21. Dual Line Receiver/Sense Amplifier

In the formatter, the Type 75107 is employed as dual differential comparators. As a differential comparator, a 75107 may be connected so as to compare the non-inverting input terminal with the inverting input. Thus, a logic 1 or 0 is experienced as the output resulting from one input being greater than the other. The strobe inputs allow additional control over the circuit so that either output (or both) may be inhibited.

5.2.19 OPERATIONAL AMPLIFIER (TYPE 741)

The logic symbol for the Type 741 linear intergrated circuit type of operational amplifier is shown in Figure 5-22. The 741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the epitaxial process. It is intended for a wide range of analog applications. The high gain and wide range of operating voltages provide for operation in integrator, summing amplifier, and general feedback applications. In addition, it is short-circuit protected and requires no external components for frequency compensation.

5.3 HIGH-SPEED TTL PARAMETERS

Figure 5-23 shows a typical HIGH SPEED TTL NAND circuit employed in PERTEC devices. Also shown are the electrical parameters and switching characteristics for the 74H series of devices. (Component values given in Figures 5-23 through 5-29 are nominal.)

5.3.1 HIGH-SPEED 2-INPUT NAND GATE (TYPE 74H00)

The Type 74H00 2-input NAND gate logic symbol and truth table are shown in Figure 5-24. Typically, each IC of this type contains four gates.

5.3.2 HIGH-SPEED INVERTER (TYPE 74H04)

Figure 5-25 shows the Type 74H04 high-speed inverter logic symbol and truth table. Normally, 6 inverters are packaged in a single IC.

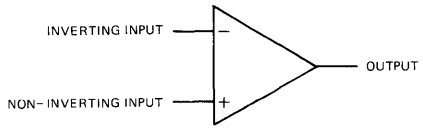
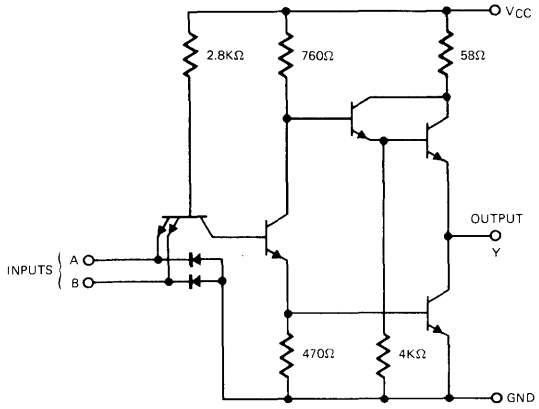


Figure 5-22. Operational Amplifier



ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} (1)	LOGIC 1 INPUT VOLTAGE REQUIRED AT INPUT TERMINAL TO ENSURE LOGIC 0 LEVEL AT OUTPUT		2			V
V_{IN} (0)	LOGIC 0 INPUT VOLTAGE REQUIRED AT INPUT TERMINAL TO ENSURE LOGIC 1 LEVEL AT OUTPUT				0.8	V
V_{OUT} (1)	LOGIC 1 OUTPUT VOLTAGE	V_{CC}=MIN. V_{IN} = 0.8 V I_{LOAD} =500μA	2.4			V
V_{OUT} (0)	LOGIC 0 OUTPUT VOLTAGE	V_{CC}=MIN. V_{IN} = 2 V I_{SINK}=20 mA			0.4	V
I_{IN} (0)	LOGIC 0 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 0.4 V			2	mA
I_{IN} (1)	LOGIC 1 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 2.4 V			50	μA
		V_{CC} =MAX. V_{IN} = 5.5 V			1	mA

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PD} 0	PROPAGATION DELAY TIME TO LOGIC 0 LEVEL	C_L = 25 PF R_L = 280Ω		6.5	10	NS
T_{PD} 1	PROPAGATION DELAY TIME TO LOGIC 1 LEVEL	C_L = 25 PF R_L = 280Ω		6	10	NS

Figure 5-23. Typcal High-Speed TTL Parameters

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5-24. High-Speed 2-Input NAND Gate

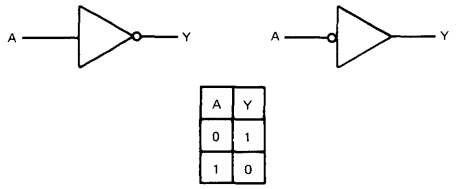


Figure 5-25. High-Speed Inverter

5.3.3 HIGH-SPEED J-K MASTER-SLAVE FLIP-FLOP (TYPE 74H76)

The Type 7476 J-K Master-Slave Flip-Flop with preset and clear inputs is shown in Figure 5-26. Operation is based upon the master-slave principle. Inputs to the master section are controlled by the clock impulse. The clock also regulates the state of the coupling transistors which correct the master and slave sections.

Operationally, the slave section is isolated from the master section. Information is entered via the J and K inputs to the master section; the J and K inputs are then disabled. Information is transferred from the master section to the slave section.

Two flip-flops are packaged in each IC of this type.

5.3.4 MOS SILICON GATE (TYPE 1103)

The Type 1103 is a fully decoded random access 1024-bit dynamic memory chip. It is a 1024-word-by-1-bit random access element using normally off P-channel MOS devices integrated on a monolithic array.

This fully decoded device allows the use of an 18-pin dual in-line package. The pin configuration, logic symbol, and block diagram for the Type 1103 is shown in Figure 5-27. Information stored in the memory is non-destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles and is required every two milliseconds.

5.3.5 SCHOTTKY BIPOLAR-TO-MOS LEVEL SHIFTER AND DRIVER (TYPE 3207A)

The Type 3207A pin configuration and logic symbol are shown in Figure 5-28. The device accepts TTL and DTL input signals and provides high output current and voltage suitable for driving MOS circuits. Two common enable inputs per pair of devices permit some logic to be performed at their input. Typical ac switching characteristics and waveforms are shown in Figure 5-29.

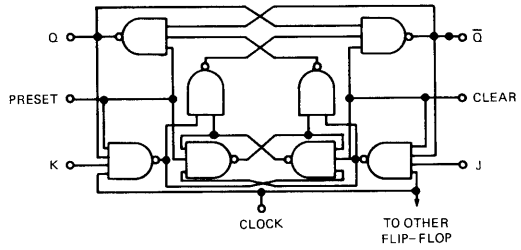


Figure 5-26. High-Speed J-K Master-Slave Flip-Flop

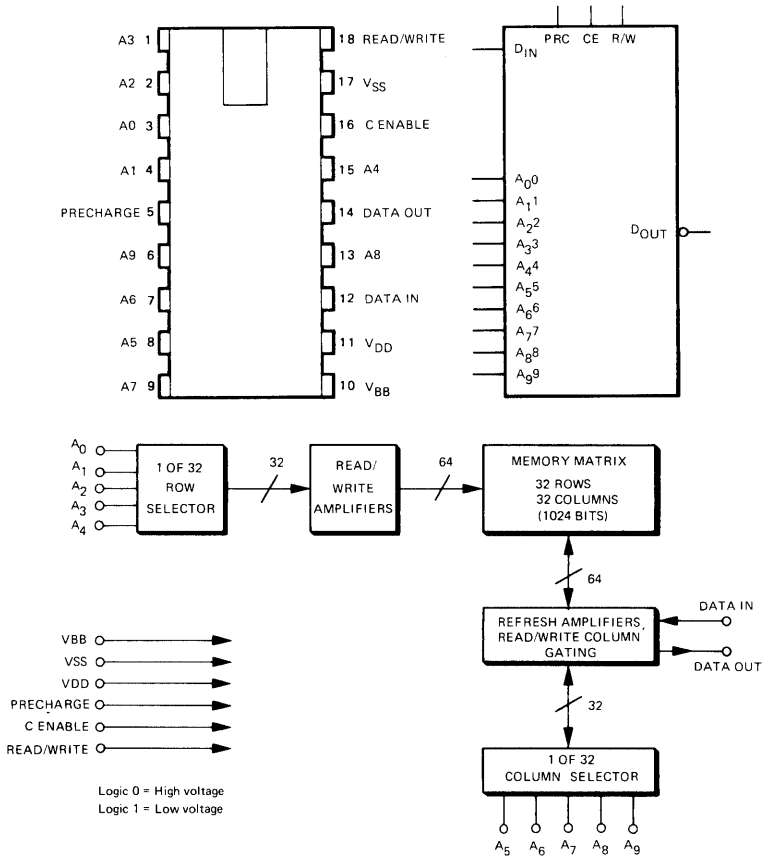


Figure 5-27. MOS Silicon Gate

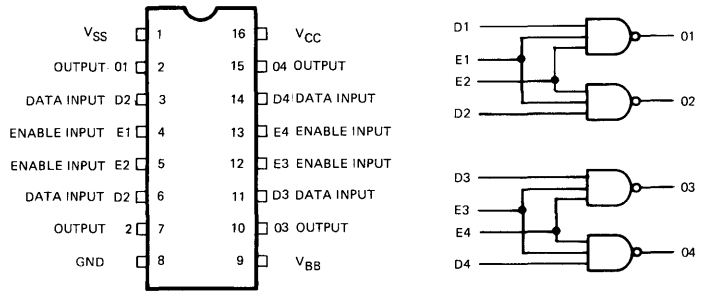


Figure 5-28. Schottky Bipolar Pin Configuration and Logic Symbol

SYMBOL	TEST	LIMITS (ns)				
		C_L = 100 pF		C_L = 200 pF		DELAY DIFFERENTIAL (1) C_L = 200 pF
		MIN.	MAX.	MIN.	MAX.	MAX.
t_{+-}	INPUT TO OUTPUT DELAY	5	15	5	15	5
t_{-+}	INPUT TO OUTPUT DELAY	5	25	5	25	10
t_r	OUTPUT RISE TIME	5	20	5	30	10
t_f	OUTPUT FALL TIME	5	20	10	30	10
t_D	DELAY + RISE OR FALL TIME	10	35	20	45	10

(1) Defined as the maximum skew between any output in the same package, eg., all input to output delays for the t_{-+} parameter are within a maximum of 10 nsec of each other in the same package.

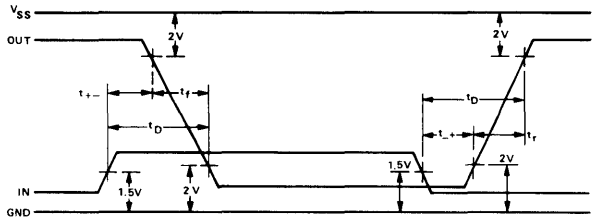
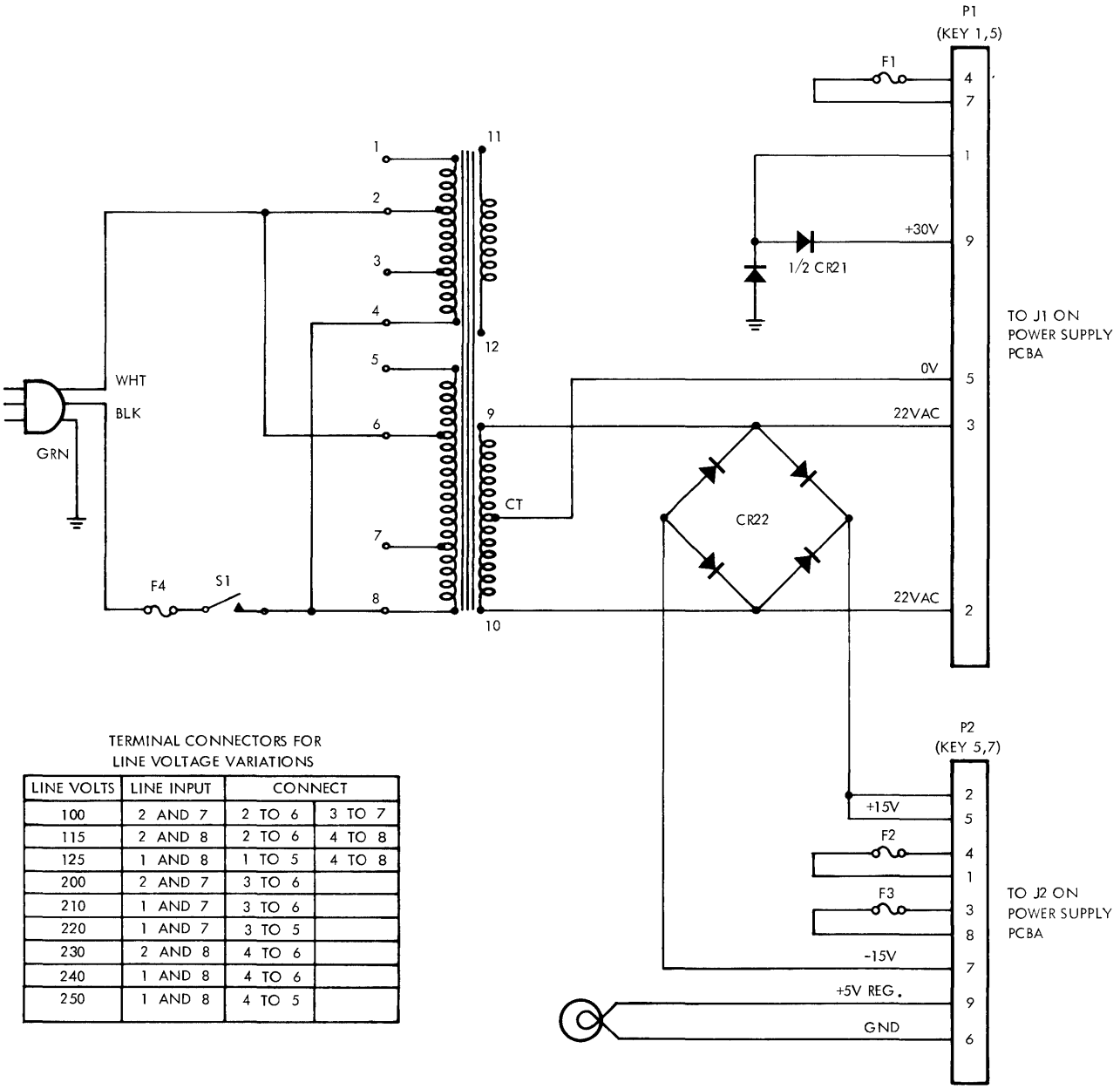


Figure 5-29. Schottky Bipolar Waveforms and Switching Characteristics

5.4 POWER SUPPLY ASSEMBLY

The power supply assembly is mounted on the left side of the formatter; it generates dc supplies of +5v at 7 amps, —5v at 1 amp, and +20v at 1 amp. The assembly is self-contained and can be removed from the formatter main frame.

Major components such as the transformer, bridge rectifier, power switch, etc., are mounted directly to the side support. These components are wired together and connect to a printed circuit board through two molex connectors P1 and P2. Transformer taps are provided for line voltages in the range of 100 to 250v ac. Figure 5-30 illustrates the circuitry and transformer tap connections.



TERMINAL CONNECTORS FOR
LINE VOLTAGE VARIATIONS

LINE VOLTS	LINE INPUT	CONNECT	
100	2 AND 7	2 TO 6	3 TO 7
115	2 AND 8	2 TO 6	4 TO 8
125	1 AND 8	1 TO 5	4 TO 8
200	2 AND 7	3 TO 6	
210	1 AND 7	3 TO 6	
220	1 AND 7	3 TO 5	
230	2 AND 8	4 TO 6	
240	1 AND 8	4 TO 6	
250	1 AND 8	4 TO 5	

Figure 5-30. Chassis Mounted Power Supply Components

5.4.1 POWER SUPPLY PCBA

The power supply printed circuit board is mounted on the buffered formatter power supply assembly. Schematic No. 103304 and Assembly No. 103305 should be referred to for the discussion in the following paragraphs which detail the functions of the Buffered PCBA in the following order.

(1) + 5v Regulator
(2) —5v Regulator
(3) + 20v Regulator
(4) Overcurrent Protection
(5) Overvoltage Protection
(6) Logic Enable

5.4.1.1 + 5v Regulator

The + 5v regulator is a switching regulator which converts unregulated + 15v to regulated + 5v. The switching is performed by Q18 and its drivers Q6 and Q7. The + SENSE is tied to the + 5v line at the load for remote sensing. The voltage across the load is compared with a reference voltage developed by the zener diode VR4 and divided by potentiometer R17. When the voltage at pin 2 of U2 is less than the voltage at pin 3 of U2, Q6 and Q7 will turn on the switching transistor Q18. The filter action of choke L2 and capacitor C9 smoothes the pulse waveform (see Figure 5-31). The voltage comparator has a small amount of hysteresis (approximately 80 mv) so that the output voltage must increase to 5.04v before Q18 will be turned off, and must decrease to 4.96v before Q18 will be turned on again.

5.4.1.2 —5v Regulator

The —5v regulator is a linear regulator which converts unregulated —15v to regulated —5v. Zener diode VR6 supplies a reference voltage that is compared by Q9 and Q10 to the output of potentiometer R33. This comparison determines the *on* state of the Darlington pair (Q11 and Q12) and maintains regulation. The —5v output may be monitored at TP4.

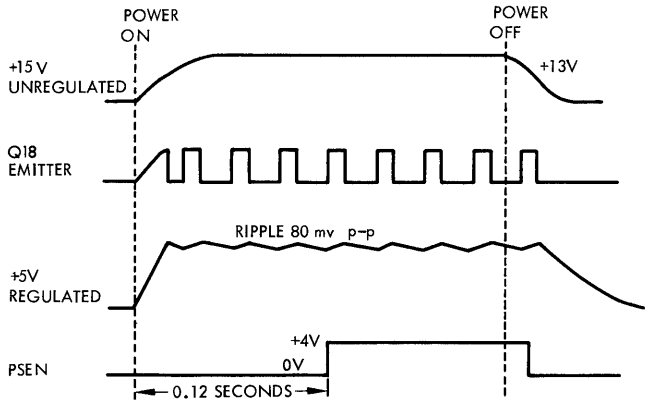


Figure 5-31. Switching Regulator Waveforms

5.4.1.3 + 20v Regulator

The + 20v regulator is a linear regulator which converts unregulated + 30v to regulated + 19.5v. The voltage across the load is compared by U1 with a reference voltage generated by the zener diodes VR1, VR8, and divided by potentiometer R3. The output of U1 causes Q2, Q3, and Q17 to maintain a + 19.5v output. The + 19.5v sense is tied to the + 19.5v line at the load for remote sensing.

5.4.1.4 Overcurrent Protection

Current to the + 5v regulator is sensed across R23 by Q8. The values of R25 and R26 are selected such that Q8 will turn on when the current to the load exceeds 14 amps. The conduction of Q8 causes SCR3 to fire, which removes the reference voltage, turning Q5 off.

It is important to note that the supply will not restart automatically when the overload condition is removed. It is necessary to turn off ac power for approximately one minute before turning power on again; this is the time required for C5, C6, and C10 to discharge and remove the holding current from SCR3.

5.4.1.5 Overvoltage Protection

If the + 5v regulator output voltage to the load exceeds + 7.5v, SCR4 will fire and the regulator will shut down via the overcurrent circuit. At + 22v SCR2 will fire and shut down the + 20v supply. The —5v supply will shut down when SCR5 fires at —7.5v.

5.4.1.6 Logic Enable (PSEN)

The logic enable signal PSEN is used to reset all formatter logic to the quiescent state. This is done while the + 5v supply is being established after power is applied and while the supply is decaying after power turns off. This ensures that the logic is in a defined state after power-on, and that no spurious signals are sent to the transport logic.

When ac power is applied, the regulated output builds up to + 5v causing C19 to charge through R42 and R43. When the voltage on C19 reaches 1.6v, Q15 and Q16 will turn on causing the output PSEN to go to + 4.5v approximately 0.12 second after power is applied.

A loss of ac power is detected by Q15 when the voltage on C19 drops below + 5v. This occurs after the absence of one-half cycle of ac power and causes Q16 to turn off and the PSEN output to go to 0v, resetting the formatter logic.

5.5 FIXED OSCILLATOR PCBAS

A fixed frequency oscillator subassembly is used on the PE Write PCBA. This oscillator consists of an etched board approximately 2.5 inches square which is attached to the PCBA by four nylon standoffs. Interconnections between the oscillator and PCBA are made by a flat cable and a 14-pin IC connector which mates with J4 on the PCBA. The subassembly can be easily removed for repair or replacement.

The oscillator generates a fixed frequency clock that controls all basic timing within the formatter. The frequency of the oscillator is controlled by a 10-turn potentiometer and is adjusted according to tape speed. The oscillator is set to 6 times the data rate at 1600 cpi, e.g.,

$$f = 6 \times 1600 \times S \times 10^{-3}$$
$$= 9.6S$$

where

f = frequency in kHz

S = tape speed in ips

For a tape speed of 37.5 ips

f = 9.6 X 37.5 = 360 kHz

One of two fixed oscillator assemblies is used. The Single Speed Fixed Oscillator (Schematic No. 102095, Assembly No. 102096) is used when all transports attached to the formatter are of the same speed. The Dual Speed Fixed Oscillator (Schematic No. 101994, Assembly No. 101995) is used when transports of two different tape speeds are attached to the formatter. The condition of the transport configuration line, ISPEED, selects one dual oscillator circuit.

For discussion of the oscillators, refer to the relevant schematic and assembly drawings which are included in Section VII of this manual.

The oscillator assembly is versioned to cover tape speeds in the range of 6.25 to 75 ips.

The basic oscillator circuit is similar for both assemblies. It consists of an emitter-coupled multivibrator circuit composed of transistors Q1 and Q2. Operating frequency of the circuit is determined by components C2, R5, and potentiometer R4. Typical waveforms for this circuit are shown in Figure 5-32. The waveform appearing at the emitter of Q2 is amplified and inverted by Q3 to form the output clock waveform.

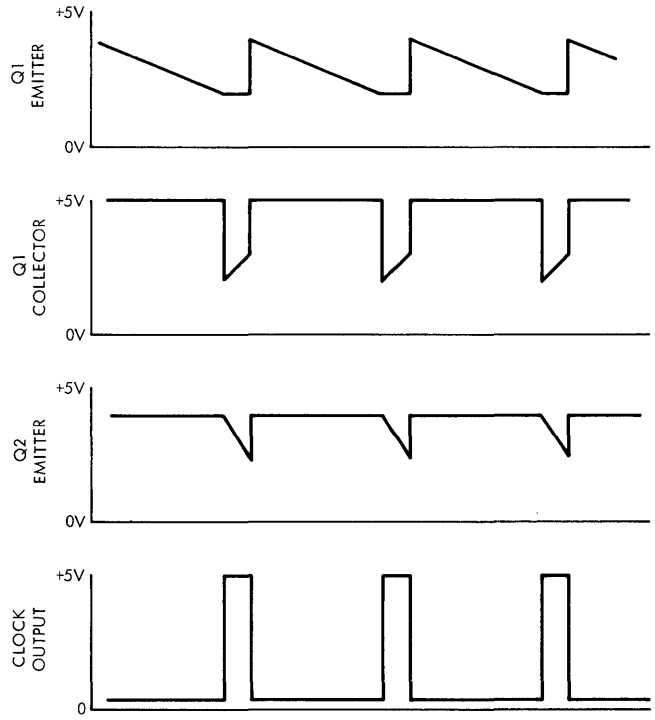


Figure 5-32. Fixed Oscillator Waveforms

The dual speed oscillator (Assembly No. 101995) contains a second oscillator circuit composed of Q5, Q6, and adjustment potentiometer R17. The outputs of the two oscillators are ORed together at the base of Q3.

The incoming control waveform ISPEED, disables one oscillator or the other by opening the emitter return of Q2 or Q6. The ISPEED line is high-true at this point; hence, oscillator Q1, Q2 corresponds to the higher tape speed (and frequency), and oscillator Q6, Q7 corresponds to the lower tape speed (and frequency).

5.6 TRACKING OSCILLATOR

A tracking oscillator subassembly is used on the PE Read PCBA. This oscillator consists of an etched board approximately 2.5 inches square which is attached to the PCBA by four nylon standoffs. Interconnections between the oscillator and PCBA are made by a flat cable and a 14-pin IC connector which mates with J4 on the PCBA. The subassembly can be easily removed for repair or replacement.

The tracking oscillator controls all timing on the PE Read PCBA. It operates in conjunction with control logic on the PE Read PCBA, and generates a clock waveform whose frequency is always 24-1/2 times the instantaneous data rate of the phase mode read signals. In effect, the oscillator tracks tape speed and allows the read logic to compensate for average and instantaneous speed variations of the transport reading the tape.

When read signals are absent, the oscillator reverts to its center frequency at approximately the center of the tracking range. The center frequency, fc, is controlled by a 10-turn potentiometer, and is initially adjusted according to the nominal tape speed, as follows.

$$fc = 24\text{-}1/2 \times 1600 \times S \times 10^{-3}$$
$$= 39.2S$$

where

fc = center frequency in kHz

S = tape speed in ips.

For example, at a tape speed of 37.5 ips

$$fc = 39.2 \times 37.5$$
$$= 1470\ kHz$$

There are two different tracking oscillator assemblies. Schematic and assembly drawings relevant to the companion formatter are included in Section VII of this manual; reference should be made to these drawings for the following discussions.

The Single Speed Tracking Oscillator (Schematic No. 102093 and Assembly No. 102094) is used when all transports attached to the formatter are of the same speed.

The Dual Speed Tracking Oscillator (Schematic No. 101989 and Assembly No. 101990) consists of two independent tracking oscillator circuits and is used when transports of two different tape speeds are attached to the formatter. The condition of the transport configuration line, ISPEED, selects one oscillator circuit or the other.

Each oscillator assembly is versioned to cover tape speeds in the range of 6.25 to 75 ips.

The circuit used is essentially the same for both assemblies; the following discussion applies to both assemblies.

The basic oscillator is an emitter-coupled multivibrator circuit consisting of transistors Q1 and Q2. Frequency is determined by components C2, R4, and potentiometer R5, and also by the dc tracking voltage applied to the base of Q1. The waveform appearing at the emitter of Q2 is amplified and inverted by Q3 to form the output clock waveform. Typical multivibrator waveforms are shown in Figure 5-33.

The tracking voltage, V_T, is varied by charging or discharging capacitors C1 and C5 under the control of two external waveforms, NER1 and NER2. The control waveforms are generated on the PE Read PCBA, and are used to servo the oscillator frequency in such a manner that there are more than 24 and less than 25 output clock pulses for each phase mode data cell. The oscillator frequency will therefore average 24.5 times the instantaneous data rate.

When NER1 is at 0v, capacitors C1, C5, and C6 begin to discharge through R12 causing the oscillator frequency to decrease. When NER2 is at 0v, C2, C5, and C6 begin to charge through R11 causing the oscillator frequency to increase.

The tracking range is defined by a voltage divider consisting of R1 and R2, and clamp diodes CR1 and CR2. R1 and R2 define a voltage of 1.6v, and the diodes limit excursions of V_T to within one diode drop of this figure. Hence,

$$V_T(\text{max}) = 1.6 + 0.7 = 2.3\text{v}$$
$$V_T(\text{min}) = 1.6 - 0.7 = 0.9\text{v}$$

This results in a tracking range of approximately $\pm$ 25 percent above the center frequency.

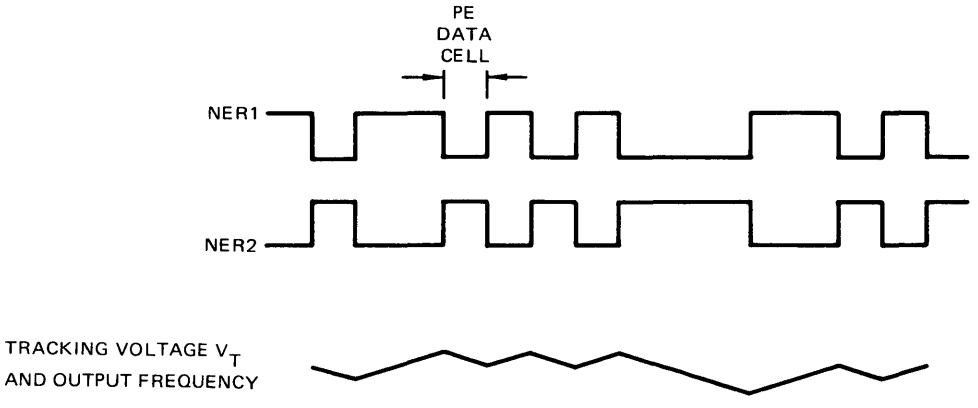


Figure 5-33. Tracking Oscillator Control Waveforms

When no data are being read, the formatter control logic holds both NER1 and NER2 to 0v. R11 and R12 now act as a voltage divider and define a voltage, V_T (center), that determines the oscillator center frequency. The ratio of R11 to R12 is chosen so that this is at approximately the center of the tracking range (~1.6v).

The maximum tracking rate is determined by components R11, C1, C5 when tracking upwards in frequency, and by R12, C1, C5 when tracking downwards in frequency. These rates are made equal and are chosen to provide the best overall system tolerance for ISV amplitude, ISV frequency, and for differences in average tape speed. A tracking rate of approximately 10 percent in 35 character periods is used on all tracking oscillators. Typical operation of the tracking oscillator is shown in Figure 5-34.

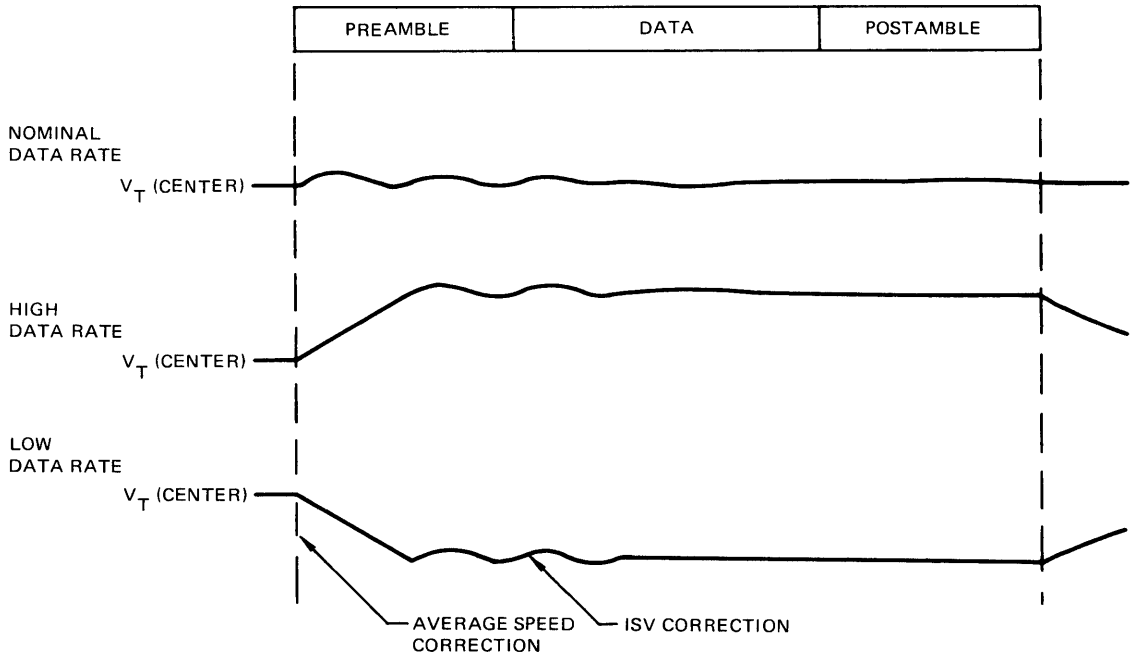


Figure 5-34. Operation of Tracking Oscillator

5.7 PE WRITE PCBA

The PE Write PCBA is one of two logic board assemblies employed in the formatter. For discussion of this PCBA refer to Schematic No. 101385 and Assembly No. 101386; Figure 5-35 illustrates the placement of each connector and test point on the PCBA.

The PE Write PCBA contains the logic used to write PE data onto tape and provides the various control and timing functions required by the formatter. Another assembly, the PE Read PCBA, contains all logic associated with reading PE data.

Both the PE Write PCBA and the PE Read PCBA are employed in formatters having full read/write capability. For a Write Only formatter, only the PE Write PCBA is required.

The PE Write PCBA performs the following major logic functions.

(1) Formatter and transport address selection.

(2) Status and configuration reporting of the selected transport to the controller.

(3) Interpretation and storage of various formatter commands.

(4) Provides the basic control and timing required for the execution of commands including the interchange of control signals with the PE Read PCBA.

(5) Write control logic.

(6) Encodes write data, preamble, and postamble patterns into phase encoded form for transmission to the transport.

Schematic No. 101385 (sheet 1) illustrates the physical layout of the PE Write PCBA. Interconnections to the controller and transport interfaces are made through two 100-pin edge connectors, J1 and J2, respectively. J1 also carries local control signals between the Write PCBA and the Read PCBA. It is important to note that pin connections at J1 and J2 are reversed at the external formatter interface connectors. For example, a signal on J1-A3 appears on J101-B3 or J103-B3 at the external connectors. Sheet 2 of Schematic No. 101385 provides identification of the signals present at J1 and J2 as referenced in the text.

Ground and +5v power connections are made through J1 and J2 in parallel. Pins B48, B49, and B50 supply the +5v; pins A48, A49, and A50 are used for ground. The PCBA draws approximately 2-1/4 amps from the +5v supply.

A removable fixed oscillator assembly is mounted at the front left of the PCBA and mates with a 14-pin IC connector, J4. The oscillator generates a clock waveform which controls the timing of all PCBA waveforms.

Selection of the internal/external Write Parity option is made on a jumper platform assembly which mates with the IC connector, J6. Other jumpers on this platform are used to ground the transport configuration lines as required when the formatter is dedicated to a particular transport type.

Three different versions of the Write PCBA, Assembly No. 101386, are required to cover the various formatter applications.

(1) Assembly No. 101386-01 — Standard version. This version consists of a PCBA with a full complement of ICs and is used in Single, Read/Write, and Write Only formatters.

(2) Assembly No. 101386-02 — Controller interface terminators omitted. This version is used in Dual PE/NRZI formatters which have separate transport interface ports.

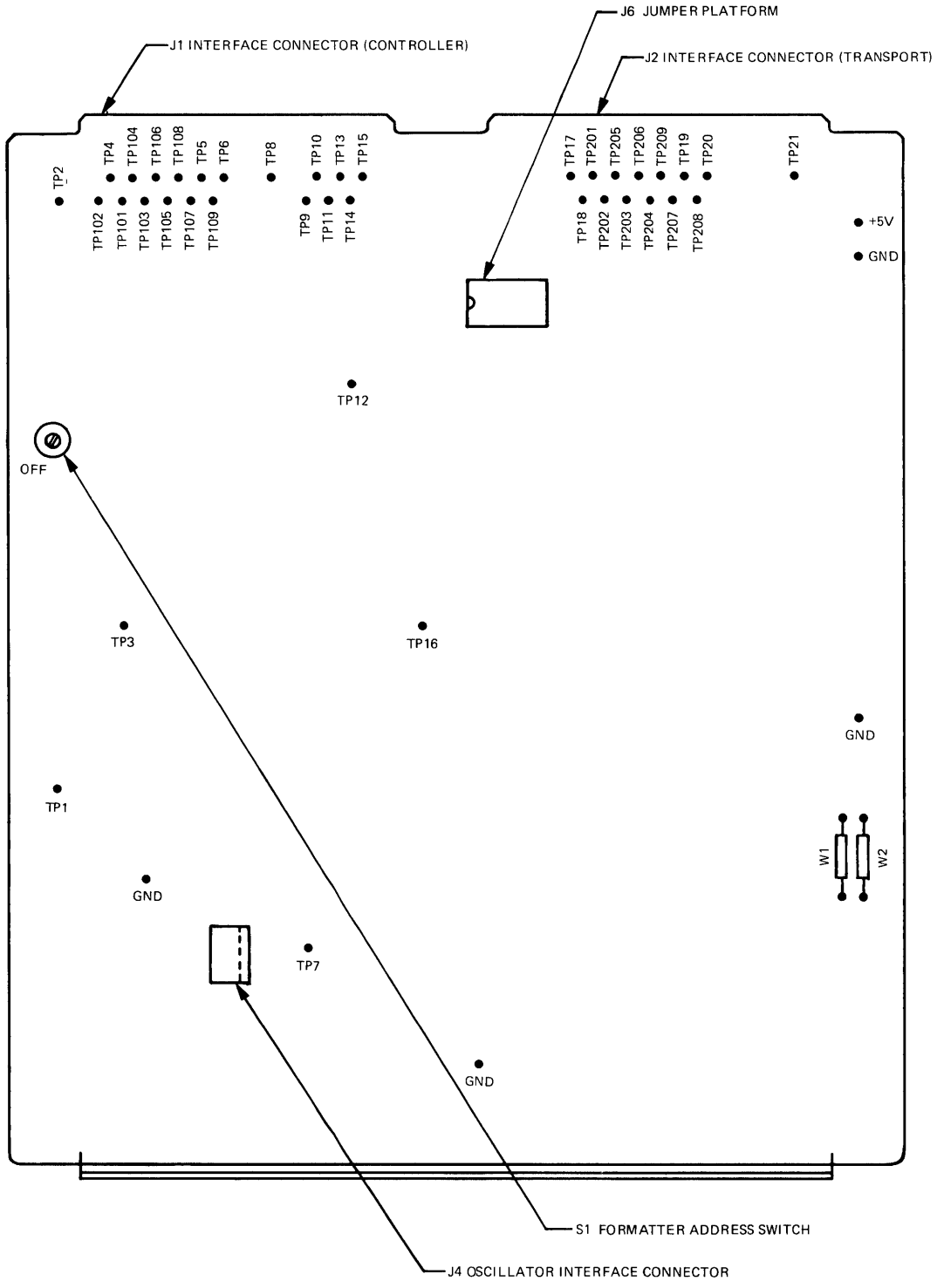


Figure 5-35. PE Write PCBA, Test Point and Connector Placement

(3) Assembly No. 101386-03 — Controller and transport interface terminators omitted. This version is used in Dual PE/NRZI formatters having a common transport interface port.

5.7.1 FORMATTER AND TRANSPORT ADDRESS SELECTION, CIRCUIT DESCRIPTION

The formatter address is preselected by a 3-position switch, S1 (sheet 3 of 6, zone H7) on the Write PCBA. The first switch position is an *off* position in which the formatter will not recognize any address. The second and third positions correspond to an address of 0 and 1, and are wired to the appropriate polarity of the formatter address line, IFAD.

When the address specified by the controller agrees with the switch setting, the switch output FSLT (formatter selected) goes high and the formatter is connected to the controller. FSLT, and its inverse NFSLT, are routed to various parts of the logic to perform the required gating.

When selected, the formatter routes the transport address lines ITAD0 and ITAD1 (sheet 3, zone G8) to four gated driver elements. These drivers decode the individual transport select lines, ISLT0-3, as follows.

ITAD0	ITAD1	Select Line
0	0	ISLT0
0	1	ISLT1
1	0	ISLT2
1	1	ISLT3

By virtue of the coding, only one of the four select lines can be true at a time. When the formatter is not selected, transport 0 (ISLT0) is always selected.

Another input to the drivers, PSEN (power supply enable) (sheet 3, zone G8) causes all select lines to be disabled when power is applied or removed from the formatter. This prevents the transports from responding to spurious signals which might occur on other interface lines during this period. Resistor R74 provides a load for the transistor that generates PSEN. Additionally, it serves as a ground to disable the formatter in the case of a broken cable.

5.7.2 TRANSPORT STATUS AND CONFIGURATION LINES, CIRCUIT DESCRIPTION

Status and configuration information from the selected transport is reported to the formatter on the following lines.

(1) Status: IRDY, IONL, IRWD, IFPT, ILDP, IEOT

(2) Configuration: INRZ, ISGL, ISPEED

The three configuration lines (sheet 3, zone C6) are provided with ground jumpers at J6 which allow the formatter to be dedicated to a particular transport type.

Each of the status and configuration lines is gated with NFSLT (formatter selected) (sheet 3, zone H6) then retransmitted through a driver element to the controller interface. When necessary, the inverse waveform is generated for internal formatter use.

5.7.3 RESET (RST)

A general reset waveform, RST, is formed by the 4-input gate, A8/8 (sheet 3, zone E7). When true, this signal causes all control logic in the formatter to be dc reset to the inactive state. This reset occurs if any one or more of the gate inputs is low, as follows.

(1) FSLT — when the formatter is not selected.

(2) NNRZ — the selected transport is not phase mode.

(3) PSEN — power is being applied to or removed from the formatter.

(4) FEN — the formatter is being reset by the controller.

Capacitor C26 provides filtering of high-frequency noise transients (less than 500 nanoseconds) which could be picked up at the interface on IFAD, IFEN, and INRZ when the system is operated in a heavy noise environment.

5.7.4 CLOCK LOGIC

Included on the Write PCBA is a fixed oscillator assembly which generates a clock waveform that controls all timing on the PCBA. The frequency is set to 6 times the phase mode data rate at 1600 cpi.

$$f = 6 \times 1600 \times 10^{-3} \times S$$
$$= 9.6S$$

where

f = frequency in kHz

S = tape speed in ips

A description of the various fixed oscillator assemblies (single and dual speed) and the relevant schematic and assembly identification number is contained in Paragraph 5.5.

The oscillator output, CLKS, is applied to a 3-stage counter that divides the input by six. The first two stages, CCTR0 and CCTR1, divide by three, and the third stage toggles CCTR1 for a further divide by two.

Typical waveforms are illustrated in Figure 5-36. The falling edge of ODD marks the boundary between adjacent phase mode data cells. Waveform ODD is true during the odd half of each bit cell, and the inverse, NODD, is true during the even half.

CCTR1 and ODD are gated together at B8/8 (sheet 4, zone D2) and the result is reinverted to form CCLK (character clock). CCLK is used to clock all timing and control flip-flops on the PCBA.

Another waveform, WCLK (write clock) (sheet 4, zone C1) is generated in a similar manner by gating CLKS, NCCTR0, CCTR1, and WCN6. The first three inputs define a pulse at the end of each half cell period, and the fourth, WCN6, enables the output during certain parts of a write command. This waveform clocks the register which encodes write data into phase mode form.

5.7.5 FORMATTER COMMANDS

The REWIND (IREW) and OFF-LINE (IOFL) commands differ from other formatter commands in that they are obeyed by the transport logic and do not cause the formatter to go busy. The IREW and IOFL lines (sheet 3, zone F8) are gated with NFSLT and retransmitted to the transport interface on IRWC and IOFC, respectively.

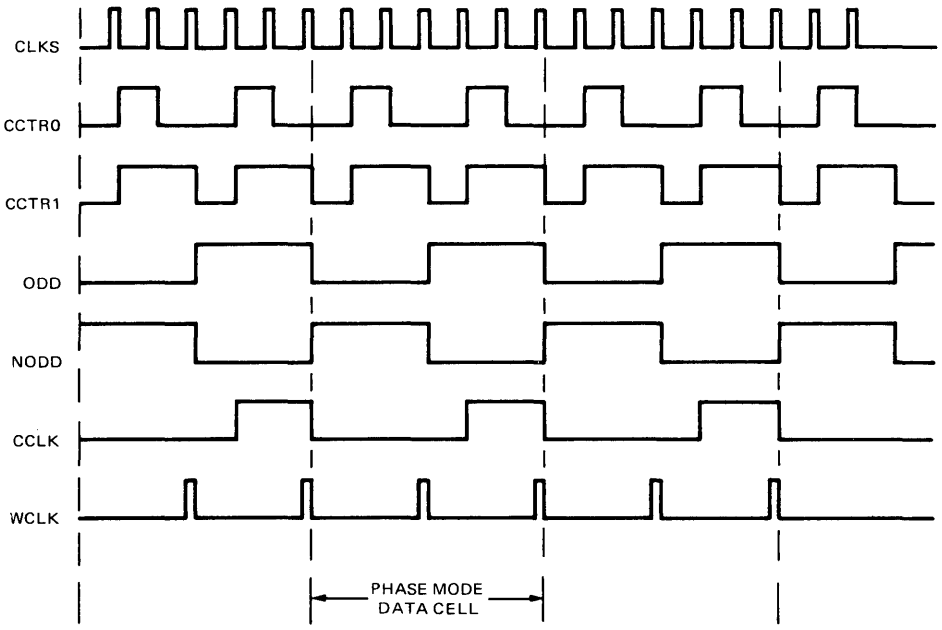


Figure 5-36. Clock Waveforms

The controller initiates other commands by setting a group of coded command lines to the required state and pulsing IGO. Coding for the various commands is shown in Table 3-1.

IGO (sheet 4, zone G8) is gated with DCN5 (formatter ready for new command) and RDY (selected transport ready), then inverted to form the GOP (GO pulse). GOP is a high-true pulse that is connected to the clock inputs of a 7-stage command register (sheet 3, zone H2). On the falling edge of GOP each command line is copied into a corresponding register stage. The command remains stored in the register until it is either overwritten by the next command, or the register is dc reset by NRST.

Outputs from the command register control the various formatter operations, and in some cases serve as control signals to the transport interface (ISWS, IREV, IOVW, IRTH1, and IRTH2).

Initial synchronization with CCLK is performed by flip-flops GO1, GO2 (sheet 4, zone H6) and DCN5. Typical waveforms are shown in Figure 5-37. GO1 is clocked true by the falling edge of GOP and causes GO2 to set on the trailing edge of the next CCLK pulse. One clock time later, DCN5 sets and GO2 is reset via the K input. DCN5 now dc resets GO1 and disables GOP, preventing the formatter from recognizing any further commands until the current command is completed. Thus, GO2 consists of a single pulse, one clock period wide at the beginning of each formatter command.

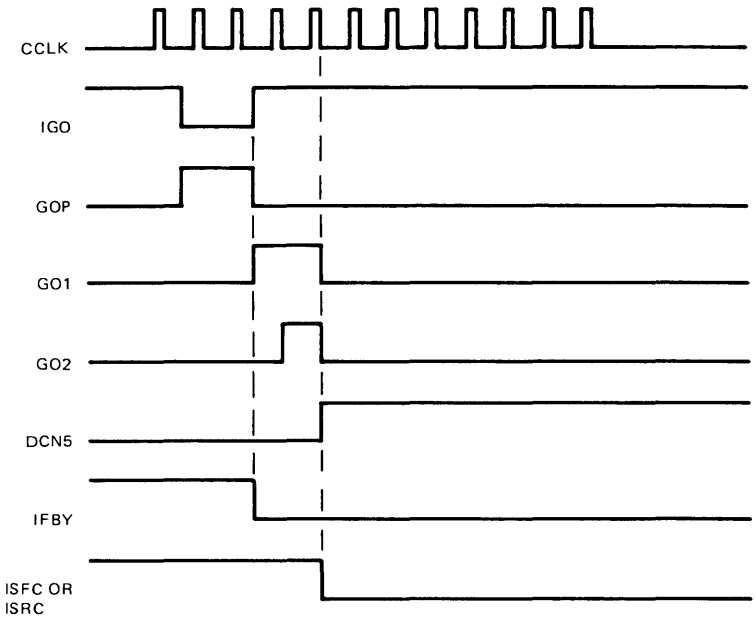


Figure 5-37. Command Initiation Waveforms

5.7.5.1 Delay Logic

All commands (except Rewind and Off-line) are executed as follows.

(1) A pre-record delay is generated during which time the tape ramps up to speed and traverses the IBG.

(2) Data transfer then takes place under the control of the read and/or write logic.

(3) On completion of the command, a post-record delay is generated which determines head positioning in the IBG after the record.

(4) Finally, a rampdown delay is generated during which the tape decelerates to rest.

Different pre- and post-record delays are required for the various formatter commands. All delays are scaled to the required tape speed by selecting the appropriate oscillator frequency. Table 5-1 lists these delays and shows specific values at a number of common tape speeds.

The delays are generated by a counter circuit consisting of four control flip-flops (DCN1-4) (sheet 4, zone F3-6), a 16-bit ripple counter (DCTR1-16) (sheet 4, zone A3-7), a number of decoding gates, and associated logic. DCN1 is used for generation of the long pre-record delays associated with reading or writing from BOT, and DCN2 for the normal pre-record delays. DCN3 and DCN4 control the post-record and rampdown delays, respectively.

The gates decode counts equivalent to the various delays and are selected by suitable inputs from the control flip-flops and command register. Only one gate can be enabled at a time. The gate outputs are ORed together then connected to the J input of flip-flop DP (sheet 4, zone C4).

Table 5-1

Formatter Delays

	Delay	Control Flip Flop	Gate	Tape Speed (ips)						
				6.25	12.5	18.75	25	37.5	45	75
Pre-Record Delays (msec)	Read from BOT	DCN1	C6/6	2.556	127.8	85.2	63.9	42.6	35.5	21.3
	Write from BOT	DCN1	C6/8	1023.6	511.8	341.2	255.9	170.6	142.2	85.3
	Read Fwd or Rev	DCN2	D7/6	51.0	25.5	17.0	12.7	8.5	7.08	4.25
	Write (Single Stack)	DCN2	D6/8	89.4	44.7	29.8	22.3	14.9	12.4	7.45
	Write (Dual Stack)	DCN2	D6/6	67.2	33.6	22.4	16.8	11.2	9.33	5.6
	Write File Mark	DCN2	D7/8	614.4	307.2	204.8	153.6	102.4	85.3	51.2
Post-Record Delays (msec)	Read Fwd	DCN3	C5/6	0.3	0.15	0.1	0.075	0.05	0.042	0.025
	Read Rev	DCN3	D5/6	12.6	6.3	4.2	3.15	2.1	1.75	1.05
	Read Rev (Edit)	DCN3	D5/8	22.2	11.1	7.4	5.55	3.7	3.08	1.85
	All Write Commands	DCN3	C5/8	12.6	6.3	4.2	3.15	2.1	1.75	1.05
	Rampdown Delay (msec)	DCN4	D4/6	76.8	38.4	25.6	19.2	12.8	10.67	6.4

Phase Mode Data Rate (kHz)	10	20	30	40	60	72	120
Fixed Oscillator Frequency (kHz)	60	120	180	240	360	432	720
Transport Start/Stop Ramp (msec)	60	30	20	15	10	8.3	5

The ripple counter is initially clamped to the reset state by a false signal on DCNT (sheet 4, zone B3). When one of the control flip-flops is set, the 4-input gate C8/6 (sheet 4, zone B3) goes true and sets DCNT. The counter is now enabled and proceeds to count CCLK pulses (one every PE data cell) until the required delay has been accomplished.

When the required count is reached, the selected gate operates and a pulse is generated on DP during the following clock time. The counter is immediately reset by NDP on C3/1 (sheet 4, zone A8) and the control flip-flop is reset at the end of the same clock time. DCNT now goes false, reapplying the clamp to the counter, and the delay cycle is completed.

The counter circuit is also used to generate the 40-bit preamble and postamble patterns required during write operations. Control waveform (WCN1 + 5) (sheet 4, zone C4) and decoding gate D4/8 are used in this case.

5.7.6 COMMAND EXECUTION, CIRCUIT DESCRIPTION

Refer to Figure 5-38 in conjunction with Schematic No. 101385 for the following description. Upon receipt of a command, NGO2 causes either DCN1 or DCN2 to set, depending on whether or not the tape is at Load Point. The pre-record delay is then generated as described in Paragraph 5.7.5.1. The DP pulse for this delay is gated through B5/8 (sheet 4, zone F4), E8/4, and B6/4 to form the waveforms SP and SWP. SP consists of a pulse at DP time which marks the end of the pre-record delay for all commands. SWP is a similar waveform for write commands only.

At this time either the Read PCBA is enabled by IRGATE, or the write logic is enabled by SWP, and the required data transfer takes place. When operating with a transport utilizing a dual stack head, both the read and write logic are enabled simultaneously, and a read-after-write data check takes place.

The end of data transfer is signaled by a pulse on REND (read end) or WEND (write end) from the read or write control logic. The combination AND/OR GATE B5/6 (sheet 4, zone G4) selects one or the other of these signals to initiate the post-record delay, as follows.

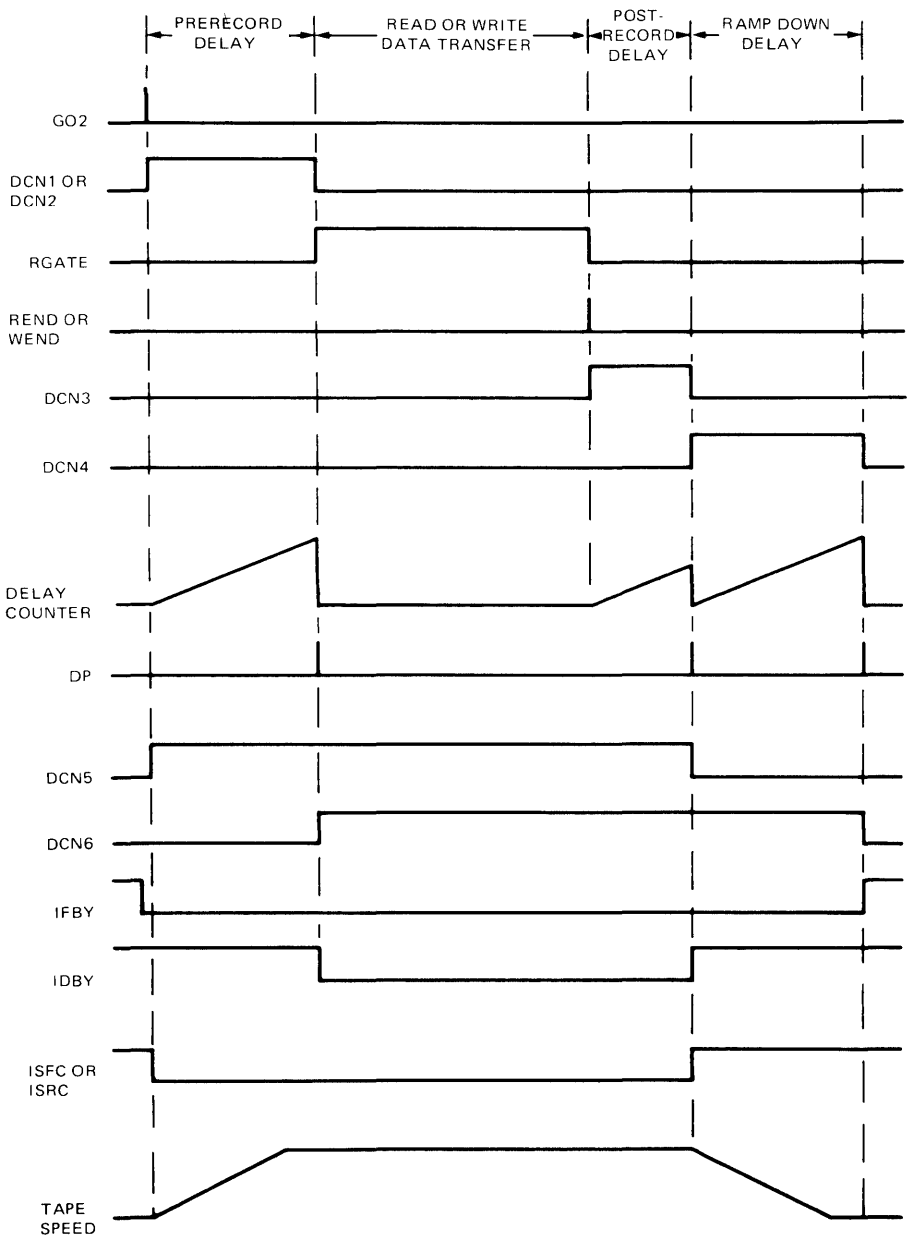


Figure 5-38. Command Timing

(1) WEND
- Single Stack. All write commands.
- Dual Stack. Erase commands only.

(2) REND
- Single Stack. All read commands.
- Dual Stack. All read and write commands, except erase.

During a read-after-write operation, the waveform NWCN7 at B5/3 (sheet 4, zone G4) inhibits any spurious REND pulse that could occur (because of tape dropouts, etc.) until the complete record has been written. B5/6 now sets DCN3 via the present input, and the appropriate post-record delay is generated. At the end of this delay DCN3 and the counter are reset, and DCN4 is set by B6/13 (sheet 4, zone F3). The rampdown delay is now generated during which the tape decelerates to rest. At the end of this period, execution of the current command has been completed, and the logic reverts to the idle state until the next command is received.

5.7.6.1 Control Waveforms

Flip-flops DCN5 (sheet 4, zone G4) and DCN6 assist in the generation of other formatter waveforms. DCN5 is set by GO2 at the beginning of a command, and reset at the end of the post-record delay. It represents the times during which tape motion is required. DCN6 is set at the end of the pre-record delay, and reset at the end of the rampdown delay.

The following waveforms are derived from DCN5 and DCN6.

(1) FBY (Formatter Busy) (sheet 4, zone G1). Formed by ORing GO1, DCN5, and DCN6 at B7/8. FBY goes true coincident with the trailing edge of GO and remains true until the command has been fully executed. The controller will normally make use of this waveform to inhibit further commands. It can be used to verify that a command has been accepted by the formatter logic.

(2) DBY (Data Busy) (sheet 4, zone G1). DCN5 and DCN6 are gated at C7/13 to form this waveform. DBY goes true when the read or write data transfer begins, and resets when a stop command is given to the transport. The trailing edge of this waveform informs the controller that the transfer is somplete, and that all errors have been reported.

(3) RGATE (Read Gate) (sheet 5, zone C1). This is the enable signal to the Read PCBA. RGATE is formed at E2/6 and D2/6 by gating DBY, NDCN3, and the output of C3/6. It is true from the end of the pre-record delay to the beginning of the post-record delay for all read commands (single or dual stack), and for write commands on a dual stack head (read-after-write).

(4) SFC and SRC (Tape Motion Commands) (sheet 3, zone H1). SFC and SRC are formed by gating DCN5 with the appropriate polarity of the Forward/Reverse command flip-flop at C7/10 and C7/4, respectively. SFC causes forward tape motion, and SRC causes reverse tape motion.

5.7.6.2 On-the-Fly Operation

The controller may issue a new command to the formatter during the rampdown delay (after DBY has gone false) provided that the new command is in the same read/write and forward/reverse status as the previous one. The controller must furnish the logic necessary to detect these conditions. This results in a time saving of up to one ramp time (the rampdown delay) per command. Figure 5-39 illustrates the waveforms encountered during an on-the-fly operation.

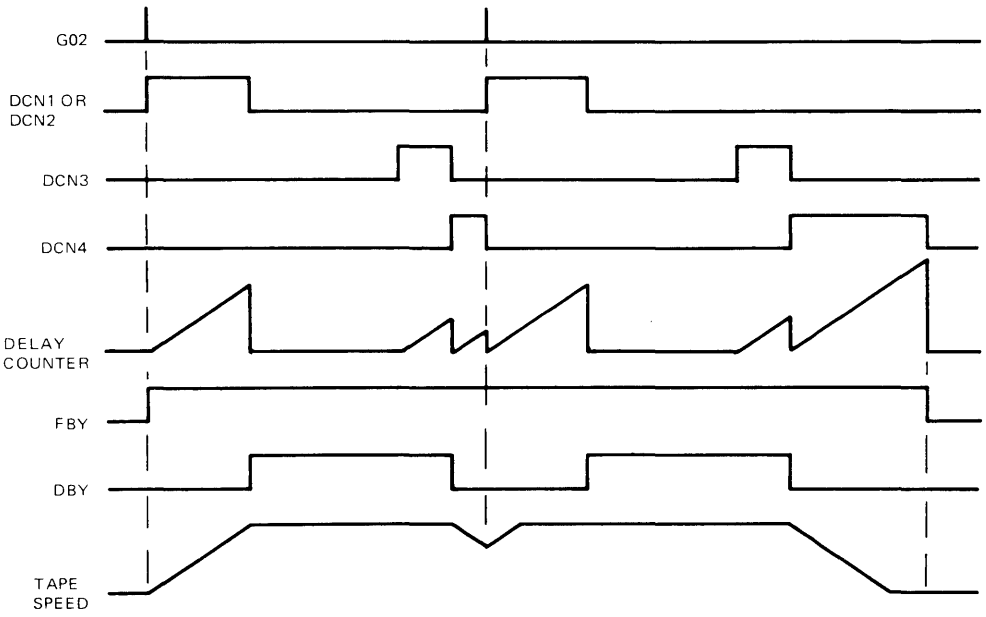


Figure 5-39. On-the-Fly Operation

In this mode DCN4 (sheet 4, zone F3) and DCN6 are still set when the new command is issued. GO1 resets these flip-flops via OR gate B6/1 (sheet 4, zone E5) and the remainder of the rampdown delay is canceled. At the same time DCNT goes false and the delay counter is reset. DCN1 now sets, and the pre-record delay for the new command is generated in the normal manner.

FBY is held true continuously during on-the-fly operation and resets only when the rampdown delay times out.

5.7.6.3 Identification Timing

When writing from BOT, a PE identification burst is recorded on tape in the vicinity of the BOT tab. When reading from BOT, the read logic tests for the presence or absence of this burst and reports the result to the controller. These operations take place automatically during the pre-record delay and are closely associated with the delay counter timing.

Flip-flops ID (E3/15) (sheet 5, zone E3) and IDT (E3/11) are used to generate the identification waveforms. Figure 5-40 is a detailed timing diagram of the identification waveforms.

ID is initially clamped to the reset state by gates D3/13, C3/11, and E8/6. It is enabled when DCN1 is true, provided that DCTR13 and DCTR14 are both reset. A false signal on ID causes IDT to reset.

When a read or write command is issued at BOT, DCN1 goes true, ID is enabled, and the appropriate pre-record delay begins. ID is set true by the first falling edge on DCTR7 after DCTR10 goes true. This occurs shortly after the tape has reached operating speed. IDT is now enabled, and is set by the first falling edge on DCTR8 after DCTR12 goes true.

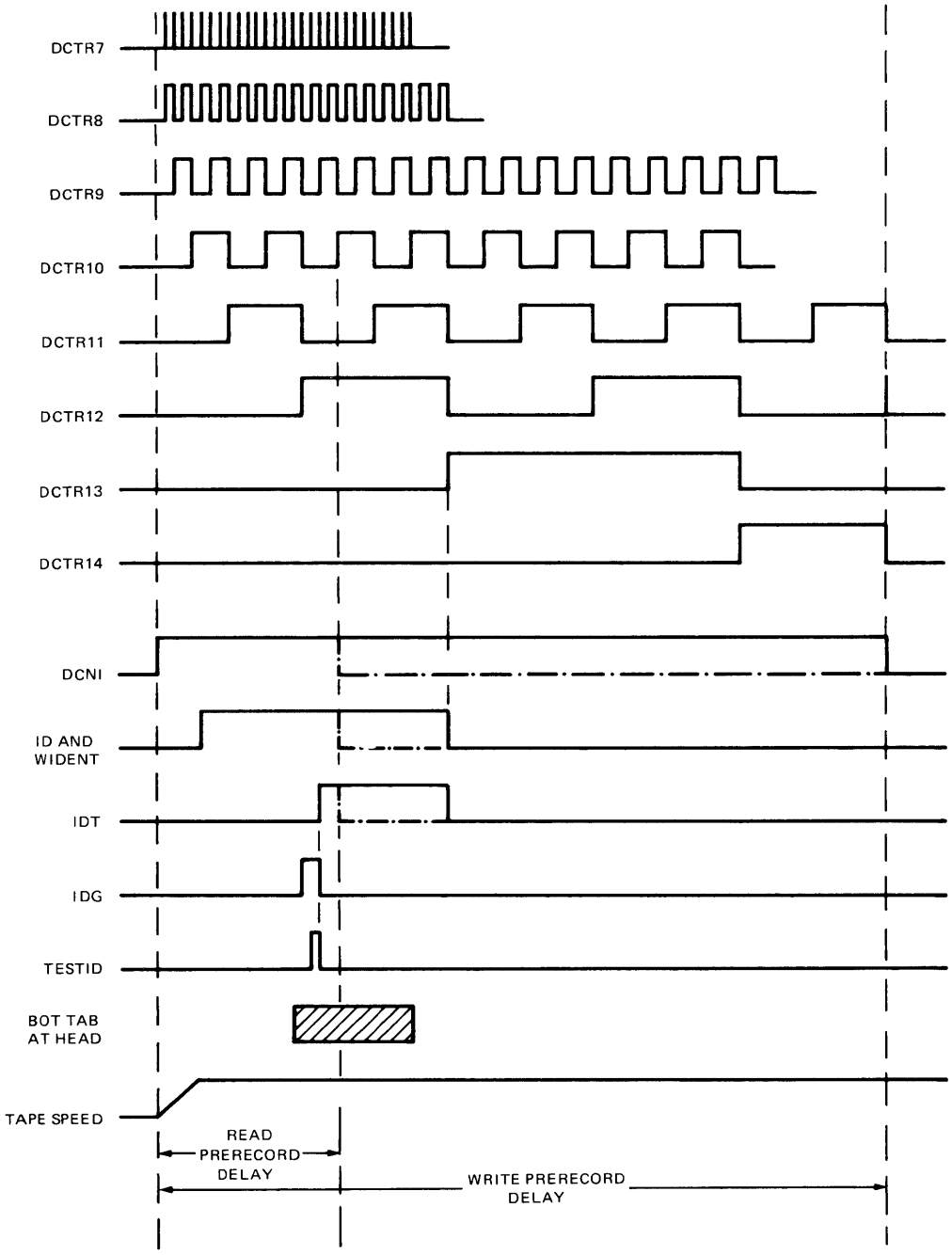


Figure 5-40. Identification Timing, Read and Write

ID and IDT remain set until cleared at the following times.

(1) Read commands. When DCN1 resets at the end of the read pre-record delay.

(2) Write commands. When DCTR13 sets. During the remainder of the delay DCTR13 and DCTR14 inhibit further operation of the circuit.

A control signal, WIDENT, is formed by gating ID and WRT at D3/10 (sheet 5, zone D3). This signal goes true during write commands when the tape reaches operating speed, and remains true until the BOT tab moves past the read/write head. The PE identification burst is written onto tape during this time.

The PE Read PCBA requires two signals, IDG and TESTID, for the identification test. IDG (E2/8 and D2/8) (sheet 5, zone B2) is generated by gating ID, NIDT, and DCTR12, and goes true for a short time as the BOT tab moves over the read head. TESTID (D3/4, sheet 5, zone C2) is a gate of IDG and DCTR8 and is true during the latter half of IDG. IDG and TESTID are both disabled by C3/6 when writing on a dual stack transport.

IDG partially enables the read logic so that the presence or absence of identification data can be detected. TESTID performs the required test.

5.7.7 WRITE CONTROL LOGIC, CIRCUIT DESCRIPTION

The control and timing functions required during execution of write commands are performed by this logic.

Basic timing is achieved by two sets of flip-flops, WCN-5 and WCN6-7 (sheet 5, zone G2-7). WCN1-5 set in turn and define the times during which the preamble, data, and postamble patterns are written. WCN6-7 form suitable gating waveforms for the generation of clock, strobe, and control patterns. The flip-flops have a common clock input, CCLK (one pulse each data cell), and are clamped to the reset state by DCN5 when not in use.

Figure 5-41 details the timing waveform of the write control logic. At the end of the pre-record delay, WCN1 is set true by SWP. (WCN1 + 5) goes high and the delay counter logic is enabled. The counter now counts 40 data cells which is the equivalent to the preamble zero bits. During the fortieth cell DP goes true causing WCN1 to reset, and WCN2 to set.

WCN2 remains true for one cell-time (preamble one bit), then WCN3 sets. During the following cell times write data from the controller is copied character-by-character into the write data logic. WSTR (sheet 5, zone B6) signals the controller when each character has been transferred.

When the last data character is transmitted the controller sets LWD (sheet 5, zone G7) true. At the end of this cell time WCN3 resets and WCN4 sets. WCN4 and WCN5 now time out the postamble one bit, and the 40 postamble zero bits, respectively.

During a WRITE FILE MARK command, WCN2-5 are clamped reset by the connection of WFM to H10/3 (sheet 5, zone F7). In this case only the 40-bit preamble pattern will be generated.

Note that WCN1-5 correspond to the times during which data is presented to the encoding logic. Each bit is encoded and recorded onto tape during the following cell time.

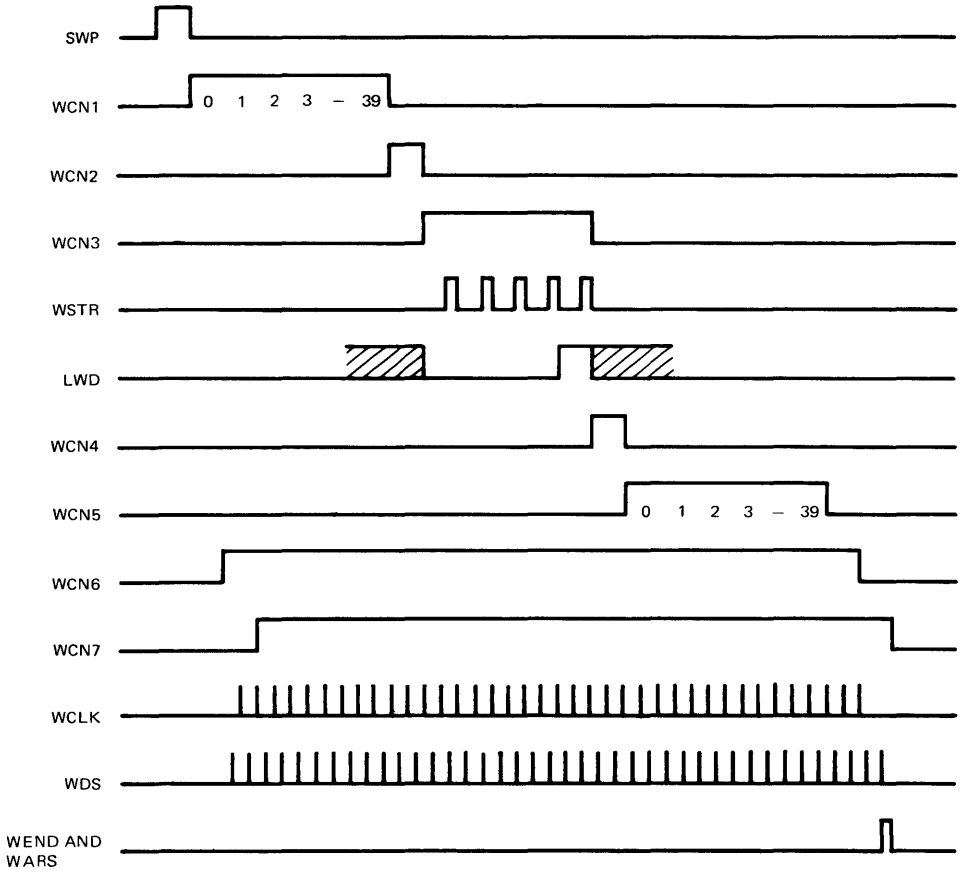


Figure 5-41. Write Sequence

The input to WCN6 is formed by ORing together the times at which data patterns are recorded on tape. WCN1-5 are ORed at G8/8 (sheet 5, zone F4), then this is ORed with WIDENT, the time when the PE identification burst is to be written. The resulting waveform is delayed one cell time each by WCN6 and WCN7, to form the required gating waveforms.

In addition to the signals and waveforms previously discussed, the following interface waveforms are generated by the write control logic.

(1) WSTR (sheet 5, zone B6). This signal controls the transfer of write data from the controller to the formatter. It is formed by gating CCLK and WCN3 at E13/1. The controller should set up the next character on, or within, a half-cell time after the trailing edge of each WSTR pulse.

(2) WDS (sheet 5, zone D6). This pulse is formed by H9/11, H11/4, and G12/1. It consists of a pulse at the center of each half cell period when either WCN6 or WCN7 is set. It is used to copy the 9 channels of phase encoded data into the tape transport logic. The connection of NERASE to H9/12 inhibits this waveform during erase commands.

(3) WARS (and WEND) (sheet 5, zone C6). This signal is formed by gating CCLK, WCN7, NWCN6, and NDCN1 at C8/8 and G12/4. It consists of a pulse at the end of the write sequence just after the last postamble bit has been recorded. WEND is used to initiate the post-record delay. WARS is employed to turn off write current in the selected transport when a WRITE (Edit) command is performed.

NOTE

Presence of DCN1 on C8/12 prevents generation of a pulse when the identification burst is written.

The following are control waveforms which are generated by the write control logic for the write data logic of the formatter.

(1) WCLK (sheet 4, zone C1). This waveform is described in Paragraph 5.7.4.

(2) NWTOG (sheet 5, zone G1). This is formed by gating WCN6 and NODD at E11/6. It is low during the even (first) half of each bit cell when WCN6 is set.

(3) NWONES (sheet 5, zone F1). This is formed by H9/3, G8/6, and H8/2. WIDENT and DCTR1 are first gated at H9/3 to form the identification data pattern (0101). The output of H9/3 is then ORed with NWCN2, NWCN4, and NWTOG at G8/6. The result is inverted to form NWONES. This waveform is low during the even half cell if a zero bit (preamble, postamble, or identification) is to be recorded, or is low for the complete cell time if a one bit is to be recorded. Waveforms for NWTOG and NWONES are shown in Figure 5-42.

(4) NWRES1 (sheet 5, zone G1). This is the reset line for Channels 0, 2, 5, 6, and 7 of the encoding register. It is formed by gating WCN6 and NDCN1 at H9/6. These channels are enabled when WCN6 is set (data is being recorded onto tape), except during the pre-record delay.

(5) NWRES2 (sheet 5, zone F1). This is the reset line to Channels 1, 3, and 4 of the encoding register, and is formed by gating NWRES1 and WFM at H10/10. These channels are enabled when WCN6 is set, except during the pre-record delay or a WRITE FILE MARK command.

The sequence of events which occur during the execution of different write commands can be summarized as follows.

(1) WRITE (Normal) / WRITE (Edit). At the end of the pre-record delay, the preamble, data, and postamble patterns are generated and recorded onto tape. WEND (or REND for a dual-stack head) initiates the post-record delay, then a stop command is given to the transport. The head comes to rest further into the IBG for a write command than for a read command.

(2) WRITE From BOT. At the beginning of the pre-record delay WIDENT causes the PE identification burst to be written (see Figure 5-40). This consists of a 0101 pattern written only on Channel P, with the other channels erased. A read-after-write test for identification is also performed on transports utilizing a dual stack head. Approximately 3-1/2 inches of tape is then erased before the pre-record delay times out. The first data record is then written in the normal manner.

(3) WRITE FILE MARK. A long pre-record delay is generated (equivalent to a 3-1/2 inch gap), then a file mark pattern is recorded. This consists of 40 zero bits on Channels P, 0, 2, 5, 6, and 7 with the other channels erased.

(4) ERASE (Variable) / ERASE (Fixed). These commands are executed in the same manner as a WRITE or a WRITE FILE MARK command, respectively. In this case, WDS is inhibited and no data is copied into the transport electronics. The equivalent length of tape is erased.

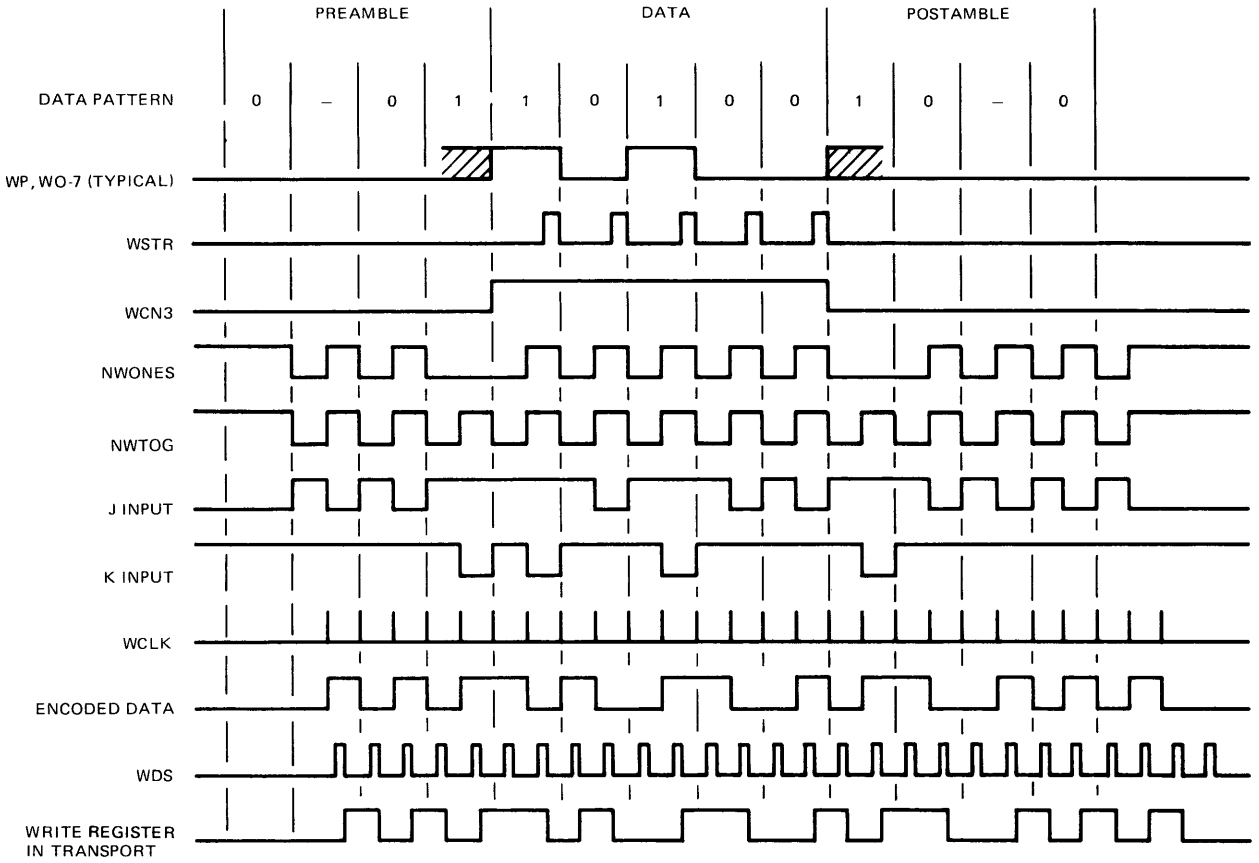


Figure 5-42. Write Data Encoding

5.7.8 WRITE DATA LOGIC, CIRCUIT DESCRIPTION

The incoming write data lines from the controller (IWP, IW0-7) (sheet 6, zone G8-B8) are terminated, then inverted to form WP, W0-7. W0-7 are fed to a parity generator which forms the odd parity bit, WPAR, for the eight data bits. Either WPAR, or the parity bit specified by the controller, WP, can be selected for writing on tape by suitable jumper connections on J6.

W0-7 and the selected parity are then fed to nine encoding circuits which add preamble, postamble, and identification information as required, and encode the result into phase mode form. The circuit for Channel 0 will be used as an example in the following description. Refer to Figure 5-42 for the appropriate waveforms.

Controller data (W0) is first gated with WCN4 at C11/8 (sheet 6, zone G5). The output of this gate goes low when a one bit is being transmitted. During the preamble, postamble, and identification times this gate is disabled (WCN3 false) and zero bits will normally be recorded onto tape.

Encoding is performed by two gates (D11/8 and D10/6) (sheet 6, zone F4), and a flip-flop (F10/15) which is clocked each half-cell time by WCLK when encoding is required. The encoding method is as follows.

(1) At the end of each cell the condition of the data bit to be recorded (0 or 1) is copied into the encoding flip-flop.

(2) A half-cell time later (center of the following cell) the flip-flop is toggled to the opposite state.

(3) At the end of this cell the next bit is copied, and the process is repeated.

The copy/toggle action is controlled by two waveforms, NWONES and NWTOG, from the write control logic (refer to Paragraph 5.5.5). During the odd half-cell these waveforms are normally high and the value of the data bit, and its inverse, are routed to the J and K inputs, respectively. One bits (for the preamble, postamble, and identification) are introduced by holding NWONES low during this time. This information is copied into the flip-flop by WCLK at the end of the half-cell period (at the cell boundary).

During the even half-cell of the next cell time, NWONES and NWTOG force the J and K inputs high and the toggle action takes place.

When not in use, the nine encoding flip-flops are clamped to the reset state by WCN6, NWRES1, and NWRES2. When a data record is to be written, these signals go true and encoding takes place on all channels. For a WRITE FILE MARK command, NWRES2 remains low causing Channels 1, 3, and 4 to be erased. A file mark pattern (40 zeros) is encoded on the other channels. When writing identification, NWRES1 and NWRES2 are both low, and the identification pattern (0101) is encoded for Channel P only. The remaining channels are erased.

Encoded data for the 9 channels is routed through driver elements to the transport interface lines, IWDP, IWD0-7. This information is copied into a write register in the selected transport by IWDS, then recorded onto tape.

5.8 PE READ PCBA

The PE Read PCBA is one of the two logic board assemblies employed in the PE Formatter. For discussion of this PCBA, refer to Schematic No. 101380 and Assembly No. 101381; Figure 5-43 illustrates the placement of each connector and test point on the PCBA.

The PE Read PCBA accepts phase encoded signals from tape in IBM format, converts this information, and transmits the result to the controller interface. Basic operations include the removal of preamble and postamble patterns, data decoding, deskewing, error detection, and error correction. The PCBA is designed for use with PERTEC PE Tape Transports at tape speeds from 6.25 to 75 ips.

In most formatter applications this PCBA is used in conjunction with the PE Write PCBA (Assembly No. 101386). A number of internal control signals are interchanged between the two boards.

Schematic No. 101380 (sheet 1) illustrates the physical layout of the PE Read PCBA. Interconnections to the buffer and transport interfaces are made through two 100-pin connectors, J1 and J2, respectively. J1 also carries the internal control connections to/from the PE Write PCBA. Note that pin connections at J1 and J2 are reversed at the external formatter interface connectors. For example, a signal on J1-A37 appears on J101-B37 or J103-B37 at the external interface.

Sheet 2 provides identification of the signals present at J1 and J2 as referenced in the text.

Ground and +5v power connections are made through J1 and J2 in parallel. Pins B48, B49, B50 supply the +5v, and pins A48, A49, A50 are used for ground. The PCBA draws approximately 3.25 amps from the +5v supply.

A removable tracking oscillator assembly is mounted at the rear left of the PCBA and mates with a 14-pin IC connector, J4. The oscillator tracks variations in tape speed and compensates the read logic timing accordingly.

A monitor socket, J5 (sheet 3, zone G5), is provided for maintenance purposes. The various error conditions are wired to this socket and can be individually displayed by use of an oscilloscope.

Three different versions of the PE Read PCBA (Assembly No. 101381) are required to cover the various formatter applications.

(1) Assembly No. 101380-01 — Standard version. This version consists of a PCBA with a full complement of ICs and is used for single PE Formatters and for dual PE/NRZI Formatters which have separate transport interface ports.

(2) Assembly No. 101380-02 — Transport Terminators Omitted. This version is used on Dual PE/NRZI Formatters having a common transport interface port.

(3) Assembly No. 101380-03 — Internal Control Terminators Omitted. Special applications only.

The read logic consists of 9 channels of data logic, and a group of control logic which supervises the reading of each data record.

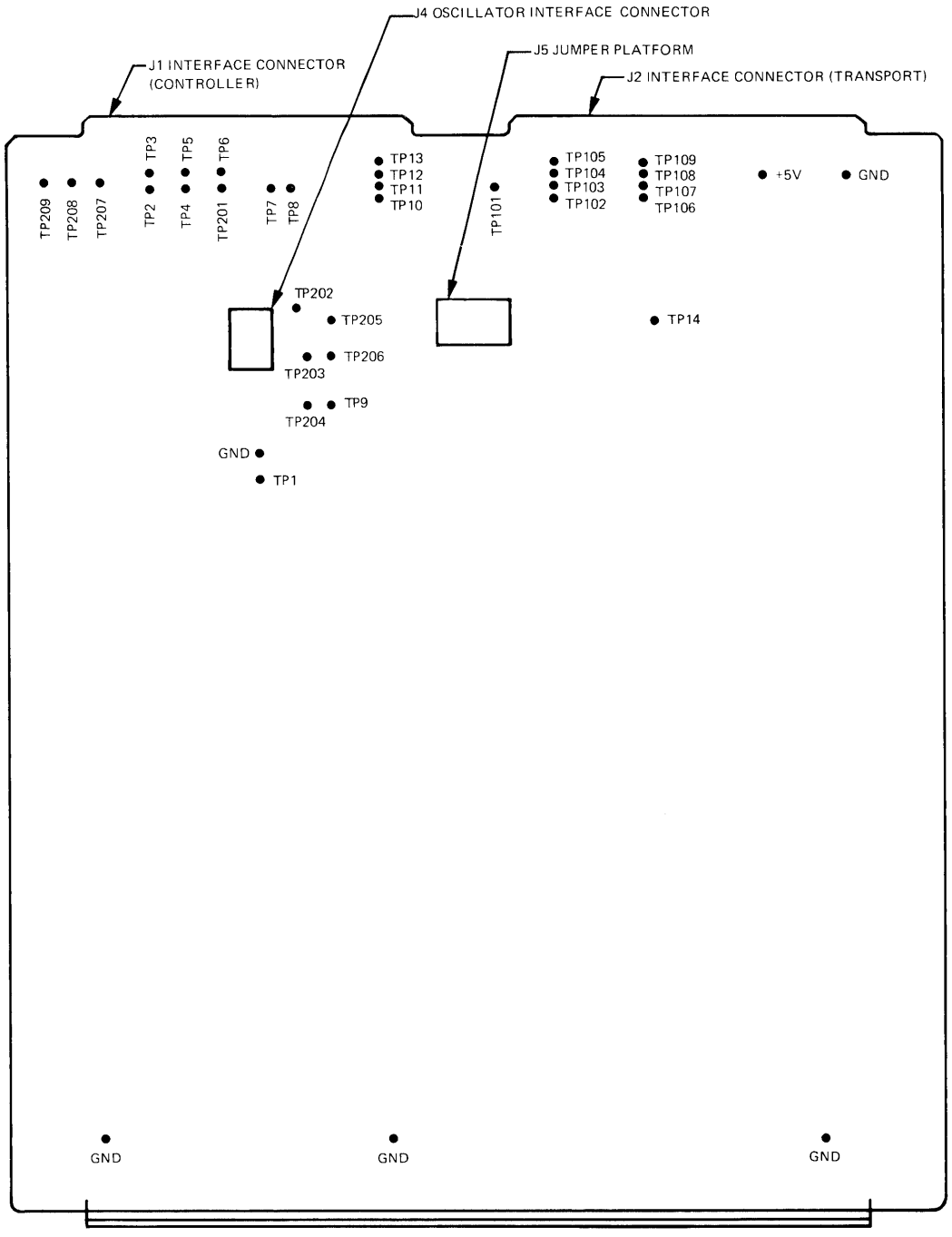


Figure 5-43. PE Read PCBA, Test Point and Connector Placement

The design is entirely digital and is based on a tracking oscillator which compensates the read logic timing for average and instantaneous variations in tape speed. The oscillator servos on incoming data such that its frequency is 24-1/2 times the instantaneous data rate (there are nominally 24-1/2 clock pulses (RCLK) in each phase mode data cell). The oscillator frequency is high in relation to the data rate to achieve the required decoding resolution. Descriptions of the oscillator and tracking control logic are contained in Paragraphs 5.3 and 5.4.

5.8.1 READ DATA INPUT

The transport electronics contains threshold and envelope circuits which require that read signals exceed a minimum amplitude, and persist for four consecutive cell times before being recognized as genuine data. The first four bits of preamble are therefore not transmitted to the formatter logic.

The transport read data lines, IRDP, IRD0-7 (sheet 3, zone B/E7, G8) are terminated and then fed to one input of a set of nine exclusive OR elements. The second input is controlled by IREV (from the Write PCBA), and causes the data to be either inverted or not, depending on whether the tape is moving in the forward or reverse direction. As a result, any given flux transition on tape appears at the output (IRDP, IRD0-7) as the same change in signal polarity, regardless of tape direction. This is illustrated in Figure 5-44.

In particular, the data transition for a zero bit appears as a change from low to high, and the data transition for a one bit appears as a change from high to low.

Operation of the remainder of the read logic is independent of tape direction. Note that the roles of the preamble and postamble are interchanged when reading reverse.

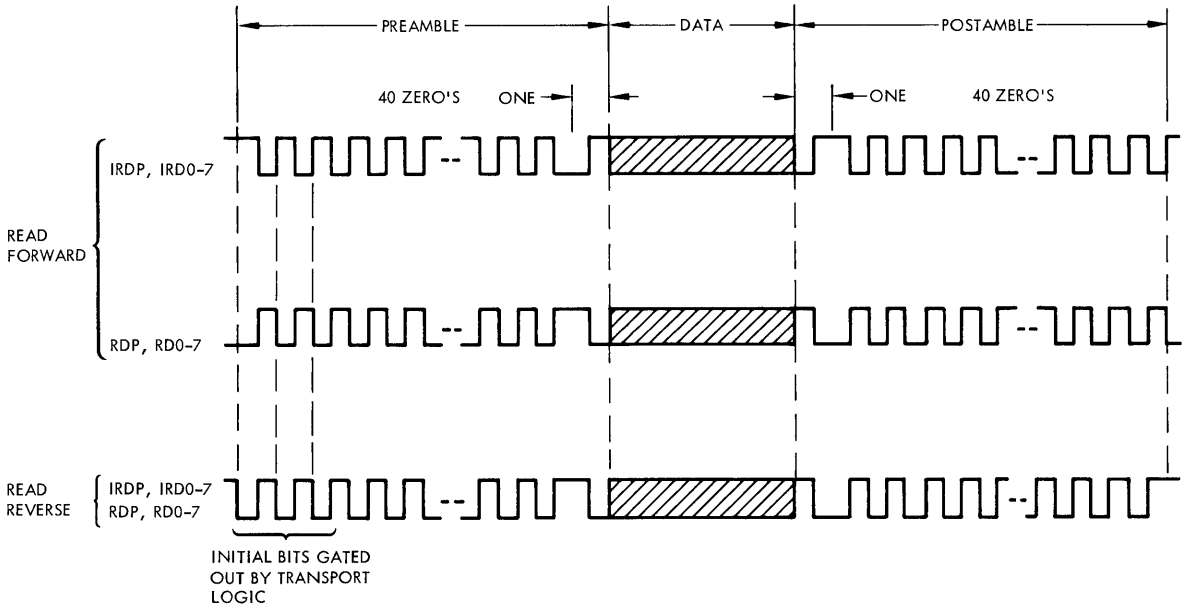


Figure 5-44. Read Input Signals

5.8.2 DATA CHANNEL LOGIC, CIRCUIT DESCRIPTION

IRDP, IRD0-7 feed 9 sets of data logic which process the information from each track separately. Operation of the data channel logic is discussed with reference to circuit 100 shown on sheet 4.

The logic is divided into two parts:

(1) Decoding and Deskewing. This includes data decoding, envelope and dropout detection, a 4-bit skew register (S1-4) (sheet 4, zone E4), and a control register. It accounts for most of the channel logic. The timing of this logic is closely associated with incoming data, and operates independently of the other channels.

(2) Parallel Buffer and Error Correction. This consists of a 2-bit buffer (D1-2) (sheet 4, zone E3), and gating logic for the insertion of error corrected data. Considering the 9 channels, this provides 2 characters of parallel storage for the assembly and transmission of read data to the controller interface. Data transfers take place simultaneously on all channels.

5.8.2.1 Data Decoding

The decoding method makes use of the self-clocking property of the PE format, i.e., there is a guaranteed data transition at the center of each cell. There may, or may not, be a phase transition depending on the data pattern.

Two steps are required.

(1) A data clock is generated by means of a three-quarter cell timer circuit. When triggered by the data transition the timer remains set until after the phase transition (if any) has occurred. It is then re-triggered by the following data transition, and this process is repeated each cell-time for the duration of the record. Initial synchronization is performed during the preamble pattern.

(2) The data content (0 or 1) of each cell is decoded by inspecting the polarity of the incoming data shortly after the data transition occurs.

Decoding is accomplished by flip-flops RD1 (A4/15) (sheet 4, zone E7), RD2 (A4/11) (sheet 4, zone E6), DSTR (A6/15) (sheet 4, zone E6), DGATE (A6/11) (sheet 4, zone C7), a 4-bit ripple counter (A1) (sheet 4, zone D6), and the associated gates. Decoding waveforms are shown in Figure 5-18. The logic is enabled by a true signal on RGATE when reading is required.

Incoming data on IRDP, IRD0-7 is synchronized with RCLK (24-1/2 pulses each data cell) at IRD1, and then delayed one clock-time by IRD2. Appropriate outputs from these flip-flops are gated together to form pulses which mark the positive- and negative-going transitions on the input data.

Assume that the first transition is the data transition for a zero bit, as shown in Figure 5-45. The corresponding pulse is gated through A5/6, A7/6 (sheet 4, zone F6), and causes a pulse to be generated on DSTR (data strobe) during the following clock time. This initiates a delay circuit consisting of DGATE and the 4-bit ripple counter. The DSTR pulse resets the counter, and causes DGATE to set.

The counter proceeds to count 16 RCLK pulses equivalent to a three-quarter cell delay. A count of 16 (rather than 18) is required since a delay of 2 clock-times has already been introduced by DSTR and DGATE.

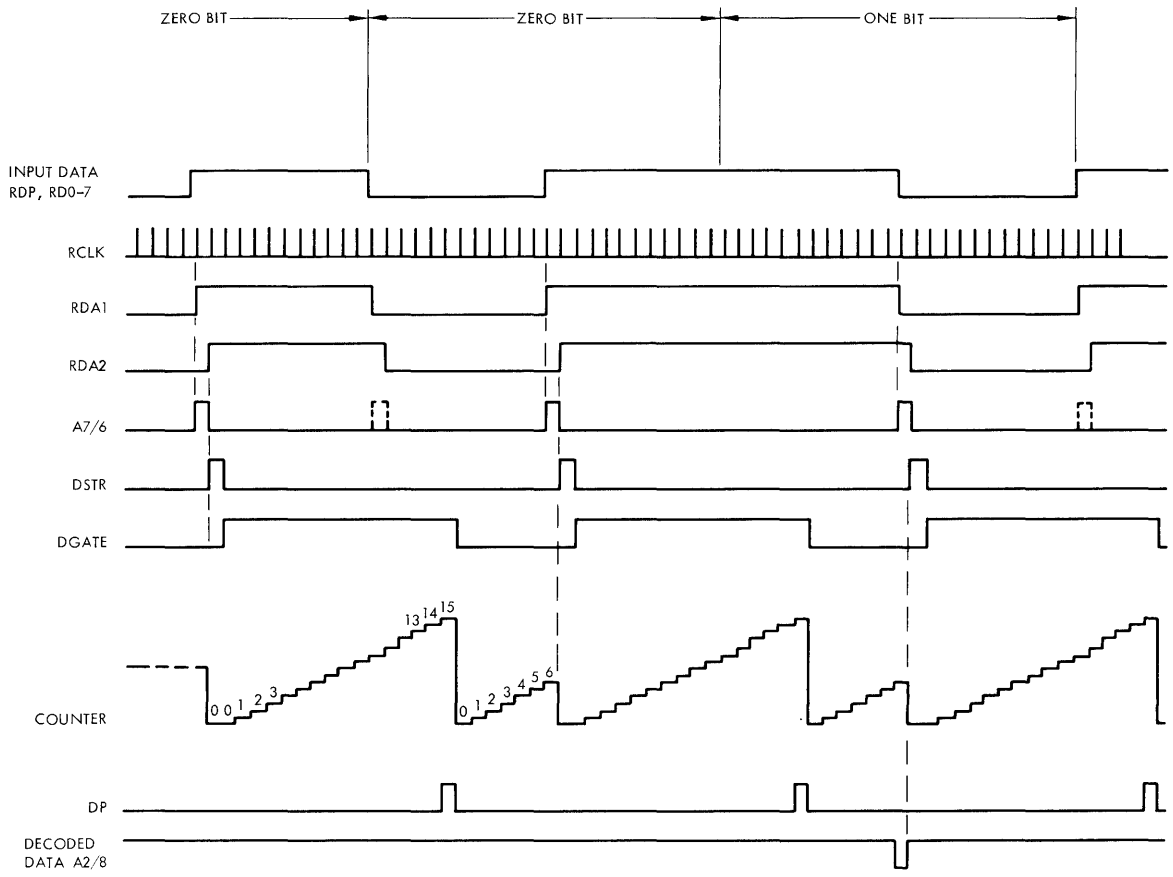


Figure 5-45. Data Decoding Waveforms

During the delay period NDGATE goes low and inhibits A5/6 and A5/8 (sheet 4, zone E6). This prevents another DSTR pulse being generated as a result of the phase transition.

On the sixteenth clock, a count of 15 (the capacity of the counter) is detected by the ripple counter (A1) and DP goes true. DGATE is now reset, A5/6 and A5/8 are re-enabled, and the delay cycle is complete.

The counter overcarries and continues counting until the data transition for the following cell arrives. Approximately 6 clock pulses are counted (depending on bit crowding and other effects) before the DSTR pulse occurs. A dropout is detected if a count of 15 is reached.

The above sequence is repeated each cell time for the duration of the record. A data clock is formed on DSTR, consisting of one pulse each cell time just after the data transition.

Initial synchronization is performed by the control signal NLO (sheet 4, zone E8). During the first part of the preamble this waveform disables A5/8, thus preventing the recognition of phase transitions for the preamble zero bits. The logic is therefore forced to synchronize on the data transition.

Data is detected by gating DSTR and NRD2 at A2/8 (sheet 4, zone E5). This gate goes low at DSTR time when a one-bit is detected. The output is inhibited by NDROP if a dropout has occurred.

5.8.2.2 Envelope and Dropout Detection

Two flip-flops, ENV and DROP (sheet 4, zone B6, B7) are associated with the decoding logic. The appropriate waveforms are shown in Figure 5-46.

ENV monitors the presence or absence of incoming data throughout each record. It is set by DSTR when data is detected, and reset by A8/4 (sheet 4, zone C7) when a dropout is detected, i.e., when a count of 15 is reached with DGATE reset. A loss of signal is sensed approximately one-half cell time after a missing data transition was due. In the complete absence of data a reset pulse is generated on A8/4 each time the counter re-cycles.

DROP is enabled by REN1 (sheet 4, zone A8) from the time of lock-on until mid-way through the postamble. If a dropout is detected during this time the flip-flop is set and the following data from this channel is discarded. Error correction is performed provided that no other channel has experienced a dropout.

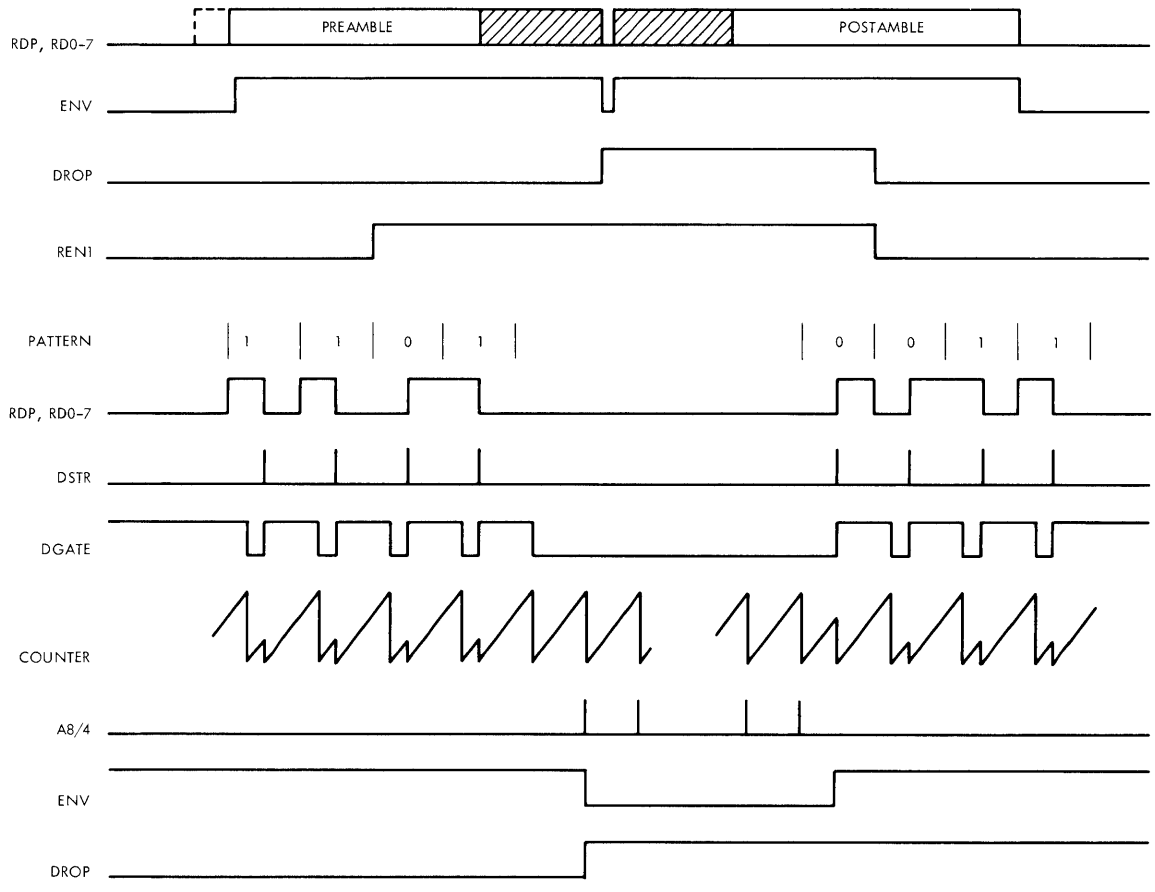


Figure 5-46. Envelope and Drop Waveforms

5.8.2.3 False Preamble/Postamble Check

Decoded data from A2/8 (sheet 4, zone F5) is routed through A9/4 (sheet 4, zone E5) to an open collector inverter A14/2 (sheet 4, zone D3). The output of this element is collector ORed over the 9 channels to form NONEDET. This goes low when a one bit is decoded on any one of the data channels.

Shortly after lock-on, the error logic inspects this waveform to verify that all channels are successfully decoding the preamble zero bits. A similar check is performed during the first part of the postamble period.

5.8.2.4 Synchronization Detection

At the end of the preamble test, REN2 (sheet 4, zone C8) goes true and the synchronous flip-flop (SYNC) is enabled. The first one-bit to be decoded after this time is interpreted as the one-bit at the end of preamble, and causes SYNC to set. (See Figure 5-47).

The bits following the one-bit detected at the end of the preamble are interpreted as data bits until the postamble is detected. A data clock, DSTR SYNC is formed by gating DSTR and SYNC.

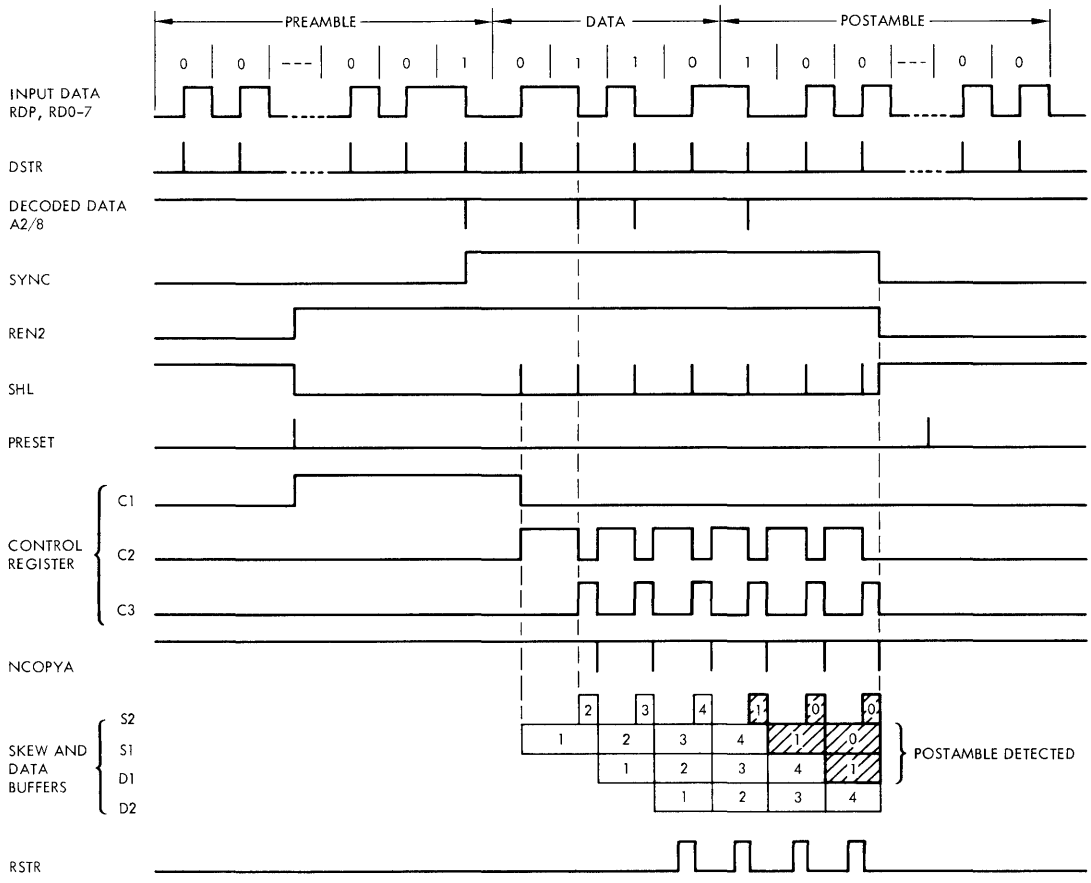


Figure 5-47. Data Buffering

5.8.2.5 Data Buffering

The skew register and parallel buffer consist of a 5-bit shift register A13 (sheet 4, zone E3), and the flip-flop A10/11 (sheet 4, zone E2). The skew register (S1-4) provides temporary storage for incoming data on each channel until all bits of a character have been assembled. A maximum of 2.9 characters of skew can be tolerated between the 9 channels. When all bits have arrived the character is shifted, in parallel form, to the data buffer (D1-2).

Decoded data is gated with NECLK (sheet 4, zone F5) then applied to the common input of the skew buffer preset gates. The timing of NECLK is approximately 50 nanoseconds earlier than NRCLK, and makes it possible to enter and shift data in the skew register in the same clock time.

The second input to these gates is controlled by the corresponding stage of a 4-bit shift-left/shift-right register, A12 (sheet 4, zone G3), which is initially loaded with a one-bit in the right-most (C1) stage. This bit is shifted left or right as required as data is entered or copied from the skew register, so that it *points* to the stage where the next data bit is to be entered.

Shifting is controlled by the following three waveforms.

(1) Mode Control, SHL (A9/12) (sheet 4, zone D4). This waveform controls the mode select input to the control register. When true, the shift-left mode is selected; when false, the shift-right mode is selected. SHL is set true for one clock time by DSTR SYNC each time a data bit is entered into the skew register. It is also held true by low signals on REN2 and NDROP when it is necessary to clear the control register.

(2) Shift-Left Clock, SLCLK (A11/10) (sheet 4, zone G5). This waveform consists of a pulse each clock time when SHL is true, except when NCOPY-A is low (when a shift-right operation is required). Each shift pulse causes the contents of the control register to shift left one place. As the shift takes place, the condition (0 or 1) of the control waveform PRESET (sheet 4, zone H3) is copied into the C1 stage.

(3) Shift-Right Clock, SRCLK (A11/4) (sheet 4, zone G5). When all bits of a character have been assembled in the skew register, the read control logic generates a low-true pulse on NCOPY-A. This generates a shift-right clock pulse at A11/4 which causes the control register, skew register, and data buffer to shift right one place. This shift takes place simultaneously on all channels. The bits entered into C4 and S4 via A12/1 and A13/9, respectively, are zeros.

5.8.2.6 Character Detection

The presence of a fully assembled character is detected as follows. The C1 stage of the control register is connected to an open collector inverter whose output is collector ORed for the 9 channels to form the waveform CHDET (character detect) (sheet 4, zone F2). This waveform goes high only when the control bit in each channel has moved away from the C1 position, i.e., after a data bit has been entered into S1 on all channels. The read control logic detects this condition and generates a pulse on NCOPY-A which causes a shift-right to occur as previously described. The assembled character is copied into D1, and the contents of D1 are transferred to D2. The following character is then assembled in S1.

5.8.2.7 Buffer Overflow

A buffer overflow error is detected by A16/10 (sheet 4, zone D4) if a data bit is decoded when the control bit is in the C4 position. This occurs if there are three or more characters of skew between this and the latest occurring channel. The DSTR SYNC pulse for this bit causes the control bit to shift out of the control register, resulting in the loss of subsequent data. The output of A14/6 (sheet 4, zone D4) is collector ORed with a similar signal from the other channels to form a common error signal, NBODET.

5.8.2.8 Postamble Detection

The postamble is detected by decoding the first two postamble characters (a character of all ones followed by a character of all zeros). This is performed by A11/13, A11/1, and A/14/12 (sheet 4, zone E2).

A11/13 tests for the required pattern (10) at the output of D1 and S1. If a dropout has occurred, the preamble test for this channel is forced true by the connection of DROP to A11. The result is collector ORed for all channels at A14/12 to form POSTDET.

The read control logic tests POSTDET as each shift-right transfer takes place (when all bits have been assembled in S1). If true, postamble is detected.

5.8.2.9 Buffer Operation

The following buffer sequence takes place when reading each record. Refer to Figure 5-47 for the appropriate waveforms.

The skew register and data buffer are initially dc reset by a low signal on SYNC and REN2. At the same time the control register is cleared by a continuous shift-left operation. Zero bits from the PRESET input cause the register to be cleared.

Midway through the preamble, PRESET goes true for one clock time just before REN2 is set. This causes the control bit to be loaded into the C1 stage of the control register. The input gate of S1 is now enabled.

At the end of the preamble, SYNC goes true and the skew buffer is enabled. One cell time later the first data bit is decoded and is entered into S1. At the same time DSTR SYNC causes the control bit to shift left one place to C2. If this bit is still present when the second bit arrives, the second bit is copied into S2 and the control bit moves to C3, etc.

When all bits of the first character have arrived, a NCOPY-A pulse is issued. The assembled character is shifted from S1 to D1, and the skew and control registers are shifted right one place to make room for new data.

This process is repeated for each data character until postamble is detected. This occurs just before the postamble all-ones character is entered into the output (D2) register. REN2 now goes low causing the entire buffer logic to be reset to the initial state.

The decoding logic continues processing postamble information until the end of record is reached.

5.8.2.10 Data Output

Data is taken from both the Q and $\overline{Q}$ outputs of the D2 register.

The Q outputs, DAP, DA0-7, are fed to a parity generator circuit, E17 (sheet 3, zone C5). If no dropouts have occurred, this circuit checks that the parity of each output character is odd. If a single track dropout has occurred, the circuit re-generates corrected data for the affected channel using the data from the other 8 channels.

The $\overline{Q}$ outputs are ORed with corrected data at A15/3 (sheet 4, zone E2) to form DATA P, DATA 0-7; and then transmitted to the Controller interface read lines, IRP, IR0-7, by driver elements.

A strobe waveform, RSTR, is generated by the read control logic. This consists of a pulse for each data character, and is used to strobe IRP, IR0-7 into the controller logic.

5.8.2.11 Error Correction

Error correction takes place when there has been a single track dropout, and no other error conditions. The following actions take place when the DROP flip-flop is set.

(1) Decoding gate A2/8 (sheet 4, zone F5) is disabled. This prevents preamble/ postamble check errors from being caused by this channel.

(2) SYNC is cleared. This causes S1-S4 and D1 to be cleared. D2 is not affected.

(3) The control register is cleared by a continuous shift left. This channel no longer takes part in character detection (CHDET).

(4) The postamble test is forced true. This channel no longer takes part in postamble detection (POSTDET).

(5) Error correction gate, A15/6 (sheet 4, zone E2) is enabled.

Error correction does not begin until the next character is transferred to the output buffer. In the meantime, the transmission of the current character (still in D2) to the controller is completed.

When the next character is transferred to D2, a zero bit is copied for the channel in error. At the same time the presence of the dropout is detected by the read control logic. An error correction bit, PARC, is now formed by the parity logic on the basis of the information in the other channels. This is routed through A15/6 and A15/3 on the channel in error to perform the required correction. Correction is performed on each of the following characters until postamble is detected.

The interface line, ICER, indicates to the controller when error correction is taking place.

5.8.3 SINGLE/MULTIPLE TRACK DROPOUT DETECTION

Associated with the data channel logic is a circuit which detects the presence of single or multiple track dropouts.

This takes the output of the nine DROP flip-flops (sheet 3, zone D3) and forms the following signals.

(1) DROPDET1. This goes high if any one or more of the channels have dropped.

(2) NDROPDET2. This goes low if any two or more of the channels have dropped.

The logic consists of a number of identical circuits, one for each channel. It is broken into two parts, one for Channels P, 0-3, and the other for Channels 4-7. The two halves are then combined by F16/1, F14/4, and F15/8 (sheet 3, zone D3).

Operation of the Channel 1 stage is as follows. The input from the stage above is an OR of DROP signals from the previous channels in the chain (P and 0). This is ORed with DROP/1 inverted, and then passed on to the following stage. The two signals are also gated at C16/1 (sheet 3, zone F3) and the result is collector ORed onto the DROPDET2 line by C14/4 (sheet 3, zone F3). NDROPDET2 therefore goes low if Channel P has dropped, and either one of Channel P or 0 has dropped.

By repeating this process stage-by-stage the required signals are formed.

5.8.4 CONTROL LOGIC

5.8.4.1 Tracking Control Logic

The tracking control logic generates the control waveforms which servo the tracking oscillator frequency to 24-1/2 times the instantaneous data rate. The decoding waveform DGATE (sheet 5, zone F8) from Channel 2 is normally used as the tracking input. This waveform goes true for 16 clock times each data cell, and should therefore be false for an average of 8-1/2 clock times before the next data transition occurs. The control logic counts the number of RCLK pulses during this time and generates the appropriate error signal. If Channel 2 drops out, control is automatically switched to Channel 0. Figure 5-48 illustrates the tracking control waveforms.

AND/OR gate E21/8 (sheet 5, zone E7) selects either DGATE/2 or DGATE/0 as the tracking input depending on whether or not there is input data on Channel 2. The output, TRACKSIG, is then delayed one clock time by B18/15 (sheet 5, zone E7). When this flip-flop is set, a 3-bit ripple counter (A17/15, A17/11, B17/15) (sheet 5, zone F6, F7) is enabled, and counts off the number of RCLK pulses which occur during this time. If a count of eight or more is reached the counter overcarries and sets the next flip-flop in line. If the count is less than eight, the flip-flop remains reset. Gates A15/8 and A16/4 (sheet 5, zone E5, E6) generate a clock pulse which copies the contents of the overflow-flip-flop to B18/11 (sheet 5, zone F5) during the last clock time before B18/15 goes false.

B18/11 is therefore set or reset each data cell depending on whether the oscillator frequency is too high or too low. The two outputs are inverted to form the oscillator control waveforms NER1 and NER2. When NER1 is low the frequency is decreased; when NER2 is low the frequency is increased.

In the absence of input data, DATA2 (sheet 5, zone F5) clamps B18/11 off at the dc set and reset inputs. This causes NER1 and NER2 to go low at the same time, and the tracking oscillator reverts to its center frequency.

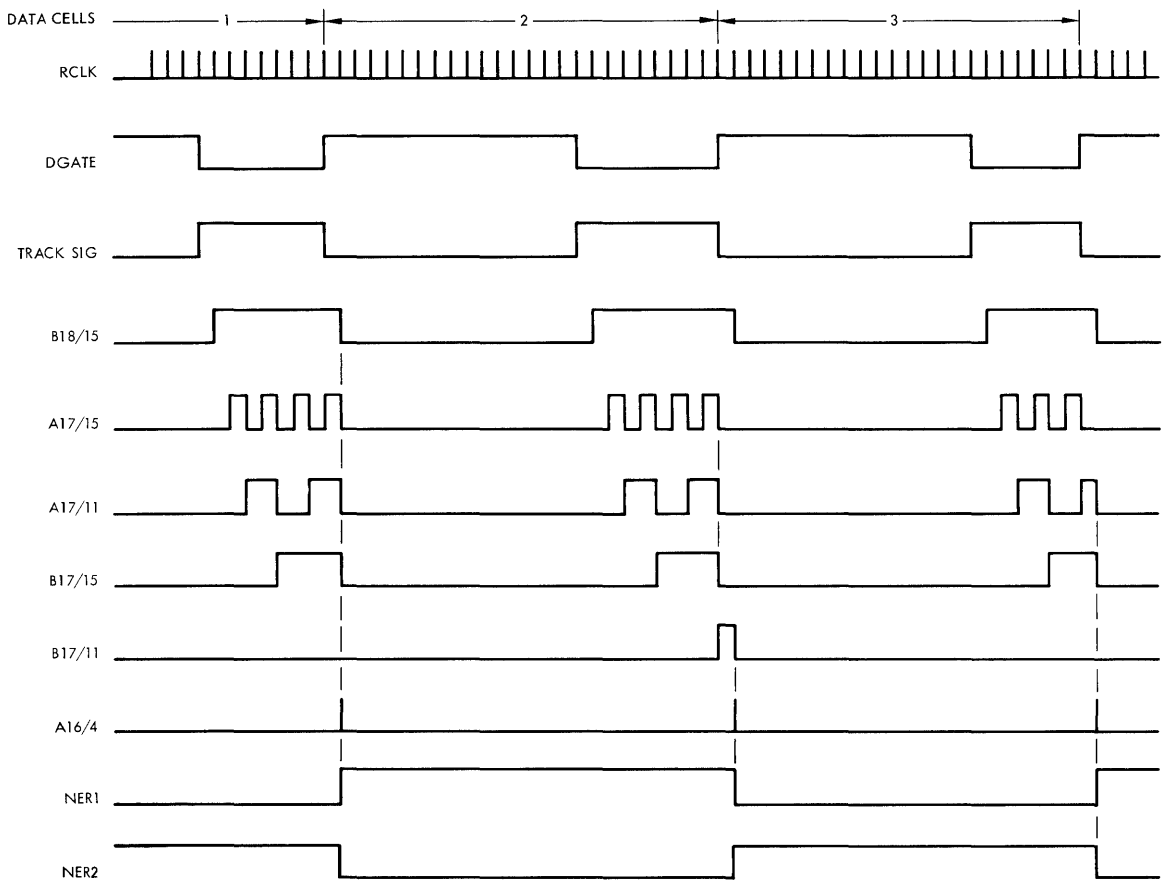


Figure 5-48. Tracking Control Waveforms

5.8.4.2 Clock Distribution

The output from the tracking oscillator is fed to a delay chain of six inverter elements, and then inverted at H17/8 (sheet 5, zone H5) to form NRCLK. Six power gates, RCLK1-6, distribute the waveform to various parts of the read logic. The relevant area is indicated beneath each waveform name.

The first inverter in the chain, NECLK, is timed approximately 50 ms earlier than NRCLK. This is used to gate decoded data to the skew buffer in the data channel logic (see Figure 5-49).

5.8.4.3 Read Enable

IRGATE (sheet 5, zone E8) is set true by the PE Write PCBA when the reading of a data record is required. This signal is fed to three power gates, RGATE1-3, which drive the 9 channels of data logic. When reading is required, RGATE1-3 go high, and allow the decoding logic in each channel to recognize input data from tape.

For control purposes, the presence of data on either Channel 2 or Channel 0 is used to indicate that data (data record or file mark) are being read from tape. The same two

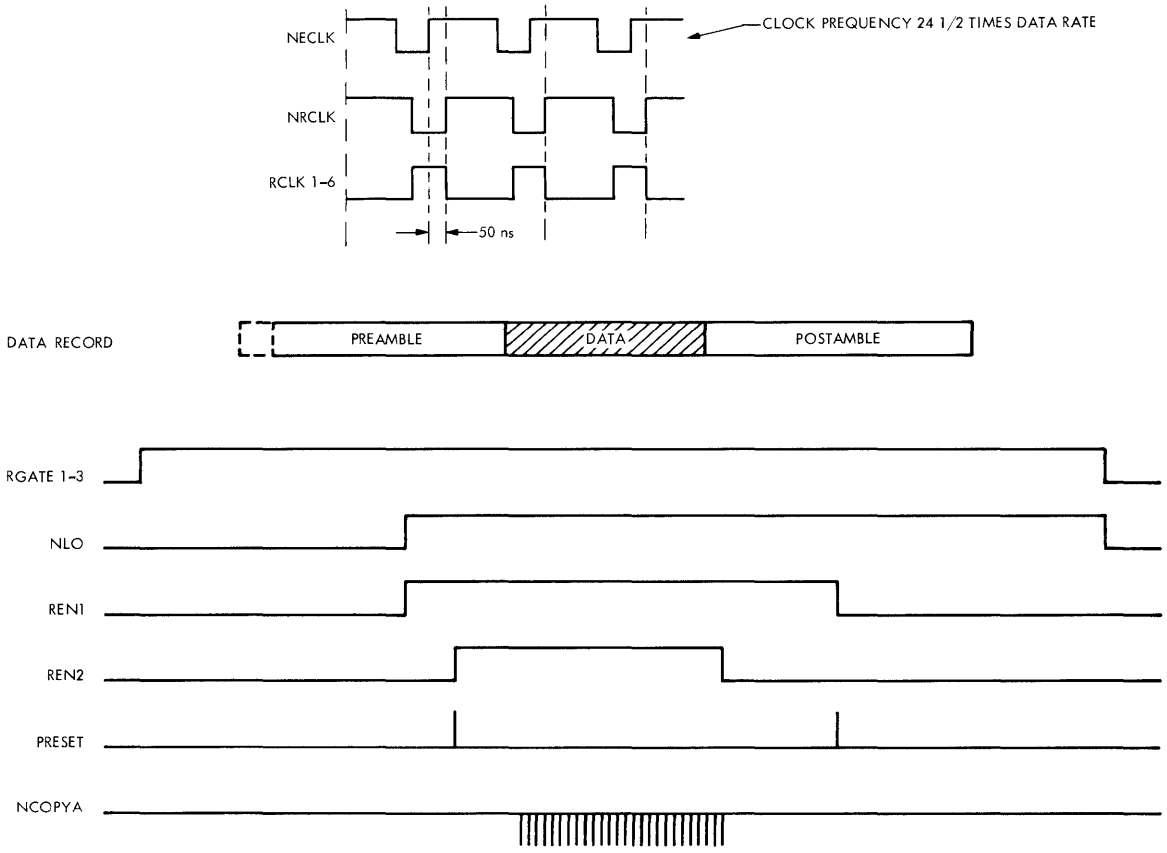


Figure 5-49. Control Signals to Data Channels

channels are used for tracking control. Envelope waveforms NENV/2 and NENV/0 are ORed at F17/8 (sheet 5, zone D7) for this purpose. The waveforms NDATA, DATA1, and DATA2 are then formed.

When a data pattern begins, DATA2 goes high, and the oscillator begins tracking from its center frequency to the instantaneous data rate. At the same time, NDATA and DATA1 enable the read control logic and allows the initial timing sequence to begin.

5.8.4.4 Sequence Control

Basic timing is provided by a sequence register consisting of 7 flip-flops, RCN1-7 (sheet 6, zone G3-7), and a counter register RCTR0-11 (sheet 5, zone D2-5). RCN1-7 set up in turn and mark off the various stages in reading a record. Appropriate control and timing waveforms are derived from the RCN flip-flop counter logic.

The counter logic times out the various delays required during the preamble, postamble, and gap periods, and is also used for data transfer.

The count logic consists of a 12-bit ripple counter (RCTR0-11), a set of decoding gates (F21/8, F20/8, and F20/6) (sheet 5, zone F2), the flip-flop RP, and the counter reset gates.

The counter input (G20/14) (sheet 5, zone D5) is tied to RCLK so that the counter is always counting except when it is reset by the NOR gate E22/6.

The length of the delay is determined by one of the three decode gates which are ORed into F21/6 (sheet 5, zone F2). F21/8 is a 22-character delay time and is always enabled. F20/8 is enabled when RCN2 is true and RCN4 is false and has a delay of four character times. F20/6 has a delay of 0.7 character times and is enabled by CCN2 during a read data transfer. When the counter reaches the count of one of the enabled decode gates, RP is set true for one clock time. RP is one of the reset terms of the counter so that the counter is reset to all zeros at every RP.

The read control sequence (see Figure 5-50) is initiated when the data signal goes true. This removes the reset level from the counter by disabling E21/6 (sheet 5, zone C3). The counter issues a RP after 22 character times which sets RCN1 and RCN2 true. RCN1 causes NLO to go true and RCN2 causes REN1 to go true. The decode gate F20/8 is now enabled and a RP will be issued after four character times which will set RCN3 true.

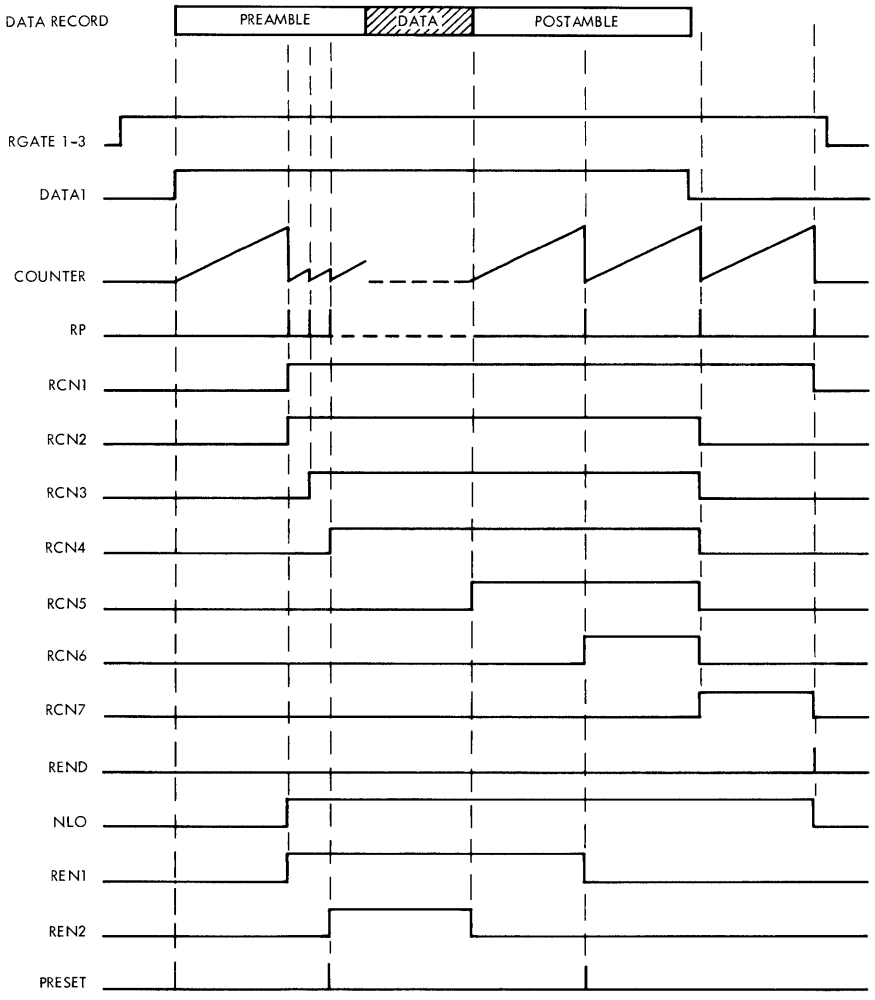


Figure 5-50. Sequence Control

During the next four character times, before RCN4 is set true, a test for one bits in the preamble will be made by the AND/NOR gate H22/8 and the NAND gate D22/1 (sheet 6, zone F7).

When RCN4 goes true, REN2 will be enabled and the decode gate F20/8 will be disabled. The logic is now looking for the all-ones character at the end of the preamble. If it does not occur within 22 character times from the time RCN4 was set true (52 character times from start of read) the NAND gate E20/6 (sheet 6, zone E7) (NERR3) goes true to indicate a format error.

When the postamble is detected RCN5 will be set true which disables REN2 and enables AND/NOR H22/8 for a ones test of the postamble. After 22 character times RCN6 is set true by RP and REN2 is disabled. At the end of another 22 character times when RCN7 is set true a test is performed by the NAND gate E20/8 (NERR4) to check for the end of data and the start of the gap. RCN7 will be set true for 22 character times during which no data can occur, and RCN7 also resets RCN2-7. At the end of 22 character times the read end pulse (REND) is set true for one clock time; RCN1 is also reset at this time. REND signals the end of the read sequence.

5.8.4.5 Data Control

The data control consists of three flip-flops (COPY, CCN1, and CCN2) (sheet 5, zone B5, 6, 7) which are enabled when RCN4 goes true. When the first character has been deskewed (see Figure 5-51) Character Detect (CHDET) goes true which sets the COPY flip-flop true for one clock time and shifts the first character into the data buffer. CCN1 is set true on the next clock pulse. The next CHDET will set COPY true for one clock which will shift the first character of the record to the output flip-flop of the data register and set CCN2 true. CCN2 enables the decode gate F20/6 and the NOR gate H19/1 (sheet 5, zone B2) so that a read strobe (RSTR) will be issued in the center of the data cell. RP will go true 17 clock pulses from the time CCN2 was set true and reset CCN2. When CCN2 is true the NOR gate H19/3 is disabled so that the transfer of the next character will not start until the first character has been transmitted out of the interface.

This sequence of data transfer continues until the all ones bit of the postamble is shifted into the first stage of the data buffer. The postamble detect signal (POSTDET) will go true and after the last character of the record has been strobed the first character of the postamble will cause COPYCLK to set RCN5 true. RCN5 true will reset all the data control flip-flops.

5.8.5 FILE MARK

A file mark is identified by 40 zeros in Channels P, 0, and 5, with Channels 1, 3, and 4 dc erased. Channels 2, 6, and 7 can be dc erased or have 40 zeros. NAND gates D17/6 and D17/8 (sheet 6, zone D7) look for data in Channels P, 0, and 5, or 2, 6, and 7. NAND gate F17/6 looks for the absence of data in Channels 1, 3, and 4. At the end of 22 character times from the start of data (see Figure 5-52), RP will set RCN1, RCN2, and FM true. FM going true enables H22/6 (sheet 6, zone E4) so that RCN7 is set true on the next clock pulse which in turn resets RCN2. The read sequence logic then waits for the end of data at which time the read counter counts for 22 character times and sets REN1 true for one clock time. The REND pulse resets RCN1, RCN7, and the FM flip-flop.

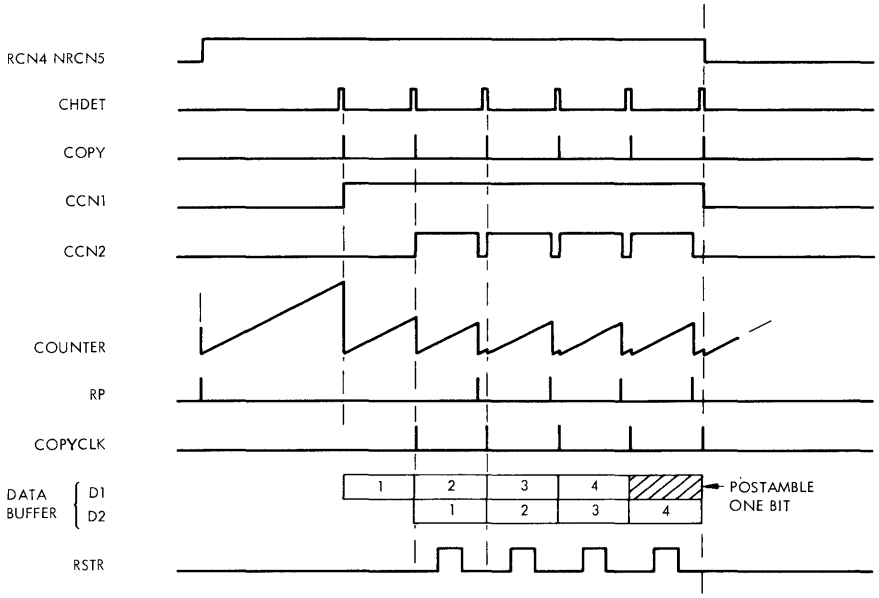


Figure 5-51. Data Control

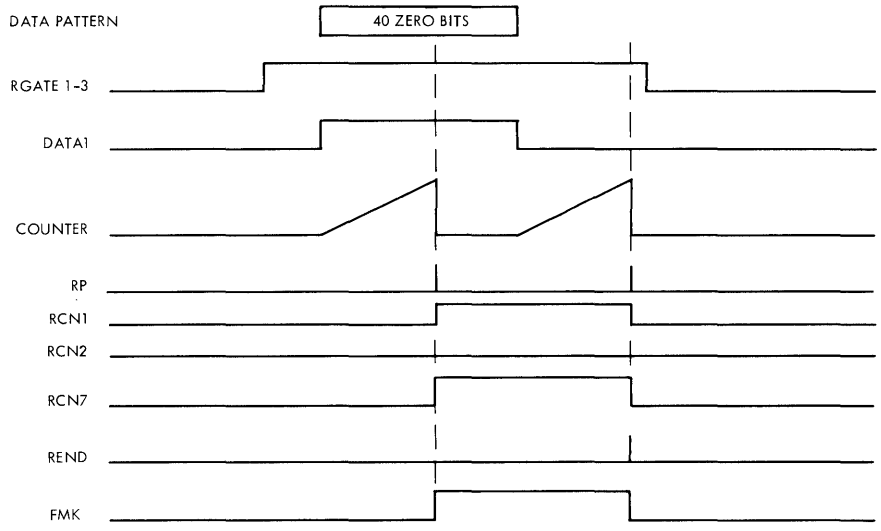


Figure 5-52. File Mark Waveforms

5.8.6 IDENTIFICATION BURST

When the controlled transport is at the beginning of tape (LDP) a test is made for the identification burst. To enable the test IDG (sheet 5, zone D8) goes true which causes RGATE to go true so that the front half of all the channels are enabled, NLO is held high because the identification burst is a 1 0 1 0 1 pattern and DATA is held false so that the control logic is disabled. Half way through the IDG waveform ITESTID is set true and the NOR gate D16/13 (sheet 6, zone A7) looks for data on Channel P and no data on Channels 1, 3, and 4. If these conditions are met the interface signal IDENT is set true. After the identification test is completed IDG and ITESTID are reset and IRGATE is set true so that the control logic will read the first record.

5.8.7 ERROR DETECTION

Hard errors (i.e., uncorrectable errors) are of two types; parity errors and format errors. Parity errors are checked with the parity generator IC, E17/6 (sheet 3, zone C5), which generates odd parity of Channels DA/0 through DA/7 and compares it with the data from the parity Channel (DA/P). If the compare fails, the PE line goes true and the NAND gate D21/8 (sheet 6, zone B4) will be enabled during the read strobe for the character in error. Therefore, the IHER interface line will be pulsed at the same time the IRSTR pulse strobes the character into the controller if the character had a parity error. The strobed parity error line is available on pin 3 of the test connector J5 (NER1) for maintenance and test purposes.

Format errors are indicated by the flip-flop F22/11 (FE) (sheet 6, zone E6) going true which sets the IHER interface line true and forces the logic to look for the end of the record by setting RCN7 true. With RCN7 true a REND pulse will be issued when the DATA signal is false for 22 continuous character times.

The FE flip-flop is set true by one of the four inputs to the NAND gate E22/8 (sheet 6, zone E6). NDROPDET2 goes low when two or more channels have lost synchronization. This can occur any time after the lock-on signal (NLO) has gone false. The NERR2 input is the combination of a buffer overflow error and the test for ones in the preamble and postamble. The buffer overflow error (NBODET) indicates that one of the channels has more bits of data than it can store. A test is made for ones in the preamble during the four character times DCN3 is true and DCN4 is false and the same is performed during the first 22 character times of the postamble when RCN5 is true and RCN6 is false. If, during these test periods, a one bit appears in any of the channels the NONEDET signal will go low and enable D22/1 (sheet 6, zone F7).

NERR3 going low indicates that the first data character of the record was not transmitted within 22 character times from the time RCN4 was set true. This error occurs when one or more of the channels fails to detect the one bit at the end of the preamble.

NERR4 is a test to verify that gap at the end of the postamble is within 44 character times from the start of the postamble. This test checks that a false postamble was not detected in the center of a record.

5.8.8 ERROR CORRECTION

If one of the channels looses synchronization during the record, DROPDET 1 will set the flip-flop (D23/15) (sheet 6, zone B6) CORRECT true. The CORRECT flip-flop true enables D21/6 (sheet 6 of 6, zone B4) which causes the reconstructed data from the parity generator to feed to all the channels via the PARC line. At the same time the parity error NAND gate D21/8 (sheet 6, zone B4) is disabled by the correct flip-flop and IHER interface line is set true.

5.9 BUFFER PCBA

The Buffer PCBA contains the logic and high-speed dynamic MOS random access memory necessary to buffer data asynchronously between a controller and PERTEC's family of tape formatters. The high-speed memory cycle time (less than 700 nanoseconds) services both interfaces simultaneously by time multiplexing. The functional block diagram shown in Figure 4-6 and Schematic No. 101810 should be referenced in conjunction with the description of this PCBA.

The buffer performs the following major logic functions.

(1) Accepts data asynchronously from the controller at rates from 0 to 750 kHz.

(2) Supplies data asynchronously to the controller at rates from 0 to 750 kHz.

(3) Buffers up to 4096 eight-bit characters for transfer to the tape formatter.

(4) Accepts data from PERTEC formatters at the specified synchronous rate of the transport.

(5) Supplies data to PERTEC formatters at the specified synchronous rate of the controlled transport.

(6) Provides for automatic (and automatic continuous) transfer of data to or from the controller, from and to the selected tape transport.

(7) Provides for the generation of tape file marks (when used with the appropriate formatter and transport), and for the searching of tape file marks.

(8) Provides for back- and forward-spacing over a record on tape.

(9) Provides for erasure and editing of pre-recorded tapes via the formatter PCBA.

Illustrated in Figure 5-53 is the physical layout of test points, jumper connections and external connectors on the Buffer PCBA. Interconnections to the formatter and controller interfaces are made through two 100-pin edge connectors, J1 and J2, respectively. It is important to note that connection at J1 and J2 is reversed at the external interface provided for the customer, e.g., a signal on J2-A3 appears on J104-B3 at the controller interface. Table III, located on sheet 1 of Schematic No. 101810, provides sheet location of these interface signals.

Ground and +5v power connections are made through J1 and J2 in parallel. Pins B48, B49, and B50 are used for +5v; pins A47, A48, A49, and A50 are used for ground. Power connections for the —5v is made at B47; +20v connections are made at A45 and B45.

Four basic versions of the Buffer PCBA (101811) provide the four basic memory lengths; these are listed in Table 5-2.

The Buffer PCBA utilizes a crystal oscillator to provide the basic 12 MHz clock signal. This signal is used for generating the clocks for the memory and control circuits throughout the buffer.

5.9.1 CIRCUIT DESCRIPTION

The operating frequency of the oscillator is determined by the resonant frequency of the crystal Y1 (refer to Schematic No. 101810, sheet 2, zone G7). The basic circuit consists of amplifier Q1, Q2, emitter follower Q3, and the crystal Y1, used in a series resonant mode. Resistors R1 through R5 provide the dc bias and negative feedback for transistor Q1 (Q1 is connected in a common emitter configuration). These values of R1 through R5 are selected for a given crystal frequency to account for different values of crystal series resistance.

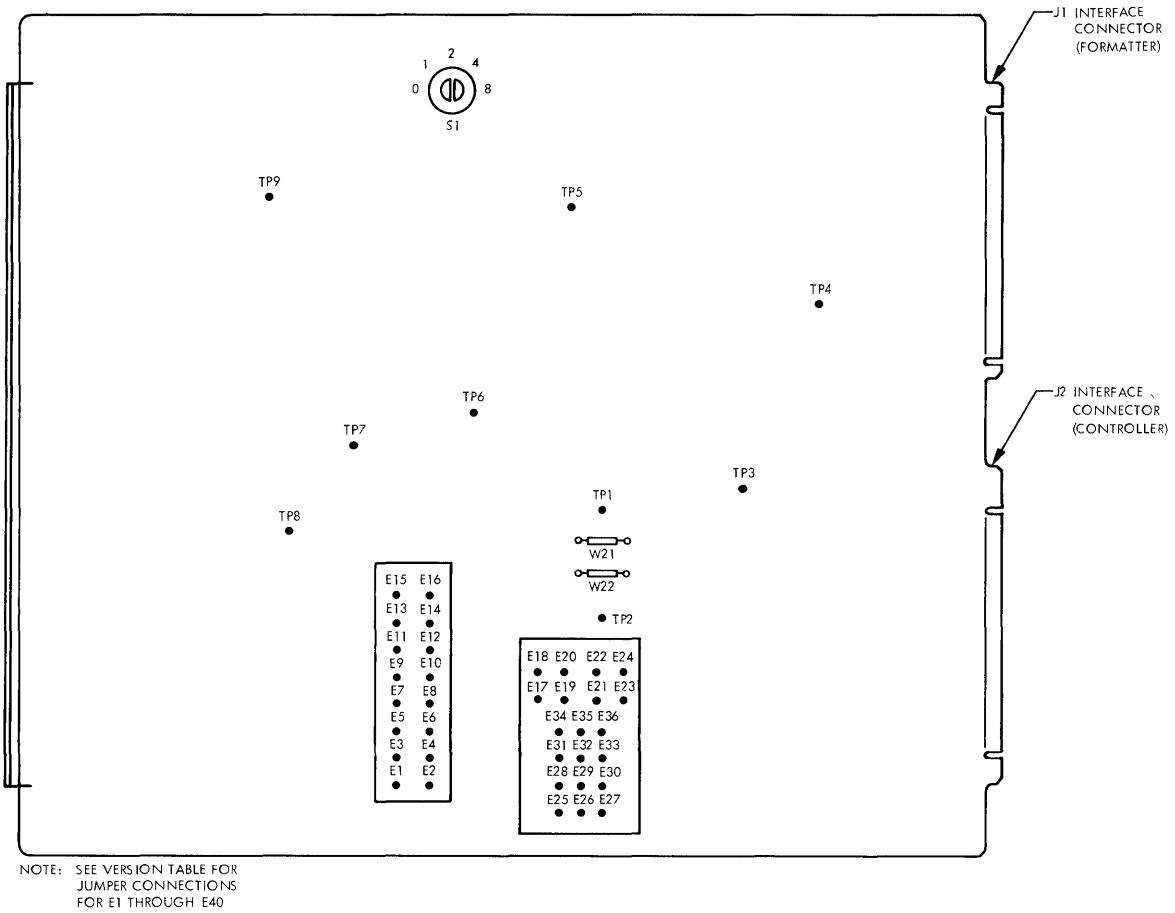


Figure 5-53. Buffer PCBA, Test Point and Connector Placement

Table 5-2
Buffer Version Identification

Version	Buffer Length (Bits)	
	Single Buffer	Split Buffer
101811-01	1024	512
101811-02	2048	1024
101811-03	4096	2048
101811-04	512	256

A capacitor provides dc isolation for the crystal and stabilizes the crystal resonant frequency. The crystal is connected between emitters of Q1 and Q2, the low impedance nodes. Transistor Q1 provides more than unity loop gain at the crystal resonant frequency in the loop formed by Q1 collector, Q2 base, Q2 emitter, through the crystal Y1, Q1 emitter and back to Q1 collector. There is a total phase shift of 360° around the loop with the crystal providing 180° of the phase shift. Emitter follower Q3 isolates the basic oscillator circuit from the load.

Memory access is controlled by a priority circuit consisting of two 3-bit registers and associated combinational logic (refer to sheet 11). The first register is the memory queue register consisting of flip-flops U64, U84, and U62 (zone G, E, D6). This register latches requests from the 3 sources (controller interface, tape interface, and refresh circuit). Since these requests can occur asynchronously with respect to the memory cycle, the requesting device places its request into the queue register and awaits service from the memory. When the memory has completed a service cycle and is ready to accept new requests, the SAMPH output of U82 pin 12 (zone B2) goes low allowing the contents of the queue register to be clocked into the second set of flip-flops which comprise the memory access register.

When a set of requests is absorbed into the memory access register, the requests are decoded to obtain their relative priority. The tape interface, being synchronous, is given highest priority (Tape Priority I); the high-speed asynchronous controller interface is next in priority (Buffer Priority II); and, lowest priority is assigned to the refresh cycle (Refresh Priority III) which is needed to ensure data retention in the dynamic memory array. The memory access lines NMAC1, NMAC2, and NMAC3 control the memory operation for controller, refresh, and tape, respectively, and go low in order of priority to direct the memory cycle to the requesting device.

When a memory cycle is completed, the corresponding bit in the memory queue register is reset. Thus, the requesting device is informed that its request has been serviced.

Three clocks are provided to the Memory Matrix (sheet 3). These clocks are generated by the Memory Cycle Logic (sheet 2). The clocks are generated by decoding the proper state of U23 (a type 74161 counter) (sheet 2, zone G4). High-speed logic gates are employed to minimize propagation delays. This logic also generates the strobes needed to route data out of the memory. Data flow into the Read Memory latches are controlled by the memory cycle logic while the individual controllers control the Write Memory latches.

Additionally, the Memory Control Logic is clocked by the 12 MHz clock oscillator. When no memory requests are pending, SAMPH is low, holding U23 reset by means of pin 9, thus disabling the memory logic.

The 1103 Memory Matrix for a 4096-bit configuration is shown on sheet 3 of the schematic. Rows 2 and 3 are omitted for 2K versions, rows 1, 2, and 3 are omitted for 0.5K and 1K versions. The voltage levels required to drive the type 1103 memory chips are provided by type 3207 MOS driver chips for clock, data, and address inputs.

The Buffer PCBA utilizes two memory address counters: Memory A Address Counter and Memory B Address Counter. These counters and their associated circuitry are shown on sheets 4 and 5 for Memory A and Memory B, respectively. Data are controlled and referenced in memory through the action of these counters.

The Memory A Address Counter consists of a 13-bit counter U19, U60, U117, and one-half of U79 (zone G4 - G7), a 13-bit latch U18, U59, U116, and one-half of U79 (zone E4 - E7), and a 13-bit comparator U17, U58, U115, and one-quarter of U78 (zone C4 - C7). The counter is always preset to zero and counts up as each character is transferred to or from memory. Two overflow terms, SBOVFH (Single Buffer Overflow) and ABOVFH (A Buffer Overflow) are jumper selected, dependent on the buffer size, to signal that the last memory location of the appropriate buffer has just been referenced. Jumper connections for the overflow signals from the Memory A Address Counter are given in Table 5-3.

The Memory B Address Counter is similar to the Memory A Address Counter. It consists of a 13-bit counter U39, U96, U137, and one-half of U80 (zone F4 - F7), a 13-bit latch U38, U95, U136, and one-half of U80 (zone D4 - D7), and a 13-bit comparator U37, U94, U135, and one-quarter of U78 (zone B4 - B7). This counter is preset as a function of buffer length which is jumpered at the counter inputs. This jumper arrangement is shown on sheet 5, zone G5. Since the Memory B Address Counter is used only in split-buffer configurations, it has only one overflow term BBOVFH (zone F1). Jumper connections for the BBOVFH signal are shown in Table 5-4.

Overflow signals from both the Memory A and B Address Counters are presented to the controller interface via J2 (sheet 13, zone D2).

The buffer Refresh Oscillator (shown on sheet 6) is a relaxation oscillator. The oscillator operates at 18 kHz and provides a pulse LEREFH at the 18-kHz rate; this pulse initiates the refresh cycle to the memory logic, thus ensuring data retention when the memory is idle.

Table 5-3

Memory A Address Counter Jumper Connections

Version	Buffer Size	W1	W2	W3	W4	W5	W6	W7	W8
101811-01	1K			X	X				
101811-02	2K					X	X		
101811-03	4K							X	X
101811-04	0.5K	X	X						

Table 5-4

Memory B Address Counter Jumper Connections

Version	Buffer Size	W9	W10	W11	W12
101811-01	1K		X		
101811-02	2K			X	
101811-03	4K				X
101811-04	0.5K	X			

Consecutive refresh cycles address different rows in each memory chip. Flip-flop U108 (sheet 6, zone E4) and counter U16 (zone F3) serve as a row address counter for the memory matrix. Every row of the memory matrix is refreshed each 2 milliseconds by REFAD0 - REFAD4 signals via the Buffer PCBA memory address MUX (sheet 9).

A 4-bit synchronous counter U106 (sheet 6, zone D4) provides the buffer-generated IGO pulses to the associated formatter via J1 (zone D1). The counter is triggered by the individual tape micro controllers (shown on sheets 18 and 19). The IGOI pulse may also come directly from the controller in case of a Write File Mark (WFM) or Space operation. This circuitry is shown on sheet 6.

Also contained on sheet 6 is the error counter for the tape error recovery circuits. Each time the buffer rewrites or rereads an erroneous record, U102 (zone C6) is incremented. A rotary switch S1 (zone B5) allows the user to select the number of retries, to a maximum of 8. (The options are 0, 1, 2, 4, 8 retries.) When the retry number is exceeded and the record is still in error, IHERI is asserted to the controller via J2 (zone B4).

The Read Tape/Write Buffer interface input to the buffer and the Memory Data Driver logic is shown on sheet 7. Read tape and write buffer data are captured by latches U213, U212, U189, and U190 under control of the Read Tape Micro Controller (sheet 18) and the Write Buffer Micro Controller (sheet 17). The relevant data are then passed through the type 74158 data selector/multiplexer U192 (zone G4), U191 (zone C4), and one-half of U169 (zone A3) to the Memory Data Driver logic. Level translation between the TTL logic and the 20v MOS levels of the 1103 Memory is performed by the 3207 drivers.

Due to the relatively high power dissipated by the type 3207 drivers, they are gated with ADENH2, the inverse of SAMPL at U85 (zone E2). ADENH2 causes the Memory Data Drivers to revert to the quiescent (high) state during periods when the memory is idle. The low-true output of the Memory Data Drivers are damped by 10-ohm resistors to reduce overshoot and ringing on the memory input lines.

Shown on sheet 8 are the Memory Clock Drivers used for row select in the memory matrix. U86 (zone C6) decodes the last two address bits from the Buffer PCBA Memory Address MUX, U93 (sheet 9), to obtain the row of memory to be addressed. U66 allows all chips to be addressed during a refresh cycle when NMAC2 (sheet 8, zone B8) is low. The three memory clocks CENH, PREDH, WRTH are applied to the selected memory row by the type 3207 Driver/Translator logic.

The Buffer PCBA Memory Address MUX (sheet 9) functions to select either the Memory Address Counter A or B or the Refresh Address Counter, depending on the type of memory cycle in operation. ENAL (zone G8) goes low for a Buffer A operation, while MAC2 (zone G8) going high selects the Refresh Counter. The B Counter is normally selected.

Since the Refresh Counter only has 5 bits, the most significant 7 bits of the MUX require a 2-to-1 MUX while the remainder is a 3-to-1 MUX.

Also shown on sheet 9 of the schematic are the Memory Address Driver chips; these are type 3207 drivers whose operation is identical to the Memory Data Drivers previously described.

The Memory Data Routing Logic is shown on sheet 10. This logic decodes the state of the command register and the BCC lines (zone D, E8) to determine the value of the operation. The enable terms are also generated to direct data flow in the desired path.

U193 (zone D, E7) is the BCC control MUX for the Automatic Continuous modes of operation. External BCC lines are disconnected for these operations.

The Read Buffer/Write Tape interface output of the buffer and the Memory Sense Amplifiers are shown on sheet 12. Data from memory are captured by latches U194, U195, U196, and U197 under the control of the Memory Cycle Logic. The output of the latches drive the J1/J2 interface through type 7416 Inverter Buffer/Drivers.

The Counter Control Logic (sheet 13) is used to preset the Memory A and Memory B Address Counters. The output signals PSETAL and PSETBL from U208 pins 10 and 4, respectively, preset the 74193 counters and 7474 flip-flops shown on sheets 4 and 5. Presetting occurs during either a general reset of the buffer by CLRH, or just after the address latches are loaded following transmittion of the last character into or out of the buffer. The A and B latches are loaded by LDCAL and LDCBL, respectively. U207 and U206 (zone 7) perform the decode which determines which micro controller is to signal the load and preset operation. Internal overflow signals are provided to the micro controllers via U174 (zone B, G3) to prevent buffer overflow.

Sheet 14 is primarily concerned with feed-through signals. U109 is the Tape Error flip-flop (zone F7) which is set by the IHER line from the formatter. This signal is used in conjunction with the Retry circuitry shown on sheet 6. U165 (zone E7) is an input/output synchronizer for asynchronous signals to the micro controllers. U81 (zone F3), in conjunction with U181 and U209, is used as a reversing circuit to reverse tape direction during backspacing for rewrite.

The Buffer Command register is shown on sheet 15. This register latches the type of command being performed to activate the proper micro controller. The register can be set by the controller through the IGOI pulse, or internally by the micro controllers themselves. The micro controllers can change buffer commands to perform automatic and automatic continuous functions without additional controller commands.

The Read Buffer Micro Controller (RBMC) as well as the three other micro controllers (Write Buffer Micro Controller, Read Tape Micro Controller, and Write Tape Micro Controller) are shown on sheets 16, 17, 18, and 19. These micro controllers each consist of a program counter (type 74161), a test MUX (type 74151), and a sequence decoder (type 74155). Each micro controller is hardwired to perform an algorithm containing up to eight instruction steps. A step can be any one of the following seven types. It is important to note that the seven types of steps listed are hardwired into a predetermined order of execution.

(1) NO-OP. No operation; used as a time fill.

(2) TEST AND WAIT. Used to wait for an event to occur.

(3) TEST AND BRANCH. Used to interrupt the sequential count of steps.

(4) TEST AND CLEAR. Used to return to the initial instruction in the program.

(5) EXECUTE. Used to actuate control lines to data handling circuits.

(6) TEST AND EXECUTE. Used to conditionally actuate control lines.

(7) CLR. Used to return to the initial instruction in the program.

Control sequences and associated flow diagrams for the micro controller are contained in Paragraphs 5.9.3 through 5.9.6.

5.9.2 CONFIGURATION CONTROL LINES

Data flow in and out of the buffer is controlled by four Buffer Configuration Control lines (IBCC0, IBCC1, IBCC2, and IBCC3). It is the controller's responsibility to control all four lines when performing any of the commands in Group 1 or Group 2 (refer to Paragraph 4.2.4.1 for definitions of the Group commands).

For Automatic Continuous commands, the buffer assumes the responsibility for IBCC0, IBCC2, and IBCC3; the controller need be concerned with IBCC1 only. IBCC1 false will enable the straight automatic type commands; IBCC1 true will cause automatic and continuous data transfer. Further descriptions are contained in the following paragraphs.

5.9.3 BUFFER/CONTROLLER COMMANDS (GROUP 1)

5.9.3.1 Write Buffer Control Sequence

When the Write Buffer flip-flop U150 pin 11 (sheet 15, zone D2) is set, the Write Buffer Micro Controller (WBMC) is enabled at pin 7 of the Write Buffer Program Counter (WBPC) U163 (sheet 17, zone F4). Since the WBPC is normally in state 0, the fall of NWB at pins 14 and 2 of U162 (zone E4) enables the Write Buffer Sequence Decoder (WBSD) causing WBSQ0L to go low at pin 9.

Refer to the write buffer simplified flow diagram shown in Figure 5-54* and to the write buffer timing diagram shown in Figure 5-55* in conjunction with the following explanation of the Write Buffer Control sequence.

(1) Step 0. In Step 0 of the Write Buffer Control Sequence, U202 (sheet 17, zone D2) the Request flip-flop is set, asserting IREQ to the interface. The WBPC waits in Step 0 until the controller replies with the leading edge of Answer (NANS), indicating that the controller has placed data on the interface data lines.

If the controller replies with Last Word (ILWD) in Automatic Continuous mode, or the buffer is full, the WBMC branches to Step 5. Otherwise, the WBPC goes to Step 1.

(2) Step 1. In Step 1, the WBMC requests a memory cycle, clears the Write Buffer latches, and increments the WBPC on the rise of the next clock.

(3) Step 2. During Step 2 the WBMC loads the Write Buffer latches from the data lines and enters Step 3 on the next clock transition.

(4) Step 3. In Step 3 the WBMC causes the REQ flip-flop to reset and the WBMC waits for the controller to clear its IANS line. When IANS is cleared, the WBMC increments to Step 4 on the next clock transition.

(5) Step 4. In Step 4, the WBPC waits for the completion of the memory cycle. When the cycle is completed, the WBMC returns to Step 0, then sets the Request flip-flop. Setting the Request flip-flop serves to inform the controller that the next data character may be placed on the line.

(6) Step 5. The WBMC enters Step 5 when ILWD has been received from the controller, the buffer is full, or end of Automatic Continuous is received. In Step 5, the WBMC stores the address of the last word in the Address Counter latches. The WBMC then clears the Address Counter.

When the controller clears ILWD the WBPC increments to Step 6 on the next clock transition.

(7) Step 6. In Step 6, the WBMC clears the Request flip-flop. If the mode is not Automatic Continuous, the WBMC clears the Write Buffer flip-flop disabling the

*Foldout drawing, see end of this section.

WBMC and ending the Write Buffer operation. If the mode is Automatic Continuous, the Write Tape flip-flop (U130 pin 11, sheet 15 zone G2) is set, initiating the Write Tape sequence.

If the Automatic Continuous mode is asserted, the WBPC increments to Step 7 on the next clock cycle.

(8) Step 7. In Step 7, if the First Time flip-flop (FTACH) has not been cleared, the WBMC WAITS FOR THE WTMC (Write Tape Micro Controller) to halt in WTSQ7H, indicating that the Write Tape sequence is completed. If FTACH is set, or the WTMC has finished, WBMC proceeds to Step 8.

(9) Step 8. In Step 8, the WBMC toggles the AUTCOD flip-flop (U187 pin 11, sheet 18 zone G3) which changes the BCC lines to write the opposite buffer half and clears FTACH. The WBSD is then allowed to interpret WBPC state 1000 as state 000 which starts the WBMC in Step 0 again. Any subsequent branch or clear will return the counter to the lower half of the counter states.

5.9.3.2 Read Buffer Control Sequence

When the Read Buffer flip-flop (U150 pin 15, sheet 15 zone C2) is set, the Read Buffer Micro Controller (RBMC) is enabled. The Read Buffer Program Counter (RBPC) (U186, sheet 16 zone E3) is enabled by the rise of the signal RB at pin 7. The Read Buffer Sequence Decoder (RBSD) is enabled by the fall of NRB at pins 14 and 2 of U185 (zone C3).

Since the RBPC is initially in Step 0, RBSQ0L (Read Buffer Sequence 0 Low) falls, starting the Read Buffer Control Sequence in Step 0.

Refer to the Read Buffer simplified flow diagram shown in Figure 5-56* and to the Read Buffer timing diagram in Figure 5-57* in conjunction with the following explanation of the Read Buffer Control Sequence.

(1) Step 0. In Step 0 of the Read Buffer Control Sequence, the Request flip-flop (U202, sheet 17 zone D2) to the interface is cleared. This is done to clear any set caused by a previous character transfer.

If there is no indication that the Last Word has been transferred (indicated by COMPL), the RBMC requests the next memory cycle. If COMPL has been detected, the RBMC branches to Step 5.

The RBMC waits in Step 0 until the requested memory cycle has actually started, thus indicating that the memory will output data to the controller within 700 nanoseconds. When the cycle starts, NMAC1 (sheet 16 zone G5) is asserted (low) causing the RBPC to increment on the next clock cycle into Step 1.

(2) Steps 1 and 2. The RBMC waits in Step 1 for 167 nanoseconds for the memory to output data, then increments to Step 2 for an additional 167 nanoseconds. This cycle is a no-operation time fill.

(3) Step 3. In Step 3, the RBMC sets the Request flip-flop, asserting Request to the controller. In Step 3, the RBMC waits for the controller to respond with an IANS pulse. On the clock pulse after the leading edge of IANS has been detected the RBPC increments to Step 4.

(4) Step 4. In Step 4, the RBMC waits for the controller to clear its IANS pulse, indicating the data has been accepted by the controller. On the leading edge of IANS going false, the RBMC clears the RBPC and returns to Step 0.

(5) Step 5. Step 5 is reached only if COMPL has been detected. Step 5 is a no-operation time fill on the next clock transition. The RBPC then increments to Step 6.

*Foldout drawing, see end of this section.

(6) Step 6. In Step 6, the Address Counter is preset and, if the operation is not an Automatic Continuous mode the Read Buffer flip-flop is cleared. This causes the RBSD to be disabled and the RBPC to return to Step 0. If the mode is Automatic Continuous, the RBPC increments to Step 7 on the next clock transition.

(7) Step 7. In Step 7, the RBPC waits for the Read Tape Micro Controller (RTMC) to reach Step 7. When the RTMC reaches Step 7, the RBMC is free to output the next buffer half to the controller. The RBPC is allowed to count through its remaining steps until it reaches Step 1000. Step 1000 is decoded as Step 000 by the RBSD. The algorithm then starts again at Step 0 for the next buffer half.

5.9.4 BUFFER/FORMATTER COMMANDS (GROUP 2)

5.9.4.1 Write Tape Control Sequence

When the Write Tape flip-flop (U130 pin 11, sheet 15, zone H2) is set, the Write Tape Micro Controller (WTMC) is enabled at pin 7 of the Write Tape Program Counter (WTPC) (U123, sheet 19, zone F5). Since the WTPC is normally in Step 0, the fall of NWT at pins 2 and 14 of the Write Tape Sequence Decoder (WTSD) causes WTSQ0L to go low at pin 9.

Refer to the Write Tape simplified flow diagram shown in Figure 5-58* and to the Write Tape timing diagram shown in Figure 5-59* in conjunction with the following explanation of the Write Tape Control Sequence.

(1) Step 0. In Step 0 of the Write Tape Control Sequence, the buffer is asserting IWRT to the formatter. Step 0 causes the WTMC to issue a GO to the formatter, then waits until the trailing edge of GO is detected before advancing to Step 1. The Tape Error flip-flop (U109 pin 11, sheet 14, zone F7) is also cleared in Step 0 as a function of GGO signal of the GO generator.

(2) Step 1. During Step 1, the WTMC requests a memory cycle and allows incrementing the WTPC on the rise of the next clock cycle.

(3) Step 2. The Memory Cycle Logic loads the Write Tape latches with a character from memory and the WTMC waits for a Write Strobe (IWSTR) from the formatter. The IWSTR from the formatter indicates that the character has been transferred.

(4) Step 3. The WTMC waits for the trailing edge of IWSTR then increments to Step 4.

(5) Step 4. The WTMC enters Step 4 when the trailing edge of IWSTR has been detected. In Step 4 a test is made of NTLWD to determine if the buffer contents have been completely transferred.

If the test indicates the presence of additional data to transfer, the WTMC branches to Step 1.

If the buffer is empty as indicated by NTLWD being low, the WTPC advances to Step 5.

(6) Step 5. In Step 5, the address of the last record transferred is loaded into the Address Latches and the Address Counter circuitry is preset. The WTMC then waits until the trailing edge of IFBY is detected, then inspects the error lines for indication of detected errors. If no errors are detected, or the retry limit is reached, the WTPC branches to Step 7. If an error is indicated, and the retry limit has not been reached, the WTPC advances to Step 6 on the trailing edge of IFBY.

(7) Step 6. The first action taken in Step 6 is incrementing of the retry counter. Step 6 is concerned with rereading the last data transferred to tape in order to position the tape for another write operation.

*Foldout drawing, see end of this section.

The tape direction signal is reversed and an IGO is sent to the formatter to read the tape in reverse. The tape error flip-flop is cleared.

At the trailing edge of IFBY a branch is made to Step 0. The rewrite operation can now be attempted.

(8) Step 7. In Step 7, the retry counter is cleared and a test made to determine if the buffer is in the Automatic Continuous mode. If not in the Automatic Continuous mode, the Write Tape flip-flop is reset, disabling the WTMC and ending the Write Tape operation. If the Automatic Continuous mode is active, the WTMC waits for an indication that the WBMC has completed its operation. The WTMC then branches to Step 0.

5.9.4.2 Read Tape Control Sequence

When the Read Tape flip-flop (U130 pin 15, sheet 15, zone F2) is set, the Read Tape Micro Controller (RTMC) is enabled. If the File Mark Search flip-flop U144 (sheet 18, zone F7) is also set, the operation becomes a File Mark Search operation.

Refer to the Read Tape simplified flow diagram shown in Figure 5-60* for the following explanation of the Read Tape Control Sequence.

(1) Step 0. In Step 0 of the Read Tape Control Sequence the buffer GO generator is enabled and, if DBY is false from the formatter, an IGO pulse is sent to the formatter. The Tape Error flip-flop is also cleared. The RTMC remains in Step 0 until GO has been sent and DBY from the formatter is true, then increments to Step 1.

(2) Step 1. In Step 1, the Read Tape latches are cleared in preparation for accepting a character from the formatter.

In the Read Tape mode the RTMC waits for the leading edge of the Read Tape Strobe (IRSTR) from the formatter. If IDBY falls before the IRSTR occurs, a last word is indicated and the RTMC branches to Step 5. A branch is also made if a buffer overflow condition is indicated.

In the File Mark Search (IFMS) mode the RTMC continues to Step 2 without waiting for IRSTR.

(3) Step 2. In Step 2 of the IFMS mode the RTMC waits for IDBY to drop, indicating the end of a record. If an IFMK or Load Point (ILDP) indication occurs, the RTMC clears the buffer and the formatter is cleared by FEN when LDP is asserted. IFMK or ILDP is indicated to the interface.

If in the RT mode, the Read Tape latches are loaded from the formatter interface and a memory cycle is requested.

In either mode the RTMC increments to Step 3 when RTRUNH and the next clock occur.

(4) Step 3. In Step 3, if in the FMS mode, the RTMC immediately is cleared to Step 0 to search for the next record. If in the RT mode, the RTMC awaits the fall of IRSTR, then goes to Step 4.

(5) Step 4. In Step 4, the RTMC branches to Step 1 to accept the next character of the record.

(6) Step 5. In Step 5, the contents of the Address Counter are latched into the Address latches, the record is finished, and the Address Counter is preset.

If the Tape Error flip-flop has been set and the number of retries has not been exceeded, the RTMC waits for IFBY to drop before going to Step 6 (entry point on flow diagram). If no retry is to be attempted, the RTMC branches to Step 7 (entry point on flow diagram).

*Foldout drawing, see end of this section.

(7) Step 6. In Step 6, the Error Counter is incremented, the tape direction is reversed, and an IGO is sent to the formatter to backspace the tape. When the test for GO is completed, the RTMC clears the RTPC to Step 0 to reread the record.

(8) Step 7. Step 7 indicates that the record is complete or the retries are exhausted. The RTMC clears the error counter and, if not in the Automatic Continuous mode, clears the RT latch. If in the Automatic Continuous mode and no EOO has been given, the Read Buffer (RB) flip-flop is set to start the Read Buffer sequence.

In the Automatic Continuous mode, the RTPC waits until the Read Buffer sequence is complete if the FTACH flip-flop is set. Otherwise, the AUTOCOD flip-flop (U187 pin 11, zone G3) is toggled and the FTACH flip-flop is cleared as the RTPC branches to Step 0.

5.9.5 AUTOMATIC COMMANDS (GROUP 3)

5.9.5.1 Automatic Write Tape

The Automatic Write operation is a combination of a Write Buffer Control Sequence followed by a Write Tape Control Sequence. Reference should be made to the Write Buffer Control Sequence, Paragraph 5.9.3.1, and to the Write Tape Control Sequence, Paragraph 5.9.4.1, in conjunction with the following discussion.

Upon receipt of an Automatic Write Tape command the WB flip-flop is set and ABSY goes true. In this configuration the buffer is not split and the buffer operation utilizes the 'A' reference circuitry. When the WB sequence has been completed, the Write Buffer Micro Controller resets the WB flip-flop and sets the WT flip-flop which enables the Write Tape sequence. At the end of the WT sequence the Write Tape Micro Controller resets the WT flip-flop clearing the buffer for the next command.

There are two advantages of using this Automatic Write Tape command versus using the individual Write Buffer (WB) followed by a Write Tape (WT) command. First, the controller is not required to issue two individual commands; second, the controller does not need to be concerned with the buffer input/output configuration control lines. The Automatic Write Tape mode requires the controller to configure the buffer in either configuration 0000 or 1010. Configuration 1010 may also be used with Read Tape Automatic commands.

5.9.5.2 Automatic Write Tape Continuous

The Automatic Write Tape Continuous operation is a combinational sequence of WB and WT commands. The operation always starts with an initial Write Buffer into Buffer B and ends with a final Write Tape Sequence from either Buffer A or Buffer B. The details of the individual Write Buffer and Write Tape Control sequences are contained in Paragraphs 5.9.3.1 and 5.9.4.1, respectively, and should be referenced in conjunction with the following discussion.

Figure 5-61 is an illustration of the sequence of events for an Automatic Write Tape Continuous transfer. The buffer will continue this sequence until the controller emits an End Of Operation (IEOO) signal. IEOO must occur in response to the first request following a LWD indication for the previous record. IEOO should be asserted until both buffer busy signals go false.

There are a number of advantages when using the Automatic Write Tape Continuous command versus a step-by-step sequence of the individual WB and WT commands. These advantages are:

(1) The controller is required to generate only one command strobe (IGOI) to begin the operation and a subsequent IEOO to end the operation.

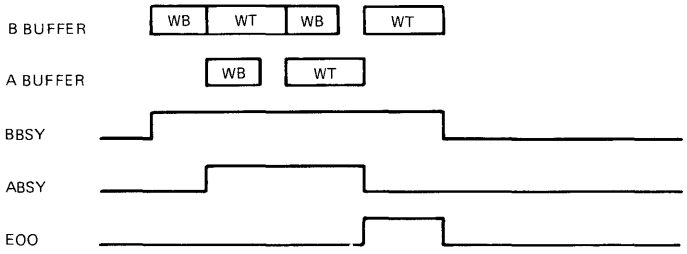


Figure 5-61. Automatic Write Continuous Transfer

(2) Maximum through-put can be attained with the proper choice of buffer length, tape speed, and record size. Figure 4-14 illustrates this 3-way relationship.

(3) The controller does not need to be concerned about input/output configuration control since the buffer automatically selects the correct configuration for the desired data flow.

In the Automatic Write Tape Continuous mode, the buffer configuration lines are controlled internally and are switched from configuration 1001 to configuration 1110, depending on which half of the buffer is being read or written at a given time.

Both Buffer Busy lines will be asserted as shown in Figure 5-61. In this configuration the controller sees the buffer as a continuous source of data and needs only to respond to the buffer IREQ line in order to cause data to be transferred. Data transfer will continue until IEOT is sensed or until the controller issues an IEOO. Data transfer may occur in bursts determined by the controller without issuing an individual IGO for each burst.

It is important to differentiate between Automatic and Automatic Write Tape Continuous. The specific difference is the IBCC1 configuration control line and the use made of it by the controller. When IAUTO is true, and IBCC1 is not true, the buffer is configured in the straight automatic mode. IAUTO true and IBCC1 true (split buffer) sets up the automatic continuous sequence.

5.9.5.3 Automatic Read Tape

The Automatic Read Tape operation is a combination of a Read Tape (RT) sequence followed by a Read Buffer (RB) sequence. The details of the individual Read Tape and Read Buffer sequences are contained in Paragraphs 5.9.4.2 and 5.9.3.2, respectively, and should be referenced in conjunction with the following discussion.

Upon receipt of an Automatic Read Tape command, the RT flip-flop is set and ABSY goes true. A tape formatter IGO is generated by the buffer GO generator. In the Automatic Read Tape configuration the buffer is not split and utilizes the 'A' reference circuitry. Upon completion of the RT sequence the RT flip-flop is reset and the RB flip-flop is set by the Read Tape Micro Controller. The IABSY line will remain asserted until the end of the Read Buffer operation.

Upon completion of the RB sequence (refer to Paragraph 5.9.3.2) the buffer is ready to accept another command and IABSY will fall. There are two advantages of using the Automatic Read command versus using the individual Read Tape (RT) followed by a Read Buffer (RB) command. First, the controller is not required to issue two individual

commands; second, the controller does not need to be concerned with the buffer input/output configuration control lines. The Automatic Read Tape mode requires the controller to configure the buffer in either configuration 0001, 0011, or 1011. Configuration 1011 may also be used for Write Tape Automatic commands.

5.9.5.4 Automatic Read Tape Continuous

The Automatic Read Tape Continuous operation is a combinational sequence of RT and RB commands. The operation always starts with an initial Read Tape into Buffer A and ends with a final Read Buffer sequence. The details of the individual Read Tape and Read Buffer sequences are contained in Paragraphs 5.9.4.2 and 5.9.3.2, respectively, and should be referenced for the following discussion.

Figure 5-62 is an illustration of the sequence of events for this automatic continuous transfer. The buffer will continue this sequence until the controller emits an End Of Operation (IEOO) signal. IEOO must occur after the output of the last desired record has begun as indicated in the illustration. Note the time when IEOO was issued for the particular sequence shown. Due to the fact that the buffer always reads one record ahead of the controller, after IEOO is issued the last record in the buffer will not be output. This record may be output by a manual Read Buffer command or, alternately, by backspacing tape and starting a new read continuous operation.

There are a number of advantages when using this Automatic Read Tape Continuous command versus a step-by-step sequence of the individual RT and RB commands. These advantages are:

(1) The controller is required to generate only one command and one command strobe (IGOI) to begin the operation, and a subsequent IEOO to end the operation.

(2) Maximum throughput can be attained with the proper choice of buffer length, tape speed, and record size. Figure 4-14 illustrates this 3-way relationship.

(3) The controller does not need to be concerned about input/output configuration control since the buffer automatically selects the correct configuration for the desired data flow.

In the Automatic Read Tape Continuous mode, the buffer configuration lines are controlled internally and are switched from configuration 1001 to configuration 1110, depending on which half of the buffer is being read or written at a given time.

Both Buffer Busy lines will be asserted as shown in Figure 5-62. In this configuration the controller sees the buffer as a continuous source of data and needs only to respond to the buffer IREQ line in order to cause data to be transferred. Data transfer will continue until IEOT is sensed or until the controller issues an IEOO. Data transfer may occur in bursts determined by the controller without issuing an individual GO for each burst.

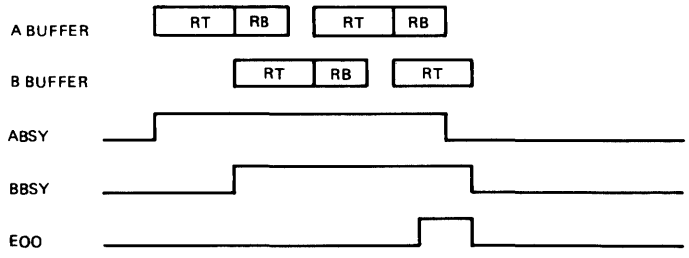


Figure 5-62. Automatic Read Continuous Transfer

5.9.6 MISCELLANEOUS COMMANDS (GROUP 4)

There are a number of commands that are executed by the buffer and its control logic but do not require buffer storage or buffer clocking. These commands are uniquely decoded, converted, then sent to the selected tape formatter. The code conversion is performed and the actual command that is generated is shown in Table 3-1.

5.9.6.1 File Mark Operation

The buffer ensures writing file marks, detecting them when reading, and searching for them when commanded to do so.

The buffer contains the logic for searching for file marks. The search can be made in either the forward or reverse mode of tape operation. Command coding for these search operations sets the RT flip-flop. This means that the buffer goes busy for these operations; however, no data are loaded into the buffer and previous data will be preserved.

The File Search command, as it is sent to the formatter, is simply a Read Reverse/Forward command. If the record read does not contain a file mark or is not a file mark itself, the buffer will generate another GO strobe instructing the tape formatter to read another record. The file search operation continues until:

(1) A file mark is found (IFMK pulse).

(2) If the operation is a file search reverse, the sequence will halt when the transport reaches BOT (Load Point).

The operation is stopped when either FMK or LDP occurs and subsequently clears the input command register. Details of the File Mark search are contained in the Read Tape Control Sequence discussion, Paragraph 5.9.4.2.

5.9.6.2 Back-Space/Forward-Space Operation

The buffer takes care of back-spacing and forward-spacing over one record on tape via dummy Read Reverse and Read Forward commands to the tape formatter.

The codes for these commands do not activate any of the four basic buffer functions; hence, the buffer does not go busy. Controller IGOI enables the circuitry that generates the formatter GO strobe. The buffer converts the code and sends it to the formatter. In this operation, the customer must monitor FBY (Formatter Busy) before attempting to execute any Buffer/Formatter commands. The customer may command the buffer to execute Buffer/Controller (Group 1) commands while monitoring these Group 4 commands.

5.9.6.3 Erase Tape Operation

The buffer also takes care of the erase tape commands in much the same manner as the operation described in Paragraph 5.9.6.2.

The buffer does not go busy when carrying out these commands. The buffer code converts the command and then strobes a GO pulse to the selected tape formatter. The formatter performs a dummy write tape operation for both erase commands. The fixed length erase is handled in its entirety by the tape formatter. The variable length erase command is initiated by the tape formatter via the buffer but a length of tape equal to the length of the previous record stored in the buffer will be erased.

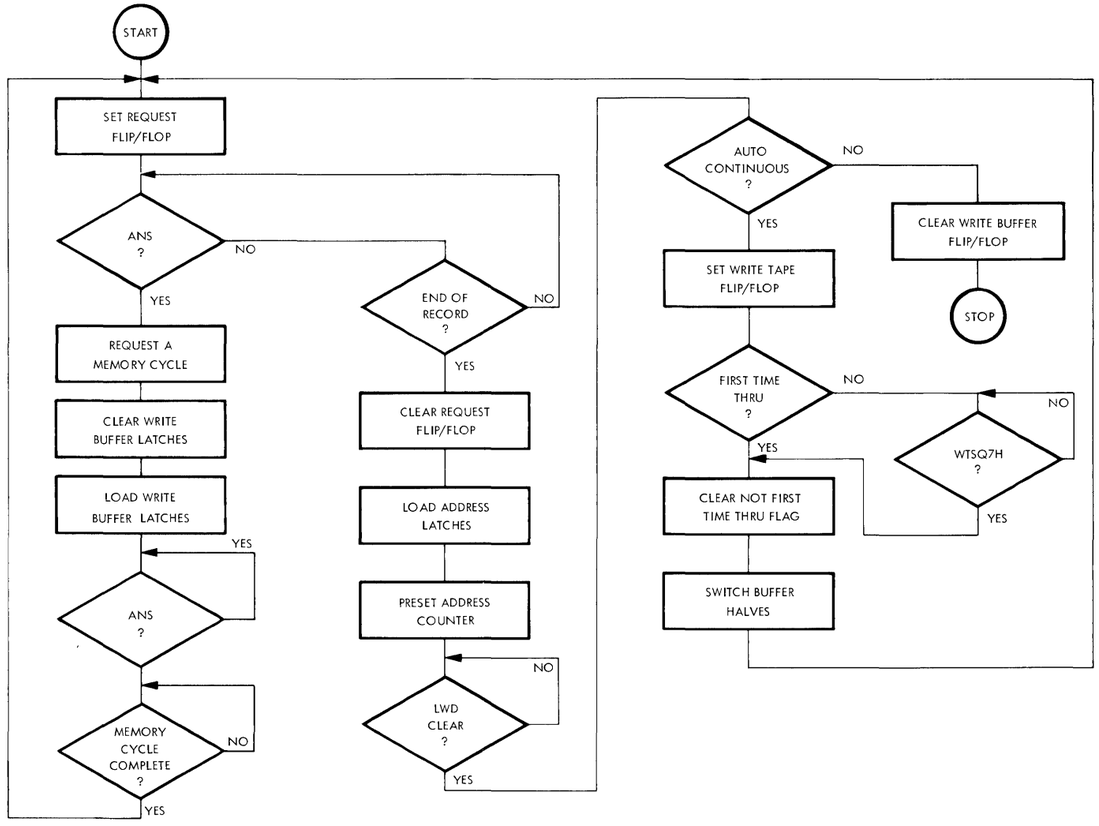


Figure 5-54. Write Buffer, Simplified Flow Diagram

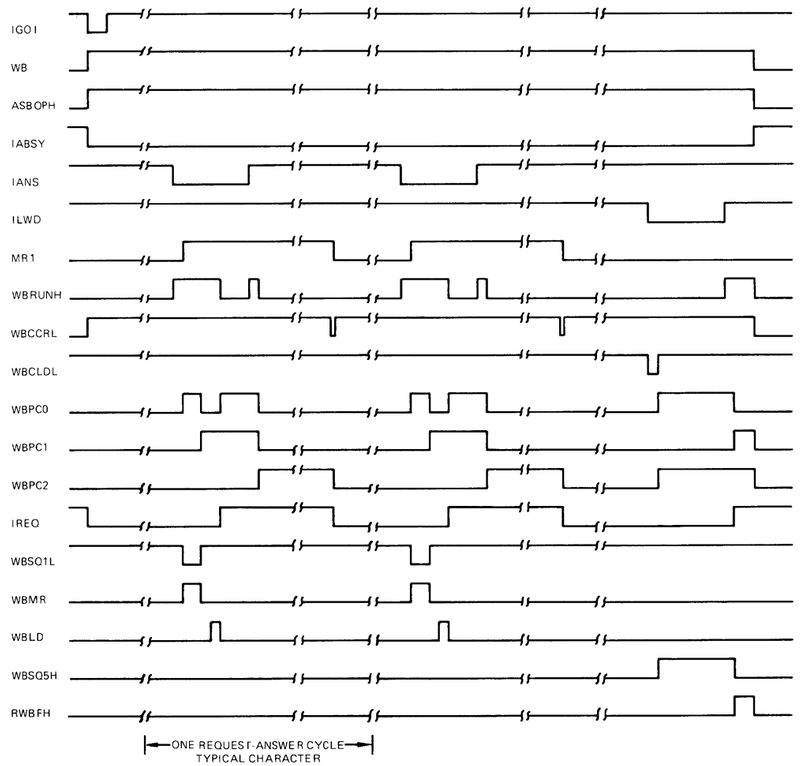


Figure 5-55. Write Buffer, Timing Diagram

802B

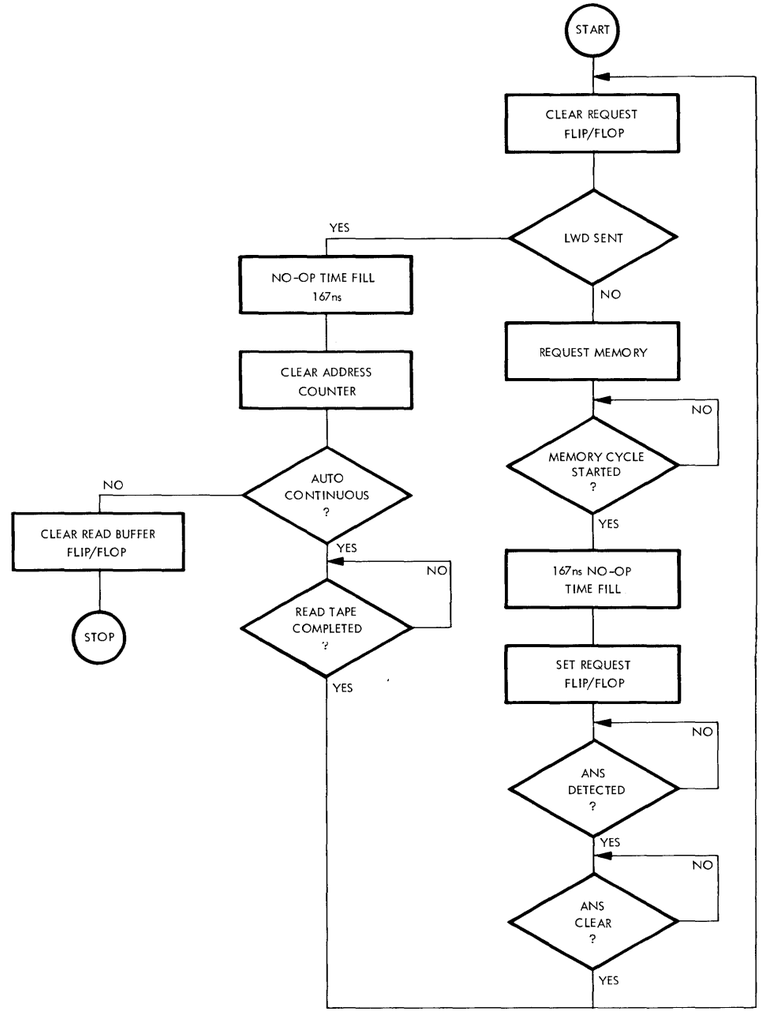


Figure 5-56. Read Buffer, Simplified Flow Diagram

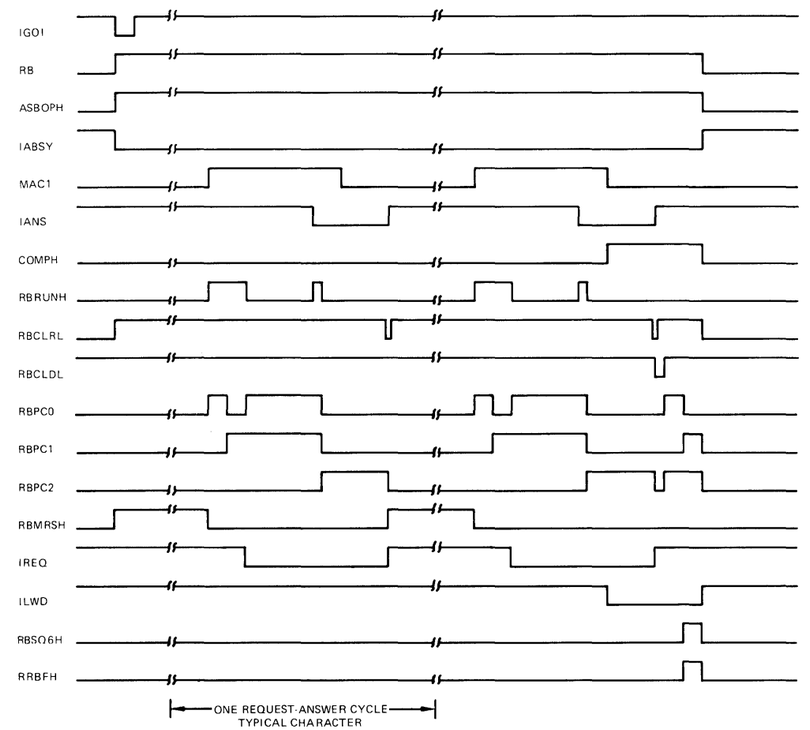


Figure 5-57. Read Buffer, Timing Diagram

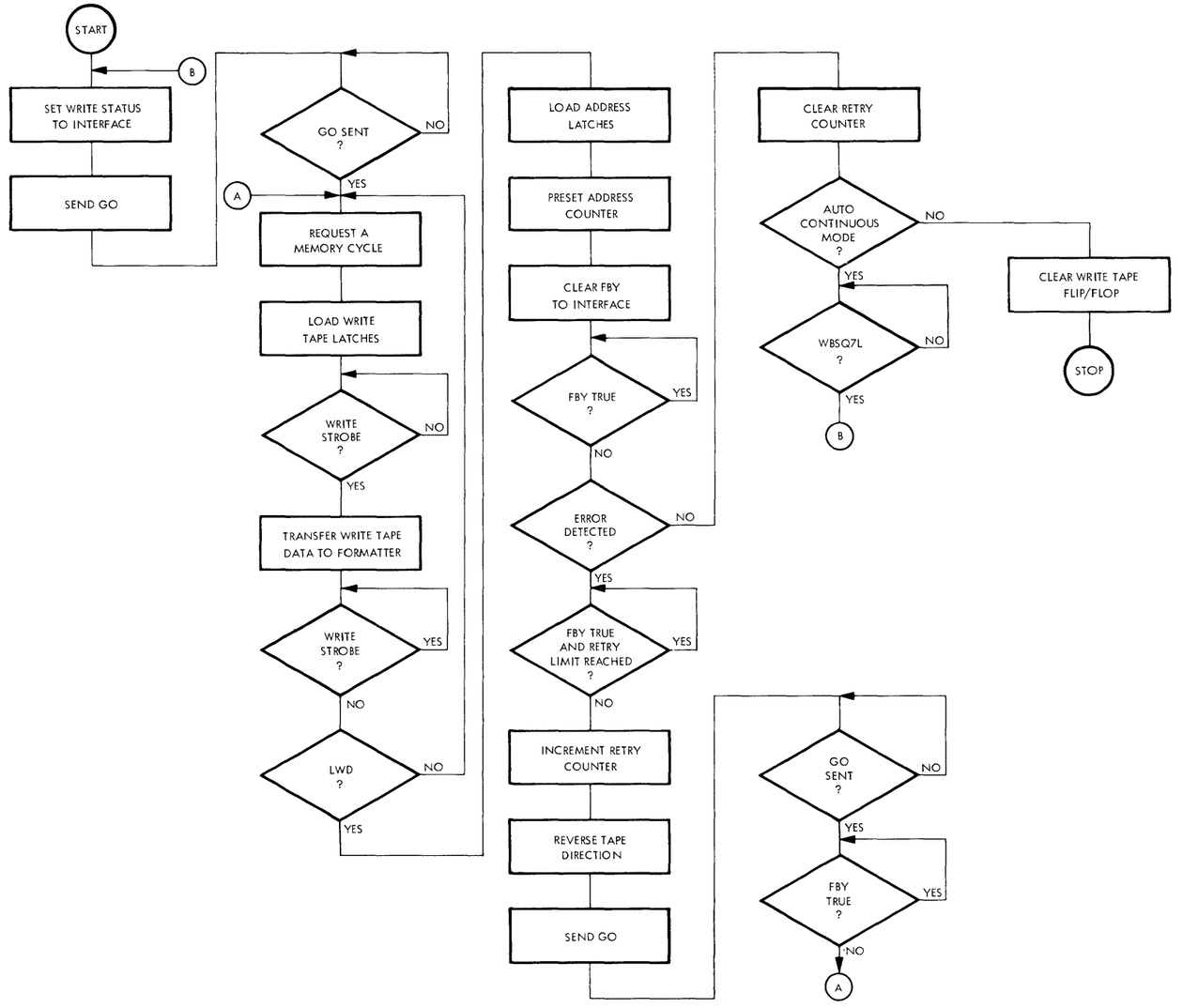
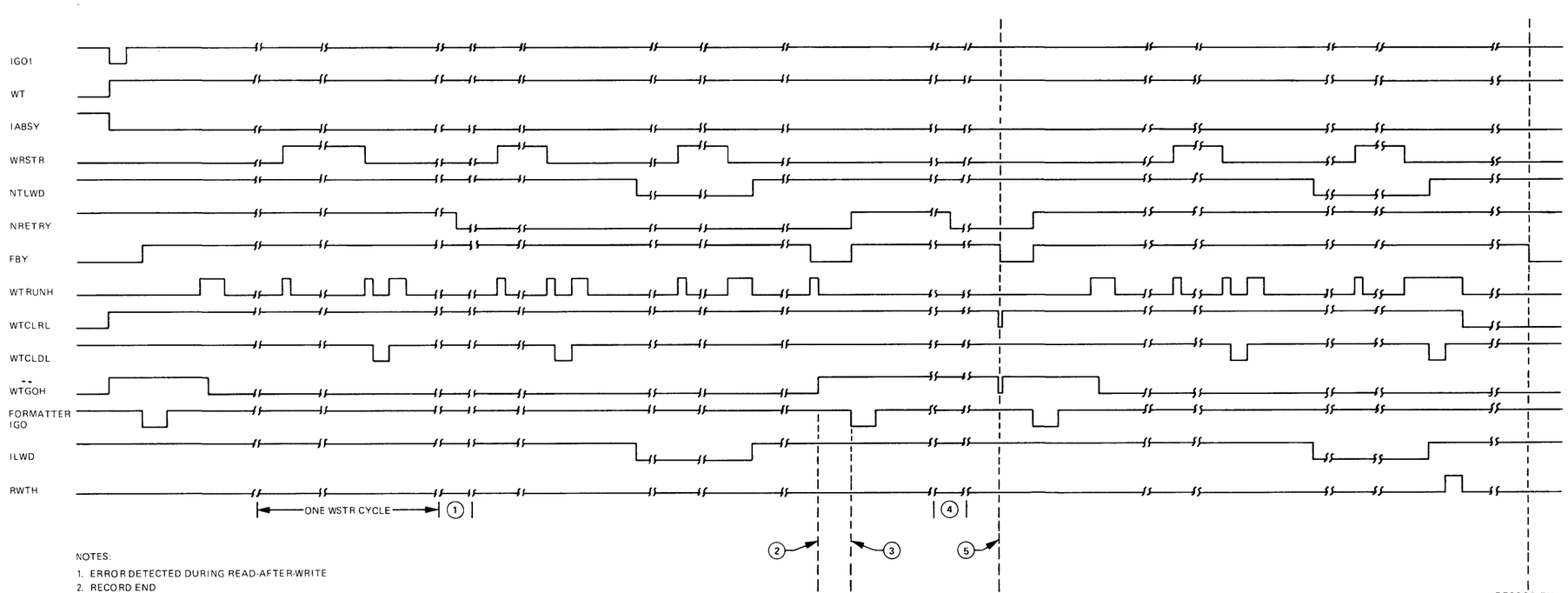


Figure 5-58. Write Tape, Simplified Flow Diagram



NOTES:

1. ERROR DETECTED DURING READ-AFTER-WRITE
2. RECORD END
3. BEGIN BACKSPACE
4. ERROR DETECTED ON BACK SPACE
5. BACKSPACE ENDS–WRITE FORWARD BEGINS

Figure 5-59. Write Tape, Timing Diagram

802B

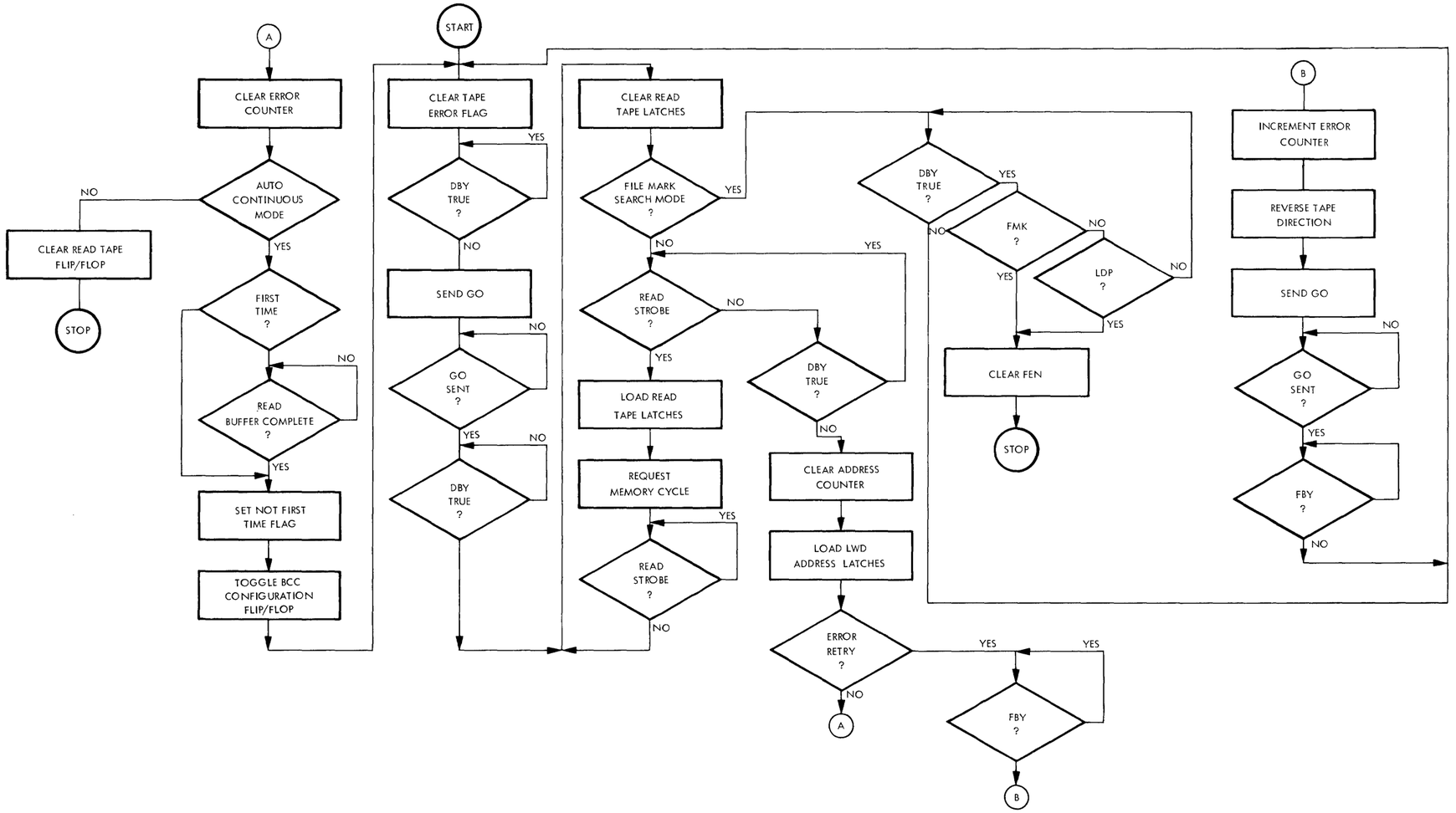


Figure 5-60. Read Tape, Simplified Flow Diagram

SECTION VI
MAINTENANCE ADJUSTMENTS

6.1 INTRODUCTION

This section provides information necessary to perform maintenance adjustments and parts replacement. Sections IV and V contain the theory of operation of components and circuits for reference.

6.2 FUSE REPLACEMENT

Three fuses are located on the power supply assembly at the front of the formatter. A fourth fuse (line fuse) is located at the rear of the formatter.

- Line Fuse: 2 amp, SB
- + 20v Circuits: 1 amp, FB
- + 5v Circuits: 10 amp, FB
- —5v Circuits: 1 amp, FB

6.3 SCHEDULED MAINTENANCE

The formatter is designed to operate with a minimum of maintenance and adjustments and replacement of parts is designed to be as simple as possible. Repair equipment is kept to a minimum and only simple tools (e.g., Phillips-head screwdriver, standard screwdriver) are required in most cases.

6.4 CLEANING THE FORMATTER

The PCBAs may require periodic cleaning to remove accumulated dust. It is recommended that a low-pressure dry filtered air source be employed for this purpose.

To clean the front panel, use a lint-free cloth moistened in isopropyl alcohol or Du Pont Freon TF.

6.5 PARTS REPLACEMENT ADJUSTMENTS

When it is necessary to repair or replace a major formatter assembly (e.g., Power Supply, PE Write PCBA, PE Read PCBA, Buffer PCBA) the basic adjustments described in Paragraphs 6.6 through 6.6.6.4 should be performed.

6.6 ELECTRICAL ADJUSTMENTS

The following paragraphs describe the test configurations, test procedures, and related adjustments within the formatter.

The following test equipment (or equivalent) is required.

(1) Oscilloscope, Tektronix 561 (or equivalent), vertical and horizontal sensitivity specified to ± 3 percent accuracy.

(2) Digital Volt Meter, Fairchild 7050, ± 0.1 percent specified accuracy.

(3) Monsanto Counter Timer Model 100B.

6.6.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.6.

When the measured value of any parameter is within the acceptable limits, NO ADJUSTMENT should be made. Should the measured value fall outside the specified acceptable limits, adjustments should be made in accordance with the relevant procedure. When adjustments are made, the value set should be the exact value specified (to the best of the operator's ability).

6.6.2 POWER SUPPLY PCBA (+ 5v)

Potentiometer R17 is employed to adjust the + 5v power supply. Refer to Schematic No. 103304 and Assembly No. 103305.

6.6.2.1 Test Configuration

(1) Loosen the two captive screws located on the front panel and extend the formatter unit.

(2) Depress and release the spring-loaded button located on the right side of the unit; this permits the front panel to swing down.

(3) Remove the four Phillips-head screws securing the perforated cover to the formatter assembly. The cover can now be removed.

(4) Ensure that all PCBAs are installed and properly seated.

6.6.2.2 Test Procedure

NOTE

The ground [GND] and the + 5v test points are located at the rear of the PE Read PCBA, adjacent to J2.

(1) Using a Fairchild 7050 Digital Volt Meter (or equivalent) measure the voltage between the GND (0v) and the + 5v test points on the PE Read PCBA as follows.

(2) Acceptable limits:

- + 5.1v maximum
- + 4.9v minimum

6.6.2.3 Adjustment Procedure

When the acceptable limits are exceeded, adjust potentiometer R17 (located on the Power Supply PCBA) as follows.

(1) Monitor the voltage between the GND (0v) and the + 5v test point on the PE Read PCBA.

(2) Adjust R17 to + 5v.

6.6.2.4 Related Adjustments

The Fixed Oscillator must be checked and adjusted, if necessary, when adjustments are made to the + 5v power supply.

6.6.3 POWER SUPPLY PCBA (—5V)

Potentiometer R33 is employed to adjust the —5v power supply. Refer to Schematic No. 103304 and Assembly No. 103305.

6.6.3.1 Test Configuration

(1) Loosen the two captive screws located on the front panel and extend the formatter unit.

(2) Depress and release the spring-loaded button located on the right side of the unit. This permits the front panel to swing down.

(3) Remove the four Phillips-head screws securing the perforated cover to the formatter assembly. The cover can now be removed.

(4) Ensure that all PCBAs are installed and properly seated.

6.6.3.2 Test Procedure

NOTE

The ground [GND] and the —5v test points are located at the rear of the Read Recovery PCBA, adjacent to J2.

(1) Using a Fairchild 7050 Digital Volt Meter (or equivalent) measure the voltage between the GND (0v) and the —5v test points on the PE Read PCBA, as follows.

(2) Acceptable limits:

- —5.1v maximum
- —4.9v minimum

6.6.3.3 Adjustment Procedure

When the acceptable limits are exceeded, adjust potentiometer R33 (located on the Power Supply PCBA) as follows.

(1) Monitor the voltage between the GND (0v) and the —5v test point on the PE Read PCBA.

(2) Adjust R33 to —5v.

6.6.3.4 Related Adjustments

- None.

6.6.4 POWER SUPPLY PCBA (+ 20V)

Potentiometer R3 is employed to adjust the + 20v power supply. Refer to Schematic No. 103304 and Assembly No. 103305.

6.6.4.1 Test Configuration

(1) Loosen the two captive screws located on the front panel and extend the formatter unit.

(2) Depress and release the spring-loaded button located on the right side of the unit. This permits the front panel to swing down.

(3) Remove the four Phillips-head screws securing the perforated cover to the formatter assembly. The cover can now be removed.

(4) Remove the PE Write PCBA and the PE Read PCBA.

(5) Remove jumpers W21 and W22 from the Buffer PCBA; refer to Buffer Assembly No. 101811 for location of jumpers.

6.6.4.2 Test Procedure

(1) Using a Fairchild 7050 Digital Volt Meter (or equivalent) measure the voltage between A45 of J2 and the ground (GND) located at the rear of the Buffer PCBA.

NOTE

Jumpers W21 and W22 must be removed prior to measurement of the + 20v.

(2) Acceptable limits:

- +20.2v maximum
- +19.8v minimum

(3) Replace jumpers W21 and W22 if the values obtained in Step (2) are within the acceptable limits.

6.6.4.3 Adjustment Procedure

When the acceptable limits are exceeded, adjust potentiometer R3 (located on the Power Supply PCBA) as follows.

(1) Monitor the voltage between A45 and GND located at the rear of the Buffer PCBA.

(2) Adjust R3 to +20v.

(3) Replace jumpers W21 and W22; refer to Buffer Assembly No. 101811 for location.

6.6.4.4 Related Adjustments

- None.

6.6.5 FIXED OSCILLATOR (SINGLE SPEED FORMATTER)

A fixed frequency oscillator is employed on the PE Write PCBA; refer to Schematic No. 101385 and Assembly No. 101386.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Fixed Oscillator.

6.6.5.1 Test Configuration

Establish test configuration outlined in Paragraph 6.6.2.1.

6.6.5.2 Test Procedure

(1) Calculate the appropriate frequency for the Fixed Oscillator as follows.

- Frequency (kHz) = 9.6 X Speed (ips)

(2) Record the operating frequency of the oscillator as measured between TP4 and TP1 (0v) on the Single Fixed Oscillator, using a Monsanto Counter Timer Model 100B (or equivalent).

(3) Acceptable limits:

- ±0.5 percent of value calculated in Step (1).

6.6.5.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits, proceed as follows.

(1) Connect a Monsanto Counter Timer Model 100B (or equivalent) between TP4 and TP1 (0v) on the Single Fixed Oscillator.

(2) Adjust potentiometer R5, located on the fixed oscillator assembly, until the measured frequency equals the calculated oscillator frequency (refer to Paragraph 6.6.5.2).

6.6.5.4 Related Adjustments

- None.

6.6.6 FIXED OSCILLATOR (DUAL SPEED FORMATTER)

Formatters designed to operate with transports of different speeds are equipped with a dual fixed oscillator. Refer to the relevant schematic and assembly drawings.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Fixed Oscillator.

6.6.6.1 Test Configuration

Establish test configuration outlined in Paragraph 6.6.2.1.

6.6.6.2 Test Procedure

(1) Set the ISPEED interface line false; this enables the oscillator circuitry to operate at the higher frequency.

(2) Calculate the appropriate frequency for the Fixed Oscillator as follows.

- Frequency (kHz) = 9.6 X Speed (ips)

(3) Record the operating frequency of the oscillator as measured between TP4 and TP1 (0v) on the Dual Fixed Oscillator using a Monsanto Counter Timer Model 100B (or equivalent).

(4) Acceptable limits:

- ±0.5 percent of value calculated in Step (2).

(5) Set the ISPEED interface line true; this enables the oscillator circuitry to operate at the lower frequency.

(6) Repeat Steps (2) through (4).

6.6.6.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits, proceed as follows.

(1) Set the ISPEED interface line false.

(2) Connect a Monsanto Counter Timer Model 100B (or equivalent) between TP4 and TP1 (0v) on the Fixed Oscillator assembly.

(3) Adjust potentiometer R5 on the Fixed Oscillator assembly until the measured frequency equals the higher of the calculated oscillator frequencies (refer to Paragraph 6.6.6.2).

(4) Set the ISPEED interface line true.

(5) Adjust potentiometer R17 on the Fixed Oscillator assembly until the measured frequency equals the lower of the calculated oscillator frequencies (refer to Paragraph 6.6.6.2).

6.6.6.4 Related Adjustments

- None.

6.6.7 TRACKING OSCILLATOR (SINGLE SPEED FORMATTER)

A tracking oscillator is employed on the PE Read PCBA. Refer to the relevant schematic and assembly drawing.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Fixed Oscillator.

6.6.7.1 Test Configuration

(1) Establish test configuration outlined in Paragraph 6.6.2.1.

(2) Ensure that the formatter is in an inactive state, i.e., controlled transports not performing a read or write function.

6.6.7.2 Test Procedure

(1) Calculate the center frequency for the tracking oscillator as follows.

- Frequency (kHz) = 39.2 X Speed (ips)

(2) Record the center frequency of the oscillator measured between TP4 and TP1 on the Tracking Oscillator assembly using a Monsanto Counter Timer Model 100B (or equivalent).

(3) Acceptable limits:

- ±1 percent of value calculated in Step (1).

6.6.7.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits, proceed as follows.

(1) Connect a Monsanto Counter Timer Model 100B (or equivalent) between TP4 and TP1 (0v) on the Tracking Oscillator assembly.

(2) Adjust potentiometer R5, located on the Tracking Oscillator assembly until the measured frequency equals the calculated oscillator frequency (Paragraph 6.6.7.2).

6.6.7.4 Related Adjustments

- None.

6.6.8 TRACKING OSCILLATOR (DUAL SPEED FORMATTER)

Formatters designed to operate with transports of different speeds are equipped with a dual speed tracking oscillator. Refer to the relevant schematic and assembly drawing.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Tracking Oscillator.

6.6.8.1 Test Configuration

(1) Establish test configuration outlined in Paragraph 6.6.2.1.

(2) Ensure that the formatter is in an inactive state, i.e., controlled transports not performing a read or write function.

6.6.8.2 Test Procedure

(1) Set the ISPEED interface line false. This enables the oscillator circuitry designed to operate at the higher of the two specified frequencies.

(2) Calculate the appropriate center frequency for the PE Tracking Oscillator as follows.

- Frequency (kHz) = 39.2 X Speed (ips)

(3) Record the center frequency of the oscillator measured between TP4 and TP1 on the Tracking Oscillator assembly using a Monsanto Counter Timer Model 100B (or equivalent).

(4) Set the ISPEED interface line true. This enables the oscillator circuitry designed to operate at the lower of the two specified frequencies.

(5) Record the center frequency of the oscillator measured between TP4 and TP1 on the Tracking Oscillator assembly using a Monsanto Counter Timer Model 100B (or equivalent).

(6) Acceptable limits:

- +1 percent of value calculated in Step (1).

6.6.8.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits, proceed as follows.

(1) Set the ISPEED interface line false.

(2) Connect a Monsanto Counter Timer Model 100B (or equivalent) between TP4 and TP1 (0v) on the Tracking Oscillator assembly.

(3) Adjust potentiometer R5, located on the Tracking Oscillator assembly, until the measured frequency equals the higher of the calculated oscillator frequency (Paragraph 6.6.8.2).

(4) Set the ISPEED interface line true.

(5) Adjust potentiometer R17, located on the Tracking Oscillator assembly, until the measured frequency equals the lower of the calculated oscillator frequency (Paragraph 6.6.8.2).

6.6.8.4 Related Adjustments

- None.

SECTION VII
PARTS LIST AND SCHEMATICS

7.1 INTRODUCTION

This section includes illustrated parts lists, schematics, and assembly drawings.

7.2 ILLUSTRATED PARTS BREAKDOWN (IPB)

Figures 7-1 and 7-2, used in conjunction with Tables 7-1 and 7-2, provide identification by PERTEC part number for the mechanical and electrical components of the formatter.

7.3 SPARE PARTS

Table 7-3 provides a description of suggested spare parts for the formatter. The Customer should always furnish model number and serial number of the formatter when ordering parts.

7.4 PART NUMBER CROSS REFERENCE

Table 7-4 provides a cross reference to the manufacturer part number and typical PERTEC part number.

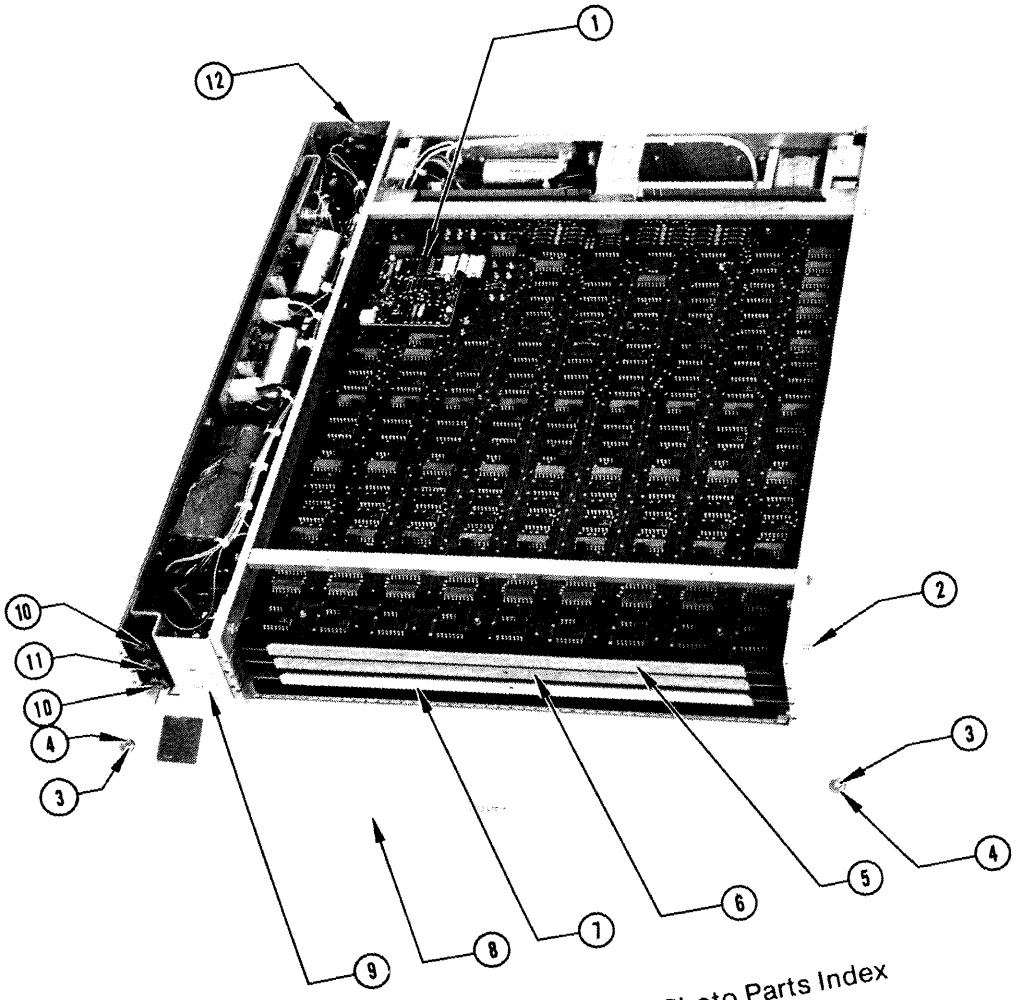


Figure 7-1. Buffered Formatter Photo Parts Index

Table 7-1
Buffered PE Formatter Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-1		
-1	102094-*	Tracking Oscillator
-2	615-0033	Latch Assembly
-3	615-7500	No. 10 Captive Fastener Floating Screw
-4	612-5622	Mylar Washer (2 ea. Fastener)
-5	101381-*	PE Read PCBA
-6	101386-*	PE Write PCBA
-7	101811-*	Buffer Formatter PCBA
-8	101315-01	Front Panel
-9	102222-01	Bezel, Switch
-10	663-3010	Fuse (F1, F3), 1A, 3AG, Fast Blow
-11	663-3100	Fuse (F2), 10A, 3AG, Fast Blow
-12	663-3520	Fuse (F4), 2A, 3AG, Slow Blow

*See version table for applications and tape speeds.

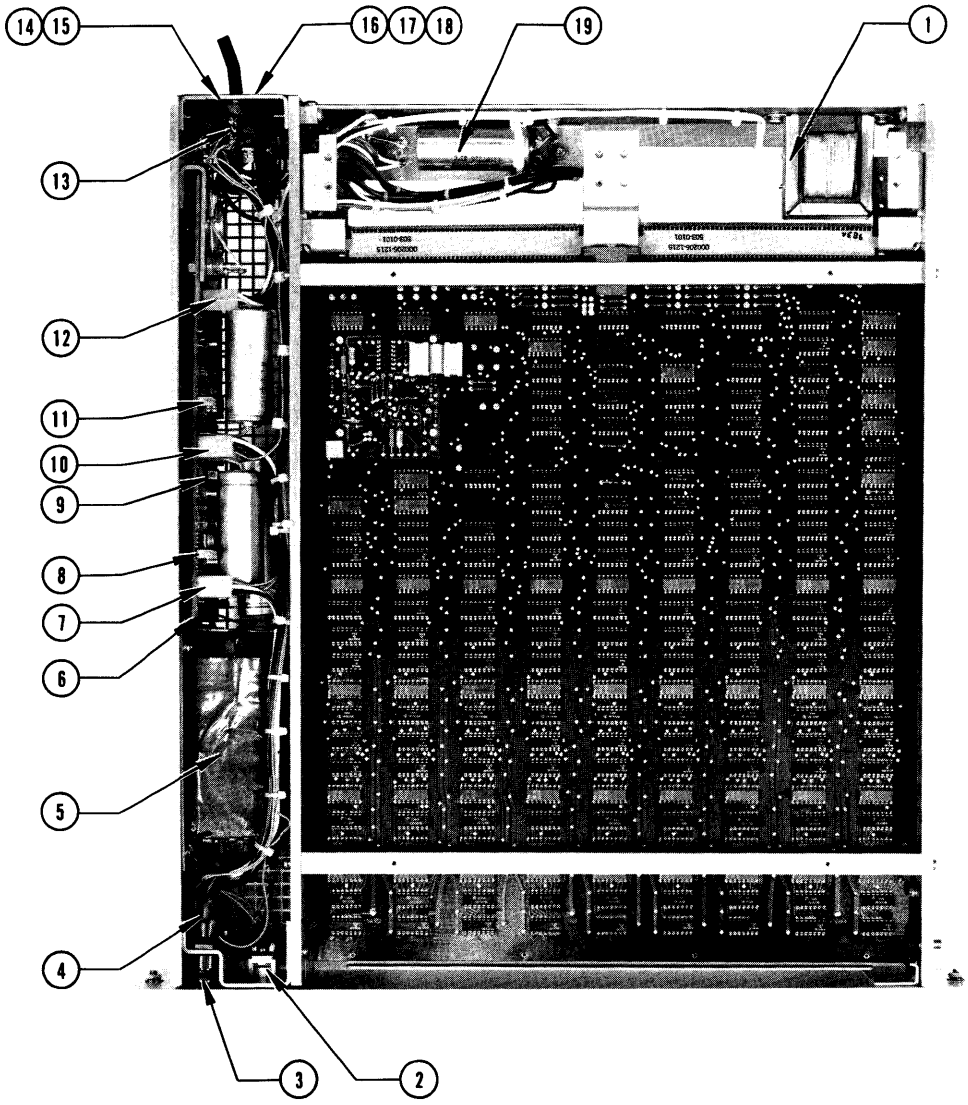


Figure 7-2. Buffered Formatter Photo Parts Index

Table 7-2
Buffered PE Formatter Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-2		
-1	515-0750	Power Inductor
-2	506-0808	Rocker Switch
-3	658-2038	Fuse Holder
-4	669-0080	Fuse Holder, Shrink Boot
-5	511-0003	Power Transformer
-6	103305-01	Power Supply PCBA
-7	*	Receptacle J2
-8	*	Variable Resistor R17
-9	*	Variable Resistor R33
-10	*	Receptacle J1 (Upper) J3 (Lower)
-11	*	Variable Resistor R3
-12	*	Receptacle J5 (upper) J4 (Lower)
-13	320-9802	Rectifier Bridge
-14	692-0001	Power Cable (3-conductor)
-15	660-0011	Strain Relief Bushing
-16	663-3520	Fuse, 2A, 3AG, Slow Blow
-17	658-2038	Fuse Holder
-18	669-0080	Fuse Holder Shrink Boot
-19	134-2600	Capacitor (2600 μf, 40v dc)

*Identification Only.

Table 7-3
Spare Parts List

Item	Part No.
1. PE Read PCBA	101381-*
2. PE Write PCBA	101386-*
3. Buffer Formatter PCBA	101811-*
4. Interconnect C PCBA	103311-01
5. Fixed Oscillator PCBA	
6.25 ips	102096-01
12.5 ips	102096-03
18.75, 22.5, 25 ips	102096-05
37.5 ips	102096-07
45.0 ips	102096-08
75.0 ips	102096-09
6. Tracking Oscillator PCBA	
6.25 ips	102094-06
12.5 ips	102094-04
18.75 ips	102094-03
22.5 ips	102094-09
25.0 ips	102094-02
37.5 ips	102094-01
45.0 ips	102094-07
75.0 ips	102094-08
7. Dual Speed Fixed Oscillator PCBA	
18.75/22.5/25.0/37.5 ips	101995-07
8. Dual Speed Tracking Oscillator PCBA	
6.25/12.5 ips	101990-01
12.5/25.0 ips	101990-02
18.75/37.5 ips	101990-03
22.5/45.0 ips	101990-04
37.5/75.0 ips	101990-05
9. Power Supply PCBA	103305-01
10. Power Supply Assembly	103314-01
11. ON/OFF Rocker Switch	506-0808
12. Incandescent Lamp, Slide Base, 6v	659-0003
13. Fuse, 1A, 3AG, FB (2 req'd)	663-3010
14. Fuse, 10A, 3AG, FB	663-3100
15. Fuse, 2A, 3AG, SB	663-3520
16. Extender Board	101595-01
17. Interface Board C PCBA	102546-01

*See version table for applications and tape speeds.

Table 7-4
Part Number Cross Reference

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Composition Resistors		
100-1015	QPL	RC07GF100J (1/4w, ±5%, 10 ohms)
100-1025	QPL	RC07GF102J (1/4w, ±5%, 1K ohms)
100-1035	QPL	RC07GF103J (1/4w, ±5%, 10K ohms)
100-1045	QPL	RC07GF104J (1/4w, ±5%, 100K ohms)
100-1215	QPL	RC07GF121J (1/4w, ±5%, 120 ohms)
100-1245	QPL	RC07GF124J (1/4w, ±5%, 120K ohms)
100-1505	QPL	RC07GF150J (1/4w, ±5%, 15 ohms)
100-1515	QPL	RC07GF151J (1/4w, ±5%, 150 ohms)
100-1835	QPL	RC07GF183J (1/4w, ±5%, 18K ohms)
100-2205	QPL	RC07GF220J (1/4w, ±5%, 22 ohms)
100-3305	QPL	RC07GF330J (1/4w, ±5%, 33 ohms)
100-4715	QPL	RC07GF470J (1/4w, ±5%, 470 ohms)
100-4735	QPL	RC07GF473J (1/4w, ±5%, 47K ohms)
100-5605	QPL	RC07GF560J (1/4w, ±5%, 56 ohms)
100-5625	QPL	RC07GF562J (1/4w, ±5%, 5.6K ohms)
100-5635	QPL	RC07GF563J (1/4w, ±5%, 56K ohms)
100-6805	QPL	RC07GF680J (1/4w, ±5%, 68 ohms)
100-6815	QPL	RC07GF681J (1/4w, ±5%, 680 ohms)
100-6825	QPL	RC07GF682J (1/4w, ±5%, 6800 ohms)
100-8205	QPL	RC07GF820J (1/4w, ±5%, 82 ohms)
101-1005	QPL	RC20GF100J (1/2w, ±5%, 10 ohms)
101-1025	QPL	RC20GF102J (1/2w, ±5%, 1K ohms)
101-1825	QPL	RC20GF182J (1/2w, ±5%, 1.8K ohms)
101-2215	QPL	RC20GF221J (1/2w, ±5%, 220 ohms)
101-2705	QPL	RC20GF270J (1/2w, ±5%, 27 ohms)
102-3315	QPL	RC32GF331J (1w, ±5%, 330 ohms)
102-6815	QPL	RC32GF681J (1w, ±5%, 680 ohms)
103-1515	QPL	RC42GF151J (2w, ±5%, 100 ohms)
103-4715	QPL	RC42GF471J (2w, ±5%, 470 ohms)
Precision Film Resistors		
104-1100	QPL	RN60D1101F (1/4w, ±1%, 1.1K ohms)
104-2610	QPL	RN60D2610F (1/4w, ±1%, 261 ohms)
104-5110	QPL	RN60D5110F (1/4w, ±1%, 511 ohms)
Wire Wound Resistors, Chassis Mounted		
110-0011	Dale Electronics	RS-10 (10w, ±3%, 0.1 ohm)
Wire Wound Resistors, Axial Leads		
114-0271	IRC	IRC AS-2 (2w, ±1%, 2.7 ohms)
Resistor Network, Microcircuit		
120-0001	Dale Electronics	TKR-152, Resistor Module, 14-pin, (DIP)

Table 7-4
Part Number Cross Referene (cont'd)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Variable Resistors		
121-1020	Beckman/Helipot	79PR1K (3/4w, ±10%, 1K ohms)
Dipped Mica Capacitors		
130-2205	QPL	DM-15-220J (22 pf, ±5%, 500v dc)
130-4715	QPL	DM-15-471J (470 pf, ±5%, 500v dc)
Mylar Film Capacitors		
131-1020	Callins	424B102K (0.001 μf, 100v dc, ±10%)
131-1030	Callins	424B103K (0.01 μf, 100v dc, ±10%)
131-1040	Callins	424B104K (0.1 μf, 100v dc, ±10%)
131-2230	Callins	424B223K (0.022 μf, 100v dc, ±10%)
131-3320	Callins	424B332K (0.0033 μf, 100v dc, ±10%)
Solid Tantalum Polarized Capacitors		
132-2262	Components	EG06-226-20 (22 μf, ±20%, 6v dc)
132-2752	Components	EG35-275-10 (2.7 μf, ±10%, 35v dc)
Aluminum Foil Polarized Capacitors		
133-7060	Mallory	MTA70E20 (70 μf, 20v dc, —10 +100%)
Aluminum Electrolytic Fixed Polarized Capacitors		
134-1230	Mallory	TCG123U015N3L3P (12,000 μf, 15v dc)
134-2403	Mallory	TCG242U030L2L3P (2400 μf, —10 +75%, 30v dc)
134-3000	Sprague	39D308GO15JL4
134-3303	Sprague	601D338GOJT4 (3300 μf, —10 +75%, 30v)
134-8000	G. E.	86F (8000 μf, —10 +75%, 25v dc)
Tantalum Capacitors		
139-1055	Kemet	T310A104K035AS (0.1 μf, 35v)
Transistors		
200-3053	RCA	2N3053 (NPN Silicon Annular T05)
200-3055	RCA	2N3055 (NPN Silicon Power T03)
200-3771	Motorola	SJ5254 (NPN High-power Silicon T03)
200-4037	RCA	2N4037 (PNP High-power Silicon T05)
200-4123	Motorola	2N4123 (NPN Silicon T092)
200-4125	Motorola	2N4125 (PNP Silicon T092)
200-5321	RCA	2N5321 (NPN High-power Silicon T05)
200-5323	RCA	2N5323 (PNP High-power Silicon T05)
Silicon Controlled Rectifier		
201-3228	RCA	2N3228 (T066)
201-4654	RCA	40654 (T05)

Table 7-4
Part Number Cross Reference (cont'd)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Diodes		
300-3889	Motorola	1N3889 (20A, 50V, D05)
300-4002	Motorola	1N4002 (1A, 100v, D041)
300-4446	Components, Inc.	1N4446 (Planer Silicon Switching)
Bridge Rectifiers		
320-9802	Motorola	MDA980-2 (10A, 100v)
Zener Diodes		
330-0395	Motorola	1N4730A (3.9v, ±5%, 1w)
330-0685	Motorola	1N4736A (6.8v, ±5%, 1w)
331-0335	Motorola	1N5226B (3.3v, ±5%, 500 mw)
331-1905	Motorola	1N5249B (19.0v, ±5%, 500 mw)
Linear Integrated Circuits		
400-2741	T. I.	SN72741P (Op-Amp, 8-pin, Internal Compensation)
Sockets		
503-7541	AMP, Inc.	583529-1 (16-pin, IC, solder terminal)
503-7544	AMP, Inc.	583527-1 (14-pin, IC, solder terminal)
503-7613	AMP, Inc.	1-380852-0 (16-pin, IC, wire wrap)
503-8358	AMP, Inc.	1-380845-0 (14-pin, IC, wire wrap)
Switches, Card Mounted		
514-8715	Spectrol	87-11-15 (Rotary, Single Pole, 5-position)
Crystal		
524-1202	PERTEC Specification No. 102545	12.00 MHz, ±0.01%
Integrated Circuits		
700-0001	T. I.	SN74H76N (Dual J-K Master-Slave FF)
700-0002	T. I.	SN74H04N (Hex Inverters)
700-0003	T. I.	SN74H00N (Quad, 2-Input, Positive NAND Gates)
700-1103	Micro Electronics	C1103 (1024-bit Dynamic Memory (RAM) 18-pin DIP Ceramic)
700-3207	Signetics	N3207I (Schottky Bi-Polar 3207A Quad Bi-Polar to MOS Level Shifter and Driver)
700-4110	T. I.	SN74H11A (Triple 3-Input Positive AND Gate)
700-4151	T. I.	SN74151N (8-line-to-1-line Data Selector/Multiplexor)
700-4153	T. I.	SN74153N (Dual 4-to-1-line Data Selector)
700-4155	T. I.	SN74155N (Dual 2-line-to-4-line Decoders/ Demultiplexers)
700-4157	T. I.	SN74157N (Quad 2-to-1-line Data Selector (Non-Invert))
700-4158	T. I.	SN74158N (Quad 2-to-1-line Data Selector Invert)
700-4161	T. I.	SN7416N (Synchronous 4-bit Binary Counter)
700-4175	T. I.	SN74175N (Quad D-type FF with Direct Clear)
700-4180	T. I.	SN74180N (8-bit Odd/Even Parity Generator/Checker)
700-5107	T. I.	SN75107N (Dual Line Receiver)

Table 7-4
Part Number Cross Reference (cont'd)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Integrated Circuits (Con't)		
700-7400	T. I.	SN7400N (Quad 2-Input Positive NAND Gate)
700-7402	T. I.	SN7402N (Quad 2-Input Positive NOR Gate)
700-7404	T. I.	SN7404N (Hex Inverter)
700-7410	T. I.	SN7410N (3-Input Positive NAND Gate)
700-7416	T. I.	SN7416N (Hex Inverter Buffer with Open Collector High Voltage Output)
700-7419	T. I.	SN74193N (4-Bit U/D Synchronous Binary Counter
700-7430	T. I.	SN7430N (8-input Positive NAND Gate)
700-7438	T. I.	SN7438N (Quad 2-Input Positive NAND Buffers (Open Collectors)
700-7440	T. I.	SN7440N (Dual 4-Input Positive NAND Buffer)
700-7450	T. I.	SN7450N (Expandable Dual 2-wide, 2-input, AND-OR-INVERT Gate)
700-7474	T. I.	SN7474N (Dual D-Type Edge Triggered FF)
700-7476	T. I.	SN7476N (Dual J-K Master-Slave FF)
700-7485	T. I.	SN7485N (4-bit-to-4-bit Magnitude Comparator)
700-7486	T. I.	SN7485N (Quad 2-Input EXCLUSIVE-OR Gate)
700-7493	T. I.	SN7493N (4-bit Binary Counter)
700-7495	T. I.	SN7495N (4-bit Right-Shift/Left Shift Register)
700-7496	T. I.	SN7496N (5-bit Shift Register)
700-8360	T. I.	SN15836N (Hex Inverter)
700-8440	T. I.	SN15844N (Expandable Dual 4-Input NAND Power Gate)

*Or equivalent.

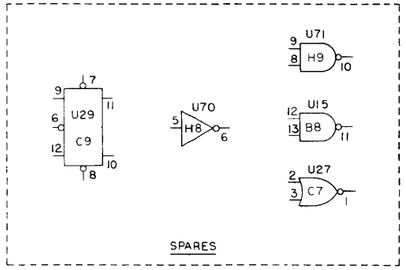
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BC	11/71	[illegible]		[illegible]
B	ECN 2599	5/72	[illegible]	[illegible]	[illegible]
C	ECN 2651	8/72	[illegible]	[illegible]	[illegible]
D	ECN 3037A	10/72	[illegible]	[illegible]	[illegible]
E	ECN 5017	4-3-73	CJ	[illegible]	[illegible]
E1	ECN 5097	5-9-73	CW	[illegible]	[illegible]

VERSION TABLE (7)

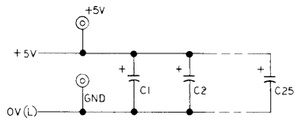
DASH NO	U19,20,31,32,41-44, U54-57,59-61,63, U65-67,70-73	R1-48	R51-68	W1,2	DESCRIPTION
-01	USE	USE	USE	OMIT	NORMAL
-02	USE	OMIT	USE	OMIT	OMIT CONTROLLER INTERFACE TERMINATOR
-03	USE	OMIT	OMIT	OMIT	OMIT CONTROLLER AND TRANSPORT INTERFACE TERMINATORS

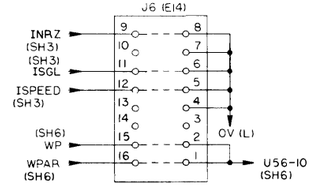
GROUND AND POWER PIN NUMBERS

INTEGRATED CIRCUITS	GND	+5V
700-7400, 7402, 7404, 7416, 7420, 7440, 7450, 74180, 8440	7	14
700-7476	13	5
700-7493	10	5

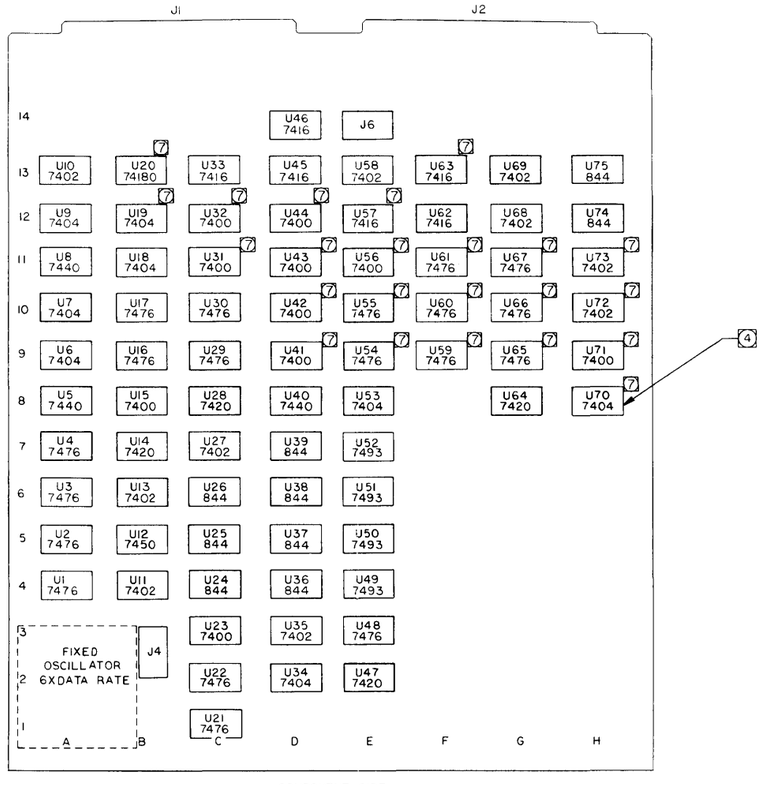


SPARES



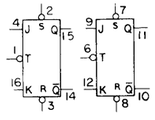


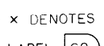
JUMPER PLATFORM
SEE ASSY DWG NO 102100, 102101, 102102 & 102103.



COMPONENT SIDE

REFERENCE DESIGNATION	
LAST USED	DELETED
R74	
C26	
U75	
TP109	
TP209	
TP21	



8. ALL FLIP FLOPS USED FUNCTIONALY AS FOLLOWS:
(7) SEE VERSION TABLE FOR USAGE.
6.  X DENOTES OPEN COLLECTOR OUTPUT.
5. INTERNAL LABEL (C2) DENOTES COORDINATE LOCATION ON ASSY.
(4) ALL INTEGRATED CIRCUITS ARE PEC PART NO. PREFIX 700-.
3. ALL CAPACITORS ARE 2.7UF, 100V, 10%.
2. ALL RESISTORS ARE 1/4W, 5%, VALUES ARE IN OHMS.
1. REFERENCE DRAWINGS: ASSEMBLY-101386
SPECIFICATION -101389

NOTES: UNLESS OTHERWISE SPECIFIED:

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR
.XXX ± .005 ± ½°
FRACTIONS ± 1/32
BREAK ALL SHARP CORNERS
APPROX. 010

THE INFORMATION HEREON IS THE PROPRIETARY PROPERTY OF PEC AND IS COPYRIGHTED. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE

SIGNATURES	DATE
DR [illegible]	11/71
CHK [illegible]	[illegible]
DES	
ENGR [illegible]	12-1-71
ENGR	

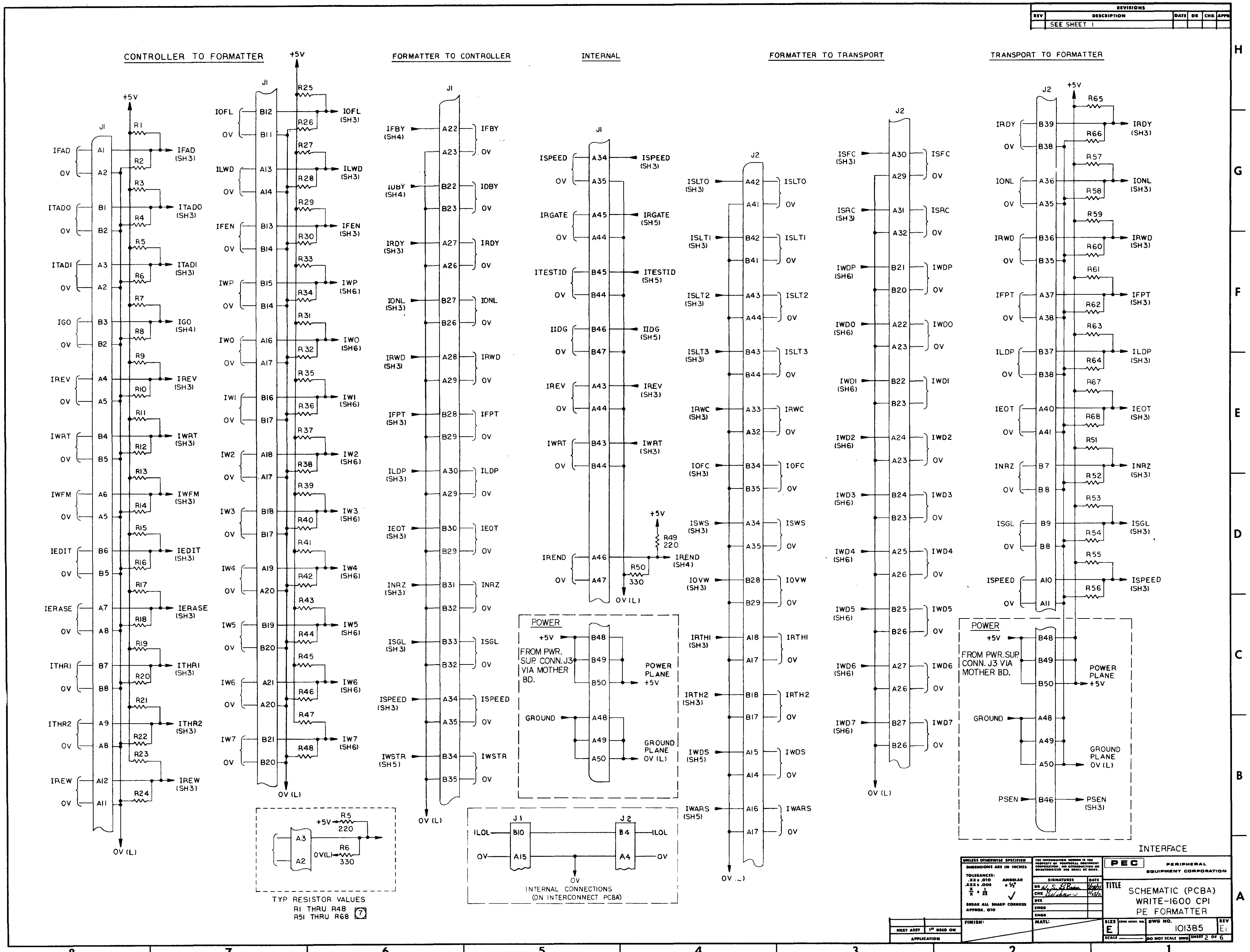
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) WRITE-1600 CPI PE FORMATTER

NEXT ASSY | 1ST USED ON | APPLICATION | FINISH: | MATL:

SIZE E | CODE IDENT. NO. | DWG NO. 101385 | REV E1

SCALE | DO NOT SCALE DWG | SHEET 1 OF 6


REVISIONS
SEE SHEET 1
CONTROLLER TO FORMATTER
FORMATTER TO CONTROLLER
INTERNAL
FORMATTER TO TRANSPORT
TRANSPORT TO FORMATTER
POWER
FROM PWR. SUP. CONN. J3 VIA MOTHER BD.
POWER PLANE +5V
GROUND PLANE OV (L)
INTERNAL CONNECTIONS (ON INTERCONNECT PCBA)
TYP RESISTOR VALUES
R1 THRU R48
R51 THRU R68
INTERFACE
PEC PERIPHERAL EQUIPMENT CORPORATION
TITLE SCHEMATIC (PCBA) WRITE-1600 CPI PE FORMATTER
SIZE E
DWG NO. 101385
REV E1
SHEET 2 OF 6

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

TRANSPORT STATUS

IFAD J1-A1 → U9 AI2 → SI → FSLT; OFF → OV (L)

FSLT, NFSLT → U8 AI1

ITADO J1-B1 → U10 AI3 → TADO → U9 AI2 → NTADO

ITADI J1-A3 → U10 AI3 → TADI → U9 AI2 → NTADI

IREW J1-A12 → U10 AI3 → REW

IOFL J1-B12 → U10 AI3 → OFL

TADO, NTADO → U75 HI3 → ISLT 0 J2-A42; U75 HI3 → ISLT 1 J2-B42

NTADO → U74 HI2 → ISLT 2 J2-A43

TADI, NTADI → U74 HI2 → ISLT 3 J2-B43

REW → U62 FI2 → IRWC J2-A33

OFL → U46 DI4 → IOFC J2-B34

PSEN J2-B46 → TP21; R74 82 OV (L)

IFEN J1-B13 → U9 AI2 → U5 A8 → (SH4) NRST

TP4; ILWD J1-A13 → U9 AI2 → LWD (SH5)

TP3 (SH4) RST

C26 .01 100V, 10% OV (L)

NNRZ

IRDY J2-B39 → U68 GI2 → U33 CI3 → IRDY J1-A27; RDY (SH4)

IONL J2-A36 → U69 GI3 → U33 CI3 → IONL J1-B27

IRWD J2-B36 → U69 GI3 → U45 DI3 → IRWD J1-A28

IFPT J2-A37 → U69 GI3 → U45 DI3 → IFPT J1-B28

ILDP J2-B37 → U69 GI3 → U45 DI3 → ILDP J1-A30; LDP (SH4)

IEOT J2-A40 → U68 GI2 → U33 CI3 → IEOT J1-B30; U53 EI8 → NLDP (SH4)

INRZ J2-B7; INRZ J6-9 (SH1) → U58 EI3 → U45 DI3 → INRZ J1-B31; U53 EI3

ISGL J2-B9; ISGL J6-1 (SH1) → U58 EI3 → U45 DI3 → ISGL J1-B33; SGL (SH4,5); U53 EI8 → NSGL (SH4)

ISPEED J2-A10; ISPEED J6-12 (SH1) → U58 EI3 → U45 DI3 → ISPEED J1-A34; SPEED (SH4)

TRANSPORT CONFIGURATION

COMMAND REGISTER

GOP (SH4)

IREV J1-A4 → U7 AI0 → U30 CI0 → REV (SH4); NREV (SH4)

NDCN5 (SH4) → U27 C7 → U33 CI3 → TP19 → ISFC J2-A30

U27 C7 → U62 FI2 → TP20 → ISRC J2-A31

IWRT J1-B4 → U7 AI0 → U30 CI0 → WRT (SH4,5); NWRT (SH4,5)

U62 FI2 → ISWS J2-A34

U46 DI4 → TP10 → IREV J1-A43

IWFM J1-A6 → U7 AI0 → U17 BI0 → WFM (SH4,5); NWFM (SH4)

U46 DI4 → TP9 → IWRT J1-B43

IEDIT J1-B6 → U6 A9 → U29 C9 → EDIT (SH4); NEDIT (SH4)

U62 FI2 → IOVW J2-B28

IERASE J1-A7 → U6 A9 → U16 B9 → NERASE (SH4,5)

ITHR1 J1-B7 → U6 A9 → U16 B9 → THR1 → U62 FI2 → IRTH1 J2-A18

ITHR2 J1-A9 → U18 BI1 → U17 BI0 → THR2 → U62 FI2 → IRTH2 J2-B18

NRST

INTERFACE CONTROL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: .XX ± .010 ANGULAR; .XXX ± .005 ± ½°; X/X ± 1/8; BREAK ALL SHARP CORNERS APPROX. 010	THE INFORMATION HEREIN IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.	SIGNATURES	DATE	PEC PERIPHERAL EQUIPMENT CORPORATION			
		DR WCS	7/1/80	TITLE SCHEMATIC (PCBA) WRITE-1600CPI PE FORMATTER			
		CHK					
		MFG					
		ENGR					
		ENGR					
NEXT ASSY	1ST USED ON	FINISH:	MATL:	SIZE E	CONT. NO.	DWG NO. 101385	REV
APPLICATION				SCALE —	DO NOT SCALE DWG	SHEET 3 OF 6	

8 7 6 5 4 3 2 1

H G F E D C B A

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

TP14
IREND
J1-A46
U53 E8
REND
GO2
NDCN5 (SH3,5)
TP2
IGO
J1-B3
U11 B4
(SH3) RDY
U15 B8
U8 A11
(SH3) GOP
NGO1
GO1
U1 A4
GO2
+5V
R73 4700
W1 (7)
OV (L)
U12 B5
U4 A7
DCN5 (SH5)
SP
NDCN6
U14 B7
U33 C13
TP5
IFBY
J1-A22
U27 C7
TP6
IDBY
J1-B22
DBY (SH5)
(SH3) RST
OV(L)
(SH5) NWCN7
(SH3) NSGL
U15 B8
WEND (SH5)
NERASE (SH3)
DCN5
NDCN5
CCLK
U53 E8
U11 B4
U2 A5
NLDP (SH3)
DCN1 (SH5)
NDCN1 (SH5)
U12 B5
DCN2
NDCN2
U3 A6
DCN3
(SH5) NDCN3
U13 B6
DCN4
NDCN4
(SH3) NRST
LDP (SH3)
DP
RST (SH3)
NWRT (SH3)
U13 B6
SWP (SH5)
NDP
+5V
R71 1000
R69 1000
R72 1000
R70 1000
J4
FIXED OSCILLATOR 6XDATA RATE
14
4
3
7
+5V
CLKS
(SH3) SPEED
OV (L)
CCTRO (SH5)
U21 C1
U22 C2
ODD
NODD (SH5)
NCCTRO
CCTRI
U15 B8
U40 D8
TP1
CCLK (SH5)
NCCLK (SH5)
U14 B7
TP16
WCLK (SH6)
WCN6 (SH5)
DCN1
(SH3) NWRT
DCTR12
DCTR10
U26 C6
(SH3) WRT
DCTR14
DCTR12
DCN3
(SH3) NWRT
(SH3) NREV
DCTR2
U25 C5
(SH3) WRT
DCTR8
DCN4
DCTR10
DCTR 9
U36 D4
(SH3) SGL
DCTR10
DCTR 9
DCTR8
U38 D6
DCN2
(SH3) NWRT
DCTR10
U39 D7
(SH3) NEDIT
DCTR8
U37 D5
(SH5)(WCNI+5)
DCTR 6
DCTR 3
DCTR2
(SH3) NSGL
DCTR10
DCTR8
DCTR6
(SH3) WFM
DCTR13
DCTR12
(SH3) EDIT
DCTR8
DCTR 7
DCTR6
(SH3) REV
U34 D2
DCN4
DCTR10
DCTR 9
U24 C4
(SH3) WRT
(SH3) NWFM
U23 C3
TP7
NDP (SH5)
(SH5) (WCNI+5)
NDCN1
NDCN2
NDCN3
NDCN4
U28 C8
U35 D3
U34 D2
DCNT
(SH5) DCTR1
DCTR2
DCTR3
DCTR4
DCTR5
DCTR6
DCTR7
DCTR8
DCTR9
DCTR10
DCTR11
DCTR12
DCTR13
DCTR14
DCTR15
DCTR16
CCLK
U23 C3
NDP
DCNT
E4
E5
E6
E7
U49
U50
U51
U52

CONTROL LOGIC

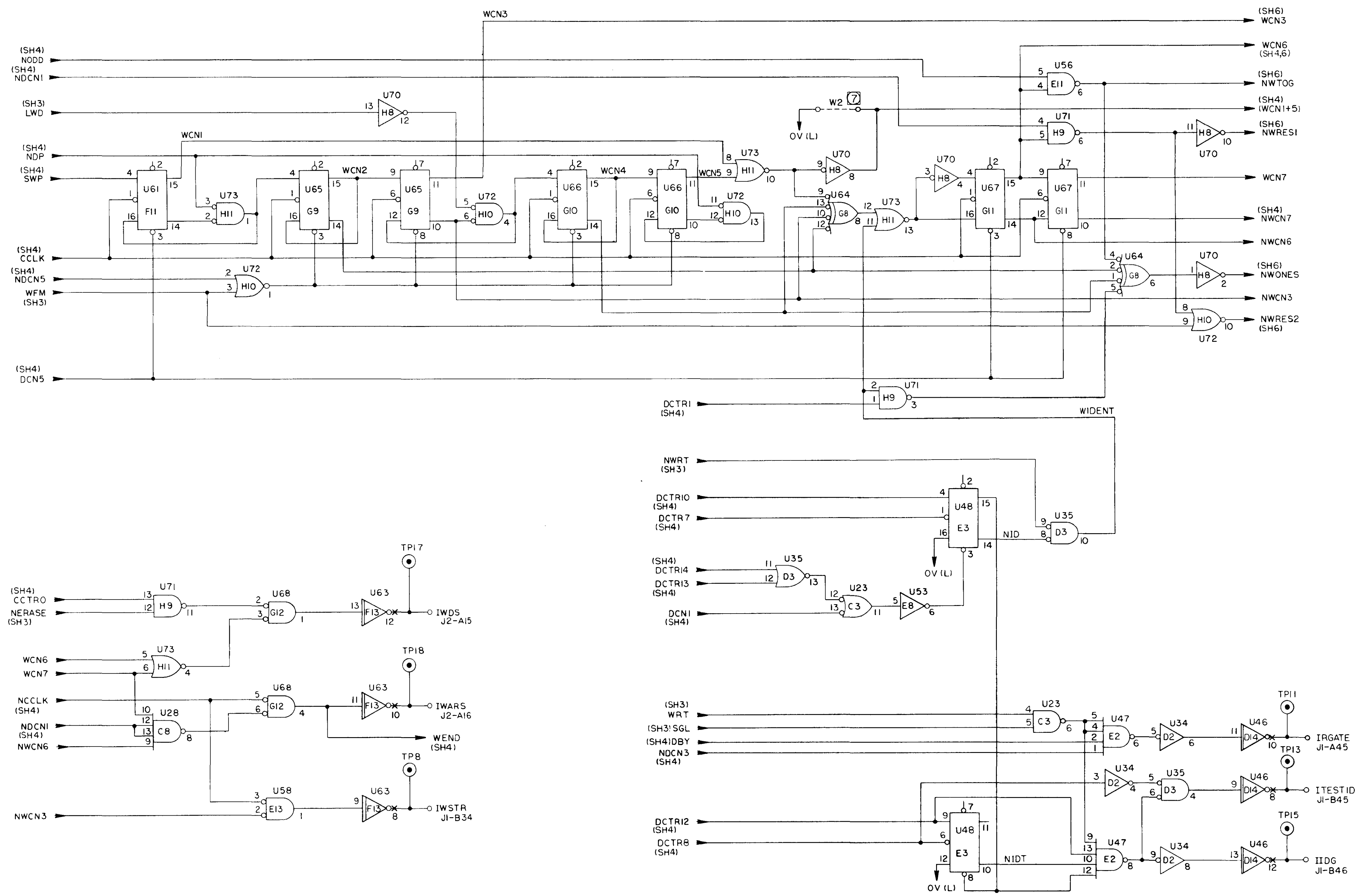
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
ANGULAR ± ½°
BREAK ALL SHARP CORNERS APPROX. .010
THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE
SIGNATURES / DATE
DR
CHK
DES
ENGR
ENGR
MATL:
FINISH:
NEXT ASSY | 1ST USED ON APPLICATION

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) WRITE-1600 CPI PE FORMATTER

SIZE E | CODE IDENT NO | DWG NO. 101385 | REV F
SCALE —— | DO NOT SCALE DWG | SHEET 4 OF 6

REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				



WRITE CONTROL

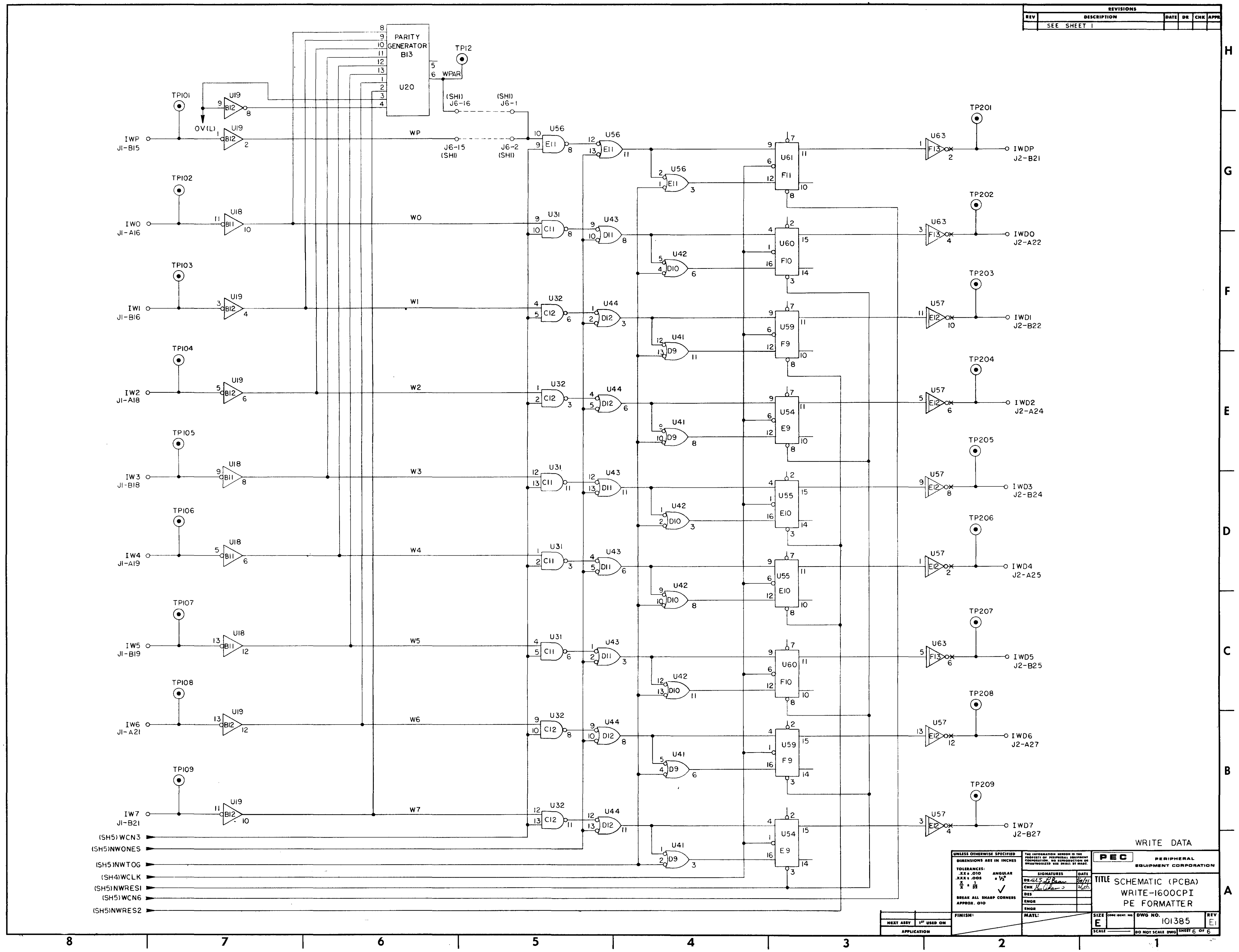
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) WRITE-1600 CPI PE FORMATTER

SIZE E DWG NO. 101385 REV E1

DO NOT SCALE DWG SHEET 5 OF 6


REVISIONS
REV DESCRIPTION DATE DR CHK APPR
SEE SHEET 1
PARITY GENERATOR B13
U20
TP12
WPAR
(SH1) J6-16
(SH1) J6-1
J6-15 (SH1)
J6-2 (SH1)
OV(L)
TP101
IWP J1-B15
WP
TP102
IW0 J1-A16
W0
TP103
IW1 J1-B16
W1
TP104
IW2 J1-A18
W2
TP105
IW3 J1-B18
W3
TP106
IW4 J1-A19
W4
TP107
IW5 J1-B19
W5
TP108
IW6 J1-A21
W6
TP109
IW7 J1-B21
W7
(SH5)WCN3
(SH5)NWONES
(SH5)NWTOG
(SH4)WCLK
(SH5)NWRES1
(SH5)WCN6
(SH5)NWRES2
TP201
IWDP J2-B21
TP202
IWD0 J2-A22
TP203
IWD1 J2-B22
TP204
IWD2 J2-A24
TP205
IWD3 J2-B24
TP206
IWD4 J2-A25
TP207
IWD5 J2-B25
TP208
IWD6 J2-A27
TP209
IWD7 J2-B27
WRITE DATA
PEC PERIPHERAL EQUIPMENT CORPORATION
TITLE SCHEMATIC (PCBA) WRITE-1600CPI PE FORMATTER
SIZE E
DWG NO. 101385
REV E1
SHEET 6 OF 6
DO NOT SCALE DWG
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
BREAK ALL SHARP CORNERS APPROX. .010
NEXT ASSY
1ST USED ON
APPLICATION
FINISH:
MATL:

REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 3-BC	7/23/71	W/B		
C	ECN 2635	10/30/71			
D	ECN 3105A	10/2/72	D.C		
E	ECN 4342	10/2/72	D.C		
E1	ECN 5103	4/25/73	C.W.		
E2	ECN 5097	5-9-73	C.W		
F	ECN 6091	3/13/74	S.C		
G	ECN 7257	4/2/75	CJ		

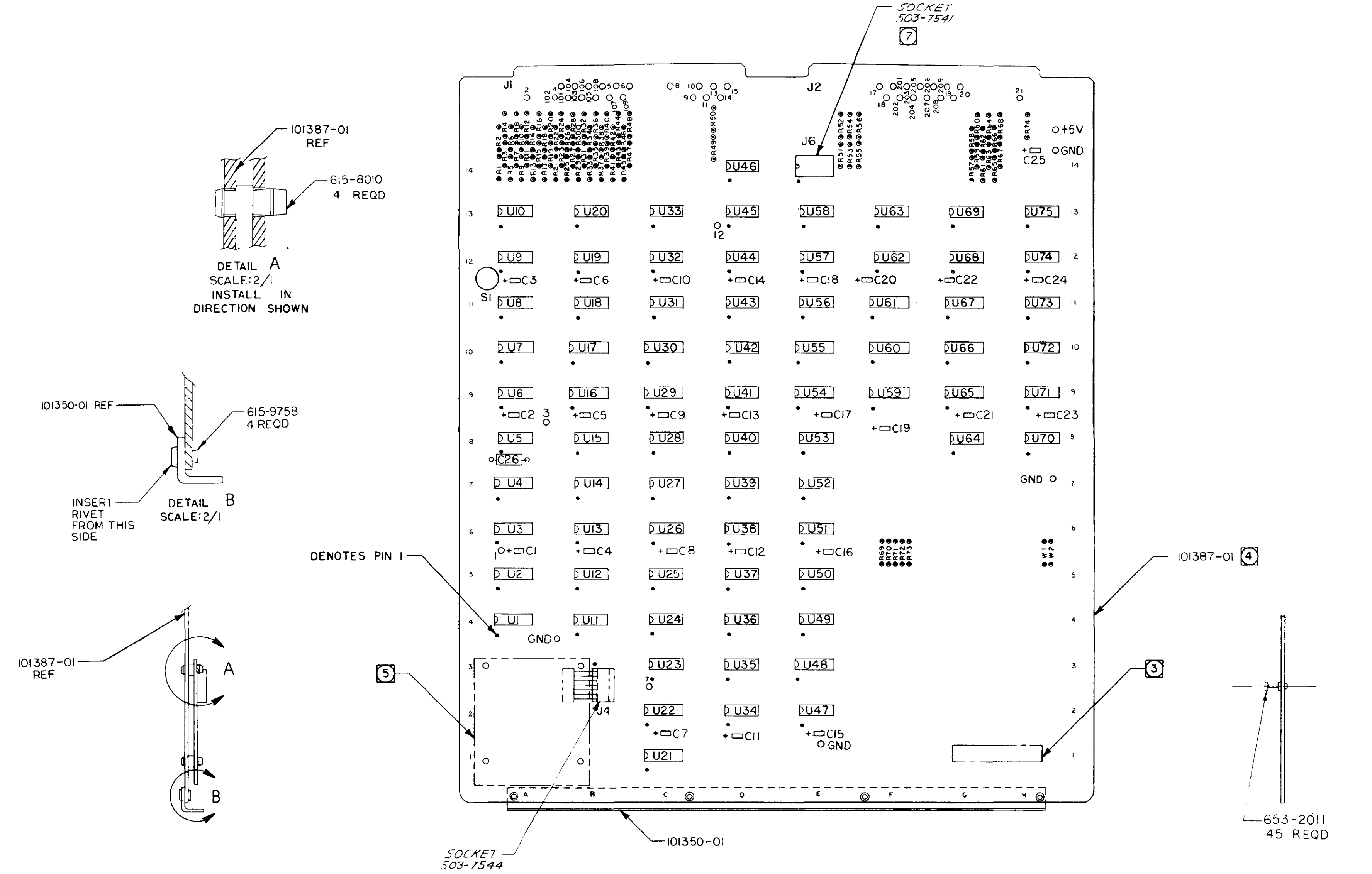


TABLE I

PART NUMBER	REFERENCE DESIGNATION
100-1025	R69-72
100-2215	R1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31, R33,35,37,39,41,43,45,47,49,51,53,55, R57,59,61,63,65,67
100-3315	R2,4,6,8,10,12,14,16,18,20,22,24,26,28, R30,32,34,36,38,40,42,44,46,48,50, R52,54,56,58,60,62,64,66,68
100-4725	R73
100-8205	R74
131-1030	C26
132-2752	C1-25
700-7400	U15,23,31,32,41,42,43,44,56,71
700-7402	U10,11,13,27,35,58,68,69,72,73
700-7404	U6,7,9,18,19,34,53,70
700-7416	U33,45,46,57,62,63
700-7420	U14,28,47,64
700-7440	U5,8,40
700-7450	U12
700-7476	U1,2,3,4,16,17,21,22,29,30,48,54,55,59, U60,61,65,66,67
700-7493	U49,50,51,52
700-4180	U20
700-8440	U24,25,26,36,37,38,39,74,75
100373-02	W1,2
514-8711	S1

TABLE II 6

VERSION	U19,20,31,32, U41-44,54-57, U59-61,63, U65-67,70-73	R1-48	R51-68	W1,2	REMARKS
-01	USED	USED	USED	NOT USED	NORMAL
-02	USED	NOT USED	USED	NOT USED	OMIT CONTROLLER INTERFACE TERMINATORS
-03	USED	NOT USED	NOT USED	NOT USED	OMIT CONTROLLER & TRANSPORT INTERFACE TERMINATORS

7 SEE TOP BILL FOR CORRECT VERSION OF 16 PIN DIP JUMPER PLATFORM.

6 FOR PARTS AFFECTED BY VERSION NO. SEE TABLE II.

5 SEE TOP BILL FOR CORRECT VERSION OF FIXED OSCILLATOR.

4 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101387-01 REV K AND SUBSEQUENT.

3 RUBBER STAMP ASSY PART NO INCLUDING VERSION NUMBER & VERSION ISSUE LTR.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC-101385 SPECIFICATION-101389.

NOTES: UNLESS OTHERWISE SPECIFIED.

PART NO 101386-01 REV G

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010 .XXX ± .005 X/X ± 1/32 ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR W.S. LeBaron	2/12/71
CHK	7/23/71
DES	
ENGR R. Johnson	2/24/71
ENGR	

TOP ASSY | NEXT ASSY | 1ST USED ON | APPLICATION

FINISH:

MATL:

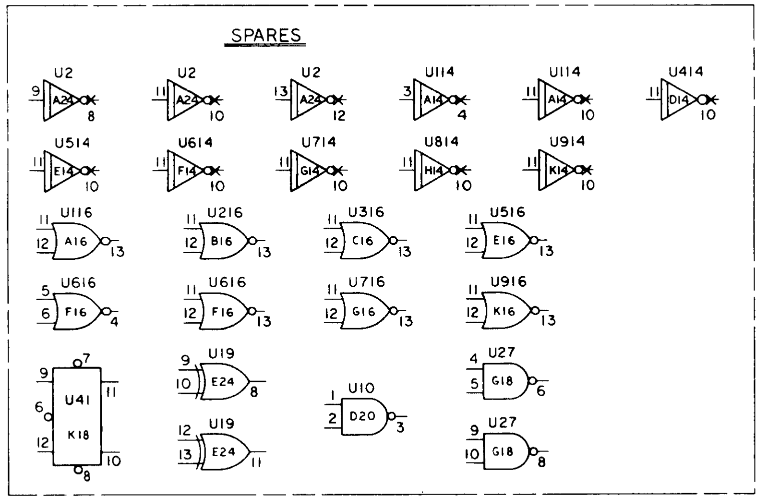
PEC PERIPHERAL EQUIPMENT CORPORATION

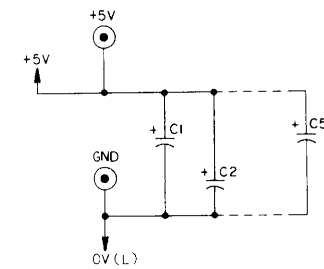
TITLE PCBA WRITE-1600 CPI PE FORMATTER

SIZE E | CODE IDENT. NO. | DWG NO. 101386 | REV G

SCALE FULL | DO NOT SCALE DWG | SHEET 1 OF 1

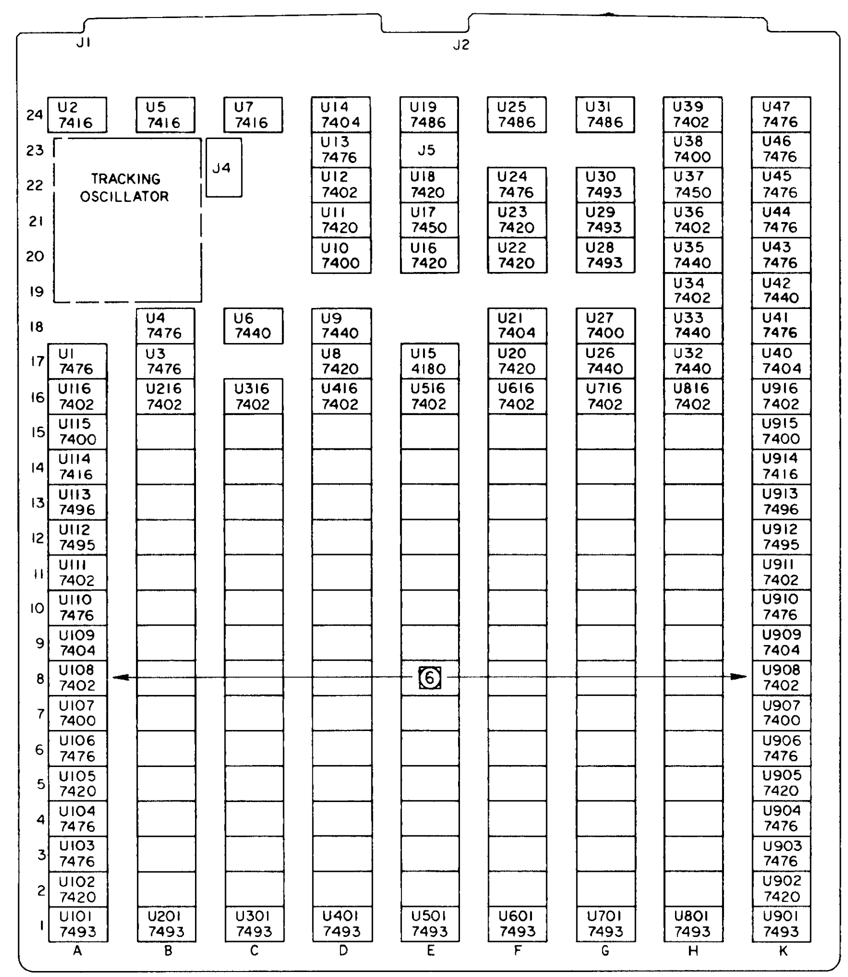
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-CA	3/15/71			K.J.
B	ECN 2640	5-21-71			
C	ECN 4079				
C1	ECN 8045		FFP		





GROUND AND POWER PIN NUMBERS

INTEGRATED CIRCUITS	GND	+5V
7400, 7402, 7404, 7416, 7420, 7440, 7450, 7486, 7495, 4180	7	14
7476	13	5
7493	10	5
7496	12	5



REFERENCE DESIGNATION		
LAST USED		DELETED
U47	U916	
R34		
C50		
TP14	TP209	

TABLE I

9	INTERNAL INTERFACE RESISTORS	TRANSPORT INTERFACE RESISTORS
VERSION	R1, R4 THRU R12	R15, R16, R18 THRU R33
-01	USE	USE
-02	USE	OMIT
-03	OMIT	USE

9. SEE VERSION TABLE FOR USAGE.

8. × DENOTES OPEN COLLECTOR OUTPUT.

7. INTERNAL LABEL (D16) DENOTES COORDINATE LOCATION ON ASSY.

6. CIRCUIT 100 IS TYPICAL OF CIRCUITS 200 THRU 900. CIRCUIT 100 IS CHANNEL P, LOCATION A1 THRU A16. CIRCUIT 200 IS CHANNEL O, LOCATION B1 THRU B16. CIRCUITS 300 THRU 900 ARE CHANNELS 1 THRU 7 RESPECTIVELY, LOCATION C1 THRU C16 ON THRU K1 THRU K16.

5. 3 DIGIT REFERENCE DESIGNATIONS ARE ASSIGNED TO REPETITIVE CIRCUITS. EX: U101 IS CIRCUIT 100. U901 IS CIRCUIT 900. SINGLE DIGIT REFERENCE DESIGNATIONS ARE ASSIGNED TO NON-REPETITIVE CIRCUITS. EX: U1, U2.

4. ALL INTEGRATED CIRCUITS ARE PEC PART NO. PREFIX 700-.

3. ALL RESISTORS ARE 1/4W, ±5%, VALUES ARE IN OHMS.

2. ALL CAPACITORS ARE 2.7UF, 35V, ±20%.

1. REFERENCE DRAWINGS: ASSEMBLY - 101381
   SPECIFICATION - 101384

NOTES: UNLESS OTHERWISE SPECIFIED:

101381	1600
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010, .XXX ± .005, X/X ± 1/32; ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

SIGNATURES		DATE
DR	L. G. Smith	
CHK		
DES		
ENGR		
ENGR		

MATL:

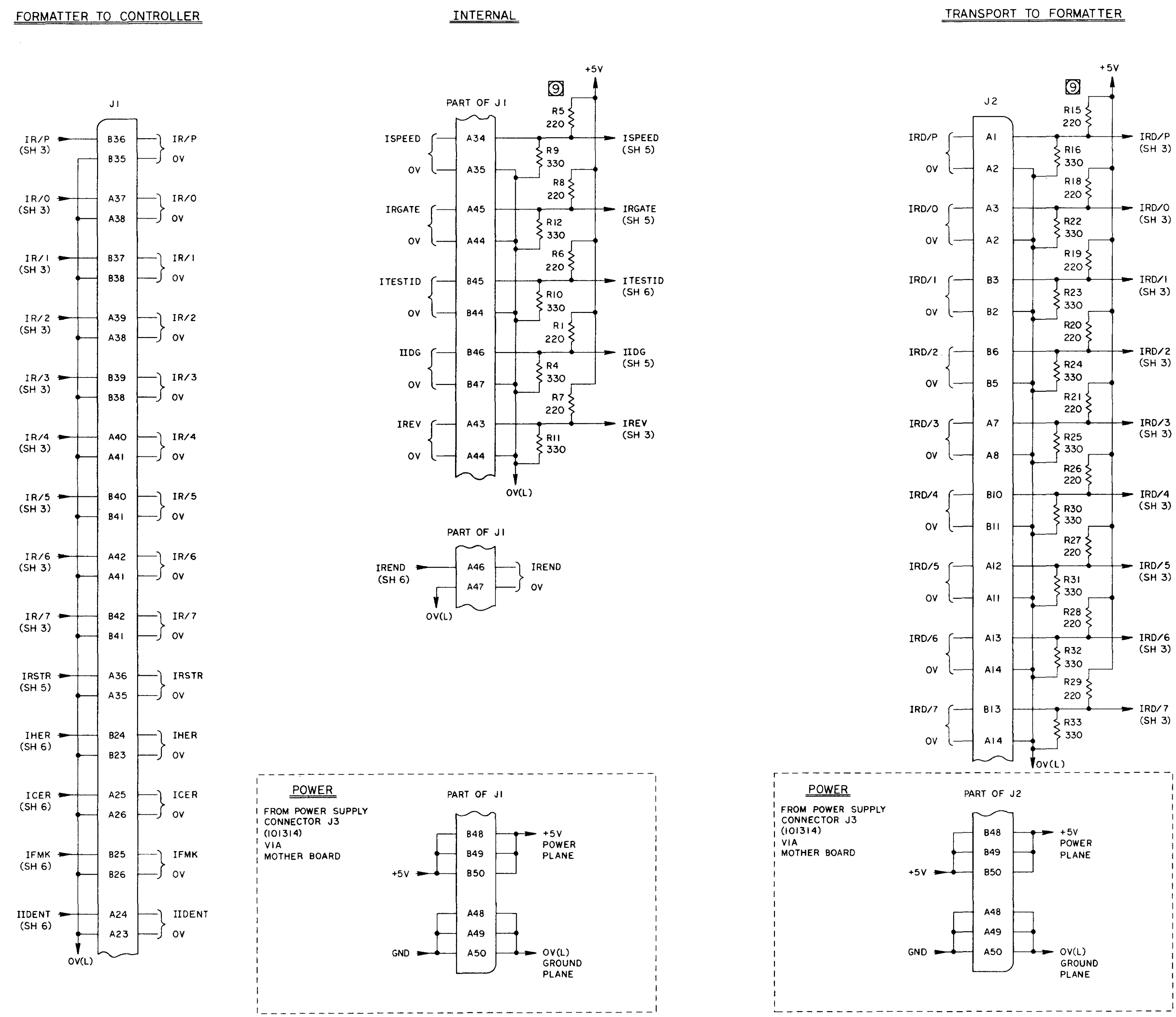
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) READ 1600 CPI PE FORMATTER

SIZE	CODE IDENT. NO.	DWG NO.	REV
E		101380	C1

SCALE — DO NOT SCALE DWG SHEET 1 OF 6

REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				



INTERFACE

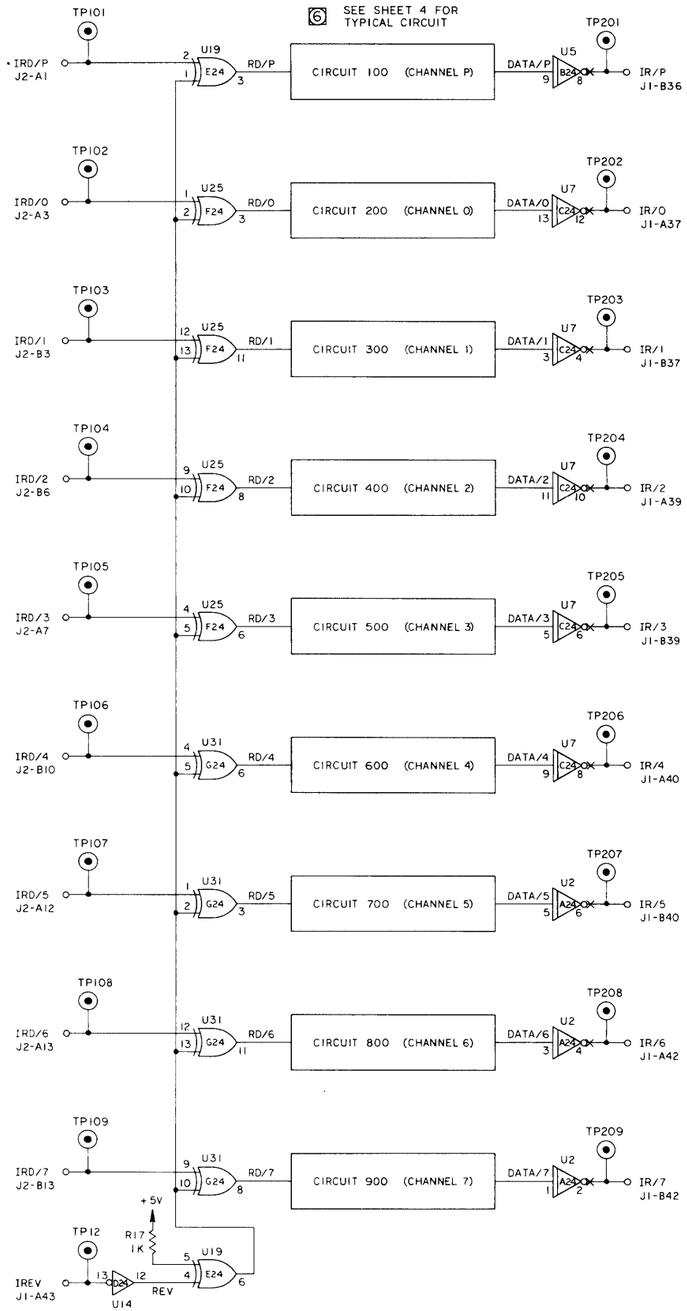
PEC PERIPHERAL EQUIPMENT CORPORATION

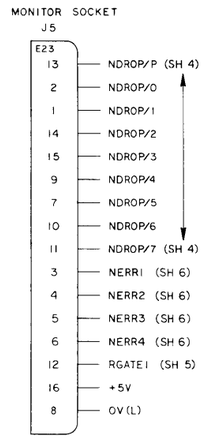
TITLE SCHEMATIC (PCBA) READ 1600 CPI PE FORMATTER

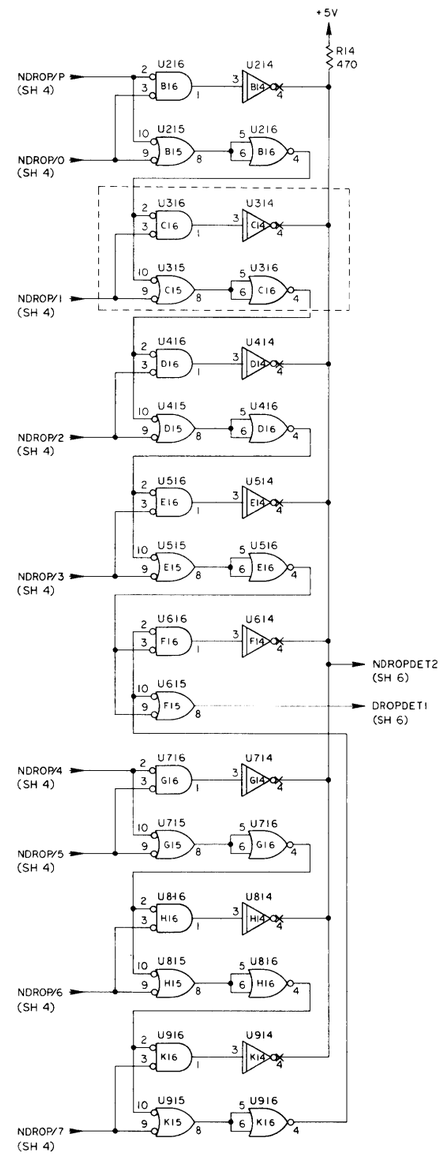
SIZE E | DWG NO. 101380 | REV C1

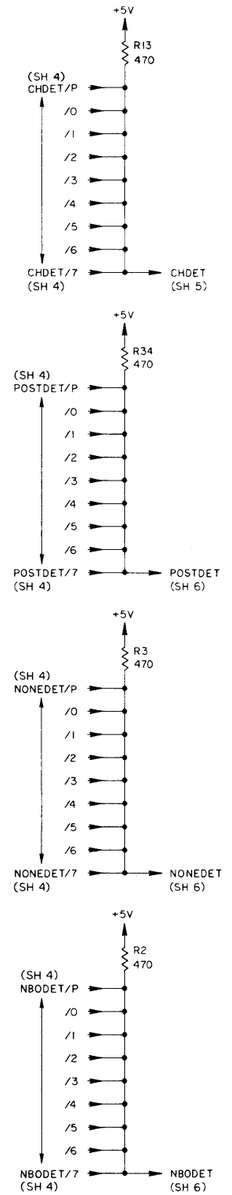
SHEET 2 OF 6

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				









COMBINED CHANNEL LOGIC

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .010, .XXX ± .005, ANGULAR ± ½°
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES		DATE
DR	[illegible]	7/8/75
CHK	[illegible]	7/8/75
DES		
ENGR		
ENGR		

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA)
READ 1600 CPI
PE FORMATTER

NEXT ASSY | 1ST USED ON | APPLICATION | FINISH: | MATL:

SIZE E | CONT IDENT NO. | DWG NO. 101380 | REV C!

SCALE — | DO NOT SCALE DWG | SHEET 3 OF 6

8 7 6 5 4 3 2 1

H G F E D C B A

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

PARC (SH 6)
PRESET (SH 6)
CIRCUIT 100 (6) (CHANNEL P)
SLCLK
SRCLK
SHL
NCOPYA (SH 5)
NRCLK (SH 5)
NECLK (SH 5)
CONTROL
U112 A12
OV(L)
U114
CHDET/P,0,1 THRU 7 (SH 3)
RD/P 0 1 THRU 7 (SH 3)
NLO (SH 5)
BUFFER
S4 S3 S2 S1 D1
SYNC
U113 A13
DA/P,0,1 THRU 7 (SH 3)
DATA/P,0,1 THRU 7 (SH 3)
PARC 5
POSTDET/P,0,1 THRU 7 (SH 3)
NONEDET/P,0,1 THRU 7 (SH 3)
NBODET/P,0,1 THRU 7 (SH 3)
NSYNC
DSTR·SYNC
RGATE1 (CHANNEL P,0 & 1)
RGATE2 (CHANNEL 2,3 & 4)
RGATE3 (CHANNEL 5,6 & 7) (SH 5)
REN2 (SH 6)
NDP
REN2
DGATE
NDGATE
DP
DROP
NDROP
DGATE/0 & 2 (CKT 200 & 400 ONLY) (SH 5)
NDROP/P,0,1 THRU 7 (SH 3)
J5 (SH 3)
RCLK1 (CHANNEL P)
RCLK2 (CHANNEL 0 & 1)
RCLK3 (CHANNEL 2 & 3)
RCLK4 (CHANNEL 4 & 5)
RCLK5 (CHANNEL 6 & 7) (SH 5)
DSTR
ENV
ENV/2 (SH 5)
ENV/P,0,2,5,6,7 (SH 6) (CKT 100,200, 400, 700, 800 & 900 ONLY)
NENV/0,2 (SH 5)
NENV/1,3,4 (SH 6) (CKT 200 THRU 600 ONLY)
REN1 (SH 6)

INDIVIDUAL CHANNEL LOGIC

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X ± 1/64
X ± 1/32 ✓
BREAK ALL SHARP CORNERS APPROX. 010

THE INFORMATION HEREON IS THE PROPRIETARY PROPERTY OF PEC. REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES	DATE
DR	
CHK	
DES	
ENGR	
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA)
READ 1600 CPI
PE FORMATTER

NEXT ASSY | 1ST USED ON | APPLICATION
FINISH: | MATL:
SIZE E | CODE IDENT. NO. | DWG NO. 101380 | REV C1
SCALE — | DO NOT SCALE DWG | SHEET 1 OF 6

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

TRACKING OSCILLATOR
J4
CLOCK
+5V
NER2
NER1
OV(L)
TP10
ISPEED J1-A34
U14 SPEED
RCLK6
(SH 4) DGATE/2
(SH 4) ENV/2
(SH 4) DGATE/0
NENV/2 (SH 4)
U17 E21
TRACKSIG
U116 A16
U115 A15
U1 A17
U3 B17
U4 B18
DATA2
TP1
ER1
ER2
U314 C14
U214 B14
U32 H17
U40 K17
NECLK (SH 4)
U6 C18
RCLK1 (CHANNEL P) (SH 4)
U9 D18
RCLK2 (CHANNEL 0 & 1) (SH 4)
RCLK3 (CHANNEL 2 & 3) (SH 4)
U33 H18
RCLK4 (CHANNEL 4 & 5) (SH 4)
RCLK5 (CHANNEL 6 & 7) (SH 4)
RCLK6 (CONTROL) (SH 6)
NRCLK (SH 4 & 6)
U26 G17
RGATE1 (CHANNEL P,0 & 1) (SH 3, 4 & 6)
RGATE2 (CHANNEL 2,3 & 4) (SH4 & 6)
(SH 4) RGATE3 (CHANNEL 5,6 & 7)
NRGATE (SH 6)
TP13
IRGATE J1-A45
U816 H16
RGATE
TP7
IIDG J1-B46
IDG
NIDG
U27 G18
NL0 (SH 4)
NRCN1 (SH 6)
NENV/0 (SH 4)
F17
U21 F18
NDATA
DATA1
(S/FE) (SH 6)
CHDET (SH 3)
U34 H19
CCN2
RCLK6
U46 K23
U47 K24
CCN1
U38 H23
NCOPYP
U39 H24
NCCN2
NCOPY
OV(L)
(RCN4·NRCN5) (SH 6)
COPY (SH 6)
U35 H20
NCOPYA (SH 4)
NRCLK
U34 H19
COPYCLK (SH 6)
RCTR9
(SH 6) RCN4
(SH 6) NRCN2
RCTR6
RCTR5
RCTR1
RCTR0
RCTR4
U34 H19
U23 F21
U22 F20
U24 F22
TP14
RP (SH 6)
NRP (SH 6)
RP
RCTR0 RCTR1 RCTR2 RCTR3
RCTR4 RCTR5 RCTR6 RCTR7
RCTR8 RCTR9 RCTR10 RCTR11
U28 G20
U29 G21
U30 G22
NRCN1
NDATA
U17 E21
U18 E22
NRP
RCN7 (SH 6)
(SH 6) NRCN7
(S/RCN7) (SH 6)
U38 H23
RSTR (SH 6)
TP6
U34 H19
U5 B20
RSTR
IRSTR J1-A36
NCCN2 (SH 6)
NDATA (SH 6)
DATA1 (SH 6)

READ CONTROL LOGIC

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
X.X ± .010
XXX ± .005
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES	DATE
DR	7/1/81
CHK	7/1/81
DES	
ENGR	
ENGR	
MATL:	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA)
READ 1600 CPI
PE FORMATTER

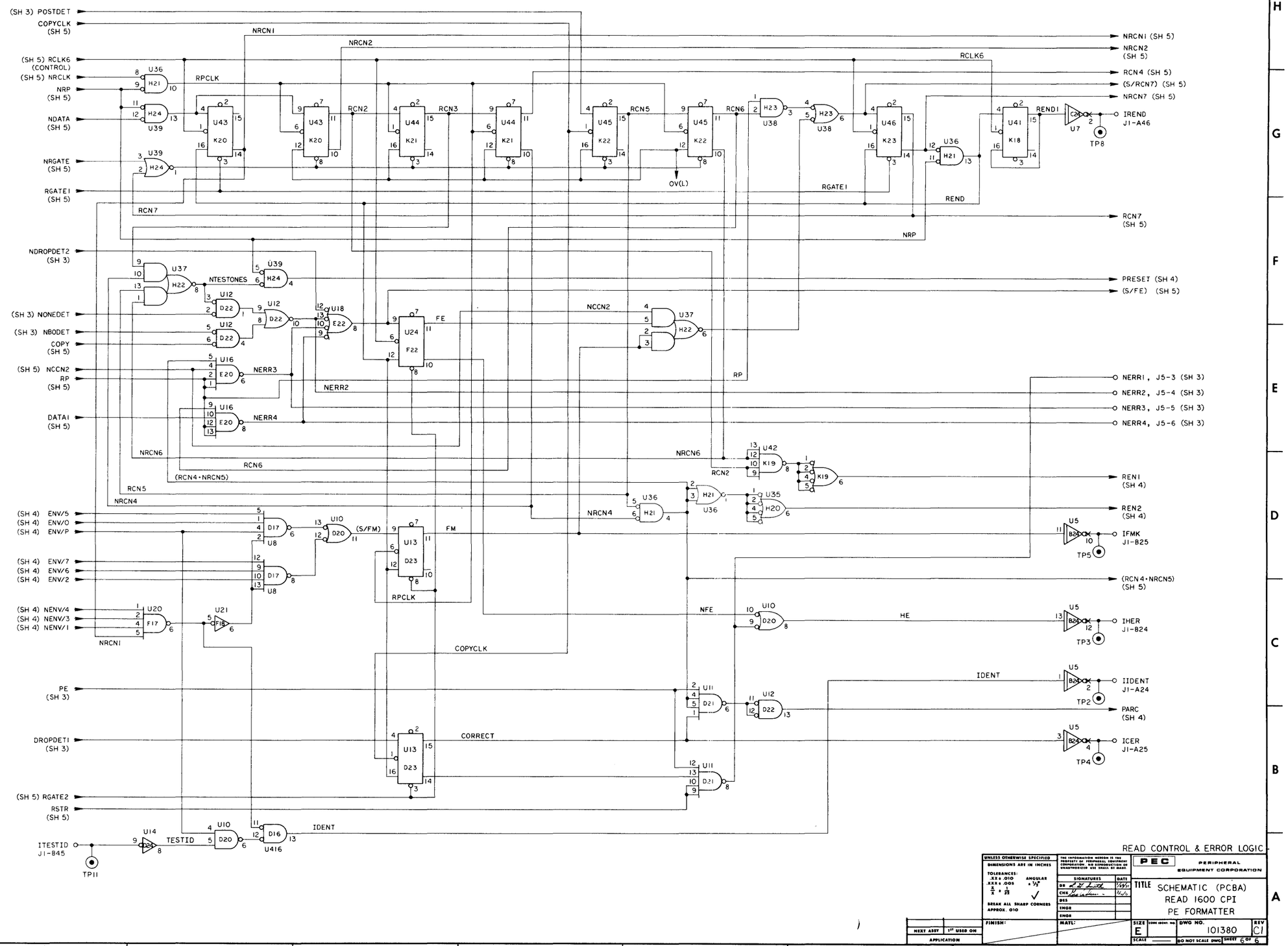
NEXT ASSY | 1ST USED ON | APPLICATION | FINISH:

SIZE E | DWG NO. 101380 | REV C1
SCALE — | DO NOT SCALE DWG | SHEET 5 OF 6

H G F E D C B A

8 7 6 5 4 3 2 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				



READ CONTROL & ERROR LOGIC

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

THE INFORMATION HEREON IS THE PROPRIETARY PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES	DATE
DR	1/19/71
CHK	4/1/71
QUA	
ENGR	
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

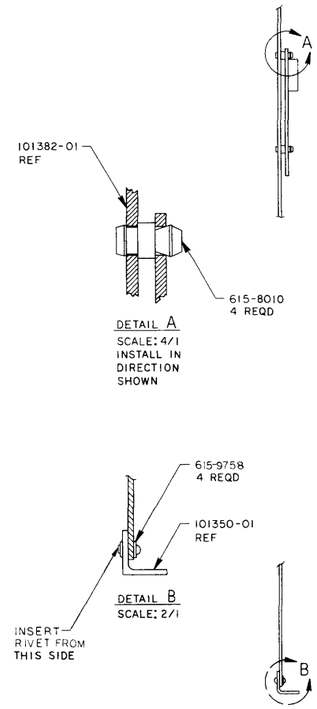
TITLE SCHEMATIC (PCBA)
READ 1600 CPI
PE FORMATTER

NEXT ASSY | 1ST USED ON
APPLICATION

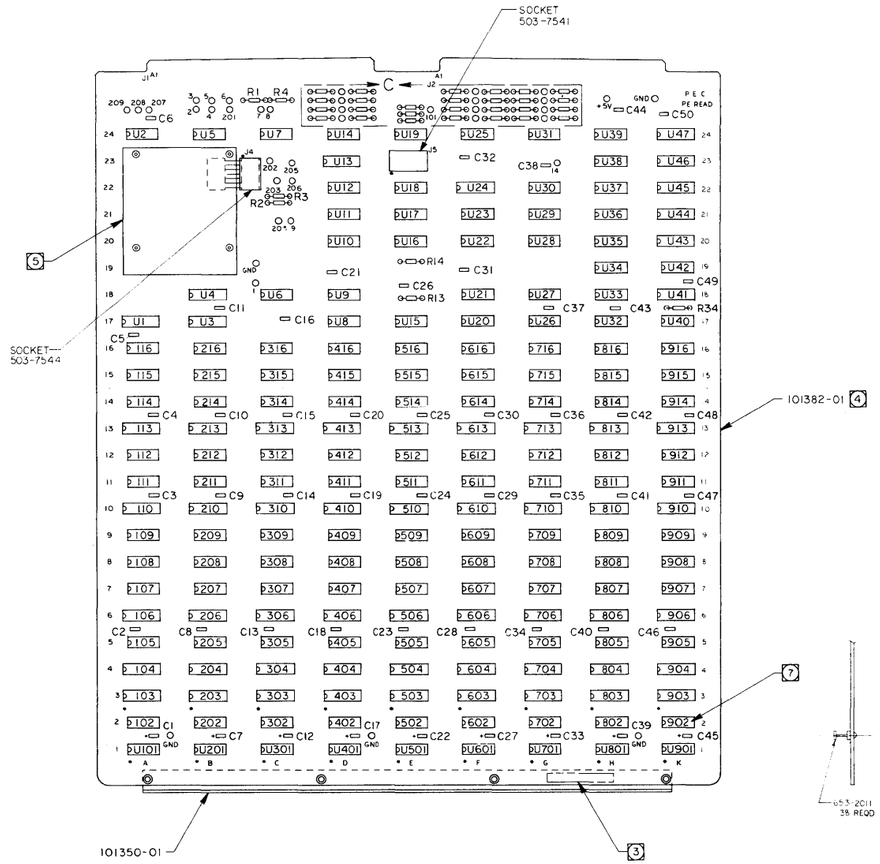
FINISH:
MATL:

SIZE E | CODE IDENT. NO. | DWG NO. 101380 | REV C1
SCALE — | DO NOT SCALE DWG | SHEET 6 OF 6

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 3-CA	3/25/71	[illegible]	[illegible]	[illegible]
C	ECN 2496	3/31/71	[illegible]	[illegible]	[illegible]
D	ECN 2558A	9/7/71	[illegible]	[illegible]	[illegible]
E	ECN 2539	9/7/71	[illegible]	[illegible]	[illegible]
F	ECN 2635	9/30/72	[illegible]	[illegible]	[illegible]
G	ECN 3105A	9/10/73	[illegible]	[illegible]	[illegible]
G1	ECN 3103	9/21/73	[illegible]	[illegible]	[illegible]
H	ECN 6091	3/14/74	[illegible]	[illegible]	[illegible]



DETAIL A
SCALE: 4/1
INSTALL IN
DIRECTION
SHOWN



DETAIL C
SCALE: 2/1

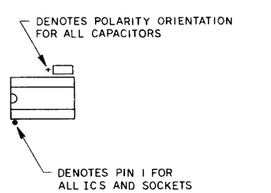


TABLE I

PART NUMBER	REFERENCE DESIGNATION
100-1025	R17
100-2215	R1, 5-8, 15, 18-21, 26-29
100-3315	R4, 9-12, 16, 22-25, 30-33
100-4715	R2, 3, 13, 14, 34
132-2752	C1-50
700-4180	U15
700-7400	U10, 27, 38, 107-907, 115-915
700-7402	U12, 34, 36, 39, 108-908, 111-911, 116-916
700-7404	U14, 21, 40, 109-909
700-7416	U2, 5, 7, 114-914
700-7420	U8, 11, 16, 18, 20, 22, 23, 102-902, 105-905
700-7440	U6, 9, 26, 32, 33, 35, 42
700-7450	U17, 37
700-7476	U1, 3, 4, 13, 24, 41, 43-47, 103-903, 104-904, 106-906, 110-910
700-7486	U19, 25, 31
700-7493	U28, 29, 30, 101-901
700-7495	U112-912
700-7496	U113-913

TABLE II

(6)	INTERNAL INTERFACE RESISTORS	TRANSPORT INTERFACE RESISTORS
VERSION	R1, R4 THRU R12	R15, R16, R18 THRU R33
-01	USE	USE
-02	USE	OMIT
-03	OMIT	USE

(7) DESIGNATION U, IS INTENTIONALLY OMITTED ON SOME ICS FOR CLARITY.

(6) FOR PARTS AFFECTED BY VERSION NO. SEE TABLE II.

(5) SEE TOP BILL FOR CORRECT VERSION OF TRACKING OSCILLATOR.

(4) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101382-01 REV J AND SUBSEQUENT.

(3) RUBBER STAMP ASSY PART NO. INCLUDING VERSION NUMBER AND VERSION ISSUE LETTER.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC-101380
SPECIFICATION-101384

NOTES: UNLESS OTHERWISE SPECIFIED:

PART NO. 101381 01 REV G

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± 1/2°
.XXX ± .005
X ± 1/64 ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR USE AUTHORIZED EXCEPT AS MADE

SIGNATURES	DATE
DR L.F. Smith	9/6/73
CHK [illegible]	9/6/73
DES	
ENGR [illegible]	9/6/73
ENGR	
MATL:	

TOP ASSY 1600
NEXT ASSY 1ST USED ON
APPLICATION
FINISH:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
PCBA —
READ 1600 CPI
PE FORMATTER

SIZE E | CONF IDENT. NO. | DWG NO. 101381 | REV H
SCALE 1/1 | DO NOT SCALE DWG | SHEET | OF

8 7 6 5 4 3 2 1
H G F E D C B A

4867A 4867B

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 5-YY PROD. RELEASE	12/19/73			
B	ECN 6002A	3/20/74			
C	ECN 6100	5/1/74			
D	ECN 6143	5/10/74			
E	ECN 5923	5/17/74			
F	ECN 6160	8/22/74			
G	ECN 6194	9/1/74			
H	ECN 6236B	10/1/74			
J	ECN 6380	10/22/74			
K	ECN 6526	1-31-75			
L	ECN 6561	2-5-75			
M	ECN 6722	9/25/75			
N	ECN 6831	11-11-75			
P	ECN 6916A	11/25/75			
R	ECN 7149	3/24/76			
S	ECN 7454	5/21/76			

TABLE I (1)	
PART NUMBER	REFERENCE DESIGNATIONS
100-1005	R18 THRU 26, 28 THRU 30, 41 THRU 50
100-1025	R8 THRU 11,13 THRU 16,51,79 THRU 82,86,87,88,90,91,92, 94 THRU 105
100-2215	R6,7,12,52 THRU 69
100-2225	R84
100-2235	R70 THRU 78
100-4715	R17,27,40
100-8205	R83
100-8215	R4
103-1515	R85
100-1225	R1
100-2715	R5
100-5615	R2,3
120-0001	U210,211,214
130-2205	C2
130-4715	C3
131-4720	C5
132-2752	C1,6 THRU 9,22 THRU 26, 39 THRU 44,56 THRU 120
139-1055	C4
200-3055	Q4
200-4123	Q1,2,3
300-4446	CR1 THRU 4
514-8715	S1
524-1202	Y1
700-0001	U42,43,62,64,84,202
700-0002	U1,85,110,3
700-0003	U66,86
700-1103	U67 THRU 75
700-3207	U4,24,45,76,46,35,56
700-4110	U2,22,61,112,128,148
700-4151	U124,127,152,153,164,172,173 188
700-4153	U16,36,57,77
700-4155	U122,125,162,185
700-4157	U93
700-4158	U191,192,193
700-4161	U15,23,102,106,123,126, 186
700-4175	U165
700-5107	U87 THRU 91
700-7400	U104, 129,132,133,167,181
700-7402	U41,63,83,105,111,131,141, 147,149,151,161,166,171 182,208
700-7404	U 142,145,168,183,209
700-7410	U82,107,205,121
700-7416	U103,201,203,204,215,216,217
700-7419	U19,39,60,96,117,137
700-7438	U143,146,184,206,207
700-7450	U169,170,174
700-7474	U79,80
700-7476	U108,109,130,144,150,187
700-7485	U17,37,58,94,115,135
700-7486	U78,81
700-7495	U18,38,59,95,116,136
700-7496	U189,190,194,195,197,212,213 196
(14) 103596-01	W21,22
700-4163	U163

TABLE II (2)															
ASSY 101811 VERSION NUMBER	VERSION CHARACTERISTIC	R36 THRU 39 100-1005 C10 THRU 21 C27 THRU 38 132-2752	R31 THRU 35 100-1005 U25 700-3207	U5 700-3207 U6 THRU 14 U26 THRU 34 700-1103	U47 THRU 55 700-1103 C45 THRU 55 132-2752	103596-01									
						W1 W2 W9 W13	W3 W4 W10 W15	W5 W6 W11 W17	W7 W8 W12 W19	W14	W16	W18	W20
-01	1K	OMIT	OMIT	OMIT	OMIT	OMIT	USE	OMIT	OMIT	USE	OMIT	USE	USE
-02	2K	OMIT	USE	OMIT	USE	OMIT	OMIT	USE	OMIT	USE	USE	OMIT	USE
-03	4K	USE	USE	USE	USE	OMIT	OMIT	OMIT	USE	USE	USE	USE	OMIT
-04	.5K	OMIT	OMIT	OMIT	OMIT	USE	OMIT	OMIT	OMIT	OMIT	USE	USE	USE

TABLE III (9)															
EDGE CONNECTION															
SHT	ZONE	J1-A SIGNAL	PIN NO.	J1-B SIGNAL	SHT	ZONE	SHT	ZONE	J2-A SIGNAL	PIN NO.	J2-B SIGNAL	SHEET	ZONE
⚠		IFAD	1	ITADØ	⚠		⚠		IFADO	1	ILOL		
		GND	2	GND					GND	2	ITADØ	⚠	
⚠		ITADI	3	IGO	6	1	15	8	IGOI	3	ITADI	⚠	
14	4	IREV	4	IWRT	14	4	14	6	IREVI	4	IWRT	15	8
		GND	5	GND					GND	5	IWFM	15 ⚠	8
			6	IEDIT	⚠		⚠		IEDIT	6	IERASE	15 ⚠	8
⚠		IERASE	7	ITHRI	⚠		⚠		ITHRI	7	ITHR2	⚠	
		GND	8	GND					GND	8	IDEN	⚠	
⚠		ITHR2	9	IDEN	⚠		14	6,15-6,17-3	IAUTO	9	IPAR	⚠	
	⚠	IPAR	10	ILOL			⚠		IREW	10	IOFL	⚠	
		GND	11	GND					GND	11	IFENI	14	6
⚠		IREW	12	IOFL	⚠		15	8,17-2	IEOO	12	ILWDI	14	8
19	6	ILWD	13	IFEN	14	2	14	6,16-7,17-5	IANS	13	IWBP	7	8
		GND	14	GND					GND	14	IWBØ	7	8
		——	15	IWP	12	1	7	8	IWBI	15	IWB2	7	8
12	1	IWØ	16	IWI	12	1	7	8	IWB3	16	IWB4	7	8
		GND	17	GND					GND	17	IWB5	7	8
12	1	IW2	18	IW3	12	1	7	8	IWB6	18	IWB7	7	8
12	1	IW4	19	IW5	12	1	10	8	IBCCØ	19	IBCCI	10	8
		GND	20	GND					GND	20	——		
12	1	IW6	21	IW7	12	1	10	8	IBCC2	21	IBCC3	10	8
14	8 ⚠	IFBY	22	IDBY	14	8 ⚠	13	8	ICAI	22	——		
		GND	23	GND					GND	23	IFBY	⚠	
18	8 ⚠	IDENT	24	IHER	14	8	13	8	ICBI	24	——		
⚠		ICER	25	IFMK	18	3 ⚠	10	1	IABSY	25	IBBSY	10	1
		GND	26	GND					GND	26	IDBY	⚠	
⚠		IRDY	27	IONL			13	2	IAOVFL	27	IBOVFL	13	2
⚠		IRWD	28	IFPT			⚠		IDENT	28	IHER	6	4
		GND	29	GND					GND	29	ICER	⚠	
18	3 ⚠	ILDP	30	IEOT	⚠		⚠		IRDY	30	IFMK	⚠	
		——	31	INRZ	⚠		⚠		IONL	31	IRWD	⚠	
		GND	32	GND					GND	32	IFPT	⚠	
⚠		I7TRK	33	ISGL	⚠		⚠		IEOT	33	ILDP	⚠	
⚠		ISPEED	34	IWSTR	14	8	⚠		INRZ	34	I7TRK	⚠	
		GND	35	GND					GND	35	ISGL	⚠	
18	1	IRSTR	36	IRP	7	8	17	1	IREQ	36	ISPEED	⚠	
7	8	IRØ	37	IRI	7	8	16	6	IBLWD	37	IRBP	12	1
		GND	38	GND					GND	38	IRBØ	12	1
7	8	IR2	39	IR3	7	8	12	1	IRBI	39	IRB2	12	1
7	8	IR4	40	IR5	7	8	12	1	IRB3	40	IRB4	12	1
		GND	41	GND					GND	41	IRB5	12	1
7	8	IR6	42	IR7	7	8	12	1	IRB6	42	IRB7	12	1
		——	43	——					——	43	——		
		GND	44	GND					GND	44	GND		
		——	45	——			14	6	+20V BBI	45	+20V BBI	14	6
		——	46	——					——	46	PSENH	14	6
		GND	47	GND					GND	47	-5V		
14	8	GND	48				14	8	GND	48	+5V	14	8
14	8	GND	49				14	8	GND	49	+5V	14	8
14	8	GND	50				14	8	GND	50	+5V	14	8

⚠ LOCATED ON SCHEMATIC INTERCONNECT 'C' DWG NUMBER 103310

TABLE IV (10)		
GROUND AND VOLTAGE		
REFERENCE DESIGNATION	PIN NO. +5V	PIN NO. GND
U1,2,3,18,22,38,41,59,61,63,66,78 THRU 83,85,86,95,103,104,105,107, 110,111,112,116,121,128,129,131,132, 133,136,141,142,143,145,146 THRU 149,151,161,166 THRU 171,174,181 THRU 184,201,203 THRU 211,214 THRU 217	14	7
U15,16,17,19,23,36,37,39,57,58,60, 77,93,94,96,102,106,115,117,122 123,124 THRU 127,135,137,152,153, 162 THRU 165,172,173,185,186,188, 191,192,193	16	8
U42,43,62,64,84,108,109,130, 144,150,187,202	5	13
U189,190,194 THRU 197, 212,213	5	12

REFERENCE DESIGNATION	PIN NUMBERS V_{SS} +16V	V_{BB} +20V	V_{DD} GND	V_{CC} +5V	$-V_{CC}$ -5V
U6 THRU 14,26 THRU 34,47 THRU 55, 67 THRU 75	17	10	11	—	—
U87 THRU 91	—	—	7	14	13
U4,24,25,35,45, 46,56,76,5	1	9	8	16	—

REFERENCE DESIGNATIONS		
LAST USED	NOT USED	DELETED
C120		
CR4		
Q4		
R105	R89,93	
TP12		
U217	U20,21,40,44,65,92,97,98 99,100,101,113,114,118 119,120,134,138 THRU 140 154 THRU 160,175 THRU 180,198 THRU 200	
W22		
Y1		

(17) SHEET 20 APPLIES TO THE FOLLOWING VERSIONS
101811-01F + ECN 6160 + ECN 6194 + ECN 6236 + ECN 6380
101811-02F
101811-03F
101811-04E + ECN 6160 + ECN 6194 + ECN 6236 + ECN 6380

(16) SHEET 17 APPLIES TO THE FOLLOWING VERSIONS
101811-01K AND SUBSEQUENT
101811-02K
101811-03K
101811-04J AND SUBSEQUENT

15.

(14) DO NOT INSTALL W21 AND W22 UNTIL AFTER POWER SUPPLY VOLTAGE HAS BEEN CONFIRMED

(13) FOR TERMINATING RESISTOR MODULE INFORMATION SEE SHEET 19

(12) FOR DECOUPLING INFORMATION SEE SHEET 19

(11) FOR SPARE LOGIC ELEMENTS SEE SHEET 19

(10) FOR IC GROUND AND VOLTAGE PIN NUMBERS SEE TABLE IV

(9) FOR SIGNAL IDENTIFICATION SEE TABLE III

8. I.C. TYPE IDENTIFICATION: 2 INPUT NAND GATES ARE 7400, 2 INPUT NOR GATES ARE 7402, INVERTERS ARE 7404, 3 INPUT NAND GATES ARE 7410

7. ALL DIODES ARE 1N4446

6. ALL NPN TRANSISTORS ARE 2N4123

5. ALL CAPACITORS ARE 2.7 MICROFARADS, ±20%, 35V

4. ALL RESISTORS ARE 10 OHMS, ±5%, 1/4W

3. SIGNALS ARE CROSS-REF BETWEEN SHEETS AND WITHIN A SHEET BY NUMBERS APPEARING UNDER THE ASSOCIATED LOGIC TERM MNEMONIC. THE FIRST NO. IS THE SHEET NO. AND THE SECOND NO. IS THE ZONE NO.

(2) FOR VALUE, PART NUMBER AND USAGE OF COMPONENTS AFFECTED BY VERSION NUMBER, SEE TABLE II

(1) FOR PART NUMBER OF COMPONENTS NOT AFFECTED BY VERSION NUMBER, SEE TABLE I

NOTES: UNLESS OTHERWISE SPECIFIED

ASSY NO. 101811

SPECIFICATION NO. 101814
BLOCK DIAGRAM NO. 103322

REFERENCE DRAWINGS:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
X ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

SIGNATURES	DATE
DR. COMPUTER	11-73
CHK	1-74
DES	77
ENGR	
PROJ. ENGR	

PERTEC PERIPHERAL EQUIPMENT

TITLE: SCHEMATIC, BUFFER

NEXT ASSY	1ST USED ON
APPLICATION	

FINISH: MATL:

SIZE F | CODE IDENT NO | DWG NO. 101810 | REV S
SCALE NONE | DO NOT SCALE DWG. | SHEET 1 OF 5

3/72 DIETERICH-POST CLEARPRINT 1030

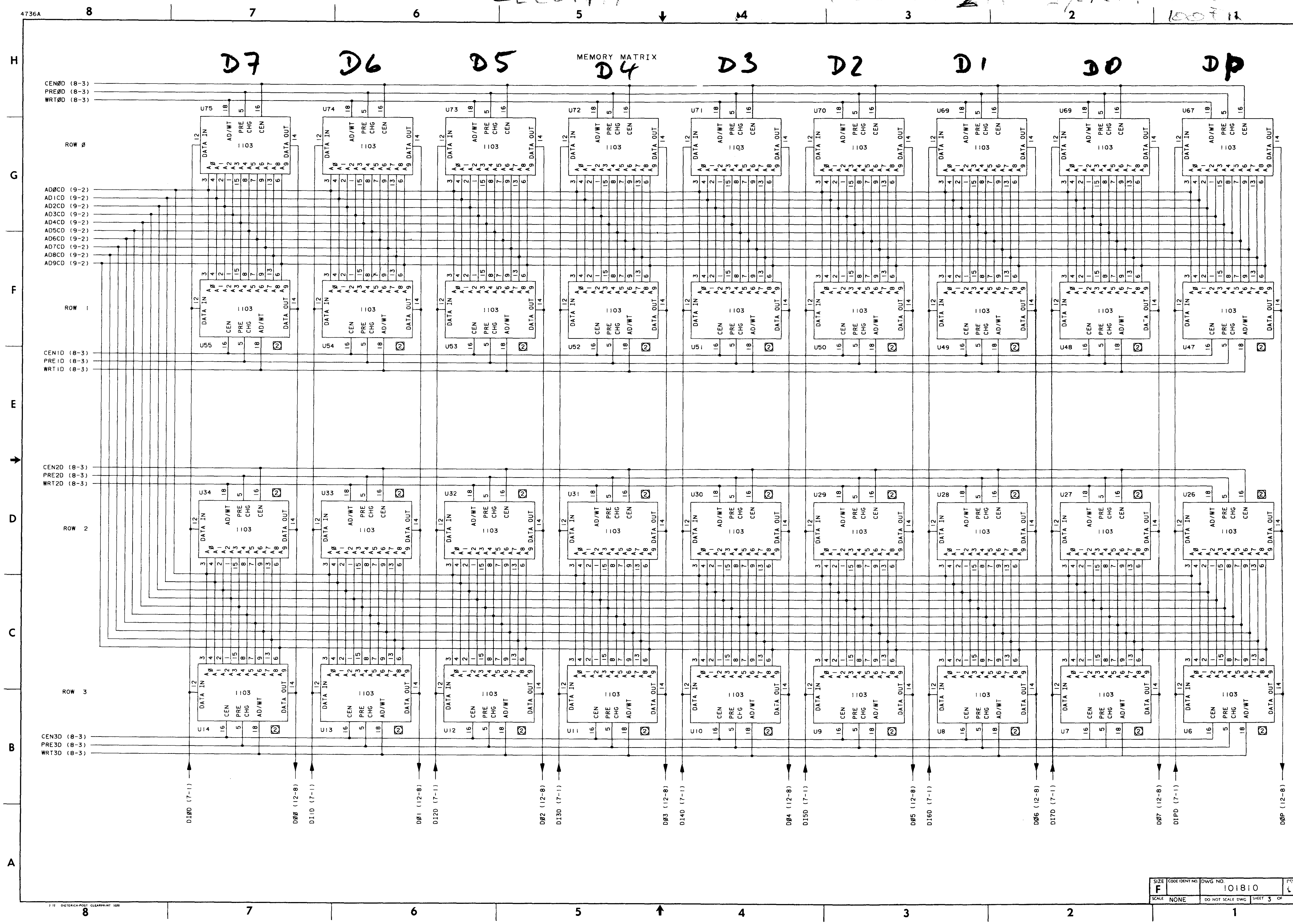
4735A

MEMORY CYCLE LOGIC

+5V
C1 2.7
R3 560
R1 1.2K
R4 820
Q1
Q2
Q3
Y1 12MHZ
C2 22PF 5% 500V
R2 560
R5 270
R6 220
R7 220
U1 74H04
C12SQT
C12ML1 (11-7) (17-2)
TP11
C12ML2 (6-6,11-7)
SAMPH (11-4)
U23 74161 LD CK CL T P A B C D CY
MC.75
QRSTL
MC1.5
NMC1.5
MC3
NMC3
MC6
NMC6
CM12MH
C12MLD
U22 74H11
U2 74H11
PREDJH
C12MLD
U43 74H76
R8 1K
U42-2,3 (16-6)
PREDH (8-5)
PSENL
U41
PREDR
CENL
CENDH
C3 470 5% 500V
ENRBH (10-2)
U132
RBLCL (12-5)
U61
LTCLR
U133
WTLCL (12-5)
ENWTH (10-2)
U112
WTLDH (12-5)
RBLDH (12-5)
CENJH
CENH (8-5)
CENL (10-3)
PSENH (14-4)
WRTSH
WRTSL
CENKH (10-2)
WRTH (8-5)
PSENL (14-3)
WRTENL (10-2)
WRTRL

SIZE	CODE IDENT NO.	DWG NO.	R'
F		101810	5
SCALE NONE		DO NOT SCALE DWG	SHEET 2 OF

3/72 DIETERICH-POST CLEARPRINT 1020


ELCOMA 01 44 22 11 ZH
MEMORY MATRIX
D7
D6
D5
D4
D3
D2
D1
D0
DP
ROW Ø
ROW 1
ROW 2
ROW 3
CENØD (8-3)
PREØD (8-3)
WRTØD (8-3)
ADØCD (9-2)
AD1CD (9-2)
AD2CD (9-2)
AD3CD (9-2)
AD4CD (9-2)
AD5CD (9-2)
AD6CD (9-2)
AD7CD (9-2)
AD8CD (9-2)
AD9CD (9-2)
CEN1D (8-3)
PRE1D (8-3)
WRT1D (8-3)
CEN2D (8-3)
PRE2D (8-3)
WRT2D (8-3)
CEN3D (8-3)
PRE3D (8-3)
WRT3D (8-3)
1103
DATA IN
DATA OUT
CEN
PRE
CHG
AD/WT
DIØD (7-1)
DØØ (12-8)
DI1D (7-1)
DØ1 (12-8)
DI2D (7-1)
DØ2 (12-8)
DI3D (7-1)
DØ3 (12-8)
DI4D (7-1)
DØ4 (12-8)
DI5D (7-1)
DØ5 (12-8)
DI6D (7-1)
DØ6 (12-8)
DI7D (7-1)
DØ7 (12-8)
DIPD (7-1)
DØP (12-8)
SIZE F
DWG NO. 101810
SCALE NONE
DO NOT SCALE DWG
SHEET 3
4736A

4737A

MEMORY A ADDRESS COUNTER

U19 74193 — INCRAH (10-1), CA1
U60 74193 — CA2, TO R97 (5-8)
U117 74193 — CA3
PSETAL (13-4)
+5V, R9 1K — TO U39-4 (5-8)
LDCAL (13-6)
U18, U59, U116 7495
U17, U58, U115 7485 — CMPAH (16-8) (19-8)
ACAD01, ACAD00, ALAD00, ALAD01, ALAD02, ALAD03, ACAD03, ACAD02, ACAD05, ACAD04, ALAD04, ALAD05, ALAD06, ALAD07, ACAD07, ACAD06, ACAD09, ACAD08, ALAD08, ALAD09, ALAD10, ALAD11, ACAD11, ACAD10
ACAD03 (9-8), ACAD02 (9-8), ACAD01 (9-8), ACAD00 (9-8)
ACAD07 (9-8), ACAD06 (9-8), ACAD05 (9-8), ACAD04 (9-8)
ACAD11 (9-8), ACAD10 (9-8), ACAD09 (9-8), ACAD08 (9-8)

+5V, R10 1K — U78,U80 (5-3)
U79 7474 — ACAD12, ACAD11, ADAD10, ADAD09
E1 W7 4K E2 — SBOVFH (13-4)
E3 W5 2K E4
E11 W3 1K E12
E13 W1 5K E14
E5 W8 4K E6 — ABOVFH (13-4)
E7 W6 2K E8
E9 W4 1K E10
E15 W2 5K E16
U78 7486 — LDCAH
U79 7474 — ALAD12
U78 7486 — ACMP3

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE		DO NOT SCALE DWG	SHEET 4 OF

2-72 DIETERICH-POST CLEARPRINT 1000

4738A

MEMORY B ADDRESS COUNTER

+5V
R11
1K
E35 E26 E29 E32
W13 W15 W17 W19
.5K 1K 2K 4K
E34 E25 E28 E31
W14 W16 W18 W20
E36 E27 E30 E33
2

2⁰ 2¹ 2² 2³ 2⁴ 2⁵ 2⁶ 2⁷

U39 74193 U96 74193 U137 74193
CL UP DN LD A B C D CY BORROW

INCRBH (10-1)
CB1 CB2 CB3
R9 (4-8)
PSETBL (13-4)

R10 (4-3)
U80 7474
PR D CK CL Q
BCAD12 E23 W12 4K E24 BBOVFH (13.4)
BCAD11 E21 W11 2K E22
BCAD10 E19 W10 1K E20
BCAD09 E17 W9 .5K E18

+5V
R97
1K
U117-4 (4-5)

U38 U95 U136
MC SERIAL IN CK1 CK2 7495

LDCBL (13-6)

U78 7486
LOCBH
U80 7474
BLAD12
U78 7486 BCMP3

BCAD01 BCAD00 BLAD00 BLAD01 BLAD02 BLAD03 BCAD03 BCAD02
BCAD05 BCAD04 BLAD04 BLAD05 BLAD06 BLAD07 BCAD07 BCAD06
BCAD09 BCAD08 BLAD08 BLAD09 BLAD10 BLAD11 BCAD11 BCAD10

U37 U94 U135
A0 A1 A2 A3 A>B IN A=B IN A<B IN A>B OUT A=B OUT A<B OUT
7485
B0 B1 B2 B3

CMPBH (16-8) (19-8)

BCAD03 (9-8)
BCAD02 (9-8)
BCAD01 (9-8)
BCAD00 (9-8)
BCAD07 (9-8)
BCAD06 (9-8)
BCAD05 (9-8)
BCAD04 (9-8)
BCAD11 (9-8)
BCAD10 (9-8)
BCAD09 (9-8)
BCAD08 (9-8)

SIZE	CODE IDENT NO	DWG NO.	REV
F		101810	5
SCALE NONE	DO NOT SCALE DWG	SHEET 5 OF	

2-72 DIETERICH-POST CLEARPRINT 1020

4739A

REFRESH AND 6MHZ CLOCK LOGIC

U110 74H04 — TPI2 — R12 220 — C4 .1 10% — ½ 18KHZ — C5 .0047 10% 100VDC — U111

LEREFH (11-7)

+5V — R15 1K — U15 74161 (LD, CK, CL, T, P, A, B, C, D, CY, Q_A–Q_D)

REFAD4 (9-8)
REFAD3 (9-8)
REFAD2 (9-8)
REFAD1 (9-8)
REFAD0 (9-8)

+5V — R14 1K — U109 (18-8)

U108 7476 — C12ML2 (2-5) — PSENH (14-4) — PSENH

C6MH (14-7, 16-5, 17-5, 18-5, 19-5)
C6ML (14-7, 15-3, 18-8, 16-6)

+5V — R16 1K — U103 7416 — U105 — WTGOH (19-3) — RTGOH (18-2) — SGOL — SGOH

U106 74161 (LD, CK, CL, T, P, A, B, C, D, CY, Q_A–Q_D)

TAPE6H — U104 — FBYOVR (18-1) — GOCL

U105 — DBY (14-6)

GGO (14-7) — U201 7416 — J1 B3 IGO

U167 — WFM (15-6) — WRT (15-4) — FMWRTL — FMWRTL (14-5)

U167 — IWRTI (15-7) — ERASE (15-6) — ERWRTL

U167 — EXTOGH — U184 7438 — GO (15-6)

GOVERL (19-6)

U107 — GSQ2H — GSQ1H — GSQ0H — GOVERL

U107 — GOVERH (18-7)

U102 74161 (LD, CK, CL, T, P, A, B, C, D, CY, Q_A–Q_D)

WTSQ6L (19-3) — RTSQ6L (18-4) — U104 — TAPE6H

RTSQ7H (18-2) — WTSQ7H (19-3) — U105 — TAPE7L

8 RETH
4 RETH
2 RETH
1 RETH

+5V — R13 1K — U81-4 (17-8)

S1 — U103 7416 — J2 B28 IHERI

ø

THER (14-6) — U104 — NRETRY (18-7, 19-7)

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	5
SCALE NONE		DO NOT SCALE DWG	SHEET 6 OF

2-72 DIETZGEN-POST CLEARPRINT 1020

READ TAPE/WRITE BUFFER INTERFACE

MEMORY DATA DRIVER

U214 U213 U211 U212 U210 U189 U190 U192 U191 U4 U24 U45 U85 74H04 U169 7450 U129

J2: IWBØ B14, IWB1 A15, IWB2 B15, IWB3 A16, IWB4 B16, IWB5 B17, IWB6 A18, IWB7 B18, IWB8 B13

J1: IRØ A37, IR1 B37, IR2 A39, IR3 B39, IR4 A40, IR5 B40, IR6 A42, IR7 B42, IRP B36

WBLØØL WBLØ1L WBLØ2L WBLØ3L WBLØ4L WBLØ5L WBLØ6L WBLØ7L WBLDPL

RTLØØL RTLØ1L RTLØ2L RTLØ3L RTLØ4L RTLØ5L RTLØ6L RTLØ7L RTLDPL

WBLDH (17-3)
WBSQ1L (17-4)
RTMRH (18-2)
RTSQ1L (18-4)

DATIØ DATI1 DATI2 DATI3 DATI4 DATI5 DATI6 DATI7

+5V R17 470

DIØD (3-7) DI1D (3-7) DI2D (3-6) DI3D (3-5) DI4D (3-4) DI5D (3-4) DI6D (3-3) DI7D (3-2) DIPD (3-1)

SAMPL (11-1) ADENH1 (9-5) ADENH2 DATSLH (10-2) DATSLL DATIP

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	-
SCALE NONE		DO NOT SCALE DWG	SHEET 7 OF

MEMORY CLOCK DRIVERS

ADI1Ø (9-6)
ADI11 (9-6)
U85 74H04
NADI1Ø
NADI11
U86 74H00
RS1L
RS2L
RS3L
U66 74H00
SELØH
SELIH
SEL2H
SEL3H
CENH (2-1)
PREDH (2-1)
WRTH (2-1)
NMAC2 (11-2)
+5V
R27 470
U46 3207
CENØ
PREØ
WRTØ
WRTI
R28
R29
R30
R31 2
CENØD (3-8)
PREØD (3-8)
WRTØD (3-8)
WRTID (3-8)
U25 2 3207
CENI
PREI
CEN2
PRE2
R32 2
R33 2
R34 2
R35 2
CEN1D (3-8)
PRE1D (3-8)
CEN2D (3-8)
PRE2D (3-8)
U5 2 3207
WRT2
WRT3
CEN3
PRE3
R36 2
R37 2
R38 2
R39 2
WRT2D (3-8)
WRT3D (3-8)
CEN3D (3-8)
PRE3D (3-8)

SIZE	CODE IDENT NO	DWG NO	REV
F		101810	
SCALE NONE	DO NOT SCALE DWG	SHEET 8 OF	

4742A

BUFFER PCBA MEMORY ADDRESS MUX

U16 — 74153

ACADØØ (4-7)
BCADØØ (5-7)
REFADØ (6-3)
ACADØ1 (4-7)
BCADØ1 (5-7)
REFAD1 (6-3)
ENAL (10-2)
MAC2 (11-1)

ADIØØ
ADIØ1

U36 — 74153

ACADØ2 (4-7)
BCADØ2 (5-7)
REFAD2 (6-3)
ACADØ3 (4-7)
BCADØ3 (5-7)
REFAD3 (6-3)

ADIØ2
ADIØ3

U57 — 74153

ACADØ4 (4-5)
BCADØ4 (5-5)
REFAD4 (6-3)
ACADØ5 (4-5)
BCADØ5 (5-5)

ADIØ4
ADIØ5

U77 — 74153

ACADØ6 (4-5)
BCADØ6 (5-5)
ACADØ7 (4-5)
BCADØ7 (5-5)

ADIØ6
ADIØ7

U93 — 74157

ACADØ8 (4-4)
BCADØ8 (5-4)
ACADØ9 (4-4)
BCADØ9 (5-4)
ACADIØ (4-4)
BCADIØ (5-4)
ACADI1 (4-4)
BCADI1 (5-4)

ADIØ8
ADIØ9
ADIIØ (8-8)
ADII1 (8-8)

SAMPL (11-1)

U85 74H04

ADENHI (7-3)

+5V

R40 470

MEMORY ADDRESS DRIVERS

U35 — 3207

ADØC — R41 — ADØCD (3-8)
AD1C — R42 — AD1CD (3-8)

U56 — 3207

AD2C — R43 — AD2CD (3-8)
AD3C — R44 — AD3CD (3-8)

3207

AD4C — R45 — AD4CD (3-8)
AD5C — R46 — AD5CD (3-8)

U76 — 3207

AD6C — R47 — AD6CD (3-8)
AD7C — R48 — AD7CD (3-8)

3207

AD8C — R49 — AD8CD (3-8)
AD9C — R50 — AD9CD (3-8)

3207

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE		DO NOT SCALE DWG	SHEET 9 OF

2/72 DIETERICH-POST CLEARPRINT 1020

MEMORY DATA ROUTING LOGIC

U172 74151 — WT (15-2), RT (15-2), RTWT (15-1) → ASTOPH (13-8) (19-8), ASTOPL
U173 74151 — → BTOPH (13-8) (19-8), BTOPL
U152 74151 — → ASBOPH (13-8) (16-8), ASBOPL
U153 74151 — RB (15-2), RBWB (15-1), WB (15-2) → BBOPH (13-8)(16-8), BBOPL

U214 (T 1 2 3 4) — IBCC1 (13-4), MBCC1 (13-4) (15-7)

J2 — IBCC0 A19, IBCC1 B19, IBCC2 A21, IBCC3 B21

U193 74158 — IBCC0 → MBCC0, IBCC1 → MBCC1, IBCC2 → MBCC2, IBCC3 → MBCC3; NAUTCOD (18-2), AUTCOD (18-2), EN, SEL

U132 — AUTO (14-3) → INCONL (17-8)

NWB (15-2) NMAC1 (11-2) → U131 → DATSLH (7-5)
NRT (15-2) NMAC3 (11-2) → U131 → U171 → WRTENL (2-4)
NRB (15-2) → U131 → ENRBH (2-7)
NWT (15-2) → U131 → ENWTH (2-7)

U171 → TENAH; U151 → CENAH; U171 → TENBH; U151 → CENBH

ENAL (9-8) → U111 → INCRAH (4-8)
CENKH (2-2) → U1 74H04 → CENKL (11-7)
CENL (2-1) → U61 74H11 → U41 → U111 → INCRBH (5-8)

U215 7416 — ASBOPH (13-8) (16-8) → J2 A25 IABSY
U215 7416 — BBOPH (13-8)(16-8) → J2 B25 IBBSY
U133 — AFRSTL (18-3)

SIZE	CODE IDENT NO.	DWG NO.	RFV
F		101810	--
SCALE NONE	DO NOT SCALE DWG	SHEET 10 OF	

MEMORY ACCESS LOGIC

+5V
R51
1K

WTSQIL
(19-3)
RTMRH
(18-2)
U64
74H76
NMR3
U63
SQ3
C12ML2
TAPE PRIORITY I
NMAC3
(10-4)

WBMRH
(17-3)
RBMRSH
(16-7)
U83
U84
74H76
C12ML2
(2-5)
NMR1
NMR1
(17-6)
SQ1
BUFFER PRIORITY II
U82
NMAC1
(10-4,16-5)

CENKL
(10-1)

REFRESH PRIORITY III

LEREFH
(6-5)
U62
74H76
NMR2
SQ2
C12ML1
NMAC2
(8-8)
U110
74H04
MAC2
(9-8)

C12ML1
(2-5)
PSENH
(14-3)
NNQ3
NNQ2
NMAC3
SAMPH
(2-6)
U85
74H04
SAMPL
(7-3,9-5)

SIZE	CUSTOMER NO	DWG NO	REV
F		101810	
SCALE	NONE		

4745A

MEMORY SENSE AMPLIFIERS

READ BUFFER/WRITE TAPE INTERFACE

+5V +5V
R79 1K
R80 1K

DØØ (3-7) R52 220
D01 (3-6) R53 220
D02 (3-5) R54 220
D03 (3-5) R55 220
D04 (3-4) R56 220
D05 (3-3) R57 220
D06 (3-2) R58 220
D07 (3-1) R59 220
DOP (3-1) R60 220

+5V R70 22K R61 220 — U91
+5V R71 22K R62 220 — 5107
+5V R72 22K R63 220 — U90
+5V R73 22K R64 220 — 5107
+5V R74 22K R65 220 — U89
+5V R75 22K R66 220 — 5107
+5V R76 22K R67 220 — U88
+5V R77 22K R68 220 — 5107
+5V R78 22K R69 220 — U87
5107

SDØØ
SDØ1
SDØ2
SDØ3
SDØ4
SDØ5
SDØ6
SDØ7
SDØP

WTLDH (2-6)
WTLCL (2-6)

U194 7496: A SDØØ, B SDØ1, C SDØ2, D SDØ3, E SDØ4, CK WTLCL, SI, PR, CL
U195 7496: A SDØ5, B SDØ6, C SDØ7, D SDØP, E WTLDH, CK WTLCL, SI, PR, CL
U196 7496: A RBØ, B RB1, C RB2, D RB3, E RB4, CK RBLCL, SI, PR, CL
U197 7496: A RB5, B RB6, C RB7, D RBP, E RBLDH, CK RBLCL, SI, PR, CL

U194: QA 15 WØ, QB 14 W1, QC 13 W2, QD 11 W3, QE 10 W4
U195: QA 15 W5, QB 14 W6, QC 13 W7, QD 11 WP, QE 10
U196: QA 15 RBØ, QB 14 RB1, QC 13 RB2, QD 11 RB3, QE 10 RB4
U197: QA 15 RB5, QB 14 RB6, QC 13 RB7, QD 11 RBP, QE 10

U203 7416: 3→4, 1→2, 9→8, 11→10, 13→12
U204 7416: 1→2, 3→4, 5→6, 11→10, 13→12
U216 7416: 3→4, 1→2, 5→6, 11→10, 13→12
U217 7416: 1→2, 9→8, 11→10, 13→12, 5→6, 3→4

J1: A16 IWØ, B16 IW1, A18 IW2, B18 IW3, A19 IW4, B19 IW5, A21 IW6, B21 IW7, B15 IWP
J2: B38 IRBØ, A39 IRB1, B39 IRB2, A40 IRB3, B40 IRB4, B41 IRB5, A42 IRB6, B42 IRB7, B37 IRBP

RBLDH (2-6)
RBLCL (2-6)

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE	DO NOT SCALE DWG	SHEET 12 OF	

2-72 DIETERICH-POST CLEARPRINT 1000

4746A

COUNTER CONTROL LOGIC

J2 ICAI A22 — U214 T — U209 — CAI

ASBOPH (10-4) — U207 7438 — ASTOPH (10-4) — U207 7438 — RBSQ6H (16-2) — U207 7438 — RTSQ5H (18-2) — U207 7438

+5V R81 1K — LDCAL (4-8) — U208 — U208 — PSETAL (4-8)

ASBOPH — U174 7450 — CNTOVL (17-7)

BBOPH — U174

CLRH (14-3)

ABOVFH (4-1) MBCCI (10-6) — U169 7450 — SABOVL — U171 — IO SABOVH

SBOVFH (4-1) IBCCI (10-7) — U169

NWB (15-1) — U171

U216 7416 — J2 A27 IAOVFL

+5V R105 1K — U215 7416

U216 7416 — J2 B27 IBOVFL

WB (15-1) BBOVFH (5-1) — U112 74H11

WBSQ5H (17-3) — U206 7438 — WTSQ5H (19-3) — U206 7438 — BBOPH (10-4) — U206 7438 — BTOPH (10-4) — U206 7438

+5V R82 1K — LDCBL (5-8) — U208 — U208 — PSETBL (5-8)

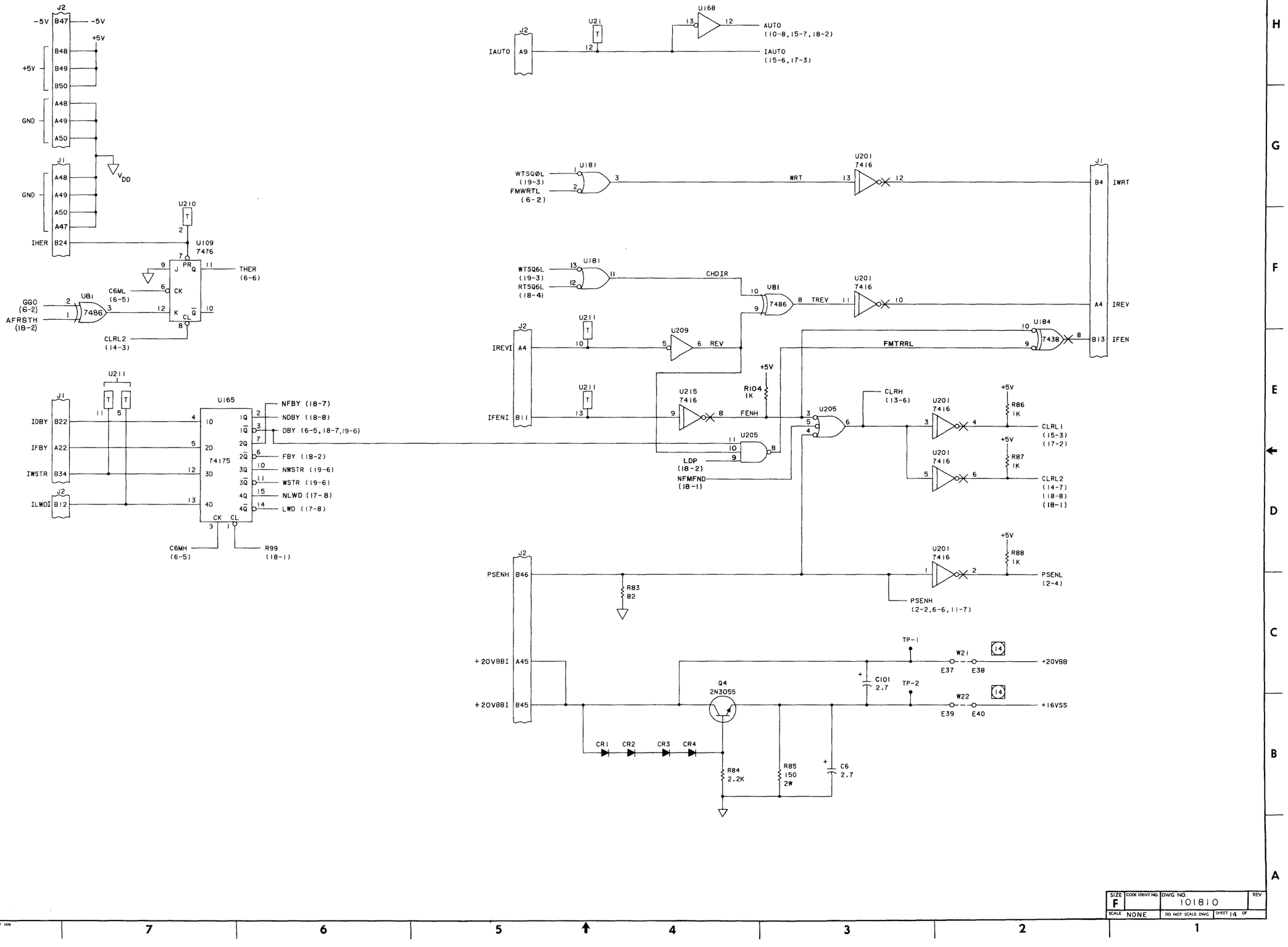
ASTOPH — U174 7450 — TAPOVL — U209 — TAPOVH (18-8)

BTOPH

J2 ICBI A24 — U214 T — U209 — CBI

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE	DO NOT SCALE DWG	SHEET 13 OF	

2-72 DIETERICH-POST CLEARPRINT 1020



SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE	DO NOT SCALE DWG	SHEET 14 OF	

4748A

BUFFER COMMAND REGISTER

J2 IWRTI B4 — U211 T — IWRTI (6-3)
J2 IEOO A12 — IEOO (17-3)
J2 IERASE B6 — U168 — ERASE (6-3)
J2 IGOI A3 — U210 T
J2 IWFM B5 — IWFM

U168 — WRT — WRT (6-3)

U149 — RTGO

U148 74H11 — AUTO (14-3), MBCC1 (10-6) — ATOCON (16-3,17-3,18-2,19-3)

U128 74H11 — WFM — FMSSET (18-8)

U149 — IAUTO (14-4), BGOL — AWTL

U168 — EOO (18-2)

U133 — GO (6-2)

U149 — MANGO

U128 74H11 — WTH
U148 74H11 — WBH
U148 74H11 — RBH
U128 74H11 — RTH

U129 — ARTL

U130 7476 — WTSL (17-3), RWTH (19-3) — WT (10-6,19-5), NWT (10-3,19-6)
U130 7476 — RT (10-6,18-5), NRT (10-3,18-6)
U150 7476 — WB (10-4,13-4,17-5), NWB (10-4,13-4,17-6)
U150 7476 — RBSL (18-2), RRBFH (16-2) — RB (10-6,16-7), NRB (10-3,16-4)

U132 — RTWT (10-6)
U132 — RWB (10-6)

RWBFH (17-3)
C6ML (6-5)
CLRL1 (14-3)

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE	DO NOT SCALE DWG	SHEET 15 OF	

4749A

READ BUFFER MICRO CONTROLLER

J2 IANS AI3 — U211 T — U209 — TO R8 (2-2) — U42 74H76 — C6ML (6-5) — ANS (17-6)

U188 74151 — RTSQ7L (18-4) — NMAC1 (11-2) — RBRUNH — NANS (17-6)

+5V — R91 1K — +5V — R90 1K

ASBOPH (10-4) — CMPAH (4-4) — BBOPH (10-4) — CMPBH (5-1) — U170 7450 — COMPL

U182 — RBCLDH — U183 — U184 7438 — RBCLRL

U186 74161 — C6MH (6-5) — RBPCØ — RBPC1 — RBPC2

U203 7416 — NRB (15-1)

U185 74155 — RBSQ7L — U183 — RBSQ7H (18-7)

RBSQ6L — U183 — RBSQ6H (13-8)

ATOCON (15-6) — U182 — RRBFH (15-3)

RBSQ4L — U145 — RBSQ4H

RBSQ3L — U183 — RBSQ3H (17-2)

RBSQØL (17-3)

COMPH — U182 — RBWRSH (11-7)

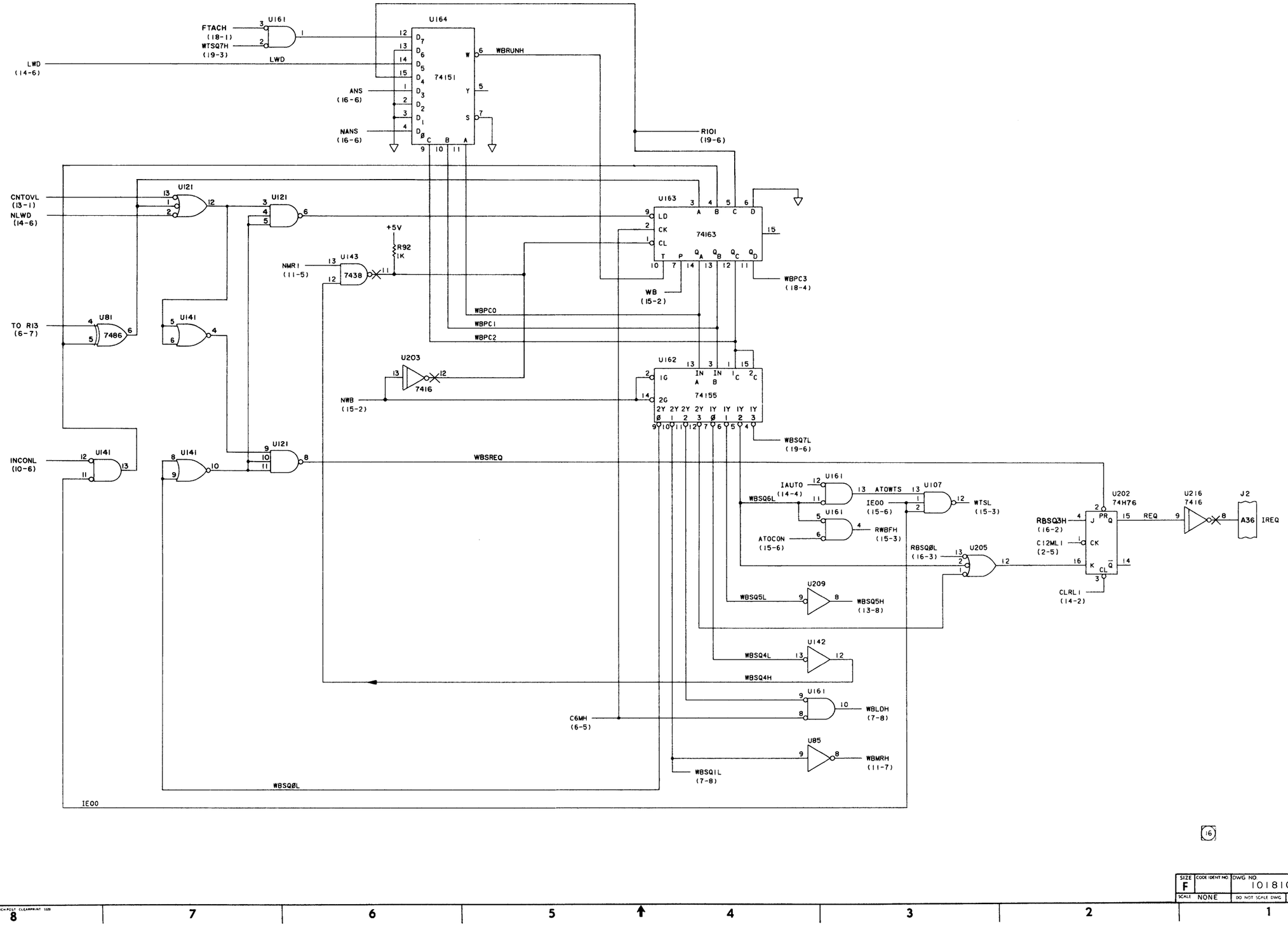
U183 — U184 7438 — J2 A37 IBLWD

RB (15-2)

SIZE	CODE IDENT NO.	DWG NO.	REV.
F		101810	
SCALE NONE		DO NOT SCALE DWG	SHEET 16 OF

2/72 DIETERICH-POST CLEARPRINT 3600

WRITE BUFFER MICRO CONTROLLER



(16)

SIZE	CODE IDENT NO	DWG NO	REV
F		101810	
SCALE NONE		DO NOT SCALE DWG	SHEET 17 OF

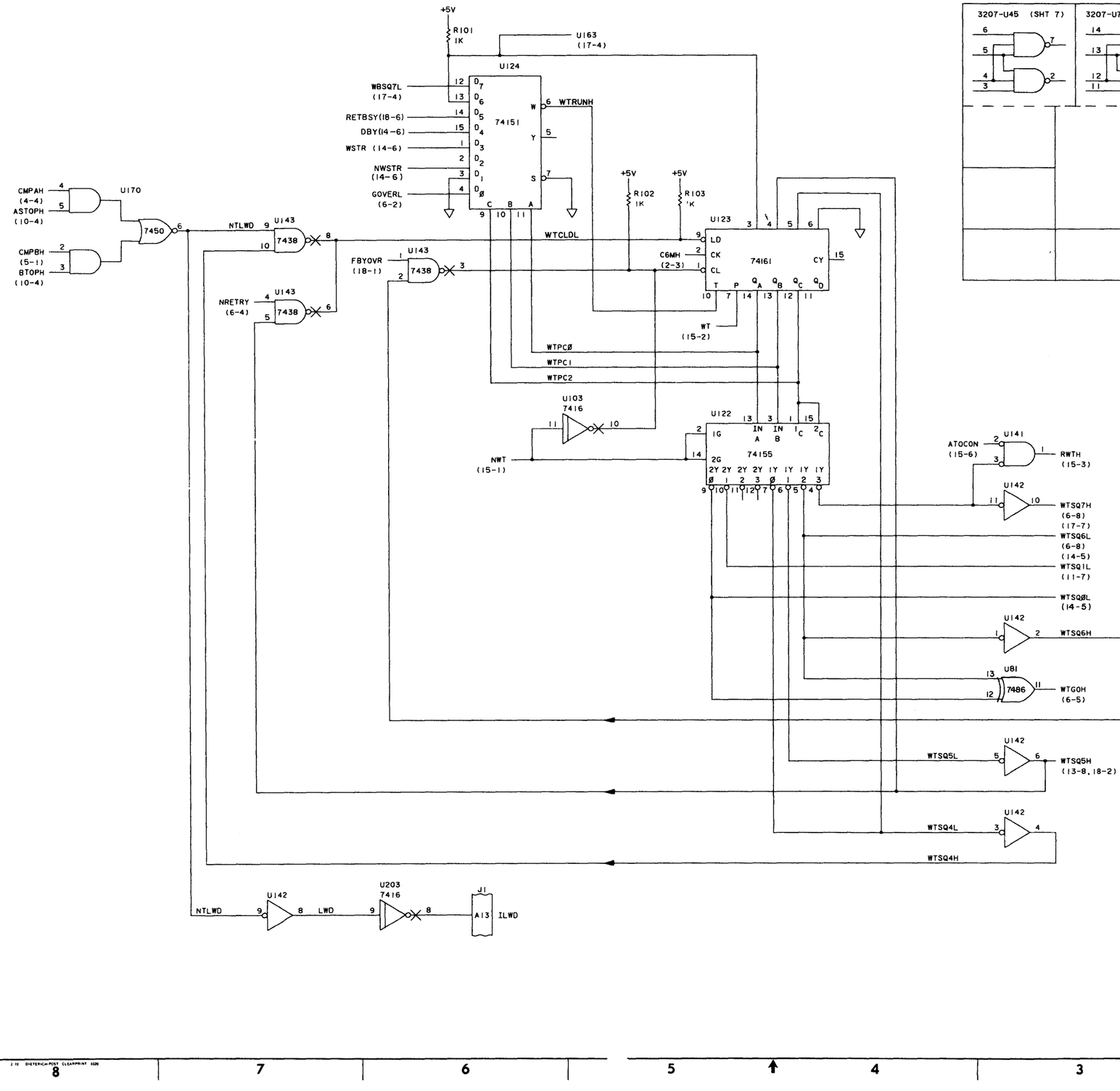
READ TAPE AND FMK SEARCH MICRO CONTROLLER

U210 T
U110 74H04
JI IRSTR A36, ICCG (IIDENT) A24
RI4 (6-4)
U109 7476
FMSSET
C6ML (6-4)
U144 7476
CLRL2 (14-3)
U182 NDBY (14-6), TAPOVH (13-1), TOVERL
U166 FBYFCL
FTACH
RBSQ7H (16-2)
U147
NFBY (14-6)
NRETRY (6-4)
RETBSY (19-6)
RSTRG
NDBY
NFMS
FMS
DBY (14-6)
GOVERH (6-1)
U167
U146 7438
U103 7416
RTLDL
NRT (15-1)
U127 74151
RTRUNH
RTCLDL
+5V
R94 1K
R95 1K
R96 1K
U126 74161
C6MH (6-4)
RT (15-2)
RTPCØ
RTPC1
RTPC2
U125 74155
RTSQ7L (16-5)
RTSQ5L
RTSQ6L
RTSQ4L
RTSQ6L (6-8, 14-6)
RTSQ3L
RTSQ6L
RTSQØL
RTSQ2L
RTSQ6H
RTSQ3H
RTSQ5H
RTSQ4H
FBYOVR
RTSQIL (7-8)
RTCLRL
U145
U187 7476
AUTCOD (10-8)
NAUTCOD (10-8)
FBY (14-6)
R98 1K
R99 1K
U165 (14-7)
U144 7476
FBYOVR (6-4) (19-6)
FTACH (17-7)
U111
U133
AFRSTL (10-2)
AFRSTH (14-7)
WBPC3 (17-4)
RTPC3
AFLGCK
U105
ATOCON (15-6)
RRTH (15-3)
RTSQ7H (6-8)
U129
AUTO (14-3)
RBSL (15-3)
RTSQ5H (13-8)
WTSQ5H (19-2)
FBYFCL
EOO (15-4)
U149
R100 1K
U202 74H76
FMS
NFMFND (14-5)
CLRL2 (14-2)
U104
RTGOH (6-5)
U166
RTMRH (7-8, 11-7)
U181
FMCLK
JI ILDP A30, IFMK B25
U181
FMKIND
U183
LDP (14-5)

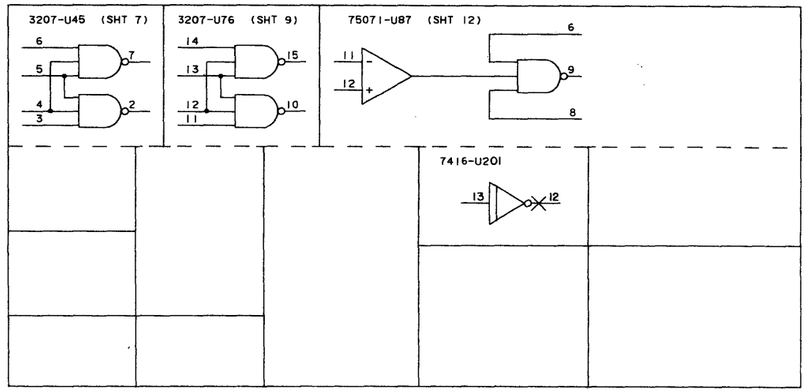
SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	
SCALE NONE		DO NOT SCALE DWG	SHEET 18 OF

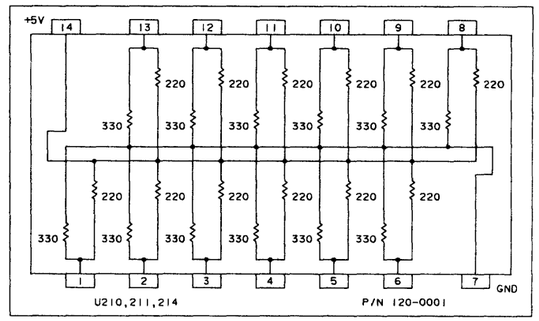
4752A

WRITE TAPE MICRO CONTROLLER



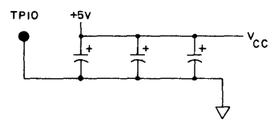
SPARE LOGIC ELEMENTS



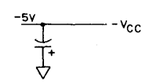


DECOUPLING

REF: TTL LOGIC, ALL SHEETS



REF: APPLIES TO SHT 3 MEMORY



REF: APPLIES TO SHT 12 MEMORY SENSE AMPS

SIZE	CODE IDENT NO	DWG NO	REV
F		101810	
SCALE NONE	DO NOT SCALE DWG	SHEET 19 OF	

WRITE BUFFER MICRO CONTROLLER

FTACH (18-1)
WTSQ7H (19-3)
U161
LWD (14-6)
LWD
U164
74151
WBRUNH
ANS (16-6)
NANS (16-6)
RIOI (19-6)
CNTOVL (13-1)
NLWD (14-6)
U121
U121
+5V
R92 180
NMRI (11-5)
U143
7438
U163
74163
LD
CK
CL
WB (15-2)
WBPC3 (18-4)
WBPC0
WBPC1
WBPC2
TO RI3 (6-7)
U81
7486
U141
U203
7416
NWB (15-2)
U162
74155
WBSQ7L (19-6)
INCONL (10-6)
U141
U141
U121
WBSREQ
IAUTO (14-4)
U161
ATOWTS
U107
WBSQ6L
IE00 (15-6)
WTSL (15-3)
U161
RWBFH (15-3)
ATOCON (15-6)
RBSQ2H (16-2)
U202 74H76
REQ
U216 7416
J2
A36
IREQ
C12ML1 (2-5)
CLRL1 (14-2)
RBSQ0L (16-3)
U205
WBSQ5L
U209
WBSQ5H (13-8)
U142
WBSQ4L
WBSQ4H
U161
WBLDH (7-8)
C6MH (6-5)
U85
WBMRH (11-7)
WBSQ1L (7-8)
WBSQ0L
IE00

17

SIZE	CODE IDENT NO.	DWG NO.	REV
F		101810	U
SCALE NONE		DO NOT SCALE DWG	SHEET ... OF

REWORK INSTRUCTIONS:

A. FOR ASSYS USING PROCESS BOARDS 101812-01J OR 101812-01K:

CUT ETCH:

1. BETWEEN U111-12 AND FEEDTHRU (CIRCUIT SIDE).
2. AT U185-11 (COMPONENT SIDE).
3. AT U124-15 (COMPONENT SIDE)
4. AT U23-2 (CIRCUIT SIDE BOTH SIDES OF PIN)

ADD JUMPERS ON CIRCUIT SIDE AS NOTED (USING 691-6030):

FROM	TO	NOTES
U43-14	U61-3	
U43-16	U61-4 & 5	
U41-1	U111-12	
U185-12	U183-11	
U61-6	U41-2 & 3	COVER ETCH BETWEEN U41-2 & U41-3 WITH SOLDER MASK TOUCH-UP. KEEP WIRE AS FAR UP ON U41-2 & 3 AS POSSIBLE.
U87-8	U87-11 & 12	
U105-3	U124-15	
U3-4	U43-1	
U23-2	U1-9	

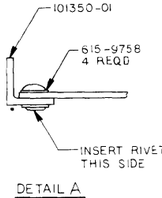
B. FOR ASSYS USING PROCESS BOARDS 101812-01L:

CUT ETCH:

1. BETWEEN U111-12 AND FEED THRU (CIRCUIT SIDE)
2. AT U185-11 (COMPONENT SIDE)
3. AT U85-14 (2 PLACES CIRCUIT SIDE)
4. AT U124-15 (COMPONENT SIDE)
5. AT U23-2 (CIRCUIT SIDE BOTH SIDES OF PIN)
6. AT U171 BETWEEN U171 BETWEEN PINS 8 & 9 (CIRCUIT SIDE)
7. AT U174-4 BOTH TRACES (CIRCUIT SIDE)
   U174-3 (CIRCUIT SIDE)
   U174-10 (CIRCUIT SIDE)
   U174 BETWEEN PINS 3 & 10 (COMPONENT SIDE)
8. ON CIRCUIT SIDE, BOTH SIDES OF FEED THRU CONNECTING U64-6 & U84-1

ADD JUMPERS ON CIRCUIT SIDE AS NOTED (USING 691 6030):

FROM	TO	NOTES
U43-14	U61-3	
U43-16	U61-4 & 5	
U41-1	U111-12	
U185-12	U183-11	
U24-14	TO FEEDTHRU LOCATED APPROX ON ℄ BETWEEN U164 & 184	
U61-6	U41-2 & 3	COVER ETCH BETWEEN U41-2 & 3 WITH SOLDER MASK TOUCH UP. KEEP WIRE AS FAR UP ON U41-2 & 3 AS POSSIBLE.
U87-8	U87-11&12	
U105-3	U124-15	
U3-4	U43-1	
U23-2	U1-9	
U216-11	U174-10	
U174-3 U112-13	TO FEED THRU LOCATED APPROX ON CENTER LINE OF U153-5	
U174-1	U216-13	
U215-6	U174-4	
U112-12	U216-11	
U150-11	U12-1 &2	
U150-10	U171-9	
R105	U215-6	SLEEVE LEADS USING 669-0122 AS REQD
R105	U217-14 (5V)	
J1-B10	J2-B1	
U215-5	U171-8	
U64-1	U1-8	
U64-6	U84-1	



DETAIL A
SCALE: 4/1

3. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101812-01 REV L AND SUBSEQUENT.

(2) MARK VERSION NO. AND VERSION ISSUE LETTER.

1. ASSEMBLE PER STANDARD MFG METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
T	ECN 7445				
U	ECN 7283				
V	ECN 7454				

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 5YG PROD RELEASE	-	-		
B	ECN 5079				
C	ECN 6002A				
D	ECN 6100				
E	ECN 6143				
F	ECN 5923 REVISED & REDRAWN				
G	ECN 6160				
H	ECN 6194				
J	ECN 6236 B REVISED & REDRAWN				
K	ECN 6380				
L	ECN 6400				
M	ECN 6526				
N	ECN 6559				
P	ECN 6722				
R	ECN 6831				
S	ECN 6976A				

SEE REWORK INSTRUCTIONS (ETCH CUTS)

DENOTE POLARITY ORIENTATION FOR ALL CAPACITORS

SEE REWORK INSTRUCTIONS (ETCH CUTS)

FOR ASSYS USING PROCESS BOARDS 101812-01 L:
ETCH: 1. BETWEEN U111-12 AND FEED THRU (CIRCUIT SIDE)
2. AT U185-11 (COMPONENT SIDE)
3. AT U85-14 (2 PLACES CIRCUIT SIDE)
4. AT U124-15 (COMPONENT SIDE)
5. AT U23-2 (CIRCUIT SIDE BOTH SIDES OF PIN)
6. AT U171 BETWEEN U171 BETWEEN PINS 8 & 9 (CIRCUIT SIDE)
7. AT U174-4 BOTH TRACES (CIRCUIT SIDE)
U174-3 (CIRCUIT SIDE)
U174-10 (CIRCUIT SIDE)
U174 BETWEEN PINS 3 & 10 (COMPONENT SIDE)
8. ON CIRCUIT SIDE, BOTH SIDES OF FEED THRU CONNECTING U64-6 & U84-1
ADD JUMPERS ON CIRCUIT SIDE AS NOTED (USING 691 6030):

FROM	TO	NOTES
U43-14	U61-3	
U43-16	U61-4 & 5	
U41-1	U111-12	
U185-12	U183-11	
U24-14	TO FEEDTHRU LOCATED APPROX ON ℄ BETWEEN U164 & 184	
U61-6	U41-2 & 3	COVER ETCH BETWEEN U41-2 & 3 WITH SOLDER MASK TOUCH UP, KEEP WIRE AS FAR UP ON U41-2 & 3 AS POSSIBLE.
U87-8	U87-11 & 12	
U105-3	U124-15	
U3-4	U43-1	
U23-2	U1-9	
U216-11	U174-10	
U174-3 U112-13	TO FEED THRU LOCATED APPROX ON CENTER LINE OF U153-5	
U174-1	U216-13	
U215-6	U174-4	
U112-12	U216-11	
U150-11	U1-2-1 & 2	
U150-10	U171-9	
R105	U215-6	SLEEVE LEADS USING 669-0122 AS REQD
R105	U217-14 (5V)	
J1-B10	J2-B1	
U215-5	U171-8	
U64-1	U1-8	
U64-6	U84-1	

PERTEC BUFFER 101811-

TP8 GND

TP12 REF

TP1 +20V

TP2 +15V

TP3 GND

TP4 GND

TP5 GND

TP6 +5V

TP7 GND

TP9 GND

TP10 GND

TP11 OSC

W14 E34 W12 E35 E36
W20 E31 W19 E32 E33
W18 E28 W17 E29 E30
W16 E25 W15 E26 E27

101811 01F +ECN'S 6160, 6194, 6236, 6561, 6722, 6831, 6916
02F
03F
101811 04E +ECN'S 6160, 6194, 6236, 6561, 6722, 6831, 6916

DETAIL B

E15 W2 E16
E13 W1 E14
E11 W3 E12
E9 W4 E10
E7 W6 E8
E5 W8 E6
E3 W5 E4
E1 W7 E2

E18 E20 E22 E24
W9 W10 W11 W12
E17 E19 E21 E23

E35 W13 E34 W14 E36
E32 W19 E31 W20 E33
E29 W17 E26 W18 E30
E26 W15 E25 W16 E27

101811-01 K & SUBS 02K 03K
101811-04 J & SUBS

DETAIL C

FOR SPECIFICATION SEE 101814.
FOR ASSY VERSION INFORMATION SEE SCHEMATIC 101810.

PART NO 101811-02 REV V1

101350-01
615-9758 4 REQD
INSERT RIVET THIS SIDE

DETAIL A
SCALE: 4/1

PIN 1 TYP FOR ALL INTEGRATED CIRCUITS

SEE REWORK INSTRUCTIONS (ETCH CUTS)

SEE REWORK INSTRUCTIONS (ETCH CUTS)

DRILL .031 +.004 -.001 DIA 2 PLACES (SEE REWORK INSTRUCTIONS)
(NOTE: DRILL HOLES BEING SURE TO CLEAR CIRCUITRY BOTH SIDES OF BOARD)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .01, .XXX ± .005, X ± 1/64, ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

SIGNATURES	DATE
DWN	
CHK	
ENGR	
PROJ. ENGR	

PERTEC PERIPHERAL EQUIPMENT

TITLE: PCBA BUFFER

NEXT ASSY | 1ST USED ON | APPLICATION

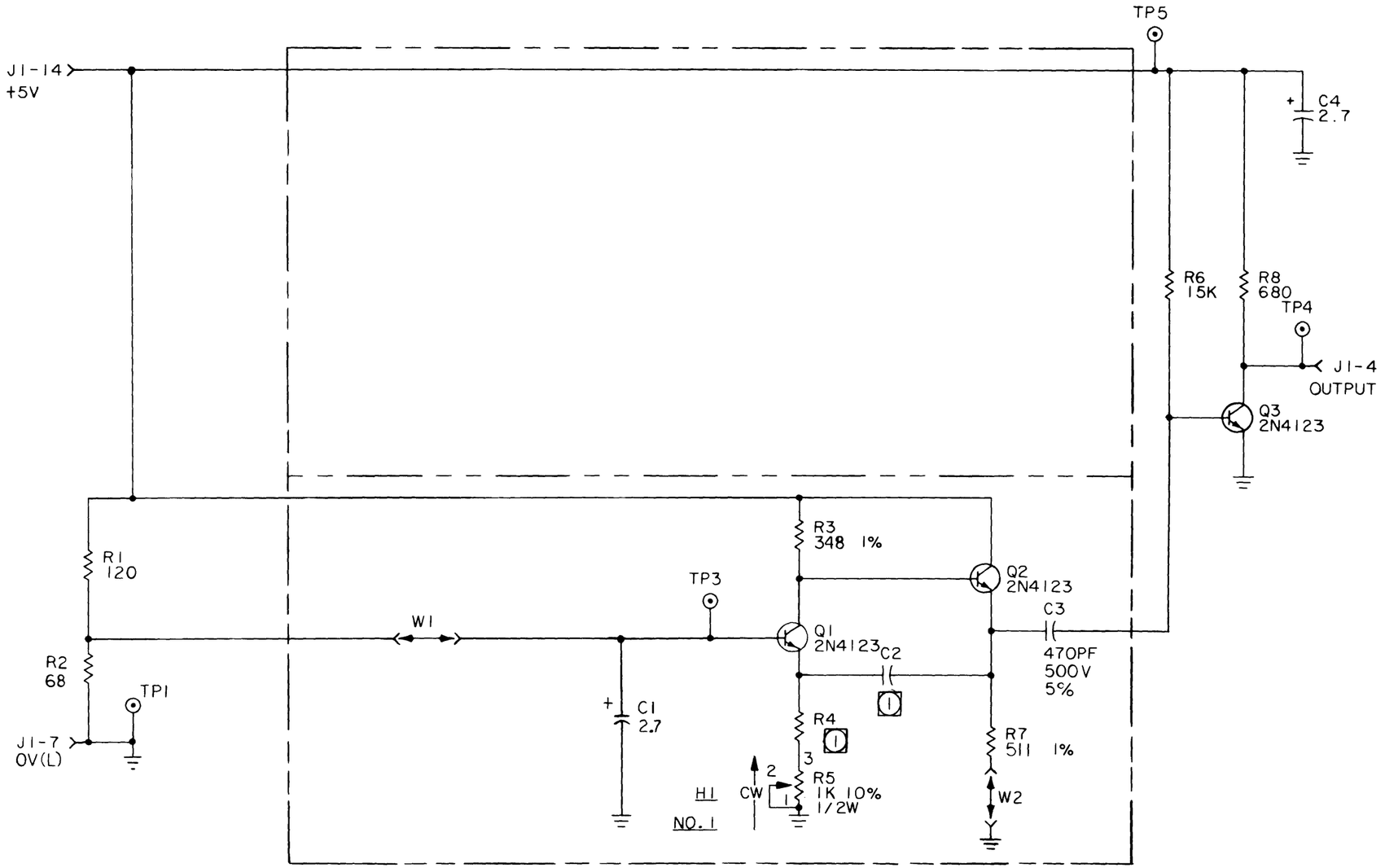
FINISH:

MATL: SEE LM

SIZE	CODE IDENT NO.	DWG NO.	REV
J		101811	V

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BW	18 Feb 1971			
B	ECN 4469	11-8-72			
C	ECN 5157	1/16/73			
C1	ECN 5289	7/9/73			



VERSION TABLE (1)			
DASH NO.	TAPE SPEED (IPS) NRZ / PE	R4, 1%	C2, 100V, 10%
-01	3.75<4.75 / 4.75<7	1330	.01
-02	4.75<7 / 7<9	619	.01
-03	7<9 / 9<13	1000	.0068
-04	9<13 / 13<18	1000	.0047
-05	13<18 / 18<26	1000	.0033
-06	18<26 / 26<33	1000	.0022
-07	26<33 / 33<42	1330	.0015
-08	33<42 / 42<55	1000	.0015
-09	42<55 / 55<85	1000	.001
-10	55<85 / 85<125	511	.001

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C4	
Q3	
R8	
W2	
TP5	TP2

5. ALL CAPACITOR VALUES ARE IN MICROFARADS, 35V, 20%.
4. ALL RESISTOR VALUES ARE IN OHMS, 1/4W 5%.
3. FOR ASSEMBLY DRAWING SEE 102096.
2. FOR SPECIFICATION SEE 101360.
(1) SEE VERSION TABLE FOR VALUE.

NOTES: UNLESS OTHERWISE SPECIFIED.

102096	1600
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
X ± 1/32
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX. .010

FINISH:

MATL:

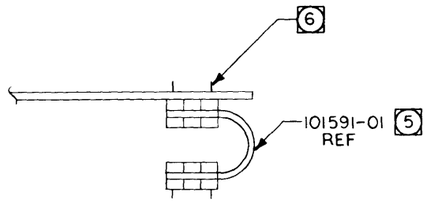
SIGNATURES	DATE
DR	18 FEB 1971
CHK	2/1/71
DES	
ENGR	2/9/71
ENGR	

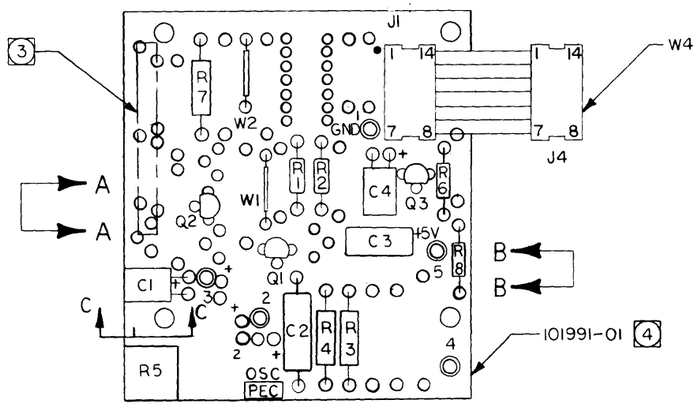
PEC PERIPHERAL EQUIPMENT CORPORATION

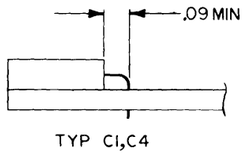
TITLE
SCHEMATIC — SINGLE FIXED OSCILLATOR

SIZE	CODE IDENT NO	DWG NO.	REV
D		102095	C1
SCALE NONE	DO NOT SCALE DWG	SHEET 1 OF 1	

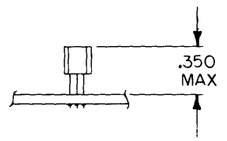
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BW	3/8/71	[illegible]	[illegible]	[illegible]
B	ECN 2483	5/4/71	TB	[illegible]	[illegible]
C	ECN 4469	11-6-72	[illegible]	[illegible]	[illegible]
D	ECN 5157	5-16-73	CW.	[illegible]	[illegible]
E	ECN 6056	5/29/74	[illegible]	[illegible]	CCB



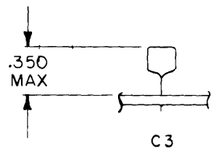




VIEW C-C
SCALE 4/1



VIEW A-A
ROTATED 90° CCW



VIEW B-B
ROTATED 90° CW

(7) TABLE I

PART NO.	REF. DES.
100-1535	R6
100-6815	R8
100-1215	R1
100-6805	R2
104-3480	R3
104-5110	R7
126-1020	R5
132-2752	C1,4
130-4715	C3
200-4123	Q1,2,3
100373-02	W1,2
101591-01	W4

(8) TABLE II

DASH NO.	TAPE SPEED (IPS) NRZ	TAPE SPEED (IPS) PE	R4	C2
-01	3.75<4.75	4.75<7	104-1331	131-1030
-02	4.75<7	7<9	104-6190	131-1030
-03	7<9	9<13	104-1001	131-6820
-04	9<13	13<18	104-1001	131-4720
-05	13<18	18<26	104-1001	131-3320
-06	18<26	26<33	104-1001	131-2220
-07	26<33	33<42	104-1331	131-1520
-08	33<42	42<55	104-1001	131-1520
-09	42<55	55<85	104-1001	131-1020
-10	55<85	85<125	104-5110	131-1020

(8) FOR PART NO.'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.
(7) FOR PART NO.'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.
(6) CLIP LEADS AFTER WAVE SOLDERING. ALL LEADS SHALL EXTEND A MAXIMUM OF .045 INCH THRU BOARD.
(5) BEND CABLE APPROXIMATELY AS SHOWN BEFORE WAVE SOLDERING.
(4) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101991-01 REV "C" AND SUBSEQUENT.
(3) RUBBER STAMP PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MFG METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC-102095.
SPECIFICATION-101360.

NOTES: UNLESS OTHERWISE SPECIFIED.

TOP ASSY	1600
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

FINISH:

MATL:

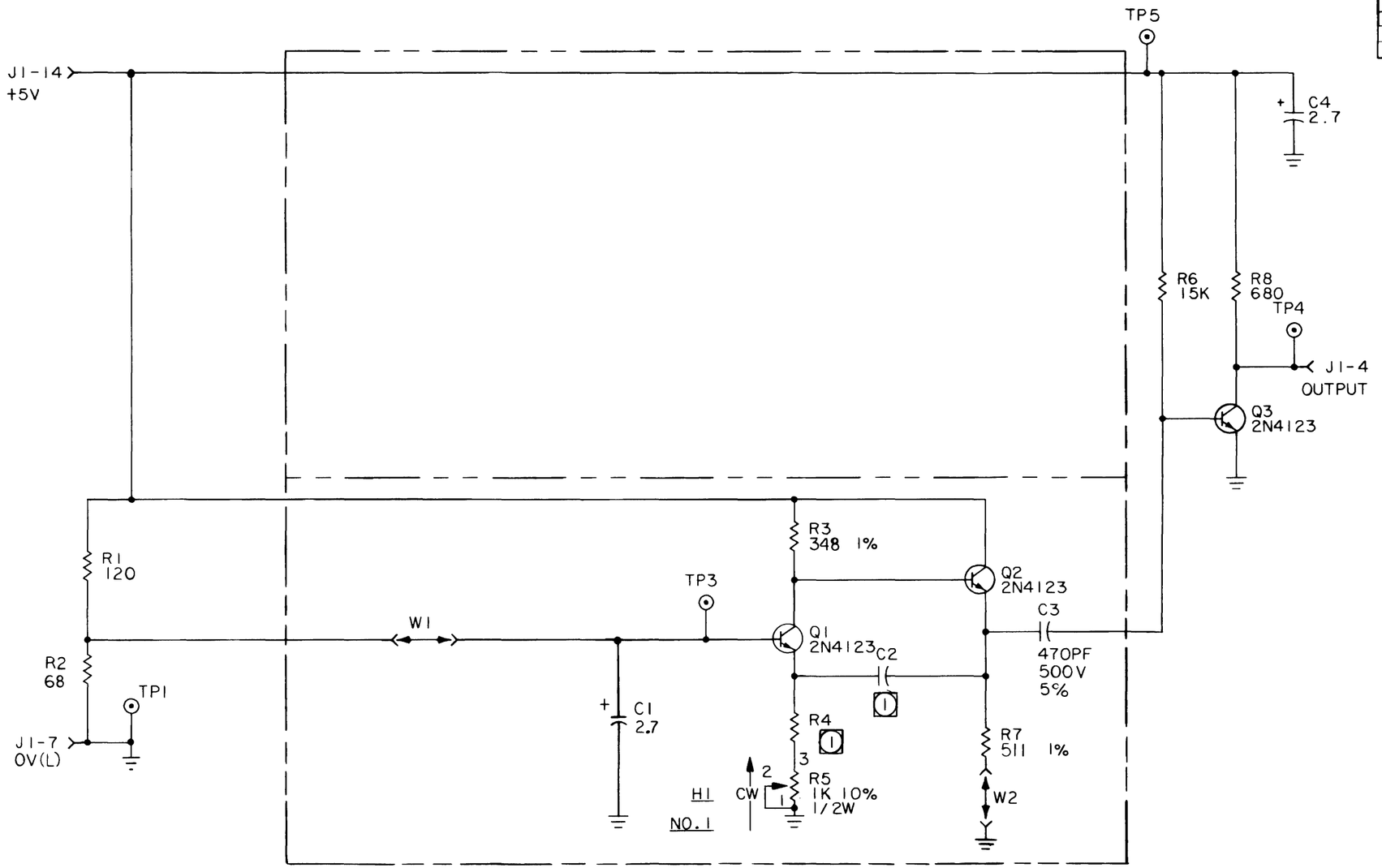
SIGNATURES		DATE
DR	[illegible]	2/9/71
CHK	[illegible]	2/24/71
DES		
ENGR	[illegible]	2/9/71
ENGR		

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
PCBA-
SINGLE FIXED
OSCILLATOR

SIZE	CODE IDENT. NO.	DWG NO.	REV
D		102096	E
SCALE 2/1	DO NOT SCALE DWG	SHEET 1 OF 1	

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BW	18 Feb 1971			
B	ECN 4469	11-8-72			
C	ECN 5157	1/4/73			
C1	ECN 5289	11/9/73			



VERSION TABLE (1)			
DASH NO.	TAPE SPEED (IPS) NRZ / PE	R4, 1%	C2, 100V, 10%
-01	3.75<4.75 / 4.75<7	1330	.01
-02	4.75<7 / 7<9	619	.01
-03	7<9 / 9<13	1000	.0068
-04	9<13 / 13<18	1000	.0047
-05	13<18 / 18<26	1000	.0033
-06	18<26 / 26<33	1000	.0022
-07	26<33 / 33<42	1330	.0015
-08	33<42 / 42<55	1000	.0015
-09	42<55 / 55<85	1000	.001
-10	55<85 / 85<125	511	.001

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C4	
Q3	
R8	
W2	
TP5	TP2

5. ALL CAPACITOR VALUES ARE IN MICROFARADS, 35V, 20%.
4. ALL RESISTOR VALUES ARE IN OHMS, 1/4W 5%.
3. FOR ASSEMBLY DRAWING SEE 102096.
2. FOR SPECIFICATION SEE 101360.
(1) SEE VERSION TABLE FOR VALUE.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X/X ± 1/33
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES		DATE
DR		18 FEB 1971
CHK		3/9/71
DES		
ENGR		3/9/71
ENGR		

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
SCHEMATIC — SINGLE FIXED OSCILLATOR

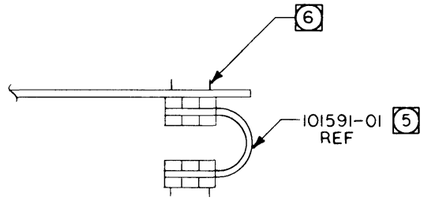
102096	1600
NEXT ASSY	USED ON
APPLICATION	

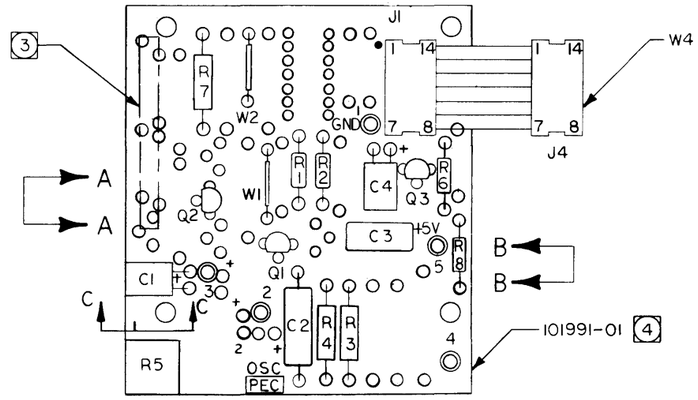
FINISH:

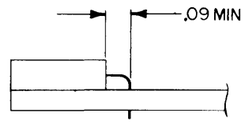
MATL:

SIZE	CODE IDENT NO	DWG NO.	REV
D		102095	C1
SCALE NONE	DO NOT SCALE DWG	SHEET 1 OF 1	

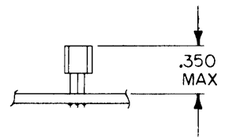
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BW	3/6/71	JHR	AG	KG
B	ECN 2483	5/10/71	TB	AG	JHR
C	ECN 4469	11-6-72	JHR	JHR	GDB
D	ECN 5157	5-16-73	CW.	KP	WCB
E	ECN 6056	3/27/74	JHR	KP	WCB



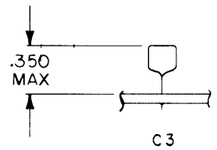




VIEW C–C
SCALE 4/1



VIEW A–A
ROTATED 90° CCW



VIEW B-B
ROTATED 90° CW

7 TABLE I

PART NO.	REF. DES.
100-1535	R6
100-6815	R8
100-1215	R1
100-6805	R2
104-3480	R3
104-5110	R7
126-1020	R5
132-2752	C1,4
130-4715	C3
200-4123	Q1,2,3
100373-02	W1,2
101591 -01	W4

8 TABLE II

DASH NO.	TAPE SPEED (IPS) NRZ	TAPE SPEED (IPS) PE	R4	C2
-01	3.75<4.75	4.75<7	104-1331	131-1030
-02	4.75<7	7<9	104-6190	131-1030
-03	7<9	9<13	104-1001	131-6820
-04	9<13	13<18	104-1001	131-4720
-05	13<18	18<26	104-1001	131-3320
-06	18<26	26<33	104-1001	131-2220
-07	26<33	33<42	104-1331	131-1520
-08	33<42	42<55	104-1001	131-1520
-09	42<55	55<85	104-1001	131-1020
-10	55<85	85<125	104-5110	131-1020

8. FOR PART NO.'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.
7. FOR PART NO.'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.
6. CLIP LEADS AFTER WAVE SOLDERING. ALL LEADS SHALL EXTEND A MAXIMUM OF .045 INCH THRU BOARD.
5. BEND CABLE APPROXIMATELY AS SHOWN BEFORE WAVE SOLDERING.
4. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101991-01 REV "C" AND SUBSEQUENT.
3. RUBBER STAMP PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MFG METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC-102095. SPECIFICATION-101360.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
X/X ± 1/32
ANGULAR ± ½°
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES		DATE
DR	L.S. Reese	3/19/71
CHK	Geo Adams	3/24/71
DES		
ENGR	R. Johnson	3/1/71
ENGR		

PEC PERIPHERAL EQUIPMENT CORPORATION

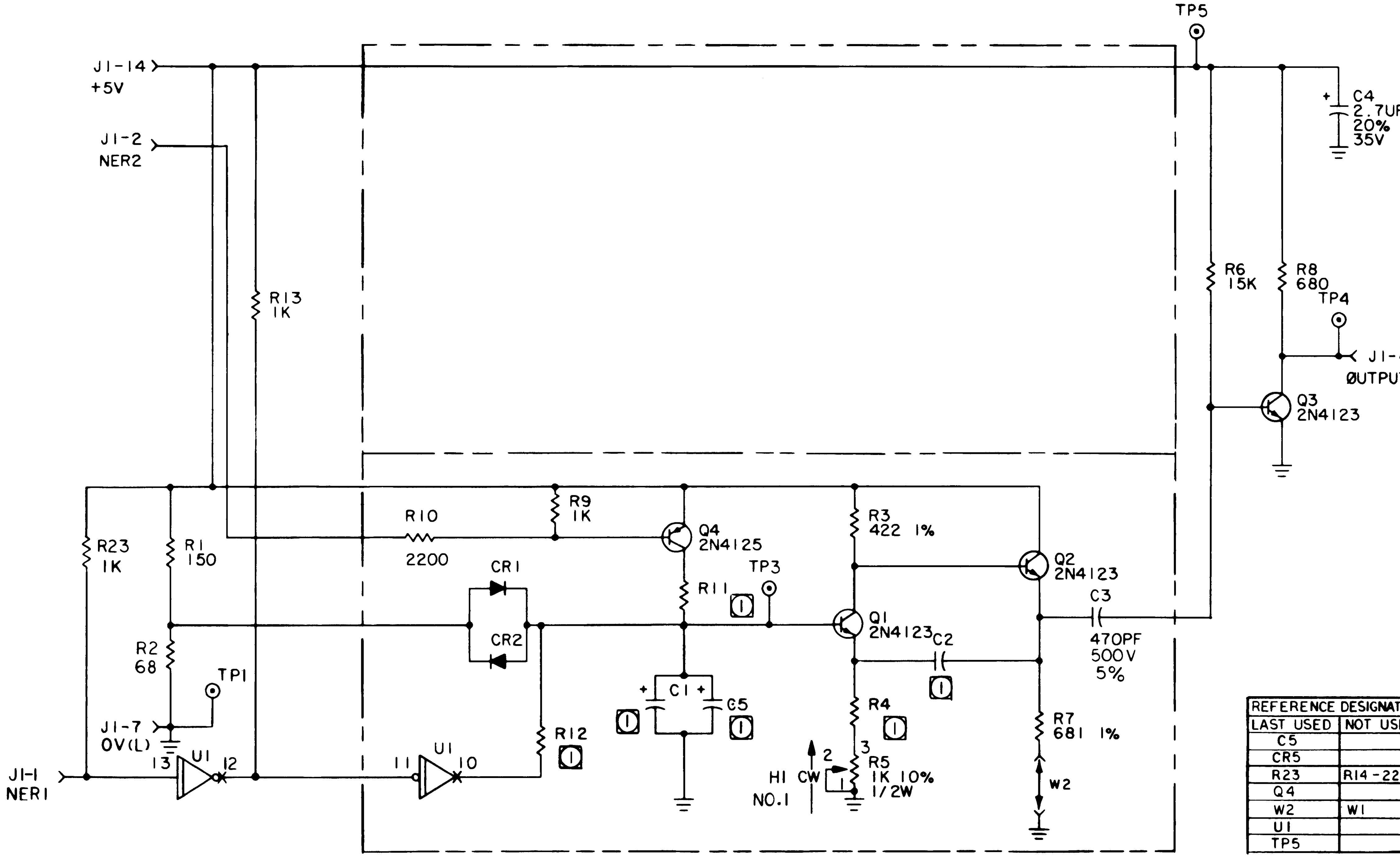
TITLE
PCBA-
SINGLE FIXED
OSCILLATOR

TOP ASSY	1600
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:
MATL:

SIZE D | CODE IDENT. NO. | DWG NO. 102096 | REV E
SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 38V				
A1	ECN 5282				



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C5	
CR5	
R23	R14-22
Q4	
W2	W1
U1	
TP5	

(1) VERSIONS

DASH NO.	PE TAPE SPEEDS (IPS)	R4 (1%)	R11 (1%)	R12 (1%)	C2 500V,5%	C2 100V,10%	C1 35V,20%	C1 6V,20%	C5 35V,20%
-01	31<40	1330	1620	750	330PF	—	2.7UF	—	2.7 UF
-02	24<31	1470	2370	1100	470PF	—	2.7 UF	—	2.7 UF
-03	14.5<22	750	825	383	—	.001UF	—	22UF	—
-04	11<14.5	825	1210	562	—	.0015UF	—	22UF	—
-05	7.5<11	1000	1470	681	—	.0015UF	—	22UF	—
-06	5<7.5	1000	2370	1100	—	.0022UF	—	22UF	—
-07	40<56	909	1470	681	330 PF	—	2.7UF	—	2.7UF
-08	56<90	825	825	383	220PF	—	2.7UF	—	2.7 UF
-09	22<24	1780	2610	1210	470PF	—	2.7UF	—	2.7 UF

5. ALL DIODES ARE PEC PART NO 300-4446.
4. U1 IS PEC PART NO 700-7416.
3. ALL RESISTORS IN OHMS, 1/4 W, 5 %.
2. FOR ASSY SEE DRAWING NO. 102094. FOR SPECIFICATION SEE DRAWING NO. 101397.
(1) SEE VERSION TABLE FOR VALUES.

NOTES: UNLESS OTHERWISE SPECIFIED

102094	1600
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010
.XXX ± .005
X/X ± 1/32
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX. .010

FINISH:

MATL:

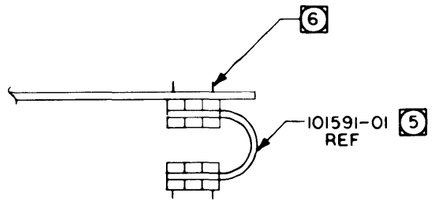
SIGNATURES	DATE
DR	2/23/71
CHK	3/9/71
DES	
ENGR K. Johnson	3/9/71
ENGR	

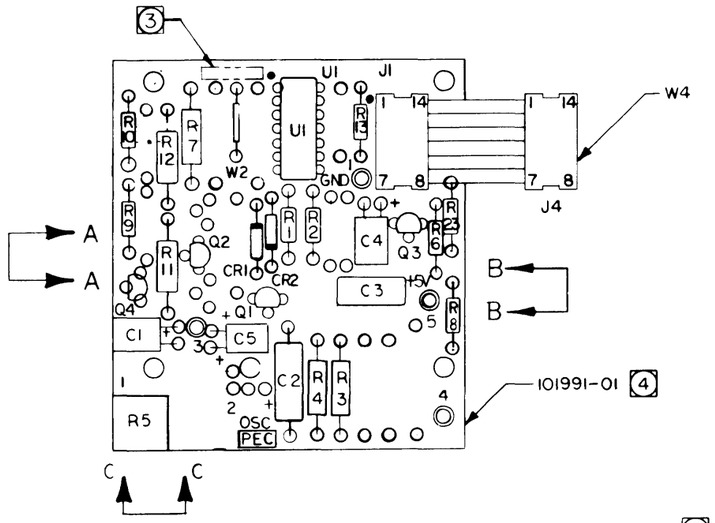
PEC PERIPHERAL EQUIPMENT CORPORATION

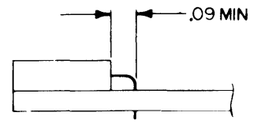
TITLE
SCHEMATIC - SINGLE TRACKING OSCILLATOR

SIZE D | CODE IDENT. NO. | DWG NO. 102093 | REV A1
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

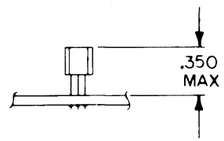
REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3BV	10/5/71	HLR	JC	
B	ECN 3346	8-21-72	JC		
B_1	ECN 5282	7/9/73			
C	ECN 6056	8/27/74			



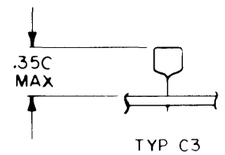




TYP C1, C4 & C5
VIEW C–C
SCALE 4/1
R5 REMOVED FOR CLARITY



VIEW A–A
ROTATED 90° CCW



TYP C3
VIEW B–B
ROTATED 90° CW

7 TABLE I

PART NO.	REF. DES.
100-1025	R9,13,23
100-1535	R6
100-6815	R8
100-1515	R1
100-6805	R2
104-4220	R3
104-6810	R7
100-2225	R10
126-1020	R5
132-2752	C4
130-4715	C3
300-4446	CR1,2
200-4125	Q4
200-4123	Q1,2,3
700-7416	U1
100373-02	W2
101591-01	W4

8 TABLE II

DASH NO.	PE TAPE SPEEDS (IPS)	R4	R11	R12	C1	C2	C5
-01	31 < 40	104-1331	104-1621	104-7500	132-2752	130-3315	132-2752
-02	24 < 31	104-1471	104-2371	104-1101	132-2752	130-4715	132-2752
-03	14.5 < 22	104-7500	104-8250	104-3830	132-2262	131-1020	——
-04	11 < 14.5	104-8250	104-1211	104-5620	132-2262	131-1520	——
-05	7.5 < 11	104-1001	104-1471	104-6810	132-2262	131-1520	——
-06	5 < 7.5	104-1001	104-2371	104-1101	132-2262	131-2220	——
-07	40 < 56	104-9090	104-1471	104-6810	132-2752	130-3315	132-2752
-08	56 < 90	104-8250	104-8250	104-3830	132-2752	130-2215	132-2752
-09	22 < 24	104-1781	104-2611	104-1211	132-2752	130-4715	132-2752

8. FOR PART NO.'S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.
7. FOR PART NO.'S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.
6. CLIP LEADS AFTER WAVE SOLDERING. ALL LEADS SHALL EXTEND A MAXIMUM OF .045 INCH THRU BOARD.
5. BEND CABLE APPROXIMATELY AS SHOWN BEFORE WAVE SOLDERING.
4. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101991-01 REV "C" AND SUBSEQUENT.
3. RUBBER STAMP PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MFG METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC-102093.
SPECIFICATION-101397.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X ± 1/64 X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR [illegible]	3/24/72
CHK [illegible]	3-4-72
DES	
ENGR R. Johnson	3/4/72
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
PCBA-
SINGLE TRACKING
OSCILLATOR

TOP ASSY	1600
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:
MATL:

SIZE D | CODE IDENT NO | DWG NO. 102094 | REV C
SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

POWER SUPPLY ASSEMBLY 103314
WIRE LIST 103318

PCBA 103305

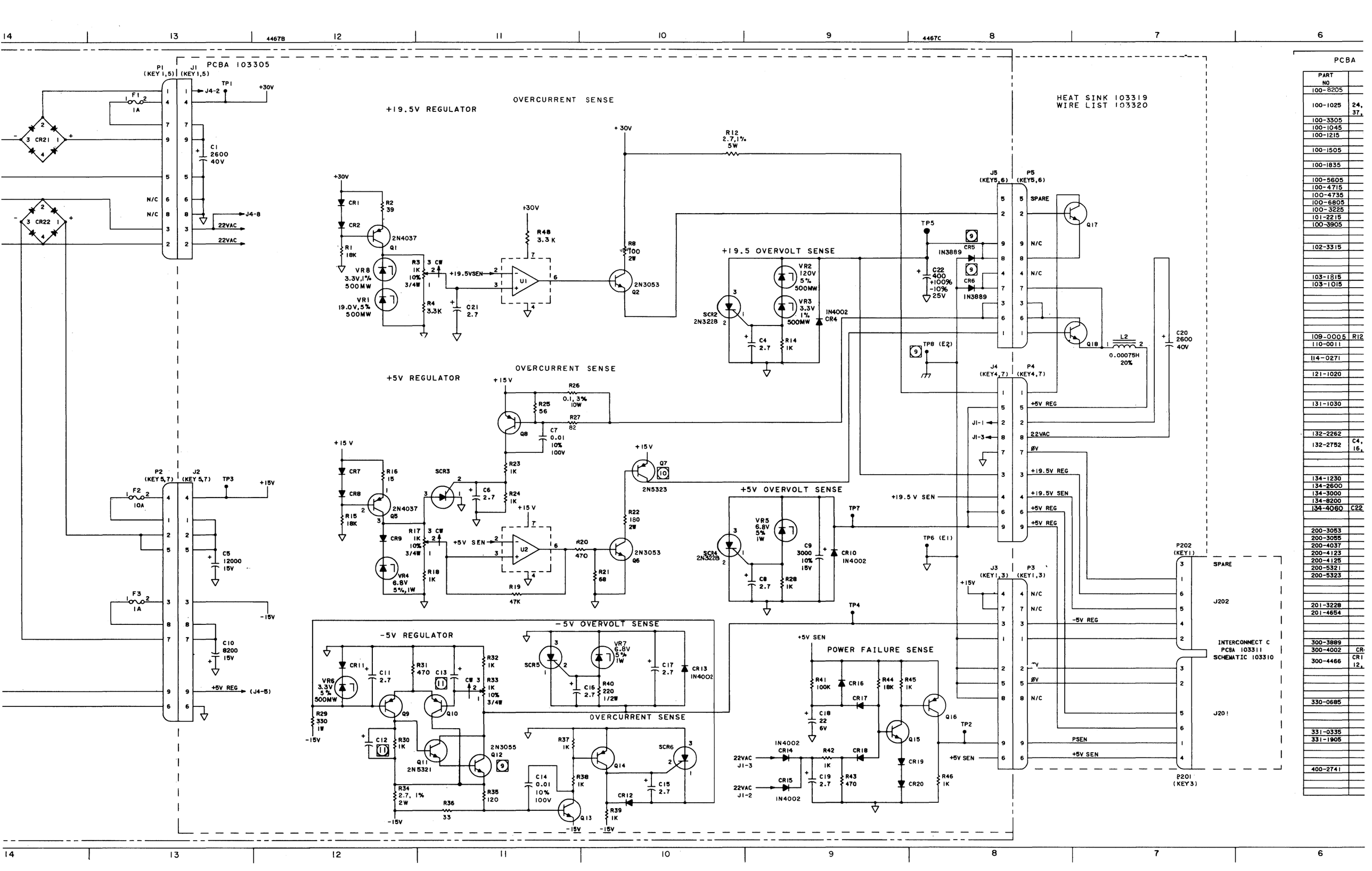
TABLE II (2)

TRANSFORMER PRIMARY CONNECTIONS			
LINE VOLTS	LINE INPUT	JUMPER	
100	2 AND 7	2 TO 6	3 TO 7
115	2 AND 8	2 TO 6	4 TO 8
125	1 AND 8	1 TO 5	4 TO 8
200	2 AND 7	3 TO 6	
210	1 AND 7	3 TO 6	
220	1 AND 7	3 TO 5	
230	2 AND 8	4 TO 6	
240	1 AND 8	4 TO 6	
250	1 AND 8	4 TO 5	

+19.5V REGULATOR

+5V REGULATOR

-5V REGULATOR



PCBA

PART NO	
100-8205	
100-1025	24, 37,
100-3305	
100-1045	
100-1215	
100-1505	
100-1835	
100-5605	
100-4715	
100-4735	
100-6805	
100-3225	
101-2215	
100-3905	
102-3315	
103-1815	
103-1015	
109-0005	R12
110-0011	
114-0271	
121-1020	
131-1030	
132-2262	
132-2752	C4, 16,
134-1230	
134-2600	
134-3000	
134-8200	
134-4060	C22
200-3053	
200-3055	
200-4037	
200-4123	
200-4125	
200-5321	
200-5323	
201-3228	
201-4654	
300-3889	
300-4002	CR
300-4466	CRI 12,
330-0685	
331-0335	
331-1905	
400-2741	

HEAT SINK 103319
WIRE LIST 103320

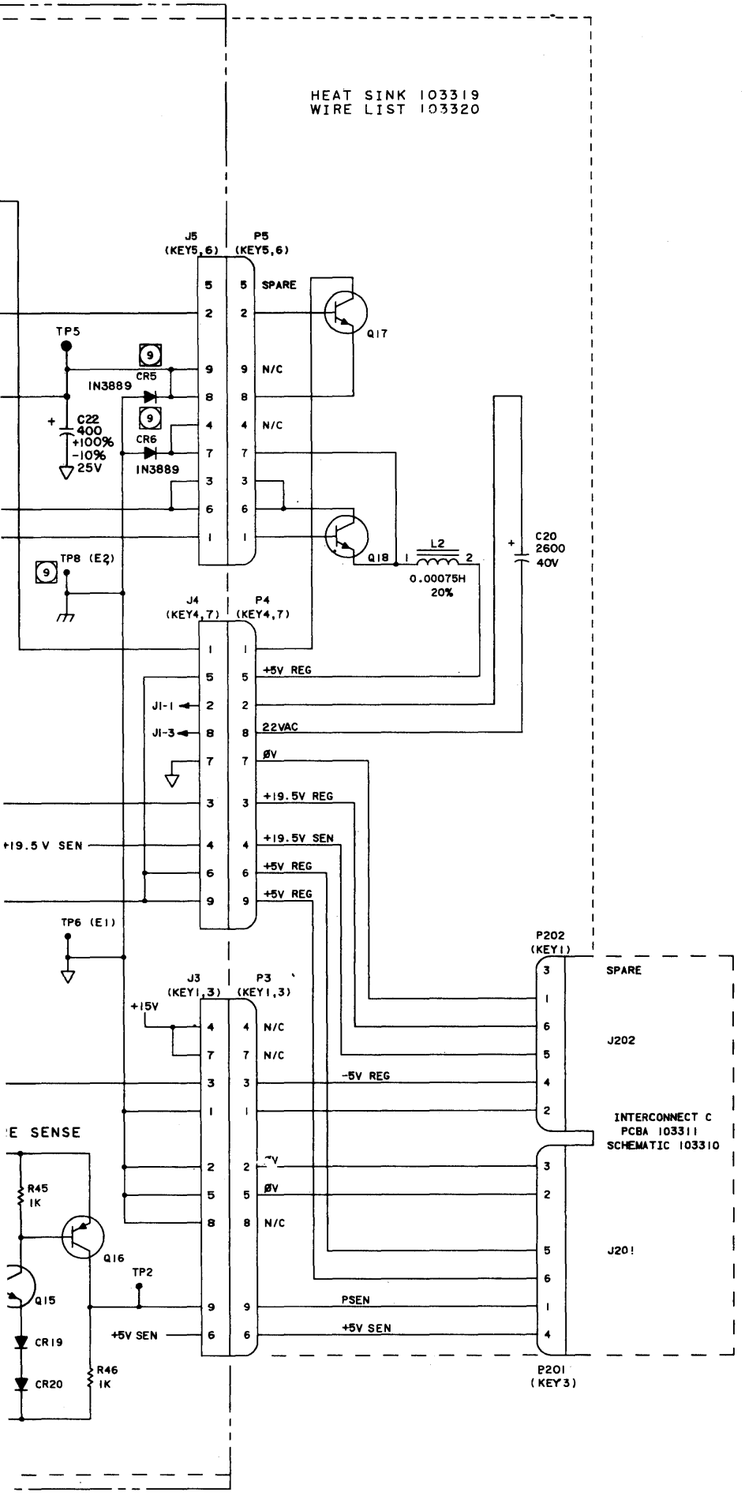


TABLE I (1)

PCBA 103305

PART NO	REF DESIGNATION
100-8205	R27
100-1025	R14,18,23, 24,28, 30,32, 37,38,39,42,45,46
100-3305	R36
100-1045	R41
100-1215	R35
100-1505	R16
100-1835	R1, 15, 44
100-5605	R25
100-4715	R20, 31, 43
100-4735	R19
100-6805	R21
100-3225	R4,48
101-2215	R40
100-3905	R2
102-3315	R29
103-1815	R22
103-1015	R8
109-0005	R12
110-0011	R26
114-0271	R34
121-1020	R3,17,33
131-1030	C7,14
132-2262	C18
132-2752	C4, 6, 8, 11, 15, 16,17,19,21
134-1230	C5
134-2600	C1
134-3000	C9
134-8200	C10
134-4060	C22
200-3053	Q2,6
200-3055	Q12
200-4037	Q1,5
200-4123	Q13,15
200-4125	Q8,9,10,14,16
200-5321	Q11
200-5323	Q7
201-3228	SCR2,4
201-4654	SCR3,5,6
300-3889	CR5,6
300-4002	CR4,10,13,14,15
300-4466	CR1,2, 7,8,9,11, 12,16,17,18,19,20
330-0685	VR4,5,7
331-0335	VR3,8,6
331-1905	VR1,2
400-2741	U1,2

POWER SUPPLY ASSY 103314

PART NO	REF DESIGNATION
320-9802	CR21, 22
506-0808	S1
511-0003	T1
OR/511-6800	T1
663-3010	F1, 3
663-3100	F2
663-3520	F4

HEAT SINK 103319

PART NO	REF DESIGNATION
134-2600	C20
200-3771	Q17, 18
515-0750	L2

REFERENCE DESIGNATIONS

LAST USED	DELETED
C22	C2,3
CR22	
F4	
L2	L1
Q18	Q3,4
R48	R 5,6,7,9,10,11,13,47
S1	
SCR6	SCR1
T1	
U2	
VR8	
TP7	

(11) C12 AND C13 ARE NOT USED IN PRESENT VERSION, PROVISION FOR FUTURE USAGE HAS BEEN MADE.

(10) TOP HAT HEAT SINK REQUIRED.

(9) PART IS MOUNTED ON HEAT SINK.

8. ALL FUSES ARE FAST BLOW (F.B.).

7. ALL DIODES ARE 1N4446

6. ALL PNP TRANSISTORS ARE 2N4125.

5. ALL NPN TRANSISTORS ARE 2N4123.

4. ALL CAPACITOR VALUES ARE IN MICROFARADS, 20%, 35V.

3. ALL RESISTOR VALUES ARE IN OHMS, 5%, 1/4W.

(2) TRANSFORMER PRIMARY CONNECTIONS SHOWN FOR 115V LINE VOLTAGE.
FOR OTHER LINE VOLTAGE SEE TABLE II

(1) FOR VALUE, PART NO. OR USAGE OF COMPONENTS SEE TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 5-PV PROD. RELEASE	11/6/73	RAS		
B	ECN 5904	12/17/73	C.J.		
C	ECN 6064	2/14/74			
D	ECN 6079	3/22/74			
E	ECN 6199	4/26/74			
F	ECN 7319	4/29/75			
G	ECN 7476	10/21/75	W.L.S.		
H	ECN 7715	8-20-76	DMP		

INTERCONNECT C 103311
HEAT SINK 103319
BUFFER POWER SUPPLY 103305
REFERENCE DRAWINGS :

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ±
.XXX ±
X
X ±
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES		DATE
DR. COMPUTER		9-73
CHK		10/9/73
DES		
ENGR		10/19/73
PROJ. ENGR		10/19/73

NEXT ASSY | 1RT USED ON
APPLICATION

FINISH:
MATL:

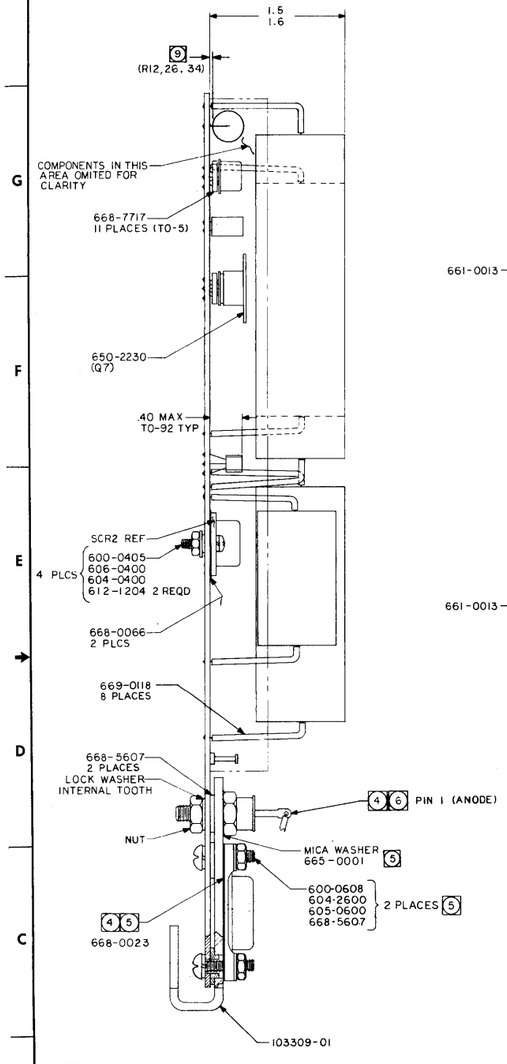
PERTEC PERIPHERAL EQUIPMENT

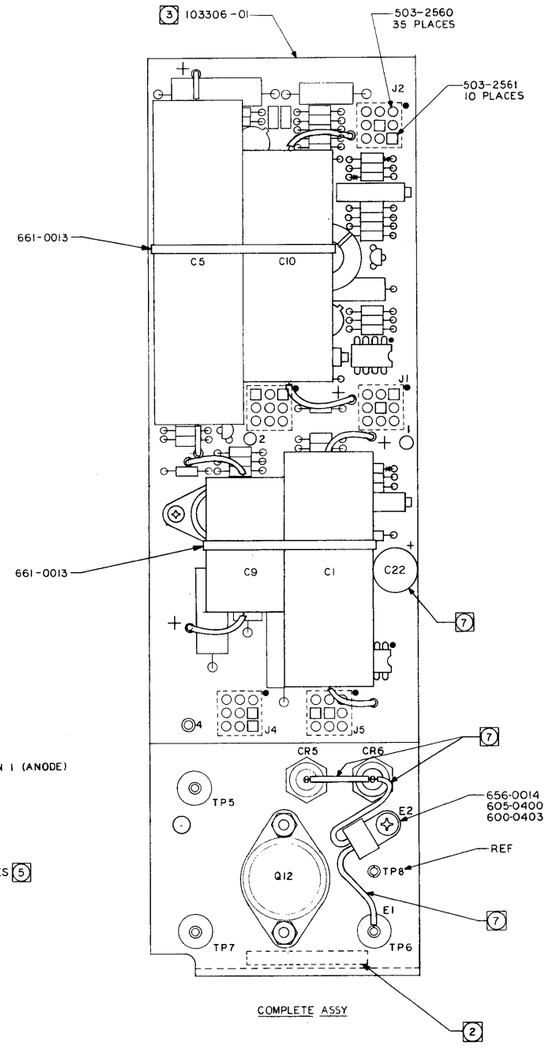
TITLE
SCHEMATIC, BUFFER POWER SUPPLY

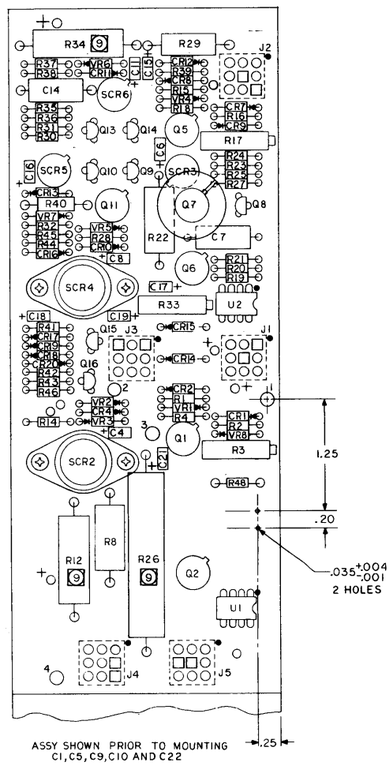
SIZE	CODE IDENT NO.	DWG NO.	REV
H		103304	H

SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	GEN S-DY PRODUCTION RELEASE	4-21-72	[illegible]	[illegible]	[illegible]
B	ECN 5904	1-16-74	C.J.	[illegible]	[illegible]
C	ECN 6064	[illegible]	[illegible]	[illegible]	[illegible]
D	ECN 6079	[illegible]	[illegible]	[illegible]	[illegible]
E	ECN 6199	[illegible]	[illegible]	[illegible]	[illegible]
F	ECN 7319	[illegible]	SDL	[illegible]	[illegible]







7 WIRE CHART			
FROM	TO	WIRE P/N	SLEEVING P/N
E1	E2	695-0018	669-0118
E2	CR6-1	695-0018	669-0118
CR6-1	CR5-1	695-0018	669-0118
10 C22 (+)	VR2-C	695-0018	669-0018
10 C22 (−)	CR4-A	695-0018	669-0018

10 CONNECT JUMPER WIRES FROM C22 ON CIRCUIT SIDE.

9 3/16 MIN AIR GAP BETWEEN RESISTOR BODY AND BOARD
8. FOR ASSY VERSION INFORMATION SEE SCHEMATIC 103304.

7 FOR CONNECTION SEE WIRE CHART.

6 MOUNTING HARDWARE INCLUDED WITH COMPONENTS CR5 & CR6. ASSEMBLE AS INDICATED USING ONLY PARTS SHOWN.

5 APPLY 665-0001 (SILICONE GREASE) TO BOTH SIDES OF MICA WASHER • A MIN OF 90% COVERAGE IS REQUIRED. ALL SCREWS (600-0608) MUST BE TORQUED TO 11 IN. LBS.

4 BEFORE INSTALLING CR5, CR6 AND Q12 TO HEATSINK, EXTREME CARE MUST BE TAKEN TO SEE THAT ALL BURRS AND MISC CHIPS OF METAL ARE REMOVED FROM ENTIRE MOUNTING SURFACE.

3 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 103306-01 REV C AND SUBSEQUENT.

2 RUBBER STAMP ASSY PART NO. 103305 INCLUDING VERSION NO. AND VERSION ISSUE LETTER.

1. ASSEMBLE PER STANDARD MANUFACTURING METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED.

SPECIFICATION 103308
SCHEMATIC 103304
REF DRAWINGS:
PART NO. 103305-01 REV K

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± —
.XXX ± —
FRACTIONS ± —
ANGULAR ± —
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES	DATE
DR. [illegible]	7-24-72
CHK. [illegible]	7/24/72
DES. [illegible]	7-24-72
ENGR. [illegible]	7/24/72
PROJ. ENGR. [illegible]	7/24/72

PERTEC PERIPHERAL EQUIPMENT

TITLE: PCBA BUFFER POWER SUPPLY

103314	
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH: [illegible]
MATL: SEE L/M

SIZE	CODE IDENT NO.	DWG NO.	REV
E		103305	F

SCALE 2:1 DO NOT SCALE DWG SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 5-PB PROD RELEASE	8-27-73	C.J.	JBB	WLS

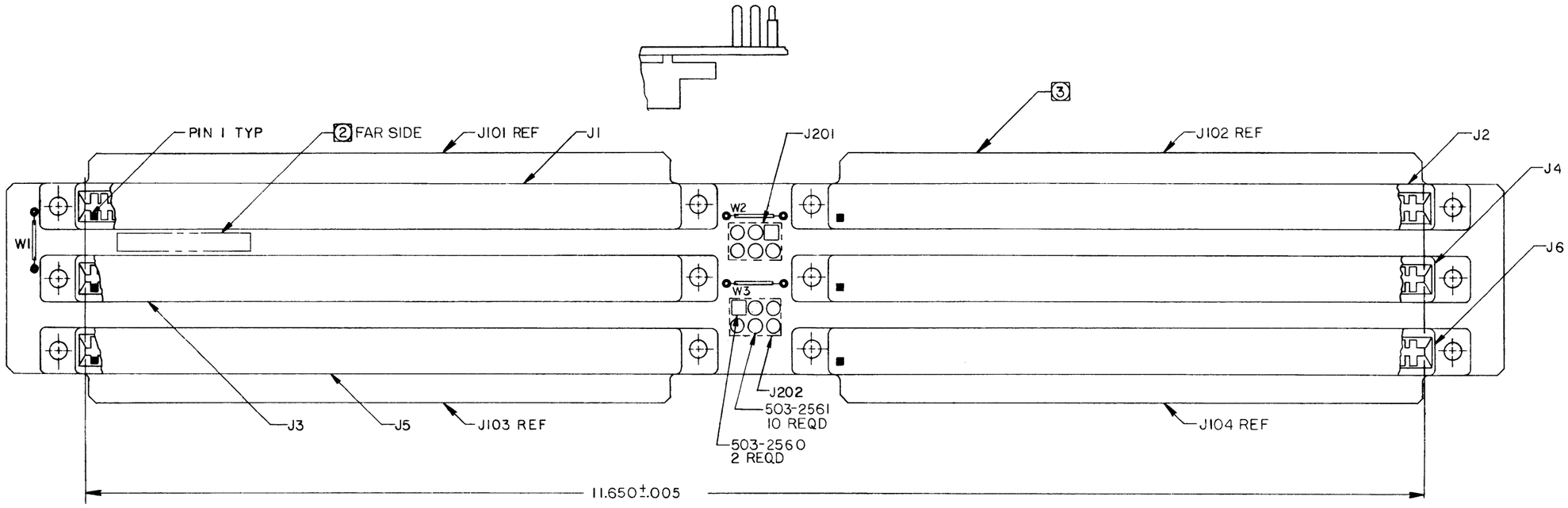


TABLE I [4]

ASSEMBLY 103311 VERSION NO.	W1, W2, W3
-01	USE
-02	OMIT

[4] FOR USAGE OF COMPONENTS AFFECTED BY VERSION NO., SEE TABLE I.
[3] THIS ASSY SHALL BE MADE FROM PROCESS BOARD 103312-01 REV A AND SUBSEQUENT.
[2] MARK PART NO. 103311 INCLUDING VERSION NO. AND VERSION ISSUE LETTER.
1. ASSEMBLE PER STANDARD MFG METHODS.
NOTES: UNLESS OTHERWISE SPECIFIED.

SCHEMATIC 103310
REF DRAWINGS:

PART NO. 103311-01 REV A

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± ANGULAR
.XXX ± ± 1/2°
X
X ±
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES	DATE
DR. Caroline Jones	8/24/73
CHK James B Bauer	8/24/73
DES J. R. Palmer	8/24/73
ENGR	
PROJ. ENGR W. L. Shaw	9/4/73

PERTEC PERIPHERAL EQUIPMENT

TITLE
PCBA
INTERCONNECT C

TOP ASSY	
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:

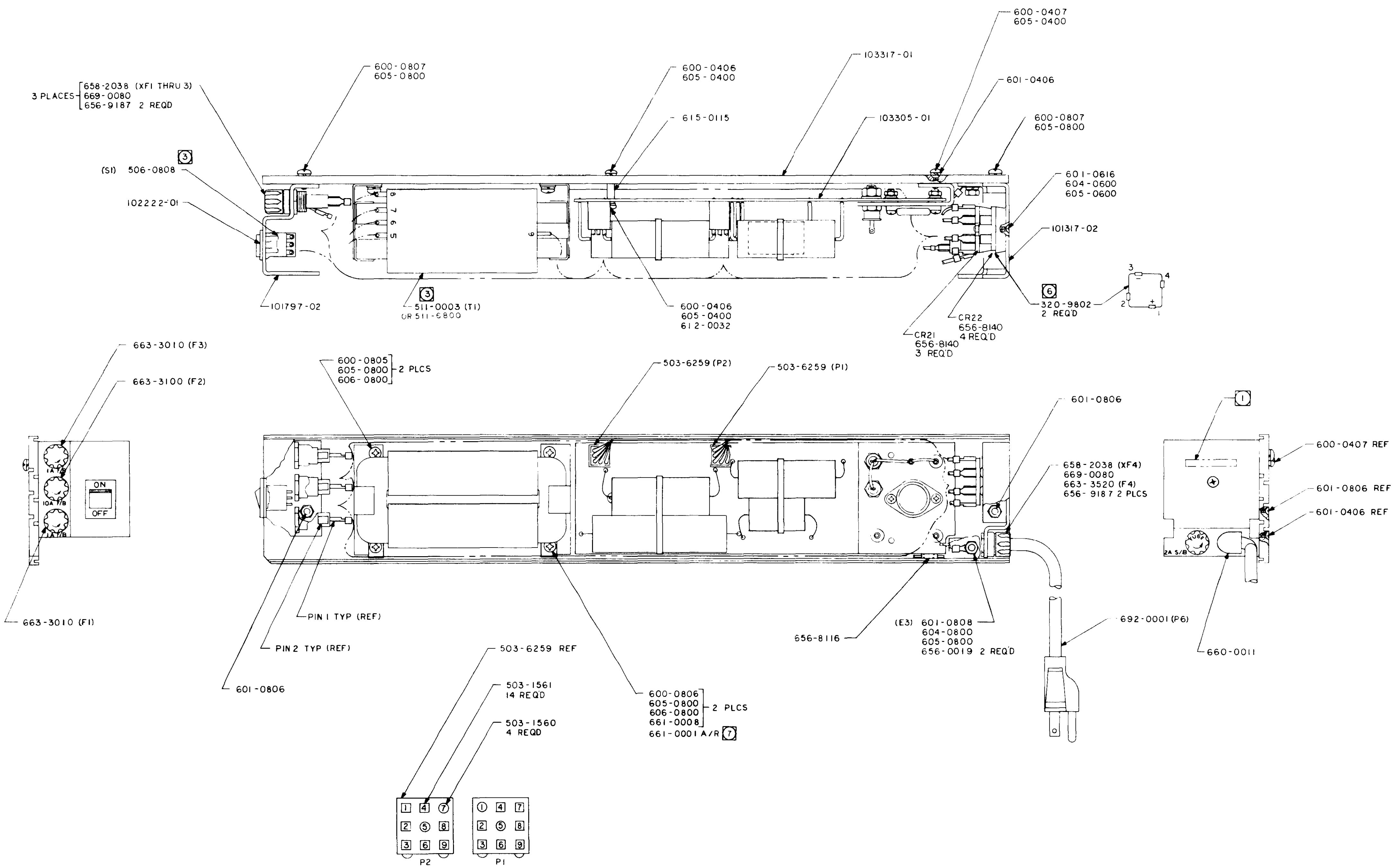
MATL: SEE LM

SIZE	CODE IDENT NO.	DWG NO.	REV
D		103311	A

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

103311 A

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 5-PV PRODUCTION RELEASE	9-11-73	A.V.	[illegible]	MJ
B	ECN 6064	9/14/74	J.L.	[illegible]	[illegible]
C	ECN 6199	4/3/74	[illegible]	JBR	[illegible]



PIN INSERTION VIEW SHOWN

7. TIE WRAP CABLE AT TWO INCH INCH INTERVIALS USING 661-0001.
6. APPLY 665-0001 SILICONE GREASE TO BOTTOM SIDE OF CR21 & CR22. A MIN OF 90% COVERAGE IS REQ'D.
5. USE PART NO. 689-0018, 689-5518, 689-9918 AND 689-8822 AS REQ'D PER WIRE LIST 103318. USE PART NO. 661-001 WIRES TO TERMINAL
4. ALL SCREWS TO BE TORQUED AS FOLLOWS: NO. 4 TO 6 IN. LBS; NO. 6 TO 11 IN. LBS; NO. 8 TO 20 IN. LBS.
3. USE SHRINK SLEEVING (669-0030) ON ALL TERMINALS AS REQ'D.
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
1. MARK ASSEMBLY P/N 103314 INCLUDING VERSION NUMBER AND VERSION ISSUE LETTER.

NOTES: UNLESS OTHERWISE SPECIFIED

WIRE LIST 103318
SCHEMATIC 103304
REFERENCE DRAWINGS:

PART NO. 103314 0/REV A

101310	BUFFER
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES: .XX ± .XXX ± ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

SIGNATURES	DATE
DR	8-5-73
CHK	9/3/73
DES	
ENGR	
PROJ ENGR	

FINISH:
MATL: SEE L/M

PERTEC PERIPHERAL EQUIPMENT

TITLE
POWER SUPPLY ASSEMBLY

SIZE E | CODE IDENT NO. | DWG NO. 103314 | REV C
SCALE 1:1 | DO NOT SCALE DWG | SHEET 1 OF 1