CASSETTE INTERFACE

Assembly, Checkout, and Theory

PolyMorphic
Systems

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1 Introduction

PolyMorphic Systems is pleased to have your order for POLY 88 series equipment. We have endeavored to supply the most thoroughly tested and documented material on the market. The system is modular and Altair compatible, and is designed to accept nearly every peripheral device available. We ask you scan this manual before assembly.

POLY 88 modules are designed for ease of assembly, use and durability. If, however, after having read the manual, you have any doubt of your faith in the project please return the kit(s) to us , in original condition, for a full no-questions-asked refund.

1.1 WARRANTY

KITS: All parts and materials are warranted to be free of defects at the time of shipment. Defective parts will be replaced free of charge if returned to the factory within ten (10) days of receipt of delivery or upon written statement by purchaser that the unit was unassembled or untested for up to ninety (90) days due to circumstances beyond his control. Completed units returned under similar circumstances will be repaired at a labor cost of $20/hour, with defective parts replaced free. Should the estimated cost of repair exceed 20% of the original cost of the unit, the customer will be notified prior to repair.

THE WARRANTY IS VOID IF THE KIT IS SOLDERED WITH CORROSIVE FLUX.

ASSEMBLED: The assembled units are fully warranted to be free of defects for ninety (90) days from the time of shipment. If they are found to be defective in this period they may be returned to the factory for repair or replacement free of charge (including return shipping).

1.2 Inspection

If your package has arrived in poor condition please inspect the contents for damage. The units are shipped in damage resistant containers. In the unlikely event of damage or breakage, please return the kit to us in the original container for replacement.

1.3 Handling precautions:

As with any sensitive MOS (metal oxide semiconductor) caution must be exercised to avoid damage to the chip. The most frequent problem is damage caused by static electricity. While handling the chips (Integrated Circuits) we recommend that cotton clothing be worn in preference to synthetic materials.

More importantly, these devices should never be handled by the leads. They should be handled only by the ends of the chips. Since they come packed to protect the leads, there is no reason to actually endanger the chip until it is time to install them in the IC sockets on the board.

1.4 Soldering tips:

1. Use a soldering iron of 25 watts or less. Larger soldering tools such as soldering guns and bigger irons are too hot. The lower wattage irons do the job efficiently and reduce the risk of burning the printed-circuit board.
2. Use a small, clean tip on the iron. Clean it after each use on a small piece of damp sponge.
3. Use the 60-40 rosin-core solder. This type is provided with your kit. Use the supplied solder or the smallest diameter available. Do not use acid-core solder or externally applied fluxes. USE OF EXTERNAL FLUXES OR ACID CORE SOLDER VOIDS YOUR WARRANTY.
4. To solder, first apply a light coat of solder to the tip of your iron. Place the tip against both the component lead and printed circuit juncture to be soldered. Add ample solder to the juncture of lead and printed circuit pad but not to the iron itself. The solder will melt when the unit to be soldered is sufficiently heated and will bond by forming a capillary film between the lead and pad.
5. Remove the solder after one or two seconds. The rosin will bubble (boil) out. Allow three to four bubbles then remove the iron. Do not keep the heat applied for more than ten seconds.

6. Solder bridges look very neat but are a constant source of trouble. Solder bridges are caused by an excess of solder being built up on one conductor and overflowing to another. Great care must be exercised to avoid the occurance of solder bridges. Use the minimum amount of solder possible. Inspect each IC socket and individual component after soldering. Solder bridges can be a constant source of trouble when boards of a high trace density are being assembled.
7. The best method of removing solder bridges is the use of a vacuum "solder-puller" available at most electronic supply houses. They are relatively inexpensive. The joint is heated and vacuum applied to the bridge. Another method is to remove the bridge with wick-type solder remover after heating the troublesome area.

   Yet another assault on a solder bridge can be made by reheating the bridge with the iron and drawing or pulling the solder away until it is thin enough to be broken or cleaned witn an X-acto knife or other keen tool.
8. Be careful not to burn through traces on the PC board.

1.5 SAFETY:

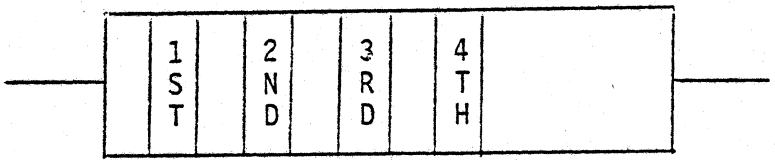
We strongly recommend that after a component has been soldered, the excess lead be cut only with a pliers attached to the free end. This method of trimming, while a bit awkward at first but prevents small pieces of lead from flying into the eyes. If you do not wish to follow this procedure, we recommend wearing safety glases.

1.6 DIODE POLARITY:

anode cathode anode cathode

GUIDE TO RESISTOR COLOR CODE AND CAPACITOR POLARITY

1.7 Resistor Color Code (Values in Ohms)



	1st Band	2nd Band	3rd Band		4th Band (Tolerance)
Black	0	0	x1		
Brown	1	1	x10		
Red	2	2	x100		
Orange	3	3	x1000	or x1K	
Yellow	4	4	x10,000	or x10K	
Green	5	5	x100,000	or x100K	
Blue	6	6	x1,000,000	or x1 meg	
Violet	7	7	x10,000,000	or x10meg	
Gray	8	8	x100,000,000	or x100 meg	
White	9	9	x1,000,000,000	or x1 giga	
Gold			x0.01		± 5%
Silver			x0.1		±10%
No Band					±20%

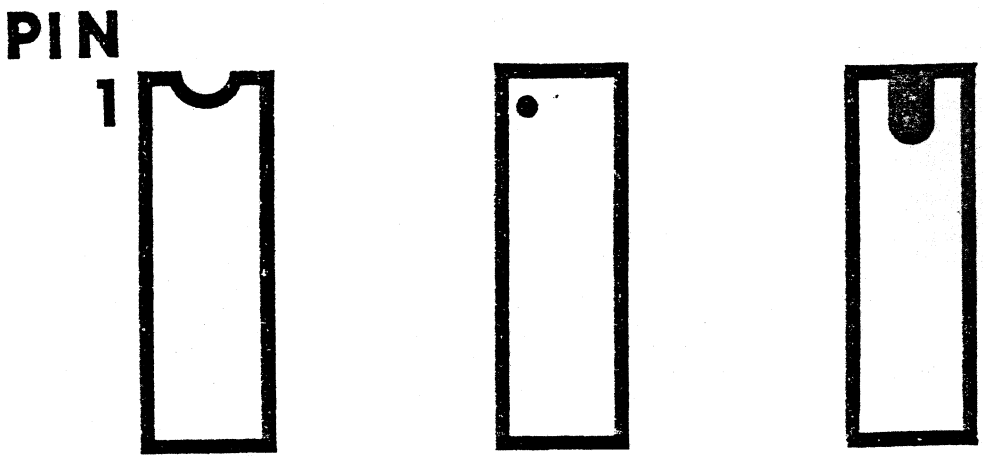
Capacitor Polarity Markings

All tantalum and electrolytic capacitors must be oriented properly to prevent destruction. The positive terminal or lead is usually marked. The mark can be a plus sign (+), a dot or stripe down the side of the component nearest the positive lead. On larger "can" type electrolytic capacitors, the positive terminal is often marked by a red or white dot. Always trust the dot, not the markings on the can.

1.8 LOADING DUAL IN-LINE PACKAGES (DIP)

Most DIP have their leads slightly spread. They must be walked into the socket using the below mentioned procedure. We strongly urge that sockets be used for the installation of these integrated circuit packages because of the difficulty in installing them directly to the board. The use of sockets also relieves some of the damage hazard caused by static electricity.

Orient the device properly. Pin 1, always indicated by a notch on the assembly diagram, is sometimes indicated by an embossed dot instead of a notch on the IC itself. Refer to the drawing below for indication of pin 1. (Pins are counted counter-clockwise from pin 1.



To install a DIP into the socket, insert the pins on one side a very slight distance into the socket. Apply a slight sideways pressure on the pins of this side. Now, reverse the procedure. Bend the pins only until both sides begin to enter the socket holes.

Press the IC straight down until it seats in the socket. Use a gentle pressure in the center of a small chip or two pressure points of equidistant spacing on the larger units such as MCM6571A or 8212.

2. GENERAL INFORMATION

Here is your PolyMorphic Cassette Interface. It is a "minicard" which fits nicely in the backpanel of your Poly 88 system and operates through the serial port on the CPU board.

The PolyMorphic Systems Cassette Interface provides two recording techniques, Byte Standard and a special Polyphase. The Byte Standard is a technique which allows a great range of recorder quality, and is therefore the best for program exchange. However, Byte Standard is a relatively slow technique. It operates at 300 Baud (approx. 30 characters per second).

The Polyphase method allows a much faster rate but is not as tolerant to recorder quality. It operates at 2400 Baud (approx. 240 characters per second, 8 times faster than Byte Standard) which allows a much more satisfying system operation when used with a good quality recorder. It will read or write 1024 bytes in about 6½ seconds compared to 52 seconds for the same amount in Byte. (The last figure includes allowance for format overhead, including inter-record gap, sync characters, block type, memory address, block length, etc. as described in detail in the description of the 4.0 monitor.) The interface is controlled by the System monitor and the dumper program.

2.1 IMPORTANT! We have used the following recorders with this interface:

Superscope	C101
Superscope	C102
Superscope	C103
Superscope	C104
Sears	799.21682501
Panansonic	RQ - 309DS & RQ - 413S
Sony	TC110B

Of these, only the Superscope models C103 and C104 are recommended for reliable Polyphase use. All tested models work reliably with the Byte mode. A minimal requirement for Byte use is a tone control.

2.2 MATERIAL

In addition to this manual, you should have the following bags of hardware -

Part No.	Unit
101101	Byte-Biphase Circuit Board
101102	Cassette Bag Ø
101103	Cassette Hardware (inside Bag 1)
101104	Cassette Bag 1
101105	Cassette Bag 2

2.3 Parts list and check-off sheet.
Check the contents of each package against each list.

2.3.1 BAG Ø

Check	Quantity	Part Number	Description
( )	1	018008	8-pin IC sockets
( )	2	018014	14-pin IC sockets
( )	4	018016	16-pin IC sockets
( )	1	031086	74LS86
( )	1	031257	74LS257
( )	1	034227	8T20
( )	1	034263	CD4013
( )	1	034277	CD4027
( )	1	034520	96L02
( )	1	034530	75453

2.3.2 Cassette Hardware

101103

Cassette Hardware

2	2-56 x3/8" F. H. machine screw
2	#2 lock washer
2	#2 hex nuts
3'	Solder
6"	#24 wire

2.3.3 BAG 1

Check	Quantity	Part Number	Description
	1	012515	68pF capacitor
	1	012545	0.001μF ±20% ceramic disc cap
	1	012560	.01μF cap (mylar)
	1	012562	0.01μF ±20% 100V ceramic disc cap
	1	012585	.047μF cap (mylar)
	8	012600	0.1μF/16V capacitors (ceramic)
	1	017330	25-pin connector
	1	012550	0.0047μF ±20% capacitor
	1	017329	Hardware for connector
	1	047202	20K single-turn trimpot
	1	047205	100K single-turn trimpot
	1	053519	15Ω ¼w carbon comp. resistor
	2	053547	220Ω ¼w carbon comp. resistor
	14	053571	2200Ω ¼w carbon comp. resistor
	2	053573	2.7K ¼w carbon comp. resistor
	2	053587	10K ¼w carbon comp. resistor

(4)	1	053591	15K ¼w carbon comp.
(4)	3	053616	100K ¼w car. comp. resistor
(4)	1	072185	2N5447 transistor (pnp)
(4)	1	079100	Ribbon Cable (14 cond - 2 plugs)

2.3.4 BAG 2

( )	1	101105	Small Dumper on cassette tape

3. Install DIP sockets:

Orient the PC board so that the word "TOP" is on the right side of the board.

According to figure 1-1 and the check-off list, install sockets on top of the PC board.

Install IC sockets

Check	Location	Component
(1)	IC1	16 pin socket for 8T20
(1)	IC2	16 pin socket for 96L02
(1)	IC3	14 pin socket for 4013
(1)	IC4	16 pin socket for 74LS257
(1)	IC5	14 pin socket for 74LS86
(1)	IC6	16 pin socket for 4027
(1)	IC7	8 pin socket for 75453

3.1 Install resistors:

Number	Description	Color
1	15Ω ¼W	brown-green-black
2	2.7K ¼W	red-violet-red
3	220Ω ¼W	red-red-brown
4	2.2K ¼W	red-red-red
5	2.2K ¼W	red-red-red
6	15K ¼W	brown-green-orange
7	220Ω ¼W	red-red-brown
8	2.2K ¼W	red-red-red
9	2.7K ¼W	red-violet-red
10	2.2K ¼W	red-red-red
11	2.2K ¼W	red-red-red
12	2.2K ¼W	red-red-red
13	100K ¼W	brown-black-yellow
14	10K ¼W	brown-black-orange
15	10K ¼W	brown-black-orange
16	2.2K ¼W	red-red-red
17	2.2K ¼W	red-red-red
18	100K ¼W	brown-black-yellow
19	100K ¼W	brown-black-yellow
20	2.2K ¼W	red-red-red
21	2.2K ¼W	red-red-red
22	2.2K ¼W	red-red-red
23	2.2K ¼W	red-red-red
24	2.2K ¼W	red-red-red
25	2.2K ¼W	red-red-red

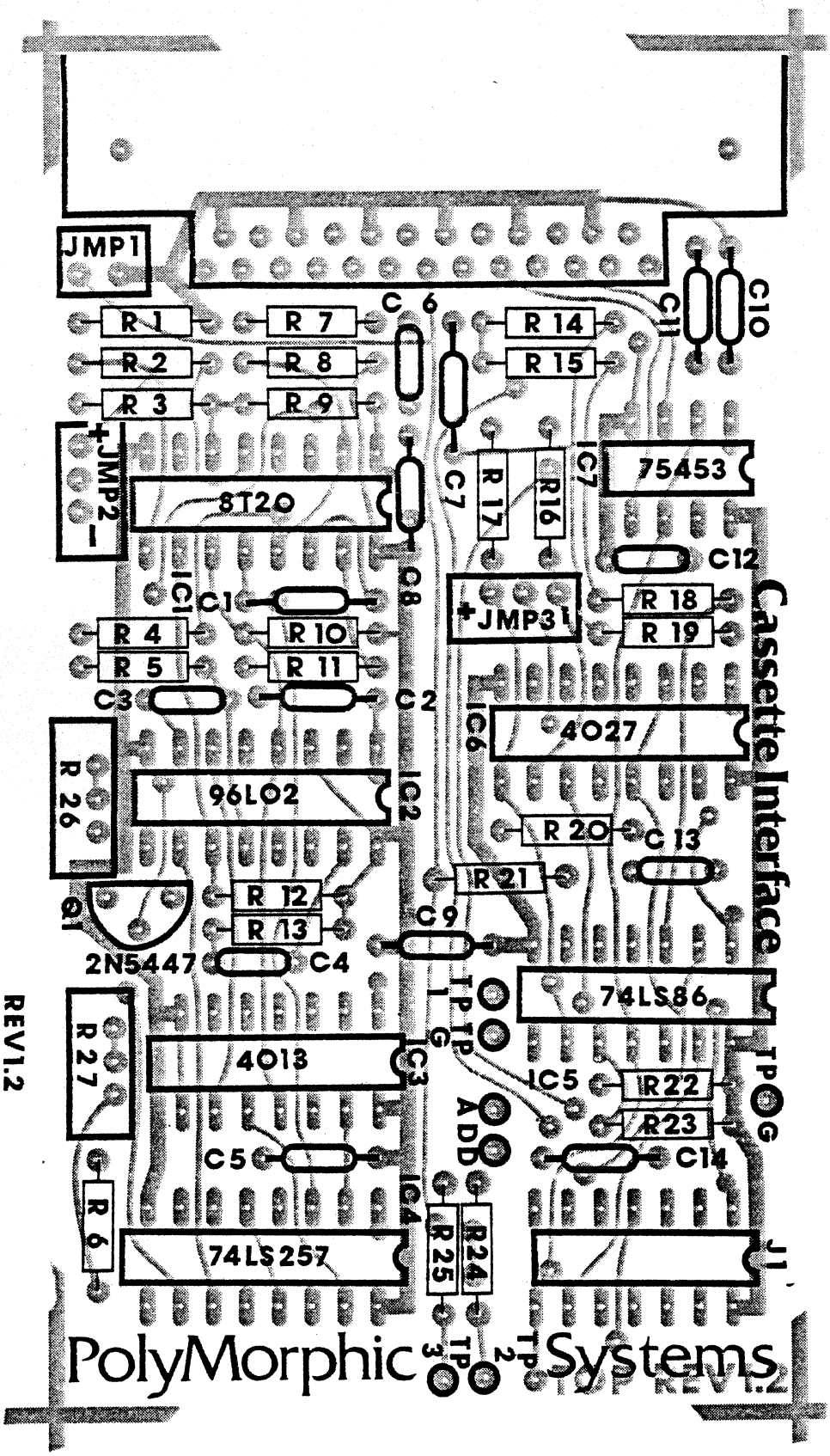
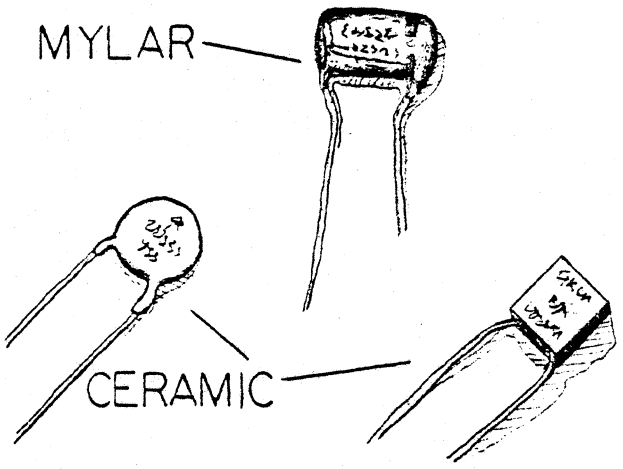


FIG. 1-1
ASSEMBLY DRAWING

REV1.2

3.2 Install capacitors;

Number	Description
1	.047μF 100V mylar
2	.01μF 100V mylar
3	.001μF ceramic disc
4	68pF ceramic disc
5-9	.1μF 16V ceramic disc
10	.0047μF 100V ceramic disc
11	.1μF 16V ceramic disc
12	.01μF 100V ceramic disc
13-14	.1μF 16V ceramic disc



3.3 Install 2N5447 transistor following the assembly drawing (fig. 1-1)

3.4 Install pontentiometers

Orient the potentiometers so that the screw adjustments are toward the outside of the board.

R26	20K
R27	100K

3.5 Install connectors.

Mount the 25 pin connector on the top of the card. You will probably need a thin, stiff tool such as an awl or screwdriver or needlenose pliers to align each pin with its hole in the PC card. Begin at one end and work toward the other, partially inserting each pin. Do not force the connector into position; it will slide into place with slight pressure if all 25 pins are oriented properly. Fasten the connector to the card with 2-56 screws, nuts, and lock-washers. Solder the pins.

Orient the card so that the 25 pin "D" connector is on the left edge. Insert the cable plug, on the component side of the board, so that the colored wire (usually red) is at the top, and the cable extends

to the right. Notice that pin 1 of the plug is in the upper left hand corner. Solder the pins.

3.6 Examine the board very carefully for:

solder bridges
unsoldered joints
cold solder joints

3.7 Install integrated circuits. Note: The ICs marked * are MOS, and can sometimes be damaged by the voltages present on your hands. Do not touch the pins on these chips any more than is absolutely necessary.

Check	Layout Position #	Description
( )	IC1	8T2Ø bidirectional one shot
( )	IC2	96LØ2 retriggerable one shot
( )	IC3*	4Ø13 D flip flop
( )	IC4	74LS257 QUAD 2-1 Multiplexor
( )	IC5	74LS86 exclusive OR gate
( )	IC6*	4Ø27 J-K flip flop
( )	IC7	75453 OR gate

3.8 Circuit power up and adjustment:

First use an ohmmeter to check +5V and -5V to ground. Pin 14 to pin 10 of the ribbon cable should give a reading of approximately 1000Ω in the forward direction and 450Ω in the reverse. Pin 11 to pin 10 should give 1000Ω forward and 20KΩ reverse. These are typical values and will vary between different ohmmeters. Connect the ribbon cable to the serial port; make sure pin one is down when installing the DIP plug in the CPU board. Check for +5V ±0.25V on the highest numbered pin (8, 14 or 16) on each of the IC's. Check for -5V ± 0.25V on IC1 pin 4.

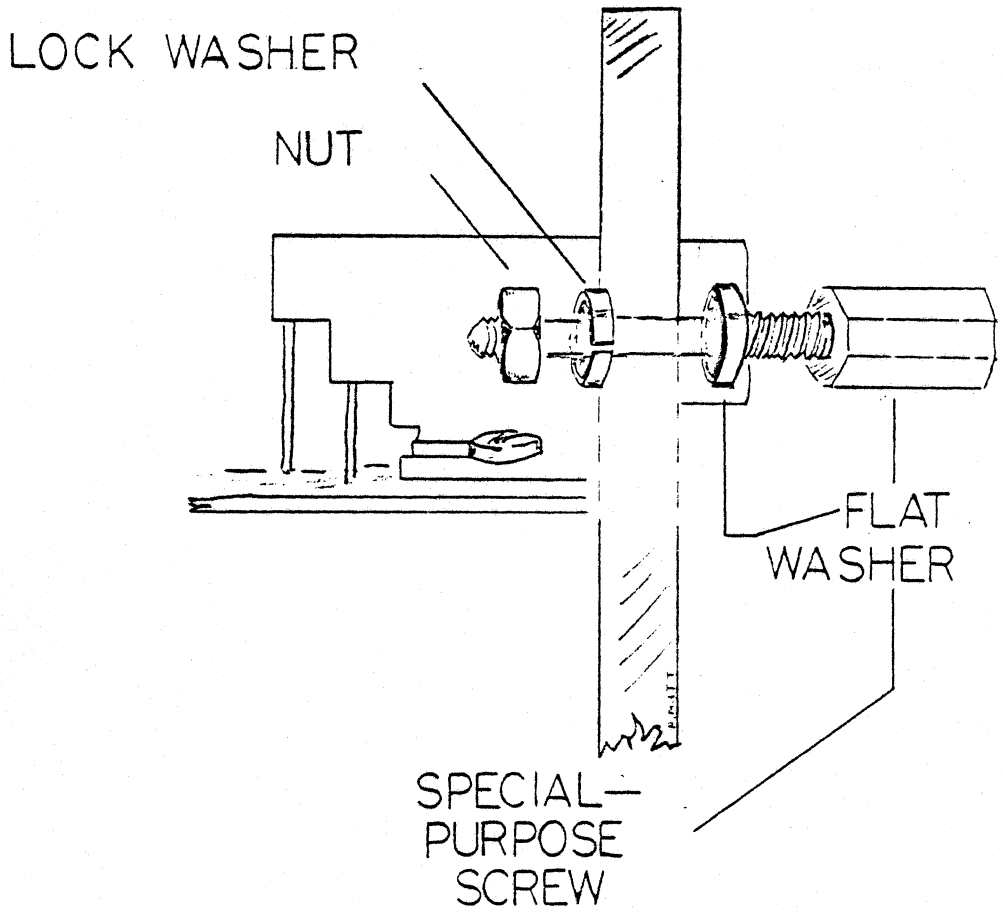


FIG. 1-2

3.9 Device Address Selection and Installation

As supplied, the cassette board is set up to be serial device #Ø. Device Ø is used as the bootstrap loader device when the Poly 88 system is powered up.

If this is your second cassette board the address should be set to 1. This is accomplished by breaking the printed trace connecting the two pads labeled ADD on the assembly drawing. The trace is located on the bottom side of the PC card, and may be easily cut with an X-acto knife.

Using the hardware supplied, (P/N 017329) install the card in the cassette connector cutout (above transformer) on the back panel of the Poly 88 (see Fig. 1-2). Then plug the free end of the ribbon cable into one of the two serial I/O connectors in the upper right hand corner of the CPU card. Make sure that pin* 1 of the DIP plug corresponds to pin 1 of the socket. If installed backwards the cassette card may be destroyed when power is applied to the system. *see 3.5

3.9.0 Byte Setup.

For setup the Byte/Polyphase cassette card you will need a logic probe, a voltmeter, three clip leads and a 1-10uF capacitor.

Make sure JMP1 is shorted by a trace on the bottom of the board. Temporarily connect a 1-10uF capacitor from pin 1 of IC6 (+ end) to pin 5 of IC1 (- end). Connect a voltmeter (6-10V scale) to test point 1 and ground (TPG). Adjust pot R27 fully clockwise. Check test point 1 with a logic probe It should be continuously high. Now measure the voltage on TP1. It should be 2 and 5 volts. Now multiply this value by 3/4 for use in the next step.

Connect a temporary jumper between IC5 and pin 9 and ground (TPG). Set pot R27 to give the voltage previously calculated on TP1. With a logic probe check the RXC- is low with positive pulses. This gives you 75% duty cycle at TP1.

3.9.1 Polyphase Setup

Remove the jumper from IC5 pin 9 to ground. Remove the short on JMP1 (cut the trace on the bottom of the board). Make sure the

power is still off and carefully remove the 8T20 from its socket. Turn on the power and press P on the keyboard. This will enable the cassette board. Measure the voltage at TP3. It should be between 2 and 5 volts. Multiply the measured value by ¼. This value will be needed later in the setup procedure. Turn off the power and reinsert the 8T20.

Load the following program* into onboard RAM at ØDØØ:

ADDR	DATA		PROGRAM	
ØDØØ	2118ØD	BIPH:	LXI	H,TISR
ØDØ3	2216ØC		SHLD	SRA4
ØDØ6	CDADØ2		CALL	SETUP
ØDØ9	Ø5		DB	ØØ5H
ØDØA	AA		DB	ØAAH
ØDØB	4Ø		DB	Ø4ØH
ØDØC	ØC		DB	ØØCH
ØDØD	E6		DB	ØE6H
ØPØE	E6		DB	ØE6H
ØDØF	ØØ		DB	ØØØH
ØD1Ø	3E21		MVI	A,Ø21H
ØD12	D3Ø1		OUT	Ø1
ØD14	76	LOOP:	HLT	
ØD15	C3140D		JMP	LOOP
ØD18	3E 55	TISR:	MVI	A,55H
ØD1A	D3ØØ		OUT	Ø
ØD1C	C364ØØ		JMP	IORET

* Note: This program is set up to run with a 4.0 monitor ROM.

PolyMorphic Systems Byte/Biphase Cassette Interface

This program sets up the USART for Polyphase operation, and outputs a string of alternate ones and zeros. Run the program starting at address ØDØØ. Turn the Polyphase setup pot (R26) fully counterclock wise. Place your voltmeter on TP3 and turn the trimpot slowly clockwise until the voltage calculated in the first part of the procedure is reached.. Be careful because there are two settings of the pot that will give you this value. The correct one is the one furthest counterclockwise. Check TP3 with the logic probe. It should be low with positive pulses. Check TP2. It should be half ones and half zeros. This completes the Polyphase setup procedure. Remove the temporary 1 to 10μF capacitor.

Note: The best final trim of both the Byte and Polyphase setup is to read data and adjust the appropriate potentiometer (R27 for Byte ,R26 for Polyphase) one way and then the other, until errors result, then center the pot in the range found.

PLEASE READ THIS

To insure proper operation, read the Theory of Operation section thoroughly. This section contains important setup information.

4. Theory of Operation.

The function of the byte standard cassette interface is to enable the recording and playback of digital data on average or better audio cassette recorders with the POLY 88 system using the Provisional Audio Cassette Data Interchange Standard as described in Byte Magazine (February, 1976, pp. 72 & 73).

This standard was developed to provide a common, reliable, and inexpensive means of software exchange and mass storage. It defines a character oriented, serial, frequency shift modulation method at a nominal transfer rate of 300 Baud. A logical one is defined as eight cycles of 2400 Hz and a logical zero as four cycles of 1200 Hz. A character consists of a start bit (a zero), eight data bits and two (or more) stop bits (ones). See figure 1b. Intervals between characters are unspecified amounts of time filled with one bits.

The POLY 88 system, controlled by its ROM monitor, outputs and inputs this character format through the serial port in NRZ (non-return to zero) form. It also provides a syncronized 16X clock, TXC- (16 clock cycles per bit = 4800 Hz) during output to the tape interface. The interface in the write mode must convert this NRZ data plus the clock to the Byte format and present this, at the proper level, to the AUX input of the recorder.

IC5, IC6, R14, R19, C7 and C12 accomplish this. When the data input (TXD+) is a one, IC5 forces the inputs to the first flop of IC6 to zero. Also TXD+ is applied to IC6's set terminal forcing its output to a one. This output is connected to the input of the second flop causing it to toggle with each rising clock edge. This action

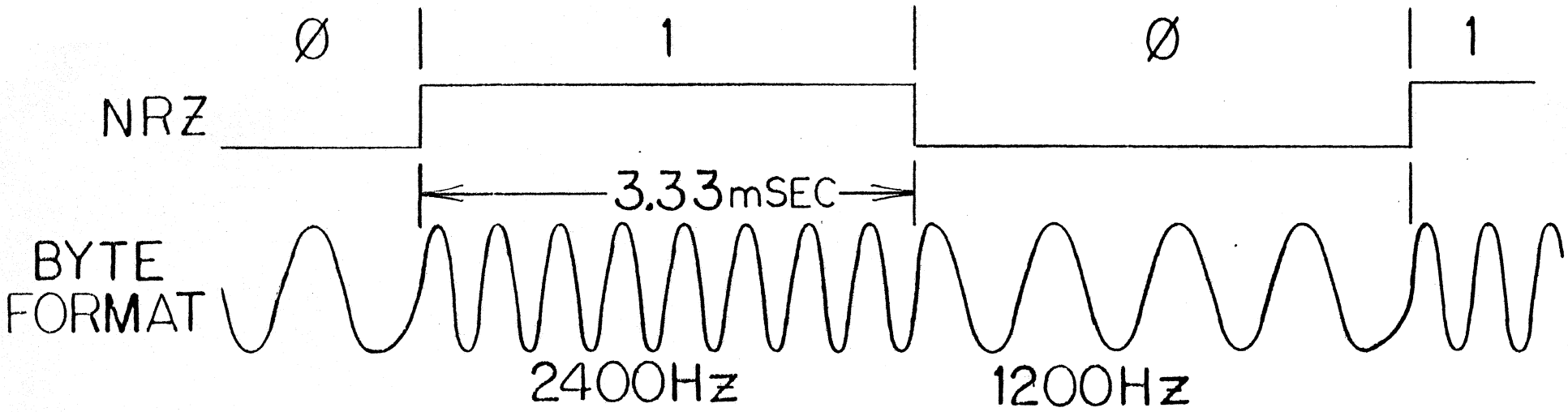


FIG1a. NRZ and Byte format per bit.

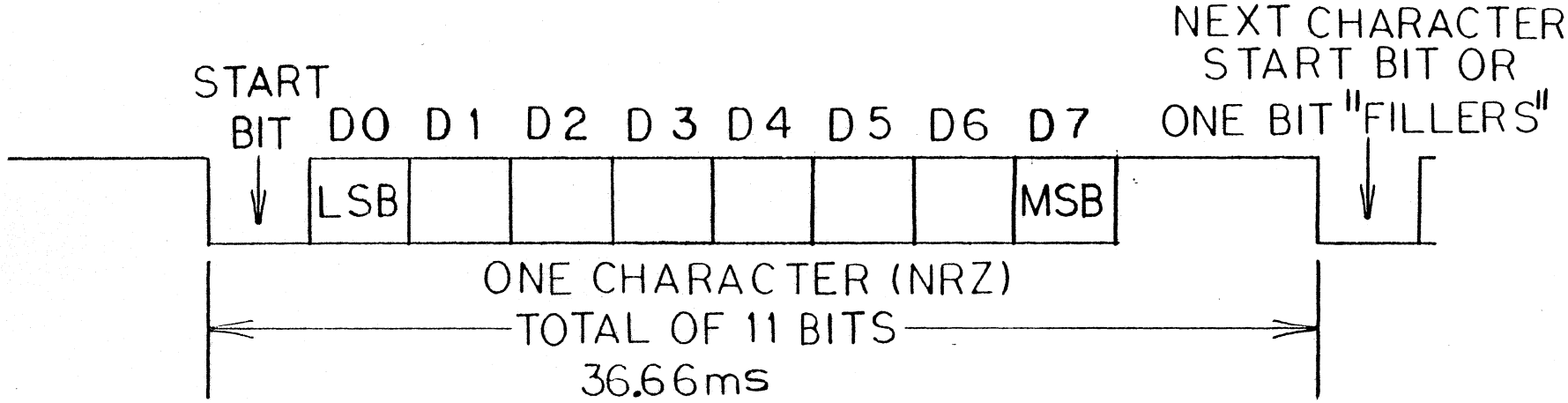


FIG1b. Byte character format.

divides the clock by two at the second flop's output creating 2400 Hz for the one level input. For a one bit, exactly eight cycles are produced because exactly 16 clocks are given. When TXD+ is a zero, the set is removed and the inputs are forced to one on the first flop. So the output of flop one is divided by two and the second flop divides by two again so its putput is 1200 Hz. For a zero input exactly four cylces are produced because 16 clocks were input. Resistors R14, and 19 form a resistive divider to reduce the 5V output of the flop to 500mV for the AUX input. C7 and C12 roll-off the high frequency components of the square wave output to better match the bandwidth of the recorder. Figure 2 shows the relationship between TXD+, TXC- and the signal for the AUX input to the recorder.

When reading data, the recorder output looks like the MON waveform shown in Figure 2B. This signal is adjusted to a nominal 2Vp-p with the volume adjust on the recorder. IC1, the 8T20, is a bi-directional oneshot. It accepts analog inputs and, as configured here, outputs short pulses at each zero crossing (both positive and negative going). R1 is a line termination resistor. R2, 7, 9 and 3 provide positive feedback to give a wide noise margin. R11 and C1 set the width of the output pulse. It is nominally 700μs. See Figure 2B, IC1-11 waveform. These pulses trigger IC2, a retriggerable one shot. It is set to a nominal 312μ s (3/4 of the period of 1200 Hz zero's waveform). If ones are being received, IC2 gets a new trigger every 208μ s, so it is constantly retriggered and makes its output a constant one. If a zero is being received, it gets a new trigger every 416μ s and therefore times out. This output is applied to IC3, a D flip-flop. Since this flop is clocked by the positive edge of IC1's output, ones are shifted through when 2400 Hz is being received and since its input is zero at each clock pulse during 1200 Hz, zeroes are output. IC3's output is now an NRZ reproduction of recording. It is buffered to the serial port by a multiplexor, IC4, as RXD+. It is also necessary to output 16 clocks per data bit back to the serial port. The negative

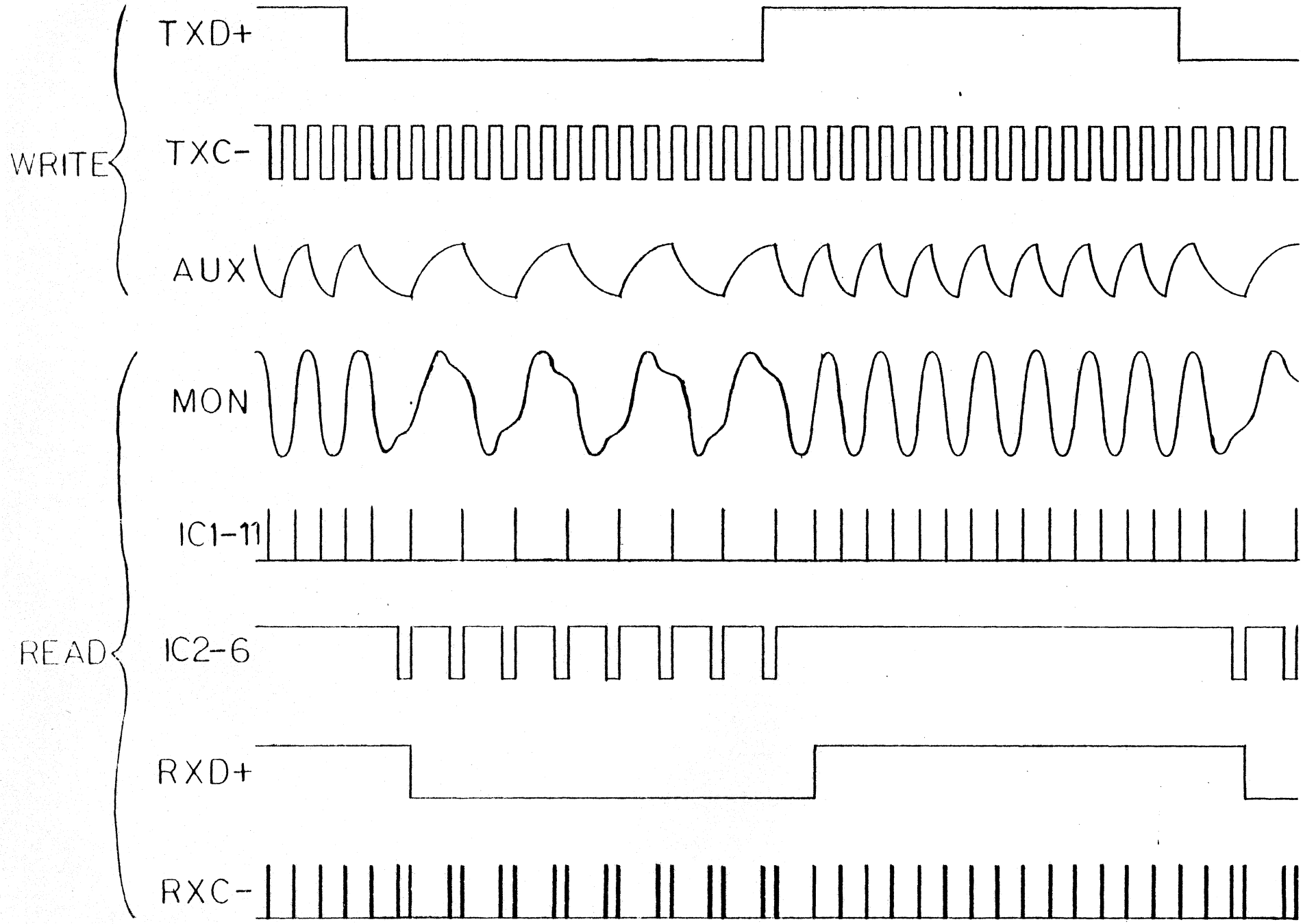


FIG 2B. BYTE TIMING WAVEFORMS

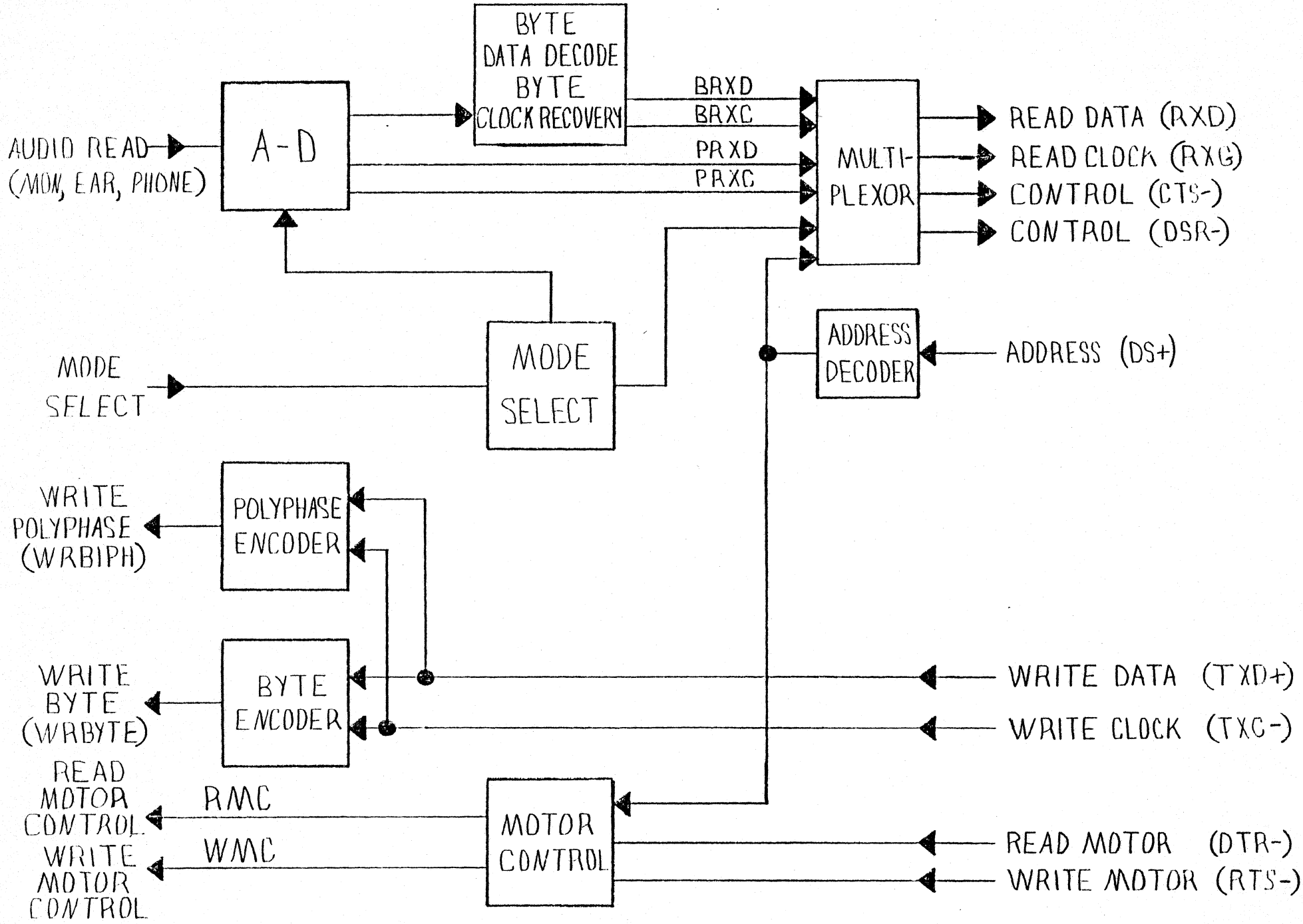


FIG 1D. CASSETTE INTERFACE BLOCK DIAGRAM

outputs of IC1 and IC2 are connected to the second one shot in IC2 in a manner that it produces a nominal 1μ s pulse for each IC1 pulse and each IC2 timeout. During the 1200 Hz zero 16 clocks are produced; eight from IC1 and eight from IC2. They are not evenly spaced but they do fill the requirements. This pulse train is buffered out to the RXC- line by a section of IC4. See Figure 2B.

4.1 Address decoder

The address decoder is needed because there are two serial ports on the CPU board which share the USART and therefore can only be operated one at a time. The cassette interface is normally set to address Ø with its jumper selection. The monitor expects tape operations to be there. But the other serial port, address 1 may be implemented as a second cassette, therefore the need for the jumper.

The DS+ signal is the device select input. When the ADD jumper is installed, output is enabled for DS+ equal to zero. This allows the POLY 88 to software select one of two devices plugged into the serial port.

The address logic is part of IC5, a 74LS86 exclusive OR used as a comparator.

The address jumper (ADD) is normally connected through by a printed trace on the PC card. This forces a logic Ø on pin 12 of IC5, an exclusive OR gate. Cutting this trace causes pin 12 to be pulled up to a logic 1 level by resistor R22. The output of IC5 (pin 11) is the enable line for the cassette board. When at a logic 1 level the outputs of IC4 are tri-stated and the motor controls are disabled (IC7). A logic Ø will enable the board, placing

data on pin 2 of J1, clock on pin 8 and logic Ø (ground) on pins 4 and 6 the clear to send and data set ready inputs to the USART. The cassette board is enabled when DS+ (device select) goes low if the ADD jumper is in place or high if the jumper is removed.

4.2 The Motor Control circuit IC7 takes the logic level USART outputs, Request to Send (RTS-) and Data Terminal Ready (DTR-), as controlled by the Monitor, and converts them to open collector current sink outputs, Write Motor Control (WMC-) and Read Motor Control (RMC-), which are directly capable of controlling the motor of the recorder used if it is of the type with a positive motor voltage source, and the remote jack between the motor and ground. The other recorder types described in Appendix A may be used with appropriate level shift circuitry or a relay. Attempted use of recorder types other than that described above will destroy the 75453 chip, IC7.

The 75453 driver has an open collector output which will sink 330ma and handle up to 30VDC.

Caution: See the appendix before connecting the motor control output to your recorder.

4.3 The Mode Select block switches the interface from the Byte Standard mode to the Polyphase mode. Jumper 1 controls the selection. A jumper installed puts the board in the Byte Standard mode (a jumper is printed on the solder side of the board when it is produced). No jumper puts the board in the Polyphase mode. The jumper connections are brought out to the recorder connector so that a switch may be installed at the recorder or a switch may be put on the Poly 88 backpanel in the hole over the video connector and wired to the jumper pads. A closed switch gives Byte and an open Polyphase.

The switch grounds the mode select line which causes the multiplexor to output the Byte output and Q1 to change the time constant of the A/D stage to the short value necessary for the Byte operation.

When the mode select line is shorted (logic Ø), transistor Q1 will conduct (due to current flowing from the emitter through R4 to ground) causing resistor R26 to be shorted out. R26 is the polyphase timing adjustment and is not needed for Byte operation. When the mode select goes high (unshorted) Q1 ceases to conduct (base and emitter voltages are nearly equal) and R26 is switched into the circuit.

4.4 The multiplexor, IC5, is basically a four pole 2-position switch. When pin 1 (mode select) is low for Byte, the "A" inputs (pins 2, 5, 11 14) are connected to the output and when high the "B" inputs (pins 3, 6, 10, 13) are connected. Pin 2 is Byte data and pin 11 Byte clock. Pins 3 and 10 are Polyphase data and clock, respectively. IC4's outputs are tristate and are put in the high impedance state if the interface address is not selected. When it is selected by the address decoder, it also outputs a low active state for the Clear To Send (CTS-) and Data Set Ready (DSR-) control lines in both modes.

5. The Polyphase technique is the PolyMorphics implementation of Phase encoded (P.E.), or Biphase, or Manchester encoding scheme. It is more efficient than the Byte method in that it encodes each bit of information into one cycle length of the clock frequency. Therefore the necessary clock frequency is 1X the data rate. The USART in the POLY 88 CPU may be programmed to operate in this mode. The encoding rules are simple; a "one" bit is a cycle in phase with the clock a "zero" is a cycle 180 degrees out of phase with the clock. This is implemented by a single exclusive OR gate, section a of IC5, the 74LS86. Data is applied to pin 1 of IC5 and the clock to pin 2. When the data is low the clock is passed through IC5 without inversion. When pin 1 goes high the clock is complemented or shifted in phase 180°. JMP 3 is provided to invert the data using section C of IC5 (pin 8, 9, 10). As supplied JMP 3 is wired to the + position. R15 should be 10K for most applications but if your recorder does not have an auxiliary input jack, R15 may be changed to 1000 ohms and used with the mircophone input. The auxiliary input should be used whenever possible as it produces the most reliable recordings. The waveshaping network (C10, C11, R15, R18) adjusts the TTL level out of IC5 to one compatible with the AUX input of the recorder, and filters out the high frequency components converting the wave form to a semi-sawtooth which fits the bandwidth of the recorder better.

Here is the first place a higher quality recorder is required. It must have sufficient fidelity to record this waveform without excessive phase shift. 2400 Baud was chosen because it produces waveforms with 2400 and 1200 Hertz primary frequency components which are most nearly centered in the audio freq. range of most recorders. But lesser quality recorders have narrow bandwidths which introduce phase shift in the important harmonics which make it difficult to reproduce the original waveform with sufficient accuracy to produce error free recordings.

Upon read back, the MON output of the recorder is applied to the 8T20, IC1. It is a bidirectional one-shot which will produce a timed pulse out for each zero crossing of the input. It also has an

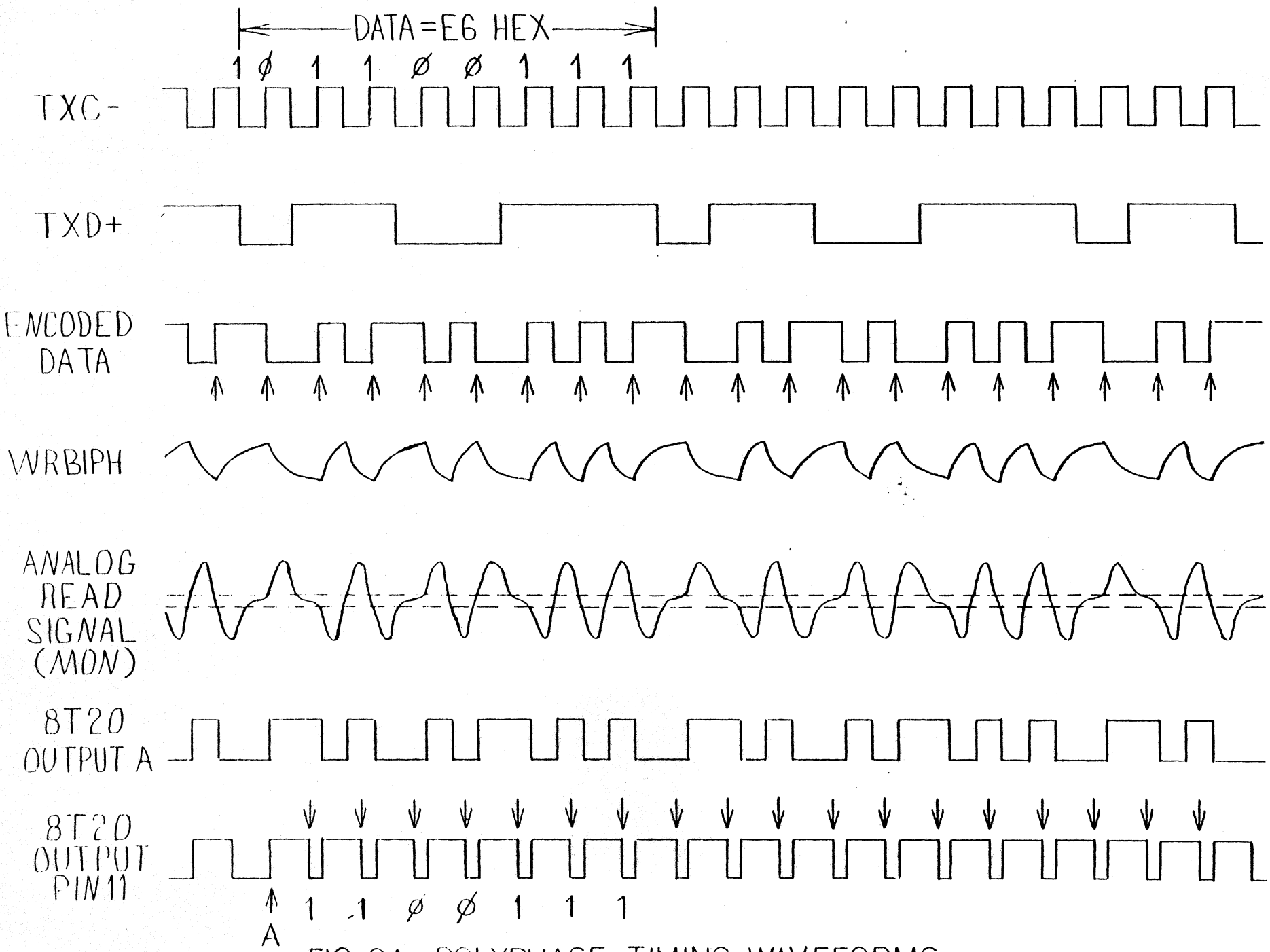


FIG. 2A POLYPHASE TIMING WAVEFORMS

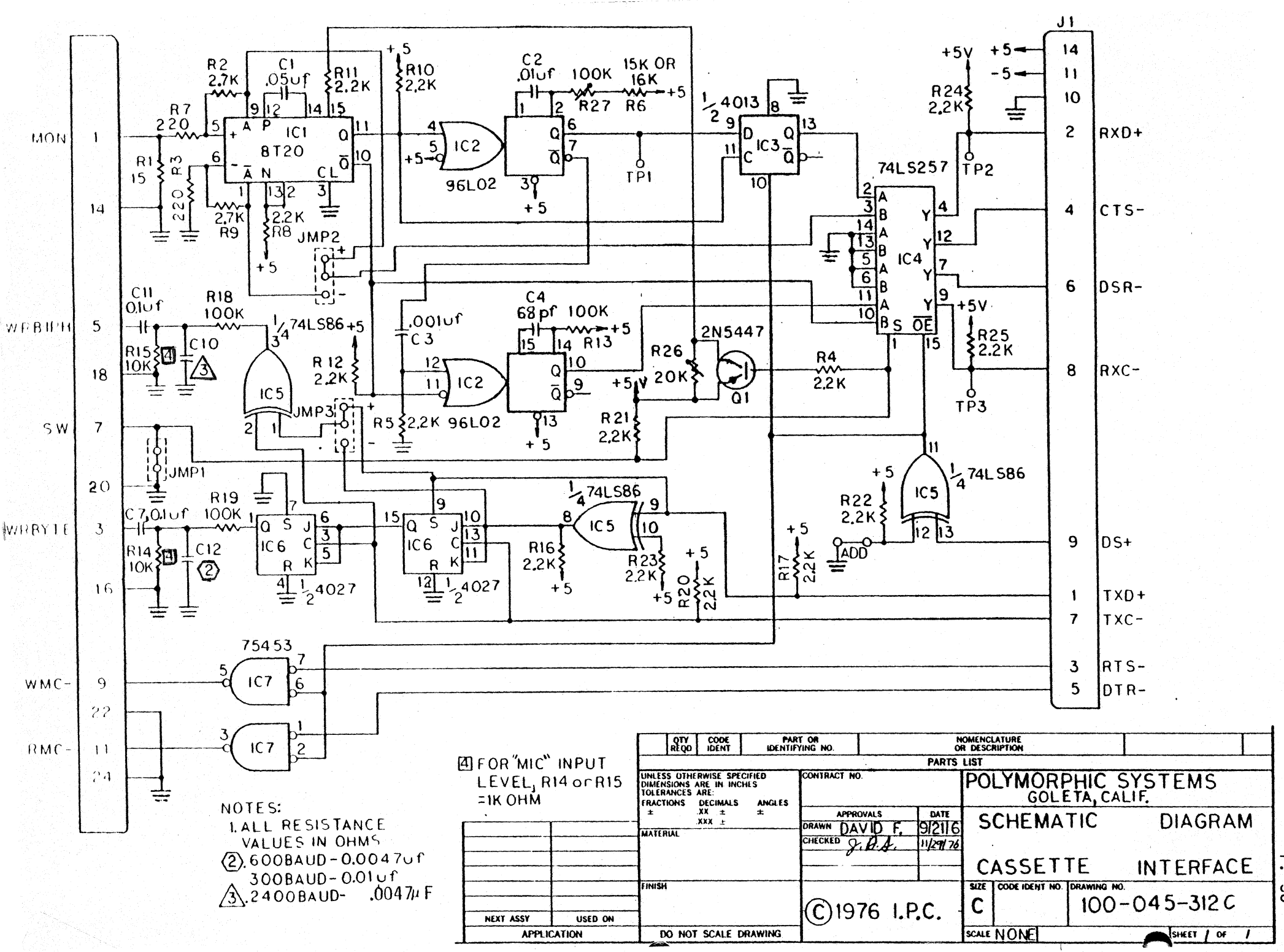
output from the first analog comparator stage. By setting the timed output to 3/4 of the bit period. IC1 will recover the clock with its negative going edge strobing the comparator output into the USART at the data level times. This is a sufficient set of inputs for the Poly 88 USART.

Going into more detail, R1 is a termination resistor to get rid of noise. R7, R2, R3 and R9 form a feedback circuit to cause hysteresis in IC1 to further increase noise margins. C1 and R11 plus pot R26 set the time constant for the one-shot. R26 needs to be adjusted for 3/4 of a bit period or 312 usec for 2400 Baud.

Looking at figure 2A we can see how the decoding process works. Each bit cell begins and ends with a transition. (Lines below encoded data delineate the bit cells.) If we send a long string of ones or zero's in biphase we end up with a 2400HZ square waves with in or out of phase with the original carrier. Two transitions occur during each bit cell with one exception - when we change from 1's to Ø's. There is no transition in the middle of this bit cell. This can be used to synchronize the one-shot IC1. At the beginning of each data record in polyphase is a string of bytes containing hexidecimal E6. (See Fig. 2A). IC1 may trigger on any of the transitions but upon excounting a 1 to Ø transition can trigger only at the edge of a bit cell. (Point A in Fig. 2A) Thereafter it will trigger only at the edges of a cell because we have selected the period of the oneshot to time out 3/4 of the way through the bit cell. Thus transitions in the middle of the bit cell are ignored. We now have a reference with which to compare the phase of the signal we are decoding. The USART samples the polarity of the phase encoded data once every bit cell. This occurs on the trailing edge of the output of the oneshot. If a one has been recorded the signal will be positive at this point. If zero has been recorded the phase will be reversed and the signal will be negative at this point. The output of the voltage comparator (pin 1 or 9 of IC1) is high or low depending upon signal polarity and is fed into the USART data input.

Note that the decoding process is sensitive to the polarity of the signal. If in Fig. 2d, the polarity of the analog read signal was inverted the data recovered would also be inverted. Since we are using phase modulation to encode data the system is sensitive to phase inversions. Some recorders may invert the phase of signals when playing back while others don't. Jumper area 2 (JMP 2) is provided to remedy this situation. If the recorder you are using inverts phase on playback, the center pad of JMP 2 may be wired to the pad marked negative and the trace from the center to positive may be cut. This re-inverts the data. When the recording circuitry inverts the phase going to onto a tape, JMP 3 may be reconnected similarly. When JMP 2 and JMP 3 are configured properly data recorded on one cassette recorder may be interchanged between recorders as the polarity of the flux changes on the tape are all consistent.

The Polyphase technique is controlled by the dumper program for recording and the loader in the monitor for playback. The format of the block structure is discussed in the monitor documentation.



[4] FOR "MIC" INPUT LEVEL, R14 or R15 =1K OHM

NOTES:
1. ALL RESISTANCE VALUES IN OHMS
(2). 600BAUD - 0.0047uf
300BAUD - 0.01uf
(3). 2400BAUD - .0047μF

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN DAVID F.	9/2/76
CHECKED J. B. S.	11/29/76

POLYMORPHIC SYSTEMS
GOLETA, CALIF.

SCHEMATIC DIAGRAM

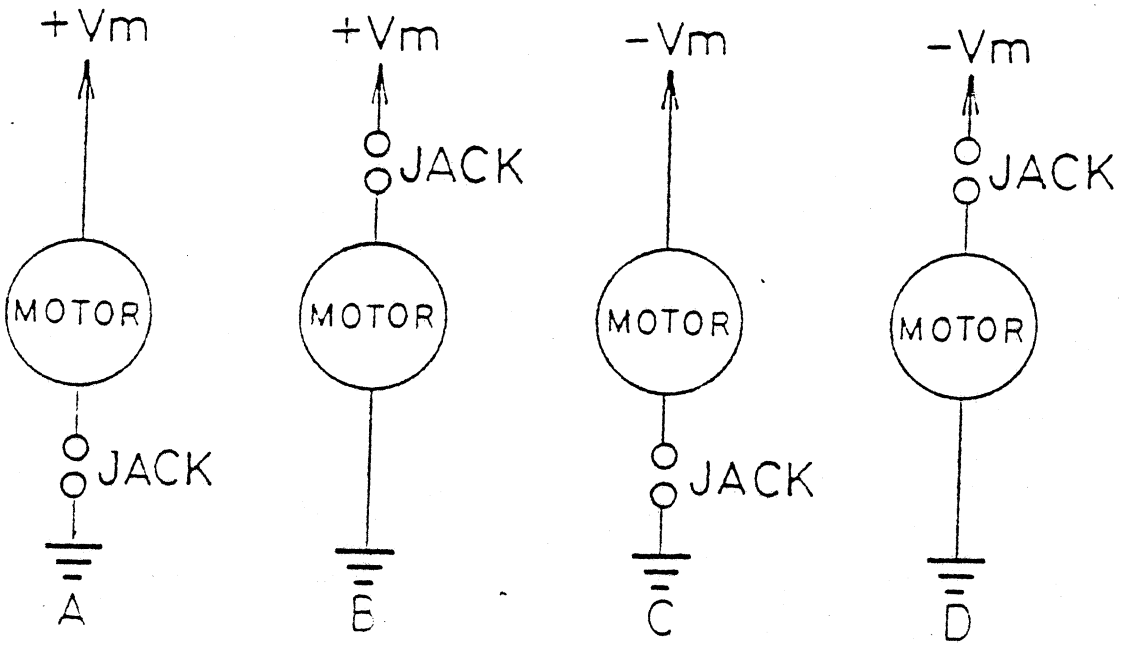
CASSETTE INTERFACE

SIZE	CODE IDENT NO.	DRAWING NO.
C		100-045-312 C

SCALE NONE SHEET 1 OF 1

Appendix A Motor Control Circuitry

Caution; Before attempting to use the motor control, determine the circuit location of your remote switch jack. Only one configuration can be connected directly to the cassette interface motor control circuitry. You can use a direct connection if the motor supply voltage is positive and the jack is between the motor and ground (Figure A). The other three possible configurations require a buffer circuit consisting of resistors and a transistor or relay.

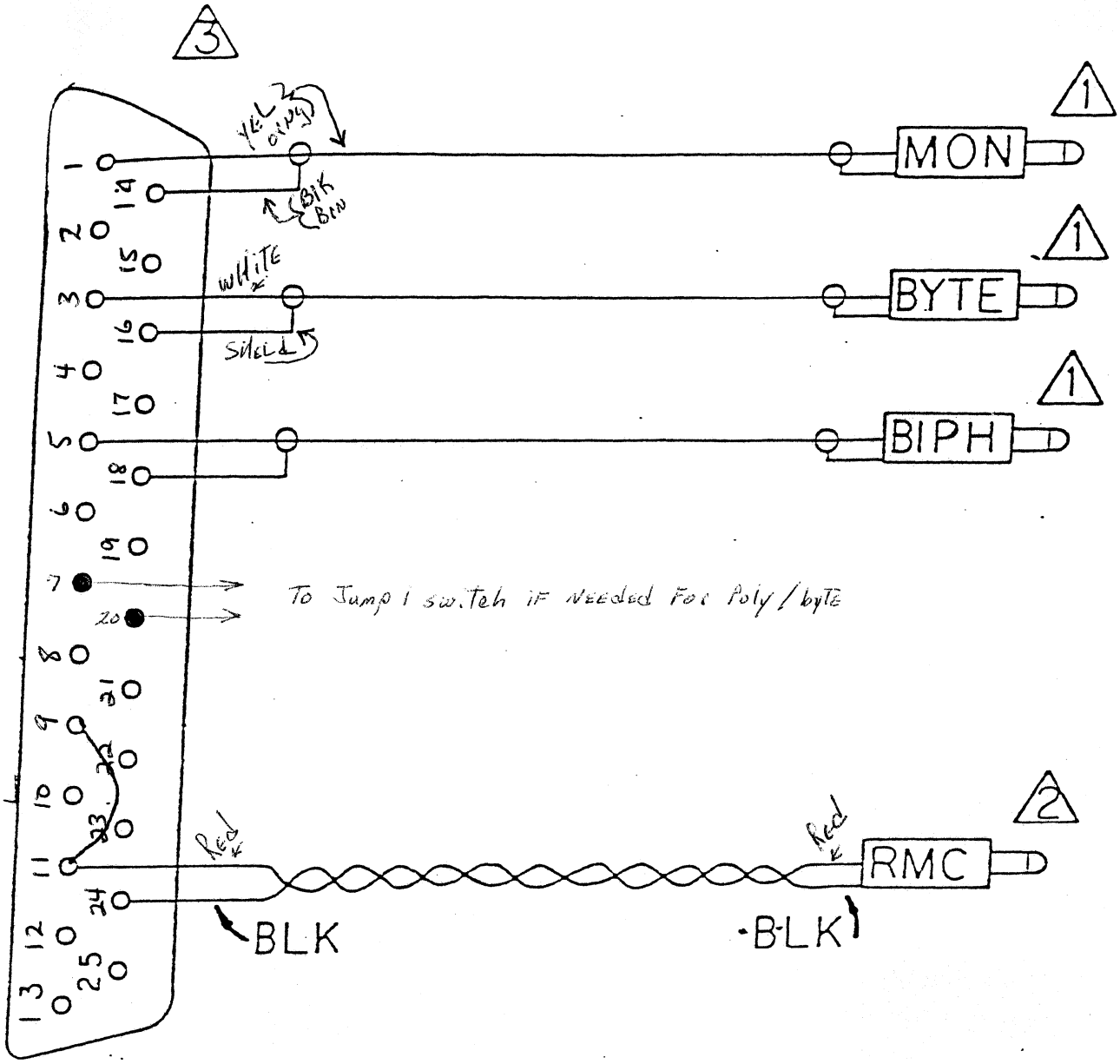


To determine which configuration your recorder employs, insert a shorted sub-miniature plug, put the recorder in the play mode, and measure the voltage between the plug and the recorder ground. You can usually trust the outside of the microphone jack (or MIC cable shield) to be ground. If the voltage is zero plus or minus a few millivolts, you have configuration A or C. If this is the case, separate the sub-miniature plug leads (remove the short) and measure the voltage on each lead -- one should be at ground; the other will be a positive or negative

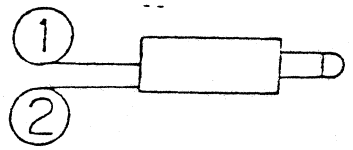
voltage. A positive voltage indicates configuration A and a negative voltage indicates configuration C. If the initial measurement (shorted plug) yielded a positive voltage, your recorder uses configuration B. If the initial measurement yielded a negative voltage, your recorder uses configuration D.

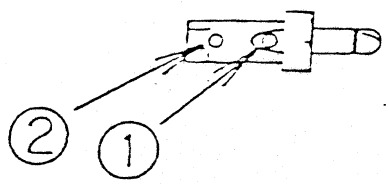
The following three pictorial diagrams show suggested circuits for connection to the 4 different types of recorders.

TAPE RECORDER CABLE



PHONE PLUG ASSEMBLY DETAIL



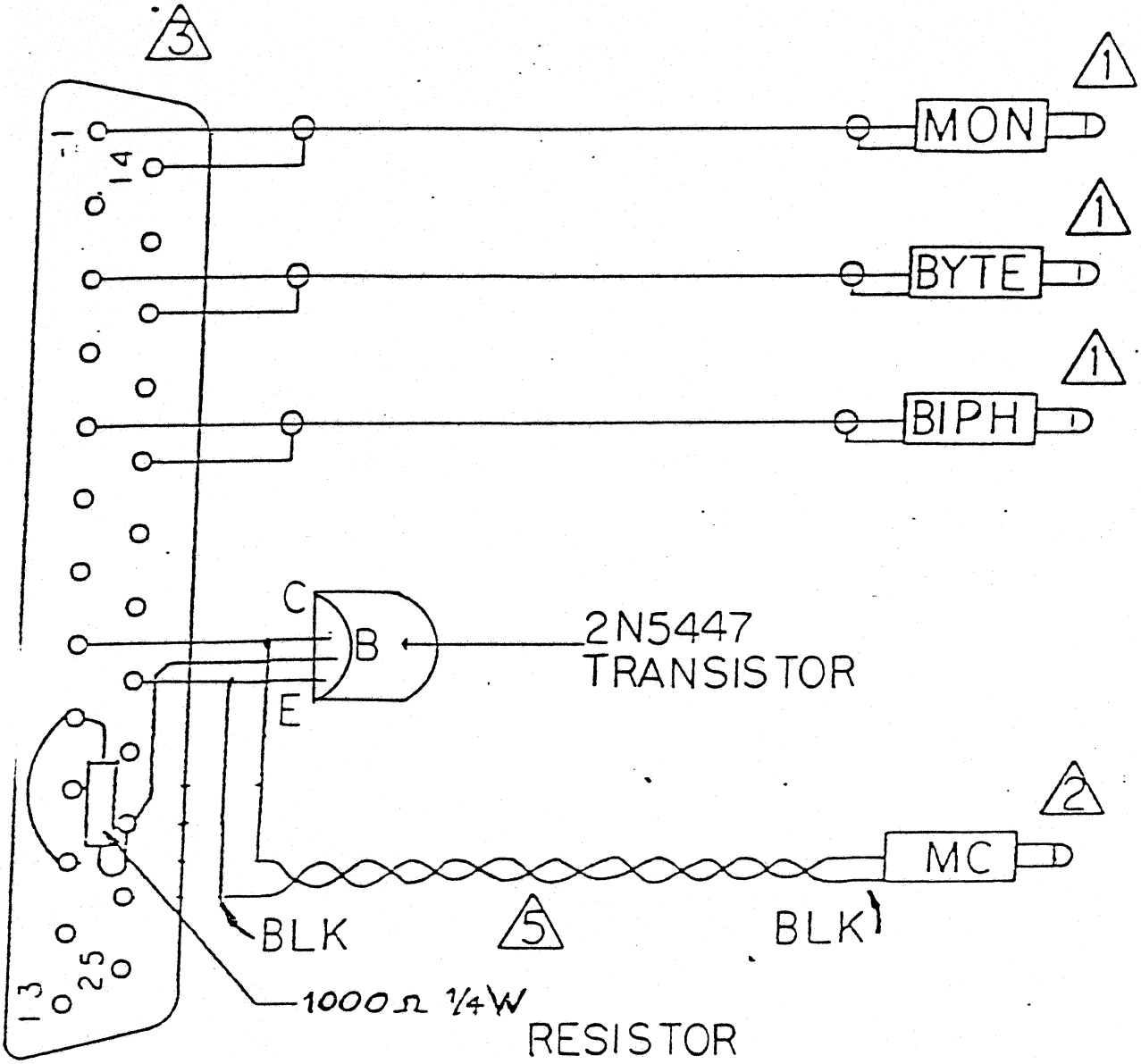


Use with Type A

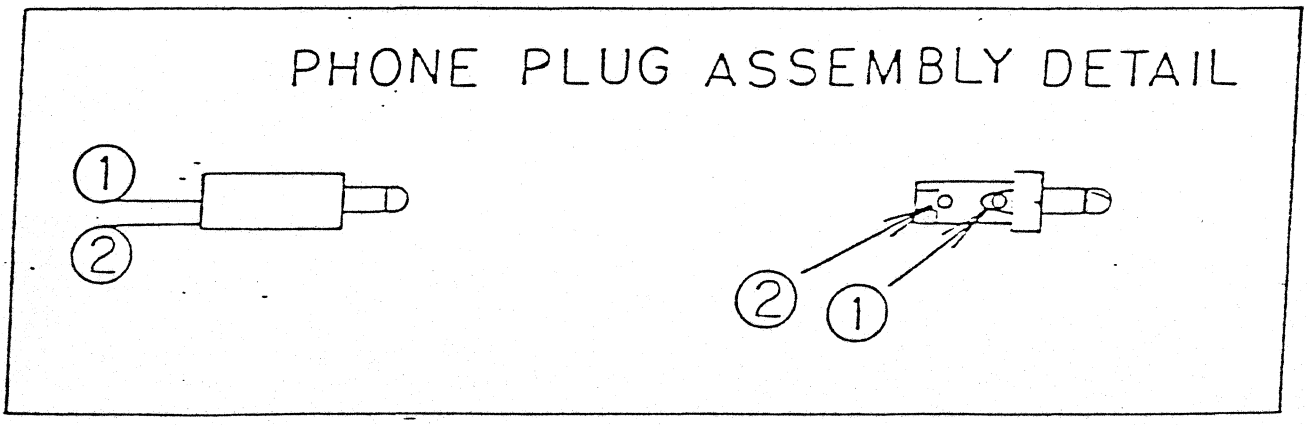
Sony TC110B
Pansonic RQ4135

* See page six for model recommendations.

TAPE RECORDER CABLE



PHONE PLUG ASSEMBLY DETAIL

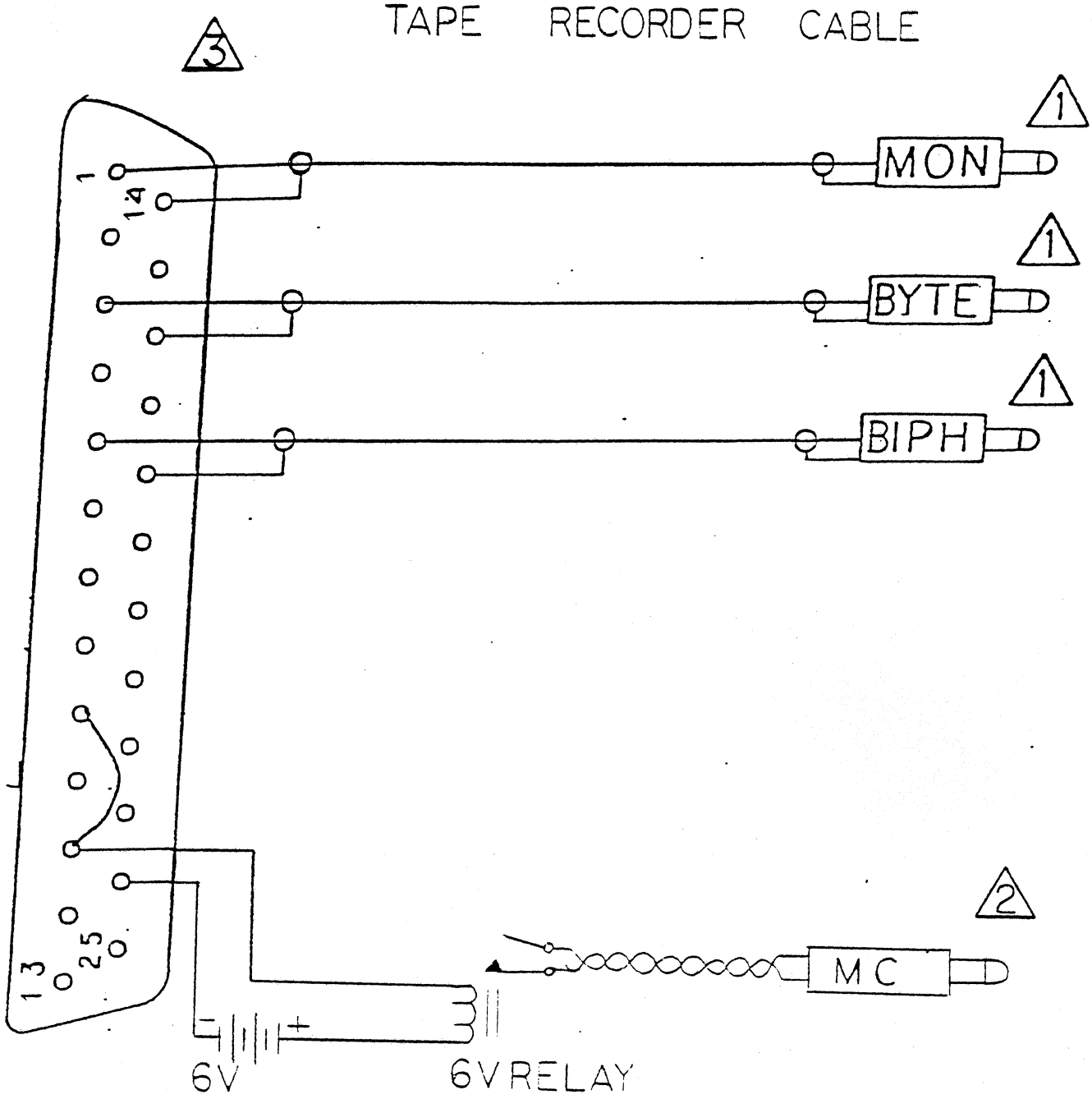


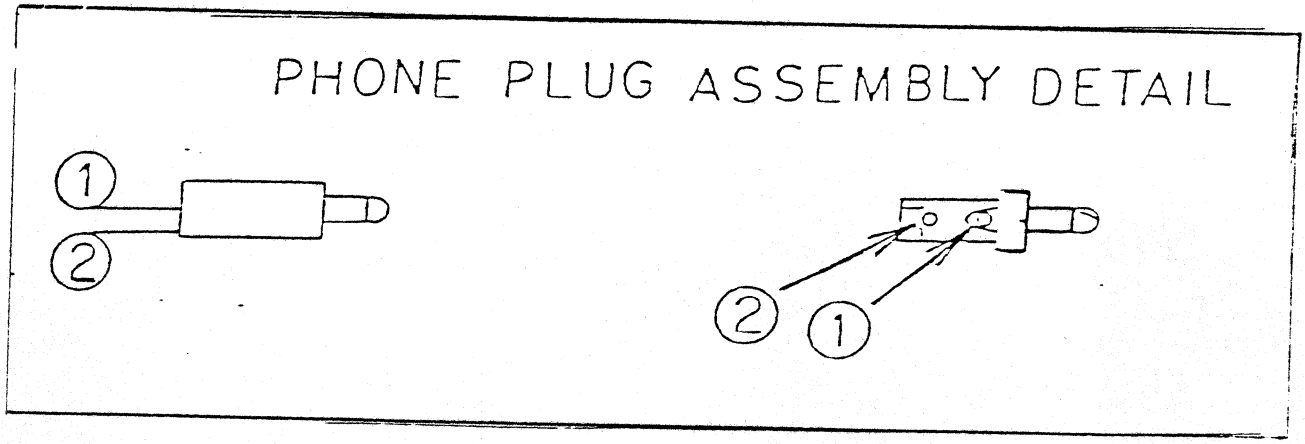
Use with Type A or B

Superscope	C103
"	C104
Sears	799.21682501
Panasonic	RQ413E
Sony	TC110B

* See page six for model recommendations

TAPE RECORDER CABLE





TYPE A,B,C OR D RECORDER

If you have any questions about monitor commands for cassette usage, refer to the appropriate Poly 88 manual section.

Recorder controls must be set properly for reliable operation. The two controls of importance are TONE and VOLUME.

Tone Control. The tone control(s) must be set for flat response over the frequency range used by the interface. On most portable recorders with a single tone control, adjust the control to full treble. This keeps the treble circuit from clipping higher frequencies. With higher quality recorders having two or three tone controls, set all controls to the center of their range.

Volume control. The cassette interface input requires a nominal 2 volt p-p signal. At this level, the interface has sufficient input to recover the signal without clipping it.

The required volume setting varies from recorder to recorder. To determine the optimum setting for your recorder with an oscilloscope find the setting for a 2 volt p-p signal at the speaker output (labeled monitor output on some recorders). Use a prerecorded digital tape. If you do not have access to an oscilloscope, you must use a trial and error method. Start with a low volume setting and try to read a prerecorded digital tape. If errors occur (question mark on the screen), stop the tape and rewind it. Turn up the volume control slightly and repeat until you can just recover data without mistakes. Make note of this setting. Continue increasing the volume in small steps as above until mistakes occur again. Note this setting and use the setting half way between the two noted.

To Load into Computer

Press T
B
SMD (CR)

Tape Loaded when screen clears

SMD is a simple absolute dumper which runs entirely within the onboard monitor RAM from C6AH to D9CH. Its starting address is C6A hex. When run, it clears the screen and expects an encoding specification and filename just as the 4.Ø resident loader. After these are input, the starting and ending hex addresses are input as shown in the folloiwng example where the SMD is used to copy itself:

Key in → SPJTC6A (CR) G
(Screen Cleared, Cursor in Upper Left)

B
SMD (CR)
C6A,D9D(CR)* (D9D used for safety)
C6A
D6A
D6A (This last is an endrecord)
(Screen clears again, ready for another dump)

*Before data is dumped, the cassette recorder should be setup with the proper plug in the microphone jack. The Byte/Biphase cassette card has two plugs for writing - one for byte and one for biphase. The read plug (labelled usually "EAR" or "SPKR") should not be plugged in. Also make sure that enough tape runs before typing the final carriage return on the end address specification so that non-recordable leader gets a chance to pass by before dumping starts.

The onboard dumper was hand optimized to fit inside the free space on system RAM, but the system stack also resides there. This means that the stack may over-run the dumper, erasing part of it. If the dumper has been in RAM while BASIC has been run, for example, the stack has probably squashed it at some time. If there is doubt, check the byte at D9CH. It should be a C9 (return instruction). If it is not, or you just want to make sure, reload the dumper just before using it.

When the dumper is dumping, each record will be displayed as a hex number on the screen. The hex number represents the address of the data being dumped on each record. That address is put on the header of the record so the 4.Ø resident loader will know where to put it when it is read back in.

The last record is an "END" type record. It is put on automatically. It will display as a record with dump address equal to the address of the record before it. Optimization of the dumper's code requires some strangeness such as this, but in any case, the last record (dump finished) will be signaled by the screen clearing. This puts the dumper back in its initial mode, just as if it had been restarted at C6AH. More data may be dumped if desired.

```
                        ; ******* ONBOARD DUMPER FOR 4.0 *******
                        ;
                        ;       THIS IS A POLYFORMAT DUMPER FOR ABSOLUTE
                        ;DATA WHICH RUNS FROM C6A TO D9F (OR SO), START ADDRESS
                        ;C6AH.  WHEN RUN, IT ACTS LIKE 4.0 MONITOR TAPE LOAD IN
                        ;THE WAY IT ACCEPTS ENCODING SPECIFICATION (B OR P) AND
                        ;FILE NAME.  THEN IT EXPECTS TWO HEX NUMBERS FOR
                        ;START AND END DUMP ADDRESSES.  EACH RECORD DUMPED SHOWS
                        ;ADDRESS USED IN HEX ON SCREEN.  WHEN DONE, IT PUTS OUT
                        ;AN "END" TYPE RECORD AND CLEARS SCREEN, READY
                        ;FOR ANOTHER DUMP.
                        ;
                        ;ORIGINAL 2.2 DUMPER SYSTEM WRITTEN BY DAVID FAIMAN
                        ;REWRITTEN,DOCUMENTED AND CONVERTED TO ONBOARD FOR 4.0
                        ;BY R.L.DERAN
                        ;
                        ;
0C20                    WH0     EQU     0C20H
0C24                    WH1     EQU     0C24H
0C16                    SRA4    EQU     0C16H
02AD                    SETUP   EQU     02ADH
03AA                    HEXC    EQU     03AAH
03D1                    DEOUT   EQU     03D1H
0C5A                            ORG     0C5CH-2
0C5A                    LENGTH: DS      2
0C5C                    WNAME:  DS      8
0C64                    WRN:    DS      2
0C66                    WLEN:   DS      1
0C67                    WADR:   DS      2
0C69                    WTYPE:  DS      1
0C6A 21450D             START:  LXI     H,TISR
0C6D 22160C                     SHLD    SRA4
0C70 3E0C               STAR2:  MVI     A,0CH   ;FORM FEED
0C72 CD240C                     CALL    WH1     ;CLEAR SCREEN
0C75 CD200C                     CALL    WH0
0C78 CD240C                     CALL    WH1
0C7B FE42                       CPI     'B'
0C7D CA920C                     JZ      BITE
0C80 FE50                       CPI     'P'
0C82 C2700C                     JNZ     STAR2
0C85 CDAD02             POLY:   CALL    SETUP
0C88 05                         DB      005H
0C89 AA                         DB      0AAH
0C8A 40                         DB      040H
0C8B 0C                         DB      00CH
0C8C E6                         DB      0E6H
0C8D E6                         DB      0E6H
0C8E 00                         DB      000H
0C8F C39A0C                     JMP     NAMER
0C92 CDAD02             BITE:   CALL    SETUP
0C95 06                         DB      006H
0C96 AA                         DB      0AAH
0C97 40                         DB      040H
```

```
0C98 CE                 DB      0CEH
0C99 00                 DB      000H
                ;
                ;       NAMEING ROUTINE
                ;
0C9A 210000     NAMER:  LXI     H,0
0C9D 22640C             SHLD    WRN
0CA0 0E08               MVI     C,8     ;BLANK NAME FIELD
0CA2 21630C             LXI     H,WNAME+7
0CA5 3620       NAM:    MVI     M,020H
0CA7 2B                 DCX     H       ;BACKUP H TO WNAME
0CA8 0D                 DCR     C
0CA9 C2A50C             JNZ     NAM
0CAC 23                 INX     H
0CAD 0E08               MVI     C,8
0CAF CD180D             CALL    CRLF
0CB2 CD200C     NAM0:   CALL    WH0
0CB5 CD240C             CALL    WH1
0CB8 FE0D               CPI     00DH    ;CR
0CBA CAC30C             JZ      DUMPC
0CBD 77                 MOV     M,A
0CBE 23                 INX     H
0CBF 0D                 DCR     C
0CC0 C2B20C             JNZ     NAM0
0CC3 AF         DUMPC:  XRA     A
0CC4 32690C             STA     WTYPE
0CC7 CD180D             CALL    CRLF
0CCA CDAA03     SIZE:   CALL    HEXC
0CCD 22670C             SHLD    WADR
0CD0 78                 MOV     A,B
0CD1 CD240C             CALL    WH1
0CD4 EB                 XCHG
0CD5 CDAA03             CALL    HEXC
0CD8 CD180D             CALL    CRLF
0CDB 7D                 MOV     A,L
0CDC 93                 SUB     E
0CDD 6F                 MOV     L,A
0CDE 7C                 MOV     A,H
0CDF 9A                 SBB     D
0CE0 67                 MOV     H,A
0CE1 225A0C             SHLD    LENGTH
0CE4 CDF60C             CALL    DUMPR
0CE7 3E02       ENDC:   MVI     A,2
0CE9 32690C             STA     WTYPE
0CEC 3D                 DCR     A
0CED 32660C             STA     WLEN
0CF0 CD540D             CALL    DUMP
0CF3 C36A0C             JMP     START
                ;
                ;       DUMP DATA RECORDS
                ;
0CF6 215B0C     DUMPR:  LXI     H,LENGTH+1
0CF9 7E                 MOV     A,M
0CFA B7                 ORA     A
0CFB CA100D             JZ      OVER
0CFE 35                 DCR     M
0CFF AF                 XRA     A
0D00 32660C             STA     WLEN
```

```
0D03 CD540D            CALL    DUMP
0D06 2A670C            LHLD    WADR
0D09 24                INR     H
0D0A 22670C            SHLD    WADR
0D0D C3F60C            JMP     DUMPR
0D10 2B       OVER:    DCX     H
0D11 7E                MOV     A,M
0D12 32660C            STA     WLEN
0D15 C3540D            JMP     DUMP
                ;
0D18 3E0D     CRLF:    MVI     A,0DH
0D1A CD240C            CALL    WH1
0D1D C9                RET
                ;
                ;       ROUTINE TO OUTPUT A RECORD
                ;
0D1E 0600     PUT:     MVI     B,0     ;CLEAR CHECKSUM
0D20 4F                MOV     C,A     ;PUT LENGTH OF RECORD IN C
0D21 7E       PUT0:    MOV     A,M
0D22 23                INX     H
0D23 F5                PUSH    PSW
0D24 80                ADD     B
0D25 47                MOV     B,A
0D26 F1                POP     PSW
0D27 CD340D            CALL    TO
0D2A 0D                DCR     C
0D2B C2210D            JNZ     PUT0
0D2E 78                MOV     A,B
0D2F 2F                CMA
0D30 3C                INR     A
0D31 C3340D            JMP     TO
                ;
                ;       TAPE OUTPUT ROUTIME
                ;
0C08          TBUFF    EQU     0C08H
0D34 E5       TO:      PUSH    H
0D35 21080C            LXI     H,TBUFF
0D38 F5                PUSH    PSW
0D39 7E       TO1:     MOV     A,M
0D3A B7                ORA     A
0D3B C2390D            JNZ     TO1
0D3E 23                INX     H
0D3F F1                POP     PSW
0D40 77                MOV     M,A
0D41 2B                DCX     H
0D42 34                INR     M
0D43 E1                POP     H
0D44 C9                RET
                ;
                ;       TISR IS A SIMPLE USART READER WHICH WILL
                ;       RE-TRANSMIT THE CHARACTER IN TBUFF IF IT HAS NOT
                ;       BEEN REPLACED BY THE WORMHOLE ROUTINE.  IT
                ;       DOES NOT CHECK THE FLAG, BECAUSE IT ASSUMES
                ;       THAT THE PROGRAM CALLING THE WORMHOLE IS FASTER
                ;       THAN THE USART AND SO IT ALWAYS HAS A VALID
                ;       CHARACTER FOR US TO TAKE.
                ;
0D45 AF       TISR:    XRA     A
```

```
0D46 32080C            STA     TBUFF
0D49 3A090C            LDA     TBUFF+1
0D4C D300              OUT     0
0D4E E1        IORET:  POP     H
0D4F D1                POP     D
0D50 C1                POP     B
0D51 F1                POP     PSW
0D52 FB                EI
0D53 C9                RET
                ;
                ;       DUMP PUTS OUT ONE COMPLETE RECORD.
                ;       IT TURNS ON USART AND MOTORS,WAITS A WHILE
                ;       FOR AN IRG, PUTS OUT 64 SYNCH CHARACTERS,
                ;       DUMPS A RECORD ACCORDING TO THE WRITE CONTROL
                ;       BLOCK  AT WNAME (IT ALSO PUTS THE WCB
                ;       ON THE RECORD AS HEADER), INCREMENTS THE RECORD
                ;       NUMBER, STOPS USART AND MOTORS, AND RETURNS.
                ;
0D54 3E21      DUMP:   MVI     A,021H
0D56 D301              OUT     1
0D58 2A670C            LHLD    WADR
0D5B EB                XCHG
0D5C CDD103            CALL    DEOUT   ;DISPLAY THE ADDRESS WE'RE DUMPI
0D5F CD180D            CALL    CRLF
0D62 21FF8F            LXI     H,08FFFH
0D65 2B        DELAY:  DCX     H
0D66 7C                MOV     A,H
0D67 B7                ORA     A
0D68 C2650D            JNZ     DELAY
0D6B 0E40              MVI     C,64
0D6D 3EE6              MVI     A,0E6H  ;SYNC CHARACTER
0D6F CD340D    DUMP0:  CALL    TO
0D72 0D                DCR     C
0D73 C26F0D            JNZ     DUMP0
0D76 3E01              MVI     A,001H  ;START OF HEADER
0D78 CD340D            CALL    TO
                ;
                ;       DUMP HEADER AND DATA RECORDS
                ;
0D7B 3E0E              MVI     A,00EH  ;LENGTH OF HEADER RECORD
0D7D 215C0C            LXI     H,WNAME
0D80 CD1E0D            CALL    PUT
0D83 3A660C            LDA     WLEN
0D86 2A670C            LHLD    WADR
0D89 CD1E0D            CALL    PUT
0D8C 21640C            LXI     H,WRN
0D8F 34                INR     M
0D90 AF        OFF:    XRA     A
0D91 CD340D            CALL    TO      ;THESE PUSH OUT LAST BYTES FROM
0D94 CD340D            CALL    TO      ;THE USART AND WH BUFFER PIPELIN
0D97 CD340D            CALL    TO      ;TURN OFF MOTOR AND TRANSMITTER
0D9A D301              OUT     1
0D9C C9                RET
0000                   END
```

THE FOLLOWING MODIFICATION IS REQUIRED TO THE CASSETTE BOARD FOR REVISIONS UP TO 1.2.

1. Remove R17, R19, R14, C7 and C12
2. Change R18 from 100K to 82K ¼W
3. Cut trace from pin 3 of IC5 to R18 SHT.3
4. Cut trace from pin 5 to pin 13 on IC4 SHT.3
5. Cut trace from pin 6 of JI to pin 7 of IC4 SHT.3
6. Cut trace from pin 6 to common on IC4 SHT.4
7. Cut trace from pin 5 to pin 6 on IC4 SHT. 4
8. Jumper pin 8 to pin 13 on IC4 SHT. 5
9. Jumper pin 1 of IC4 to pin 6 of JI SHT. 5
10. Jumper pin 5 of IC4 to pin 1 of IC6 SHT. 5
11. Jumper pin 7 of IC4 to R18 top SHT. 5
12. Jumper pin 6 of IC4 to pin 3 of IC5 SHT. 5
13. Cut trace at Jumper #1 SHT. 4
14. Cut trace at Jumper #2 SHT. 4

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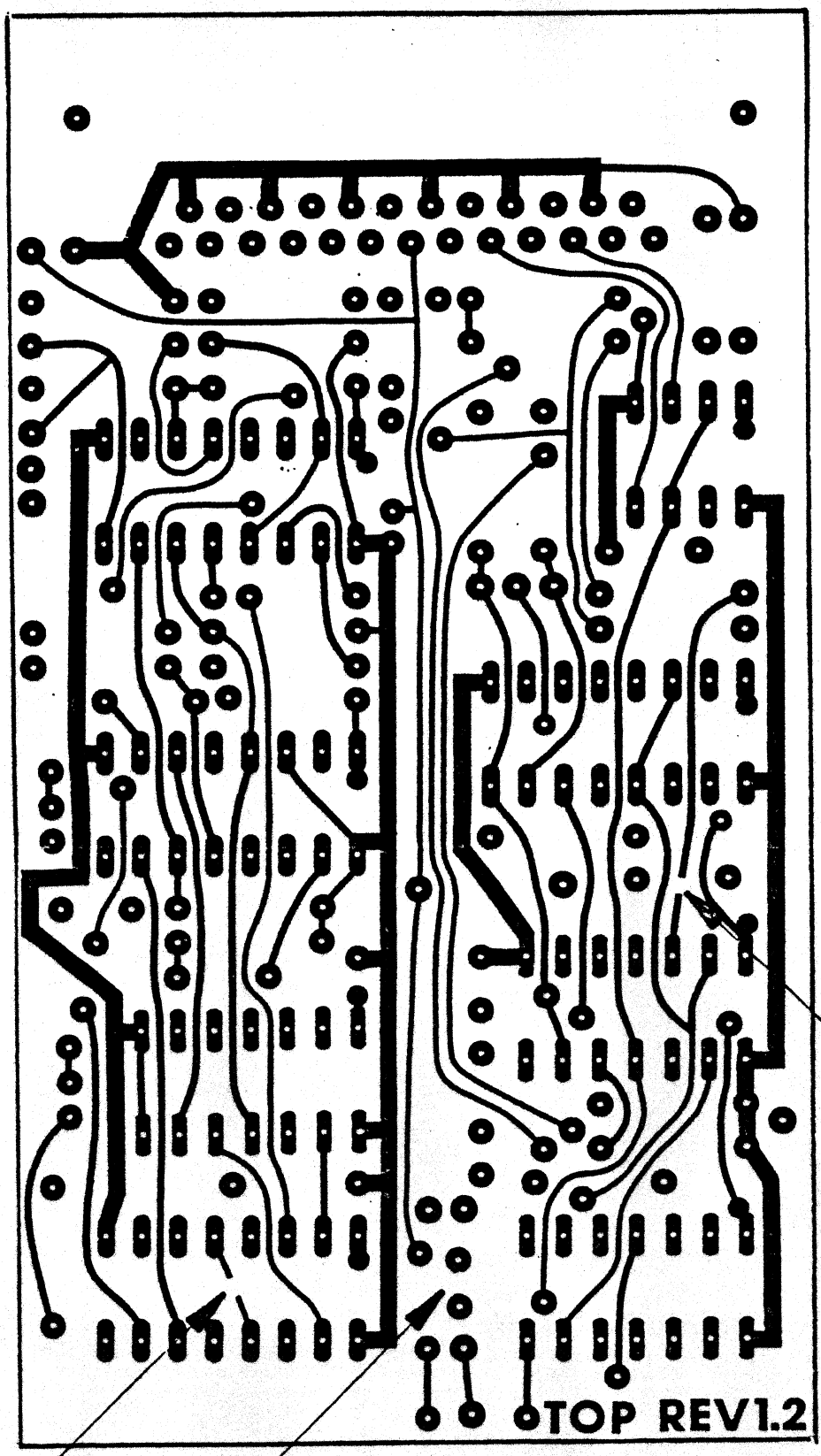

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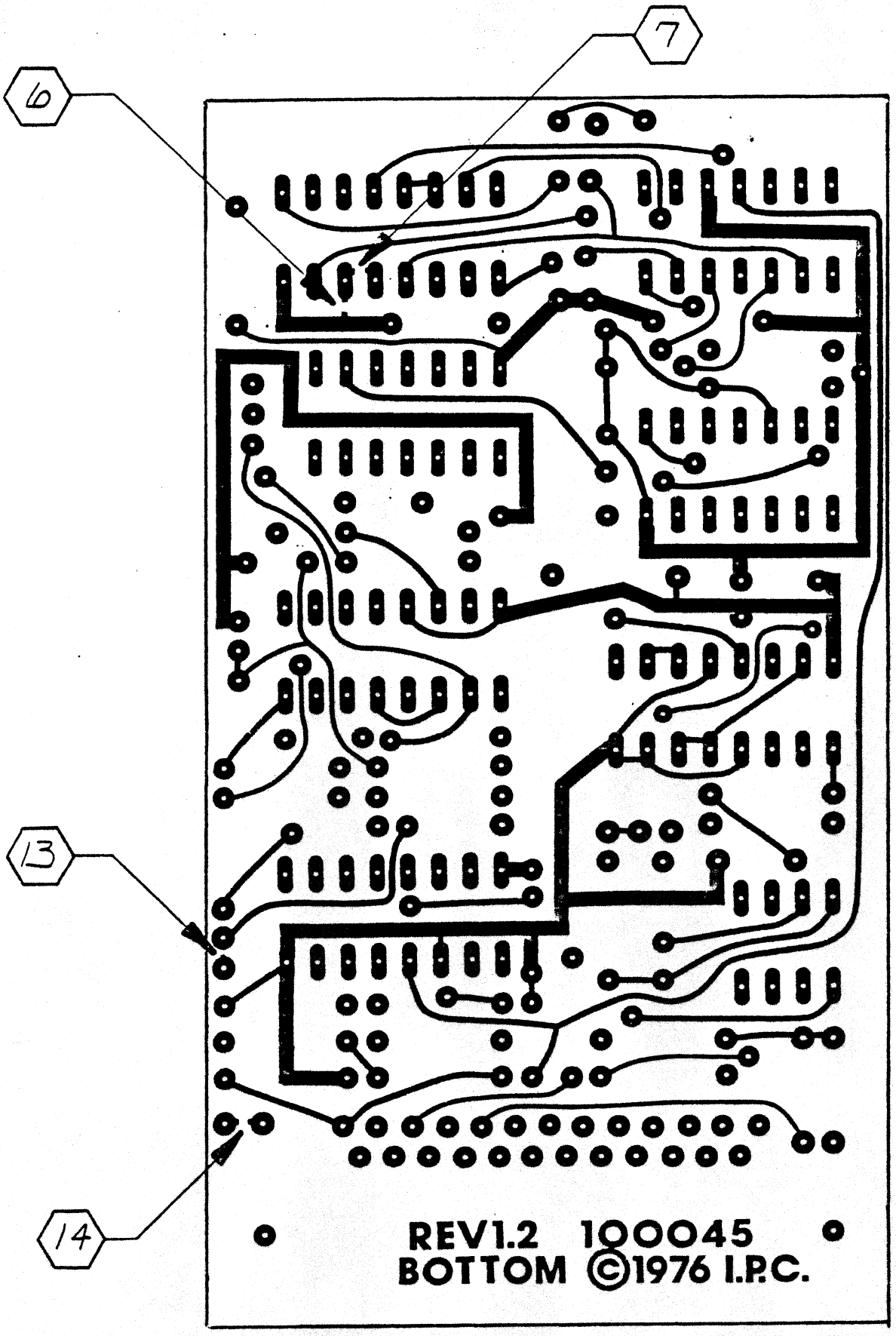

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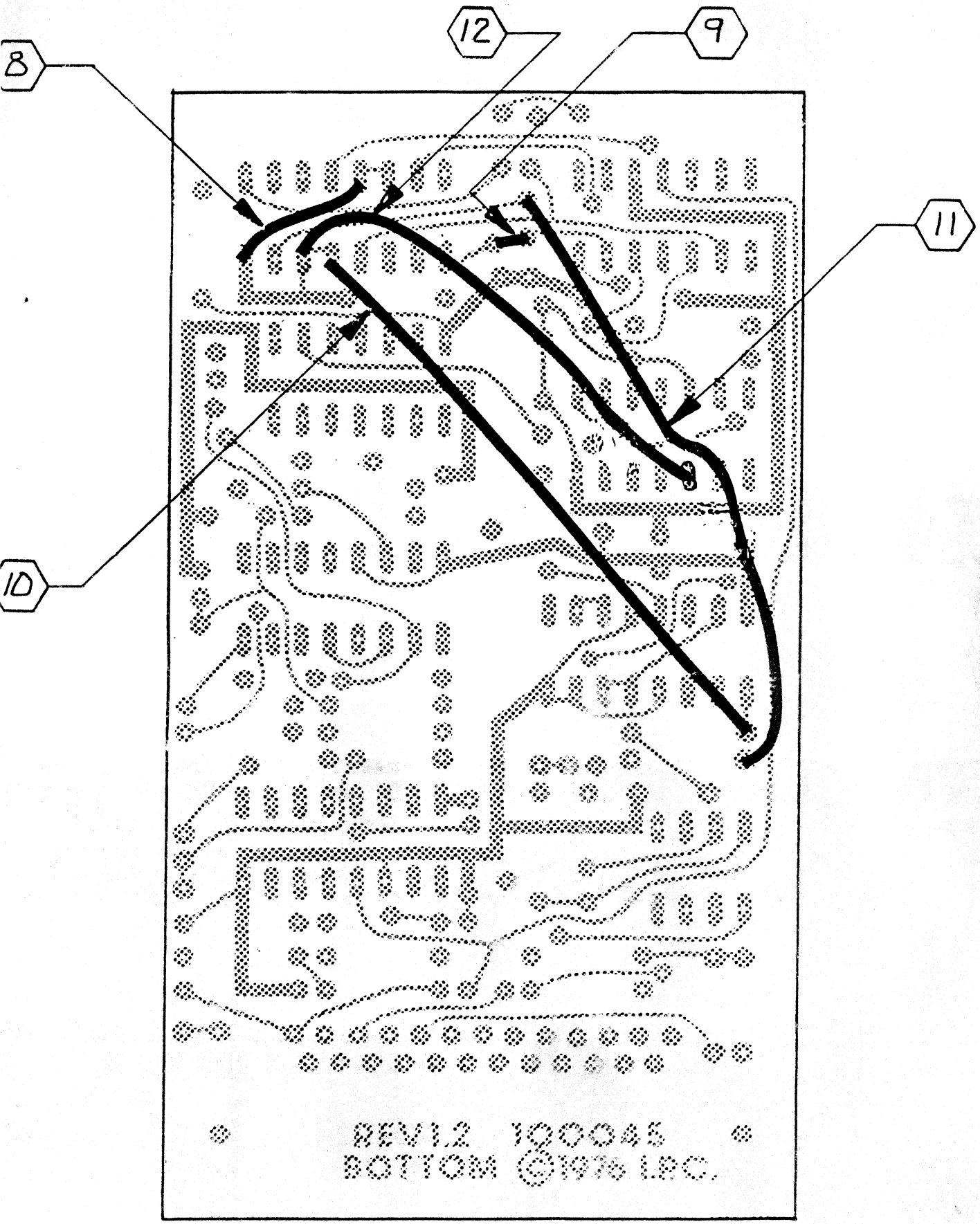

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