Data Sheet
No. 1-410

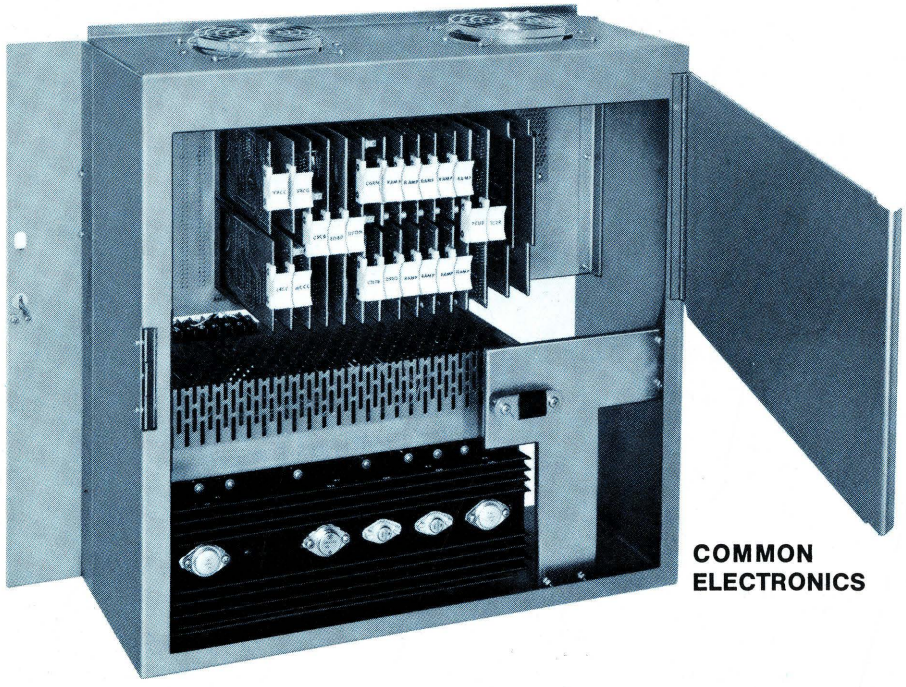
Potter

MA 360 Read/Write Switching Amplifier

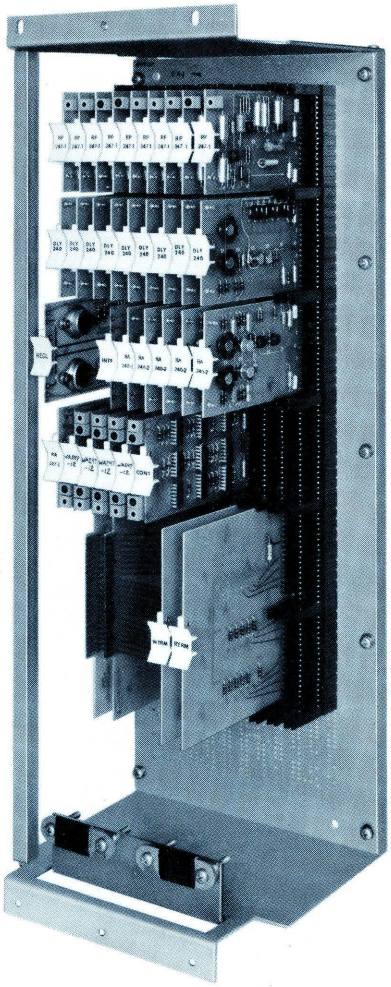
Total NRZI Performance for Potter Magnetic Tape Transports

FEATURES

- Industry Compatible NRZI Read/Write Operation
- Logic Sharing of up to 8 Tape Transports
- Operation From 25 to 200 ips
- Data Integrity Check-Read Insures Data Reliability
- Read Reverse Capability



COMMON ELECTRONICS



LOCAL AMPLIFIER

THE MA 360 READ/WRITE SWITCHING AMPLIFIER is designed for the OEM user who requires the latest technology with the highest degree of reliability. It is ideally suited for single speed applications (25-200 ips) with up to 8 Potter SC 1051, SC 1081, AT 1082 or AT 1092 Single Capstan Magnetic Tape Transports. Utilizing advanced integrated circuitry the unit will record digital information on magnetic tape, then check-read that data to insure recording accuracy. The MA 360 Amplifier is IBM-compatible for 200/556/800 bpi NRZI operation, and all 7 track units are prewired for immediate field expansion to 9 track, 800 bpi compatible operation. Each MA 360 Amplifier is modular in construction and is physically divided into two separate sections, common electronics and local amplifiers.

THE MA 360 COMMON ELECTRONICS accommodates up to eight local amplifiers and serves as the control point for the system. It handles all transport commands, replies to and from the computer, and performs transport selection, read digitizing output, read strobe and read/write enable functions.

THE MA 360 LOCAL AMPLIFIER contains all static skew compensation circuits, thereby establishing plug-to-plug interchangeability between "local" tape transports. The local amplifier contains: (1) 7 (or 9) identical circuits which receive read head signals and subsequently accomplish required amplification, and deskewing functions; (2) 7 (or 9) write circuits with deskewing and symmetry adjustment. Tape interchangeability between IBM-compatible tape transports is assured.

MAINTENANCE is rarely required, but quickly accomplished when needed. Test points are provided at the front of chassis so that most adjustments may be made with the modules in their normal position. Extension frames permit complete module exposure for circuit testing under actual operating conditions. Output and power circuits are short-circuit proof. A rugged, value-engineered design assures long life with minimum maintenance.

ADDITIONAL MA 360 FEATURES include:

- Operation in simultaneous read/write mode.
- Logic sharing of up to 8 tape units.
- Read reverse capability.
- Information transfer rates to 160,000 cps.
- Accurate read/write deskewing.
- Compensated writing of the longitudinal redundancy check character (7 & 9 track).
- Strobed write input.
- Individual adjustments for pulse pairing by write amplifier compensation.
- In-line read output of all character bits and clock pulse output.
- Two standard threshold levels; check-read and read.
- Automatic reduction of strobe delay during check read operation.
- Peak detectors employed in read amplifiers.
- Multiple select error indicator.
- Write memory status.
- Remote density select.
- Provision for ODD or EVEN lateral parity read generation and/or check (7 track).

SPECIFICATIONS

	7 TRACK COMPENSATED	9 TRACK COMPENSATED
Packing Density	200/556/800 bpi	800 bpi
Writing Mode	NRZI	NRZI
Tape Speed (Single)	25-200 ips (simultaneous read/write)	25-200 ips (simultaneous read/write)
Read Direction	FWD/REV	FWD/REV
Compatible Head Types Simultaneous Read/Write Operation (Dual Gap)	LD 702	LD 902

Power Supply — Local ..... Input power provided by power supply modules in Single Capstan Series Tape Transports.

PS1087 ..... Integral power supply for the common electronics.

Dimensions ..... Designed to be mounted internally in Potter SC & AT Series Tape Transports.

	Height	Width	Depth
Local	25¼"	8½"	7½"
Common	18½"	22¼"	7½"

Weight ..... Local — 14 lbs. maximum, Common — 36 lbs. maximum

INPUT/OUTPUT LINES

INPUT LINES

Input Levels (available in standard logics)	Logic "1" Logic "0"	0V ±.7V at 28 ma +5V ±1V 3 ma
Write Inputs (7 and 9 lines)	Level (NRZ)	A "1" is written on tape when the input is at "1" at write clock time.
Write Clock	Pulse	All Write inputs are simultaneously enabled when the Write Clock line is raised to the level corresponding to Logic "1" Level and a "1" is written by all Write input lines which are at Logic "1" Level. Pulse width 1-2 μs.

INPUT/OUTPUT LINES (Continued)

Write Mode	Level	Enabled with Logic "1" signal. (Simultaneous Erase head enable.)
Write Reset	Pulse	Reset with Logic "1" signal. Pulse width is 1-2 μs.
Density Select — 200	Level	Selected with Logic "1" signal (optional).
Density Select — 556	Level	Selected with Logic "1" signal (optional).
Even Lateral Parity Select (optional)		EVEN selected with Logic "1" signal.
Read Enable	Level	Enables Read Amplifiers when at Logic "1".
Address Lines		Four binary coded lines.

OUTPUT LINES

Output Levels (available in standard logics)	Logic "1" Logic "0"	Ground $\pm$.7V 35 ma source capability. +5VDC $\pm$1.0V 3 ma
Read Outputs	Level (NRZ)	"1" for output line at Logic "1".
Clock Output	Pulse	1.0 microsecond duration.
Data Error	Level	Set to Logic "1" on detection of a data error. Reset to Logic "0" when Read Enable goes to Logic "0".
End of Block	Pulse	1 microsecond duration.
Multiple Select	Level	Two, or more, transports responding to address.

In addition to the above Input/Output lines associated with the MA 360, all transport interface signals are routed through the Common Electronics.

INPUT

Run	Level	A "1" causes addressed transport to run.
Direction	Level	A "1" conditions addressed transport to reverse.
Rewind	Pulse	Logic "1" causes addressed transport to rewind. Pulse width 5.0 μs minimum.
Rewind & Unload	Pulse	Logic "1" causes addressed transport to rewind and unload. Pulse width 5.0 μs minimum.

OUTPUT

Ready	Level	Addressed transport is ready.
Rewinding	Level	Addressed transport is rewinding.
Write Ring In	Level	Addressed transport has Write Ring.
Write Status	Level	Addressed transport is in Write Status.
EOT	Level	Addressed transport is at EOT.
BOT	Level	Addressed transport is at BOT.
Seven Track	Level	Addressed transport is Seven Track.

FUNCTIONAL DESCRIPTION OF MODULES

		9 TRACK		7 TRACK	
		CE CHASSIS	LOCAL CHASSIS	CE CHASSIS	LOCAL CHASSIS
		800 BPI		200/556/800 BPI	
Local Chassis MA 360L		One Local Chassis Required Per Transport			
CE Chassis MA 360C		One CE Chassis Required Per System			
Read Pre Amp RP 247	Provides linear amplification of playback signals. One circuit per board.		9		7
Read Amp RA 240-2	Two linear signal drivers per board.		4		3
Read Amp RA 240-1	One linear signal driver per board.		1		1
Deskew Delay DLY 240	Provides forward and reverse read deskewing by means of a tapped lumped delay line. One circuit per board.		9		7
Write Amp WA 247-12	Provides write flip-flops, write asymmetry adj. and write skew one shots for compensated operation. Two circuits per board.		5		4
Interface Bd. INTF	Generates replies for the CE and TCU. Detects multiple select error when more than one transport respond to the address lines.		1		1
Control Bd. CONT	Controls write functions and forward and reverse read deskew delay selection. (See note 1)		1		1
Jumper Bd. JUMP	Jumpers read signals into the daisy chain. (See note 2)		3		3
Terminator Boards WTRM RTRM	Termination resistors for the daisy chain. Fitted to the last R/W chassis in the chain. (See note 2)		 1 1		 1 1

FUNCTIONAL DESCRIPTION OF MODULES (Continued)

		9 TRACK		7 TRACK	
		CE CHASSIS	LOCAL CHASSIS	CE CHASSIS	LOCAL CHASSIS
		800 BPI		200/556/800 BPI	
Regulator Board REGL ZENR	Accepts voltage lines from the transport and generates supplies required by the local amplifier		1 (SC1081) (AT1082) 1 (SC1051)		1 (SC1081) (AT1082) 1 (SC1051)
Receiver Board FXAJ	Receives write data lines from CE		1		1
Read Amp RAMP	Processes linear read signals from the daisy chain. Threshold levels for check and read are selected automatically. One channel per board.	9		7	
Data Register DREG	Provides deskew and output buffering.	1		1	
Clock Gen. CGEN	Generates system clocks at 20 times bit rate. Density selection (200/556/800 bpi) is by interface lines.	1		1	
Counter CNTR	Eight stage binary counter driven by the clock generator.	1		1	
Data Control DCON	Generates read and check read strobe gates by decoding counter outputs. Generates read clocks to channel, detects missing characters and excessive write skew. Contains error flop.	1		1	
Controller Receiver TCUR	Contains line receivers. (See note 1)	1		1	
Controller Drive TCUD	Contains line drivers.	1		1	
Daisy Chain Receiver DCHR	Contains daisy chain receivers.	1		1	
Daisy Chain Driver DCHD	Contains daisy chain drivers. (See note 1)	1		1	
Extension EX 06	Extension frame for double boards.	1	1	1	1
Extension EX 05	Extension frame for single boards.	1	1	1	1
End of Block Detection EOBD	Signals EOB and checks character gap centers. Generates read clocks for CRC and LRC. (See note 1)	OPTIONAL One each in CE chassis. When VRCC or LRCC are used, EOB is also required. When VRCG is used, WCCC is also required. When CRCB is used to generate, WCCC is also required. When CRCB is used for checking, EOB is required.			
Cyclic Redundancy Check CRCB	Generates a CRC byte from write or read data.				
Write Check Character Check WCCC	Controls EOB write operation.				
Vertical Parity Gen. VRCG	Provides vertical parity generation (odd or even for 7 track).				
Vertical Parity Check VRCC	Provides vertical parity checking for up to 9 tracks (odd or even for 7 track).				
LRC Check LRCC	Provides LRC checking				
Power Supply PS 1087	Integral power supply for the common electronics. (Power for local chassis supplied by the transport)	1		1	

Notes:

1. The following circuit options are available on a no charge basis and must be specified when ordering.
   - A. Controller receiver — FWD/STOP — REV/STOP or RUN/STOP — REV/FWD.
   - B. Control board — write enable flop reset by FWD read command and on reverse and local or on reverse and local only.
   - C. Daisy chain driver — permit external *or* internal CRC clocking.
   - D. End of block detection — provide EOB pulse only *or* EOB and check gap pulses.
2. Transports in the daisy chain require 3 jumper boards. Single transports or last transport in the daisy chain requires one jumper board and one each terminator board (WTRM, RTRM).

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