OEM/SERVICE MANUAL

DISKOS 3450
DISKOS 7050

EIGHT INCH
WINCHESTER
DISC DRIVES

PRIAM

PRIAM

8-Inch Winchester Disc Drives
OEM/Service Manual

JULY 1982

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Changes to this Manual

This manual will be changed periodically to keep it current with improvements as we make them. Changes start with Field Engineering Bulletins that alert field service technicians to critical problem areas and changes in maintenance procedures. After a series of these notes are issued or a critical one is issued, we will publish changed pages, which are the remove-the-old and insert-the-new type. A vertical bar in the margin of the changed page indicates the revised material. After about 20% of the manual's pages are changed, we will reissue the entire manual. When PRIAM prepares a change package, it sends announcements to its users. The change packages are available upon request and without charge.

Reader Comments

If you are dissatisfied with this publication, we want to hear from you. Tell us about inaccurate information, typographical errors, or missing information. If you know a way to improve a procedure, please let us know about that, too. Please be specific and give the page number, line reference, and the paragraph number, if possible.

Change Notation

A vertical line in the outer margin of a page indicates the portion of text affected by changes. Shaded areas indicate changes to illustrations and diagrams.

The total number of pages in this document is 69.

Page No.	Change Number*	Page No.	Change No.*

Dates of issue for original and changes pages are: *0 in this column indicates an original page.

Safety Precautions

As with any electronic equipment, precautions consistent with all standard industrial safety practices must be observed while servicing this equipment since it contains potentially dangerous voltages. Any servicing that requires removing cabinet covers should be performed by qualified service personnel. Always disconnect power prior to inspection or servicing.

Admonishments are included throughout this manual to alert the reader to problem areas or situations that could cause loss of data, hardware damage, or personal injury.

A WARNING statement precedes the text of procedures that, if not strictly observed, could result in injury to the service technician. A CAUTION statement precedes the text of a procedure that, if not strictly observed, could result in damage or destruction of equipment (hardware or software). A NOTE statement highlights essential operating or maintenance procedures, conditions, or clarifying facts. NOTEs also provide information that, though not necessary, is helpful to the understanding of a concept or the completion of a procedure.

The following are general safety precautions that are not related to any specific procedure and therefore do not appear elsewhere in this manual. Personnel must heed these warnings during many phases of installation and maintenance.

WARNING

KEEP AWAY FROM LIVE CIRCUITS.

Observe safety precautions at all times. Observe all the CAUTIONS and WARNINGS in this manual when working with the equipment.

DO NOT SERVICE OR ADJUST ALONE.

Never reach into the cabinet to service the equipment unless someone capable of giving aid is present.

The following WARNING applies to any service inside the equipment cabinet. It appears elsewhere in the text of this manual and is introduced here for emphasis:

WARNING

Voltage hazardous to human life are exposed in the cabinet. Use extreme caution when servicing either the power supply or any area where power terminals are exposed.

Warranty

For warranty information, contact PRIAM:

(408) 946-4600.

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1. GENERAL INFORMATION

1.1 The DISKOS 3450 and 7050 use advanced Winchester and microprocessor technologies to provide users with low-cost disc drives having high capacity, fast access, and long-term reliability. Linear motor voice coil positioners with track following servos enable the DISKOS 3450 and 7050 to position Winchester type heads quickly and precisely. These low-force heads assure high data reliability.

Advanced 8-inch Winchester-technology discs are driven by an outer-rotor, brushless DC motor. The head positioner coil and carriage, heads and discs are enclosed in a sealed, contamination-resistant chamber to assure high reliability.

One head serves each disc surface, and a full surface is dedicated to servo information for fully servoed track following, head positioning, and write timing. Three discs recorded at 480 tracks per inch are used in the DISKOS 3450 to provide a capacity of 35 megabytes, unformatted. In the DISKOS 7050, the three discs are recorded at 960 tracks per inch to accommodate 70 megabytes (unformatted) of data.

Microprocessors are used in the disc-drive electronics to provide interface flexibility and to monitor drive operation. For example, they control power up and down sequencing, and a self-test program checks drive performance during each power-up sequence. Any malfunction detected by these tests will prevent drive start-up, reducing the chance of loss of data or damage to the drive.

PRIAM disc drives are constructed in a modular fashion, so that defective assemblies can be easily replaced. This greatly reduces down time due to servicing. The three assemblies are:

Head Disc Assembly
Servo and Motor control PCB
Read/Write Digital PCB

The Head Disc Assembly (HDA) is a sealed enclosure. It contains the drive spindle assembly, drive motor, Hall Effect sensors, voice coil actuator, head carriage assembly, read/write heads, magnetic discs, and air filter assemblies.

The Servo and Motor Control PCB contains the circuitry associated with driving the spindle motor. This circuitry receives an On/Off command from the Read/Write Digital PCB, and spindle rotation feedback from the Hall Effect sensors in the HDA.

The Servo and Motor control PCB also contains the circuitry used for processing the servo signals from the servo read head, and for controlling the position of the head carriage.

The Read/Write Digital PCB contains all the circuitry associated with read/write control, command execution, and information transfers across the user interface.

1.2 Options

1.2.1 Interface Options. The PRIAM 8-inch disc drives are available with a variety of interface options. Each of these interface options can be used, without modification, on any disc drive in the 8-inch family. All PRIAM interfaces include on-board data separation.

The standard PRIAM interface is designed for low cost and for efficient use with microprocessor-based systems. Up to four drives may be daisy-chained, when this interface is used. The PRIAM interface provides a basic 8-bit bidirectional bus, which may be used with the currently popular 8-bit and 16-bit microprocessors. It also provides bit-serial NRZ data exchange. No elaborate handshaking protocols are required. The PRIAM interface is built into the disc drive's read/write digital PCB. A 50-conductor flat ribbon cable is used between the PRIAM interface and the host system.

The SMD Interface permits a PRIAM drive to be used with existing Storage Module Drive (SMD) controllers. In the 8-inch drives the SMD interface is available as an adapter which is installed between the drive electronics and the SMD controller. The line drivers and line receivers in the SMD interface are matched to those of typical SMD controllers. There are two interface cables between the host system's SMD controller and the PRIAM disc drive's SMD Interface — a 60-conductor twisted-pair flat cable ("A" cable) and a 26-conductor flat ribbon cable ("B" cable).

The ANSI interface complies with the disc drive interface standard proposed by ANSI Technical Committee X3T9. Characteristics of the ANSI interface include variable and fixed sector sizes, data transfer rates up to 10 megabits per second, and radial attention and select capability. Up to eight drives may be daisy-chained, on a single 50-conductor flat ribbon cable.

1.2.2 Interface Cables and Terminators. I/O cables are available from PRIAM, for connecting the user's controller to the PRIAM disc drive, and for connecting daisy-chained drives to one another.

Terminators are available for I/O signal lines, to minimize reflections and to ensure maximum data integrity. One set of terminators is required for a single drive, or for the last drive in a daisy chain.

1.2.3 Power Supplies and Cables. PRIAM's optional power supply allows PRIAM disc drives to operate from 100, 120, 220, and 240 VAC, 50 or 60 Hz power. The optional power supply must be mounted separately from the drive. It does not fit within the drive frame.

1.2.4 Mounting Hardware. PRIAM 8-inch drives may be mounted horizontally or vertically. Standard floppy disc mounting may be used.

Table 1-1. Specifications for PRIAM 8-inch Disc Drives

OPERATING CHARACTERISTICS	DISKOS 3450	DISKOS 7050
Capacity (unformatted)	35 MB	70 MB
Transfer rate (megabytes/second)	0.806	0.806
Track-to-track seek time (typical)	8 msec	8 msec
Average seek time (typical)	42 msec	42 msec
Maximum seek time (typical)	75 msec	75 msec
Average latency	8.3 msec	8.3 msec
Tracks per inch	480	**960**
Bits per inch	6,670	6,670
Number of data surfaces	5	5
Number of data cylinders	525	1,049
Nominal RPM	3,600	3,600
Bytes per track	13,440	13,440

Power Requirements

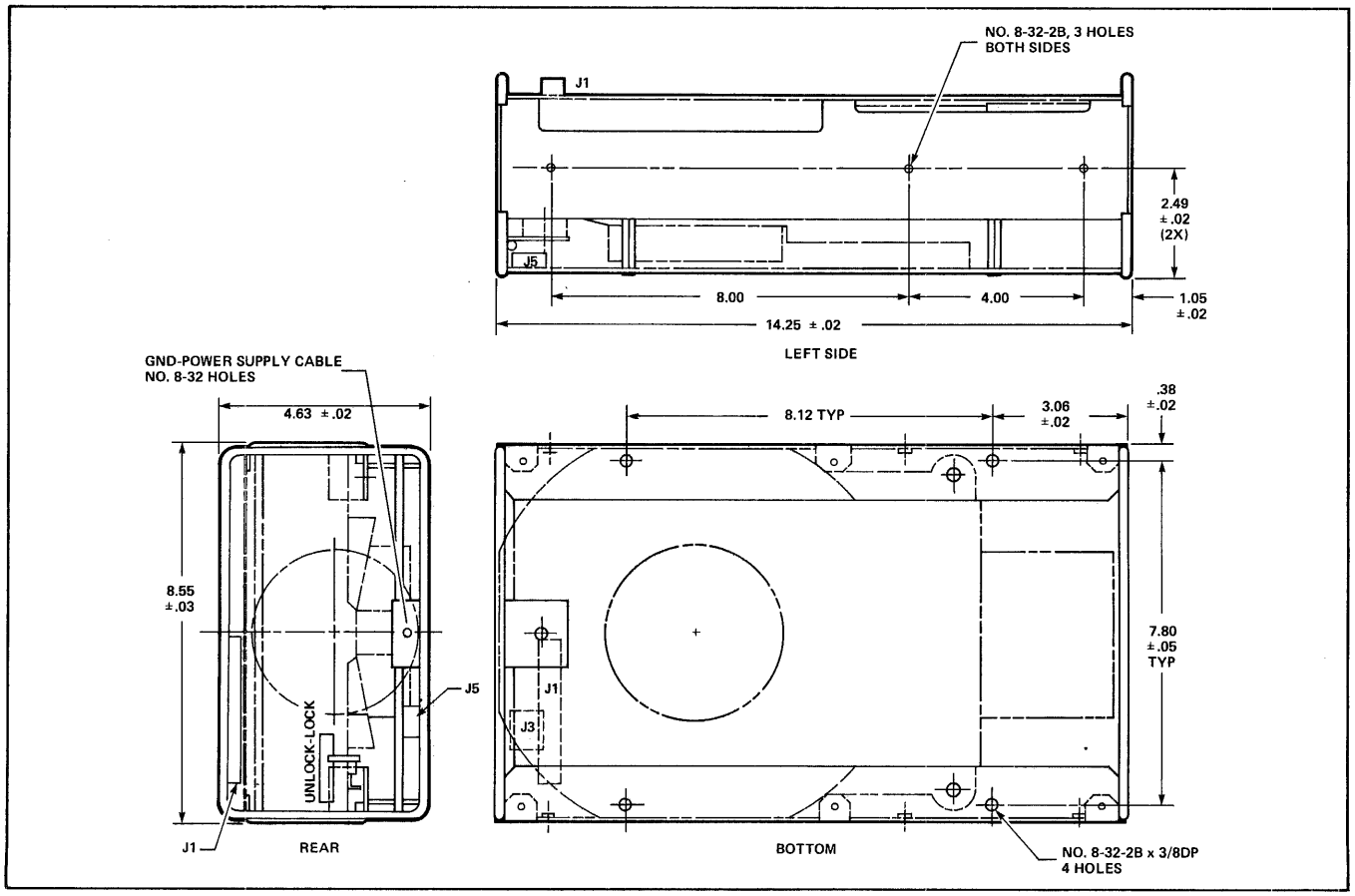
Power requirements are the same for both drives:

DC Voltage	Maximum	Typical
+24 VDC (±5%)	4.0 A	3.5 seeking 2.2 non-seeking
+5 VDC (±5%)	2.0 A	1.5 A
−5 VDC (±5%)	2.0 A	1.5 A
−12 VDC (±5%)	0.7 A	0.4 A

NOTE: This data does not include adapter/interface option power requirements.

Dimensions

Physical dimensions are the same for both drives:
Weight 20.00 pounds



2. INSTALLATION

2.0 Introduction. This Chapter contains procedures for installing the 3450 Disk Drive. It includes instructions for unpacking and inspecting, and procedures for interconnecting the equipment to the power source.

2.1 Unpacking and Receiving Inspection. When the 3450 Disc Drive is delivered by a transfer company, it must be carefully inspected (inside the shipping container as well as out) for damage. If the unit is to be reshipped, it must be repacked in a manner that will prevent damage while in transit.

2.2 Shipping Damage Inspection. Prior to accepting delivery of the 3450 Disc Drive from the carrier, carefully inspect the shipping container for obvious damage. If damage is found, note it on the waybill and require the delivery agent to sign the waybill. Notify the transfer company immediately and submit a damage report to the carrier. If no exterior damage exists, unpack the system and inspect for hidden damage.

2.3 System Unpacking. The 3450 Disc Drive is shipped with the accessories and schematics in one shipping container.

Unpack the system from the shipping container with care; avoid using sharp instruments to open the container. We recommend saving all packing materials for possible reuse in reshipping the equipment.

If hidden damage is found, immediately notify the transfer company of the damage. Save all packing materials for the transfer company's inspection, file a damage report with the carrier. Damage to the equipment is not covered under warranty. All repairs for shipping will be billed. Prompt notification of damage will ensure claim validity and will help expedite payment for necessary repairs by the transfer company or its insurance agent.

2.4 Inspection Procedures. After unpacking the 3450 Disc Drive, Inspect it thoroughly for damage hidden by the packaging and for loose components or fittings, as follows:

a. Inspect the interior for shipping damage.
b. Examine internally mounted components for loose or missing hardware.
c. Tighten all loose hardware.
d. Clean the cabinet interior by removing loose debris.
e. Check that head and spindle lock is secure.

2.5 Reshipping Procedures. Should the equipment be reshipped prepare the equipment for shipping as follows:

a. Check the integrity of the cabling and the security of internal mounting hardware.
b. Place the drive flat on a bench top and then place the spindle head lock in the LOCK position.
c. Repack the equipment in the original shipping container or other suitable materials.

Table 2.4-1. Switch Settings on the Read/Write Digital PCB

Switch # in Group	Switch Group Location on PCB	
	6K	5H
1	Drive Select 1	1 sector/track
2	Drive Select 2	2 sectors/track
3	Drive Select 3	4 sectors/track
4	Drive Select 4	8 sectors/track
5		16 sectors/track
6		32 sectors/track
7	Write Clock Off = Open On = Closed	64 sectors/track
8	On = Write Enable	See Note Below

NOTE: 128 SECTORS/TRACK

2.6 Switch Settings. The drive address, write protect parameters and sector size are all switch selectable. The switches are located on the read/write digital PCB. Referring to Figure 2-1 and to T **2.4-1**, set the switches according to the desired operating conditions.

2.7 Cabling. The power cable should be installed to connector J3 on the servo and motor control board (See Figure 2.2). The DC voltages required at the respective pins on J3 are listed in the 3.18.2 section. Interface cables to the host system are described in the sections covering each of the available interface options. Figure 2.3 shows how the interface cables are connected

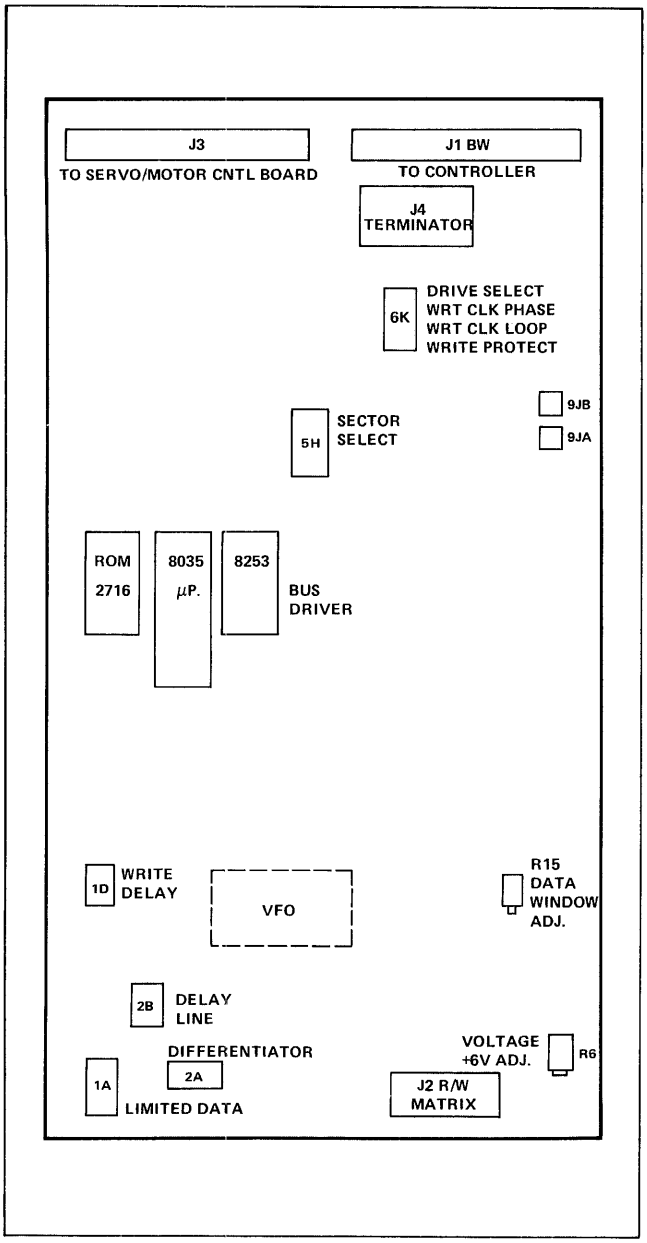


Figure 2-1. Read/Write Digital PCB

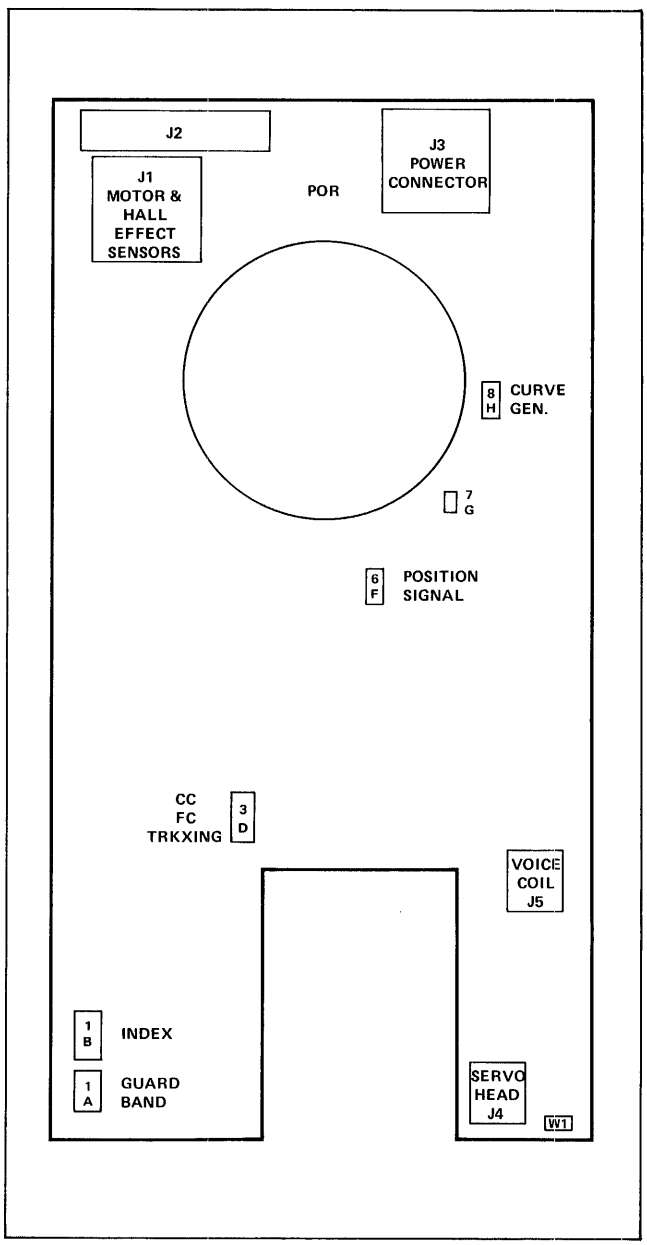


Figure 2-2. Servo and Motor Control PCB

for the PRIAM interface. Cabling between assemblies within the disc drive is completed at the factory prior to shipment. More details on inter-assembly cabling are given in the ASSEMBLY REPLACEMENT PROCEDURES section.

2.8 Unlocking. Both the drive spindle and the head carriage assembly are locked prior to shipment. After the drive has been completely mounted and cabled, these must be unlocked to enable normal operation.

The drive spindle and head carriage lock is fully accessible from one end of the HDA (Head Disc Assembly). Referring to Figure 2-4, place this lever in the UNLOCK position.

CAUTION

Avoid manual rotation of the spindle or movement of the carriage. Damage to the disc surface may occur if the heads are moved across a non-rotating disc surface. Do not move the drive with the spindle and head carriage assembly unlocked.

2.9 Locking. The drive spindle and the head carriage should be locked whenever the drive is to be physically moved, even if it is not to be shipped. To lock the drive, refer to Figure 2-4, and place the lever in the LOCK Position.

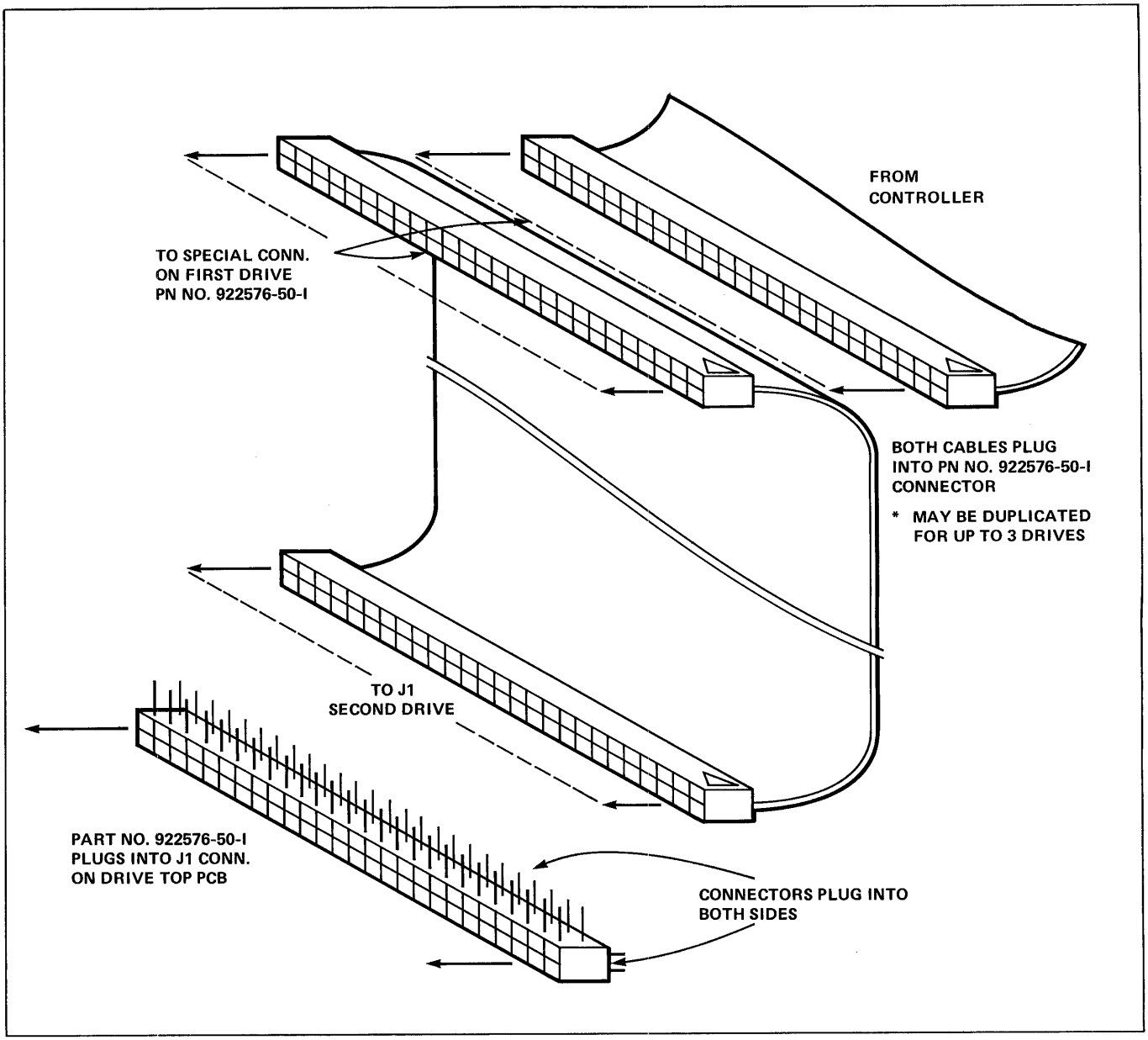


Figure 2-3. Daisy-Chaining an 8-inch Drive with PRIAM Interface

2.10 Repacking. Repacking is the reverse of the unpacking procedure. Prior to repacking the drive, make sure that the spindle and carriage lock level is in the LOCK position.

2.11 Storage. When the environment is severe, or when the drive is to be stored for a long time, it should be repacked prior to storage.

When storing unpacked drives, avoid dusty or unstable environments.

2.12 Shipping. Contact PRIAM Customer Service for a return authorization number prior to shipping a drive or assembly to PRIAM. After locking the drive spindle and head carriage, pack the drive in its original carton or an equivalent one.

2.13 Spindle and Head Locks. Before the drive can be operated, it is necessary to have the drive mounted or placed flat on a bench, then place the spindle and head lock lever in the UNLOCK position. Refer to Figure 2-4 for the location of this lever.

CAUTION

Whenever the drive is to be moved for any reason, the spindle and head lock lever should be placed in the *lock* position.

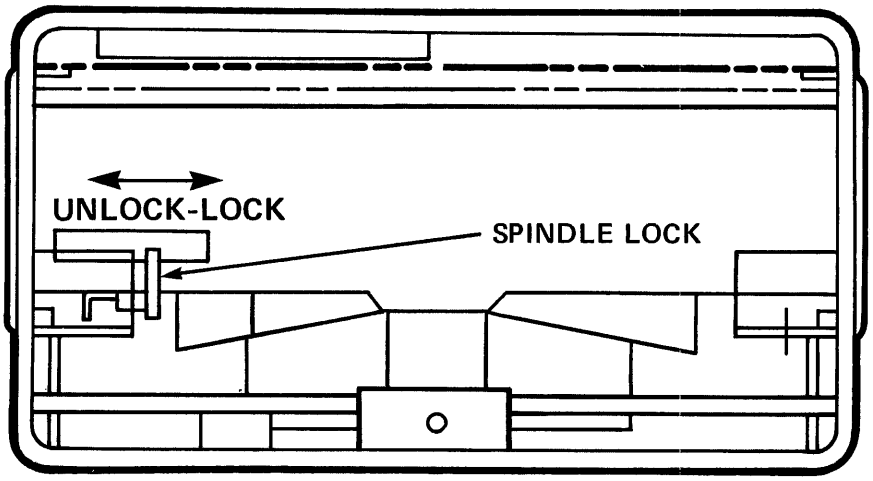


Figure 2-4. Location of Head and Spindle Lock

2.14 Powering Up/Down. The exact procedure for powering up the drive depends on the interface option present:

If the drive has a standard PRIAM interface, apply DC power, select the drive (via the -DRIVE SELECT lines) and issue a Sequence Up command.

If the drive has an SMD interface, apply DC power, select the drive (via the UNIT SELECT lines), then bring PICK and HOLD to ground.

If the drive has an ANSI interface, apply DC power, select the drive (via the SELECT/ATTENTION lines), then issue a Spin Up command.

Similarly, the procedure for powering down also depends on the interface option present:

If the drive has a standard PRIAM interface, issue a Sequence Down command and disconnect DC power supply.

If the drive has an SMD interface, remove the ground from PICK or HOLD and disconnect DC power supply.

If the drive has an ANSI interface, issue a Spin Down command and disconnect DC power supply.

2.15 Performance Check. The following procedures are recommended as an initial check for proper operation on the disc drive:

a. Watch for the drive to become Ready. If no faults are detected during the power up sequence, this will take about 30 seconds. If a fault is detected (by the safety circuits within the drive), Ready will be inhibited and a fault condition will be reported. If, after two minutes, the microprocessor within the drive is unable to sense that the spindle is rotating at the specified speed, READY will be inhibited and spindle rotation will stop.

b. Check the head positioning operation by issuing seek commands. The following seek pattern is suggested:

   From 000 to 001 to 000 to 002 to 000 to 003 to 000 to 004 to 000 to 005 to 000...to maximum cylinder address.

c. Check for proper data transfer operation by writ-

ing and then reading data with each read/write head.

CAUTION

Write operations alter previously recorded data

Most disc systems require a formatted disc before data transfer can be performed.

A disc surface defect map is supplied by PRIAM with each disc drive. The defect map indicates the location of defects discovered during manufacturing and testing. A defect location is specified by the number of byte positions from the index mark.

NOTES

3. FUNCTIONAL DESCRIPTION

3.1 Overview. The PRIAM 3450 Disc Drive has three discs, with a total of six magnetic surfaces. Each surface accommodates one head, as shown in Figure 3-1. On the "bottom" surface, the head reads the servo information. The remaining heads write and read data surfaces 0 through 4.

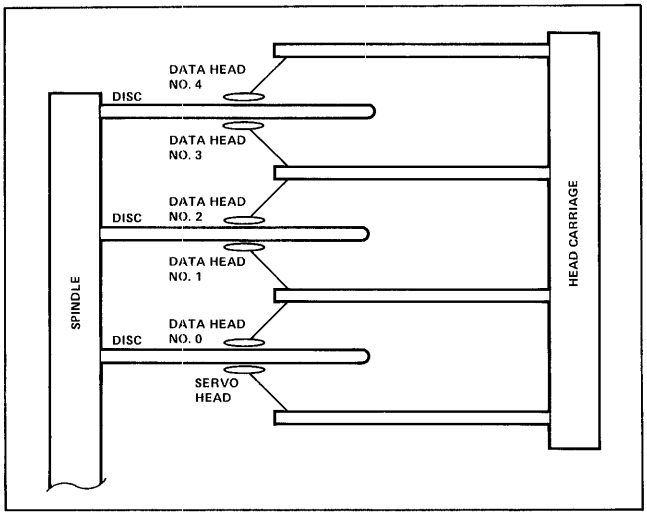


Figure 3-1. Servo and Data Surfaces

The PRIAM 7050 has exactly the same configuration of disc surfaces and heads as the 3450, but it achieves twice the storage capacity by having twice as many data tracks per inch.

3.2 Servo Surface. The purpose of the servo surface is to provide a coordinate system by which the electrical circuitry of the disc drive can locate specific areas for writing or reading data. The servo surface is written once at the factory, and thereafter is a read-only area. The information on the servo surface determines the angular position of the disc, as well as the radial position of the head carriage.

The servo surface is divided into four distinct groups of tracks. From the inside (hub) out, these are as follows:

a. Guardband 2 (landing zone)
b. Guardband 1
c. Servo Data Band
d. Guardband 1

Within each of these bands, there are four types of tracks—odd normal tracks, odd quadrature tracks, even normal tracks, and even quadrature tracks. Each track type produces a characteristic signal at the servo read head, as described below in the SERVO PATTERN section. The closer the servo read head is to a particular track, the greater will be that track's contribution to the servo head's output.

The servo circuitry compares the amplitudes of the signals from adjacent tracks, and identifies an equal-ampliture condition as a "track crossing." During seek operations, the servo circuitry counts the track crossing in order to stop at the cylinder address requested by the controller. During write and read operations, the servo circuitry adjusts the position of the head carriage in such a manner as to preserve the equal-amplitude condition, thus keeping the write/read head "on track."

3.3 Servo Pattern. Figure 3-2 shows the four kinds of servo track signals. The normal servo data patterns are written on the integer tracks, and the quadrature servo data patterns are written on the half-integer tracks.

The negative pulses are sync pulses. In the all "0" pattern, these pulses occur at regular intervals, and serve to define the frame boundaries. When the servo head reads a "1," an additional negative pulse occurs in the mid-frame position. The frame time interval (T) is equal to 16 write/read data bit times. Most of a given track is written with the "0" pattern. The "1" pattern occurs once each revolution of the disc, and serves to define the INDEX location.

The positive pulses are used by the servo circuitry to recognize track crossings or to maintain the on-track condition. Referring again to the all "0" pattern, it can be seen that the even normal track generates positive pulses occurring one-third of the way across the frame, while the odd normal track generates positive pulses occurring at the two-thirds point. The quadrature track patterns have positive pulses alternately at the one-third and two-thirds positions.

When the servo read head is midway between two adjacent tracks (a "track-crossing" position) the output resembles the patterns shown at the bottom of Figure **3-5.** Successive frames produce the equal-amplitude positive peaks, alternating with single large peaks. By analyzing which frames have the equal-amplitude peaks, and whether the large peaks occur at the one-third or the two-thirds locations within the frame, the servo circuitry is able to determine which of the four kinds of "track-crossing" positions is being indicated. Note that the servo read head is midway between two adjacent tracks when the data write/read heads are "on-track."

The servo circuitry counts the track crossing in

order to determine the current cylinder address. In the 3450, data tracks are written at alternate cylinder address (all integer or all half-integer). In the 7050, data tracks are written at both the integer and half-integer cylinder addresses.

3.4 Data Surface. The configuration of tracks on the data surfaces has a one-to-one correspondence with the configuration of servo tracks on the servo surface. Thus, for example, when the servo head is in the servo data band, all the write/read heads are in the corresponding positions in their respective write/read data bands. When the servo head is in the servo landing zone, each data head is also in its own landing zone.

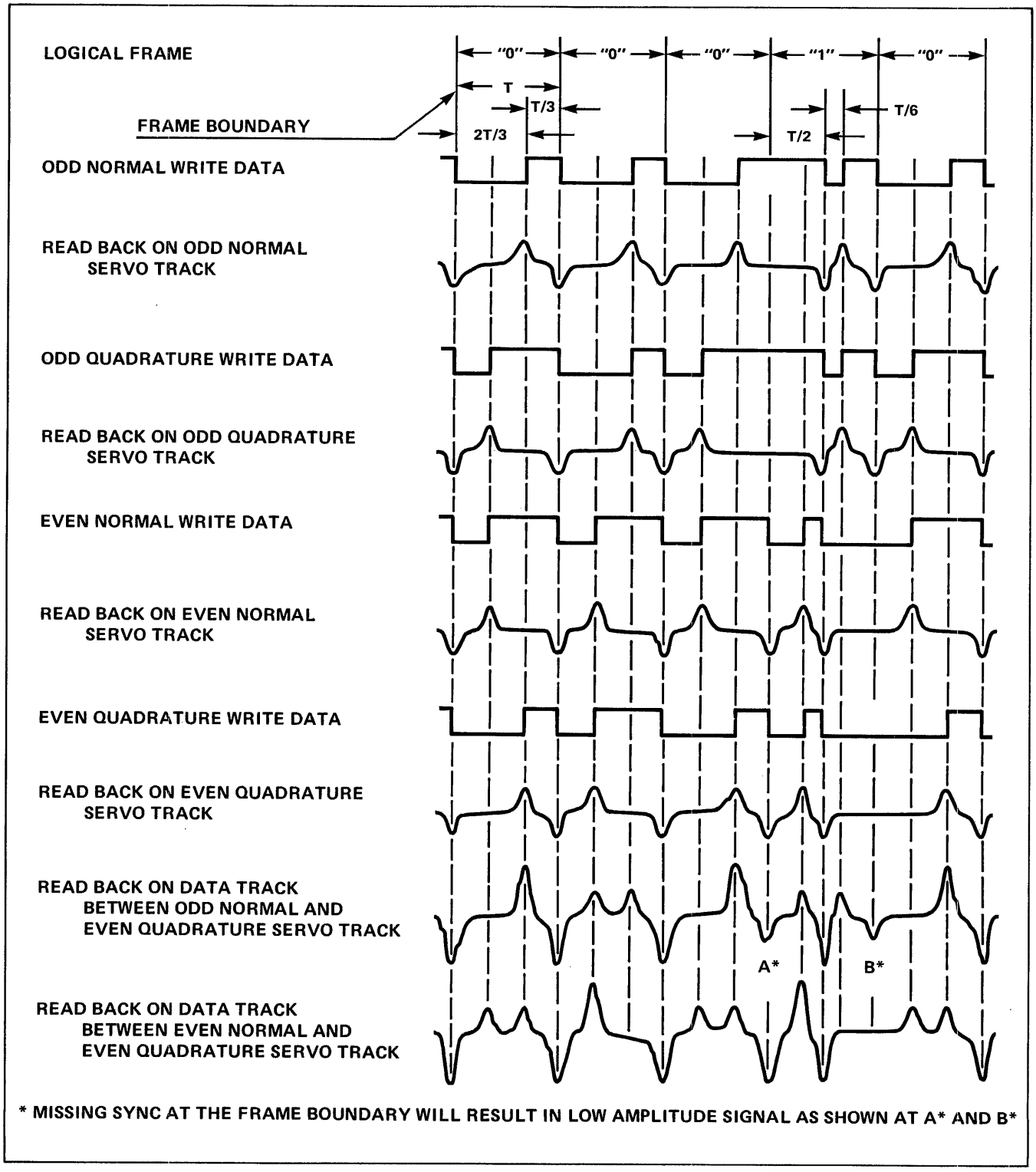


Figure 3-2. Servo Track Signals

The write/read data tracks are numbered consecutively, starting with track 0 nearest the outside edge of the disc. Each write/read data track is divided into sectors. The division of tracks into sectors can be adjusted by the user through switch settings on the read/write digital PCB, as detailed in the INSTALLATION section.

3.5 Track Format. In a typical track format, each track is divided as follows:

Index Mark
Gap (type 1)
Skip Defect Record
N Identical Data Sectors
Gap (type 3)

The index mark is a 1.92 microsecond (two-byte times) pulse, derived from the index pattern on the servo data surface.

The type 1 gap allows for VFO synchronization for data separation. It consists of zeros, and has a minimum length of 23 bytes.

The composition of the Skip Defect Record and of the N identical Data Sectors are described below.

The type 3 gap is a function of sector size, and is used to fill (with zeros) the space left over after the largest possible integer number of sectors (commensurate with the switch settings) have been written.

It should always be remembered that the switch settings determining sector size are read by the microprocessor as part of the Sequence Up process. Thus, a change in these switch settings will not take effect until the drive is once again sequenced up, or re-initialized from a power down condition.

3.6 Defect Location Record Format. The Defect Record (PRIAM interface only) can identify up to three defective sectors on the track.

The format for the Skip Defect Record is as follows:

Data sync (FB hex)	1 byte
1st defect location	2 bytes
2nd defect location	2 bytes
3rd defect location	2 bytes
Check sum	2 bytes
Fill characters (zeros)	2 bytes

3.7 Data Sector Format. The N identical Data Sectors have the following structure:

Sector Mark
Gap (type 1) — zeros (23 bytes minimum)
Address Field
Gap (type 2) — zeros (11 bytes minimum)
Data Field

The sector mark is a 960 nanosecond (one byte time) pulse which occurs at the beginning of each sector. It is generated by the servo circuitry, using a byte clock which is initialized by the index pulse.

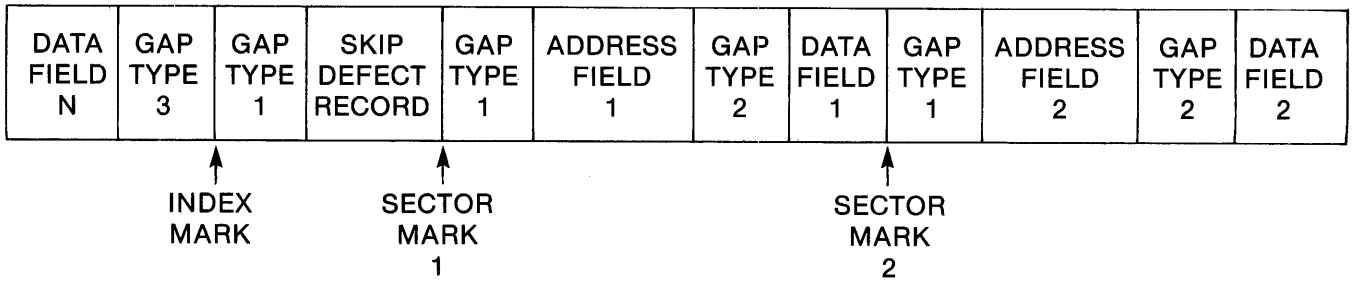
The format for the Address Field is as follows:

Sync pattern (F9 hex)	1 byte
Head and high order cylinder address	1 byte
Low order cylinder address	1 byte
Sector address	1 byte
Sector length and flag	1 byte
CRC	2 bytes
Fill characters (zeros)	2 bytes

The Data Field has the following structure:

Sync pattern (FD hex)	1 byte
Data bytes (according to sector length)	
CRC	2 bytes
Fill characters (zeros)	2 bytes

The following diagram summarizes the typical track format:



3.8 Overview. Figure 3-3 is a simplified block diagram of a PRIAM 8-inch disc drive with the standard PRIAM interface. The overall organization shown is the same for all drives in the 8″ family. However, the names of the specific interface signals vary as a function of the interface option present.

The disc drive has its own (8035) microprocessor, which controls the sequencing of all the operations that occur in the drive.

3.9 Drive Selection. The disc drive must be properly selected before it will respond to any of the signals on the controller interface. On the standard PRIAM interface, this is accomplished by placing the proper address on the DRIVE SELECT 1-4 lines. On the SMD interface, the proper address is placed on the UNIT SELECT 1, 2, 4 and 8 lines and the UNIT SELECT TAG line is activated. In general, the interface lines to be used may be determined by referring to the section (below) describing the specific interface involved.

The address of an individual drive is determined by switch settings on the read/write digital PCB, as discussed in the INSTALLATION section. The drive responds to the selection procedure only when its switch-selected address matches that placed on the interface by the controller.

3.10 Power Up/Down Sequences. When power is applied, the Microprocessor Initialization sequence occurs automatically. The microprocessor then goes into the idle state, in which it monitors the controller interface for a command.

The controller may then issue a Sequence Up command to the drive (the exact manner in which this is done depends on the interface option present). The microprocessor recognizes this command and starts the spindle motor. When the motor is running at the proper speed, the microprocessor reads the sector length switches, and configures the drive to operate in terms of the chosen sector length. Next it calls the RSTRGO subroutine, which moves the heads to cylinder zero. It then enables the drive ready status, resets the busy condition, and returns to the idle state.

The drive is stopped by issuing a Sequence Down command. This causes the heads to return to the landing zone, and stops the spindle motor.

3.11 Motor Control Circuitry. The spindle motor is a brushless (electronic commutating) permanent magnet DC motor. The speed of the motor is controlled by a closed-loop circuit containing Hall effect sensors and a comparator.

Figure 3-4 is a block diagram of the motor control circuitry. The microprocessor sets the OFF signal true to inhibit spindle rotation, or false to allow spindle rotation. The microprocessor monitors the speed of spindle rotation. If, during the power up sequence, the motor does not reach its specified speed within one minute, or if, during normal operation, the motor speed passes outside the specified speed range, the microprocessor will set the Fault condition, restore the heads to the landing zone, and inhibit the spindle rotation.

3.12 Seek Modes. The servo system has two main modes of operation — On Track mode (also called Position mode) and Move mode.

Move mode becomes active when the drive is commanded to move the heads. The microprocessor receives the new target cylinder address and the seek command, determines the direction of travel and the number of tracks to be crossed, and sets Move mode.

When the servo is in Move mode, a velocity profile (produced by a digital-to-analog converter) is compared (via a summing junction) with the output of an electronic tachometer, which indicates the velocity of headmotion. The difference signal from the summing junction is fed to the servo power amplifiers, which control the voice coil motion. The heads are driven toward the new cylinder address. The servo circuitry monitors the track crossings and decreases the velocity of head motion as the selected cylinder is approached.

When the heads are within 100 microinches of the new cylinder, the On Track mode becomes active.

In the On Track mode, the heads are held precisely over the designated track. Any unintended head movement is detected by the electronic tachometer and fed to the summing junction. This in turn causes the servo power amplifiers to adjust the head position, so that the heads remain at the desired location.

Servo safety circuits drive the heads to the landing zone upon detection of a low power condition, or if both Move and On Track modes occur simultaneously. The safety circuits also monitor the voice coil speed. If the specified speed is exceeded, or if the continuous position information is lost, an Overspeed signal is established and the servo power amplifiers are disabled. Seek Fault is set if any of the above conditions develop.

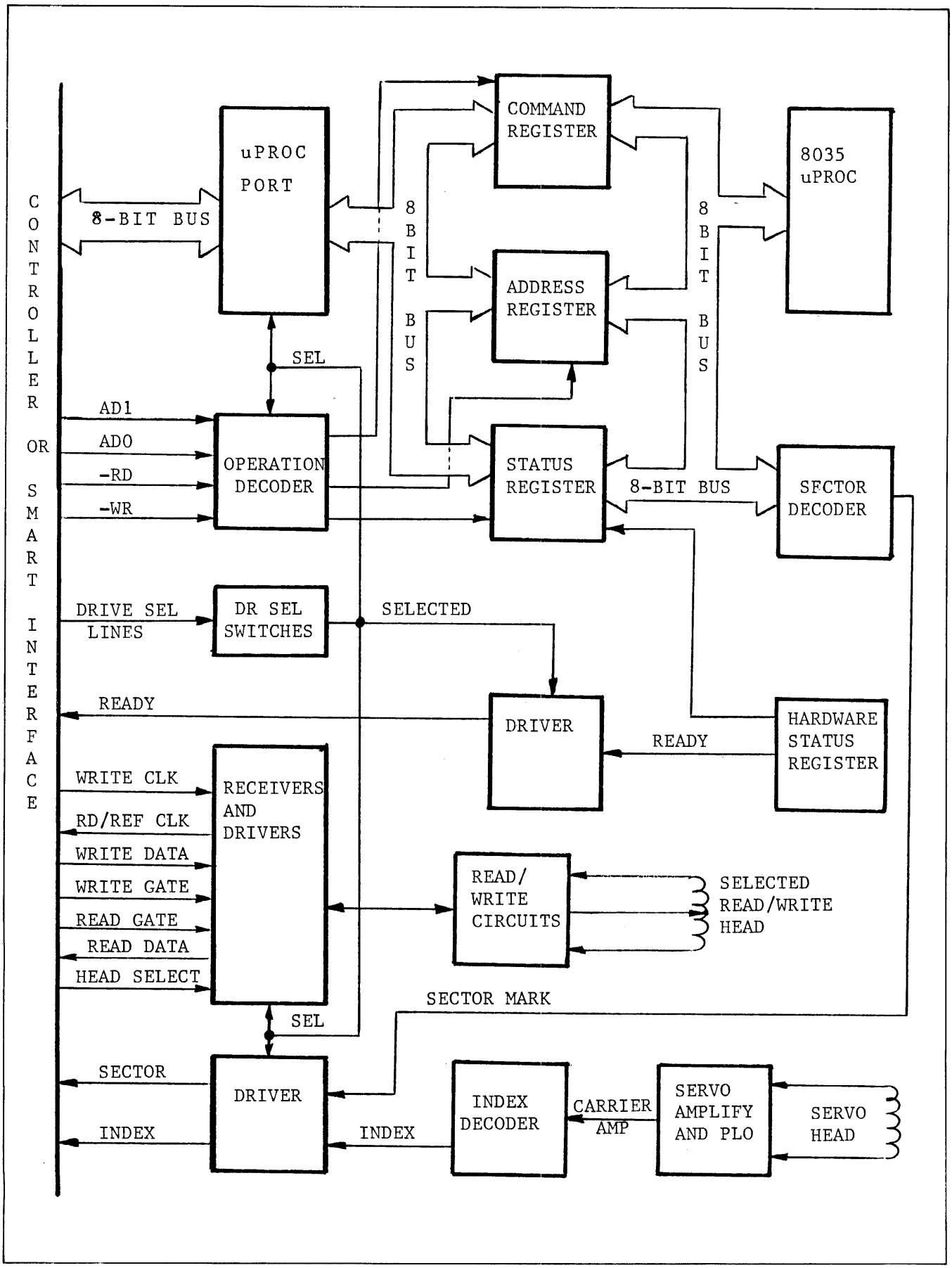


Figure 3-3. Simplified Block Diagram of a PRIAM 8-inch Disc Drive

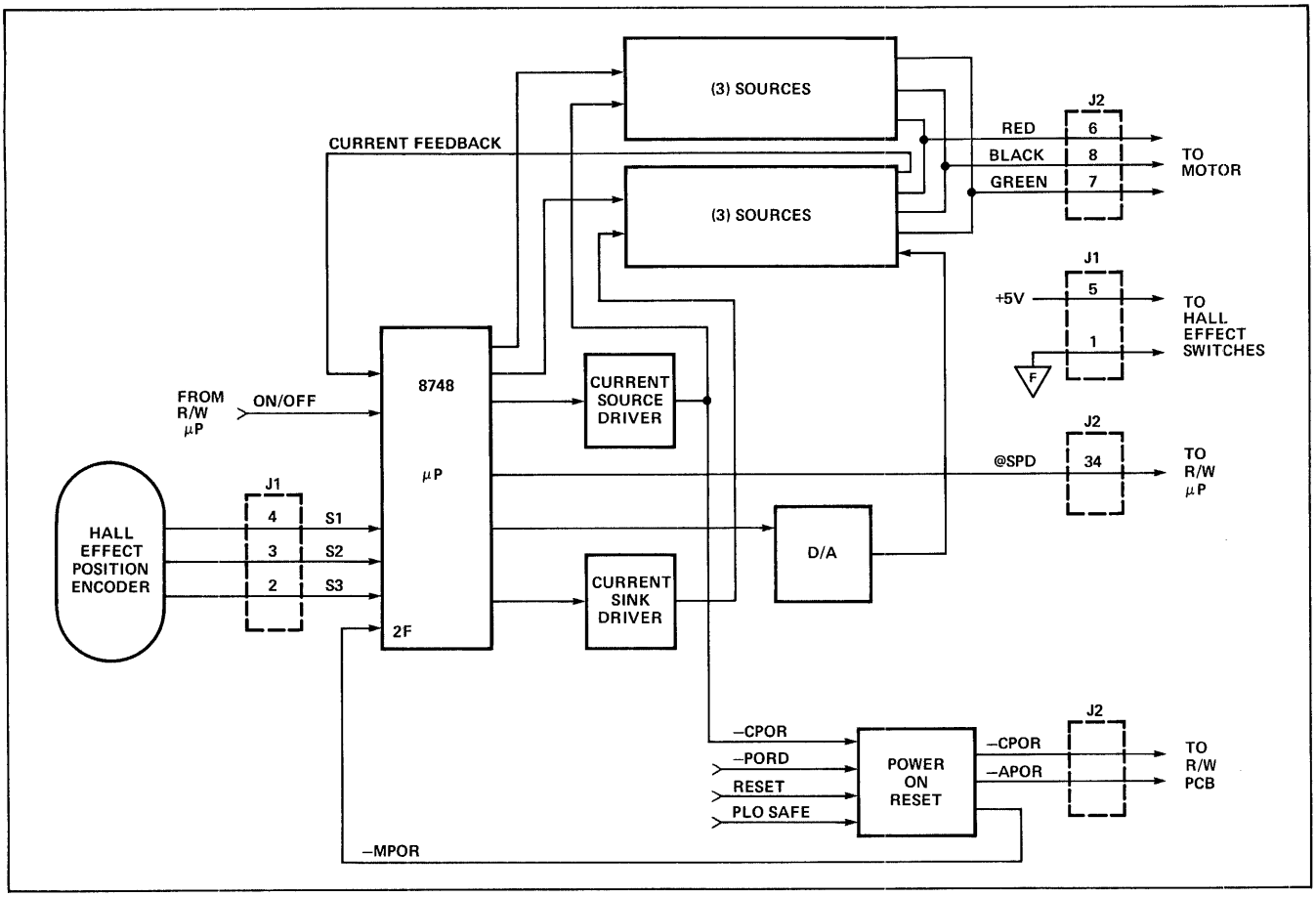


Figure 3-4. Motor Controller

3.13 Servo Circuitry. Figure 3-5 is a block diagram of the servo circuitry. The signal from the servo head is amplified by a preamp located adjacent to the head in the head disc assembly. On the main PCB it is further amplified by an AGC amplifier. The output of this amplifier has the waveform shown as ABCD in Figure 3-5, when the servo head is located midway between an odd track and an even track, and the servo data pattern is all 0s. A and D are the sync pulses occurring at the bit cell boundaries. When a 1 is present in the servo data stream, an additional "sync" pulse appears at the mid-cell position.

A sync detect circuit detects the sync pulses at the A and D positions, and uses these pulses as input for the PLO (phase locked oscillator). The PLO generates a steady clock signal of approximately 6 MHz, which is phased locked to the servo data.

The pulses marked B and C are the pulses that occur at the 1/3 and 2/3 points in the bit cell.

In the On Track mode, the Position Demodulator and On Track Compensator are used to compare the B and C amplitudes, and to apply any discrepancies as an error signal to the input of the voice coil power amplifier, in such a way that the servo head remains midway between the two tracks.

In the Move mode, the B and C amplitudes are monitored, and the threshold detector identifies the track crossings, outputting a TRK XING signal which is used to update a cylinder address counter (on the read/write digital PCB). The Velocity Tachometer, Curve Generator, and Combiner together control the input to the voice coil power amplifier, in order to control the head carriage velocity.

3.14 Data Read/Write Functions. PRIAM disc drives use the MFM (modified frequency modulation) recording method. The MFM encoding rules determine the relationship between the flux transitions on the recording medium, the data being written, and the bit cell boundaries. The following three rules must be observed:

1. If a 1 is written, there is a flux transition at the center of the bit cell (data bit).
2. There is always a flux transition at the bit cell boundary between consecutive 0s (clock bit).
3. There is never a flux transition at the boundary of a 0 and a 1.

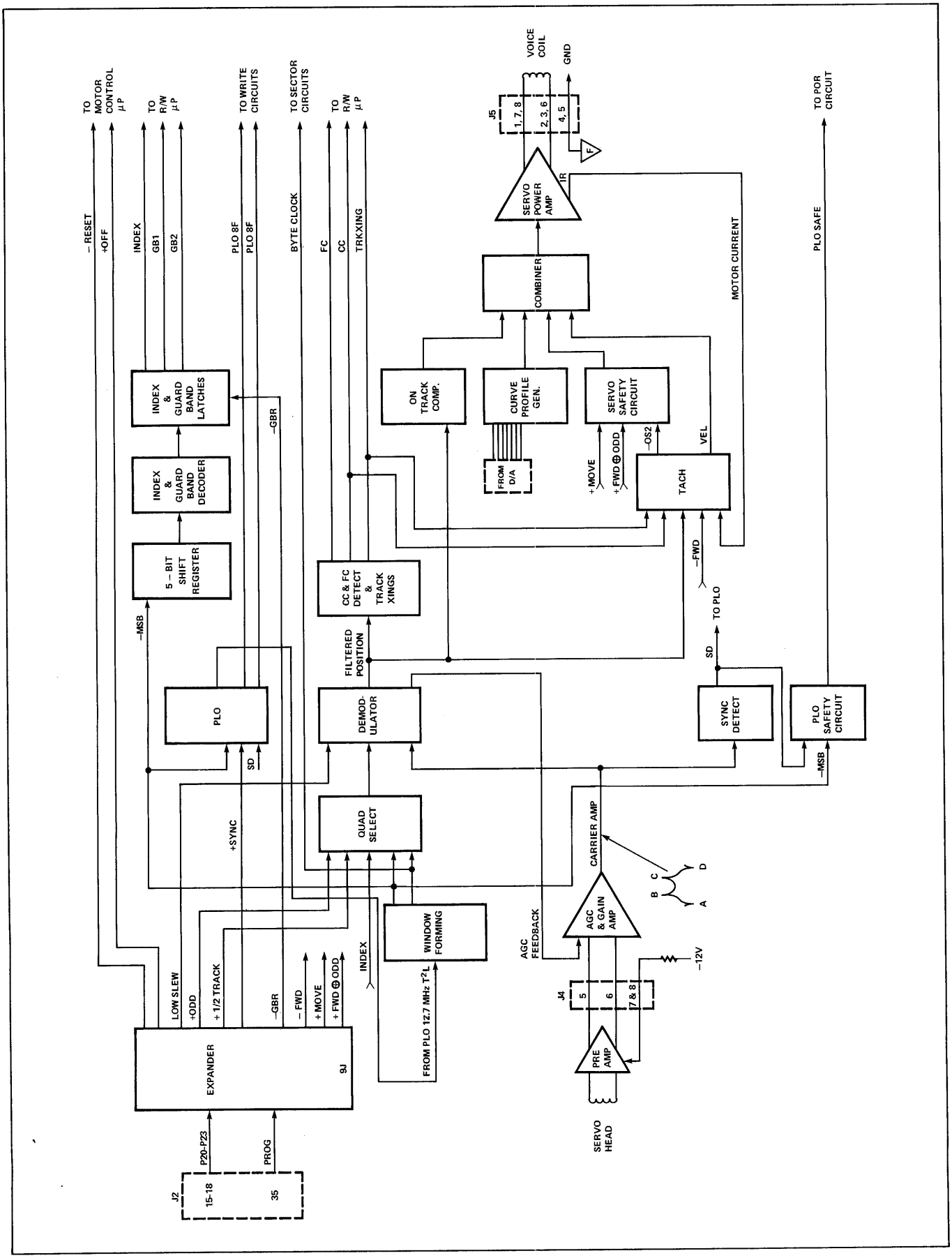


Figure 3-5. Servo Circuitry

Figure 3-6 shows how the MFM encoding works in practice. The bit cells are 155 nanoseconds long, which corresponds to a data read/write rate of approximately 6.4 megabits per second. The MFM technique assures that there will never be more than two bit-cell times between successive flux transitions, and thus there will always be enough information to properly reconstruct and synchronize the original NRZ data.

Figure 3-7 is a block diagram of the circuitry involved in the data write and read operations. The controller initiates a write operation by supplying the disc drive with Head Select, Write Gate, Write Clock, and NRZ Write Data. If the drive is selected and ready and if Write Protect is off, the write operation will begin. The write circuits will encode the NRZ data to MFM, synchronize the data to the write clock, and record the data transitions on the selected disc surface.

Safety circuits monitor the write operation. If a fault is detected, writing is inhibited, Fault is set, and Ready is inhibited.

The controller initiates a read operation by supply-

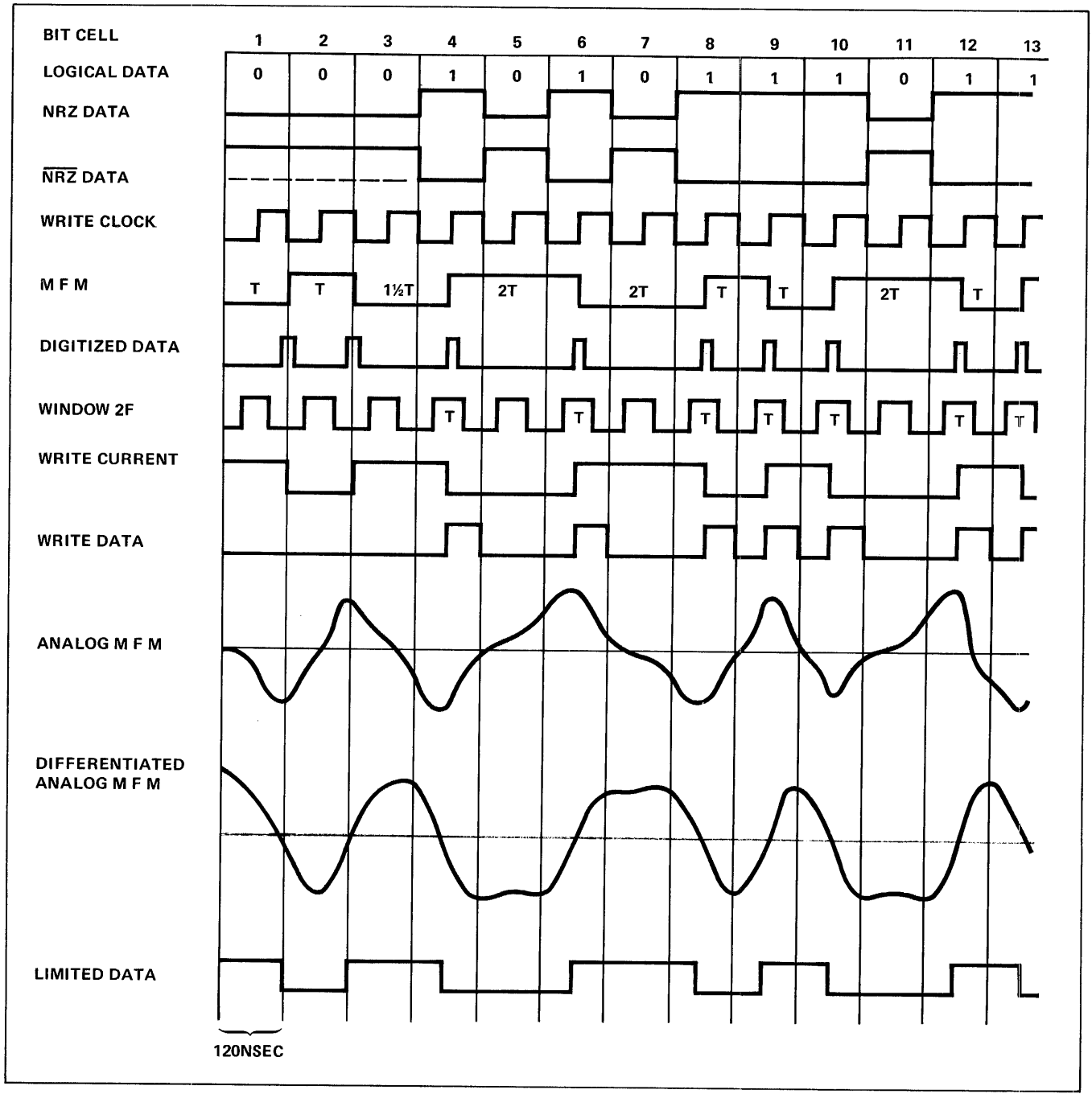


Figure 3-6. Read/Write Timing and Encoding

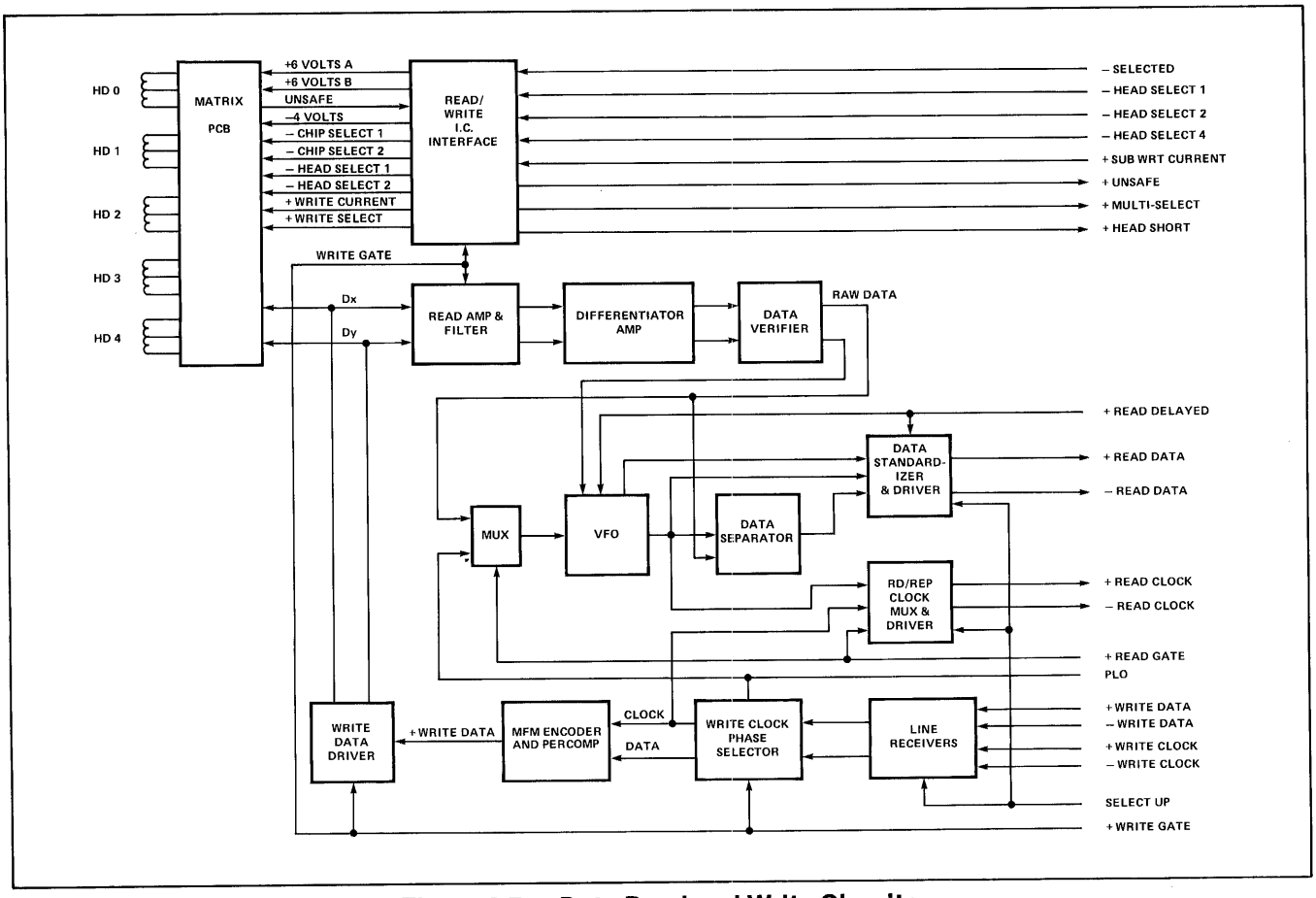


Figure 3-7. Data Read and Write Circuitry

ing the disc drive with Head Select and Read Gate. The controller sets Read Gate true in the gap area immediately preceding the desired data. The gap area serves to allow time for the data separation circuits to synchronize to the recorded data.

During the read operation, voltage peaks of alternate polarities are induced in the selected head. A voltage peak occurs at each detected data transition. The following functions are performed by the read circuitry:

1. Amplify, differentiate, and digitize the signal from the read head.
2. Verify the pulse width of the digital data and eliminate any false zero crossings.
3. Separate the data pulses from the clock pulses.
4. Discard the detected clock pulses.
5. Transform the data pulses to the NRZ format.
6. Develop a Read Clock signal to identify the beginning of each bit cell.
7. Transmit the NRZ data and Read Clock to the controller.

A recoverable read error (soft error) resulting from a transient condition can usually be corrected by re-reading the particular record involved. An error of this type is normally detected by the cyclic redundancy checking (CRC) performed by the controller.

A non-recoverable error (hard error) is one which persists after several attempts to read the record. This may be a write error, in which case the error is cleared by re-writing the record. A hard error may also be caused by a disc surface defect, in which case the error may persist even after the record has been re-written.

3.15 PLO/VFO. Two of the circuits shown in Figure 3-7 (the VFO and the PLO) are used to provide the proper synchronization between the information recorded on the disc and the data being transferred over the interface to the controller. The PLO proceeds at a uniform rate, while the VFO is subject to variations because of the analog nature of the write and read operations at the disc and head level.

The VFO generates the clock signals to be sent to the controller. During data read operations the raw data stream is used as a source of sync signals. The VFO adjusts its output clock frequency in such a manner that the bit rate at the interface is equal to the average rate at which the bit cell boundaries are detected in the raw data stream.

During procedures other than read operations, there is no data stream to synchronize to. At these times the input to the VFO comes from the PLO, which operates continuously from the servo data. Thus, for example, during write operations, the PLO generates a surrogate clock to which the VFO becomes a slave. The VFO output is used to generate the Read Clock signal to the controller. The controller then uses this signal as a basis for the Write Clock signal it returns with the data to be written.

3.16 Microprocessor Flow Charts. This section contains the flow charts that give details on the microprocessor controlled sequences used in the disc drive. When power is initally applied to the main PCB, the INIT (Figure 3-8) routine is automatically executed. The microprocessor then enters the IDLE state (Figure 3-9), where it waits for a command, as shown in the IDLE (Figure 3-10) flow chart.

If a command is received, the CMDET (Figure 3-11) routine is executed. If the command is not rejected (CMDREJ, Figure 3-11) the microprocessor executes the particular command routine specified.

Power sequencing for the spindle motor is controlled by the SEQUP (Figures 3-12 and 3-13) and SEQDWN (Figure 3-14) routines. Seek operations are controlled by the RESTOR (Figure 3-15) and SEEK (FIgure 3-16) routines, and their subroutines RSTR2 (Figure 3-17), RSTRGO (Figure 3-17), SEEKGO (Figure 3-18), **LTRK** (Figure 3-20), HTRK (Figure 3-20 and 3-21). Seek operations terminate with the SKDNE (Figure 3-22), SKCMP (Figure 3-22), or SKERR (Figure 3-19) routines. Commands in general terminate with the CMDEND (Figure 3-11) or CMDREJ (Figure 3-11) routines.

The Fault Reset command is executed by the FLTRST (Figure 3-23) routine.

The DRIVE ID & Read Command is executed by the RDRVID and RDBPS (Figure 3-24) routine. The Seek Start command is executed by the SKSTRT (Figure 3-25) routine. Calibration is performed using the CALIBRATE (Figure 3-26) routine.

3.17 PRIAM Interface. PRIAM offers a basic 8-bit bidirectional bus control interface designed to be readily connected to popular 8-bit and 16-bit microprocessors. Across this interface all spindle and head positioning controls are passed.

Read and write data is passed via synchronous serial-bit NRZ signal lines. The interface provides INDEX, SECTOR MARK, READ/REFERENCE CLOCK, and WRITE CLOCK signals.

Up to four drives may be daisy chained along a single 50-conductor flat ribbon cable. Power is provided via a separate connector. Control switches are provided on the PCB.

3.18 Connectors and Pin Assignments. All drive signal connections are made via a single 50-pin ribbon cable connector. A second 50-pin connector is available for daisy chaining to another drive or for a terminator for the last drive in the string. Up to four drives may be daisy chained.

A separate connector for DC power is provided. However, if the PRIAM optional power supply is used, then its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

Mini-dip switches are provided on the PCB to select drive address, sector length, write protect functions, and write clock control.

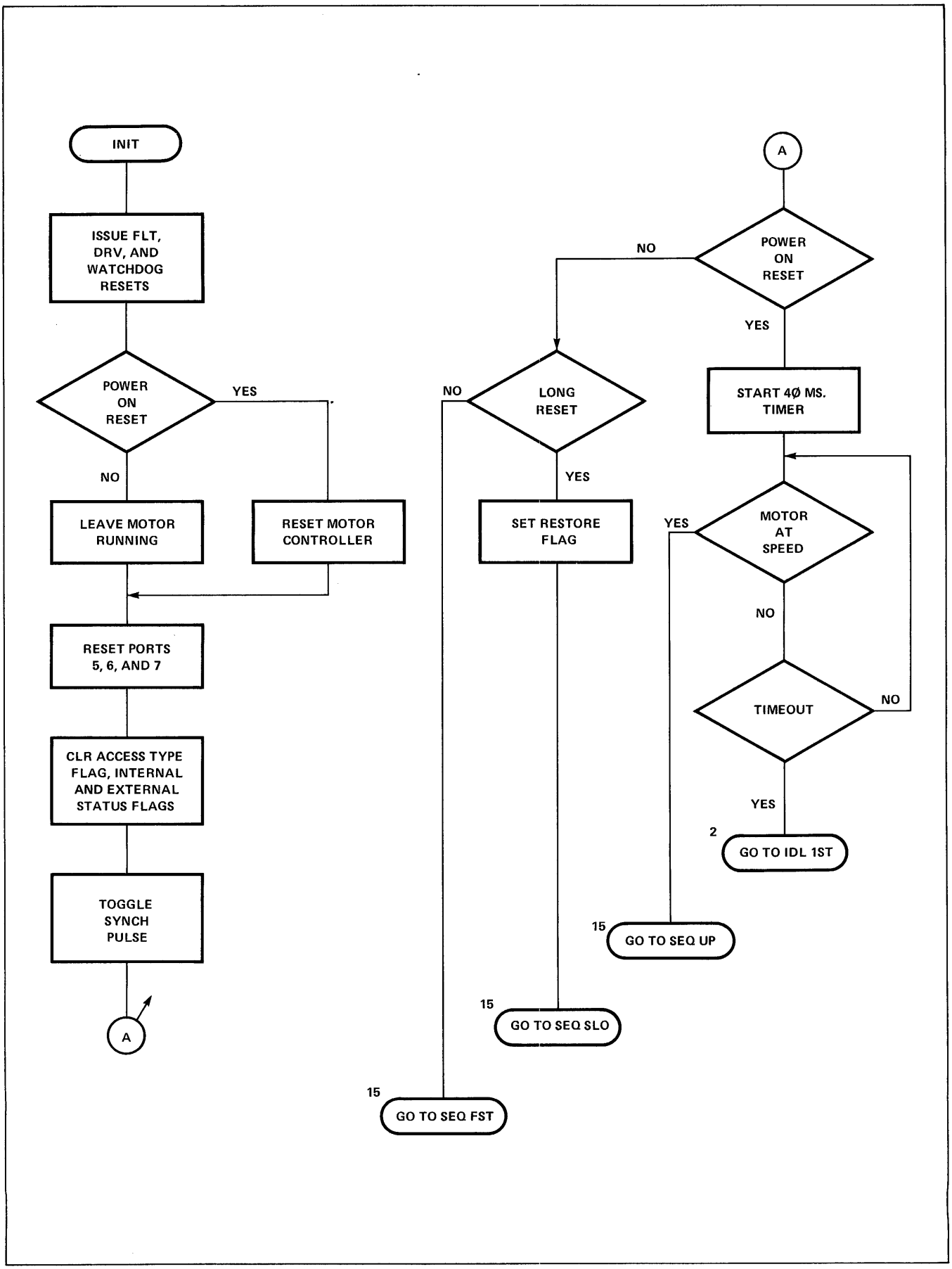


Figure 3-8. Initialization Flow Chart

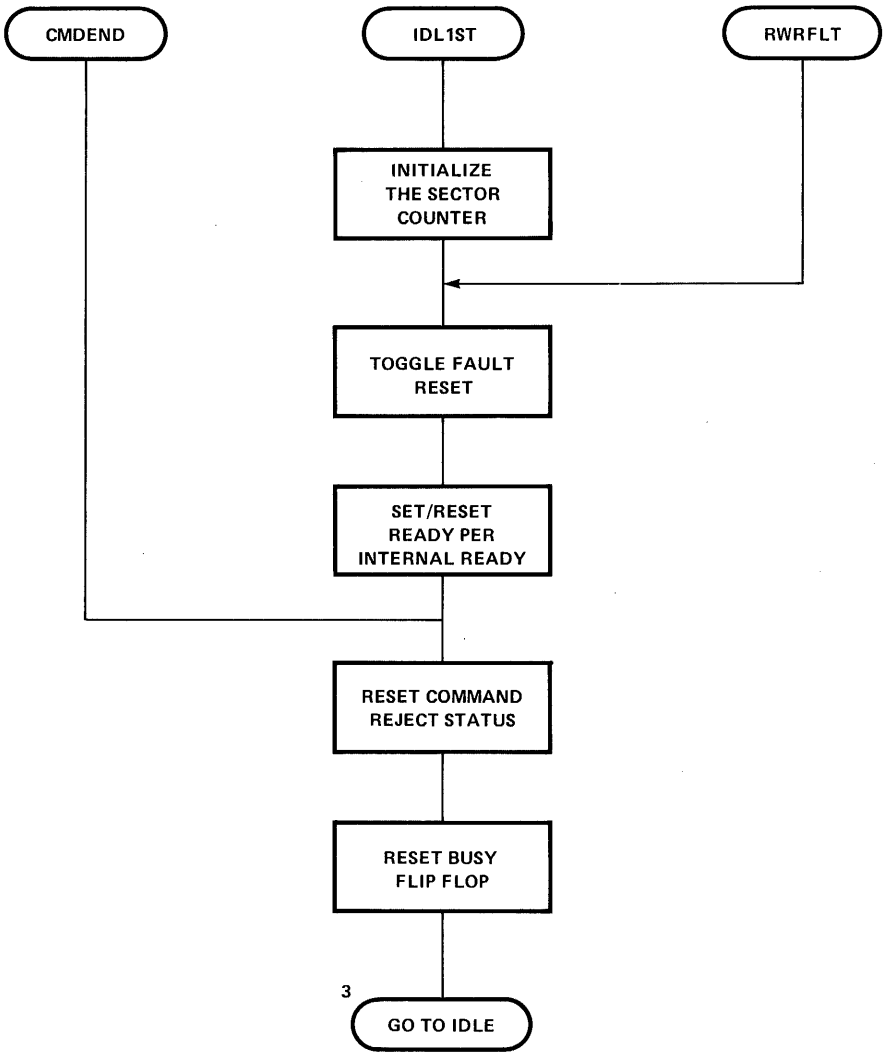


Figure 3-9. First Idle Flow Chart

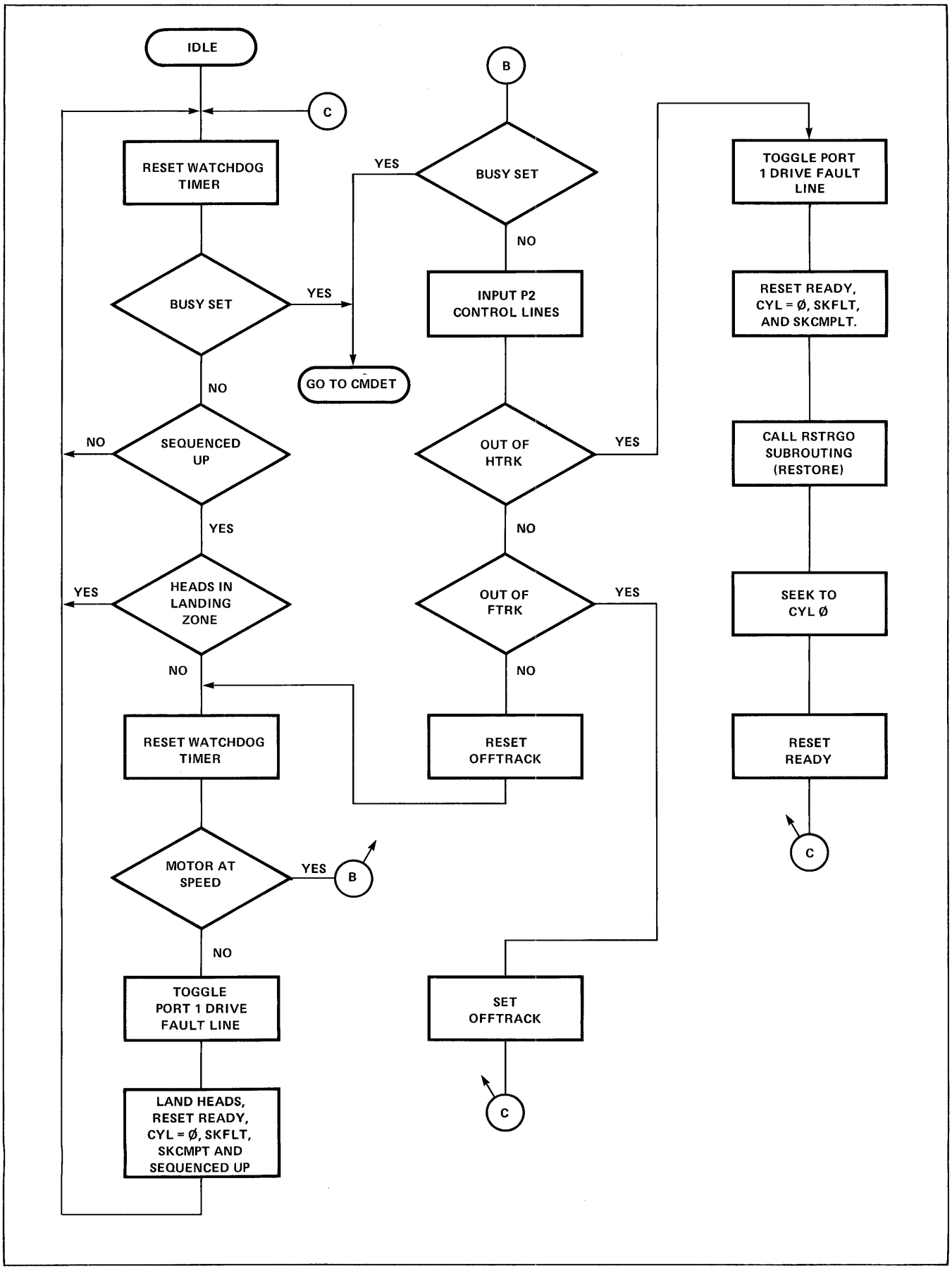


Figure 3-10. Idle Flow Chart

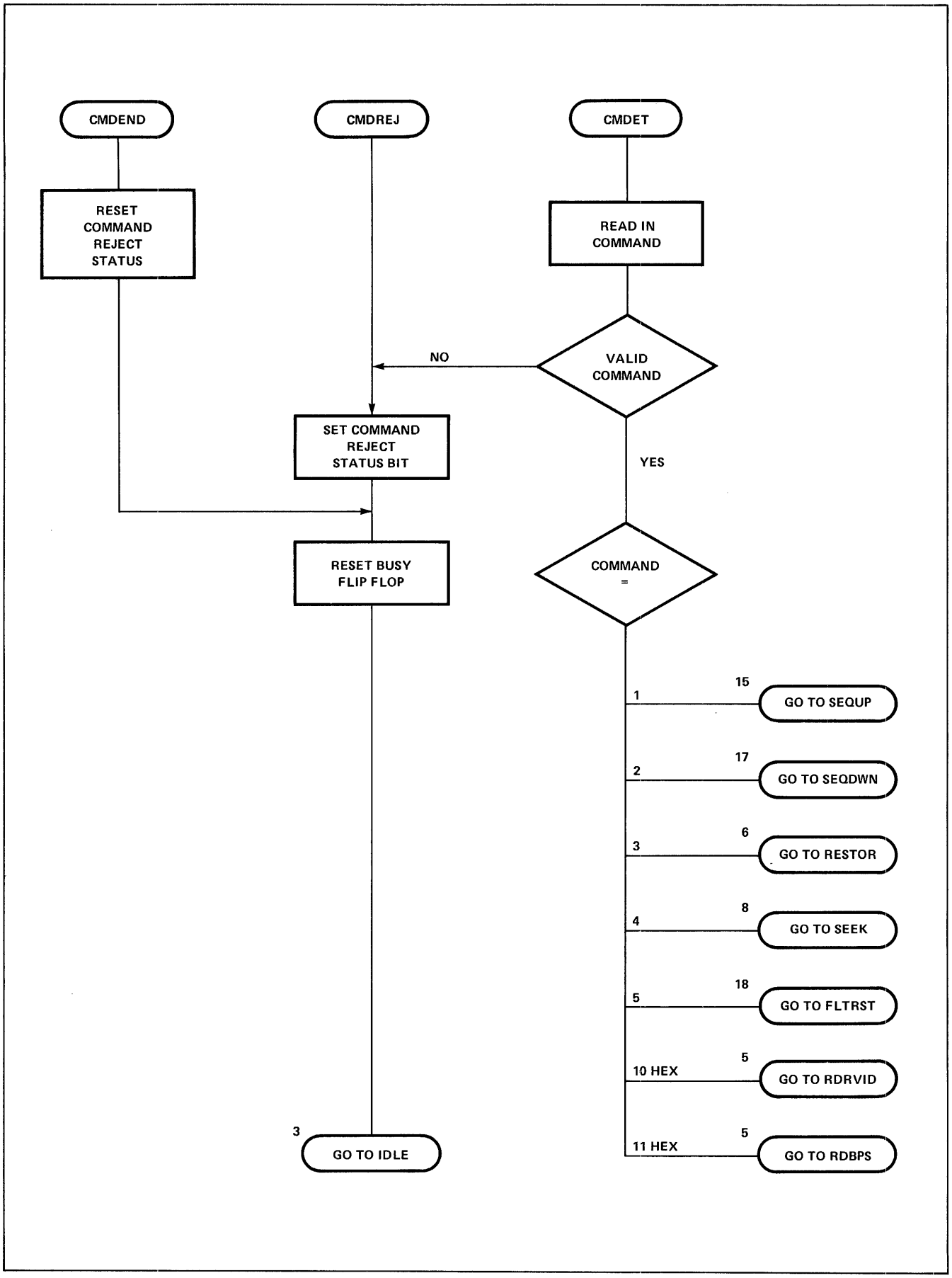


Figure 3-11. Command Decode Flow Chart

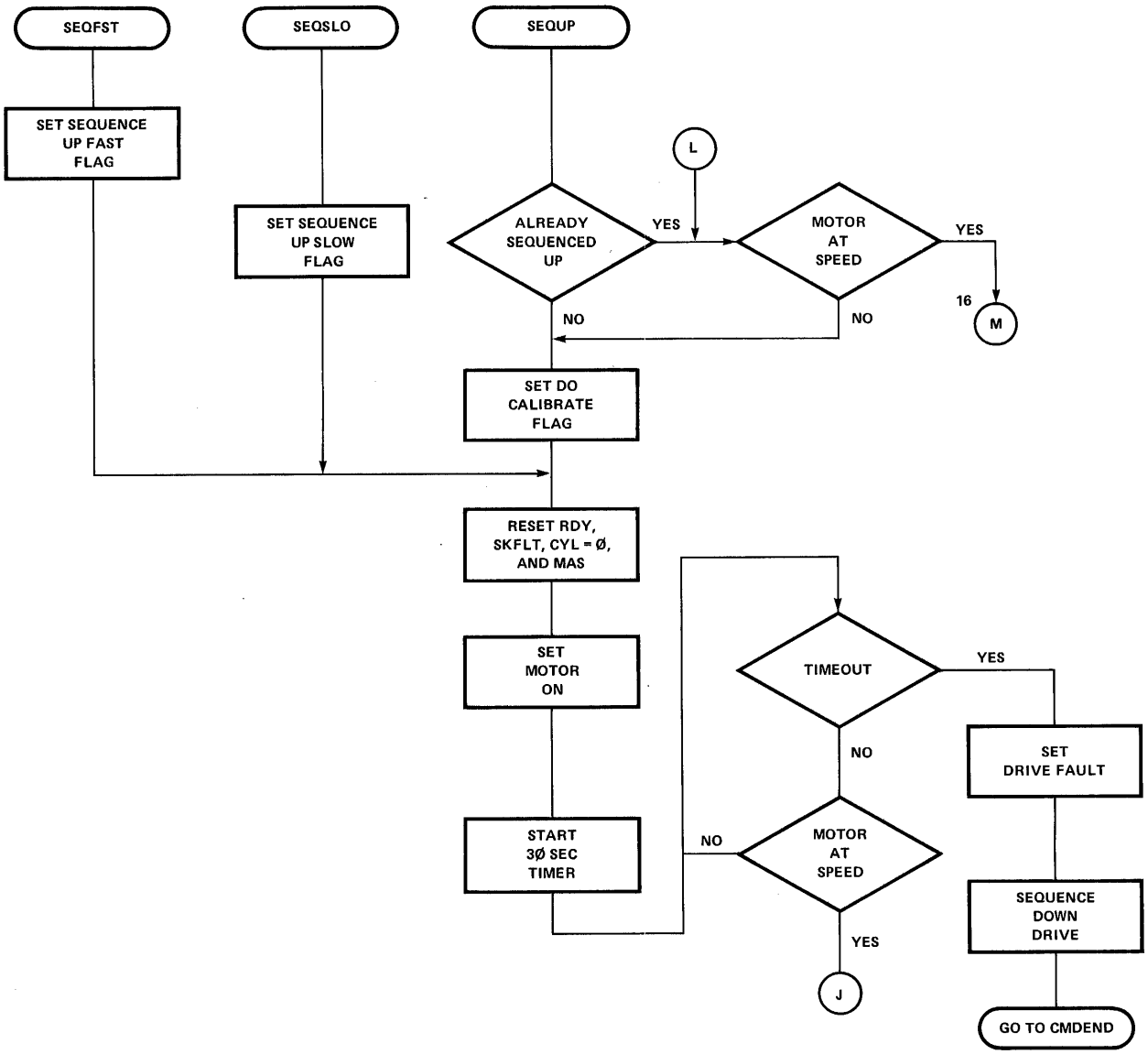


Figure 3-12. Sequence Up Flow Chart #1

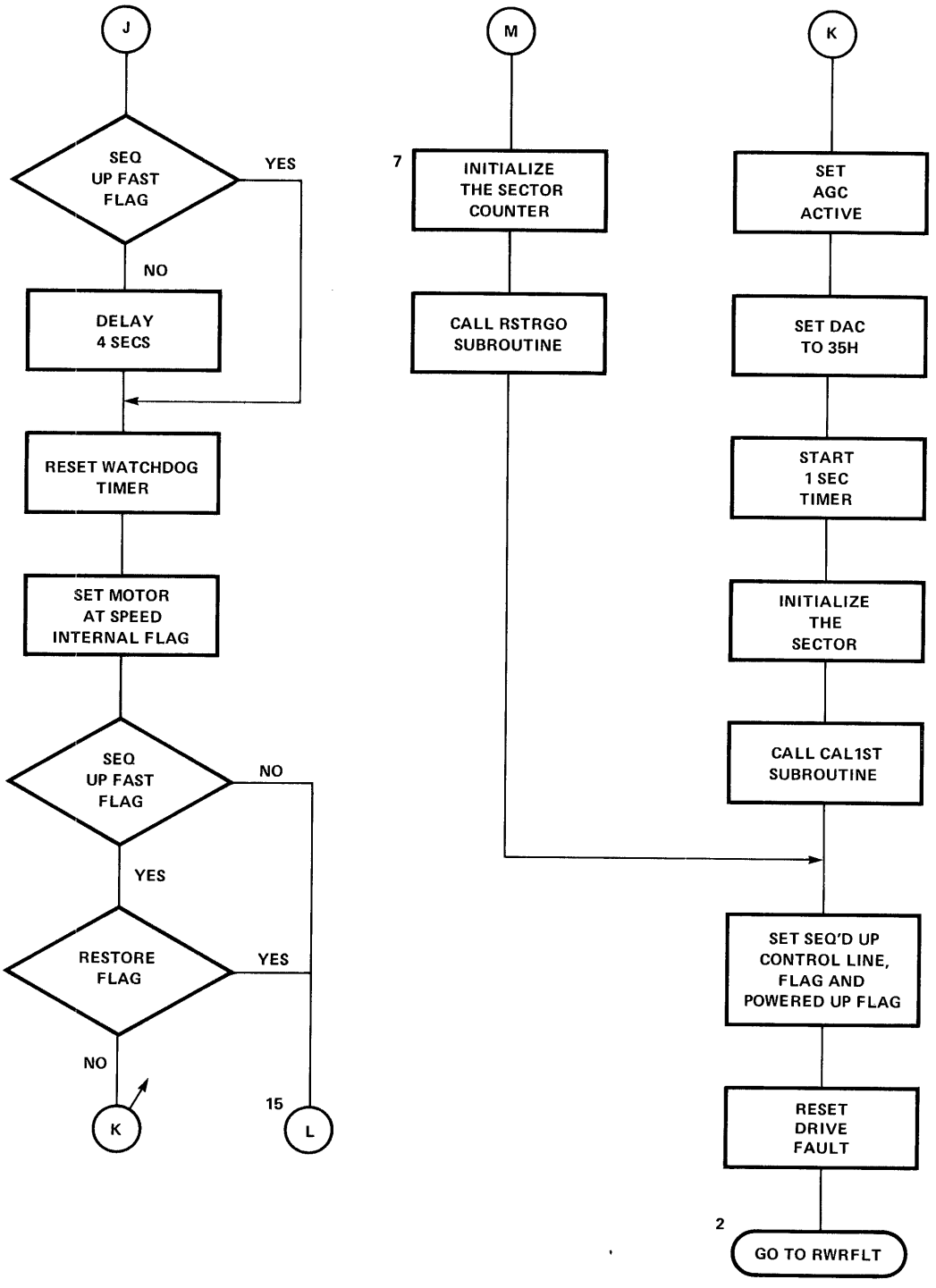


Figure 3-13. Sequence Up Flow Chart #2

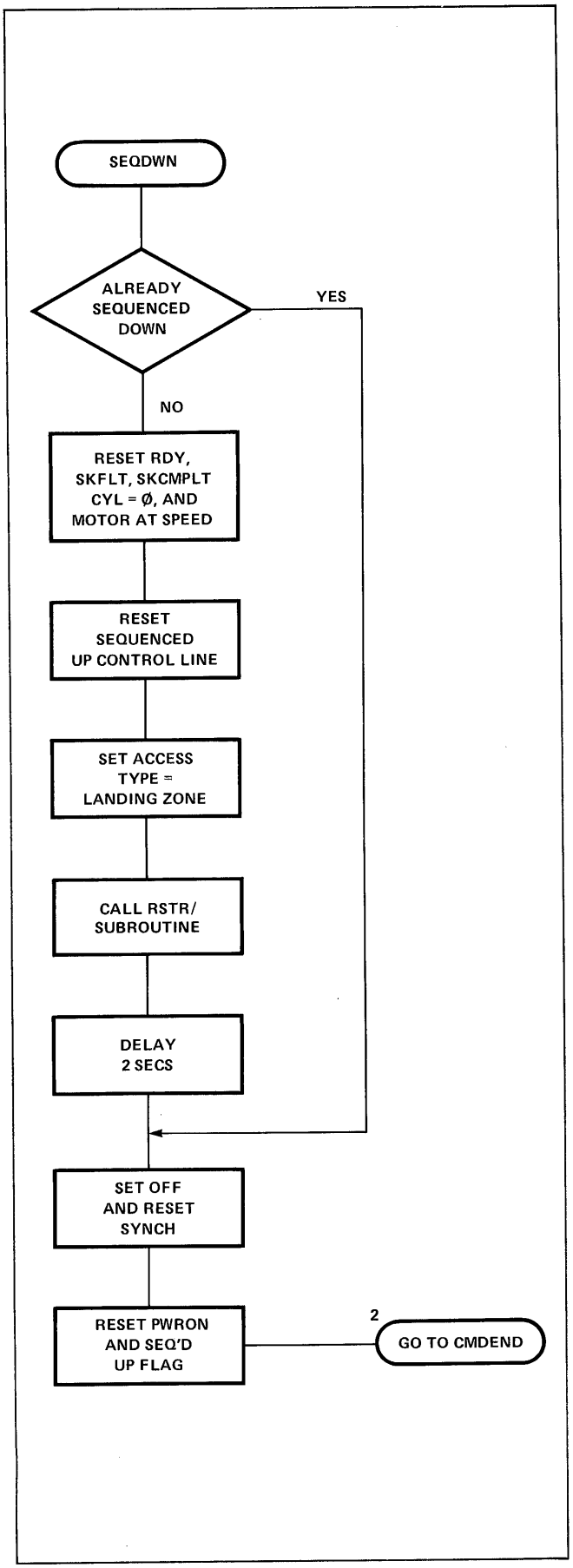


Figure 3-14. Sequence Down Flow Chart

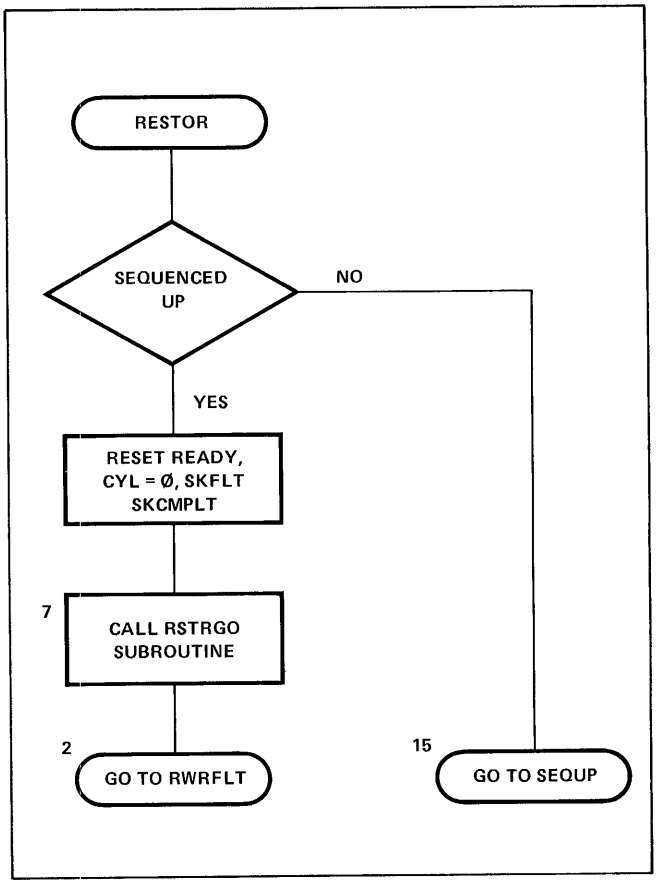


Figure 3-15. Restore Flow Chart

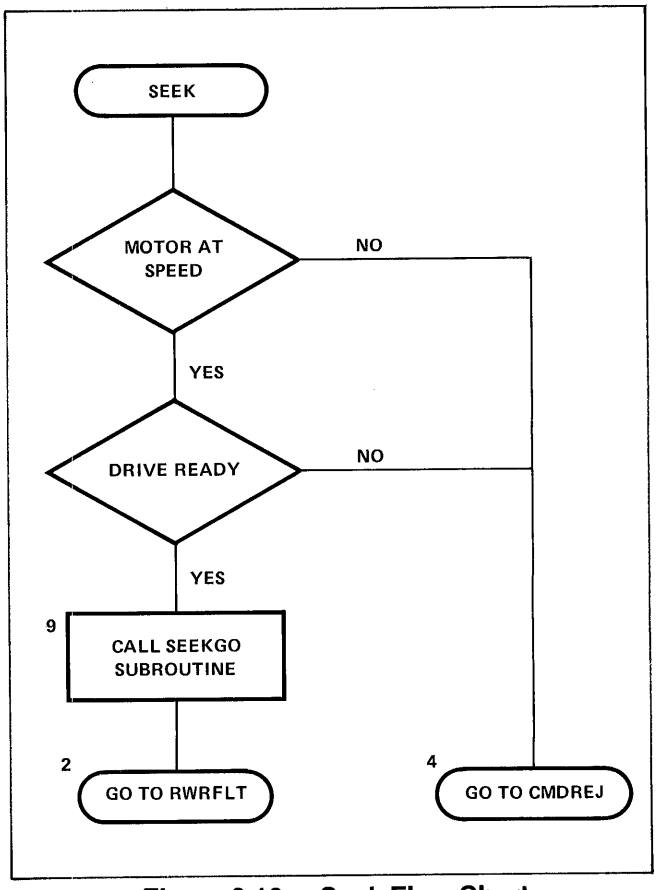


Figure 3-16. Seek Flow Chart

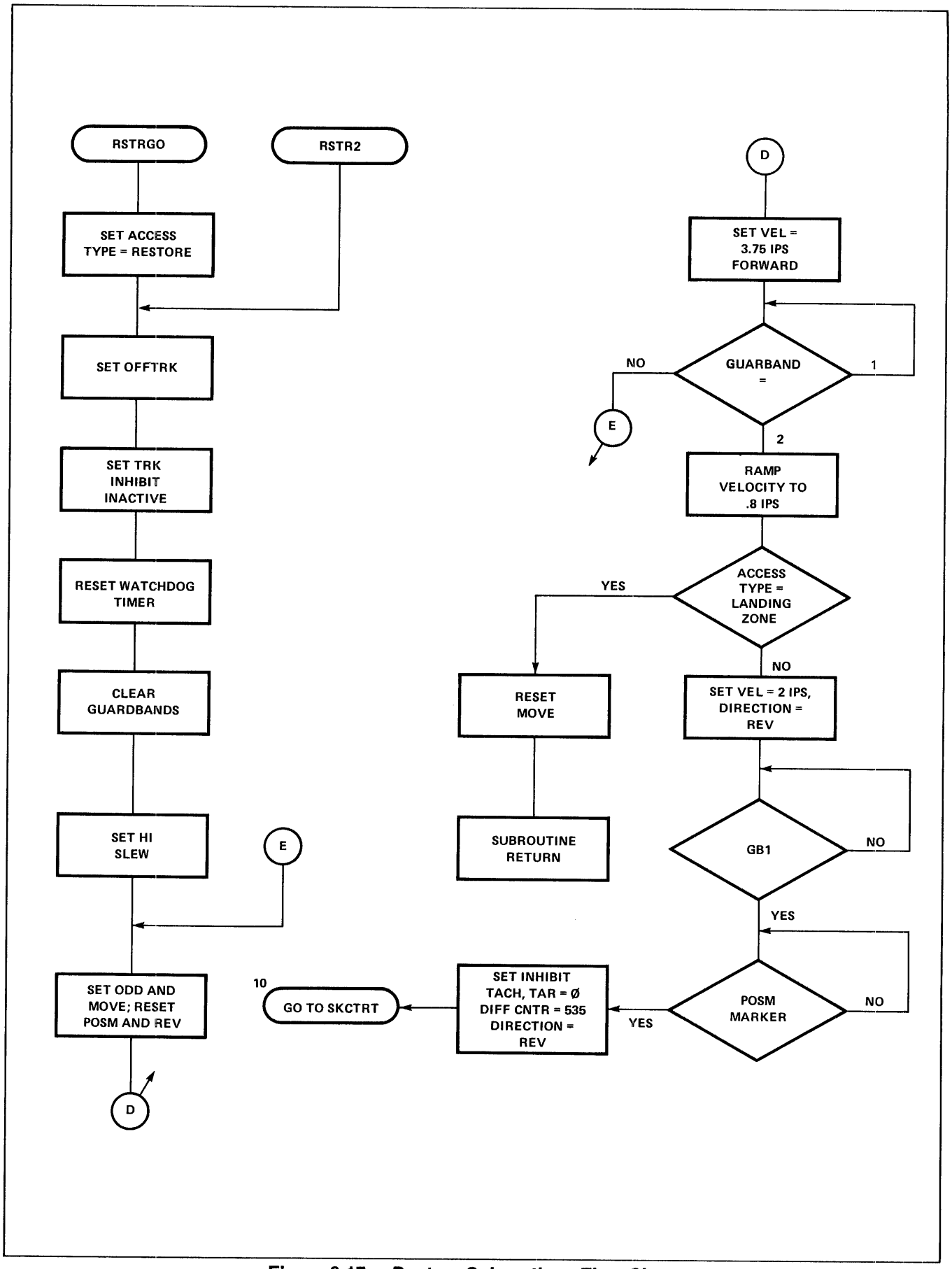


Figure 3-17. Restore Subroutines Flow Chart

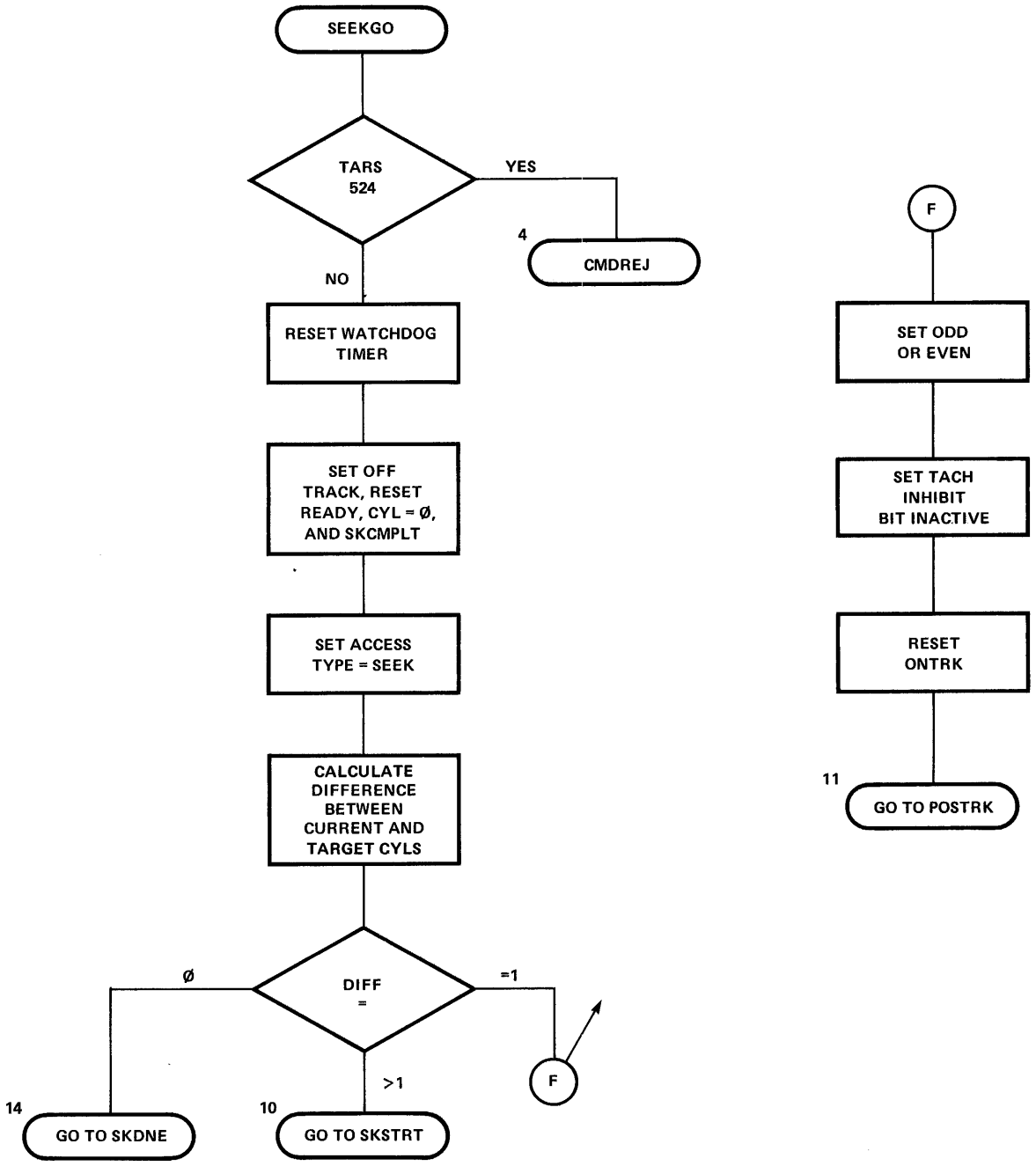


Figure 3-18. Seek Subroutines Flow Chart #1

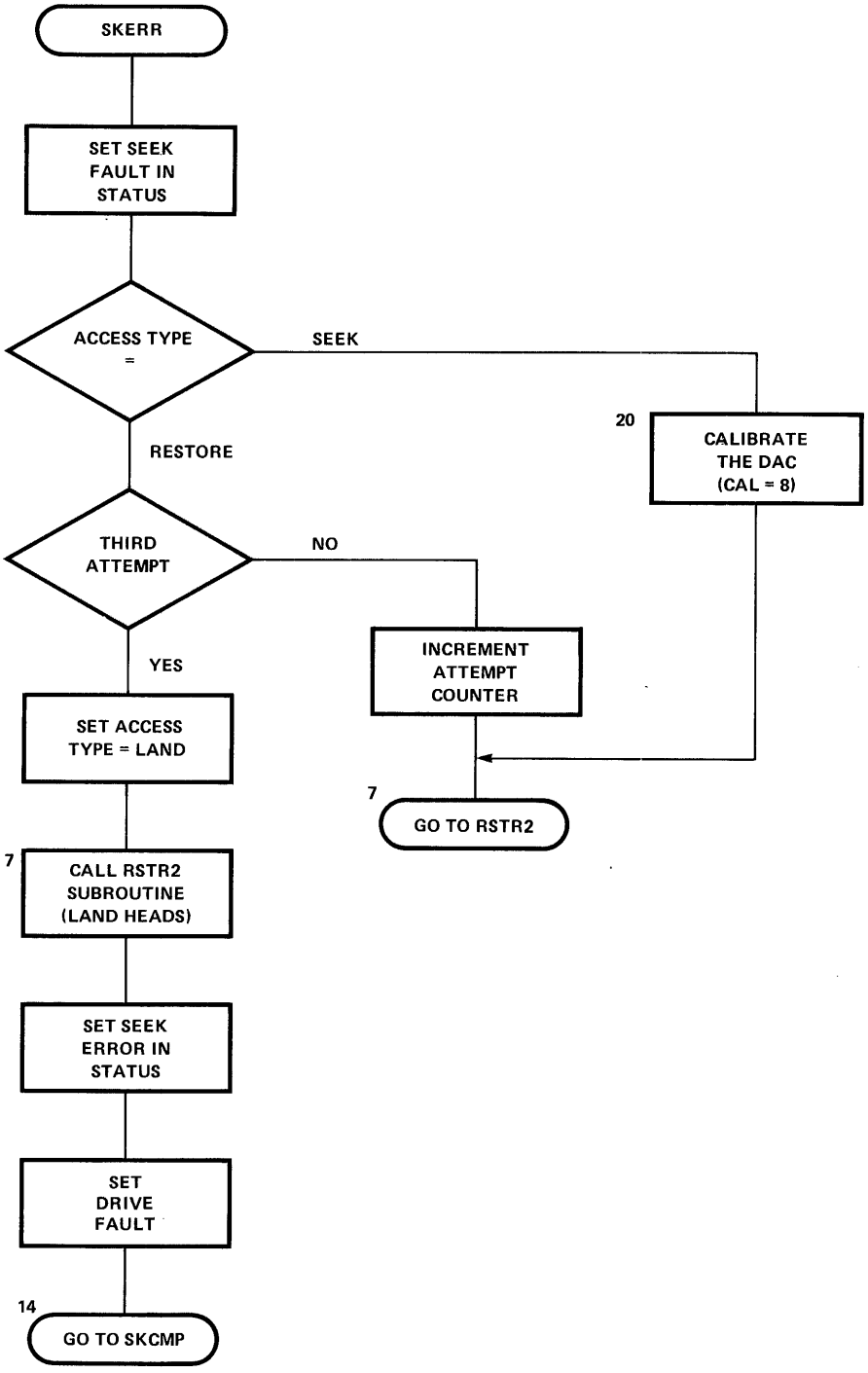


Figure 3-19. Seek Error Flow Chart

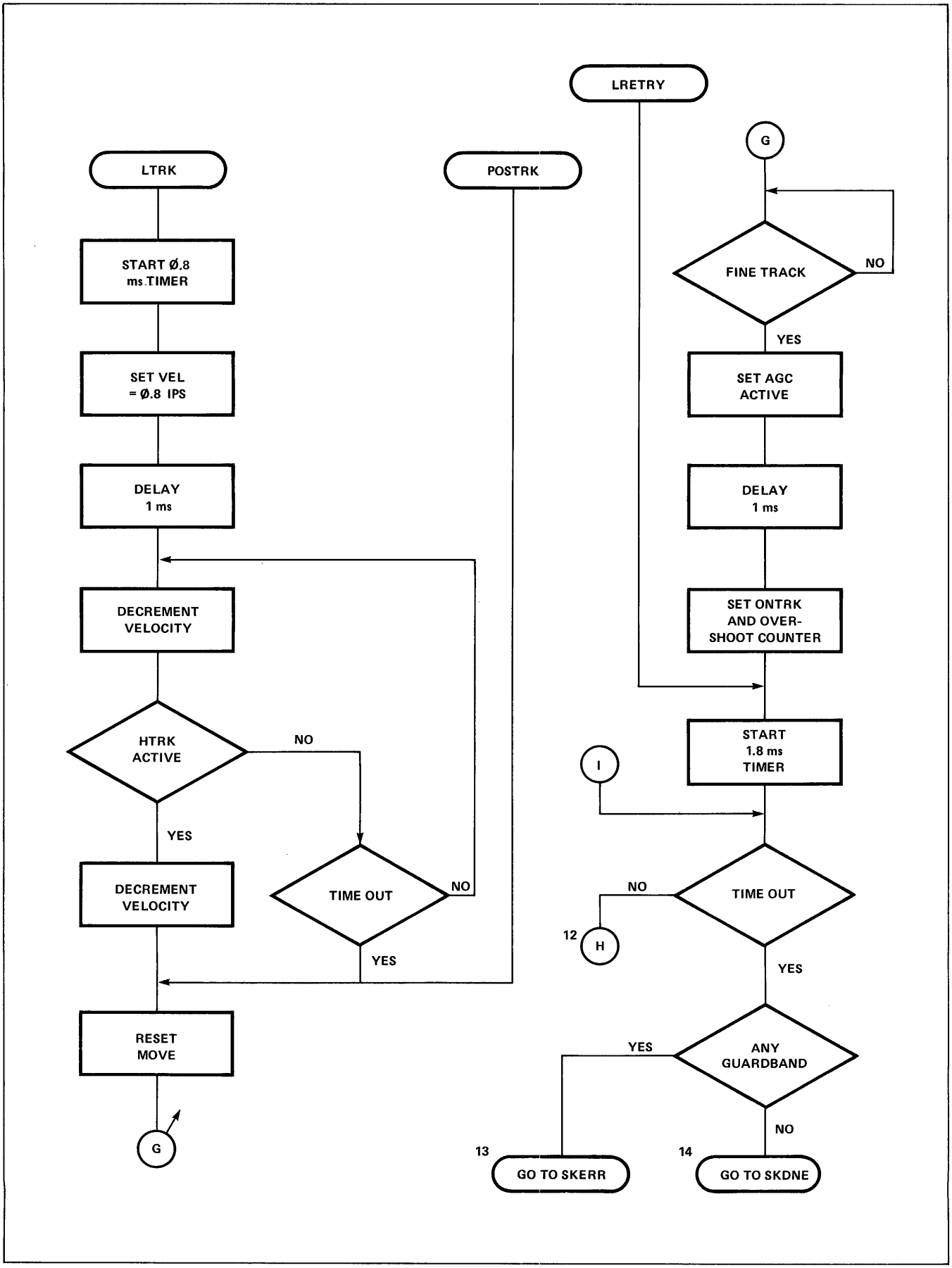


Figure 3-20. Last Track Flow Chart #1

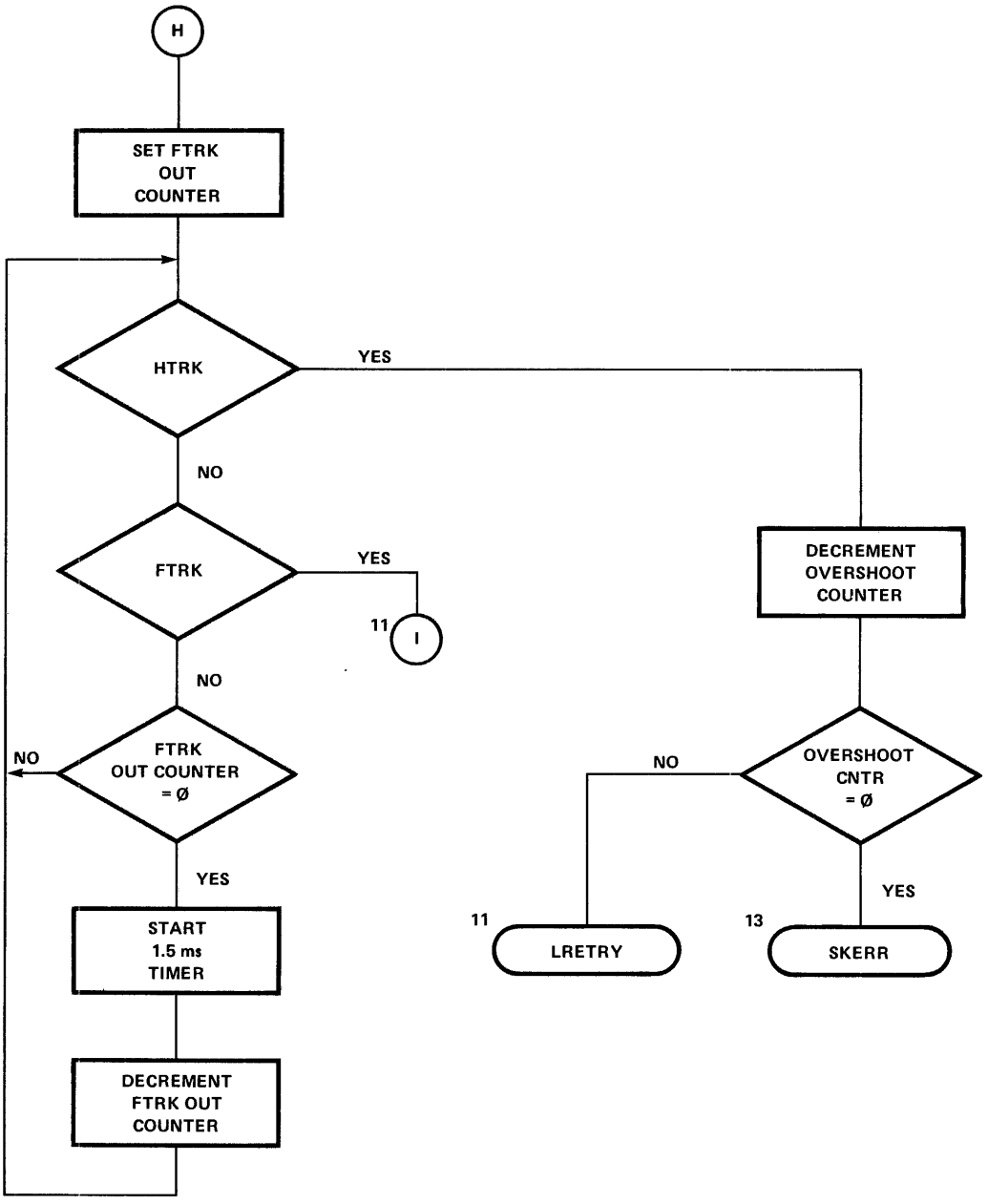


Figure 3-21. Last Track Flow Chart #2

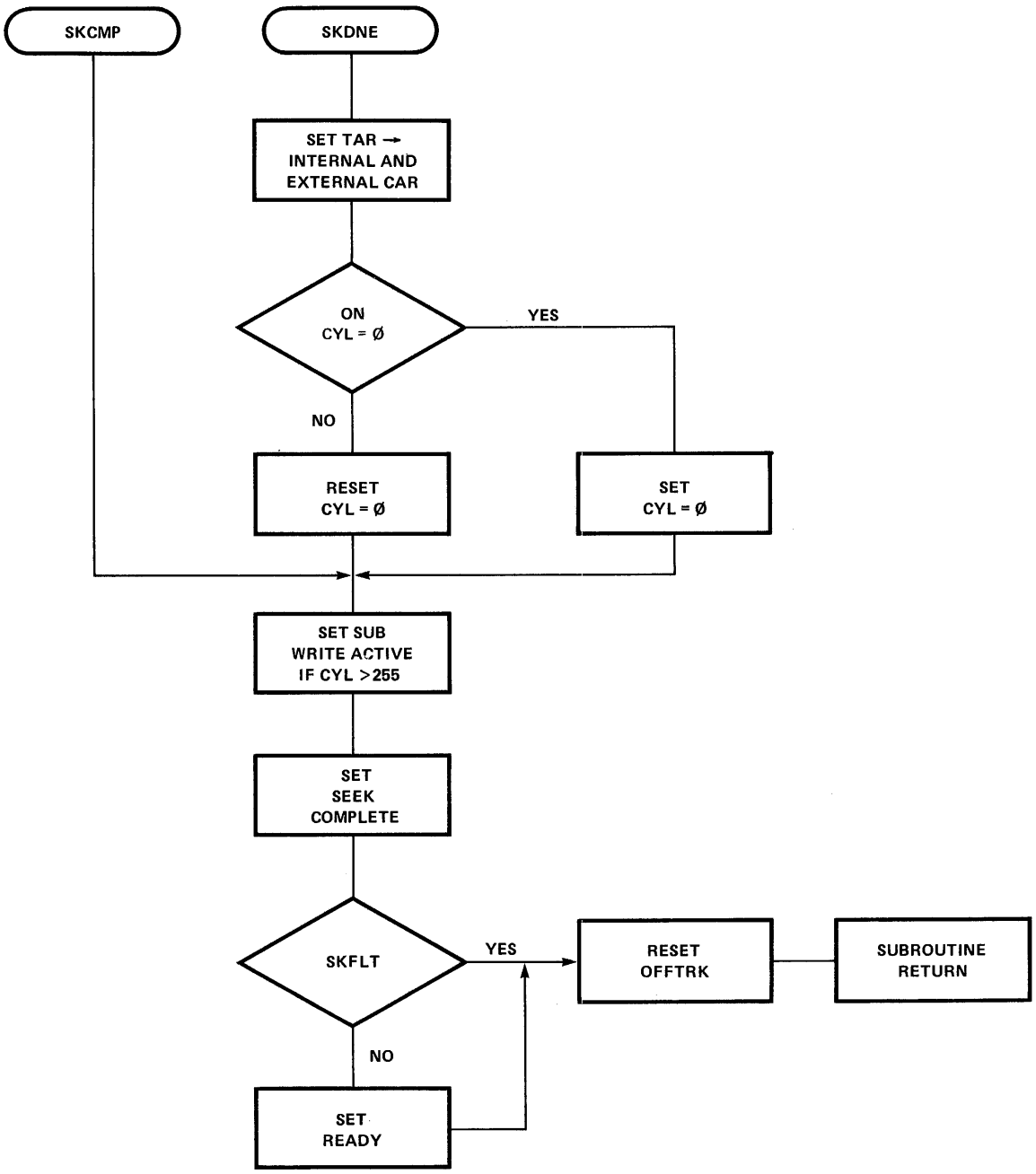


Figure 3-22. Seek Done Flow Chart

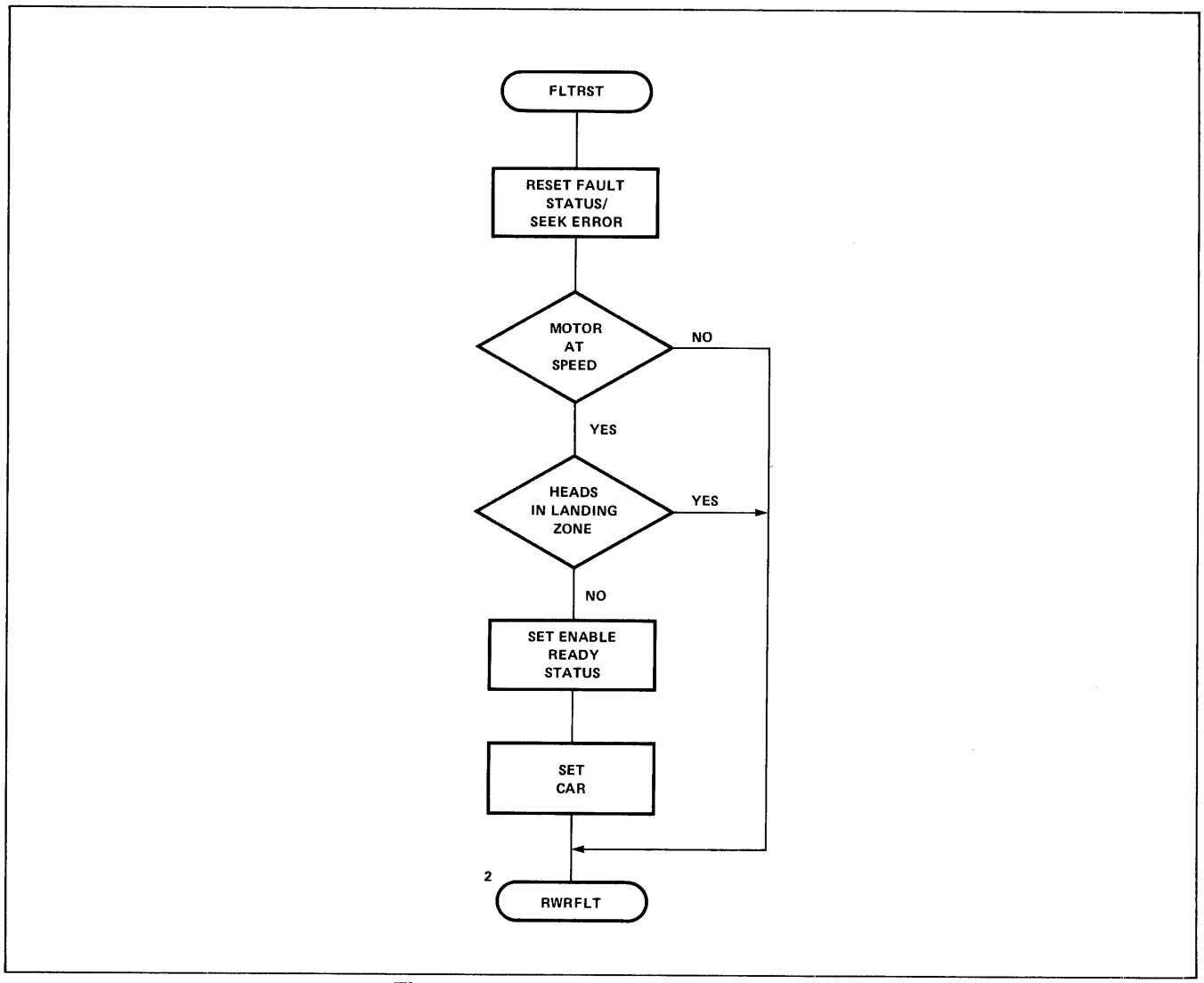


Figure 3-23. Fault Reset Flow Chart

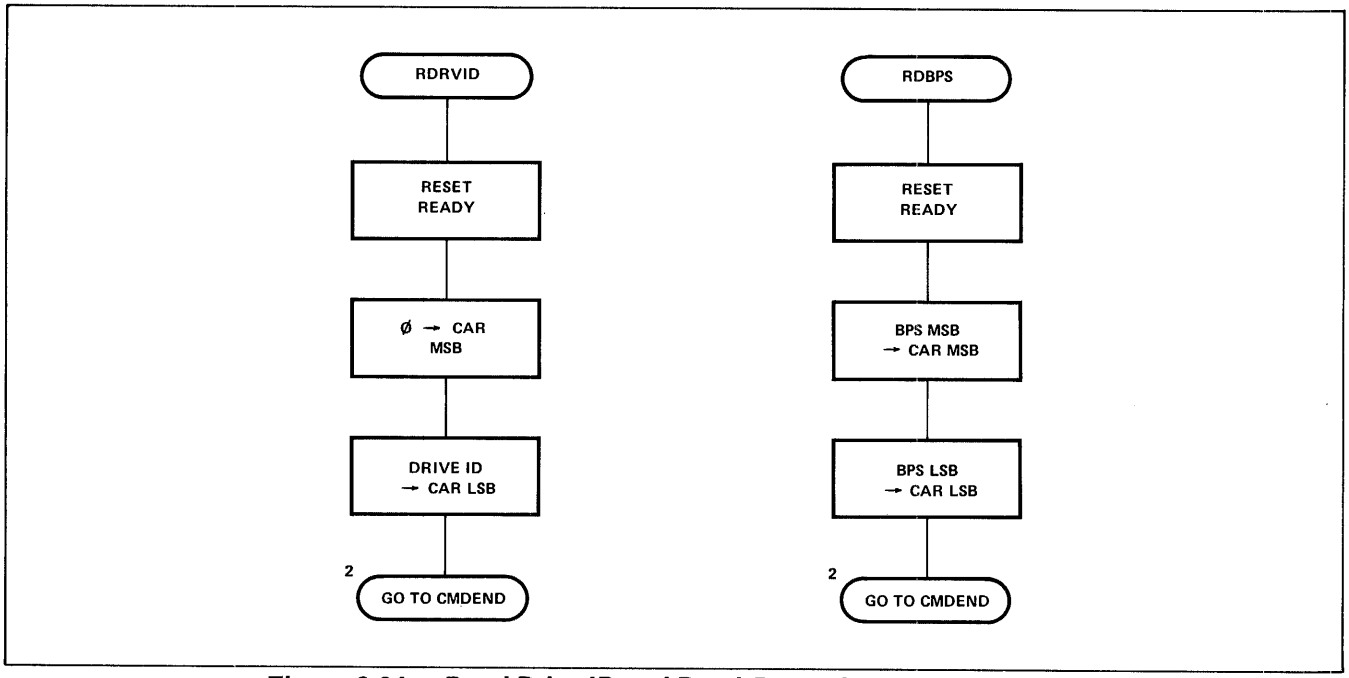


Figure 3-24. Read Drive ID and Read Bytes/Sectors Flow Chart

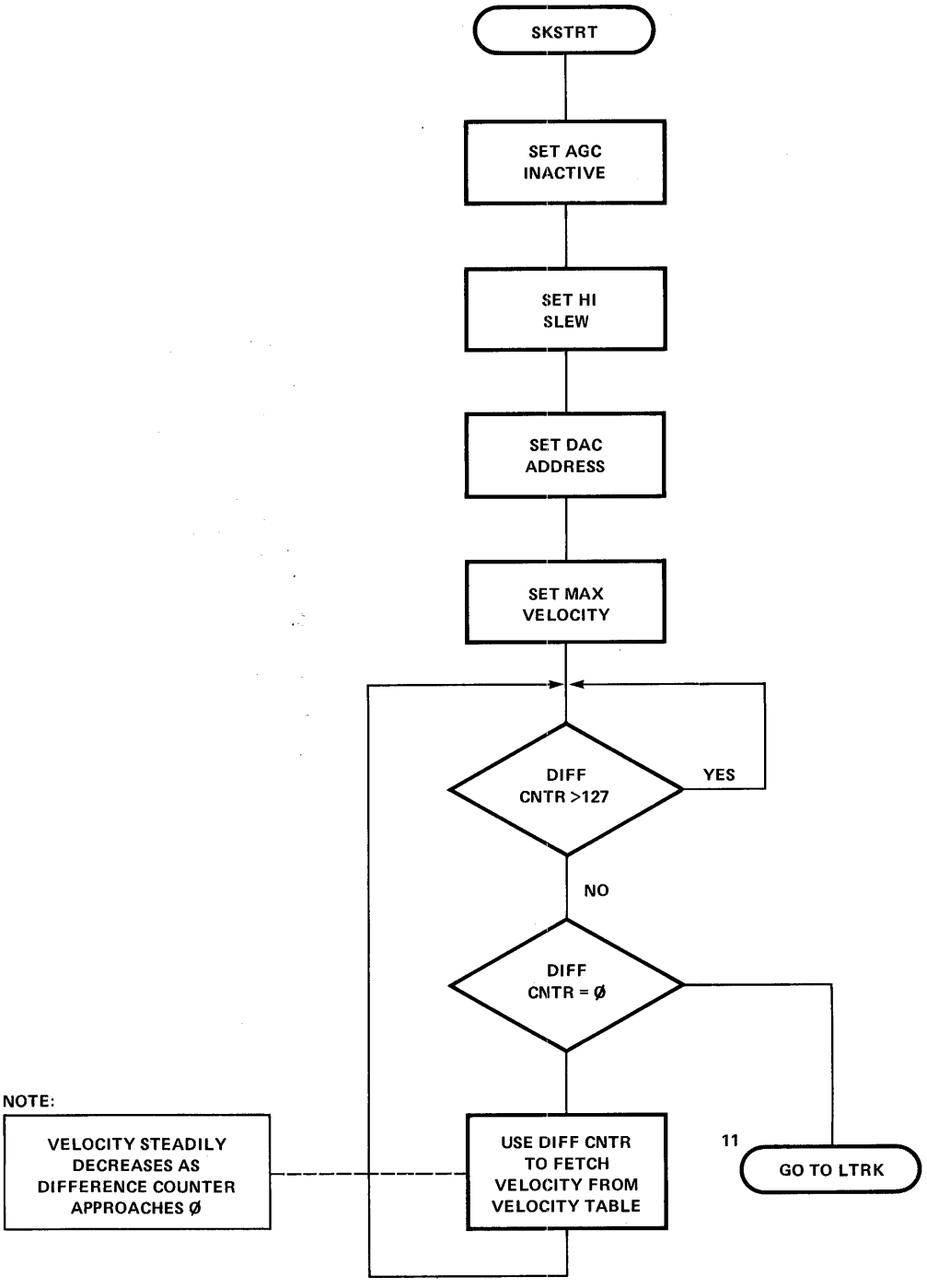


Figure 3-25. Seek Start Flow Chart

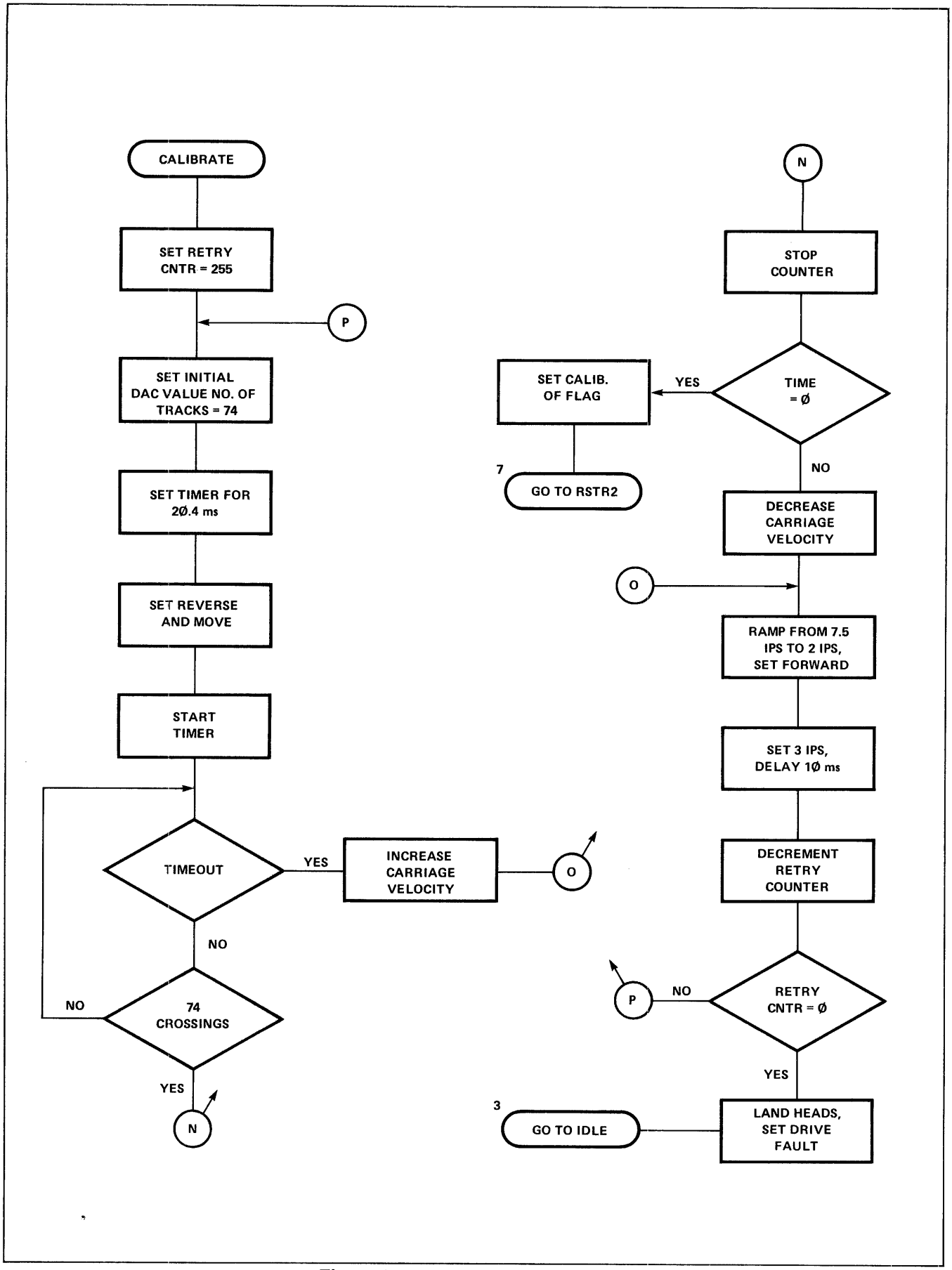


Figure 3-26. Calibrate Flow Chart

3.18.1 Interface Connectors. The interface connectors are 50-pin ribbon cable connectors, and provide for interface cable and terminator connections. The pins are numbered 1 through 50. A recommended mating connector is Spectra Strip 802-050-004 or Scotchflex 3425-0000. The lines (at the drive end) are described below.

PRIAM Interface Connector

Pin	Signal Name	Line Type
1	Ground	Ground
2	+DBUS 0	Bidirectional/Single
3	+DBUS 1	Bidirectional/Single
4	+DBUS 2	Bidirectional/Single
5	+DBUS 3	Bidirectional/Single
6	+DBUS 4	Bidirectional/Single
7	+DBUS 5	Bidirectional/Single
8	+DBUS 6	Bidirectional/Single
9	+DBUS 7	Bidirectional/Single
10	Ground	Ground
11	−READ GATE	Received/Single
12	Ground	Ground
13	−RESET	Received/Single
14	Ground	Ground
15	−WRITE GATE	Received/Single
16	Ground	Ground
17	−RD Received/Single	
18	−WR Received/Single	
19	+AD 1	Received/Single
20	+AD 0	Received/Single
21	Ground	Ground
22	−DRIVE SELECT 1	Received/Single
23	−DRIVE SELECT 2	Received/Single
24	−DRIVE SELECT 3	Received/Single
25	−DRIVE SELECT 4	Received/Single
26	Ground	Ground
27	Ground	Ground
28	+5 VCD (Terminator Box)	Diode OR'ed/Single
29	−HEAD SELECT 4	Received/Single
30	−HEAD SELECT 2	Received/Single
31	−HEAD SELECT 1	Received/Single
32	Ground	Ground
33	−INDEX	Transmitted/Single
34	Ground	Ground
35	−READY	Transmitted/Single
36	Ground	Ground
37	−SECTOR MARK	Transmitted/Single
38	Ground	Ground
39	+WRITE DATA	Received/DIFF
40	−WRITE DATA	Received/DIFF
41	Ground	Ground
42	+WRITE CLOCK	Received or Transmitted/DIFF
43	−WRITE CLOCK	Received or Transmitted/DIFF
44	Ground	Ground
45	+READ/REFERENCE CLOCK	Received or Transmitted/DIFF
46	−READ/REFERENCE CLOCK	Received or Transmitted/DIFF
47	Ground	Ground
48	+READ DATA	Transmitted/DIFF
49	+READ DATA	Transmitted/DIFF
50	Ground	Ground

3.18.2 DC Power Connector. This connector is used to supply DC power to the drive. It is a 6-pin AMP MATE-N-LOK connector, and the recommended mating connector is an AMP 1-480270-0 socket with AMP 0619-1 pins.

DC POWER CONNECTOR

J3− PIN	VOLTAGE
1	Ground
2	+24 VDC
3	−5 VDC
4	−12 VDC
5	+5 VDC
6	Ground (+24V Return)

3.18.3 AC Power Connector. This connector is used to supply AC power to the disc drive when the PRIAM optional power supply is used. The mating connector is a Belden 5PH-386 or equivalent.

AC POWER CONNECTOR

PIN	VOLTAGE
L	110 or 220 VAC (HOT)
E	Frame Ground
N	110 or 220 VAC (COMMON)

3.19 Interface Signal Descriptions. This section gives functional description for the signals on the 50-pin interface connector.

3.19.1 +DBUS 0-7. This high-active 8-bit wide bus is used to transfer commands and status (head carriage control and interface) between the disc drive and the controller. These lines connect directly to an 8304B (or 8286) bus transceiver, as shown in Figure 3.27. DC characteristics are listed in Table 3-2. These lines should be terminated at each end.

3.19.2 +AD 0-1. This high-active 2-bit wide address bus is used to select one of three registers into which data can be stored, or one of three registers from which data can be read. These lines connect directly to a 74LS244 Schmitt-triggered receiver gated by DRIVE SELECTED, as shown in Figure 3-28. The DC characteristics are listed in Table 3-3. These lines should be terminated at the drive end.

3.19.3 −RD. This low-active signal is used to gate the contents of the selected register (decode of ADI, ADO) onto the DBUS. This line is connected to a 74LS244, gated by DRIVE SELEC-

TED, as shown in Figure 3-28. The DC characteristics are listed in Table 3-3. This line should be terminated at the drive end.

3.19.4 −WR. This low-active signal is used to gate the DBUS into the selected register (decode of AD1, AD0). This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 3-28. The DC characteristics are listed in Table 3-28. The DC characteristics are listed in Table 3-3. This line should be terminated at the drive end.

3.19.5 −RESET. This low-active signal resets the drive logic. If the drive is sequenced down when RESET occurs, it will remain sequenced down. If the drive is sequenced up, it will remain up and the head carriage will Restore to cylinder zero. This line is connected to 74LS244, gated by DRIVE SELECTED, as shown in Figure 3-28. The DC characteristics are listed in Table 3-3. This line should be terminated at the drive end.

3.19.6 −DRIVE SELECT 1-4. These low-active signals (decoded) enable drive response. No readying, writing, register selection, or command response will occur unless the drive is selected. These lines are connected to single-ended receivers, as shown in Figure 3-29. The DC characteristics are listed in Table 3-4. This line should be terminated at the drive end.

3.19.7 −HEAD SELECT 1, 2, and 4. These low-active signals are used to select the desired data head for reading or writing. Head selection decoding is shown in Table 3-2. This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 3-28. The DC characteristics are listed in Table 3-3. This line should be terminated at the drive end.

3.19.8 −READY. This low-active signal from the drive indicates that the drive is up to speed and ready to read, write, or seek. This line is driven by a 75462 open collector driver, as shown in Figure 3-30. The DC characteristics are listed in Table 3-5. This line must be terminated at the controller end.

3.19.9 −INDEX. This low-active signal occurs once per revolution and indicates the beginning of a track. This line is driven by a 75462 open collector driver, as shown in Figure 3-30. The DC characteristics are listed in Table 3-5. This line must be terminated at the controller end.

3.19.10 −SECTOR MARK. This low-active signal indicates the beginning of a sector. This line is driven by a 75462 open collector driver, as shown in Figure 3-30. The DC characteristics are listed in Table 3-5. This line must be terminated at the controller end.

3.19.11 −WRITE GATE. This low-active signal enables the writing of data by a selected head. This line is connected to a 74LS244, as shown in Figure 3-28. The DC characteristics are listed in Table 3-3. If long cables are used, this line should be terminated at the drive end.

3.19.12 −READ GATE. This low-active signal initiates synchronization of the drive's phase lock loop for data separation. READ GATE must be enabled during a gap. This line is connected to a 74LS244, as shown in Figure 3-28. The DC characteristics are listed in Table 3-3. If long cables are used, this line should be terminated at the drive end.

3.19.13 +, −WRITE DATA. WRITE DATA is an NRZ serial data signal synchronous with WRITE CLOCK. WRITE DATA is received by an RS422 type differential line receiver as shown in Figure 3-31. The DC characteristics are listed in Table 3-6.

3.19.14 +, −WRITE CLOCK. This signal is switch selectable. It can be a square wave signal from the controller which is phased locked to the WRITE DATA, or (if the switch is in the other position) it can be a square wave signal from the drive to the controller to provide clocking and synchronization for WRITE DATA. The controller should be designed so that WRITE DATA is stable at the drive connector during the negative transition of WRITE CLOCK. WRITE CLOCK is received by an RS422 type differential line receiver, as shown in Figure 3-33. The DC characteristics are listed in Table 3-6. These lines should be terminated. If long cables are used, cable delays must be considered.

3.19.15 +, −READ/REFERENCE CLOCK. This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the servo clock or the VFO synchronized to the READ DATA signal. It is driven by an RS422 type differential driver, as shown in Figure 3-31. The DC characteristics are listed in Table 3-7.

3.19.16 +, −READ DATA. This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 9 microseconds after READ GATE is enabled. It is driven by an RS422 type differential drivers, as shown in Figure 3-31. The DC characteristics are listed in Table 3-7.

Of the above signals, there are several that are used specifically to facilitate serial data transfer between the disc drive and the controller. These are described below, with some additional details.

1. *INDEX* The INDEX pulse occurs whenever the servo track index mark is encountered, to indicate the beginning of a track.

2. *READY* The READY signal indicates that the selected drive is ready to read, write, or seek. When READY is false, the controller should not initiate WRITE, READ, or SEEK commands. However, READY will go false when a SEEK command is initiated. READY will later go true when the head carriage is positioned on the specified cylinder, if no fault condition exists.

3. *SECTOR MARK* The SECTOR MARK pulse occurs at the beginning of each sector (sector size is selectable by setting the mini-switches on the read/write digital PCB).

4. *HEAD SELECT 1, 2, and 4* These low-active signals are gated by DRIVE SELECTED, and are used to select the data head, as shown in Table 3-1.

Table 3-1. Head Selection

Head Select 1	Head Select 2	Head Select 4	Selected Head 3450 7050
High	High	High	Zero
Low	High	High	One
High	Low	High	Two
Low	Low	High	Three
High	High	Low	Four
Low	High	Low	Zero*
High	Low	Low	Zero*
Low	Low	Low	Zero*

* = Selected by default because of the number of heads available.

5. *WRITE GATE* WRITE GATE when active, enables data to be written on the disc. READY must be true before WRITE GATE is activated. Any attempt to write between INDEX and the first SECTOR MARK will result in a DRIVE FAULT, because the prerecorded skip defect information is write protected. DRIVE FAULT will also be set if any of the following conditions occur during a write operation.

Drive Fault Conditions

1. WRITE GATE without write current at the head
2. Write current at the head without WRITE GATE
3. WRITE GATE without READY
4. More than one head selected
5. No transitions during write
6. WRITE GATE with WRITE PROTECT
7. Spindle speed error
8. RESET while drive is Sequenced Up
9. Off-Track condition when track following (READY true)
10. Failure to Restore
11. Software Error (time out of watch dog timer)

6. *WRITE CLOCK* WRITE CLOCK provides clocking and synchronization for WRITE DATA. The controller generates WRITE CLOCK by echoing the READ/REFERENCE CLOCK signal back to the drive, with suitable phase delay relative to WRITE DATA.

7. *WRITE DATA* WRITE DATA provides the data to be stored on the disc. NRZ (non-return-to-zero) data is required for WRITE DATA. READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is retransmitted back to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry.

8. *READ GATE* READ GATE must be enabled in a gap area (all 0s recorded), and at least 9 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Activating READ GATE during a data record may cause the VFO to spuriously lock in an incorrect phase relationship for decoding the recorded information.

   Six microseconds after the leading edge of READ GATE, the internal READ CLOCK signal is enabled to the READ/REFERENCE CLOCK interface signal lines.

9. *READ/REFERENCE CLOCK* READ/REFERENCE CLOCK provides clocking and synchro-

nization for reading and writing data. When READ GATE is not active, READ/REFERENCE CLOCK is switched to the PLO clock, which is phased locked to the servo signal. A change in the phase of READ/REFERENCE CLOCK will occur when it is switched between the servo and VFO clocks.

10. *READ DATA* Data from the drive is in serial NRZ (non-return-to-zero) form, and is synchronized with READ/REFERENCE CLOCK after a 6-microsecond delay from the leading edge of READ GATE. READ DATA may not be valid for the first 9 microseconds after READ GATE is enabled.

3.19.17 Interface DC Characteristics. This section, through tables and figures, sets forth the details that need to be observed, in order to properly transmit and receive the interface signals. The signal characteristics are shown in Table 3-2 to 3-10 and Figures 3-27 to 3-24.

Table 3-2. DBUS Transceiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OL}	Output Low Level		0.5	V	$I_{OL}=32$ mA
V_{OH}	Output High Level	2.4		V	$I_{OL}=-5$ mA
I_{OFF}	Output Off Current		−0.2	mA	$V_{OFF}=0.45$ V
		+0.2		mA	$V_{OFF}=5.25$ V
V_{IL}	Input Low Level		0.9	V	
V_{IH}	Input High Level	2.0		V	

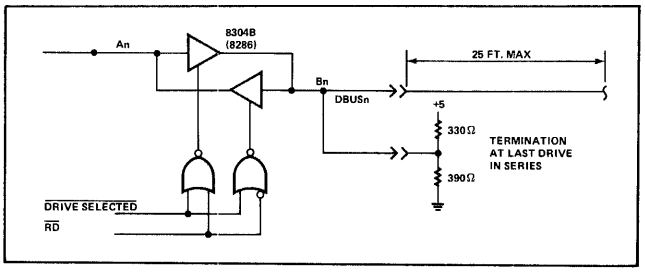


Figure 3-27. DBUS Transceiver

Table 3-3. Single End Line Receiver Gated by DRIVE SELECTED Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Level	2.0		V	
V_{IL}	Input Low Level		0.8	V	
I_{IH}	High Level Input Current		0.02	mA	$V_I=2.7$ V
I_{IL}	Low Level Input Current		−0.2	mA	$V_I=0.4$ V

Cable connections should be terminated at the last drive.

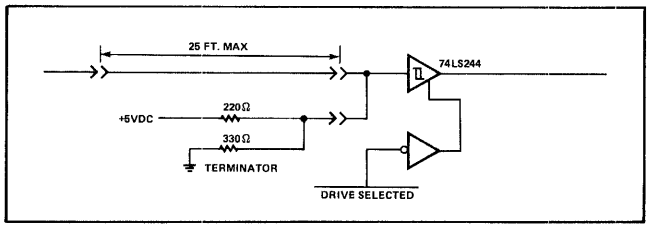


Figure 3-28. Single End Line Receiver Gated By DRIVE SELECT

Table 3-4. Single End Line Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{T+}	Positive-going Threshold	1.4	1.9	V	
V_{T-}	Negative-going Threshold	0.5	1.0	V	
I_{IH}	High Level Input Current		0.02	mA	$V_I=2.7$ V
I_{IL}	Low Level Input Current		−0.2	mA	$V_I=0.4$ V

Cable connections should be terminated at the last drive.

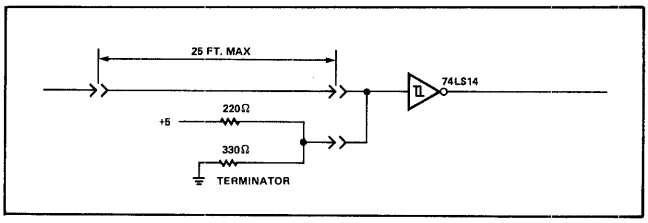


Figure 3-29. Single End Line Receiver

Table 3-5. Single End Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OH}	High Level Output Current		0.1	mA	
I_{OL}	Low Level Output Current	300		mA	
V_{OH}	High Level Output Voltage	2.4		V	
V_{OL}	Low Level Output Voltage		0.8	V	I_{OL} = 300 mA

This line must be terminated at the controller end.

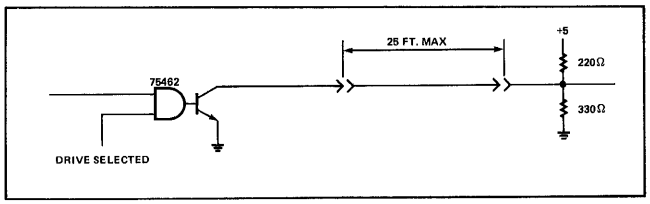


Figure 3-30. Single End Line Driver

Table 3-6. Differential Line Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{TH}	Differential Input High Threshold		0.2	V	
V_{ICR}	Common Mode Input Range	±15		V	
$I_{I(REC)}$	Reveiver Input Current		2.3	mA	

Table 3-7. Differential Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	High Level Output Voltage	2.5		V	I_{OH} = −20 mA
V_{OL}	Low Level Output Voltage		0.32	V	I_{OL} = 20 mA
I_{OZ}	Output Off Current		±0.2	mA	
I_{OH}	High Level Output Current		−20	mA	
I_{OL}	Low Level Output Current		+20	mA	
I_{OS}	Short Circuit	−30	−150	mA	

Note: The last drive in a string should be terminated.

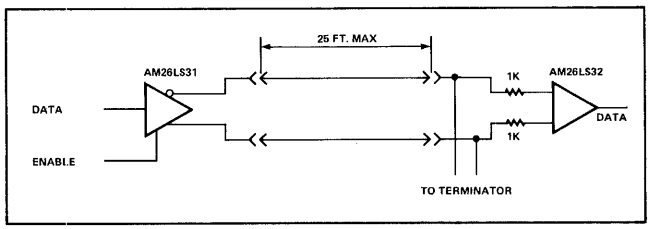


Figure 3-31. Differential Line Drivers and Receivers

3.19.18 Interface Timing. This section discusses the timing requirements for the various operations performed on the controller interface.

1. *Register Load Timing* Register load timing is shown in Figure 3-32. The AC characteristics are listed in Table 3-8.

Table 3-8. Register Load AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{AW}	Address stable before WR	60		ns
t_{WA}	Address hold time for WR	30		ns
t_{WW}	WR pulse width	100		ns
t_{DW}	Data set up time for WR	60		ns
t_{WD}	Data hold time for WR	30		ns
t_{RV}	Recovery time between WR	200		ns

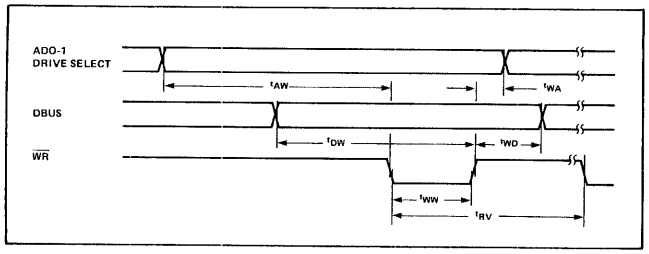


Figure 3-32. Register Load Timing

2. *Register Read Timing* Register read timing is shown in Figure 3-33. The AC characteristics are listed in Table 3-9.

Table 3-9. Register Read AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{AR}	Address stable before RD	60		ns
t_{RA}	Address hold time for RD	30		ns
t_{RR}	RD pulse width	100		ns
t_{RD}	Data delay from RD		60	ns
t_{DF}	RD to data floating	10	40	ns

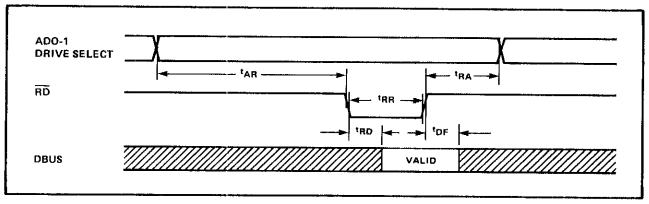


Figure 3-33. Register Read Timing

3. *Reset Timing* Reset timing is shown in Figure 3-34. The AC characteristics are listed in Table 3-10.

Table 3-10. Reset AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{RST}	RESET pulse width	100		ms
t_{SR}	DRIVE SELECT TO RESET	0		ns

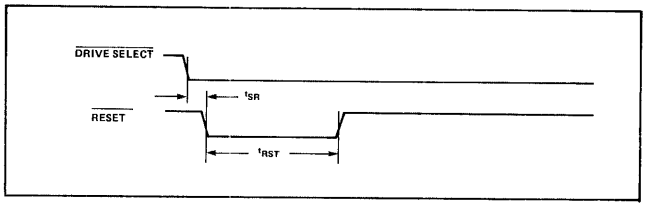


Figure 3-34. Reset Timing

4. *INDEX AND SECTOR MARK Timing* INDEX and SECTOR MARK timing is shown in Figure 3-35. The AC characteristics are listed in Table 3-11.

Table 3-11. INDEX and SECTOR MARK AC Characteristics

Symbol	Parameter	Timing	Units
t_{IW}	INDEX pulse width	2.48 ± .25	μs
t_{IR}	INDEX period	16.67 ± .4	ms
t_{SW}	SECTOR MARK pulse width	1240 ± 160	ns
t_{IS}	INDEX to first SECTOR	44.6 ± 1.4	μs
t_{BYTE}	Byte period	1240 ± 184	ns

t_{SR} = Sector width = (Sector size in bytes) x (t_{BYTE}) ± 10%

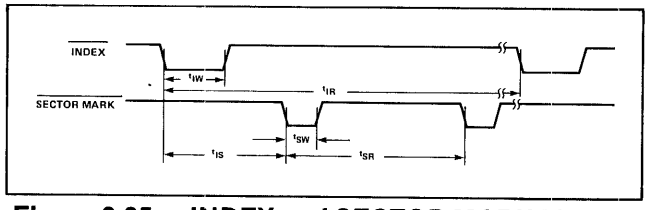


Figure 3-35. INDEX and SECTOR MARK Timing

5. *WRITE DATA and WRITE CLOCK Timing* WRITE DATA and WRITE CLOCK timing is shown in Figure 3-36. The AC characteristics are listed in Table 3-12.

Table 3-12. WRITE DATA and WRITE CLOCK AC Characteristics

Symbol	Parameter	Timing	Units
t_{CLK}	WRITE CLOCK period	155 ± 25	ns
t_{WH}	WRITE CLOCK high pulse width	77.5 ± 12.5	ns
t_{WL}	WRITE CLOCK low pulse width	77.5 ± 12.5	ns
t_{BIT}	WRITE DATA bit period	155 ± 23	ns
t_{DC}	WRITE DATA setup time	20*	ns min
t_{CD}	WRITE DATA hold time	20*	ns min
t_{BYTE}	Byte period	1240 ± 184	ns
*	60 ns typical		

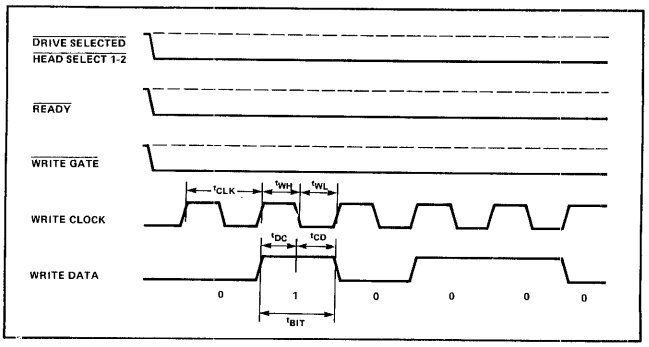


Figure 3-36. WRITE DATA and WRITE CLOCK Timing

6. *READ DATA and READ CLOCK Timing* READ DATA and READ CLOCK timing is shown in Figure 3-37. The AC characteristics are listed in Table 3-13.

Table 3-13. READ DATA and READ CLOCK AC Characteristics

Symbol	Parameter	Timing	Units
t_{CLK}	READ CLOCK period	155 ± 25	ns
t_{WH}	READ CLOCK high pulse width	77.5 ± 12	ns
t_{WL}	READ CLOCK low pulse width	77.5 ± 12	ns
t_{BIT}	READ DATA bit period	155 ± 23	ns
t_{DC}	READ DATA setup time	40*	ns min
t_{CD}	READ DATA hold time	40*	ns min
t_{BYTE}	Byte period	1240 ± 184	ns
*	60 ns is typical		

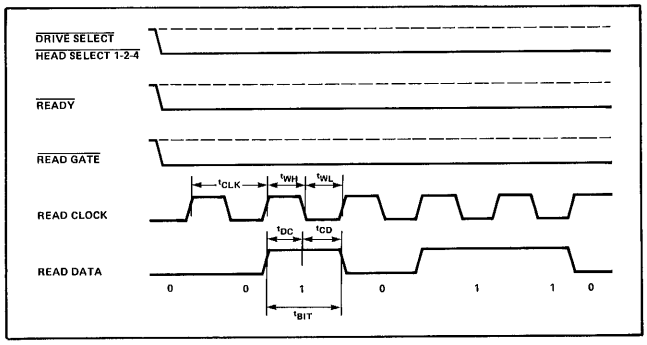


Figure 3-37. READ DATA and READ CLOCK Timing

7. *Record Writing* Figure 3-38 shows the timing requirement for writing full sectors (ID and data fields) and also writing data fields only. The AC characteristics are listed in Table 3-14.

Table 3-14. Record Writing Control AC Characteristics

Symbol	Parameter	Timing	Units
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20	μs min
t_{SR}	DRIVE SELECTED to READY	100	ns min
t_{SG}	SECTOR MARK to WRITE GATE	0 ± 1	μs min
t_{IDG}	ID gap timing	23	bytes min
t_{IDF}	ID fill	2	bytes min
t_{DG}	Data gap (no write-to-read transitions)	11	bytes min
T_{DF}	Data fill	2	bytes min
t_{HW}	HEAD SELECTED OR WRITE GATE	100	ns
t_{BYTE}	Byte period	1240 ± 184	ns

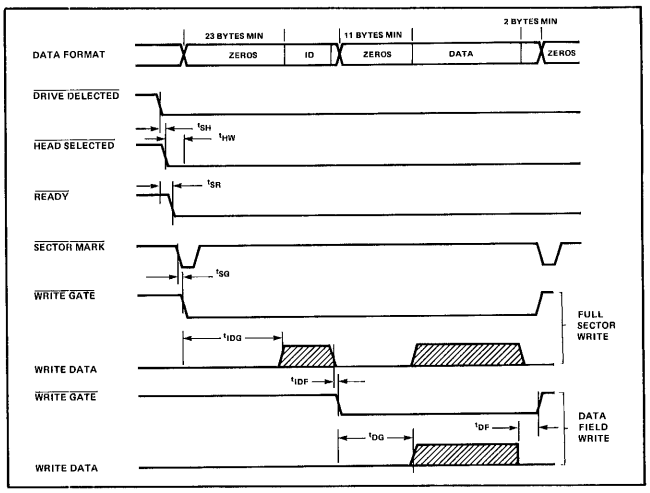


Figure 3-38. Record Writing Timing

8. *Record Reading* Figure 3-39 shows the timing requirements for reading full sectors (ID and data fields) and also for reading data fields only. The AC characteristics are listed in Table 3-15.

Table 3-15. Record Reading Control AC Characteristics

Symbol	Parameter	Timing	Units
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20	µs
t_{SR}	DRIVE SELECTED to READY	100	ns min
t_{RDLW}	READ GATE delay for gaps allowing write-to read transitions	13	µs min
t_{RDLR}	READ GATE delay for gaps limited to read-to-read or read-to-write transitions	1.9	µs min
t_{SYN}	Read PLO synchronization (data not valid during this period)	9	µs min
t_{HR}	HEAD SELECTED to READ GATE	25	µs min
t_{BYTE}	Byte period	1240 ± 184	ns

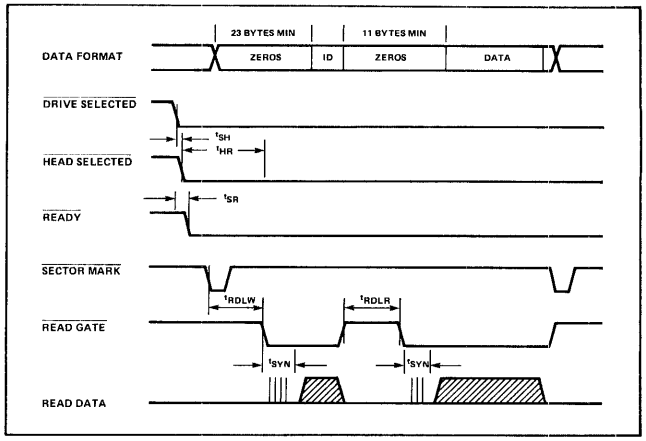


Figure 3-39. Record Reading Timing

The combined operations are shown in Figure 3-40.

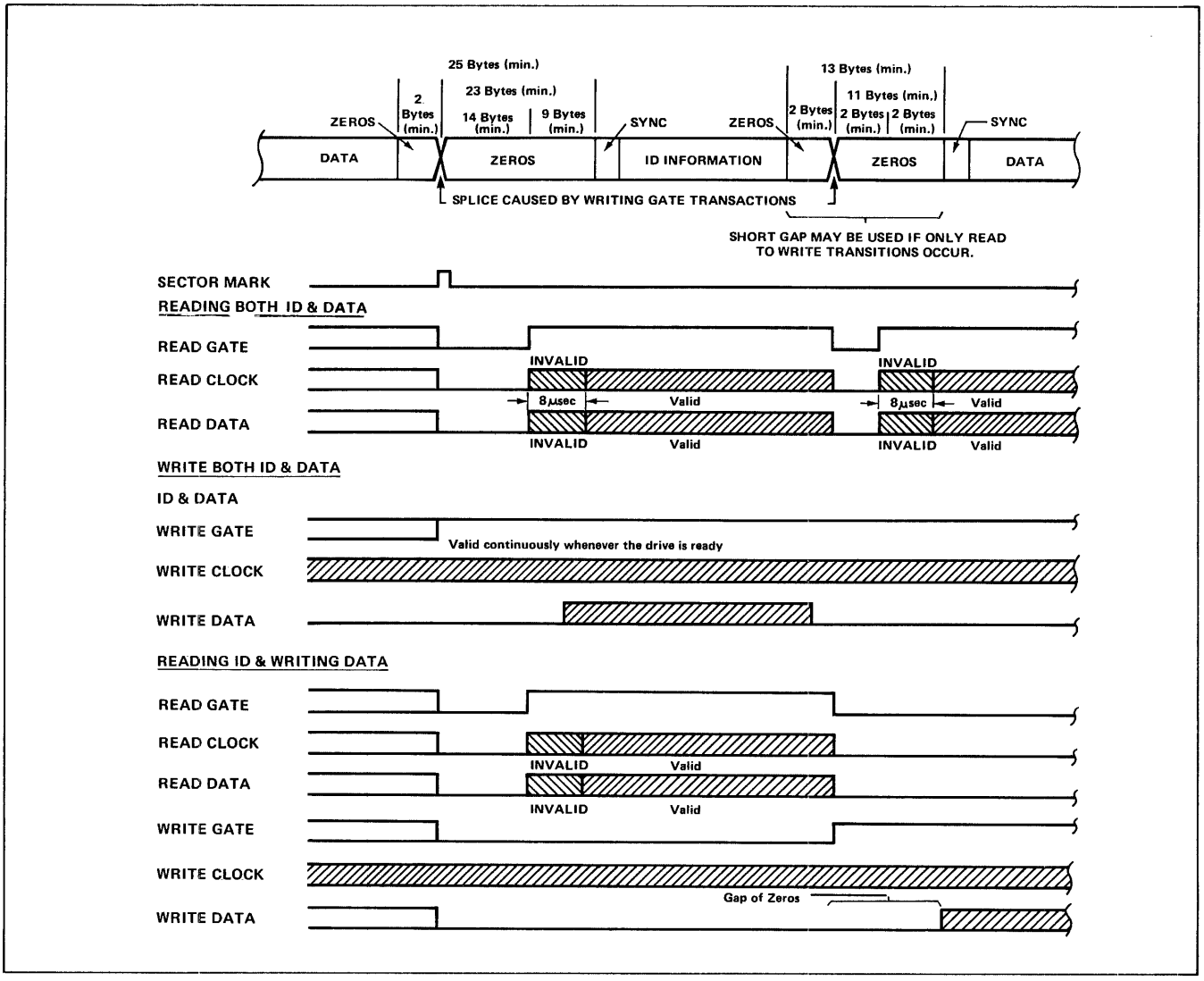


Figure 3-40. Read and Write Transitions During Gap

3.19.19 User-Accessible Registers. The user (controller) sends control commands and target cylinder addresses to the disc drive via the eight bidirectional bus lines DBUS 0-7. The disc drive sends status information and current cylinder address information to the controller via these same eight lines. DBUS 0-7 is a tri-state bus, and thus these lines present an open circuit to the controller's data bus unless they have been activated by DRIVE SELECT. An active DRIVE SELECT combined with an active WR enables the drive's line receivers on DBUS 0-7, so that the information on the bus can be written into the drive's three control registers. An active DRIVE SELECT combined with an active RD enables the drive's line drivers on DBUS 0-7, so that the information in the drive's three status-like registers can be returned to the controller. The following six registers are involved:

The COMMAND REGISTER receives and stores commands from the controller.

The TARGET ADDRESS REGISTER—UPPER BYTE receives and stores the two or three most significant bits of the desired cylinder address.

The TARGET ADDRESS REGISTER—LOWER BYTE receives and stores the eight least significant bits of the desired cylinder address.

The STATUS REGISTER holds current drive status information.

The CURRENT ADDRESS REGISTER—UPPER BYTE holds the two or three most significant bits of the current cylinder address.

The CURRENT ADDRESS REGISTER—LOWER BYTE holds the eight least significant bits of the current cylinder address.

The registers are accessed by activating the appropriate combinations of address lines A1 and A0, and the WR or RD signal, as shown in Table 3-16. Note that the command and target address registers are write-only, while the status and current address registers are read-only.

Table 3-16. Register Selection.

RD	WR	A1	A0	Selected Register
0	1	0	0	Command Register
0	1	0	1	Target Address—Upper Byte
0	1	1	0	Target Address—Lower Byte
1	0	0	0	Status Register
1	0	0	1	Current Address—Upper Byte
1	0	1	0	Current Address—Lower Byte

Note: 1 = Active, 0 = Inactive.

3.19.20 Commands. Table 3-17 lists the command codes for the valid commands. The commands are discussed individually following Table 3-17.

Table 3-17. Command Code Summary.

	DBUS							
Command Name	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Sequence Up	0	0	0	0	0	0	0	1
Sequence Down	0	0	0	0	0	0	1	0
Restore	0	0	0	0	0	0	1	1
Seek	0	0	0	0	0	1	0	0
Fault Reset	0	0	0	0	0	1	0	1
Read Drive ID	0	0	0	1	0	0	0	0
Read Bytes/Sector	0	0	0	1	0	0	0	1

3.19.21 Sequence Up. The Sequence Up command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and after the drive is up to speed, the heads are positioned to cylinder zero. The drive presents BUSY status (BUSY bit set in the status register) while Sequence Up is in process. At the successful completion of Sequence Up, BUSY is cleared and CYLINDER ZERO, SEEK COMPLETE, and READY are set. If Sequence Up is unsuccessful, WRITE PROTECT and DRIVE FAULT are set.

3.19.22 Sequence Down. The Sequence Down command causes the heads to be positioned to the landing zone, and the spindle motor to be braked to a stop. WRITE PROTECT status is set at the completion of Sequence Down.

3.19.23 Restore. The Restore command causes the head carriage to be positioned to cylinder zero. The drive Restores automatically on Sequence Up, or when a SEEK FAULT is detected. If the Restore command is unsuccessful, the heads will be positioned to the landing zone, and DRIVE FAULT status will be set. If the drive is not sequenced up, the Restore command will function as a Sequence Up Command.

3.19.24 Seek. The Seek command causes the drive to seek to a specified cylinder. Prior to issuing the Seek command, the controller must place the desired cylinder address in the target address registers. Upon receipt of the Seek command, the drive clears READY status and sets BUSY, while moving the head carriage to the correct cylinder. When this has been done, the drive sets READY and also sets SEEK COMPLETE status. If the Seek command is unsuccessful, the drive Restores to cylinder zero, and sets READY, CYLINDER ZERO, and SEEK FAULT status.

3.19.25 Fault Reset. The Fault Reset command clears the two fault conditions — SEEK FAULT and DRIVE FAULT.

3.19.26 Read Drive ID. The Read Drive ID command loads the drive ID into the lower byte of the current address register, and clears READY status. The controller may then retrieve the information by reading the lower byte of the current address register. The values of the ID code for various PRIAM disc drives are given in Table 3-18.

After the DRIVE ID information has been read by the controller, a Sequence Up or Restore command must be issued to bring the drive back to the READY state. In general, the current address registers contain the current cylinder address if the drive is READY, and the last requested parameter information if the drive is not READY.

3.19.27 Read Bytes per Sector. The Read Bytes per Sector command loads the number of bytes per sector into the current address registers, and clears READY status.

As with the Read Drive ID command, a Sequence Up or Restore command must be issued to bring the drive back to the READY state.

Table 3-18. Drive ID Assignments

ID Code (Hex)	Drive Designation	
00	Not Valid	
01	DISKOS 3350-10 or 3350-10	(20,160 bytes/track)
02	DISKOS 3350-01	(19,960 bytes/track)
03	DISKOS 3450	(12,960 bytes/track)
04	DISKOS 3450	(13,440 bytes/track)
05	DISKOS 7050	(13,440 bytes/track)
06	DISKOS 6650	
07	DISKOS 15450	
08-0F	Reserved	
10	Reserved	
11	DISKOS 1070-1	
12	CD8005	
13	CD8010	
14	Reserved	
15	DISKOS 1070-2	
16-1F	Reserved	
20-FF	Reserved	

3.19.28 Register Bit Definitions. Register Bit Definitions are presented in Tables 3-19 and 3-20.

Table 3-19. Status Register Bit Definitions

Bit	Name	Description
0	READY	The drive is up to speed, the servo system is locked onto a servo track, and the drive is able to read, write or seek.
1	SEEK COMPLETE	A seek operation has been completed. This bit is not valid when the BUSY bit is set.
2	SEEK	A fault was detected during a seek operation. This bit is not valid when the BUSY bit is set.
3	CYLINDER ZERO	The head carriage is at cylinder zero. This bit is not valid when the BUSY bit is set.
4	BUSY	The drive is in the process of executing a command.
5	DRIVE FAULT	A fault was detected during a write operation, or a drive unsafe condition was detected.

Table 3-19. Status Register Bit Definitions (cont'd.)

Bit	Name	Description
6	WRITE PROTECT	The selected head is write protected. WRITE PROTECT is set by switches on the main PCB. The entire drive is write protected when it is not sequenced up.
7	COMMAND REJECT	The controller attempted to write to a register when the drive was not READY, or an invalid command was received by the drive. This bit is not valid when the BUSY bit is set.

Table 3-20. Address Register Bit Definitions

Byte	Bit Number 7	6	5	4	3	2	1	0
Upper Byte	0	0	0	0	0	C_{10}	C_9	C_8
Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

As indicated in the above table, up to eleven bits of information can be stored in the address registers. This information may be the target cylinder address, the current cylinder address, or the requested parametric information, such as bytes per sector or drive ID. C_{10} is the most significant bit, and C_0 is the least significant bit.

3.20 SMD Interface

3.20.1 Overview. PRIAM offers an optional SMD interface, designed to permit PRIAM Winchester disc drives to be used with existing Storage Module Device (SMD) controllers. This interface is available as an SMD Adapter with all PRIAM 8-inch disc drives.

Two interface cables are used with the SMD interface — a 60-conductor "A" cable and a 26-conductor "B" cable. Line drivers and receivers in the SMD interface are matched to those of typical SMD controllers.

Two SMD drive characteristics that are not supported by PRIAM drives are the support of address marks and dual porting. Also, PRIAM uses pin numbers 59 and 60 ("A" cable spares) to allow, at the user's option, 11-bit cylinder addresses, whereas 10-bit cylinder addresses are the SMD standard.

Some interface lines have timing characteristics that vary somewhat as a function of the PRIAM drive type. This variation is due to differences in the basic product characteristics. The following lines are affected:

Tag 2
Index
Sector
Seek End
On Cylinder
Return to Zero
Power Sequence Pick
Power Sequence Hold

3.20.2 Connectors and Pin Assignments. Two cables are used for transmitting signals between the disc drive and the controller. One (the "A" cable) contains parallel data, status, Unit Select, and control signals. The other ("B" cable) contains serial data, clocking and sync signals.

A termination resistance is required at the transmitter and receiver end of each transmission line in the "A" cable. This resistance is provided on the drive by an optional terminator assembly which must be ordered separately. A standard SMD termination resistance is required at the controller end of each "A" cable line, except for the Open Cable Detect Line.

A termination resistance (as shown in Section 11.4) is required at the receiver end of each transmission line in the "B" cable. At the disc drive end, this resistance is provided on the SMD adapter.

Characteristics of the required connectors and cables are listed on the following pages.

I/O Cable Connectors

"A" Cable

Description	Berg Part Number	Spectra Strip Part Number
Connector (60 pin)	65043-007	
Contact, insert	48048	
Flat Cable (twisted Pair) 30 pairs, 28 AWG		3CT-6028-7B-05-100

"A" Cable Mating Connector on Drive or Controller

Description	AMP Part Number
60 pin right angle header	3-86479-4
60 pin vertical header	3-87227-0

"B" Cable

Description	3M Part Number
Connector (26 pin)	3399-3000
Connector pull tab	3490-2
Flat cable (26 connector) with ground plane and drain wire	

"B" Cable Mating Connector on Drive or Controller

Description	AMP Part Number
26 pin right angle header	1-86479-0
26 pin vertical header	1-87227-3

I/O Cable Characteristics

"A" Cable

Type:	30 twisted pair, flat cable
Twists per inch:	2
Impedance:	100 ± 10 ohms
Wire size:	28 AWG, 7 strands
Propagation time:	1.6 to 1.8 ns/foot
Maximum cable length:	100 feet cumulative
Voltage rating:	300 volts rms

"B" Cable (With Ground Plane)

Type:	26 conductor, flat cable with ground plane and drain wire
Impedance:	65 ohms (3M part number 3476-26)
Wire size:	28 AWG, 7 strands
Propagation time:	1.5 to 1.8 ns/foot
Maximum cable length:	50 feet
Voltage rating:	300 volts rms

"B" Cable

Type:	Twinax
Impedance:	160 ± 16 ohms
Wire size:	30 AWG, 7 strands
Diameter over outer insulator:	0.620″ maximum
Propagation velocity:	70% minimum
Maximum cable length:	50 feet

3.20.3 Interface Signal Descriptions. This section gives functional descriptions for the signals on the "A" and "B" interface connectors.

Address and control information is transferred to the drive on a 10-bit bus, with three tag lines defining the type of information on the bus. Unit selection is provided by four binary coded lines gated into the drive by a Unit Select tag. Major status conditions of the selected drive, as well as index and sector marks, are returned to the controller on seven lines.

Data and clock signals between the drive and the controller require five lines. These lines are associated with a physical drive using a radial connection between the drive and the controller. Two additional lines in this cable supply an interrupt signal (Seek End) and an indication of selection (Unit Selected). See Tables 3-21, 3-22, and 3-23 for the pin assignments of these lines on the two interface cables.

Table 3-21. Tab Bus I/O Interface ("A" Cable)

Function	Connector Pins Low	High
Unit Select Tag	43	44
Unit Select 2^0	45	46
Unit Select 2^1	47	48
Unit Select 2^2	51	52
Unit Select 2^3	53	54
Tag 1	1	2
Tag 2	3	4
Tag 3	5	6
Bit 0	7	8
Bit 1	9	10
Bit 2	11	12
Bit 3	13	14
Bit 4	15	16
Bit 5	17	18
Bit 6	19	20
Bit 7	21	22
Bit 8	23	24
Bit 9	25	26
Open Cable Detector	27	28
Index	35	36
Sector	49	50
Fault	29	30
Seek Error	31	32
On Cylinder	33	34
Unit Ready	37	38
Unused (always 0)	39	40
Write Protected	55	56
Power Sequence Pick		57
Power Sequence Hold		58
Unused	41	42
Spare (Optional Bus Bit 10)	59	60

60 position, 28 AWG, 30 twisted pair straight flat cables maximum length — 100 feet

Table 3-22. Tag Bus Decode ("A" Cable)

Bus	Tag 1 Cylinder Address	Tag 2 HEAD Select	Tag 3 Control Select
Bit 0	2^0	2^0	Write Gate
Bit 1	2^1	2^1	Read Gate
Bit 2	2^2	2^2	Unused
Bit 3	2^3	Unused	Unused
Bit 4	2^4	Unused	Fault Clear
Bit 5	2^5	Unused	Unused
Bit 6	2^6	Unused	RTZ
Bit 7	2^7	Unused	Unused
Bit 8	2^8	Unused	Unused
Bit 9	2^9	Unused	Unused
Bit 10 (optional)	2^{10}	Unused	Unused

Table 3-23. "B" Cable Interface.

Function	Connector Pins Low	Connector Pins High	Connector Pin Layout	
Write Data	15	14	2	1△
Ground		13	4	3
Write Clock	11	12	6	5
Ground		10	8	7
Servo Clock	3	2	10	9
Ground		1	12	11
Read Data	5	6	14	13
Ground		4	16	15
Read Clock	9	8	18	17
Ground		7	20	19
Seek End	19	20	22	21
Unit Selected	18	17	24	23
Ground		16	26	25
Index	23	22		
Ground		21		
Sector	25	26		
Ground		24		

26 connector flat cable
maximum length — 50 feet

1. The 10 bus lines are used to transmit cylinder address, head address, or control functions from the controller to the drive. Bit 0 is the least significant bit, and Bit 9 is the most significant bit (unless Bit 10 is used).

   If the optional Bus Bit 10 is used, Bit 10 is the most significant bit. The normally spare pair, pins 59 and 60 of "A" Cable, is used for this purpose. This bit is enabled (on the SMD adapter attached to a 7050) by moving the jumper from position W10 to position W21.

2. *Tag 1 (Cylinder Address)* When Tag 1 is active, the ten (or eleven) bus lines are used to carry the cylinder address to the drive. Since the drive is a direct addressing device, the controller need only place the new address on the lines and strobe the lines with Tag 1 (see Figure 3-44). The drive must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

3. *Tag 2 (Head Select)* When Tag 2 is active, the bus bit lines are used to carry the head address information to the drive. The controller places the head addresses on the lines with Tag 2.

   In the 3450 and 7050, only bus bits 0, 1, and 2 are used. All other bus bits are ignored.

4. *Tag 3 (Control Select)* Tag 3 acts as an enable, and must be true for the entire control operation (see Table 3-22).

   a. Bit 0 (Write Gate)

      Write Gate enables the write driver. See Figure 3-47 for typical Write Gate timing requirements.

      NOTE: Write Gate to Read Gate timing is 14 microseconds (see Figure 3-47) instead of the 10 microseconds required by the standard SMD specification.

   b. Bit 1 (Read Gate)

      Read Gate enables digital read data onto the Read Data lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern (see Figures 3-45, 3-46, and 3-47 for typical Read Gate timing).

      NOTE: Write Gate to Read Gate timing is 14 microseconds (see Figure 3-47) instead of the 10 microseconds required by the standard SMD specification.

   c. Bit 2 (Servo Offset Plus)

      In all drives using the SMD adapter, this function is not supported, and no response will occur when this operation is attempted.

   d. Bit 3 (Servo Offset Minus)

      In all drives using the SMD adapter, this function is not supported, and no response will occur when this operation is attempted.

e. Bit 4 (Fault Clear)

This line clears Fault status. The Fault status may recur if the fault condition still exists.

f. Bit 5 (AM Enable)

Not supported by this interface. No response will occur when this operation is attempted.

g. Bit 6 (RTZ)

This line moves the head carriage to cylinder zero, sets the head address to head zero, and clears Seek Error.

h. Bit 7 (Data Strobe Early)

Not supported by this interface. No response will occur when this operation is attempted.

i. Bit 8 (Data Strobe Late)

Not supported by this interface. No response will occur when this operation is attempted.

j. Bit 9 (Release)

Not supported by this interface. No response will occur when this operation is attempted.

5. *Unit Select Tag* Unit Select Tag is used to select the drive defined by the Unit Select 1, 2, 4 and 8 lines. The drive is selected at the leading edge of Unit Select Tag, and responds (within 200 nanoseconds) with Unit Selected. The drive address on the Unit Select lines must be stable 200 nanoseconds before the leading edge of Unit Select Tag.

   In all drives using the SMD adapter, the Unit Select Tag must remain stable throughout the time that the drive is selected. For detailed timing information, see Figure 3-49.

6. *Unit Select 1, 2, 4 and 8* These four lines are binary coded to select one of 16 logical drive addresses. The address placed on the Unit Select lines is compared by each drive against the logical address determined by the settings of the drive address switches on the main PCB. When the Unit Select Tag rises, the drive which compares equal becomes the one selected. Care must be taken to assure that each physical drive is assigned a different logical address.

   Four dip switches are used for assigning the drive a logical address at installation time, or at any subsequent time.

7. *Individual Lines*

   a. Sector

   The sector mark is derived from the servo track data, using a byte counter. Timing integrity is maintained throughout seek operations (see Figure 3-48). The number of sectors per revolution and/or the number of bytes per sector, is switch selectable. In the 3450 and 7050, the sector switches are located on the read/write digital PCB. See the INSTALLATION section for specific information on switch settings.

   The microprocessor sets sector size during initialization. If the switch settings are changed while the drive is powered up, power must be removed from the drive and then restored to cause the newly selected sector size to be established at the drive.

   b. Fault

   When the Fault Line is true, a fault condition exists at the drive. The drive can detect the following types of faults:

   1. Write Fault (Write Gate with Write Protect)
   2. Write Off Cylinder (Write Gate without On Cylinder)
   3. Multiple Heads Selected
   4. No transitions during write (MFM format)
   5. Write Gate without write current at the head
   6. Write current at the head without Write Gate
   7. Write when servo is off track
   8. Write during a Servo Offset operation
   9. Write Gate and Read Gate occurring simultaneously
   10. Read Off Cylinder (Read Gate without On Cylinder)
   11. Unable to Restore (RTZ) drive

A Fault condition immediately inhibits writing. The Fault line may be reset by Fault Clear, or by Restore (RTZ).

   c. *Seek Error* When the Seek Error line is true, a seek error has occurred. The Seek Error line may be reset by RTZ. Seek Error indicates that the drive was unable to complete a seek operation. When this condition is detected, the drive automatically returns to cylinder zero.

Note: For 3450s a seek address greater than 525 (20D hex), or for 7050s a seek address greater than 1049 (419 hex) will cause Seek Error to go true within 450 microseconds, instead of the 100 nanoseconds required by the standard SMD specification.

d. On Cylinder

On Cylinder indicates that the servo has positioned the heads over the desired data tracks. On Cylinder is reset by a Seek operation or a Restore operation.

e. Index

The Index signal occurs once per revolution. Its leading edge is considered the leading edge of Sector Zero. Index is typically a two-byte wide pulse (see Figure 3-48). Timing integrity is maintained throughout seek operations.

f. Unit Ready

Unit Ready indicates that the drive is up to speed, the heads are positioned over the recording surface, and no fault condition exists.

g. Open Cable Detector

Open Cable Detector must be false to Gate the select bits into the compare circuitry.

The open cable detect circuit disables the interface whenever the "A" Cable is disconnected.

h. Address Mark Found

Address Mark Found is not supported by this interface. This line is always false.

i. Unit Selected

When the four Unit Select lines compare with the setting of the drive address switches on the SMD adapter, and the Unit Select Tag is active, the Unit Selected line on the "B" Cable goes true (see Figure 11.5-6). If, on a multi-drive system, multiple Unit Selected responses are received by the controller, it may indicate that duplicate switch settings have been used.

j. Write Protected

Setting the Write Protect switch on the drive's read/write digital PCB inhibits all write operations, and causes the Write Protected line to be true.

Attempting to write to a protected drive will cause the Fault line to go true.

k. Seek End

Seek End is the OR combination of On Cylinder or Seek Error. It indicates that a seek operation has terminated (see Figure 11.5-1 for timing details).

l. Power Sequencing

Power Sequencing is not supported by this interface. Power Sequence Pick and Power Sequence Hold are interconnected to represent a Sequenced Up drive at all times.

Both Power Sequence Pick and Power Sequence Hold must be held at ground potential to enable drive operation. If either line is open, or at +1.4 volts or greater, the drive will sequence down (move the heads to the landing zone and stop the spindle motor) and remain sequenced down until both lines are again at ground potential. When this occurs, the drive will sequence up and, when the motor is at speed, become Ready.

m. Busy

The Busy indication is not supported by this interface.

8. *Data and Clock Line* (see Figure 3-50)

a. Write Data

The Write Data Lines carry NRZ data to be recorded on the disc.

b. Servo Clock

The Servo Clock is a phased-locked clock generated from the servo track data. It is used to synchronize write data. Servo Clock is available at all times (not gated by Unit Select) that the drive is Ready.

c. Read Data

The Read Data lines transmit the recovered data in NRZ form.

d. Read Clock

The Read Clock signal defines the beginning of data bit cell. Read Clock is an internally

derived clock signal that is synchronous with the recovered data, as shown in Figure 3-50. Read Clock is in phase sync with the Read Data within 8 microseconds after the leading edge of Read Gate.

e. Write Clock

The Write Clock signal from the controller to the drive must be synchronized with the NRZ write data, as shown in Figure 11.5-7. The Write Clock is the Servo Clock retransmitted to the drive during a write operation. Write Clock need not be transmitted continuously, but must be transmitted during, and at least 250 nanoseconds prior to Write Gate.

3.20.4 Interface DC Characteristics. This section, through tables and figures, sets forth the details that need to be observed in order to properly transmit and receive the interface signals.

All input and output signals are digital, using SMD standard transmitters and receivers to provide a terminated, balanced transmission system.

The "A" cable is a twisted pair flat cable. The "B" cable is a flat ribbon cable with ground plane and drain wire. Twisted pair or ground plane shielding, or both, are used to minimize crosstalk and to reduce inductive coupling.

1. *Terminated and Balanced Transmission System* Transmitters and receivers of the SMD standard types 75110A and 75108 or equivalent are used to provide a terminated and balanced transmission system, as shown in Figure 3-41.

*Terminating resistors are on adapter logic card or controller. These signals must be star cabled.

2. *Line Transmitter Characteristics* The SMD standard line transmitters (Figure 3-42) are compatible with the line receivers described below.

a. Output Signal Levels

Data Signals: see Figure 3-41.
Control Signals: see Figure 3-42.

b. Output Line Polarity

Control Signals: On the "A" Cable, the transmitters are connected to the I/O line so that the output, labeled Z (Figure 3-42) is connected to the odd numbered pin of the cable connector. This output in turn connects to the receiver pin labeled B (Figure 3-43) except for the Unit Selected line, which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver,

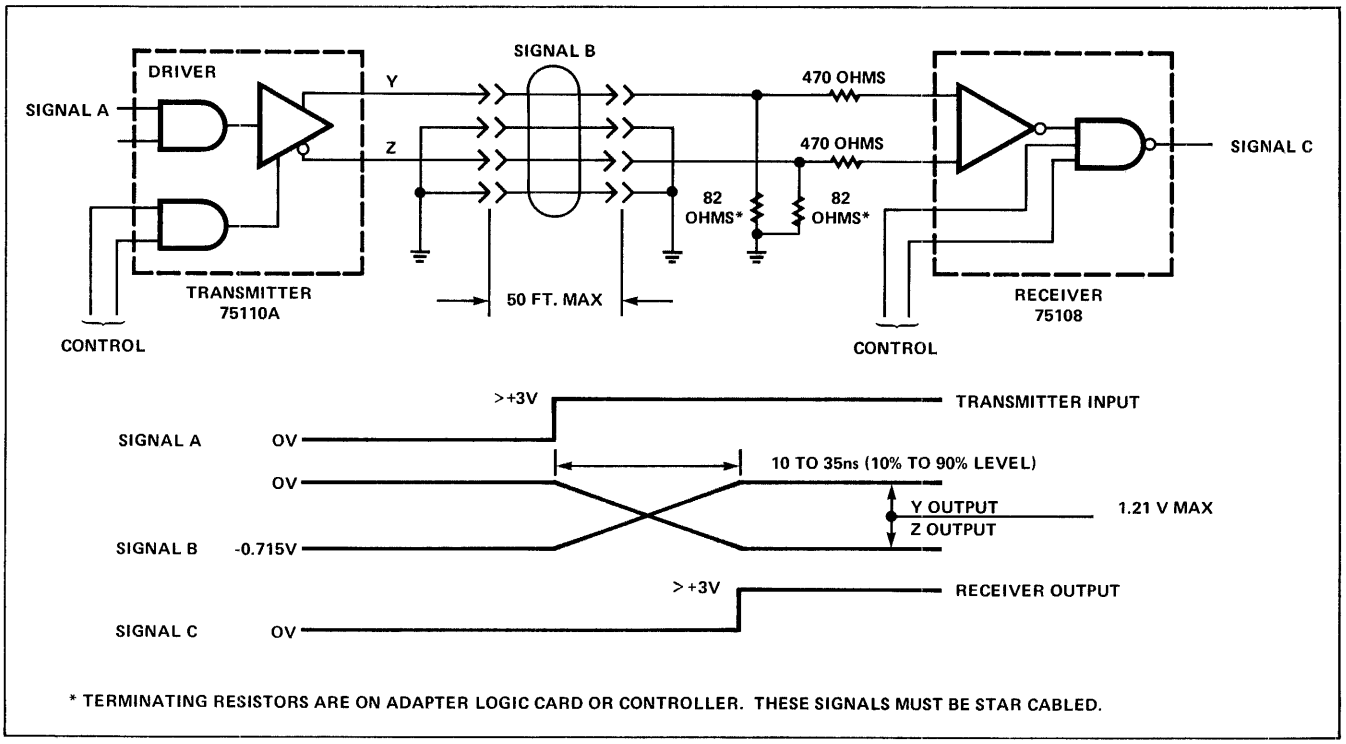


Figure 3-41. Typical Read/Write Data and Clock Transmitter and Receiver

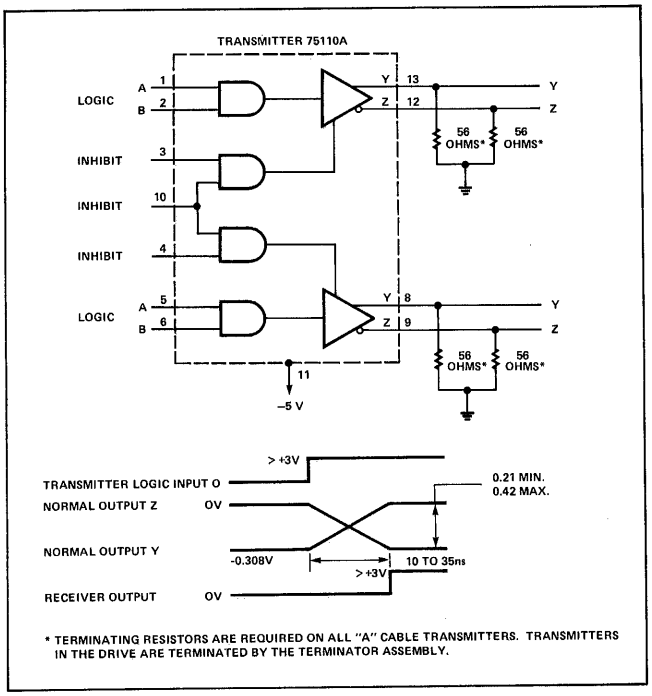


Figure 3-42. Control Line Transmitter

except for the Unit Selected line, where a logical 1 into the transmitter produces a logical 0 out of the receiver.

3. *Input Amplifier (Receiver) Characteristics* The drive's input amplifier (Figure 3-43) is SMD-standard compatible with the line transmitter described above.

   a. Receiver Propagation Delay

   The receiver propagation delay is typically 17 nanoseconds, both for a logical 0-to-1 transition and for a logical 1-to-0 transition.

   b. Receiver Input Polarity

   Control Signals: The input, labeled B (Figure 3-43) of the receiver is connected to the odd numbered pin of the cable connector, and thus connects to the transmitter pin labeled Z (Figure 3-42).

   Data Signals: see Figure 3-41.

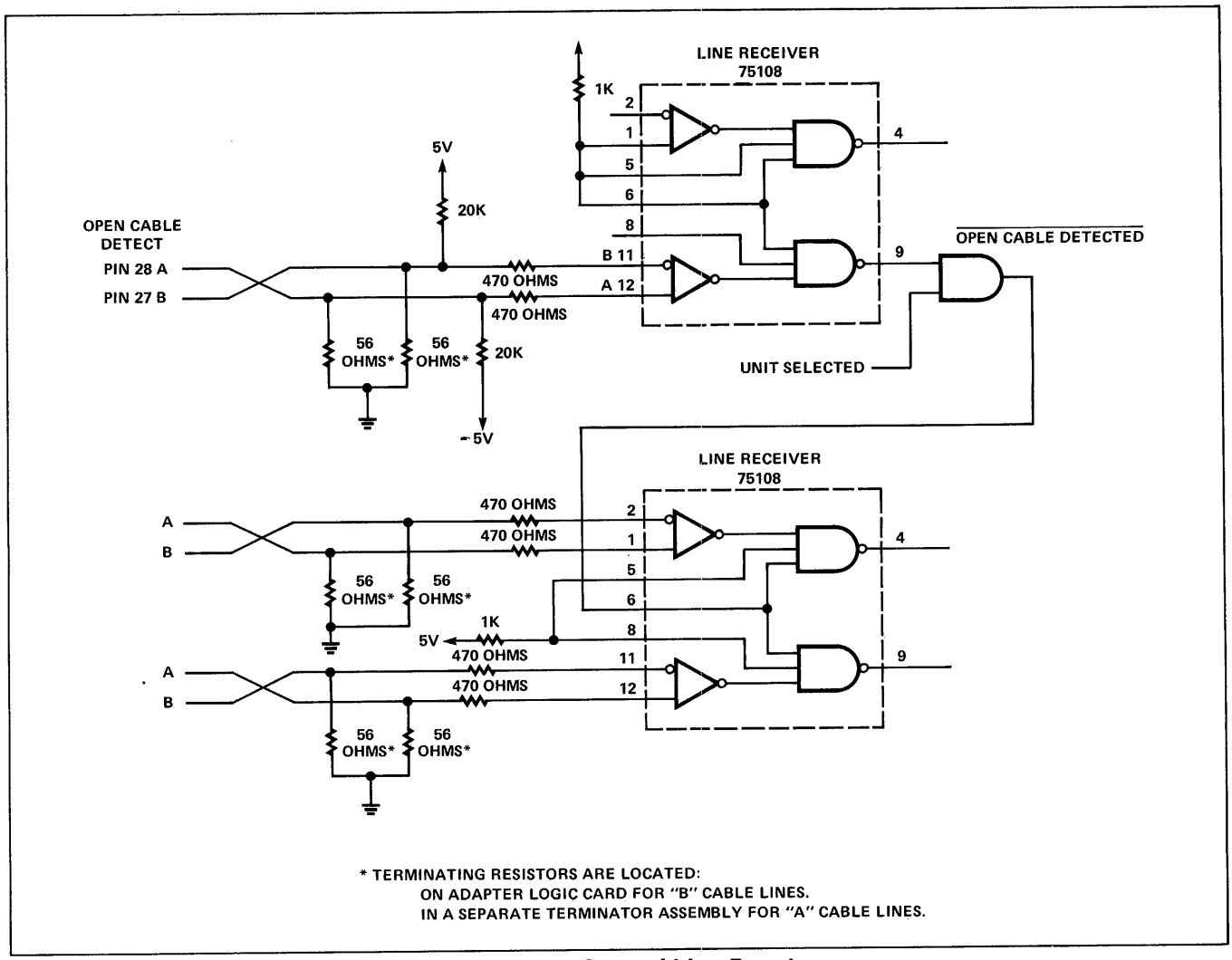
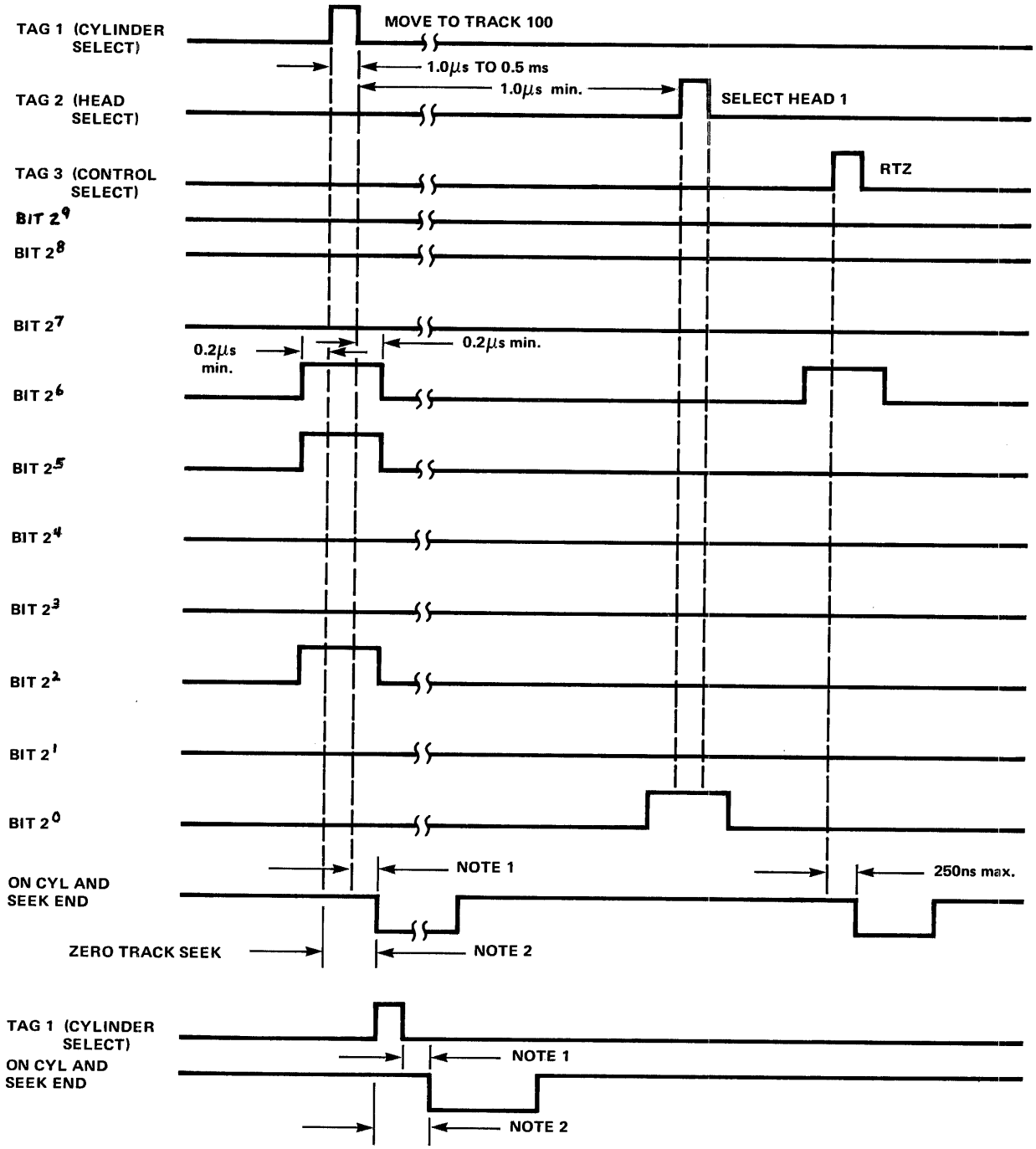


Figure 3-43. Control Line Receiver

3.20.5 Interface Timing. This section discusses the timing requirements for the various operations performed on the controller interface.



NOTE 1: 120 ns MAXIMUM FOR 3350 SMD, 6650 SMD, AND 15450 SMD (14" DRIVES WITH IMBEDDED SMD INTERFACE). SEE NOTE 2 FOR ALL OTHER DRIVES.

NOTE 2: 450 ns FROM LEADING EDGE OF TAG 1 FOR ALL DRIVES USING SMD ADAPTER.

ON CYLINDER AND SEEK END SIGNALS ARE IDENTICAL UNLESS A SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END UNTIL RTZ CLEARS THE ERROR.

Figure 3-44. Tag and Bus Timing

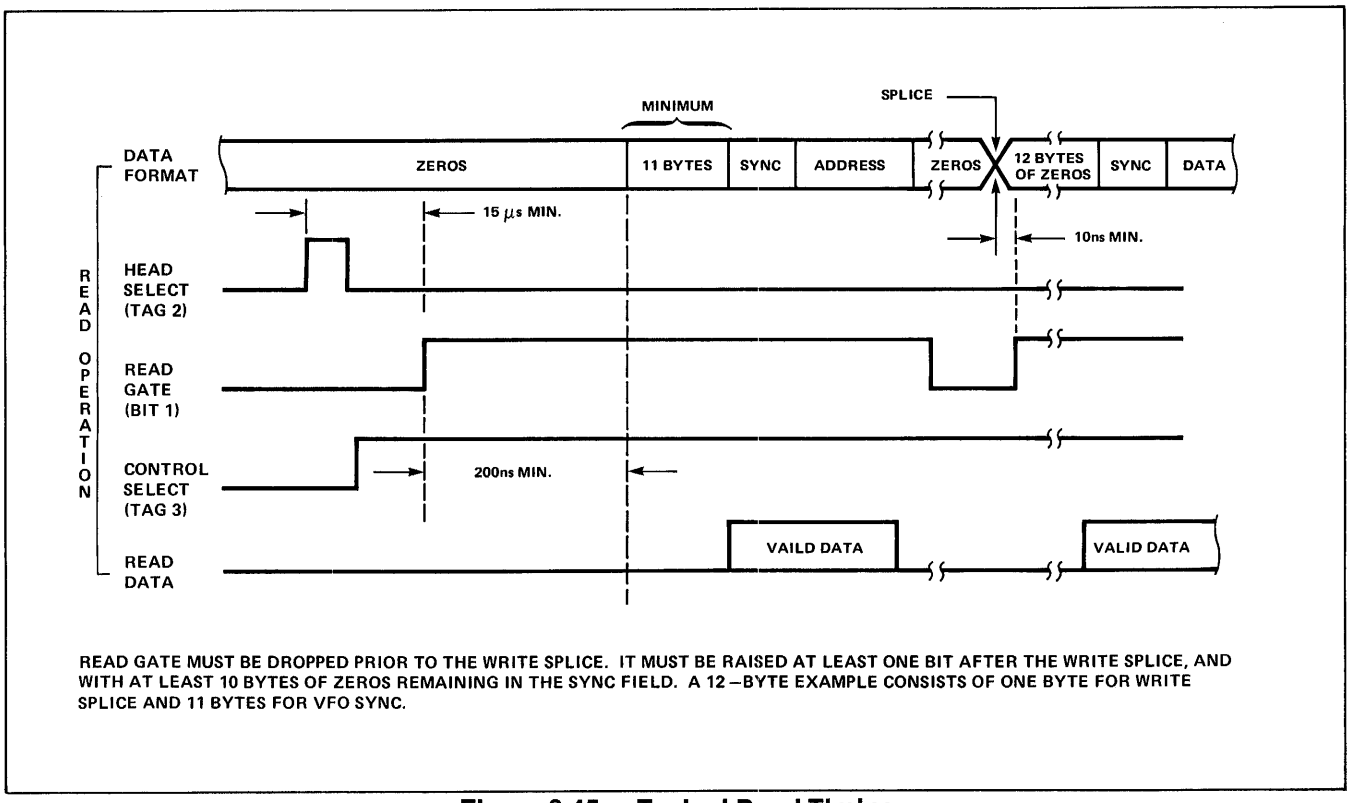


Figure 3-45. Typical Read Timing

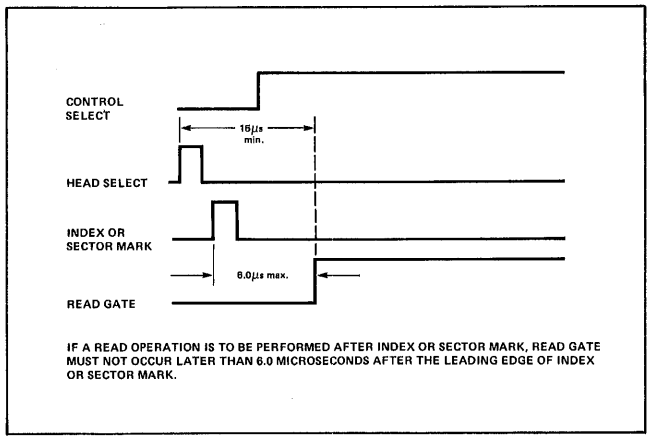


Figure 3-46. Typical Read Control Timing

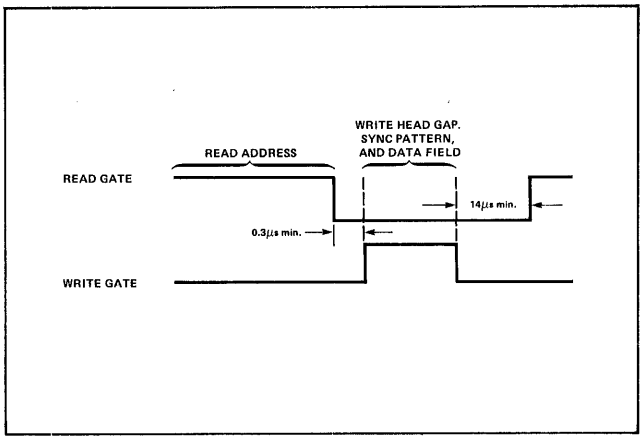


Figure 3-47. Typical Write Control Timing

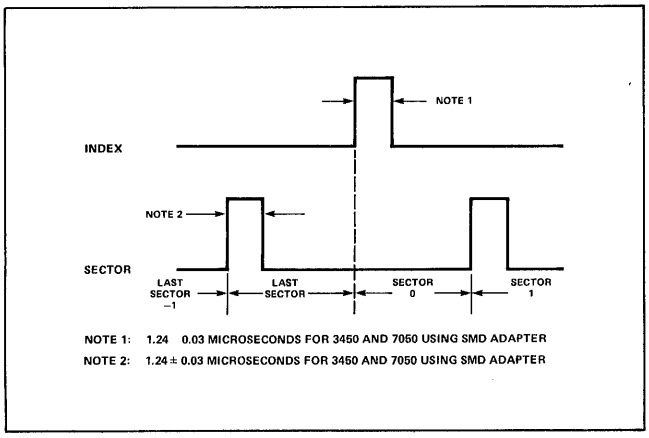


Figure 3-48. Index and Sector Mark

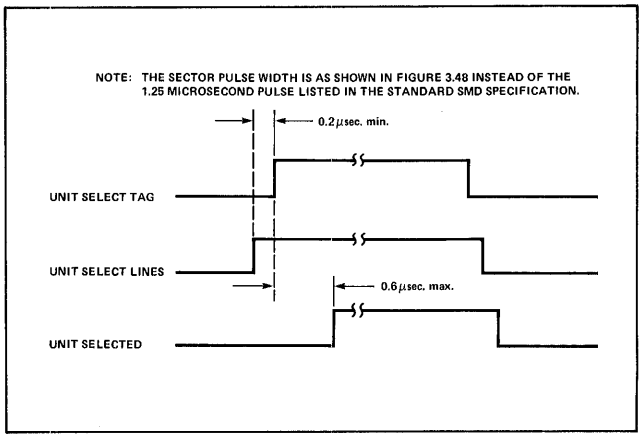


Figure 3-49. Drive Select Timing

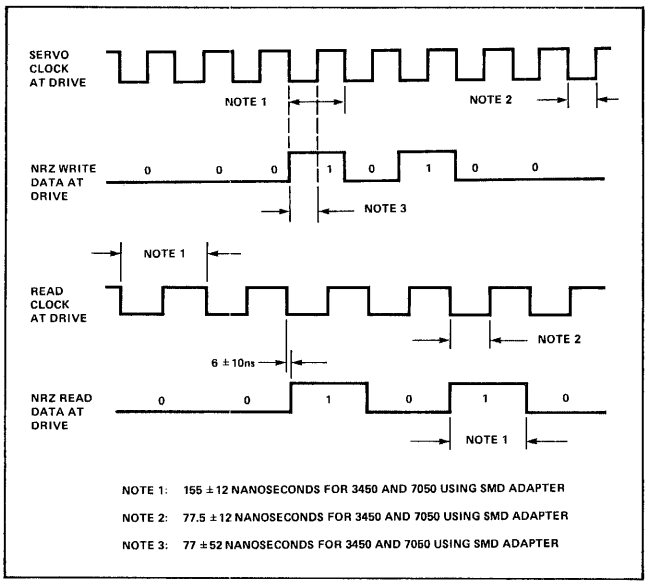


Figure 3-50. NRZ Data and Read Clock Timing

3.20.6 Format Design. Some hardware oriented constraints must be observed when designing a format. The following is a list of the parameters involved:

a. *Read Initialization Time* Between the deselection of one head and the selection of another head, there is a 5-microsecond delay within the drive, due to circuit characteristics. The time from the initiation of a head change until data can be read using the selected head is 24 microseconds maximum (5 microseconds for head selection, 10 microseconds for read amplifier stabilization, and 9 microseconds for phase lock synchronization).

b. *Write-to-Read Recovery Time* Assuming head selection is stabilized, the time before Read Gate can be enabled after switching Write Gate off is 10 microseconds minimum.

c. *Read-to-Write Recovery Time* Assuming head selection is stabilized, the time before Write Gate can be enabled after switching Read Gate off is 1.0 microsecond minimum.

d. *Beginning-of-Record Tolerance* This tolerance (a gap of 9 bytes) allows for write splice and write-to-read recovery time for multisector operations (see Figure 3-51).

e. *Read VFO Synchronization* 8 microseconds are needed for the variable frequency oscillator to synchronize. Zeros should be written during this time.

f. *Sync Pattern* The sync pattern, indicating the beginning of the address or data area, consists of 1 byte.

g. *Write Driver Turn On* The write driver turn on time is about 960 nanoseconds (one byte time). This time must be accounted for, in order to know where the splice areas are located.

3.20.7 Write Format Procedure. Provision must be made to format the disc. A suggested format is shown in Figure 3-51. The following procedure is recommended:

a. Select desired drive, cylinder, head, and sector.

b. The controller must provide a 5 microsecond minimum delay after selecting a head before starting a search for the leading edge of the sector pulse is detected.

c. Search for leading edge of desired sector.

d. Detect leading edge of the desired sector and raise Write Gate.

e. Write all zeros for write recovery and VFO sync field (20 bytes minimum).

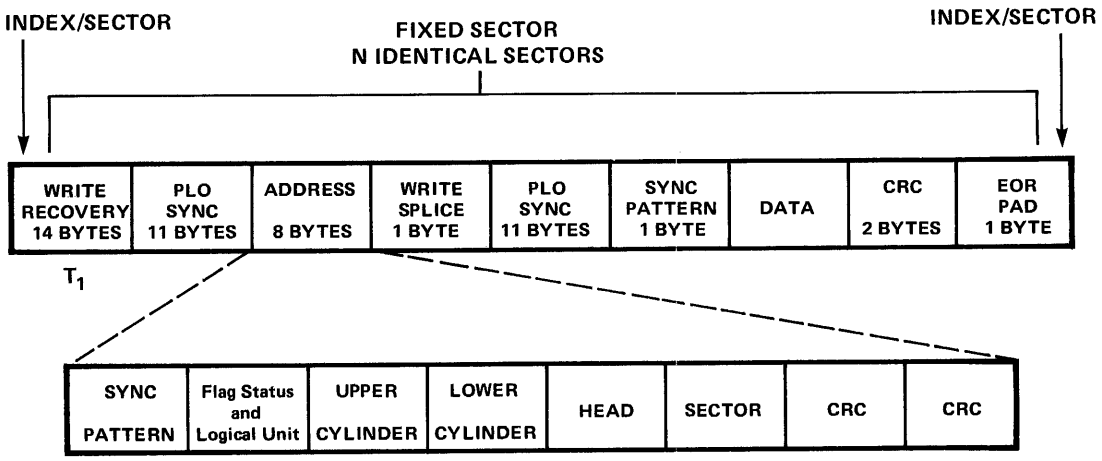
f. Write a sync pattern, the address, and the address checkword.

g. Write all zeros for write splice gap and VFO sync field (12 bytes minimum).

h. Write a sync pattern, the data field, the two-byte data field checkword, and the five-byte field of zeros (see Figure 3-51). The data field should preferably be a worst case pattern.

i. The end tolerance gap specified by the standard SMD specification is not required by this drive. However, if it is used, it is recommended that zeros be written to the next sector pulse.

j. If the next sector of the same track is to be formatted, and the head is not deselected, Write Gate should be left on. In this case, all zeros should be written until the leading edge of the next sector or index pulse.



T_1 = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

EXAMPLE: WHAT IS THE DATA FIELD LENGTH USING 66 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE, GAPS AND ADDRESSES)}$$

$$= \frac{20{,}160^*}{66} - 49 = 256 \text{ BYTES/SECTOR}$$

$$\%\ \text{EFFICIENCY} = \frac{256 \times 66}{20{,}160} \times 100 = 83.8\%$$

* 20,160 BYTES/TRACK ASSUMED.

NOTE: WRITE RECOVERY IS 14 BYTES INSTEAD OF 16 BYTES, AND EOR PAD IS 1 BYTE INSTEAD OF 8 BYTES, AS RECOMMENDED BY THE STANDARD SMD SPECIFICATION.

Figure 3-51. Recommended Sector Format

3.20.8 Control Timing.

a. Read Data Field

Read Gate is the control line associated with a read operation.

The leading edge of Read Gate allows the VFO to synchronize on all-zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines. There may be invalid data transitions on these lines during the synchronization period. Read Gate must be dropped and raised again after going through a splice area. Read Gate may be enabled 60 ± 4 clock periods after the leading edge of index or sector.

The sync pattern search may begin 48 servo clock periods (6 byte times) after the leading edge of Read Gate.

Head switching and read amplifier stabilization requirements (Figure 3-45) determine the latest time at which a head can be selected, in order to read the next successive sector, using the format shown in Figure 3-51.

Read Data and Read Clock may not have valid data until 8 microseconds after the leading edge of Read Gate, due to the VFO synchronizing time.

There should be no splice area while Read Gate is raised.

b. Write Data Field

Write Gate is the control line associated with a write operation.

The sector address must always be read and verified, prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the VFO sync field and sync pattern.

The controller must provide an internal delay of at least two bit times (approximately 240 nanoseconds) between the trailing edge of Read Gate and the leading edge of Write Gate. This delay allows for signal propagation tolerances and prevents overlap of Read Gate and Write Gate in the drive.

Writing the data field must always be followed by writing the data checkword and at least an eight-bit gap of zeros at the end of the checkword.

During formatting, Write Gate is raised upon detecting index or sector. During a record update, Write Gate is raised within two byte times after the last bit of the address.

4. TROUBLESHOOTING

4.0 Introduction. The overall purpose of field service for PRIAM disc drives is to restore system operation by the quickest and most economical means possible. This usually involves the replacement of a faulty or suspected assembly with an operational spare. The assembly in question may then be returned to a PRIAM repair depot for component level diagnosis and repair.

Requests for maintenance assistance may be directed to PRIAM's Customer Service Department. PRIAM offers the following services:

1. Telephone Assistance: Service representatives are available (during PRIAM's normal working hours) to assist customers with maintenance, interfacing, and spare parts inquiries.

2. On-site Assistance: PRIAM can provide a factory trained technician to assist the customer's system technician in the testing and repair of PRIAM products.

3. Factory Repair: PRIAM maintains repair facilities for the convenience of its customers. An entire disc drive, or any repairable assembly, may be returned to PRIAM for repair. Contact PRIAM Customer Service for a return authorization number prior to shipping any drive or assembly to PRIAM.

4.1 Field Adjustments and Preventive Maintenance. PRIAM 8-inch disc drives require no field adjustments and no preventive maintenance.

4.2 General Inspection. The following checklist may be used as a preliminary procedure to be performed whenever a disc drive is suspected of being faulty:

1. Check that the spindle and head carriage lock lever is in the UNLOCK position.

2. Check for proper DC voltages within the disc drive, as described in 3.18.2.

3. Check the fuse in the power supply.

4. Check the fuse in the servo and motor control PCB.

5. Check that the device address, write protect, and sector size switches are correctly set, according to the information given in the INSTALLATION section.

6. Check for component discoloration, and for loose or faulty connections.

7. Check and recheck all cable and controller connectors.

If all of the above items seem to be in order, troubleshooting can be performed simply by replacing each of the major assemblies one-by-one until the problem disappears. This obviously works best on problems that are stable, as opposed to intermittent.

A more symptom-specific approach to troubleshooting is described below in the SYMPTOMS AND CAUSES section.

4.3. Status and Error Codes. The disc drive is capable of providing information concerning its internal conditions by status indications on the user interface. The exact information available, and the signal lines involved depend on the specific interface used.

4.4 Symptoms and Causes. The functions performed by the disc drive fall into the following five categories:

1. Spindle Rotation
2. Command/Status Transfer
3. Head Positioning/Servo
4. Data Write Operations
5. Data Read Operations

In the following pages, symptoms are listed from each of these categories, along with possible causes and the corresponding suggested courses of action.

SPINDLE ROTATION

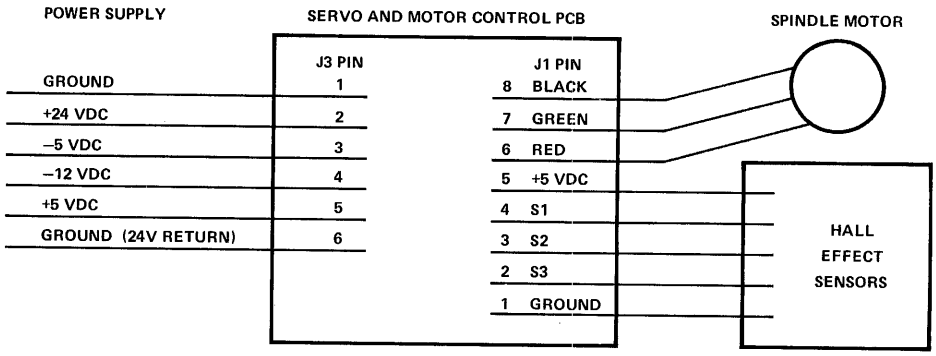
Symptom	Possible Cause	Suggested Action
Rotation does not start.	Spindle locked.	Place in UNLOCK position.
	Incorrect or zero voltage at servo and motor control PCB connector J3.	Check power supply.
	+ OFF signal is + 5 VDC (should be 0 volts for rotation).	Check microprocessor reset signal on R/W digital PCB. Check power-on reset (POR). Check power reset (PRST). All these should be false.
	Defective motor control circuitry.	Check the fuse in the servo and motor control PCB.
	Defective Hall Effect sensors.	Replace entire disc drive.
	Defective spindle motor.	Manually rotate spindle in clockwise (viewed from bottom) direction *only.* If motor is binding, replace entire disc drive. Depot repair is required.
Spindle rotates, but stops after about one minute.	Defective motor control circuitry.	Replace servo and motor control PCB.
	Defective Hall Effect sensors.	Replace entire disc drive.
	Speed control not being sensed by microprocessor.	Replace R/W digital PCB. Replace Servo and Motor Control PCB.
	Spindle motor has excessive drag.	Replace entire disc drive.
Spindle rotates, but drive does not come Ready, or Ready comes and goes.	Fault condition.	Check Fault status.
	Intermittent power supply failure.	Replace power supply.
	Defective R/W digital PCB.	Replace R/W digital PCB.
	Defective motor control circuitry.	Replace servo and motor control PCB.
	Defective head disc assembly.	Replace entire disc drive.

Comments: Upon completion of power on reset (POR) the microprocessor disables the + OFF signal to the spindle motor. With + OFF at 0 volts the spindle motor should rotate at its specified speed (3600 RPM).

The microprocessor examines Index Marks to determine spindle speed. If the specified spindle speed is not reached within two minutes, the + OFF signal is enabled and spindle rotation is stopped.

Power to the disc drive must be cycled (off and then on) to allow the microprocessor to disable the + OFF signal.

The following diagram shows the connections among the power supply, the servo and motor control PCB, the Hall Effect sensors, and the spindle motor.



Power Supply	Servo and Motor Control PCB J3 Pin #	J1 Pin #	
Ground	1	8 Black	Spindle Motor
+24 VDC	2	7 Green	
–5 VDC	3	6 Red	
–12 VDC	4	5 +5 VDC	Hall Effect Sensors
+5 VDC	5	4 S1	
Ground (24V RETURN)	6	3 S2	
		2 S3	
		1 Ground	

COMMAND/STATUS TRANSFER

Symptom	Possible Cause	Suggested Action
Incorrect state on Unit Selected.	Wrong setting on device address switch.	Refer to Section 2.4 for correct switch settings.
	Pick and Hold false or Open Cable Detect true (SMD interface only).	Check controller, cable, and connectors.
	Unit Select Tag or Unit Address missing or mistimed (SMD interface only).	Check controller, cable, and connectors.
Selected drive does not issue status.	Drive not Ready.	See SPINDLE ROTATION (above).
	Fault condition.	See FAULT CONDITIONS section (below).
	Defective R/W digital PCB.	Replace R/W digital PCB.
Selected drive does not accept commands.	Tag and bus data malfunction (SMD interface only).	Check controller, cable, and connectors.
Selected drive issues Fault.	Fault condition.	See FAULT CONDITIONS section (below).
Selected drive issues Seek Error.	Defective servo operation.	See HEAD POSITIONING/SERVO (below).
Selected drive fails to issue Index.	Defective R/W digital PCB or servo and motor control PCB.	Replace R/W digital PCB. Replace servo and motor control PCB.

Comments: During servo and data write operations, most circuit functions are monitored by the microprocessor. If Ready is true and Fault is false, it is likely that the spindle speed, servo, and data write circuitry are all functioning in a normal manner.

HEAD POSITIONING/SERVO

Symptom	Possible Cause	Suggested Action
Drive fails to move to new address.	Command transfer circuitry defect.	See COMMAND/STATUS TRANSFER (above).
Continuous Seek Error condition.	Defective circuitry.	Defective servo circuitry on servo and motor control PCB. If fault persists with operational spare, and the fault is not in the spindle speed circuitry, replace the entire disc drive.
	Faulty connection to servo read head.	Check connector J4.
	Faulty connection to voice coil actuator.	Check connector J5.
	Incorrect power voltage.	Check connector J3. Refer to Section 3 for correct voltages.
Drive seeks to wrong cylinder.	Inadequate signal from controller.	Check controller, cable, and connectors.
	Defective circuitry or servo system.	Defective circuitry on servo and motor control PCB. If the symptom persists with operational spare, and the fault is not in the controller or cable, replace the entire disc drive.

Comments: Note that the seek operation may be functional, while the circuitry that checks for seek errors may be defective.

A large number of symptoms may be associated with malfunctions of the servo circuitry. If servo malfunction is suspected, the recommended procedure is to replace the servo and motor control PCB. If the head disc assembly is defective, it is highly likely that non-servo related faults (e.g., data errors, failure to come Ready, Fault status true) will also be in evidence.

DATA WRITE OPERATIONS

Symptom	Possible Cause	Suggested Action
Fault is set with each attempt to write data.	Incorrect switch setting or circuit defect.	Verify whether multiple heads have been selected. If this is the case, the following signal will be high: Chip 7H pin 2 on R/W PCB Check for the Act Unsafe condition. Act unsafe will be high if there are write transitions with Write Gate false, or no write transitions with Write Gate true. See the section on SEEK ERRORS AND FAULT CONDITIONS for other possibilities and corresponding suggested actions.
Data is written incorrectly and Fault does not set.	Difficulty in data read operation.	See DATA READ OPERATIONS (below).

DATA READ OPERATIONS

Symptom	Possible Cause	Suggested Action
Drive fails to read, but will write without a Fault.	Defect in read circuitry.	Check all cable connections. Replace terminator. Replace R/W digital PCB. Replace I/O cable.
Drive reads data fields and header fields correctly, but will not read newly written data.	Difficulty in data write operation.	See DATA WRITE OPERATIONS (above). If Fault is set during write operation, see the section on SEEK ERRORS AND FAULT CONDITIONS.

Comments: If read errors persist after replacement of the terminator and the R/W digital PCB, and if the cable connections are correct, it is possible that the format being used is erroneous.

If the format is correct, replacement of the entire disc drive is recommended.

4.5 Seek Errors and Fault Conditions. Seek errors result when a head does not lock on the target track. Whenever a seek error occurs, the drive's track counter is reset to zero. This is done automatically by restoring the head to cylinder zero. The fault must be reset, and a new seek command may then be issued.

The Seek Error indication will be set true whenever the microprocessor detects any of the following conditions:

1. Seek Incomplete (track following servo unable to lock onto track within the prescribed time).

2. Restore or Rezero not completed within the prescribed time.

3. Invalid seek address detected (SMD and ANSI interfaces only).

4. Guardband Error (servo head has entered the guardband area).

When the microprocessor detects one of these conditions, it issues an internal Restore or Rezero command, which returns the head to cylinder zero and sets a Seek Error Latch. The Seek Error Latch must be cleared by a Fault Reset, Restore or Rezero command issued to the drive by the user.

The exact manner in which the Seek Error indication appears on the user interface depends on which interface option is present. See the individual interface description sections for details.

Fault status is set, Ready is disabled, and writing of data is inhibited whenever the safety circuitry detects a Fault condition. The following list discusses (for PRIAM and ANSI interfaces) the possible origins of such a condition, and suggests what remedial actions could be taken in each case:

1. Write Gate true with Write Protect switch ON (or Write Enable switch OFF).

   Check switch for correct setting.

2. Act Unsafe (Write gate without Write Current or Write Current without Write Gate).

   If the fault is isolated to an individual data head, return the entire disc drive to a repair depot.

   If the fault occurs on all data heads, replace the read/write digital PCB.

3. Multiple heads selected (only one data head should be selected at a given time).

4. Write Gate and Read Gate both true at the same time.

   Check the controller for proper operation and the interface cable for the proper connections.

   If the problem persists, replace the read/write digital PCB.

5. Write Gate true, but heads not precisely located over the designated cylinder.

   Replace the servo and motor control PCB.

   If the problem persists, replace the entire disc drive.

6. No seek request, but head movement is detected.

   Replace the servo and motor control PCB.

   If the problem persists, replace the entire disc drive.

7. The PLO signal is not synchronized.

   Replace the servo and motor control PCB.

   If the problem persists, replace the entire disc drive.

8. Spindle rotation is outside of specification.

   Check the servo and motor control PCB for a defective component.

   Check the hall effect sensor and motor connector.

   Check the power supply for a defective connection, DC voltage level, or component.

   If the fault cannot be corrected by replacing the servo and motor control PCB and power supply, then replace the entire disc drive.

9. More than one control tag is active (SMD and B4 interfaces only).

   Check controller, cable, and procedures.

   If the problem persists, replace the read/write digital PCB.

If any of conditions 6, 7, or 8 (above) are detected, the microprocessor will attempt a restore to cylinder zero.

Any of the following measures will reset Fault status:

1. Power On Reset — remove and reapply DC power.

2. Fault Clear — Tag 3 and Bit 4 on interface "A" or BUS cable (SMD interface).

3. Fault Reset command (PRIAM and ANSI interfaces).

4. Ground potential at 5J pin 4 on R/W PCB.

Assembly Replacement Procedures

All of the replaceable assemblies in a PRIAM disc drive may be removed and replaced using standard hand tools. It is highly recommended that maintenance personnel use the assembly replacement approach to field service, rather than attempting component level repair.

4.6 Precautions.

1. Always make sure that the head and spindle lock lever is in the LOCK position before the drive is moved in any way.

2. Always make sure that the power is off when removing or reinserting any printed circuit boards or connectors.

3. Use proper size screwdrivers, wrenches, and other tools. Keep track of the screws and other parts you remove, and use the same hardware when reinstalling each assembly.

4. Use properly calibrated test equipment.

5. Keep accurate records of all observations made during servicing.

Before attempting to remove any assemblies, make sure that the head and spindle lock lever is in the LOCK position.

4.7 Head Disc Assembly. The head disc assembly (HDA) is a sealed contamination-resistant enclosure containing all moving parts in the disc drive. It should not be opened for any reason. If the HDA is defective, the entire disc drive should be returned to a qualified repair depot. Do not remove the HDA from the frame assembly.

4.8 Servo and Motor Control PCB. The servo and motor control PCB is mounted on the bottom of the frame. To remove the servo and motor control PCB, first unplug the five connectors. Note that the connector at J2 does not unplug at the servo and motor control PCB. Therefore, unplug the connector at the R/W digital PCB end of the cable. Then remove the four mounting screws which are on the standoff posts.

Extreme care should be taken in removing the IC connectors (J4 and J5), which go to the head disc assembly. Gently pry the connectors off, using a suitable size slender screwdriver. If the connectors to the HDA are broken, it will be necessary to replace the entire disc drive.

4.9 Read/Write Digital PCB. The read/write digital PCB is mounted on the top of the frame. To remove it, first unplug all the connectors, carefully noting their positions and orientations for later replacement. Then remove the six mounting screws.

Extreme care should be taken in removing the IC connector (J2), which goes to the head disc assembly. Gently pry the connector off, using a suitable size slender screwdriver. If the connectors to the HDA are broken, it will be necessary to replace the entire disc drive.

4.10 Power Supply. The power supply must be mounted separately from the disc drive. To remove the power supply, simply unplug the power connector (J3) from the servo and motor control PCB.

Spare Parts List

Replaceable assembly part numbers are given below. Additional part number information (and/or a bill of material listing for customers establishing depot repair) is available from PRIAM Customer Service.

Description	P/N
Head Disc Assembly (3450, 7050)	330503
Servo and Motor Control PCB (3450, 7050)	200228
Read/Write Digital PCB (PRIAM Interface) (3450)	200233-01
Read/Write Digital PCB (PRIAM Interface) (7050)	200233-02
SMD Interface Adapter	200178
ANSI Interface Adapter	200198
Power Supply (3450, 7050)	340541
Power Cord AC (for 8″ Power Supply)	101116
DC Power Cable (3 feet)	340539
Daisy Chain T-connector	101101
Cable SMD "A" 6′	330278
Cable SMD "A" 15′	330259
Cable SMD "A" 25′	330260
Cable SMD "B" 6′	330179
Cable SMD "B" 15′	330262
Cable SMD "B" 25′	330263
Drive Cable PRIAM 50 Pin 6′	300287
Drive Cable PRIAM 50 pin 15′	300288
Drive Cable PRIAM 50 pin 25′	300289
Terminator (PRIAM Interface)	200153
Terminator (SMD Interface Adapter)	200128

Orders for spare parts may be placed with your PRIAM Sales Representative or with PRIAM Customer Service at the factory.

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