(ANSI 1226)

BSR X3.101

DEVICE LEVEL INTERFACE

PRELIMINARY

JUNE 1983

ABSTRACT:

Strict mechanical, electrical, and functional specifications are defined for attaching disk drive(s) to their host(s). This interface will facilitate the interconnection of disk drive(s) to the host(s) and thus provide a common interface specification for both.

FOREWORD

This interface was developed to specify a common interface definition and specify connector pin assignments and functional protocols. Physical characteristics of the disk, recording methods and formats for interchange are beyond the scope of this standard.

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1.0 Scope

This standard applies to fixed disk drive(s) and defines the necessary functional and electrical requirements (including logic signals) and the mechanical requirements of the interface for connection of conforming fixed disk drive(s) to host system(s). This standard is distinct from a specification in that it delineates a minimum set of requirements consistent with compatibility and interchangeability at the interface level.

This standard will facilitate the interconnection of rigid disk drive(s) to host system(s) by a user that has available the technical capabilities to verify and test performance up through the functional level. The user should have the capability to specify the overall system hardware and software that will be unique for a particular device and host combination.

This standard by itself does not guarantee plug compatibility of devices meeting this standard. To obtain total interchangeability of devices an operational specification must be defined. Neither the operating specification nor the power requirements are defined by this standard.

This standard does not prescribe the magnetic encoding or decoding method, the recording techniques, nor the format used to write or read data but allows the reporting of all of the above. Unique characteristics offered by a vendor are allowed.

The design of this interface provides the following features:

1. Addressability of up to 8 devices.

2. Transfer data across the interface via a close loop clocked NRZ format

3. Daisy chain configuration utilizing a 50 wire flat ribbon cable.

4. Supports a radial attention and selection capability throught the daisy chain bus.

5. Permits self configuration of the system and self definition of the individual devices.

6. Extensive error reporting and status information is provided.

1.1 Definitions

1.1.1 State Nomenclature

The nomenclature used to define voltage levels and signal states on the interface and used to define logical states internally to the device and their correlation is defined in Table 1-1.

TABLE 1-1

State Nomenclature

Interface			Internal		
Voltage Level		Signal State	Logical State		Logical Transition
Single Ended	Differential		Tables	Text	
"LOW"	+ line > - line	Active	1	one	SET = X to one
"HIGH"	+ line > + line	Inactive	0	zero	RESET = X to zero

2.0 Physical Characteristics

Unless otherwise indicated, all values are specified with a plus or minus five percent tolerance.

2.1 Cabling Configuration

The device shall be connected to a host by means of a 50 conductor flat ribbon or equivalent cable. Five meters (5 m) shall be the maximum length of the interface cable. Note that the cumulative length of the cable in a daisy chain string shall not exceed five meters. See Figure 2-1.

Delivery of primary power (AC and/or DC) shall not be accomplished on the interface cable. A separate DC common (ground) may be provided. Specifications for power supply cabling and grounding requirements are not a subject of this standard. Refer to vendor specifications for power/ground information.

2.2 Connector Specification

The connector type shall be the 50 pin two row, inline flat ribbon rectangular connector illustrated in Figure 2-2 and 2-3 with dimensions specified in Table 2-1 and 2-2.

Pin assignments and signal nomenclature are illustrated in Table 2-3. Termination of the individual cable lines shall be at the host and at the last device according to the electrical requirements of Section 2.4.

The cable plug (Figure 2-2) shall be polarized and polarization shall be done with a center top tab.

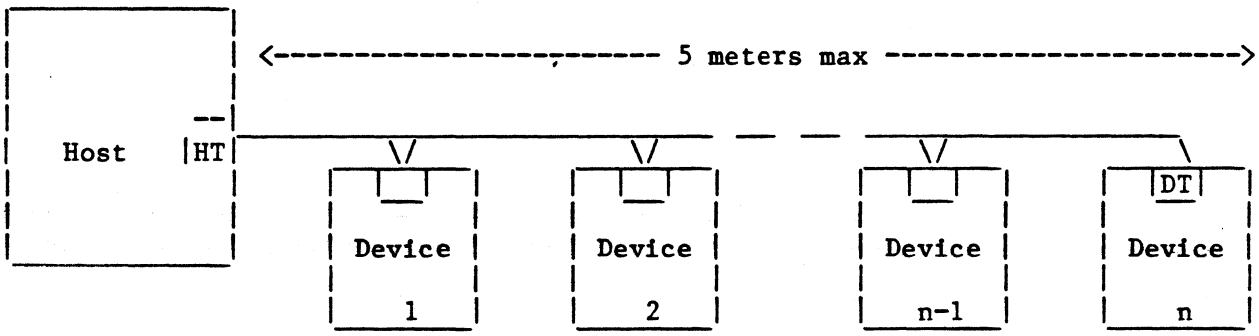
2.3 Cable Characteristics

The flat ribbon or equivalent cable shall consist of 50 conductors of 28 AWG. The characteristic impedance of the lines shall be 100 ohms plus or minus 10%. Conductor spacing shall be 1.27 millimeters (0.050 inch) center to center to provide for mechanical termination. Additionally, the flat ribbon cable shall be marked in such a way as to identify line number one (pin 1).

If the cable contains a shield ground it shall be connected to pin number one of the interface connector.

Figure 2-1

Interface Configuration



HT = Terminator installed at the Host.
DT = Terminator installed at the last Device.

Table 2-1

Dimensions of Interface Cable Plug (see Figure 2-2

	Millimeters	Inches
C1	2.54	0.100
C2	60.96	2.4
C3	2.54	0.100
C4	8.357	0.329
C5	3.3025	0.130
C6	68.072	2.680
C7	6.096	0.240
C8	8.153	0.321
C9	13.487	0.531
C10	3.81	0.150
C11	1.27	0.050
C12	6.096	0.240
C13	32.385	1.275
C14	3.302	0.130
C15	7.493	0.295
C16	2.667	0.105
C17	1.625	0.064

NOTE 1: 50 Contacts on 1.27 mm (0.050 in)
staggered spacing = 62.23 mm (2.450 in)

NOTE 2: Tolerances +/- 0.127 mm (.005 in) noncumulative

Table 2-2

Dimensions of Interface Cable Receptacle (see Figure 2-3

	Millimeters	Inches
D1	2.54	0.100
D2	82.80	3.260
D3	2.54	0.100
D4	4.83	0.190
D5	8.51	0.335
D6	72.64	2.860
D7	78.74	3.100
D8	13.94	0.549
D9	4.19	0.165
D10	6.09	0.240
D11	6.60	0.260

NOTE 1: 50 Contact on 2.54 mm (0.100 in)
spacing = 60.96 mm (2.40 in)

NOTE 2: Tolerances +/- 0.127 mm (.005 in) noncumulative

Figure 2-2

Interface Cable Plug

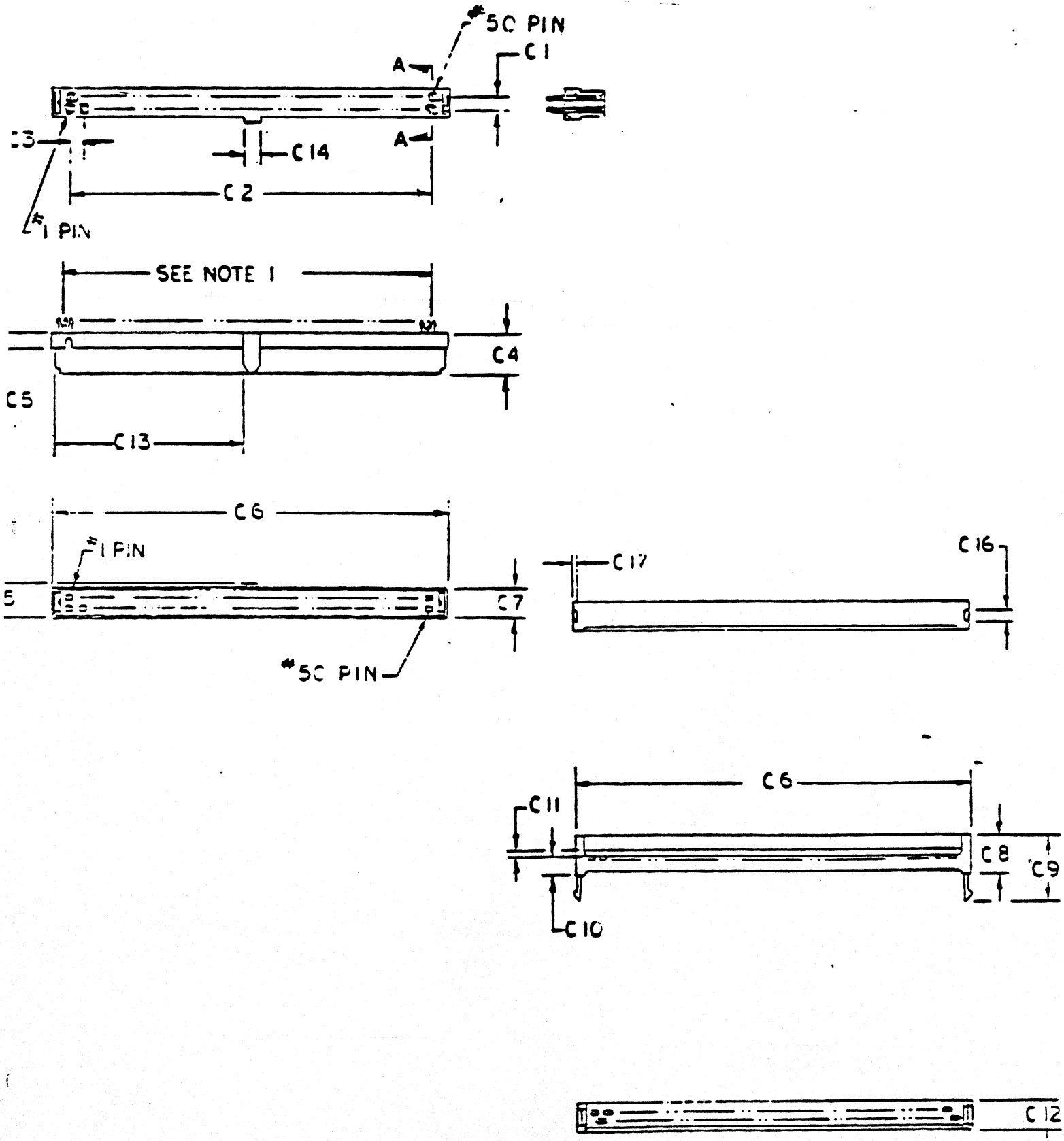
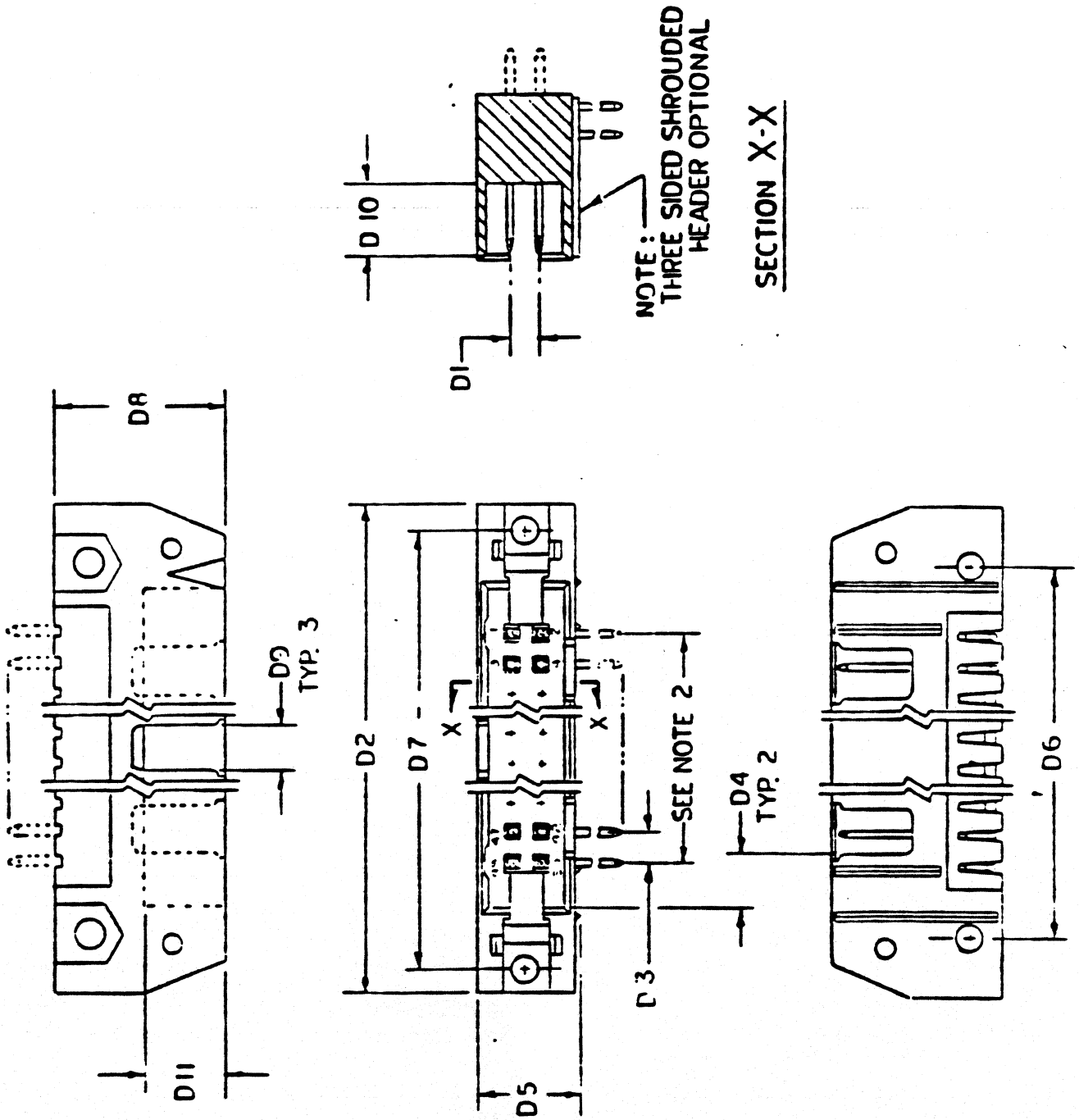


Figure 2-3

Interface Cable Receptacle



2.4 Electrical Characteristics

2.4.1 Bidirectional Control Bus Lines

The bidirectional Control Bus is used in two different modes:

Daisy Chain Mode and Radial Mode.

In the Daisy Chain Mode eight bits of information and an optional parity bit shall be tranferred between the host and the selected device.

In Radial Mode each of the eight Control Bus lines shall be used separately for communication with one specific device. In this way, one bit of information is transferred to or from all devices simultaneously. Each device shall have provisions (jumper, switches, etc) to connect the radial line to any one of the eight Control Bus lines. The configuration of the bidirectional Control Bus lines is shown in Figure 2-4.

2.4.1.1 Control Bus Drivers

The bus drivers for the parallel information shall be either three-state or open collector. The driver for the radial signal in the device shall be open collector.

All bus driver outputs for "LOW" level shall sink 24 milliamps minimum. The "LOW" level output voltage shall be 0.5 volt maximum. Driver outputs for "HIGH" level shall have a "HIGH" level output voltage of 2.4 volts minimum, 5.25 volts maximum. A 10 milliamps source current is provided by the 470 ohms terminator discussed in Section 2.4.1.3.

The leakage current in the high impedance state ("OFF" state for open collector drivers) shall not exceed 0.25 milliamp for either "HIGH" or "LOW" level on the Control Bus.

The total number of drivers connected to any Control Bus line shall not exceed ten (one in the host, one in each of the eight devices for the parallel lines, and one in a single device for the radial line).

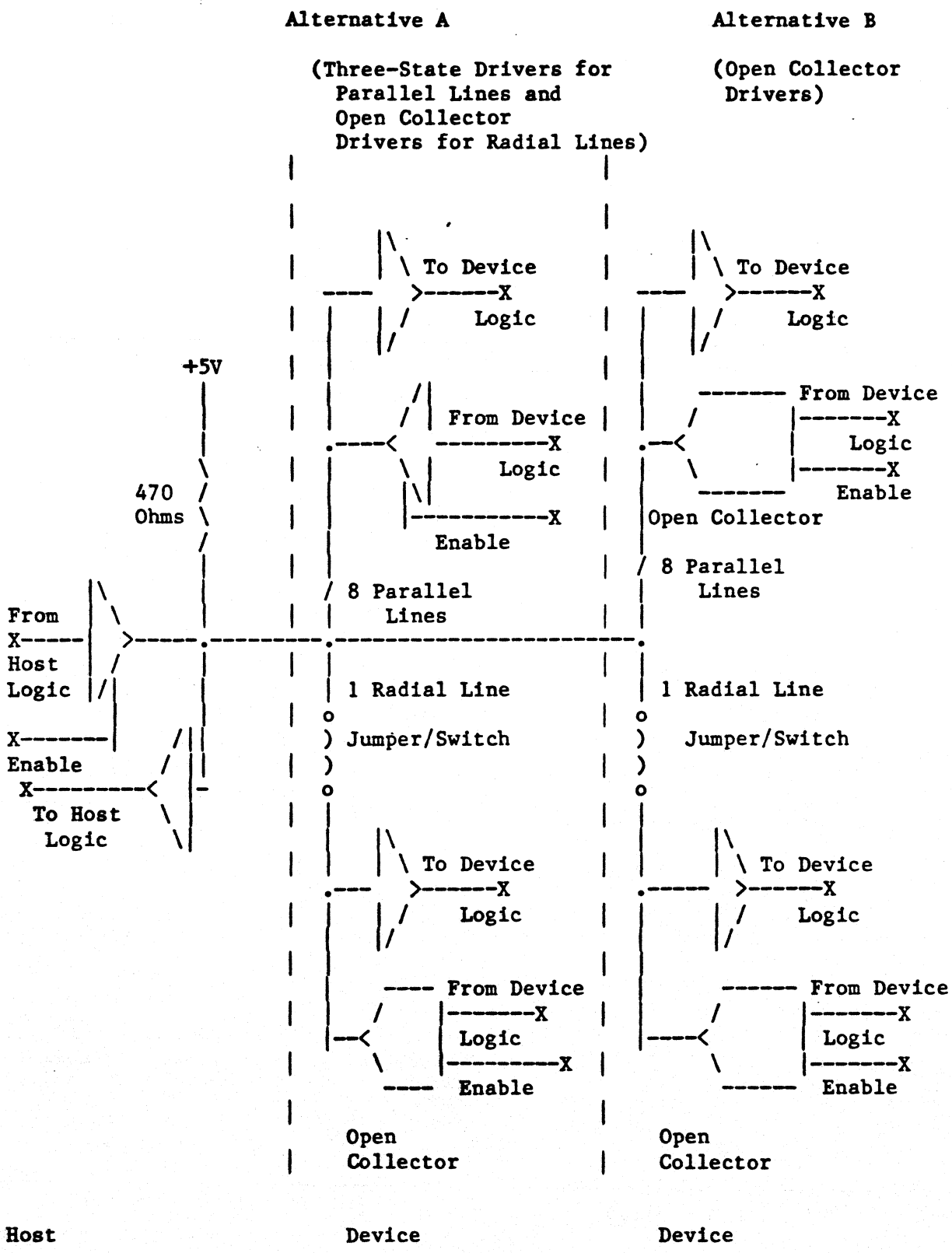
2.4.1.2 Control Bus Receivers

The maximum "LOW" level input current shall be -400 microamps. The maximum "HIGH" level input current shall be 80 microamps. The maximum "LOW" level input voltage shall be 0.9 volt. The minimum "HIGH" level input voltage shall be 2.0 volts.

The total number of receivers connected to any Control Bus line shall not exceed ten (one in the host, one in each of the eight devices for the parallel lines, and one in each device for the radial selection mode).

Figure 2-4

Cable Configuration for Bidirectional Control Bus Signals



2.4.1.3 Control Bus Termination

A 470 ohms resistor, plus or minus 10% shall be installed at the host end of all Control Bus lines (Control Bus Bits 0-7) connected to +5 volts, plus or minus 5%. See Figure 2-4.

2.4.2 Single Ended Lines

The cable configuration of the single ended lines shall be as shown in Figures 2-5 to 2-7.

2.4.2.1 Single Ended Line Drivers

The drivers shall have open collector outputs capable of sinking 40 milliamps at "LOW" levels. "LOW" level output voltage shall not exceed 0.4 volt. The high level leakage current shall not exceed 250 microamps.

2.4.2.2 Single Ended Line Receivers

The receivers shall accept TTL logic levels. For noise immunity the receivers shall have an input hysteresis of 0.4 volt minimum, with a postitive going threshold voltage between 1.4 and 2.0 volts and a negative going threshold voltage between 0.5 and 1.1 volts. "LOW" level input current shall be -1.2 milliamps or less. The "HIGH" level input current shall be 40 microamps maximum.

2.4.2.3 Single Ended Line Termination

All single ended lines originating at the host shall be terminated at the last device with 330 ohms, plus or minus 5%, to ground and 220 ohms, plus or minus 5%, to +5 volts. All single ended lines originating at the devices shall be terminated in the same way at the host.

2.4.2.4 Port Enable Termination

A 10 kilohms plus or minus 10% pullup resistor to +5 volts shall be added to the Port Enable line in each device to generate an inactive signal state whenever the device is not connected (see Figure 2-6).

Figure 2-5

Cable Configuration for Unidirectional Single Ended Lines From Host (Except Port Enable)

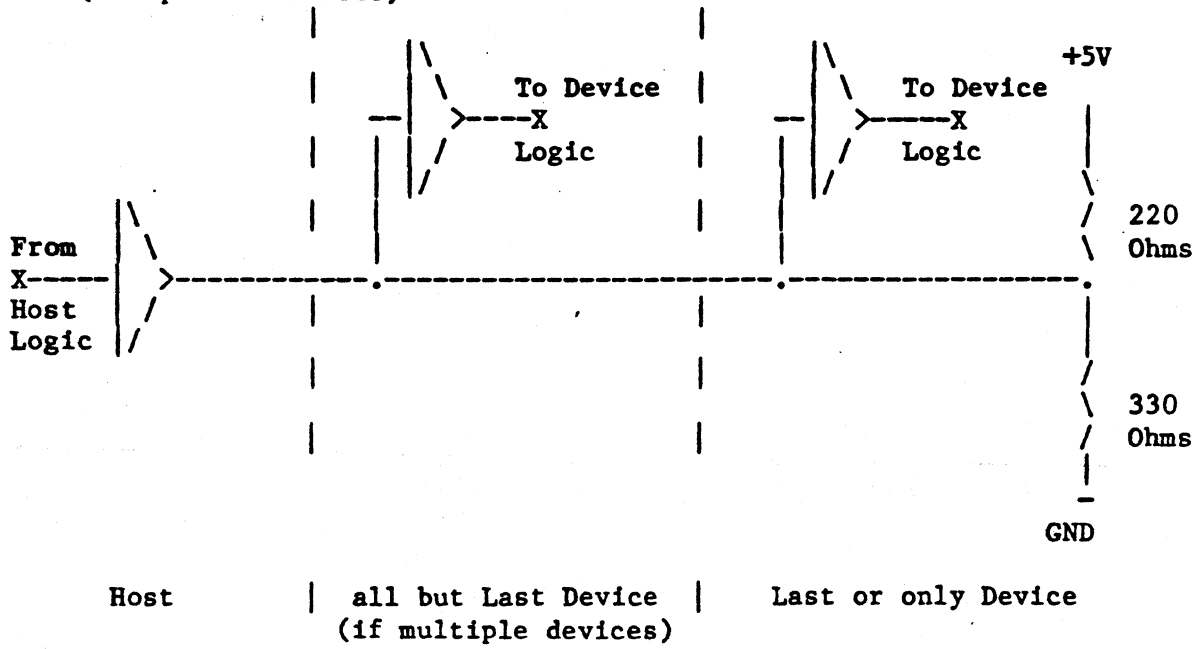


Figure 2-6

Cable Configuration for Port Enable

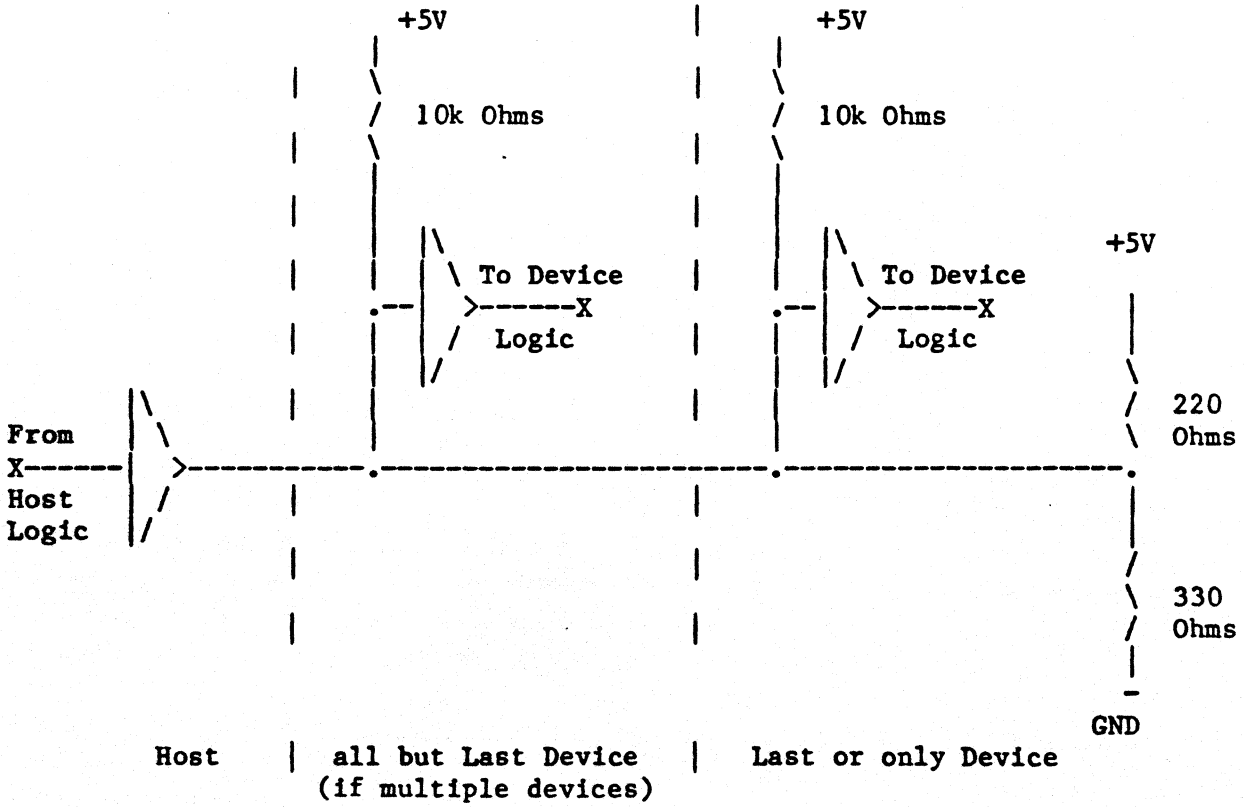
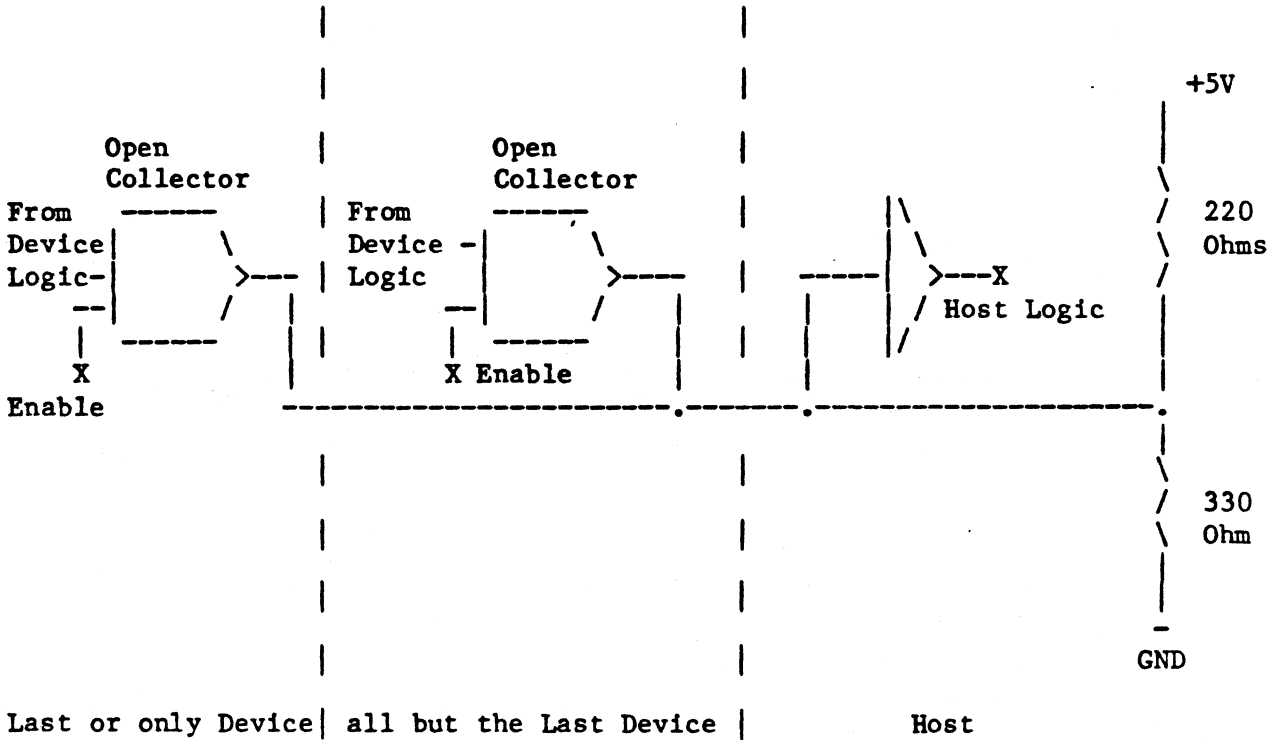


Figure 2-7

Cable Configuration for Unidirectional Single Ended Lines From Devices



2.4.3 Differential Lines

The differential lines drivers and receivers shall operate from a single +5 volts supply. They shall operate at 9.67 MHz and shall be capable of meeting the timing requirements of Sections 5.3 and 5.4 while operating the recommended terminated cable configuration.

The cable configuration of the differential lines shall be as shown in Figures 2-8 and 2-9.

An active signal state is defined as the "+" line being equal or more postitive than the "-" line. An inactive signal state is defined as the "-" line being more positive the the "+" line.

2.4.3.1 Differential Line Drivers

The differential line drivers shall have a three-state output and be capable of sinking or sourcing a minimum of 20 milliamps in the active state. In the inactive or high impedance state, leakage current shall not exceed plus or minus 20 microamps. RS422 compatible line drivers.

2.4.3.2 Differential Line Receivers

The common mod input range capability of the receivers shall be at least +7 to -7 volt. The differential input voltage shall be -0.2 volt minimum and +0.2 volts maximum. RS422 compatible line receivers.

2.4.3.3 Differential Line Termination

Each line of all pairs of differential lines shall be terminated with 100 ohms, plus or minus 10%, to ground both at the host and the last device.

Figure 2-8

Cable Configuration for Differential Lines from Host

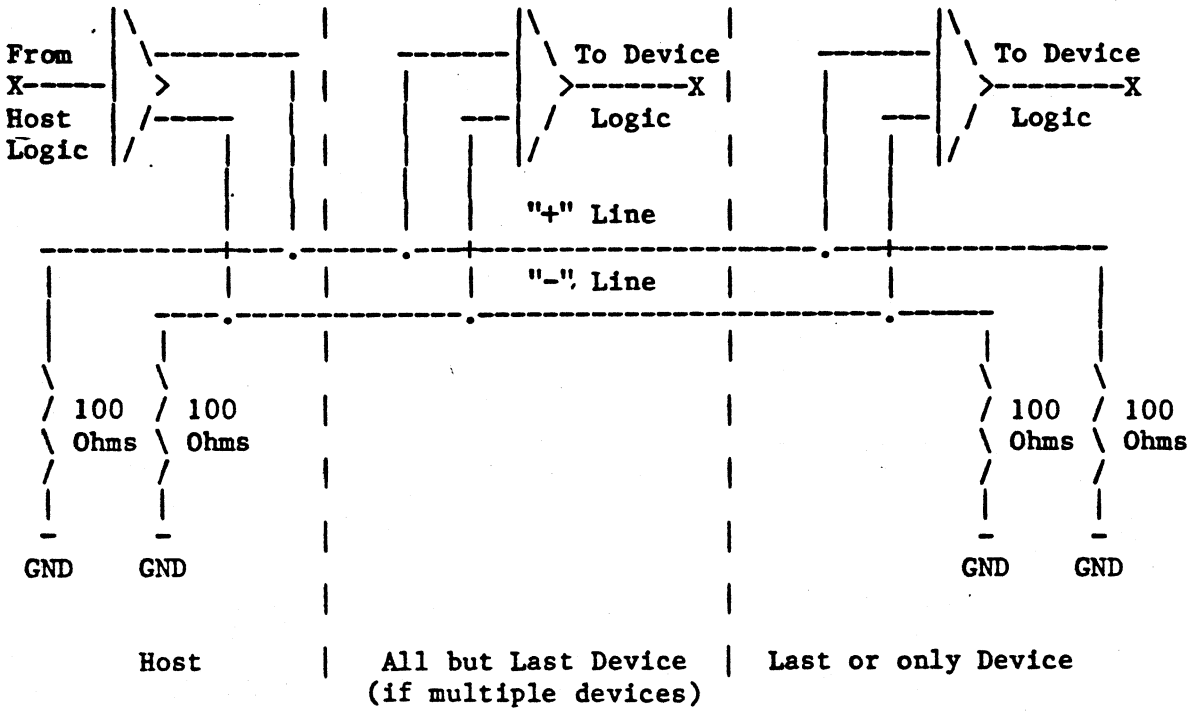


Figure 2-9

Cable Configuration for Differential Lines from Device

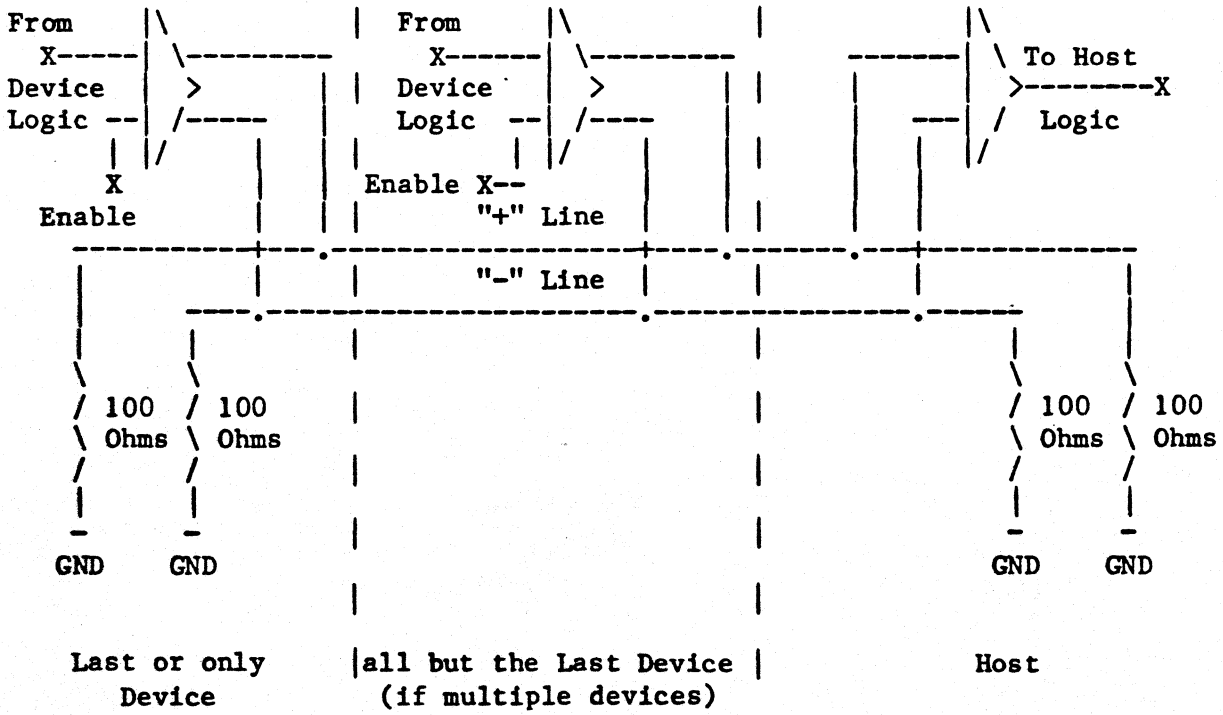


Table 2-3

Pin Assignment

Signal Pin	Ground Pin	Signal Name	Signal Source
1		Ground	---
		Control Bus	
2	10	Bit 0, Select/Attn. Device 0	Host/Device
3	10	Bit 1, Select/Attn. Device 1	Host/Device
4	10	Bit 2, Select/Attn. Device 2	Host/Device
5	10	Bit 3, Select/Attn. Device 3	Host/Device
6	10	Bit 4, Select/Attn. Device 4	Host/Device
7	10	Bit 5, Select/Attn. Device 5	Host/Device
8	10	Bit 6, Select/Attn. Device 6	Host/Device
9	10	Bit 7, Select/Attn. Device 7	Host/Device
11	12	Reserved	---
13	14	Select Out/Attn. In Strobe	Host
15	16	Command Request	Host
17	18	Parameter Request	Host
19	20	Bus Direction Out	Host
21	22	Port Enable	Host
23	24	Reserved	---
25	26	Read Gate	Host
27	28	Write Gate	Host
29	30	Bus Acknowledge	Device
31	32	Index	Device
33	34	Sector Mark	Device
35	36	Attention	Device
37	38	Busy	Device
39	38	Read Data +	Device
40	38	Read Data -	Device
42	41	Read/Reference Clock +	Device
43	41	Read/Reference Clock -	Device
45	44	Write Clock +	Host
46	44	Write Clock -	Host
48	47	Write Data +	Host
49	47	Write Data -	Host
	50	Ground	---

3.0 Signal Definitions

This section provides signal definitions and their intended operation and/or status. Relative signal timing and tolerance is defined in Section 5.

Note: The timing diagrams of Section 5 shall take precedence over all other timing definitions.

3.1 Control Bus

The Control Bus shall be used for bidirectional transfer of information. The direction of transfer shall be determined by the Bus Direction Out signal.

The electrical characteristics of the Control Bus signals are defined in Section 2.4.1 The Control Bus Lines shall be "LOW" for an active signal state and shall be "HIGH" for an inactive signal state.

Throughout the specification of this interface the host shall be in control of the Control Bus. All communications between the host and the selected device shall be determined by the host.

The Control Bus is used in two modes. When Select Out/Attention In Strobe is active, the Control Bus shall be in Radial Mode. When the Command Request, Paramenter Request, or Bus Acknowledge is active, the Control Bus shall be in Daisy Chain Mode.

3.1.1 Radial Mode

Each device shall be assigned a unit number 0-7, by radially attaching the one Select/Attention device (0-7) line as per Table 2-3.

3.1.1.1 Select Out Mode

When both Bus Direction Out and Select Out/Attention In Strobe are active each radial line shall transfer the selection information to the corresponding device.

3.1.1.2 Attention In Mode

When Bus Direction Out is inactive and Select Out/Attention In Strobe is active, each device shall gate its internal Attention Condition onto its corresponding Control Bus line.

3.1.2 Daisy Chain Mode

When in the Daisy Chain Mode, all Control Bus transfers shall consist of a two byte sequence. The transfer is asynchronous and controlled with a handshake protocol. The first byte is transferred using a handshake between the Command Request Signal and the Bus Acknowledge signal. The second byte is transferred using a handshake between the Parameter Request Signal and the Bus Acknowledge Signal. Refer to Section 4 for the command definitions.

3.1.2.1 Command Out

When both the Bus Direction Out and Command Request are active the host shall transfer a Command Byte to the selected device.

When bit 6 in the Command Code (first byte) is one, the second byte shall be Parameter Out (see Section 3.1.2.2 and Table 4-1).

When bit 6 in the Command Code (first byte) is zero, the second byte shall be Parameter In (see Section 3.1.2.3 and Table 4-2).

When the state of the Bus Direction Out Signal for the transfer of the parameter (second byte) does not comply with the definition of bit 6 of the Command Code, this condition shall set the Attention Condition and the Control Bus Error Bit in the General Status Byte (see Section 4.4.1.2).

The condition of the Bus Direction Out Signal being inactive and the Command Request Signal being active is a violation of protocol and may optionally set the Attention Condition and the Control Bus Error Bit in the General Status Byte (see Section 4.4.1.2).

3.1.2.2 Parameter Out

When both Bus Direction Out and Parameter Request are active, the host shall transfer a Parameter Byte to the selected device (see Table 4-1).

3.1.2.3 Parameter In

When the Bus Direction Out Signal is inactive and the Parameter Request signal is active, the host is requesting a Parameter Byte (status) to be transferred from the selected device (see Table 4-2).

3.1.3 Control Bus Bits 0-7, Select/Attention Device 0-7

The eight Control Bus signals, 0-7, shall be used for communication between the host and the device as defined in Sections 3.1.1 and 3.1.2. Control Bus Bit 0 shall be the least significant bit.

3.2 Control Interface

This group of signals are unidirectional in nature. The electrical characteristics of the control interface lines is defined in Section 2.4.2. All control interface Lines shall be "LOW" for an active signal state and shall be "HIGH" for an inactive signal state.

3.2.1 Port Enable

This signal is normally held active by the host. When this signal is active all devices attached to the interface shall respond to the interface protocol as described by this specification.

This signal may be used to disable all devices when host power is lost and/or as a programmed reset. If the interface cable is being disconnected from a device, the device shall be reset by the active to inactive transition on this line.

When this signal changes from active to inactive all devices shall be deselected within 20 milliseconds maximum except for the write circuitry in each device which shall be disabled within 1 microsecond maximum. The device shall remain deselected while Port Enable is inactive.

Upon detecting Port Enable going inactive each device must go to its Initial State as defined below (also see the vendor specification). After Port Enable changes from inactive to active and after the initial state is reached the device shall set the Attention Condition.

Initial State — This is the state a device shall reach within 90 seconds maximum after being powered up, Port Enable has become active or a Selective Reset Command has been received.

The conditions are:

1. The device shall be deselected.

2. The device shall respond to the Select Out/Attention In Strobe Signal.

3. All parameters of commands with Parameters Out in Table 4-1 shall be reset to zero (except Spin Control - see Section 4.1.8).

4. The Device Attribute Table shall be set to its initial value (see Section 4.3).

5. All resettable error conditions shall be reset. If the cause of the error still exists, it shall set the error conditions again.

6. The Initial State bit in Sense Byte 2 shall be set.

3.2.2 Bus Direction Out

The Bus Direction Out Signal is transferred from the host to all attached devices. Bus Direction Out controls the direction of transfer on the Control Bus. When the Bus Direction Out Signal is active, this defines a transfer from the host to the device.

3.2.3 Select Out/Attention In Strobe

This signal is transferred from the host to all attached devices. It has two different functions depending on the state of the Bus Direction Out Signal.

When the Bus Direction Out Signal is active, the signal is Select Out Strobe.

When the Bus Direction Out Signal is inactive, the signal is Attention In Strobe.

3.2.3.1 Select Out Strobe

Only one device shall be selected at any one time. When the Bus Direction Out Signal is active, the active going edge of the Select Out Strobe Signal is used for selecting/deselecting the device.

When any Control Bus Signal is active and Select Out Strobe transitions to active, the device connected to that specific Control Bus line shall become selected.

When any Control Bus Signal is inactive and Select Out Strobe transitions to active, the device connected to that specific Control Bus line shall become deselected.

When all Control Bus Signals are inactive and the Select Out Strobe transitions to active, all attached devices shall become deselected.

3.2.3.2 Attention In Strobe

When the Bus Direction Out Signal is inactive, the Attention In Strobe shall be used to gate the device's internal Attention Condition (see 3.2.8) onto the corresponding Control Bus line connected to that device.

3.2.4 Command Request

This signal initiates the handshake control from the host to the selected device. The active state of this signal signifies the transfer of the first byte of each two-byte transfer. Until the receipt of Bus Acknowldge, the Command Request Signal shall remain active.

3.2.5 Parameter Request

This signal is also a handshake control line from the host to the selected device. The active state of this signal for a Parameter Out Command indicates that the output Parameter Byte is valid on the Control Bus. The active state of this signal for a Parameter In Command requests the selected device to place the Parameter Byte on the Control Bus. Until the receipt of Bus Acknowledge, the Parameter Request Signal shall remain active.

3.2.6 Bus Acknowledge

This signal is returned from the selected device to the host. The Bus Acknowledge Signal has two functions.

When the Control Bus is used in Radial Mode (Select Out/Attention In Strobe active), the selected device shall make the Bus Acknowledge Signal active to acknowledge its selection.

When the Control Bus is used in Daisy Chain Mode, the Bus Acknowledge Signal performs the asynchronous handshake with the Command Request Signal or the Parameter Request Signal.

3.2.7 Busy

The Busy Signal shall change to the active state before the active going edge of the Bus Acknowledge of a Time Dependent Command (see Section 4.0) that causes the device to become busy. The busy Condition will occur during power up sequencing, seeking, or execution of diagnostics.

The busy to not busy transition within the device shall set the Attention Condition within the device (see Section 3.2.8).

If Command Request becomes active when the Busy signal is already active the device will not respond with Bus Acknowledge before the function is completed and Busy is made inactive.

Note: The Busy Interface signal is different from the Busy Executing status bit (see Section 4.4.1.7).

3.2.8 Attention

This signal is a party line signal ("wired OR") from all devices to the host, independent of the selection of a device.

The Attention Signal shall be made active by a device, if the device's internal Attention Condition is set to one, and if Attention is enabled (see Attention Control Command Section 4.1.1). The Attention Condition shall be set if the device requires service from the host. The detailed conditions to set the Attention Condition are defined in Section 4.

The Attention Condition of the selected device shall only be reset by the Clear Attention Command or the Clear Fault Command. Issuing the Clear Fault Command shall reset only those error status bits and the resulting Attention Condition if the error condition can be reset. A Clear Attention Command shall reset the Attention Condition independent of error conditions.

3.2.9 Index

Index is a signal that indicates to the host that a reference point or index area is passing under the heads of the selected device. One Index Pulse shall be generated by the selected device per revolution of the recording media.

Whenever the device is ready, a valid Index Signal shall be transferred from the selected device to the host.

3.2.10 Sector Mark

The Sector Signal establishes rotational reference points on the recording surface. Each track may be divided into sectors with the initial sector ("Zero") starting coincident with the Index Pulse. All subsequent sectors start coincident with the active going edge of a Sector Pulse. When the Index Pulse is activated, the Sector Pulse is omitted.

Whenever the device is ready, a valid Sector Mark Signal shall be transferred from the selected device to the host.

In the event that the sector signal is not an even division of this track capacity, the last sector shall be elongated to include the remainder. Short sectors are not allowed.

3.2.11 Read Gate

The Read Gate Signal is transferred from the host to the selected device.

The Read Gate Signal enables and synchronizes the read circuitry to transfer the serialized data information on the Read Data lines from the recording medium.

3.2.12 Write Gate

The Write Gate Signal is transferred from the host to the selected device.

The Write Gate Signal enables the write circuitry in the device to transfer the serialized information on the Write Data lines to the recording medium. Note, a write operation shall not take place unless a write enable condition has been established by a previous Write Control Command.

3.3 Read/Write Signals

This section describes the signals used when transferring data to and from the host. These signals are only valid if a device is selected. All of these signals are driven differentially (see Section 2.4.3). All data sent to the device or host shall be Non-Return-to-Zero (NRZ).

3.3.1 Read Data

When Read Gate is active, the Read Data lines transfer the serial NRZ read data from the selected device to the host. This data is synchronized with Read Clock. The Read Data signal shall be static when Read Gate is not active.

3.3.2 Read/Reference Clock

The Read/Reference Clock is transferred from the selected device to the host. This signal shall transfer Read Clock when Read Gate is active. Read Clock shall be synchronous with the serial NRZ read data. This signal shall transfer the Reference Clock at all other times. The transitions between Read Clock and Reference Clock shall be glitch free.

3.3.3 Write Data

When Write Gate is active, the Write Data lines shall transfer the serial NRZ write data from the host to selected device for recording. The serial write data shall be synchronized to the Write Clock. This signal shall be held static at all times except when Write Gate is active.

3.3.4 Write Clock

Write Clock shall be used by the selected device to properly phase the Write Data lines while recording. Write Clock shall be generated in the host by returning the Reference Clock Signal back to the selected device at the same frequency with an unspecified but constant shift in phase. This signal shall be held static at all times except when used to precede the active going edge of Write Gate by at least one bit cell but not more than 16 bit cells and when Write Gate is active.

4.0 Command Structure

All command, status, and parameter information passed between the selected device and the host shall be transferred via the Control Bus and shall conform to the command protocol defined in this standard.

The command protocol requires that each command sequence consists of a two byte transfer. The first byte, the Command Byte, shall always be transferred from the host to the selected device. The second byte, the Parameter Byte, may be transferred from the host to the selected device or from the selected device to the host. The direction of the transfer of the Parameter Byte is determined by the state of the Bus Direction Out signal.

The Command Byte therefore, indicates the particular function that the selected device is to perform. This may include functions such as accepting parametric information from the host, performing requested head motion, or reporting specific status conditions. The Command Byte also conditions the device as to the direction of the transfer of the Parameter Byte portion of the command sequence.

The Parameter Byte completes the command sequence by providing the parameter or status information demanded by the Command Byte. In cases where the Command Byte is sufficient to indicate the complete nature of the command, the General Status Byte is transferred as Parameter Byte to complete the command sequence.

Below all defined command sequences are specified. They are divided into two groups: one which requires the Parameter Byte transferred go the device (Parameter Out) and one which requires the Parameter Byte transferred to the host (Parameter In).

There are two kinds of commands:

Immediate Commands and Time Dependent Commands.

For Immediate Commands the active going edge of the second Bus Ackowledge shall not be generated until the required action has been performed. In the case that action is not performed, Attention Condition shall be set prior to the active going edge of the Bus Acknowledge Signal that is returned as a response to Parameter Request.

For Time Dependent Commands the Attention Condition shall be set when the action for the Time Dependent Command is completed. The resetting of the Attention Condition by the Immediate Command, Clear Fault or Clear Attention, completes the Time Dependent Command.

All commands, once in progress, shall proceed to completion utlizing parameters established prior to the issuance of the command.

A new Time Dependent Command may be issued only after the current Time Dependent Command has completed, and the Busy Executing bit of the General Status Byte has been cleared.

While all commands are defined individually, there are logical groupings of commands that represent functional operations. For example, the loading of parameter information (cylinder address) and the execution of a particular operation (seek). Unusual command sequences within such groupings may result in violations of an implied protocol and will cause responses which are implementation dependent and will vary among vendors.

It should be noted that in some implementations such violations may cause a loss of data or functional error with or without an error indication. The user is urged to consult vendors's specifications to determine what results, if any, are defined for such command sequences.

Table 4-1 Commands With Parameters Out

Function	Command Code	Parameter Out
Attention Control	40 Hex	Bit 7 0 = Enable Attention 1 = Disable Attention
Write Control	41 Hex	Bit 7 1 = Write Enable 0 = Write Disable
Set Upper Cyl. Address	42 Hex	MSB of Cylinder Address
Set Lower Cyl. Address	43 Hex	LSB of Cylinder Address
Select Moving Head	44 Hex	Head Number
Load Attribute Number	50 Hex	Address Byte
Load Device Attribute	51 Hex	Information Byte
Spin Control *	55 Hex	Bit 7 1 = Spin Up 0 = Spin Down
Load Sec. Pulses Per Track High	59 Hex	MSB of Sector Pulses Per Track
Load Sec. Pulses Per Track Medium	5A Hex	MedSB of Sector Pulses Per Track
Load Sec. Pulses Per Track Low	5B Hex	LSB of Sector Pulses Per Track
Load Test Byte	6F Hex	Test Byte

All unused bits in parameters shall be zero.

The commands with a "*" appended are Time Dependent Commands that generate an Attention Condition upon completion.

Table 4-2

Commands With Parameters In

Function	Command Code	Parameter In
Report "Illegal Cmd."	00 Hex	General Status
Clear Fault	01 Hex	General Status
Clear Attention	02 Hex	General Status
Seek *	03 Hex	General Status
Rezero *	04 Hex	General Status
Report Sense Byte 2**	0D Hex	Sense Byte 2
Report Sense Byte 1**	0E Hex	Sense Byte 1
Report General Status**	0F Hex	General Status
Report Device Attribute	10 Hex	Device Attribute Byte
Set Attention *	11 Hex	General Status
Selective Reset *	14 Hex	General Status
Partition Track *	16 Hex	General Status
Report Cyl. High	29 Hex	MSB of Cylinder Address
Report Cyl. Low	2A Hex	LSB of Cylinder Address
Report Test Byte	2F Hex	Echo Byte

The commands with "*" appended are Time Dependent Commands that set an Attention Condition upon completion.

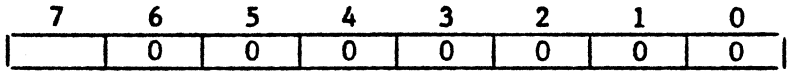
** Events reported in these status and sense bytes can set an Attention Condition even without a preceding command.

4.1 Commands With Parameter Out

All commands defined in this section require a Parameter Byte to be transferred to the device. These commands are summarized in Table 4.1.

4.1.1 Attention Control (Command Code 40 Hex)

This command shall condition the selected device to enable or disable its attention circuitry based on the value of the Parameter Byte as shown below.



0 = Enable Attention
1 = Disable Attention

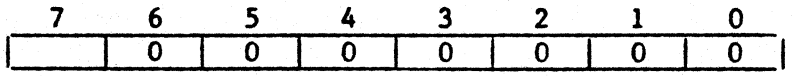
This command allows the host to selectively ignore attention requests from certain devices on the interface. This might be done in response to a device that generates spurious attention requests due to a malfuntion.

The Enable Attention Command shall cause the selected device to gate its internal Attention Condition onto the party line ("wired OR") Attention Signal. The Disable Attention Command shall cause the selected device to disable the gating of the internal Attention Condition onto the party line Attention Signal. This command shall have no impact on the function of the radial status returned with the Attention In Strobe Signal (see Signal 3.2.3.2).

Devices shall be initilized with the Attention circuitry enabled.

4.1.2 Write Control (Command Code 41 Hex)

This command shall condition the selected device to enable or disable its write circuitry based on the value of the parameter Byte as shown below:



1 = Write Enable
0 = Write Disable

This command is used in conjunction with the Write Gate Signal and therefore merely enables the write circuitry while the Write Gate Signal activates the circuitry at the proper time. An active Write Gate Signal while the device's write circuitry is disabled shall result in no data being recorded.

Devices shall be initialized with the write circuitry disabled.

A Write Control Command execute during a write operation is a violation of protocol.

4.1.3 Set Upper Cylinder Address (Command Code 42 Hex)

This command shall condition the selected device to accept the Parameter Byte as the most significant Byte of a cylinder address.

This command is used in conjunction with the Seek Command (see Section 4.2.4) and therefore is a means of supplying the most significant byte of a target cylinder address.

This command shall not cause any head motion. Loading a cylinder address outside the range of a device shall not cause an error unless a subsequent Seek Command is issued to that illegal cylinder.

Devices shall be initialized with the target cylinder address equal to zero.

4.1.4 Set Lower Cylinder Address (Command Code 43 Hex)

This command shall condition the selected device to accept the Parameter Byte as the least signficant byte of a cylinder address.

This command is used in conjunction with the Seek Command (see Section 4.2.4) and therefore is a means of supplying the least significant byte of a target cylinder address.

This command shall not cause any head motion. Loading a cylinder address outside the range of a device shall not cause an error unless a subsequent seek command is issued to that illegal cylinder.

Devices shall be initialized with the target cylinder address equal to zero.

4.1.5 Select Moving Head (Command 44 Hex)

This command shall condition the selected device to accept the Parameter Byte as the binary address of the head selected for read or write operations. This command shall enable the moving heads and shall disable the fixed heads.

A Select Moving Head Command issued during a read or write operation is a violation of protocol.

The device shall set the Attention Condition and the Illegal Parameter Bit in the General Status Byte upon receipt of a head address outside the head address range of the device.

Devices shall be initialized with moving head zero selected.

4.1.6 Load Attribute Number (Command Code 50 Hex)

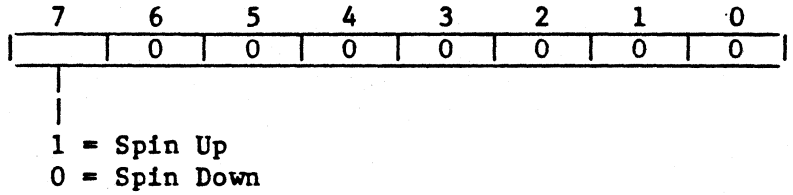
This command shall condition the selected device to accept the Parameter Byte as the number of a Device Attribute as defined in Table 4-3. This command prepares the device for a subsequent Load Device Attribute Command or Report Device Attribute Command (see Sections 4.1.7 and 4.2.9). This command may be issued at any time.

4.1.7 Load Device Attribute (Command Code 51 Hex)

This command shall condition the selected device to accept the Parameter Byte as the new value of a Device Attribute. The number of the Device Attribute must have been previously defined by the Load Attribute Number Command (see Section 4.1.6).

4.1.8 Spin Control (Command Code 55 Hex)

This command shall condition the seleted device to enter a spin up or spin down cycle based on the value of the Parameter Byte as shown below.



A spin up cycle shall consist of starting the rotation of the spindle. A spin down cycle shall consist of stopping the rotation of the spindle.

Upon completion of a spin control cycle the device shall set the Attention Condition. Issuing a spin up command to a device whose spindle is already at full speed or issuing a spin down command to a device whose spindle has already stopped shall also set the Attention Condition.

The Spin Control Command is a Time Dependent Command and as such shall set the Busy Executing bit in the General Status Byte (see Section 4.4.1.7) while command execution is in process. Also, the device shall exercise appropriate control over the Busy signal at the interface (see Section 3.2.7).

A spin down cycle shall cause the repositioning of the moving head(s) over the landing zone and stop the rotation of the spindle. If the device detects that it cannot successfully seek to the landing zone it shall set the Attention Condition and set bit 0 of Sense Byte 1.

See vendor specification for initial state of the Spin Control.

4.1.9 Load Sector Pulses Per Track High (Command Code 59 Hex)

This command shall condition the selected device to accept the Parameter Byte as the most significant byte of a 24 bit number that represents the total number that will control the number of sector pulses between (but excluding) Index Pulses generated by hard sectored devices when a Partition Track Command (see Section 4.2.12) is executed.

This command is used in conjunction with the Partition Track Command and is a means of supplying the most significant byte of the Sector Pulses Per Track value.

Prior to completion of the execution of the Partition Track Command, the contents of this byte will be set into the Sector Pulses Per Track High Attribute (16 Hex). See Table 4-3 and section 4.3.14.

This command functions in conjunction with the Load Sectors Per Track Medium and Low Commands (see Sections 4.1.10 and 4.1.11) and operates in the same way.

4.1.10 Load Sector Pulses Per Track Medium (Command Code 5A Hex)

This command shall condition the selected device to accept the Parameter Byte as the medium significant byte of a 24 bit number that represents the total number that will control the number of sector pulses between (but excluding) Index Pulses generated by hard sectored devices when a Partition Track Command (see Section 4.2.12) is executed.

This command is used in conjuntion with the Partition Track Command and is a means of supplying the medium significant byte of the Sector Pulses Per Track value.

Upon completion of the execution of the Partition Track Command the contents of this byte will be set into the Sector Pulses Per Track Medium Attribute (17 Hex). See Table 4-3 and section 4.3.15.

This command functions in conjunction with the Load Sectors Per Track High and Low Commands (see Sections 4.1.9 and 4.1.11) and operates in the same way.

4.1.11 Load Sector Pulses Per Track Low (Command Code 5B Hex)

This command shall condition the selected device to accept the Parameter Byte as the least significant byte of a 24 bit number that represents the total number that will control the number of sector pulses between (but excluding) Index Pulses generated by hard sectored devices when a Partition Track Command (see Section 4.2.12) is executed.

This command is used in conjunction with the Partition Track Command and is a means of supplying the least significant byte of the Sector Pulses Per Track value.

Upon completion of the execution of the Partition Track Command the contents of this byte will be set into the Sector Pulses Per Track Low Attribute (18 Hex). See Table 4-3 and section 4.3.16.

This command functions in conjunction with the Load Sectors Per Track High and medium Commands (see Sections 4.1.9 and 4.1.10) and operates in the same way.

4.1.12 Load Test Byte (Command Code 6F Hex)

This command shall condition the selected device to accept the Parameter Byte as a specific test byte that shall be returned to the host as part of the Report Test Byte Command (see Section 4.2.15).

This command pair allows the host to test the integrity of data transfer over the Control Bus.

4.2 Commands with Parameter In

The commands defined in this section require a Parameter Byte to be transferred to the host. These commands are summarized in Table 4.2.

4.2.1 Report "Illegal Command" (Command Code 00 Hex)

This command shall force the Illegal Command Bit to be set in the General Status Byte (see Section 4.4). The General Status Byte, with the Illegal Command Bit equal to one, is returned to the host by the Parameter Byte of the command sequence.

4.2.2 Clear Fault (Command Code 01 Hex)

This command shall cause all fault status bits of the selected device to be reset, provided the fault condition has passed. If the fault condition persits the appropriate status bit shall continue to be equal to one. The General Status Byte, cleared of previous fault status, shall be returned by the Parameter Byte of the command sequence.

The Clear Fault Command shall also reset the Attention Condition caused by the fault condition, again only if the fault condition no longer exists.

4.2.3 Clear Attention (Command Code 02 Hex)

This command shall cause the Attention Condition to be reset in the selected device. The General Status Byte shall be returned by the Parameter Byte of the command sequence.

If the error or other condition that caused the Attention Condition persists, the Attention Condition shall not be set again. If, however, the condition is reset and the error reoccurs, the Attention Condition shall be set again.

4.2.4 Seek (Command Code 03 Hex)

This command shall cause the selected device to seek to the cylinder identified as the target cylinder by the Load Cylinder Address Commands (see Sections 4.1.3 and 4.1.4). The General Status Byte shall be returned to the host by the Parameter Byte of the command sequence with the Busy Executing bit set (see Section 4.4.1.7).

The Seek Command shall set the Attention Condition and the Illegal Parameter Bit in the General Status Byte if the target cylinder address is outside the cylinder address range of the device.

Upon completion of any seek (including a zero length seek) the device shall clear the Busy Executing bit in the General Status Byte and set the Attention Condition.

4.2.5 Rezero (Command Code 04 Hex)

This command shall cause the selected device to position the moving head(s) over cylinder zero. The General Status byte shall be returned to the host by the Parameter Byte of the command sequence with the Busy Executing bit set (see Section 4.4.1.7).

Upon the completion of the positioning of the moving head(s) over cylinder zero the device shall clear the Busy Executing bit in the General Status byte and set the Attention Condition.

4.2.6 Report Sense Byte 2 (Command Code 0D Hex)

The command shall cause the selected device to return Sense Byte 2 by the Parameter Byte of the command sequence. No other action shall be taken in the device.

4.2.7 Report Sense Byte 1 (Command Code 0E Hex)

This command shall cause the selected device to return Sense Byte 1 by the Parameter Byte of the command sequence. No other action shall be taken in the device.

4.2.8 Report General Status Byte (Command Code 0F Hex)

This command shall cause the selected device to return the general Status Byte by the Parameter Byte of the command sequence. This command shall not perform any other function in the device and acts as a "no-op" in order to allow the host to monitor the device's General Status Byte without changing any device condition.

4.2.9 Report Device Attribute (Command Code 10 Hex)

This command shall cause the selected device to return a byte of information that is the Device Attribute whose number was defined in the Load Attribute Number Command (see Section 4.1.6). The contents of the byte is defined by Table 4-3 and Section 4.3.

4.2.10 Set Attention (Command Code 11 Hex)

This command shall cause the selected device to set the Attention Condition. No other action shall be caused.

The General Status Byte shall be transferred to the host by the Parameter Byte of the command sequence.

4.2.11 Selective Reset (Command Code 14 Hex)

This command shall cause the selected device to reach Initial State (see Section 3.2.1). This is a time dependent command and as such shall set the Busy Executing bit prior to the assertion of the acknowledge to parameter request and shall be reflected in the returned General Status Byte. Upon completion of the parameter byte transfer the device shall go to the initial state and all resetable parameter, attentions, errors, etc., shall be reset. When the initial state is reached bit 0 of Sense Byte 2 will be set and bit 6 of the General Status Byte shall be cleared. (This causes the setting of the Attention Condition).

4.2.12 Partition Track (Command Code 16 Hex)

This command shall cause the selected device to reconfigure the arrangement of Sector Pulse generation according to parameters received via the Load Sector Pulses Per Track Commands (see Sections 4.1.9 to 4.1.11). The General Status Byte shall be returned to the host by the Parameter Byte of the command sequence.

The Partition Track Command is a Time Dependent Command and as such shall set the Busy Executing bit in the General Status Byte returned by this command (see Section 4.4.1.7) and it is to remain set while this command execution is in process. Also, the device shall exercise appropriate control over the Busy signal at the interface (see Section 3.2.7).

Upon the completion of execution of this command the Bytes Per Sector and the Sector Per Track will be updated in the Attribute Table and also bit 6 of Attribute byte OE Hex will be cleared and this shall set the Attention Condition.

The Partition Track Command shall set the Attention Condition and the Illegal Parameter Bit in the General Status Byte if the Sector Pulses Per Track create a set that is outside the range of the device.

Issuing this command while Read Gate or Write Gate is active or activating Read Gate or Write Gate while this command is executing is a violation of protocol.

4.2.13 Report Cylinder High (Command Code 29 Hex)

This command shall cause the selected device to return a byte of information that is the most significant byte of a 16 bit number that indicates the cylinder address of the current position of the moving heads. This number shall not reflect the most recent cylinder address set by the Set Cylinder Address Commands (see Sections 4.1.3 and 4.1.4), unless there has been an intervening Seek Command completed (see Section 4.2.4).

If executed during a seek operation, the information returned shall be ascertained by the vendor specification.

The information shall be transferred by the Parameter Byte of the command sequence.

4.2.14 Report Cylinder Low (Command Code 2A Hex)

This command shall cause the selected device to return a byte of information that is the least significant byte of a 16 bit number that indicates the cylinder address of the current position of the moving heads. This number shall not reflect the most recent cylinder address set by the Set Cylinder Address Commands (see Sections 4.1.3 and 4.1.4) unless there has been an intervening Seek Command completed (see Section 4.2.4).

If executed during a seek operation, the information returned shall be ascertained by the vendor specification.

The information shall be transferred by the Parameter Byte of the command sequence.

4.2.15 Report Test Byte (Command Code 2F Hex)

This command shall cause the selected device to return a copy of the Test Byte transferred to the device via the Load Test Byte Command. (See Section 4.1.12.)

The Test Byte shall be transferred by the Parameter Byte of the command sequence.

Table 4-3 Device Attribute

Attribute	Number	Parameter
User ID	00 Hex	User defined
Model ID High	01 Hex	Vendor defined
Model ID Low	02 Hex	Vendor defined
Revision ID	03 Hex	Vendor defined
Device Type ID	0D Hex	Device dependent
Table Modification	0E Hex	Action dependent
Table ID *	0F Hex	Vendor defined
Bytes Per Track High	10 Hex	MSB of # of Bytes
Bytes Per Track Med.	11 Hex	MedSB of # of Bytes
Bytes Per Track Low	12 Hex	LSB of # of Bytes
Bytes Per sector High	13 Hex	MSB of # of Bytes
Bytes Per sector Med.	14 Hex	MedSB of # of Bytes
Bytes Per sector Low	15 Hex	LSB of # of Bytes
Sec Pulses Per Track High	16 Hex	MSB of # of Sec Pulses
Sec Pulses Per Track Med.	17 Hex	MedSB of # Sec Pulses
Sec Pulses Per Track Low	18 Hex	LSB of # of Sec Pulses
Sectoring Method	19 Hex	Sectoring Method
Number of Cylinder High	20 Hex	MSB of # of Cylinders
Number of Cylinder Low	21 Hex	LSB of # of Cylinders
Number of Moving Heads	22 Hex	Number of Heads
Encoding Method #1	30 Hex	Encoding Method
Preamble #1 Length	31 Hex	# of Bytes
Preamble #1 Pattern	32 Hex	Preamble Pattern
Sync #1 Pattern	33 Hex	Sync Pattern
Postamble #1 Length	34 Hex	# of Bytes
Postamble #1 Pattern	35 Hex	Postamble Pattern
Gap #1 Length	36 Hex	# of Bytes
Gap #1 Pattern	37 Hex	Gap Pattern
Encoding Method #2	40 Hex	Encoding Method
Preamble #2 Length	41 Hex	# of Bytes
Preable #2 Pattern	42 Hex	Preamble Pattern
Sync #2 Pattern	43 Hex	Sync Pattern
Postamble #2 Length	44 Hex	# of Bytes
Postamble #2 Pattern	45 Hex	Postamble Pattern
Gap #2 Length	46 Hex	# of Bytes
Gap #2 Pattern	47 Hex	Gap Pattern

All unused bits in parameters shall be zero.

*** See Section 4.3.7 for validity of this byte.**

4.3 Device Attribute Commands

These optional commands allow the host to manage the device's mass memory configuration. The host can interrogate each device on the daisy chain bus to determine each device's attributes. The host may then modify the attributes of the devices to optimize parameters of the subsystem. Device type, model IDs, etc. are also provided.

The Device Attribute Commands are: Load Attribute Number, Load Device Attribute, and Report Device Attribute. They are used to load and/or report device attributes but they do not cause any operation that effects the characteristics of the device. All Device Attribute Commands are optional.

The Parameter Byte transferred with the Load Attribute Number Command is used as a number to select a device attribute. This number remains valid for all subsequent Load Device Attribute Commands and Report Device Attribute Commands until changed by another Load Attribute Number Command. If for a received number no attribute is assigned or the function is not implemented in the particular device, the Attention Condition and the Illegal Command Bit in the General Status Byte shall be set.

The Load Device Attribute Command shall set the selected attribute to the value transferred with the Parameter Byte. If the selected attribute can be read only and not be altered, the Attention Condition and the Illegal Command Bit in the General Status Byte shall be set. If an illegal value is loaded the Attention Condition and the Illegal Parameter Bit in the General Status Byte shall be set.

The Report Device Attribute Command shall cause the selected device to return the current value of the selected attribute. The Report Device Attribute Command shall work for all implemented attributes.

4.3.1 User ID (Number 00 Hex)

This attribute is a user settable and readable byte that can be used by the user for any purpose. It is intended to be used to identify the characterisics of the device the host is communicating with.

4.3.2 Model ID High (Number 01 Hex)

This attribute is a read only byte that the device vendor may set to any value for any purpose. It is intended to be used to identify a particular device model.

4.3.3 Model ID Low (Number 02 Hex)

This attribute is a read only byte that the device vendor may set to any value for any purpose. It is intended to be used to identify a particular device model.

4.3.4 Revision ID (Number 03 Hex)

This attribute is a read only byte that the device vendor may set to any value for any purpose. It is intended to be used to identify the revision level of a particular device.

4.3.5 Device Type ID (Number 0D Hex)

This attribute is a read ony byte that identifies the device as defined below:

00 Hex = Not used
01 Hex = Non-removable disk
02 Hex = Removable disk
03 Hex = Combination removable and non-removable disk
04-FF Hex = Reserved for future standardization

4.3.6 Attribute Table Modification (Number 0E Hex)

The pupose of this attribute is to permit an orderly modification of the Attribute Table (see Table 4-3).

When the device goes to Initial State, bit 7 of this attribute is set. After or during the Initial State generation the device initializes the Attribute Table. When the table is initialized by the device bit 7 is reset and bit 6 is set. A host may at its option modify any byte and if it does the device must reset bit 6. After all bytes have been modified the host sets bit 5.

When any subsequent byte, except number Hex 0E, is modified, bits 5 and 6 are reset and bit 4 is set. After a host has modified the byte(s) it must execute a Load Device Attribute Command with number Hex 0E selected. This shall reset bit 4 and set bit 5.

When either bit 6 or bit 5 is equal to one, the table is safe to use. As long as bit 6 remains set the table contains the initial values set by the device.

This attribute is defined as follows:

7	6	5	4	3	2	1	0
				0	0	0	0

Bit 7 = One : The Attribute Table is being modified by the device. This bit is set by the device and is reset by the device upon completion of the modification process.

Bit 6 = One : The initial device attribute values have not been modified. This bit is set by the device upon attaining the Initial State and is reset when any Load Device Attribute Command (except to number Hex 0E) is executed or the Partition Track Command is executed.

Bit 5 = One : This bit, which is set by a host, is used to signify that the Attribute Table is complete and ready for use. This bit is reset on any Load Device Attribute Command except to number OE Hex. This bit can be set only by executing a Load Device Attribute Command to number OE Hex.

Bit 4 = One : This bit is set by the device after a Load Device Attribute Command is executed. This bit can only be reset by executing a Load Device Attribute Command to number OE Hex.

The setting of this bit causes bit 5 of Sense Byte 2 to be set.

Bits 0, 1, 2 and 3 shall be zero.

4.3.7 Table ID (Number OF Hex)

This attribute defines the meaning of numbers 10 - FF Hex.

When the value of this attribute is equal to 01 Hex, then Sections 4.3.8 to 4.3.36 define the attributes for numbers 10 - FF Hex.

When the value of this attribute is equal to FF Hex, see vendor specifications for meaning of numbers 10 - FF Hex.

When the value of this attribute is equal to 00 Hex, the values of all table numbers are undefined.

All other values of this attribute are reserved for future standardization.

4.3.8 Bytes Per Track High (Number 10 Hex)

This attribute is the most significant byte of a 24 bit number that represents the total number of unformatted bytes that occur between active going edges of Index Pulses.

4.3.9 Bytes Per Track Medium (Number 11 Hex)

This attribute is the medium significant byte of a 24 bit number that represents the total number of unformatted bytes that occur between active going edges of Index Pulses.

4.3.10 Bytes Per Track Low (Number 12 Hex)

This attribute is the least significant byte of a 24 bit number that represents the total number of unformatted bytes that occur between active going edges of Index Pulses.

4.3.11 Bytes Per Sector High (Number 13 Hex)

This attribute is the most significant byte of a 24 bit number that represents the total number of bytes that occur between active going edges of Sector pulses, and between the active going edge of the Index Pulse and the active going edge of the first Sector Pulse.

4.3.12 Bytes Per Sector Medium (Number 14 Hex)

This attribute is the medium significant byte of a 24 bit number that represents the total number of bytes that occur between active going edges of Sector Pulses, and between the active going edge of the Index Pulse and the active going edge of the first Sector Pulse.

4.3.13 Bytes Per Sector Low (Number 15 Hex)

This attribute is the least significant byte of a 24 bit number that represents the total number of bytes that occur between active going edges of Sector Pulses, and between the active going edge of the Index Pulse and the active going edge of the first Sector Pulse.

4.3.14 Sector Pulses Per Track High (Number 16 Hex)

This attribute defines the most significant byte of a 24 bit number that indicates the number of Sector Pulses between but excluding Index Pulses generated by hard sectored devices. The Sector Pulses are used to divide a track into sectors. The length of the sectors (distance between Sector Pulses) is defined by the Bytes Per Sector attribute.

4.3.15 Sector Pulses Per Track Medium (Number 17 Hex)

This attribute defines the medium significant byte of a 24 bit number that indicates the number of Sector Pulses between but excluding Index Pulses generated by hard sectored devices. The Sector Pulses are used to divide a track into sectors. The length of the sectors (distance between Sector Pulses) is defined by the Bytes Per Sector attribute.

4.3.16 Sector Pulses Per Track Low (Number 18 Hex)

This attribute defines the least sgnificant byte of a 24 bit number that indicates the number of Sector Pulses between but excluding Index Pulses generated by hard sectored devices. The Sector Pulses are used to divide a track into sectors. The length of the sectors (distance between Sector Pulses) is defined by the Bytes Per Sector attribute.

4.3.17 Sectoring Method (Number 19 Hex)

This attribute defines the sectoring method used in the device. The sectoring methods are defined as follows:

Value	Sectoring Method
00 Hex	Invalid
01 Hex	Hard Sectoring
02-FF Hex	Reserved for future standardization

4.3.18 Number of Cylinders High (Number 20 Hex)

This attribute is the most significant byte of a 16 bit number that represents the number of cylinders implemented in the device. This number is one greater than the maximum allowable cylinder address that can be addressed.

4.3.19 Number of Cylinders Low (Number 21 Hex)

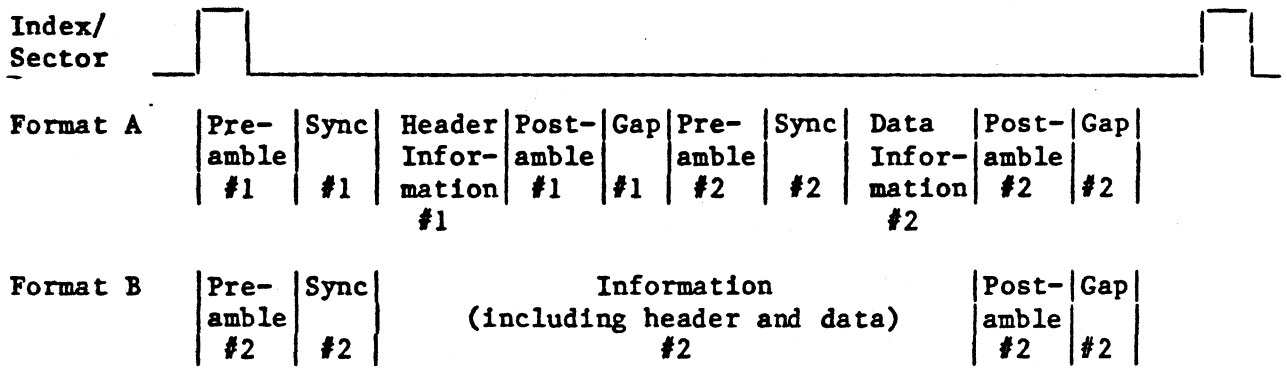
This attribute is the least significant byte of a 16 bit number that represents the number of cylinders implemented in the device. This number is one greater that the maximum allowable cylinder address that can be addressed.

4.3.20 Number of Moving Heads (Number 22 Hex)

This attribute represents the number of moving heads implemented in the device. This number is one greater than the maximum allowable moving head address that can be addressed.

Figure 4-1

Sector Formats for Attributes Hex 30 - 47



4.3.21 Header Encoding Method #1 (Number 30 Hex)

This attribute represents the header encoding method used for all fields labeled "#1" in the device and is defined as follows:

Value	Encoding Method
00 Hex	Modified Frequency Modulation (MFM)
01 Hex	ANSI Group Code Recordng (GCR)

The definition of formatting requirements as defined by Commands 30 - 47 is based on one of the formats in Figure 4-1.

4.3.22 Preamble #1 Length (Number 31 Hex)

This attribute represents the minimum number of header preamble bytes required by the device.

4.3.23 Preamble #1 Pattern (Number 32 Hex)

This attribute represents the pattern to be recorded in the header preamble bytes. The pattern shall be recorded starting with the most significant bit.

4.3.24 Synchronization #1 Pattern (Number 33 Hex)

This attribute represents the pattern to be recorded in a one byte header synchronization field following the preamble. The pattern shall be recorded starting with the most significant bit.

4.3.25 Postamble #1 Length (Number 34 Hex)

This attribute represents the minimum number of header postamble bytes required by the device. A value of zero indicates that no postamble is required.

4.3.26 Postamble #1 Pattern (Number 35 Hex)

This attribute represents the pattern to be recorded in the header postamble bytes. The pattern shall be recorded starting with the most significant bit.

4.3.27 Gap #1 Length (Number 36 Hex)

This attribute represents the minimum number of bytes in the header gap (splice area) between postamble and the next preamble.

4.3.28 Gap #1 Pattern (Number 37 Hex)

This attribute represents the pattern to be recorded in the header gap bytes. The pattern shall be recorded starting with the most significant bit.

4.3.29 Data Encoding Method #2 (Number 40 Hex)

This attribute represents the encoding method used for all fields labeled "#2" in the device and is defined as follows:

Value	Encoding Method
00 Hex	Modified Frequency Modulation (MFM)
01 Hex	ANSI Group Code Recording (GCR)
02 - FF Hex	Reserved for future standardization

The definition of formatting requirements as defined by Commands 30 - 47 is based on one of the formats in Figure 4-1.

4.3.30 Preamble #2 Length (Number 41 Hex)

This attribute represents the minimum number of preamble bytes required by the device.

4.3.31 Preamble #2 Pattern (Number 42 Hex)

This attribute represents the pattern to be recorded in the preamble bytes. The pattern shall be recorded starting with the most significant bit.

4.3.32 Synchronization #2 Pattern (Number 43 Hex)

This attribute represents the pattern to be recorded in a one byte synchronization field following the preamble. The pattern shall be recorded starting with the most significant bit.

4.3.33 Postamble #2 Length (Number 44 Hex)

This attribute represents the minimum number of postamble bytes required by the device. A value of zero indicates that no postamble is required.

4.3.34 Postamble #2 Pattern (Number 45 Hex)

This attribute represents the pattern to be recorded in the postamble bytes. The pattern shall be recorded starting with the most significant bit.

4.3.35 Gap #2 Length (Number 46 Hex)

This attribute represents the minimum number of bytes in the gap (splice area) between postamble and the next preamble.

4.3.36 Gap #2 Pattern (Number 47 Hex)

This attribute represents the pattern to be recorded in the gap bytes. The pattern shall be recorded starting with the most signficant bit.

Table 4-4

General Status Byte

Bit #	Meaning	Method of Clearing
0	Not Ready **	Self Clearing
1	Control Bus Error*	Clear Fault Command
2	Illegal Command *	Clear Fault Command
3	Illegal Parameter *	Clear Fault Command
4	Sense Byte 1 **	**
5	Sense Byte 2 **	**
6	Busy Executing	Self Clearing
7	Normal Complete	Clear Attention Command

* A zero to one transition of this bit shall set the Attention Condition.

** See Sense Byte 1 and Sense Byte 2.

*** The ready to not ready and not ready to ready transition shall set the Attention Condition.

Table 4-5

Sense Byte 1

Bit #	Meaning	Method of Clearing
0	Seek Error *	Clear Fault Command
1	Read/Write Fault *	Clear Fault Command
2	Power Fault *	Clear Fault Command
4	Speed Error *	Clear Fault Command
5	Command Reject *	Clear Fault Command

Table 4-6

Sense Byte 2

Bit #	Meaning	Method of Clearing
0	Initial State *	Clear Attention Command
1	Ready Transition *	Clear Attention Command
5	Device Attribute Table Modified	Clear Attention Command
6	Postioned Within Write Protected Area	Self Clearing

Note: All undefined bits must be zero.

* A zero to one transition of this bit shall set the Attention Condition.

4.4 Status Reporting

4.4.1 General Status Byte

4.4.1.1 Bit 0 - Not Ready

The Not Ready Bit shall be set if the device is unable to perform any head motion or read/write operation.

Index, Sector Mark, and Read/Reference Clock are invalid when the device is not ready.

The Not Ready Bit shall be reset when the device becomes ready.

The ready to not ready and not ready to ready transition shall set the Attention Condition.

4.4.1.2 Bit 1 - Control Bus Error

This bit shall be set if the device detects a protocol error during the transfer of a command or parameter such as:

- Command Request and Bus Direction Out inactive
- The level of the Bus Direction Out Signal for the transfer of the Parameter Byte does not comply with the Command Code.
- Two consecutive Parameter cycles
- Two consecutive Command cycles

The device shall not act upon the command transferred during a Command/Parameter cycle resulting in a Control Bus Error. If the Bus Direction Out Signal is inactive for the second byte and a Control Bus Error has been detected, the device shall return the General Status Byte.

The Control Bus Error Bit shall be reset by the Clear Fault Command.

The detection of a Control Bus Error shall set the Attention Condition.

4.4.1.3 Bit 2 - Illegal Command

This bit shall be set if the device detects an illegal command such as:

a) The command received is not implemented in the device.

   This error may occur because of a hardware or software error, during a self-configuring process or when receiving the "Report Illegal Command" Command.

The Illegal Command Bit shall be reset by the Clear Fault Command.

This error shall set the Attention Condition.

4.4.1.4 Bit 3 - Illegal Parameter

This bit shall be set if the device tests for and detects an illegal parameter or part of a parameter such as:

a) The parameter is an address and exceed the valid range (e.g. illegal head address).

b) Any other illegal parameter value.

The Illegal Parameter Bit shall be reset by the Clear Fault Command.

This error shall set the Attention Condition.

4.4.1.5 Bit 4 - Sense Byte 1

This bit shall be generated by an "OR" function of all bits in the Sense Byte 1 status byte. The Sense Byte 1 Bit shall be reset if all bits of the Sense Byte 1 are zero.

4.4.1.6 Bit 5 - Sense Byte 2

This bit shall be generated by an "OR" function of all bits in the Sense Byte 2 status byte. The Sense Byte 2 Bit shall be reset if all bits of the Sense Byte 2 are zero.

4.4.1.7 Bit 6 - Busy Executing

This bit shall be set during the execution of all Time Dependent Commands and shall be set prior to the return of General Status for those Commands With Parameters In that return the General Status as the parameter (see Table 4-1, Table 4-2, and Section 4.2).

This bit is automatically cleared when the execution of the Time Dependent Command is completed and the Normal Complete or error status is set.

Note: This status bit is different from the Busy interface signal (see Section 3.2.7).

4.4.1.8 Bit 7 - Normal Complete

This bit shall be set if the device has successfuly completed the execution of a Time Dependent Command. See Table 4-1 and 4-2.

The Normal Complete Bit shall be reset by the Clear Attention Condition.

4.4.2 Sense Byte 1

4.4.2.1 Bit 0 - Seek Error

The Seek Error Bit shall be set if a head positioning command (Seek, Rezero, Seek To Landing Zone or Offset) cannot be completed successfully.

If a Rezero Command is required for recovery, a successful rezero operation shall reset this bit. If no Rezero Command is required, the Clear Fault Command shall reset this bit.

The zero to one transition of this bit shall set the Attention Condition.

4.4.2.2 Bit 1 - Read/Write Fault

This bit shall be set if the device is not able to execute a Read Command or a Write Command or detects a fault during reading or writing. Two kinds of faults are distinguished:

a) Bit 1 and Bit 5 shall be set if the execution of a read/write function requested by making Read Gate or Write Gate active is prevented by one of the following conditions:

   - Write Gate active and writing disabled with a Write Control Command (see Section 4.1.2).

b) Bit 1 only shall be set if the device detects a fault in its read/write section, for example:

   - Simultaneous selection of more than one head.
   - Write Gate active but no write current.
   - Optionally the bit may be set if the device detects Read Gate and Write Gate active simultaneously.

The Read/Write Fault Bit shall be reset by the Clear Fault Command.

The zero to one transition of this bit shall set the Attention Condition.

4.4.2.3 Bit 2 - Power Fault

This bit shall be set if the device tests for and detects a failure such as overvoltage or undervoltage in one of its supply voltages.

This bit shall be reset by the Clear Fault Command if the power failure no longer exists. The Zero to one transition of this bit shall set the Attention Condition.

4.4.2.4 Bit 4 - Speed Error

This bit shall be set if the device tests for and detects that the spindle speed is not within the device vendor specified tolerances.

This bit shall be reset by the Clear Fault Command if the spindle speed is within the specified tolerance.

The zero to one transition of this bit shall set the Attention Condition.

4.4.2.5 Bit 5 - Command Reject

This bit shall be set if the device received a command which it cannot execute at this time because of some interlocking condition or command sequence error.

This status bit may be set in combination with another status bit that defines the reason why the command was rejected. e.g. - The device is not ready and has received a command that cannot be executed (such as, Seek when the disk is not rotating).

The Command Reject Bit shall be reset by the Clear Fault Command.

The zero to one transition of this bit shall set the Attention Condition.

4.4.3 Sense Byte 2

4.4.3.1 Bit 0 - Initial State

This bit shall be set if an initialize procedure has been entered and the procedure has been completed.

The Initialize State Bit shall be reset by a Clear Attention Command.

The zero to one transition of this bit shall set the Attention Condition.

4.4.3.2 Bit 1 - Ready Transition

This bit shall be set if a zero to one or a one to zero transition of the Not Ready Bit (see Section 4.4.1.1) has occurrd.

The Ready Transition Bit shall be reset by a Clear Attention Command.

The zero to one transition of this bit shall set the Attention Condition.

4.4.3.3 Bit 5 - Device Attribute Table Modified

This bit shall be set if bit 4 of the Table Modification Attribute Number Hex OE is set to a one (see Section 4.3.6).

This bit shall be reset by a Clear Attention Command.

The zero to one transtion of this bit shall set the Attention Condition.

4.4.3.4 Bit 6 - Positioned Within Write Protected Area

This bit shall be set by the device whenever Write Control (see Section 4.1.2) has placed the device in the write disable state.

This bit shall be set by the device whenever the head is positioned within an area that has been defined as Write Protected (see Section 4.1.2.15 & 16) and the device is write enabled.

Any device detectible means that write protects an area of the device shall be reflected in this bit.

This bit shall be cleared whenever the head(s) is postioned outside of the Write Protected area.

This bit is not defined during head movement.

5.0 Timing Specification

The timing characterists described in the following paragraphs are referenced to the signals at the device interface connector. The host timing shall be designed to accommodate cable delays and signal skew within the cable.

Note: This section takes precedence, with respect to actions and timing, over all preceding sections. All waveforms in the timing diagrams show the voltage levels of the signals. A "-" in front of a signal name indicates a "LOW" - active, "HIGH" - inactive signal. A "+" in front of a signal name indicates a "HIGH" - active, "LOW" - inactive signal.

5.1 Control Bus Timing

5.1.1 Selection Timing

The active going edge of the Select Out/Attention In Strobe shall be used to clock the information on the dedicated Control Bus line into the device. A successful seletion shall be acknowledged by making Bus Acknowledge active. In the host the inactive going edge of the Select Out/Attention In Strobe Signal shall be used to sample the Bus Acknowledge Signal. If Bus Acknowledge is not active within the specified time, the host shall assume that the desired device does not exist or is inoperable. The state of the Busy Signal indicates to the host if the selected device will accept commands and respond to the Control Bus handshake.

Deselecting all devices shall be accomplished by an active going edge of Select Out/Attention In Strobe with none of the Control Bus lines active.

The select timing is defined in Figure 5-1.

5.1.2 Attention Timing

In general the timing of the party line Attention Signal (see Section 3.2.8) is asynchronous to the Control Bus Signals. However, if a command error or parameter error is detected, the Attention Condition shall be set and if enabled the Attention Signal shall be made active prior to the active going edge of Bus Acknowledge which is returned as a response to the Parameter Request. All other events (completion or errors) shall make Attention active (if enabled) immediately, when they occur.

Attention shall be made inactive prior to the active going edge of the Bus Acknowledge which is returned as a response to the Parameter Request of a Clear Attention Command or Clear Fault Command. Attention shall not be made inactive by a Clear Fault Command if the error that caused Attention to be made active still exists.

To determine which one of the attached devices has caused the party line Attention Signal to be active, the host polls all devices simultaneously by making the Bus Direction Out Signal inactive and changing the Select Out/Attention In Strobe from inactive to active. Each device shall then immediately gate its internal Attentional Condition onto its dedicated Control Bus line. Additionally, the selected device, if any, shall make the Bus Acknowledge Signal active.

The Attention timing is defined in Figure 5-2.

5.1.3 Control Bus Handshake Timing

The Control Bus handshake is performed by three interface signals: Command Request, Parameter Request, and Bus Acknowledge.

The Control Bus handshake timing is defined in Figures 5.3 and 5.4.

5.2 Index and Sector Timing

The timing of the Index Signal and the Sector signal for hard-sectored devices is shown in Figure 5-5. There is one and only one Index Pulse per revolution. The Sector Pulses are used to divide a track into sectors. The device inhibits the Sector Pulse during the Index Pulse such that a Sector Pulse is not transmitted at Index.

The Index Signal and Sector Signal are enabled with device selection. The Index Signal and Sector Signals shall not be considered valid until at least 500 nanoseconds after the active going edge of the Select Out/Attention In Strobe Signal which caused the selection of the device.

5.3 Reference Clock Timing

The Reference Clock timing is defined in Figure 5-6.

5.4 Read Timing

The read timing is defined in Figure 5-7.

5.5 Write Timing

The write timing is defined in Figure 5-8. The Write Clock shall be generated in the host from the Reference Clock. The delay time from the Reference Clock to Write Clock is a function of cable length and circuit delays. The phase difference between the two signals shall be constant during the complete write operation. The Write Data Signal and the Write Clock Signal shall be synchronzied as defined in Figure 5-8. The Read Data Signal is undefined during a write operation.

5.6 Data Format and Data Control Timing

The Record Format on the disk is under control of the host. The index and sector pulses are available for use by the host to indicate the beginning of a track or sector. Suggested formats are shown in Figures 4-1.

Some hardware-oriented constraints must be recongized when designing a format. The following is a list of those format parameters:

5.6.1 Read Initialization Time

The deselection of one head and the selection of another head shall occur within the Select Moving Head command, and the device shall be ready for reading or writing at the termination of the second occurrence of Bus Acknowledge.

5.6.2 Write-To-Read Recovery Time

Assuming head selection is stablized, the time lapse before read gate can be enabled after switching the write gate off is 10 us, minimum.

5.6.3 Read-To-Write Recovery Time

Assuming head selection is stabilized, the time lapse from dropping read gate to enabling write gate shall be 0.3 us, minimum.

5.6.4 Read PLO Synchronization

The synchronization time needed to allow the phase-locked oscillator to synchronize is 9 us of zeros.

5.6.5 Sync Pattern

The Sync Pattern consists of "1" bits indicating the beginning of the address or data area one "1" bit is the minimum required . See Sections 4.3.24 and 4.3.32.

5.6.6 Write Driver Turn On

The Write Driver Turn On time is about 0.8 us or one byte. This time has to be accounted for in order to know where possible splice areas are located.

5.6.7 Gap 2 Tolerance

This tolerance is a pad of zeros which eliminate the possibility of destroying the end of a record written. See Attribute Table for size.

5.7 Control Timing

5.7.1 Read

The control line associated with a read command is the Read Gate line.

The leading edge of Read Gate forces the phase locked oscillator to synchronize on a preamble pattern. Read Gate also enables the output of the data separator onto the I/O lines after a lock-to-data internal time out. Read Gate must be dropped and raised again after going through a splice area (Gap). Read Gate may be enabled 60 $\pm$ 4 clock counts after the leading edge of index or sector.

Read Data may not have valid data until 9 us from leading edge of Read Gate, due to phase lock synchronizing time.

There should be no splice area after Read Gate is brought up.

5.7.2 Write Data Field

The control line associated with a Write operation is Write Gate.

The sector address must always be read and verified prior to writing the data field, except while formatting.

Writing the data field must always be preceded by writing the PLO sync field and sync pattern.

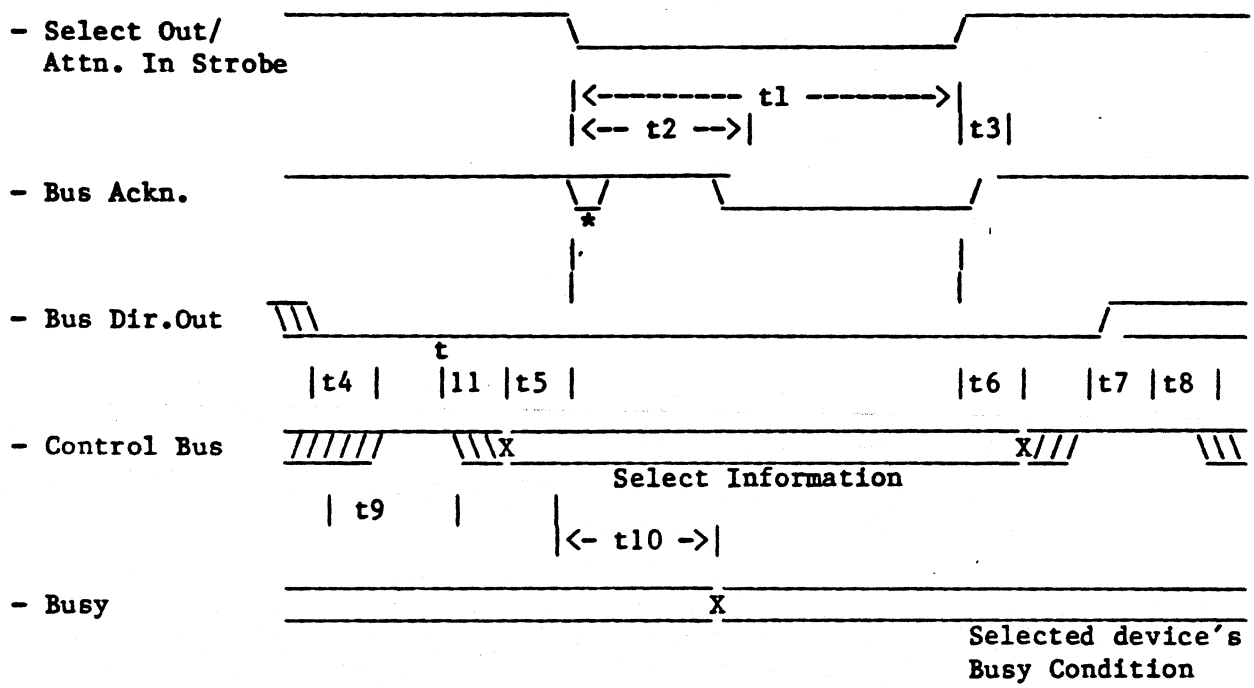
The Controller must provide a three bit internal delay (approximately 0.2 us) between the trailing edge of the Read Gate signal and the leading edge of the Write Gate signal see Figure 8A or 8B . This delay will allow for signal propagation tolerances and prevent a possible overlap of the Read and Write Gate in the unit.

Writing the data field must always be followed by writing the checkword and at least an eight bit pad at the end of the checkword.

During formatting, Write Gate is raised upon sensing index or sector. During a record update, Write Gate is raised within two bits of the last bit of an address, but no closer than 1 bit.

Figure 5-1

Select Timing

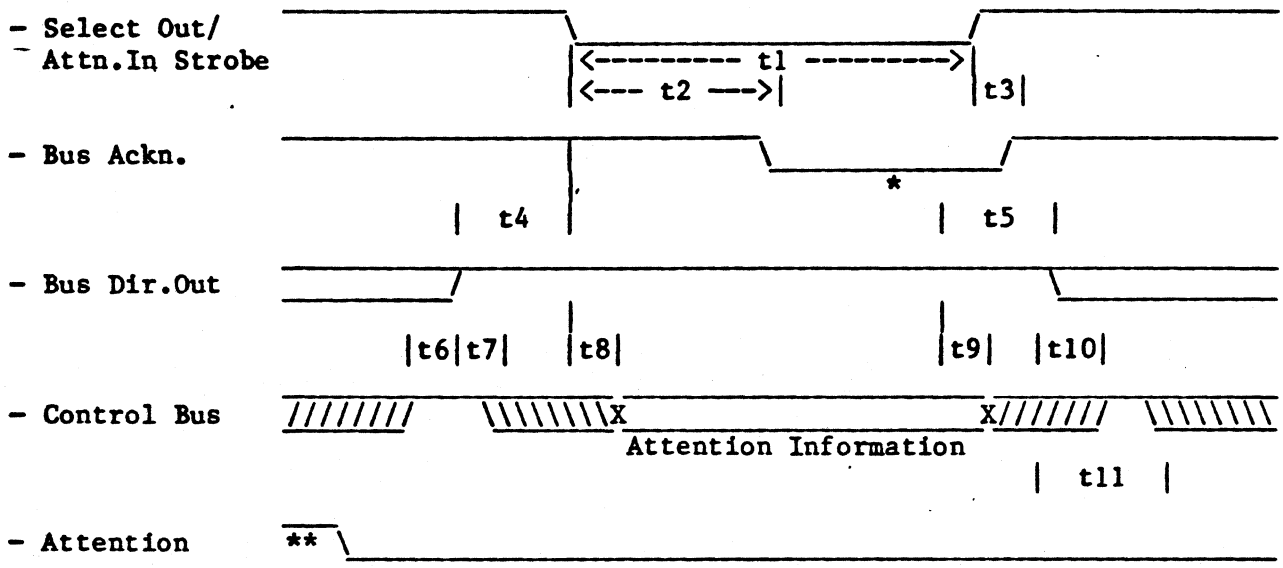


* Glitch possible - due to previously selected device. To avoid glitch deselect all devices and then select.

Label	Description	min.	max.	Units
t1	Select/Attention Strobe Width	500	---	nanoseconds
t2	Bus Acknowledge invalid	0	300	nanoseconds
t3	Bus Acknowledge hold time	0	100	nanoseconds
t4	Device - Control Bus release time	0	100	nanoseconds
t5	Control Bus - Data setup time	100	---	nanoseconds
t6	Control Bus - Data hold time	0	---	nanoseconds
t7	Host - Control Bus release time	100	---	nanoseconds
t8	Device - Control Bus access time	0	---	nanoseconds
t9	Host - Control Bus access time	100	---	nanoseconds
t10	Busy invalid	0	300	nanoseconds
t11	Device to Host transition	0	---	nanoseconds

Figure 5-2

Attention Timing



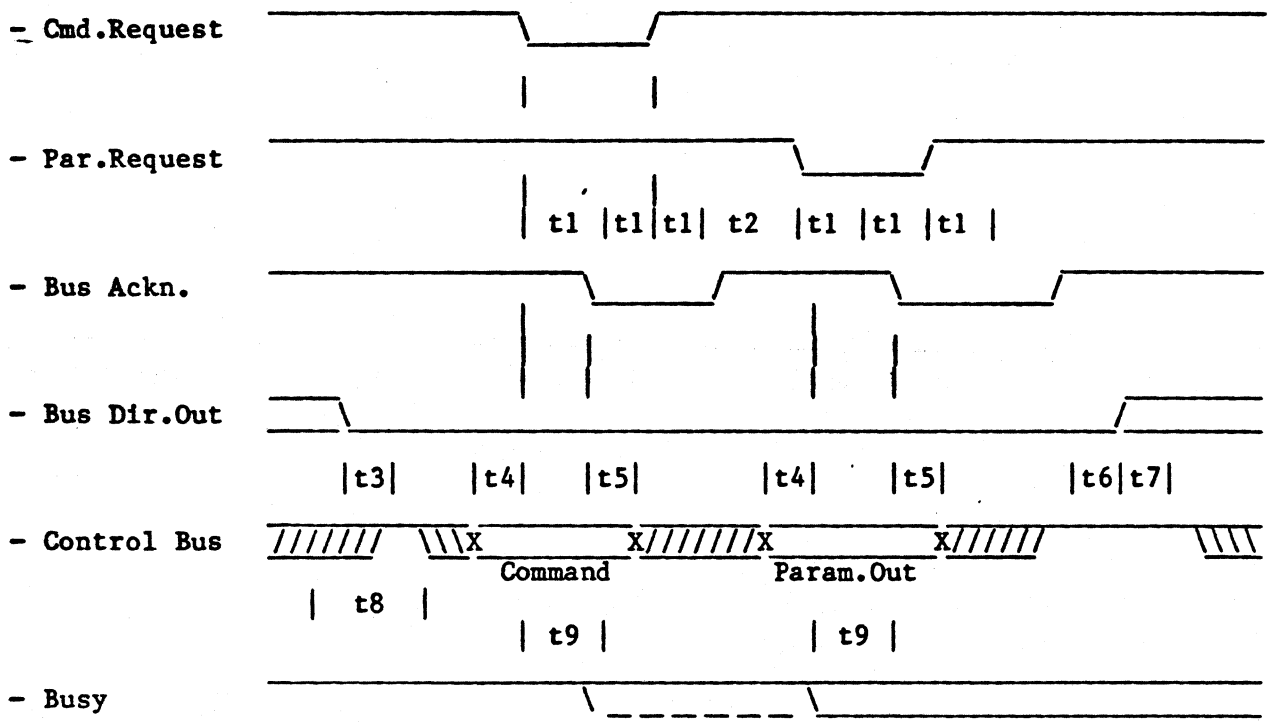
* Active only if there is a ..... selectived device inactive if all devices are deselected.

** Some devices may have Attention active causing the host to perform the Attention timing sequence.

Label	Description	min.	max.	Units
t1	Select/Attention Strobe Width	500	---	nanoseconds
t2	Bus Acknowledge invalid *	0	300	nanoseconds
t3	Bus Acknowledge hold time	0	100	nanoseconds
t4	Bus Direction Out - setup time	100	---	nanoseconds
t5	Bus Direction Out - hold time	0	---	nanoseconds
t6	Host - Control Bus release time	100	---	nanoseconds
t7	Device - Control Bus access time	0	---	nanoseconds
t8	Attention Information invalid	0	100	nanoseconds
t9	Attention Information hold time	0	---	nanoseconds
t10	Device - Control Bus release time	0	100	nanoseconds
t11	Host - Control Bus access time	100	---	nanoseconds

Figure 5-3

Command/Parameter Out Sequence

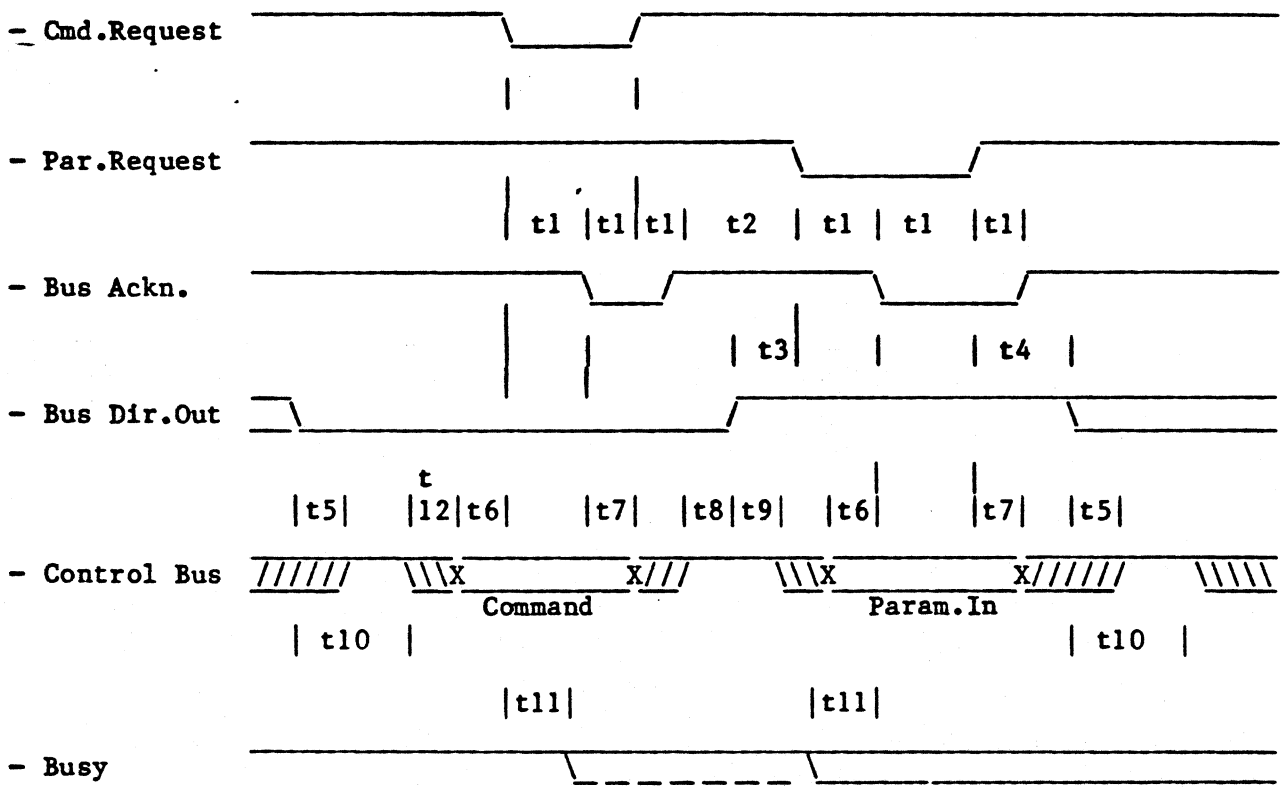


Label	Description	min.	max.	Units
t1	Handshake response time	0	10*	milliseconds
t2	Spacing	0	10*	milliseconds
t3	Decice - Control Bus release time	0	100*	nanoseconds
t4	Control Bus - Data setup time	100	---	nanoseconds
t5	Control Bus - Data hold time	0	---	nanoseconds
t6	Host - Control Bus release time	100	---	nanoseconds
t7	Device - Control Bus access time	0	---	nanoseconds
t8	Host - Control Bus access time	100	---	nanoseconds
t10	Busy set-up time	0*	---	nanoseconds

* This value is valid only if the Busy Signal is not active at beginning of sequence.

Figure 5-4

Command/Parameter In Sequence

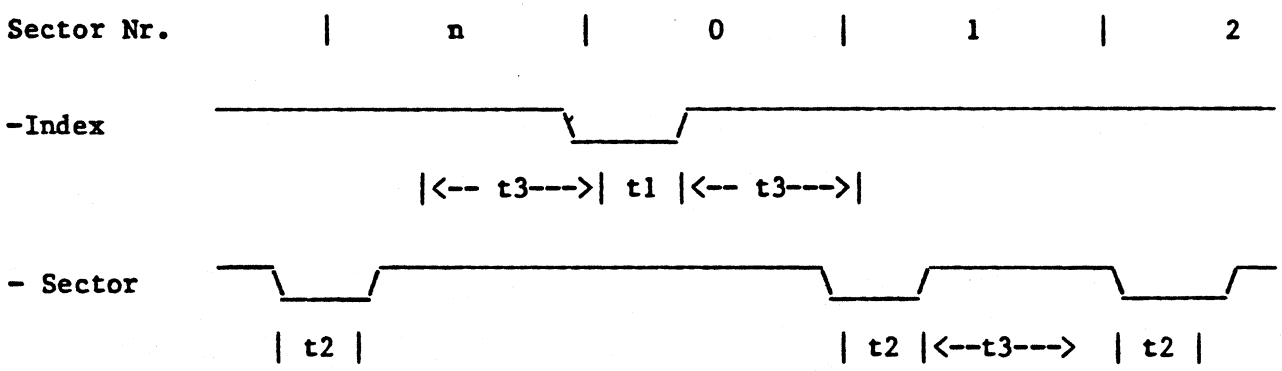


Label	Description	min.	max.	Units
t1	Handshake response time	0	10*	milliseconds
t2	Spacing	0	10*	milliseconds
t3	Bus Direction Out - setup time	100	---	nanoseconds
t4	Bus Direction Out - hold time	0	---	nanoseconds
t5	Device - Control Bus release time	0	100	nanoseconds
t6	Control Bus - Data setup time	100	---	nanoseconds
t7	Control Bus - Data hold time	0	---	nanoseconds
t8	Host - Control Bus release time	100	---	nanoseconds
t9	Device - Control Bus access time	0	---	nanoseconds
t10	Host - Control Bus access time	100	---	nanoseconds
t11	Busy setup time	0 *	---	nanoseconds
t12	Device to Host transition	0	---	nanoseconds

*This value is valid only if the Busy Signal is not active at beginning of sequence

Figure 5-5

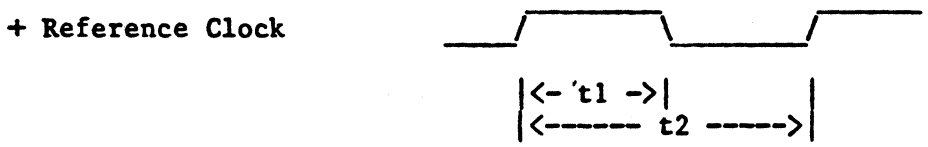
Index/Sector Timing (Hard Sectoring)



Label	Description	min.	max.	Units
t1	Index Pulse width	0.5	---	microseconds
t2	Sector Pulse width	0.5	---	microseconds
t3	Interpulse spacing	0.5	---	microseconds

Figure 5-6

Reference Clock Timing

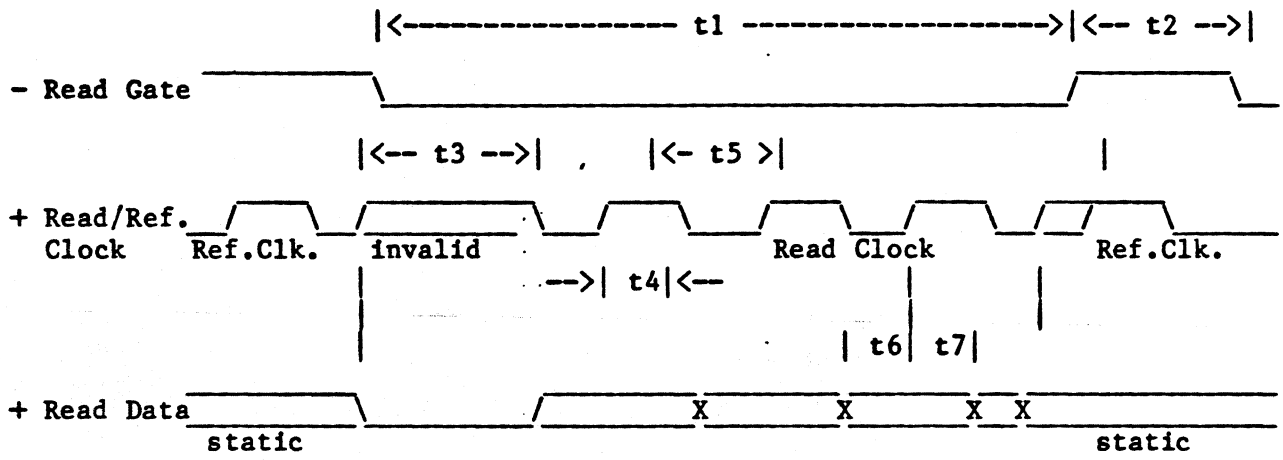


Label	Description	min.	max.
t1	Reference Clock active time	0.4*tp	0.6*tp
t2	Bus Acknowledge invalid	0.95*tp	1.05*tp
tp	nominial Reference Clock period		

* = Multiply

Figure 5-7

Read Timing

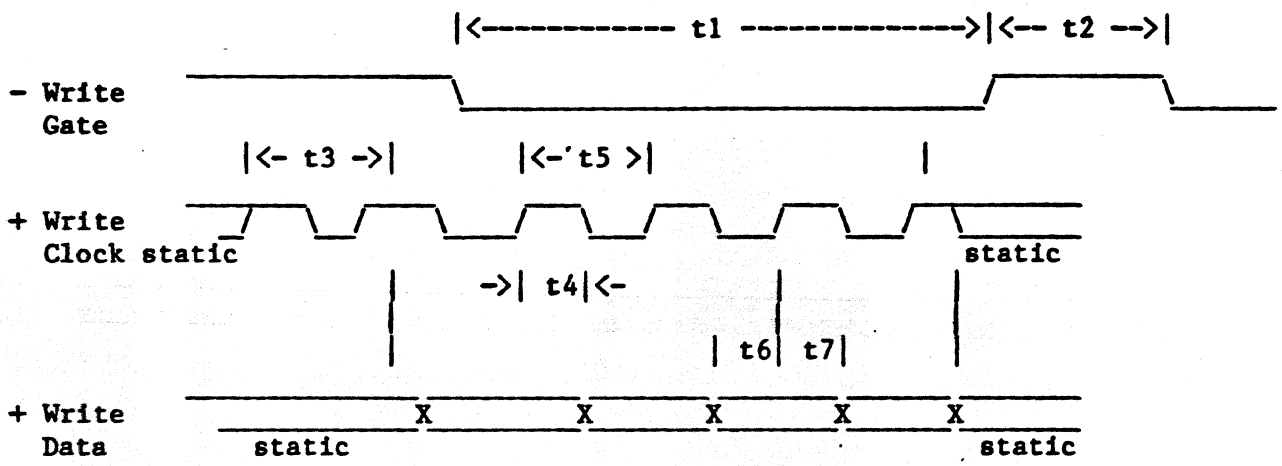


Label	Description	min.	max.
t1	Read Gate active	0	---
t2	Read Gate inactive	2*tp	---
t3	Read Gate to valid Read Data and Read Gate	See vendor specifications	
t4	Read Clock active time	0.4*tp	0.6*tp
t5	Read Clock period	0.95*tp	1.05*tp
t6	Read Data setup time	0.25*tp	---
t7	Read Data hold time	0.25*tp	---
tp	nominal Reference Clock period		

* = Multiply

Figure 5-8

Write Timing



Label	Description	min.	typ.	max.
t1	Write Gate active	0	---	---
t2	Write Gate inactive	0	---	---
t3	Write Clock valid	tp	---	16*tp
t4	Write Clock active time	0.4*tp	---	0.6*tp
t5	Write Clock period	---	tp	---
t6	Write Data setup time	0.25*tp	---	---
t7	Write Data hold time	0.25*tp	---	---
tp	nominal Reference Clock period			

* = Mulitply