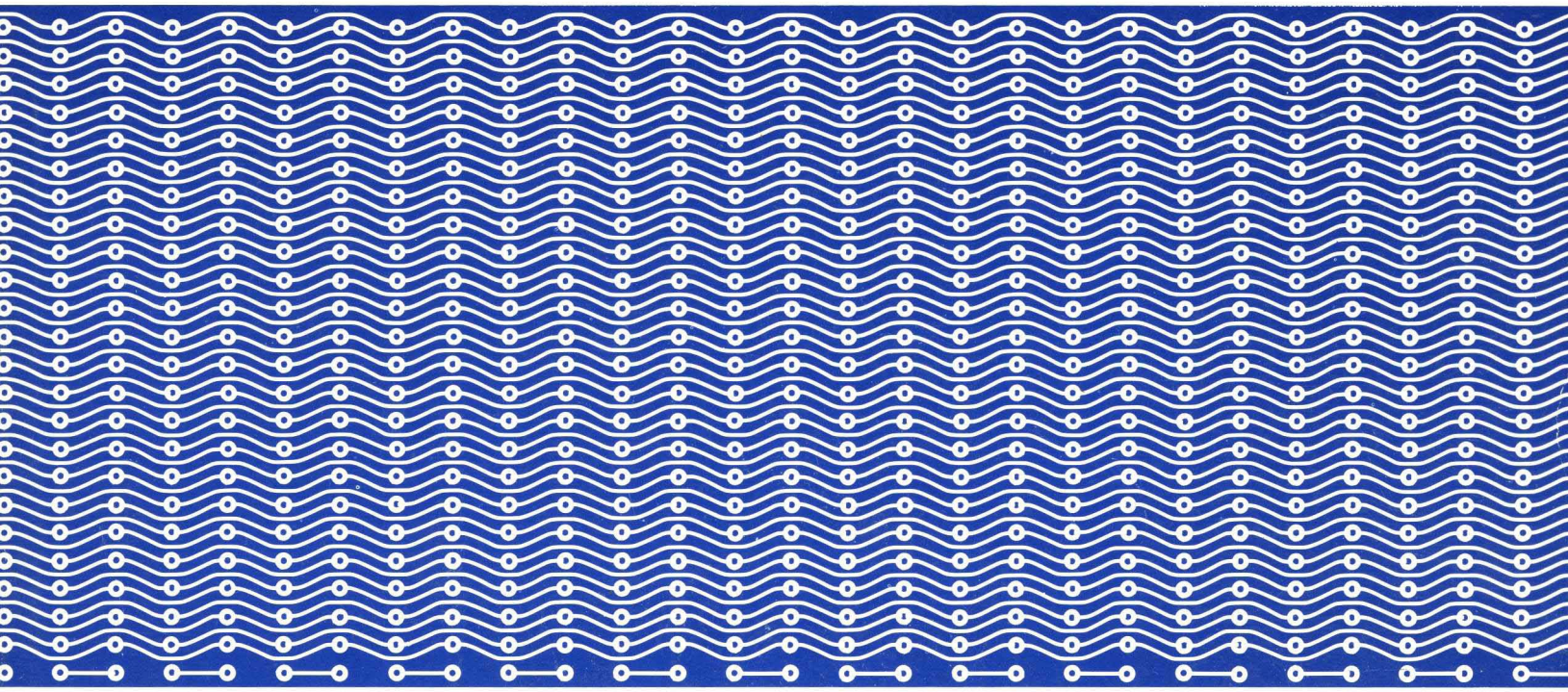
Series 7000 STD BUS

Technical Manual



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Introduction

This manual defines the standards that constitute the STD BUS and the parameters which are common to the Series 7000 cards. The Series 7000 Data Sheets are included to illustrate the compatibility of the Series 7000 cards and provide design guidelines and application information.

It is aimed primarily at the professional design engineer who contemplates using the STD BUS in his company's products.

The STD BUS is a concept conceived by Pro-Log Corporation and developed jointly with MOSTEK as a simple bus structure for 8 bit microprocessors. It is a 56 pin bus, logically organized and easily learned. The number of pins and their use is a well thought out compromise between the simplest possible bus and an infinitely flexible bus. The bus was kept simple to facilitate design, production and maintenance. It was made sufficiently flexible to work with all industry standard 8 bit microprocessors and to be used in both dedicated control and data processing applications.

The company using STD BUS hardware in its products generally wants to control the design, production and maintenance of those products with his existing personnel. Pro-Log's Series 7000 hardware helps him attain this goal because these products are modular, standardized, use only second sourced industry standard parts, are thoroughly documented and have a manufacturing rights option which allows Pro-Log customers to produce the STD 7000 products themselves, if they wish.

Pro-Log also teaches courses on how to design with, and use, Microprocessors and the STD BUS products, instruments such as PROM Programmers and System Analyzers with which to manufacture and service STD BUS products.

THE STD BUS PROVIDES

- Standard 8-Bit Microprocessor BUS Pin Out
- Standard 56 Pin Connector
- Standard 4½"x6½" Card Size
- Standard ½" Card Spacing

THE STD BUS OFFERS

- Multiple Sources
- Unrestricted Use, Not Trademarked, Copyrighted or Patented
- Function Modularity
- Card Slot Independence
- Separate Digital and Analog Power Busses

THE SERIES 7000 CARDS ADD

- Motherboard Interconnect
- High Functional Density
- Low Power Consumption
- Industry Standard Components
- Second Sourced Components
- Completely Tested Cards
- Power On Burn-In
- RETMA Rack Mounting Compatible Card Cages
- Choice of Microprocessor

Series 7000 STD BUS

Technical Manual

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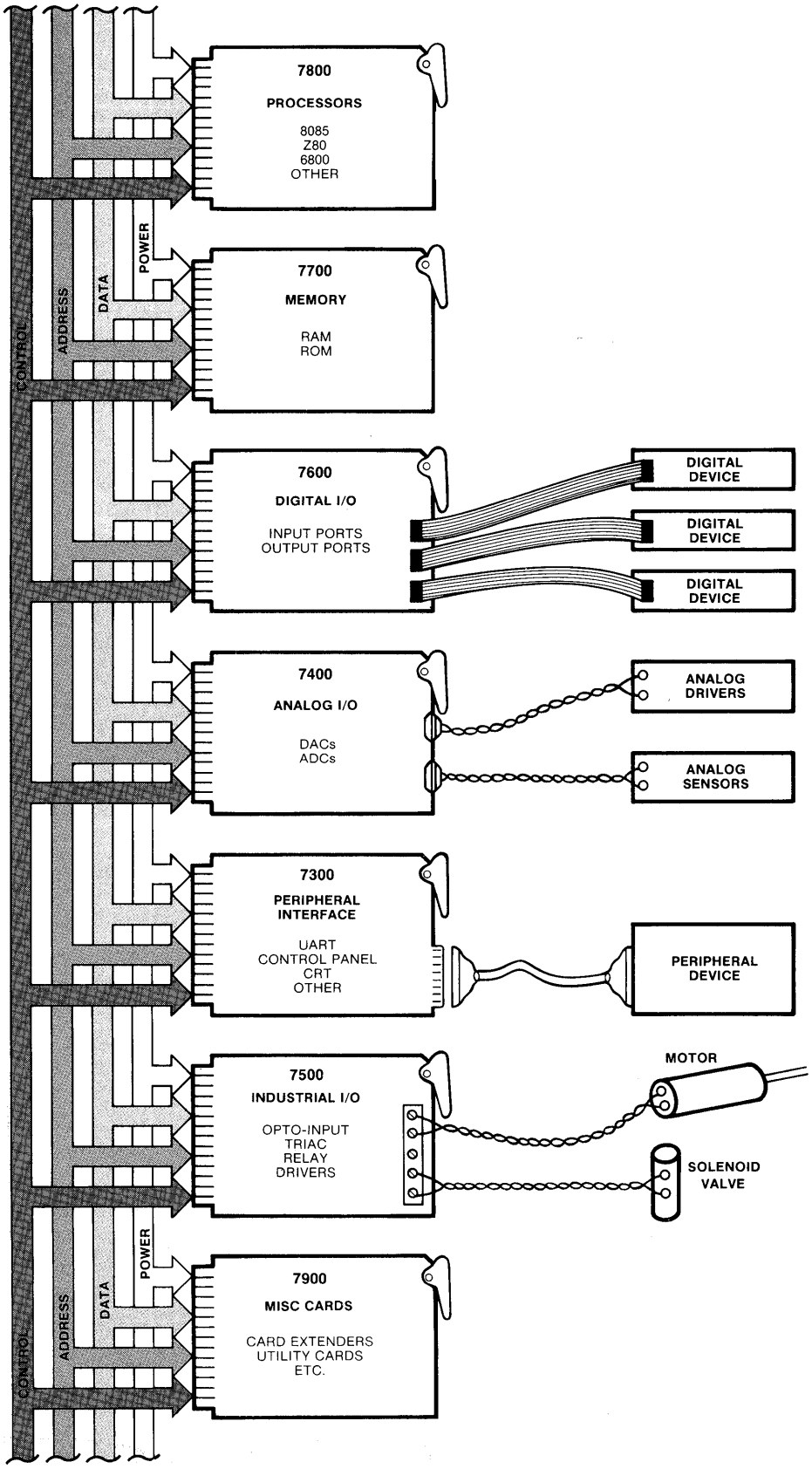


Figure 1-1 STD Implementation

Section 1

The STD BUS

Introduction

This section defines the standards that constitute the STD BUS.

The STD BUS standardizes the physical and electrical aspects of modular 8-bit microprocessor card systems, providing a dedicated orderly interconnection scheme. The standardized pinout and 56 pin connector lends itself to a bussed motherboard that permits any card to work in any slot. The STD BUS is dedicated to internal communications, with all other interconnections made via suitable connectors at the I/O interface card edge. The concept gives an orderly signal flow across the cards. Peripheral and I/O devices can be connected to the system according to their own unique connector and cabling requirements.

A diagram showing STD BUS implementation with Pro-Log Series 7000 cards is given in Figure 1-1.

Figure 1-2 and 1-3 show typical hardware implementations of some of the elements of Figure 1-1.

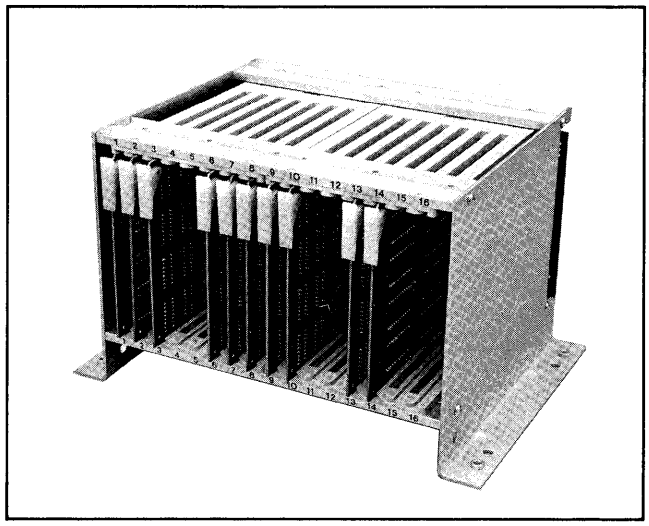


Figure 1-2

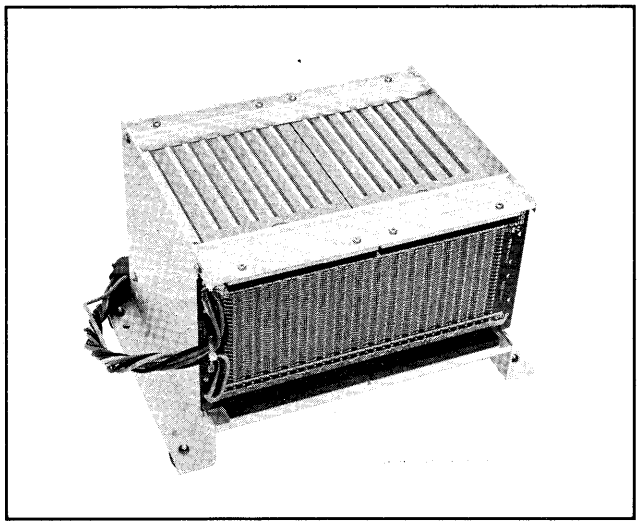


Figure 1-3

ORGANIZATION AND FUNCTIONAL SPECIFICATIONS (WITH PIN DEFINITIONS)

The STD BUS pinout is organized into five functional groups:

Logic Power Bus	Pins 1-6
Data Bus	Pins 7-14
Address Bus	Pins 15-30
Control Bus	Pin 31-52
Auxiliary Power Bus	Pins 53-56

The organization and pinouts are shown in Figure 1-4. This figure gives the mnemonic function and signal flow direction (referenced to the processor card in control of the BUS) for each pin of the STD BUS. The STD BUS is further defined as requiring a 56 pin (dual 28) card edge connector with 0.125 inch pin centers. The connectors are on a standard spacing interval of 0.5 inch centers and accept the standard 4½"x6½"x0.062" card.

STD BUS

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5V	In	+5 Volts DC (Bussed)	2	+5V	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5	-5V	In	-5 Volts DC	6	-5V	In	-5 Volts DC
DATA BUS	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
ADDRESS BUS	15	A7	Out	Low Order Address Bus	16	A15	Out	High Order Address Bus
	17	A6	Out	Low Order Address Bus	18	A14	Out	High Order Address Bus
	19	A5	Out	Low Order Address Bus	20	A13	Out	High Order Address Bus
	21	A4	Out	Low Order Address Bus	22	A12	Out	High Order Address Bus
	23	A3	Out	Low Order Address Bus	24	A11	Out	High Order Address Bus
	25	A2	Out	Low Order Address Bus	26	A10	Out	High Order Address Bus
	27	A1	Out	Low Order Address Bus	28	A9	Out	High Order Address Bus
	29	A0	Out	Low Order Address Bus	30	A8	Out	High Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read to Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP*	In/Out	I/O Expansion	36	MEMEX*	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Non-Maskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
POWER BUS	53	AUXGND	In	AUX Ground (Bussed)	54	AUXGND	In	AUX Ground (Bussed)
	55	AUX+V	In	AUX Positive (+12 Volts DC)	56	AUX-V	In	AUX Negative (-12 Volts DC)

*Low Level Active Indicator

Figure 1-4 STD BUS Pinouts

LOGIC POWER BUS - PINS 1-6

Provides basic voltage lines for predominant system logic.

- +5V - Pins 1 & 2 - +5 Logic Voltage, (VCC)
  Main logic voltage lines (+5 volts). Both pins are bussed together for current capacity.
- GND - Pin 3 & 4 - Logic Ground
  Ground for logic power. Both pins are bussed together for current capacity.
- -5V - Pin 5 - Negative 5 Volt Bias, (VBB)
  A low current (-5 volt) bias voltage line.
- -5V - Pin 6 - Negative 5 Volt Bias, (VBB)
  A secondary low current (-5 volt) bias voltage line.

DATA BUS - PINS 7-14

An 8-bit bidirectional 3-state bus. (Bidirectional means signals may flow either into or out of any card on the Bus.) Direction of data is normally controlled by the processor card via the Control Bus. The data direction is normally affected by such signals as Read (RD*), Write (WR*) and Interrupt Acknowledge (INTAK*).

The Data Bus uses high-level active logic levels. All cards are required to release the bus to a high impedance state when not in use. The Processor card releases the data bus in response to Bus Request (BUSRQ*) input from an alternate system controller, as in DMA transfers.

ADDRESS BUS - PINS 15-30

A 16-bit 3-state high-level active bus. The address will normally originate at the processor card. The processor card releases the Address Bus in response to a Bus Request (BUSRQ*) input from an alternate controller.

The Address Bus provides 16 address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines are used to distinguish between the two operations. The particular microprocessor used will determine the number of address lines and how they are used.

Example:

PROCESSOR	NO. OF MEM. ADR. LINES	ADR. LINES DURING REFRESH	NO. OF I/O ADDRESS LINES	
			I/O MAPPED I/O	MEMORY MAPPED I/O
8080	16		Lower 8 (3)	16
8085	16		Lower 8 (3)	16
Z80	16	Lower 7 (1)	Lower 8 (2)	16
6800	16		—	16
6809	16		—	16

(1) During the REFRESH cycle, A0 through A6 contain the REFRESH Address for dynamic RAMs while A7 is a Logic 0 and the Upper 8 Bits of the Address Bus contain the I register contents.

(2) During I/O operations the upper 8 address lines output the accumulator contents.

(3) During I/O operations the upper 8 address lines also output the I/O address.

CONTROL BUS - PINS 31-52

Provides control signals for memory, I/O, interrupt and fundamental system operations.

Control lines are available for memory expansion, memory mapped I/O, dynamic memory refresh, direct memory access, multi-processing, single-stepping, slow memory, power-fail-restart, fixed interrupt, priority vectored interrupt and bus analysis.

Bus pins have been allocated for special operations. Actual capabilities depend on the processor card used and the capabilities of supporting control cards.

- WR* - Pin 31 - Write to Memory or I/O
  A 3-state, active-low control line that indicates the BUS holds valid data to be written in the addressed memory or output device.
- RD* - Pin 32 - Read from Memory or I/O
  A 3-state, active-low control line that indicates the processor or other bus controlling device wants to read data from memory or an I/O device. The selected I/O device or memory should use this signal to gate data onto the BUS.
- IORQ* - Pin 33 - I/O Address Select
  A 3-state, active-low processor output control line. IORQ* indicates that the address lines hold a valid I/O address for an I/O Read or Write.
- MEMRQ* - Pin 34 - Memory Address Select
  A 3-state, active-low memory request line. MEMRQ* indicates that the address bus holds a valid address for memory read or memory write operations.
- IOEXP* - Pin 35 - I/O Expansion
  An active-low control signal used to expand or enable I/O Port addressing. If this pin is not used its is strapped to logic ground.
- MEMEX* - Pin 36 - Memory Expansion
  An active-low control signal used to expand or enable memory addressing. If this pin is not used it is strapped to logic ground.

Four control signals are provided to handle the timing requirements of various microprocessors. These signals are normally used for interfacing to memory and peripheral devices. They are REFRESH*, MCSYNC*, STATUS 0* and STATUS 1*.

- REFRESH* - Pin 37
  A 3-state active-low control line normally used to refresh dynamic memory. The signal may be generated on the processor card or on a separate control card. The nature and timing of the singal may be a function of the memory device or the microprocessor.
- MCSYNC* - Pin 38 - Machine Cycle Sync
  A 3-state, active-low Processor output signal that occurs once during each processor machine cycle. (Machine cycle is defined as the sequence that involves Addressing, Data Transfer and Execution.) MCSYNC* defines the beginning of the machine cycle. The exact nature and timing of this signal is microprocessor dependent.

Example REFRESH*

PROCESSOR	SIGNAL PIN 37
Z80	REFRESH*
8085	Provided by controller on another card
8080	
6800	
6809	

Example MCSYNC*

PROCESSOR	SIGNAL PIN 38
8080	SYNC
8085	ALE (Address Latch Enable)
Z80	(RD+WR+INTAK)
6800	02*
6809	02*

- STATUS 1* - Pin 39 - Status Control Line 1
- STATUS 0* - Pin 40 - Status Control Line 0
  Status control lines provide timing information related to special machine cycle operations. Where specifically available, STATUS 1* is considered to be a signal to identify instruction fetch.

PROCESSOR	STATUS 1*	STATUS 0*
8080	M1	—
8085	S1	SO
Z80	M1	—
6800	—	VMA
6809	LIC	—

- BUSAK* - Pin 41 - BUS Acknowledge
  Normally an active-low output line from all processors. The controlling processor responds to a BUSRQ* by releasing the BUS and giving an acknowledge signal on the BUSAK* line. BUSAK* normally occurs at the completion of the current machine cycle.

  In complex systems this line can be an input, an output or it may be bidirectional, depending on the supporting hardware.
- BUSRQ* - Pin 42 - BUS Request
  Normally an active-low input line to all processors. A BUSRQ* causes the controlling processor to suspend operations on the BUS by releasing all 3-state BUS lines for use by another processor. Normally the BUS is released once the current machine cycle is completed.

  In complex systems this line can be an input, an output or it may be bidirectional, depending on the supporting hardware.
- INTAK* - Pin 43 - Interrupt Acknowledge
  An active-low output line from the Processor card that occurs in response to (INTRQ*). It is used to tell the interrupting device that the processor card is ready to respond to the interrupt. For vectored interrupts the vector address is placed on the data bus by the interrupting device during INTAK*.
- INTRQ* - Pin 44 - Interrupt Request
  An active-low processor card input line that conditionally interrupts the program. It is masked and ignored by the Processor unless deliberately enabled by a program instruction. If the Processor accepts the interrupt, it usually acknowledges by dropping INTAK* (Pin 43). Other actions depend on the specific Processor type, interrupt-related program instructions and hardware support of the interrupt mechanism.
- WAITRQ* - Pin 45 - Wait Request
  An active-low input line to the processor that suspends processor operations as long as it remains low. Normally the processor will hold in a state that maintains a valid address on the address bus.
- NMIRQ* - Pin 46 - Non-Maskable Interrupt
  An active-low processor card interrupt input line of highest priority.
- SYSRESET* - Pin 47 - System Reset
  An active-low output from the system reset circuit. The system reset circuit is triggered by power-on detection or by the pushbutton reset. The system reset bus line should be applied to all cards on the bus that have latch circuits requiring initialization.
- PBRESET* - Pin 48 - Push Button Reset
  An active-low input line to the system reset circuit.
- CLOCK* - Pin 49 - Clock from Processor
  A buffered processor clock signal used for system synchronization or as a general clock source.
- CNTRL* - Pin 50 - Control
  An auxiliary circuit for special clock timing. It may be a multiple of the processor clock signal, a real time clock signal or an external clock input to the processor.

- PC0 - Pin 51 - Priority Chain Out
- PC1 - Pin 52 - Priority Chain In
  A priority "daisy chain" bus with a priority chain "in" and a priority chain "out". This is a card slot dependent interrupt structure.

AUXILIARY POWER BUS - PINS 53-56

The Auxiliary Power bus provides interconnection for supplemental voltages.

- AUX GND - Pins 53 &54
  The ground or return bus for auxiliary power. These pins are bussed together for extra capacity.
- AUX +V - Pin 55
  Auxiliary positive voltage line (+12V).
- AUX -V - Pin 56
  Auxiliary negative voltage line (-12V).

GENERAL SPECIFICATIONS

The STD BUS definition includes physical parameters which are an inherent part of the STD BUS specification.

STD BUS cards must meet the mechanical and electrical specifications detailed, in the following pages, over the card's specified temperature range.

MECHANICAL SPECIFICATIONS

The STD BUS circuit card size and outline are defined by Figure 1-5 and Figure 1-7. The dimensions exclude the card ejector and I/O interface connections. Additional card length is allowed for I/O edge connector interfacing as defined in Figure 1-5.

STD CARD DIMENSIONS	INCHES		CENTIMETERS	
	NOMINAL	TOLERANCE	NOMINAL	TOLERANCE
Card Length	6.500	±.025	16.510	±.063
Card Height	4.480	±.0050	11.380	±.0127
Plated Board Thickness	0.062	±.003	0.158	±.008
Card Spacing	0.500	MIN	1.27	MIN
Added Length for I/O Edge Connector	0.400	±.025	1.016	±.063

Figure 1-5 STD Card Dimensions

Minimum card spacing requires consideration for component height, lead protrusion and card clearance in addition to the board thickness. Figure 1-6 gives recommended dimensions for these parameters but tradeoffs can be made between component height and lead protrusion. Cards not meeting these requirements may require multiple card slot positions.

RECOMMENDED DIMENSIONS FOR MINIMUM CARD SPACING	INCHES		CENTIMETERS	
	MAXIMUM	MINIMUM	MAXIMUM	MINIMUM
Component Height	0.375	—	0.952	—
Component Lead Protrusion ⚠1	0.040	—	.102	—
Adjacent Card Clearance	—	0.010	—	.025

⚠1 The card ejector occupies the top 1.4" (3.56 cm) of the card and protrudes 0.1" (0.254 cm) on each side of the card.

Figure 1-6 Profile Dimensions For Minimum Spacing

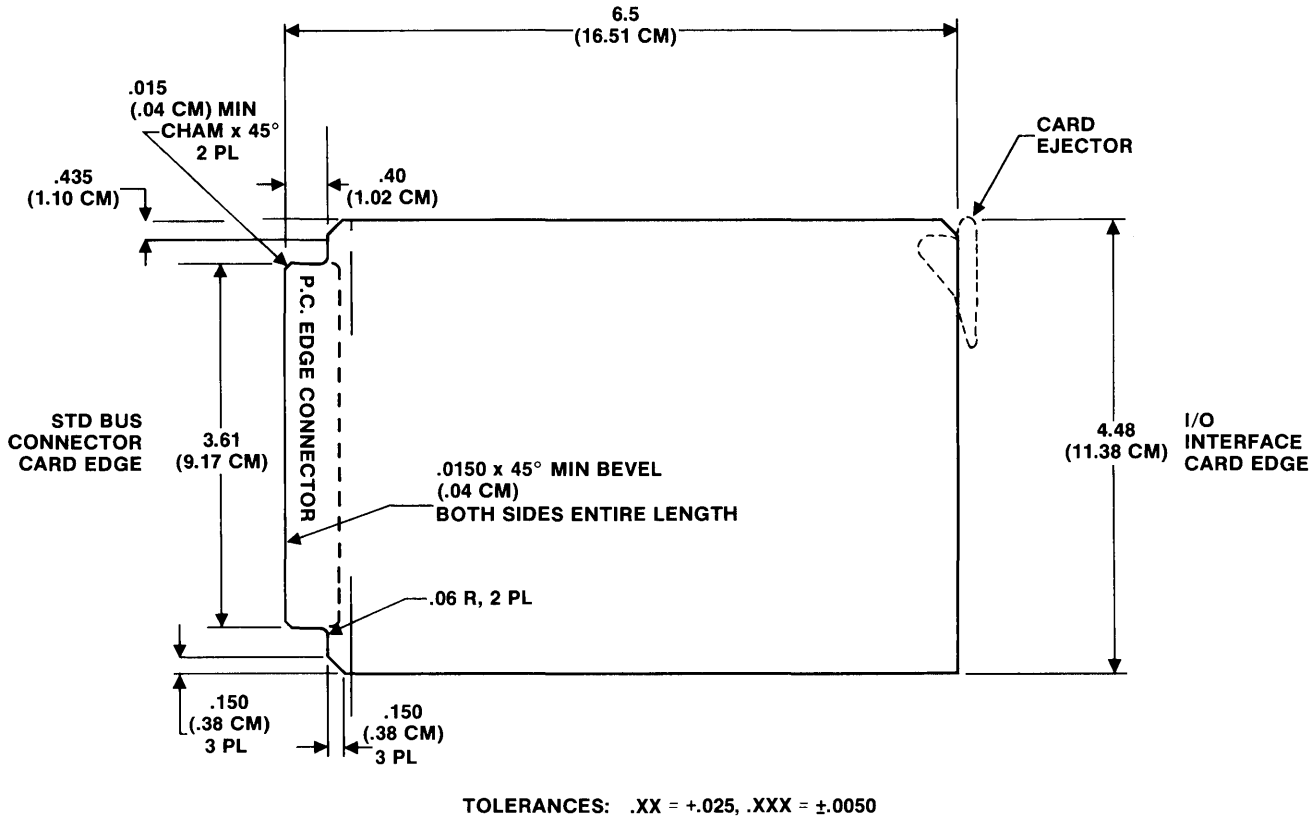


Figure 1-7A Standard Card Outline

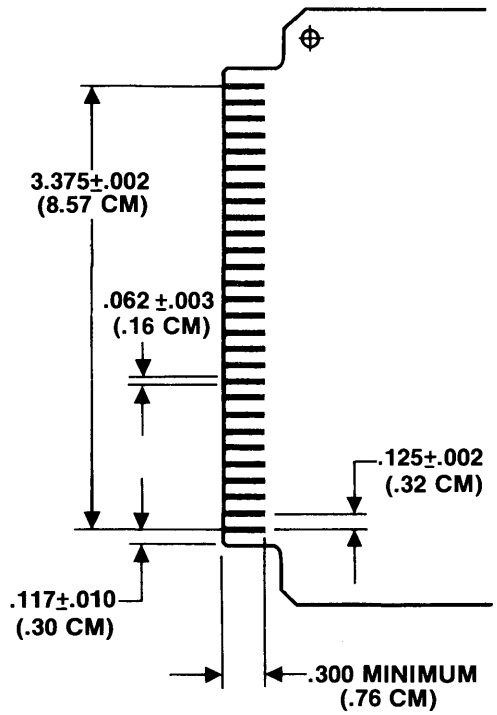


Figure 1-7B Recommended Edge Card Finger Design

ELECTRICAL SPECIFICATIONS

These specifications will assure power supply and logic level compatibility among STD BUS cards.

ABSOLUTE MAXIMUM RATINGS:

The following specifications are the STD BUS card edge connector pin maximum ratings. They are not recommended operating conditions. Above these values damage to card components is possible. The specific voltage at which damage will occur is component dependent.

PARAMETER	LIMIT	REFERENCE
Positive voltage applied to a logic input or disabled 3-state output	+5.5 Volts	GND pins 3, 4
Negative DC voltage applied to a logic input or disabled 3-state output	-0.4 Volts	

Figure 1-8 Electrical Ratings

Note:

Unless otherwise specified, the removal of STD BUS compatible circuit cards or their components parts from sockets is not recommended while operating voltages are applied.

POWER BUS VOLTAGE TOLERANCES

STD BUS cards normally require +5V for logic operation. Other operating voltages may be needed according to individual card function and device types. The table below shows the STD BUS power busses and voltage values. Note that these voltage values are specified at the card pins, not the back plane traces.

CARD PIN	SUPPLY VOLTAGE	TOLERANCE	REFERENCE
1, 2	+5V (VCC)	±0.25 Volts	GND pins 3, 4
5, 6	-5V (VBB)	±0.25 Volts	GND pins 3, 4
55	AUX +V (+12)	±0.5 Volts	AUX GND pins 53, 54
56	AUX -V (-12V)	±0.5 Volts	AUX GND pins 53, 54

Figure 1-9 Power Voltages and Tolerances

LOGIC SIGNAL CHARACTERISTICS

The STD BUS is designed for compatibility with industry standard TTL logic. These specifications apply over the STD BUS specified temperature range.

STD BUS CARD PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{OH} High-state output voltage	VCC=MIN V_{IH}=2V V_{IL}=0.8V I_{OH}=-15mA	2.4	—	Volts
V_{OL} Low-state output voltage	VCC=MIN V_{IL}=0.8V V_{IH}=02V I_{OL}=24mA	—	0.5	Volts
V_{IH} High-state input voltage		2.0	—	Volts
V_{IL} Low-state input voltage		—	0.8	Volts
T_R, T_F Risetime, Falltime		4	100	ns

Figure 1-10 STD BUS Logic Levels

STD UNIT LOADS

The unit load is a convenient method for specifying the input loading and output drive capability of STD BUS cards. In STD BUS systems one unit load is equal to one LSTTL load as follows:

Maximum high level input current: 20 μA
Maximum low level input current: -400 μA

The STD BUS unit load reflects input current requirements at worst-case conditions over the recommended supply voltage and ambient temperature ranges. An output rated at 60 unit loads can drive 60 STD BUS cards having inputs rated at one unit load.

RECOMMENDED BUS DRIVERS & RECEIVERS

Bus Drivers - 74LS240, 74LS241, 74LS244, 74LS373, 74LS374

Bus Receivers - 74LS240, 74LS241, 74LS244

Bus Transceivers - 74LS242, 74LS243, 74LS245

Section 2

Common Specifications for Series 7000 STD BUS Microprocessor Cards

INTRODUCTION

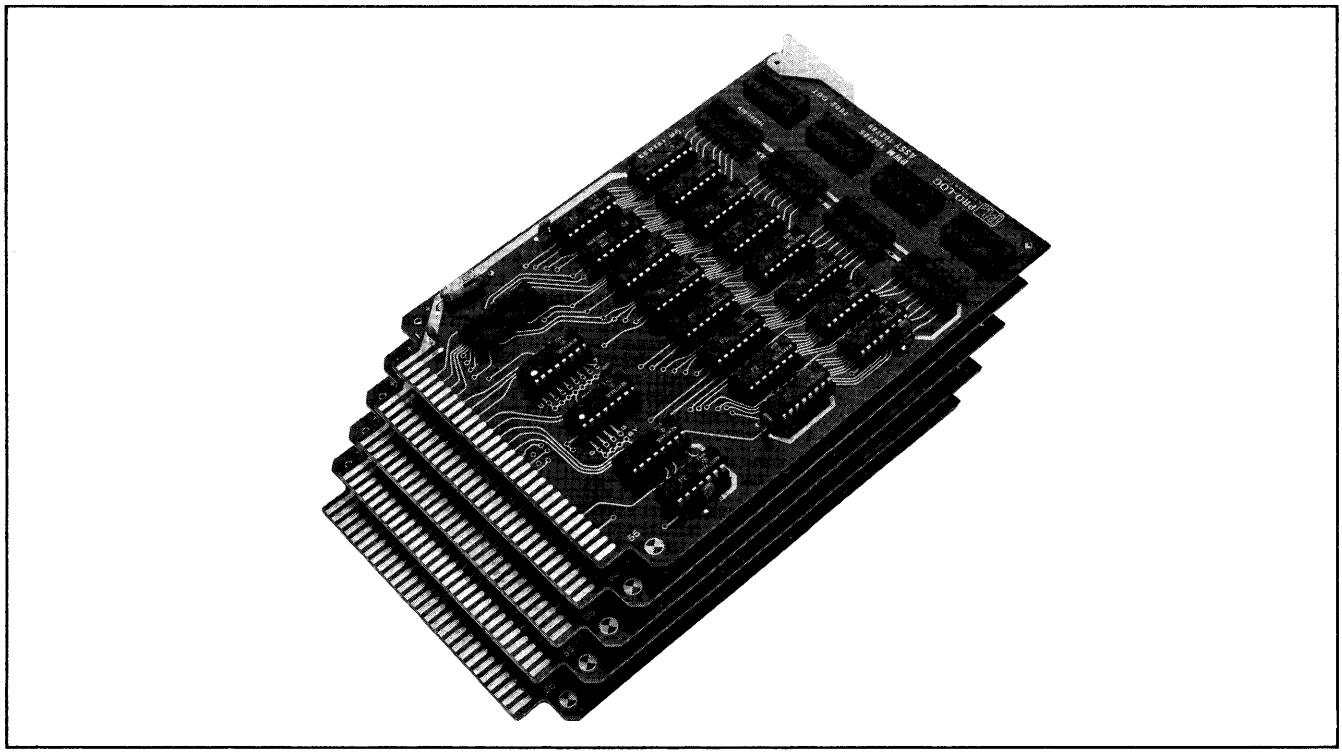
This section contains specifications common to the Series 7000 cards. These specifications, combined with the STD BUS specifications and the individual card data sheets, fully specify each card. Configuring the hardware for a Series 7000 STD BUS system simply requires the defining of the memory size and the number and type of I/O lines needed for the application, together with the selection of the appropriate card rack and special cards. Mapping of the memory and I/O is preassigned, change may be incorporated by moving jumper wire.

This section also contains the memory and I/O mapping information that is used with data sheets for the memory card address assignments and for the port address assignments (mapping).

Series 7000 cards combine high functional density with the design options needed for efficient system partitioning.

Series 7000 comprises a wide range of modular microprocessor system elements, including Processor, Memory cards, I/O cards, motherboards, card racks, utility cards and power supplies. The cards are divided into the following categories:

7100 System Support Cards (non-4½"x6½") including Motherboards
7300 Peripheral Interface
7400 Analog I/O
7500 Industrial I/O
7600 Digital (TTL) I/O
7700 Memory
7800 Processors
7900 Utility (extenders, blanks, prototyping aids, etc.)



Series 7000

MECHANICAL SPECIFICATIONS

The Series 7000 cards conform to the STD BUS standards, with the following additional requirements, including those shown in Figure 2-1.

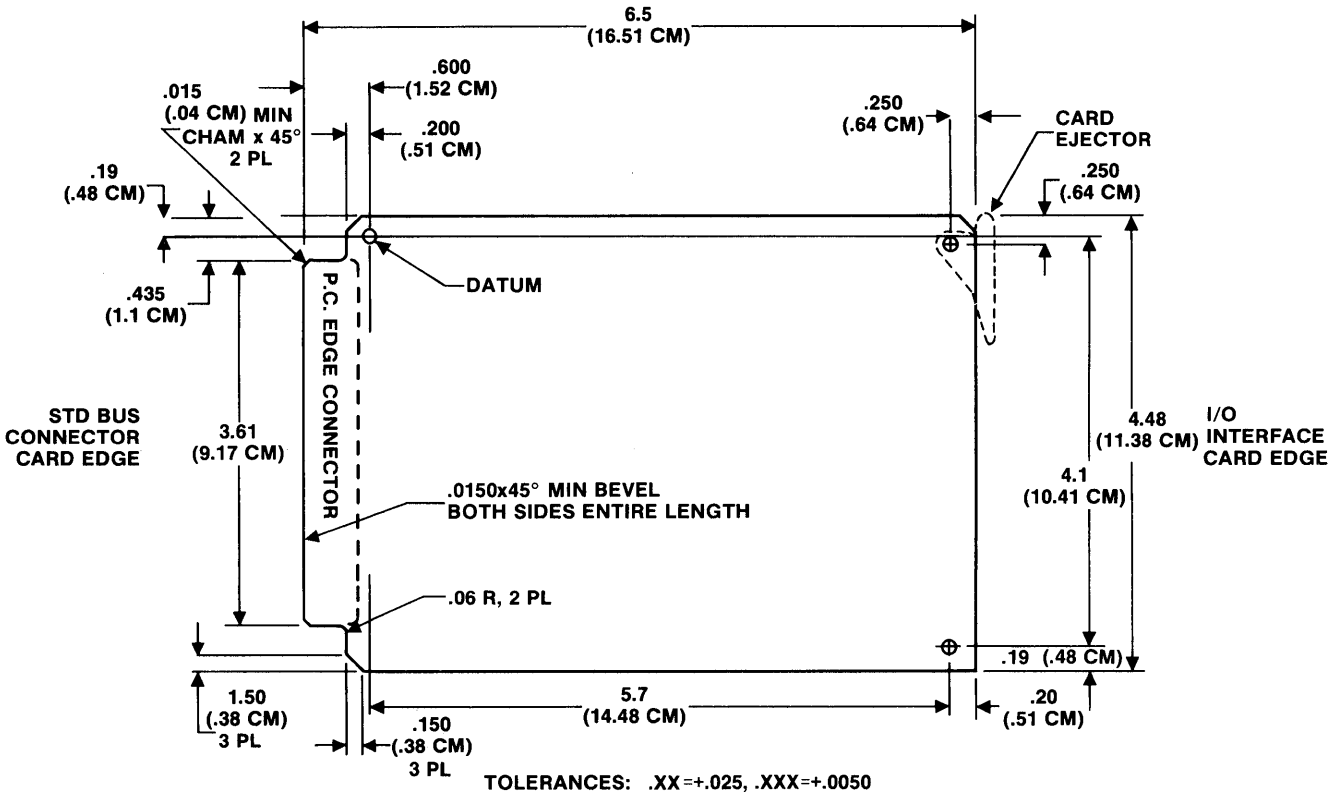


Figure 2-1A Series 7000 STD BUS Standard Card Outline

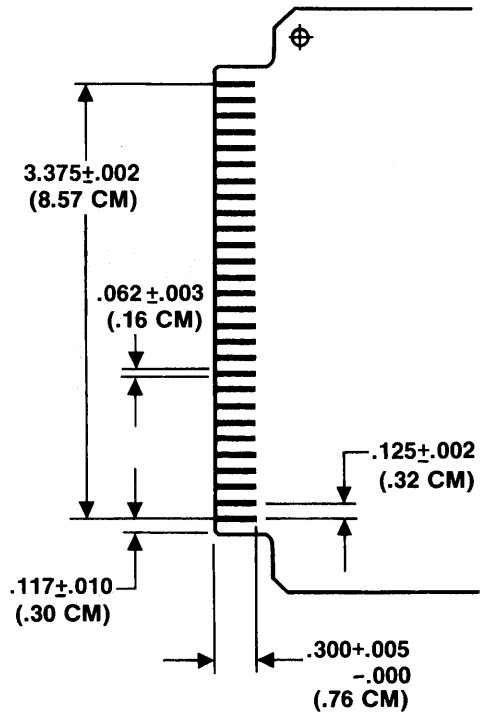


Figure 2-1B Series 7000 STD BUS Edge Card Finger Specifications

MATERIALS

The card base material is blue type FR4 laminated epoxy glaze with UL-94-V0 rating. Dual-sided cards have the equivalent of 2 ounces of copper per side, which is 2.4 mils thick, minimum. Edge connector fingers are copper with gold (0.03 mil) over nickel (0.1 mil) in accordance with MIL-G-45204.

SOCKETS

All integrated circuits on Series 7000 cards are socketed for ease of maintenance. Socketed ICs also allow for rapid insertion for PROM program development, plug-in of system test programs and expansion of system RAM memory.

CARD ADDRESSING OPTIONS

User addressing options are made by a jumper selection on all Processor Memory and I/O cards. These cards have jumper pads adjacent to on-card decoder sockets which allow the user to permanently change the address of the card and on-card elements such as memory chips and ports.

For jumper selection refer to the appropriate Memory or I/O Address Decoder Schematics and corresponding Address Map and Jumper Selection tables provided later in this section.

TEMPERATURE SPECIFICATION

Pro-Log's Series 7000 microprocessor card systems are designed to meet STD BUS specifications over the temperature range 0°C to 55°C ambient.

ELECTRICAL SPECIFICATIONS

Low-power Schottky (LSTTL) support logic and buffering are used to give the cards low input loading and low power consumption, without sacrificing speed or output drive capability. Most cards use LSTTL buffers with 200 mV of hysteresis for noise immunity.

The Series 7000 cards meet the following STD BUS specifications of Section 1: Absolute Maximum Ratings, Power Supply Voltages, Logic Signal Characteristics, Standard Bus Unit Loads.

One STD load or drive unit is equivalent to the 74LSXX unit load or drive as defined in Section 1.

Series 7000 cards have been divided into two sets of drive and loading specifications in accordance with the following categories:

7800 Processor Cards
Memory and I/O Cards

The 7800 Processor cards have 4.7K pullup resistors for each logic input and output. These pullups provide enhanced noise immunity and facilitate system testing. They pull the lines up to the +5V supply when the 3-state drivers are disabled. The pullups slightly reduce the 7800 Processor card's output drive capability and increase the input loading compared to the other card categories.

To determine the number of STD BUS cards possible in a system, first total the number of LSTTL input loads (STD unit loads) on each bus line. Then every output driver on the same line must be capable of driving at least that number of loads. This assures system operation over the worst-case combination of voltage tolerance and ambient temperature.

VCC = +5V ± 5%, TA = 0-55°C

PARAMETER	CARD TYPE	MIN	MAX	UNITS
INPUT LOADING	7800 Processor cards	—	4	LSTTL Loads
	Memory & I/O Cards	—	1	
OUTPUT DRIVE	7800 Processor Cards	55	—	LSTTL Loads
	Memory & I/O Cards	60	—	
OUTPUT 3-STATE LEAKAGE	7800 Processor Cards (with 4.7K pullups)	—	4	LSTTL Loads
	Memory & I/O Cards	—	1	

Figure 2-2 Series 7000 Card Drive And Loading

SERIES 7000 STD BUS TIMING

The 7800 Processor card generates all Processor and STD BUS timing in normal operation (unless a DMA-related operation has caused the Processor card to relinquish the system bus). The Processor card implements the capability of the microprocessor chip and interfaces it to the STD BUS with the minimum alteration of the chip's characteristics. The timing characteristics of a 7800 Processor card are essentially those of the microprocessor itself with added delays due to buffering.

Unless otherwise specified on individual data sheets, the following propagation delays apply between the 7800 Processor card edge signal pins and the microprocessor chip pins:

VCC = +5V, TA = 25°C

PARAMETER	MAX	UNITS	CONDITIONS
Buffer delay, input to output	20	ns	50 pF, 700 Ω
3-state driver enable	30	ns	50 pF, 700 Ω

Figure 2-3 Processor Card Buffer Timing

With the above delays added, timing information for 7800 Processor cards is available from the microprocessor manufacturer's data sheet specification.

Multilevel gating is sometimes required on the Processor card to produce STD BUS control signals that are not directly available from the microprocessor. Section 1 gives examples of how these signals may be derived for existing microprocessors. Refer to the processor card schematic and IC manufacturer's data sheets for exact delays.

SERIES 7000 MEMORY CARD TIMING

Series 7000 cards are designed to communicate over the STD BUS backplane in any combination without user timing considerations. The following information is provided to accommodate the use of pin compatible memory chip variations which can be used in the Series 7000 memory cards.

Figure 2-4 shows the functional blocks of the 7700 Memory cards. The delays contributed by these blocks are added to the memory chip delays and access times to determine the AC characteristics of the card. The table in Figure 2-5 gives maximum propagation delays for the memory card. For exact delays use the IC manufacturer's data sheets and the appropriate schematics.

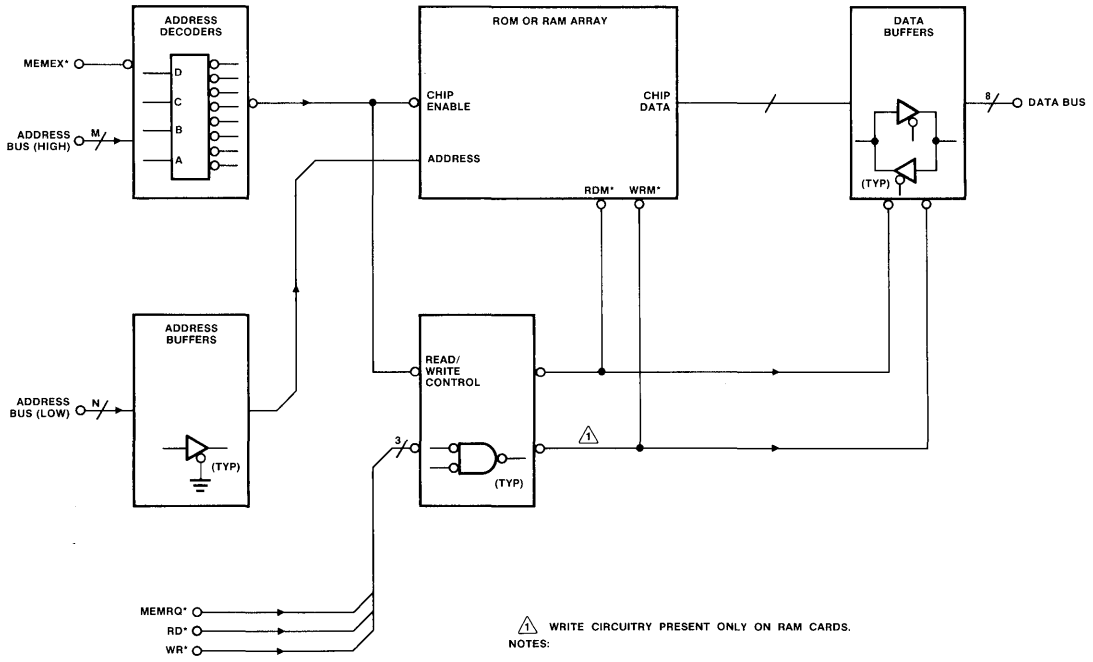


Figure 2-4 Memory Card Functional Blocks

VCC = +5V, TA = 25°C

CIRCUIT	PROPAGATION DELAY			LOAD CONDITIONS	
	FROM	TO	T_{PD} MAX	CL	RL
ADDRESS DECODERS	ADDRESS BUS OR MEMEX*	MEMORY CHIP ENABLE OR READ/WRITE ENABLE	75 ns	15 pF	—
ADDRESS BUFFERS	ADDRESS BUS	MEMORY CHIP ADDRESS	35 ns	160 pF	—
DATA BUFFERS	MEMORY CHIP DATA (OUT)	DATA BUS	20 ns	45 pF	4.7KΩ
	DATA BUS	MEMORY CHIP DATA (IN)	25 ns	80 pF	—
	READ WRITE CONTROL	VALID OUTPUT ENABLE	30 ns	100 pF	4.7KΩ
READ WRITE CONTROL	DECODER OUTPUT RD*, WR*, OR MEMRQ*	RDM* OR WRM* (RAMs ONLY)	70 ns		

Figure 2-5 Generalized Maximum Delays For Memory Cards

For example, the 2114 RAM chip's specified Data Read access time from an address change (A0-A9) is 450 ns. In the 7701 this is increased by the address buffers (35 ns) and data buffers (20 ns) to 505 ns. In this case the decoding of A10-A15 and the Data Bus buffer control are presumed to occur during the RAM data access time.

TTL INPUT/OUTPUT CARD TIMING

I/O Port read and write operations are under program control and occur in multiples of the Processor's time state as defined by the instruction set. Input Ports are addressable 3-state buffers which, when selected, drive the STD BUS Data Buffer. Output Ports are addressable D type latches which, when selected, copy the STD BUS data and latch it at the rising edge of WR*.

The following table provides timing information relative to the rising edge of RD* and WR* control lines. This information fully defines the TTL I/O Port timing since the following assumptions can be made:

IORQ*, IOEX*, DATA & ADR are all stable for more than 150 ns prior to RD* or WR* rising and that RD* and WR* are active low for more than 150 ns.

VCC = +5V, TA = 25°C

	PARAMETER	MIN	MAX	UNITS
T_{OD}	Output Delay: Output port line valid after WR* rises CL=15 pF	—	60	ns
T_{ID}	Input Delay: STD DATA BUS stable after input Data stable CL=50 pF	—	40	ns
T_H	Input Hold Time: Input port data valid after RD* rises	0	—	ns

Figure 2-6 TTL Input/Output Port Timing

MAPPING

Each class of Series 7000 cards are mapped at a different address to minimize the need for the users to remap cards. The standard mapping that follows is recommended since software availabe in the future from Pro-Log will utilize this standardized mapping scheme.

All memory cards can be mapped to cover the full 64K memory space and can be bank enabled. All I/O cards decode the lower 8 bits and ports can be mapped anywhere in the 256 Port field without using the I/O expansion pin for port bank switching.

STANDARD SERIES 7000 STD BUS MAPPING

The following is the standardized mapping scheme for the Series 7000 cards. The center column gives the mapped address of the first port or memory location on the card. The remainder of the ports or memory locations are consecutive from that point. The second column gives the recommended address locations for additional mapping of the same type of cards.

CARD TYPE	CARD MAPPED AT HEX PORT ADDRESS	ASSIGNED HEX ADDRESS SPACE FOR SYSTEM EXPANSION
7100 & 7200	NA	NA
7300 Peripheral Interface	C0	C0-CF
7400 Analog I/O	80	80-BF
7500 Industrial I/O	40	40-7F
7600 TTL I/O	00	00-3F
Non-Specified Types	D0	D0-FF

Figure 2-7 Standard I/O Card Mapping

CARD TYPE 7700 MEMORY	CARD MAPPED AT HEX MEMORY PAGE	ASSIGNED HEX ADDRESS SPACE FOR SYSTEM EXPANSION
RAM	80	16K space not used by CPU or 16K ROM Card (1)
ROM	40	16K space not used by CPU or 16K RAM Card (1)

(1) An additional 16K space is available for second memory card without using memory expansion techniques.

Figure 2-8 Standardized Memory Card Mapping

CPU TYPE	HEXADECIMAL ADDRESSES			
	CPU MEMORY	ROM/PROM	RAM	OPTIONAL
8085 & Z80	ROM 0000-1FFF (8K) RAM 2000-2FFF (4K) UNSUABLE 3000-3FFF (4K)	4000-7FFF (16K)	8000-BFFF (16K)	C000-FFFF (16K) (2)
6800 & 6809	ROM E000-FFFF (8K) RAM D000-DFFF (4K) UNUSABLE C000-CFFF (4K) I/O AT 0000-00FC	4000-7FFF (16K)	8000-BFFF (16K)	0000-3FFF (16K) (2)

(2) The Processor card's 12K onboard memory may also be disabled, allowing an external 16K memory card to occupy the space assigned.

Figure 2-9 Standardized Processor Card On Board Memory Mapping

MEMORY MAP

To facilitate memory mapping the following pages contain memory maps, each with an associated address decoding schematic for 1K, 2K & 4K memory blocks. Below each chart is an example of its use. This memory mapping information, and the associated data sheet, summarize the Series 7000 mapping configurations.

The data sheets give the address range to which each card is mapped when shipped. It also has each memory blocks appropriate integrated circuit U-numbers.

If the memory is to be mapped to another location the following procedure is recommended:

1. Find the appropriate memory address map and schematic as referenced on the data sheet.
2. Find the Hexadecimal address range on the appropriate map and determine from the right hand column of the Memory Address Map and Jumper Selection Table which decoder outputs require jumpers.
3. Remove the Jumper (S) shown on the data sheet and solder in bus wire at the newly selected jumper locations.
4. Install memory devices.

The memory card is now mapped and ready for use.

CARD TYPE 7700 MEMORY	CARD MAPPED AT HEX MEMORY PAGE	RESERVED HEX ADDRESS SPACE FOR SYSTEM EXPANSION
RAM	80	16K space not used by CPU or 16K ROM Card ⚠1
ROM	40	16K space not used by CPU or 16K RAM Card ⚠1

⚠1 An additional 16K space is available for a second memory card without using memory expansion techniques.

Figure 2-10 Standardized Memory Card Mapping

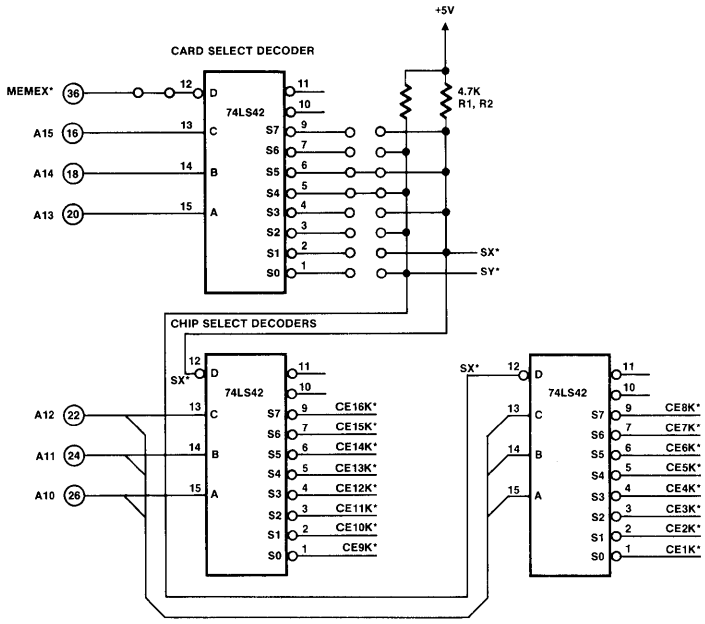


Figure 2-11A Address Decoder & Schematic For 1K Memory Blocks (16K Memory Card)

64K Address Map (A0-A15)

PAGE XX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	A15	A14	A13	A12	JUMPER SELECT TO X, Y
0 X	MB0				MB1				MB2				MB3								S0 TO SY
1 X	MB4				MB5				MB6				MB7								
2 X	MB0				MB1				MB2				MB3								S1 TO SX
3 X	MB4				MB5				MB6				MB7								
4 X	MB0				MB1				MB2				MB3								S2 TO SY
5 X	MB4				MB5				MB6				MB7								
6 X	MB0				MB1				MB2				MB3								S3 TO SX
7 X	MB4				MB5				MB6				MB7								
8 X	MB0				MB1				MB2				MB3								S4 TO SY
9 X	MB4				MB5				MB6				MB7								
A X	MB0				MB1				MB2				MB3								S5 TO SX
B X	MB4				MB5				MB6				MB7								
C X	MB0				MB1				MB2				MB3								S6 TO SY
D X	MB4				MB5				MB6				MB7								
E X	MB0				MB1				MB2				MB3								S7 TO SX
F X	MB4				MB5				MB6				MB7								
PAGE XX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	A15	A14	A13	A12	
A11																	PAGE ADDRESS				
A10																					
A9																					
A8																					

Figure 2-11B Memory Address Map & Jumper Selection Table For 1K Memory Block (16K Memory Cards)

Example:

To remap a 16K memory card with 1K memory blocks from 8000-8FFF to C000-FFFF simply move the jumpers as follows:

(S4-SY) to (S6-SY) & (S5-SX) to (S7-SX)

Figure 2-11 1K Memory Block Mapping Scheme

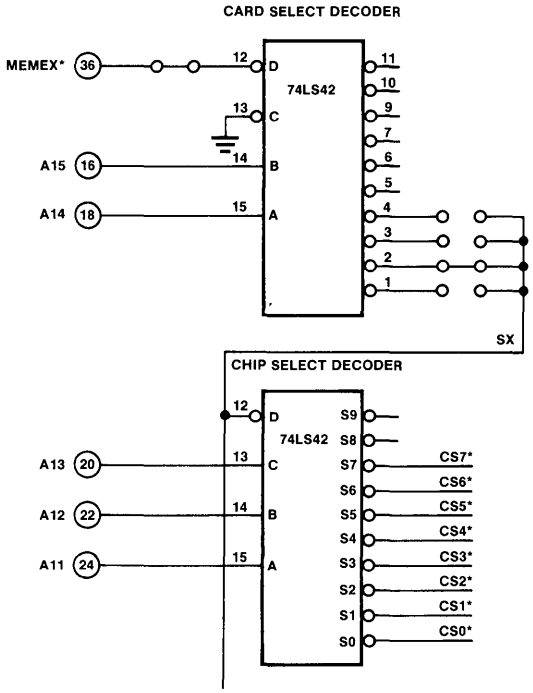


Figure 2-12A Address Decoder Schematic For 2K Memory Blocks (16K Memory Card)

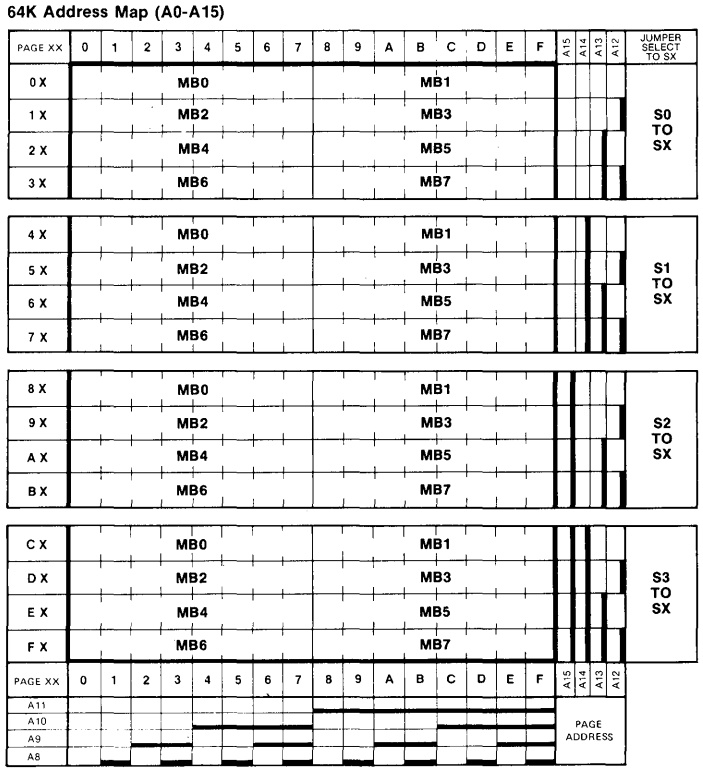


Figure 2-12B Memory Address Map & Jumper Selection Table For 2K Memory Block (16K Memory Cards)

Example:

To remap a 16K memory card with 2K memory blocks from 4000-7FFF to 8000-BFFF simply move jumper S1 to the S2 position.

Figure 2-12 2K Memory Block Mapping Scheme

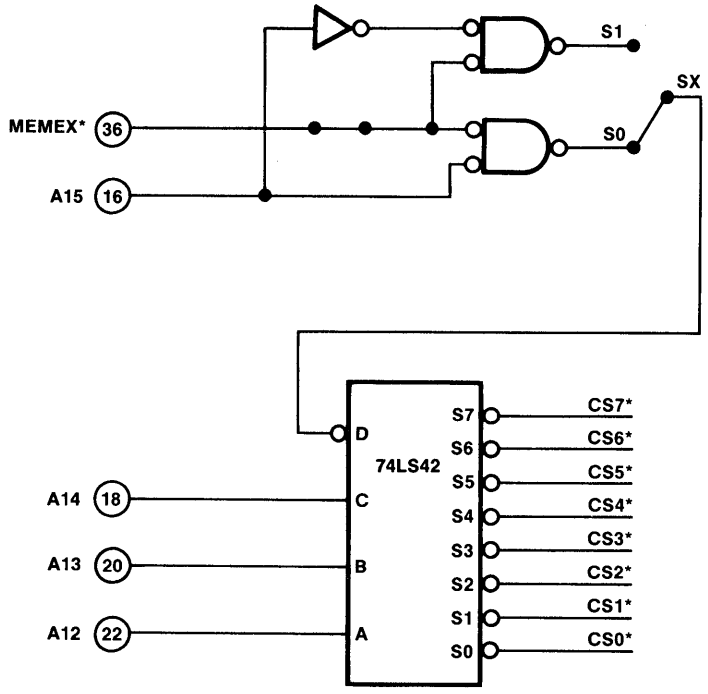


Figure 2-13A Address Decoder Schematic For 4K Memory Blocks (32K Memory Card)

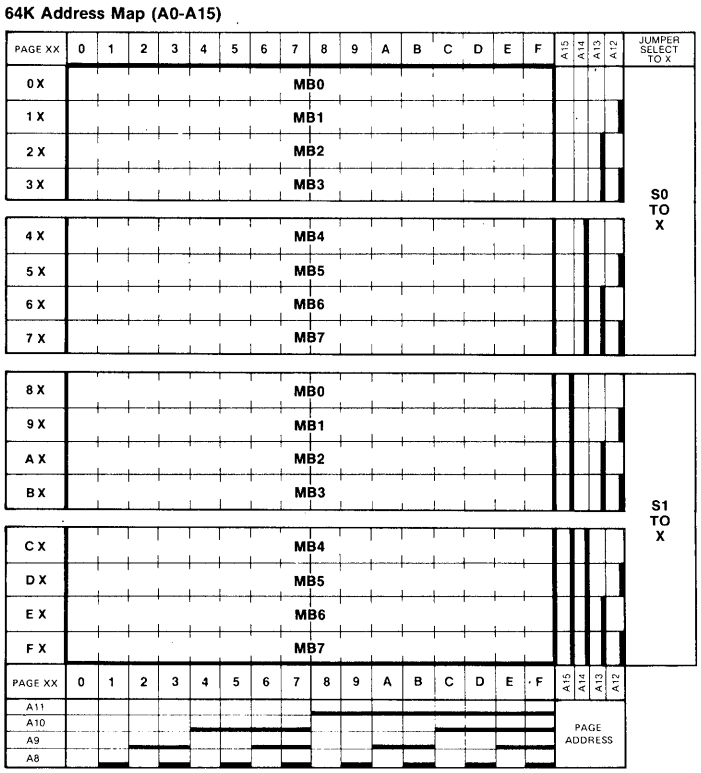


Figure 2-13B Memory Address Map & Jumper Selection Table For 4K Memory Block (32K Memory Cards)

Example:

To remap a 32K memory card with 4K memory blocks from 0000-7FFF to 8000-FFFF move jumper (S0-SX) to (S1-SX).

Figure 2-13 4K Memory Block Mapping Scheme

I/O MAP

To facilitate port mapping (address assignments), the following tables are provided together with associated decoder schematics and examples. This information, along with the appropriate data sheets, fully defines I/O mapping for Series 7000 cards.

These charts provide the most significant Hex address in the left hand column with the least significant Hex address across the top. The jumper selection is taken from the body of the table associated with the proper Hex address. The appropriate address decoder schematic and an example of the use of each chart is provided for each I/O decoder type.

If I/O remapping is required the following procedure is recommended:

1. Use the charts by determining how many I/O addresses will be used by the card in question. Remember that many of the boards use the same address for Input ports and Output ports. A card with 4 Input ports and 4 Output ports uses only 4 I/O addresses.
2. Find the schematic of the decoding logic that matches that number of port addresses. This logic is common to all boards that use that number of addresses. This schematic indicates the number of jumpers, denoted by X, Y and Z, needed to fully select the address block. However, not every card will require all three jumpers. The jumper locations are shown on the associated data sheets.
3. Find the Hexadecimal address range on the appropriate I/O Address Mapping Jumper Selection table.
4. Select the desired I/O port address block and consult the matrix of jumper configurations to determine which jumpers are required.
5. Remove the existing jumpers and insert jumpers at the new positions found in Step 4.

The I/O card is now mapped and ready for use.

Notice that the Series 7000 boards fully decode the Lower 8 address lines and are manufactured with the jumpers as follows:

CARD TYPE	CARD MAPPED AT HEX PORT ADDRESS	RESERVED HEX ADDRESS SPACE FOR SYSTEM EXPANSION
7100 & 7200	NA	NA
7300 Peripheral Interface	C0	C0-CF
7400 Analog I/O	80	80-BF
7500 Industrial I/O	40	40-7F
7600 TTL I/O	00	00-3F
Non-Specified Types	D0	D0-FF

Figure 2-14 Standard I/O Card Mapping

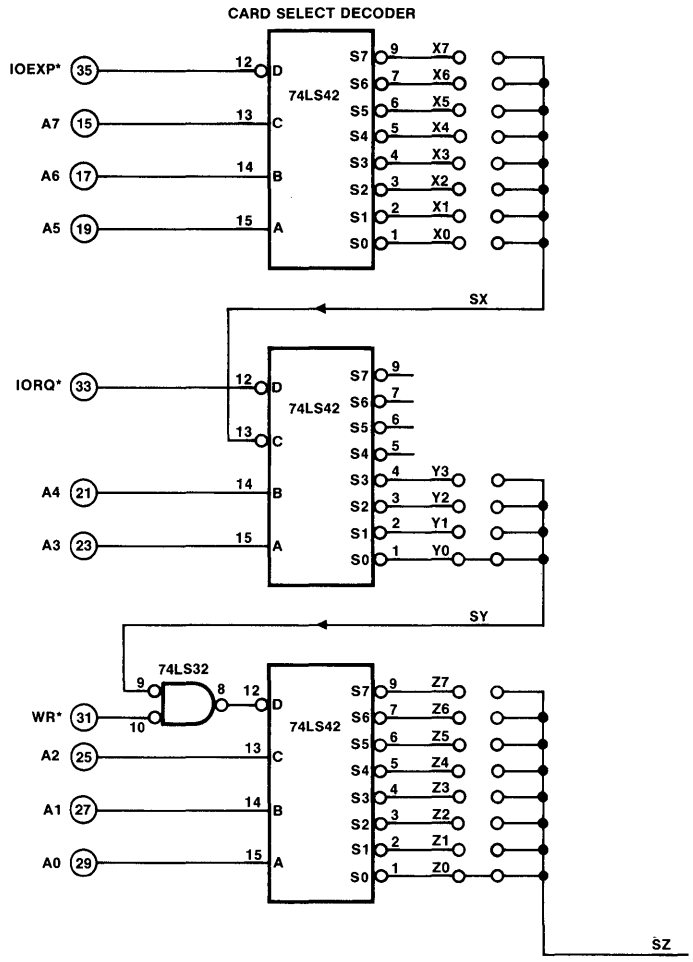


Figure 2-15A I/O Address Decoder And Schematic For 1 Address Per Card

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X, Y & Z
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	Z0	Z1	Z2	Z3	Z4	Z5	Z6	Z7	← Z
0	X0 Y0								X0 Y1								
1	X0 Y2								X0 Y3								
2	X1 Y0								X1 Y1								
3	X1 Y2								X1 Y3								
4	X2 Y0								X2 Y1								
5	X2 Y2								X2 Y3								
6	X3 Y0								X3 Y1								X
7	X3 Y2								X3 Y3								AND
8	X4 Y0								X4 Y1								
9	X4 Y2								X4 Y3								Y
A	X5 Y0								X5 Y1								
B	X5 Y2								X5 Y3								
C	X6 Y0								X6 Y1								
D	X6 Y2								X6 Y3								
E	X7 Y0								X7 Y1								
F	X7 Y2								X7 Y3								

Figure 2-15B I/O Address Mapping And Jumper Selection Table For 1 Address Per Card

Example:

To jumper a card to operate at I/O port address AB jumper pairs X5, Y1 and Z3.

Figure 2-15 Port Mapping Scheme 1 Address Per Card

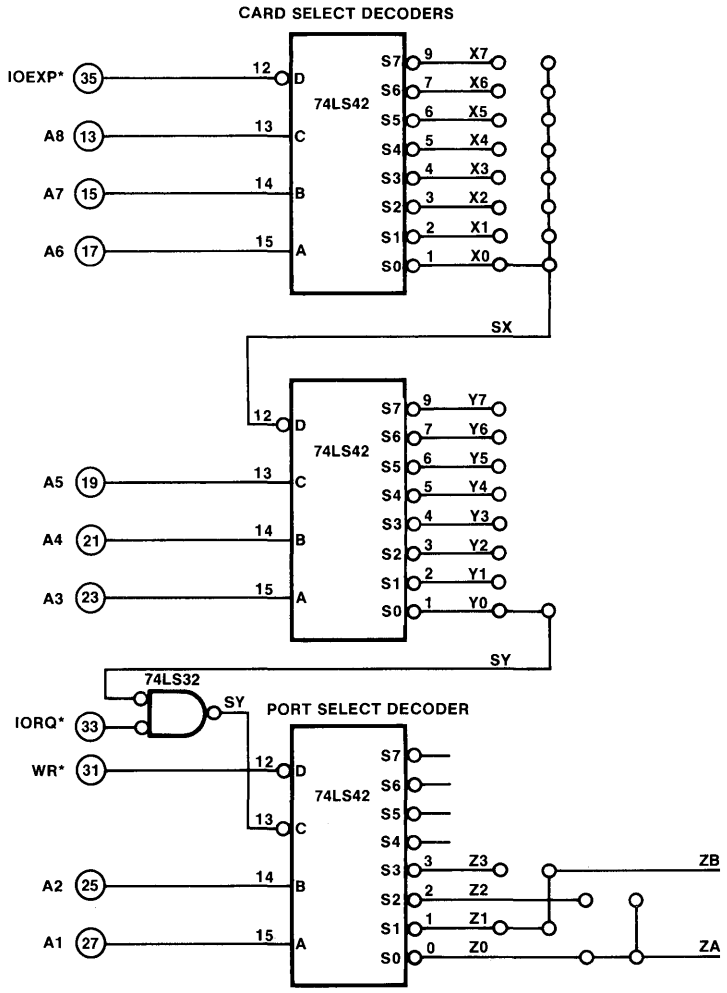


Figure 2-16A I/O Address Decoder And Schematic For 2 Addresses Per Card

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X, Y & Z
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
	Z0	Z1	Z2	Z3	Z0	Z1	Z2	Z3	Z0	Z1	Z2	Z3	Z0	Z1	Z2	Z3	← Z
0	X0			Y0	X0			Y1	X0			Y2	X0			Y3	X AND Y
1	X0			Y4	X0			Y5	X0			Y6	X0			Y7	
2	X1			Y0	X1			Y1	X1			Y2	X1			Y3	
3	X1			Y4	X1			Y5	X1			Y6	X1			Y7	
4	X2			Y0	X2			Y1	X2			Y2	X2			Y3	
5	X2			Y4	X2			Y5	X2			Y6	X2			Y7	
6	X3			Y0	X3			Y1	X3			Y2	X3			Y3	
7	X3			Y4	X3			Y5	X3			Y6	X3			Y7	
8	X4			Y0	X4			Y1	X4			Y2	X4			Y3	
9	X4			Y4	X4			Y5	X4			Y6	X4			Y7	
A	X5			Y0	X5			Y1	X5			Y2	X5			Y3	
B	X5			Y4	X5			Y5	X5			Y6	X5			Y7	
C	X6			Y0	X6			Y1	X6			Y2	X6			Y3	
D	X6			Y4	X6			Y5	X6			Y6	X6			Y7	
E	X7			Y0	X7			Y1	X7			Y2	X7			Y3	
F	X7			Y4	X7			Y5	X7			Y6	X7			Y7	

Figure 2-16B I/O Address Mapping And Jumper Selection Table For 2 Addresses Per Card

Example:

To jumper a card that uses two I/O port addresses to operate at addresses 32 and 33, connect jumper pairs X1, Y4 and also Z2 and Z3.

Figure 2-16 Mapping Scheme 2 Addresses Per Card Port

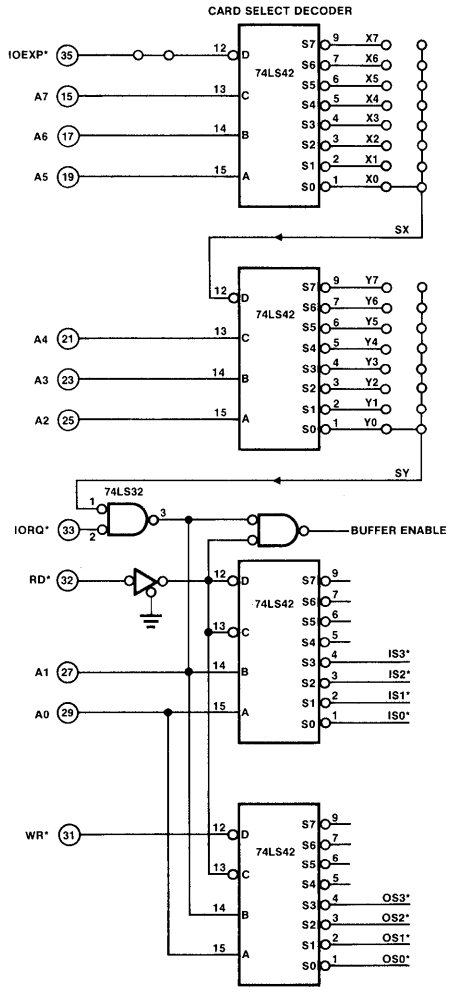


Figure 2-17A I/O Address Decoder And Schematic For 4 Addresses Per Card

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X & Y
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0				X0 Y1				X0 Y2				X0 Y3				X AND Y
1	X0 Y4				X0 Y5				X0 Y6				X0 Y7				
2	X1 Y0				X1 Y1				X1 Y2				X1 Y3				
3	X1 Y4				X1 Y5				X1 Y6				X1 Y7				
4	X2 Y0				X2 Y1				X2 Y2				X2 Y3				
5	X2 Y4				X2 Y5				X2 Y6				X2 Y7				
6	X3 Y0				X3 Y1				X3 Y2				X3 Y3				
7	X3 Y4				X3 Y5				X3 Y6				X3 Y7				
8	X4 Y0				X4 Y1				X4 Y2				X4 Y3				
9	X4 Y4				X4 Y5				X4 Y6				X4 Y7				
A	X5 Y0				X5 Y1				X5 Y2				X5 Y3				
B	X5 Y4				X5 Y5				X5 Y6				X5 Y7				
C	X6 Y0				X6 Y1				X6 Y2				X6 Y3				
D	X6 Y4				X6 Y5				X6 Y6				X6 Y7				
E	X7 Y0				X7 Y1				X7 Y2				X7 Y3				
F	X7 Y4				X7 Y5				X7 Y6				X7 Y7				

Figure 2-17B I/O Address Mapping And Jumper Selection Table For 4 Addresses Per Card

Example:

To jumper a 7601 card to operate at I/O port addresses 94, 95, 96, and 97, connect jumper pairs X4 and Y5.

Figure 2-17 Port Mapping Scheme 4 Addresses Per Card

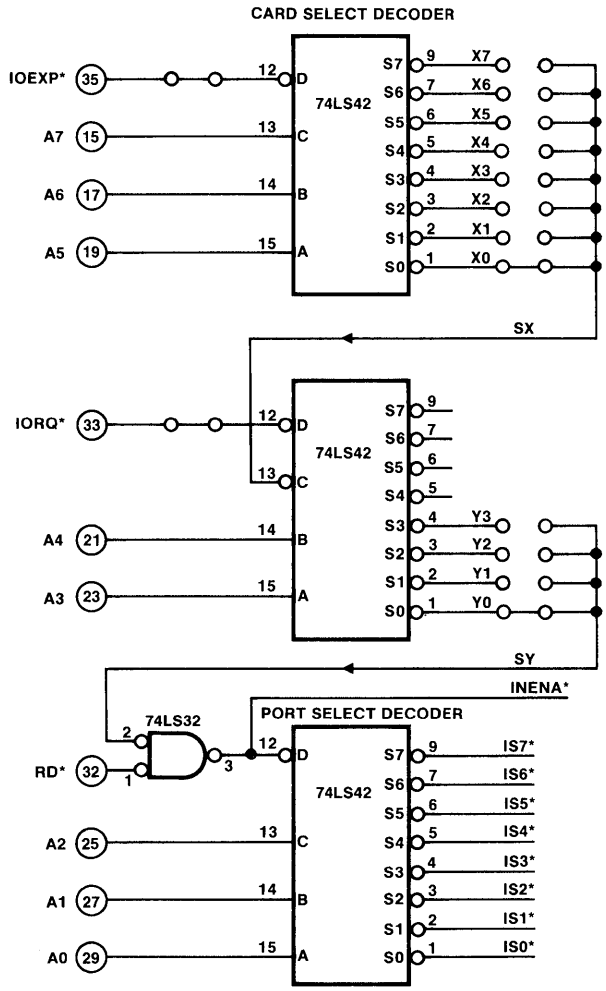


Figure 2-18A I/O Address Decoder And Schematic For 8 Addresses Per Card

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0								X0 Y1								X AND Y
1	X0 Y2								X0 Y3								
2	X1 Y0								X1 Y1								
3	X1 Y2								X1 Y3								
4	X2 Y0								X2 Y1								
5	X2 Y2								X2 Y3								
6	X3 Y0								X3 Y1								
7	X3 Y2								X3 Y3								
8	X4 Y0								X4 Y1								
9	X4 Y2								X4 Y3								
A	X5 Y0								X5 Y1								
B	X5 Y2								X5 Y3								
C	X6 Y0								X6 Y1								
D	X6 Y2								X6 Y3								
E	X7 Y0								X7 Y1								
F	X7 Y2								X7 Y3								

Figure 2-18B I/O Address Mapping And Jumper Selection Tables For 8 Addresses Per Card

Example:

To jumper a 7603 card to operate at I/O port addresses A0 through A7, connect jumper pairs X5 and Y0.

Figure 2-18 Mapping Scheme 8 Addresses Per Card Port

Section 3

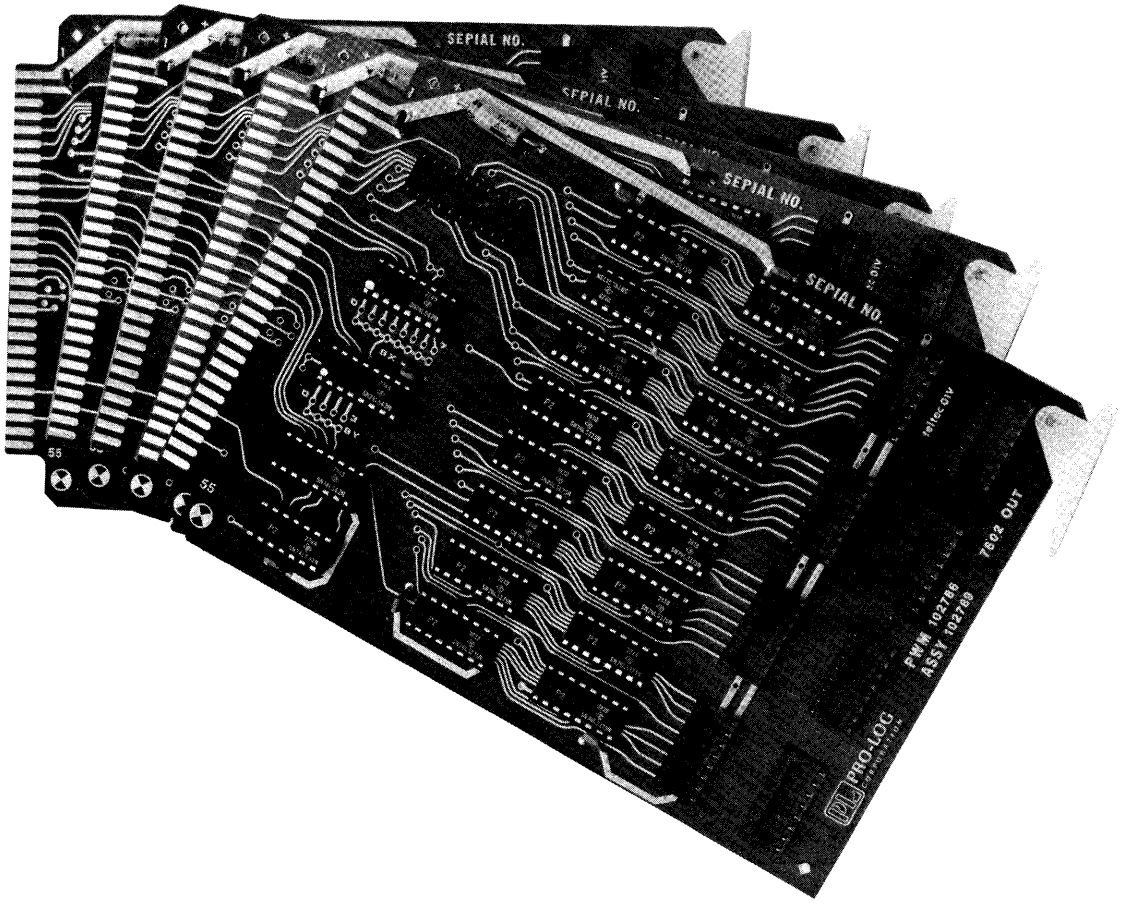
Series 7000 Data Sheets

INTRODUCTION

This section contains Series 7000 Data Sheets which give additional specifications and operating requirements for specific Series 7000 cards and accessories.

For convenience, the data sheets of the Series 7000 cards are arranged by function in the following sequence:

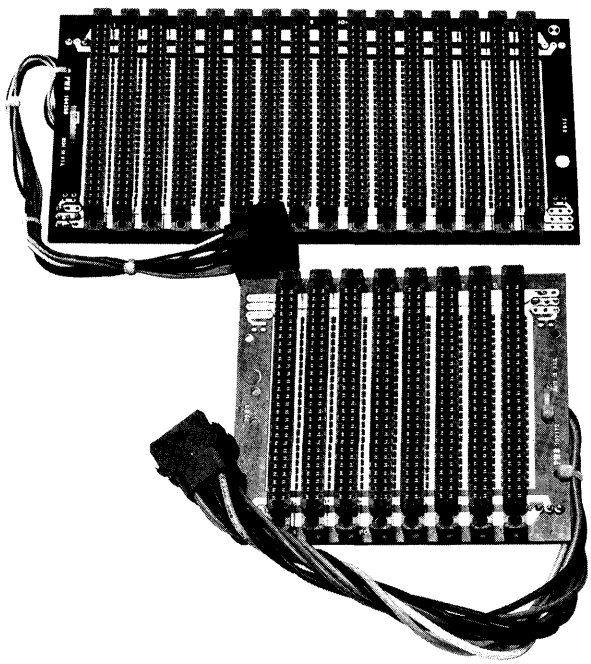
7100 System Support Cards (non - 4½"x6½")
7300 Peripheral Interface
7400 Analog I/O
7500 Industrial I/O
7600 Digital (TTL) I/O
7700 Memory
7800 Processors
7900 Utility (extenders, blanks, etc.)



7101, 7102 MOTHERBOARDS

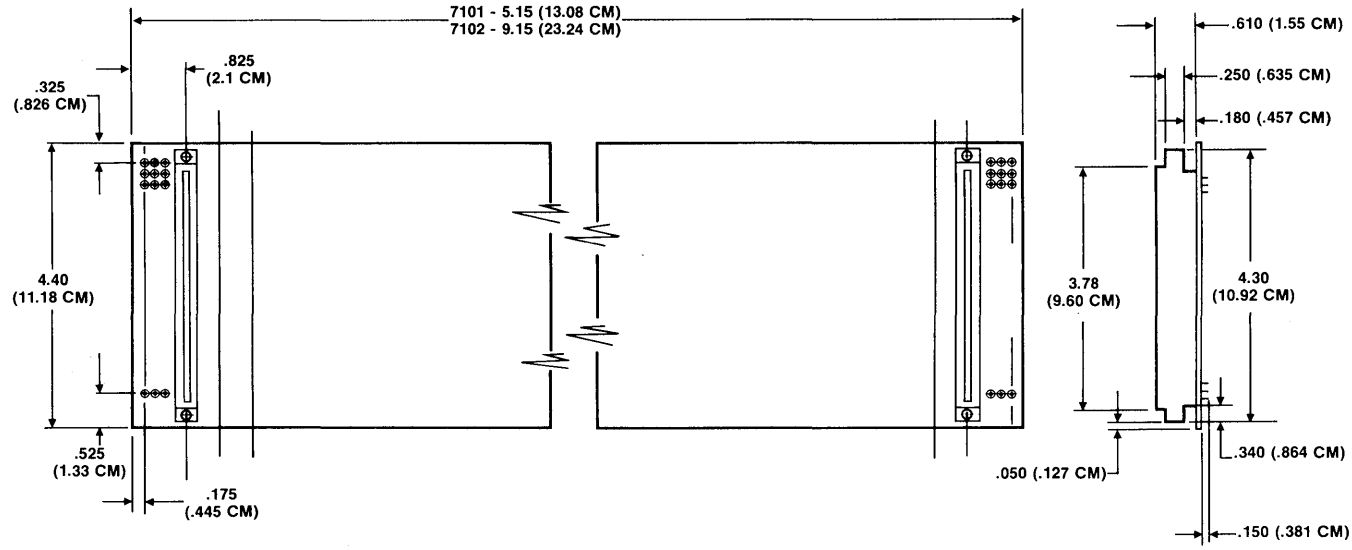
7101, 7102 MOTHERBOARDS

The 7101 and 7102 Motherboards implement the STD BUS backplane interconnection scheme, as defined by the STD BUS general specifications. They are available as single units or as an integral part of the CR8 and CR16 preassembled STD BUS card racks.



FEATURES

- **56-pin edge connectors and interconnect wiring for STD BUS microprocessor systems**
- **7101 provides 8 edge connectors on 0.5 inch centers**
- **7102 provides 16 edge connectors on 0.5 inch centers**
- **Power cable with 9-pin keyed and locking connector**
- **High current power distribution and logic bus traces**
- **Groundplane for reduced crosstalk and noise**



DIGITAL POWER TRACES

Pins 1 and 2 (VCC) are bussed together at each edge connector and to all edge connectors.

Pins 3 and 4 (Logic Ground) are bussed together at each edge connector and to all edge connectors and the groundplane.

Pin 5 (-VBB) and Pin 6 are separated and bussed pin-for-pin to each edge connector. These traces are not connected to the -VBB power harness. Jumper pads are provided for connection of traces to -VBB.

		7101	7102	
PARAMETER FOR TOTAL MOTHERBOARD		MAX	MAX	UNITS
I_{VCC}	VCC trace current (Pins 1 and 2) (10°C rise from 20°C)	17.0	17.0	Amps
I_{LG}	Logic Ground Trace (Pin 3 and 4) (10°C rise from 20°C)	17.0	17.0	Amps
I_{BB}	VBB current (Pin 5 or Pin 6) (10°C rise from 20°C)	1.0	1.0	Amp
R_{VCC}	VCC trace resistance (Pins 1 and 2) at 20°C	3	6	mΩ
R_{LG}	Logic ground trace resistance (Pin 3 and 4) at 20°C	3	6	mΩ
R_{BB}	VBB trace resistance (Pin 5 or 6) at 20°C	135	270	mΩ

LOGIC BUS TRACES

Pin 7 through 50 are bussed pin-for-pin to all edge connectors. Pins 51 and 52 (PC0 and PCI) are open across each edge connector.

		7101	7102	
PARAMETER FOR TOTAL MOTHERBOARD		MAX	MAX	UNITS
I_{LT}	Logic Trace Current (10°C rise from 20°C)	1.0	1.0	Amps
C_{LL}	Logic Trace to Logic Trace Capacitance (measured at 1.0 MHz)	13	25	pF
C_{LG}	Logic Trace to Logic Ground Capacitance (measured at 1.0 MHz)	25	50	pf
R_{LT}	Logic Trace Resistance at 20°C	135	270	mΩ

AUXILIARY POWER TRACES

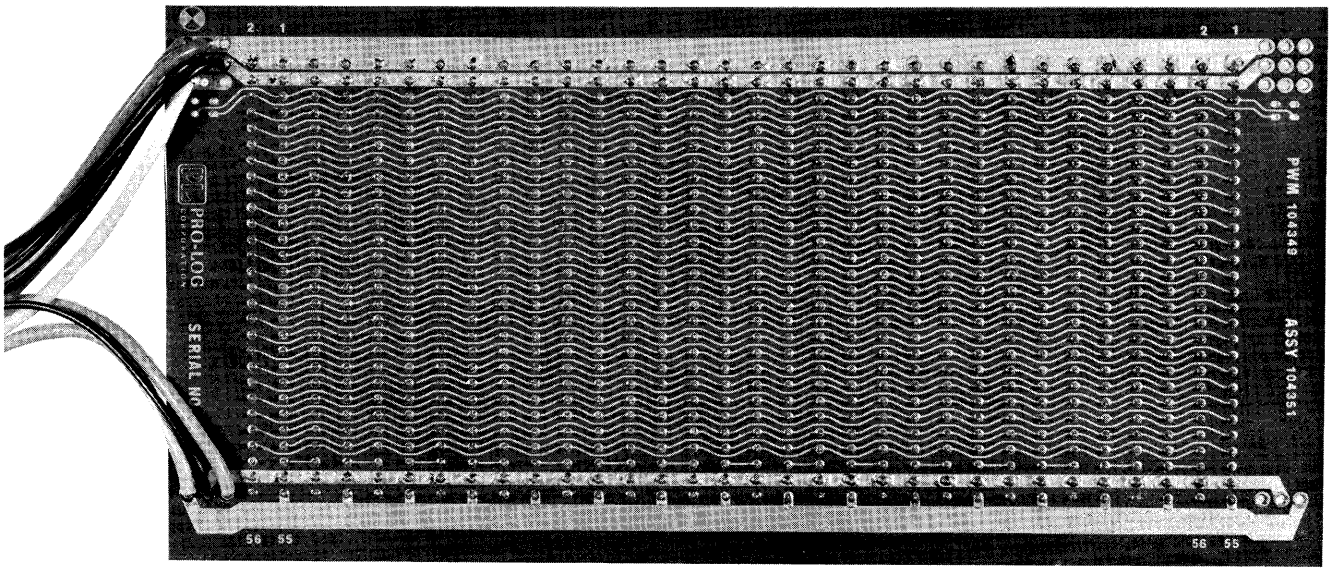
Pin 55 (AUX +V) and Pin 56 (AUX -V) are bussed pin-for-pin to all edge connectors.

Pins 53 and 54 (AUXGND) are bussed together at each edge connector and to all edge connectors.

		7101	7102	
PARAMETER FOR TOTAL MOTHERBOARD		MAX	MAX	UNITS
I_{A+}	Analog V+ trace current (10°C rise from 20°C)	7.0	7.0	Amps
I_{A-}	Analog V- trace current (10°C rise from 20°C)	7.0	7.0	Amps
I_{AG}	Analog ground trace current (10°C rise from 20°C)	12.0	12.0	Amps
R_{A+}	Analog V+ trace resistance at 20°C	7.5	15	mΩ
R_{A-}	Analog V- trace resistance at 20°C	7.5	15	mΩ
R_{AG}	Analog ground trace resistance at 20°C	7.5	15	mΩ

For card edge connector information, refer to the CW56, CW56-1 Edge Card connector data sheet.

For power connector information see CR8/CR16 Data Sheet.



7102 STD BUS Backplane

7301 RS232 & TTY DRV/REC CARD

RS232 & TTY DRIVER/RECEIVER CARD

The 7301 combines the I/O ports and voltage translation needed to interface a microprocessor to both RS-232 and TTY serial data communications lines.

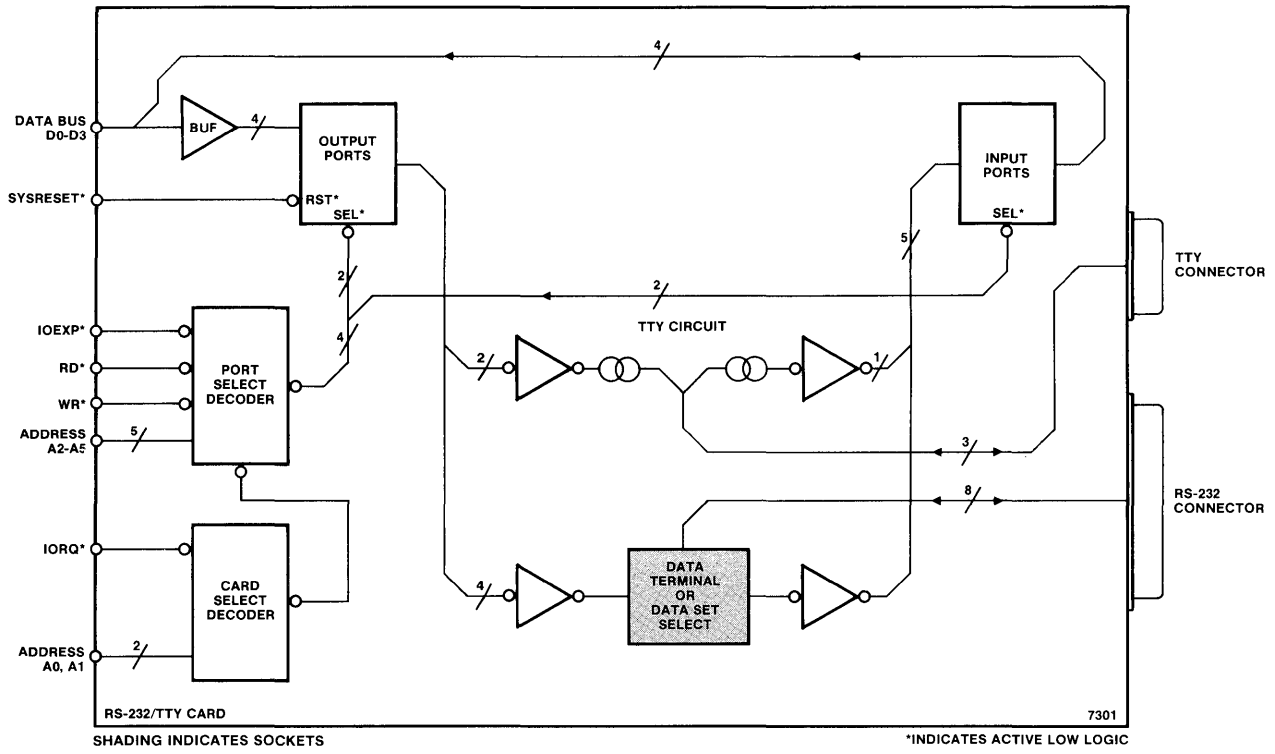
The RS-232 portion provides four each EIA Standard RS-232-C drivers and receivers, and a 25-pin D type cable connector. A pair of DIP sockets on the card allow the user to select Data Terminal or Data Set (modem) configurations by inserting a shorting plug (included) into one of the sockets. Operates over 0-20,000 Baud range.

The TTY portion consists of separate send and receive 20 mA current loops, a relay driver for remote control of an ASR-33 type console tape reader and a 9-pin D type cable connector. Operates over 0-300 Baud range.

Both the RS-232 and TTY circuits feature separate input and output ports for programming convenience, and cable interlocks which can be tested under program control. The microprocessor card used in conjunction with the 7301 must provide timing and serial/parallel conversion for both interface circuits.

FEATURES

- **EIA Standard RS-232-C Interface**
- **ASR/KSR TTY Interface**
- **Simultaneous Full Duplex Operation**
- **On-Card Industry Standard Cable Connectors**
- **Program Readable Cable Interlocks**
- **User Selectable Data Terminal/Data Set Configuration**
- **User Selectable Port Addresses**
- **System Processor generates Baud Rate**
- **+5V, -12V Operation**
- **All ICs Socketed**



SHADING INDICATES SOCKETS

*INDICATES ACTIVE LOW LOGIC

FUNCTIONAL

RS-232 Section

The 7301 provides four line drivers and four line receivers which meet EIA Standard RS-232-C. The drivers and receivers are connected to the eight RS-232 signal pins at the card's interface cable connector J2 as shown in the table below. The 7301 can occupy either the Data Terminal or Data Set position in an RS-232 communication link according to the position of the shorting plug P1 in signal configuration sockets J3 and J4. Four of the signals (TD*, DTR, RTS and SCD) originate at the Data Terminal and four signals (RD*, DSR, CTS and CD) originate at the Data Set. The four line receivers are used to monitor the complimentary signals originating at the other end of the communications link. The signal configuration sockets determine which signals are driven and which are received, thus establishing the Data Terminal or Data Set configuration for the 7301.

RS-232 SIGNAL	DRIVER AT	RECEIVER AT	7301 J2 PIN
Transmitted Data (TD*)	Data Terminal	Data Set	2
Received Data (RD*)	Data Set	Data Terminal	3
Data Terminal Ready (DTR)	Data Terminal	Data Set	20
Data Set Ready (DSR)	Data Set	Data Terminal	6
Request To Send (RTS)	Data Terminal	Data Set	4
Clear To Send (CTS)	Data Set	Data Terminal	5
Secondary Transmitted Data (SCD)	Data Terminal	Data Set	14
Carrier Detect (CD)	Data Set	Data Terminal	8

Driver/Receiver Assignments

Signal Options: As shipped, the 7301's RS-232 cable pin connections are suitable for serial data send/receive and handshake control for most commercially available computer terminals, modems, Pro-Log's M900 and M920 PROM Programmers, UART and USART cards from other manufacturers, or another 7301. In many instances only one to three of the driver/receiver pairs need be used for the interface. Three of the pairs (DTR/DSR, RTS/CTS and SCD/CD) are jumpered to the interface connector J2 and may be rejumpered to other J2 pins as required in the application. Pads are provided on the card for jumpering undriven pins to positive and negative DC supplies as permanent signals when needed.

The RS-232 drivers are controlled independently by a 4-bit latching output port on the 7301, and the RS-232 receivers are monitored by a 4-bit gated input port. The input and output port share the same HEX port address (C0 as shipped) which may be remapped in the range 00-FF. Both the input and output port communicate with a processor card over the four least significant bits of the STD Data Bus.

DATA TERMINAL CONFIGURATION

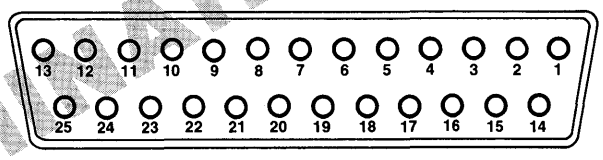
PORT CO	BIT FUNCTION							
	7	6	5	4	3	2	1	0
INPUT (RECEIVERS)	1	1	1	1	DSR	CD	CTS	RD
OUTPUT (DRIVERS)	X	X	X	X	DTR	SCD	RTS	TD

DATA SET CONFIGURATION

PORT CO	BIT FUNCTION							
	7	6	5	4	3	2	1	0
INPUT (RECEIVERS)	1	1	1	1	DTR	SCD	RTS	TD
OUTPUT (DRIVERS)	X	X	X	X	DSR	CD	CTS	RD

X = Don't Care

Port CO Bit Functions



RS-232 Connector Pins; Female (7301 J2 Front View)

TTY Current Loop Section

The 7301 provides one 20 mA current loop driver and one 20 mA receiver plus an open collector, diode clamped 12V/60mA driver suitable for controlling the tape reader in ASR-33 consoles. Application information for the installation of a tape reader control relay is available from Pro-Log.

The TTY drivers are controlled independently by a 4-bit latching output port on the 7301, and the receiver is monitored by a gated input port. The input and output port share the same HEX port address (C1 as shipped) which may be remapped in the range 00-FF. The table below shows the bit/function of these port bits.

TTY CURRENT LOOP

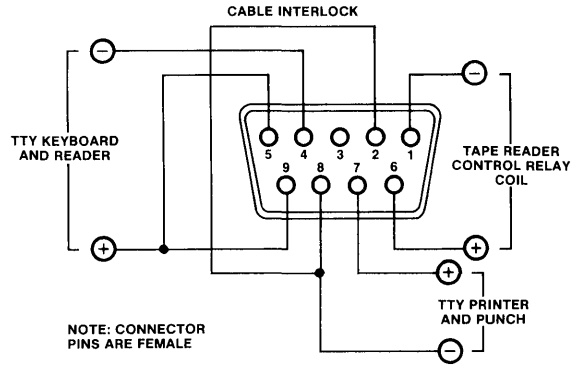
PORT C1	BIT FUNCTION							
	7	6	5	4	3	2	1	0
INPUT	1	1	1	1	SPARE*	RS-232 INTLK	TTY INTLK	DATA IN
OUTPUT	X	X	X	X	SPARE	SPARE	TAPE CTRL	DATA OUT

X = Don't Care

* = Low Level Logic

Port C1 Bit Functions

FUNCTIONAL (continued)



Recommended TTY Hookup (J1 Front View)

Common Features

The RS-232 cable connection is made on the 7301 by an industry standard 25-pin D-type connector. The TTY connector is a 9-pin D-type. Both are located below the card ejector. Both circuits include input port pins for a user-added cable interlock. These are used by connecting the pins shown in the Pin Tables to signal ground in the cable assembly.

The SYSRESET* input to the 7301 clears both the RS-232 and TTY output ports, resulting in STOP bits on the RS-232 and TTY serial data lines, TTY tape reader off and inactive RS-232 control signals. SYSRESET* has no effect on the gated input ports.

Card Address Mapping

The 7301 card is selected by a decoded combination of address lines A1-A7. The user chooses the card address combination by connecting one jumper wire each from SX, SY, SZA and SZB to pad matrices adjacent to U2, U3, U4 and U5. The 7301 is shipped with HEX port addresses C0 (RS-232) and C1 (TTY) connected. To map the 7301 anywhere in the HEX address range 00-FF, change the decoder output jumpers. To determine the appropriate connections for a particular port address, use the 2 addresses-per-card Port Mapping Scheme as defined in the Series 7000 STD BUS Technical Manual.

Port Addresses: Address line A0 selects one of the two sequential port addresses to select either the RS-232 or TTY circuits. One input port and one output port (4 bits only) reside at each address on the 7301. The RD* and WR* control inputs differentiate between input gating or output latch functions.

ELECTRICAL

- VCC = +5V ± 5%
- ICC = 525 mA maximum (380 mA typical)
- AUX -V = -12V ± 5%
- AUX I = -200 mA maximum
- Address, Data and Control Busses meet all STD BUS general electrical specifications.
- AUX GND (pins 53, 54) is connected to LOGIC GND (pins 3, 4) on the 7301 by a user removeable jumper trace.

	PARAMETER	MIN	MAX	UNITS	NOTE
V_{OH}	High Level Output Voltage	+3		V	1
V_{OL}	Low Level Output Voltage		-3	V	
I_{OS}	Output Short Circuit Current, Output Connected To ±12V (Duration 1 Second Maximum)		85	mA	
CL	Output Load Capacitance		2500	pF	2
Tr Tf	Output Rate Of Change		30	V/μs	
V_{IH}	Input High Level Voltage	+3	+25	V	3
V_{IL}	Input Low Level Voltage	-25	-3	V	
I_{IH}	Input High Level Current	+0.5	+8.5	mA	
I_{IL}	Input Low Level Current	-8.5	-0.5	mA	
EL	Output Termination Bias	-2.0	+2.0	V	
	BAUD Rate (Bits/Second)	0	20,000	BAUD	
	Recommended Cable Length		50 16	feet meters	
VO	Driver Open Circuit Output Voltage	-12	+5	V	
RO	Driver Output Resistance, Power Off	300		ohms	
RL	Input Load Resistance	3K	6K	ohms	3

NOTES:
1. Minimum load resistance 3K ohms
2. Includes cable and terminator capacitance
3. Except Cable Interlock, which is 4 LSTTL input loads

7301 RS-232 Connector J2

ELECTRICAL (continued)

J1 PIN	FUNCTION
1	Paper tape motion control relay coil power source; provides -12V through a 100 ohm, 1/4 Watt, 5% resistor (diode clamp to pin 6)
2	Interface cable interlock input; active low logic; use is optional. Designed to be connected to logic ground (pin 8) by the interface cable when the cable is plugged into 7301 J1. Read into the processor as input port C1 bit 1; a logic 1 is returned when pin 2 is grounded, or a logic 0 when open. Input loading 4 LSTTL loads.
3	Spare pin; connected to a pad on the 7301 adjacent to pads supplying +5V or -12V. User may connect a jumper wire or a 1/2 Watt resistor to either voltage for special applications.
4	Current loop return (7301 receive); supplies -12V through a 470 ohm, 1/2 Watt, 5% resistor supplying 20 mA return and pin 9 voltage pulldown when the TTY commutator is closed (spacing). Not required in some instrument interfaces.
5	20 mA source (7301 receive); supplies +20 mA from +5V through a 220 ohm, 1/4 Watt, 5% resistor when the TTY commutator is closed (spacing) and pulls up pin 9 when the commutator is open (marking).
6	Paper tape control relay drive; supplies up to +50 mA through a switching transistor and 100 ohm, 1/4 Watt, 5% resistor when output port C1 bit 1 is at logic 1 (+5V current source). When output port C1 bit 1 is at logic 0 or the 7301 is reset, output leakage current is 0.1 mA maximum (pin 6 at 0V).
7	20 mA source (7301 transmit); provides +20 mA minimum (measured with pin 7 at 0V) from the +5V supply through a switching transistor and a 200 ohm, 1/4 Watt, 5% resistor when output port C1 bit 0 is at logic 0. Output leakage current (pin 7 at 0V) with output port C1 bit 0 at logic 1 is 0.1 mA maximum. Note that this output supplies +20 mA when the 7302 is reset. Pads are provided for jumpering across the 200Ω resistor in instrument interface applications requiring additional drive voltage.
8	Logic ground out; connects to LOGIC GROUND (STD BUS pin 3, 4) and AUX GND (STD BUS pins 53, 54). A user removable trace on the 7301 connects the two ground busses together.
9	Current Loop Receive (7301 receive); a transistor base input through a 4.7K ohm, 1/4 Watt, 5% resistor and negative current clamp diode. A voltage greater than +2.5V applied to pin 9 is returned to the processor as input port C1 bit 0 at logic 1. A voltage lower than +0.8V is read as logic 0.

J1 Current Loop Connector Specifications

MECHANICAL

- Meets all STD BUS general mechanical specifications except RS-232 and TTY cable connectors which protrude from the card front 0.375 inches (0.953 cm), and card width which requires two card slots for cable connector clearance on the card wiring side.

TTY CONNECTOR PIN LIST					
PIN NUMBER	SIGNAL FLOW	SIGNAL	PIN NUMBER	SIGNAL FLOW	SIGNAL
-12V/100Ω SOURCE	OUT	1	6	OUT	SWITCHED RELAY SINK*
CABLE INTERLOCK*	IN	2	7	OUT	CURRENT LOOP TRANS*
(SPARE)		3	8	OUT	LOGIC GROUND
-12V/470Ω SOURCE	OUT	4	9	IN	CURRENT LOOP RECV*
+5V/220Ω SOURCE	OUT	5			

*Designates Active Low Level Logic

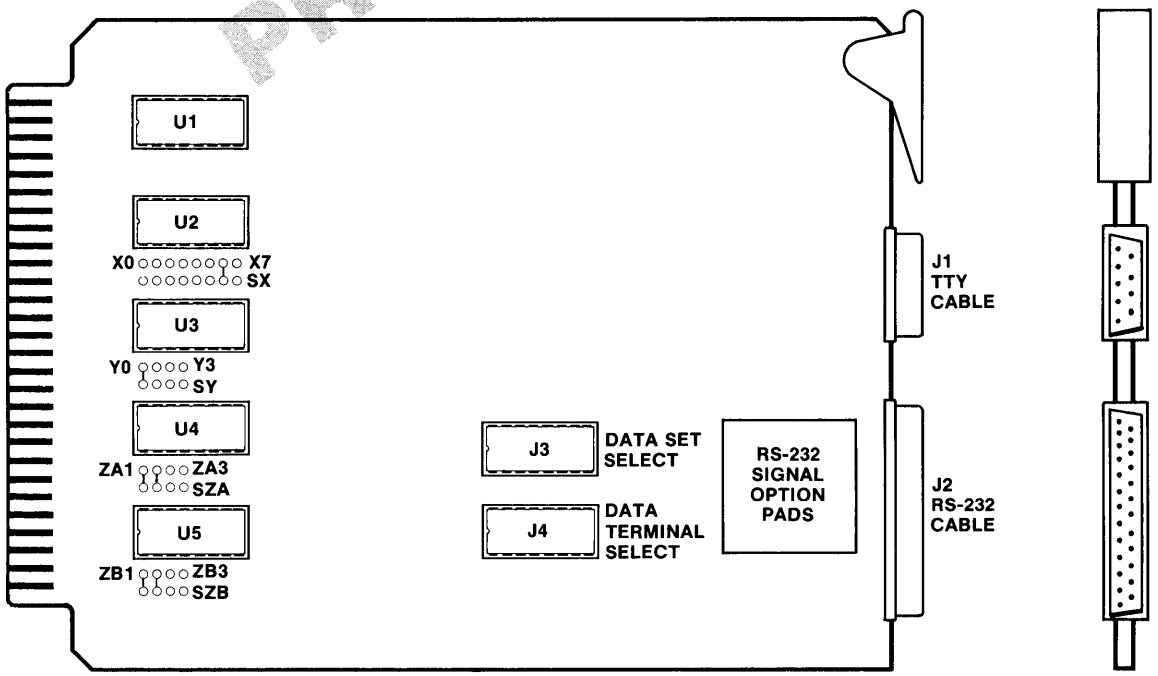
TTY Connector Pin List

RS-232 CONNECTOR PIN LIST					
PIN NUMBER	SIGNAL ORIGIN	SIGNAL	PIN NUMBER	SIGNAL ORIGIN	SIGNAL
PROTECTIVE GROUND		1	14	T□	SEC. TRANSMITTED DATA*
TRANSMITTED DATA*	T■	2	15	S	TRANS SIGNAL TIMING
RECEIVED DATA*	S■	3	16	S	SEC. RECEIVED DATA*
REQUEST TO SEND	T□	4	17	S	RECV. SIGNAL TIMING
CLEAR TO SEND	S□	5	18		(UNASSIGNED)
DATA SET READY	S□	6	19	T	SEC. REQUEST TO SEND
SIGNAL GROUND	OUT	7	20	T□	DATA TERMINAL READY
CARRIER DETECT	S□	8	21	S	SIGNAL QUALITY DETECT
(TEST)		9	22	S	RING INDICATOR
(TEST)		10	23	T/S	DATA SIGNAL RATE SEL.
(UNASSIGNED)		11	24	T	TRANS. SIGNAL TIMING
SEC. CARRIER DETECT	S	12	25	IN□	CABLE INTERLOCK*
SEC. CLEAR TO SEND	S	13			

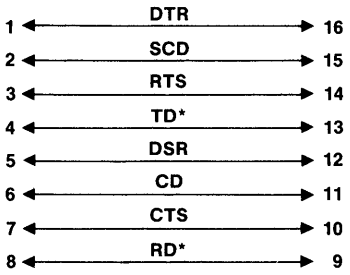
*Designates Active Low Level Logic

LEGEND:
T - Signal Originates At Data Terminal (DTE)
S - Signal Originates At Data Set (DCE)
■ - Permanent Connection On 7301
□ - Jumper Connection On 7301; May Be Relocated By User

RS-232 Connector Pin List



7301 User Options



Data Terminal/Data Set Select Plug P1 Wiring
Shorting Bars Exposed For Scope Test Points

STD/7301 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5 VOLTS	IN		2	1		IN	+5 VOLTS
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7			8	7	60	1	D3
D6			10	9	60	1	D2
D5			12	11	60	1	D1
D4			14	13	60	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43		1	INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND	IN		54	53	IN		AUX GND
AUX-V (-12V)	IN		56	55			AUX +V

*Designates Active Low Level Logic

Connector Pin Lists

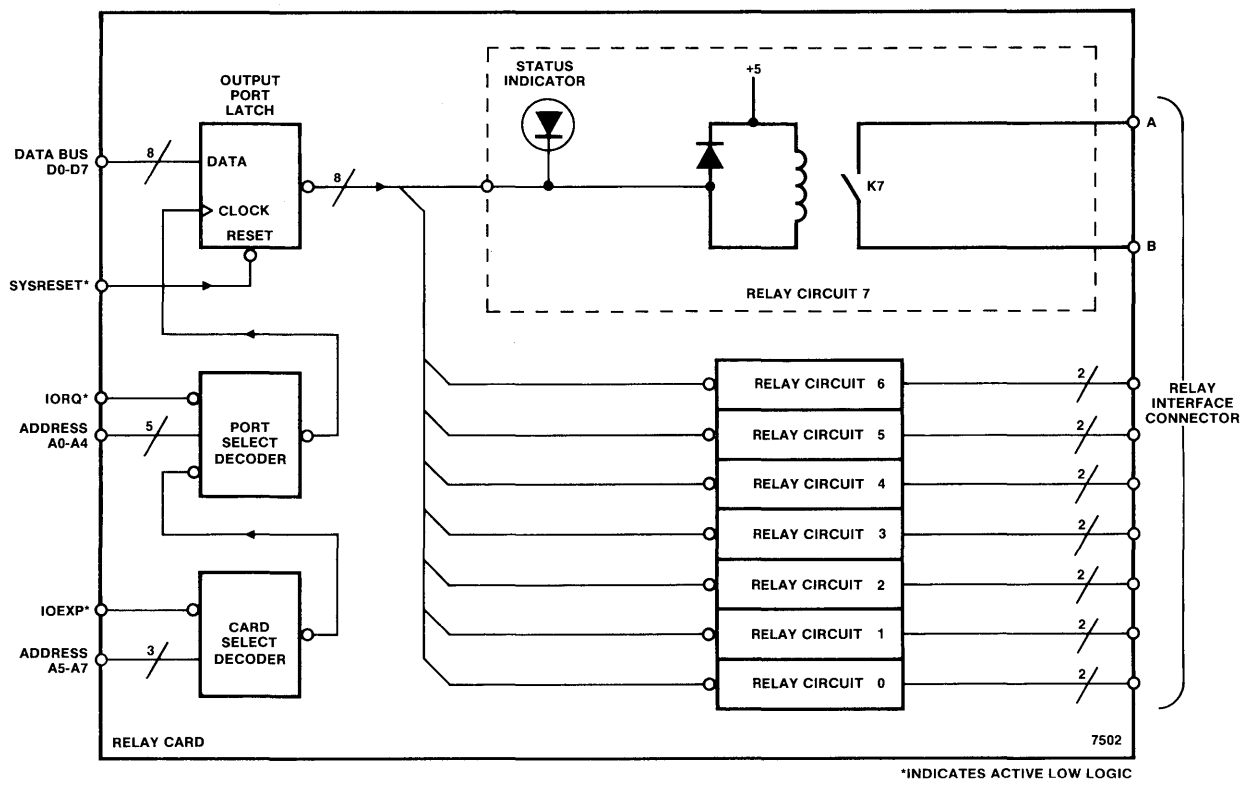
7502 SPST RELAY OUTPUT CARD

SPST RELAY OUTPUT CARD

The 7502 consists of eight independent SPST dry reed relays controlled by a fully decoded, latched 8-bit output port. Each 7502 gives the processor direct control of eight additional reed relay switches.

FEATURES

- **Eight independent SPST dry reed relays**
- **On-card LED display of relay closures**
- **User selected port address**
- **Keyed front-edge connector for relay outputs**
- **All ICs socketed**
- **Single +5V operation**



7502, SPST RELAY OUTPUT CARD

FUNCTIONAL

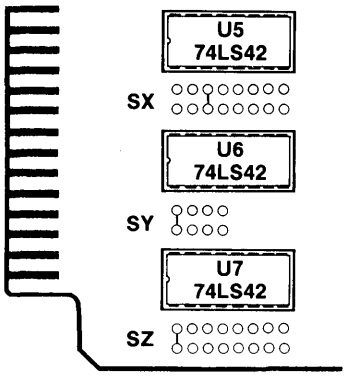
The 7502's eight relays are switched independently by the eight bits from a single on-card output port. When an output port bit is latched high, the corresponding reed relay closes. The relay remains closed until its output port bit is latched low or reset.

Card Address Mapping

The 7502 card is selected by a decoded combination of address lines A0 through A7. The user chooses the card address combination by connecting a jumper wire from SX, SY and SZ to pad matrices adjacent to U5, U6 and U7. The 7502 is shipped with hexadecimal port address 40. To map the 7502 anywhere in the Hexadecimal port address range of 00-FF, change the decoder outputs connected to SX, SY and SZ. Refer to the Series 7000 STD BUS Technical Manual for additional card mapping information.

Reset

The SYSRESET* input clears the output port and opens all eight reed relays simultaneously.



Card Address Selection

ELECTRICAL

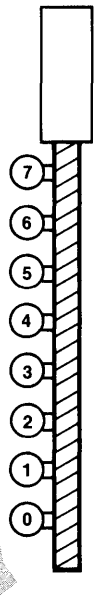
- VCC = +5V ± 5%
- ICC = 400 mA maximum (300 mA typical), all relays energized.
- Address, Data and Control Busses meet all STD BUS general electrical specifications.
- Pads are provided at each relay contact set for user-added RC suppression networks.

PARAMETER	MIN	MAX	UNITS	COMMENTS
Contact Current		0.5	Amp	Combined DC and peak transient currents during contact opening or closure.
Contact Voltage		200	Volts	DC and peak voltage across open relay contacts.
Breakdown Voltage	300		Volts	DC and peak voltage between relay contact sets, and between the relay interface edge connector and the STD BUS edge connector.
Contact Resistance		0.2	Ohms	Initial contact resistance.
		1.0	Ohm	At end of life
Contact Lifetime	10^7		Operations	At 0.5 Amp load
Switching Time		0.5	msec	Open or close
Bounce Time		0.5	msec	After open or close

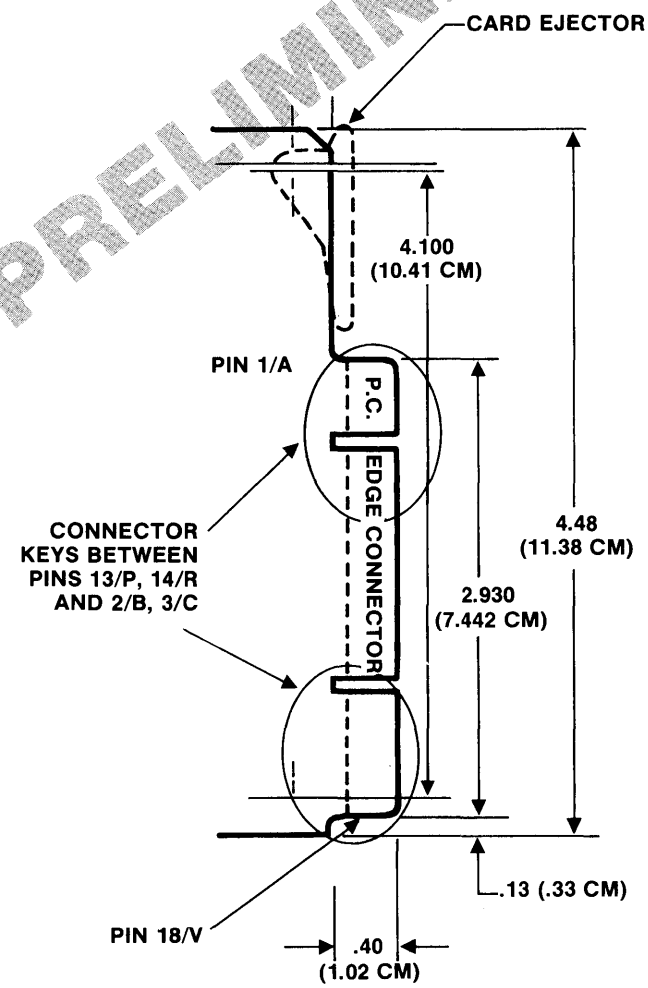
Reed Relay Contact Characteristics

MECHANICAL

- Meets all STD BUS general mechanical specifications, except:
  1. The I/O interface connector is a 36-pin (dual 18-pin) edge connector. Overall card length is extended to 6.90 ± 0.025 inches (17.53 ± 0.064 cm). Edge connector height is 2.930 ± 0.005 inches (7.442 ± 0.012 cm). Contact fingers are on 0.125 inch (0.318 cm) centers. Opposing fingers are shorted, yielding 18 isolated contacts. Two non-reversible connector keys are provided between pins 2 and 3, and 13 and 14.
  2. An LED Relay status display visible from the card front is provided. Each LED is illuminated by its corresponding output port bit to indicate that the Relay is energized.
  3. The 7502 requires one open card slot on either side of itself for clearance of the safety shields and interface connector (three card slots total).



LED Status Display



Front Edge Connector
(Component - Side View)

7502, SPST RELAY OUTPUT CARD

INTERFACE CONNECTOR PIN LIST 7502	
PIN NUMBER	SIGNAL
1/A	RELAY K7A
2/B	K7B
3/C	RELAY K6A
4/D	K6B
5/E	RELAY K5A
6/F	K5B
7/H	RELAY K4A
8/J	K4B
9/K	RELAY K3A
10/L	K3B
11/M	RELAY K2A
12/N	K2B
13/P	RELAY K1A
14/R	K1B
15/S	RELAY K0A
16/T	K0B
17/U	SPARE
18/V	SPARE

Interface Connector Pin List

STD/7502 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)						OUTPUT (DRIVE)	
INPUT (LOADING)							INPUT (LOADING)
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*			32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

The following connectors will mate with the 7502 Interface Edge Connector:

TRW CINCH #250-18-30-220
VIKING #2VH18/1AB5
WINCHESTER #8B18S002G314G1S

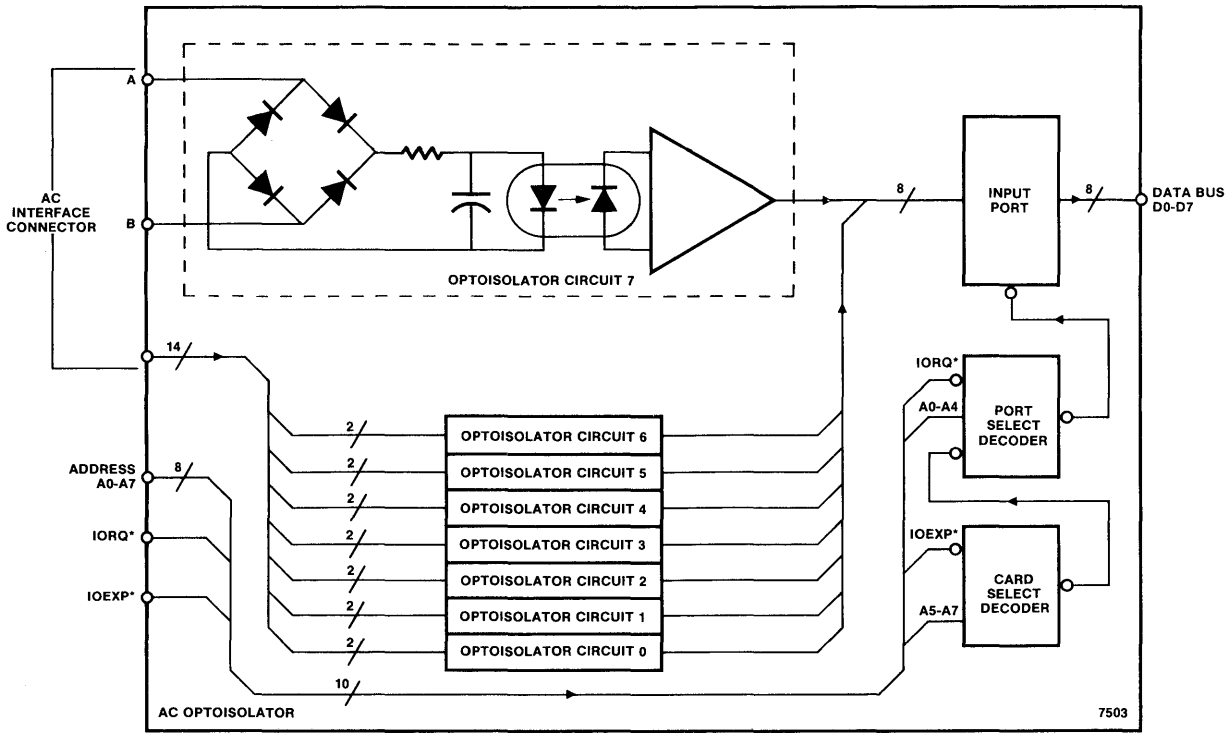
7503 OPTOISOLATED AC INPUT CARD

OPTOISOLATED AC INPUT CARD

The 7503 provides optical isolation and voltage translation to TTL levels for up to eight AC inputs. The on or off conditions of these inputs are gated into the processor by a fully decoded 8-bit input port on the card. A full-wave bridge rectifier and RC filter are provided at each input, with pads for additional user-added signal conditioning components. The card may be used with inputs up to 115 VAC.

FEATURES

- **Eight independent AC inputs**
- **Input voltages to 115 VAC (±160 VDC)**
- **Steady state input loading 500 μA maximum**
- **Optical isolation for 1500 V breakdown**
- **Clear plastic safety shield**
- **User selectable input port address**
- **Keyed interface connector for AC inputs**
- **All ICs socketed**
- **Single +5V operation**



7503, OPTOISOLATED AC INPUT CARD

FUNCTIONAL

Input Sensing

The 7503's eight AC inputs are sensed independently as the eight output bits from a single on-card input port. When an AC input is present, the corresponding input port bit will be high. The bit remains high until the AC input is removed. Each input circuit consists of a full-wave bridge rectifier and RC filter. DC inputs up to the peak AC rating of the card may be applied without regard to polarity.

Card Address Mapping

The 7503 card is selected by a decoded combination of address lines A0 through A7. The user chooses the card address combination by connecting one jumper wire each from SX, SY and SZ to pad matrices. The 7503 is shipped with Hexadecimal Port Address 40. To map the 7503 anywhere in the Hexadecimal port address range of 00-FF, change the decoder outputs connected to SX, SY and SZ. Refer to the Series 7000 STD BUS Technical Manual for additional card mapping information.

ELECTRICAL

- VCC = +5V ± 5%
- Address, Data and Control Busses meet all STD BUS general electrical specifications.

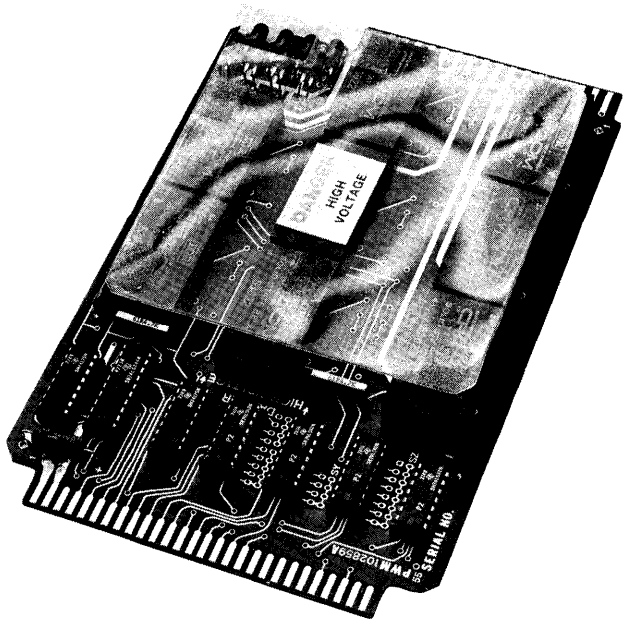
INTERFACE CONNECTOR PIN LIST 7503	
PIN NUMBER	SIGNAL
1/A	AC INPUT 7A
2/B	7B
3/C	AC INPUT 6A
4/D	6B
5/E	AC INPUT 5A
6/F	5B
7/H	AC INPUT 4A
8/J	4B
9/K	AC INPUT 3A
10/L	3B
11/M	AC INPUT 2A
12/N	2B
13/P	AC INPUT 1A
14/R	1B
15/S	AC INPUT 0A
16/T	0B
17/U	SPARE
18/V	SPARE

Interface Connector Pin List

7504 TRIAC OUTPUT CARD

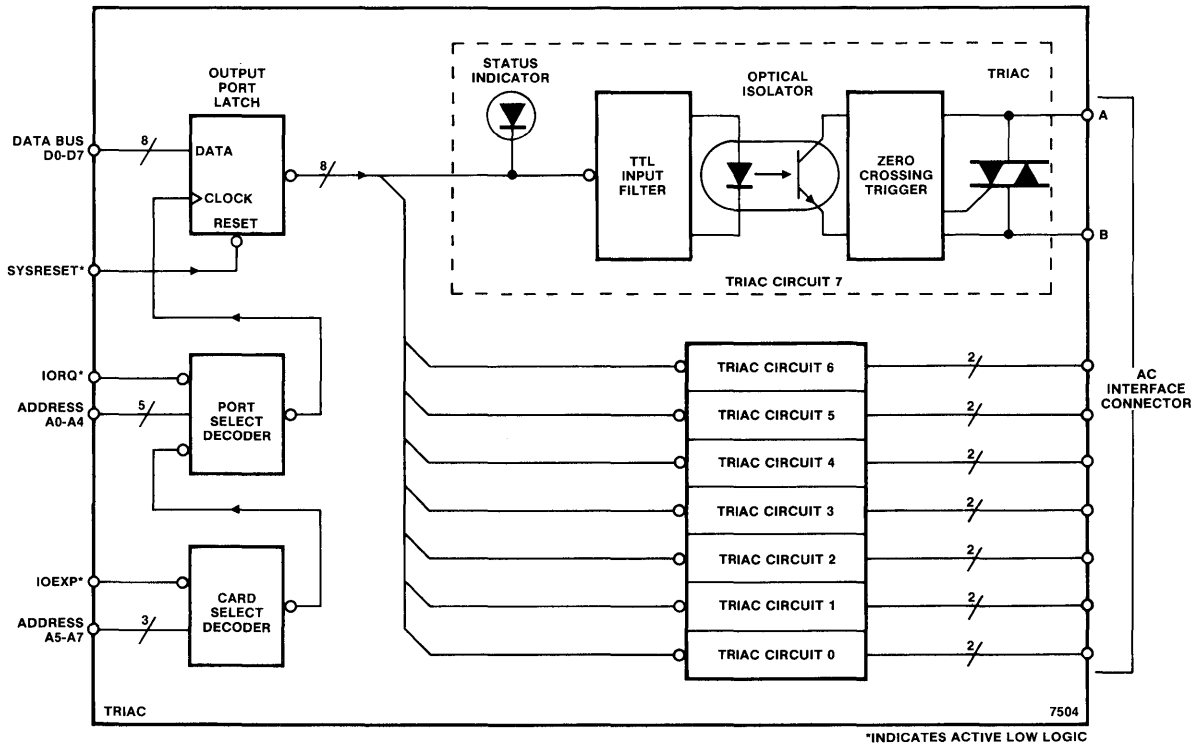
TRIAC OUTPUT CARD

The 7504 consists of eight independent solid state AC relays (Triacs) controlled by a fully decoded, latched 8-bit output port. Each 7504 gives the processor direct control of eight additional switched AC power circuits.



FEATURES

- **Eight independent 40-280 VAC 2 Amp Triacs**
- **Optical isolation for low noise and 1500 VAC breakdown**
- **Zero-crossing power switching**
- **Clear plastic safety shields**
- **On-card LED display of Triac status**
- **User selectable port address**
- **Keyed front-edge connector for AC power**
- **Snubber networks built in**
- **All IC's socketed**
- **Single +5V operation**



7504, TRIAC OUTPUT CARD

FUNCTIONAL

Triac Switching

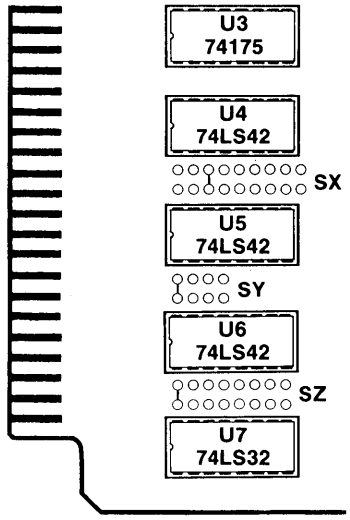
The 7504's eight Triac circuits are switched independently by the eight bits from a single on-card output port. When an output port bit is latched high, the corresponding Triac is armed and will switch on at the next zero-volt crossing of its AC input. The Triac remains on until the first zero volt crossing after the output port bit is latched low or reset.

Card Address Mapping

The 7504 card is selected by a decoded combination of address lines A0 through A7. The user chooses the card address combination by connecting one jumper wire each from SX, SY and SZ to pad matrices adjacent to U4, U5 and U6 (see diagram). The 7504 is shipped with Hexadecimal Port address 40. To map the 7504 anywhere in the Hexadecimal port address range of 00-FF, change the decoder outputs connected to SX, SY and SZ. Refer to the Series 7000 STD BUS Technical Manual for additional card mapping information.

Reset

The SYSRESET* input clears the output port and allows each Triac to switch off at the next zero-volt crossing of each AC input.



Card Address Selection

ELECTRICAL

- VCC = +5V ± 5%
- ICC = 500 mA maximum (450 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications.
- Snubbers included. Additional snubbers may be desired at the load.

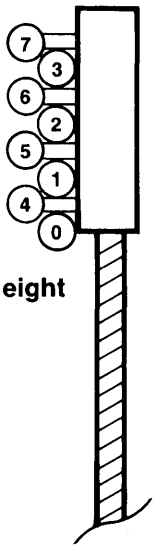
Triac Electrical Characteristics

PARAMETER, Each Triac (0°-55° unless noted)		7504-1 MIN	7504-1 MAX	UNITS	NOTE
AC Voltage Operating Range		40	280	Volts RMS	
AC Frequency Range		47	63	Hz	
Load Current	Ambient Temperature 0°-40°C	0.02	2.0	Amps RMS	1
	Derated at 55°C	0.02	1.5		
On-State Voltage Drop at Rated Load Current			1.2	Volts	2
Surge Current	Duration 16.3 milliseconds		55.0	Amps Peak	
	Duration 1.0 seconds		14.0		
Off-State Leakage Current			5.0	mA	3
Peak Operating Voltage (Nonrepetitive)			500	Volts Peak	
Zero Crossing Uncertainty Range		-30	30	Volts	4
Isolation of AC Power	Insulation Resistance	10^{10}		Ohms	5
	Breakdown Voltage	1500		Volts RMS	
Internal Snubber Values (RC Suppressor Networks)		47		Ohms	
		0.01		μF	

Notes:
1. Derate linearly at 33 mA/°C (7504-1) to 55°C maximum.
2. Measured at 25°C at the rated maximum load current.
3. Measured at 500 VDC.
4. Describes the on/off switching characteristics of the Triac.
5. Describes the isolation between the AC Power connections and the STD BUS edge connector.

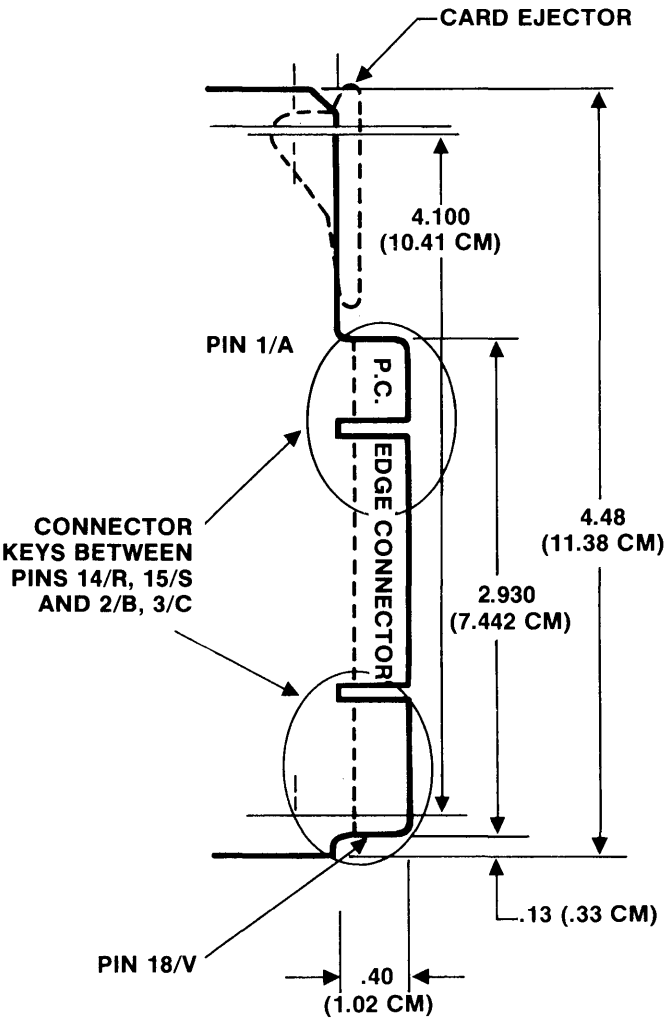
MECHANICAL

- Meets all STD BUS general mechanical specifications, except:
  1. The I/O interface connector is a 36-pin (dual 18-pin) edge connector. Overall card length is extended to 6.90 ± 0.025 inches (17.53 ± 0.064 cm). Edge connector height is 2.930 ± 0.005 inches (7.442 ± 0.012 cm). Contact fingers are on 0.125 inch (0.318 cm) centers. Opposing fingers are shorted, yielding 18 isolated contacts. Two non-reversible connector keys are provided between pins 2 and 3, and 14 and 15.
  2. An LED Triac status display visible from the card front is provided. Each LED is illuminated by its corresponding output port bit to indicate that the Triac is on or armed.
  3. The 7504 requires one open card slot on either side of itself for clearance of the safety shields and interface connector (three card slots total).



Maximum Component Height
0.85" (2.16 cm)

LED Status Display



Front Edge Connector
(Component - Side View)

7504, TRIAC OUTPUT CARD

INTERFACE CONNECTOR PIN LIST 7504	
PIN NUMBER	SIGNAL
1/A	TRIAC K7A
2/B	K7B
3/C	TRIAC K6A
4/D	K6B
5/E	TRIAC K5A
6/F	K5B
7/H	TRIAC K4A
8/J	K4B
9/K	TRIAC K3A
10/L	K3B
11/M	TRIAC K2A
12/N	K2B
13/P	TRIAC K1A
14/R	K1B
15/S	TRIAC K0A
16/T	K0B
17/U	SPARE
18/V	SPARE

Interface Connector Pin List

STD/7504 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)				OUTPUT (DRIVE)			
INPUT (LOADING)						INPUT (LOADING)	
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*			32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PC I	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

The following connectors will mate with the 7504 Interface Edge Connector:

TRW CINCH #250-18-30-220
VIKING #2VH18/1AB5
WINCHESTER #8B18S002G314G1S

7000 STD BUS

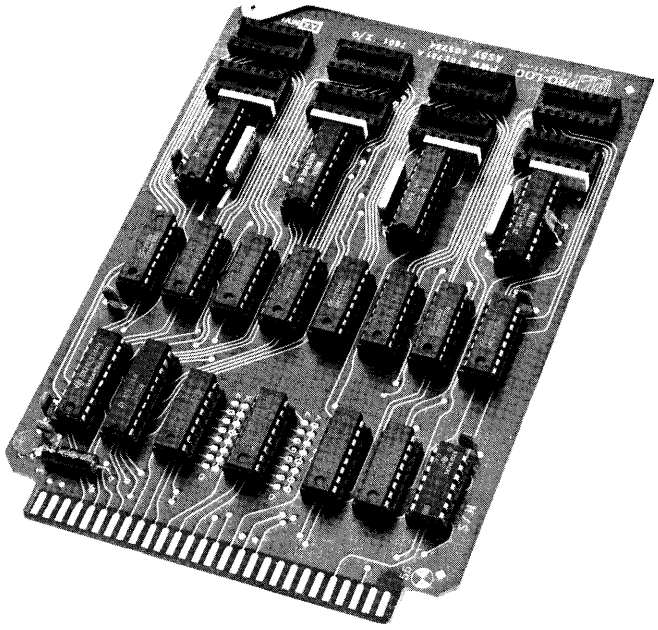
7601 INPUT/OUTPUT PORT CARD

TTL INPUT/OUTPUT PORT CARD

This card provides four 8-bit gated input ports (32 input lines) and four 8-bit latched output port (32 output lines).

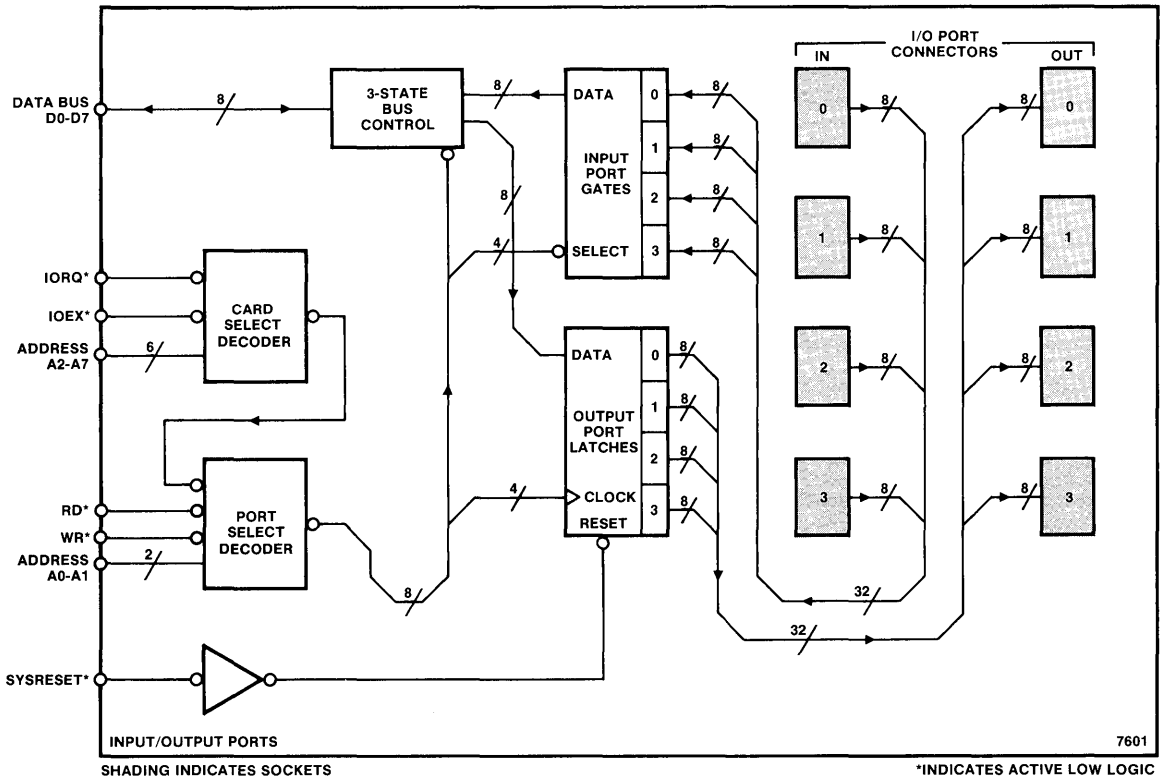
Input port lines and output port lines are accessed at 16-pin DIP sockets on the card. I/O lines are TTL compatible with an input rating of 4 low-power Schottky TTL loads and an output drive rating of 20 low-power Schottky TTL loads (5 TTL loads). A reset line is available.

The 7601 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows users to establish the four consecutive I/O port pair addresses occupied by the 7601.



FEATURES

- **User selected port address (256 port field)**
- **Input rating: 4 LSTTL loads**
- **Output rating: 20 LSTTL loads (5 TTL loads)**
- **Provision for expansion and memory mapping**
- **Input buffers have 200 MV of hysteresis for additional noise margin**
- **Input lines include 4.7K pullup resistors**
- **All IC's socketed**
- **Single +5V operation**



7601, INPUT/OUTPUT PORT CARD

FUNCTIONAL

Card Address Mapping

The 7601 card is selected by a decoded combination of address lines A2 through A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U3 and U4 (See Diagram). The 7601 is mapped at Port 00 to 03 hexadecimal. To map the 7601 anywhere in the hexadecimal address range of 00-FF change the decoder outputs connected to SX and SY. To determine the appropriate connections for a desired port address use the 4 address per card Port Mapping Scheme as defined in the Series 7000 STD BUS Technical Manual.

Port Addresses

Address lines A0 and A1 select one of four sequential port addresses. One input port and one output port reside at each address. The RD* and WR* control inputs differentiate between input gating or output latch functions.

Reset

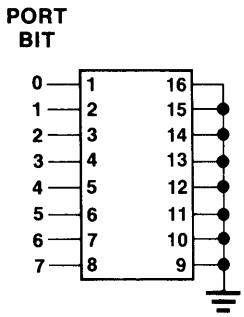
The SYSRESET* line clears all four output ports to zero simultaneously. The input ports are unaffected.

ELECTRICAL

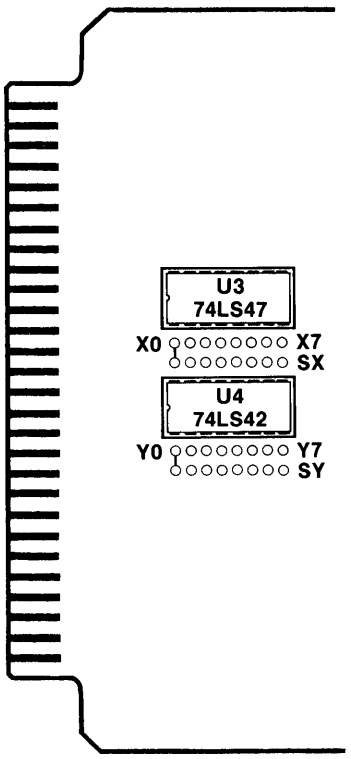
- VCC = +5V ± 5%
- ICC = 475 mA maximum (300 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications
- Each input port line presents 4 LSTTL loads, and each output port line can drive 20 LSTTL loads
- 16-pin DIP sockets are provided for access to Input and Output Port bit lines. The diagram below shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width (0.5 inch) for ribbon cable access to port sockets.
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T and B Ansley catalog No. 609-M165H or equivalent



Input or Output Port Socket



Card Address Selection

STD/7601 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)				OUTPUT (DRIVE)			
INPUT (LOADING)				INPUT (LOADING)			
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	60	8	7	60	1	D3
D6	1	60	10	9	60	1	D2
D5	1	60	12	11	60	1	D1
D4	1	60	14	13	60	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47	1		SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

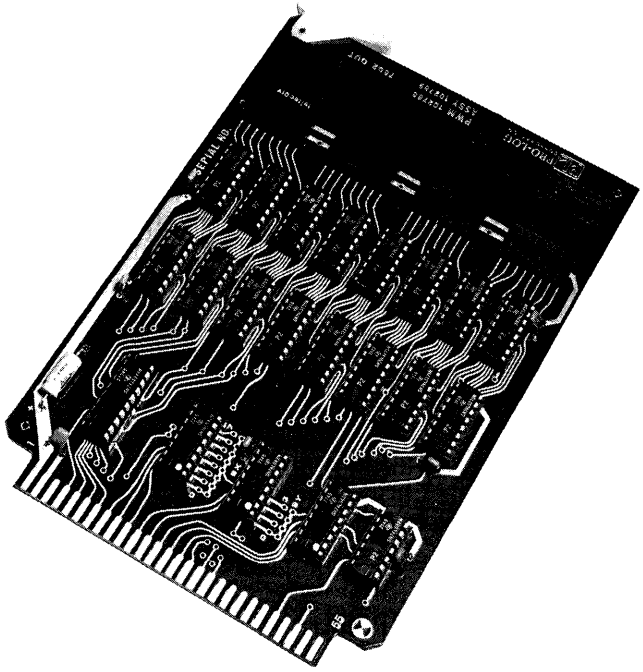
7602 OUTPUT PORT CARD

TTL OUTPUT PORT CARD

This card provides eight 8-bit latched output ports (64 output lines).

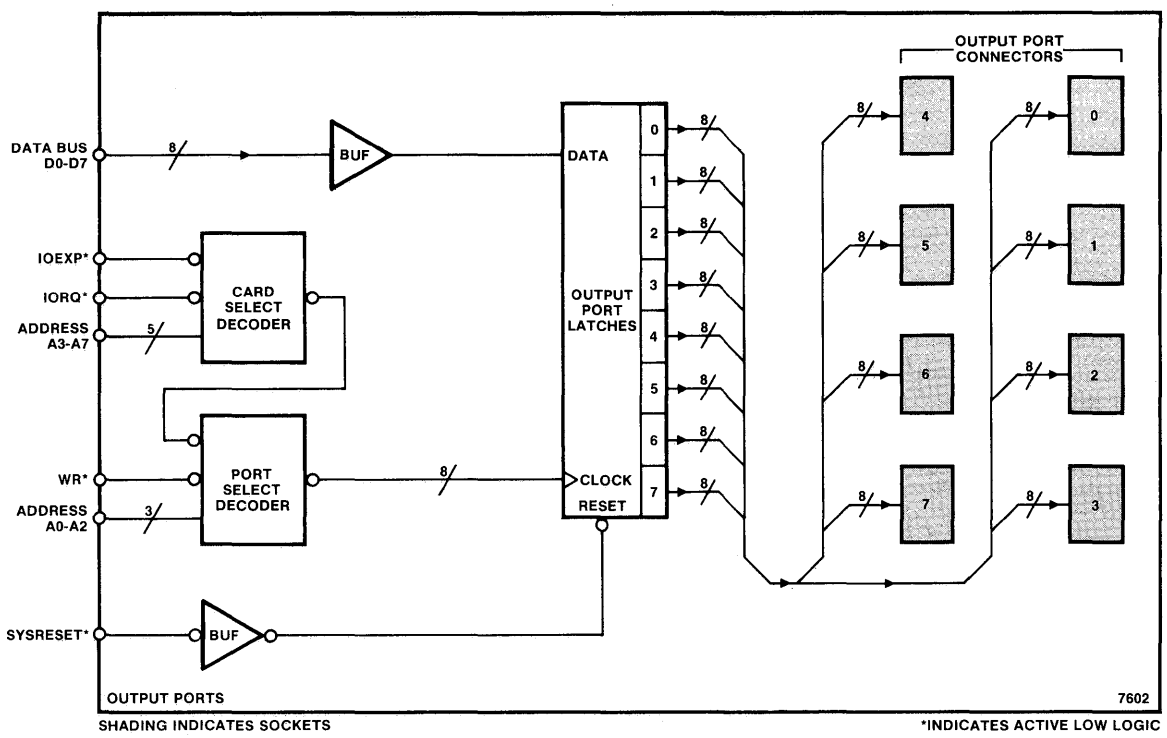
Output port lines are accessed at 16-pin DIP sockets on the card. The output lines are TTL compatible with the ability to drive 20 low-power Schottky TTL loads each (5 TTL loads). A reset line is available to clear all ports simultaneously.

The 7602 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows users to establish the eight consecutive output port addresses occupied by the 7602.



FEATURES

- **User selectable port address (256 port field)**
- **Output Drive: 20 low-power Schottky TTL loads**
- **Provision for expansion and memory mapping**
- **All IC's socketed**
- **Single +5V operation**



SHADING INDICATES SOCKETS

*INDICATES ACTIVE LOW LOGIC

7602, OUTPUT PORT CARD

FUNCTIONAL

Card Address Mapping

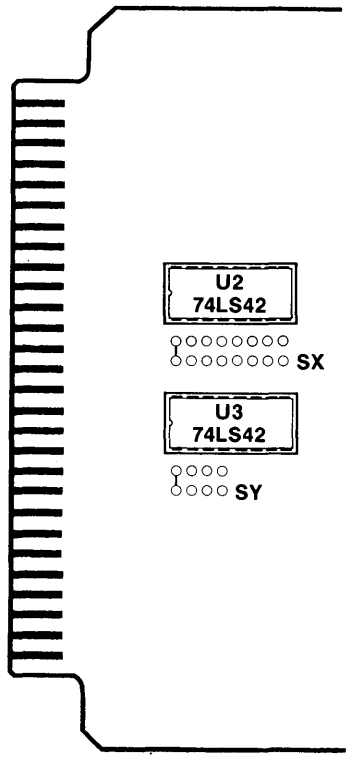
The 7602 card is selected by a decoded combination of address lines A3-A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U2 and U3 (See Diagram). The 7602 is shipped with Port address 00-07 Hexadecimal. To map the 7602 anywhere in the hexadecimal range of 00-FF change the decoder outputs connected to SX and SY. To determine the appropriate connections for a desired port address use the 8 address per card port mapping scheme as defined in the Series 7000 STD BUS Technical Manual.

Port Addresses

Address lines A0, A1 and A2 select one of eight sequential output port addresses. The WR* input controls the output latch function.

Reset

The SYSRESET* input clears all eight output ports to zero simultaneously.



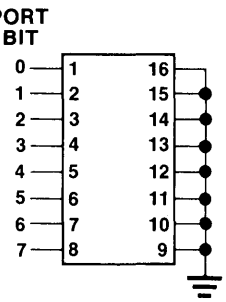
Card Address Selection

ELECTRICAL

- VCC = +5V ± 5%
  ICC = 325 mA maximum (210 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications
- Each output port line can drive 20 LSTTL loads.
- 16-pin DIP sockets are provided for access to Output Port bit lines. The diagram below shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width for ribbon cable access to output port sockets (connector dependent).
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T & B Ansley Catalog No. 609-MH165H or equivalent.



7602 Output Port Socket

STD/7602 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*			32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PC I	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

7602 Edge Connector Pin List

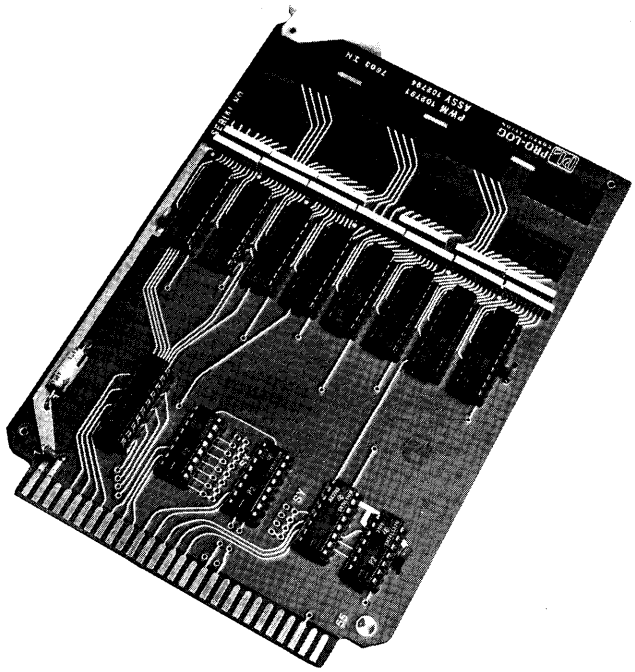
7603 INPUT PORT CARD

TTL INPUT PORT CARD

This card provides eight 8-bit gated input ports (64 input lines).

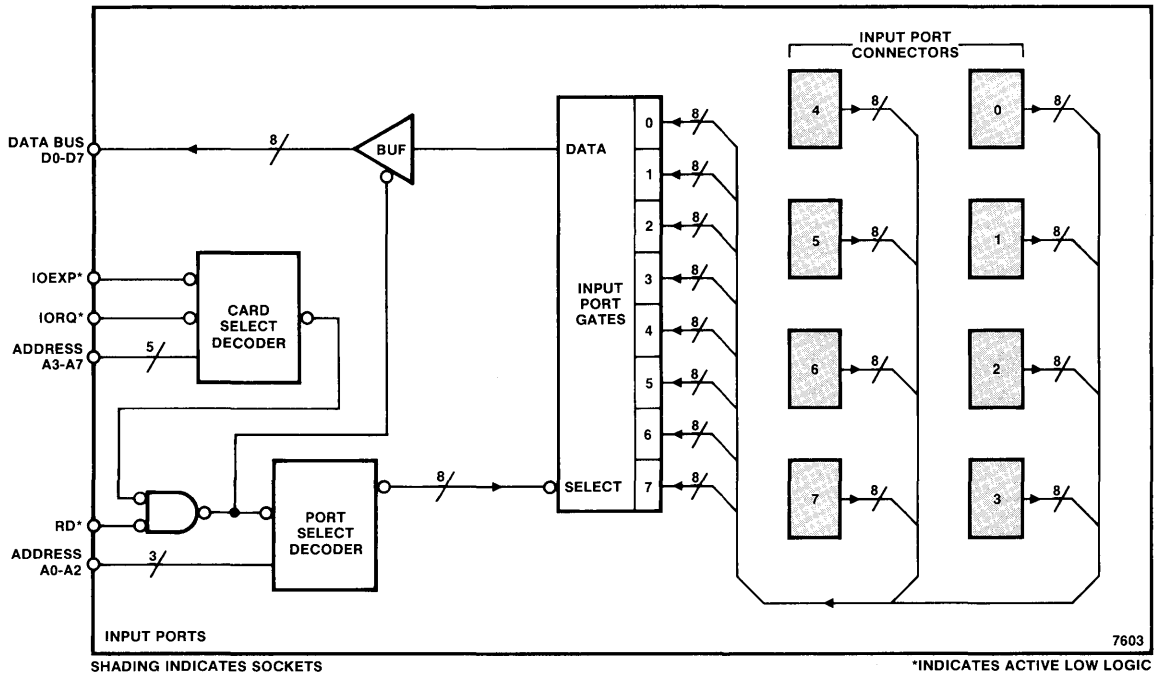
Input port lines are accessed at 16-pin DIP sockets on the card. The input lines are TTL compatible with an input rating of 4 low-power Schottky TTL loads.

The 7603 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows users to establish the eight consecutive input port addresses occupied by the 7603.



FEATURES

- **User selectable port address (256 port field)**
- **Input rating of 4 low-power Schottky TTL loads.**
- **Provision for expansion and memory mapping**
- **Input buffers have 200 MV of hysteresis**
- **Input lines include 4.7K pullups**
- **All IC's socketed**
- **Single +5V operation**



7603, INPUT PORT CARD

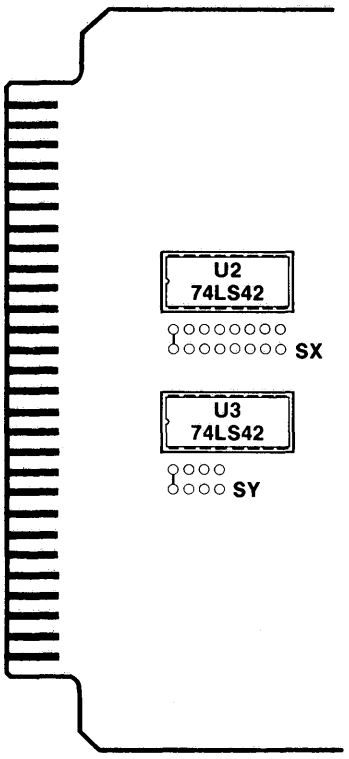
FUNCTIONAL

Card Address Mapping

The 7603 card is selected by a decoded combination of address lines A3-A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U2 and U3 (See Diagram). The 7603 is shipped with Port address 00-07 Hexadecimal. To map the 7603 anywhere in the hexadecimal port address of 00-FF change the decoder outputs connected to SX and SY. To determine the appropriate address use the 8 address per card Port Mapping Scheme as defined in the Series 7000 STD BUS Technical Manual.

Port Addresses

Address lines A0, A1 and A2 select one of eight sequential input port addresses. The RD* input controls the input gating function.



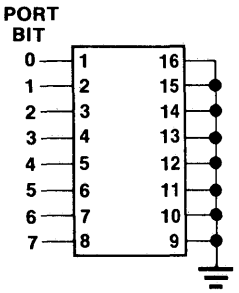
Card Address Selection

ELECTRICAL

- VCC = +5V ± 5%
  ICC = 525 mA maximum (350 mA typical)
- Address, Data and Control Busses meet all STD BUS general electrical specifications
- Each input port line presents 4 LSTTL loads
- 16-pin DIP sockets are provided for access to Input Port bit lines. The diagram below shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width for ribbon cable access to input port sockets (connector dependent).
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T and B Ansley Catalog No. 609-M165H or equivalent.



Input Port Socket

STD/7603 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)					OUTPUT (DRIVE)		
INPUT (LOADING)						INPUT (LOADING)	
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		60	8	7	60		D3
D6		60	10	9	60		D2
D5		60	12	11	60		D1
D4		60	14	13	60		D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		1	A1
A8			30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PC I	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

TTL INPUT/OUTPUT CARD

This card provides 8 ports of which any number can be input or output ports or output ports with readback (64 I/O lines total).

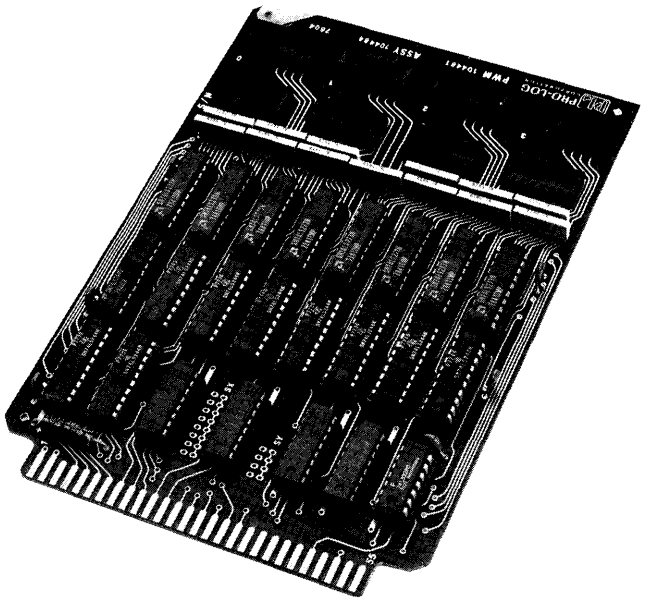
The ports are accessed at 16-pin DIP sockets on the card.

The output lines are TTL compatible with the ability to drive 16 low power Schottky TTL Loads each (4 TTL loads). A reset line is available to clear all output ports simultaneously.

The input lines are TTL compatible with an input rating of 4 low-power Schottky loads.

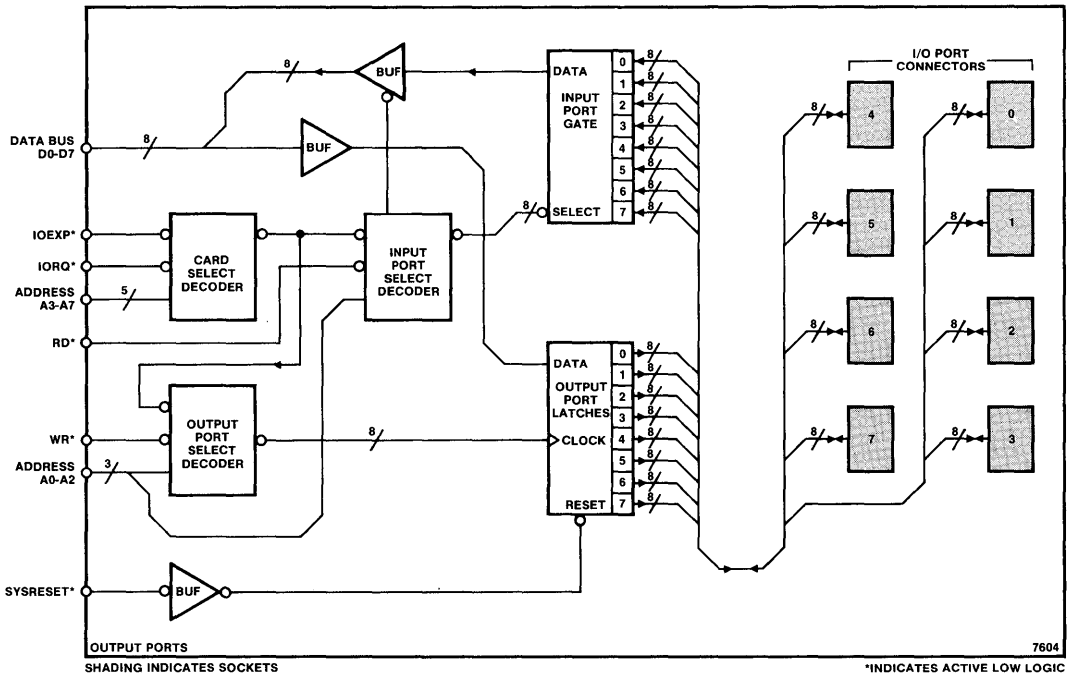
The ports are configured as input or output ports simply by removing the unused IC associated with that port. If the input buffer is retained, output port data may be read back into the Processor.

The 7604 decodes eight address lines with provisions for expansion and memory mapping. An on-card jumper system allows users to establish the eight consecutive port addresses occupied by the 7604.



FEATURES

- **8 Ports configurable as input or output or output with readback**
- **User selectable port address (256 port field)**
- **Outputs Drive 16 low-power Schottky TTL loads**
- **Provision for expansion and memory mapping**
- **All IC's socketed**
- **Single +5V operation**



7604 TTL I/O CARD

FUNCTIONAL

The 7604 is shipped fully populated. The card is customized (to A input and B output ports such that A + B = 8 ports) by removing the unused input buffer or output port latch according to the following table.

	OUTPUT PORTS	INPUT PORTS
PORT NO.	IC NUMBER	IC NUMBER
Port 0	U17	U9
Port 1	U19	U11
Port 2	U21	U13
Port 3	U23	U15
Port 4	U16	U8
Port 5	U18	U10
Port 6	U20	U12
Port 7	U22	U14

Leaving the input buffer in at output ports allows the Processor to read back the output port data to check for noise alteration or to use the output port as a data register.

Card Address Mapping

The 7604 Card is selected by a decoded combination of address lines A3-A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U3 and U4 (see diagram). The 7604 is shipped mapped at Hex Port Address 00. To map the 7604 anywhere in the hexadecimal address range 00 to FF, change the decoder outputs connected to SX and SY. To determine the appropriate connections for a desired port address, use the 8 address per card Mapping Scheme as defined in the Series 7000 STD BUS Technical Manual.

Port Addresses

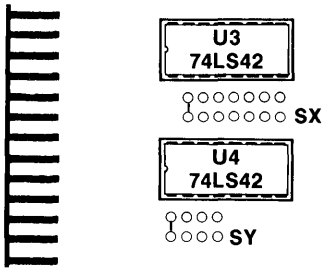
Address lines A0, A1 and A2 select one of eight Port addresses. One input port and one output port reside at each address. The RD* and WR* inputs control the input gating and output latch functions.

ELECTRICAL

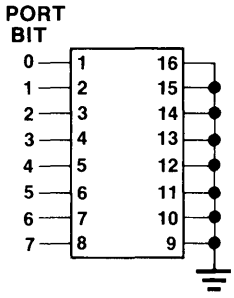
- VCC = +5V ± 5%
- ICC = 700 mA maximum (450 mA typical) for worst case conditions. Subtract 54 mA max. per input port and 27 mA per output port removed.
- Address, Data and Control Busses meet all STD BUS general electrical specifications except A0, A1 and A2 which are 2 LSTTL loads each.
- Each input port line presents 4 LSTTL loads.
- 16-pin DIP sockets are provided for access to input port bit lines. The diagram to the right shows the pin connections to these sockets for each port.

MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width for ribbon cable access to ports (connector dependent).
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T and B Ansley Catalog No. 609-M165H or equivalent.



Card Address Selection



Input/Output Port Socket

STD/7604 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)				OUTPUT (DRIVE)			
INPUT (LOADING)				INPUT (LOADING)			
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	60	8	7	60	1	D3
D6	1	60	10	9	60	1	D2
D5	1	60	12	11	60	1	D1
D4	1	60	14	13	60	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

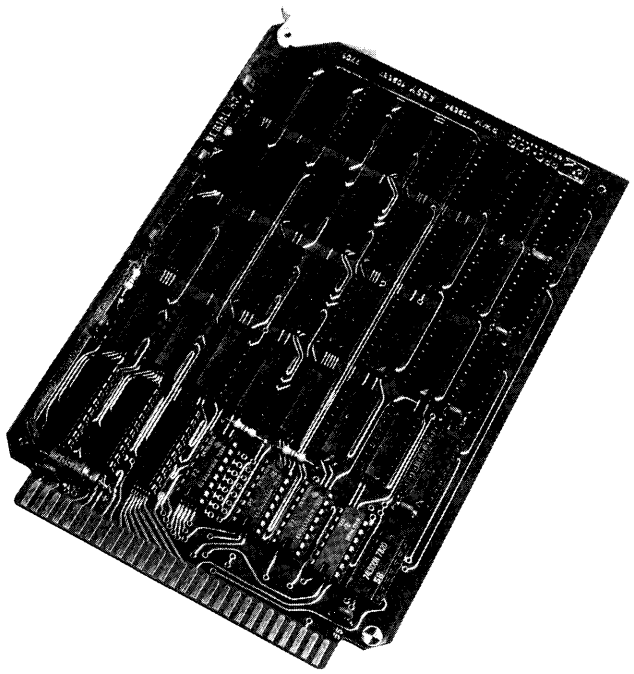
Edge Connector Pin List

7701 MEMORY CARD

16K BYTE STATIC RAM MEMORY CARD

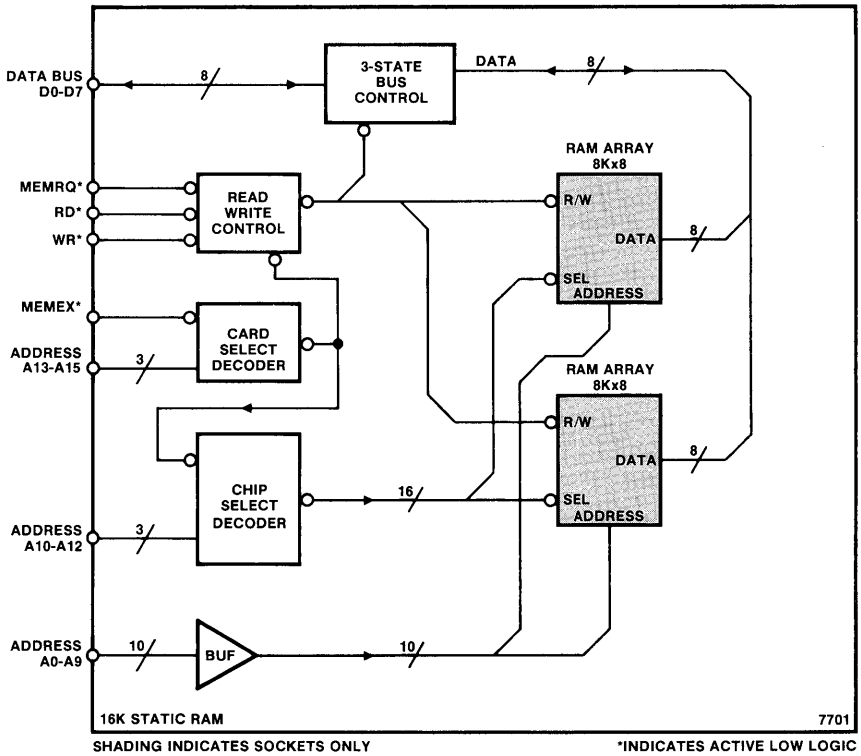
This card provides sockets for up to 16,384 bytes of Read-Write or PROM Memory. The card uses 2114 type RAMs or equivalent and has sockets for 16 pairs of RAMs. Alternately the card will accept 3625 type PROMs or equivalent. PROMs and RAMs can not be mixed on the same card.

The 7701 decodes 16 address lines, and can be mapped into either 8K or 16K bytes of consecutive address space. An on-card jumper system allows users to establish which 16K segment of a 64K microprocessor memory each 7701 occupies.



FEATURES

- **Sockets for 16K bytes of 2114L RAMs or 3625 PROMs**
- **User selectable card address**
- **All STD BUS lines buffered**
- **Minimal logic bus loading**
- **All IC's socketed**
- **Single +5V operation**
- **Use Pro-Log D1004, 1Kx8 memories (two 2114L's)**



SHADING INDICATES SOCKETS ONLY

*INDICATES ACTIVE LOW LOGIC

7701, MEMORY CARD

FUNCTIONAL

Card Address Mapping

The 7701 is organized as two blocks of consecutive RAM address segments containing 8,192 8-bit words. Each segment of RAM is enabled by a unique decoded combination of address lines A13, A14 and A15. The user chooses the address combinations of the 8K segments by connecting one jumper wire to SX and one jumper wire to SY from two of the eight decoder outputs. The illustration shows the pad matrix adjacent to U4 used to map the memory. The 7701 is shipped with S4 connected to SX and S5 connected to SY with the card responding to Hex addresses 8000-9FFF and A000-BFFF respectively. To map the card at a different address segment use the 1K Memory Block mapping scheme as defined in the Series 7000 STD BUS Technical Manual.

The card can occupy one 8K address block with only one select line (SX or SY) connected, or it can occupy two separate 8K blocks or a single consecutive 16K block.

Note that the card's data bus drivers are enabled anytime a valid address is present even if memory chips are not plugged in. The card address range is chosen to prevent bus contention with other system memory elements including Processor on-card memory, other memory cards and memory mapped I/O.

Plug-in RAMs

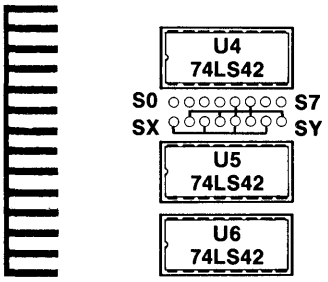
Sockets are provided for thirty-two type 2114 RAM devices. Each pair of these 1024x4 devices adds 1K 8-bit bytes of RAM, which are designated Memory Blocks 0-7 (MB0-MB7). Insert the RAMs to add memory according to the following table. If the memory card mapping is changed use the table below and the Memory Address Map and Jumper Selection for 1K memory blocks to determine the new address range of each memory block.

MAPPED BY LINE SX					
RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED	RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED
U9, U17	MB0	8000-83FF	U13, U21	MB4	9000-93FF
U10, U18	MB1	8400-87FF	U14, U22	MB5	9400-97FF
U11, U19	MB2	8800-8BFF	U15, U23	MB6	9800-9BFF
U12, U20	MB3	8C00-8FFF	U16, U24	MB7	9C00-9FFF

MAPPED BY LINE SY					
RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED	RAM SOCKETS	MEMORY BLOCK	ADR RANGE AS SHIPPED
U25, U33	MB0	A000-A3FF	U29, U37	MB4	B000-B3FF
U26, U34	MB1	A400-A7FF	U30, U38	MB5	B400-B7FF
U27, U35	MB2	A800-ABFF	U31, U39	MB6	B800-BBFF
U28, U36	MB3	AC00-AFFF	U32, U40	MB7	BC00-BFFF

PROM Option

The 7701 will accept type 3625 PROMs in place of 2114 RAMs with an increase in card power consumption. PROMs and RAMs may not be mixed on the same card.



Card Address Selection

ELECTRICAL

- VCC = +5V ± 5%
  ICC = 2.08A maximum (1.6A Typical) with RAM sockets fully loaded (65 mA per RAM maximum).
- Address, Data and Control Busses meet all STD BUS general electrical specifications except:
  A10, A11, A12 - These address bus inputs present 2 LSTTL loads maximum each.

MECHANICAL

- Meets all STD BUS general mechanical specifications.

STD/7701 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)		PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	60	8	7	60	1	D3
D6	1	60	10	9	60	1	D2
D5	1	60	12	11	60	1	D1
D4	1	60	14	13	60	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	2		22	21		1	A4
A11	2		24	23		1	A3
A10	2		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*	1		34	33			IORQ*
MEMEX*	1		36	35			IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

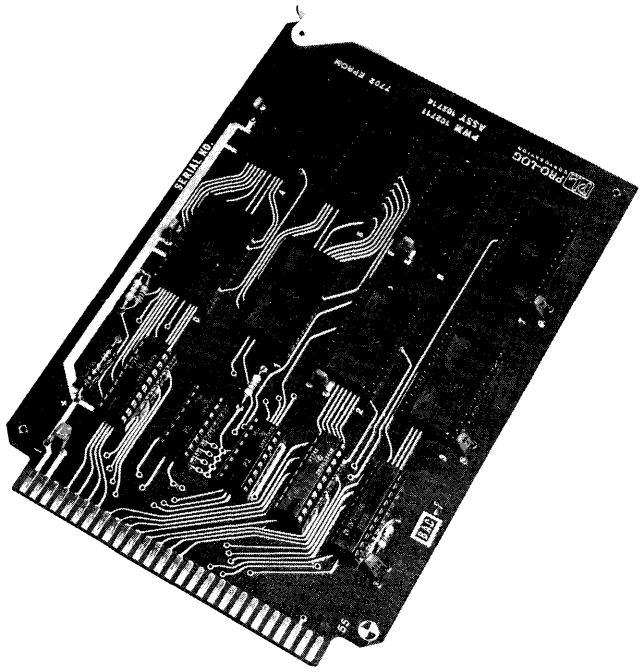
Edge Connector Pin List

7702 MEMORY CARD

16K BYTE 2716 EPROM MEMORY CARD

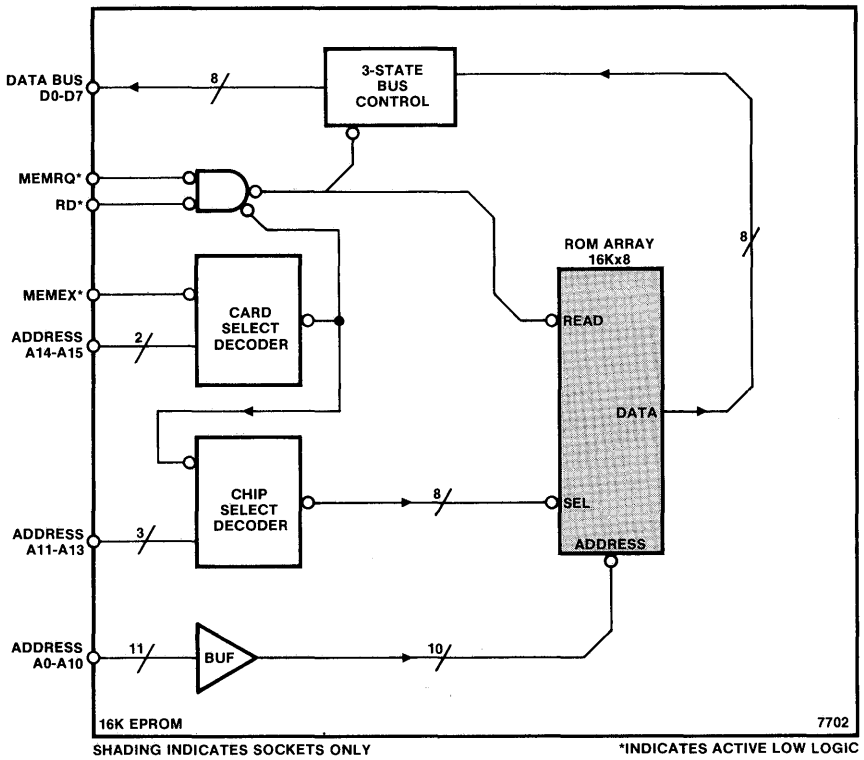
This card provides sockets for up to 16,384 bytes of EPROM memory. The card uses 2716 EPROMs or equivalent and has sockets for 8 EPROMs.

The 7702 decodes 16 address lines and occupies 16K consecutive addresses. An on-card jumper system allows users to establish which quadrant of a 65K microprocessor memory each 7702 occupies.



FEATURES

- **Sockets for 16K bytes ROM (2716 EPROMs)**
- **User selectable card address**
- **All STD BUS lines buffered**
- **Minimal logic bus loading**
- **All IC's socketed**
- **Single +5V operation**
- **Use Pro-Log D2002 2Kx8 EPROMs**



SHADING INDICATES SOCKETS ONLY

*INDICATES ACTIVE LOW LOGIC

FUNCTIONAL

Card Address Mapping

The 7702 is organized as one block of 16,384 consecutive EPROM addresses. The card is enabled by a decoded combination of address lines A14 and A15. The user chooses the card address combination by connecting a jumper wire to SX from one of four decoder outputs at a pad matrix adjacent to U2 (see diagram). The card is shipped with X1 connected to SX and therefore responds to Hex addresses 4000-7FFF. To map the memory to respond to a different segment of addresses use the 2K Memory Block mapping scheme as defined in the Series 7000 STD BUS Technical Manual.

Note that the card's data bus drivers are enabled anytime a valid address is present even if memory chips are not plugged in .The card address range is chosen to prevent bus contention with other system memory elements including Processor on-card memory, other memory cards and memory mapped I/O.

Plug-in EPROMs

Sockets numbered 0 through 7 are provided for eight +5V 2716 EPROM devices. Each of these 2048x8 devices adds 2K bytes of Read Only Memory, designated Memory Blocks 0-7 (MB0-MB7). Insert EPROMs to add memory blocks according to the following table. If the memory card mapping is changed use the table below and the Memory Address Map and Jumper Selection Table for 2K memory blocks to determine the new address range of each memory block.

ROM SOCKET	BLOCK MEMORY	ADDRESS RANGE AS SHIPPED
0	MB0	4000-47FF
1	MB1	4800-4FFF
2	MB2	5000-57FF
3	MB3	5800-5FFF
4	MB4	6000-67FF
5	MB5	6800-6FFF
6	MB6	7000-77FF
7	MB7	7800-7FFF

ROM Option

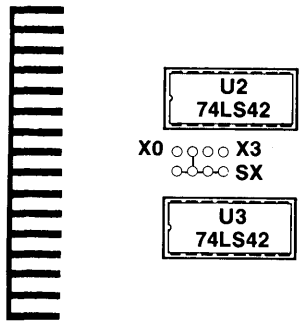
Type 2316E masked ROMs may be used in any combination with 2716 erasable PROMs. 2316E's increase card power consumption.

ELECTRICAL

- VCC = +5V ±5%
  ICC = 300 mA maximum (200 mA typical) with EPROM sockets fully loaded (100 mA maximum per EPROM selected, 25 mA standby)

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- All EPROM sockets accept Pro-Log SZ-24 ZIF sockets for PROM program development.



Card Address Selection

STD/7702 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)				OUTPUT (DRIVE)			
INPUT (LOADING)				INPUT (LOADING)			
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7		60	8	7	60		D3
D6		60	10	9	60		D2
D5		60	12	11	60		D1
D4		60	14	13	60		D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31			WR*
MEMRQ*	1		34	33			IORQ*
MEMEX*	1		36	35			IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47			SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

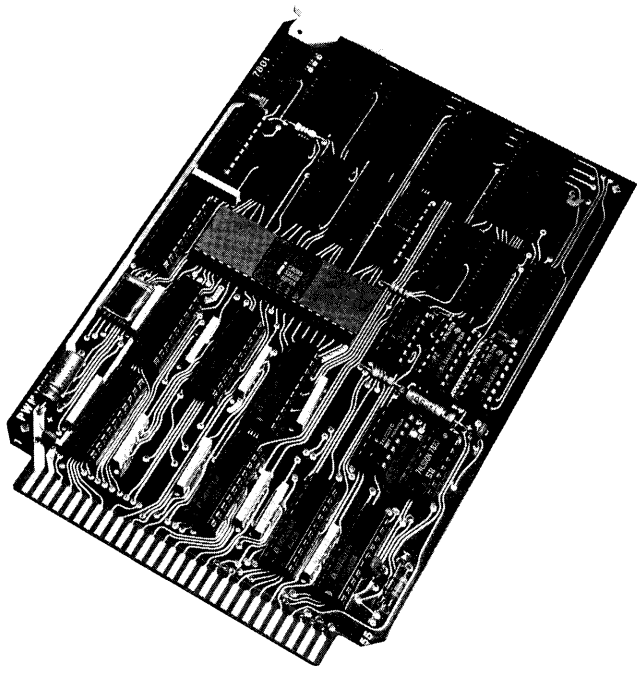
Edge Connector Pin List

7801 PROCESSOR CARD

8085A PROCESSOR CARD

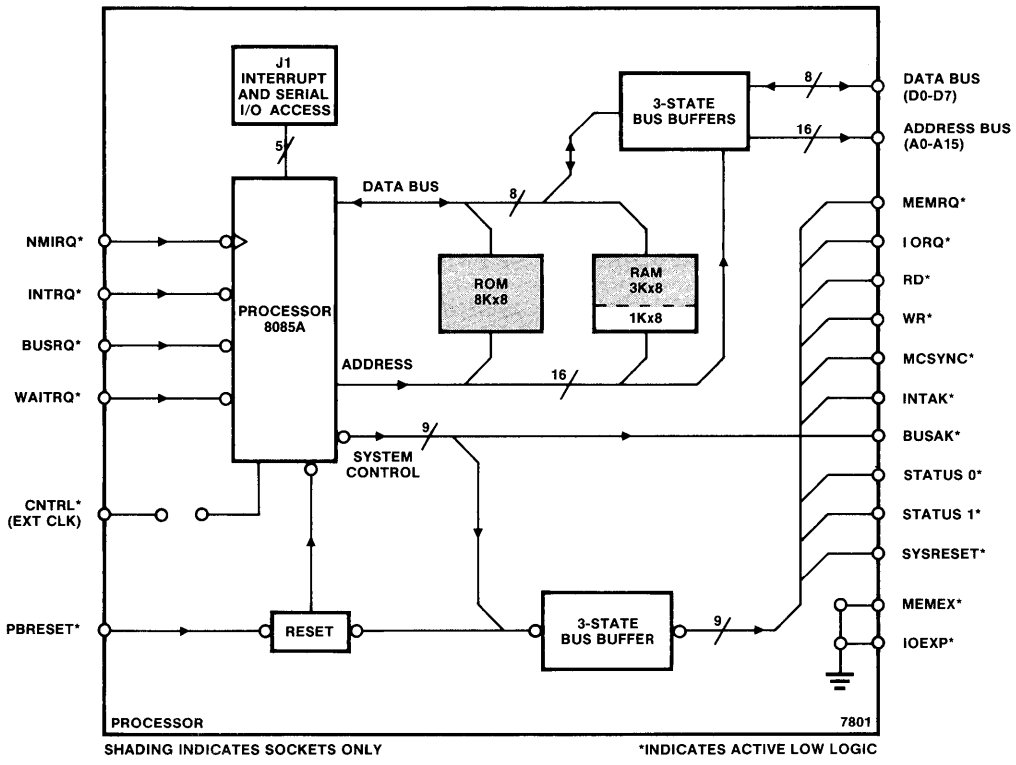
This card combines a buffered and fully expandable 8085A microprocessor with onboard RAM and PROM sockets.

The 7801 includes 1K byte of RAM with sockets for up to 4K, and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7801 card can be expanded to full 8085A memory and I/O capability. The 7801 STD BUS interface may be disabled for DMA and multiprocessor applications.



FEATURES

- **8085A Processor**
- **4096 bytes RAM capacity onboard**
- **1024 bytes RAM included**
- **8192 bytes ROM capacity onboard**
- **3 State Address, Data, Control Buses**
- **Crystal controlled 320 ns clock**
- **Power-on reset or pushbutton reset input**
- **Five interrupts**
- **Serial I/O lines**
- **All IC's socketed**
- **Single +5V operation**
- **Use Pro-Log D1004 1Kx8 memories (two 2114L's)**



SHADING INDICATES SOCKETS ONLY

*INDICATES ACTIVE LOW LOGIC

7801, PROCESSOR CARD

FUNCTIONAL

- Executes all of the 8080 and 8085A Processor Instructions
- Crystal Oscillator produces 320 nanosecond ± 0.05% time states. External clock input range 1 to 6 MHz, 25% to 50% duty cycle (card operates at ½ input frequency).
- DIP socket access to SID and SOD (Serial input/output data) and interrupts 5.5, 6.5, 7.5.
- Power-on reset and PBRESET* one-shot hold SYSRESET* active for 50 ms maximum.
- Sockets are provided for up to four +5V type 2716 EPROMs (8192 bytes total) which occupy HEX memory addresses 0000-1FFF (8K).
- Two Type 2114L RAMs (1024 bytes) included, with sockets for up to eight total RAM devices (4096 bytes total) which occupy HEX memory addresses 2000-2FFF (4K).
- Jumper pads are provided for disabling the onboard memory or remapping it from HEX memory addresses 0000-2FFF (12K) to C000-EFFF (12K). If any onboard memory is used, external memory cards may not be mapped in HEX memory address 0000-3FFF (16K) or C000-FFFF (16K) if onboard remapping option used.

ELECTRICAL

- VCC = +5V ± 5%
  ICC = 1.4A maximum (1.0 typical) with EPROM and RAM sockets fully loaded (100 mA per EPROM and 65 mA per RAM maximum).
- Address, Data and Control Busses meet STD BUS general electrical specifications except:
  WAITRQ* - Input loading 14 LSTTL loads maximum
  PBRESET* - Input capacitance 1.0 μF nominal.
  MEMEX*, IOEXP* - These bus lines are grounded on the 7801 by user removable traces.
- A 16-pin DIP socket is provided for access to the serial I/O lines and three additional interrupts. The interrupts and Serial Input Data (SID) each present 4 LSTTL loads, and Serial Output Data (SOD) can drive 60 LSTTL loads.

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- Normally requires one additional card slot width for ribbon cable access to J1.

*Indicates Active Low Level Logic

J1 SERIAL I/O INTERRUPT PIN LIST					
PIN NUMBER SIGNAL FLOW SIGNAL			PIN NUMBER SIGNAL FLOW SIGNAL		
INTR 7.5*	IN	1	16	OUT	GND
INTR 6.5*	IN	2	15	OUT	GND
INTR 5.5*	IN	3	14	OUT	GND
SOD*	OUT	4	13	OUT	GND
SID*	IN	5	12	OUT	GND
(SPARE)		6	11	OUT	GND
(SPARE)		7	10	OUT	GND
(SPARE)		8	9	OUT	GND

*Designates Active Low Level Logic

J1 Serial I/O Interrupt Pin List

STD/7801 EDGE CONNECTOR PIN LIST							
PIN NUMBER OUTPUT (DRIVE) INPUT (LOADING) MNEMONIC				PIN NUMBER OUTPUT (DRIVE) INPUT (LOADING) MNEMONIC			
+5 VOLTS	IN		2	1		IN	+5 VOLTS
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	5	55	8	7	55	5	D3
D6	5	55	10	9	55	5	D2
D5	5	55	12	11	55	5	D1
D4	5	55	14	13	55	5	D0
A15	5	55	16	15	55	5	A7
A14	5	55	18	17	55	5	A6
A13	5	55	20	19	55	5	A5
A12	5	55	22	21	55	5	A4
A11	5	55	24	23	55	5	A3
A10	5	55	26	25	55	5	A2
A9	5	55	28	27	55	5	A1
A8	5	55	30	29	55	5	A0
RD*	5	55	32	31	55	5	WR*
MEMRQ*	5	55	34	33	55	5	IORQ*
MEMEX* (GROUND)		OUT	36	35	OUT		IOEXP* (GROUND)
MCSYNC* (ALE*)	5	55	38	37			REFRESH*
STATUS 0* (S0*)	5	55	40	39	55	5	STATUS 1* (S1*)
BUSRQ*	5		42	41	55	5	BUSAK*
INTRQ*	5		44	43	55	5	INTAK*
NMIRQ*	5		46	45		14	WAITRQ*
PBRESET*	1 μF		48	47	55		SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

7802 PROCESSOR CARD

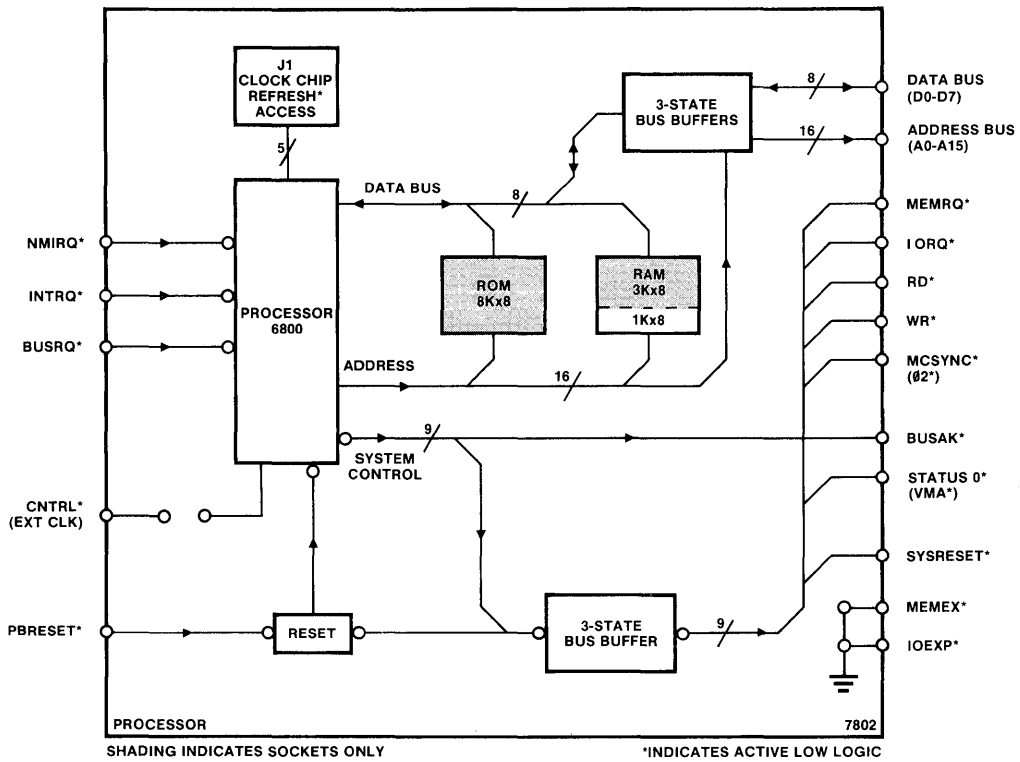
6800 PROCESSOR CARD

This card provides a buffered and fully expandable 6800 microprocessor with onboard RAM and PROM sockets.

The 7802 includes 1K byte of RAM with sockets for up to 4K, and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7802 may be expanded to the full memory and I/O capacity of the 6800. The STD BUS interface may be disabled for DMA and multiprocessor applications.

FEATURES

- **6800 Processor**
- **4096 bytes RAM capacity onboard**
- **1024 bytes RAM included**
- **8192 bytes ROM capacity onboard**
- **3 state Address, Data, Control Buses**
- **Crystal controlled 1 μs clock**
- **Power-on reset and pushbutton reset input**
- **STD BUS compatible I/O mapping**
- **Standard and custom memory and I/O remapping options**
- **All IC's socketed**
- **Single +5V operation**
- **Use Pro-Log D1004 1Kx8 memories (two 2114L's)**



7802, PROCESSOR CARD

FUNCTIONAL

- Executes all of the 6800 Processor instructions
- Crystal oscillator produces 1.0 microsecond ± 0.05% clock cycles. External clock input range 0.4 to 4.0 MHz, 50% duty cycle (card operates at ¼ input frequency).
- Power-on reset holds SYSRESET* active for 50 ms maximum. Provision is made for protection of external dynamic RAM during PBRESET* (pushbutton reset).
- Sockets are provided for up to four +5V type 2716 EPROMs (8192 bytes total) which occupy HEX memory addresses D000-DFFF (4K).
- The 7802 generates IORQ* (I/O request) when HEX memory page address 00 is decoded, providing for 256 each input and output ports (2048 input and 2048 output lines total) on external I/O cards. This provides compatibility with Series 7000 I/O cards which are addressed by A0-A7 only, and does not preclude the use of memory mapped I/O cards.
- An I/O and RAM remapping option is provided for the user. This option moves the I/O allocation from HEX memory page 00 to page D0, and moves RAM from HEX memory address D000-DFFF (4K) to addresses 0000-0FFF (4K). This permits either I/O or RAM to be used with the 6800's base page memory direct instructions.
- Replacement of a field programmable PROM on the 7802 allows the user to disable the 7802's 12K onboard memory, or to remap all system I/O and memory by memory page without restriction.

ELECTRICAL

- VCC = +5V ± 5%
- ICC = 1.85 maximum (1.25 typical) with EPROM and RAM sockets fully loaded (100 mA per EPROM and 65 mA per RAM maximum).
- Address, Data and Control Busses meet STD BUS general electrical specifications, except:
  WAITRQ* - This line is not connected on the 7802 because its function is duplicated by the BUSRQ* line.
  PBRESET* - Input capacitance 0.5 μF nominal. This line is recommended for momentary grounding by pushbutton.
  MEMEX*, IOEXP* - These bus lines are grounded on the 7802 by user removable jumper traces.
- A 16-pin DIP socket is provided for access to certain MC6875 clock chip inputs and the 7802's tristatable REFRESH* buffer as shown at right.

MECHANICAL

- Meets all STD BUS general mechanical specifications.
- Normally requires one additional card slot width for ribbon cable access to the DIP socket described above.

STD/7802 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5 VOLTS	IN		2	1		IN	+5 VOLTS
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	5	55	8	7	55	5	D3
D6	5	55	10	9	55	5	D2
D5	5	55	12	11	55	5	D1
D4	5	55	14	13	55	5	D0
A15	5	55	16	15	55	5	A7
A14	5	55	18	17	55	5	A6
A13	5	55	20	19	55	5	A5
A12	5	55	22	21	55	5	A4
A11	5	55	24	23	55	5	A3
A10	5	55	26	25	55	5	A2
A9	5	55	28	27	55	5	A1
A8	5	55	30	29	55	5	A0
RD*	5	55	32	31	55	5	WR*
MEMRQ*	5	55	34	33	55	5	IORQ*
MEMEX* (GROUND)		OUT	36	35	OUT		IOEXP* (GROUND)
MCSYNC* (02*)	5	55	38	37	[60]		REFRESH* (DRIVER)
STATUS 0* (VMA*)	5	55	40	39			STATUS 1*
BUSRQ*	5		42	41	55	5	BUSAK*
INTRQ*	5		44	43			INTAK*
NMIRQ*	5		46	45			WAITRQ*
PBRESET*	0.5μF		48	47	55	5	SYSRESET*
CNTRL* (EXT CLK)	[1]		50	49			CLOCK*
PCI	IN		52	51		OUT	PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic
[] Brackets Indicate User Optional Connection

Edge Connector Pin List

DIP SOCKET J1 PIN LIST					
PIN NUMBER	SIGNAL FLOW	SIGNAL	PIN NUMBER	SIGNAL FLOW	SIGNAL
MC6875 DMA*	IN	1	16	OUT	LOGIC GROUND
MC6875 MEM RDY	IN	2	15	OUT	LOGIC GROUND
SPARE	IN/OUT	3	14	OUT	LOGIC GROUND
SPARE	IN/OUT	4	13	OUT	LOGIC GROUND
SPARE	IN/OUT	5	12	OUT	LOGIC GROUND
SPARE	IN/OUT	6	11	OUT	LOGIC GROUND
SPARE	IN/OUT	7	10	OUT	LOGIC GROUND
EXTERNAL REFRESH*	IN	8	9	OUT	LOGIC GROUND

*Designates Active Low Level Logic

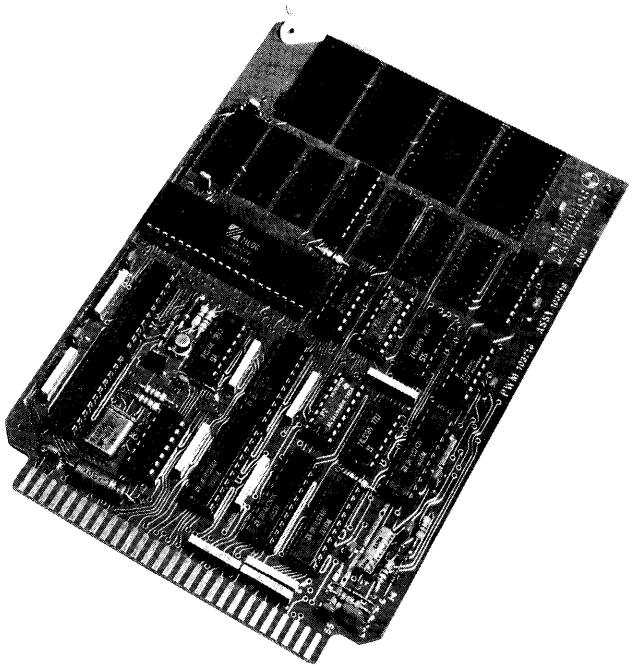
Dip Socket J1 Pin List

7803 PROCESSOR CARD

Z-80 PROCESSOR CARD

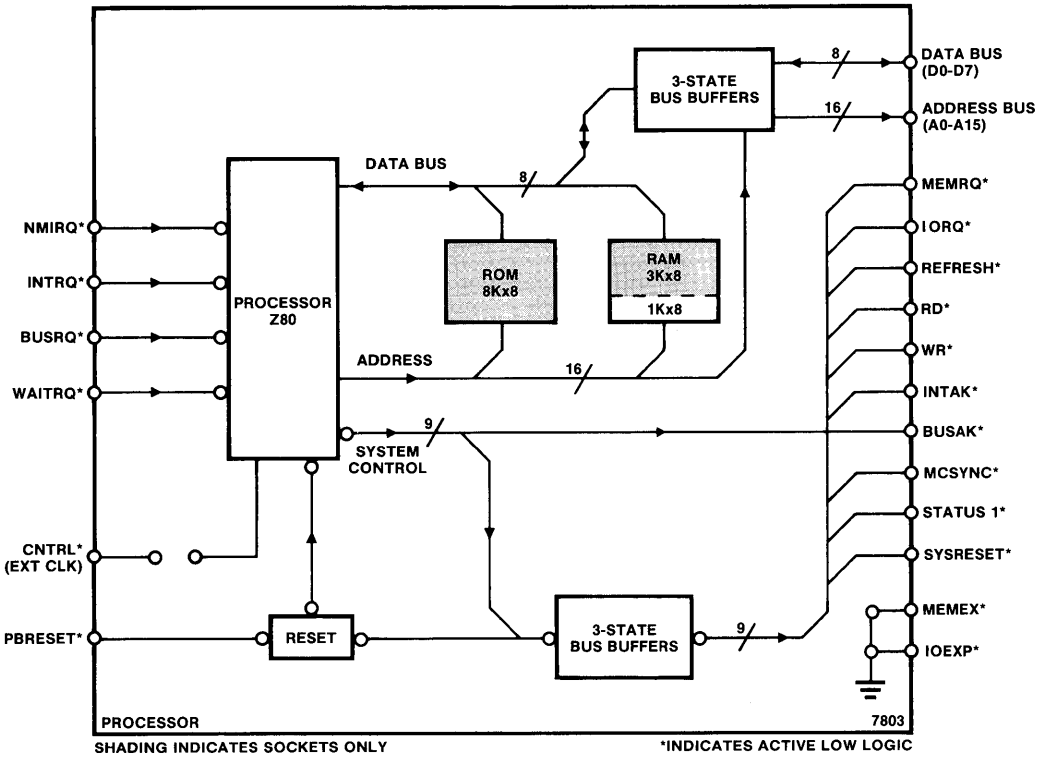
This card combines a buffered and fully expandable Z-80 microprocessor with onboard RAM and PROM sockets.

The 7803 includes 1K byte of RAM with sockets for up to 4K bytes and sockets for up to 8K bytes of ROM or EPROM. An STD BUS system using the 7803 card can be expanded to the full Z-80 memory and I/O capability. The 7803 STD BUS interface may be disabled for DMA and multiprocessor applications.



FEATURES

- **Z-80 Processor**
- **4096 bytes RAM capacity (2114)**
- **1024 bytes RAM included**
- **8192 bytes ROM capacity onboard (2716 EPROM)**
- **3 State Address, Data, Control Bus**
- **Crystal controlled 400 ns clock**
- **Power-on reset or pushbutton reset input**
- **Dynamic RAM refresh control**
- **All IC's socketed**
- **Single +5V operation**
- **Use Pro-Log D1004 1Kx8 memories (two 2114L's)**



7803, PROCESSOR CARD

FUNCTIONAL

- Executes all of the 8080 and Z80 Processor instructions.
- Crystal oscillator produces 400 nanosecond ± 0.05% time states.
- SYSRESET* is activated by either power-on or the PBRESET* input. The power-on one-shot holds SYSRESET* low for 50 ms maximum. PBRESET* is intented for momentary grounding by pushbutton and is synchronized to the processor timing. This input holds SYSRESET* low for 10 μs maximum to allow a manual processor reset without excessive interruption of the REFRESH* output to dynamic memories.
- Sockets are provided for up to four +5V type 2716 EPROMs (8192 bytes total) which occupy HEX memory address 0000 to 1FFF (8K).
- Two type 2114 RAMs (1024 bytes) included, with sockets for up to eight total RAM devices (4096 bytes total) which occupy HEX memory addresses 2000-2FFF (4K).
- Jumper pads are provided for disabling the onboard memory or remapping it from HEX memory addresses 0000-2FFF (12K) to C000-EFFF. If any onboard memory is used, external memory cards may not be mapped in HEX memory addresses 0000-3FFF (16K), or C000-FFFF (16K) if onboard remapping option used.

ELECTRICAL

- VCC = +5V ±5%
  ICC = 1.65 maximum (1.15A typical) with EPROM and RAM sockets fully loaded (100 mA per EPROM and 65 mA per RAM maximum).
- Address, Data and Control Busses meet STD BUS general electrical specifications except:
  PBRESET* - Input loading is 15 LSTTL loads. This line is recommended for momentary grounding by pushbutton.
  MEMEX*, IOEXP* - These bus lines are grounded on the 7803 by user removable jumper traces.

MECHANICAL

- Meets all STD BUS general mechanical specifications.

*Indicates Active Low Logic

STD/7803 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC	PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)	MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	5	55	8	7	55	5	D3
D6	5	55	10	9	55	5	D2
D5	5	55	12	11	55	5	D1
D4	5	55	14	13	55	5	D0
A15	5	55	16	15	55	5	A7
A14	5	55	18	17	55	5	A6
A13	5	55	20	19	55	5	A5
A12	5	55	22	21	55	5	A4
A11	5	55	24	23	55	5	A3
A10	5	55	26	25	55	5	A2
A9	5	55	28	27	55	5	A1
A8	5	55	30	29	55	5	A0
RD*	5	55	32	31	55	5	WR*
MEMRQ*	5	55	34	33	55	5	IORQ*
MEMEX* (GROUND)		OUT	36	35	OUT		IOEXP* (GROUND)
MCSYNC* (RD*+WR*+INTA*)	5	55	38	37	55	5	REFRESH*
STATUS 0*			40	39	55	5	STATUS 1* (M2*)
BUSRQ*	5		42	41	55	5	BUSAK*
INTRQ*	5		44	43	55	5	INTAK*
NMIRQ*	5		46	45		5	WAITRQ*
PBRESET*	15		48	47	55	5	SYSRESET*
CNTRL*			50	49	55	5	CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

7901
UTILITY CARD EXTENDER

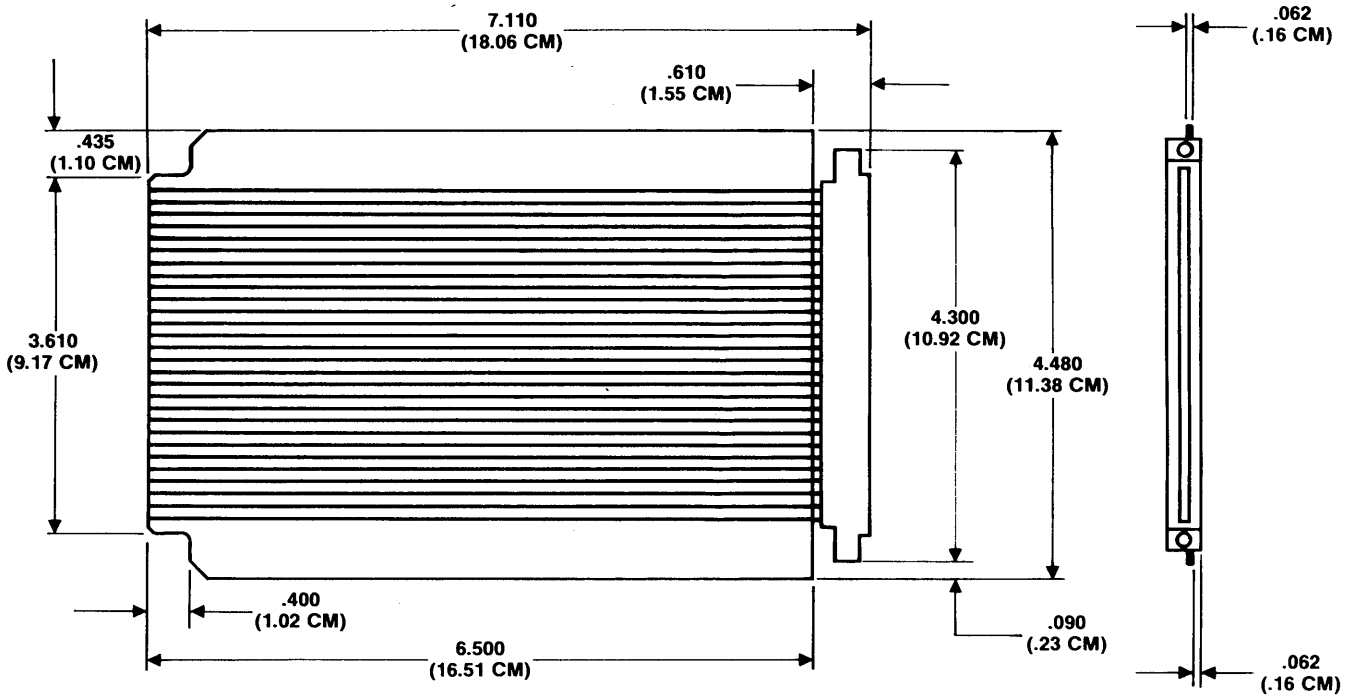
A printed circuit card for extending cards out of the card cage for easy access. The 7901 (8411, P560) card extender can be used with all Pro-Log edge connected cards.

CARD DIMENSIONS

- 4.48 in. (11.38 cm) high by 7.11 (18.06 cm) long
- 0.062 in. (0.16 cm) printed circuit board thickness

CONNECTOR REQUIREMENTS

56 pin, 28 position, dual readout on 0.125 inch (0.318 cm) pin centers. See CW56, CW56-1 Edge Card Connector Data Sheet.

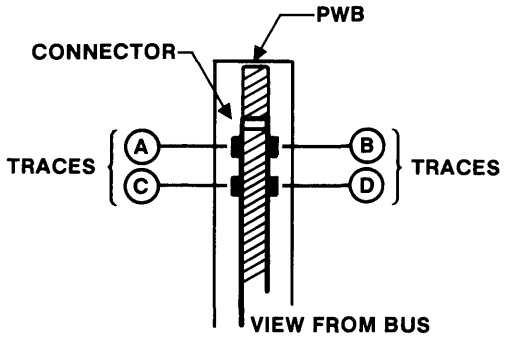


MAX TRACE TO TRACE CAPACITANCE INCLUDING THE CONNECTOR	
A-B	13 pf
A-C	7 pf
A-D	6 pf

Maximum current per trace and contact: 1 Amp

Maximum insertion resistance: 10 milli Ω/contact and 60 mΩ per trace.

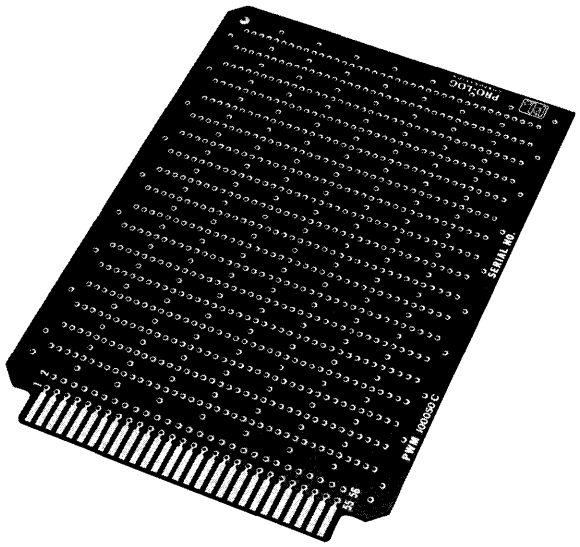
For connector specifications see CW56 Connector Data Sheet.



STD BUS Card Edge Connector Configuration

UTILITY DIP CARD

A printed circuit card for prototyping with Dual-in-line (DIP) packaging. Accommodates 8, 14, 16 and 18 pin DIPs on 0.300 inch (0.76 CM) centers and 24, 28 and 40 pin DIPs on 0.600 inch (1.52 CM) centers. Card has printed power distribution bus. Plated-thru holes accommodate 0.025 inch (0.76 CM) square posts for wrapped wire connection.



CARD DIMENSIONS

- 4.48 in. (11.38 cm) high by 6.5 in. (16.5 cm) long
- 0.062 in. (0.16 cm) printed circuit board thickness
- 0.035 in. (0.09 cm) diameter plated-thru holes

CONNECTOR REQUIREMENTS: 56 pin, 28 position, dual readout on 0.125 inch (0.32 CM) centers. See CW56, CW56-1 Edge Card Connector data sheet.

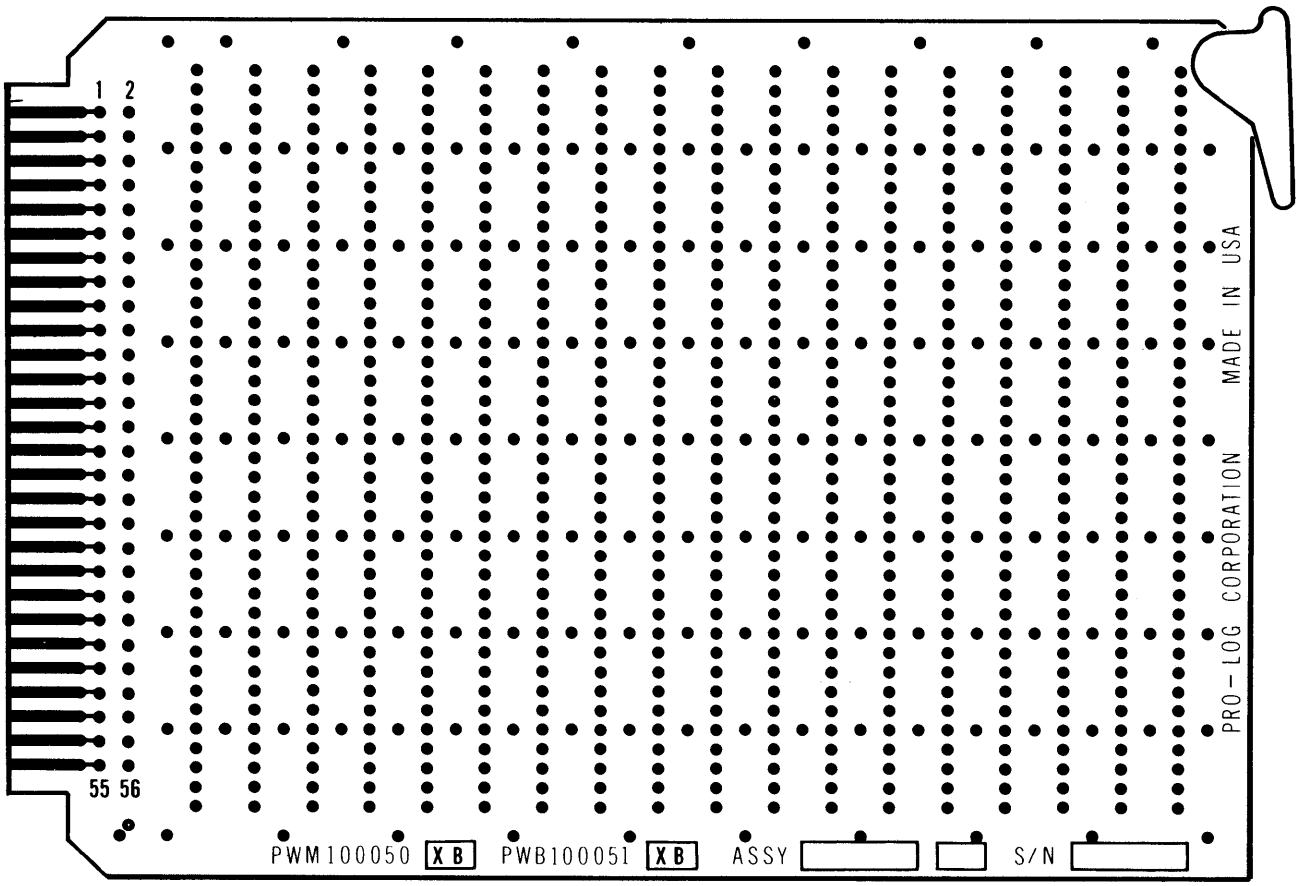
APPLICATION NOTES

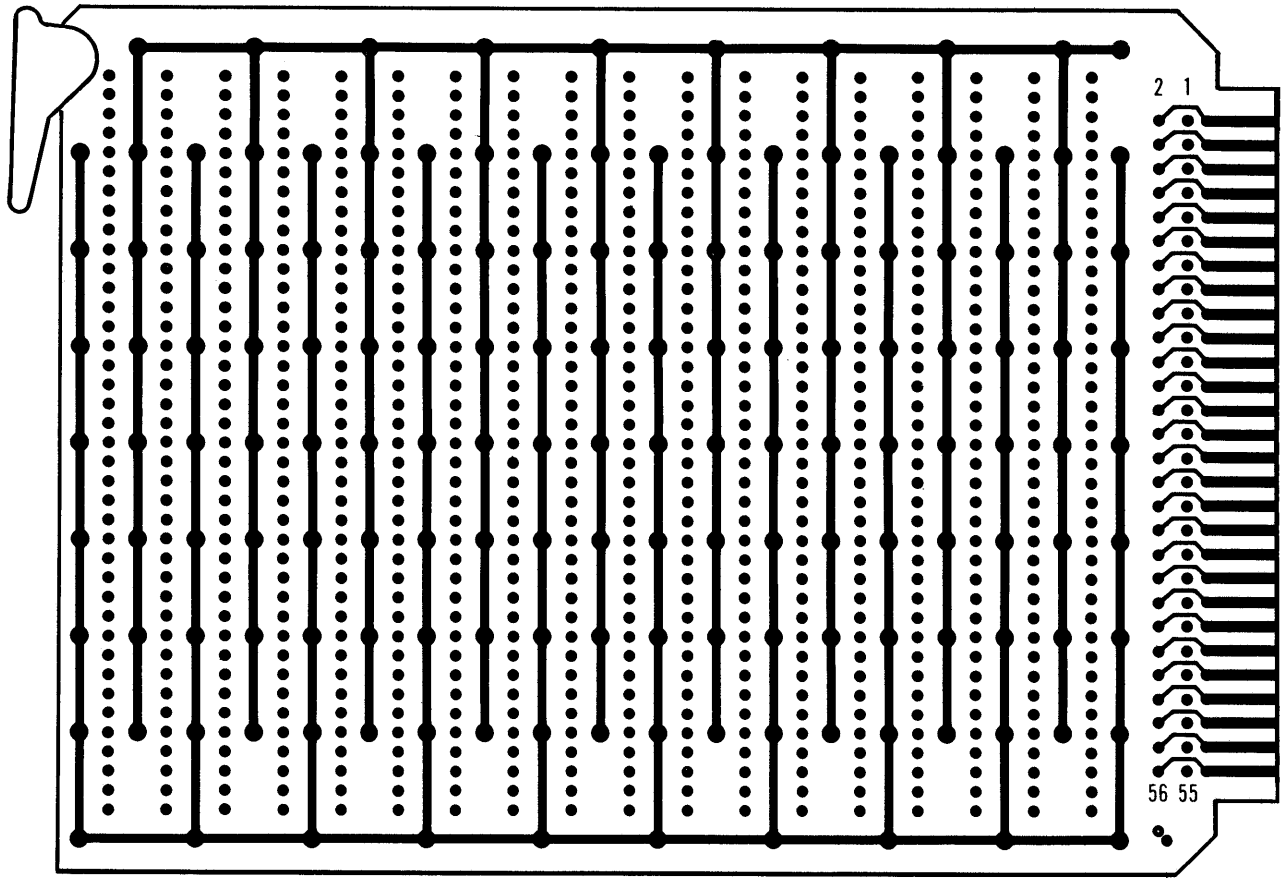
For wire-wrapping; insert wrap sockets in desired position. Solder two or more pins to pads to hold socket. For connections to card-edge fingers, power bus or mounting of discrete components solder wire-wrap stakes in desired holes. Suitable wrap stakes can be obtained from Vector Electronics Company, Inc., part number T-44.

For direct soldering of components, insert component at desired location. Solder wires direct to protruding component leads.

7902, UTILITY DIP CARD

COMPONENT SIDE





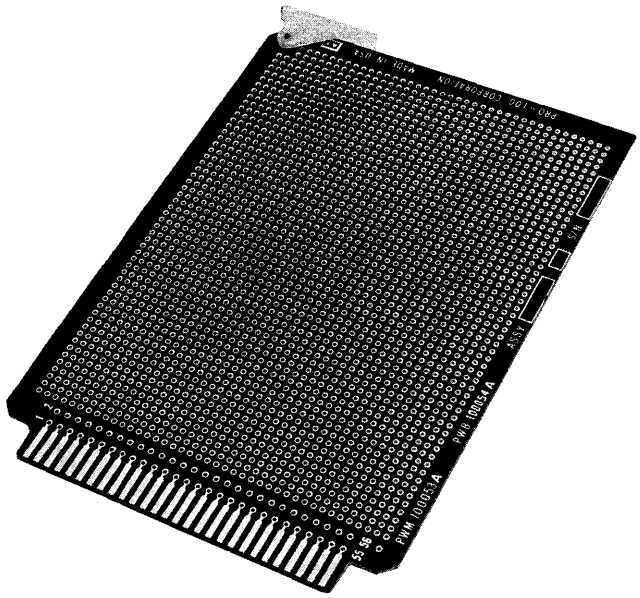
SHOWN ACTUAL SIZE

WIRE SIDE

7903 GENERAL UTILITY CARD

GENERAL UTILITY CARD

A printed circuit card for prototyping with 0.100 inch (0.25 CM) grid hole pattern. Accommodates discrete components or Dual-in-line (DIP) packaging. Plated-thru holes accommodate 0.025 inch (0.06 CM) square posts for wrapped wire connections.



CARD DIMENSIONS

- 4.48 in. (11.38 cm) high by 6.5 in. (16.5 cm) long
- 0.062 in. (0.16 cm) printed circuit board thickness
- 0.035 in. (0.09 cm) diameter plated-thru holes

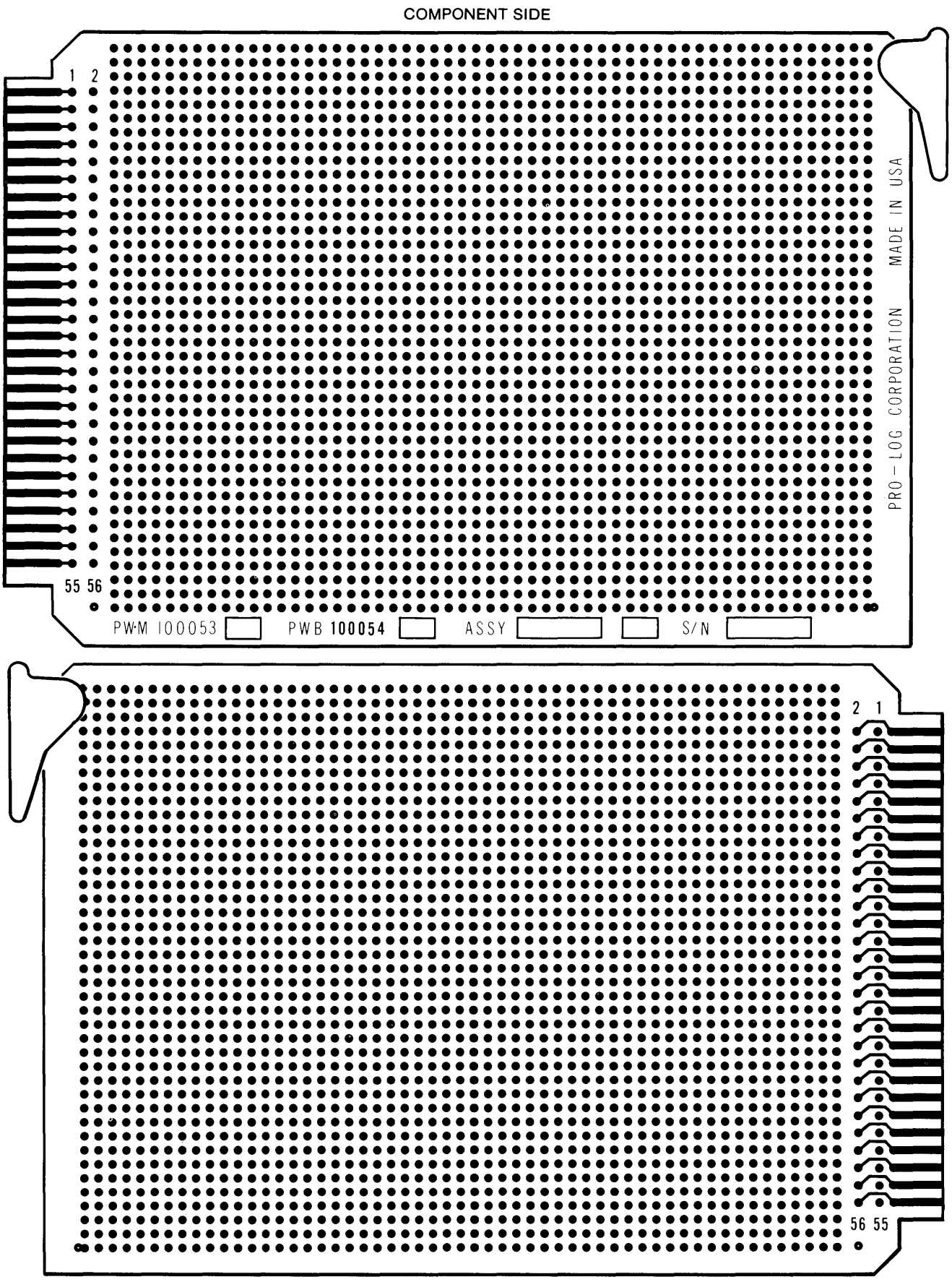
CONNECTOR REQUIREMENTS: 56 pin, 28 position, dual readout on 0.125 inch (0.32 CM) centers. See CW56, CW56-1 Edge Card Connector data sheet.

APPLICATION NOTES

For wire-wrapping; insert wrap sockets in desired position. Solder two or more pins to pads to hold socket. For connections to card-edge fingers, power bus or mounting of discrete components solder wire-wrap stakes in desired holes. Suitable wrap stakes can be obtained from Vector Electronics Company, Inc., part number T-44.

For direct soldering of components, insert component at desired location. Solder wires direct to protruding component leads.

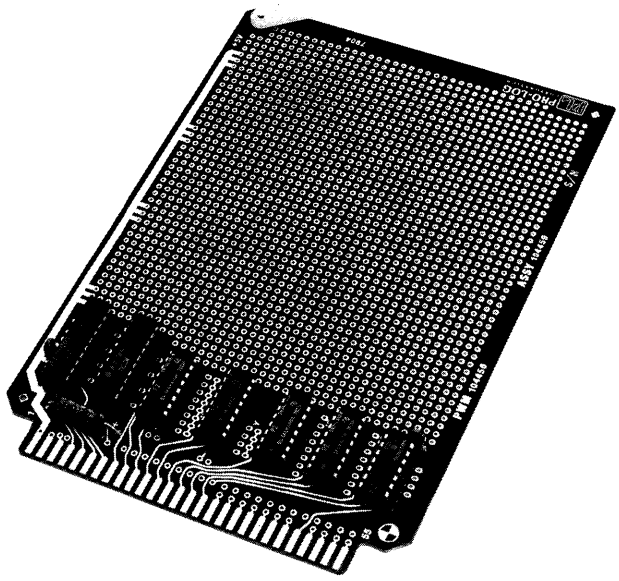
7903, GENERAL UTILITY CARD



7904 DECODED I/O UTILITY CARD

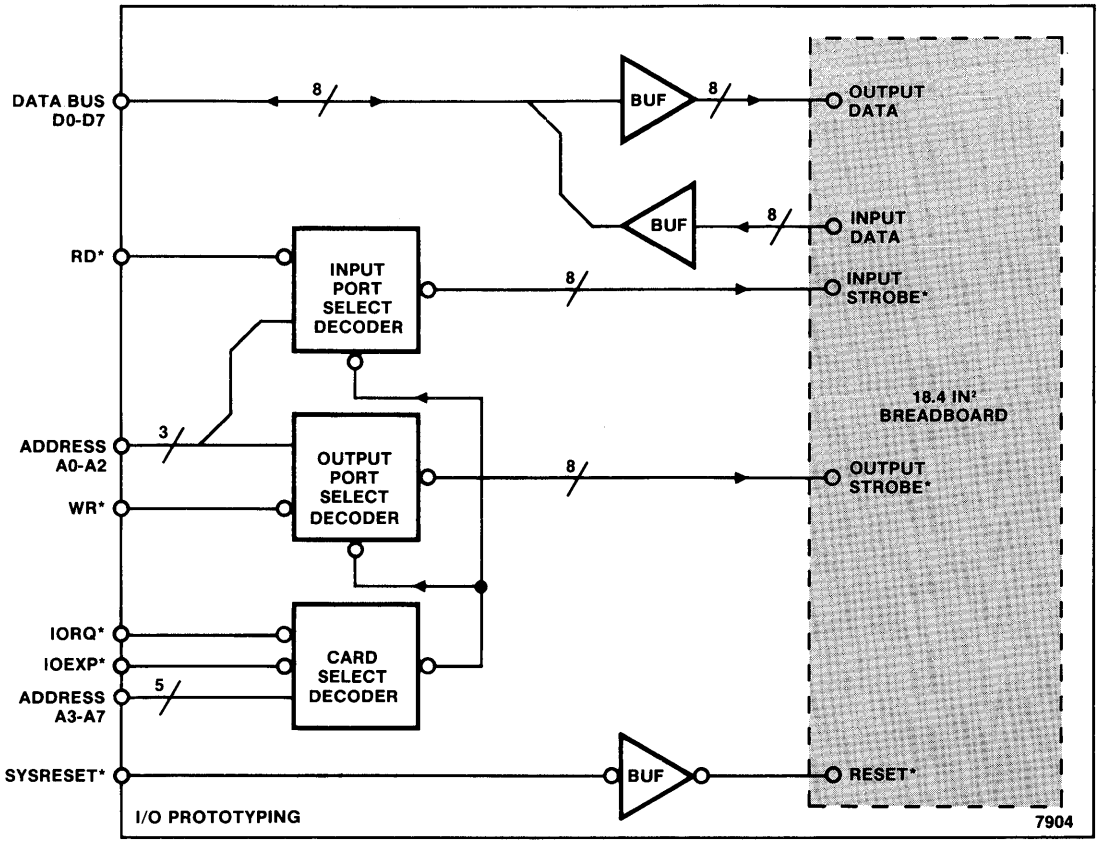
DECODED I/O UTILITY CARD

A printed circuit card for prototyping I/O circuitry. The 7904 provides complete STD BUS buffering and decoding for I/O cards, with input and output port strobe logic and access to memory page and CPU/memory control lines. A 4"x4.6" grid of holes on 0.1" centers is provided for adding dual-in-line or discrete packages. These plated through holes accommodate 0.025" square wirewrap posts.



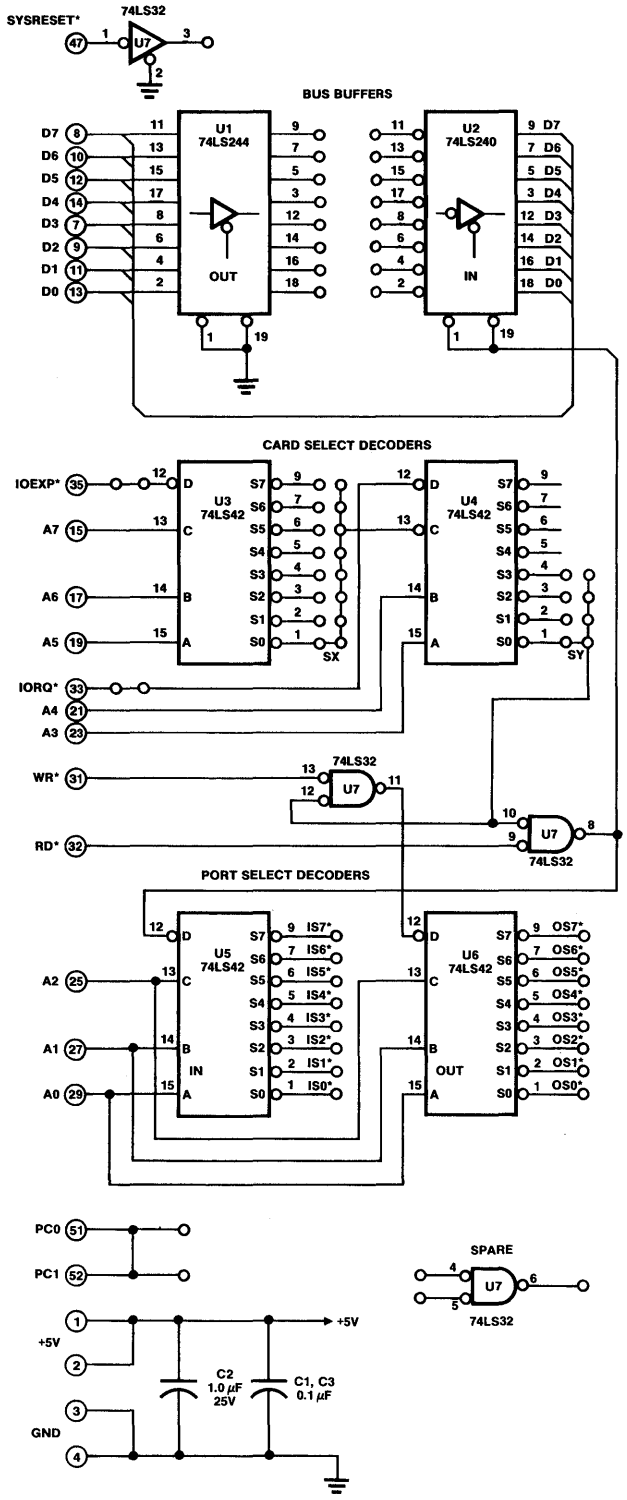
FEATURES

- **User selectable port address (256 port field)**
- **Data bus buffers with hysteresis**
- **8 sequentially addressed input port strobes**
- **8 sequentially addressed output port strobes**
- **Access to all STD BUS signals and power busses**
- **LSTTL logic**
- **All IC's socketed**
- **Plated through holes accommodate 0.025 in. sq. post**
- **18.4 sq. in. of breadboard area**



*INDICATES ACTIVE LOW LOGIC

7904, DECODED I/O UTILITY CARD



7904 Schematic

ELECTRICAL

- VCC = +5V ± 5%
- ICC = 161.8 mA maximum (91.9 mA typical) for logic provided
- Address, Data and Control Busses meet STD BUS general electrical specifications except: A0, A1 and A2 input loading 2 LSTTL loads.

MECHANICAL

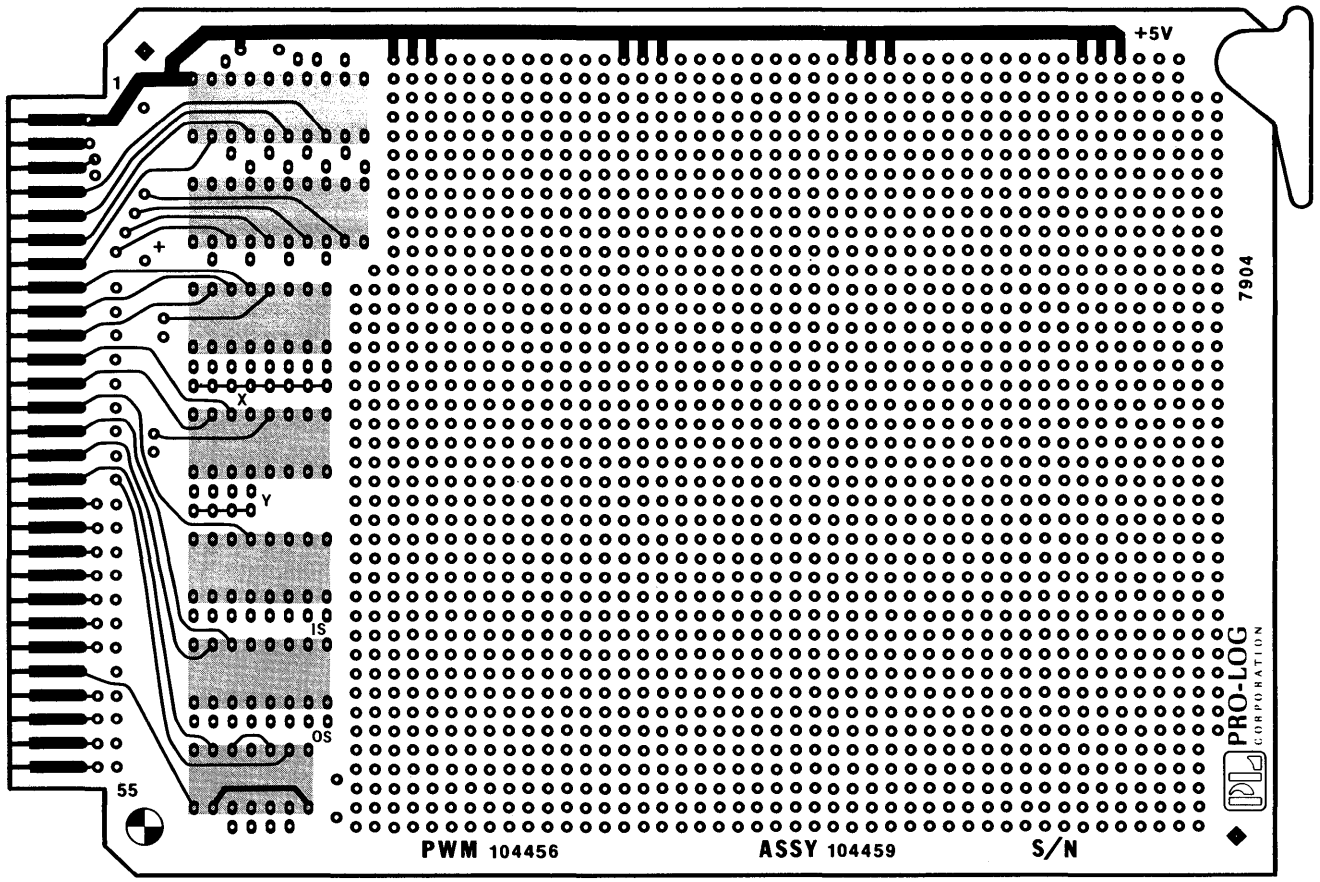
- Meets all STD BUS general mechanical specifications.

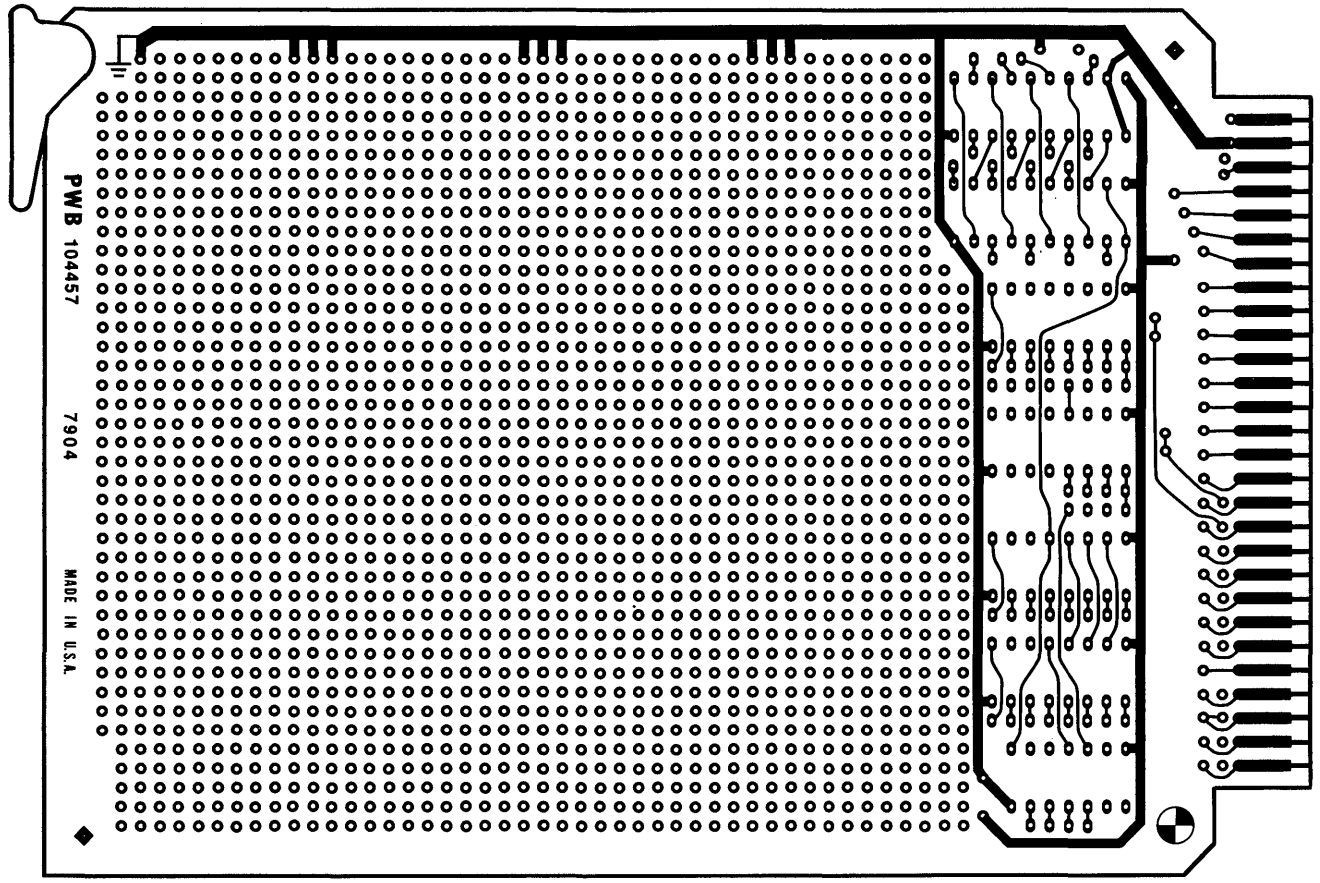
STD/7904 EDGE CONNECTOR PIN LIST							
PIN NUMBER				PIN NUMBER			
OUTPUT (DRIVE)						OUTPUT (DRIVE)	
INPUT (LOADING)						INPUT (LOADING)	
MNEMONIC							MNEMONIC
+5 VOLTS	VCC		2	1		VCC	+5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1	60	8	7	60	1	D3
D6	1	60	10	9	60	1	D2
D5	1	60	12	11	60	1	D1
D4	1	60	14	13	60	1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		2	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Designates Active Low Level Logic

Edge Connector Pin List

COMPONENT SIDE





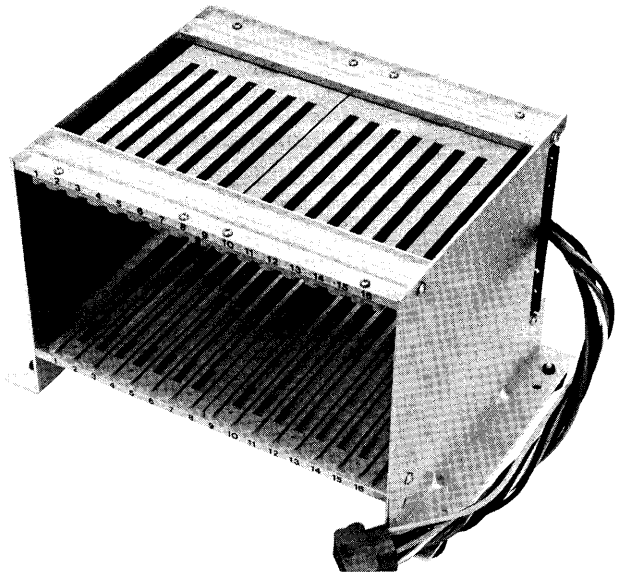
SHOWN ACTUAL SIZE

WIRE SIDE

CR8, CR16 MOTHERBOARD RACKS

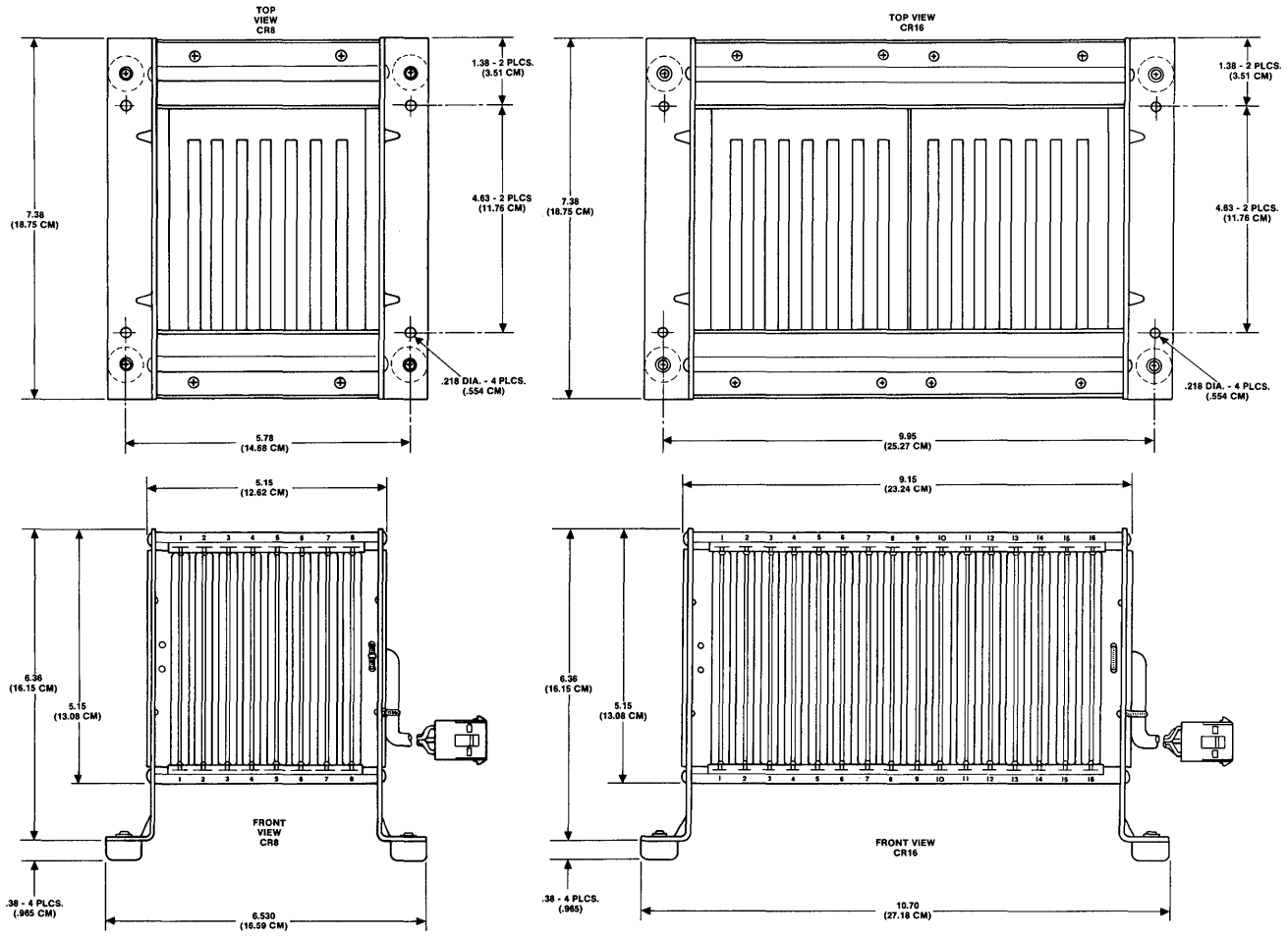
MOTHERBOARD RACKS

Includes motherboard containing a complete STD BUS on one side and, to minimize noise, ground plane on the opposite side. Includes card edge connectors. Power interconnect is provided by a 9-pin locking type connector. Mounting brackets permit mounting in a number of different enclosures.



FEATURES

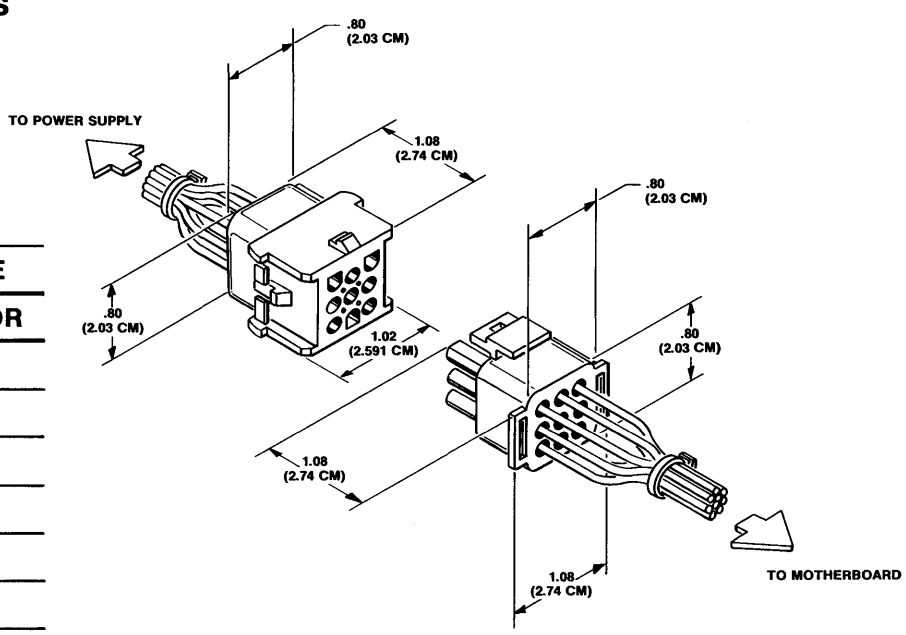
- **Accepts all Series 7000 STD cards**
- **CR16 accepts up to 16 cards**
- **CR8 accepts up to 8 cards**
- **Card spacing 0.5" centers**
- **Power cable with 9-pin keyed and locking connector with mating assembly interface cable routing space provided under rack**



CR8, CR16, MOTHERBOARD RACKS

POWER CABLE SPECIFICATIONS

POWER CABLE COLOR CODE	
FUNCTION	**CABLE COLOR**
VCC	Red
GND	Black
VBB	White
AUX +V	Orange
AUX GND	White/Black
AUX -V	Violet



POWER INTERCONNECT CABLE

POWER CABLE AND CONNECTOR SPECIFICATIONS			
FUNCTION	**RESISTANCE MAX**	**TEST CONDITIONS**	**RECOMMENDED LOADS**
Single Contact	3.0 milli Ω	18 AWG, 6.0A	15A Max, 0.1A min.
Single Wire	1.3 milli Ω	2', 18 AWG	
VCC	2.15 milli Ω	2', 18 AWG with connector (2 wires)	20A Max, 0.1A min.
GND	1.44 milli Ω	2', 18 AWG with connector (3 wires)	
VBB, AUX +V AUX -V, AUX GND	4.3 milli Ω	2', 18 AWG with connector (1 wire)	15A Max, 0.1A min.

SOURCE FOR CONNECTOR AMP INC		
DESCRIPTION	**AMP PART NO.**	**NO. PER ASSY**
Connector - Cap 9 Position	Cap #350782-1	1
Contact Pin	#350547-1	9
Connector Plug 9 Position	Plug #350720-1	1
Contact Socket	#350550-1	9

MOTHERBOARD SPECIFICATIONS: See Motherboard Data Sheet 7101 and 7102.

7000
STD BUS

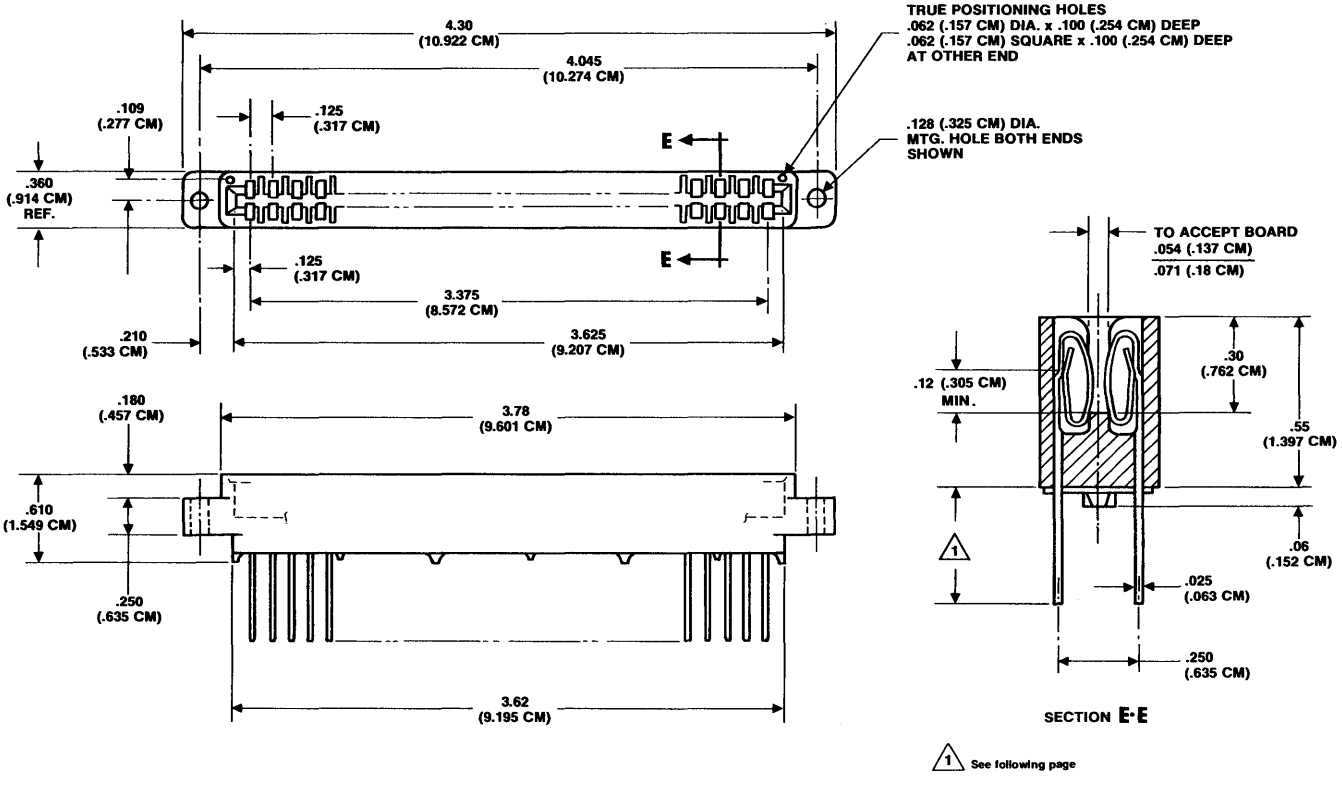
CW56, CW56-1
EDGE CARD CONNECTORS

EDGE CARD CONNECTOR

The CW56 and CW56-1 are card edge, 56-pin connectors. The CW56 is a 3-level wire wrap connector with 0.025 inch square wire wrap post on 0.125 inch centers. The CW56-1 is a solder tail version of the same connector.

FEATURES

- **3A per contact**
- **Accepts .062 thick PCB's**
- **Multiple sourced**

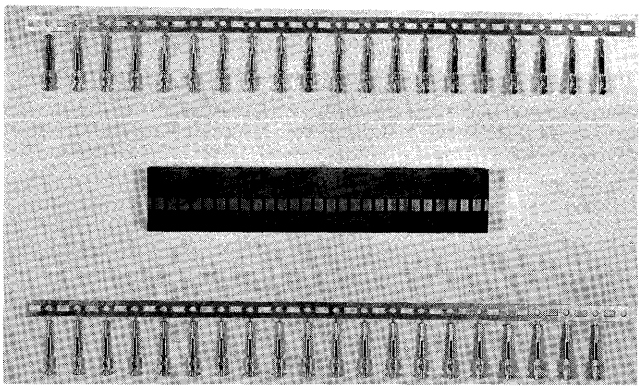


CW56, CW56-1 EDGE CARD CONNECTORS

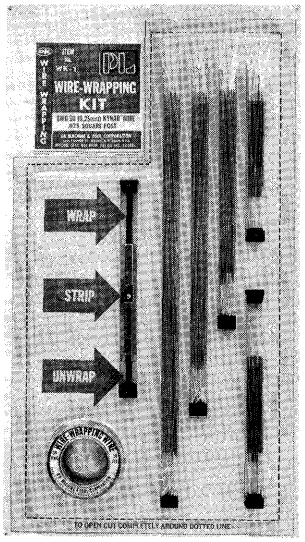
Requirements for 56 pin Edge Card Connector 0.125"x0.250 grid spacing:

- Current Rating: 3A per contact
- Max. Voltage Drop: 30mV at 3 amps per contact
- Operating Voltage: 600 VDC at sea level
- Operating Temperature: -65°C to + 125°C
- PC Board thickness: 0.054 through 0.071 inches
- Non polarized
- Dielectric: Green glass filled diallyl
- Phthalate per Mil-M-14, SDG-F or equivalent
- Contacts: Phasphor bronze, gold over nickel
- Insertion/Withdrawal Forces: 2 to 8 oz. per contact pair using 0.062 ± (0.00005) steel test blade.

The following table provides the Pro-Log model numbers and suppliers, with their part numbers, for connectors suitable for motherboard mounting and 3 level wire wrap applications



CT56 Transition Connector



WK-1 Wire Wrapping Kit

ACCESSORIES

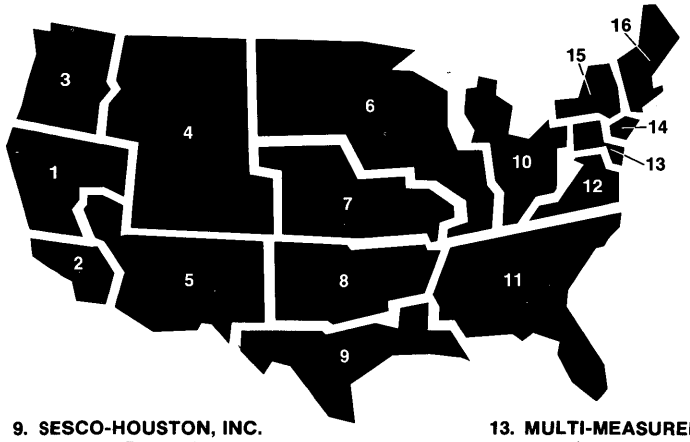
- CT56-Transition Connectors-female connector that slides on CW56 wire wrap post and notes to discrete wires via self crimp connections.
- The WK 1 wire wrapping kit provides wire and wire wrap, unwrap and strpping tool.

The Kit Includes:

Pre-cut and stripped 30 AWG Blue Kynar wire.
200 pieces 2 in. (5.08 cm) insulation length
150 pieces 4 in. (10.16 cm) insulation length
100 pieces 6 in. (15.24 cm) insulation length
50 pieces 8 in. (20.32 cm) insulation length
One 100 foot (30.5 meter) roll 30 AWG Blue Kynar wire
One 30 AWG wrap, unwrap and stripping tool

56 PIN CARD EDGE CONNECTORS ON 0.125 x .250 GRID		VENDOR PART NO.			
PRO-LOG MODEL NO.	DESCRIPTION ⚠1	WINCHESTER HWD SERIES	VIKING	SULLINS	SYLVANIA SERIES "AB"
CW56	3 Level Wire Wrap 0.635" (1.61 cm)	HW 28 D0-111	VH28/1CND5	ISA 28 DRMH	6AB03-28-IC100
CW56-1	Solder Tail, one level Wire Wrap 0.230"(0.58cm)	2HW 28 D0-111	VH28/1CNK5	ISA 28 DRSH	6AB03-28-IC500

Sales Representatives



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   Portland, OR (503) 292-3505

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   Utah (801) 364-0606

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