Xerox RAD Storage System

Models 3211/3214

Reference Manual

90 31 17A

RAD STORAGE SYSTEM ORDER CODES

Code (Hexadecimal)	Function
01	Write
02	Read 2 (and report any transmission error at count-done)
03	Seek
04	Sense
05	Check-Write
07	Reserve
0F	Condition Release Interrupt (dual access systems only)
12	Read 1 (and if an error is encountered, terminate the data transfer and report any transmission error at the end of the current sector)
13	Select Test Mode (for diagnostic purposes only)
17	Release
1F	Condition Release Interrupt (and set an interrupt call at device release – dual access systems only)
83	Seek (and cause a device interrupt on minimum access reached or Seek time-out error)

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XEROX

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Models 3211/3214

Reference Manual

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RELATED PUBLICATIONS

Title	Publication No.
Xerox 550 Computer/Reference Manual	90 30 77
Xerox 560 Computer/Reference Manual	90 30 76
Xerox Symbol/LN, OPS Reference Manual	90 17 90
Xerox Meta-Symbol/LN, OPS Reference Manual	90 09 52
Xerox Assembly Program (AP)/LN, OPS Reference Manual	90 30 00
Xerox Control Program-Five (CP-V)/BP Reference Manual	90 17 64
Xerox Control Program for Real-Time (CP-R)/RT, BP Reference Manual	90 30 85
Xerox Cartridge Disk System/Reference Manual (Models 3211/3242/3243)	90 31 16
Xerox Computer Systems/Interface Design Manual	90 09 73

Manual Content Codes: BP - batch processing, LN - language, OPS - operations, RP - remote processing, RT - real-time, SM - system management, TS - time-sharing, UT - utilities

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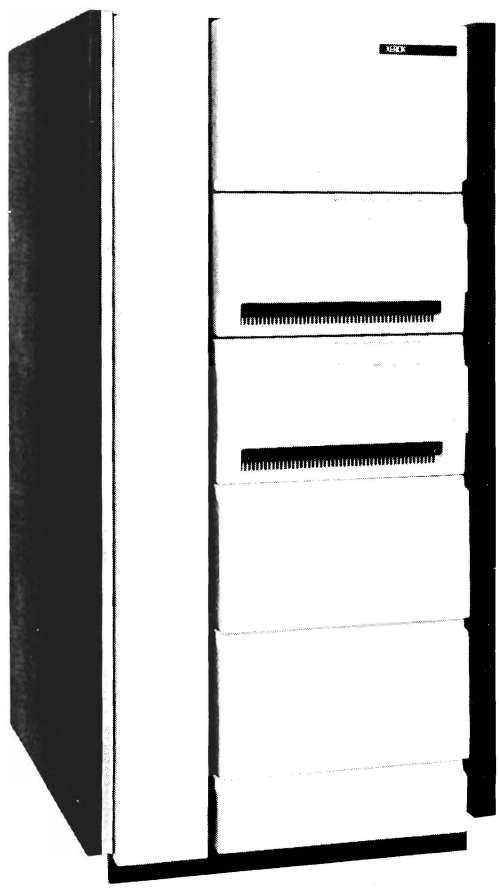
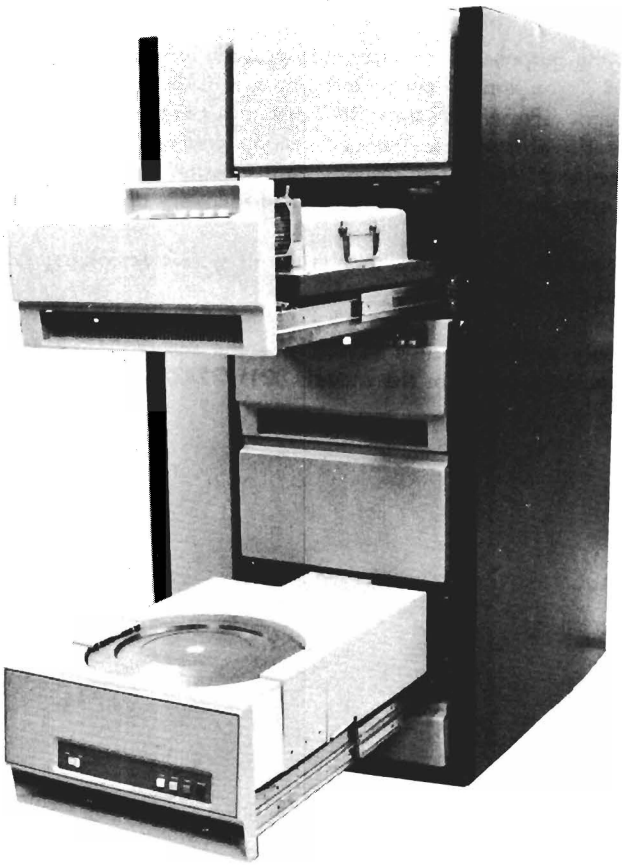




Xerox Rapid Access Data Storage System

PREFACE

It is the purpose of this manual to provide referential material for the programming and operation of the Models 3211/3214 Xerox Rapid Access Data Storage (RAD) System which is designed for inclusion in Xerox 550 and 560 computer systems. Presented are a RAD system summary; functional and physical descriptions of the equipment including I/O operational flow, device addressing, and system states; a description of the program interface including the I/O orders and RAD system response; a discussion of programming considerations including the interrupt environment, and the error detection environment and recovery procedures; and operating procedures.

The manual is intended for the use of system designers, system programmers, application programmers, and the computer operations staff.

Closely related to this manual are the respective reference manuals for the Xerox 550 and 560 computers and the reference manual for the Models 3211/3242/3243 cartridge disk system.

1. GENERAL DESCRIPTION

INTRODUCTION

The Xerox Model 3211/3214 Rapid Access Data Storage (RAD) System is a rotating disk memory that provides extremely fast and highly reliable random-access, secondary storage for Xerox 550/560 computer systems (32-bit words). It is a fixed-disk, rotating memory whose speed (average access time of 8.5 milliseconds) derives from the design of one fixed head assembly for each recording track (as contrasted with moving-head disk memories that have one moving head per surface and move the head to the desired track). The RAD's high reliability is concomitant with its limited exposure to atmospheric contaminants and handling.

RADs are desirable in a variety of application types. They may be used as random access memory in on-line control applications where access time is critical; as scratch pad or working storage for processing programs; as extensions of main memory for software and data storage (particularly when data are keyed, tabled, and indexed); as memory concentrators, i.e., as the hub of multilayered, hierarchical, data base systems; as associative memory wherein parallel bit paths match the data size of the computer, which is used as a data manager; and as swap storage and storage for real-time and back-up programs in a time-sharing system.

A RAD system comprises one Model 3211 rotating storage controller housed in the Xerox 550/560 computer mainframe, and one to eight Model 3214 RADs housed in one or two peripheral cabinets. On Xerox 550 computer systems, as the controller also serves as the controller for Model 3242/3243 cartridge disk drives, RADs and cartridge disk drives may be intermixed in any combination on a single controller to a maximum of eight devices. If the eighth device is a Model 3243 cartridge disk drive, access is limited to the removable disk (disk cartridge) only. As many as four RADs and/or cartridge disk drives may be mounted in each peripheral cabinet.

Each RAD is slide-mounted in a drawer in the peripheral cabinet for ease of servicing. The 3214 RAD is available in two versions: one that operates on 60 Hz power; and one that operates on 50 Hz power. Model 3214 RAD has a total sectored storage capacity of 2.88 million bytes.

Figures 1, 2, and 3 illustrate, respectively, a typical single-access system with devices connected in a "daisy-chain" fashion; a maximum single-access system using the Model 1048 controller expansion feature; and a maximum dual access system using the Model 1049 dual access feature and the Model 1048 controller expansion feature.

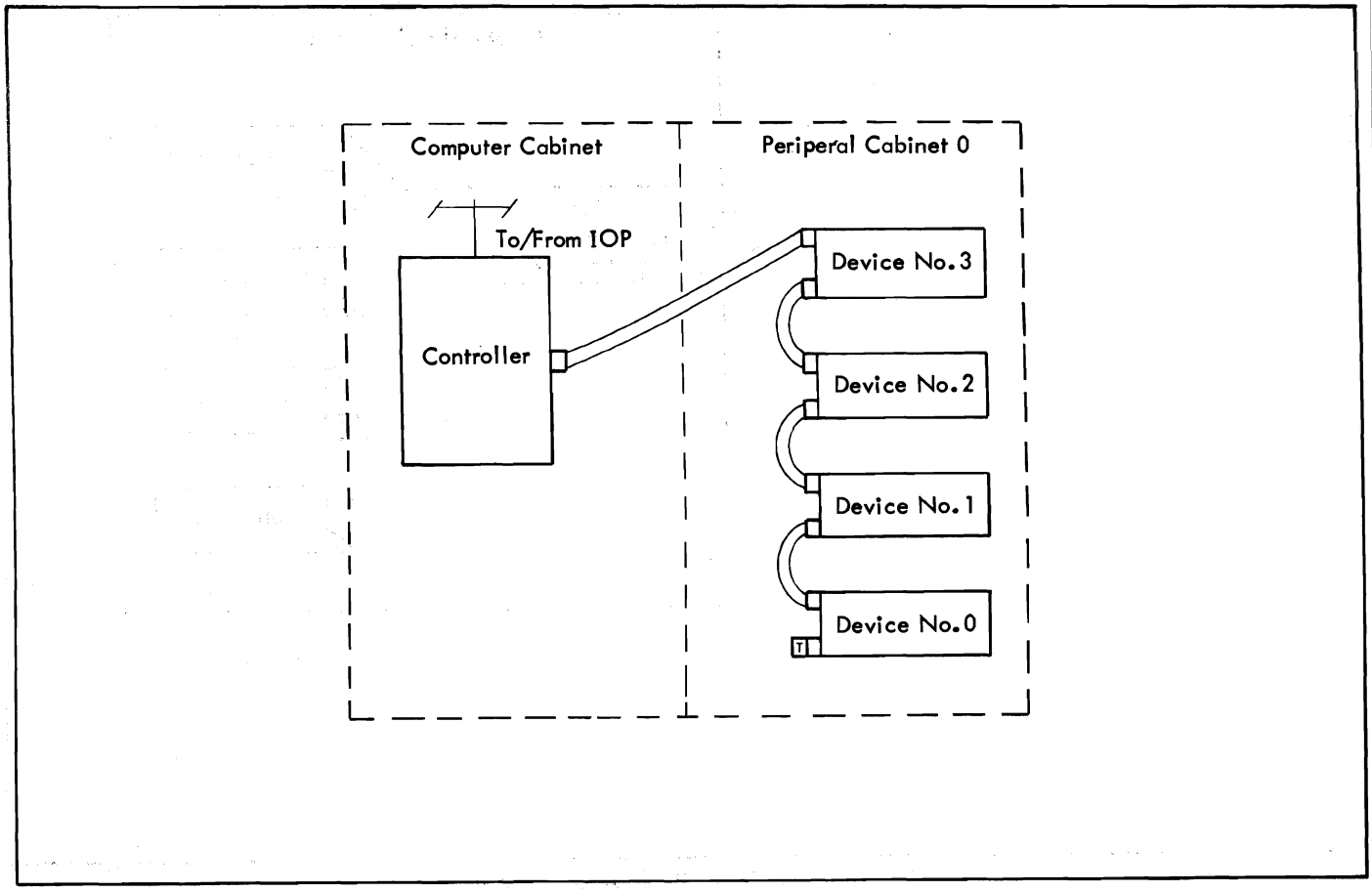


Figure 1. Typical Single Access System

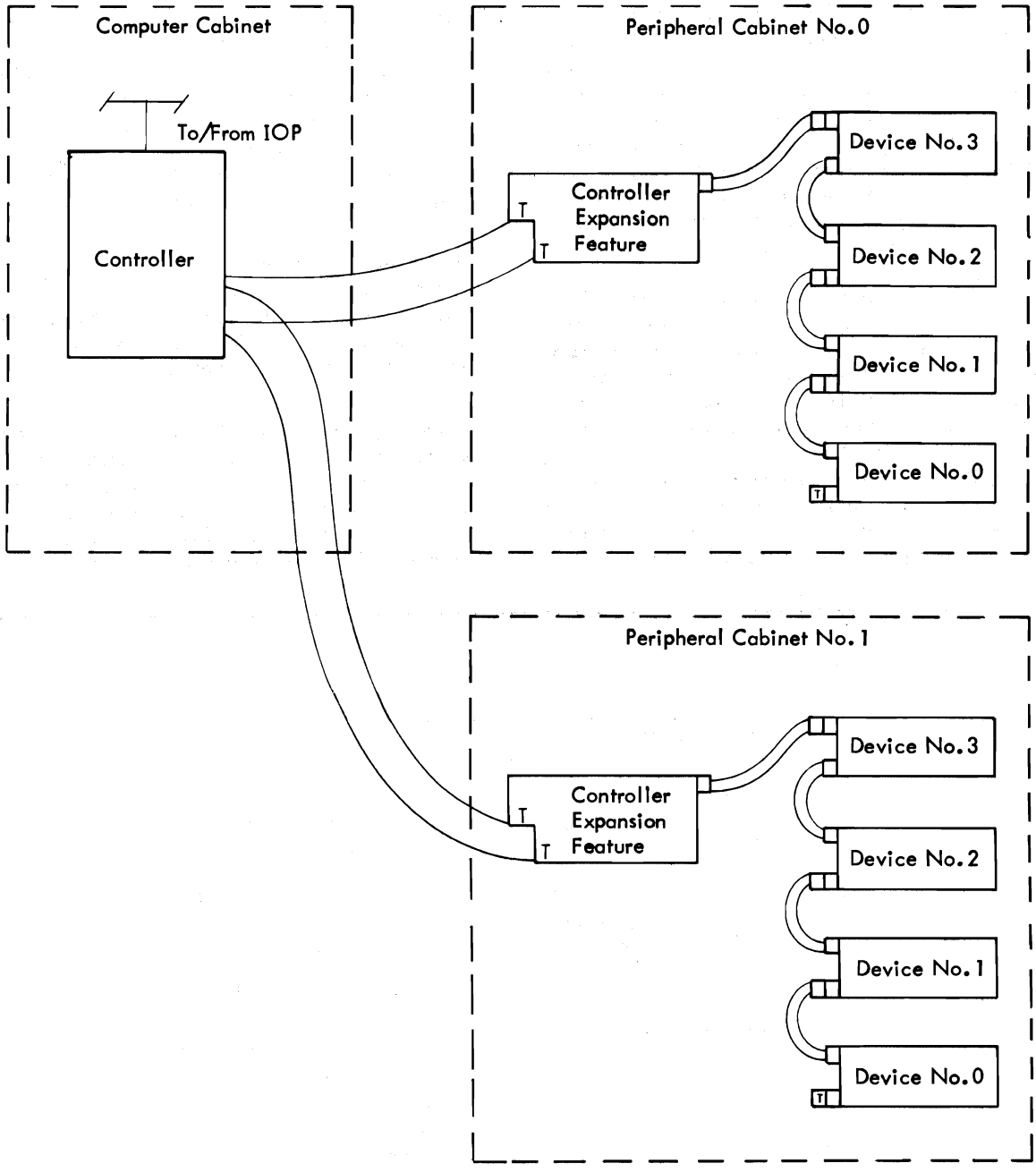


Figure 2. Maximum Single Access System

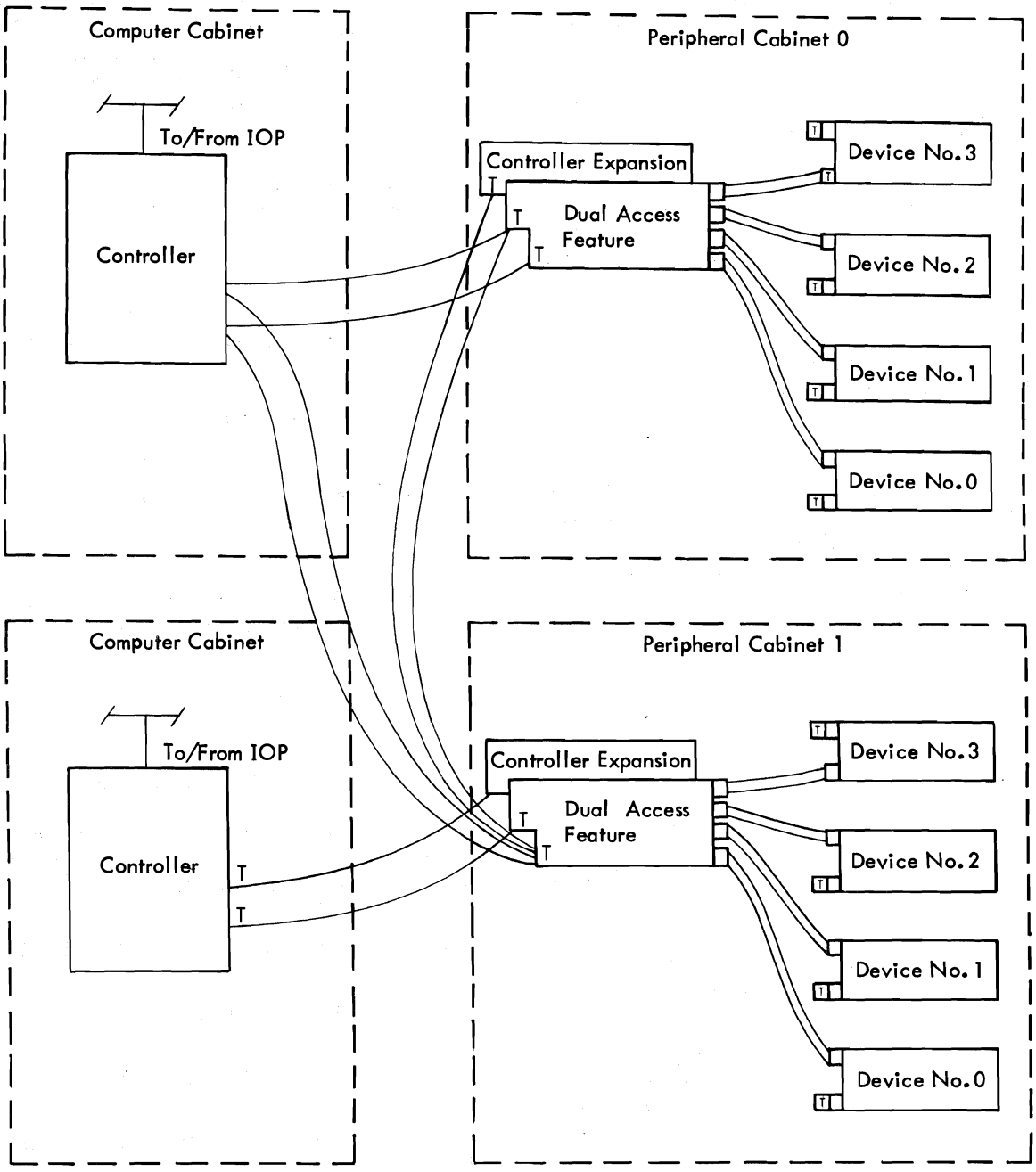


Figure 3. Maximum Dual Access System

When a cable length longer than 20 feet from controller to last device is desired, and/or more than four devices are to be connected to a single controller, one Model 1048 controller expansion feature must be installed in each peripheral cabinet. With the Model 1048 controller expansion feature installed, the total cable length may be as long as 100 feet.

The Model 1048 controller expansion feature is also required in each peripheral cabinet when dual access capability is configured for the RAD system. Additionally required is one Model 1049 dual access feature for each unit (RAD and cartridge disk) to which dual access is desired. Dual access capability means that any two Model 3211 controllers attached to the same or different Xerox 550/560 CPUs may access any one unit, or access two units simultaneously. A maximum of eight units are accessible in a dual access system, with this restriction applicable to the eighth unit: if the eighth unit is a Model 3243 cartridge disk drive, access is limited to the removable disk (disk cartridge) only.

Note: Xerox 550/560 computer systems with more than 160K words of main memory require a Model 1048 in the peripheral cabinet.

To use this manual effectively, the reader must be familiar with the Xerox 550 or 560 Computer Reference Manual (whichever applies), particularly the chapters on input/output instructions and operations; see "Related Publications" at the front of this manual.

FEATURES

Several significant equipment features affect system performance and the reliability of recorded data:

- Fast access is achieved by increased rotational speed and the lack of head movement.
- Greater reliability results from simplified mechanisms and limited exposure to atmospheric contaminants.
- The high throughput rate (approximately 750,000 bytes per second) results from a rotational speed of approximately 3540 revolutions per minute and a serial data transfer rate of approximately 6,000,000 bits per second.
- High bit density contributes to the small size of the RAD.
- RAD contents are permanently protected against power failure.
- A check character (two bytes) is recorded in each written sector for error detection and analysis.

Other features that have programming implications:

- The Model 3214 RAD contains 128 accessible tracks on either disk surface (plus spare tracks) and each track is electronically sectored into 11 sectors.
- Data are recorded on the RAD surfaces in fixed-length sectors of 1024 bytes. A RAD header is automatically recorded preceding the data portion of each written sector with every execution of a Write order. The controller zero-fills the remainder of the data sector for a record smaller than 1024 bytes.
- The controller automatically augments sector and track addresses; hence a record may comprise any integral number of contiguous sectors within one RAD.
- A switch-selectable write-protect feature ensures file protection in groups of 64-track increments.
- The simplified system design facilitates I/O programming.
- Average latency is 8.5 milliseconds, 17 milliseconds maximum.
- The RAD I/O program can reduce access time to near-zero (see Data Access in Chapter 2).

SYSTEM COMPONENTS

Table 1 summarizes the system components described in this section, and Table 2 presents the operating, physical, and environmental characteristics.

The minimum configuration RAD system (2,883,584 bytes) is

One Model 3211 controller.

One Model 3214 RAD (256 tracks).

The maximum configuration RAD system (23,068,772 bytes) is

Two Model 3211 controllers.

Eight Model 3214 RADs (256 tracks each).

Two Model 1048 controller expansion features.

Eight Model 1049 dual access features.

Table 1. RAD System Components

Model	Component	Prerequisite Component
3211	Rotating storage controller that serves as many as eight Model 3214 RADs and Model 3242/3243 cartridge disk drives intermixed in any combination.	IOP
3214	RAD providing a storage capacity of 2.88 million bytes.	3211
1048	Controller expansion feature installed in each peripheral cabinet to allow a cable length longer than 20 feet and up to 100 feet from controller to last device, and/or to allow five or more devices to be served by the controller, and/or to accommodate 550/560 systems with more than 160K words of main memory, and/or to accommodate the dual access capability.	3211, and one or more devices – 3214, 3242, 3243
1049	Dual access feature to allow two controllers to access two devices simultaneously, or to allow two controllers to have access to the same device at different times. One required for each device for which dual access is required.	3211, 1048

Table 2. Characteristics

Operating Characteristics	
On-line capacity (sectored)	2,883,584 bytes/disk (256 tracks accessible)
Recording surfaces	2
Recording format	128 tracks accessible/surface 1 head/track 1024 data bytes/sector 11 sectors/track
Nominal access time (latency)	
Average	8.47 milliseconds
Maximum	17 milliseconds
(can be reduced to near-zero under special program control)	
Rotational speed	3540 rpm + 1.5%, -4.5%
Nominal transfer rate	755,200 bytes/second, once data transfer begins
Physical Characteristics	
Peripheral cabinet	
Height	63.4 inches
Width	31 inches
Depth	34.7 inches

Table 2. Characteristics (cont.)

Physical Characteristics (cont.)	
RAD unit	
Height	10.5 inches
Width	19 inches
Depth	30 inches
Weight	95 pounds
Environmental Characteristics	
Power requirements	
Model 3211	Provided by computer
Model 3214 (60 Hz)	120 VAC ± 10%, 60 Hz ± 1%, single-phase, 6 amps steady state
Model 3214 (50 Hz)	220 VAC ± 10%, 50 Hz ± 1%, single-phase, 3 amps steady state
Operating temperature	50° to 100°F
Operating humidity (relative)	20% to 80%
Thermal dissipation (Model 3214)	3400 BTU/hour

2. FUNCTIONAL DESCRIPTION

This chapter functionally describes the RAD system. It begins with the principal system components and the flow of information between those components; continues with the organization of tracks and sectors on the RAD disk surfaces and the organization of data within a sector; and concludes with the RAD system states and a list of recommendations.

EQUIPMENT

In addition to presenting the functional characteristics of the controller and the RADs, this section describes some of the physical features of the equipment. The descriptions introduce the equipment terminology used throughout this manual and are intended as background information only. System designers, programmers, and operators who have previous experience with disk equipment may prefer to skip this section.

MODEL 3211 CONTROLLER

Physically, the controller is resident in the computer mainframe and shares computer power. The controller consists of electronic circuitry that enables it to interact with the IOP, to direct each of four RADs via a single serial bus, and to direct more than four RADs via the controller expansion feature.

Functionally, the controller accepts and interprets I/O instructions; requests and interprets device orders such as Seek, Read, and Write; and directs the RADs in their execution of these orders. During an I/O operation the controller transfers data between the IOP and one of the RADs. Moreover, the controller sets and returns the status response after each I/O instruction and device order has been executed; automatically records the sector header with each Write operation; and performs error checks as data are being transferred.

STATUS RESPONSE

Following the acceptance (and possibly the execution) of an I/O instruction, the controller reports the device condition ready, busy, not operational, or not available. The controller also reports whether the device address was recognized or not, and whether the I/O instruction was accepted or not. Similarly, after the execution of a device order, the controller reports the type of termination, e.g., channel end, unusual end, or transmission error.

RECORDING SECTOR HEADER

With each Write operation, the controller automatically records a header comprising the current RAD address (track and sector numbers) at the beginning of each written sector.

ERROR CHECKING

To detect errors in data transmission, the controller computes a two-byte, cyclic error detection check character for each sector. During a Write operation, the controller computes and writes a check character in each accessed sector. Subsequently, during a Read or Check-Write operation on the same sector, the controller recomputes the check character and compares it with the check character recorded on the disk. Any discrepancy results in the termination of the operation with transmission error indicated for error in data records, and with unusual end indicated for error in headers.

The controller also performs this check: During each Read operation, the controller verifies the header of each read sector on the RAD by comparing it with the current RAD address in its address registers. The controller indicates address verification error with unusual end for the Read operation.

MODEL 3214 RAD

A RAD unit consists of a drive mechanism for a single, magnetic-coated, fixed disk. One hundred twenty-eight tracks on either disk surface are accessible. Spare tracks and heads are available, should a track be flawed or a head defective.

Each RAD is slide-mounted in a pull-out drawer in the peripheral cabinet for ease of servicing. A RAD disk surface is written on or read from using one fixed read/write head per track.

OPERATOR CONTROL PANEL

The operator control panel, which appears at the front of the RAD, has a READY indicator and four alternate-action PROTECT switch/indicators. These are described briefly below and detailed in Chapter 4.

- The READY indicator, when lighted, indicates that all power is up to specification, the RAD has completed its start-up cycle and is rotating up to speed, and the RAD is ready to accept orders such as Seek, Read, and Write from the RAD I/O program.

- The alternate-action PROTECT switches/indicators, when lighted, indicate that the associated 64-track group is write-protected. To allow writing on a protected 64-track group, the operator depresses the appropriate PROTECT switch/indicator and the light is extinguished.

START-UP CYCLE

The function of the start-up cycle is to get the RAD rotating up to operational speed (3540 rpm +1.5%, -4.5%). The start-up cycle begins when power is supplied to the RAD. (Note that once installed and powered up, a RAD stays "up" and is not turned on and off for each use.) The READY indicator on the RAD operator control panel is illuminated when the start-up cycle is completed.

WRITE-PROTECT FEATURE

The write-protect feature guards against inadvertent writing on the RAD. When a PROTECT switch/indicator on the operator control panel is illuminated, the associated group of 64 tracks cannot be written on – they are write-protected. To allow writing on a protected group of tracks, the operator must depress the appropriate PROTECT switch/indicator and extinguish the light – the associated tracks are no longer protected. To set write-protect back on, the operator depresses the extinguished PROTECT switch/indicator; the indicator is then illuminated and the associated tracks are again protected.

I/O OPERATIONAL FLOW

Figure 4 illustrates the flow of information among system components in a Xerox 550/560 configuration with a RAD system. The purpose of the diagram is to define the source and destination of critical items of information.

Before an I/O operation can begin, specific registers in the Basic Processor must be set and tables in main memory must be made available to the computer system. During and after an I/O operation, the controller transmits the status response to specific registers whose contents may then be analyzed to determine the result of the operation. Significant registers and tables appear in the diagram.

Chapter 3 describes the device orders interpreted by the controller and the RADs. It also describes condition code bits 1 and 2 and the device status byte for each I/O instruction, and describes the flags in the operational status byte. The Xerox 550/560 Computer Reference Manual describes in detail the I/O instructions, the types of required tables, and the required register contents.

DEVICE ADDRESSING

The controller is capable of addressing as many as eight units – unit numbers 0 through 3 in cabinets 0 and 1. The concatenated values of the cabinet number and the unit number form the device number, which can range in value from 0 through 7.

Two device addresses – one even and one odd – are available for assignment to each device except device 7, the eighth device. Thus, device addresses 0 and 1 are available for assignment to device 0, addresses 2 and 3 to device 1, and so forth. Device 7 can have only address X'E', because address X'F' is reserved for addressing the controller.

The device address is formed of the concatenation of the values of the cabinet number (bit 28), unit number (bits 29 and 30), and device select (bit 31) in the I/O instruction (SIO, TIO, TDV, or HIO). Note that for RADs, device select is always zero. Consequently, RADs always have even device addresses:

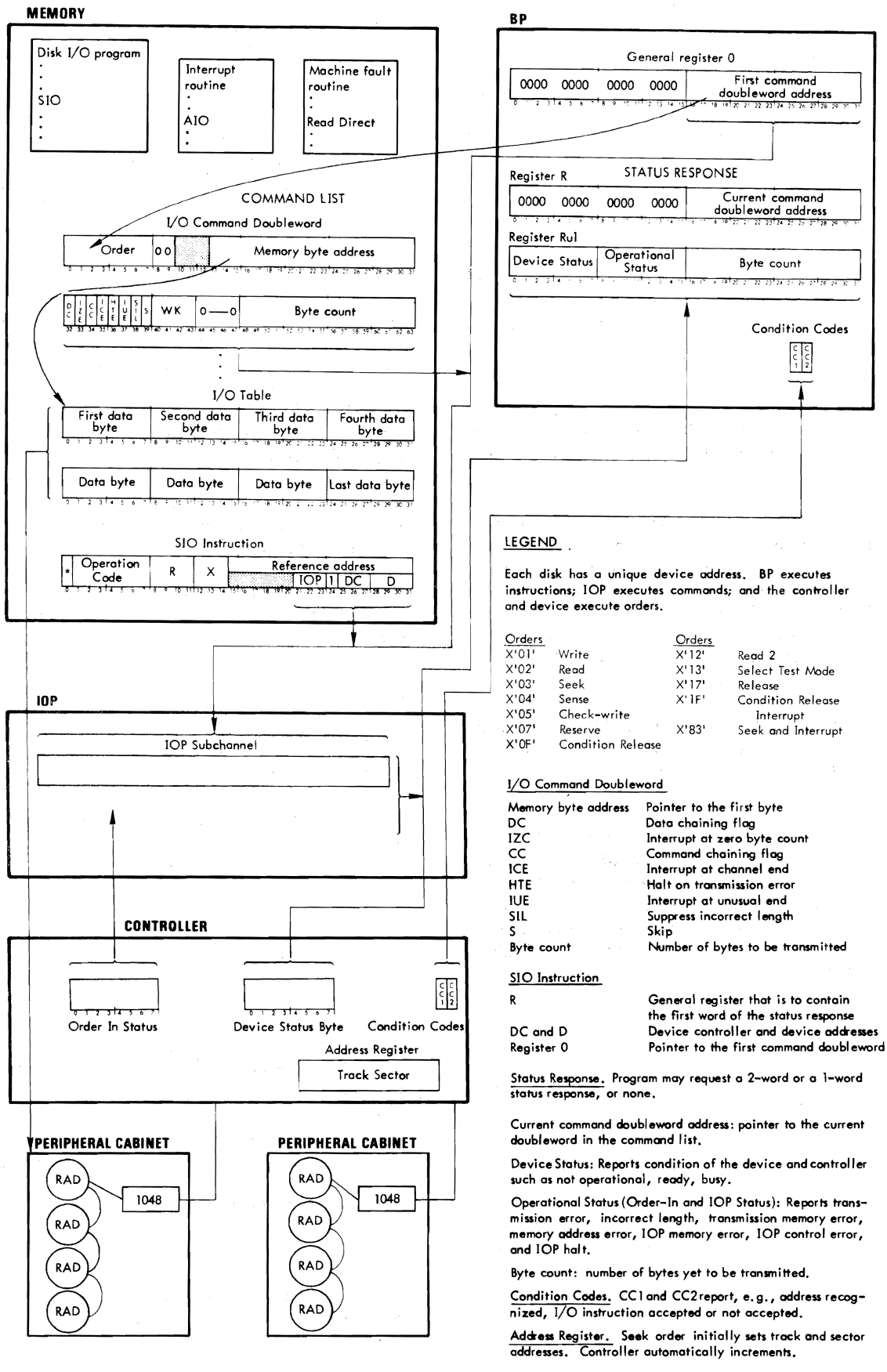
RAD Device Number	Binary Values			RAD Device Address
	Cabinet Number	Unit Number	Device Select	
0	0	00	0	X'0'
1	0	01	0	X'2'
2	0	10	0	X'4'
3	0	11	0	X'6'
4	1	00	0	X'8'
5	1	01	0	X'A'
6	1	10	0	X'C'
7	1	11	0	X'E'

The applicability of an even and an odd address pertains only to Model 3243 cartridge disk drives configured in the same system and serviced by the same controller as the RADs – Model 3243 cartridge disk drives house two disks whose addresses are differentiated by the value of the device select field.

DISK ORGANIZATION

A disk surface is organized into tracks (concentric circles) and sectors (electronic segmentation of each track into fixed-size areas for the storage of data). Each RAD has 256 tracks accessible. Normally there are 128 accessible tracks and 11 sectors on either surface. (In the case of the required use of spare tracks and read/write heads to replace flawed tracks or defective heads, a disk may actually have more tracks accessible on one surface than the other; this eventuality is of no consequence, however, to the RAD I/O program.)

The sector data areas are identical on either surface, and sector addresses range from 0 through 10 on either surface. Sector sizes are arranged to provide a long sector at every other sector location on the disk to allow time for command chaining (see also Command Chaining and Data Chaining in Chapter 3). Because the number of sectors per rotation is odd (11), the location of long sectors differs from track to track. Track 0 and all even-numbered tracks have short sectors 0, 2, 4, 6, and 8, and long sectors 1, 3, 5, 7, and 9.



LEGEND

Each disk has a unique device address. BP executes instructions; IOP executes commands; and the controller and device execute orders.

Orders		Orders	
X'01'	Write	X'12'	Read 2
X'02'	Read	X'13'	Select Test Mode
X'03'	Seek	X'17'	Release
X'04'	Sense	X'1F'	Condition Release
X'05'	Check-write		Interrupt
X'07'	Reserve	X'83'	Seek and Interrupt
X'0F'	Condition Release		

I/O Command Doubleword

Memory byte address	Pointer to the first byte
DC	Data chaining flag
IZC	Interrupt at zero byte count
CC	Command chaining flag
ICE	Interrupt at channel end
HTE	Halt on transmission error
IUE	Interrupt at unusual end
SIL	Suppress incorrect length
S	Skip
Byte count	Number of bytes to be transmitted

SIO Instruction

R	General register that is to contain the first word of the status response
DC and D	Device controller and device addresses
Register 0	Pointer to the first command doubleword

Status Response. Program may request a 2-word or a 1-word status response, or none.

Current command doubleword address: pointer to the current doubleword in the command list.

Device Status: Reports condition of the device and controller such as not operational, ready, busy.

Operational Status (Order-In and IOP Status): Reports transmission error, incorrect length, transmission memory error, memory address error, IOP memory error, IOP control error, and IOP halt.

Byte count: number of bytes yet to be transmitted.

Condition Codes. CC1 and CC2 report, e.g., address recognized, I/O instruction accepted or not accepted.

Address Register. Seek order initially sets track and sector addresses. Controller automatically increments.

Figure 4. I/O Operational Flow

Track 1 and all odd-numbered tracks have short sectors 1, 3, 5, 7, and 9, and long sectors 0, 2, 4, 6, and 8. Sector 10 (the last sector) on all tracks is always a long sector. These are the sector gap sizes:

Type	Gap Size
Short sector	50 bytes
Long sector	154 bytes
Last sector (10)	196 bytes

DATA ACCESS

Data are stored in groups of 1024 bytes (one sector) and each data group has a unique address comprising controller address, device address, and track and sector within the device.

To select a RAD for an operation, the I/O instruction must contain the controller and device addresses. (The I/O instruction also includes the IOP address.) Because the 3211 is a multidevice controller, the controller address lies in the range X'8' through X'F' and the device addresses in the range X'0' through X'E'. Device address X'F' is for the controller and may be used for any I/O instruction (SIO, HIO, TIO, or TDV) intended for the controller only.

Average access time is 8.47 milliseconds. Optimum access can be achieved when several consecutive sectors are read or written after a Seek order is issued, and the RAD I/O program can overlap Seek orders to separate RADs.

Rotational delay can also be reduced to near-zero; the RAD I/O program senses the rotational position of a given track and then begins the Read or Write operation at the first available sector that would normally be included in the record to be acted on. Once reading or writing begins, data are transferred at an instantaneous rate of 755,200 bytes per second, nominal.

TRACK AND SECTOR AUGMENTATION

Reading or writing always occurs at the current RAD address; this may be the last sector-track read or written, augmented by one, or the particular RAD address just obtained with a Seek order.

Within the controller is an address register for maintaining the current track and sector addresses; this register is initially loaded with a Seek order. The particular read/write head is then selected, the sector located, and the Read or Write order is executed. After reading or writing the sector, the controller automatically augments the sector address to the next sector in sequence (same track). When it completes the last sector of a track, the controller resets the sector address to zero and augments the track address to the next track in sequence. In that manner the controller automatically augments the address register until the latter is changed by another Seek order, or until the end of the last sector of the last track is reached.

Note that the 3211 controller allows any integral number of contiguous sectors within the same RAD to be treated as a single record of information. Thus, because of automatic address augmentation, a data record may extend from sector to contiguous sector, and from track to track within one RAD.

EXAMPLE OF AUTOMATIC ADDRESS AUGMENTATION

Assume that a Seek order specifies track 0 and sector 0. The controller will load the track and sector addresses in its address register and will select the appropriate read/write head and locate sector 0. Next assume that a Write order specifies a byte count of 2000. As soon as the controller begins writing in track 0, sector 0, it augments the contents of the address register to sector 1 (still track 0). Because a sector contains a maximum of 1024 bytes, the controller writes the remaining bytes in track 0, sector 1 (and zero-fills this sector), and augments the contents of the address register as soon as it begins writing in sector 1. At the end of this operation, the address register contains track 0, sector 2, the current RAD address. Unless an intervening Seek order is received, subsequent reading or writing will commence at this address.

ERROR CONDITIONS

An error condition exists should the RAD I/O program attempt to seek a track address ≥ 256; should the RAD I/O program issue a Seek order specifying a nonexistent sector address; or should the transfer of more data be attempted after the last sector of track 255 is reached.

SYSTEM STATES

"System state" refers to the combination of RAD system mode and condition of the addressed controller and device. The two modes are automatic, and not operational. Controller conditions are ready, busy, and not operational. The controller is considered busy if one of its devices is busy, and ready if all of its devices are ready. Device conditions are ready, busy, not available, and not operational. The not available condition is said to apply to a device when the device has been reserved for use by another controller.

Table 3 lists the controller and device conditions and their meanings. These conditions are directly related to the section "Status Response" in Chapter 4.

Table 4 illustrates the circumstances under which the RAD system transits from one state to the next.

Table 3. Conditions

Condition	Interpretation
Not operational	The power is turned off, or the controller or device is not operational.
Ready	The controller can accept an SIO instruction if the addressed device is available and if the system is free of impending interrupts. To become ready, the device must be operational and the execution of an order must not be in progress or pending.
Busy	The controller has accepted an SIO instruction. It will not accept a new order until the current order is completed and no interrupt is pending.
Not available	The device is reserved by another controller and cannot accept an I/O order. Therefore the controller cannot accept the SIO instruction.

Table 4. State Transitions

Current State \ Next State	Not Operational	Ready Automatic	Busy Automatic
Not operational		Power is turned on.	Not possible.
Ready automatic	Power is turned off.		SIO instruction has been accepted.
Busy automatic	Power is turned off.	HIO instruction received, I/O reset signal received, or operation associated with the last order is completed.	

DEVICE OPERATIONAL

A device is operational when the READY indicator on the device control panel is lighted. The light indicates that

1. The power is on.
2. The start-up cycle is completed and the RAD disk is revolving at 3540 rpm.

The exact status can be determined by examining the status responce for the SIO, HIO, or TIO instruction. Other I/O instructions, TDV and AIO, provide additional status indications.

DATA TRANSFERS

A data transfer may be initiated with an SIO instruction when the following criteria are satisfied:

1. The I/O address is recognized.
2. The controller is in the ready condition.
3. No interrupt is pending on the channel.
4. The addressed device is available.

If those criteria are satisfied, the controller enters the busy condition and transfers data to or from the RAD as

specified by the order (e.g., Read or Write), until the required number of bytes have been transferred. When the operation terminates, the controller returns to the ready condition. The operation can also be halted by

1. An IOP halt, generated by the IOP on some errors.
2. Execution of an HIO instruction.
3. An I/O RESET action taken by the operator at the 550 or 560 system control console (SCC).
4. Exceeding the end of the last sector on the last track.

In those cases, all data may not have been transferred when the halt takes place. Following an IOP halt, execution of an HIO instruction, or an I/O RESET action, the controller is in the ready condition.

RECOMMENDATIONS

The following recommendations and suggested use apply to the RAD system:

1. The system is recommended for
   a. Operating system, language processor, and public library residence.
   b. Permanent storage of user programs.
   c. Permanent storage of data.
   d. Temporary storage of data.
   e. Booting the system into main memory.
   f. Swap storage in a time-sharing system.
2. In a single-access RAD system, an operation cannot be initiated on a device when the controller is busy; therefore, operations cannot take place simultaneously on two devices. While one device is busy, however, a TIO or TDV instruction may be issued to another device.
3. In a dual-access system, operations can take place simultaneously on two devices when each device has been accessed through a separate controller. Moreover, either controller can access any device (configured for dual access) that is neither busy, nor reserved by the other controller.

3. PROGRAM INTERFACE

This chapter contains information required for writing RAD I/O programs for the RAD system. It describes the device orders, summaries of the key events that may occur during I/O operations, and tables that define the status response for the I/O instructions. The section entitled "Additional Programming Considerations" contains information relating to the protection of recorded information; to command chaining and data chaining; to surface operations; and to surface flawing. The section also discusses Seek operations; the program I/O interrupt environment; the RAD system interrupt environment; dual access considerations; the RAD system error detection environment; Seek, Read, and Write errors; and I/O fault detection and recovery actions.

DEVICE ORDERS

When the controller successfully completes an SIO instruction or command chain, it makes a one-byte, order out service call to the IOP to get the order for the next operation. Table 5 lists the order codes for the I/O orders described in the following sections; all other order codes are treated as invalid. Moreover, all orders to device address X'F' (except a Condition Release Interrupt order or a Select Test Mode order) are invalid unless the controller is first placed in device simulation test mode by a Select Test Mode order.

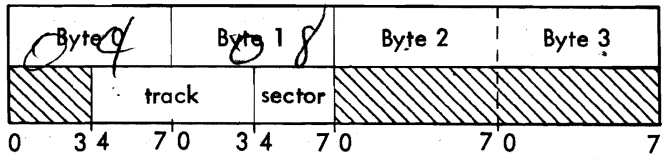
Table 5. Orders

Order	Binary Representation Bit Position 0 1 2 3 4 5 6 7	Hexadecimal Code
Seek	M 0 0 0 0 0 1 1	X'83', X'03'
Write	0 0 0 0 0 0 0 1	X'01'
Check-Write	0 0 0 0 0 1 0 1	X'05'
Read 1	0 0 0 1 0 0 1 0	X'12'
Read 2	0 0 0 0 0 0 1 0	X'02'
Reserve	0 0 0 0 0 1 1 1	X'07'
Release	0 0 0 1 0 1 1 1	X'17'
Condition Release	0 0 0 M 1 1 1 1	X'1F', X'0F'
Select Test Mode	0 0 0 1 0 0 1 1	X'13'
Sense	0 0 0 0 0 1 0 0	X'04'

The "M" represents the interrupt modifier bit which has meaning only for the Seek and Condition Release Interrupt orders. When set, the interrupt modifier bit allows a device interrupt to be initiated when an event specific to the order being executed occurs.

SEEK (X'83',X'03')

The Seek order alerts the controller to expect a two-byte disk address from the IOP; the controller loads that address into its own address register, wherein it becomes the current disk address. (Note that although the controller will accept a four-byte disk address, it ignores the contents of bytes two and three. Moreover, for a three-byte or four-byte disk address, the controller indicates incorrect length and continues the Seek operation. If a disk address greater in size than four bytes is specified, the controller terminates the operation and indicates unusual end.) The two or four bytes must be in the I/O Table in memory, starting at the address specified in the IOCD. The controller then directs any subsequent data transmissions to begin at this current disk address. The two (or four) byte address has this format:



where

track represents the desired track address and must be in the range $0 \leq \text{track} \leq 255$.

sector represents the desired sector address and must be in the range $0 \leq \text{sector} \leq 10$.

A byte count other than two causes the controller to signal "incorrect length", and a byte count other than two, three, or four also causes "unusual end" in the operational status byte without completing the Seek operation.

After the controller sends the last communication to the device to initiate the Seek, the controller executes order-in to the IOP and enters the ready state.

When the interrupt modifier bit of the Seek order is set (X'83'), a device interrupt is initiated when the controller senses the device is ready to Read, Seek, or Write – within 400 microseconds. If the controller is busy when the Seek is completed, the interrupt call to the IOP is postponed until the controller is no longer busy. Furthermore, the interrupt call may be temporarily withdrawn upon receipt of an SIO, HIO, TIO, or TDV instruction for another device.

Seek orders may be issued successively to several devices, and each device will interrupt as it completes its operation. The time involved is less than 10 microseconds.

WRITE (X'01')

The Write order causes the controller to automatically record the following on the RAD at the current RAD address: the header (current RAD address comprising track and sector numbers as specified and maintained in the controller address register) followed by the 1024 data bytes. Should the byte count field in the IOCD specify fewer than 1024 bytes, the remainder of the sector is zero-filled (X'0'). The current RAD address is determined by the previous Seek order, or by the last sector accessed, augmented by one. The data to be recorded must be in the I/O Table in memory starting at the memory address indicated in the IOCD. Because the controller automatically records the current RAD address with each Write operation, no address verification is possible.

Writing is initiated at the start of the addressed sector after recording the sector header. Should the record length be greater than one sector, the controller automatically augments the sector address to the next sector in sequence, and writes its header before writing the data bytes therein. Upon completing the last sector of a track, the controller sets the sector number to zero and augments the track address to the next track in sequence. Thus a single Write order may cause a number of sequential sectors or tracks to be written on.

Writing continues until one of these events terminates the operation:

1. An output data parity error is detected from the IOP. Writing terminates at count-done with transmission error set.

2. Count-done was received coincident with end-of-sector, (i.e., after writing a record on the sector).

3. Count-done was received, the remainder of the sector was written with zeros, and the check character (cyclic error detection bytes) was written.

4. The RAD system becomes not operational. Writing terminates with unusual end set.

5. The controller track address was augmented past the last track address, and another data operation was attempted. Writing terminates with unusual end set, with TDV status bit 2 set, and with track end error set (bit 4 of byte 8 retrieved with a Sense order).

6. A rate error (data overrun) occurs. Writing terminates with transmission error set.

7. The operator performs an I/O RESET action at the 550 or 560 system control console, or an HIO instruction is executed. Writing terminates, and the controller becomes ready without further communication with the IOP.

8. An IOP halt is indicated in the terminal order to the controller. If the terminal order indicating IOP halt occurs before the order-in sequence, the controller sets unusual end in the order-in and becomes ready. If the terminal order indicating IOP halt occurs during the order-in sequence, the controller becomes ready without further communication to the IOP.

9. A write-protect signal is received from the device. Writing terminates with unusual end set.

See the discussion of soft and hard Write errors in the section Read, Write, and Seek Errors, later in this chapter.

CHECK-WRITE (X'05')

The Check-Write order verifies recorded data – that is, it causes the controller to compare bytes read from RAD storage with the bytes received from the IOP. Data on the RAD and in memory are not recorded or modified, only compared. When a byte does not compare (check-write error), the operation terminates at the completion of the sector with transmission error set. Note that a byte count that is not a multiple of the sector length results in incorrect length being set.

The comparison continues until one of these events terminates the operation:

1. Count-done signal is received.

2. The RAD system becomes not operational. Check-writing terminates with unusual end set.

3. The controller track address was augmented past the last track address, and another data operation was attempted. Writing terminates with unusual end set, with TDV status bit 2 set, and with track end error set, (bit 4 of byte 8 retrieved with a Sense order).

4. A rate error (data overrun) occurs. Check-writing terminates with transmission error set.

5. The data bytes do not compare, or an error is encountered in the data check character (cyclic error detection bytes). The operational status indicates transmission error.

6. The operator performs an I/O RESET action, or an HIO instruction is executed. Check-writing terminates, and the controller becomes ready without further communication with the IOP.

READ 1 (X'12')

The Read 1 order causes the controller to begin reading from the RAD, at the current RAD address in the controller address register, the number of data bytes specified by the byte count field in the IOCD; the controller verifies the header before reading the data. The data will be stored in the I/O Table in memory, starting at the address indicated in the IOCD. The current RAD address is determined by the previous Seek order or by the last sector accessed, augmented by one.

Sector data parity errors are reported following the reading of the sector in which they occurred. Sector parity is determined from the cyclic error detection bytes (check character) written at the end of each sector. Such errors are reported as transmission data errors in the operational status. If the specified data byte count is not a multiple of the sector record length, incorrect length is set.

Transfer of data from the disk to the IOP is initiated at the start of the addressed sector after reading and verifying the header. Should the record length be greater than one sector, the controller automatically augments the sector address to the next sector in sequence, and reads and verifies its header before reading the data bytes therein. Upon completing the last sector of a track, the controller sets the sector number to zero and augments the track address to the next track in sequence. Thus a single Read 1 order may cause a number of sequential sectors or tracks to be read.

Reading continues until one of these events terminates the operation:

1. Count-done signal is received coincident with the end of a sector, after the check character has been read and compared.

2. Count-done signal is received prior to the end of a sector. The controller reads the remaining data bytes without transmitting them to the IOP, and reads and compares the check character.

3. The RAD system becomes not operational. Reading terminates with unusual end set.

4. The controller track address was augmented past the last track address, and another data operation was attempted. Reading terminates with unusual end set, with TDV status bit 2 set, and with track end error set (bit 4 of byte 8 retrieved with a Sense order).

5. A rate error (data overrun) is detected. Reading terminates with transmission error set.

6. A check character that does not compare is encountered. Reading terminates at the end of the errored sector, and transmission error is set.

7. The operator performs an I/O RESET action, or an HIO instruction is executed. Reading terminates, and the controller becomes ready without further communication with the IOP.

8. An IOP halt is indicated in a terminal order to the controller. If the terminal order indicating IOP halt occurs before the order-in sequence, the controller sets unusual end in the order-in and becomes ready. If the terminal order indicating IOP halt occurs during the order-in sequence, the controller becomes ready without further communication with the IOP.

9. A verification error is detected. Reading terminates with unusual end set and the current RAD address preserved (i.e., not augmented). The controller does not automatically perform a reread.

See the discussion of soft and hard Read errors in the section Read, Write, and Seek Errors, later in this chapter.

READ 2 (X'02')

A Read 2 order differs from a Read 1 order in that any data check character error is reported following the sector in which count-done occurs. Otherwise, the operation is the same as described for the Read 1 order (see the previous section, Read 1 (X'12').

See the discussion of soft and hard Read errors in the section Seek, Read, and Write Errors, later in this chapter.

RESERVE (X'07')

The Reserve order causes the controller to select and reserve the addressed device and then to terminate with channel-end set. Note that any SIO instruction automatically selects and reserves the addressed device. Thus a Reserve order is a no operation order. In dual access mode, the addressed device remains reserved and is automatically released upon completion of the subsequent I/O order if the automatic release feature is enabled in the controller; otherwise, a Release order is required to release the addressed device. See also Release (X'17') later in this chapter, and Dual Access Considerations.

RELEASE (X'17')

The Release order causes the controller to issue a release control signal to the addressed device, thereby releasing that device for use by the other controller. If the controller is in automatic release mode (implicit release), or if dual access is not configured, this order is a no operation order.

CONDITION RELEASE INTERRUPT (X'1F',X'0F')

The Condition Release Interrupt order sets (order code X'1F'), or resets (order code X'0F') an interrupt indicator bit in the controller, and terminates the order with channel end set.

When the controller recognizes that a device has been released by the other controller, it generates a device interrupt if this indicator is set.

The program must use SIO device address X'F' to initiate this order, thereby allowing the controller to set the condition release interrupt flag even if all devices are reserved by the other controller.

A reset signal received from the IOP causes the controller to reset the condition release interrupt flag. An HIO instruction with address X'F' also resets the flag and releases any pending interrupts.

SELECT TEST MODE (X'13')

The Select Test Mode order is used only for diagnostic purposes. A detailed description can be found in the design specification.

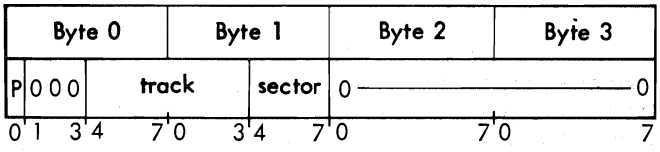
The Select Test Mode order puts the controller into the selected test mode of operation. The selectable test modes are data turnaround and device simulation. To indicate to the RAD I/O program that it is in test mode, the controller responds to TDV and AIO instructions by setting condition code bit 2 (CC2).

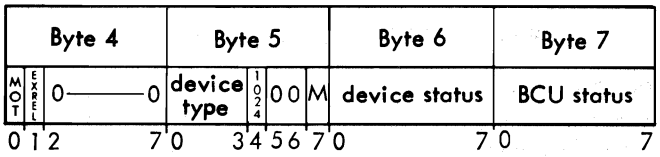
The data turnaround test mode is selected to verify data transmission between the IOP and the controller, to check data handling within the controller, and to test parity checking and parity error detection within the controller.

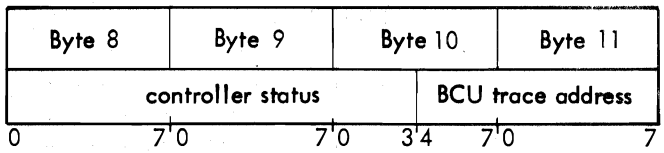
The device simulation test mode is selected to test the completeness of Seek, Sense, Write, Read 1, Read 2, and Check-Write operations without actually using a device; a device simulator in the controller is used instead.

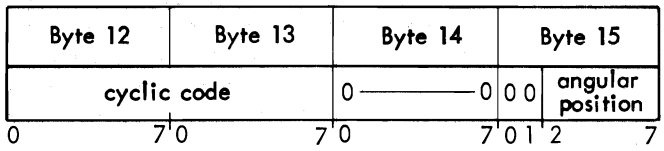
SENSE (X'04')

The Sense order causes the controller to transfer to the IOP as many as 16 bytes of information that describe the current state of the controller and device. The sense bytes are stored in the I/O Table in memory, starting at the address specified in the IOCD. The format of the 16 bytes sent to the IOP by a Sense order is









where

P represents write-protect bit; set if the current track address is write-protected.

track represents the current 8-bit track address stored in the controller.

sector represents the current 4-bit sector address.

MOT represents the not ready-to-Seek, Read, or Write indicator from the RAD; 1 means not ready, and 0 means ready to execute any of those operations. (This value is always inverse the value of bit 1 of Sense byte 6 – device status.)

EXREL represents the explicit release bit; 0 means implicit reserve and release of device, and 1 means implicit reserve and explicit release of device.

device type represents the 4-bit device type. Value may be only

Value	Type of Disk
0001	Full RAD, 256 tracks, 11 sectors, Model 3214.

M represents the value of Seek interrupt modifier bit; 0 means no interrupt is pending, and 1 means an interrupt is pending the device's reaching seek time-out (Seek operation).

device status represents the eight indicators describing device status. Bit position assignments are

Bit	Meaning When Set
0	Logical address interlock.
1	Ready.
2	Available (dual access function).
3	Ready to Seek, Read, or Write.
4	Write check.
5	Dual access mode.
6	Write-protected.
7	Seek interlock.

BCU represents the six indicators describing BCU status and has meaning only to diagnostic routines. Bit position assignments are

Bit	Meaning When Set
0	0 (not set).
1	Controller sequence error.
2	Sequence decode error.
3	Microorder decode error.
4	Link stack underflow.
5	Link stack overflow.
6	Link pointer decode error.
7	Control word parity error.

controller status represents 21 single-bit indicators that describe the status of the controller. Byte and bit position assignments are

Byte	Bit	Meaning When Set
8	0	Check-write error.
8	1	Cyclic code error.
8	2	IOP parity error.
8	3	Data overrun.
8	4	Track end error.
8	5	Seek error.
8	6	Order parity error.
8	7	Test mode order error.
9	0	(not used.)
9	1	Device not ready.
9	2	(not used.)
9	3	Header sector error.
9	4	Header track error.
9	5	Reserve error.
9	6	Channel address error.
9	7	RAD address error.
10	0	Device parity error.
10	1	Data parity error.
10	2	Data control field error, or address field error.
10	3	A bus parity error.

BCU trace address represents the 12-bit value contained in the BCU trace address register and has meaning only to diagnostic routines. Byte and bit assignments are

Byte	Bits	Meaning
10	4-7	Contain the value of bits 0-3 of the BCU trace address register.
11	0-7	Contain the value of bits 4-11 of the BCU trace address register; or contain the data control address at the time of the error if byte 7 bit 1 is set or byte 10 bit 5 is set.

cyclic code represents the 16-bit value of the last cyclic code written, or read from a device; or byte 12 contains the track number and byte 13 the sector number read from the RAD if byte 9 bit 3 is set or byte 9 bit 4 is set.

angular position represents the current angular position of the device. In order to read the angular position from the device, a Sense order with a byte count of 16 will take up to 1600 microseconds longer than a Sense order with a byte count of 14.

KEY EVENTS

The following key events can occur during a RAD I/O operation:

- Start of input/output.
- Channel end condition.
- Unusual end error condition.
- Transmission data error condition.
- Incorrect length error condition.

Each key event is described below separately. Assume no chronological order of occurrence from the order of presentation, for none is intended. What generally happens in an I/O operation is that I/O is started and sometime subsequently terminated with an interrupt. The RAD I/O program queries the interrupt to determine whether the latter was device-generated (and thus indicated successful termination), or generated because of an error (unsuccessful termination), or generated because of a time-out occurrence (a hardware malfunction that is generally recoverable).

START INPUT/OUTPUT

An I/O operation is initiated with the execution of an SIO instruction in the RAD I/O program. If the I/O address is recognized, and the controller is in the ready condition with no interrupt pending, and the device is "available" and in the ready condition, the controller then sets its "I/O address recognition" and "SIO accepted" indicators. The controller then advances from the ready condition to the busy condition, requests an I/O order byte from the IOP, and proceeds with the I/O operation defined by the order byte.

CHANNEL END CONDITIONS

The controller signals channel end with each order-in. The order-in takes place after any of the following events occurs:

1. Controller received a count-done signal during a Sense operation.
2. Controller executed a Seek order to a device.
3. The check character has been written in the last sector following issue of the count-done signal for a Write order.
4. The check character has been received for the last sector following issue of the count-done signal for a Check-Write order.
5. A Release order, Select Test Mode order, or Condition Release Interrupt order has been received and executed.
6. An IOP data-out parity error was detected.
7. Data overrun (rate error) was detected.
8. The check character was read during either a Read 1 order or a Check-Write order with a transmission error recognized.
9. An unusual end condition was detected.

UNUSUAL END ERROR CONDITIONS

The controller indicates unusual end when any of these events occurs:

1. The controller received an out-of-range or illegal Seek address, or attempted to transfer data when the address had been incremented out of range.
2. An invalid order was detected, or an order parity error was detected.
3. The not operational condition occurred during the busy state.
4. The controller detected incorrect parity or a verification error during a Read, Write, or Check-Write operation.
5. IOP Halt occurred.
6. Incorrect length was detected for a Seek order.
7. The controller detected a device interface error.
8. A write-protect violation occurred (there was an attempt to write on a write-protected volume).
9. An IOP parity error was detected on order-out, terminal order, channel address, or Seek address.

TRANSMISSION DATA ERROR CONDITIONS

The controller indicates data transmission error when any of these events occurs:

1. The check character check failed at the end of a sector during a Read or Check-Write operation.
2. Data comparison failed during a Check-Write operation.
3. Data overrun (rate error) was detected.
4. An IOP data-out parity error was detected.

INCORRECT LENGTH ERROR CONDITIONS

The controller indicates incorrect length error when either of these conditions occurs:

1. Byte count was other than two or four for a Seek order.
2. Byte count of data record was other than a multiple of the sector length for a Read, Write, or Check-Write order.

STATUS RESPONSE

The I/O instructions can request a device to return detailed I/O status information when the instruction is executed. Detailed descriptions of the I/O instructions can be found in the Xerox 550/560 Computer Reference Manuals; summary status information is discussed in the following sections and related tables and figures.

CONDITION CODES

When an I/O instruction is executed, condition code bits 1 and 2 (CC1 and CC2) are set or reset to describe the general status of the addressed I/O device and controller. Table 6 lists the CC1 and CC2 values and their significance for the I/O instructions.

Table 6. Condition Code Settings

I/O Instruction	CC1	CC2	Meaning
SIO	0	0	I/O address recognized and SIO accepted.
	0	1	I/O address recognized and SIO not accepted.
	1	0	Controller busy with device other than addressed device and unable to send status.
	1	1	I/O address not recognized.
TIO	0	0	I/O address recognized and SIO can currently be accepted.
	0	1	I/O address recognized and SIO cannot currently be accepted.
	1	0	Controller busy with device other than addressed device and unable to send status.
	1	1	I/O address not recognized.
HIO	0	0	I/O address recognized and device not busy when halt occurred.
	0	1	I/O address recognized and device busy when halt occurred.
	1	0	HIO not accepted. Controller busy with device other than addressed device. Status unavailable.
	1	1	I/O address not recognized.
TDV	0	0	I/O address recognized.
	0	1	Controller in test mode; TDV instruction used as a diagnostic tool.
	1	0	Controller busy with device other than addressed device; controller unable to send status.
	1	1	I/O address not recognized.

Table 6. Condition Code Settings (cont.)

I/O Instruction	CC1	CC2	Meaning
AIO	0	0	Normal interrupt recognition.
	0	1	Unusual condition interrupt recognition, or controller switched to a test mode.
	1	0	Invalid code.
	1	1	No-interrupt recognition.

DEVICE STATUS BYTE

The current status of the device and controller is returned to the IOP (and the register) at the beginning of an SIO, TIO, HIO, TDV, or AIO instruction in the form of the Device Status Byte. See Tables 7, 8, and 9.

A Device Status Byte is sent to the IOP upon receipt of an AIO instruction if there is an interrupt pending. Device Status is reset upon completion of the AIO. See also Disk System Interrupt Environment later in this chapter for a discussion of the kinds of interrupts that could be pending.

OPERATIONAL STATUS

When the controller terminates any operation, before it leaves the busy state it makes an order-in service call to the IOP and transmits the following status to condition code bits 1 and 2:

- Transmission data error (CC1).
- Incorrect length (CC2).

and this status in the Operational Status Byte:

- Channel end (always set).
- Unusual end.

See the Xerox 550/560 Computer Reference Manuals for the position of the status elements in the Operational Status Byte. See Key Events, earlier in this chapter, for the lists of conditions that can cause a data transmission error, incorrect length indication, channel end, and unusual end.

ADDITIONAL PROGRAMMING CONSIDERATIONS

INFORMATION PROTECTION

The contents of the RAD are protected in the event of primary power failure — the recorded information will not be lost or altered. Moreover, the contents are further protected by the write-protect feature, which disables the write

Table 7. Device Status Byte for SIO, TIO, and HIO

Bit Position	Function	Value	Meaning
0	Interrupt pending	1	Set if device interrupt is pending (issued, and not yet acknowledged by an AIO instruction).
1,2	Device condition		Describes the device's current condition as follows:
		00	Device ready.
		01	Device not operational.
		10	Device unavailable (reserved by other channel).
		11	Device busy, or arm in motion.
3	Mode	1	Always set to indicate automatic mode.
4	Unusual end	1	Set if the previous controller operation terminated with an unusual end.
5,6	Controller condition		Describes the controller's current condition as follows:
		00	Controller ready.
		01	Controller not operational.
		10	Not applicable.
		11	Controller busy.
7	Unassigned	0	Always zero.

Table 8. Device Status Byte for TDV

Bit Position	Function	Value	Meaning
0	Unassigned	0	Always zero.
1	Flaw detection	0	Not applicable to RAD – always zero.
2	Programming error	1	Any of these events occurred: • Data record length incorrect for Seek order. • Byte count greater than 16 specified for Sense order. • Data address incremented to a nonexistent address and a Read or Write was attempted. • Seek attempted while an on-sector interrupt was pending. • Invalid order detected.

Table 8. Device Status Byte for TDV (cont.)

Bit Position	Function	Value	Meaning
2	Programming error (cont.)		• Test mode order with invalid data bytes attempted, or byte count other than two specified for test mode data. • Invalid order attempted for device address X'F'. • Out-of-range or illegal Seek address received.
3	Write protection violation	1	Controller detected a write-protection violation.
4	Parity error	1	Any of these events occurred: • Parity error detected on order from IOP. • Parity error detected on Seek address data from IOP. • Parity error detected on terminal order from IOP. • Parity error detected by IOP on channel address from controller. • Invalid code from IOP detected. • Parity error detected on test mode bytes.
5	Operational error	1	Any of these events occurred: • Controller detected a device interface error. • Device became deselected or nonoperational, or detected an operational error while busy with the controller. • Data address comparison failure during comparison of track or sector address; or difference detected in Seek, track, or sector address during a Read or Check-Write operation with the device. • Controller became nonoperational while busy. • Internal controller error detected.
6	Verification error or Seek time-out		Either of these events occurred: • Verification error detected while comparing header with data address. • Seek time-out occurred while controller busy with Seek, Read, Write,or Check-Write operation.
7	Header parity error	0	Not applicable to RAD – always zero.

Table 9. Device Status Byte for AIO

Bit Position	Function	Value	Meaning
0	Data overrun	1	Data overrun (rate error) occurred during execution of the previous order.
1	Attention interrupt	1	RAD transited from not operational state to ready automatic state.
2	Release interrupt	1	Release interrupt acknowledged.
3	Unassigned	0	Always zero.
4	Seek complete interrupt	1	Seek complete interrupt acknowledged.
5	Unassigned	0	Always zero.
6	Seek time-out error interrupt	1	Seek time-out error interrupt acknowledged.
7	Unassigned	0	Always zero.

amplifier to reduce the possibility of recorded information being inadvertently written over. If writing is to be performed, the operator must depress the applicable front panel PROTECT switch(es) to extinguish the indicator(s) and enable the write process. The operator can reestablish the write-protect status at any time by again depressing the appropriate PROTECT switch(es) and reilluminating the PROTECT indicator(s).

COMMAND CHAINING AND DATA CHAINING

The RAD system is designed to permit a multiple number of orders relating to an I/O operation to be executed consecutively – that is, track switching and order modification: Read to Write and vice versa, multiple Reads or Writes, Read or Write to Seek to Read or Write. These chained orders are executed without the program's having to specify another SIO instruction. To take advantage of the command chaining feature, the command chain flag must be set in the IOCD for each record except the last.

Command chaining in the intersector gap can be accomplished only at the end of long sectors – that is, at the end of odd sectors in even-numbered tracks, even sectors in odd-numbered tracks, or any last sector (sector 10). Command chaining at any other point results in the loss of one rotation.

Seeking from even to even track at the end of long sectors, odd to odd track, and even to odd track can be accomplished without rotational loss. However, seeking from an odd track to an even track at the end of an even sector will result in the loss of one rotation if the Seek is to the next sector position.

Because optimizer routines in a RAD I/O program usually allow one or more sector spaces between records, implications of the long and short sector sizes pertain only to the limitation just described to seeking operations. Routines using a Sense operation prior to a Seek will always perform as expected, for the Sense information will always be correct, and the Seek will occur to the next available sector – that is, one sector later. See also, Xerox 550 or 560 Computer Reference Manual, Chapter 4, for a discussion of command chaining.

The RAD system is also designed to handle data chaining – gather data from several areas of memory to write a single logical record on the RAD (gather-write), and read data from a single logical record on RAD into several areas of memory (scatter-read). If two or more IOCDs are required to perform a gather-write or scatter-read operation, the data chain flag (DC) must be set in each IOCD except the last for the logical record. The IOP automatically fetches the next IOCD when the byte count of the current IOCD reduces to zero, and updates parameters. The device and controller continue to perform as though the operation were specified by a single IOCD.

Frequent data chaining (small byte counts) or frequent use of test instruction loops (TIOs and TDVs) reduce the transfer rate as much as 50 percent, and can cause data overruns

(rate errors). That is because of the additional communication required between the I/O system and the Basic Processor, and because of the memory required for data chaining for test instruction loops.

See also, Xerox 550/560 Computer Reference Manuals, Chapter 4, for a discussion of data chaining.

SURFACE OPERATIONS

After reading or writing a sector, the controller automatically augments the sector address to the next sector in sequence. When it completes reading or writing the last sector of a track, the controller sets the sector address to zero and increments the track address to the next track in sequence. Thus a single order can cause a number of sequential sectors or tracks to be written.

Note that frequent TIO and TDV instructions during surface operations can cause data overrun conditions.

Should a track be flawed, a spare head must be wired in.

SEEK OPERATIONS

When the Seek interrupt modifier bit (order code X'83') is set, an interrupt occurs when the controller senses device ready and Seek complete.

PROGRAM I/O INTERRUPT ENVIRONMENT

The program establishes its I/O interrupt environment by setting flags in the IOCDs, and by using specified time-out delays in software time-out routines. The recommended software time-out delay for disk operations is a minimum of one second.

These flags must be set:

ICE — Interrupt at Channel End. Set only in last IOCD of a command list.

IUE — Interrupt at Unusual End. Set in all IOCDs.

HTE — Halt on Transmission error. Set in all IOCDs.

SIL — Suppress Incorrect Length. Set whenever an incorrect length condition should inhibit an IOP halt and the subsequent unusual end I/O interrupt.

The IZC (Interrupt at Zero Byte Count), DC (data chaining), CC (command chaining) and Skip flags may be set as needed.

RAD SYSTEM INTERRUPT ENVIRONMENT

The RAD system interrupt environment comprises two types of interrupts. The first type is that generated by the IOP to the controller to indicate channel end, unusual end, transmission error, or incorrect length. The second type is initiated by the device (and generated by the controller) to indicate Seek completed or device released. The IOP-generated interrupts have priority over the device-initiated interrupts. The controller-busy-with-one-device situation has priority over an interrupt generated by another device.

Interrupts are cleared by an AIO or HIO instruction, or by an I/O RESET action taken by the operator at the 550 or 560 system control console. An AIO or HIO instruction to a single device will clear only one interrupt, whereas an HIO instruction to device X'F', or the I/O RESET action clears all interrupts by clearing all device interrupt flags.

The Seek time-out interrupt, Release interrupt, and IOP-generated interrupt are discussed individually in the following sections.

SEEK TIME-OUT INTERRUPT

The controller generates a Seek time-out interrupt when it detects a device error immediately following a Seek and Interrupt operation.

The interrupt can be cleared by an AIO or HIO instruction, or by an I/O RESET action taken by the operator. An HIO to a device address other than X'F', or an AIO instruction will clear a single instruction. An HIO to device address X'F', or the I/O RESET action will clear all pending interrupts for all devices.

RELEASE INTERRUPT (DUAL ACCESS MODE)

The Model 1049 dual access feature originates the release interrupt when a device is released by the other controller. The current controller recognizes no release signals from devices unless a Condition Release Interrupt order has been issued to enable the release interrupt logic – that is, unless the interrupt modifier bit in the order code for the Condition Release Interrupt order was set (order code X'1F').

The release interrupt call is temporarily removed by a TIO, TDV, HIO, or SIO instruction issued to another device, until the I/O instruction is completed. An AIO or HIO instruction to the interrupting device clears the interrupt.

IOP-INITIATED INTERRUPT

The IOP can set an interrupt call by setting data bit zero in a terminal order. An AIO or HIO instruction, or an I/O RESET action clears the interrupt.

DUAL ACCESS CONSIDERATIONS

Two dual access configurations are possible: a single Basic Processor (BP) with two controllers sharing one or more devices, and dual BPs sharing one or more devices through separate controllers. In a dual BP configuration, no status communication is shared between the BPs.

In dual access mode, the Model 104 dual access feature selects and reserves the device upon acceptance of the first SIO instruction from either controller. The device remains reserved until released either by execution of a Release order, by an I/O RESET or SYS RESET action taken by the operator at the 550 or 560 system control console, by a power failure, or by shut down in the reserving controller. This method is called programmed release.

Note by contrast that in single access configurations (one BP and one controller), all orders reserve the device and automatically release it at channel end. This method is called implicit reserve and release.

Note: Care must be taken when operating with dual access systems to avoid accessing a RAD via a second IOP, while between a Seek, Read, or Write operation and a Sense operation via the first IOP. If this situation does occur, the Sense data may be misleading for these fields: P (byte 0 bit 0), MOT (byte 4 bit 0), and device status (byte 6).

RAD SYSTEM ERROR DETECTION ENVIRONMENT

The controller is provided with logic for automatically detecting errors in data transmission to and from the controller. The controller will implement no error correction on its own; the program must provide routines for error recovery. The controller logic can detect these errors: IOP parity error, device parity error, read error, and file address error. They are discussed in the following sections.

IOP PARITY CHECK

Odd parity is generated and checked for all data-in transfers to the IOP, and is checked for all data-out transfers on the single-byte interface. "Data transmission error" indicates a data parity error, and "unusual end" indicates an order parity error.

DEVICE PARITY CHECK

The controller generates odd parity for the interface lines. If an interface is configured in the RAD system, it checks the interface lines for odd parity; otherwise no device parity check is performed.

READ CHECK CHARACTERS CHECK

In a Write operation, the controller computes and writes a two-byte check character at the end of each data sector written on the RAD. During a Read or Check-Write operation, the controller again computes a two-byte check character and compares it with the check character read from the RAD. "Transmission error" indicates any error in a data record, and "unusual end" indicates any error in a header.

The controller read-check-characters check can detect absolutely all single-burst errors of fewer than 17 bits, single-burst errors of 17 bits with a probability of $1-(1/2)^{15}$, and burst errors of greater than 17 bits with a probability of $1-(1/2)^{16}$. In general, the controller has a Read error detection capability of 99.9997 percent for any possible error.

FILE ADDRESS VERIFICATION

The controller verifies file address by comparing it with that read in the header during a Read or Check-Write only. Any file address verification error results in order termination with unusual end.

I/O FAULT DETECTION AND ERROR RECOVERY ACTIONS

The RAD I/O program must consider three events during the performance of an I/O operation – initiation of the I/O operation, occurrence of an I/O interrupt, and the non-occurrence of an expected I/O interrupt. This section and the following primarily describe error detection at the time an I/O interrupt is received. Start I/O failures and the software time-out fault are included for completeness.

The RAD I/O program can determine whether a RAD I/O operation was terminated successfully or because of a fault condition by evaluating the status response and condition code bits 1 and 2 (CC1 and CC2) returned from the issue of AIO and TDV instructions after an I/O interrupt. Moreover, the program can perform tests to determine whether the I/O interrupt occurred because of a device interrupt, or because of a channel end or unusual end interrupt.

Note: Controller busy with device other than the one addressed (CC1, CC2 = 10) will be given during controller self-test and initialization following an I/O RESET action. Time of this operation is approximately four milliseconds plus time to respond to the I/O instruction.

SIO FAILURE

CC1 and CC2 reset to zero following an SIO instruction indicate a successful I/O operation. If both bits are not zero, perform recovery action 1 (see Recovery Actions following Table 10). After a successful SIO instruction, the RAD I/O program is informed of the completion of the current I/O operation through an I/O interrupt, or alternately by a software time-out if no interrupt is generated.

I/O INTERRUPT

The program must perform tests (see Fault Testing Sequence, later in this chapter) to determine whether the I/O interrupt resulted from a device interrupt, or from a channel end or unusual end interrupt. The two (device interrupts and channel end/unusual end interrupts) are mutually exclusive. If bit 1, 2, 4, or 6 of the status from an AIO instruction is set to one, the current I/O interrupt is a device interrupt. Otherwise the program may assume a channel end or unusual end interrupt.

DEVICE INTERRUPT

Of the device interrupts (release, IOP, and Seek time-out), only the Seek time-out interrupt is considered a fault. Use recovery action 3 for this fault. No other device interrupt indicates a fault condition.

CHANNEL END OR UNUSUAL END INTERRUPT

The program can evaluate the status response and CC1 and CC2 following AIO and TDV instructions after an I/O interrupt to determine whether the I/O operation was completed successfully or was terminated because of a fault condition. If a fault condition terminated the operation, use the fault testing sequence in Table 10 to determine the recovery action to take.

An I/O operation can be considered successful if all the status response bits and CC1 and CC2 are as follows:

1. After an AIO instruction, CC1 and CC2 are both zero.
2. After a TDV instruction, CC1 and CC2 are both zero.
3. Bits 8, 9, and 12 of the AIO status are all zero.
4. Bits 8-15 of the TDV status are all zero.

If one or more of those bits is not zero, the program must issue a TIO instruction to obtain more information about the RAD system.

SOFTWARE TIME-OUT FAULT

The software time-out fault is a software-detectable fault situation that occurs when the I/O interrupt for the current I/O operation is not received within the software time-out period allowed for the current (type) I/O operation. The RAD I/O program must issue an HIO and a TDV instruction to determine the current state of the RAD system (see Table 10).

READ, WRITE, AND SEEK ERRORS

Before presenting the recommended fault testing sequence, it is necessary to define what is meant by "soft" and "hard" Read and Write errors, and by Seek errors. An error can be considered a Read error only if the data were read correctly at least once after they were written. A soft Read error is an error that occurs during a Read operation and can be corrected as the result of one or more re-Read operations (not to exceed 10). A hard Read error is a Read error that cannot be corrected in as many as 10 re-Read operations.

In like manner, errors can be considered Write errors only if a Write operation is immediately followed by verification by reading (Read after Write or Check-Write); only if such verification is successful can the data be considered error-free. A soft Write error is a Write error that can be corrected after one re-Write, whereas a hard Write error is a Write error that cannot be corrected by one re-Write – it is an irrecoverable error (see Irrecoverable Errors, later in this chapter).

A Seek error is declared when a Seek time-out fault occurs, or the track register in the RAD disagrees with that in the controller, or the controller receives a Seek order to an out-of-range address.

FAULT TESTING SEQUENCE

The fault testing sequence is meaningful only to the programmer writing an I/O handler. It is therefore not applicable to programs performing input/output operations through an operating system.

Because one or more status bits may be set when a fault occurs, the RAD I/O program must perform testing for the fault occurrence in a fixed sequence. Table 10 shows the testing sequence priorities. The recovery actions annotated in Table 10 are described in the section following the table.

Before it performs fault testing, the RAD program must issue a TIO instruction to determine the device and controller conditions.

RECOVERY ACTIONS

The following recovery actions, which are annotated in Table 10, are based on the application of the fault testing sequence defined by Table 10. To determine the correct recovery action to take, first determine the failing order (Seek, Sense, etc.). The fault testing sequence was designed with the assumption that for multisector operations, the failing sector can be determined and recovery action taken on the appropriate sector. For that reason it is recommended that read operations use the Read 1 order (order code X'12') to ensure that a failure is reported immediately following the failing sector. If the Read 2 order (X'02') is used, any fault indications may actually be attributable to more than one sector, and an alternate fault testing sequence may be required.

Table 10. RAD Fault Testing

Sequence and Summary Description	Status Response Bits and Detailed Information	Seek	Sense, Release, Condition Release Interrupt	Read 1, 2, Write	Check-Write	Recommended Corrective Action
Step 1. Perform only if CC1, CC2 ≠ 00 for a TDV instruction.	TDV CC1, CC2 = 01. Test Mode. The controller has been placed in test mode because of a programming error or a hardware failure.	X	X	X	X	See recovery action 1.
	TDV CC1, CC2 = 10. Controller busy with device other than one addressed. This error is the result of a hardware failure.		X			See recovery action 2.
		X		X	X	See recovery action 3.
	TDV CC1, CC2 = 11. Address not recognized.	X	X	X	X	See recovery action 1.
Step 2. Perform only if TIO 5, 6 ≠ 00, indicating the controller is not ready.	TIO 5, 6 = 01. Not operational. This error is the result of an internal controller failure.	X	X	X	X	See recovery action 1.
	TIO 5, 6 = 10. Not defined. The controller was not ready immediately after an I/O interrupt.	X	X	X	X	See recovery action 1.
	TIO 5, 6 = 11. Busy. The controller failed to return to the ready state immediately after the I/O interrupt because of a hardware malfunction or because the command list was coded with multiple interrupts.		X			See recovery action 2.
		X		X	X	See recovery action 3.
Step 3. Perform only if TIO 1, 2 ≠ 00, indicating the device is not ready.	TIO 1, 2 = 01. Not operational. The device is not operational as the result of a power failure, or because the device has been placed in the off-line state. Consider both circumstances hardware malfunctions.	X	X	X	X	See recovery action 1.
	TIO 1, 2 = 10. Unavailable. In a dual access configuration, the addressed device is unavailable to the addressed controller because the device is reserved by the other controller.	X	X	X	X	See recovery action 1.

Table 10. RAD Fault Testing (cont.)

Sequence and Summary Description	Status Response Bits and Detailed Information	Seek	Sense, Release, Condition Release Interrupt	Read 1,2, Write	Check-Write	Recommended Corrective Action
Step 3. (cont.)	TIO 1,2 = 11. Busy. The device failed to return to the ready state because of a hardware malfunction, or because the command list is coded with multiple interrupts.		X			See recovery action 2.
		X		X	X	See recovery action 3.
Step 4. Perform only if TDV 10, 11, 12, 13 ≠ 0000, indicating an IOP operational error.	TDV 11 = 1. Memory address error. This error may be the result of a hardware malfunction, or a programming error.	X	X			See recovery action 2.
				X	X	See recovery action 3.
	TDV 12 = 1. IOP memory error. This error is the result of a hardware malfunction.	X	X			See recovery action 2.
				X	X	See recovery action 3.
	TDV 13 = 1. IOP control error. This error is the result of a hardware malfunction, or a programming error.	X	X			See recovery action 2.
				X	X	See recovery action 3.
	TDV 10 = 1. Transmission memory error. This error is the result of a hardware malfunction.			X	X	See recovery action 3.
Step 5. Perform only if TDV 4 ≠ 0, indicating a parity error on information received from the IOP.	TDV 4 = 1. Parity error (IOP). This error is the result of a hardware malfunction caused by one of these circumstances: 1. Parity error detected on order from IOP. 2. Parity error detected on Seek address data from IOP. 3. Parity error detected on terminal order from IOP. 4. Parity error detected by IOP on channel address from the controller. 5. Invalid instruction code from IOP.	X	X			See recovery action 2.
				X	X	See recovery action 3.

Table 10. RAD Fault Testing (cont.)

Sequence and Summary Description	Status Response Bits and Detailed Information	Seek	Sense, Release, Condition Release Interrupt	Read 1, 2, Write	Check-Write	Recommended Corrective Action
Step 6. Perform only if TDV 5 = 0, indicating operational error.	TDV 5 = 1. Operational error. This error is the result of a hardware malfunction in the controller, in the controller to device interface, or in the device. Specifically, these circumstances generate the error: 1. Controller detected a device interface error. 2. The device became deselected or not operational, or it detected an operational error while it was busy with the controller. 3. Internal controller error.	X	X			See recovery action 2.
				X	X	See recovery action 3.
Step 7. Perform only if TDV 2 ≠ 0, indicating a probable programming error.	TDV 2 = 1. Programming error. This error is the result of one of these circumstances: 1. Incorrect byte count was specified for a Seek operation. 2. A byte count greater than 16 was specified for a Sense operation. 3. An illegal Seek address was transmitted to the controller during a Seek operation. 4. Data address was automatically incremented to an illegal address (last track address +1) and a data operation (Write, etc.) was attempted. 5. A Seek was attempted while the arm was in motion or a sector interrupt was pending. 6. Invalid order code was detected. 7. Invalid test mode order attempted. 8. Invalid order for device address attempted.	X	X	X	X	See recovery action 5.

Table 10. RAD Fault Testing (cont.)

Sequence and Summary Description	Status Response Bits and Detailed Information	Seek	Sense, Release, Condition Release Interrupt	Read 1, 2, Write	Check-Write	Recommended Corrective Action
Step 7. (cont.)	If the above programming error is produced by a hardware malfunction, an alternate corrective action may be used.		X			See recovery action 2.
		X		X	X	See recovery action 3.
Step 8. Perform only if TDV 3 ≠ 0, indicating a write-protect violation.	TDV 3 = 1. Write-protect violation. The addressed sector is write-protected by manual hardware switches. The Write operation has been aborted.			X	X	See recovery action 5.
Step 9. Perform only if TDV 6 ≠ 0, indicating a seek verification error or a time-out error.	TDV 6 = 0. Verification error or time-out error. This error is the result of a hardware malfunction. The following circumstances can generate this error. 1. Sector address verification error during a data operation. 2. Track address verification error during a data operation. 3. Seek time-out detected during a Seek operation.	X		X	X	See recovery action 3.
Step 10. Perform only if TDV 9 ≠ 0.	TDV 9 = 1. Transmission data error. This error is the result of one of the following hardware errors:			X		See recovery action 3.
	1. Data overrun. The system failed to maintain the required data transfer rate during a Read, Write, or Check-Write operation. 2. Check-Write error. A data comparison error was detected during a Check-Write operation. 3. Sector parity error. The comparison of sector data parity with the expected parity failed during a Read or Check-Write operation. 4. Data-out parity error. A data parity error was detected on data from the IOP during a Write or Check-Write operation.				X	See recovery action 4.

Table 10. RAD Fault Testing (cont.)

Sequence and Summary Description	Status Response Bits and Detailed Information	Seek	Sense, Release, Condition Release Interrupt	Read 1, 2, Write	Check-Write	Recommended Corrective Action
Step 11. Perform only if steps 1 through 10 did not lead to a recovery procedure.	Inconsistent status error. The device-dependent status has failed to indicate the specific failure for which device-dependent status checking was invoked. Consider the error to be a hardware malfunction.		X			See recovery action 2.
		X		X	X	See recovery action 3.

These are the recovery actions:

Action	Description
1	Abort – operator intervention. Issue an HIO instruction and retry the order. Repeat the sequence – HIO, retry order – three times before considering the device not operational. The current operation must be aborted and the operator notified that the addressed device or controller (or both) has become not operational, or unavailable, or has entered the test mode. The operator must then perform the appropriate action before returning the controller and device to the operational state.
2	Order retry – program recovery. Issue an HIO instruction (in the case of controller condition busy) and retry the order. Repeat the sequence – HIO, retry order – 10 times before considering the fault irrecoverable.
3	Order retry after Seek – program recovery. Issue an HIO instruction (in the case of controller condition busy) followed by a Seek order to reestablish the surface address and the track position. Then retry the original order. Repeat that sequence 10 times before considering the fault irrecoverable.

Note: For recovery actions 2 and 3, allow approximately 10 microseconds between the HIO instruction and the order retry.

Action	Description
4	Order retry after Seek and Write. Take recovery action 3; however, before retrying the Check-Write operation, rewrite the failing sector.
5	Program notification – no recovery required. The program is notified of the following occurrences for which recovery action is not necessarily appropriate: • A write-protect violation has occurred on a write-protected surface. • An incorrect length indication appeared during an operation for which partial data transfer was acceptable. • Programming error – See Table 10, Step 7.

IRRECOVERABLE ERRORS

The action to be taken after an irrecoverable error varies with the order and with the user's application. For instance, the system may tolerate Sense failures, whereas Read failures can cause an action range from job abortion to system shutdown. Irrecoverable Write failures may merely require the

choice of another surface area and the disallowance of further operations on the failing sector, or sectors, to correct the situation. Consequently, it falls outside the scope of this manual to describe a specific action to take after an irrecoverable error.

FAULT LOGGING

An important part of the fault recovery procedure is the use of the Sense order to obtain additional failure indicators and the logging of that Sense data. Use a byte count of 14 for logging. Place the 14 bytes of Sense status and fault data in the error log with the I/O instruction status. These are the reasons for getting and logging Sense data:

1. The specific failure information is valuable for hardware repair.

2. A Sense order resets (clears) the failure indicators. The importance of this reason is that the failure indicators would otherwise remain set after the first occurrence of each fault. Note that if Sense orders are issued only occasionally, and not after every fault, the Sense bytes returned will contain misleading (i.e., past history) failure data.

4. OPERATIONS

Model 3214 RADs are housed four to a peripheral cabinet and may share a cabinet with Model 3242/3243 cartridge disk drives. Each RAD is slide-mounted in a separate pull-out drawer for ease of servicing. Figure 5 shows a peripheral cabinet housing a mix of RADs and cartridge disk drives.

This chapter, which describes the operating characteristics of the RAD system, comprises two main sections: The first illustrates and describes the operator control panel on the front of each RAD, and the last contains operating procedures that apply to RADs.

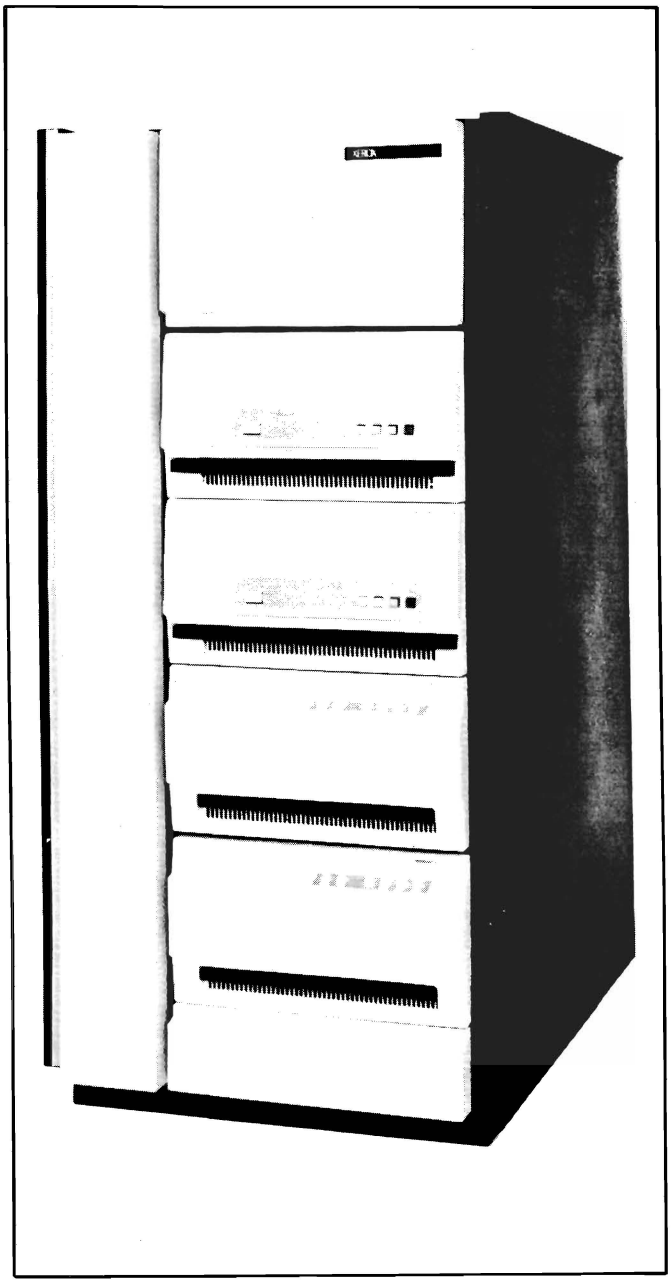


Figure 5. Peripheral Cabinet Housing RADs and Cartridge Disk Drives.

OPERATOR CONTROL PANEL

Displayed on the face of each RAD is an operator control panel containing one READY indicator lamp and four alternate-action PROTECT switches/indicators (see Figure 6). The controls and indicators are described below; their functions are summarized in Table 11 for quick reference.

READY INDICATOR

The READY indicator is a green signal light indicating that the RAD is ready to accept and execute orders from the RAD I/O program. The light comes on and remains on when all power is up to specification, the disk is rotating at its nominal speed, and no circumstance exists that would prevent seeking, reading, or writing.

PROTECT SWITCHES/INDICATORS

The PROTECT switches/indicators are four, white, backlighted, momentary-contact, alternate action, pushbutton switches used to guard against inadvertent writing on the RAD. Each PROTECT indicator glows white whenever writing is inhibited on the 64-track group associated with it. When the operator depresses a glowing PROTECT switch, the light is extinguished and write-protection is reset (inhibited) to allow writing. The operator can later set write-protection back on by depressing the unlighted PROTECT switch; the indicator will be illuminated.

OPERATING PROCEDURES

RADs require very little operator intervention. The information in this section includes the few general practices for operating RADs.

GENERAL OPERATING PROCEDURES

Follow these practices while operating the RADs to obtain the best performance and reliability from the equipment:

1. Keep the cabinet drawers closed.

2. A sustained tingling or scratching sound may be caused by head-to-disk contact. If this sound persists, stop the RAD and investigate the cause (see RAD Power Turn-Off Procedure, later in this main section;) perform steps 1 through 3 for the troubled unit.

3. Do not force a cabinet drawer open.

4. Do not try to override the cabinet thermal over-temperature interlock. This safety feature shuts down all equipment in the peripheral cabinet if the cabinet should become overheated.

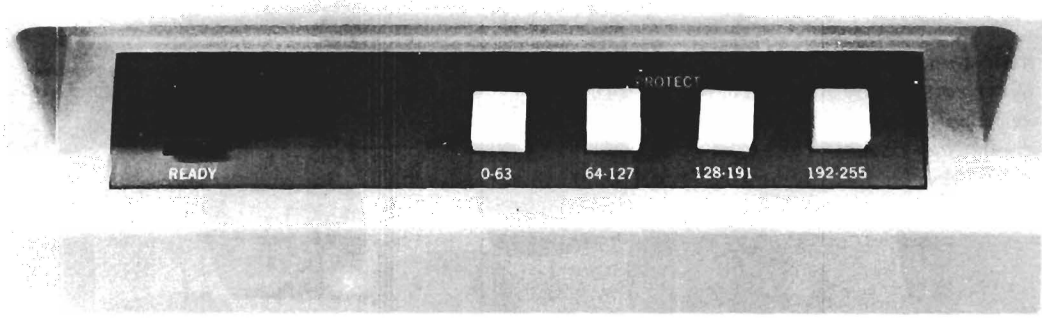


Figure 6. Operator Control Panel

Table 11. Operator Control Panel Summary

Indicator or Switch/Indicator	Function
READY	Illuminated when the disk is rotating at approximately 3540 rpm and no circumstance prevents normal RAD operations.
PROTECT 0-63	Illuminated when writing is inhibited (write-protection is on) for this group of 64 consecutive tracks. Extinguished when writing is allowed. To allow writing, depress the illuminated PROTECT switch. To inhibit writing, depress the extinguished PROTECT switch.
PROTECT 64-127	Illuminated when writing is inhibited (write-protection is on) for this group of 64 consecutive tracks. Extinguished when writing is allowed. To allow writing, depress the illuminated PROTECT switch. To inhibit writing, depress the extinguished PROTECT switch.
PROTECT 128-191	Illuminated when writing is inhibited (write-protection is on) for this group of 64 consecutive tracks. Extinguished when writing is allowed. To allow writing, depress the illuminated PROTECT switch. To inhibit writing, depress the extinguished PROTECT switch.
PROTECT 192-255	Illuminated when writing is inhibited (write-protection is on) for this group of 64 consecutive tracks. Extinguished when writing is allowed. To allow writing, depress the illuminated PROTECT switch. To inhibit writing, depress the extinguished PROTECT switch.

POWER

Power to the controller is on so long as power to the host computer is on.

The RADs have their own power supplies and require 120 VAC for the 60 Hz version and 220 VAC for the 50 Hz version. The power supplies are mounted on the bottom of each RAD above the bottom cover. Note that after power is initially turned on when a RAD system is installed, it must not be turned on and off under normal operating conditions.

POWER DISTRIBUTION PANEL

A power distribution panel (accessible through the rear cabinet door and located at the bottom of the cabinet – see Figure 7) houses these major power switches: a three-position rotary switch, four circuit breakers, and one appliance button. See Figure 8.

RADs are referred to as nonswitched units, because there is no switch on the RAD operator control panel for starting and stopping a RAD. Conversely, cartridge disk drives are referred to as switched units, because the LOAD/RUN switch on the cartridge disk operator control panel allows the operator "remote" control over starting and stopping a cartridge disk drive. The powering up of both kinds of units is locally controlled by the setting of the sequence switch.

The three-position, rotary, sequence switch (labeled REMOTE LOCAL OFF) affects power to all nonswitched and switched units (RADs and cartridge disk drives) in the cabinet. When the switch is in the OFF position, only the RADs will have power supplied to them. When the switch is in the LOCAL position, power is supplied to both RADs and cartridge disk drives in the cabinet; the operator, however, has no remote control over the cartridge disk drives – the LOAD/RUN switch is ineffectual. When the switch is in the REMOTE position, power is supplied both to RADs and cartridge disk drives, and the operator has further (remote) control over the cartridge disk drives via the LOAD/RUN switch.

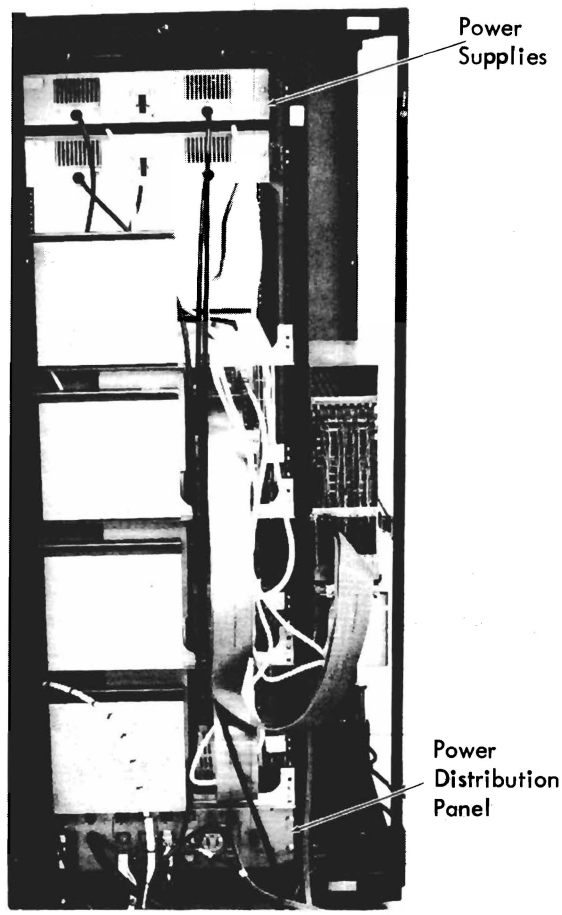


Figure 7. Power Supplies and the Power Distribution Panel

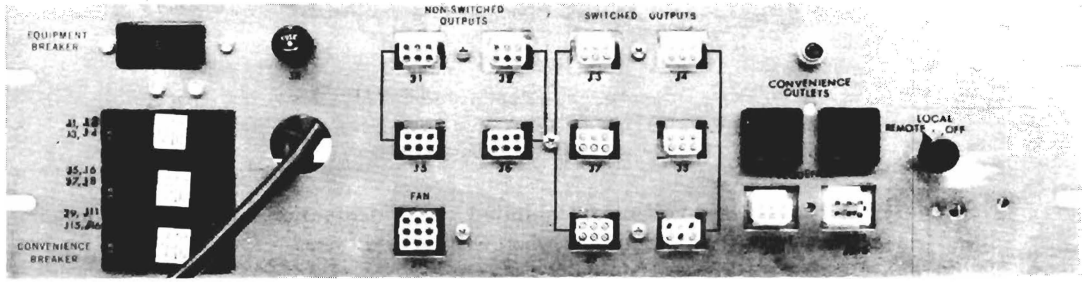


Figure 8. Power Distribution Panel

The main circuit breaker, labeled EQUIPMENT BREAKER, controls power to the entire ac distribution panel. The main breaker automatically shuts off if the cabinet temperature should cause the fan thermostat to close, and thereby protects all equipment in the cabinet from damage.

Two circuit breakers (one labeled J1 J2 J3 J4, and the other labeled J5 J6 J7 J8) control power to the maximum of four units installed in the cabinet – one circuit breaker for each two units. The outlets labeled J1, J2, J5, and J6 are for the plug-in of nonswitched units (RADs) and the outlets labeled J3, J4, J7, and J8 are for the plug-in of switched units (cartridge disk drives).

The fourth major circuit breaker, labeled J9 J11 J15 J16, controls power to the autotransformer, which in turn controls power to the ac contractors, the sequencer and the PT50 power supplies (outlet J9), the cabinet fan (outlet J11) and to whatever equipment is plugged into the convenience outlets (J15 and J16). Note that on the 50 Hz version system, this circuit breaker is labeled J9 J11, as there are no convenience outlets on the power distribution panel.

The appliance button, labeled CONVENIENCE BREAKER, is a red pushbutton designed for convenience protection against an overload situation that might arise from the plug-in of such testing equipment as oscilloscopes in the convenience outlets. There are no appliance button and convenience outlets on the 50 Hz version power distribution panel.

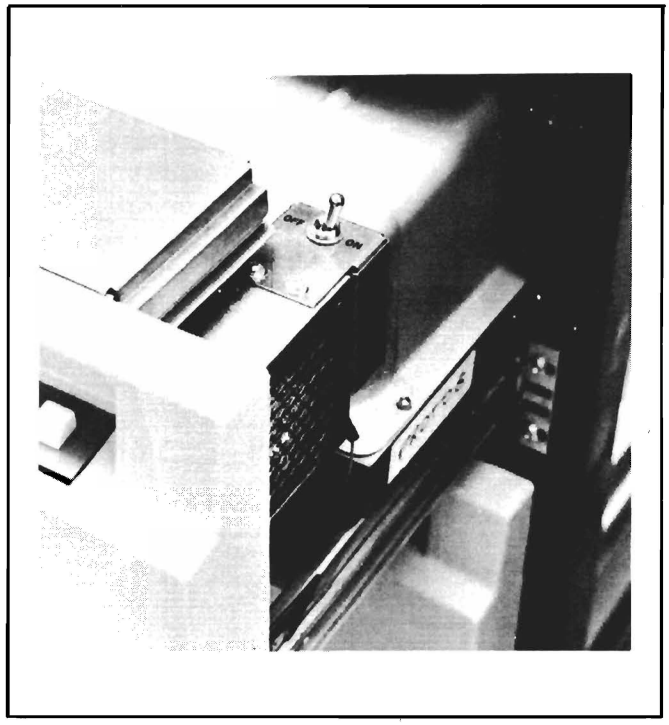


Figure 9. Location of dc Power Switch

RAD POWER TURN-OFF PROCEDURE

Power to the RADs is not normally turned off. Exceptions to this rule are any instructions for power turn-off at the installation itself, or any laws or regulations. Another exception is an emergency. In some installations the customer service engineer will turn off the power if required. In others, the operator may have to turn off the power. This is the procedure:

1. Pull up the black handle bar located across the front of the RAD to open the RAD drawer. Located behind the operator control panel and to the right of the electronics chassis is the dc power switch. Toggle it to the OFF position. Close the drawer. Repeat for each RAD in the cabinet (see Figure 9).

2. Open the rear door of the peripheral cabinet.

3. Located at the rear of each RAD unit (see Figure 10) is a single toggle switch – the motor switch. Toggle it down. Repeat for each RAD.

4. Wait until the motors have stopped.

5. Throw the main circuit breaker (labeled EQUIPMENT BREAKER) on the power distribution panel.

Power to the RADs has now been properly shut down.

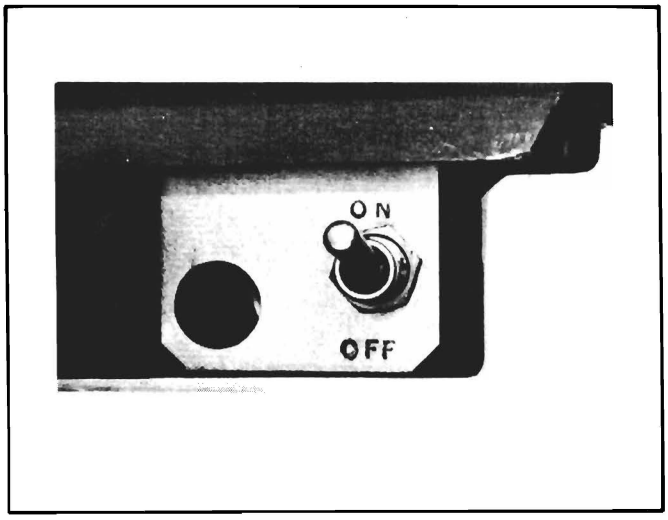


Figure 10. Location of RAD Motor Switch

If cartridge disk drives are also installed in the cabinet, before performing the RAD power turn-off procedure, set the LOAD/RUN switch on each cartridge disk operator control panel to LOAD, and wait for the LOAD indicators to light.

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