SCP-500C

DISK MASTER (TM) DISK CONTROLLER

Note: When it becomes available, a regular instruction manual will be sent to replace this temporary manual. Those end-users purchasing this product through their local computer store should write to us requesting this replacement manual so we know where to send it.

Revision A:

October 4, 1982

Preliminary User's Manual for the
Model SCP–500C <u>D</u>ISK <u>M</u>ASTER Floppy Disk Controller

Features

> Handles up to eight disk drives, four 8–inch <u>and</u> four 5.25–inch.

> Physically and electrically seperate connectors for 8–inch and 5.25–inch disk drives to eliminate crosstalk and overloading of signal drivers.

> Configuration header to handle the different pin arrangement of PerSci drives.

> Complete <u>automatic</u> hardware support for disk drives with "voice–coil" head positioners.

> Complete <u>automatic</u> hardware support for disk drives with spindle–motor control.

> A breakthrough in data separator design for unsurpassed data–recovery reliability—patent pending.

> Based on the famous Western Digital 1793 disk controller chip.

> 100–percent compliance with the IEEE–696 standard.

> Direct Memory Access capability when combined with Seattle Computer's forthcoming Direct Memory Access Controller board.

PORT ADDRESS switch – The Disk Master requires six I/O ports which are grouped consecutively starting on any eight-port boundary called the BASE. The BASE is selected using the top five positions of the PORT ADDRESS switch. These five switches are labeled A7 – A3 and correspond to the address lines A7 – A3 on the bus.

A7	A6	A5	A4	A3	I/O port address base
0	0	0	0	0	00 hex
0	0	0	0	1	08 hex
0	0	0	1	0	10 hex
0	0	0	1	1	18 hex
0	0	1	0	0	20 hex
0	0	1	0	1	28 hex
0	0	1	1	0	30 hex
0	0	1	1	1	38 hex
0	1	0	0	0	40 hex
0	1	0	0	1	48 hex
0	1	0	1	0	50 hex
0	1	0	1	1	58 hex
0	1	1	0	0	60 hex
0	1	1	0	1	68 hex
0	1	1	1	0	70 hex
0	1	1	1	1	78 hex
1	0	0	0	0	80 hex
1	0	0	0	1	88 hex
1	0	0	1	0	90 hex
1	0	0	1	1	98 hex
1	0	1	0	0	A0 hex
1	0	1	0	1	A8 hex
1	0	1	1	0	B0 hex
1	0	1	1	1	B8 hex
1	1	0	0	0	C0 hex
1	1	0	0	1	C8 hex
1	1	0	1	0	D0 hex
1	1	0	1	1	D8 hex
1	1	1	0	0	E0 hex
1	1	1	0	1	E8 hex
1	1	1	1	0	F0 hex
1	1	1	1	1	F8 hex

The bottom three positions of the "Port Address" switch are not used.

INTERRUPT jumper – interrupts from the Disk Master can be sent to any of the eight Vectored Interrupt lines VI0 – VI7 or directly to the INT line for systems without interrupt controllers. The blue shunt should be placed to cover one of the nine vertical pairs of pins corresponding to the nine different interrupt lines. If none of the interrupt lines should be used, put the shunt on any two of the pins in the upper row.

WAIT jumper – this jumper selects whether or not the Disk Master asks for wait-states when the CPU talks to the 1793 disk controller chip. The WAIT jumper should be in the ON position for all CPUs faster than a 2-MHz 8080 or Z80. With the WAIT jumper in the ON position, the number of wait states asked for depends on the CPU speed: the faster the CPU's clock, the more wait-states will be requested.

The following switch and jumper only need attention if you have a DMA controller in your system.

DMA PRIORITY switch — this switch selects the DMA priority to which the Disk Master will respond. Since the DMA controller is not physically located on the Disk Master board, the Disk Master must monitor the S-100 bus to determine when a DMA cycle is being run for it. The DMA priority lines are used to determine when the Disk Master's DMA controller (one of up to sixteen possible DMA controllers) is active. The DMA PRIORITY switches are labeled "DMA 0 – 3" on the board to the left of the switch and "1" and "0" above the switch.

DMA 3	DMA 2	DMA 1	DMA 0	priority hex	priority decimal	
0	0	0	0	0	0	lowest priority
0	0	0	1	1	1	
0	0	1	0	2	2	
0	0	1	1	3	3	
0	1	0	0	4	4	
0	1	0	1	5	5	
0	1	1	0	6	6	
0	1	1	1	7	7	
1	0	0	0	8	8	
1	0	0	1	9	9	
1	0	1	0	A	10	
1	0	1	1	B	11	
1	1	0	0	C	12	
1	1	0	1	D	13	
1	1	1	0	E	14	
1	1	1	1	F	15	highest priority

DMA jumper — the Disk Master sends DMA requests to the Direct Memory Access Controller board using one of the "NDEF" pins of the S-100 bus. This jumper selects which one is used.

CH1   pin 65
CH2   pin 66

AUTO MOT/SM AUTO/ON jumper – this jumper lets the Disk Master know which drives have spindle motors which are under it's control.

AUTO MOT	Disk Master controls motors of both 8–inch and 5.25 inch drives.
SM AUTO	Disk Master controls 5.25–inch spindle motors, 8–inch spindle motors are assumed always on.
ON	Spindle motors of both 8–inch and 5.25–inch drives are assumed to be always on.

LARGE MOT ON jumper – controls the polarity of the "motor on" signal going to the 8–inch disk drives.

LO	active–low motor–on (PerSci drives)
HI	active–high motor–on (Tandon drives)

Most standard–height 8–inch drives have AC spindle motors which can't be turned on and off, so the setting of this jumper is irrelevant when using these drives.

MOT ON jumper – this jumper selects how long the Disk Master will wait for the spindle motors to come up to speed.

F	1/2 second
S	1 second

MOTOR OFF DELAY – this jumper selects how long the Disk Master will keep the spindle motors going after the disk heads have been unloaded.

F	7.5 seconds
S	15 seconds

HEAD LOAD jumper – this jumper selects whether 8–inch drives use the "head load" signal or the "drive select" signal to load the heads.

HL	drives use "head load"
DS	drives use "drive select"

FAST SEEK jumper – this jumper selects whether the 8–inch drives have standard stepper motor head positioners or "voice coil" head positioners.

ON	voice coil positioner
OFF	stepper motor positioner

PRECOMP jumper – this jumper selects whether write precompensation is turned on and off by the 1793 disk controller chip using the TG43 signal, or whether write precompensation is enabled by a bit in the Auxilliary Command port. If the 1793 controls write precompensation, it will be turned on for all tracks beyond track 43. Write compensation is not used with single–density.

PROG	write precompensation controlled by Auxilliary Command port.
AUTO	write precompensation controlled by 1793's TG43 signal.

8-INCH DRIVE CONFIGURATION HEADER — this sixteen-pin socket between IC17 and IC18 is used to re-arrange the signals on the 50-pin connector for the 8-inch drives.

```
          function   pin   pin   function
                 _____
               |          |
     RESTORE  | 1       16 |
 DISK CHANGE  | 2       15 |  connector pin 12
 SIDE SELECT  | 3       14 |  connector pin 14
        TG43  | 4       13 |  connector pin  2
 DRIVE SELECT 3 | 5     12 |  connector pin 30
   HEAD LOAD  | 6       11 |  connector pin 18
 DRIVE SELECT 4 | 7     10 |  connector pin 32
             | 8        9 |  connector pin  4
             |_____|
```

```
   standard drive            PerSci drive

     1      16                1 ⟍    16
     2 ——— 15                 2    ⟍ 15
     3 ——— 14                 3 ⟍    14
     4 ——— 13                 4    ⟍ 13
     5 ——— 12                 5 ⟍    12
     6 ——— 11                 6    ⟍ 11
     7 ——— 10                 7 ⟍    10
     8       9                8    ⟍  9
```

The Disk Master uses a total of six I/O ports for communication with the CPU. These six ports can be set on any eight–port boundary called the BASE. See the description of how to select the BASE using the PORT ADDRESS switch as described above in the section "Switches and Jumpers – Bus Interface." The six I/O ports are used as follows:

> BASE+0 – 1793 Command/Status register (see 1793 data sheet)
> BASE+1 – 1793 Track register   "   "
> BASE+2 – 1793 Sector register   "   "
> BASE+3 – 1793 Data register   "   "
> BASE+4 – Auxilliary Command/Status port
> BASE+5 – Wait Synchronization port

The 1793 uses the first four ports, these will be fully described in the complete manual which will be released later. Till that manual is available, refer to a 1793 data sheet.

Bits of the Auxilliary Command port:

```
   Bit 7    Bit 6    Bit 5    Bit 4    Bit 3    Bit 2    Bit 1    Bit 0

    DMA      DMA     precomp   small   double    side     DS1      DS0
   write    enable   enable    drive   density

    I_____I
             I
         restore
```

DMA WRITE – this bit controls the DMA direction.

> 0 – read memory (write disk)
> 1 – write memory (read disk)

Notice that the DMA direction refers to the direction of the _memory_ access, not the disk access. DMA WRITE should be low when DMA ENABLE is low otherwise RESTORE will be activated (see below).

DMA ENABLE – with this bit on, DMA requests are passed to the DMA controller and the Disk Master responds to DMA cycles on the bus. With this bit off, no DMA requests are sent to the DMA controller and the Disk Master ignores DMA cycles on the bus. To turn off DMA, be sure to turn off both DMA ENABLE _and_ DMA WRITE otherwise RESTORE will be activated (see below).

RESTORE – the RESTORE function for PerSci drives is activated by selecting

> DMA WRITE = 1
> DMA ENABLE = 0

If you don't have PerSci drives, all RESTORE does is load the head of the selected drive. This can be a handy way to keep the head loaded to perform head alignment or other maintenance of disk drives.

PRECOMP ENABLE – this bit controls whether or not write precompensation is used when writing to double–density disks. It also controls the "low write current" or "TG43" signal to 8–inch drives. If the PRECOMP jumper (see the above section "Jumpers and Headers – Disk Interface") is in the AUTO position this bit does nothing: write precompensation and write current are controlled by the TG43 signal from the 1793 disk controller chip.

SMALL DRIVE – this bit selects whether a 5.25-inch drive or an 8-inch drive is being used. When 5.25-inch drives are selected, the 8-inch drive selects are disabled, and vice-versa. It is this feature which allows having four 8-inch drives <u>and</u> four 5.25-inch drives connected to the Disk Master at the same time.

        0 – 8-inch
        1 – 5.25-inch

DOUBLE-DENSITY – this bit selects double-density operation when high, single-density operation when low.

        0 – single-density
        1 – double-density

SIDE – this bit selects side zero of double-sided disks when low. Side one is selected when this bit is high.

DS1 & DS0 – these two bits select one of four drives of each size.

DS1	DS0	drive
0	0	1
0	1	2
1	0	3
1	1	4

Bits of the Auxilliary Status port:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
disk change*	2-sided	head load	X	X	X	X	interrupt request

DISK CHANGE* – Many Shugart-type 8-inch disk drives provide a "disk change" signal on pin 12 of the 50-pin connector which can be read using this status bit. If the disk has been changed, this bit will be <u>low</u>.

2-SIDED / SEEK COMPLETE – If your 8-inch drives are standard Shugart-type double-sided drives, there is probably a "two-sided" signal on pin 10 of the 50-pin connector which can be read using this status bit. When a double-sided disk is used, this bit will be <u>high</u>.

If your 8-inch drives are PerSci drives, the state of the Seek Complete signal can be read using this bit. This bit will be <u>high</u> when the seek is completed.

HEAD LOAD – this bit will be high when the disk drive head is loaded (including a head-load forced by RESTORE).

INTERRUPT REQUEST – the state of the 1793's interrupt request pin can be read using this bit. If this bit is high, the disk controller is requesting an interrupt.

X – the X bits are undefined, so don't count on them to have any particular value.

The Wait Synchronization port duplicates the function of the Auxilliary Command/Status port with the exception that any access of this port will hold the CPU in wait states till either Interrupt Request or Data Request from the 1793 disk controller chip become active. This port is usually used to make the CPU wait till the 1793 disk controller is ready to accept data or have data taken from it in non-DMA systems.