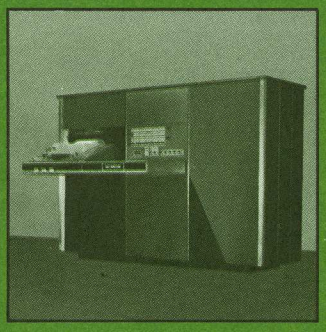
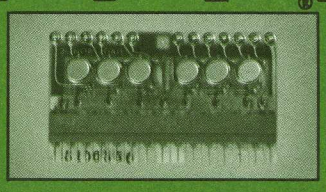
systems engineering laboratories, incorporated

BULLETIN 9056A

SEL 840A GENERAL PURPOSE DIGITAL COMPUTER

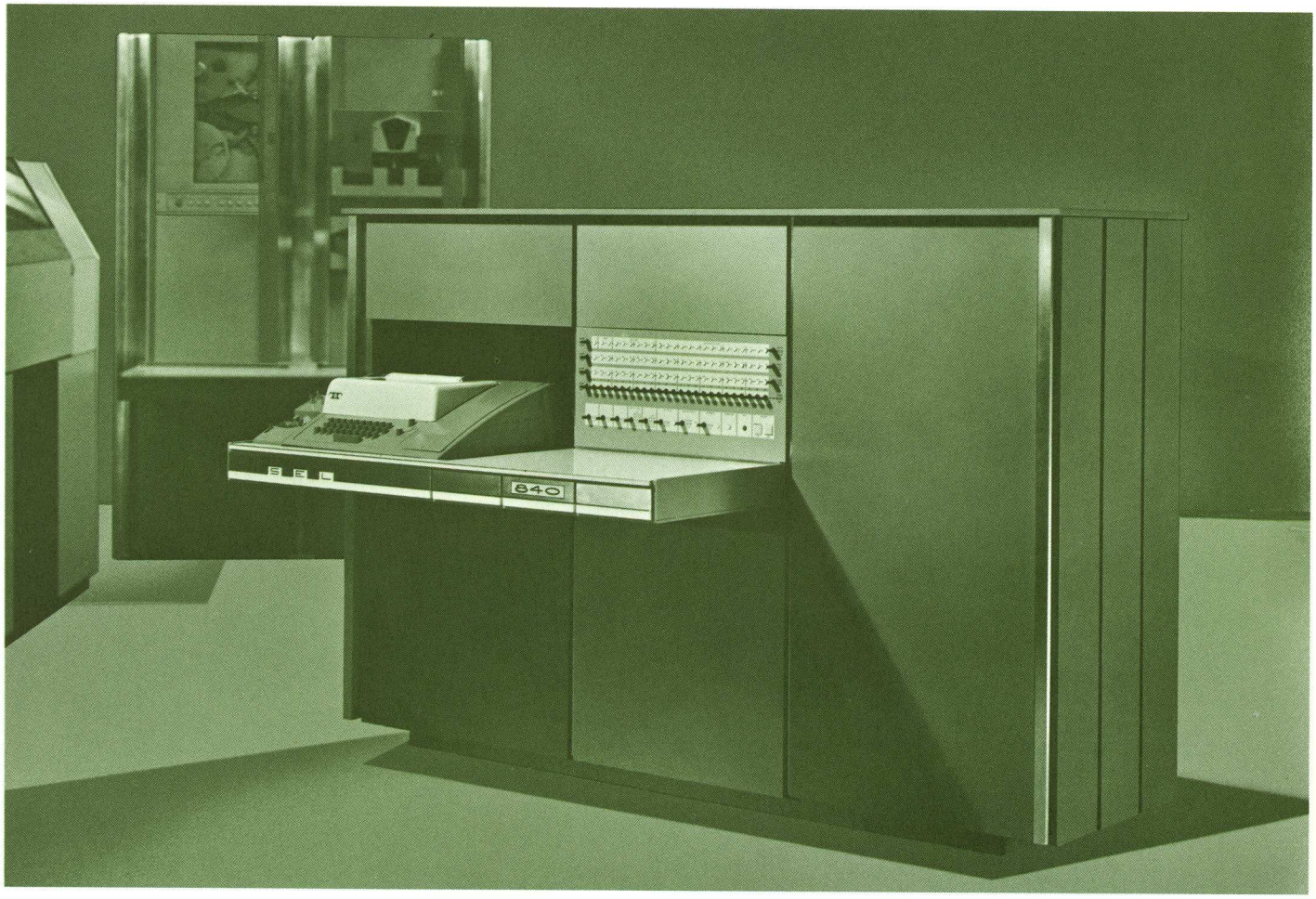


SEL®



FEATURES

- **ALL SILICON MONOLITHIC INTEGRATED CIRCUITS**
- ONE PASS ASA FORTRAN IV INCLUDING RECURSIVE SUBROUTINE CAPABILITY
- OPTIONAL EXTENDED ARITHMETIC UNIT PROVIDES CONCURRENT FLOATING POINT ARITHMETIC
- 1.75-MICROSECONDS FULL CYCLE - FULL PARALLEL OPERATION
- UP TO 32,768 WORDS OF MEMORY DIRECTLY ADDRESSABLE
- BINARY TWO'S COMPLEMENT NUMBER REPRESENTATION
- 24-BIT BINARY WORD PLUS PARITY AND PROGRAM PROTECT BITS (MAXIMUM OF 26 BITS)
- UP TO THREE HARDWARE INDEX REGISTERS
- MULTI-LEVEL INDIRECT ADDRESSING
- UP TO 60 TRUE LEVELS OF PRIORITY INTERRUPT
- UP TO EIGHT FULLY BUFFERED I/O CHANNELS
- EXTENSIVE AND VERSATILE INSTRUCTION LIST
- UNIT I/O CONTROL COMMUNICATING WITH UP TO 128 UNITS
- COMPLETE SET OF PERIPHERAL UNITS
- COMPATIBLE WITH SEL STANDARD ACQUISITION AND PROCESS CONTROL SUB-SYSTEMS



THE SEL 840A GENERAL PURPOSE 24-BIT PARALLEL COMPUTER HAS THE HIGHEST THROUGHPUT RATE OF ANY MACHINE IN ITS SIZE AND PRICE CLASS. IN ADDITION TO FULFILLING REQUIREMENTS FOR VERSATILE HIGH SPEED COMPUTATION, THE SEL 840A PROVIDES SYSTEM CAPABILITIES DEVELOPED THROUGH EXTENSIVE SEL EXPERIENCE IN THE DATA ACQUISITION AND CONTROL FIELDS. A COMPREHENSIVE INPUT/OUTPUT CONFIGURATION PRODUCES THE FLEXIBILITY NECESSARY FOR SEL 840A USE IN THESE APPLICATIONS:

- GENERAL PURPOSE SCIENTIFIC COMPUTATION
- HIGH SPEED DATA PROCESSING
- ON-LINE, REAL TIME DATA READOUT IN ENGINEERING UNITS
- ON-LINE DATA COMPRESSION, CORRECTION AND RECORDING
- REAL TIME CLOSED LOOP DIRECT DIGITAL CONTROL
- HIGH SPEED AUTOMATIC CHECKOUT AND TESTING
- AUTOMATION OF INDUSTRIAL PROCESSES
- SUPERVISORY CONTROL SYSTEMS

SEL 840A BASIC SPECIFICATIONS

WORD SIZE

24 Bits + Parity Bit

INTERNAL OPERATION

Fully Parallel

INTERNAL MEMORY FULL CYCLE TIME

1.75 Microseconds

CORE STORAGE

4096 Words

I/O UNIT

ASR-33 Typewriter with Paper Tape Reader and Punch (10 Characters/Second)

TEMPERATURE ENVIRONMENT

10°C to 35°C (50°F to 95°F)

SIZE

72" Wide x 53" High x 27" Deep
(43" Deep Including Desk Top)

COMPUTATION TIMES INCLUDING ACCESS AND INDEXING:

ADD .....3.5 Microseconds
SUBTRACT .....3.5 Microseconds
MULTIPLY .....10.5 Microseconds
DIVIDE .....26.25 Microseconds

THE FOLLOWING HARDWARE AND FEATURES ARE ALSO INCLUDED WITH MAIN FRAME:

Hardware Program Counter
Double Length Accumulator
Multi-Level Indirect Addressing
Complete Software Package
Manual Program Stop and Four Sense Switches
Hardware Index Register
Two Independent Levels of True Priority Interrupt
Unit I/O Control with Drivers for 16 Output Units and Terminators for 16 Input Units
Memory Parity Check
Multiply and Divide Hardware

SEL 840A STANDARD OPTIONS

ADDITIONAL CORE STORAGE IN MAIN FRAME

Up to 32,768 words in modules of 4096 or 8192 words each

ADDITIONAL PRIORITY INTERRUPTS

Up to 60, each individually armable

BLOCK TRANSFER CONTROL UNITS

Enables block transfer logic to transfer data between memory and peripheral units in a fully buffered, cycle stealing mode. A cyclic, automatic reinitialization capability is provided.

ADDITIONAL SENSE SWITCHES

20 Available

EXTENDED ARITHMETIC UNIT (EAU)

An optional arithmetic and control unit that performs hardware single and double precision and floating point arithmetic independent of the main arithmetic unit, but sharing the memory.

TIME SHARING OPTIONS

Program Protect
I/O Instruction Trap
Stall Alarm

POWER FAIL SAFE

REAL-TIME CLOCK

Resolution 1 Millisecond

SEL 840A COMPUTER ORGANIZATION

MEMORY

Up to four 4096 or 8192 word magnetic core modules provide a maximum of 32,768 24-bit storage locations. All 32,768 locations are directly addressable.

"A" ACCUMULATOR (A)

Main Arithmetic Register

"B" ACCUMULATOR (B)

A 24-bit extension of the "A" Accumulator

TRANSFER REGISTER (T)

The register into which all words from memory are stored pending operation.

INDEX REGISTER (I)

Up to three addressable 15-bit hardware index registers.

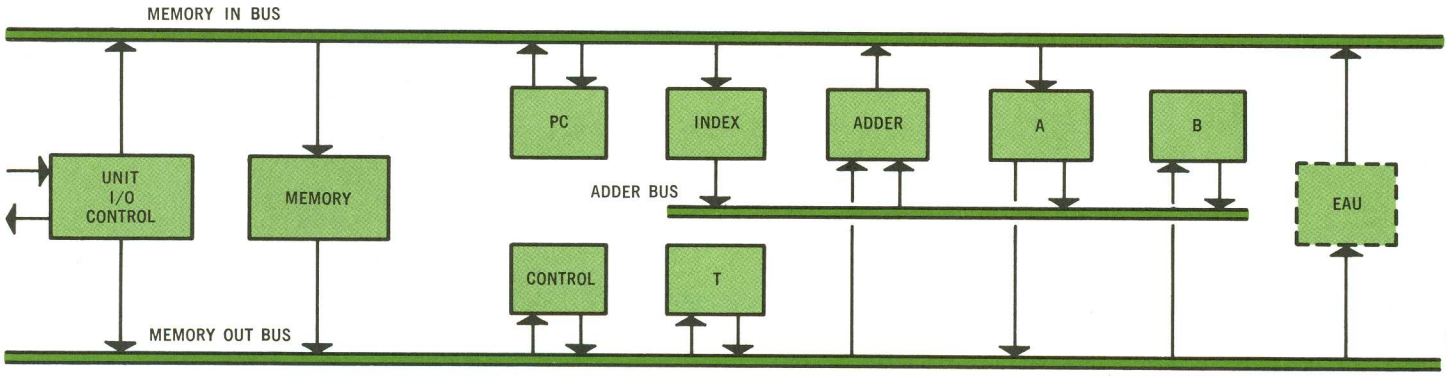
ADDER

Full 24-bit parallel adder used in all arithmetic and logical operations.

PROGRAM COUNTER (PC)

A 15-bit incremental counter that provides the current instruction address.

SEL 840A BLOCK DIAGRAM

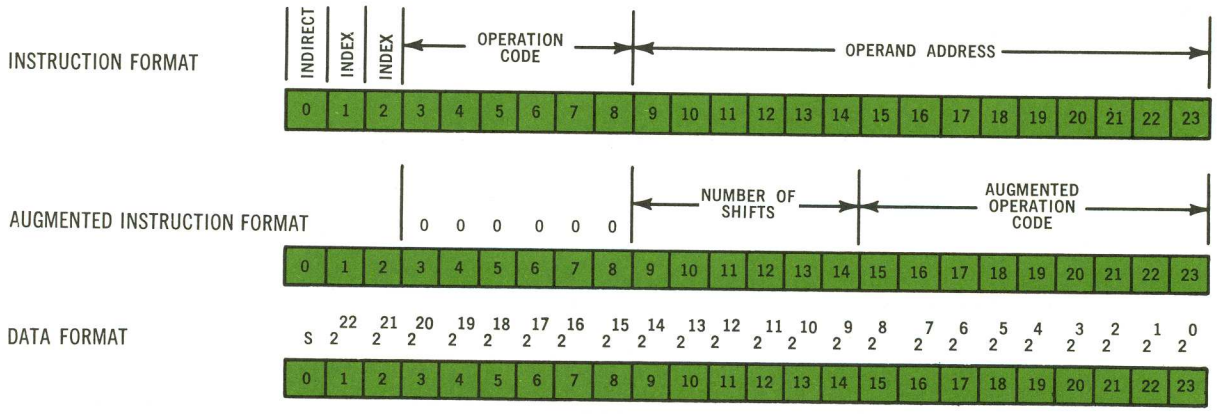


INPUT/OUTPUT CONFIGURATION

The basic SEL 840A is equipped with a Unit I/O Control which can connect 128 I/O units to the processor. For maximum versatility 24-bit data words are transferred through the I/O control to/from memory or to/from the A accumulator.

Up to eight block transfer control (BTC) units can be added as options to allow direct communication between I/O devices and computer memory. Data transfer is fully buffered and may occur at word rates up to 572 KC. Only one memory cycle is stolen for each word transferred. The block transfer logic is capable of automatic reinitialization from the contents of two fixed memory locations each time a block transfer is completed.

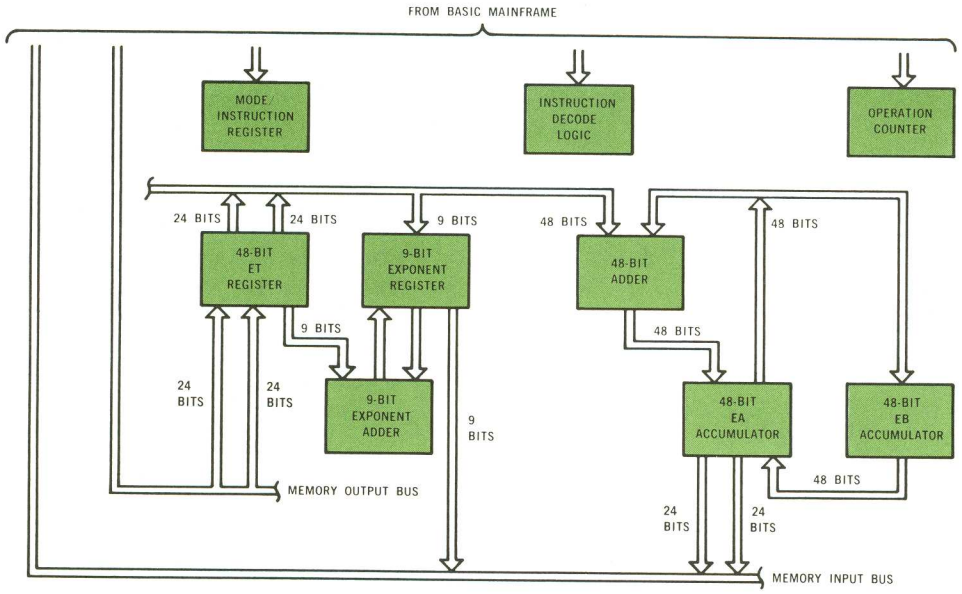
SEL 840A WORD FORMAT



EAU

The SEL 840A is the only computer in its size class that offers an independent, concurrent, second arithmetic unit. This optional extended arithmetic unit (EAU) is supplied with a complete set of twenty-two additional hardware commands. As an example of the concurrency available, the main frame is released to the next program instruction after the first 5.25 microseconds of the EAU double precision multiply command. The remainder of the 52.5 microsecond multiply time is performed concurrently with the main frame. The EAU can operate in single precision or double precision fixed point and in normalized or unnormalized floating point modes. The second word of double precision operands is fetched from (or stored in) core automatically.

EAU BLOCK DIAGRAM



EAU INSTRUCTION LIST

The following instructions are added to the basic SEL 840A repertoire when the EAU option is exercized.

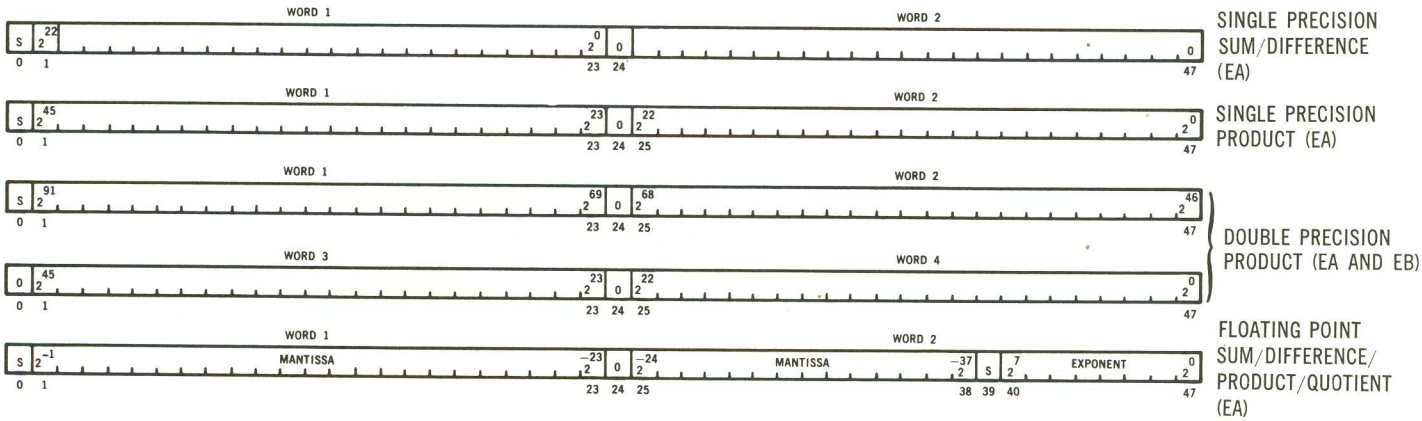
CLASS	CODE Mnemonic	TIME (Microseconds) FP	SP	DP	FUNCTION
EXTENDED ARITHMETIC UNIT (EAU)	ESP′	1.75			Set single precision. (SP)
	EDP′	1.75			Set double precision. (DP)
	EFP′	1.75			Set floating point. (FP)
	EFU′	1.75			Set floating point unnormalized.
	EAD	$5.25+\frac{n}{2}+\frac{p}{2}$	3.5	5.25	Add
	ESU	$5.25+\frac{n}{2}+\frac{p}{2}$	3.5	5.25	Subtract
	EMU	$40.25+\frac{n}{2}$	26.25	52.5	Multiply
	EDV	$49+\frac{n}{2}$	29.75	57	Divide
	ELN	5.25	3.5	5.25	Load negative in A accumulator*
	ELO	5.25	3.5	5.25	Load A accumulator*
	EST	5.25	3.5	5.25	Store A accumulator*

CLASS	CODE Mnemonic	TIME (Microseconds)	FUNCTION
EXTENDED ARITHMETIC UNIT (EAU)	EPS′	1.75	Skip A accumulator* positive.
	ESN′	1.75	Skip A accumulator* negative.
	ESZ′	1.75	Skip A accumulator* zero.
	EAR′	1.75	Skip EAU ready.
	ENO′	$1.75+\frac{n}{2}$	Normalize A accumulator.*
	EAB′	1.75	Transfer A accumulator* to B accumulator.*
	EBA′	1.75	Transfer B accumulator′ to A accumulator.*
	EIA′	1.75	Interchange A and B accumulators.*
	ELL	3.5	Load least significant half of A accumulator.*
	ESL	3.5	Store least significant half of A accumulator′.*
	ESR′	1.75	Extended Skip If Ready

′Augmented Instructions
*A and B accumulator in EAU are not the same as those in main frame and are both 48 bit registers.

n=No. of shifts to renormalize
p=No. of shifts to align exponents

TYPICAL EAU DATA FORMATS



SEL 840A SOFTWARE PACKAGE

The SEL 840A is delivered with an unusually powerful software package for a machine of its size. These programs are extremely valuable aids to the efficient use of the SEL 840A hardware. The software package includes a mnemonic assembler, compiler, a complete subroutine library, utility routines, maintenance and program debugging routines.

FORTRAN IV

The SEL 840A FORTRAN IV will allow — in addition to all the capabilities of FORTRAN II — double precision real, complex, logical, and Hollerith data type representation. Mixed mode expressions of data types are allowable and present an unusually simple method of rapidly obtaining an operating scientific program without undue attention to data representation. Mixed FORTRAN IV and assembly language statement capability is a vital feature of interest to the programmer faced with a requirement to program for real time operation. A real time version is provided which includes dynamic storage allocation and a recursive subroutine library. Only the basic 840A with 8K storage is required for the FORTRAN IV system. The SEL FORTRAN IV meets the standards of the ASA Full FORTRAN IV.

MNEMBLER

The SEL 840A MNEmonic asseMBLER is a translation program that allows machine language coding in easily written mnemonic operation codes. It also allows symbolic representation of core locations and provides many programmer conveniences, such as number base translation. Two modes are provided —a fast one-pass mnembler for speed limited I/O hardware configurations, and a two-pass mnembler that produces more compact object tapes.

LIBRARY

The SEL 840A library includes a comprehensive set of subroutines for use by the programmer. The Fortran IV set is included and is callable by both the Fortran IV compiler and mnembler. Routines include sine, cosine, arctan, square root, exponential, log, number base conversion, and many others.

UTILITY ROUTINES

The utility routines include an efficient tape editor, an on-line dynamic de-bug, dumps, listings, conversion programs, and others.

MAINTENANCE ROUTINES

The standard SEL 840A maintenance routines allow checkout of all 840A hardware.

SEL 840A INSTRUCTION LIST

The SEL 840A is equipped with a powerful repertoire of direct address and augmented instructions. These instructions, including two 3-way branch/skip instructions, are coupled with hardware indexing and indirect address chaining to provide maximum program flexibility and speed. An index operation does not increase instruction time, and an indirect operation requires only 1.75 additional microseconds. The optional extended arithmetic unit (EAU) allows concurrent arithmetic operations to take place. The EAU is completely independent of the main frame AU and can be set for single precision, double precision or floating point operation.

SEL 840A INSTRUCTION LIST

CLASS	CODE Mnemonic	TIME (Microseconds)	FUNCTION
ARITHMETIC	AMA	3.5	Add memory to A accumulator.
	SMA	3.5	Subtract memory from A accumulator.
	AAM	5.25	Add A accumulator to memory.
	MPY	10.5	Multiply.
	DIV	26.25	Divide.
	RNA	1.75	Round A accumulator.
	AMX	3.5	Add memory to designated index register
LOAD/STORE	LAA	3.5	Load A accumuiator.
	LBA	3.5	Load B accumulator.
	LIX	3.5	Load index register.
	STA	3.5	Store A accumulator.
	STB	3.5	Store B accumulator.
	STI	3.5	Store index register.
	LCS	1.75	Load control switches.
BRANCH/ SKIP	BRU	1.75	Unconditional branch.
	SPB	3.5	Store place and branch.
	PIR	3.5	Priority interrupt return.
	IIB	1.75	Increment index and branch.
	BAZ	1.75	Branch A accumulator zero.
	BAP	1.75	Branch A accumulator positive.
	BAN	1.75	Branch A accumulator negative.
	SMP	3.5	Skip memory positive.
	CMA	5.25	Compare memory and A accumulator (3 way).
	BOF	1.75	Branch on overflow.
	SNS'	1.75	Skip no signal.
	IMS	5.25	Increment memory and skip.
	SAS'	1.75	Skip on A accumulator sign (3 way).
SHIFT	RSA'	Time varies with no. of shifts.	Right shift A accumulator.
	LSA'		Left shift A accumulator.
	FRA'		Right shift A and B accumulator.
	RSL'	Shifts Time	Right logical shift A accumulator.
	FRL'	1- 4 3.5	Logical rotate A and B accumulator.
		5- 8 5.25	
	LSL'	9-12 7.0	Left logical shift A accumulator.
	FLA'	17-20 10.5	Left shift A and B accumulator.

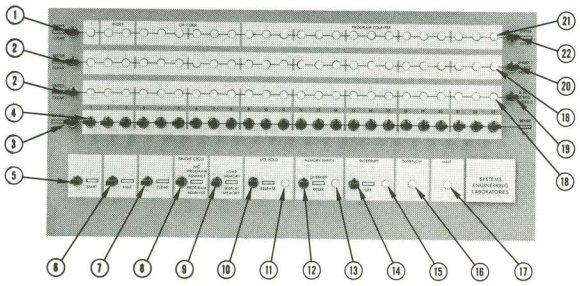
CLASS	CODE Mnemonic	TIME (Microseconds)	FUNCTION
SHIFT		Time varies with no. of shifts.	
		Shifts Time	
	FLL'	21-23 12.25	Logical left shift A and B accumulator.
	NOR	3 Shifts/ Cycle 1.75	Normalize
LOGICAL	MAA	3.5	Memory AND A accumulator.
	MOA	3.5	Memory OR A accumulator.
	NEG	1.75	Negate A accumulator.
	MEA	3.5	Memory EXCLUSIVE OR A accumulator.
	CNS	1.75	Convert number system.
	ASC'	1.75	Complement A accumulator sign.
CONTROL	EXU	1.75+	Execute.
	HLT'	1.75	Halt.
	NOP'	1.75	No operation.
	PIE'	1.75	Priority interrupt enable.
	PID'	1.75	Priority interrupt disable.
REGISTER CHANGE	CLA'	1.75	Clear A accumulator.
	TAB'	1.75	Transfer A accumulator to B accumulator.
	IAB'	1.75	Interchange A and B accumulator.
	TBI'	1.75	Transfer B accumulator to index register.
	IAM'	5.25	Interchange A accumulator and memory.
	TBA'	1.75	Transfer B accumulator to A accumulator.
	CSB'	1.75	B accumulator sign to carry and set B sign to plus.
INPUT/ OUTPUT	AOP	5.25	A accumulator output
	AIP	5.25	A accumulator input
	MOP	5.25	Memory output
	MIP	5.25	Memory input
	CEU	5.25	Command external unit
	TEU	5.25	Test external unit

'Augmented Instructions

OPERATOR'S CONSOLE

The operator's console is unusually complete with immediate selectable display of any register. Provision to enter manual data into any register or core location is standard. The SEL 840A is the only machine in its size or price class with a hardware program stop available at the console. The entire console is designed for maximum operator/machine communication.

SEL 840A CONTROL PANEL



1. Raised to transfer bits 0 - 8 of the T register to the instruction register containing the operation code and address modifiers.
   Depressed to clear the instruction register.
2. Raised to transfer the contents of the T register to the selected register.
   Upper switch is depressed to clear the selected register.
   Lower switch depressed to clear T register.
3. Raised to connect switches 0 - 23 as console SENSE switches.
   Depressed to connect switches 9 - 23 as program HALT switches. (Computer halts when the program count equals selected value.)
4. Switches 0 - 23 are raised (lock) to function as SENSE or HALT switches and depressed to enter ONE bits into the T register.
5. Depressed to start computer operation.
6. Depressed to halt computer operation.
7. Depressed to clear all major registers and control latches.
8. Raised to repeat current instruction. Does not advance program counter.
   Depressed to execute single instruction in normal sequence and advances program counter.
9. Raised to enable SINGLE CYCLE switch to load contents of T register into memory.
   Depressed to enable SINGLE CYCLE switch to transfer contents of memory address to T register.
10. Depressed to release I/O wait and allow computer to resume.
11. Lights to indicate a wait for I/O function.
12. Raised to allow computer operation in the event of a memory parity error (lock).
    Centered to halt computer operation when memory parity error is detected.
    Depressed to reset the parity error latch.
13. Lights to indicate the detection of a memory parity error.
14. Depressed to inhibit operation of priority interrupts (lock).
15. Lights to indicate a priority interrupt.
16. Lights to indicate an arithmetic overflow condition.
17. Lights to indicate a program halt.
18. Indicators display the contents of the selected register.
19. Raised to gate the contents of the T register to the B accumulator and to display the contents of B accumulator register.
    Centered to display the contents of the T register.
    Depressed to gate the contents of the T register to Index Register 3 and to display the contents of index 3 register.
20. Raised to gate the contents of the T register and clear inputs to Index Register 1 and to display the contents of index 1 register.
    Centered to gate the contents of the T Register and clear inputs to the A accumulator and to display the contents of A accumulator register.
    Depressed to gate the contents of the T register and clear inputs to Index Register 2 and to display the contents of index 2 register.
21. Display the contents of the program counter.
22. Raised to enter bits 9 - 23 of the T register into the program counter.
    Depressed to clear the program counter.

Notes: 1. Only the SENSE, HALT and display selection switches are active while the computer is operating.
2. Switches 3, 9, 21 and 22 lock in all positions.

MAINTENANCE EFFICIENCY UNSURPASSED

SEL 840A MAIN FRAME

Sel 840A Main Frame opens in rear, and "pages" containing micrologic modules swing out exposing all computer circuitry for maintenance

PAGE

Pages contain circuit modules. Each module has test points for troubleshooting ease. Connectors are Elco Varicon. Wire Wrap used exclusively for highest reliability and easiest field service.

SEL MICROLOGIC MODULE

Silicon monolithic integrated digital circuits exclusively. TO-5 cans allow same serviceability as discrete component circuits, but give latest state of the art speed and reliability. Components mounted on one side only.

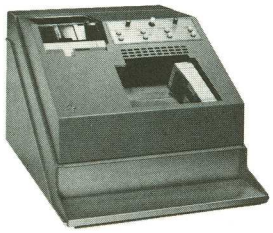
SEL SERVICES FOR 840A USERS

- Two Week Programming and 4 Week Maintenance Courses Beginning Once Each Quarter at Fort Lauderdale.
- On Call Service Contracts.
- Field Resident Service/Operation contracts.
- Programming Services.

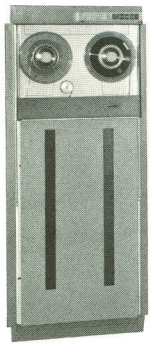
SEL 800 SERIES PERIPHERAL EQUIPMENT

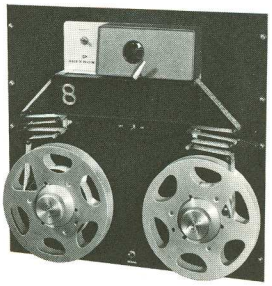
The SEL 840A computer has a wide range of available input/output equipment. Each peripheral device has its own control unit which contains a word or character buffer as required. Up to 64 input units plus 64 output units may be connected to the Unit I/O control or to fully buffered channels.

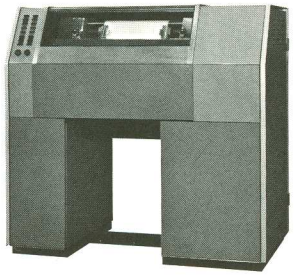
SEL 840A PERIPHERAL EQUIPMENT

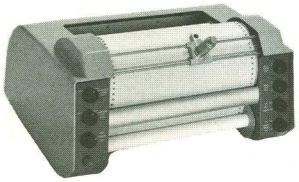


Catalog No.	Description	
80-400	**— CARD READERS AND PUNCHES**	
80-410	— Medium Speed Reader	100 Cards/Minute
80-420	— High Speed Reader	1000 Cards/Minute
80-440	— Punch	100 Cards/Minute
80-500	**— PAPER TAPE READERS AND PUNCHES**	
80-710	— ASR-33 Reader/Punch (Supplied with Main Frame)	10 Characters/Second
80-510	— High Speed Photoelectric Reader	300 Characters/Second
80-520	— High Speed Punch	110 Characters/Second
80-600	**— MAGNETIC TAPE SYSTEMS**	
80-610	— Tape Control Unit—Handles up to 8 ea. 80-615 Magnetic Tape Units	
80-615	— Magnetic Tape Unit, 200, 556 and 800 bits at up to 150 ips.	
80-700	**— TYPEWRITERS AND LINE PRINTERS**	
80-710	— ASR-33 (Supplied with Main Frame)	10 Characters/Second
80-715	— 35-AR	10 Characters/Second
80-716	— 35-AN	10 Characters/Second
80-730	— Low Speed	300 Lines/Minute } 120 Columns
80-732	— High Speed	1000 Lines/Minute } 120 Columns
80-800	**— PLOTTERS AND DISPLAYS**	
80-810	— Incremental Plotter	12 in. chart width } 300 Steps/Sec.
80-812	— Incremental Plotter	31 in. chart width } 300 Steps/Sec.
80-821	— 21" CRT Display	2048 Characters
80-806	— 6" CRT. Display	512 Characters
80-805	— High Resolution 5" CRT Display	4096 Characters
80-820	— Vector Generator	Used with 80-821 or 80-806 or 80-805
80-822	— Character Generator	
80-824	— Refresh Memory	
80-830	— Light Pen for CRT Displays	
80-900	**— SPECIAL INTERFACES**	
80-910	— SEL 600 Data Acquisition Systems	
80-920	— Direct Digital Control Outputs	
80-930	— Custom Interfaces	









SEL®
SYSTEMS ENGINEERING LABORATORIES, INCORPORATED
P. O. BOX 9148 • FORT LAUDERDALE, FLORIDA 33310 • AREA CODE 305 • 587-2900

10400 Connecticut Avenue
Kensington, Maryland 20795
PH. 301-946-7100
TWX. 301-949-6793

P. O. Box 2584
Pomona, California 91767
PH. 714-623-5235
TWX. 714-569-3255

P. O. Box 672
Framingham, Massachusetts 01701
PH. 617-879-0080

885 N. San Antonio Road
Los Altos, California 94023
PH. 415-941-1185
TWX. 415-949-7900

P.O. Box 1566
Huntsville, Alabama 35805
PH. 205-539-2181
TWX. 205-533-1276

APPENDIX F

LIST OF SEL 840A INSTRUCTIONS

MNE-MONIC	OP CODE	FUNCTION	PAGE
AAM	31	Add (A) to (M)	2-14
AIP	172	(Unit) to A	2-55
AMA	05	Add (M) to (A)	2-13
AMX	61	Add (M) to (X)	2-14
AOP	170	(A) to Unit	2-54
ASC	00-20	Comp. A sign	2-26
BAN	23	Branch if (A) neg.	2-22
BAP	24	Branch if (A) pos.	2-22
BAZ	22	Branch if (A)=0	2-21
BOF	25	Branch on O'FLOW	2-23
BRU	11	Branch to M	2-18
CEU	130	Command Ext. Unit	2-52
CLA	00-03	Clear (A) to 0	2-31
CMA	15	Compare (A) and (M)	2-21
CNS	20	Convert No. System	2-26
CSB	00-07	Copy B sign	2-33
DIV	10	Divide	2-16
EAB	21-03	(EA) to EB	2-62
EAD	45	EAU add	2-65
EBA	21-02	(EB) to EA	2-61
EDP	21-12	EAU D. P. mode	2-59
EDV	50	EAU Divide	2-68
EFP	21-14	EAU F. P. mode	2-60
EFU	21-11	Un-normalize F. P.	2-58
EIA	21-01	(EA) to EB, (EB) to EA	2-61
ELL	54	Load LSH of (EA)	2-72
ELN	51	Load (M) in EA	2-69
ELO	52	Load (M) in EA	2-70
EMU	47	EAU Multiply	2-67
ENO	21-00	EAU Normalize	2-60
EPS	21-06	Skip if (EA) pos.	2-63
ESL	55	Store LSH of (EA)	2-72
ESN	21-07	Skip if (EA) neg.	2-64
ESO	21-10	Skip on EAU O'FLOW	2-64
ESP	21-13	EAU S. P. mode	2-59
ESR	00-23	Skip if EAU not ready	2-62
EST	53	Store (EA)	2-71
ESU	46	EAU Subtract	2-66
ESZ	21-05	Skip if (EA)=0	2-63
EXU	16	Execute (M)	2-44
FLA	00-13	Full Left Shift, Arith.	2-38
FLL	00-17	Full Left Shift, Log.	2-42
FRA	00-12	Full Right Shift, Arith.	2-37
FRL	00-14	Full Left Rotate, Log.	2-39
HLT	00-00	Halt	2-45
IAB	00-06	(A) to B; (B) to A	2-32
IAM	44	(A) to M; (M) to A	2-12
IIB	34	(X)+1, Branch if not 0	2-23
IMS	14	(M)+1;Skip if 0	2-20
LAA	01	(M) to A	2-8
LBA	02	(M) to B	2-9
LCS	57	Switches to A	2-10
LIX	32	(M) to X	2-9
LSA	00-11	Left Shift A, Arith.	2-36
LSL	00-16	Left Shift A, Log.	2-41
MAA	27	(M) AND (A)	2-28
MEA	26	(M) Exclusive OR (A)	2-27
MIP	176	(Unit) to M	2-57
MOA	30	(M) OR (A)	2-29
MOP	174	(M) to Unit	2-56
MPY	07	Multiply	2-15
NEG	56	2's comp. (A)	2-25
NOP	00-22	No operation	2-45
NOR	00-32	Normalize (A) and (B)	2-43
PID	0.43	P.I. Disable	2-46
PIE	1.43	P.I. Enable	2-46
PIR	36	P.I. Return	2-19
POF	63	Protect Bit Off	2-74
PON	62	Protect Bit On	2-73
RNA	60	Round (A) by (B)	2-17
RSA	00-10	Right shift A, Arith.	2-35
RSL	00-15	Right shift A, Log.	2-40
SAS	00-21	Skip on A sign	2-24
SMA	06	Subtract (M) from (A)	2-15
SMP	35	Skip if (M) pos.	2-24
SNS	134	Sense No. Switch	2-20
SPB	12	Store Place & Branch	2-19
STA	03	(A) to M	2-10
STB	04	(B) to M	2-11
STI	33	(X) to M	2-11
TAB	00-05	(A) to B	2-32
TAI	00-01	(A) to X	2-30
TBA	00-04	(B) to A	2-32
TBI	00-02	(B) to X	2-31
TEU	132	Test Ext. Unit	2-53