SCD - DHV11/16

16-Line Asynchronous Multiplexer Manual

Sigma Information Systems

SCD - DHV11/16

16-Line Asynchronous Multiplexer Manual

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Section 1 - General Information

1 1 INTRODUCTION

This manual provides general installation and programming information for the SCD-DHV11/16 16-line asynchronous communication multiplexer manufactured by Sigma Information Systems, Anaheim, California. The material in this manual is arranged into the following sections.

Section 1 - GENERAL INFORMATION. This section provides a general description of the SCD-DHV11/16. Specifications are included.

Section 2 - INSTALLATION. This section describes the procedures for setting up and installing the 16-line multiplexer. Device address and vector interrupt switch selections are included, along with cabling to I/O devices.

Section 3 - PROGRAMMING CONSIDERATIONS. This sections contains a detailed description of the SCD-DHV11/16 registers. Diagnostic testing is included

APPENDICES. The appendices contains Q bus signals and a complete list of switch configurations for the device address and the vector interrupts.

1 2 GENERAL DESCRIPTION

The SCD-DHV11/16 is a 16-line asynchronous communication multiplexer. Sigma's dual-wide module is addressed as two separate 8-line devices that emulate two of DEC's DHV11 quad-wide boards. The SCD-DHV11/16 is software compatible with operating systems and diagnostics designed for the DEC* module All lines are compatible with EIA RS-232-C and CCITT V 24 standard (data leads only).

Each communication line is independently programmable for word format and hardware character echo. Each line is also independently programmable for split transmit and receive baud rates up to 38 4K baud and for full or half duplex or auto echo operation.

Optional 19" rackmount communication panels are available for convenient cabling to user I/O devices One panel contains 16 subminiature D-type RS-232-C connectors The other panel contains 16 RJ11 connectors with DEC's* H3173-A layout.

1 3 FEATURES

- 16 asynchronous serial lines on one dual wide module.
- Emulates two of DEC's DHV11s without requiring patches when interfacing with DEC LSI-11 and MicroVAX CPUs.
- Compatible with EIA RS-232-C and CCITT V 24
- Programmable parameters individually set for each channel: baud rate word format, and character echo.
- Two contiguous switch selectable device addresses for lines 0-7 and lines 8-15.
- Optional rackmount panels available for convenient connection to I/O devices
- Two 256 character buffers for received characters.
- DMA for transmitted data
- Hardware or program-controlled break generation.

*DEC and Q bus are registered trademarks of Digital Equipment Corporation

1.4 OPTIONAL DISTRIBUTION PANELS

Two optional 19" rackmount brackets are available for convenient cabling to user's external I/O devices.

The rackmount bracket shown in Figure 1-1 accepts one or two optional distribution panels. Each distribution panel distributes signals from each SCD-DHV11/16 line to I/O connectors. The 16 connectors can be either subminiature DB9 connectors or RJ connectors.

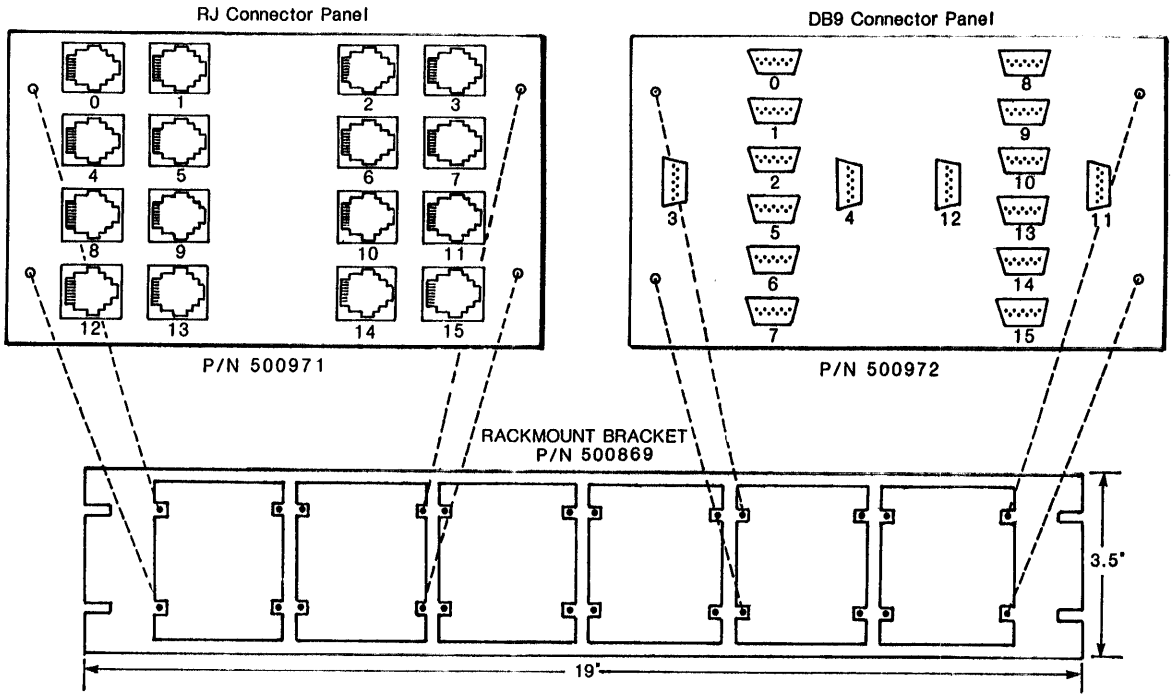


FIGURE 1-1: 3.5" DISTRIBUTION PANEL HARDWARE

The rackmount bracket shown in Figure 1-2 accepts an optional distribution panel that distributes signals from each SCD-DHV11/16 line to DB25 I/O connectors.

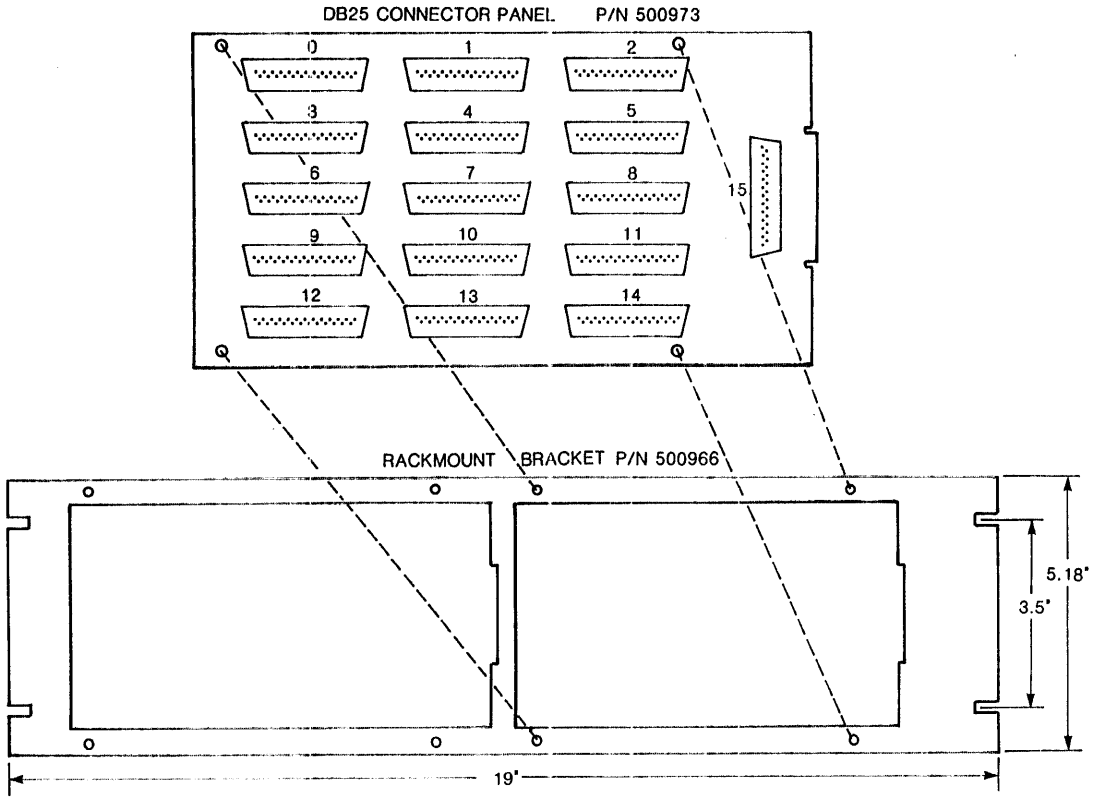


FIGURE 1-2: 5.18" DISTRIBUTION PANEL HARDWARE

1.5 SPECIFICATIONS

Size:	Standard dual-wide Q bus module
Power Requirements:	+5V @ 3.5A +12V @ 200mA
Interface:	EIA RS-232-C and CCITT V.24 standard (data leads only)
Cables (Optional):	Ribbon cable terminated with 16 D-type RS-232-C connectors or to RJ11 connectors.
Distribution Panel:	Optional 19" rackmount distribution panel contains four B I/O panels that distribute each line to a subminiature D-type RS-232-C connector or, alternately, to RJ11 connectors.

Operating Modes:	Full duplex or half duplex
Baud Rates:	Each channel independently program controlled: 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 7200, 9600, 19.2K, and 38.4K baud.
Device Address:	Two contiguous addresses for lines 0-7 and lines 8-15 are switch selectable from 17760000 to 17770000
Vector Interrupt:	Two contiguous interrupts for lines 0-7 and lines 8-15 are switch selectable from 000 to 760
Data Format:	Asynchronous. Serial by bit. Each line individually program controlled.
Stop/Start bits:	One start and 1, 1-1/2 (5 level code only), or 2 stop bits.
Character Bits:	5, 6, 7 or 8
Parity:	Odd, Even, or None
Temperature:	
Operating:	0°C to 50°C
Storage:	-45°C to 85°C
Humidity:	0% to 95% noncondensing
Altitude:	
Operating:	0 ft. to 10,000 ft.
Storage:	0 ft. to 30,000 ft.

Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The SCD-DHV11/16 is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

2.2 FACTORY-SET SWITCHES

The SCD-DHV11/16 multiplexer is shipped configured with DEC standard address 160440 and vector interrupt 300. The location of the switches that determine these parameters is shown in Figure 2-1. Before installing modules, verify that the switches are set properly. The following sections describe the procedures to verify and/or reconfigure device address and vector interrupt.

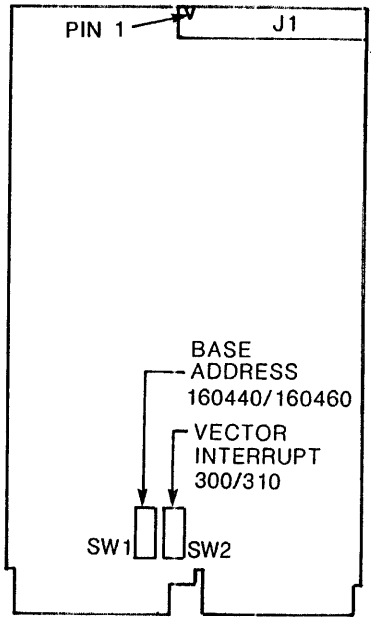


FIGURE 2-1: COMPONENT LOCATIONS

2.2.1 Device Address Selection

The device address for the SCD-DHV11/16 is set by switch SW1 shown in Figure 2-1. The address can range from 160000 to 177740. Figure 2-2 shows the relationship between the address bits and the switch positions.

The factory set address of 160440 is shown in Figure 2-2. A list of the complete address range with associated switch settings can be found in Appendix B.

OFF = 1, ON = 0																
ADDRESS BITS	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	1	1	1	SET BY SW1								0	0	0	0	0
SW1 POSITIONS				1 ON	2 ON	3 ON	4 ON	5 OFF	6 ON	7 ON	8 OFF					
BINARY ADDRESS	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0
OCTAL ADDRESS	1		6			0			4			4			0	

FIGURE 2-2: ADDRESS SELECTION

NOTE

The SCD-DHV11/16 can be considered as two of DEC's DHV11s. Lines 0 through 7 will have the device address selected by switch SW1. Lines 8 through 15 will have the selected device address +20 (octal).

2.2.2 Interrupt Vector Selection

The interrupt vector for the SCD-DHV11/16 is set by switch SW2 shown in Figure 2-1. The vector interrupt can range from 000 to 770. Figure 2-3 shows the relationship between the interrupt vector bits and the switch positions.

The factory set interrupt of 300 is shown in Figure 2-3. A list of the complete interrupt range with associated switch settings can be found in Appendix C.

----------OFF = 0, ON = 1----------

VECTOR BITS	08	07	06	05	04	03	02	01	00
	------SET BY SW2------						0	0	0
SW2 POSITIONS	3	4	5	6	7	8			
	OFF	ON	ON	OFF	OFF	OFF			
BINARY INTERRUPT	0	1	1	0	0	0	0	0	0
OCTAL INTERRUPT	---------			---------			---------		
	3			0			0		

FIGURE 2-3: INTERRUPT VECTOR SELECTION

NOTE

Lines 0 through 7 will have the interrupt vector selected by SW2. Lines 8 through 15 will have that vector +10 (octal).

2.3 MODULE INSTALLATION AND CABLING

The SCD-DHV11/16 plugs directly into an LSI-11 backplane dual slot (see Figure 2-2). The J1 connector provides the interface signals for the I/O panels described in Figure 1-1. Pin assignments for the 50-pin connector are listed in Table 2-1.

LINE NUMBER	----SIGNALS---- RECEIVE J1 PIN NUMBERS	TRANSMIT
0	2	12
1	9	5
2	21	17
3	15	23
4	26	30
5	33	35
7	38	42
7	45	48
8	3	11
9	8	6
10	20	18
11	14	24
12	27	29
13	32	36
14	39	41
15	44	47

Pins not listed are ground

TABLE 2-1: J1 CONNECTOR PIN ASSIGNMENTS

The cables from J1 plug into the PCBA of the I/O connector panels. The PCBA distributes J1 signals to each of the I/O lines specified on the connector side of the panels described in Figures 1-1 and 1-2.

2.4 TESTING

Diagnostic testing can be run using DEC's VDHA??, VDHB??, and VDHC?? functional verification tests. Only parts of these tests are used for the SCD-DHV11/16.

VDHA??	*TESTS 1-27
VDHB??	TESTS 1-15 AND 24-26
VDHC??	TESTS 1-4

Use the following procedure to run the functional verification tests.

1. Run the tests in the internal loopback mode (staggered loopback connector not installed). Run the diagnostics for one error-free pass. Any fault message indicates a defective SCD-DHV11/16. The underlined parameters below are keyboard entries.

RUNNING VDHA??

(*Test 11 does not run on LSI-11/23 due to timing differences)

```
.RUN VDHA??                                        ;run VDHA test
VDHABO.BIC                                         ;system response
DR>START/FLAG:HOE<CR>                              ;Start tests 1 through 27
                                                   ;with Halt on Error (HOE) flag
   .                                                  .
   .                                                  .
   .                                                  .
CHANGE HW (L) ? Y<CR>                              ;Change hardware configuration
# UNITS (D) ? 2<CR>                                ;Specify two DHV11 emulation
UNIT 0                                             ;Specify SCD-DHV11/16 address
CSR ADDRESS: (0) 160460 ? 160440<CR>               ;for lines 0-7 (unit 0)
INTERRUPT VECTOR ADDRESS: (0) 300 ? Y<CR>          ;Specify vector interrupt
ACTIVE LINE BIT MAP: (0) 377 ? <CR>                ;
INTERRUPT LEVEL: (0) 4 ? 5<CR>                     ;Specify level 5

UNIT 1                                             ;Repeat for CSR address 160460,
                                                   ;interrupt vector 310 (unit 1
                                                   ;= lines 7-15)
CHANGE SW (L) ? N<CR>                              ;Test will begin.
   .
   .
   .
CTRL C                                             ;Terminate test with CTRL C.
```

2. To run the test in the staggered loopback mode requires removal of the 50-conductor cable from the SCD-DHV11/16 module. A staggered loopback connector, shown in Figure 2-4, is installed into the 50-pin connector on the module. The pin assignments for the staggered loopback connector are shown in Appendix D.

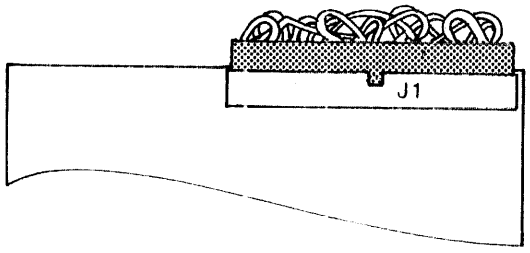


FIGURE 2-4: STAGGERED LOOPBACK CONNECTOR

3. Run the tests in the staggered loopback mode for two error-free passes. Any fault message indicates a defective SCD-DHV11/16 or cable. The underlined parameters below are keyboard entries.

RUNNING VDHB??

```
.RUN VDHB??                                    ;run VDHB test
VDHBCO.BIC                                     ;system response
DR>START/FLAG:HOE/TEST:1-15:24-26<CR>          ;Start tests 1-15 and 24-26
                                               ;with Halt on Error (HOE) flag
   .                                              .
   .                                              .
   .                                              .
CHANGE HW (L) ? Y<CR>                          ;Change hardware configuration
# UNITS (D) ? 2<CR>                           ;Specify two DHV11 emulation
UNIT 0                                         ;Specify SCD-DHV11/16 address
CSR ADDRESS: (0) 160460 ? 160440<CR>           ;for lines 0-7 (unit 0)
INTERRUPT VECTOR ADDRESS: (0) 300 ? Y<CR>      ;Specify vector interrupt
ACTIVE LINE BIT MAP: (0) 377 ? <CR>            ;
TYPE OF LOOPBACK (1 = INTERNAL, 2 =            ;Specify staggered loopback
H3277, 3 = H325: (0) 2<CR>                     ;test (H3277 installed)
INTERRUPT LEVEL: (0) 4 ? 5<CR>                 ;Specify level 5

UNIT 1                                         ;Repeat for CSR address 160460,
                                               ;interrupt vector 310 (unit 1
                                               ;= lines 7-15)
CHANGE SW (L) ? N<CR>                          ;Test will begin.
   .
   .
   .
CTRL C                                         ;Terminate test with CTRL C.
```

RUNNING VDHC??

```
.RUN VDHC??                                    ;run VDHC test
VDHCBO.BIC                                     ;system response
DR>START/FLAG:HOE/TEST:1-4<CR>                 ;Start tests 1 through 4
                                               ;with Halt on Error (HOE) flag
   .                                              .
   .                                              .
   .                                              .
CHANGE HW (L) ? Y<CR>                          ;Change hardware configuration
# UNITS (D) ? 2<CR>                            ;Specify two DHV11 emulation
UNIT 0                                         ;Specify SCD-DHV11/16 address
CSR ADDRESS: (0) 160460 ? 160440<CR>           ;for lines 0-7 (unit 0)
INTERRUPT VECTOR ADDRESS: (0) 300 ? Y<CR>      ;Specify vector interrupt
ACTIVE LINE BIT MAP: (0) 377 ? <CR>            ;
TYPE OF LOOPBACK (1 = INTERNAL, 2 =            ;Specify staggered loopback
H3277, 3 = H325, 4 = MODEM, 5 =                ;test (H3277 equivalent
KEYBOARD ECHO ): (0) 2<CR>                     ;installed)
INTERRUPT LEVEL: (0) 4 ? 5<CR>                 ;Specify level 5

UNIT 1                                         ;Repeat for CSR address 160460,
                                               ;interrupt vector 310 (unit 1
                                               ;= lines 7-15)
CHANGE SW (L) ? N<CR>                          ;Test will begin.
   .
   .
   .
CTRL C                                         ;Terminate test with CTRL C.
```

Notes

Section 3 - Programming Considerations

3.1 INTRODUCTION

There are two sets of registers for the SCD-DHV11/16. The registers listed below are associated with channels 0-7. A set of the same registers with "Base + 20 (octal) addresses is associated with channels 8-15. The term "Base" is the address selected by switch SW1 (Section 2.2.1).

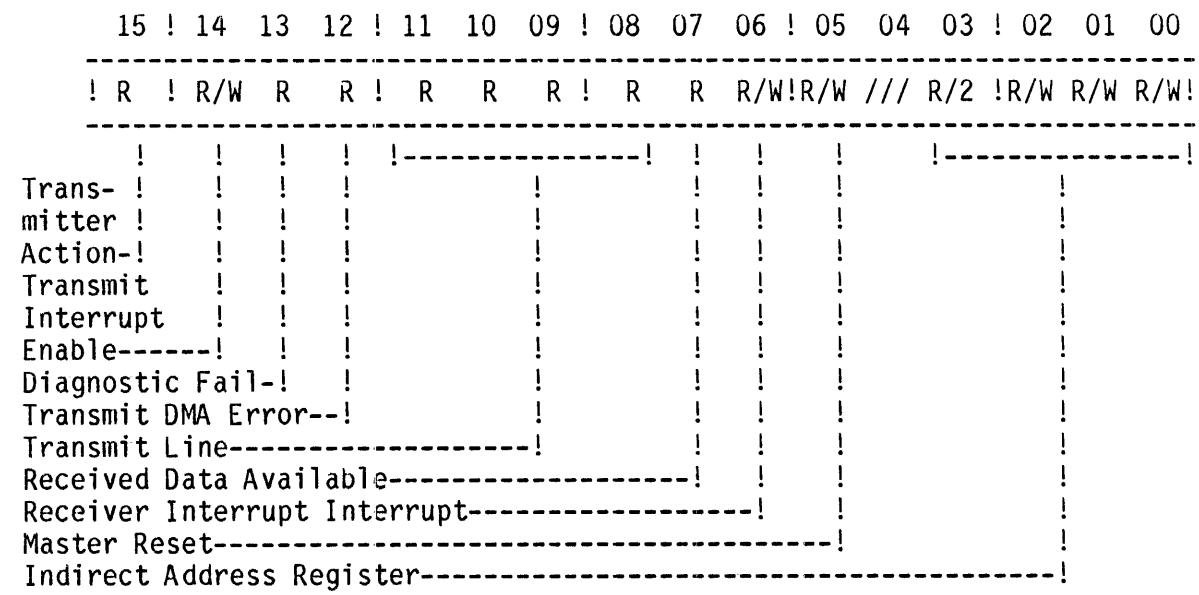
Control/Status Register	CSR	Base	Read/Write
Receive Buffer	RBUF	Base + 2	Read Only
Transmit Character	TXCHAR*	Base + 2	Write Only
Line Parameter Register	LPR*	Base + 4	Read/Write
Line Status	STAT*	Base + 6	Read Only
Line Control	LNCTRL*	Base + 10	Read/Write
Transmit Buffer Address 1	TBUFFAD1*	Base + 12	Read/Write
Transmit Buffer Address 2	TBUFFAD2*	Base + 14	Read/Write
Transmit Buffer Count	TBUFFCT*	Base + 16	Read/Write

*There are eight indirect address registers associated with each of these registers: one for each channel. When the indirect address registers are accessed, the address is indexed by the contents of CSR bits 03-00.

The SCD-DHV11/16 clears MASTER RESET when initialization and self-test are complete; the red LED is turned on and the module is then operational with the following default register parameters.

Send and receive 9600 bits/s	RX disable
Eight data bits	TX enabled
One stop bit	No break on line
No parity	DMA character counters zero
Parity odd	DMA start addresses zero
Auto-flow off	TX.DMA.START cleared
No loopback	TX.DMA.ABORT cleared.

3.2 CONTROL AND STATUS REGISTER (CSR)



BIT	MNEMONIC	DESCRIPTION
15	TX.ACTION	This bit is set by SCD-DHV11/16 when (1) the last character of a DMA buffer has left the DUART or (2) A DMA transfer has been aborted or terminated by the SCD-DHV11/16. Cleared by MASTER.RESET.
14	TXIE	When set, this bit allows the SCD-DHV11/16 to interrupt the host if CSR bit 15 becomes set. CLEARED BY BINIT (bus initialize), power up or down, but not by MASTER.RESET.
13	DIAG.FAIL	This bit is set when the internal diagnostics detects an error (LED off). Clear is indicated when LED is on.
12	TX.DMA.ERR	If this bit, along with TX.ACTION, is set, there is a memory parity error or else the channel indicated by CSR bits 11-08 has failed to transfer DMA data within the time allotted for the bus request to be acknowledged. TBUFFAD1 and TBUFFAD2 registers

contain the address of the memory location that could not be accessed. TBUFFCT will be cleared.

11-08 TX.LINE — If TX.ACTION is set, these its contain the binary number of the channel which has (1) completed a DMA block transfer, (2) accepted a single character for transmission, or (3) aborted a DMA block transfer.

If TX.DMA.ERR is also set, these bits contain the binary number of the channel that failed during a DMA transfer.

7 RX.DATA.AVAIL — When set, this bit indicates that a received character is available. This bit is cleared when the FIFO is empty. It is used to request and RX interrupt.

Set after MASTER.RESET because the FIFO contains diagnostic information.

6 RXIE — When set, this bit allows the SCD-DHV11/16 to interrupt the host when RX.DATA.AVAIL is set. An interrupt is generated if (1) RXIE is set and a character is placed into an empty FIFO and (2) the FIFO is not empty and RXIE is changed from 0 to 1. Cleared by BINIT, power up or down, but not by MASTER.RESET.

5 MASTER.RESET — Set by the host to reset SCD-DHV11/16. Cleared after self-test and initialization sequence.

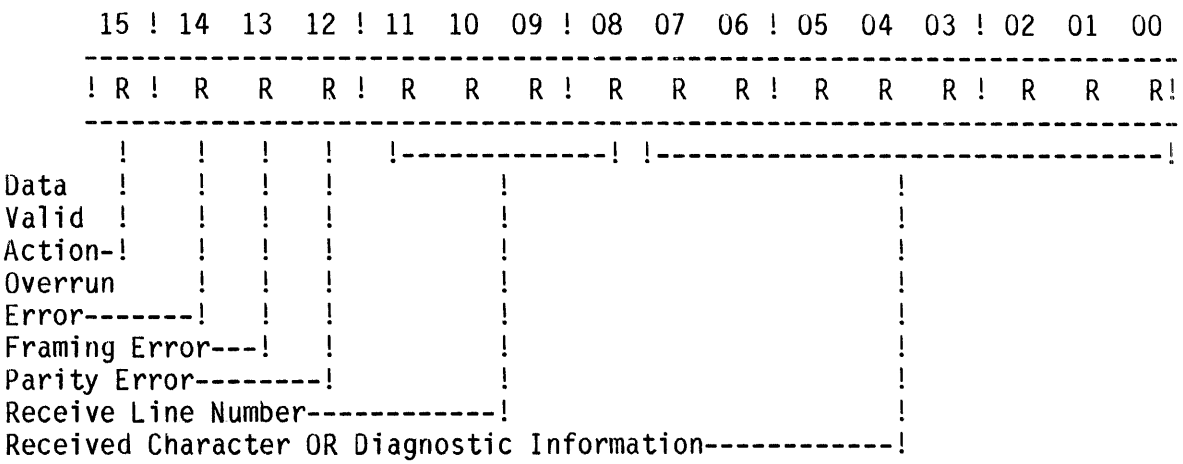
Set by BINIT (bus initialization) or by CPU setting CSR bit 5. The host should not write to this bit when it is already set.

03-00 IND.ADDR.REG — These bits specify the channel to be used for accessing a block of indexed register (Section 3.1). They form the binary number of the channel to be accessed.

--Bit-- 3 2 1 0	-----Channel----- (DHV A)	*(DHV B)
0 0 0 0	0	8
0 0 0 1	1	9
0 0 1 0	2	10
0 0 1 1	3	11
0 1 0 0	4	12
0 1 0 1	5	13
0 1 1 0	6	14
0 1 1 1	7	15

*DHV B Base Address = DHV A Base Address + 20_8

3.3 RECEIVE BUFFER (RBUF)



BIT	MNEMONIC	DESCRIPTION
15	DATA.VALID	Set if FIFO is not empty. Cleared by MASTER.RESET or by the FIFO becoming empty. Always set after a successful MASTER.RESET since self-test information is loaded into the FIFO.
14	OVERRUN.ERR	Set if one or more previous characters of the channel (bits 11-08) were lost due to a full FIFO or failure to service the UARTs (see RX.CHAR).

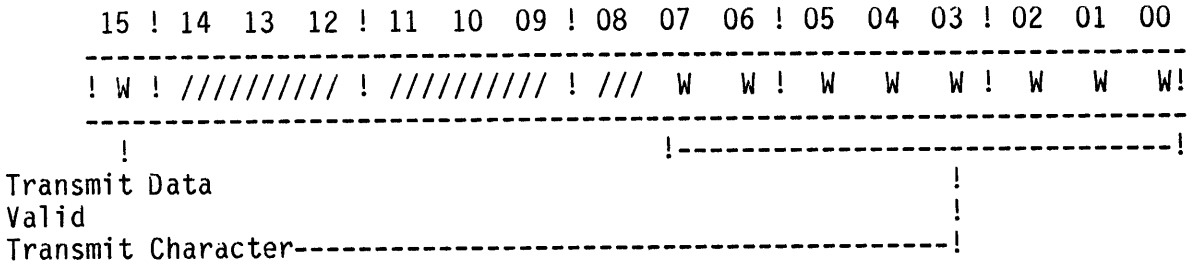
NOTE

The all 1s code for bits 14-12 indicates that diagnostic information is held in RBUF bits 07-00.

13	FRAME.ERR	Set if the first stop bit of the received character was not detected (see RX.CHAR).
12	PARITY.ERR	Set if a character has a parity error and if parity is enabled for the channel specified by bits 11-08 (see RX.CHAR).
11-08	RX.LINE	These bits contain the binary number of the channel on which the character of RBUF bits 07-00 was received. See CSR bits 03-00 for channel binary definitions.

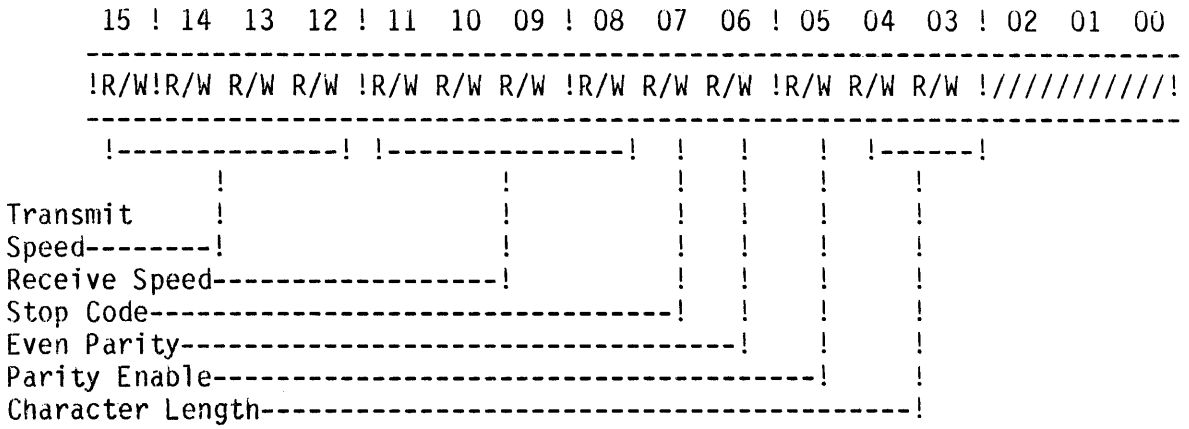
07-00	RX.CHAR	If RBUF bits 14-12 = 000, these bits contain the oldest character in the FIFO and the character is good. If RBUF bits 14-12 = 001, 010, or 011. the oldest character in the FIFO is bad. If RBUF bits 14-12 = 111, these bits contain diagnostic information. If there is an overrun condition, the data buffer for the selected channel will be cleared and data will be lost.

3 4 TRANSMIT CHARACTER REGISTER (TXCHAR)



BIT	MNEMONIC	DESCRIPTION
15	TX.DATA.VALID	When set, this bit instructs the SCD-DHV11/16 to transmit the character contained in bits 07-00. The bit is sensed by the SCD-DHV11/16, which then transfer the character, clears the bit, and sets TX.ACTION.
07-00	TX.CHAR	These bits contain the character to be transmitted. The LSB is bit 0 for 7-, 6-, or 5-bit characters. Unused bits must be 0.

3 5 LINE PARAMETER REGISTER (LPR)



BIT	MNEMONIC	DESCRIPTION
15-12	TX SPEED	Defines the transmit data rate as shown below. Notice that the rates are associated with either Group A or Group B.

Bit				----Baud Rate----	
15	14	13	12	Group A	Group B
0	0	0	0	50	
0	0	0	1		75
0	0	1	0	110	110
0	0	1	1	134.5	134.5
0	1	0	0		150
0	1	0	1	300	300
0	1	1	0	600	600
0	1	1	1	1200	1200
1	0	0	0		1800
1	0	0	1		2000
1	0	1	0	2400	2400
1	0	1	1	4800	4800
1	1	0	0	7200	
1	1	0	1	9600	
1	1	0	0		19200
1	1	1	1	38400	

NOTE The SCD-DHV11/16 uses dual-channel ICs. Channels 0-8, 1-9, 2-10, 3-11, 4-12, 5-13, 6-14, 7-15 are paired. Baud rates for paired channels (e.g., channel 1 and channel 9) must belong to the same group. It is the responsibility of the user to select transmit and receive data rates of the same group (A or B) for any pair of channels.

Set to 1101 (9600 baud) by MASTER RESET.

11-08 RX.SPEED — Defines the receive data rate the same as TX.SPEED. Restrictions are the same; paired channels must have baud rates within the same group.

Set to 1101 by MASTER.RESET.

07 STOP.CODE — Defines the length of the transmitted stop bit.

0 = 1 stop bit for 5-, 6-, 7-, or 8-bit characters
1 = 2 stop bits for 6-, 7-, or 8-bit characters OR 1.5 stop bits for 5-bit characters

Cleared by MASTER.RESET.

07 EVEN.PARITY — If LPR bit 5 is set, this bit defines the type of parity.

1 = even parity, 0 = odd parity

Cleared by MASTER.RESET.

05 PARITY.ENAB — Causes a parity bit to be generated on transmit, and checked and stripped on receive.

1 = parity enabled, 0 - parity disabled

Cleared by MASTER.RESET.

04-03 CHAR.LGTH — Defines the length of characters.

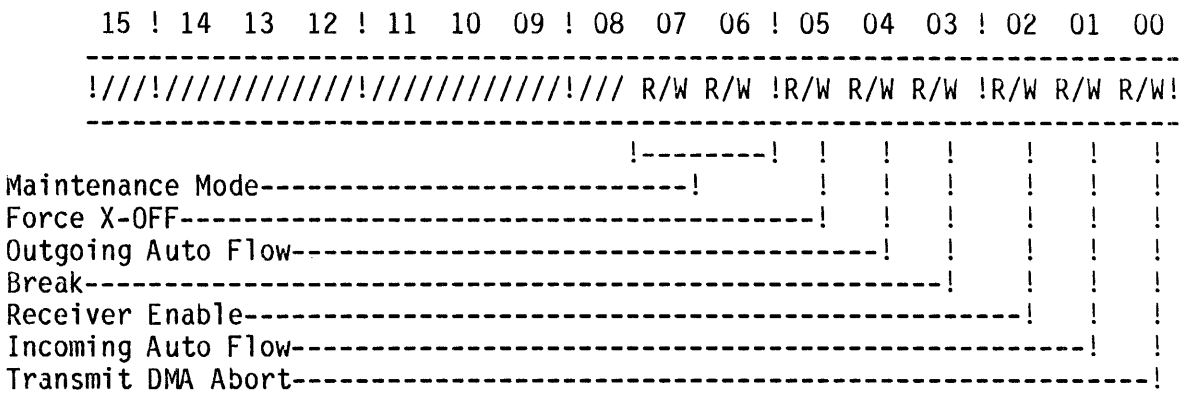
00 = 5 bits 10 = 7 bits
01 = 6 bits 11 = 8 bits

3.6 LINE STATUS REGISTER (LPR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Line Status Register is not used in the SCD-DHV11/16. All bits are read as 0s.

3.7 LINE CONTROL REGISTER (LNCTRL)



BIT	MNEMONIC	DESCRIPTION
07-06	MAINTENANCE	These bits can be written by the driver or test programs with codes are follows:

00 = Normal operation

01 = Automatic echo mode. Received data is retransmitted (regardless of TX.ENA state) at the receiver baud rate. Received characters are processed and placed in the received character FIFO. The SCD-DHV11/16 does not transmit any characters including internally generated flow-control characters). RX.ENA bit must be set when operating in this mode.

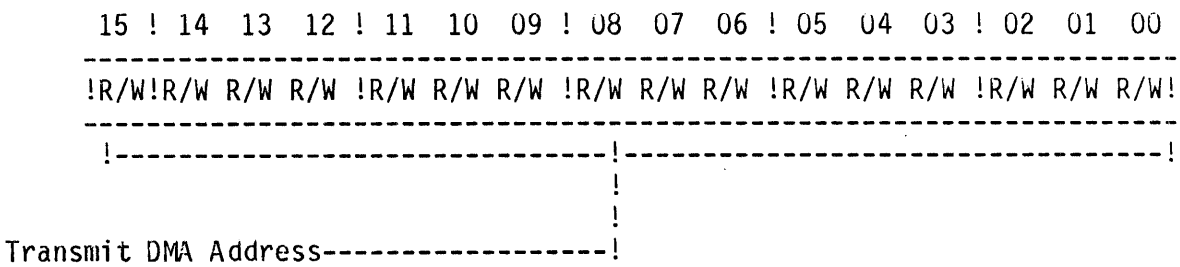
10 = Local loopback - The UART channel output is internally connected to the input. Normal received data is ignored and the transmit data line is held marking. Flow-control characters are looped back. Transmit baud rate is used both for transmission and reception. TX.ENA bit controls transmission.

11 = Remote loopback - Received data is retransmitted at the received baud rate. Data is not placed in the receiver FIFO. TX.ENA is ignored.

Cleared by MASTER.RESET.

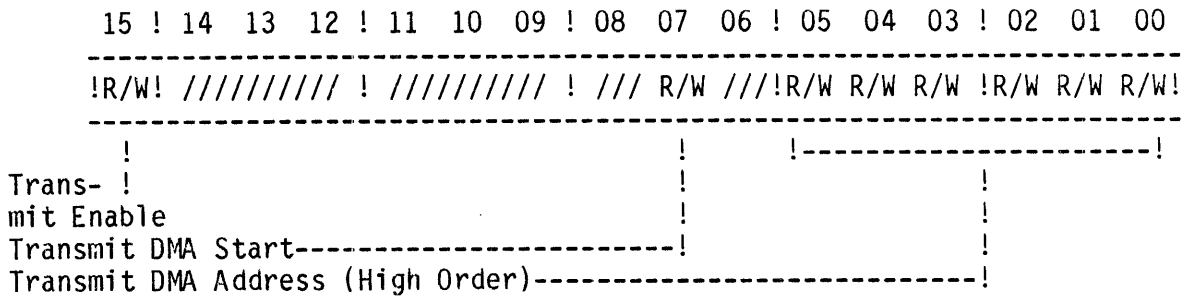
05	FORCE.XOFF	Set by the program to indicate that the selected channel is congested at the host (e.g., typeahead buffer full). The SCD-DHV11/16 sends an X-OFF code. Until the bit is reset, X-OFF is sent after every alternate character received on the channel. When the bit is reset, an X-ON is sent unless IAUTO is set and the FIFO is critical.
04	OAUTO	When set (if RX.ENA is also set) the SCD-DHV11/16 automatically responds to X-ON and X-OFF codes received from a channel. The SCD-DHV11/16 uses the TX.ENA bit in TBUFFAD2 to stop and start the flow. Cleared by MASTER.RESET.
03	BREAK	When set, this bit forces the transmitter of the selected channel to the spacing state. Transmission is restarted when the bit is cleared. Cleared by MASTER.RESET.
02	RX.ENA	If set, the receiver channel is enabled. Cleared by MASTER.RESET.
01	IAUTO	If set, the SCD-DHV11/16 controls incoming characters by transmitting X-ON and X-OFF codes. If the FIFO becomes congested, the SCD-DHV11/16 send X-OFF code to channels. X-ON is sent when the congestion is reduced. Cleared by MASTER.RESET. X-ON code = 21 (octal) = DC1 = CTRL Q X-OFF code = 23 (octal) = DC3 = CTRL S
00	TX.DMA.ABORT	Set by the driver program to halt transfer of DMA buffer. The transfer can be continued by clearing TX.DMA.ABORT and then setting TX.DMA.START. No characters are lost. TX.DMA.ABORT must be clear before setting TX.DMA.START or else the transfer is aborted before characters are transmitted. Cleared by MASTER.RESET.

3.8 TRANSMIT BUFFER ADDRESS REGISTER NUMBER 1 (TBUFFAD1)



BIT	MNEMONIC	DESCRIPTION
15-00	TBUFFAD	Contains the low byte of the Transmit DMA buffer address. Cleared by MASTER.RESET. See Section 3.9.

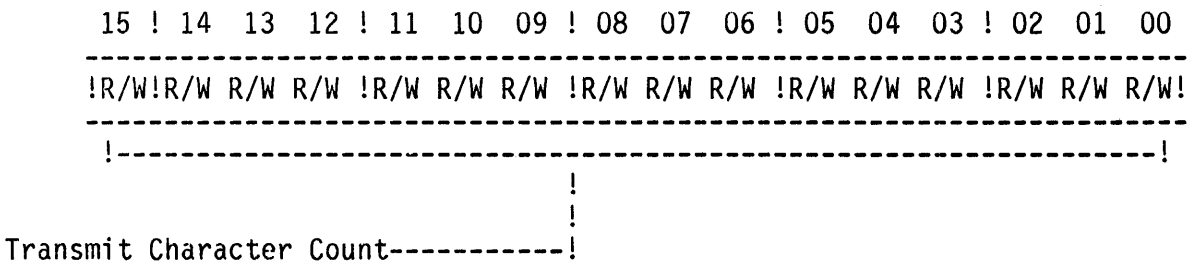
3.9 TRANSMIT BUFFER ADDRESS REGISTER NUMBER 2 (TBUFFAD2)



BIT	MNEMONIC	DESCRIPTION
15	TX.ENA	When cleared, the SCD-DHV11/16 will transmit only internally generated flow-control character. In the OAUTO mode, this bit is used by the SCD-DHV11/16 to control outgoing characters. Set by MASTER.RESET.
07	TX.DMA.START	Set by the host to start a DMA transfer. The SCD-DHV11 resets the bit before returning TX.ACTION. Cleared by MASTER.RESET. After setting this bit, the host must not write to TBUFFCT, TBUFFAD1 or TBUFFAD2 bits 07-00 until the TX.ACTION report is returned.

05-00	TBUFFAD	These bits contain the high order byte (bits 21-16) of the DMA address. Before a DMA transfer, TBUFFAD1 and the low byte of TBUFFAD2 are loaded with the start address of the DMA buffer. This address is not valid during a DMA transfer. When TX.ACTION is returned, the address is valid. Cleared by MASTER.RESET.

3.10 TRANSMIT DMA BUFFER COUNTER (TBUFFCT)



BIT	MNEMONIC	DESCRIPTION
15-00	TX.CHAR.CT	Loaded with the number of characters to be transferred by DMA. The number of character is specified as a 16-bit unsigned integer. After a DMA transfer is aborted, this location holds the number of characters left to be transferred.

Notes

PIN	SIGNAL	Micro VAX	LSI-11/73	LSI-11/23	PIN	SIGNAL	Micro VAX	LSI-11/73	LSI-11/23
AA1	BIRQ5L				AA2	+5V			
AB1	BIRQ6L				AB2	-12V	N/U	N/U	
AC1	BDAL16L				AC2	GND			
AD1	BDAL17L				AD2	+12V		N/U	
AE1	*SSPARE1	N/U	N/U	SINGLE STEP	AE2	BDOUTL			
AF1	*SSPARE2	SRUNL	SRUNL	SRUNL	AF2	BRPLYL			
AH1	*SSPARE3	N/U	N/U	SRUNL	AH2	BDINL			
AJ1	GND				AJ2	BSYNCL			
AK1	*MSPAREA	N/U	N/U	N/U	AK2	BWTBTL			
AL1	*MSPAREB	N/U	N/U	N/U	AL2	BIRQ4L			
AM1	GND				AM2	*BIAK1L		N/U	MMUSTRH
AN1	BDMRL				AN2	*BIAKOL		BIAKL	
AP1	BHALTL				AP2	BBS7L			
AR1	BREFL		N/U	N/U	AR2	*BDMG1L		N/U	UBMAAPL
AS1	+12VB	N/U	N/U		AS2	*BDMGOL			
AT1	GND				AT2	BINITL			
AU1	PSPARE1	N/U	N/U		AU2	BDALOL			
AV1	+5VB	N/U			AV2	BDAL1L			
BA1	BDCOKH				BA2	+5V			
BB1	BPOKH				BB2	-12V	N/U	N/U	
BC1	*SSPARE4	BDAL18L	BDAL18L	MMUDAL18H	BC2	GND			
BD1	*SSPARE5	BDAL19L	BDAL19L	MMUDAL19H	BD2	+12V		N/U	
BE1	*SSPARE6	BDAL20L	BDAL20L	MMUDAL20H	BE2	BDAL2L			
BF1	*SSPARE6	BDAL21L	BDAL21L	MMUDAL21H	BF2	BDAL3L			
BH1	*SSPARE8	N/U	N/U	CLKDISL	BH2	BDAL4L			
BJ1	GND				BJ2	BDAL5L			
BK1	*MSPAREB	N/U	N/U	N/U	BK2	BDAL6L			
BL1	*MSPAREB	N/U	N/U	N/U	BL2	BDAL7L			
BM1	GND				BM2	BDAL8L			
BN1	BSACKL				BN2	BDAL9L			
BP1	BIRQ7L				BP2	BDAL10L			
BR1	BEVNTL				BR2	BDAL11L			
BS1	PSPARE4	N/U	N/U	+12VB	BS2	BDAL12L			
BT1	GND				BT2	BDAL13L			
BU1	PSPARE2	N/U	N/U		BU2	BDAL14L			
BV1	+5V				BV2	BDAL15L			

*NOT BUSSED
N/U = NOT USED

NOTE

C-D slots for LSI-11/73 and LSI-11/23 are the same as A-B slots. Pin assignments for MicroVAX C-D slots are defined on the next page.

CA1	NOT USED	CA2	+5V	DA1	NOT USED	DA2	+5V
CB1	*MAA<0>L	CB2	MAA<9>L	DB1	*MAA<7>L	DB2	MAA<7>L
CC1	NOT USED	CC2	GND	DC1	NOT USED	DC2	GND
CD1	*RAS<5>H	CD2	RAS<1>H	DD1	*MAA<5>L	DD2	MAA<5>L
CE1	*BMCAS<0>H	CE2	BMCAS<0>L	DE1	*MAA<4>L	DE2	MAA<4>L
CF1	*RAS<1>H	CF2	NOT USED	DF1	*MAA<3>L	DF2	MAA<3>L
CH1	*BMCAS<1>H	CH2	BMCAS<1>H	DH1	*MAA<6>L	DH2	MAA<6>L
CJ1	*MSID<0>L	CJ2	MSID<2>L	DJ1	*MSID<2LL	DJ2	NOT USED
CK1	*MSWT<1>H	CK2	MSWT<1>H	DK1	*RAS<3>H	DK2	NOT USED
CL1	*RAS<4>H	CL2	RAS<0>H	DL1	*RAS<7>H	DL2	RAS<3>H
CM1	*MSID<1>L	CM2	MSID<3>L	DM1	*MSID<3>L	DM2	NOT USED
CN1	*MAA<1>L	CN2	MAA<1>L	DN1	*RAS<2LH	DN2	NOT USED
CP1	*MAA<2>L	CP2	MAA<2>L	DP1	*BMCAS<2>H	DP2	BMCAS<2>H
CR1	*MAA<0>L	CR2	MAA<0>L	DR1	*BMCAS<3>H	DR2	BMCAS<3>H
CS1	*MAA<8>L	CS2	MAA<8>L	DS1	*MSWT<2>H	DS2	MSWT<2>H
CT1	GND	CT2	MSID<4>L	DT1	GND	DT2	*MSID<4>L
CU1	*RAS<0>H	CU2	NOT USED	CU1	*RAS<6>H	DU2	RAS<2>H
CV1	NOT USED	CV2	NOT USED	DV1	NOT USED	DV2	NOT USED

*Used by MSA32 memory module. Not used by CPU.

MicroVAX C-D Slot Definitions

ADDRESS	SW1 1	2	3	4	5	6	7	8
	A12	A11	A10	A09	A08	A07	A06	A05
160000	ON	ON	ON	ON	ON	ON	ON	ON
160040	ON	ON	ON	ON	ON	ON	ON	OFF
160100	ON	ON	ON	ON	ON	ON	OFF	ON
160140	ON	ON	ON	ON	ON	ON	OFF	OFF
160200	ON	ON	ON	ON	ON	OFF	ON	ON
160240	ON	ON	ON	ON	ON	OFF	ON	OFF
160300	ON	ON	ON	ON	ON	OFF	OFF	ON
160340	ON	ON	ON	ON	ON	OFF	OFF	OFF
160400	ON	ON	ON	ON	OFF	ON	ON	ON
160440	ON	ON	ON	ON	OFF	ON	ON	OFF
160500	ON	ON	ON	ON	OFF	ON	OFF	ON
160540	ON	ON	ON	ON	OFF	ON	OFF	OFF
160600	ON	ON	ON	ON	OFF	OFF	ON	ON
160640	ON	ON	ON	ON	OFF	OFF	ON	OFF
160700	ON	ON	ON	ON	OFF	OFF	OFF	ON
160740	ON	ON	ON	ON	OFF	OFF	OFF	OFF
161000	ON	ON	ON	OFF	ON	ON	ON	ON
161040	ON	ON	ON	OFF	ON	ON	ON	OFF
161100	ON	ON	ON	OFF	ON	ON	OFF	ON
161140	ON	ON	ON	OFF	ON	ON	OFF	OFF
161200	ON	ON	ON	OFF	ON	OFF	ON	ON
161240	ON	ON	ON	OFF	ON	OFF	ON	OFF
161300	ON	ON	ON	OFF	ON	OFF	OFF	ON
161340	ON	ON	ON	OFF	ON	OFF	OFF	OFF
161400	ON	ON	ON	OFF	OFF	ON	ON	ON
161440	ON	ON	ON	OFF	OFF	ON	ON	OFF
161500	ON	ON	ON	OFF	OFF	ON	OFF	ON
161540	ON	ON	ON	OFF	OFF	ON	OFF	OFF
161600	ON	ON	ON	OFF	OFF	OFF	ON	ON
161640	ON	ON	ON	OFF	OFF	OFF	ON	OFF
161700	ON	ON	ON	OFF	OFF	OFF	OFF	ON
161740	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
162000	ON	ON	OFF	ON	ON	ON	ON	ON
162040	ON	ON	OFF	ON	ON	ON	ON	OFF
162100	ON	ON	OFF	ON	ON	ON	OFF	ON
162140	ON	ON	OFF	ON	ON	ON	OFF	OFF
162200	ON	ON	OFF	ON	ON	OFF	ON	ON
162240	ON	ON	OFF	ON	ON	OFF	ON	OFF
162300	ON	ON	OFF	ON	ON	OFF	OFF	ON
162340	ON	ON	OFF	ON	ON	OFF	OFF	OFF
162400	ON	ON	OFF	ON	OFF	ON	ON	ON
162440	ON	ON	OFF	ON	OFF	ON	ON	OFF
162500	ON	ON	OFF	ON	OFF	ON	OFF	ON
162540	ON	ON	OFF	ON	OFF	ON	OFF	OFF
162600	ON	ON	OFF	ON	OFF	OFF	ON	ON
162640	ON	ON	OFF	ON	OFF	OFF	ON	OFF
162700	ON	ON	OFF	ON	OFF	OFF	OFF	ON
162740	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
163000	ON	ON	OFF	OFF	ON	ON	ON	ON
163040	ON	ON	OFF	OFF	ON	ON	ON	OFF
163100	ON	ON	OFF	OFF	ON	ON	OFF	ON
163140	ON	ON	OFF	OFF	ON	ON	OFF	OFF
163200	ON	ON	OFF	OFF	ON	OFF	ON	ON
163240	ON	ON	OFF	OFF	ON	OFF	ON	OFF
163300	ON	ON	OFF	OFF	ON	OFF	OFF	ON
163340	ON	ON	OFF	OFF	ON	OFF	OFF	OFF
163400	ON	ON	OFF	OFF	OFF	ON	ON	ON
163440	ON	ON	OFF	OFF	OFF	ON	ON	OFF
163500	ON	ON	OFF	OFF	OFF	ON	OFF	ON
163540	ON	ON	OFF	OFF	OFF	ON	OFF	OFF
163600	ON	ON	OFF	OFF	OFF	OFF	ON	ON
163640	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
163700	ON	ON	OFF	OFF	OFF	OFF	OFF	ON
163740	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
164000	ON	OFF	ON	ON	ON	ON	ON	ON
164040	ON	OFF	ON	ON	ON	ON	ON	OFF
164100	ON	OFF	ON	ON	ON	ON	OFF	ON
164140	ON	OFF	ON	ON	ON	ON	OFF	OFF
164200	ON	OFF	ON	ON	ON	OFF	ON	ON
164240	ON	OFF	ON	ON	ON	OFF	ON	OFF
164300	ON	OFF	ON	ON	ON	OFF	OFF	ON
164340	ON	OFF	ON	ON	ON	OFF	OFF	OFF
164400	ON	OFF	ON	ON	OFF	ON	ON	ON
164440	ON	OFF	ON	ON	OFF	ON	ON	OFF
164500	ON	OFF	ON	ON	OFF	ON	OFF	ON
164540	ON	OFF	ON	ON	OFF	ON	OFF	OFF
164600	ON	OFF	ON	ON	OFF	OFF	ON	ON
164640	ON	OFF	ON	ON	OFF	OFF	ON	OFF
164700	ON	OFF	ON	ON	OFF	OFF	OFF	ON
164740	ON	OFF	ON	ON	OFF	OFF	OFF	OFF

ADDRESS	SW1 1	SW1 2	SW1 3	SW1 4	SW1 5	SW1 6	SW1 7	SW1 8
	A12	A11	A10	A09	A08	A07	A06	A05
165000	ON	OFF	ON	OFF	ON	ON	ON	ON
165040	ON	OFF	ON	OFF	ON	ON	ON	OFF
165100	ON	OFF	ON	OFF	ON	ON	OFF	ON
165140	ON	OFF	ON	OFF	ON	ON	OFF	OFF
165200	ON	OFF	ON	OFF	ON	OFF	ON	ON
165240	ON	OFF	ON	OFF	ON	OFF	ON	OFF
165300	ON	OFF	ON	OFF	ON	OFF	OFF	ON
165340	ON	OFF	ON	OFF	ON	OFF	OFF	OFF
165400	ON	OFF	ON	OFF	OFF	ON	ON	ON
165440	ON	OFF	ON	OFF	OFF	ON	ON	OFF
165500	ON	OFF	ON	OFF	OFF	ON	OFF	ON
165540	ON	OFF	ON	OFF	OFF	ON	OFF	OFF
165600	ON	OFF	ON	OFF	OFF	OFF	ON	ON
165640	ON	OFF	ON	OFF	OFF	OFF	ON	OFF
165700	ON	OFF	ON	OFF	OFF	OFF	OFF	ON
165740	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
166000	ON	OFF	OFF	ON	ON	ON	ON	ON
166040	ON	OFF	OFF	ON	ON	ON	ON	OFF
166100	ON	OFF	OFF	ON	ON	ON	OFF	ON
166140	ON	OFF	OFF	ON	ON	ON	OFF	OFF
166200	ON	OFF	OFF	ON	ON	OFF	ON	ON
166240	ON	OFF	OFF	ON	ON	OFF	ON	OFF
166300	ON	OFF	OFF	ON	ON	OFF	OFF	ON
166340	ON	OFF	OFF	ON	ON	OFF	OFF	OFF
166400	ON	OFF	OFF	ON	OFF	ON	ON	ON
166440	ON	OFF	OFF	ON	OFF	ON	ON	OFF
166500	ON	OFF	OFF	ON	OFF	ON	OFF	ON
166540	ON	OFF	OFF	ON	OFF	ON	OFF	OFF
166600	ON	OFF	OFF	ON	OFF	OFF	ON	ON
166640	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
166700	ON	OFF	OFF	ON	OFF	OFF	OFF	ON
166740	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
167000	ON	OFF	OFF	OFF	ON	ON	ON	ON
167040	ON	OFF	OFF	OFF	ON	ON	ON	OFF
167100	ON	OFF	OFF	OFF	ON	ON	OFF	ON
167140	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
167200	ON	OFF	OFF	OFF	ON	OFF	ON	ON
167240	ON	OFF	OFF	OFF	ON	OFF	ON	OFF
167300	ON	OFF	OFF	OFF	ON	OFF	OFF	ON
167340	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
167400	ON	OFF	OFF	OFF	OFF	ON	ON	ON
167440	ON	OFF	OFF	OFF	OFF	ON	ON	OFF
167500	ON	OFF	OFF	OFF	OFF	ON	OFF	ON
167540	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
167600	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
167640	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
167700	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON
167740	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
170000	OFF	ON	ON	ON	ON	ON	ON	ON
170040	OFF	ON	ON	ON	ON	ON	ON	OFF
170100	OFF	ON	ON	ON	ON	ON	OFF	ON
170140	OFF	ON	ON	ON	ON	ON	OFF	OFF
170200	OFF	ON	ON	ON	ON	OFF	ON	ON
170240	OFF	ON	ON	ON	ON	OFF	ON	OFF
170300	OFF	ON	ON	ON	ON	OFF	OFF	ON
170340	OFF	ON	ON	ON	ON	OFF	OFF	OFF
170400	OFF	ON	ON	ON	OFF	ON	ON	ON
170440	OFF	ON	ON	ON	OFF	ON	ON	OFF
170500	OFF	ON	ON	ON	OFF	ON	OFF	ON
170540	OFF	ON	ON	ON	OFF	ON	OFF	OFF
170600	OFF	ON	ON	ON	OFF	OFF	ON	ON
170640	OFF	ON	ON	ON	OFF	OFF	ON	OFF
170700	OFF	ON	ON	ON	OFF	OFF	OFF	ON
170740	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
171000	OFF	ON	ON	OFF	ON	ON	ON	ON
171040	OFF	ON	ON	OFF	ON	ON	ON	OFF
171100	OFF	ON	ON	OFF	ON	ON	OFF	ON
171140	OFF	ON	ON	OFF	ON	ON	OFF	OFF
171200	OFF	ON	ON	OFF	ON	OFF	ON	ON
171240	OFF	ON	ON	OFF	ON	OFF	ON	OFF
171300	OFF	ON	ON	OFF	ON	OFF	OFF	ON
171340	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
171400	OFF	ON	ON	OFF	OFF	ON	ON	ON
171440	OFF	ON	ON	OFF	OFF	ON	ON	OFF
171500	OFF	ON	ON	OFF	OFF	ON	OFF	ON
171540	OFF	ON	ON	OFF	OFF	ON	OFF	OFF
171600	OFF	ON	ON	OFF	OFF	OFF	ON	ON
171640	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
171700	OFF	ON	ON	OFF	OFF	OFF	OFF	ON
171740	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF

ADDRESS	------SW1 SWITCH POSITIONS----- 1	2	3	4	5	6	7	8
	----------ADDRESS BITS--------- A12	A11	A10	A09	A08	A07	A06	A05
172000	OFF	ON	OFF	ON	ON	ON	ON	ON
172040	OFF	ON	OFF	ON	ON	ON	ON	OFF
172100	OFF	ON	OFF	ON	ON	ON	OFF	ON
172140	OFF	ON	OFF	ON	ON	ON	OFF	OFF
172200	OFF	ON	OFF	ON	ON	OFF	ON	ON
172240	OFF	ON	OFF	ON	ON	OFF	ON	OFF
172300	OFF	ON	OFF	ON	ON	OFF	OFF	ON
172340	OFF	ON	OFF	ON	ON	OFF	OFF	OFF
172400	OFF	ON	OFF	ON	OFF	ON	ON	ON
172440	OFF	ON	OFF	ON	OFF	ON	ON	OFF
172500	OFF	ON	OFF	ON	OFF	ON	OFF	ON
172540	OFF	ON	OFF	ON	OFF	ON	OFF	OFF
172600	OFF	ON	OFF	ON	OFF	OFF	ON	ON
172640	OFF	ON	OFF	ON	OFF	OFF	ON	OFF
172700	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
172740	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
173000	OFF	ON	OFF	OFF	ON	ON	ON	ON
173040	OFF	ON	OFF	OFF	ON	ON	ON	OFF
173100	OFF	ON	OFF	OFF	ON	ON	OFF	ON
173140	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
173200	OFF	ON	OFF	OFF	ON	OFF	ON	ON
173240	OFF	ON	OFF	OFF	ON	OFF	ON	OFF
173300	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
173340	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
173400	OFF	ON	OFF	OFF	OFF	ON	ON	ON
173440	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
173500	OFF	ON	OFF	OFF	OFF	ON	OFF	ON
173540	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
173600	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
173640	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
173700	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON
173740	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
174000	OFF	OFF	ON	ON	ON	ON	ON	ON
174040	OFF	OFF	ON	ON	ON	ON	ON	OFF
174100	OFF	OFF	ON	ON	ON	ON	OFF	ON
174140	OFF	OFF	ON	ON	ON	ON	OFF	OFF
174200	OFF	OFF	ON	ON	ON	OFF	ON	ON
174240	OFF	OFF	ON	ON	ON	OFF	ON	OFF
174300	OFF	OFF	ON	ON	ON	OFF	OFF	ON
174340	OFF	OFF	ON	ON	ON	OFF	OFF	OFF

ADDRESS	------SW1 SWITCH POSITIONS----- 1	2	3	4	5	6	7	8
	----------ADDRESS BITS--------- A12	A11	A10	A09	A08	A07	A06	A05
174400	OFF	OFF	ON	ON	OFF	ON	ON	ON
174440	OFF	OFF	ON	ON	OFF	ON	ON	OFF
174500	OFF	OFF	ON	ON	OFF	ON	OFF	ON
174540	OFF	OFF	ON	ON	OFF	ON	OFF	OFF
174600	OFF	OFF	ON	ON	OFF	OFF	ON	ON
174640	OFF	OFF	ON	ON	OFF	OFF	ON	OFF
174700	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
174740	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
175000	OFF	OFF	ON	OFF	ON	ON	ON	ON
175040	OFF	OFF	ON	OFF	ON	ON	ON	OFF
175100	OFF	OFF	ON	OFF	ON	ON	OFF	ON
175140	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
175200	OFF	OFF	ON	OFF	ON	OFF	ON	ON
175240	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
175300	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
175340	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF
175400	OFF	OFF	ON	OFF	OFF	ON	ON	ON
175440	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
175500	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
175540	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
175600	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
175640	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
175700	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
175740	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
176000	OFF	OFF	OFF	ON	ON	ON	ON	ON
176040	OFF	OFF	OFF	ON	ON	ON	ON	OFF
176100	OFF	OFF	OFF	ON	ON	ON	OFF	ON
176140	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
176200	OFF	OFF	OFF	ON	ON	OFF	ON	ON
176240	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
176300	OFF	OFF	OFF	ON	ON	OFF	OFF	ON
176340	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
176400	OFF	OFF	OFF	ON	OFF	ON	ON	ON
176440	OFF	OFF	OFF	ON	OFF	ON	ON	OFF
176500	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
176540	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
176600	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
176640	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
176700	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
176740	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

ADDRESS	SW1 SWITCH POSITIONS 1	2	3	4	5	6	7	8
	ADDRESS BITS A12	A11	A10	A09	A08	A07	A06	A05
177000	OFF	OFF	OFF	OFF	ON	ON	ON	ON
177040	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
177100	OFF	OFF	OFF	OFF	ON	ON	OFF	ON
177140	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF
177200	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
177240	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
177300	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
177340	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

ADDRESS	SW1 SWITCH POSITIONS 1	2	3	4	5	6	7	8
	ADDRESS BITS A12	A11	A10	A09	A08	A07	A06	A05
177400	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
177440	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF
177500	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
177540	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
177600	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
177640	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
177700	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
177740	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Refer to DEC's "Microcomputer Interface Handbook, 1980" for recommended address and vector assignments.

VECTOR INTERRUPT	08	07	06	05	04	03
	-SWITCH SW2 POSITIONS--					
	3	4	5	6	7	8
000	OFF	OFF	OFF	OFF	OFF	OFF
010	OFF	OFF	OFF	OFF	OFF	ON
020	OFF	OFF	OFF	OFF	ON	OFF
030	OFF	OFF	OFF	OFF	ON	ON
040	OFF	OFF	OFF	ON	OFF	OFF
050	OFF	OFF	OFF	ON	OFF	ON
060	OFF	OFF	OFF	ON	ON	OFF
070	OFF	OFF	OFF	ON	ON	ON
100	OFF	OFF	ON	OFF	OFF	OFF
110	OFF	OFF	ON	OFF	OFF	ON
120	OFF	OFF	ON	OFF	ON	OFF
130	OFF	OFF	ON	OFF	ON	ON
140	OFF	OFF	ON	ON	OFF	OFF
150	OFF	OFF	ON	ON	OFF	ON
160	OFF	OFF	ON	ON	ON	OFF
170	OFF	OFF	ON	ON	ON	ON
200	OFF	ON	OFF	OFF	OFF	OFF
210	OFF	ON	OFF	OFF	OFF	ON
220	OFF	ON	OFF	OFF	ON	OFF
230	OFF	ON	OFF	OFF	ON	ON
240	OFF	ON	OFF	ON	OFF	OFF
250	OFF	ON	OFF	ON	OFF	ON
260	OFF	ON	OFF	ON	ON	OFF
270	OFF	ON	OFF	ON	ON	ON
300	OFF	ON	ON	OFF	OFF	OFF
310	OFF	ON	ON	OFF	OFF	ON
320	OFF	ON	ON	OFF	ON	OFF
330	OFF	ON	ON	OFF	ON	ON
340	OFF	ON	ON	ON	OFF	OFF
350	OFF	ON	ON	ON	OFF	ON
360	OFF	ON	ON	ON	ON	OFF
370	OFF	ON	ON	ON	ON	ON

VECTOR INTERRUPT	08	07	06	05	04	03
	-SWITCH SW2 POSITIONS--					
	3	4	5	6	7	8
400	ON	OFF	OFF	OFF	OFF	OFF
410	ON	OFF	OFF	OFF	OFF	ON
420	ON	OFF	OFF	OFF	ON	OFF
430	ON	OFF	OFF	OFF	ON	ON
440	ON	OFF	OFF	ON	OFF	OFF
450	ON	OFF	OFF	ON	OFF	ON
460	ON	OFF	OFF	ON	ON	OFF
470	ON	OFF	OFF	ON	ON	ON
500	ON	OFF	ON	OFF	OFF	OFF
510	ON	OFF	ON	OFF	OFF	ON
520	ON	OFF	ON	OFF	ON	OFF
530	ON	OFF	ON	OFF	ON	ON
540	ON	OFF	ON	ON	OFF	OFF
550	ON	OFF	ON	ON	OFF	ON
560	ON	OFF	ON	ON	ON	OFF
570	ON	OFF	ON	ON	ON	ON
600	ON	ON	OFF	OFF	OFF	OFF
610	ON	ON	OFF	OFF	OFF	ON
620	ON	ON	OFF	OFF	ON	OFF
630	ON	ON	OFF	OFF	ON	ON
640	ON	ON	OFF	ON	ON	OFF
650	ON	ON	OFF	ON	OFF	ON
660	ON	ON	OFF	ON	ON	OFF
670	ON	ON	OFF	ON	ON	ON
700	ON	ON	ON	OFF	OFF	OFF
710	ON	ON	ON	OFF	OFF	ON
720	ON	ON	ON	OFF	ON	OFF
730	ON	ON	ON	OFF	ON	ON
740	ON	ON	ON	ON	OFF	OFF
750	ON	ON	ON	ON	OFF	ON
760	ON	ON	ON	ON	ON	OFF
770	ON	ON	ON	ON	ON	ON

SIGNAL/ LINE	CONNECTION PIN--to--PIN		SIGNAL/ LINE
RX0	2	17	TX2
RX2	21	12	TX0
RX1	9	23	TX3
RX3	15	5	TX1
RX4	26	42	TX6
RX6	38	30	TX4
RX5	33	48	TX7
RX7	45	35	TX5
RX8	3	18	TX10
RX10	20	11	TX8
RX9	8	24	TX11
RX11	14	6	TX9
RX12	27	41	TX14
RX14	39	29	TX12
RX13	32	47	TX15
RX15	44	36	TX13

RXn = Receive Line, TXn = Transmit Line

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

LAST REFENCE DESIGNATION USED	
INTEGRATED CIRCUIT	U72
RESISTOR	R8
RESISTOR MODULE	RN10
CAPACITOR	C23
DIODE	CR7
CONNECTOR	J1
CRYSTAL OCILLATOR	Y 2
SWITCH	SW2
TRANSISTOR	Q1

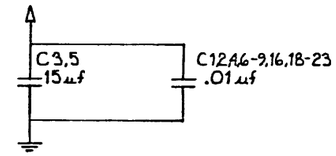
REFERENCE DESIGNATION NOT USED	
INTEGRATED CIRCUIT	U5
	U6
	U41
	U44

REF DESIG	GATES USED PER TOTAL	PART NUMBER
U21	6/8	SN745240
U42	2/6	SN74S04
U28	5/6	SN74S04
U29	4/8	SN74S08
U31	2/4	SN74LS08

SIDE 2		SIDE 1	
+5V	A	BIRQ54	SOLDER SIDE
	B	BIRQ6 L	
GND	C	BDA16 L	
+12V	D	BDA17 L	
BDOUT L	E		
BRPLY L	F		
BDIN L	H		
	J		
BSYNC L	K	GND	
BWTBT L	L		
BIRQ4 L	M		
BIAKI L	N	GND	
BIAKO L	P	BDMR L	
BBS7 L	R		
BDMGI L	S		
BDMGO L	T		
BINIT L	U	GND	
	V		
			COMPONENT SIDE
+5V	A		CONNECTOR A
	B	BPOK H	
GND	C	BDA18 L	
	D	BDA19 L	
	E	BDA20 L	
	F	BDA21 L	
	H		
	J	GND	
	K		
	L		
	M	GND	
	N	BSACK L	
	P		
	R		
	S		
	T	GND	
	U		
	V	+5V	CONNECTOR B

J1

GND	1	2	RXDO L
RXD8L	3	4	GND
TXD1 L	5	6	TXD9L
GND	7	8	RXD9 L
RXD1 L	9	10	GND
TXD8L	11	12	TXDO L
GND	13	14	RXD11 L
RXD3L	15	16	GND
TXD2 L	17	18	TXD10L
GND	19	20	RXD10 L
RXD2L	21	22	GND
TDX3L	23	24	TDX11 L
GND	25	26	RXD4 L
RXD12L	27	28	GND
TDX12L	29	30	TDX4 L
GND	31	32	RXD13L
RXD5 L	33	34	GND
TDX5L	35	36	TDX13L
GND	37	38	RXD 6 L
RXD14 L	39	40	GND
TDX14 L	41	42	TDX 6 L
GND	43	44	RXD15 L
RXD.7 L	45	46	GND
TDX15L	47	48	TDX 7 L
GND	49	50	GND



NEXT ASSY.	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
±1/64- .XX ±.020 ±0°30'
.XXX±.010

MATERIAL

FINISH

DO NOT SCALE DRAWING

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CHECKED		1/15/85
ENGINEER		
APPROVED		
APPROVED		

Sigma Information Systems Inc.

TITLE
SCHEMATIC DIAGRAM, DHV11/16

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400470	F

SCALE	WORK ORDER NO.	SHEET	OF
NONE		1	7

REV. F
SH 1
DWG. NO. SD400470

FORM NO. 801

BUS DATA/ADDRESS INTERFACE

BUS EXTEND REGISTER

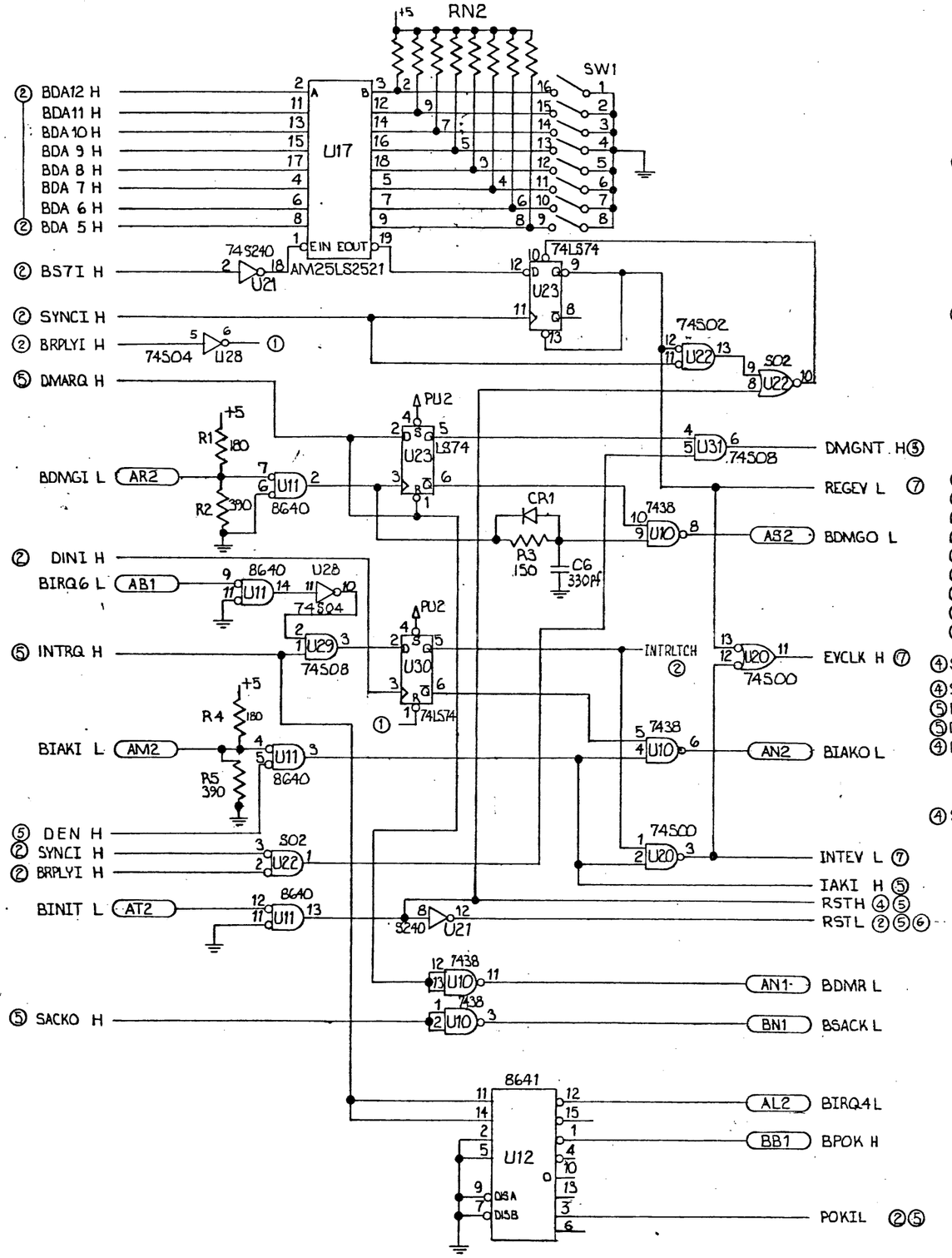
BUS EXTEND

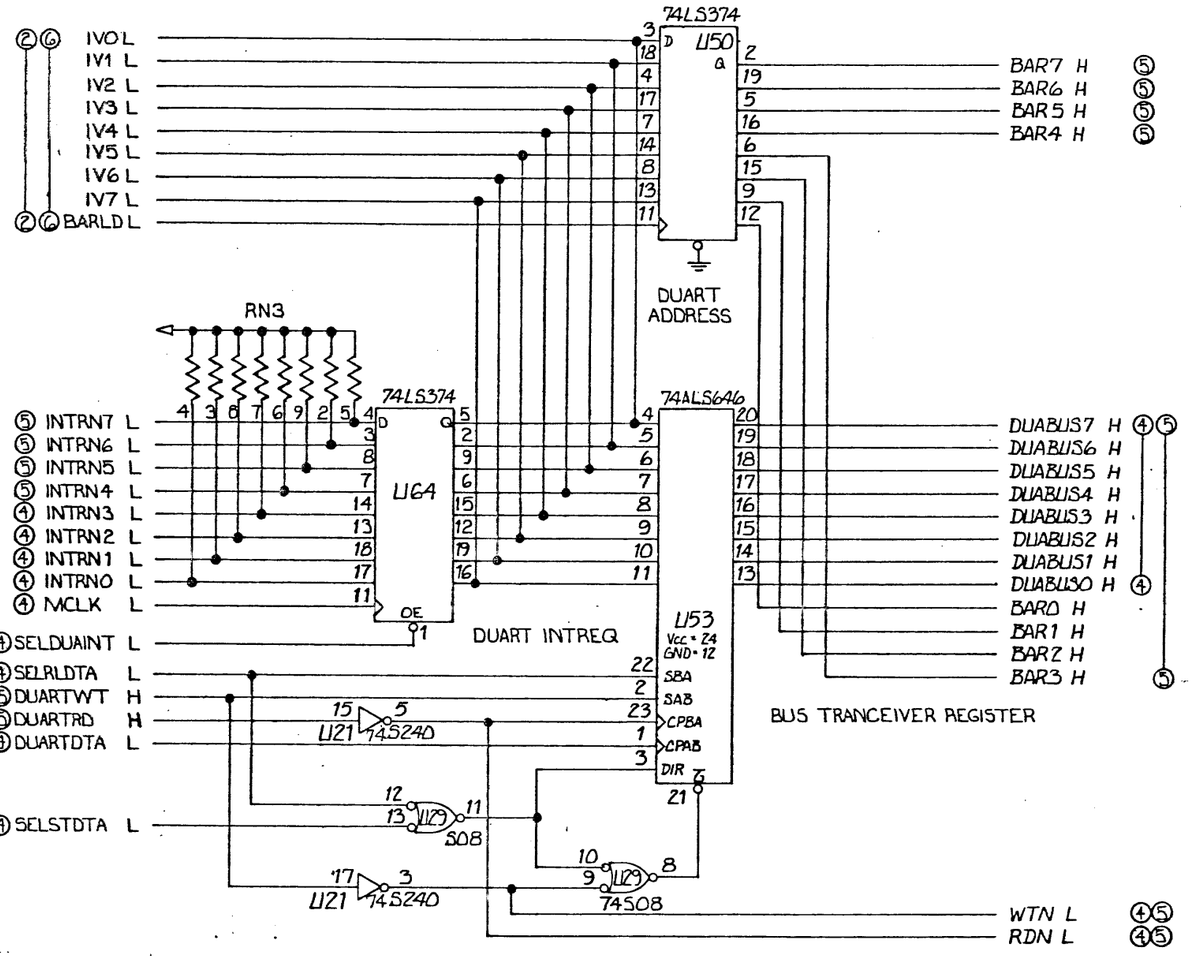
DATA IN REGISTER

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

SIZE D	CODE IDENT. NO.	DRAWING NO. SD400470	REV. F
SCALE NONE	WORK ORDER NO.	SHEET 2 OF 7	

DWG. NO. SD400470 REV. F SH. 2





REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

SIZE	CODE IDENT. NO.	DRAWING NO.	REV
D		SD400470	F
SCALE NONE	WORK ORDER NO.	SHEET 3 OF 7	

DWG. NO. SD400470 REV. F SHT. 3

FORM NO. 002

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

EXTENDED MICROWORD

⑥ MCLK H

⑥ A02 H
A03 H
A04 H
A05 H
A06 H
A07 H
A08 H
A09 H
A10 H
A11 H
⑥ A12 H

273185 U27 (2KX4)
273185 U36 (2KX4)

74LS374 U47

BDEST DECODE

745138 U46
745138 U45
745138 U37

DTALO L ②
DTAHI L ②
BEXT L ②
BCTL L ②
DUARTCTL ⑤
GPLD L ⑤
BARDAL ③

DUART DTA L ③
BRG L ⑤ ⑤

RAMLD L ⑤

SELIV L ②
SELDTAL L ②
SELDTAH L ②
SELRLDTA L ③
SELBC1 L ⑤
SELDUAINT L ③
SELSTDTA L ③
SELRAM L ⑤

74504 U28

MCLK L ②⑤⑥⑦

⑥ SC H
⑥ WC H

74502 U22

TP1

74504 U28

MCLK1L

RG 1K

⑤ UA3 H
⑤ UA2 H
⑤ UA1 H
⑤ UA0 H
③ WTN L
③ RDN L
⑤ RST' H
⑤ 3.6864 MHz H
⑦ RXDO H
⑦ RXD8 H
⑤ SELUAØ L

2681 U54

DUABUS7 H ③
DUABUS6 H
DUABUS5 H
DUABUS4 H
DUABUS3 H
DUABUS2 H
DUABUS1 H
DUABUS0 H ③
TXDO H ⑦
TXD8 H ⑦
INTRNØ L ③

2681 U55

⑦ RXD 1 H
⑦ RXD 9 H
⑤ SELUA1L

TXD1 H 1 ⑦
TXD9 H 9 ⑦
INTR1 L ③

2681 U56

⑦ RXD2 H
⑦ RXD10H
⑤ SELUA2L

TXD2 H 2 ⑦
TXD10 H 10 ⑦
INTRN2 L ③

2681 U57

⑦ RXD3H
⑦ RXD11H
⑤ SELUA3L

TXD 3 H ⑦
TXD 11 H ⑦
INTRN3 L ③

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400470	F
SCALE NONE	WORK ORDER NO.	SHEET 4 OF 7	

REV. F
SH 4
SD400470
DWG. NO.

FORM NO. 862

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

RAM 2K x 8 — Vcc = 24, GND = 12 — U51 — 7C128

74LS374 — U48

IV0 L
IV1 L
IV2 L
IV3 L
IV4 L
IV5 L
IV6 L
IV7 L

BAR10 H
BAR9 H
BAR8 H
BAR7 H
BAR6 H
BAR5 H
BAR4 H
BAR3 H
BAR2 H
BAR1 H
BARO H

SEL RAM L
RAMLD L

DUARTCT L

SELUA0 L
SELUA1 L
SELUA2 L
SELUA3 L
SELUA4 L
SELUA5 L
SELUA6 L
SELUA7 L

74LS374 — U19

DINI H
DOUTI H
BRPLYI H
IAKI H
DMGNT H
POKI H
PARER L

MCLK L

SELBC1 L
GPLD L

W1 W2 W3

74LS273 — U49

UA3 H
UA2 H
UA1 H
UAO H
NC
SACKO H
AEN H
DEN H

RSTL

74259 — U40

BRQL

DMARQ H
INTRQ H
DUARTRD H
DUARTWT H
BAR 10
BAR 9
BAR 8

+5
R7
390 Ω
LED 1

2681 — U58

UA3 H
UA2 H
UA1 H
UAO H
WTN L
RDN L
RST H
3.6864 MHZ
RXD4 H
RXD12 H
SELUA4 L

DUABUS7 H
DUABUS6 H
DUABUS5 H
DUABUS4 H
DUABUS3 H
DUABUS2 H
DUABUS1 H
DUABUS0 H
TXD4 H
TXD12 H
INTRN4 L

2681 — U59

RXD 5 H
RXD13 H
SELUA5 L

TXD 5 H
TXD13 H
INTRN5 L

2681 — U60

RXD 6 H
RXD14 H
SELUA6 L

TXD 6 H
TXD14 H
INTRN6 L

2681 — U61

RXD.7 H
RXD15 H
SELUA7 L

TXD 7 H
TXD15 H
INTRN7 L

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400470	F
SCALE NONE	WORK ORDER NO.	SHEET 5 OF 7	

DWG. NO. SD400470 REV. F SH. 5

FORM NO. 002

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

MICROPROCESSOR SYSTEM

8X305

+5V

Q1 2N5320

C17

U43

② 7MHz H

② 7MHz L

③ RST L

② HALT L

②⑤ IV0 L

IV1 L

IV2 L

IV3 L

IV4 L

IV5 L

IV6 L

②⑤ IV7 L

⑦ DISABLE H

U25, U26, U35, U34 — 2K x 4 — 2758185 — N82S185A,B — 6358411 (MMI)

IO0 H … IO7 H ⑦

IO8 H … IO15 H

A12 H … A02 H ④⑦

A01 H (N.U.)

A00 H (N.U.)

MCLK H ④

SCH ④

WCH ④

LBL (N.U.)

RBL (N.U.)

② LTTMHz H

U24 — 74S05

RN8 470

RN9 330

U32, U33 — 0026

C13, C12, C11, C10 — 1 µf

CR4, CR2, CR7, CR5, CR6, CR3

C14, C15 — 2.2 µf

-9V DC A

+5V

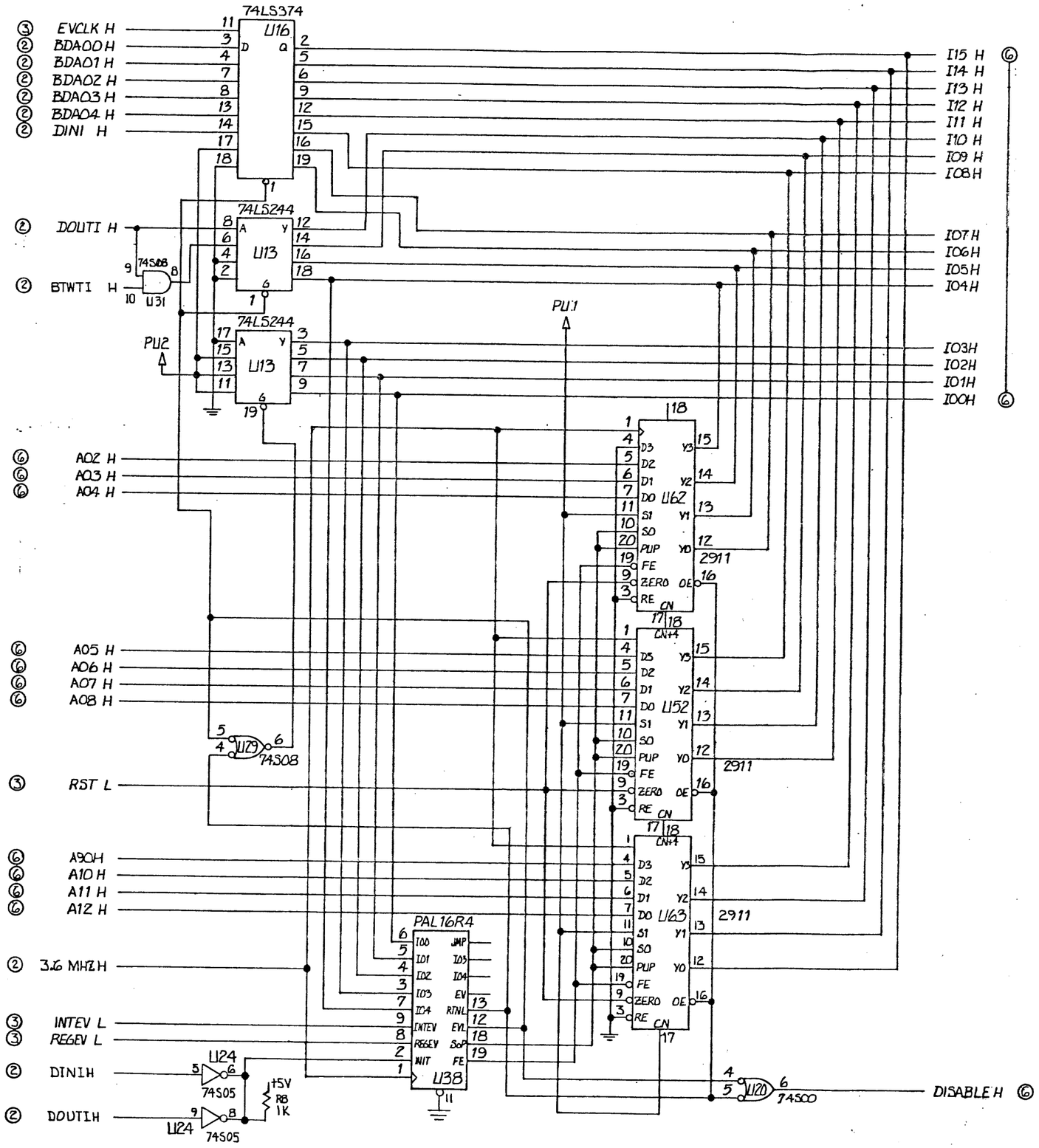
-9V DC B

+5V

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400470	F
SCALE NONE	WORK ORDER NO.	SHEET 6 OF 7	

DWG. NO. 5400470 REV. F SH 6

FORM NO. 002



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED

SIZE	CODE IDENT. NO.	DRAWING NO.	REV.
D		SD400470	F
SCALE NONE	WORK ORDER NO.	SHEET 7 OF 7	

REV. F
SH. 7
400470
DWG. NO.

FORM NO. 502