DOCUMENT NO. Y240A200M202 REV ______

ENGINEERING TECHNICAL REPORT

SKC-2000

COMPUTER CONTROL UNIT (CCU)

USER'S MANUAL

SINGER
AEROSPACE & MARINE SYSTEMS

THE SINGER COMPANY • KEARFOTT DIVISION • 1150 MC BRIDE AVENUE • LITTLE FALLS, N. J. 07424

F4200-4 2/72

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DECEMBER 1973

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ABSTRACT

This document describes the use of the SKC 2000 Computer Control Unit (CCU) from the programmers point of view. It includes a description of the panel displays and all pushbutton/switch inputs. Several common procedures for using the CCU panel are described including the Bootstrap Load procedure.

Effective use of this manual and the SKC 2000 CCU presume detailed knowledge of the architecture of the SKC 2000 computer as described in the manual SKC 2000 Principles of Operation (Document No. Y240A200M0201).

1. INTRODUCTION

The SKC-2000 Computer Control Unit (CCU) provides the user/machine interface for program loading, software checkout, and maintenance. The panel is mounted in a rack-size enclosure with a self contained power supply and interconnects with the two I/O connectors on the computer. The Computer Control Panel provides the following functions.

- Displays pertinent computer registers.
- Enables loading the computer memory manually or by use of a separate high-speed paper tape reader, and provides controls and logic to ascertain memory verification.
- Provide the controls to manually step the computer one instruction at a time.
- Provides the controls to preset the computer to any initial program location.
- Provides the controls to stop the computer at any program step.
- Provides the controls to enable the computer to repeatedly execute any program step.
- Provides the controls to enable dynamic display of any memory cell which is accessed during program execution.
- Provides the controls to enable the computer to continuously execute any one instruction.
- Provides a serial interface connection to a teletypewriter (TTY) for data entry/display.
- Provides the capability to diagnose and correct hardware and software faults in the computer.

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2. COMPUTER CONTROL PANEL DESCRIPTION AND OPERATING INSTRUCTIONS

The indicators and panel controls are shown in Figure 2-1, and are described in terms of the labeling on the controls as follows.

2.1 ADDRESS (0-17) INDICATORS

The ADDRESS indicators are controlled by the DISPLAY switch. When execution is stopped and the DISPLAY switch is set to MEMORY, these indicators display CCU Memory Address Register contents. Should the DISPLAY switch be set to any other position, the indicators will display the contents of the CPU Program Counter.

When the CPU is executing an instruction from memory, the ADDRESS indicators display the 18-bit memory address, placed into the CCU Memory Address Register through the 18 right-most DATA switches. However, should the instruction be loaded from the CCU, these ADDRESS indicators are meaningless. The 18-bit Memory Address formed by the 18 right-most DATA switches are now displayed by the corresponding DATA Indicator lights.

2.2 DATA SWITCHES (0-31)

There are 32 toggle switches, one for each bit in this switch register. They are used to perform the following functions:

1. Setup a 32-bit operand for use when the CPU is instructed to fetch an operand from the CCU in the PANEL OPER mode.

2. Setup an 18-bit memory address for loading into the CPU memory address register when the CPU is in the LOAD/EXAMINE MEMORY mode.

3. Setup an 18-bit memory address, to be used for address coincidence comparison in the ADDRESS COMP MODE of operation.

2.2.1 DATA INDICATORS (0-31)

When the computer is stopped, this set of 32 indicators display data from memory, or from a CPU register selected by the DISPLAY switch. If the computer is running in the ADDRESS COMPARE MODE, the contents of the selected register is displayed when the computer's program counter matches the selected address.

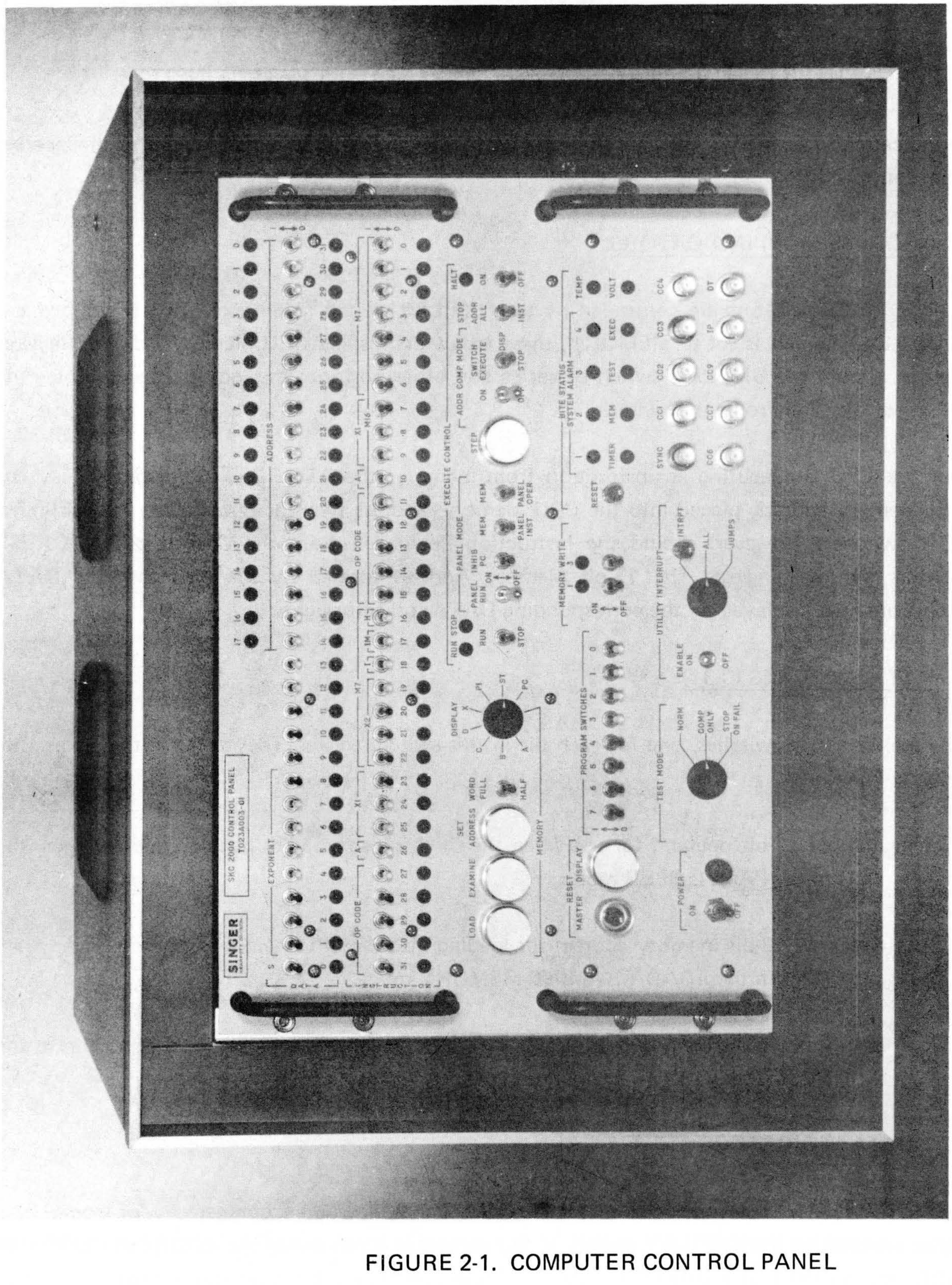

FIGURE 2-1. COMPUTER CONTROL PANEL

2.3 INSTRUCTION REGISTER SWITCHES (0-31)

This switch register enables the operator to perform the following functions:

1. Form a 32-bit instruction word, or two 16-bit instruction words used when the CPU is controlled to execute an instruction from the CCU, either in the ADDRESS COMPARE-SWITCH EXECUTE mode or the PANEL-INST mode.

2. Form a 32-bit instruction or data word, or two 16-bit short words, to be loaded into memory, when the DISPLAY selector switch is in the MEMORY position.

3. Provide a Start Address for loading the Computer's Program Counter in preparation for executing a program in the RUN or single STEP mode. By executing a long jump (JGU) instruction to the desired starting address from these switches, the program counter will be set to the desired starting address.

4. Provide a Start Address when looping in the RUN-SWITCH EXECUTE mode of operation.

2.3.1 INSTRUCTION INDICATORS (0-31)

These indicators display the contents of the Instruction Register at completion of execution of any instruction which is followed by a STOP or HALT. Note that a stop occurs:

1. After every instruction in the single STEP mode.

2. When the CPU is set to stop manually via the RUN-STOP toggle switch.

3. When the STOP address is reached in the ADDRESS COMPARE-STOP mode.

A HALT also occurs when the CPU executes a HLT instruction and the HALT toggle switch is ON.

2.4 DISPLAY SWITCH

This switch is a nine position rotary switch. When the switch is in any of the eight non-memory positions and the computer is not in RUN, the contents of the selected CPU register at completion of the last instruction executed is displayed by the DATA Indicator lights. The meaningful data that can be viewed in the display is as follows:

(A)	A Register (32 bits)	
(B)	B Register (32 bits)	
(X)	Index Register (18 bits)	Contains the contents of the most recently used index register.
(PI)	Program Interrupt Mask Register (16 bits)	
(ST)	Status Register (16 bits)	Contains the following status information: the group of index registers selected, short address extension bits, program flags, interrupt enable, carry and overflow bits, and the halfword arithmetic indicator.
(PC)	Program Counter (18 bits)	Contains the target address of the next instruction to be executed, when computer has executed instructions from memory. When executing instructions from the CCU panel, this display is meaningless. If, in the skip and transfer instructions and a condition is required without being met, there the PC contains the final address plus 1. For non-conditional transfers, the PC always contains the target address.

Not listed above are the C and D registers, which are intermediate registers, and are not accessible to the programmer. In the case of position X, the register displayed will depend upon the condition of status register bits 0 and 1, and on the condition of the X1 or X2 field bits of the last instruction that used indexing.

In the ninth position of the rotary switch, the MEMORY, LOAD, EXAMINE, SET ADDRESS, and WORD switches are activated. However, loading and examining memory in this way uses the DMA hardware, and the memory interrupts must be enabled. To accomplish this:

1. Set the DISPLAY rotary switch to A.

2. Set the appropropriate bits for the Enable Memory Interrupt instruction in the INSTRUCTION Register switches.

3. Press the STEP button. The EMI (Enable Memory Interrupt) instruction will now be executed.

4. To verify that, the memory interrupt has been enabled, turn the DISPLAY rotary switch to ST (Status). DATA indicator light 2 should be lit.

5. Reposition the DISPLAY rotary switch to MEMORY. Now the computer is ready for manual memory loading and examining.

2.5 MEMORY

2.5.1 MEMORY SET ADDRESS SWITCH

This pushbutton switch is used to set the contents of the 18 right-most DATA switches (14 thru 31) into the CCU Memory Address Register.

2.5.2 MEMORY LOAD PUSHBUTTON

Actuating the LOAD pushbutton switch, places the contents of the INSTRUCTION switches into Memory at the address previously inserted into the CCU Memory Address Register (CMAR). The first operation of the LOAD command, after a SET ADDRESS or EXAMINE MEMORY operation, loads the instruction switches into the memory location specified by the CMAR without changing the CMAR. Subsequent operations of the LOAD pushbutton, increments the CMAR two counts before memory access.

2.5.3 MEMORY EXAMINE PUSHBUTTON

This pushbutton switch causes the memory location previously inserted in the CMAR to be read out and displayed on the 32-bit DATA display indicators. The first time the Memory EXAMINE switch is actuated, after a Load Memory or Set Address operation, the address specified by the CMAR is read as it was written from the contents of the INSTRUCTION switches in memory. Subsequent operations of the EXAMINE pushbutton increments the CMAR to obtain the next memory location.

2.5.4 FULL/HALF MEMORY WORD SWITCHES

This toggle switch determines if a full or half word is to be loaded into memory. In the HALF word mode, the contents of the 16 left-most toggle switches of the Instruction Register is the data loaded.

2.6 EXECUTE CONTROL SWITCHES AND INDICATORS

2.6.1 RUN/STOP SWITCH AND INDICATORS

These indicators display which mode the computer is in. The RUN light is on if the computer is executing instructions. The STOP light is on if the computer is stopped. When the toggle switch is set to RUN, the computer starts execution at the location determined by the program counter, and it will continue executing instructions in normal sequence until:

1. The switch is put into the STOP position.

2. The CPU executes a HALT instruction and the HALT toggle switch is ON.

3. The stop address is reached and the CCU is in the ADDRESS COMPARE-STOP mode of operation.

The Run/Stop Switch, when set to STOP causes the computer to stop execution at the next program counter location. The status of the computer at this time depends upon the last instruction executed.

2.6.2 PANEL MODE SWITCHES

These two toggle switches OPER (Operand) and INST (Instruction) are used to determine if the computer is operated from Memory or Panel (CCU).

2.6.2.1 MEM/PANEL INST Switch

When set to MEM, this toggle switch enables the computer to execute instructions from Memory. When set to PANEL INST, the computer will repeatedly execute the instruction set by the INSTRUCTION switches, regardless of the CPU program counter while fetching or storing operands either from memory or the CCU as determined by the MEM/PANEL OPERAND switch. The MEM/PANEL INSTRUCTION selection switch can be used in either single step operation or in the RUN mode.

2.6.2.2 MEM/PANEL OPER Switch

When set to MEM, this switch enables the computer to operate on operands from Memory. When set to PANEL OPER, the computer will repeatedly use the data word set on the DATA switches as the operand, regardless of the CPU generated effective address, while fetching and executing instructions either from memory or the CCU as determined by the MEM/PANEL INSTRUCTION switch. The MEM/PANEL OPERAND selection switch can be used in either single step operation or in the RUN mode.

Note that for the PANEL OPERAND switch to be effective, the PANEL RUN toggle switch must be ON.

2.6.2.3 STEP Switch

When operated, this switch causes the computer to execute a single instruction if the computer is stopped, either RUN/STOP switch set to STOP, or because of a match between the computer program counter and the address setting of the 18 right-most DATA switches when in the ADDRESS COMP-STOP MODE of operation.

If the RUN/STOP switch is in STOP, operation of the STEP switch will cause the CPU to momentarily go into the run condition for one instruction execution and then return to the stopped condition.

2.6.3 ADDRESS COMP MODE

2.6.3.1 ON/OFF Switch

When ON, this switch is used to enable the ADDRESS COMPARISON MODE and generation of oscilloscope SYNC pulses.

2.6.3.2 SWITCH EXECUTE/DISP/STOP Switch

This three position switch is used to set the selected mode of operation when address coincidence occurs. For this switch to be effective, the ADDRESS COMP MODE ON-OFF toggle switch must be ON.

In the SWITCH EXECUTE mode, the CPU will execute the next instruction from the CCU INSTRUCTION switches, when a memory address compare occurs in the CPU Program Counter or Operand Address. By placing a JGU instruction to a desired address from the CCU INSTRUCTION switches, the last mentioned feature will cause the program to loop from the starting address to a STOP address specified by the 18 right-most DATA switches.

In the DISPLAY position, when Memory Address Coincidence occurs, the selected word, as determined by the DISPLAY selector switch, is displayed while the CPU continues to run. If a CPU register is selected, a momentary pause of a few microseconds occurs while the word is being extracted.

When in the STOP position, the computer will stop when the program counter reaches the address (operand or instruction) as determined by the STOP ADDR-ALL/INST toggle switch specified by the content of the 18 right-most DATA switches.

2.6.4 STOP ADDRESS SWITCH

With the ADDRESS COMP MODE switch set to STOP, and the computer in the run mode, the STOP ADDR switch, if set to INST, will cause the computer to stop when memory address coincidence occurs for instructions only.

In ALL, the computer will stop when memory address coincidence occurs for both instructions and operands.

The computer will remain stopped until the RUN/STOP switch is reset (i.e., set to STOP and then back to RUN). The indicator lights display either the RUN or the STOP state.

2.6.5 HALT SWITCH AND INDICATOR

When the switch is in the OFF position and the Halt instruction is executed by the computer, the instruction is interpreted by the CPU to be a NOP. When the switch is in the ON position, and the computer executes a Halt instruction, further execution is inhibited. Subsequently, the RUN indicator goes off, and the HALT indicator illuminates.

2.6.6 RESET/MASTER AND DISPLAY SWITCHES

Operation of the MASTER RESET pushbutton will cause the generation of J1 Initialization signal, which resets the CPU and registers to the initial power turn-on state.

The DISPLAY RESET pushbutton is used to reset all display registers in the CCU to verify the receipt of new data. When this button is pressed, all DATA indicator lights go off. Upon release of this button, the static register contents are displayed.

2.6.7 PROGRAM SWITCHES 0 THRU 7

These eight toggle switches provide control to the CPU switch inputs. The programmer can make use of these switches with a JGW instruction to control branch points within the program.

2.6.8 MEMORY WRITE SWITCH AND INDICATOR

With this switch in the ON position, the MEMORY WRITE indicator goes on and words can be loaded into protected memory. When OFF, loading into protected memory is inhibited.

2.7 PANEL RUN SWITCH

This switch must always be set to ON when using the CCU.

2.8 INHIB PC SWITCH

This toggle switch is used to inhibit incrementing the Program Counter in the computer.

2.9 POWER SWITCH

Power is controlled by this toggle switch. When set to ON, power is applied to the associated light goes on.

The contents of memory core are not affected by switching power off and or. However, the contents of the working registers and LSI memory are lost whenever power goes off (contents are random followingturn on).

2.10 TEST MODE SWITCH

This three position rotary switch is used to determine the mode of testing. The following tabulation describes the switch functions:

SWITCH POSITION	FUNCTION
NORM	If the computer unit is cabled to the I/O unit, then the BITE STATUS indicators will display the BITE register as shown in Table 2-I.
COMP ONLY	The computer unit is not cabled to the I/O unit and it is not desired to stop on a BITE failure. The BITE STATUS Indicators, will display as shown in Table 2-I.
STOP ON FAIL	The computer unit is not cabled to the I/O unit and it is desired to stop on a BITE failure. The BITE STATUS indicators will display as shown in Table 2-I.

2.11 UTILITY INTERRUPT

2.11.1 ENABLE SWITCH

This toggle switch is used to enable an external program interrupt to be generated under conditions defined by the UTILITY INTERRUPT selector switch.

2.11.2 SELECTOR SWITCH

This three position rotary switch is used to select one of three modes of operation within the utility subroutines.

When the Selector switch is set to INTERRUPT, program interruption occurs immediately after the INTERRUPT pushbutton is depressed and the Utility Interrupt ENABLE switch is set to ON.

When the Selector switch is set to ALL, after completing each instruction execution, the program interrupts to a subroutine, which can be used for tracing or other purposes. The program interrupt remains masked until the Return Address (RTA) instruction is executed.

When the Selector switch is set to JUMPS, each successful jump will cause program interrupt transfers to a subroutine which can be used for tracing or other purposes. The three program interrupt sources are combined with Teletypewriter (TTY) and paper tape reader interrupts, and merged into the control panel program interrupt No. 14 through the AGE connector.

2.11.3 INTERRUPT SWITCH

This switch is used to activate the Utility Interrupt mode when the selector switch is in the INTERRUPT position and the ENABLE switch is set to ON.

2.12 BITE STATUS INDICATORS

2.12.1 SYSTEM ALARMS (1-4)

These lights, in conjunction with the TEST MODE switch, are used to obtain a visual indication of the computer's condition. Table 2-1 below shows the conditions required to light these indicators.

TABLE 2-1.

TEST MODE SWITCH POSITION	SWITCH ALARMS	CONDITION FOR ON
NORM	1	Unprotected block of memory in modules 3 and 4.
	2	Computer not OK.
	3,4	Program Controlled
COMP ONLY	1	Lights if computer tires to execute all logic "1" or all logic "0" op code.
OR	2	DC power failure.
STOP ON	3	Memory Release Time Out.
FAIL	4	Indirect Addressing Failure.

The functions of the remaining indicators are contained in Table 2-2.

2.13 BITE STATUS RESET SWITCH

Once present, the EXEC and VOLT signals are latched to remain on. Operation of the RESET pushbutton, extinguishes the BITE STATUS indicators, if the fault has been corrected.

2.14 TEST POINTS

These test points are for diagnostic checkout of the computer, and are to be used for hardware troubleshooting only by qualified personnel.

TABLE 2-2. FUNCTIONS OF INDICATORS

INDICATOR	FUNCTION
TEMP Indicator	This light goes on when an over-temperature condition is detected.
TIMER Indicator	This light goes on when the master clock fails, when the watchdog timer in the Unit Under Test (UUT) is improperly reset, and when the BITE in the UUT is in a self-test condition.
MEM Indicator	This light goes on when the CPU makes an attempt to execute all 1's or all 0's, or if an operand address or the computed address of a jump instruction is out of the memory range.
TEST Indicator	This indicator illuminates when the BITE circuits in the computer are under test.
EXEC Indicator	This indicator, Execution Error, illuminates when an attempt is made to write data into protected memory.
VOLT Indicator	This indicator illuminates when a voltage in the Unit Under Test is out of tolerance. Illumination of this light indicates either a power or hardware failure.

3. COMPUTER START UP

This section describes the procedures to be followed to start or restart the CCU and SKC2000. It covers:

- CCU & SKC2000 power up sequence
- SKC2000 memory priming
- Program Loading
  - with ROM bootstrap loader
  - with Manual bootstrap loader

3.1 START UP OPTIONS

A wide variety of start up procedures are available with the SKC2000. Among these are:

- Read Only Memory (ROM) option

The CPU can include a ROM containing a program loader. This loader can be executed starting at location zero.

3.1.1 Start Up Location Option

The startup location, at power on, is determined by hardware:

- Location 0 - The ROM memory is available
- Location 7000 (HEX). This typically indicates that the ROM is not available (if available it must be entered as described in Section 3.5).

3.1.2 Main Memory Priming.

To condition the main memory at power up, the CPU must be set into RUN mode before entering or reading memory via the CCU. This is described in succeeding sections.

3.1.3 Manually entered bootstrap.

If ROM is not available and if the bootstrap loader (see section 3.5.3) has not been previously placed into memory it must be manually entered.

For some applications the SKC2000 hardware includes a system configuration in which a PDP11 minicomputer is connected to the CCU and acts as a front end to the SKC-2000 for peripheral devices connected to the PDP11. The hardware and PDP11 software have been constructed so that they are transparent to the user in regard to operating the CCU. The use of the PDP11 is not further described herein.

3.2 START UP FLOWCHART

The hardware and operational decisions that determine start up procedures are summarized in a flowchart, figure 3-1.

3.3 POWER UP PROCEDURES

The following CCU switch settings are used for start up

- RUN/STOP - STOP
- PANEL RUN - ON
- MEM/PANEL INST - PANEL
- MEM/PANEL OPER - PANEL
- ADDR COMP MODE - OFF
- HALT - ON
- PROGRAM SWITCHES - All Down

Then:

- Turn CCU Power Switch - ON
- Turn on SKC2000 at power source (installation dependant)
- Depress Reset Master

- POWER UP SEC 3.3
  - START ADDRESS = 7000 HEX — CORE STARTUP SEC 3.5
    - To bypass loading and go directly to execution see Section 3.5.1
    - To use preloaded core bootstrap loader, see Section 3.6
      - To place boot loader in core see Sec 3.5.2 and Sec 3.5.3
        - To load via memory pushbuttons see Sec 3.5.3.l
        - To load via load and store instructions see Sec 3.5.3.2
      - Use of core bootstrap See Sec 3.6 (Program Loading)
    - Use of loader/verifier see Sec 3.7
    - If SKC 2000 contains ROM loader to be used, transfer to location 0 (Sec 3.5), continue as 'Start Address = 0'
  - START ADDRESS = 0 ROM — STARTUP SECTION 3.4
    - To bypass loading and go directly to execution see Section 3.4.l.4
    - To load programs with ROM loader see Sec 3.4.1
      - To load via TTY see Section 3.4.1.2
      - To load via Reader see Section 3.4.1.1
      - Post Load Sec 3.4.1.3
        - To start executing see Sec. 3.4.1.4
        - To load more programs see Sec 3.4.1 (ROM loader) or Sec 3.7 (loader/verifier)

FIGURE 3-1 STARTUP FLOWCHART

The address indicators will display either 0 or 7000 (HEX) and the STOP indicator will be on. If the address is 0, see section 3.4. If the address is 7000, see section 3.5.

3.4 ROM STARTUP

When the computer initializes to location zero, the CPU contains a ROM (Note¢ When the computer program counter contains an address below 3E00 the Panel Mode switches are ignored and the mode is effectively Memory. To allow execution from the panel the program being executed must make a transfer to main memory (core). However data addresses developed in ROM programs that access main memory will still be controlled by **MEM/PANEL** Data).

The ROM contains an initialization sequence starting at locations zero, controlled by Program Switches 6 and 7 as follows:

- o Switch 6 up - Transfer to ROM loader (see 3.4.1)
- o Switch 6 down, switch 7 up - Execute instruction switches (by transferring to core location 7F9E - See 3.4.1.4)
- o both Switches Down - Transfer to 0800 (HEX) in the ROM. This location is not currently populated in the Standard ROM but is available for a special user developed load routine.

After switches 6 and 7 have been set, the ROM loader (if used) is set up as described in 3.4.1. Then, the following sequence will cause memory to be primed and execution will be initiated according to Switch settings:

- o Set both MEM/PANEL switches to MEM
- o Set HALT switch ON
- o RUN/STOP to RUN

3.4.1 Use of the ROM Loader

To utilize the ROM loader, both Panel Mode Switches should be set to MEM. The ROM loader will load FOCAP (SKC2000 Assembler) absolute format 8 level paper tape from either a teletype reader or a high speed paper tape reader. The paper tape can be either odd or even frame parity. The ROM loader will count all parity errors. When a STOP code (See 3.7.1) is recognized on the tape, the computer will halt and display the error count in the A register. The loader options are determined by panel switches 2 and 3.

- o Switch 2 Down - Odd Parity Up - Even Parity
- o Switch 3 Down - High Speed Reader Up - Teletype Input

The ROM loader uses only CPU registers and modifies only the loaded locations. The ROM loader typically loads the Loader/Verifier routine which is then used to load subsequent programs.

3.4.1.1 High Speed Reader Loading.

Place the FOCAP paper tape with leader (RUBOUTS) at the read position. Set the Program Switches as shown above. Set the CCU to RUN and the program will be loaded. See 3.4.1.3 for next procedure.

3.4.1.2 Teletype Loading

If the teletype is equipped with a paper tape reader, it can be used to load programs.

Place the FOCAP paper tape with leader (all holes) at the read position. The reader must be set to STOP or FREE. Set the Program Switches. Set the CCU to RUN. Set the teletype to START and the program will be loaded. See 3.4.1.3 for next procedure.

3.4.1.3 Post Load

After a Stop code is detected on the tape, the computer will halt (HALT indicator on) with a count of parity errors in the A register. If the count is non-zero, the load should be repeated.

The High Speed Reader halts when the computer halts. The teletype does not halt and must be stopped by setting the reader to STOP.

To load additional programs, position the next tape and toggle RUN/STOP to RUN.

3.4.1.4 Transfer To Control From ROM

To transfer control to a loaded program after a Halt in ROM set a JGU XXXX, = 6430XXXX, (HEX), where XXXX is the address, into the Instruction switches. Set Program switch 7 up and Panel Mode Switches to Panel. All others down. Set PANEL RUN ON. Toggle RUN/STOP to RUN. The address indicators will display the address. Set RUN/STOP to STOP. Set both MEM/PANEL switches to MEM. Set RUN/STOP to RUN.

3.5 MAIN MEMORY (CORE) STARTUP

To condition the core memory when power is first turned on, the CPU should be set into RUN mode before entering or reading memory via the CPU.

When the computer initializes to location 7000 (HEX), and the ROM is present in the CPU, the ROM bootstrap loader can be entered:

- o Set Program Switch 6 up
- o Place a JGU 4000 (64304000) into the Instruction Switches
- o Set both MEM/PANEL Switches to PANEL
- o RUN/STOP - RUN . This allows memory to be primed. The Address indicators will contain 4000
- o RUN/STOP - STOP
- o Place a JGU 0000 (64300000) into the Instruction Switches
- o Depress Step once. The Address indicators will contain 0000
- o Set both MEM/PANEL switches to MEM
- o Continue with 3.4

If it is known that the contents of memory contain a program (typically the core bootstrap loader) to be executed see 3.5.1. If data must be entered via the CCU see 3.4.2.

3.5.1 Start Up Program Execution

This procedure includes memory priming.

- o Place a JGU XXXX (6430XXXX) into the Instruction Switches where XXXX is some even memory location.
- o Set both MEM/PANEL Switches to PANEL
- o RUN/STOP - RUN. This allows memory to be primed. The Address indicator will contain XXXX.
- o RUN/STOP - STOP
- o Set both MEM/PANEL switches to MEM
- o RUN/STOP - RUN

3.5.2 Manual Memory Loading

Prior to loading memory the following procedure is used to prime memory:

- Place EMI - HALT (00800280) in the Instruction Switches
- Set both MEM/PANEL Switches to PANEL
- Halt - ON
- RUN/STOP - RUN
- The computer will halt with 7802 (HEX) displayed in the address indicators. The CCU can now be used to enter information into memory.

3.5.3 CORE BOOTSTRAP LOADER

The core bootstrap loader loads standard FOCAP (SKC2000 Assembler) absolute format, 8 level paper tape from a high speed reader into the memory locations indicated on the tape. By changing 2 words as shown, it can load from a teletype reader. It performs no error checking and should typically be used to load the Loader/Verifier program which is then used for loading other programs.

The Bootstrap Loader is loaded manually in one of two ways. It can be loaded directly into memory by means of the MEMORY pushbuttons, or alternatively by means of, Load and Store instructions through the panel.

Table 3.1 contains a hexadecimal listing of the Bootstrap Loader which is entered into memory, beginning at location 78C0. The source is shown in Figure 3-2. After loading, it is entered by executing a jump to 78C0. After recognizing a STOP code on the tape, the loader will halt with 78E7 displayed in the Address indicators.

To load memory with the bootstrap loader via MEMORY pushbuttons see 3.5.3.1. To use LOAD and STORE instructions, see 3.5.3.2.

TABLE 3-1 FOCAP FORMAT PAPER TAPE BOOTSTRAP LOADER (HEXADECIMAL REPRESENTATION)

SKC-2000 LOADER PROGRAM
OCCUPIES LOCATIONS 78C0 TO 78EA
LOADS OPERATIONAL PROGRAMS INTO CORE FROM PAPER TAPE
STARTING LOCATION IS 78C0

LOCATION	CONTENTS	
078C0	9C0178E8	
078C2	FC0178E8	
078C4	5C020005	
078C6	4E8178E~~A~~8	
078C8	4A830C6B	(FOR TTY READER - 4A830C64)
078CA	62824883	
078CC	0C676207	
078CE	0C7F6215	
078D0	0C7B638B	
078D2	0301608F	
078D4	0C790862	
078D6	6C030001	
078D8	08646093	
078DA	644878E0	
078DC	79003101	
078DE	0690609B	Sync Addr 078DE for display of store address with display switch set to A register. Ref Sec 2.4.
078E0	03810500	
078E2	08416085	
078E4	0C7B62A1	
078E6	028060A7	
078E8	00000000	
078E~~A~~8	02DA1AED	(FOR TTY READER - 02DA215D)

```
*                          *      SKC - 2000 LCADER
*                          *      THIS PROGRAM WILL LCAD CPERATICNAL PROGRAMS INTO CORE FROM
*                          *      PAPER TAPE.  IT IS TCGGLED INTC CORE FROM THE COMPUTER CONTROL
*                          *      UNIT ( CCU ).
*                          *          THE PROGRAM IS STARTED BY PLACING A JGU START( 643C78C0 )
*                          *      ON THE INSTRUCTION SWITCHES CF THE CCU.  TOGGLE THE RUN SWITCH
*                          *      ( IN PANEL MODE ), THEN PLACE THE CCU INTO MEMORY MODE, THE HALT
*                          *      SWITCH IN THE UP POSITICN, AND PLACE THE RUN/STOP SWITCH IN THE
*                          *      RUN POSITICN.  THE TAPE IN THE READER WILL BEGIN LOADING
*                          *      AND THE LCADER WILL CCME TC A HALT AFTER THE LOAD.
*                          ****************
078C0 30912 1 C00C0CCC XC      SETX  0              XR0
078C0 30912 1 00J00002 X2      SETX  2              XR2
078C0 30912 1 0000001C READ    SETX  10
*                          *
078C0 30912 1 9C0178E8 START   LDS   STAT           LCADER STARTING LOCATION
078C2 30914 1 FC0178E8         LDI   STAT           INITIALIZATION
078C4 30916 1 5C020C05 LDVF05  LDX   X0,5,M         FRAME COUNTER INITIALIZATION
078C6 30918 1 4E8178EA LDVF04  DOM   STED,READ,C,K  STEP THE READER
078C8 30920 1 4A83     LDVF01  DIA   READ,C,K       READ THE CCU STATUS REGISTER
078C9 30921 1     0C6B         SRC   11             CHECK BIT 10 - TAPE READER INTERRUPT
078CA 30922 1 6282             JRG   LDVF01
078CB 30923 1     4883 INPUT   DIA   READ,K         READ TAPE INTC A REGISTER
078CC 30924 1 0C67             SRC   7              CHECK BIT 6
078CD 30925 1     6207         JRG   LDVF12         BIT 6 CFF - TREAT AS DATA
078CE 30926 1 0C7F             SRC   31             CCNTRCL CHARACTER, CHECK BIT 5
078CF 30927 1     6215         JRG   LDVF03         BIT 5 CFF - CATA FOLLOWS OR STOP
078D0 30928 1 0C7B             SRC   27             BIT 5 ON - ACCR FOLOWS OR DELETE,CHK BIT C
078D1 30929 1     638B         JRL   LDVF04         BIT 0 ON - TAPE IS LEACER,GO TO NEXT FRAME
078D2 30930 1 0301             SET   1              BIT 0 CFF - SET THE ADDRESS FLAG
078D3 30931 1     6C8F         JRU   LDVF05
078D4 30932 1 0C79     LDVF12  SRC   25
078D5 30933 1     0862         SRLD  2              SHIFT 2 BITS INTC B REGISTER
078D6 30934 1 6C030001         IMN   X0,1,M         JUMP ARCUNC SHIFT OF 4 IF LAST FRAME OF
078D8 30936 1 0864             SRLD  4              WCRD IS BEING PROCESSED
078D9 30937 1     6093         JRU   LDVF04
078DA 30938 1 644878EC         JGF   LDVF09,1       JUMP IF ACCRESS
078DC 30940 1 790C             STB   0,X2           STORE THE ASSEMBLED WORD
078DD 30941 1     3101         LAE   2,X2           INCREMENT STORAGE ACCRESS POINTER
078DE 30942 1 069C     LDVF13  LXA   X2             ADDRESS PCINTER TO XR2
078DF 30943 1     6C9B         JRL   LDVF05
078E0 30944 1 0381     LDVF09  RST   1              RESET THE ACCRESS FLAG
078E1 30945 1     050C         EAB                  ADDRESS TC A REGISTER
078E2 30946 1 0841             SLL   1              PCSITICN FOR INCEX ACCRESSING
078E3 30947 1     6085         JRU   LDVF13         STCRE IN XR2
078E4 30948 1 0C7B     LDVF03  SRC   27             CHECK BIT 0
078E5 30949 1     62A1         JRG   LDVF05         IF CONTRCL BIT 0 IS OFF,DATA FOLLOWS
078E6 30950 1 028C             HLT                  STCP CODE HALT
078E7 30951 1     6CA7         JRL   START          FCR RESTART FOLLCWING LOAD
078E8 30952 1 000C0C0C STAT    HEX   0
078EA 30954 1 02DA1AED STED    HEX   02DA1AED       HIGH SPEED REACER CONTROL WORD
078EC 30956 1 00000000         END
```

FIGURE 3-2 SOURCE LISTING, BOOTSTRAP LOADER

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3.5.3.1 Bootstrap Loading Via Memory Pushbuttons

1. Verify that memory interrupt has been enabled by setting the DISPLAY switch to ST (STATUS). Data Indicator light 2 should be lit. If not

   – Set an Enable Memory Interrupt (00800080) in the Instruction Switches

   – Depress STEP. Repeat I, above

2. Set the DISPLAY switch to MEMORY

3. Set the 18 right-most DATA switches to 078C0.

4. Depress SET ADDRESS. The ADDRESS indicators will display 78C0.

5. Set the Instruction Switches to the contents of 78C0 as shown in Table 3.1.

6. Depress the LOAD pushbutton. The contents of the Instruction Switches will be stored and the ADDRESS indicators will show what address received the current contents of the Instruction Switches.

7. Set the Instruction Switches to the contents of the next memory location shown in Table 3.2.

Proceed with steps 6 and 7 until the Bootstrap has been completely loaded.

8. To verify that the data entered into memory is correct, set the 18 right-most DATA toggle switches to 78C0 and depress the SET ADDRESS pushbutton. If the EXAMINE pushbutton is depressed once, the contents of that location will be displayed on the DATA lights. Each succeeding EXAMINE switch actuation will advance the address and display the contents of the new location. If it is necessary to alter a displayed location, set the 18 right-most DATA switches to the desired address and depress the SET ADDRESS switch. Set the INSTRUCTION switches to the new data value, and depress the LOAD pushbutton. Any of these load values may be verified after entry, by depressing the EXAMINE switch.

After loading is complete, continue at 3.6.

3.5.3.2 Manual Bootstrap Loading By Load and Store Instructions From The Panel.

1. Set the PANEL RUN switch to ON.

2. Set the computer to STOP.

3. Set the DISPLAY switch to A.

4. Set the MEM/PANEL OPER switch to PANEL OPER (operand).
5. Set the MEM/PANEL INST Switch to PANEL INST.
6. Set a LDA-long (1400 HEX) into the 16 left-most INSTRUCTION switches. Set 78C0 in the 16 right-most INSTRUCTION switches.

7. Set the DATA switches to the value for this address setting as shown in Table 3.1.

8. Depress the STEP switch once. After executing this instruction, the computer will stop.

9. Set the 16 left-most INSTRUCTION switches for an STA-long (3C00 HEX) instruction.

10. Set the PANEL MODE-MEM/PANEL OPER to MEM.

11. Depress the STEP button to store into memory the value last loaded from the panel.

12. To verify that the data entered into memory is correct, reset the INSTRUCTION switches to an LDA instruction. Depressing the STEP button will display the memory contents of the address setting on the DATA bank of lights.

13. Set the 16 right-most INSTRUCTION switches for the next address called for in the Bootstrap program.

14. Repeat steps (6) through (12) until the Bootstrap has been loaded and verified.

3.6 PROGRAM LOADING

To load the Loader/Verifier or other program, the Bootstrap Loader program must be loaded into memory, and the program tape set to be read at the High Speed Reader or teletype reader (set to FREE or STOP) with the RUBOUTS/DELETES (all holes) that precede the Load data positioned under the read head.

1. Set the computer to STOP.

2. Set the HALT switch to ON.

3. Set the DISPLAY switch to A (accumulator)

4. The INSTRUCTION switches to a JGU 78C0 (643078C0)

5. Reset the program counter by depressing the MASTER RESET pushbutton.

6. Set the PANEL MODE switches to PANEL.

7. Toggle the RUN/STOP switch and make sure that the JGU instruction is read in, by checking that the corresponding bits illuminate on the INSTRUCTION display, and verify that the ADDRESS bits illuminate to 78C0.

8. Set the MEMORY WRITE switches to ON (if loading into protected memory).

9. Set the two PANEL MODE switches to MEM.

10. Set the computer to RUN. The tape unit is now activated. The High Speed Reader will run until it reaches the stop code at the end of the tape and will then halt. The teletype reader must be set to START and it will continue to run and must be set to STOP when the computer halts. After loading is complete, continue at 3.5.1.

3.7 LOADING ABSOLUTE FOCAP TAPE WITH THE LOADER/VERIFIER

The procedure for loading FOCAP format tape is similar to the steps outlined in paragraph 3.6 except for the starting address. The appropriate START address is obtained in the Loader/Verifier program listing. To verify that the assembled program has been entered into memory correctly, the tape is rewound and re-run after setting the appropriate PROGRAM SWITCHES. The tape to be loaded must be positioned with the RUBOUTS/DELETES (all holes), that precede the load data, positioned under the read head.

The function of the PROGRAM SWITCHES for loading and verifying either odd or even parity tapes is as follows.

PROGRAM SWITCHES	OFF	ON
0	LOAD	VERIFY
1	COUNT ERRORS	STOP ON ERROR
2	DATA ODD PARITY	DATA EVEN PARITY

3.7.1 Load Tapes Format

1. The format used for the paper tape memory load and verify minimizes the number of characters required and permits address and data words to be interspersed. This format is generated by SKC2000 assembler/loader software.

2. Six tape characters are required to define one 32-bit computer word. The tape format shown in Table 3-1 is used. The eighth bit is used for parity. Parity is checked in Data and Address frames only, by software. It is not checked by the CCU logic.

3. There are five control characters which are recognized by the loader/verifier:

   a. Code Delete (E1) - Ignored, may be used for tape loader.

   b. Address Following (E0) - Identifies the following data as an address.

   c. Data Following (C0) - Identifies the following data as a computer data word.

   d. Checksum Following (C2) - Identifies the following data has a checksum.

   e. Stop Code (41) - Indicates end of the tape.

   The CPU will consider all words to be data unless an Address Follows character precedes it. Data words not preceded by an address will be loaded into consecutive memory locations. An example of a programmed tape is shown in Table 3.3.

TABLE 3-2 TAPE FORMAT

DATA AND ADDRESS FORMATS

P	Z	X	X	X	X	31	30	
P	Z	29	28	27	26	25	24	Tape Direction
P	Z	23	22	21	20	19	18	
P	Z	17	16	15	14	13	12	
P	Z	11	10	9	8	7	6	
P	Z	5	4	3	2	1	0	

Bit 0: Least Significant
Bit 31: Most Significant
X = Not Used
Z = No Hole = "0"
H = Hole = "1"
P = Parity

SPECIAL CHARACTERS

H	H	H	X	X	X	X	Z	Address Follows
H	H	Z	X	X	X	X	Z	Data Follows
X	H	H	X	X	X	H	Z	Checksum Follows
X	H	Z	X	X	X	X	H	Stop Code
H	H	H	X	X	X	X	H	Code Delete

TABLE 3-3 EXAMPLE OF TAPE INTERPRETATION

CHARACTER NUMBER

24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	0						0				0	0					0	0	0		0	0	0	Bit 1 LSB
									0		0	0					0	0	0		0	0	0	Bit 2
									0	0	0	0					0	0	0		0	0	0	Bit 3
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	Sprocket
								0		0		0					X				0	0	0	Bit 4
								0		0	0						X	0	0		0	0	0	Bit 5
								0	0	0	0							0	0	0	0	0	0	Bit 6 MSB
													0							0	0	0	0	Bit 7 Control Bit
													0							0	0	0	0	Bit 8 Parity Bit

Note:

"0" represents a hole in the tape.

Characters 1, 2, 3 are leader (all holes)

Character 4 is Address Follows (E0)

A total of six frames (5 through 10) make up a 16 bit address. Characters 8 through 10 do not contain any holes. Character 5 represents the least significant digit, and character 7 represents the most significant digit. The two X's in character 7 are used when a full 18 bit address is required.

Since the punch shifts the address 1 bit right before punching, the desired address is twice the address read from the tape. In the above example, it is

7DF7 X2 = FBEE

Character 11 is Data Follows (C0)

Characters 12 through 17 is the DATA value. Unlike the address, data is not shifted by the punch routine. Hence data is used as it is.

Scanning the bits of the most significant digit in characters 16 and 17, to the least significant digit in character 12, the data represented in HEX is:

DATA = 789BCDCF

A variable amount of DATA can follow before the next address.

Character 23 is the stop code (41).