PART 3: DISK SYSTEM HARDWARE

PREFACE

This section describes the characteristics of the SSB floppy disk interface. This interface allows users of the SWTPC 6800 microcomputer system to easily interface up to four SA400/SA450 5" disk drives or four SA800/SA850 8" disk drives.

BOOT AND I/O ROUTINES

To facilitate disk I/O a ROM has been provided on the disk interface board. The ROM contains all necessary I/O routines to read, write, seek, step and restore the disk drives. In addition, a disk boot routine has been included in the ROM.

DISK CONTROL

Disk control is achieved by the use of the Western Digital FD1771B-01 floppy disk controller IC. This IC controls read/write format, head step, seeking, and checks the write protect status of the disk. The read/write format can be programmed to many formats including IBM 3740 format. CRC generation and checking are also performed within the FD1771B-01 IC. Additional information on programming the floppy disk controller chip may be found in the Western Digital FD1771B-01 product guide.

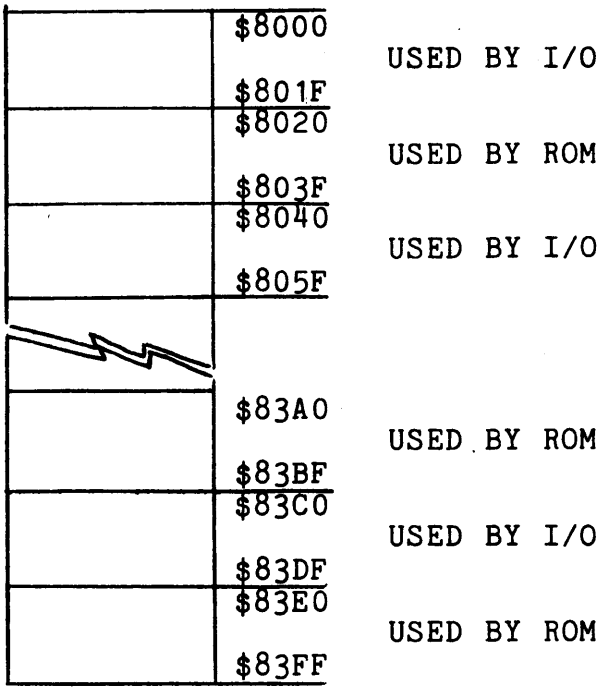
FD1771B-01 CONTROL

All communications between the host system and the FD1771B-01 IC are through a 6821 PIA. Control line functions of the FD1771B-01 are handled by the A-PORT and other programmable control input/output pins of the PIA. Data to and from the floppy disk chip is transmitted through the B-PORT of the PIA.

ROM

The ROM located at U5 provides 512x8 bits of information for the user. The ROM addressing is decoded to use all unused addresses in the I/O page between $8020 and $83FF. The 9324 decoder U7 provides high order address decoding. Use of unused areas of the I/O page is achieved by requiring address bit 5 to be true to enable the ROM. Address bits 0-4 of the ROM are driven by address lines 0-4. Address bits 5-8 are driven by address lines 6-9. The figure below illustrates the interleaving of I/O and ROM addresses.

ROM MEMORY MAP



The above figure shows I/O memory illustrated as pages of 32 words. When bit 5 is a Ø, that 32 word page is used as I/O locations. When bit 5 is a 1 that page is decoded by the ROM as one of its addresses and the particular byte of information required is placed on the system data buss.

DISK INTERFACE DESCRIPTION

Address decoding for the 6821 PIA is provided for by NAND gate U19 and the 9324 decoder, U6. The 74LS3Ø 8-input NAND gate U19 generates the non-programmable address decoding of the address bits A5-A12 at U19-8 to the CS2- input at U18 pin 23. Register selection within the PIA is controlled by address lines AØ and A1 at U18 pins 36 and 35.

The PIA data inputs (U18,26-33) are tied directly to the the negative true system data buss. Care must be exercised in programming the PIA as the PIA expects to see positive true data at the system port. All control functions sent to the PIA should first be complemented by the controlling program. All control information received from the PIA should be interpreted as negative true data by the receiving program. the DAL- lines of the FD1771B-Ø1 IC are tied to the B-PORT of the PIA at U18(1Ø-17). Data to and from the FD1771B-Ø1 on the DAL lines is defined as negative true data. As data is not inverted through the PIA, it is not necessary to invert data from or to the FD1771B-Ø1 as is required with the control registers of the PIA. Data exchange between the PIA and FD1771B-Ø1 are controlled by the following control lines:

WRITE ENABLE

CB2 of the PIA is used to strobe information from the 6821 into the FD1771B-Ø1. CRB bits 3-5 should be programmed to '1Ø1'. In this mode CB2 is cleared on the positive transition of the first 'E' pulse following a write 'B' data register operation and set high on the positive transition of the next 'E' pulse. During write operations the read flip-flop, U25, must be disabled by programming A-PORT bits 6 and 7 to 1 and Ø respectively.

REGISTER SELECT

A-PORT bits Ø and 1 drive the register select lines of the floppy disk controller chip. PAØ drives address line AØ and PA1 drives address line A1.

READ ENABLE

Reading information from the FDC is controlled by its read enable input at U17-4. This input is driven by the read enable flip-flop U25-6. Flip-flop U25 is used in two modes. Mode one is used when reading control registers in the FD1771B-Ø1. Mode two is used when reading data from the disk. In mode one PA6 (U18-8) is programmed to 'Ø'. PA6 low forces U25-6 to the low state thereby enabling information from selected register onto the DAL lines (U17,7-14). this information can then be read in on the B-PORT of the PIA. In mode two PA6 and PA7 (U18-8,9) are programmed to '1's. When DRQ (U17-38) comes true and PA7 is true flip-flop U25 will be set on the positive transition on the 1 Mhz clock (U25-12). DRQ is also tied to the CA2 input of the PIA (U18-39). This programmable pin is programmed as an input triggered by a positive transition (CRA bits 3-5 =11Ø). On the positive transition of DRQ, IRQA at U18-38 will be set low (IRQA reflects the status of the bit set by the positive transition at input CA2(U18-39)). The IRQA output is used to drive the K input for read enable flip-flop U25. As long as IRQA remains active low U25 will not be allowed to reset. U25 setting causes a byte of data from the floppy disk to be placed on the DAL lines (U17-7,14). When the processor detects CRA bit 6 set it can then read the byte of data on the DAL lines though the B-port data register. After the processor has read the data from the B-PORT the flag in the A-PORT control register is cleared by reading the A-PORT data register. Reading the A-PORT data register also deactivates IRQA. This allows U25 to reset thereby preparing the floppy disk chip for the next byte of data from the disk.

HEAD LOAD TIMING

Head load time of the SA4ØØ minifloppy is approximately 75 milliseconds. The 96Ø2 oneshot (U9) provides the delay signal required for proper operation of the FD1771B-Ø1. The time delay generated prevents the floppy disk controller from reading or writing before the head has had time to settle.

DISK INTERFACE SIGNALS

DISK SELECT

During operation one of four disks may be selected at any one time. Disk select is controlled by PIA A-Port bits 4 and 5. These lines are connected to a 74LS138 (U14-1,2) which decodes the signals to select one of four drives. The disk select lines are buffered by the 7417 buffer located at U22. U22 provides the required drive capability needed to drive the disk interface buss.

SIDE SELECT

PIA Port A Bit 3 is buffered by U15 and provides the side-select output for use in double sided disk systems.

MOTOR ON

The motors on 5" drives are turned on as soon as the disk is selected and will stay on as long as the disk system is accessed. U8 is wired as a retriggerable one-shot and has a perriod of approximately 30 seconds. After the last head load, U16-2 goes high which reverse biases D1, allowing U8 to time ouut. U1-5 is an inverting buffer used to drive the MON- line of the SA400 drive. 8" drives use AC motors designed for continuous duty and operate at all times for fastest disk access.

One-shot U9 is used to provide a motor start delay and a head load delay. The motor start delay is disabled by U8-3 if the motor is already running.

WRITE DATA

The Write Data signal at U17-31 is buffered and inverted by U23-12. Write data on the disk interface buss is negative true data (WR DATA-).

WRITE GATE

The Write Gate signal at U17-30 is buffered and inverted by U23-9. Write gatte (WR GATE-) along with WR DATA- controls writing of data to the selected disk.

STEP

The step pulse at U17-15 is buffered to the disk interface buss by U23-2 (STEP-). The step output provides the step instruction to the disk at a controlled rate. The step rate is progrrammed by the user. For the SA400 the step rate should be programmed to 40 msec per step. For additional information on step rates see the Western Digital FD1771B-01 product guide available from Western Digital.

DIRECTION

The direction output of the FD1771B-01 (U17-16) is buffered by U23-5 (DIR-). For step-in (towards the disk hub) the direction line will be high. For step-out the direction line will be low (this level will be reversed on the buss).

TRACK 00

The TRACK 00 status of the selected disk is buffered by U24-2 and is ANDed to HEAD LOAD from the WD1771-1 (U17-28). This signal "fakes" the WD1771-1 into thinking it is on track 00. This allows the system to respond faster after a reset or on power up.

WRITE PROTECT

Write protect (WRT PROT-) is buffered by U24. Resistor R26 provides the required pullup. The write protect line reflects the status of the currently active disk. If the write protect hole in the disk is covered the write protect line will be low. The buffered write protect line U24-11 drives U17-36. Before doing any write operations the write protect line is sampled. If the line is low the write operations will be aborted by the controller chip.

READ DATA

READ DATA- is buffered by NAND gate U3-(1,2). It is then sent through a one-shot to shape the signal. From here there are two options: Option 1) is to use the external data separator, and option 2) is to use the data separator internal to the FD1771-1. The FDC board is configured to operate with the external data separator. The internal separator may be selected by cutting both traces labeled J-12 and inserting jumpers at both locations labeled J-13. The difference between the two separators is one of resolution; The external separator is better at rejecting jitter from an SA400, and thus it is recommended that the external data separator be used.

The external data separator consists of IC'S U1, U2, U3, U4, U11, and U16. The separator works by generating "windows" through which data and clock pulses are gated from read DATA- to the FD1771-1. The synchronization of the separator to the incoming

data is done by retriggerable one-shot U11, associated gates, and flipflops. The one-shot timing is controlled by potentiometers R18 and R19 which are set at the factory and should not be adjusted in the field.

INDEX PULSE

The index pulse is buffered by AND gate U24-9,10 (INDEX PULSE-). Pullup is provided by resistor R25. The buffered index pulse signal at U24-8 drives U17-35. This signal provides sychronization information for the floppy disk chip.

INSTALLING ADDITIONAL DRIVES

Additional minifloppy disk drives may be installed in the field. To install a second or third drive, proceed as follows:

1) Locate the drive select jumpers located in a dip socket on the top corner of the board on the disk drive.

2) The jumpers are cut as shown in the table below for SA400 drives:

DRIVE	CUT	REMOVE
0	MX, DS2, DS3	
1	MX, DS1, DS3	RESISTOR PACK 760-3-R150 OHM
2*	MX, DS1, DS2	RESISTOR PACK 760-3-R150 OHM

The jumpers are cut as shown in the table below for B51 drives:

DRIVE	CUT	REMOVE
0	DS2, DS3, MUX, HM	
1	DS1, DS3, MUX, HM	RESISTOR PACK 760-3-R150 OHM
2*	DS1, DS2, MUX, HM	RESISTOR PACK 760-3-R150 OHM

* A fourth drive (accessed as unit #3) may be installed on J4 by jumpering it the same as unit #1 on J2. Or, drives 0 and 1 may be connected to J2 and 2 and 3 connected to J4. In that case, the drives on J4 should be jumpered the same as the drives on J2.

NOTE: The resistor pack is removed from all drives except the drive which is on the end of the ribbon cable connecting to the controller (normally this is drive zero).

To install additional SA800 drives, the jumper on the back of the SA800 printed circuit board near the cable edge connector should be moved as shown below:

DRIVE	MOVE JUMPER TO
0	DS1
1	DS2
2	DS3
3	DS4

DISKETTE REQUIREMENTS

The Smoke Signal Broadcasting disk systems use standard size media with one index hole. For maximum flexibility in adapting our system to special user requirements, we use a soft-sectored disk format. Thus, diskettes designed for the specialized requirements of hard- sectored systems such as the Northstar which use multiple index holes will not work with the our disk systems. If you inadvertently try to format a multiple index hole diskette, the formatting program will report a very large number of "bad sectors".

ADJUSTMENTS FOR 5" OR 8" DRIVES

The BFD-68 controller board can be used with either 5" or 8" drives, but not both. The proper PC jumpers are installed at the factory and the data separator timing adjusted for the type of drive shipped with the system. It is recommended that modifications required to make the controller operate with a different size disk drive than supplied with original system be made at the factory.

RESET J1-9
D7 J1-43
D6 J1-44
D5 J1-45
D4 J1-46
D3 J1-47
D2 J1-48
D1 J1-49
D0 J1-50
R/W J1-10
Ø2 J1-12
VMA J1-11
A0 J1-27
A1 J1-28
A2 J1-29
A3 J1-30
A4 J1-31
A6 J1-33
A7 J1-34
A8 J1-35
A9 J1-36
A10 J1-37
A11 J1-38
A5 J1-32
A12 J1-39
A13 J1-40
A14 J1-41
A15 J1-42
+12V J1-19
-12V J1-20
8V UNREG J1-21 J1-22 J1-23
GND J1-24 J1-25 J1-26
J2-30 J3-46 J4-30 READ DATA
WRT. PROT J2-28 J3-44 J4-28
INDEX PUL. J2-8 J3-20 J4-8
TRACK ØØ J2-26 J3-43 J4-26
X1 2.000 MHZ
J2-22 J3-38 J4-22 WR DATA
J2-24 J3-40 J4-24 WR GATE
J2-20 J3-36 J4-20 STEP
J2-18 J3-34 J4-18 DIR
J3-22 READY
J2-10 J3-26 DSØ
J2-12 J3-28 DS1
J2-14 J3-30 DS2
J3-32 J4-12 DS3
J3-18 HLD
J3-10 25/MON
J2-16 J4-16 MON
J2-32 J3-14 SSEL
I.C. 22

SMOKE SIGNAL BROADCASTING

SCALE	APPROVED BY	DRAWN BY
DATE 2/28/79		REVISED

LOGIC DIAGRAM, CONTROLLER BD

BFD-68 REV A | DRAWING NUMBER D7738

APPENDIX E

CONTROLLER PARTS LOCATION