MDX SYSTEM
OEM MANUAL

Scientific Micro Systems, Inc.

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APPLICABLE PRODUCT NUMBERS		
Board	PWB. Assy.	Prog. Assy.
FWD0106 Formatter	0004220 Rev. A and up	1002001 Rev. A and up
LSI-11 I/F	0003770 Rev. D and up	1001939 Rev. B and up

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

See section II-M for additional information.

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I. INTRODUCTION

A. PRODUCT LINE OVERVIEW

The MDX system provides power and an enclosure for a light weight, tabletop LSI-11 computer system. It includes an SMS floppy/Winchester disk controller, a choice of 5-1/4" Winchester drives plus a slim-line floppy. The disk controller is fully compatible with the SMS FW line of controllers which provide RX02 emulation for the floppy plus full Winchester support.

The following MDX System models are available:

Model Number	Winchester Capacity (formatted)
MDX01171	5.3 MByte Winchester
MDX01172	10.6 MByte Winchester
MDX01173	15.9 MByte Winchester

Input line voltage is switch selectable to either 115VAC or 230VAC.

The MDX system is also available with the following system options:

Option	Configuration
CPU2/64	LSI-11/2 MSV11-DD (64KB memory) *DLV11-J (4 port serial line unit)
CPU23/128	LSI-11/23 MSV11-LF (128KB memory) *DLV11-J (4 port serial line unit)
CPU23/256	LSI-11/23 MSV11-LK (256KB memory) *DLV11-J (4 port serial line unit)
MEM128	MSV11-LF (additional 128KB memory)
MEM256	MSV11-LK (additional 256KB memory)
SLU4	*DLV11-J (additional serial line unit)

*includes cabling to D-type connectors on rear panel of the MDX chassis.

B. FEATURES

- RX02 interface and command compatible with optional performance improvements
- Complete, high performance DMA controller for 5-1/4" Winchester and slim-line 8" floppy
- Four Quad height (8 dual height) backplane
- Dual height LSI-11 interface board for disk controller
- RX01, RX02, RX03, IBM 3740, IBM 2/2D floppy format compatibility plus additional formats
- Program selectable formats for floppy disks (128, 256, 512, 1024 bytes/sector), and for fixed disks (256, 512 bytes/sector)
- Patented data recovery circuit which requires no adjustments for maximum reliability
- Complete error retry
- Error correction
- Switch selectable input voltage (115VAC or 230VAC)
- Comprehensive self-diagnostics and test commands
- Flaw management for fixed disks
- Supports both physical and logical disk addresses
- Full 22-bit Q bus addressing
- Selectable device register and interrupt vector address
- Bootstrap from both floppy and fixed disk
- Complete RT-11 and RSX-11M Software Support for the extended function and performance mode
- Comprehensive standalone software utility package for disk formatting, backup, copying and system testing.
- Programmable sector interleave and track and head switch offsets on both the floppy and fixed disk drives for maximum performance
- Block reads/writes across cylinder boundaries up to 64K words
- Optimized DMA transfers for minimum bus loading
- Direct transfers to/from memory through 64 word First In, First Out buffer

C. FUNCTIONAL SPECIFICATIONS

Floppy drives supported:	Slim line 8" drives: Shugart SA810/SA860, Tandon TM848-1/TM848-2
Diskette formats:	IBM Diskette 1, 2/2D. DEC RX01, RX02 double density plus program selected bytes/sector of 128, 256, 512 or 1024 on both single and double density.
Fixed drives supported:	Seagate ST400 series and compatible Note: The CMI CM5000 series drives are fully compatible with the ST400 series.
Fixed drive format:	MFM encoding with selectable formats of 256 or 512 bytes/sector
Number of bus registers:	2 (4 addresses)
Register addresses:	Jumper selectable (177170_8, 177172_8 is configured at factory)
Interrupt address:	Jumper selectable (264_8 is configured at factory)
Controller Bus Loading:	All bus connections present 1 DC load and 2.5 AC loads to the bus.
Bus Termination:	Backplane mounted resistors terminate Q-bus in 180 ohm characteristic impedance, which allows the bus to be expanded.
DMA cycle time:	On a read, if reply is asserted within 150 ns of the assertion of DIN, the DMA cycle will complete in 1.0us. On a write, if reply is asserted within 150ns of the assertion of DOUT, the DMA cycle will complete within 1.15us. On Winchester transfers, multiple word bursts (up to 4 max.) are performed, minimizing arbitration overhead.

D. PHYSICAL SPECIFICATIONS

Environmental:

Relative humidity: 20-80% (required by floppy drives)

Operating temperature: 10 to 40 degrees C

Wet bulb and dew point temperatures (i.e. humidity temperature combinations) which cause internal or external condensation are not allowed.

Storage temperature: -20 to 50 degrees C

NOTE: Environmental requirements for floppy disk media may vary. Diskettes should be allowed to reach ambient temperature before formatting, reading or writing.

Electrical:

(See section II-E for detailed power requirements.)

Input: 90-130VAC or 180-260VAC switch selectable

Frequency: 47-63Hz

Maximum current: 5.0A at 115VAC
3.6A at 220VAC

Mechanical:

(See Figure 1 for detailed mechanical information.)

Size: 9.5" wide, 11.2" high, 17.0" deep

Weight: 35 pounds

E. DISK DRIVE DATA

Drive	Unformatted Capacity (MB)	No. Cylinders	No. Heads	Rot. Latency (msec.)	Access Time (msec.)	[1] Data XFR Rate Max.	Avg.
5.3MB Win	6.38	306	2	8.33	85	625	492
10.6MB Win	12.76	306	4	8.33	85	625	492
15.9MB Win	19.14	306	6	8.33	85	625	492
1.2MB Floppy	1.60	77	2	83.30	77	31.25[3]	20[2]
						62.50[4]	49[2]

Notes

[1] Data transfer in KBytes/second. AVG. = Average across track.
[2] Assumes no interleave. A 2:1 interleave (e.g. RX02) would cut average transfer rate by two.
[3] Single density.
[4] Double density.

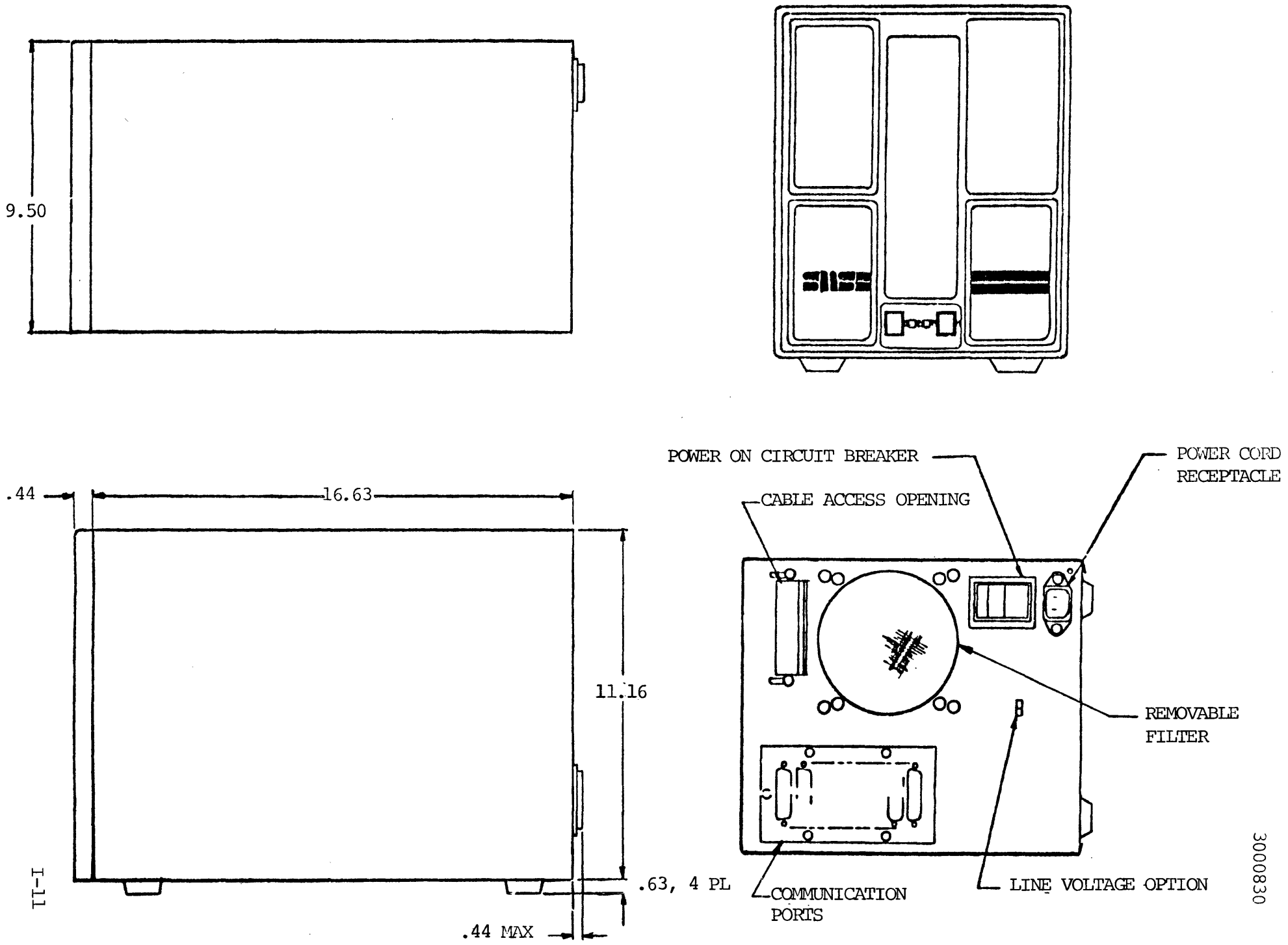


Figure 1. MDX System Enclosure

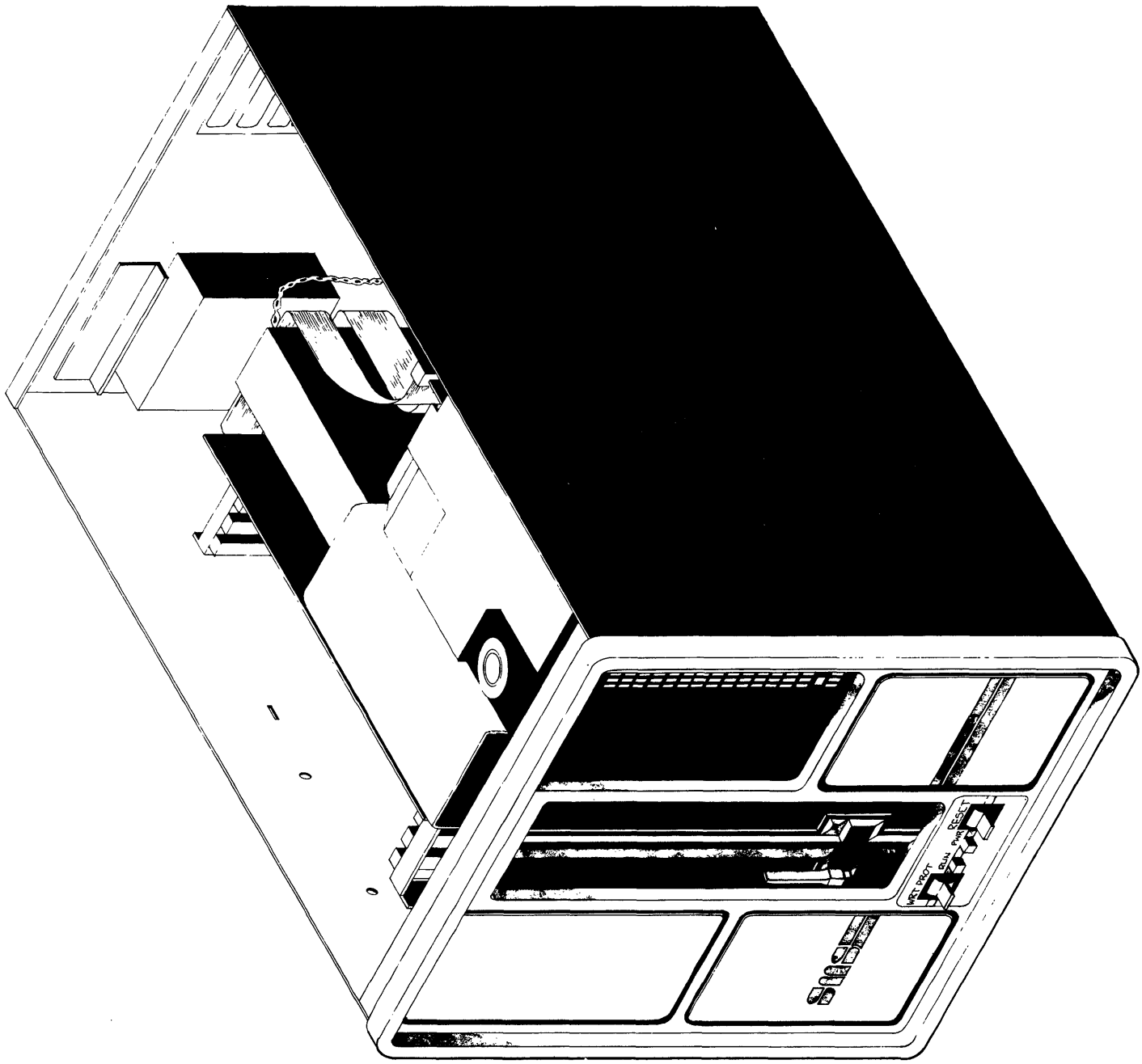


Figure 2. MDX System - Isometric View

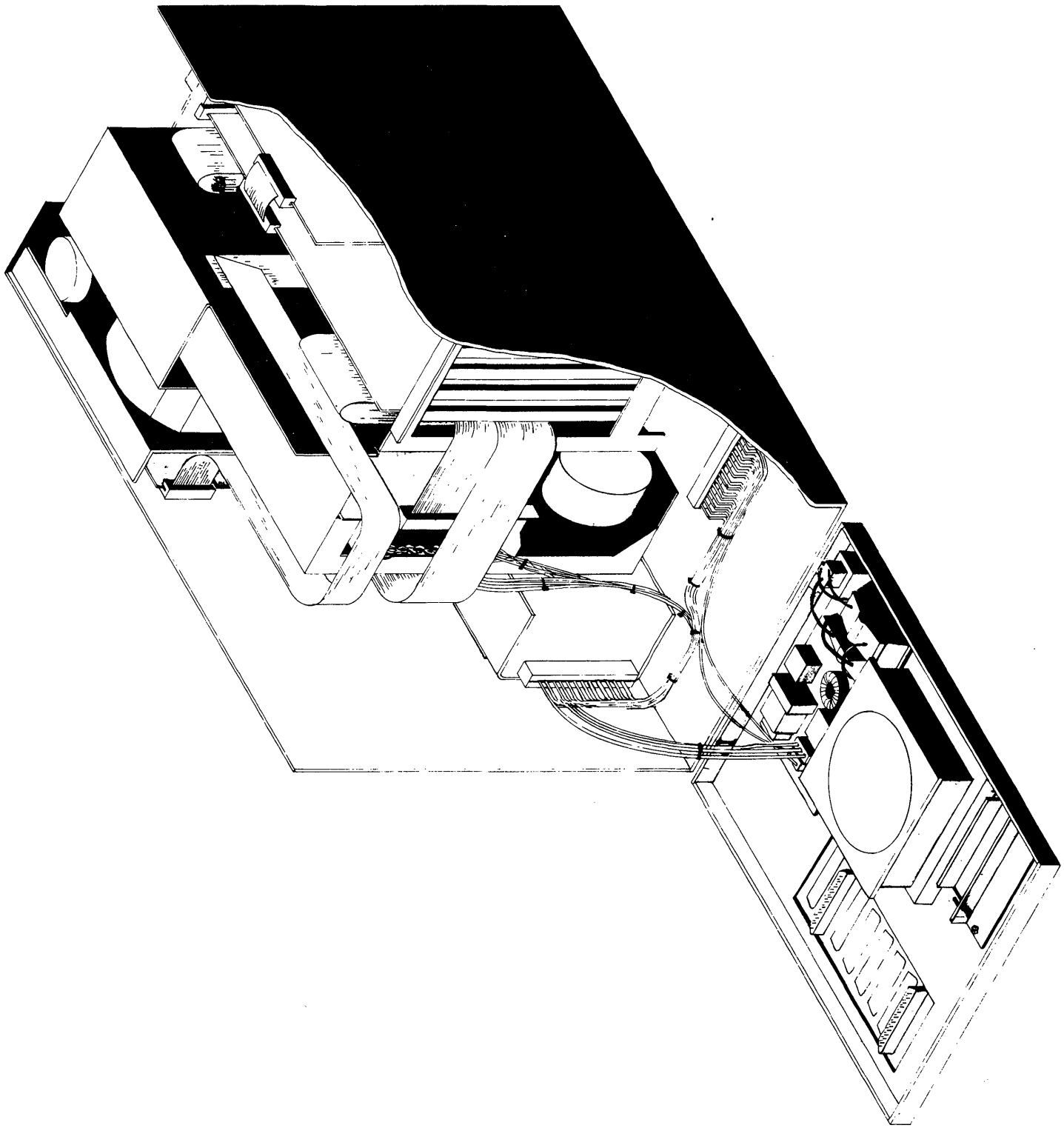


Figure 3. MDX System - Rear Panel Lowered

II. SYSTEM INSTALLATION AND OPERATION

This section of the manual describes how to install, configure, and operate the MDX system. It also describes what options are available in the system and how to select these options.

A. UNPACKING

Examine all shipping containers for evidence of damage prior to unpacking the equipment. If any damage is found, notify an authorized representative of the shipping concern before unpacking the equipment.

No special unpacking instructions are provided since the shipping containers are of a standard type and easily disassembled. All sub-assemblies are adequately protected from normal shocks incurred during shipping.

Visually inspect each assembly in the shipment for damage. Check each item against the packing list to ascertain that all items have been received.

Insure that all boards in the backplane are firmly seated and that all cables are securely in place.

B. SITE SELECTION

The site selected for the MDX System must provide ample space around the unit to allow adequate circulation of cool air and easy maintenance accessibility. Under no circumstances should any cables, walls, or mounting hardware be allowed to restrict air flow to the fan on the rear panel. Proper ac voltage must be provided for the unit as described in the specification section. The normal office environment is adequate for satisfactory operation of the unit.

C. SYSTEM GROUNDING

As shown in the wiring diagram, Figure 8, signal ground is connected to the chassis. The chassis is then connected to the ground wire of the ac input. It is imperative for safety reasons that ground continuity be provided at the customer's installation. This may be accomplished with a three wire installation.

D. POWER ON DELAY

The MDX system has a 15 second delay at power on to allow the Winchester drive to reach operational speed.

E. SYSTEM CONFIGURATION

The MDX System chassis provides support for up to 8 dual wide or 4 quad wide LSI-11 Q-bus compatible pc boards. However, certain precautions must be taken by the customer as he configures his system. This section covers the configuration capabilities and limitations of MDX System.

Power Capacity and Features

The power supply in the MDX is rated at 250 watts. To compute power available to the user, the power taken by the system components (Winchester, floppy, backplane and FWD0106 controller) must be subtracted from the 250 watts. Power available to the backplane for computer modules is as follows:

Total user power: 125 watts

+5V up to 21 amps
+12V up to 2.5 amps
-12V up to .9 amps

Thus any combination of voltages can be used up to a total of 125 watts or to the current limit of the voltage (e.g. 21A at 5V). System component power, including the FWD0106 controller (formatter and interface), take 125 watts.

These voltages are available at all backplane slots on the DEC assigned pins. See backplane logic diagram (Figure 7). The customer must insure that his total system power requirements fall within these limits.

The MDX System backplane provides complete power up sequencing and power fail detection as shown in the backplane logic diagram. At power on, BDCOK is activated once the power supplies are within range. BPOK is activated 70 ms (min) after BDCOK. On power failure BPOK is deactivated a minimum of 4 ms before BDCOK is deactivated (i.e. 4 ms before DC power is out of range). This provides time for the system to gracefully shut down in case of power failure. Note also that battery connections are provided for +5V and +12V for those customers who desire battery backup. See Figure 4.

When the RESET switch, located on the front panel, is depressed the BPOK signal is activated on the Q-bus causing a system wide reset. This provides a convenient method of bootstrapping programs without powering down the system.

System Fuses and Circuit Breakers

The power switch on the rear panel of the MDX system is also a circuit breaker which will trip in the unlikely event of a system AC power overload. In addition the power supply is protected by a 5A, 250V fuse mounted on the power supply itself.

Cooling Capacity

Cooling is available for any reasonable user system from two quad slots to four quad slots. However, certain precautions must be followed to properly configure the system. The MDX System is shipped from the factory with card guides inserted in all slots and baffles inserted in the last two quad slots. If more than 2 quad slots are required, the baffles must be removed from both ends of the cage. Spare baffles are provided in the last 2 slots on the end of the cage away from the fan. In addition the MDX System must be placed where the fans are not blocked by walls or cables and the ambient temperature should be less than 40 degrees centigrade. If this procedure is followed, a minimum of 150 linear feet per minute of 40 degrees C air will be supplied to each board.

Board Location

The MDX backplane consists of 1 quad slot (nearest the slim-line floppy) for the FWD0106 formatter plus four additional Q-Bus quad slots. The LSI-11 CPU must be inserted in the rear dual height slot next to the formatter as shown in Figure 4. The FW interface is installed in the front dual slot next to the formatter. Remaining options (memory, etc.) are installed in the sequence shown in Figure 4. This sequence must be followed to insure the priority chain is not broken. All boards must be installed with components facing the slim-line floppy.

Bus Loading

The MDX backplane can accommodate modules of up to 35 AC loads (total) and 20 DC loads (total). One AC load equals 9.35pF of capacitance and one DC load equals 105 microamperes.

Rules for Configuring the MDX Backplane

- Insure that the total available DC power is sufficient for all modules.
- Insure that no more than 20 DC bus loads and 35 AC bus loads are present.
- Insure that all modules are plugged into consecutive slots as shown in Figure 4. The slots follow an 'S' curve down the bus.
- Insure air baffles are inserted in slots which do not have boards installed.
- Insure that jumpers W1, W2, W3, W4 on the backplane are removed for operation with an LSI-11/2. The LSI-11/2 does not support 22-bit addressing and uses these lines for other purposes. An LSI-11/23 will operate correctly with the jumpers installed or removed, but the jumpers must be installed for full 22-bit addressing.

F. CABLE PROVISIONS

Cabling to external devices is provided by a variety of connector options on the MDX System rear panel. One group of 8 D-type communication connectors are provided with removable covers. The customer may uncover and use as many of these as required by sliding the plastic cover down. Do not uncover any unused connectors as this will disturb air flow for system cooling. In addition to the D connectors, a strain relieved slot is available for up to 50 conductor flat cable. Since one of the cable panels is removable, a small piece of sheet metal may be designed by the customer for any special cable requirements he may have.

The MDX System is designed such that cables may be routed from the top of the boards to the rear panel without restricting air flow to the system. Please exercise care when routing cables. Do not allow excess cable length to block air flow. SMS provides two types of custom cables for use with the DEC DLV11-J communication board to facilitate customer configuration. The first cable is P/N 0003833 as shown in Figure 5. This cable allows direct connection to most terminals. The second cable is P/N 0003784 as shown in Figure 6. This cable allows connection to most modems. The customer may either order these cables from SMS, build them himself, or use them as models to design other special purpose cables.

G. BUS TERMINATION

The MDX System backplane has termination resistors which combine with the resistors on the LSI-11 CPU to terminate the lines in its characteristic impedance. This means that the customer does not have to buy special termination boards. It also means that no board (other than the CPU) which has termination resistors should be inserted into the MDX backplane.

Extension of the Q-bus beyond the MDX System backplane is possible. Please refer to the DEC Microcomputer Processor Handbook for backplane expansion rules.

Note: Very early production models of MDX did not have backplane termination resistors. If you plan on extending the backplane, insure the backplane has termination resistors (RN2, RN3, RN4, RN5) installed or contact SMS for assistance.

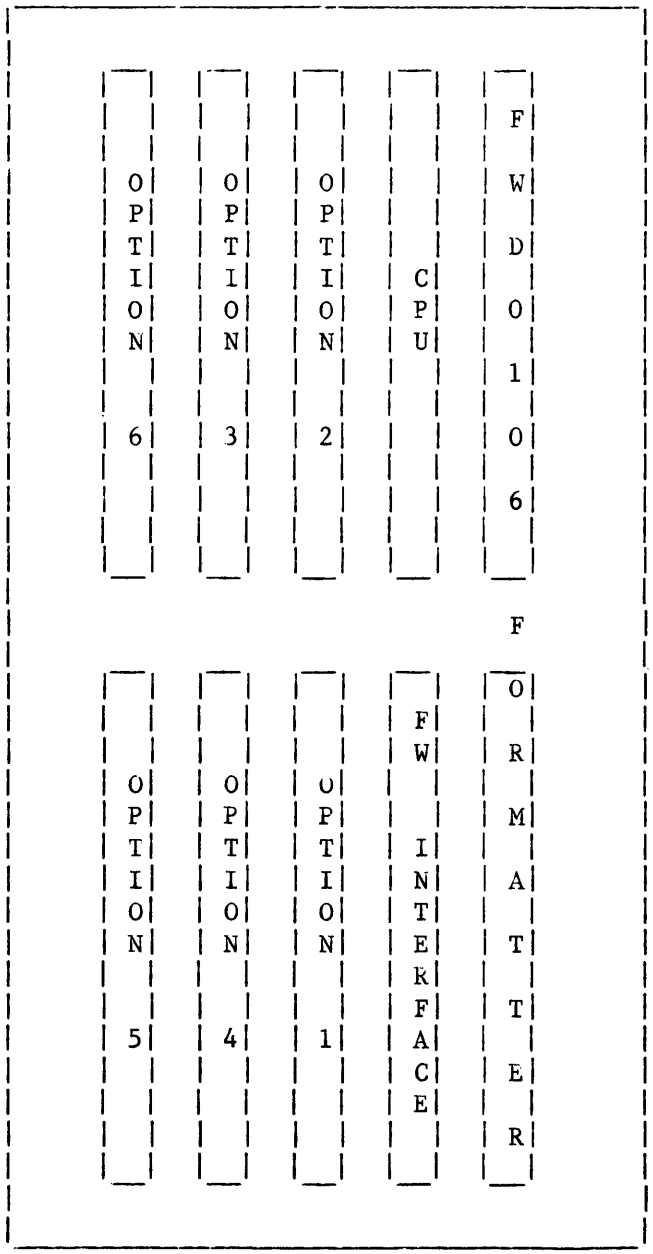
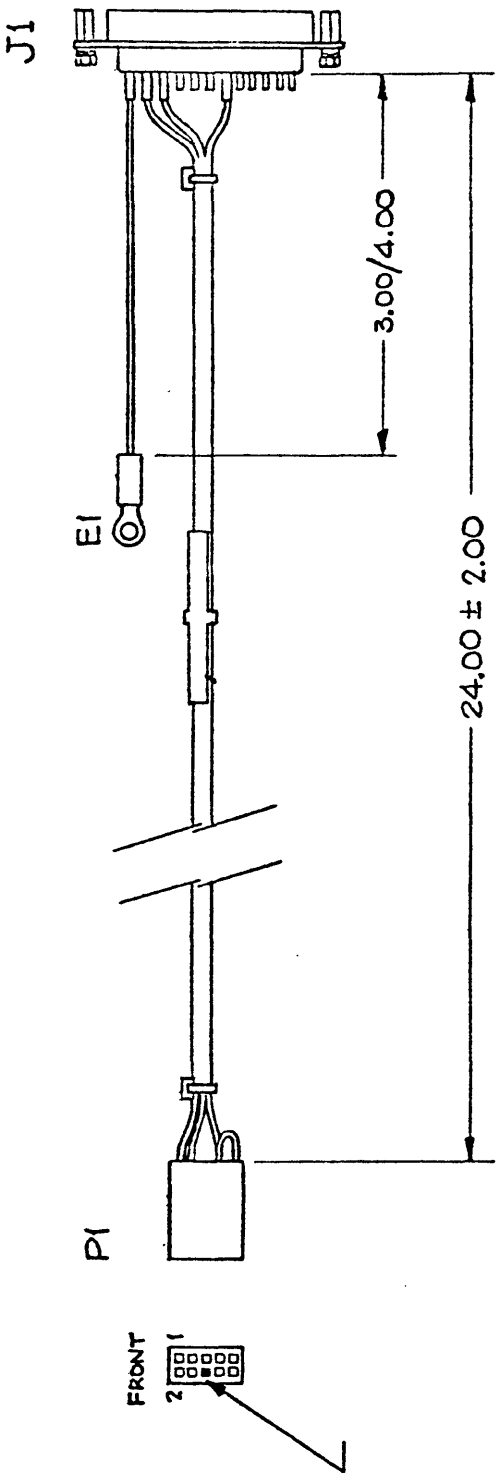


Figure 4. MDX Backplane Layout



WIRE LIST

SIGNAL	FROM	TO	COLOR
SIGNAL GROUND	P1-2	J1-7	GREEN
XMIT DATA	P1-3	J1-3	WHITE
RCV DATA -	P1-7	P1-9	BLACK
RCV DATA +	P1-8	J1-2	RED
PROTECTIVE GND	J1-1	E1	BLACK

Figure 5. Cable Assembly, DLV11-J to Terminal.

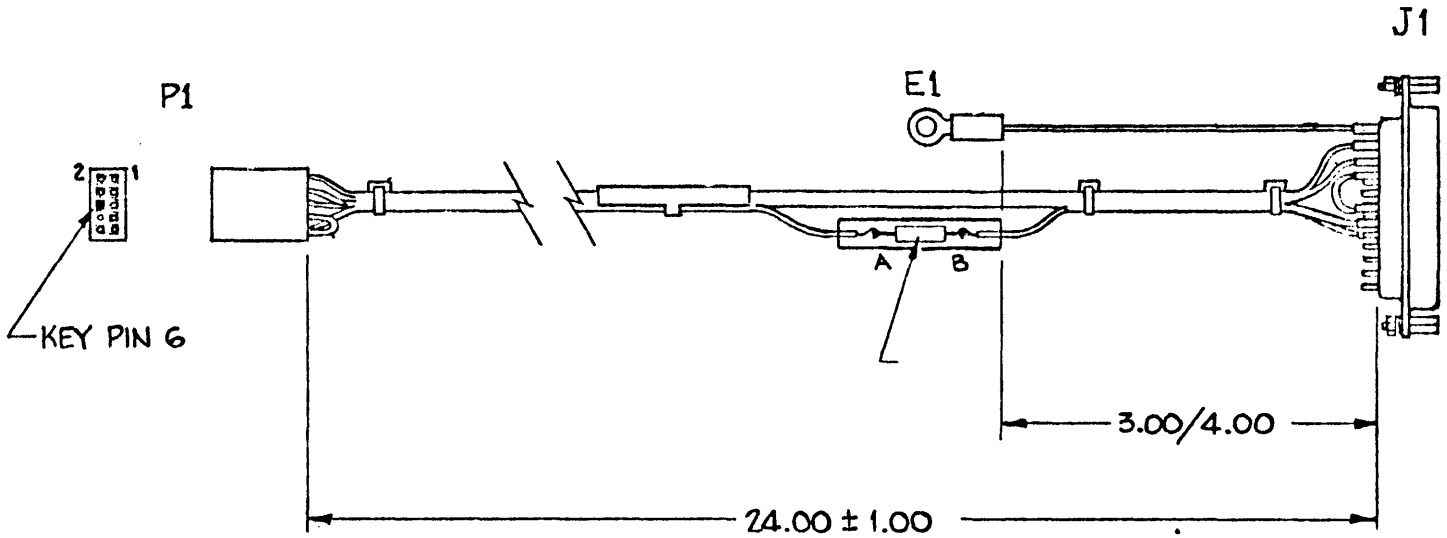


Figure 6. Cable Assembly, DLV11-J to Modem.

WIRE LIST

SIGNAL	FROM	TO	NOTES
SIGNAL GROUND	P1-2	J1-7	BLACK COND.
XMIT DATA	P1-3	J1-2	RED COND.
RCV DATA -	P1-7	P1-9	JUMPER
RCV DATA +	P1-8	J1-3	WHITE COND.
+12VDC FUSED	P1-10	R1-A	GREEN COND.
DTR	R1-B	J1-20	GREEN COND.
RTS/DSR	J1-4	J1-6	JUMPER
PROTECTIVE GROUND	J1-1	E1	CHASSIS GND

H. MDX SYSTEM SWITCHES

AC Power

The AC power switch is located on the left, bottom of the rear panel. This switch is also a circuit breaker which will protect the MDX system in the unlikely event of a short circuit.

Input Voltage Selection

The input voltage range is switch selectable to either 90-130VAC or 180-260VAC. This switch is located on the rear panel and is recessed to prevent accidentally changing it.

** WARNING **

Before applying power, insure this switch is in the correct position. If 220/240VAC power is applied when the switch is in the 115VAC range, the MDX system will be damaged.

External Switches and LED's

There are two switches and two LED indicators on the front of the MDX system. These are:

Reset Switch	This is a momentary switch which, when raised, causes a system wide reset by activating signal BPOK. This provides a method to bootstrap programs.
WRT PROT Switch	When raised, this switch write protects the entire Winchester drive.
PWR LED	When on, this LED indicates power is applied to the MDX.
RUN LED	When on, this LED indicates the CPU is running.
	Note: When the CPU is halted or executing the WAIT instruction, this LED will be off.

Internal Switches and LED's

There are four toggle switches and three LED's located behind the left lower panel on the MDX. To open this hinged panel, pull on the top of it.

The switches are:

Run/Halt	The Run/Halt switch is used to halt the CPU. When the switch is in the RUN position signal BHALTL is not activated and the CPU can run. When the switch is in the HALT position signal BHALTL is activated and the CPU will be halted.

Line Time Clock — When this switch is in the on position the signal BEVNTL is activated every 1/60 second (16.66ms). This can generate an interrupt through the vector at address 100_8 which is often used to keep the time of day.

TEST Switches — These two switches select the type of diagnostic to be run as follows:

TST1	TST2		
C	C		No self test is run
C	O	*	Self test is run once at power on
O	C		Self test is run continuously
O	O		Drive test

* indicates normal operational setting.

See section V for additinal details.

Test LED's — There are three LED's which indicate the result of the self test and drive test. See section V, Tables 9 and 10 for details.

I. SYSTEM STRAP OPTIONS

Certain strap options are provided on both the controller interface board, the controller formatter board, and the backplane itself. These options are factory set to provide the most widely used system; however, the information is presented here to allow for special customer requirements and maintenance.

The interface board strap options are listed in Table 2. Notice that all jumpers must be wirewrapped, because of height restrictions, if they are required.

The formatter board options are listed in Table 1. Factory defaults are indicated with a double asterisk.

TABLE 1. FW FORMATTER STRAPS

STRAP	MEANING	VALUES
W1	OFF-BOARD LED CONTROL	
	INSTALLED	ON BOARD LED'S ARE ENABLED
	** REMOVED	ON BOARD LED'S ARE DISABLED; LED'S ARE OFF BOARD (SECTION V-B).
W2	NUMBER OF WORDS TO TRANSFER PER DMA BURST	
	** REMOVED	4 WORD BURST
	INSTALLED	2 WORD BURST
	NOTE: NORMALLY A 4 WORD BURST IS USED FOR LSI-11 AND A 2 WORD BURST IS USED FOR PDP-11. THIS STRAP MUST BE INSTALLED WHEN THE UNIT IS USED IN A VAX COMPUTER.	
W3	W3 IS A HARDWARE DIAGNOSTIC STRAP AND MUST BE REMOVED.	
W4	FLAW MAP (SEE SECTION VI)	
	REMOVED	NO FLAW IS PRESENT ON WINCHESTER
	** INSTALLED	FLAW IS PRESENT ON WINCHESTER
W5	RESERVED	
W6	POWER UP AND INITIALIZE MODE	
	REMOVED	COMPATIBLE MODE SET ON POWER UP AND BUS INIT.
	** INSTALLED	MODE IS NOT CHANGED ON POWER UP OR BUS INIT.
	NOTE: AFTER POWER ON OR BUS INIT, THE MODE CAN BE PROGRAMMATICALLY CHANGED. ONLY THOSE SYSTEMS WHICH ARE FLOPPY ONLY AND DO NOT USE THE SMS BOOTSTRAP WILL NEED THIS STRAP REMOVED.	
W7-W8	WINCHESTER DRIVE 1 TYPE	7 8
		** C C SAME DRIVE TYPE AS WIN. DRIVE 0
		C O RESERVED
		O C RESERVED
		O O RESERVED
W9-W11	WINCHESTER DRIVE 0 TYPE	9 10 11
		C C C RESERVED
		C C O RESERVED
		C O C ST506, COMPATIBLE
		C O O RESERVED
		O C C ST406, CM5206, COMPATIBLE
		O C O ST412, CM5412, COMPATIBLE
		O O C ST419, CM5619, COMPATIBLE
		O O O RESERVED
W12-W13	W12 AND W13 ARE HARDWARE DIAGNOSTIC STRAPS AND MUST BE REMOVED.	

TABLE 1. FW FORMATTER STRAPS (CONTINUED)

STRAP	MEANING	VALUES
W14	W14 ENABLES THE WRITE OSCILLATOR AND MUST ALWAYS BE INSTALLED.	
W15-W16	PRECOMPENSATION	15 16 C C NOT DEFINED ** C O PRECOMPENSATION ENABLED O C PRECOMPENSATION DISABLED O O NOT DEFINED
W17	WINCHESTER DRIVE 0 WRITE PROTECT (WWP) INSTALLED - NOT WRITE PROTECTED ** REMOVED - WRITE PROTECTED NOTE: W17 MUST BE REMOVED FOR REMOTE CONTROL. SEE SECTION V-B.	
W18-W19 (TST1, TST2)	*SELF TEST *SEE SECTION V-D FOR SELF AND DRIVE TEST DESCRIPTION NOTE: W18 AND W19 MUST BE REMOVED FOR REMOTE CONTROL. SEE SECTION V-B.	TST1,TST2 18 19 C C NO SELF TEST IS RUN C O SELF TEST RUN ONCE AT POWER ON OR INITIALIZATION O C SELF TEST RUN CONTINUOUSLY ** O O DRIVE TEST
W20-W22	FLOPPY TYPE	20 21 22 C C C RESERVED C C O RESERVED C O C SHUGART SA460 C O O MPI 92 O C C RESERVED O C O TANDON TM848-1/TM848-2 O O C TANDON TM100-4 O O O SHUGART SA860/SA810
W23	POWER ON DELAY ** REMOVED - 15 SECONDS INSTALLED - 2 MINUTES	
W24-W29	WHEN INSTALLED, THE THREE DIAGNOSTIC LED SIGNALS AND THREE OPTION STRAP SIGNALS ARE GATED ONTO SIX Q-BUS SPARE LINES. SEE SECTION V-B. THESE STRAPS ARE INSTALLED WITH SHUNTS ON THE PWB. THE USER NEED NOT REMOVE THESE STRAPS UNLESS HE'S INSTALLING THE FORMATTER IN A Q-BUS BACKPLANE THAT BUSES AND USES SSPARE 2,3,6,8 OR MSPAREA,B. NO SMS OR DEC BACKPLANES BUS THESE SIGNALS.	

W30-W31 ARE HARDWARE DIAGNOSTIC STRAPS AND MUST BE REMOVED.

NOTE: ALL FWD0106 STRAPS EXCEPT W17 ARE READ AT POWER ON/INIT TIME. CHANGES IN STRAPPING MUST BE FOLLOWED BY A CONTROLLER INIT. W17 IS READ EACH TIME A WRITE ACCESS TO WO IS PERFORMED.

TABLE 2. LSI-11 FW INTERFACE STRAPS

STRAP NUMBER	MEANING
W1	*BOOT PROM'S DISABLE
	** REMOVED - BOOT PROM'S ARE ENABLED
	INSTALLED - BOOT PROM'S ARE DISABLED, (CONTROLLER WILL NOT RESPOND TO BOOT PROM ADDRESS)
W2, W3	*PARITY CONTROL
	W2 INSTALLED - PARITY ENABLED
	** W3 INSTALLED - PARITY DISABLED
W4 - W9	INTERRUPT PRIORITY

	W4	W5	W6	W7	W8	W9
** BR4	R	R	R	R	I	I
BR5	I	R	I	R	R	I
BR6	I	I	R	I	R	R

NOTE: THE LSI-11 I/F BOARD CANNOT BE CONFIGURED AS A BR7 DEVICE, HOWEVER IT DOES RECOGNIZE OTHER BR7 DEVICES AS SUCH, AND CORRECTLY ARBITRATES INTERRUPTS WHEN BR7 DEVICES ARE PRESENT.

S1 (U42) — INTERRUPT VECTOR SELECTION

REMOVED - 270_8

** INSTALLED - 264_8

S2-S4 (U42) — BOOT PROM'S STARTING ADDRESS

	S2	S3	S4		S2	S3	S4	
	I	I	I	160000_8	R	I	I	164000_8
	I	I	R	171000	R	I	R	175000
	I	R	I	162000	R	R	I	166000
**	I	R	R	173000 (DEFAULT)	R	R	R	177000

S5-S8 (U42) — CONTROLLER COMMAND AND STATUS REGISTER ADDRESS

	S5	S6	S7	S8		S5	S6	S7	S8	
	I	I	I	I	177040_8	R	I	I	I	177240_8
	I	I	I	R	177060	R	I	I	R	177260
	I	I	R	I	177050	R	I	R	I	177250
	I	I	R	R	177070	R	I	R	R	177270
	I	R	I	I	177140	R	R	I	I	177340
	I	R	I	R	177160	R	R	I	R	177360
	I	R	R	I	177150	R	R	R	I	177350
**	I	R	R	R	177170 (DEFAULT)	R	R	R	R	177370

U65 — FOR STRICT COMPATIBILITY WITH 18-BIT BACKPLANES THE COMPONENT (8T38) AT LOCATION U65 (SOCKETED) MAY BE REMOVED. THIS WILL PREVENT THE INTERFACE BOARD FROM ACCESSING THE FOUR EXTRA ADDRESS LINES (BDAL18-BDAL21).

* Wirewrap must be used here or height restrictions will be violated.
** Factory Option

TABLE 3. BACKPLANE STRAPS

STRAP NUMBER	MEANING
W1,W2,W3,W4	EXTENDED ADDRESS LINES (BDAL18L, BDAL19L, BDAL20L, BDAL21L) THESE STRAPS BUS THE EXTENDED ADDRESS LINES FROM THE CPU TO THE REST OF THE BACKPLANE. SINCE THE LSI-11/23 AND LATER CPU'S SOURCE THESE SIGNALS, THE W1 TO W4 STRAPS MUST BE INSTALLED WHEN THESE CPU'S ARE USED WITH MORE THAN 256KB OF MEMORY. HOWEVER THE LSI-11/2 MAKES SPECIAL USE OF THESE LINES AND DOES NOT USE THEM AS ADDRESS LINES. THUS, THE W1 TO W4 STRAPS MUST BE REMOVED WHEN AN LSI-11/2 IS INSTALLED IN THE SYSTEM. SMS SHIPS THE MDX SYSTEM WITH THESE STRAPS INSTALLED.

TABLE 4. WINCHESTER DRIVE OPTIONS

Terminate last drive on cable and install jumpers as shown:

SEAGATE ST506

DRIVE	JUMPERS	
DRIVE 0	Remove shunts 16-1, 13-4, 12-5, 11-6, 10-7.	Install 15-2, 9-8.
DRIVE 1	Remove shunts 16-1, 13-4, 12-5, 11-6, 9-8.	Install 15-2, 10-7.

The Half Step option is selected.

SEAGATE ST400 SERIES

DRIVE	JUMPERS	
DRIVE 0	Remove shunts 16-1, 12-5, 11-6, 10-7.	Install 15-2, 13-4, 9-8.
DRIVE 1	Remove shunts 16-1, 12-5, 11-6, 9-8.	Install 15-2, 13-4, 10-7.

CMI CM5000 SERIES

DRIVE	JUMPERS
DRIVE 0	Install shunt 1-2.
DRIVE 1	Install shunt 3-4.

Note: Except for strapping differences, the CM5000 series drives are fully compatible with the ST400 series.

TABLE 5. FLOPPY DRIVE OPTIONS AND SPECIFICATIONS

Terminate the last drive on the cable and option the drives as shown below:

TANDON TM848-1/TM848-2

The default strapping as shipped by Tandon must be modified as follows:

DRIVE	JUMPERS	
DRIVE 0	Remove B, M1, M2, M3	Install A,X,C,I,R,HL,Z,M4,DS1
DRIVE 1	Remove B, M1, M2, M3	Install A,X,C,I,R,HL,Z,M4,DS2

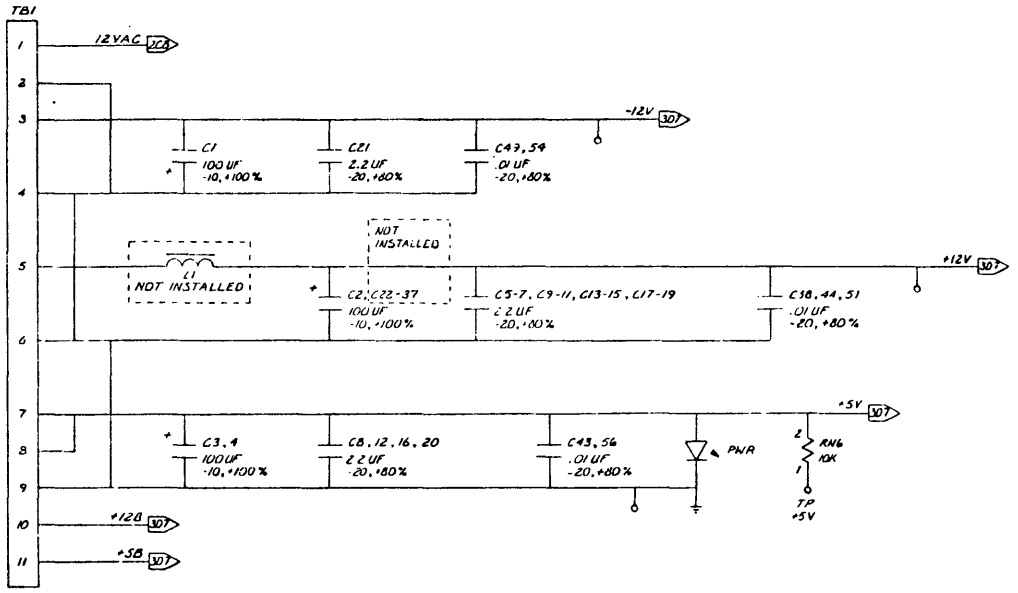
The motor on and stepper power circuits are controlled by Head Load (HL).

SHUGART SA860/SA810

DRIVE	JUMPERS	
DRIVE 0	Remove D,DC,I,MS,PD,S,SE,S1,S3,TS	Install MD,MO,R,SI,S2,TR,2S,DS1
DRIVE 1	Remove D,DC,I,MS,PD,S,SE,S1,S3,TS	Install MD,MO,R,SI,S2,TR,2S,DS2

POWER DISTRIBUTION					
REF. DESIG.	DESCRIPTION	+12V	-12V	+5V	GND
U1	LM2901	3			12
U2	8838			16	7,8,9
U3	LM2901	3	12		
U4	LM2901	3	12		
U5	LM1824	4	11		
U6	75451			8	4

REVISION				
REV LTR		DESCRIPTION	DATE	APPROVAL
A1	A2	PROTOTYPE LAYOUT	15JAN82	[illegible]
A3		REF. DESIG. AND NEW R9,10	22FEB82	[illegible]
A		RELEASE W/ REWORK	28JUN82	[illegible]
B1		NEW PWR FAIL & TERMINATION	03JUN82	[illegible]
B		REVISION PER DCO 3018	04AUG82	[illegible]



0004	0003	0002	0001	DESCRIPTION	SMS PART NUMBER	VENDOR/PART NUMBER	ITEM
QUANTITY PER DASH NUMBER				PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
XX DEC ± .02
XXX DEC ± .010
ANGLES ± ½°
FRACTIONS ±

APPROVALS — DRAWN [illegible] 15JAN82 — CHECK — APPD — APPD — APPD

Scientific Micro Systems, Inc.
MOUNTAIN VIEW CALIFORNIA 94043

MDX-11 BACKPLANE
LOGIC DIAGRAM

DASH NUMBER	PRODUCT	NEXT ASSEMBLY
	MDX-11	
APPLICATION		

SIZE D — DRAWING NUMBER 0004318 — REVISION B
SCALE — SHEET 1 OF 3

Figure 7. MDX System Backplane Logic Diagram (Sheet 1 of 3)

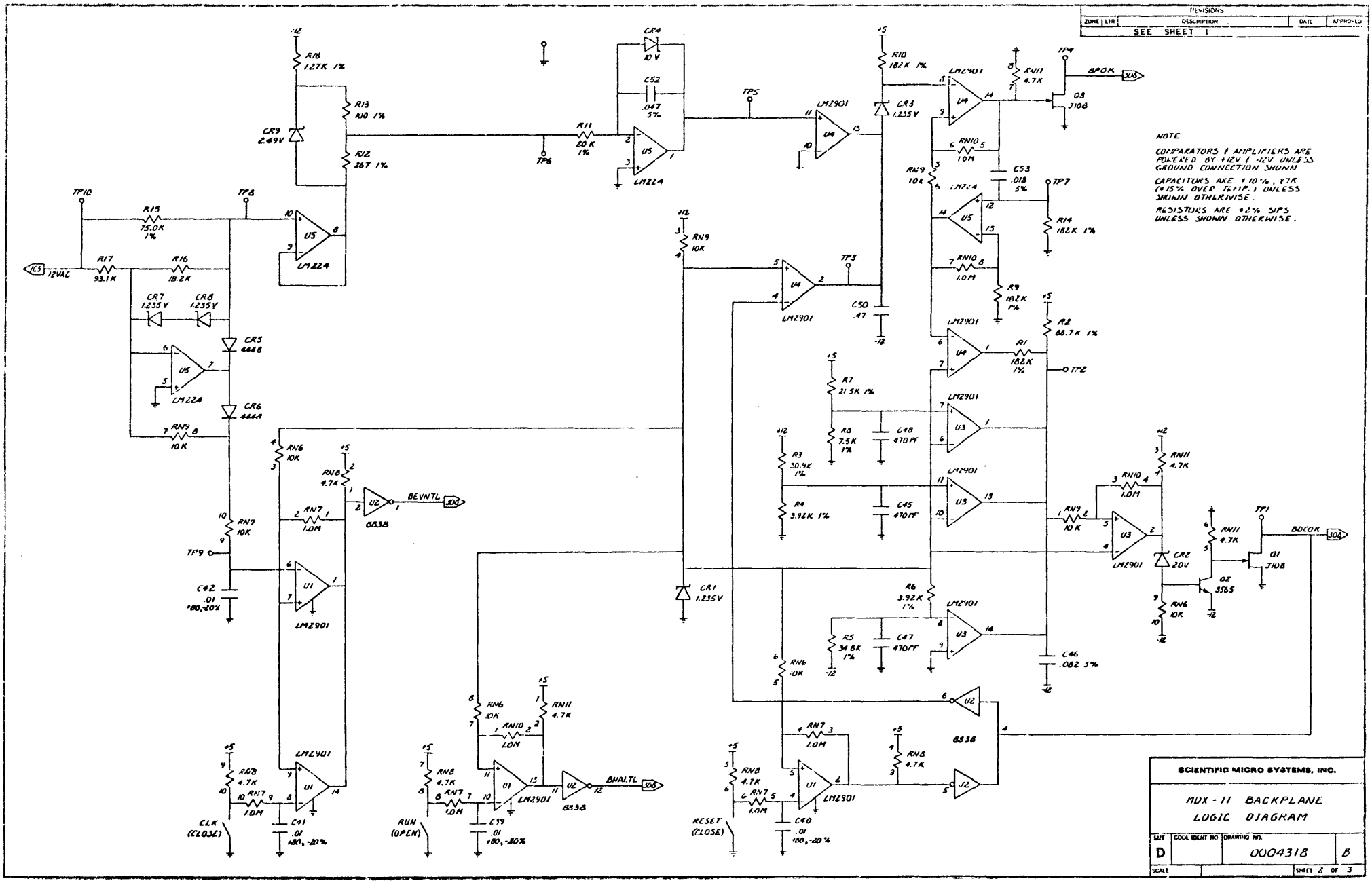


Figure 7. MDX System Backplane Logic Diagram (Sheet 2 of 3)

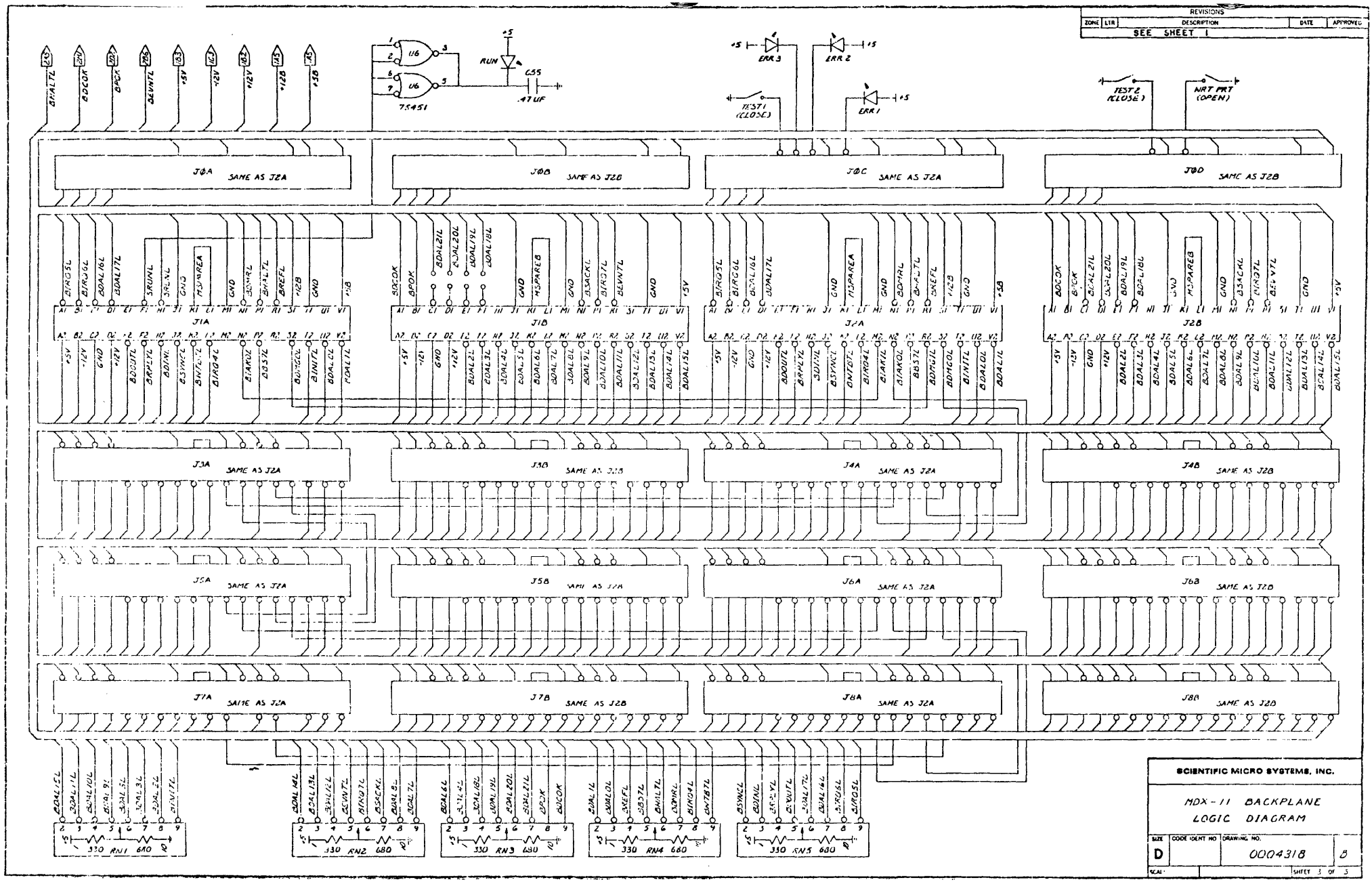


Figure 7. MDX System Backplane Logic Diagram (Sheet 3 of 3)

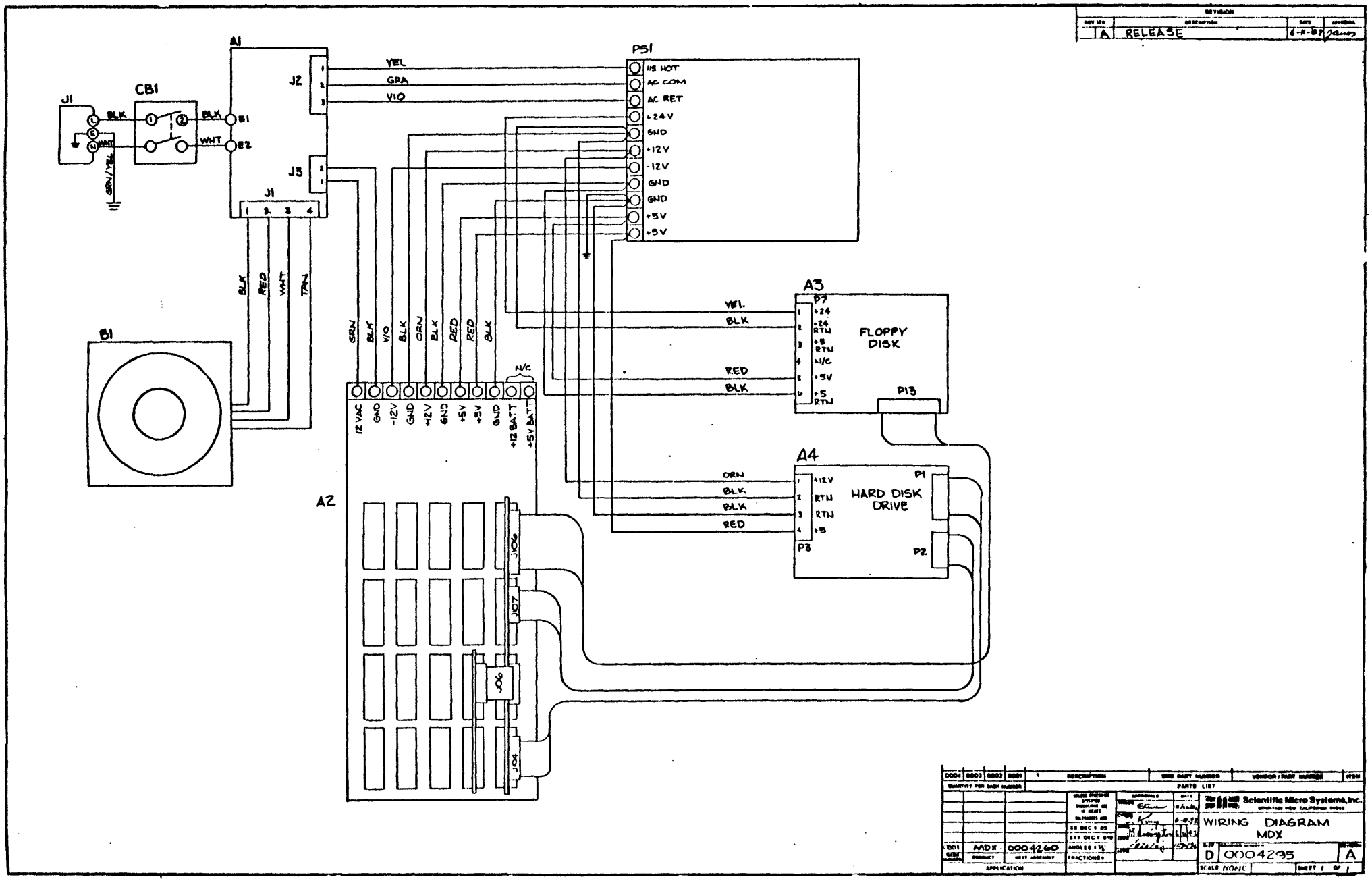


Figure 8. MDX System Wiring Diagram.

J. BOOTSTRAPPING (PROGRAM LOADING FROM DISK)

In order to load a software program from the floppy or Winchester disk, the FW controller provides a bootstrap program. This bootstrap program, plus limited CPU and memory diagnostics, resides in PROMs on the interface board and normally occupies the address range from 773000_8 to 773777_8.

The simplest and most convenient way to start the FW boot program when the CPU is in power-up mode 2 (see the DEC Microcomputer Processor Handbook) is to push the reset button on the front panel of the MDX system. This causes the CPU to start execution at a specified address, typically 773000_8. Another way is to use the console ODT 'G' command.

For example, the FW Installation and Test program can be booted as follows:

CPU in Power-Up Mode 2

1) place diskette in drive 0

2) push Reset

3) wait for the 'DRV?' prompt

4) type F0 (in upper case) to boot from the floppy or W0 to boot from the Winchester

Using Console ODT (Line Time Clock must be off for LSI-11/2 CPU)

1) place diskette in drive 0

2) push the break key on the terminal keyboard (the @ prompt should be printed)

3) type 773000G

4) wait for the 'DRV?' prompt

5) type F0 (in upper case) to boot from the floppy or W0 to boot from the Winchester

The program will then be read from the disk and its execution started.

The basic operation of the boot program is to read 512 words from the first block of the specified drive into host memory, starting at address 0, and then cause the host CPU to start execution at address 0. The program read into memory from the first block of the drive then reads the remainder of the program being booted, and thus is often called the boot block.

In order to allow for different system configurations, there are two entry points for this program -- the base address or the base address plus 20_8. The base address is normally 773000_8 but may be changed or disabled. When the program is started at the base address (using console ODT or LSI-11 power up mode 2) the following functions are executed by it:

1) Exercise host CPU

2) System memory sizing and testing

3) Boot device I/O address is tested

4) A set extended mode command is issued to the controller (if it is not already in extended mode)

5) Bootstrap prompt "DRV?" is written to the console device

6) The user then responds with one of the following (upper case alphanumerics must be used):

F0	floppy drive 0	W0	Winchester drive 0
F1	floppy drive 1	W1	Winchester drive 1

Note that these are logical addresses. The physical address of the drives may be different as shown in Table 4 and 5.

If the operator responds with one of the above prompts before the timeout expires, the controller will attempt to read 512 words from the device starting at host address 0 and disk address sector 1, track 1, head 0 for the floppy, and sector 1, track 0, head 0 for the Winchester. If the read is unsuccessful, or if host address 0 does not contain a NOP after the read, the boot program will halt.

If a successful read was from F0 or F1 and if the format of the diskette is RX01 or RX02, then the controller is issued a set compatible mode command. Host program execution is then started at address 0. It is assumed that the bootstrap block contains a valid program and that it will change the controller's mode if required.

CPU Register

When the bootstrap program, loaded from the first block of the disk, is started, R0 contains the unit number that the bootstrap block was read from:

R0 = 0	floppy drive 0	R0 = 2	Winchester drive 0
R0 = 1	floppy drive 1	R0 = 3	Winchester drive 1

If, after about 5-10 seconds, no response has been entered to the DRV? prompt, the controller will search all drives for a valid bootstrap block. The search order is F0, F1, W0, W1. If, after several minutes of trying, no valid bootstrap block is found, the program will halt to prevent excessive media wear in unattended operations. If a valid bootstrap block is found, it is read into host memory and program execution started just as above.

Note: Typically the controller should be strapped for not setting the mode at power up. This allows extended mode operation -- including bootstrap from the Winchester -- as well as bootstrap of standard DEC software from the floppy.

The bootstrap and diagnostic program is started at the second entry point when the default I/O addresses are to be overridden. The second entry assumes:

Memory Address	Contents
0	FW controller base address (default 177170_8)
2	DLV11 base address (default 177560_8)
4	0 for normal drive searching as above. No drive searching is done if this word is non-zero. This word contains the unit designator word described in section IV-F. This allows bootstrapping from any unit in any format.

Error Reporting

The bootstrap program reports all errors, either by halting or by waiting indefinitely for an event to occur. The program counter (PC) value thus indicates what the error is. Table 6 details the various error stops.

TABLE 6-A. BOOTSTRAP PROGRAM HALT LOCATIONS

Note: All of the following addresses are relative to the base address of the bootstrap program. Normally the base address of the bootstrap program is 173000$_8$.

Relative Address	Error
0-150	Host CPU Failure
142 or 650	Enter Compatible Mode Failed*
166	Fill Buffer Command failed
220	Empty Buffer Command failed
246	Memory Test failed on write of all 1's. R2 points to failed location.
256	Memory test failed on write of all 0's. R2 points to to failed location.
252 or 356	Enter Extended Mode failed
326	Memory Access error at controller CSR address (i.e., could not read CSR)
452	No valid bootstrap block could be found

* Possible CPU failure, however more probable that a controller error occurred.

TABLE 6-B. BOOTSTRAP PROGRAM HANG LOCATIONS

If the boot program does not start after waiting about 30 seconds, push the break key to determine the 'hang' location. Typically these errors indicate faulty system configurations and/or controller problems.

Relative Address	Error
24-34	Waiting for TR, Done or Error to be set on CSR
54-60	Waiting for Done or Error to be set in CSR
314-320	Waiting for Done to be set after a RESET
650-660	Waiting for TR, Done or Error to be set in CSR
666-672	Waiting for Done or Error to be set in CSR

K. OPERATION WITH THE WINCHESTER DRIVE

The Winchester drive is a simple and very reliable device. It does not require any normal preventive maintenance, however a few precautions must be taken when power is first applied.

1) All Winchester drives require a period of time to reach operational speed. When the drive is at speed, it outputs a signal called Ready and will allow disk accesses to take place. The MDX has an internal 15 second delay to allow drives to reach speed.

2) When first applying power, the drive may be cold. As the drive warms up, some thermal expansion will take place. As a result, it is recommended that the drive not be formatted or written to until after AC power has been applied for two minutes. The FWD0106 has a strap which will force a two minute wait at power on if desired. See Table 1.

L. ENABLING 22-BIT ADDRESSING

To enable 22-bit addressing four jumpers on the backplane, W1 to W4, must be installed. See Table 3 for additional details.

M. MEETING FCC RULES AND REGULATIONS

SMS has conducted testing to insure that the MDX chassis complies with the limits for a Class A device. This testing was done on a MDX01172 (floppy, Seagate ST412 Winchester) with an LSI-11/23 CPU, DLV11-J and 128KW of memory.

The addition of other components to the system such as additional peripherals (line printer, mag tape, etc.) may alter the radiation characteristics of the chassis, especialy if I/O cables are needed to connect the peripherals to the MDX chassis. It is the system integrator's responsibility to insure that the addition of other components to the MDX does not cause the entire system to exceed the FCC Class A limits.

III. DISK SURFACE MANAGEMENT AND FORMATS

A. DISK SURFACE LAYOUT

The surface of a disk (both floppy and fixed) is divided into a series of concentric circles. Each one of these circles is called a track. As the disk rotates, a track passes under a read/write head which is used to transfer information from/to the disk. Many disk drives support multiple read/write heads, all of which are mounted on a single carriage. The carriage moves or positions the heads over the disk surface. On drives which support multiple heads, all tracks which can be accessed from one position of the carriage are called a cylinder. Thus a cylinder consists of 1 to N tracks where N is the number of read/write heads mounted on the carriage. The concept of cylinders is important because switching from one head to another is very fast when compared to physically moving the carriage.

Each track is divided into several records called sectors. The sectors are numbered from 1 to X where X is the number of sectors per track. The number of sectors per cylinder is thus X times the number of heads. All sectors on one cylinder are of the same size.

B. DISK SURFACE ADDRESSING

The surface of either the floppy or fixed disk can be accessed using either a physical address or a logical address.

A physical address is one which specifies a sector position by naming the head, cylinder and sector number. Note that the head number specifies a track within the cylinder. Note also that cylinder and head numbering starts at zero while sector numbering starts at one.

A logical address is one which specifies a sector position by using a logical sector number only. When logical addressing is used, the storage area can be viewed as sequential series of sectors on the entire disk. The advantage of using logical addressing is that it is independent of disk flaws and interleave factors. For example, if logical sector K is read, then the next logical record is K+1 even though physically it may not be on the same cylinder as sector K.

Logical addressing starts with logical record one for both the floppy and Winchester drives. However logical record one is equivalent to cylinder 1, head 0, sector 1 for the floppy (i.e. logical addresses start at cylinder 1, not cylinder 0 for the floppies), and equivalent to cylinder 0, head 0, sector 1 on the Winchester assuming there are no flaws.

If the Winchester has flaws then logical record 1 will be the first non-flawed sector on the disk.

Cylinder 0 on the floppies can be accessed using physical addressing only.

C. SECTOR INTERLEAVING

When sector interleaving is used, consecutive sectors on a disk are never read or written. Interleaving typically does not affect disk storage capacity, but does affect system throughput and performance.

Interleaving is used to simplify controller design and/or reduce the effective data transfer rate. Interleaving can be accomplished logically by host or controller software, or physically when the disk is formatted.

The DEC RX02 system uses a logical 2:1 interleave. The interleave is accomplished by the device handler (i.e. DY.MAC in RT-11 and RSX-11M). The interleave is required because the DEC RX02 controller cannot read/write more than one sector at a time. The time gained by skipping a sector is used to process the status from the previous command and issue the next command. Conversely, some IBM systems use physical interleaving.

The controller does not require any interleave. In order to be compatible with other systems and allow reduced data rates, a physical interleave can be specified when either the fixed or floppy disk is formatted.

When interleaving is used, any physical offset (see next section) and interleave are not additive. The number of sectors skipped is the greater of the offset and interleave factor.

D. CYLINDER OFFSET

Cylinder offsetting is a technique used to improve system performance on transfers crossing cylinder boundaries.

To understand how cylinder offsetting works it is necessary to look at the timing constraints of a disk drive. A disk drive can take from 10 to 20 msec to move a read/write head from one cylinder to the next. If a transfer is taking place such that the last sector on track X has just been read and the next sector to be read is the first sector on track X+1, it is desirable to be able to read this sector as soon as the head has been positioned over track X+1. Typically this is not possible because step time is greater than the delay provided by the disk rotation. Thus the controller must wait an entire rotation (200 msec for 5-1/4" floppies) before the desired sector can be read.

This product provides offsets on both the fixed and floppy disks to improve system performance. The offset for the floppy can be either a physical offset done at format time, or a logical offset selected programmatically when the data is read or written. When using logical offset and/or interleave, the data must be read and written using the same offset/interleave.

E. FLOPPY DISK TRACK FORMATS

All formats are 'soft-sectored'. This means that the position of each sector on a track is marked by the controller writing a special pattern, called an address mark (AM), on the diskette. The address mark, along with other identification data (track, head, sector and format), is written only when the diskette is formatted. In normal reads/writes only the data, data address mark and data CRC bytes are written.

It is important to distinguish between what 'formatting' a diskette means versus how the data is arranged on the diskette. Format implies what the encoding type is, what address marks are used and how many bytes per sector there are. On the other hand, data can be arranged on the diskette using various interleave and offset factors.

8" Floppy Diskette Formats

1) IBM Single Density
2) DEC Double Density
3) IBM Double Density

IBM single density is physically equivalent to DEC RX01 single density. However DEC RX01 also implies a 2:1 interleave and 6 sector offset. The IBM single density format implies frequency modulation (FM) encoding and single byte address marks.

The IBM double density format implies Modified Frequency Modulation (MFM) and four byte address marks.

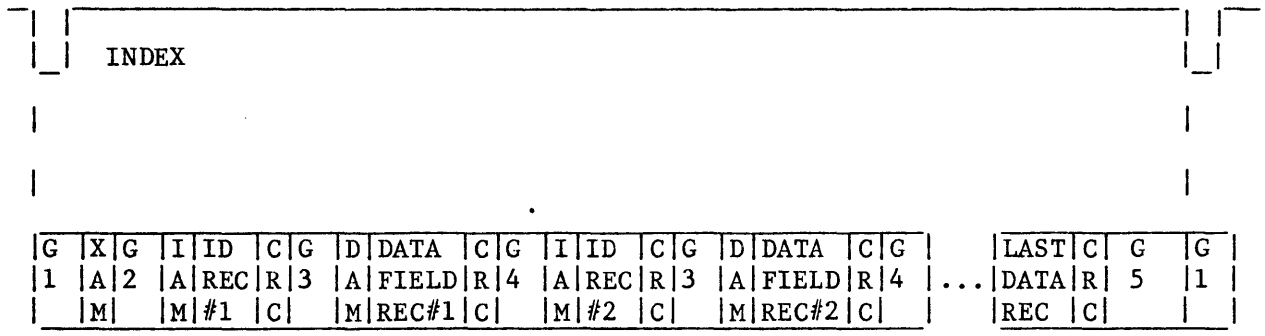
The DEC RX02 double density format uses FM encoding for the identification field (i.e. the ID's written at format time are identical to IBM single density, 128 bytes/sector) and a slightly modified MFM for the data fields. DEC RX02 also implies a 2:1 interleave and 6 sector offset.

The IBM formats have one other important feature -- the format of the first track is constant regardless of the format of the remainder of the diskette. The format for cylinder 0, head 0 is IBM single density, 128 bytes/sector. If the diskette is double sided cylinder 0, head 1 can be one of two formats only. These are single density, 128 bytes/sector if the remainder of the diskette is single density or double density, 256 bytes/sector if the remainder of the diskette is double density.

The following table summarizes the characteristics of the supported 8" floppy formats:

Density	Encoding	Bytes/ Sect.	Sect./ Track	Gap 4	Gap 5	Implied Data Arrangement
IBM SD	FM	128	26	33	274	None
		256	15	48	212	
		512	8	72	313	
		1024	4	86	667	
DEC SD (RX01)	FM	128	26	33	274	2:1 sector interleave, 6 sector offset
IBM DD	MFM	128	44	50	277	None
		256	26	66	653	
		512	16	61	352	
		1024	8	128	771	
DEC DD (RX02)	FM, Modified MFM	256	26	33	274	2:1 sector interleave, 6 sector offset

The arrangement of sectors, ID, etc. on each floppy track is shown below:



where G1 to G5 is GAP1 to GAP5
XAM is Index Address Mark (1 byte in single density,4 in double density)
IAM is ID Address Mark (1 byte in single density, 4 in double density)
ID REC is ID Record (4 bytes)
DAM is Data address mark (1 byte in single density, 4 in double density)
CRC is Cyclic Redundancy Check (2 bytes)
Gaps 1,2 and 3 are fixed and have the following values:

	Gap 1	Gap 2	Gap 3
IBM Single Density/RX02 Double Density	46	32	17
IBM Double Density	92	62	34

Gaps 4 and 5 vary depending on the diskette format and drive tolerance.

The nominal values for these gaps are shown above.

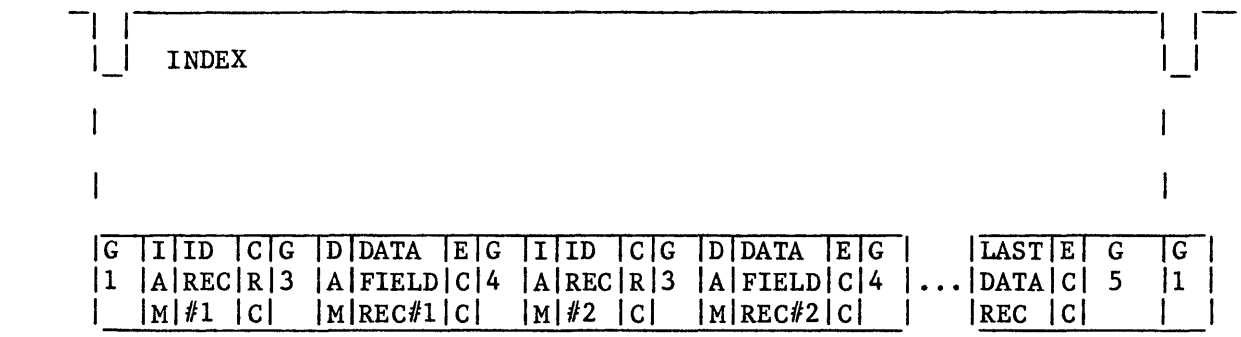
Each ID record consists of 4 bytes in the following format:

TRACK	where format* 0 = 128 bytes/sector
SIDE	or
	DEC double density 256 bytes/sector
SECTOR	1 = IBM 256 bytes/sector
	2 = IBM 512 bytes/sector
FORMAT	3 = IBM 1024 bytes/sector

*Note: Different data address marks are used to distinguish between DEC single and double density.

F. FIXED DISK TRACK FORMAT

The Winchester drives are soft sectored with a track format similar to the floppy disk. Gap 1 immediately precedes the ID address mark for sector 1. It should also be noted that the 2 byte data CRC which is used on the floppy disk is replaced with a 4 byte data ECC capable of detecting all 17 bit (or fewer) burst errors, and correcting all 6 bit (or fewer) burst errors. The arrangement of sectors, ID, etc., on each track is shown below:



where G1 to G5 is GAP1 to GAP5
IAM is ID Address Mark (2 bytes)
ID REC is ID Record (3 bytes)
DAM is Data address mark (1 byte)
CRC is Cyclic Redundancy Check (2 bytes)
ECC is Error Correction Code (4 bytes)
Gap 1 is fixed at 16 bytes (includes sync bytes which precede AM)
Gap 3 is fixed at 11 bytes (includes sync bytes which precede AM)
Gap 4 and Gap 5 depend on format (see Table 7).

Each ID record consists of 3 bytes in the following format:

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
C9	C8	FM1	FM0	H3	H2	H1	H0
S7	S6	S5	S4	S3	S2	S1	S0

where C9-C0 = the cylinder address
FM1-FM0 = the format field
00 = 256 bytes/sector
01 = 512 bytes/sector
H3-H0 = head address
S7-S0 = sector address

Since there is no clock track on the Winchester, rotational velocity variation, caused by drive tolerances and DC power fluctuation, will result in changes in the gap size after the data has been overwritten.

TABLE 7. WINCHESTER FORMAT SELECTION

BYTES/ SEC.	SEC./ TRACK	GAP 4 '00'	GAP 5 '4E'	SI	SL	SPEED TOLERANCE
256	33	19	205	2	01	+1%; with 2:1 interleave*
512	17	56	221	1	10	+1%; no interleave required

SI,SL The sector interleave (SI) and sector length (SL) are specified in the disk format descriptor parameter when the disk is formatted. See section IV-F, Disk Format Designator for Winchester drives.

*Note: A 2:1 interleave is required because gap 4 is not large enough to compensate for the 50us write to read recovery time specification of most supported drives.

TABLE 8. WINCHESTER FORMATTED CAPACITIES

ST506/ST400

			Formatted Capacity (MBytes)			
			ST506	ST406	ST412	ST419
Bytes/ Sector	Sectors/ Track	Track Capacity	4 Hds. 153 Cyls.	2 HDS. 306 Cyls.	4 Hds. 306 Cyls.	6 HDS. 306 Cyls.
256	33	8448	5.1	5.1	10.3	15.4
512	17	8704	5.3	5.3	10.6	15.9

G. ERROR DETECTION AND CORRECTION

Both error detection and correction are widely used in computer memory systems to increase the reliability of the computer systems. Error detection and correction both involve recording redundant information. In the case of error detection, the redundant information is used to detect errors. With error correction the information is used to detect and, if possible, correct errors.

The FWD0106 floppy formats use the popular CCITT CRC polynomial to maintain strict IBM compatibility. This polynomial, supporting error detection only, can detect all error bursts < 17 bits in length.

The FWD0106 Winchester formats support both error detection and error correction with a 32 bit computer generated code which can correct any error burst up to 6 bits in length and detect any single error burst up to 17 bits in length. It also is guaranteed to detect all dual error bursts of ≤ 2 bits. In order to minimize the miscorrection probability even further, error correction is not attempted until the ECC residue is identical for two successive reads. (See section IV-A, Error Correction Policy, for details.) The error correction code has been carefully designed to allow both correction and detection in normal use. However, the use of error correction does not eliminate the need for flaw mapping sectors with known flaws. This is so because if a second hard error were to develop on a sector with a flaw, then the probability of detecting and correcting this second error is significantly lower than detecting and correcting it on a sector with no flaws. Systems which use both flaw mapping and error correction will show increased reliability over those which do not use these features.

IV. PROGRAMMER'S GUIDE

A. MODES OF OPERATION

In order to be either compatible with DEC software, or, alternately, to offer enhanced performance and capacity, the controller may be operated in one of two modes. These modes are the RX02 compatible mode and the extended mode.

RX02 Compatible Mode

In this mode the controller is compatible with the DEC RX02 floppy family, including RX01 and RX02 format compatibility. When the controller is operated in the compatible mode, the following features are offered over the DEC RX02 system.

- on board bootstrap and diagnostics
- write protection on selected diskettes
- choice of 8" DC floppy disk drives and 5-1/4" DC floppy disk drives
- drive activity light
- a faster buffer/memory DMA rate
- controller boards only for OEM packaging (FWD line)

Extended Mode

The extended mode of the controller is its most powerful and useful mode. This mode offers significant functional and performance advantages over the DEC RX02 floppy disk system plus access to a fixed Winchester disk drive using a common software handler. The same device registers are used to access both the floppy and fixed drives.

Extended mode offers the following advantages over the compatible mode.

- Double density formats (all sector sizes)
- access to Winchester fixed disks and floppy disks
- direct transfers from/to host memory to/from the floppy and fixed disks
- block reads/writes of multiple sectors across cylinder boundaries
- programmable sector interleave plus cylinder offset for maximum performance on both floppy and fixed disks
- RX01/RX02 formats (DY handler compatible)
- error retry is accomplished by the controller, not the host
- full 22-bit addressing
- diagnostic commands

In this mode the command set of the controller is expanded to add eight commands and thus allow significant functional and performance increases. For example, in the extended mode direct transfers from memory to the disk (or from the disk to memory) are possible. These transfers are done through a 64 word first-in, first-out (FIFO) buffer and occur at the transfer rate of the disk. The eight commands are added by including the Unit Select bit in the Command and Status register in the function field. The unit number is passed as a parameter via the data buffer register just as other parameters are passed. The additional functions are listed in section IV-G.

The host firmware can cause the controller to enter the extended mode by issuing a Set Media Density command with a parameter of ASCII "SE" (octal pattern of 51505) instead of an ASCII "I". The host can return to the compatible mode by using the command with the parameter "EC" (octal pattern of 42503) or by setting the initialize bit in the Command and Status Register.

At power on the controller can be forced to compatible mode by correctly programming the extended/compatible mode strap (see Table 1).

Error Retry Policy

During the execution of a command in the extended mode, if an error is encountered, the controller will retry the command if the error falls into the optionally retriable class and the host has enabled retries by setting the retry bit in the unit designator word (see section IV-F). The retry policy is the same for both the floppy and Winchester drives.

The optionally retriable errors are divided into two classes -- class 1 and class 2.

The class 1 errors are retried only twice and the retry policy is:

1) seek to cylinder 0
2) seek to the desired cylinder
3) re-execute the command.

Class 1 errors:

1) head positioning
2) no address marks found on track
3) sector ID not found

The class 2 errors are retried eight times. The retry policy is to simply retry the operation on the sector that caused the error. Class 2 errors are:

1) data CRC/ECC check (and/or correction) failed
2) missing data address mark
3) data late

Whenever retries are attempted during the execution of a command, the retry bit is set in the Error and Status Word (see section IV-F) regardless of the success or failure of the retry. This alerts the host to potential media or hardware problems.

Error Correction Policy

If Error Correction is enabled on a Winchester read command then error correction on data field read errors will be attempted. However, error correction is not attempted until the ECC residue is identical for two successive reads. This insures error correction is not attempted on soft errors and thus decreases the probability of miscorrection.

If, when error correction is attempted, the error is not correctable, up to eight retries and correction attempts are made before an error is reported.

B. HOST/CONTROLLER PROTOCOL

Because of the nature of the system design, certain protocols must be followed in order to insure error free exchange of information between the host (e.g. LSI-11) and the controller. Note that the FWD0106 does not support the overlapped seek protocol available in the FWD0101 series of controllers.

RX02 Protocol

1. Issue and initiate a function by writing the function (plus parameters as required) into the CSR register with the GO bit set. Setting the GO bit results in the Done and the Error bits being cleared. The CSR can be written only when the Done bit is set (i.e. controller not busy).

   NOTE: Because the CSR contains some write only bits the bit set and bit clear instruction should not be used when accessing this register (e.g. a bit set of the function field followed by a bit set of the GO bit will not work correctly).

2. Wait for either the command to complete (Done set) or the TR bit in CSR to be set.

3. If TR is set, then write the required parameter to DBR and go to step 2. Note that writing a parameter into DBR clears TR.

4. When the command completes (Done Set) read status from DBR.

C. CONTROLLER REGISTERS

The controller is programmed by using two device registers:

1) Command and Status Registers (CSR)
2) Multipurpose Data Register (DBR)

The CSR register is normally assigned a bus address of 177170_8 while the DBR register address is 177172_8. However these addresses are jumper selectable and can be changed.

The interrupt vector address is normally 264_8. This address may also be changed using jumpers.

In the compatible mode, the CSR and DBR registers are identical to the RX02 registers RX2CS and RX2DB.

The multipurpose data register is used to pass additional command information, such as track number, from the host computer to the controller. This register can be thought of as either one physical register which is used to emulate several logical registers inside the controller, or as a data buffer used to pass parameters (track, sector, etc.) to the controller. In this document the latter concept is used.

D. REGISTER DESCRIPTION FOR COMPATIBLE MODE

Command and Status Register (CSR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ER	IN	EA	EA	RX	R	SS	DS	TR	IE	DN	US	FN	FN	FN	GO

Field Mnemonic (bit)	Description
ER (15)	Error Indicator. This bit is set when an error has been detected during the execution of a command. It is cleared by issuing a new command or by setting the initialize (IN) bit. This is a read only bit.
IN (14)	Initialize. This is a write only bit which can be set under software control to initialize the controller without affecting any other device on the bus. The following functions are performed when this bit is set: 1) Done is cleared when IN is set; done is set when all initialize functions have been completed. 2) All heads are marked as unregistered. Registration will occur on the first access. 3) Self test is executed according to switch setting (see Table 1). 4) Track 1, sector 1 on drive 0 is read into the buffer. 5) The CSR and DBR are updated.
EA (12,13)	Extended Address. These write only bits indicate an 18 bit extended bus address. Bit 13 is the most significant bit.
RX (11)	RX02 Identification bit. In compatible mode, this read only bit is always set to indicate the controller is emulating RX02 protocol. The controller does not emulate RX01 hardware protocol.
SS (9)	Side Select. For 8" floppy drives this bit is used to select the diskette side (0=side 0, 1=side 1). It is unused and must be written as a zero for 5-1/4" floppies.
R (10)	Reserved (must be written as a zero).

DS (8) Data Density. This read/write bit is readable only when Done is set at which time it indicates the density of the data of the previous command. When it is written it specifies the data density of the command to be executed. When the bit is set, RX02 format is selected. When it is clear, RX01 format is selected.

TR (7) Transfer Request. This read only bit indicates the host may write the data buffer register (DBR) when it is set.

IE (6) Interrupt Enable. This bit enables interrupts. This read/write bit is cleared when an initialize is done (bit 14=1) or by software.

NOTE: When Done is set and this bit changes from a 0 to a 1, the controller generates a host interrupt. If interrupts are enabled and the Go bit is set at the same time, an interrupt will be generated only when the command completes.

DN (5) Done. When Done is set (DN=1), this read only bit indicates the completion of a function. If Interrupt Enable is set, Done will generate an interrupt when asserted.

US (4) Unit Select. This field selects the desired disk. This read/write bit is readable when DN=1.

FN (1-3) Function Field. These bits determine the function to be executed. The Codes/Functions for these write only fields are listed below:

Code	Function
000	Fill Buffer
001	Empty Buffer
010	Write Sector
011	Read Sector
100	Set Media Density
101	Maintenance Read Status
110	Write Deleted Data Sector
111	Read Error Code

GO (0) Go. When GO=1, this write only bit will start the command.

Multipurpose Data Register (DBR)

Parameter: Track Address

Format:
```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-- N O T   U S E D -->  0  <--- T R A C K --->
```

Description: This parameter specifies which tracks (0-76) will be addressed by a given function. Bits 8-15 are unused.

Parameter: Sector Address

Format:
```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-- N O T   U S E D -->  0  0  0  <--SECTOR--->
```

Description: This parameter specifies which sector (1-26) will be addressed by a given function. Bits 8-15 are not used.

Parameter: Word Count

Format:
```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-- N O T   U S E D -->  <-W O R D  C O U N T->
```

Description: This parameter specifies the number of words (0-128 for RX02 max, 0-64 for RX01 max) to transfer. If the word count exceeds the maximum number allowed, Word Count Overflow is set in the Error and Status Register.

Parameter: Bus Address

Format:
```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<----------- B U S   A D D R E S S ---------->
```

Description: This parameter specifies the bus address of the first data word to be transferred (only 18-bit addressing is allowed).

Parameter: Mode/Set Media Density Word

Format:
```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<----------- MODE/SET DENSITY WORD ---------->
```

Description: This parameter is used to set the controller mode or to specify the RX02 set media density command. There are two allowable values. They are:

OCTAL VALUE	ASCII CODE	MEANING
000111_8	I	RX02 Set Media Density
51505_8	*SE	Set extended mode

*Note: This becomes a .WORD "ES in Macro-11.

Parameter: Error and Status Word in Compatible Mode

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<NOT	USED>			NM	WO	R	US	DR	DD	DK	DE	PF	ID	TS	CE

Field Mnemonic (Bit)	Description
NM (11)	Nonexistent Memory Error. When set, this bit indicates an invalid memory address or a parity error for a DMA transfer.
WO (10)	Word Count Overflow. This bit indicates that a fill or empty buffer function would exceed the sector size.
R (9)	Reserved (when read these bits will be 0)
US (8)	Unit Select. This bit indicates the current drive selected.
DR (7)	Drive Ready. If DR=1 the drive is ready. This bit is valid only after a Read Status function or an initialize.
DD (6)	When DD=1, indicates Deleted Data AM read or written on last operation.
DK (5)	Drive Density. This field specifies the diskette format in the last selected drive on the last access to that drive.
DE (4)	Density Error. This field indicates that the function and diskette formats differ. When this error is detected the command is terminated by setting Error and Done.
PF (3)	Indicates power failure when PF=1.
ID (2)	Initialize Done. When ID=1 the initialization sequence is complete. Initialization sequence is entered on: 1) power on; 2) bus initialize; 3) IN=1 in the command and status register.
TS (1)	Two Sided. When TS=1 a two sided, 8" floppy inserted in the selected drive. RX02 simulation on 5-1/4" floppies always presents a double sided 5-1/4" floppy as a single sided RX02 diskette; thus TS=0. RX01 simulation only uses side 0 of the 5-1/4" floppy and always sets TS=0. See section III-E.
CE (0)	CRC Error. If CE=1 the data transferred is invalid because a CRC error has been detected. When this error is detected the command is terminated by setting Error and Done.

E. COMPATIBLE MODE FUNCTIONS

In the compatible mode a total of eight functions (or commands) are available. These functions operate on the floppy disk only and are identical to the DEC RX02 functions. These functions are summarized below and described in detail in the following sections. In these sections the parameters are listed in the order in which they are written to the data register (DBR). All parameters must be sent to the controller using the protocol described in section IV-B. Commands are always initiated by writing the function to the Command and Status register with the GO bit set. This is allowed only when the Done bit is set. If a command is written to the Command and Status register when the Done bit is not set, the command is ignored. Whenever a command is initiated properly, the Done bit is cleared.

If an error is detected the command is terminated by setting Done and Error in the Command and Status Register.

The cause for the error is reported with the Error and Status word which is written to register DBR.

CODE	FUNCTION
000	Fill Buffer
001	Empty Buffer
010	Write Sector from buffer
011	Read sector to buffer
100	Set Media Density/Set Mode
101	Read Status
110	Write Deleted Data Sector from buffer
111	Read Error Code

Command: Fill Buffer (000)

Parameters: Word 1 - Word Count
Word 2 - Buffer Address (host memory)

Function: Transfer from 1 to 128 words of data from host memory to the controller data buffer.

Operation: If the word count is zero the command is terminated (Done is set). Error is not set when the word count is zero. If the word count is greater than 128 words with the DS bit set (or 64 words with the DS bit clear) the command is terminated by setting Done and Error.

If the word count is less than or equal to 128 (64 for DS=0), the requested number of words are transferred from memory to the controller's buffer. If the transfer is less than 128 words the controller fills the remaining words with zero's.

Upon completion of the command, Done is set, and the Error and Status word can be read from the data register (DBR).

Command: Empty Buffer (001)

Parameters: Word 1 - Word Count
Word 2 - Buffer Address (host memory)

Function: Transfer from 1 to 128 words of data from the controller buffer to host memory.

Operation: If the word count is zero the command is terminated (Done is set). Error is not set when the word count is zero. If the word count is greater than 128 words with the DS bit set (or 64 words with the DS bit clear) the command is terminated by setting Done and Error.

If the word count is less than or equal to 128 (64 for DS=0), the requested number of words are transferred from the controller buffer to host memory.

Upon completion of the command, Done is set, and the Error and Status word can be read from the data register (DBR).

Command: Write Sector from Buffer (010)

Parameters: Word 1 - Sector Number
Word 2 - Track Number

Function: Write one sector from the controller's buffer to a floppy drive.

Operation: After the command and parameters have been received the track number is checked to insure it is within 0 to 76. If not the command is terminated and an error reported. The sector number is not limit checked, but only the least significant byte is used.

If the parameters are valid the controller seeks to the requested track, validates the track number and locates the requested sector. The diskette format and the requested format are then compared. If they are the same the entire sector is then written; otherwise the command is terminated and an error reported.

Upon completion of the command, Done is set and the Error and Status word is available in the data register DBR.

Command: Read Sector to Buffer (011)

Parameters: Word 1 - Sector Number
Word 2 - Track Number

Function: Read one sector from a floppy drive to the controller's buffer.

Operation: After the command and parameters have been received the track number is checked to insure it is within 0 to 76. If not the command is terminated and an error reported. The sector number is not limit checked, but only the least significant byte is used.

If the parameters are valid the controller seeks to the requested track, validates the track number and locates the requested sector. The diskette format and the requested format are then compared. If they are the same the entire sector is then read; otherwise the command is terminated and an error reported.

Upon completion of the command, Done is set and the Error and Status word is available in the data register DBR. If a deleted data address mark was read the deleted data bit in the Error and Status word is set.

Command: Set Mode/Media Density (100)

Parameters: Mode/Set Media Density Word

Function: Set the controller mode or set the media density

Operation: The Mode/Set Density word is compared to one of two values. If the parameter is an ASCII 'I' then the diskette is formatted to simulate either RX01 or RX02 (based upon the DS bit of the CSR).

The Set Media Density operation must not be interrupted. If it is, the operation must be repeated.

Initializing (formatting) diskettes can be accomplished by using the format command in the extended mode.

If the parameter is an ASCII 'SE' (a .WORD "ES in Macro-11) then the controller enters the extended mode. See section IV-F,G for a description of the extended mode.

Upon completion of the command, Done is set and the Error and Status word is available in register DBR.

Command: Maintenance Read Status (101)

Parameters: None

Function: Read the Error and Status word

Operation: The drive ready status is updated.

If the drive is ready the format status is updated by starting the motor of selected drive and reading the diskette.

If the drive is not ready, the format status of the last successful read is reported.

After the above has been accomplished the Error and Status word is available in DBR.

Errors are reported if the DS bit in CSR does not agree with the format of the diskette or if it can't be read. No error is reported if the drive is not ready.

Command: Write Deleted Data Sector from Buffer (110)

Parameters: Word 1 - Sector Number
Word 2 - Track Number

Function: Write one sector using deleted data (control) address marks from the controller buffer to a floppy drive.

Operation: The operation is the same as Write Sector function except that a deleted data address mark is written in place of the standard address mark.

Command: Read Error Code (111)

Parameters: Word 1 - Buffer Address

Function: Read extended status into memory

Operation: Upon receipt of the command and parameter, the controller DMA's four words of status to the buffer address (specified by the parameter and bits 12,13 in CSR). The format of these status words is:

Word 1<7:0>	Definitive Error Code***
Word 1<15:8>	Word Count Register
Word 2<7:0>	Current Track Address of Drive 0
Word 2<15:8>	Current Track Address of Drive 1
Word 3<7:0>	Target Track of Current Disk Access
Word 3<15:8>	Target Sector of Current Disk Access
Word 4<7>	Unit Select Bit*
Word 4<5>	Motor On Bit*
Word 4<6><4>	Drive DS Bit of Both Drives*
Word 4<0>	DS of Read Error Code Command*
Word 4<15:8>	Track Address of Selected Drive**

* Five status bits are included in an 8-bit word. Unit Select = bit 7, DS of Drive 1 = bit 6, Motor On = bit 5, DS of Drive 0 = bit 4, DS of Read Error Code Command = bit 0.

**The Track Address of the Selected Drive/error is only meaningful on a code 150 error. The register contains the address of the cylinder that the head reached on a seek.

***The definitive error code is updated only when an error occurs. Thus, when a command is issued, the definitive error code will remain unchanged if no error occurs. Read Error Code cannot be used to determine if an error occurred on the last command.

The definitive error codes are (codes in octal):

Code	Error Code Meaning
0040	Tried to access a track greater than 76.
0070	Desired sector could not be found after looking at 52 headers (two revolutions).
0120	A preamble could not be found.
0130	No ID mark found within allotted time span.
0150	The header track address of a good header does not compare with the desired track.
0170	Data AM not found in allotted time.
0200	CRC error on reading the sector from the disk. No code appears in the ERREG.
0220	R/W electronics failed maintenance mode test.
0230	Word count overflow.
0240	Density Error (not RX01 or RX02 simulation format).
0250	Wrong key word for set media density command.

F. REGISTER DESCRIPTION IN THE EXTENDED MODE

Command and Status Register (CSR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ER	IN	EA	EA	AV	R	XA	SR	TR	IE	DN	FN	FN	FN	FN	GO

Field Mnemonic (bit)	Description
ER (15)	Error Indicator. This bit is set when an error has been detected during the execution of a command. It is cleared by issuing a new command or by setting the initialize (IN) bit. This is a read only bit.
IN (14)	Initialize. This is a write only bit which can be set under software control to initialize the controller without affecting any other device on the bus. The following functions are performed when this bit is set: 1) Done is cleared in the CSR. 2) All heads are marked as unregistered. Registration will occur on the first access (floppy motors off). 3) Controller power-on diagnostics are executed if enabled. 4) The command and status register (CSR) is set to 40_8, and the data bus register (DBR) is set to zero.
EA (12-13)	Extended Address. These bits are the most significant bits of an 18-bit bus address (bit 13 is the MSB), XA=0, and are write only bits. These bits are not used when XA=1.
R (10)	Reserved. Must be set to 0 when writing CSR.
AV,SR (11,8)	Available. Status read. See seek command.
XA (9)	22-bit address. If XA=1 when GO is set, then the extended address bits of the CSR are ignored (EA) and an extra word of buffer address containing the most most significant six bits of the 22-bit address is prompted for.
TR (7)	This read only bit indicates that the host may write the data buffer register (DBR) when it is set.

IE (6) Interrupt Enable. This bit enables interrupts. This is a read/write bit. It is cleared when an initialize is done (bit 14=1) or by software.

NOTE: Whenever Done is set and this bit is changed from a 0 to a 1, the controller will generate a host interrupt. If interrupts are enabled and the Go bit is set at the same time, an interrupt will be generated only when the command completes.

DN (5) Done. This read only bit indicates the completion of a function and that status can be read from the DBR. When this bit is set another command may be issued. When this bit is clear a command is in the process of being executed. Any commands issued when Done is clear are ignored.

FN (1-4) Function Field. These bits determine the function to be executed. See section IV-G for a description of the codes and functions. The function field is a write only field.

GO (0) Go. This bit, when set to a 1, will start the command. GO is a write only bit.

Multipurpose Data Register (DBR)

This register is used to pass parameters from the host CPU to the controller and for the host to receive status from the controller. The formats and meaning of the parameters passed to the controller and the status received by the host are detailed below. The host must observe the protocol described in section IV-B when writing the DBR register.

Parameter Name: Unit Designator

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA	R	R	SZ	DS	DS	SL	SL	IL	IL	DL	NR	NC	R	DT	UN

Field Mnemonic (bit)	Description
PA (15)	Determines whether the disk address is interpreted as a physical (PA=1) or logical (PA=0) address. See section III-B for a discussion of physical versus logical addressing. Note: When using physical addressing, if a flawed sector is accessed, an error will be reported.
R (14-13)	Reserved. Must be set to zero.
SZ (12)	For 5-1/4" floppies, this bit is used to limit access to side 0 only of the diskette when set=1. For 8" floppies and Winchesters, this bit is reserved for SMS use and should be writen as zero. Failure to write this bit as zero could result in loss of data on the Winchester. Since the controller cannot distinguish a single sided 5-1/4" diskette from a double sided one, the host must define the type of diskette for the FWD0106 via the SZ bit. If SZ=1 then a single sided diskette is installed. Otherwise (SZ=0) a two sided diskette is installed.
DS (10-11)	This field specifies the floppy disk encoding as shown below. This field is not used when the device is a fixed disk (DT=1). 00 Single density (RX01)* 01 RX02* 10 Double density (MFM) 11 (same as 10)
SL (8-9)	This field specifies the floppy sector length as shown below. This field is not used when the device is a fixed disk (DT=1) or when the diskette density selected is RX02 double density. 00 128 bytes/sector (DEC RX01) 01 256 bytes/sector (DEC RX02) 10 512 bytes/sector 11 1024 bytes/sector

*Whenever RX01 or RX02 formats are requested, the sector length and interleave fields are already known to the controller.

IL (6-7) This field specifies whether any logical offsetting and/or interleaving is to be done by the controller (floppies only).

00 no logical offset or interleave

01 1/4 track logical offset compatible with the SMS HIP. This format is only allowed on 512 byte DD 8" floppy format.

The algorithm used to determine the actual sector read or written on the floppy is as follows:

NOTES: 1) Integer division is used (remainder discarded);
2) logical address is converted to physical address before adding logical offset.

For cylinder 0: No offset

For cylinders 1-76: $ASN = (\text{Remainder of } (\frac{T-1}{4})) * 4 + SN$

IF ASN > NS THEN ASN = ASN-16

where ASN = Actual Sector Number read or written
T = Cylinder Number
SN = Sector Number issued by host (may have been converted from logical address).

Note: When double sided drives are being used the offset is the same for both sides because head switching occurs only at the index hole (i.e. after the last physical sector).

For a double sided diskette the sector sequence for a large block transfer starting at cylinder 3 would be:

CYL 3 Side 0, sectors 9-16
CYL 3 Side 1, sectors 1-16
CYL 3 Side 0, sectors 1-8
CYL 4 Side 0, sectors 13-16
CYL 4 Side 1, sectors 1-16
etc.

The above sequencing eliminates the need for any head switch offset for floppies.

10 six sector offset and 2:1 interleave compatible with the DEC RX02 offset and interleave done by the DEC DY Handler (e.g. the controller replaces the need to do this in the handler and allows one command to transfer multiple blocks). This offset/interleave is valid only for RX01/RX02 formats (otherwise it is ignored).

Given a logical cylinder and sector, the algorithm used to determine the physical sector written is as follows:

```
T = cylinder number-1;     S = logical sector number-1
IF    S < 13
THEN  S = (T*6) + (S*2)
ELSE  S = (T*6) + (S*2) + 1
WHILE S > 0 DO  S = S-26
ASN = S+27 = physical sector to be accessed
```

This results in the following sequence for a single sided diskette:

Cyl.	Logical Sector Number Passed to Controller									
	1	2	3...11	12	13	14	15	16...26		
1	1	3	5...21	23	25	2	4	6...26		
2	7	9	11....1	3	5	8	10	12....6		
3	13	15	17....7	9	11	14	16	18...12		
.			.							
.			.							
.			.							

Note that all odd numbered sectors are accessed first, followed by all even numbered sectors, and that two sectors are skipped on the odd to even transitions.

On double sided diskettes, the 6 sector offset is added to both head and cylinder boundaries. This results in the following sequence for a double sided diskette:

Cyl.	Head	Logical Sector Number Passed to Controller								
		1	2	3...11	12	13	14	15	16...26	
1	0	1	3	5...21	23	25	2	4	6...26	
1	1	7	9	11....1	3	5	8	10	12....6	
2	0	13	15	17....7	9	11	14	16	18...12	
2	1	19	21	23...13	15	17	20	22	24...18	
.	.			.						
.	.			.						
.	.			.						

The sectors are accessed in the same order as for the single sided diskette above. Both tracks of a cylinder are accessed before a cylinder step is made. Thus if a large block access is started at cyl 1, head 0, sector 1, then all sectors on cyl 1, head 0 will be accessed followed by all sectors on cyl 1, head 1, followed by all sectors on cyl 2, head 0, and so on.

11 Same as 10.

DL (5) Deleted Data (control data) Flag. On a floppy read, if DL=1 then any sector which has a deleted data address mark is skipped. If DL=0 and a deleted data address mark is encountered, the sector is read and the operation is terminated. Deleted Data Address marks are used on the floppy disk only.

NR (4) Retry Flag. If NR=0, retries are attempted according to the retry policy (see section IV-A) when an error is encountered. If NR=1, no retries are done when an error is encountered.

NC (3) This bit, when set, disables Winchester error correction. Under normal conditions this bit would be 0 which would enable Winchester error correction. See section III-G for a detailed discussion of Winchester error correction.

R (2) Reserved (must be written as a 0).

DT (1) Device Type. If DT=0 the device type is a floppy. If DT=1 the device type is a fixed Winchester or cartridge drive.

UN (0) Unit Number. This field selects the desired unit (0-1).

Parameter Name: Disk Address

Format: Physical Disk Address

```
          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
WORD 1    <NOT  USED> <-  HEAD ->  <---  S E C T O R --->
WORD 2    <-- NOT  USED -->  <---- C Y L I N D E R ----->
```

Format: Logical Disk Address

```
          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
WORD 1    <-------- N O T   U S E D -------->  <-- LR -->
WORD 2    <--------- LOGICAL RECORD NUMBER (LR)--------->
```

Description: The disk address can be specified as either a physical or logical address as determined by bit PA in the unit designator word. The disk address always consists of two words as shown above. The logical record number is a 20 bit field with the most significant bit in word 1, bit 3 and the least significant bit in word 2, bit 0. The logical record number starts at 1, not 0. Unused bits must be written as zero's.

Head addresses always start at 0 and go to the maximum number of heads minus one. Cylinder addressing also starts at 0 and goes to the maximum number of cylinders minus one, while sector addressing starts at 1 and goes to the maximum number of sectors per track.

Parameter: Buffer Address (least significant word)

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-------- B U F F E R   A D D R E S S -------->
```

Description: This parameter specifies the 16 least significant bits of the buffer (host memory) address. The most significant bits are either in the Command and Status register (18-bit addressing, XA=0), or in the most signifigant address word (22-bit addressing, XA=1). Bit 0 of the buffer address must always be 0. (i.e. transfers start at a word boundary).

Parameter: Buffer Address (most significant word)

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<----------not used----------><--buff addr--->
```

Description: This parameter specifies the 6 most significant bits of the buffer (host memory) address, only when XA=1 in CSR. Otherwise, the EA bits of the CSR are used. Unused bits must be written as zero's.

Parameter: Word Count

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 <---------- W O R D   C O U N T ---------->
```

Description: This parameter specifies the number of words to transfer. From 0 to 65535 words can be transferred. The actual word count is loaded with 0 to 65535 words (not two's complement).

Parameter: Mode Word

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-------------- M O D E   W O R D ------------>
```

Description: This parameter is used to set the controller to the compatible mode. The only allowable value is:

OCTAL CODE	ASCII VALUE	MEANING
42503	*EC	Enter compatible mode

*Note: This becomes a .WORD "CE in Macro-11.

Parameter: Disk Format Designator for Winchester Drives

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	SL	SL	SI	SI	SI	SI	R	R	DT	UN

Field Mnemonic (bit)	Description
DT, UN (1,0)	Same as unit designator.
SL (8-9)	This field specifies the sector length as follows: 00 not used 01 256 bytes/sector 10 512 bytes/sector 11 not used
SI (4-7)	Sector Interleave Increment. This value specifies the increment between sectors read or written. The number of sectors skipped is the interleave increment minus 1. Thus, an increment of 1 results in consecutive sectors being read or written. An increment of 2 results in one sector being skipped and so on. A sector interleave of zero is interpreted as an interleave of 16.
R (10-15, 2-3)	Reserved; must be written as zero.

Parameter: Disk Format Designator for Floppy Drives

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	SZ	DS	DS	SL	SL	SI	SI	SI	SI	R	R	DT	UN

Field Mnemonic (bit)	Description
SZ(12),DS(10-11), SL(8-9),DT(1),UN(0)	Same as unit designator parameter.
SI (4-7)	Sector Interleave Increment. Same as for Winchester drives.
R (14-15,2-3)	Reserved. Must be written as zero.

Parameter: Starting Cylinder

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 0 <----------> 0  <---- C Y L I N D E R ---->
```

Description: This parameter specifies the cylinder at which the formatting will start.

Parameter: Number of Cylinders to Format

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 0 <----------> 0  <--- NUMBER OF CYLINDERS--->
```

Description: This parameter specifies the number of cylinders to format. If this parameter is zero all cylinders will be formatted.

If this parameter is greater than the number of cylinders between the starting cylinder and the last cylinder on the disk then all cylinders between (and including) the starting cylinder and the final cylinder will be formatted.

Parameter: Head Step and Switch Offsets

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<--- Switch Offset ---> <--- Step  Offset --->
```

Description: Head Switch Offset: This field specifies the number of sectors to offset when switching from one track to another track within a cylinder (i.e. Head select time).

Head Step Offset: This field specifies the number of sectors to offset when moving the head to the next cylinder.

An offset of 0 or 1 results in no offset (e.g. a head switch will go from the last sector of the current track to the first sector of the next track).

An offset of 2 will cause one sector to be skipped, an offset of 3 will cause two sectors to be skipped, and so on.

Offsets are not applied to floppy cylinder 0.

Parameter: Subtest/Unit Number

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<------ Subtest ------>								0	0	0	0	0	0	DT	UN

Description: DT, UN (1,0) is the same as unit designator. The Subtest field is used to specify the activity of the maintenance command.

Parameter: Utility Word

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	CR3	CR2	CR1	SP	R	R	R	R	R	DT	UN

Field Mnemonic (bit)	Description
R (15-11,6-2)	Reserved. Must be written as zeroes.
CR3, CR2, CR1 (10-8)	LED's. If any of these bits are "1", the corresponding LED is turned on; otherwise the LED is turned off.
SP (7)	Shipping. If SP=1, then the drive is stepped to its shipping zone (Winchester only).
DT, UN (1,0)	Same as unit designator.

Upon completion of all commands the multipurpose data register (DBR) contains status and error information. This status information can be read only when the Done bit in the Command and Status register is set.

The meaning and format of the status and error information for the extended mode of operation is as follows.

Parameter: Error and Status Word (in extended mode)

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
SC TO EC<---------->EC TS WP RF DR DD  R DT UN
```

Field Mnemonic	Description
SC (15)	When this bit is set a seek caused by the seek command has completed on the unit indicated by the UN field.
TO (14)	Head positioned at track 0
EC (8-13)	Error Codes. This field shows what caused the error as follows (number in parentheses is in octal):

0 No error

1 (1) Illegal head address error.
The host passed the controller a head address outside the range of the drive being accessed. Head numbers start at 0.

2 (2) Illegal sector address error.
The host passed the controller a sector number outside the range of allowable values. Sector addressing starts at sector 1 with the largest sector number depending on drive type and format.

3 (3) Illegal cylinder address error.
The host passed the controller a cylinder number outside the range of allowable values of the drive being accessed. Cylinder numbers start at 0.

4 (4) Illegal logical address error.
Logical addresses range from 1 to the number of unflawed sectors on the disk. This error occurs when the host passes the controller an address outside of this range.

5 (5) Registration timeout error.
This error will occur when a drive does not report seek complete or the track 0 indication is not seen by the controller.

6 (6) Reserved for internal controller uses.
(Illegal word count in compatible mode).

7 (7) Illegal drive type error.
If an attempt is made to access a drive and the formatter board drive type switches are set to a NOT USED position, this error will occur.

8 (10) Format error (sector length wrong).
This error will occur when sector length of the diskette does not agree with that passed to the controller by the host.

9 (11) Head select error.
If after one revolution the controller cannot find the desired sector, it will read an ID to determine if the head is correct. If it is not this error will be reported.

10 (12) Write protected error.
Host attempted to write or format a write protected diskette, or the host attempted to write or format Winchester 0 when W17 is removed, or external write protect switch is open (Winchester 0 write protected).

11 (13) Deleted data error.
Deleted data (control) AM read and the DL in the unit designator word was 0. If the DL bit is 1 the sector is skipped if it has a deleted data AM and no error is reported. This error applies to floppies only.

12 (14) Key word error.
Wrong key word passed by host on the Set Mode command.

13 (15) DMA error.
The controller detected a non-existent memory or parity error when attempting to access host memory.

14 (16) Disk overrun error.
The host attempted to read beyond the end of the disk.

15 (17) Head positioning or seek error.
After positioning the carriage over the desired cylinder, if an error occurs, the controller reads an ID to determine if the cylinder is correct. If it is not, this error is reported.

NOTE: If retries are not enabled, then, following a seek error, the host should issue an initialization to re-register the heads.

16 (20) No address marks on track error
The controller could not find any valid address marks on the track. An unformatted diskette will typically cause this error.

17 (21) Sector ID not found error.
The controller could not find the sector the host has requested. This would indicate media or drive problem.

18 (22) Data CRC or non-correctable ECC error.
After reading a sector, the CRC computed did not agree with that previously written. CRC errors often indicate media problems.

19 (23) Missing data address mark error.
The controller has found the desired sector but the data address mark is invalid or missing. This error may indicate drive or media problems.

20 (24) Data late or DMA latency error.
Host memory transfers were not occurring quickly enough to keep up with the required transfer rate of the disk. Another DMA device would typically have to be "hogging" the bus for this error to occur.

21 (25) Data transfer timeout error.
The controller will timeout any host memory access request after 20 msec.

22 (26) Diskette densities don't match error.
The density of the diskette being accessed does not agree with the value given to the controller by the host.

23 (27) Media not readable error (floppy only).
The controller is unable to maintain phase lock with the diskette data. This error implies media or drive problems.

24 (30) Drive not ready error.
The drive being accessed is not ready. If a diskette is not inserted or inserted backwards, the drive will not be ready.

25 (31) Not used.

26 (32) Illegal format for RX02 error.
There must be 26 sectors/track when the IL bits of the unit designator are set to RX02 offset and interleave.

27 (33) Flaw map not valid error.
If flaw mapping is selected and a valid flaw map has not been placed on the selected Winchester, this error will be reported on any access to that drive.

If an error is detected, such as CRC, when the controller attempts to read the flaw map, the CRC error will be reported. Access errors will always override CRC or ECC errors.

28 (34) Illegal command error.
The host has passed the controller an illegal command.

29 (35) Wrong Interface.
Attempt to do 22 bit addressing with an 18 bit interface board (LSI-11 Rev. C or earlier, PDP-11).

30 (36) Winchester ID CRC error.
A CRC error was detected when reading the ID field.

31 (37) Winchester write fault error.
Write Fault from the Winchester drive. This usually indicates a drive or cabling problem.

32 (40) Spare.

33 (41) Flawed sector access error.
Attempt to access a flawed sector. This error will be reported when a flawed sector is accessed using physical addressing. Flawed sectors are skipped if logical addressing is used.

34 (42) Missing Winchester data address mark or DMA access fails. This error would typically indicate a drive is faulty. However, this error could occur if a DMA access was initiated by the controller and the DMA access was not allowed to complete.

35-47 (43-57) Spare

NOTE: Errors 48-63 are controller hardware and/or firmware failures. The error message will have little meaning to the general user but may be useful when controller repair is attempted.

48 (60) BS2=0 Timeout during format (FMTTRK)
49 (61) BS0=0 Timeout in buffered write (BFWRTE)
50 (62) BS2=1 Timeout in format, no index (FMTTRK)
51 (63) BS2=1 Timeout in format, no index (FMTTRK)
52 (64) BS2=0 Timeout in format, no index (FMTTRK)
53 (65) BS2=0 Timeout in direct transfer (DIRECT)
54 (66) BS0=0 Timeout in direct transfer (DIRECT)
55 (67) BS0=0 Timeour in direct transfer (TFUNCT)
56 (70) BP fails interface test (BPINT)
57 (71) BP fails wakeup test (BPTST)
58 (72) BP fails ECC/CRC test (ECCCRC)
59 (73) BPS=000 Timeout (TOBPSZ)
60 (74) BS0=0 Timeout (WBS0M)
61 (75) BS2=0 Timeout (WBS2R)
62 (76) BS2=1 Timeout (SSWRT)
63 (77) Spare

TS (7) Two sided diskette flag. This bit is valid only when the drive type is a floppy (DT=0). If an 8" floppy is being controlled then TS is set when a double sided floppy diskette is installed in the selected drive. If a 5-1/4" floppy is being controlled then TS is set when the format specified in the unit designator is not RX01 or RX02 simulation. It is cleared when an RX02 or RX02 simulation is specified.

WP (6) Write protect flag. When set the unit indicated by UN is write protected.

RF (5) Retry flag. Retries or error correction occurred on the last operation if this bit is set. If the error bit in the Command and Status register is not set, then the retries or error correction were successful.

DR (4) Drive ready flag. If DR=1 the drive, indicated by UN, is ready.

DD (3) Deleted data AM flag. Deleted data AM read on last operation when DD=1.

R (2) Reserved for SMS use.

DT, UN Same as in unit designator.

G. EXTENDED MODE FUNCTIONS

The extended mode functions add additional capability and increase performance over DEC RX02 floppy disk systems plus provide complete support for Winchester drives.

In the extended mode a total of sixteen function codes are available. These functions and their codes are summarized in the table below and described in detail in the following sections. In these sections the parameters are listed in the order in which they are written to the data register (DBR). All parameters must be sent to the controller using a protocol described in section IV-B. Commands are always initiated by writing the function to the Command and Status Register with the GO bit set. Whenever a command is initiated properly, the Done bit is cleared.

CODE	FUNCTION
0000	Seek
0001	Format Floppy
0010	Write Direct
0011	Read Direct
0100	Set Mode
0101	Read Drive Status
0110	Write Deleted Data Direct (floppy only)
0111	Read Extended Status
1000	Read ID
1001	Format Winchester
1010	Write Flaw Map
1011	Read Flaw Map
1100	Maintenance
1101	Identify interface
1110	Utility command
1111	Reserved

If an error is detected during command execution and if it is a retriable error then it is retried according to the retry policy (see section III-A). If retries fail or it was a non-retriable error, the command is terminated by setting Done and Error in the Command and Status Register.

The cause for the error is reported with the Error and Status word which is written to register DBR. In all cases when the error bit in the Command and Status Register is set, the error field of the Error and Status word will be non-zero.

Unless otherwise noted, the extended mode commands operate identically with either floppy or fixed drives.

Command:	Seek (0000)
Parameters:	Word 1 - Unit Designator Word 2,3 - Disk Address
Function:	Position disk head over specified cylinder
Operation:	All disk read/write commands have implied seeks. The Seek command is provided for downward compatibility with previous SMS controllers. Overlapped seeking is not performed by the FWD0106. AV is always cleared in extended mode, and always set in compatible mode. SR is ignored.

Command: Format Floppy (0001)

Parameters:
Word 1 - Disk Format Designator For Floppy Drives
Word 2 - Starting Cylinder
Word 3 - Number of Cylinders
Word 4 - Offsets

Function: Format (initialize) a diskette in one of several formats. Formatting a diskette includes the writing of header information (sector number, track number, etc.) and initializing the data field. The allowable formats are described in detail in section III.

Using this command, from one to all cylinders on a diskette can be formatted. Typically the entire surface is formatted, however, if desired, cylinders may be formatted individually.

Operation: After the command and parameter has been passed the controller validates all fields and insures the selected values apply to the drive specified.

The controller next seeks the heads to the specified starting cylinder. When index is detected the cylinder is formatted according to the format selected. After the cylinder is formatted a step to the next cylinder is done and it is formatted. This is repeated until the number of cylinders specified have been formatted.

Upon completion of the command, the Done bit is set and the Error and Status word can be read at DBR.

Note: If no logical offsetting is being done, (for better performance) SMS recommends the use of a 1/4 track physical offset as shown below:

	Bytes/ Sector	Density	Head Step Offset	Head Switch Offset
5-1/4" Floppy (MFM)	128	Double	7	2
	256	Double	4	2
	512	Double	3	2
	1024	Double	1	2
8" Floppy (FM)	128	Single	7	2
	256	Single	5	2
	512	Single	3	2
	1024	Single	1	2
8" Floppy (MFM)	128	Double	12	2
	256	Double	7	2
	512	Double	5	2
	1024	Double	3	2

Command: Write Direct (0010)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Word Count
Word 5 - Buffer Address (least significant)
Word 6 - Buffer Address (most significant, XA=1)

Function: Write the specified number of words directly from host memory to the disk.

Operation: After the commands and parameters have been passed and validated, the controller seeks to the cylinder specified by the Disk Address parameter. The disk address may be specified either as a physical (PA=1) or logical address (PA=0). The cylinder number is verified and the desired sector is located. Once the starting sector is located, the number of words specified by word count are transferred from host memory to the disk. Any cylinder boundaries are automatically crossed during the transfer. If the transfer completes with a partially filled sector the controller will zero fill this sector. The data is taken from the memory address specified by the parameter buffer address.

The command completes when either an error is detected or all requested words have been transferred. Upon completion of the command Done is set, and, if necessary, the error bit is set. When Done is set the Error and Status word is available in DBR.

Command: Read Direct (0011)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Word Count
Word 5 - Buffer Address (least significant)
Word 6 - Buffer Address (most significant, XA=1)

Function: Read the specified number of words directly from the disk to host memory.

Operation: After the commands and parameters have been passed and validated, the controller seeks to the cylinder specified by the Disk Address parameters. The disk address may be specified either as a physical (PA=1) or logical address (PA=0). The cylinder number is verified and the desired sector is located. Once the starting sector is located the number of words specified by Word Count are transferred directly from the disk to host memory specified by the Buffer Address. Any cylinder boundaries are automatically crossed during the transfer.

The command completes when all requested words have been transferred or an error is detected. Upon completion of the commmand Done is set, and the ERROR bit is set if necessary. The Error and Status word is available in DBR when the command completes.

Command: Set Mode (0100)

Parameters: Mode Word

Function: Establish the controller mode

Operation: The mode word must be the value described in section IV-F. If it is not, the command is terminated with the appropriate error and the controller mode remains unchanged.

If the mode word is correct the controller enters the compatible mode and terminates the command.

Done is set, and the Error and Status word is available in DBR when the command completes.

NOTE: To set media density on RX01/RX02 diskettes use the format command or enter the compatible mode and use the Set Media density command.

Command: Read Status (0101)

Parameters: Unit Designator

Function: Read Error and Status Word

Operation: This is the extended mode equivalent for the compatible mode read status.

After the command has been received all bits in the error and status are updated and the error status word is written to the DBR. Done is then set to indicate the host may read the DBR. This command will never cause the Error bit to be set.

Command: Write Deleted Data Direct To Floppy (0110)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Word Count
Word 5 - Buffer Address (least significant)
Word 6 - Buffer Address (most significant, XA=1)

Function: Write the specified number of words directly from host memory to a floppy disk using a deleted data address mark. Deleted data address marks are not used on Winchesters.

Operation: After the commands and parameters have been passed and validated, the controller seeks to the cylinder specified by the Disk Address parameter. The disk address may be specified either as a physical (PA=1) or logical address (PA=0). The cylinder number is verified and the desired sector is located. Once the starting sector is located, the number of words specified by word count are transferred from host memory to the disk using a deleted data address mark. Any cylinder boundaries are automatically crossed during the transfer. If the transfer completes with a partially filled sector the controller will zero fill this sector. The data is taken from the memory address specified by the parameter buffer address.

The command completes when either an error is detected or all requested words have been transferred. Upon completion of the command, Done is set. If necessary, the ERROR bit is set. When Done is set the Error and Status word is available in DBR.

Command: Read Extended Status (0111)

Parameters:
Word 1 - Unit Designator
Word 2 - Buffer Address (least significant)
Word 3 - Buffer address (most significant, XA=1)

Function: Report extended Status on a drive by drive basis

Operation: After the command and parameters have been passed and validated the controller transfers several words of status information for the drive selected to host memory. When the transfer is complete, Done is set and the Error and Status word is available in DBR.

The format of the status transferred to memory is as follows:

```
        15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
Word 1   0  0  0  0  0  0  C <-----------------------> C
Word 2   <------------------ OPTIONS ------------------>
Word 3   <------------------ OPTIONS ------------------>
Word 4   0  0  0  0  0  0  0  0  0  0  0  0  N<-MSB-> N
Word 5   N <-MIDDLE-------------------------------LSB-> N
Word 6   0  0  0  0  H <----> H  S <-----------------> S
Word 7   0  0  0  0  0  0  C <-----------------------> C
```

Word 1: Current cylinder of selected unit.
Word 2-3: Option straps*
Word 4-5: Number of logical records (sectors). Winchester flaws are deducted (fixed portion only).
Word 6-7: Physical disk address of the last R/W direct disk access. If a disk error occurs on a read/write direct this will be the address of the error. This value is valid only for R/W direct commands.
H=Head, S=Sector, C=Cylinder.

Thus, for example, if a CRC error occurs this command can be issued to determine the disk address of the error.

*Option Straps

Word 2

Bits 2	1	0	FORMATTER TYPE
0	0	0	FWD0101 REV. E AND BELOW
0	0	1	RESERVED
0	1	0	FWD0101 REV. F AND ABOVE
0	1	1	FWD0106
1	0	0	RESERVED
⌄	⌄	⌄	⌄
1	1	1	RESERVED

Bit 3	DRIVE MAPPING ENABLE
0	NO MAPPING
1	FLOPPY DRIVES REVERSED

BITS 7	6	5	4	FLOPPY TYPE
0	0	0	0	SA850
0	0	0	1	SA800
0	0	1	0	RESERVED
0	0	1	1	SA460
0	1	0	0	RESERVED
0	1	0	1	MPI92
0	1	1	0	RESERVED
0	1	1	1	TM100-4
1	0	0	0	SA860/SA810
1	0	0	1	TM848-1/TM848-2
1	0	1	0	RESERVED
⌄	⌄	⌄	⌄	⌄
1	1	1	1	RESERVED

BITS 9	8	SELF TEST
0	0	NONE
0	1	ONCE AT INIT
1	0	RESERVED
1	1	RESERVED

BIT 10	FLAW MAPPING
1	ENABLED
0	DISABLED

BIT 11	INTERRUPT VECTOR
0	264_8
1	270_8

BIT 12	POWER UP MODE
0	NO CHANGE
1	RX02 EMULATOR

BITS 15	14	13	PRECOMP ENABLE
		1	DISABLED SINGLE SIDED FLOPPY
		0	ENABLED SINGLE SIDED FLOPPY
	1		DISABLED DOUBLE SIDED FLOPPY
	0		ENABLED DOUBLE SIDED FLOPPY
1			DISABLED WINCHESTER
0			ENABLED WINCHESTER

Word 3

BITS 4	3	2	1	0	WINCHESTER DRIVE 0 TYPE
0	0	0	0	0	RESERVED
'	'	'	'	'	'
1	0	0	0	1	RESERVED
1	0	0	1	0	ST506
1	0	0	1	1	RESERVED
1	0	1	0	0	ST406
1	0	1	0	1	ST412
1	0	1	1	0	ST419
1	0	1	1	1	RESERVED
'	'	'	'	'	'
1	1	1	1	1	RESERVED

BITS 12	11	10	9	8	WINCHESTER DRIVE 1 TYPE

SAME AS WINCHESTER DRIVE 0

BITS 15-13, 7-5 RESERVED

Command: Read ID (1000)

Parameters:
Word 1 - Unit Designator
Word 2 - Buffer Address (least significant)
Word 3 - Buffer address (most significant, XA=1)

Function: Read the next available ID header information and transfer it to host memory specified by the Buffer Address.

Operation: The command and parameters are verified and the next available ID information is read and transferred to memory.

ID information transferred is as follows:

Word 1: Cylinder
Word 2: Head
Word 3: Sector
Word 4: Bytes/sector
0 = 128 bytes/sector
1 = 256 bytes/sector
2 = 512 bytes/sector
3 =1024 bytes/sector
Word 5: Density
0 = RX01 or single density (FM)
1 = RX02
2 = Double density (MFM)
3 = Winchester (MFM)

On command completion Done is set, and the Error and Status word is available in DBR. No stepping is done, unless the carriage is not registered. The floppy target head is forced to zero.

Command: Format Winchester (1001)

Parameters:
Word 1 - Disk Format Designator for Winchester Drive
Word 2 - Starting Cylinder
Word 3 - Number of Cylinders
Word 4 - Offsets

Function: Write the ID headers and data fields on the specified cylinder.

Operation: Beginning at the starting cylinder the controller writes the header portion of the sector to all sectors on all cylinders specified. The data fields are set to zero.

WARNING: This command must be followed by a write flaw map command if there are flaws on the drive.

For optimal performance, SMS recommends the following:

Bytes/ Sector	Sectors/ Track	Interleave	Head Switch Offset	Head Step Offset
256	33	2	5	9
512*	17	1	3	5

* Standard values used by SMS for maximum capacity.

Command: Write Flaw Map (1010)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Buffer Address (least significant)
Word 5 - Buffer Address (most significant, XA=1)

Function: This command allows the host to write the flaw map to the disk 128 bytes at a time. The flaw map is written starting at cylinder 0, head 0, sector 1 and duplicated at cylinder 0, head 1, sector 1.

Operation: The flaw map is a set of linked sectors of which only the first 128 bytes are used. The host must generate the flaw map as described in section V and write the flaw map one sector at a time, using physical addressing, to those sectors indicated by the link.

CAUTION: The write flaw map command bypasses the check for flawed sectors. The host must insure the sectors being written are not flawed. The controller assumes the first sector of the flaw map is not flawed.

Command: Read Flaw Map (1011)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Buffer Address (least significant)
Word 5 - Buffer Address (most significant, XA=1)

Function: This command allows the host to read the flaw map 128 bytes at a time. The flaw map is a set of linked sectors starting at cylinder 0, head 0, sector 1 and is duplicated at cylinder 0, head 1 sector 1.

Operation: When this command is received 128 bytes of the sector specified will be stored at "buffer address". Physical addressing must be used and not logical addressing.

The format of the flaw map is shown in section V.

CAUTION: The read flaw map command bypasses the check for flaws, thus allowing flawed sectors to be read. It is assumed that the first sector of the flaw map is not flawed.

Command: Maintenance (1100)

Parameters:
Word 1 - Subtest Number/Unit
Word 2 - Subtest Dependent Parameter

Function: This command provides a drive test and several floppy maintenance functions. The drive test can be run either by issuing this command or from switches on the formatter PC boards.

Subtests 1 to 4 apply to the floppy only.

Operation: This command is unique in that the command will execute (except for subtest 4) until an error occurs or until the controller is issued an initialize.

When an error is detected the controller will set Done and Error, and generate an interrupt request as with all other commands.

If no error is detected, the command will continue indefinitely and Done will not be set.

NOTE: The second parameter (word 2) must always be written even if the sub-test does not require a parameter.

Subtest 0

Function: This subtest will perform the drive test on all ready disk drives. The test will not write to any drives and thus will not destroy any existing data on the diskettes or Winchester.

If an error is detected, it will be reported to the host in the normal manner. The LED's will be off at test completion.

Parameter: N/A

Subtest 1

Function: This subtest will select the specified floppy drive, seek it to the specified track and start the motor. Various maintenance and alignment functions can then be performed.

Parameter: Track number.

Subtest 2

Function: This subtest will select the specified drive, seek it to the specified track and then turn the floppy motor on and off repeatedly.

Parameter: Track number.

Subtest 3

Function: This subtest will select the specified drive, start the motor and seek it to the specified track. It will then step the drive between the specified track and the specified track plus one repeatedly.

Parameter: Track number.

Subtest 4

Function: This subtest selects the specified drive, starts the motor, seeks to the specified track, and writes the entire track, including headers, with all 1's in single density (FM) (8" floppy only).

This test will set Done and/or Error after the track has been written.

CAUTION: The diskette must be reformatted after this subtest is issued if the diskette is to be used in normal operations again.

Command: Identify Interface (1101)

Parameters: none

Function: This command provides a programatical way to determine the interface addressing capability. All PDP-11 and LSI-11 interface boards, Rev. C or less, perform 18-bit addressing. All LSI-11 interface boards, Rev. D and up, perform full 22-bit addressing.

Operation: If the interface board is not capable of performing 22-bit addressing then report ERR29. Otherwise terminate command with no errors.

Command: Utility command (1110)

Parameters: Word 1 - utility word

Function: This command allows the host to set the diagnostic LEDs, step the Winchesters to their shipping zones, and turn off the floppy spindle motors.

Operation: The diagnostic LEDs are set according to CR1-CR3 in the utility word. If SP=1 and a Winchester is selected then the drive is stepped to its shipping zone. If SP=1 and a floppy is selected then the floppy spindle motors are powered down. If SP=0 then the selected drive is not affected.

The FWD0106 controller automatically powers down the floppies after 5 seconds from the last floppy access. The controller also automatically powers up the floppies on the next floppy access.

H. PROGRAMMING EXAMPLES

The following examples present in a straight forward manner how the controller interface is used. These examples are not intended to be used as application programs, but are for instructive purposes only. For more detailed examples refer to the FW Installation and Test source code. (See section V-B.)

Example #1

```
;
;    COMPATIBLE MODE READ FLOPPY SECTOR INTO HOST MEMORY
;
;    FIRST READ THE SECTOR INTO THE CONTROLLER'S BUFFER
;
         MOV       #407,@#177170       ;ISSUE READ SECTOR COMMAND
                                       ;TO UNIT 0, DOUBLE DENSITY
         JSR       PC,TR               ;WAIT FOR TR TO BE SET
         MOV       #2,@#177172         ;READ SECTOR 2 (THIS CLEARS TR)
         JSR       PC,TR               ;WAIT FOR TR
         MOV       #4,@#177172         ;READ TRACK 4
         JSR       PC,DONE             ;WAIT FOR COMMAND COMPLETION
         BNE       ERROR               ;BRANCH IF ERROR
;
;    NOW EMPTY THE BUFFER INTO HOST MEMORY
;
         MOV       #403,@#177170       ;ISSUE EMPTY BUFFER
         JSR       PC,TR               ;WAIT FOR TR
         MOV       #128.,@#177172      ;EMPTY ENTIRE BUFFER
         JSR       PC,TR
         MOV       #1000,@#177172      ;PLACE DATA AT LOCATION 1000
         JSR       PC,DONE             ;WAIT FOR COMMAND COMPLETION
         BEQ       EXIT
;
;    ERROR HAS OCCURRED
;
ERROR:   MOV       @#177172,R0         ;GET STATUS
         JSR       PC,RERR             ;PROCESS ERROR (APPLICATION DEPENDENT)
;
EXIT:    RTS       PC
;
;    WAIT FOR TR
;
TR:      BIT       #200,@#177170       ;TEST TR
         BEQ       TR                  ;LOOP UNTIL TR=1
         RTS       PC
;
;    WAIT FOR DONE
;
DONE:    BIT       #40,@#177170        ;TEST FOR DONE
         BEQ       DONE                ;WAIT UNTIL IT'S SET
```

```
;
;   DONE IS SET -- TEST FOR ERROR
;
        BIT     #100000,@#177170    ;ESTABLISH CONDITION CODES
        RTS     PC
```

NOTE: In normal use it is good practice to timeout waiting for TR.

Example #2

```
;
;   EXTENDED MODE WINCHESTER READ BLOCK, RX02 PROTOCOL
;
        MOV     #7,@#177170         ;ISSUE READ COMMAND (18-BIT ADDRESSING)
        MOV     #PARAM,R2           ;GET ADDRESS OF PARAMETERS
        MOV     #5,R0               ;GET PARAMETER COUNT
;
;   WAIT FOR TR OR DONE
;
30$:    BIT     #200,@#177170
        BNE     20$                  ;TR DETECTED
        BIT     #40,@#177170
        BEQ     30$                  ;DONE NOT SEEN
;
;   DONE SET BEFORE TR --> MAY BE AN ERROR
;
        BR      40$
;
;   ISSUE PARAMETERS
;
10$:    JSR     PC,TR               ;WAIT FOR TR
20$:    MOV     (R2)+,@#177172      ;WRITE PARAMETER (THIS CLEARS TR)
        DEC     R0
        BNE     10$                 ;LOOP UNTIL ALL PARAM. ISSUED
;
40$:    JSR     PC,DONE
        BEQ     EXIT
;
;   ERROR OCCURRED
;
        MOV     @#177172,R0         ;GET STATUS
        JSR     PC,REXST            ;PROCESS ERROR (APPLICATION DEPENENT)
;
EXIT:   RTS     PC
;
;   READ SECTOR PARAMETERS
;
PARAM:  .WORD   100002              ;UNIT DESIGNATOR: WINCHESTER UNIT 0,
;                                   ;PHYSICAL ADDRESS, ENABLE RETRIES,
;                                   ;ENABLE CORRECTION.
        .WORD     2                 ;DISK ADDRESS, HEAD 0, SECTOR 2
        .WORD     4                 ;CYLINDER 4
        .WORD  1000                 ;WORD COUNT
        .WORD  1000                 ;BUFFER ADDRESS
```

V. SYSTEM TESTING AND TROUBLE ISOLATION

A hierarchy of system testing is provided with all SMS FW controllers and systems. This hierarchy of testing is used to insure the system is operating correctly and, if a failure occurs, to isolate the failure to a major sub-component.

The following paragraphs detail the test programs available.

A. BOOT PROGRAM DIAGNOSTICS

Whenever the boot program (contained in PROM on the interface board) is executed, a simple host (e.g. LSI-11) CPU and memory test (up to 32 KW) is executed. Errors are reported on the console terminal (see section II-J for details).

If the CPU and memory test passes, some basic commands are issued to the controller to insure it is operational. If these tests pass, the boot program prints the 'DRV?' message and allows the boot operation to continue. If the tests fail, the boot program will either halt or hang (see section II-J).

B. CONTROLLER SELF TESTS AND DRIVE TEST

At power on or after an initialization, the user can elect, via the TEST switches, to run a self test or a drive test. The self test can be run continuously or bypassed.

To run the self test or drive test, turn power on, set the switches to the desired position (see section II-H or the overlay on the front panel), and then push the reset button.

Controller Self Test

The self test is a thorough functional test of the controller. As with all self tests, it cannot detect 100% of all possible errors, but, if the self test passes, there is a very high probability that the controller is operating correctly.

When the self test is run, if any errors are detected, the error will be reported via the light-emitting diodes (LED's) on the formatter board. If any error is detected, the controller will not set Done and will not accept any commands. The meaning of the LED's patterns during self test is shown in Table 9.

Drive Test

The drive test can be run either via the TEST switches or via a command issued by the host to the controller. The drive test exercises the controller and all ready drives. The test does not write to any drives, thus it will not overwrite any user data on the drives. The drive test will run continuously until an error is detected. When an error is detected the drive number of the suspect drive is displayed in the LED's (see Table 10) if it was run via the switches. If the drive test is run from the host, the error is reported in the normal manner in the CSR and the DBR.

When a drive test error occurs, insure that the diskettes are formatted and readable (if floppy error is indicated) and that all required cables and straps are installed. Also check drive power.

** WARNING **

If there is not an operational CPU and memory plugged into the backplane, the interface to formatter cable must be disconnected for the drive test to work correctly.

C. INSTALLATION AND TEST PROGRAM

The SMS Installation and Test program is contained on SMS diskette number 1001941 and described in SMS document number 3000500. The program serves two purposes: 1) it provides a variety of utility functions which allow the user to format his disks, install a flaw map on the Winchester, backup a Winchester to a floppy disk (at less than 1 minute per Mbyte), copy diskettes, etc.; 2) it provides system level diagnostic capability which can be run interactively from the system console.

The Installation and Test Program can be bootstrapped from the floppy as a standalone software system. This is its most typical mode of operation. The program can also be loaded and run as an RT-11 file. See document number 3000500 for details.

NOTE: The Installation and Test Program requires a minimum of 28K words of memory and assumes a standard configuration for the operator's console (vector at 60,64 and CSR at 177560).

TABLE 9. LED MEANING DURING SELF TEST

ERR1	ERR2	ERR3	Meaning
OFF	OFF	OFF	Passes all self tests
OFF	OFF	ON	Byte Processor Failure. Indicates that the formatter board is inoperative.
OFF	ON	OFF	8085 to Interface Board Failure. Indicates that the 8085 processor cannot communicate with the interface board. The interface board, formatter board or the cable between them could be bad.
OFF	ON	ON	8085 System Failure. Indicates an 8085 system component, such as an 8255 I/O port, has failed. Since the EPROM checksum and RAM test have passed, the 8085 itself is probably good. When this failure occurs, the formatter board is inoperative.
ON	OFF	OFF	RAM Failure. Indicates the RAM on the formatter board is faulty. The formatter board may be inoperative.
ON	OFF	ON	8085 EPROM Checksum Failure. Indicates either the 8085 or its program storage is faulty. When this failure occurs, the formatter board is inoperative.
ON	ON	OFF	Byte Processor to Interface Board Failure. Indicates that the byte processor cannot communicate with the interface board. The interface board, formatter board or cable between them could be bad.
ON	ON	ON	Formatter Inoperative. Indicates that the formatter board is inoperative. Check to insure DC power is correct and all socketted parts are seated firmly.

TABLE 10. LED MEANING DURING DRIVE TEST

ERR1	ERR2	ERR3	Meaning
ON	ON	ON	Floppy 0 suspect
ON	ON	OFF	Floppy 1 suspect
OFF	ON	ON	Winchester 0 suspect
OFF	ON	OFF	Winchester 1 suspect
ON	OFF	ON	No drives are ready.
OFF	OFF	OFF	Suspect Winchester 0 or 1. No seek complete indication or -12V power. All drive activity will cease.

Note: The equivalent LED's on the FWD0106 formatter are labelled CR1, CR2, and CR3.

D. TROUBLE ISOLATION GUIDE

This section of the manual outlines some steps to follow when the system is not operating as expected. A basic understanding of computer systems and console ODT is assumed.

Because the MDX unit is a complete computer system, it is both powerful and complex. It is not possible to isolate all failures in the field. However, many problems can be isolated and corrected by following the steps outlined below. These steps point out some of the most common problems. If trouble persists, please contact SMS.

Step 1: The first step is to establish communication between the computer and the system terminal.

If console ODT is working go to step 2.

If the terminal does not respond at all when the break key is pushed, or if the response is incorrect, check the following:

1) Baud rate on <u>both</u> the serial I/O board and on the terminal.

2) Is the correct cable between the terminal and MDX unit being used (pins 2 and 3 on the cable may have to be reversed)?

3) Insure there are no overlapped I/O addresses (i.e. if another I/O device were responding to the same CSR address as the terminal, neither would work).

4) Insure the cable is connected to the correct port on both the MDX and serial I/O board (with DLV11-J port 3 is the system console. On the back of the MDX, console/TTO normally connected to port 3 on the DLV11-J).

5) For console ODT to work, the CPU, memory and serial I/O boards must all be installed in the backplane and working. Insure there are no vacant slots between these boards.

6) If an LSI-11/2 is being used insure straps W1, W2, W3, W4 on the backplane are removed.

Step 2: Once console ODT is working, the next step is to execute the SMS boot and diagnostic program. See section II-J. If the boot program does <u>not</u> print 'DRV?', then check the following:

1) Line Time Clock (LTC) is off. Note: If the CPU is in power up mode 2, the LTC can be on since mode 2 will disable CPU interrupts.

2) If the boot diagnostics indicate CPU or memory problems, then corect the problems and attempt to boot again. Note: Insure the memory board is strapped to the correct starting address.

3) If the CSR address for the controller (normally 777170_8) could not be accessed, check the strapping on the interface board.

4) If no valid bootstrap block could be found then either a read error occurred or no program was on the disk(ette). Check for a read error by examining CSR address (normally 777170_8). If the most significant bit is set, an error occurred, and the error is in the DBR (normally 777172_8), bits 8-13. Note: Improper drive optioning can cause read errors. The drives must be optioned as shown in section II-I.

5) Any other halt or hang location indicates possible controller and/or CPU failures. However, these failures can also be caused by improper system configuration such as overlapped I/O or memory addresses. If the controller is suspected of being faulty, go to step 4.

Step 3: Booting the SMS Installation and Test Program

At this point the 'DRV?' prompt has been printed on the console. A typical operator response will be to type F0 (in upper case). If no valid bootstrap block could be found go to step 2 part 4. If the program appears to load (floppy LED comes on and head steps), but stops before printing the entire menu, then it is likely that interrupts are not being received. Insure all boards are inserted in the correct sequence with no vacant slots and that the interface board strapping is correct.

Note: The Installation and Test program requires a minimum of 28KW of memory and assumes the default I/O addresses and interrupt vectors for the controller and system console.

Step 4: Isolating Controller Failures

If the controller is suspected of being faulty, then:

1) Check the ERROR LED's. All LED's should be off. If they are on and blinking, check the self test (TEST SWITCHES) configuration. If they are on and not blinking, then the controller may be inoperative.

   Note: The interface board must be properly connected to the formatter board and must be installed in the CPU backplane with power applied to the backplane for the self test to pass (all LED's off).

2) If the LED's are off and power is applied, then examine the CSR register. After power on, it should be 4040_8 or 4440_8 (assuming a diskette is not installed in drive 0). If the CSR register cannot be accessed, insure the CSR address is strapped correctly. If the value in the CSR is not 4040_8 or 4440_8, insure the cable between the formatter and interface board is properly installed.

3) Execute the drive test by placing switches 1 and 2 in the off (open) position and pushing the Reset button on the MDX front panel. If the drive test fails disconnect the interface to formatter cable (40-pin very short cable) and push reset again. If it now works the CPU/memory is probably not operational, otherwise the formatter and/or drives are suspect. The drive test will work with the interface board connected to the formatter only if the CPU and memory are functional.

VI. WINCHESTER FLAW MANAGEMENT

A. OVERVIEW

Fixed Winchester disks are often shipped with known defects on the disk surface. These defects can vary from a bad bit to an entire bad track and thus can be a considerable management problem.

The defect information is provided to the user (disk purchaser) in the form of a defect map which normally lists the defect by cylinder, head, byte from index, and length of defect. The FW series disk controller provides complete bad sector/track management on the fixed disk by providing logical addressing capabilities and the capability to read/write a flaw map on the disk surface.

When the flaw management capabilities of the FW controller are used, any flaws will be automatically skipped when they are encountered. The host, if logical addressing is used, can thus view the disk as a series of consecutive records from 1 to N where N is the maximum number of records on the disk minus the number of flawed sectors (including the flaw map itself). The number N can be determined with the Read Extended status command.

The following paragraphs describe the details of flaw management done by the FW controller. In many applications the user may wish to use the SMS Installation Test Program to implement flaw management instead of writing additional programs.

All flaw management will be disabled if the formatter is strapped to do so.

At power on, (or after an initialize) if flaw management is enabled, the controller will attempt to read the flaw map from the disk into its internal memory. If a valid map is present it will then use the map to skip any flaws when logical addressing is used for disk accesses. If physical addressing is used an error is returned when a flawed sector is encountered.

If a valid flaw map is not present any read/write access will result in an error being reported. To prevent the controller from overwriting the flaw map, the sectors containing the flaw map are placed in the flaw map.

NOTE: Please refer to the FW Installation and Test Manual for additional flaw map information and for details on how to install the flaw map using the Installation and Test program.

B. FLAW MAP INITIALIZATION PROCEDURE

The following steps must be executed to initialize and write the flaw to a blank Winchester.

1) Format the Winchester.
2) Write the flaw map to the disk using the write flaw command. Only one sector per command can be written.
3) Initialize the controller to cause the flaw map to be read by the controller.
4) Scan the disk to insure all writes were successful.

C. FLAW MAP FORMAT

The first sector of the flaw map is called the pointer sector since it contains links to the remainder of the flaw map. The controller assumes the pointer sector is at cylinder 0, head 0, sector 1, or cylinder 0, head 1, sector 1. One or both can contain the pointer sector. See Figure 9.

The pointer sectors contain links (in the form of physical disk addresses) to two files. One is called the processed flaw data file and the other is called the raw flaw data file. The processed flaw data file contains a list of all flaws on the disk in physical disk address format (i.e. cylinder, head, sector). The raw flaw data file contains the flaw data as received from the Winchester manufacturer (e.g. track, byte from index, length of flaw). The controller does not read or make use of the raw flaw data file. It is used by the Installation and Test Program. By placing the raw flaw data on the disk it does not have to be re-entered each time the disk is formatted.

At power on the controller will read the pointer sector and then it will read into controller memory the processed flaw data. It is the user's responsibility to insure the pointer sector and the processed flaw data is in the correct format and that the flaw map itself is placed in the flaw map.

When the controller reads the processed flaw data, if the primary sector cannot be read it will try the alternate for that sector. The alternate and primary sector can be the same sector if desired. If neither the primary nor the alternate can be read, the appropriate error is reported.

The processed flaw data is arranged to allow simple and fast searching by the controller and must be in the format shown in Figures 9-12.

The processed flaw data can be a maximum of 256 bytes in size if there are two Winchesters in the system or 512 bytes if there is only one Winchester in the system. These maximum sizes are due to limits on controller memory size.

The alternate sectors must be placed in the map, however the alternate sectors can be the same as the primary sectors if desired.

All fill bytes must be as shown since the controller checks these to insure the pointer sector is valid.

In addition all track numbers and sector numbers must be in ascending order to allow binary searching.

BYTE	CONTENT	DESCRIPTION
0	$0AA_{16}$	Start marker
1	Drive Type	8=RESERVED, 9=ST506 COMPATIBLE, 10=RESERVED, 11=ST400 SERIES COMPATIBLE
2	0	Fill Byte
3	0	Fill Byte
4	Sector*	Pointer to first primary sector of processed flaw data
5	Head	
6	Cylinder - LSB	
7	Cylinder - MSB	
8	Sector*	Pointer to alternate first sector for processed flaw data
9	Head	
10	Cylinder - LSB	
11	Cylinder - MSB	
12	Sector*	Pointer to second primary sector of processed flaw data
13	Head	
14	Cylinder - LSB	
15	Cylinder - MSB	
16	Sector*	Pointer to alternate second sector of processed flaw data
17	Head	
18	Cylinder - LSB	
19	Cylinder - MSB	
20		Pointers to raw flaw data (Same format as above)
.		
.		
.		
36		
37	0	Not used
.	.	
.	.	
.	.	
100	$0FF_{16}$	Fill
101	0	
102	$0FF_{16}$	
103	0	
104	$0FF_{16}$	
.	.	
.	.	Alternating 0, FF's
.	.	
127		Fill

*A zero in the first byte of the disk address terminates the string.

Figure 9. Flaw Map Pointer Sector Format.

BYTE	MNEMONIC	DESCRIPTION
0	NT	Number of flawed tracks on the disk.
1,2	T1	Bad track number* (LSB first)
3,4	O1	Offset to sector table in bytes (LSB first)
5,6	T2	Bad track number
7,8	O2	Offset to sector table in bytes
		.
		. (repeated NT times)
		.
;Sector table		
O1	NS1	Number of bad sectors on first bad track (0 => entire track is bad)
O1+1	S1	List of bad sectors on first bad track
O1+2	S2	
.	S3	
.	S4	
O2	NS2	Number of bad sectors on second bad track
O2+1	S1	List of bad sectors on second bad track
.	S2	
.	S3	
.	S4	

*Track Number = (Cylinder address * number of moving heads) + head address

Figure 10. Processed Flaw Map Data Sector Format

BYTE	CONTENT (HEX)	DESCRIPTION
0	AA	Marker
1	11	ST400 series drive
2	0	
3	0	
4	2	Sector 2
5	0	Head 0
6	0	Cylinder 0
7	0	
8	3	Alternate for processed flaw data
9	0	
10	0	
11	0	
12	0	Terminator (only 1 sector of data)
.		used by controller
.		
.		
100	FF	
.	0	
.	FF	
.	0	
.	.	
.	.	
.	.	
127	0	

Figure 11. Flaw Map Pointer Sector Example

BYTE	CONTENT	DESCRIPTION
0	5	Number of flawed tracks
1,2	0,0	Track 0 flawed (flaw map itself)
3,4	17,0	Offset to sector table (LSB first)
5,6	5,0	Track 5 flawed
7,8	21,0	Offset
9,10	111,0	Track 111 flawed
11,12	23,0	Offset
13,14	171,0	Track 171 flawed
15,16	24,0	Offset
17	3	Number of flawed sectors on track 0
18	1	Sectors 1,2,3 are the flaw map itself
19	2	
20	3	
21	1	Number of flawed sectors on track 5
22	7	Sector 7 is flawed
23	0	All sectors on track 111 are bad
24	6	Number of flawed sectors on track 171
25	2	Sectors 2,8,10,11,12,13 are flawed on
26	8	track 171
27	10	
28	11	
29	12	
30	13	
31	--	Not used by the controller
.		
.		
.		
127		

Figure 12. Processed Flaw Map Data Example

D. PROCESSING THE RAW FLAW DATA

The method of reporting Winchester flaws is determined by the drive manufacturers. Some manuacturers report flaws by giving the track, head, byte from index and number of bits in the flaw. Others report a sector, head and track and assume a known format (e.g. 256 bytes/sector with so many bytes of overhead, etc.). Flaws are typically found by the drive manufacturer's analog techniques which require special equipment. A flaw does not necessarily mean a sector cannot be read/written, but simply that the flaw will result in higher soft error rates. Thus, simply scanning a disk may not be sufficient to find all flaws on a disk (i.e. the manufacturer's raw flaw data must be used).

The determination of the sector in which a flaw will appear depends on many factors. The disk format, head step/switch offsets and interleave must all be taken into account. For soft sectored drives the rotational tolerance of the drive also plays a key role in determining which sectors to flaw.

Accordingly, SMS has developed a set of rules for processing the manufacturer's flaw data. These rules have been implemented in the FW Installation and Test Program (see section V-C) and are described in the FW Installation and Test manual.

VII. SYSTEM MAINTENANCE

A. PREVENTIVE MAINTENANCE

Air Filter Cleaning

The air filter on the rear of the MDX should be cleaned periodically. To remove the filter simply turn AC power off and pull the filter out. It can be cleaned in soap and water if desired.

Floppy Disk Maintenance

A head cleaning kit (available from Shugart, SA111 P/N 54612) can be used to clean the floppy read/write heads. The normal preventative maintenance is to clean the heads once a month at 25% duty cycles or 40 hours of usage, whichever occurs first. An alternative is to clean the heads when a read error occurs (CRC error) especially when excessive diskette wear has been noticed.

B. ENCLOSURE DISASSEMBLY

The MDX chassis has been designed to allow replacement of all major subassemblies and components in the field. The following sections describe how to remove all major components and subassemblies. In all cases component installation is the reversal of the removal.

WARNING: Always disconnect AC power before beginning any chassis disassembly.

Winchester Drive Removal

1. Disconnect the 34- and 20-pin flat ribbon cables.
2. Remove the four screws (Phillips flathead 6-32) which hold the drive to the side wall of the MDX.
3. Raise the drive slightly and disconnect the DC power cable.
4. Pull the drive straight up and out of the MDX chassis.

Floppy Drive Removal

1. Disconnect the 50-pin flat ribbon cable and the DC power cable.
2. Remove the two mounting screws (pan head 8-32) which connect the card cage side wall to the floppy mounting bracket.
3. Pull the floppy with its mounting bracket up and out of the MDX chassis.
4. Remove the mounting bracket from the drive.

Fan Removal

1. The fan is mounted to the chassis rear panel by four screws (outermost pan head 6-32 by 1-1/8"). Remove these four screws.

2. The fan should now be loose in the chassis. Disconnect the AC power from the fan and pull the fan out of the chassis.

Formatter Board Removal

1. Pull the formatter free from the backplane by 1-2 inches.

2. Disconnect the 50-, 34- and 20-pin flat ribbon cables, being careful to leave the 50- and 34-pin cables in the cable holder attached to the side wall of the card cage.

3. Pull the formatter out of the card cage.

Power Supply Values

Note: The MDX power supply is not field adjustable. Power supply levels should be as follows:

+5 volts measured at front panel test point:	4.85 to 5.20
±12 volts measured at front panel test point:	11.40 to 12.60
+24 volts measured at the floppy DC power connector (yellow wire is +24, black is ground):	21.60 to 25.60

Power Supply Removal

1. Remove the backpanel by removing the 8 screws (flat head, Phillips, 6-32) which attach it to the main chassis.

2. Disconnect the DC/AC harness from the power supply.

3. Remove the 1/4" copper chassis to logic ground strap and bolt.

4. Remove the four screws (Phillips flat head, 8-32) which attach the power supply to the MDX main chassis.

5. Slide the power supply out. The power supply shield does not have to be removed.

TABLE 11. MDX SYSTEM MAJOR REPLACEABLE ASSEMBLIES

0004262-0001	Panel, Rear
0004158-0001	Plate, Mtg., D-Connector
0004177-0001	Barrier, Conn. Plate (2)
0003851-0001	Holder, Flat Cable Bundle
0003943-0001	Frame, Air Filter
0003947-0001	Barrier, Filter
0003976-0001	Filter, Air
0004267-0001	PWB Assy, AC Filter/Dist.
0004291-0001	AC Input Harness Assy
0004290-0001	Fan Assembly
9000974-0001	Circuit Breaker, Rocker, DPST
0004299-0001	Cable Assy, Drive Signal, H/D
9000959-0001	Power Supply
0004296-0001	Wiring Harness, Drives
0004315-0001	PWB Assy, MDX Backplane
0004271-0001	Chassis
0004272-0001	Enclosure, Card File
0004287-0001	Adapter, Tandon Drive
0004289-0001	Shield, Power Supply
0003752-0001	Bar, Connector, PWB (2)
0004265-0001	Bezel
0004276-0001	Panel Assy, Hinged Front
0004275-0001	Panel Assy, Bottom Front
0004273-0001	Cover, Top
0004293-0001	Cable Assy, Interface I/O
0004298-0001	Cable Assy, Drive Signal, Tandon
0004294-0001	Cable Assy, Drive Data, H/D
0004274-0001	Panel Assy, Top, Front
0004277-0001	Label, Switch Matrix
0004278-0001	Overlay, Hinged Panel
0004280-0001	Overlay, Blanch, Top Panel
0004283-0001	Overlay, MDX
0004285-0001	Overlay, Switch
1002001-0001	Top PWB Assy, FWD0106 Formatter
1001939-0001	Interface Board Assy
0004282-0001	Retainer, PC, Card