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Sun-3/E SCSI/Ethernet Board Hardware Reference Manual

Sun Microsystems, Inc. • 2550 Garcia Avenue • Mountain View, CA 94043 • 415-960-1300

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Introduction

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Introduction

This manual describes the Sun-3/E SCSI/Ethernet Controller Board (S3SE) for system programmers and engineers who wish to integrate this board into their systems.

The S3SE board (501-8027) is a standard double-height Revision B VMEBus board that provides one Ethernet interface, and one SCSI interface.

1.1. Using This Manual

This section provides information to help you use this manual. It includes a description of the manual and the intended audience, a list of the different fonts, a description of how the fonts are used, a glossary, and a list of references.

Note that this board should be used with the Sun-3/E CPU, which is described in the *Sun-3/E CPU Hardware Reference Manual* (pn # 800-8028).

NOTE *This board does NOT include a licensed Ethernet address. An Ethernet address must be downloaded to the Ethernet circuits in this board from the Sun-3/E CPU board, which includes a licensed Ethernet address, or from some other source.*

Audience

The audience includes anyone interested in understanding the S3SE board architecture at a block level. This might include designers, engineers, programmers, technicians, and anyone else who wants or needs to know how the S3SE works.

Note that this manual concerns itself with external signals and timings; for internal signals and timings, see the *Sun S3SE Engineering Manual.*

Fonts in Text

In this manual, we use the following fonts to make things more clear:

- Roman font is the normal font used for text.
- *Italic font* is used for the proper name of a text or chapter to be referred to for additional information. For example:

  For more on loopback mode, see the Intel *LAN Component User's Manual.*

- **Bold font** indicates that a word or phrase requires additional emphasis. For example:

  The **host processor** uses the bits in this register to communicate with the SCSI interface.

Glossary

The following paragraphs list and describe the words and acronyms used in this manual:

- S3SE — The Sun-3/E SCSI/Ethernet Board.
- SBC — SCSI Bus Controller. This is the NCR 5380 SCSI Bus Controller chip.
- DMA — Direct Memory Access. A method of transferring large blocks of data
- EDLC — Ethernet Data Link Controller. The Intel 85286 Ethernet chip.

References

For additional information, see:

- Intel *LAN Component User's Manual* — For programming information on the Inter 85286 Ethernet Controller chip.
- *NCR 5380 SCSI Controller Design Manual* — For information on programming the NCR 5380 SCSI Bus Controller.
- The *Sun-3/E CPU Hardware Reference Manual* — For information about the Sun-3/E CPU board. (The S3SE board is almost always used with a Sun-3/E CPU.)
- Manual for AMD 7990 Thin Ethernet transceiver

2

Unpackaging and Handling

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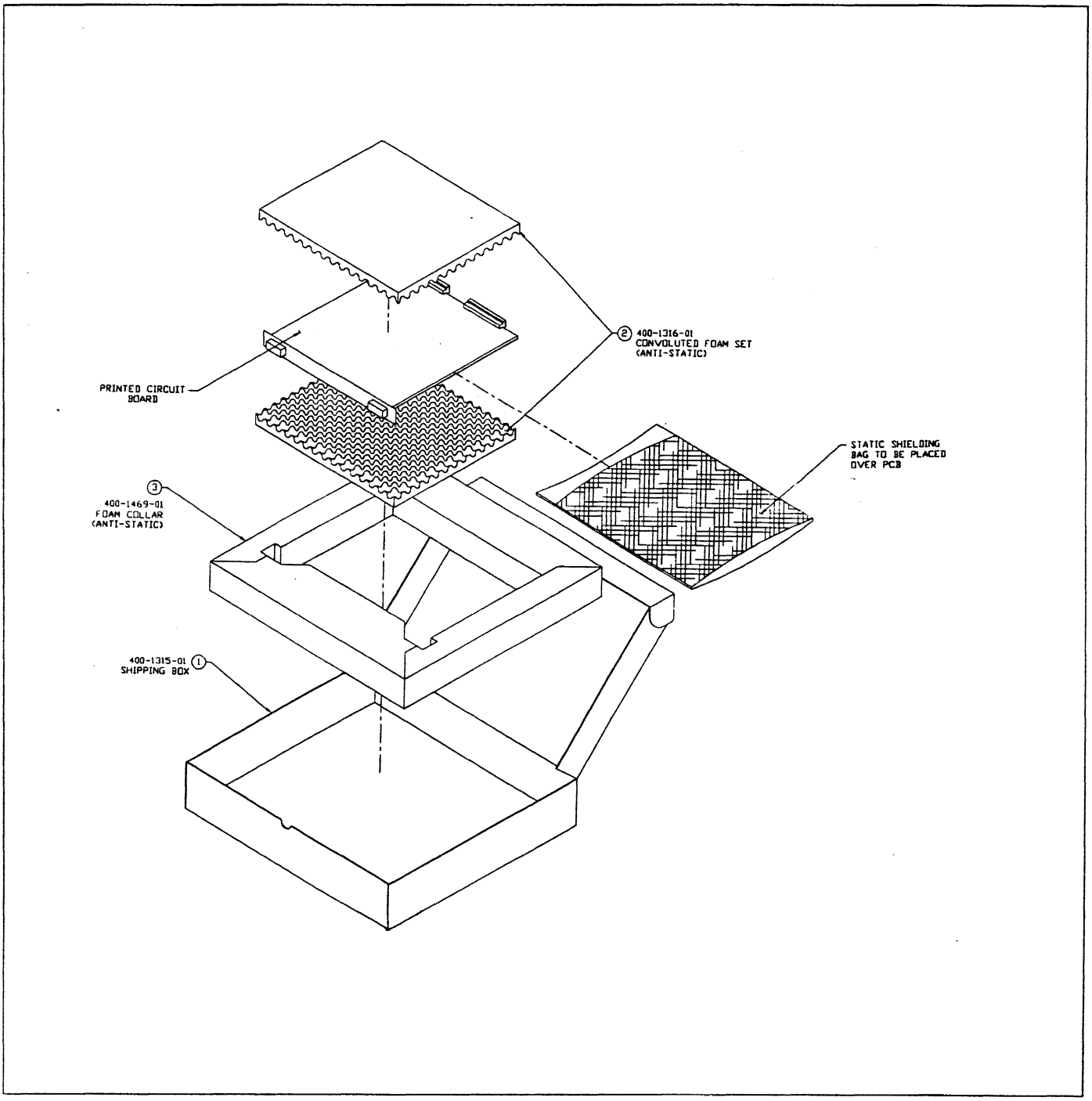
Unpackaging and Handling

Sun-3/E boards are shipped in either individual containers or in 10-board tote boxes. Inside either, the PC board is wrapped in an anti-static bag. Inside the individual boxes, it is further protected by two pieces of anti-static foam, one below it and one above. Inside the 10-board tote boxes, it is further protected by corregated partitions.

CAUTION **To avoid damaging the board, keep it in its anti-static bag for as long as possible, and handle it only by its edges. Any person handling the board when it is not in its anti-static bag should be wearing grounding straps, and should only handle the board by its edges.**

A single-board container appears in the following figure:

Figure 2-1 *Shipping Container*



3

Board Architecture

3

Board Architecture

The Sun-3/E SCSI/Ethernet board is a dual-purpose VMEbus slave device that provides a SCSI interface and an Ethernet interface.

The SCSI interface is similar to the SUN-3/50, except that it has a 64-kilobyte buffer memory instead of a FIFO. It can transfer data at a maximum rate of 2.6 megabytes/sec.

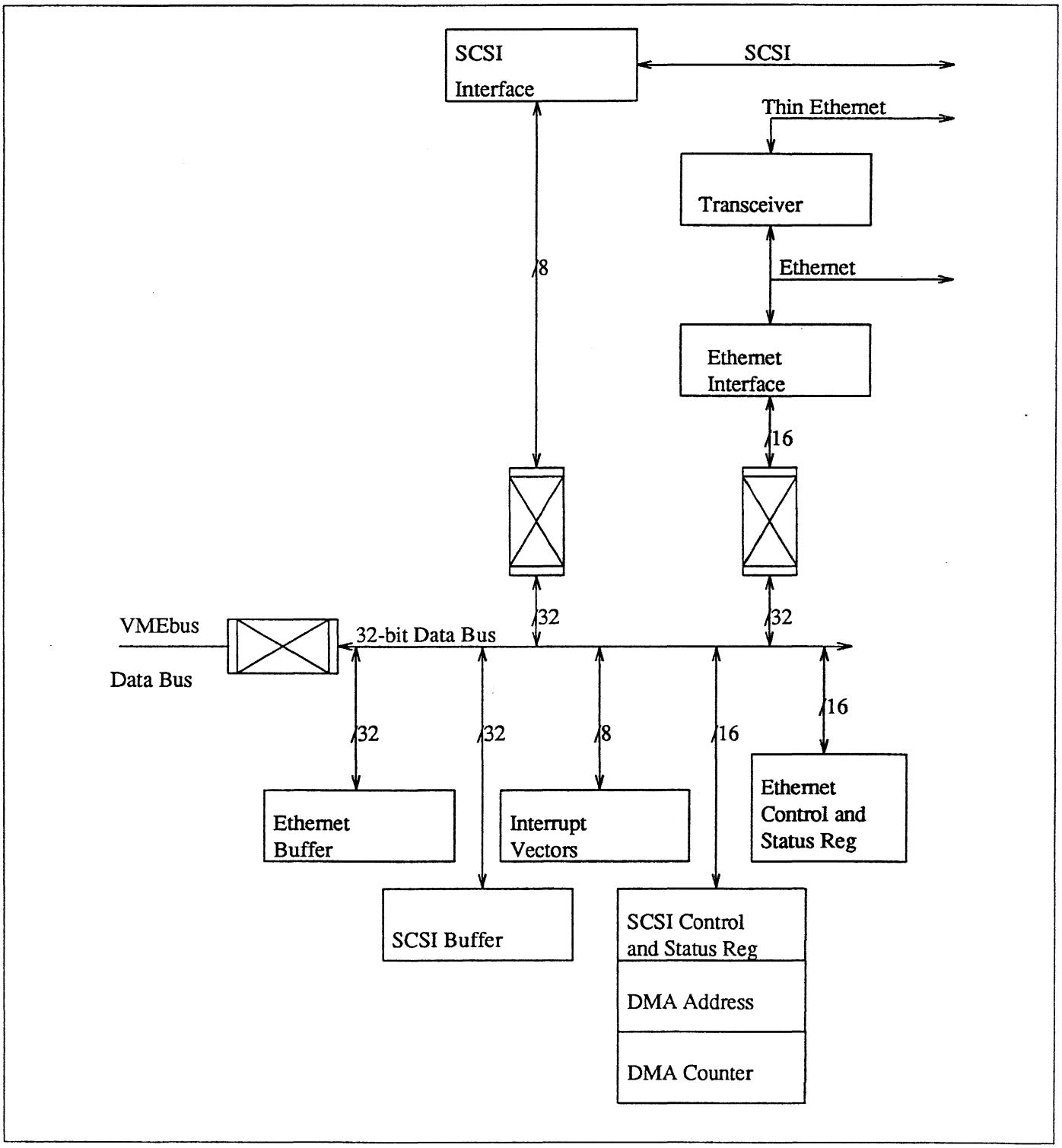
The Ethernet interface is based on the Intel 82586 Ethernet Controller. It features 128 kilobytes of on-board buffer memory, and can transfer data from the Ethernet into the on-board buffer memory at a maximum (estimated) rate of 5.3 megabytes/sec.

The Ethernet interface can also be switch-selected to support a "Thin Ethernet" (cheapernet). The thin Ethernet interface includes a transceiver on the board.

NOTE *This board does NOT include a licensed Ethernet address. An Ethernet address must be downloaded to the Ethernet circuits in this board from the Sun-3/E CPU board, which includes a licensed Ethernet address, or from some other source.*

A block diagram of the board appears in the following figure:

Figure 3-1 *S3SE Block Diagram*



3.1. Addressing and Jumpering

Switch 1 of SWO201 selects either 32-bit or 24-bit VMEbus addressing. If this switch is open (OFF) the board uses 24-bit addressing; if if is closed (ON) the board uses 32-bit addressing.

In 32-bit addressing mode, VMEbus address bits A[31:18] select the board; with 24-bit addressing, VMEbus address bits A[23:18] select the board.

The actual board location in the VMEbus address space is selected by switch packs SWO201 and SWO202. Each address bit is assigned to a switch; when the switch is open (OFF), the bit is set to 1 and when the switch is closed (ON), the bit is set to 0. Comparators compare these assignments to the actual VMEbus address bits and select the board when they match.

The switch-to-address bit assignments are as follows:

Table 3-1 *Address Switch Assignment*

DIP switch number	Switch	Address Bit
SWO201	1	24- or 32-bit addressing (ON = 32-bit)
	2	Unused
	3	A[18]
	4	A[19]
	5	A[20]
	6	A[21]
	7	A[22]
	8	A[23]
SWO202	1	A24]
	2	A[25]
	3	A[26]
	4	A[27]
	5	A[28]
	6	A[29]
	7	A[30]
	8	A[31]

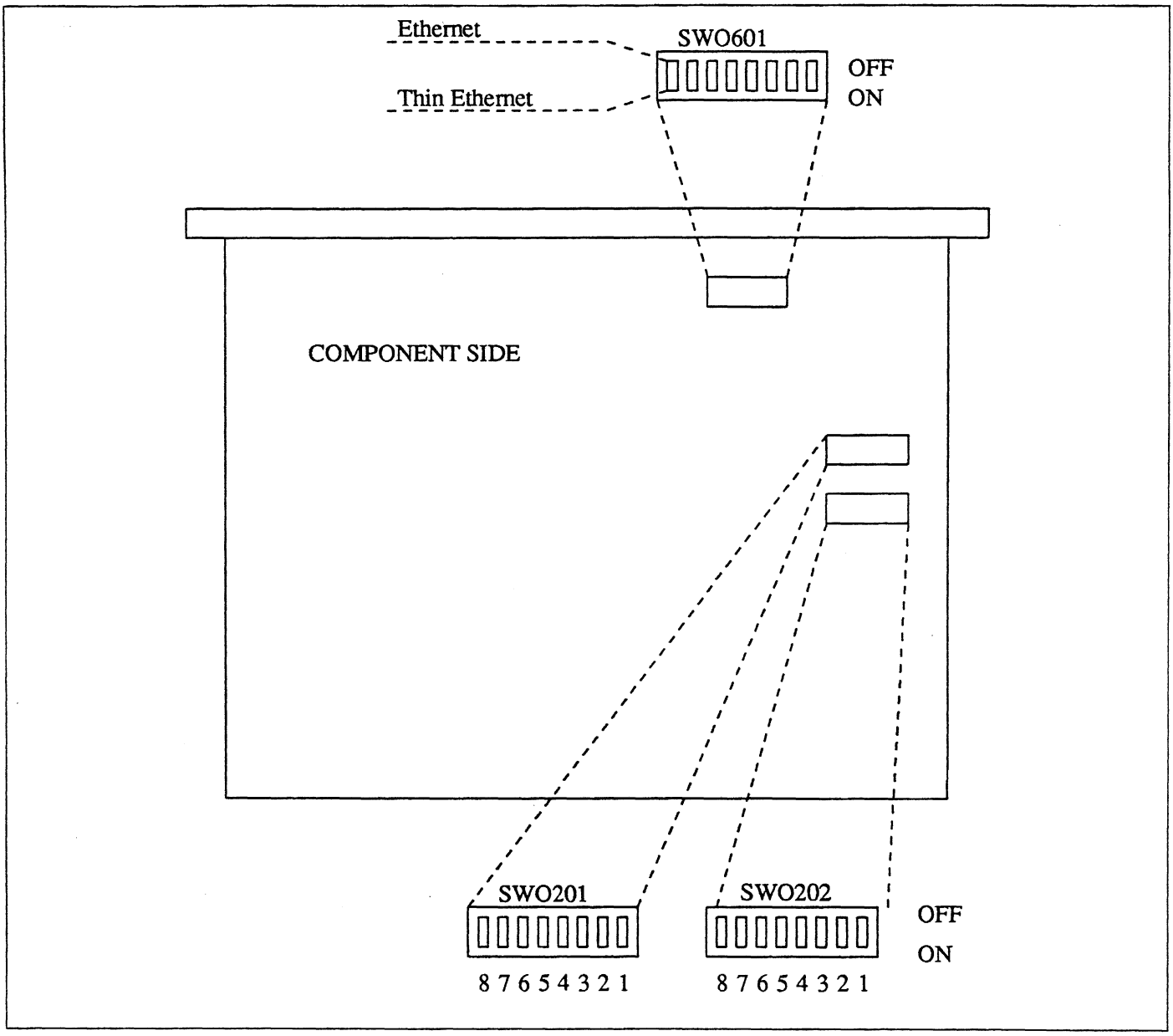
VMEbus bits A[17:0] select addresses on the board. Bits A18 and above form a base, and local addresses are offset from this base. The buffers and control/status registers are located in this space at the following addresses:

Table 3-2 *Board Device Addressing*

Name	Beginning Address	Size
Ethernet Buffer	Base + 0x20000	0x20000
SCSI Buffer	Base + 0x0	0x10000
Ethernet Control and Status Reg	Base + 0x1FF02	0x2
SCSI Control and Status Reg	Base + 0x1001A	0x2
SCSI DMA Address	Base + 0x1000A	0x2
SCSI DMA Counter	Base + 0x1000E	0x2
Interrupt Vector (Level 2)	Base + 0x1001E	0x1
Interrupt Vector (Level 3)	Base + 0x1FF12	0x1
SCSI Bus Controller	Base + 0x10000	0x8

The locations of SW01 and SW02 appear in Figure 3-2.

Figure 3-2 *Switch Locations*



3.2. Interrupts

The S3SE board generates VMEbus level 2 and level 3 interrupts. The SCSI interface causes level 2 interrupts and the Ethernet interface causes level 3 interrupts.

The architecture provides two 8-bit registers, one for each interrupt level. The host processor must load these registers with the board status/ID bits as defined by the VMEbus specification, then when an interrupt occurs, the board outputs the contents of these registers on D[07:00]. The interrupt handler must look in the appropriate SBC or Ethernet Interface internal register to learn the exact cause of the interrupt.

3.3. Bandwidth and Capability

The following table shows the estimated bandwidths of the SCSI, Ethernet, and VMEbus:

Table 3-3 *Estimated Board Bandwidths*

Interface	Bandwidth
SCSI to buffer	2.6 Mb/Sec
Ethernet to buffer	5.3 Mb/Sec
VMEbus	6.4 Mb/Sec

The S3SE board uses a 8Mhz square wave for its internal clock.

3.4. Cycle Priorities

Because the S3SE board can only process one cycle at a time, it must set priorities in case requests come in simultaneously. The following priorities are implemented in internal firmware:

DMA from Ethernet interface to Ethernet buffer (highest)

DMA from SCSI interface to SCSI buffer

VMEbus access to S3SE board

VMEbus interrupt acknowledge from S3SE board (lowest)

Note that because the board bandwidths (Table 3-3) exceed SCSI and Ethernet data rates, the S3SE is fully capable of handling SCSI and Ethernet transfers simultaneously.

4

SCSI Interface

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SCSI Interface

The SCSI interface uses an NCR 5380 SCSI Bus Controller (SBC). It should be programmed for non-block DMA transfer mode, causing the SBC to generate a DRQ for each byte transferred.

For additional information see *NCR 5380 SCSI Interface Chip Design Manual*, the manual for disk drive (controller), and the *Small Computer System Interface (SCSI) Specification*

4.1. Control and Status Registers

The host processor communicates with the SBC through 1) the SCSI Control and Status Register, 2) the SCSI DMA address register, 3) the SCSI DMA address counter, and 4) the NCR 5380 SBC's control registers. The following sections describe each of these.

NOTE *In this chapter, we assume that the SCSI interface supports a disk drive. Actually, it can control any device which conforms to the SCSI specification.*

SCSI Control and Status Register

The SCSI Control and Status Register is located in the board's VMEbus space at 0x1001A. The host processor writes information to this register to control the SCSI interface, and it reads information from this register to learn the status of the SCSI interface.

The meaning of these bits changes depending on whether the register is read or written. When it is written, the bits control the SCSI interface; when it is read, it provides status information to the host processor. Both reads and writes must be 16 bits.

The following table shows the bit values:

Table 4-1 *SCSI Control and Status Register Bits*

Bit	Control (Writes)	Status (Reads)
D0	SCSI Reset*	SCSI Reset*
D1	Unused	1
D2	SBC Interrupt Enable	SBC Interrupt Enable
D3	SCSI Send	SCSI Send
D4	Unused	0
D5	Unused	0
D6	Unused	0
D7	Unused	0
D8	Unused	0
D9	Unused	SBC Interrupt
D10	Unused	1
D11	Unused	0
D12	Unused	0
D13	Unused	0
D14	Unused	0
D15	Unused	0

The bits have the following meanings:

SCSI Reset* (active LOW)
: When sent by the host processor this bit resets the SCSI interface; reading it only reads back the state that the host processor set it to.

SCSI Interrupt Enable (active HIGH)
: Writing this bit enables interrupts to be sent from the SCSI chip to the host processor. Note that the SBC must assert SBC Interrupt for the interrupt to be posted.

SCSI Send (active HIGH)
: The host processor writes this bit to control the direction of data flow over the SCSI interface; 1 = write (to disk), 0 = read (from disk).

SCSI Interrupt (active HIGH)
: The SBC asserts this bit to cause an interrupt. Note that the interrupt will not actually be posted to the VMEbus interface unless the SCSI Interrupt Enable bit is ON.

SCSI DMA Address and SCSI DMA Counter

The host processor uses these two registers to tell the SCSI circuits where in the buffer it is to read or write from, and how many (bytes) it is to read/write. The SCSI DMA Address Register is at 0x1000A, and the SCSI DMA Counter is at 0x1000E.

Before the SCSI interface can do DMA, the host processor must load the DMA address register with the starting address and the DMA counter with the number of bytes to be transferred. The DMA counter is decremented for every byte transferred, and when it reaches zero, the hardware asserts EOP.

EOP will only be asserted on a write operation. On a read, a Bus Phase Mismatch will occur in the transition from Data In to Status.

These are both 16-bit read/write registers.

NCR 5380 Bus Controller Registers

The NCR 5380 SCSI Bus Controller chip has eight internal registers that it uses to receive instructions and report status. These are located at addresses 0x10000 to 0x10007 in the board's VMEbus address space. It can be set up to interrupt on phase mismatch, EOP from DMA, and a number of other conditions, as specified in the NCR manual.

For details about the contents of these registers, see the *NCR 5380 SCSI Interface Chip Manual.*

Note that the NCR 5380 should be set up for for non-block DMA transfer mode (this causes DRQ to be generated for every byte transferred).

Disk Controller Control Blocks

The SCSI interface requires control blocks to be sent to the disk controller as part of the data stream. These should be constructed in the SCSI buffer to be sent with the data to the disk. Sun recommends that these blocks be sent to the SCSI buffer as programmed I/O.

For the contents and format of these blocks, see the manual for the disk controller being used.

4.2. SCSI Buffer

The SCSI buffer is a 64-kilobyte block of memory located at addresses 0x0 to 0x0x0FFFF in the S3SE's VMEbus address space. It is organized as 16K long-words, but it can be accessed by the VMEBus as an 8-bit, 16-bit, or 32-bit device. It is accessed by the SCSI bus controller in 8-bit DMA mode.

4.3. SCSI Reads and Writes

The SCSI circuits use the 64 kilobyte SCSI buffer to buffer data between the host processor and the SCSI interface. For reads, the SCSI circuits load the information from the disk to the buffer, and the host processor must read the buffer. For writes, the host processor must load the buffer, then tell the SCSI circuits to write this information out on the SCSI interface.

Reads require the following sequence:

Set up the control/status register, the DMA address register, and the DMA counter.

Program the SCSI chip and start the sequence as described in the *NCR 5380 SCSI Interface Chip Design Manual.*

The SCSI/DMA circuits load the required information from the disk to the SCSI buffer.

When it's done, the hardware generates a level 2 interrupt. The host processor should respond to this interrupt by reading the data from the SCSI buffer.

The sequence for writes is similar to the sequence for reads. However, before the sequence starts, the host processor must load the data to be written to the disk into the SCSI buffer. Note that upon successful completion of a write, there is one additional cycle, so that the DMA count register will not equal 0, but 0xFFFF, and the DMA address register will be incremented by 1 more than the actual count.

5

Ethernet Interface

5

Ethernet Interface

The Ethernet interface contains an Intel 82586 EDLC Ethernet controller chip, a 128 kilobyte Ethernet buffer, an Ethernet control and status register, and a jumper-selectable AMD 7995/6 Thin Ethernet transceiver.

Most communication with the Ethernet interface is through the control blocks in the Ethernet buffer space. The first block, called the System Configuration Pointer, lives in the 6 high bytes of the Ethernet buffer space (base + (0x3FFF6 to 0x3FFFF)). This block contains a pointer to the other Ethernet control blocks, and a bit specifying the width of the bus from the Ethernet buffer to the Ethernet interface (16 bits).

For additional details see the Intel *Local Area Network (LAN) Components User's Manual.*

Another register, called the Ethernet Control and Status register, enables the host processor to communicate with the board hardware. It is a 16-bit read/write register located at address (base + 0x1FF02).

It contains the following bits:

Table 5-1 *Ethernet Control and Status Register Bits*

Bit	Name
D0 through D7	0
D8	EDLC Interrupt
D9	0
D10	0
D11	0
D12	Interrupt Enable
D13	Channel Attention
D14	Loop Back
D15	EDLC Reset

These bits perform the following functions:

EDLC Interrupt (active HIGH

The 82586 activates this bit when it needs to interrupt the host processor. Note that the interrupt is not actually posted unless the Interrupt Enable bit is ON.

Interrupt Enable (active HIGH)
This bit enables the EDLC to post an interrupt to the host processor. Only the host processor can write this bit.

Channel Attention (active HIGH))
When the host processor writes this bit, it sends a channel attention to the EDLC.

Loop Back (active HIGH))
The host processor writes this bit to place the Ethernet serial interface adapter in loopback mode. For more on loopback mode, see the *LAN Component User's Manual.*

EDLC Reset (active HIGH)
This pin causes the hardware to reset the 82586.

5.1. Ethernet Address

The S3SE board does not provide a fixed Ethernet address. A licensed Ethernet address must be downloaded from the host processor into the control space in the Ethernet buffer.

The Sun-3/E CPU board contains a valid Ethernet address in its IDPROM. See the *Sun-3/E CPU Hardware Reference Manual* (#800-8028) for more details.

5.2. Ethernet Transmits and Receives

The Ethernet control registers are in the Ethernet buffer; there are no separate Ethernet control registers.

Ethernet transmits take the following steps:

The host processor must construct a control block in the Ethernet buffer starting (base + 3FFF6). (This only needs to be done once, when the chip is initialized) The contents of this buffer are described in the Intel *Local Area Network (LAN) Components User's Manual.*

The host processor must also load the data it wants to send over the Ethernet into the Ethernet buffer.

When the Ethernet chip receives a channel attention, it fetches the control block.

The contents of the control block tell the 82586 chip the location of the data in the buffer, and where to send it. (Actually, the control block points to other control blocks which contain the actual location).

The Ethernet circuits do DMA from the buffer to the Ethernet output, then they update the control block.

When they are done, the Ethernet circuits interrupt the host processor with a level 3 interrupt. The host processor should respond by reading the updated control block.

Ethernet receives are similar to transmits:

During power-up, the host processor should load the Ethernet control block with the address where the Ethernet circuits are to place received data, then it should issue a channel attention to get the Ethernet circuits to read the control block.

When packets come over the Ethernet, the Ethernet circuits use DMA to write them into the address specified by the host processor in the control block. Then the Ethernet circuits update the control block and post a level 3 interrupt to the host processor.

The host processor should read the contents of the Ethernet buffer over the VMEBus.

5.3. Ethernet Buffer

The Ethernet buffer is a 128 kilobyte memory block located at addresses base + (0x20000 to 0x3FFFF). It is organized as 32K longwords, but it can be addressed by the VMEbus as either an 8-bit, 16-bit, or a 32-bit device. The Ethernet interface can access it in 16-bit DMA mode.

Note that the only hard assigned address in this space is the EDLC system configuration pointer, which lives are base + (3FFF6 to 3FFFF). **This behavior is built into the EDLC chip**. System software must assign all other locations, and the system configuration pointer serves as a pointer to these.

5.4. Thin Ethernet

Switch SW0601 switches the Ethernet signal from the Ethernet connector to the Thin Ethernet connector. The AMD7995/6 transceiver drives a standard 50 ohm coaxial cable directly. It is electrically compatible with the standard Ethernet but it is spec'ed for one third the maximum length of standard Ethernet.

To switch from standard to thin Ethernet, set all switches on SW0601 ON (CLOSED). To switch from thin Ethernet to standard Ethernet, set all the switches on SW601 OFF (OPEN).

Figure 3-2 shows the location of SWO601.

5.5. External Transceiver

The Sun-3/E SCSI/Ethernet board is designed to be used with a Level 2 external Ethernet transceiver.

6

VMEbus Interface

6

VMEbus Interface

The host processor communicates with the S3SE board over a standard Revision B VMEBus. The VMEbus interface consists of the control logic, the data buffer, the board selection logic, and the interrupt logic.

The S3SE board occupies 256 kilobytes of VMEbus address space. The location of the board in the VMEbus address space, and whether the board uses 24-bit or 32-bit VMEbus addressing can be selected by switches, as described in the chapter *Board Architecture*.

The S3SE board is a VMEbus slave; all transfers are initiated by the host processor.

The board has the following VMEbus parameters:

Table 6-1 *VMEbus Parameters*

Name	Title	Capability
Data Bus Size	D32 SLAVE (DYN)	32, 16, or 8 bits
Address Bus Size	A32, A24 (STAT)	32- and 24-bit addresses
Sequential Access	None	
Interrupter Options	D08(0)	8-Bit Status/ID
	I(2,3)	Level 2 = SCSI
		Level 3 = Ethernet
	RORA	Release on Register Access

A

Connectors

A

Connectors

This appendix describes the exterior connectors on the S3SE board. These include the SCSI connector, the Ethernet connector, the Thin Ethernet connector, and the rear-edge connectors, P1 and P2.

A.1. Rear Edge Connectors

The rear edge contains two connectors, P1 and P2. They are both standard 96 pin Eurodin connectors. P1 and row B (the middle row) of P2 comprise the VMEbus pins, and rows A and C of P2 are not used.

The following two tables list the rear connector pins:

Table A-1 *P1 Connector Pins*

P1A pin	Signal	P1B pin	Signal	P1C pin	Signal
1	P1.D00	33	P1.BBSY*	65	P1.D08
2	P1.D01	34	Unused	66	P1.D09
3	P1.D02	35	Unused	67	D1.D10
4	P1.D03	36	P1.BGOIN*	68	P1.D11
5	P1.D04	37	P1.BGOUT*	69	P1.D12
6	P1.D05	38	P1.BG1IN*	70	P1.D13
7	P1.D06	39	P1.BG1OUT*	71	P1.D14
8	P1.D07	40	P1.BG2IN*	72	P1.D15
9	GND	41	P1.BG2OUT*	73	GND
10	P1.CLK*	42	P1.BG3IN*	74	Unused
11	GND	43	P1.BG3OUT*	75	P1.BERR*
12	P1.DS1*	44	P1.BR0*	76	P1.SYSR*
13	P1.DS0*	45	P1.BR1*	77	P1.LWORD*
14	P1.WRITE*	46	P1.BR2*	78	P1.AM5
15	GND	47	P1.BR3*	79	P1.A23
16	P1.DTACK*	48	P1.AM0	80	P1.A22
17	GND	49	P1.AM1	81	P1.A21
18	P1.AS*	50	P1.AM2	82	P1.A20
19	GND	51	P1.AM3	83	P1.A19
20	P1.IACK*	52	GND	84	P1.A18
21	P1.IACKIN*	53	Unused	85	P1.A17
22	P1.IACKOUT*	54	Unused	86	P1.A16
23	P1.AM4	55	GND	87	P1.A15
24	P1.A07	56	P1.IRQ7*	88	P1.A14
25	P1.A06	57	P1.IRQ6*	89	P1.A13

Table A-1 *P1 Connector Pins— Continued*

P1A pin	Signal	P1B pin	Signal	P1C pin	Signal
26	P1.A05	58	P1.IRQ5*	90	P1.A12
27	P1.A04	59	P1.IRQ4*	91	P1.A11
28	P1.A03	60	P1.IRQ3*	92	P1.A10
29	P1.A02	61	P1.IRQ2*	93	P1.A09
30	P1.A01	62	P1.IRQ1*	94	P1.A08
31	Unused	63	Unused	95	P1.+12V
32	VCC	64	VCC	96	VCC

NOTE P1 pins 36 and 37, 38 and 39, and 40 and 41 are shorted together.

In the VMEbus Specification, the connectors are labelled differently. The pins in the first row of each connector are labelled A1 through A32, the pins in the second row of each connector are labelled B1 through B32, and the pins in the third row of each connector are labelled C1 through C32.

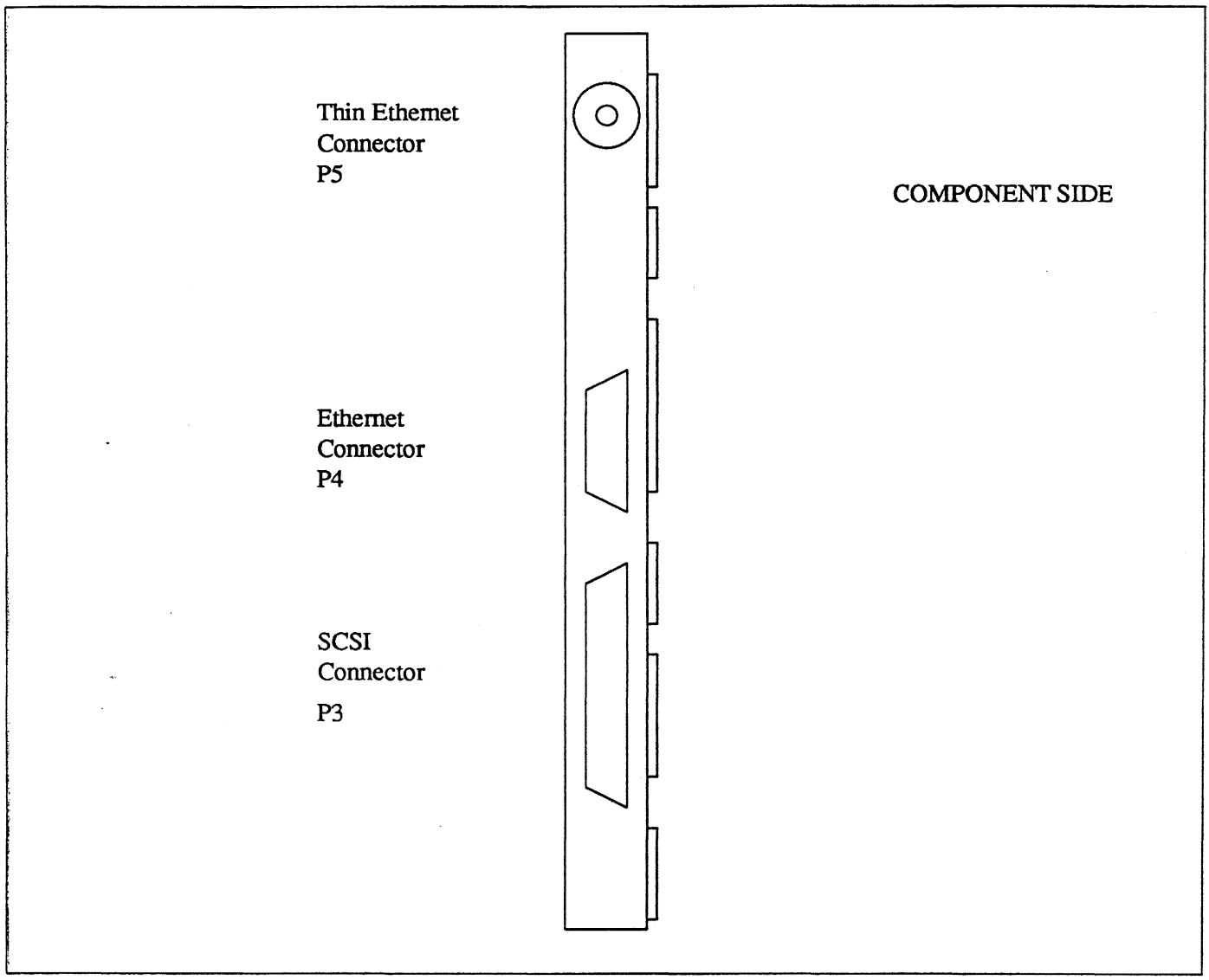
Table A-2 *P2 Connector Pins*

P2A pin	Signal	P2B pin	Signal	P2C pin	Signal
1	Unused	33	VCC	65	Unused
2	Unused	34	GND	66	Unused
3	Unused	35	Unused	67	Unused
4	Unused	36	P1.A24	68	Unused
5	Unused	37	P1.A25	69	Unused
6	Unused	38	P1.A26	70	Unused
7	Unused	39	P1.A27	71	Unused
8	Unused	40	P1.A28	72	Unused
9	Unused	41	P1.A29	73	Unused
10	Unused	42	P1.A30	74	Unused
11	Unused	43	P1.A31	75	Unused
12	Unused	44	GND	76	Unused
13	Unused	45	VCC	77	Unused
14	Unused	46	P1.D16	78	Unused
15	Unused	47	P1.D17	79	Unused
16	Unused	48	P1.D18	80	Unused
17	Unused	49	P1.D19	81	Unused
18	Unused	50	P1.D20	82	Unused
19	Unused	51	P1.D21	83	Unused
20	Unused	52	P1.D22	84	Unused
21	Unused	53	P1.D23	85	Unused
22	Unused	54	GND	86	Unused
23	Unused	55	P1.D24	87	Unused
24	Unused	56	P1.D25	88	Unused
25	Unused	57	P1.D26	89	Unused
26	Unused	58	P1.D27	90	Unused
27	Unused	59	P1.D28	91	Unused
28	Unused	60	P1.D29	92	Unused
29	Unused	61	P1.D30	93	Unused
30	Unused	62	P1.D31	94	Unused
31	Unused	63	GND	95	Unused
32	Unused	64	VCC	96	Unused

A.2. Front Panel Connectors

The front panel connectors include the SCSI connector, the Ethernet connector, and the thin Ethernet connector. Figure A-1 shows the locations of the front edge connectors.

Figure A-1 *Front Panel Connectors*



SCSI Connector

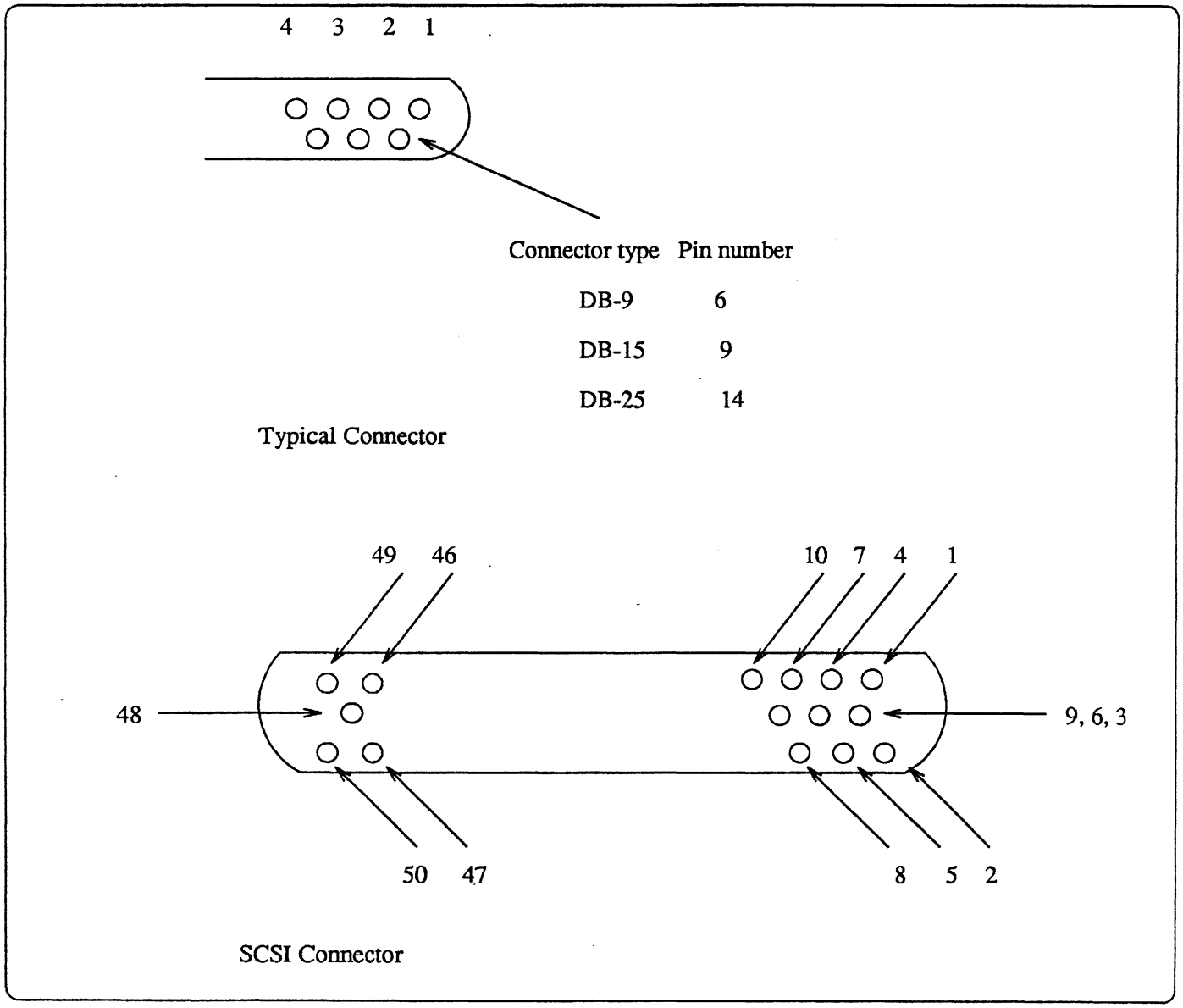
The SCSI connector attaches to P3. It is a 50-pin female D-shell, with the pins assigned as follows:

Table A-3 *SCSI Connector Pins*

Pin	Signal
2	P3.DB[0]*
4	P3.DB[1]*
6	P3.DB[2]*
8	P3.DB[3]*
10	P3.DB[4]*
12	P3.DB[5]*
14	P3.DB[6]*
16	P3.DB[7]*
18	P3.PARITY*
25	OPEN
26	OPEN
32	P3.ATN*
36	P3.BSY*
38	P3.ACK*
40	P3.RST*
42	P3.MSG*
44	P3.SEL*
46	P3.CD*
48	P3.REQ*
50	P3.IO*
All others	Ground

The arrangement of pins on the SCSI connector appear in the following figure:

Figure A-2 *SCSI Connector Pins*



Ethernet Connector

The Ethernet connects to P4, a female DB-15. The pins are assigned as follows:

Table A-4 *Ethernet Connector Pins*

Pin	Signal
1	Open
2	P4.CLSN+
3	P4.TXD+
4	Open
5	P4.RXD+ (fused)
6	Gnd
7	Vcc (jumpered)
8	Open
9	P4.CLSN-
10	P4.TXD-
11	Open
12	P4.RXD-
13	12V (fused)
14	Open
15	Open

Thin Ethernet Connector

The thin ethernet connects to P5. It uses a single female BNC coaxial cable.

B

System Design Considerations

B

System Design Considerations

This appendix lists various considerations that must be taken into account when using the S3SE board. These include power requirements, environmental characteristics, and backplane information.

B.1. System Power Considerations

The following table lists the S3SE power supply requirements:

Table B-1 *Board Power Requirements*

+5V	+12V	-12V
4.0 amp ± 5%	1.0 amp ± 5%	N/A

B.2. Environmental Characteristics

The S3SE board requires the following environmental conditions:

Operating Temperature Range — 10° to 50° C

Storage Temperature Range — -40° to 85° C

Humidity (non-condensing) — 0% to 9%

B.3. P2 Bus Design

The S3SE board is **not** P2 bus compatible; it **must not be used in a slot reserved for P2 bus expansion.**

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