9900 Cache Bus Computer Port Adapter

User's Guide

PB9920-9001-02

SYSTEM INDUSTRIES

1855 Barber Lane
Milpitas, CA 95035, USA

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case, the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Proprietary Statement

LIMITED WARRANTY

Disk Controller. System Industries warrants that its products are free from defects in materials and workmanship and meet System Industries' performance specifications. The warranty period is ninety (90) days from the date of shipment to Buyer. This warranty is limited by the paragraphs below.

Return to Factory. If Buyer discovers a defect in a System Industries product covered by this agreement, Buyer's exclusive remedy is to ship the product back to System Industries' factory where System Industries will, at its option, either repair or replace the product. This remedy applies if System Industries receives the returned product on or before the tenth day after the expiration of the warranty period and Buyer notifies System Industries of the defect before returning the product.

Cost to Buyer of Repairs or Replacement. Buyer must prepay freight charges to System Industries. System Industries will pay return freight to Buyer. There is no other charge for repair or replacement during the warranty period.

Transferrable Disk Drive Warranty. In addition to the foregoing warranty, System Industries also provides to Buyer the transferrable warranty, if any, provided to System Industries by the disk drive manufacturer.

Limitation of Warranty and Liability. The foregoing constitutes System Industries' entire warranty, expressed, implied, and/or statutory (except as to title), and states the full extent of System Industries' liability to Buyer or to any other party for any breach of such warranty and for damages, whether direct, special, incidental, or consequential. OTHER THAN AS EXPRESSLY PROVIDED IN THIS DOCUMENT, NO WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, ARE MADE. NO EMPLOYEE, REPRESENTATIVE, OR AGENT OF SELLER HAS ANY AUTHORITY, EXPRESSED OR IMPLIED, TO ALTER OR TO SUPPLEMENT THE TERMS OF THIS WARRANTY.

REVISION RECORD

REVISION NUMBER	DATE	DESCRIPTION	EO NUMBER
01	4/15/83	Initial Release	1595
02	8/23/84	RP0X	2413

PREFACE

This manual contains sufficient information to enable the end user to install and operate the System Industries 9900 Cache Bus Computer Port Adapter (CPA). It should be read in conjunction with the 9900 Disk Controller User's Guide, PB9900-9001.

The information in this manual is presented in four sections and four appendices.

Section 1	System Overview: Briefly describes the 9900 Disk Storage Subsystem (see the 9900 Disk Controller User's Guide for a detailed description of the 9900 Subsystem).
Section 2	Physical Description: Describes the Cache Bus CPA.
Section 3	Functional Description: Describes the functional operation of the Cache Bus CPA in the 9900 System.
Section 4	Installation: Describes and illustrates the procedures required to install and cable the Cache Bus CPA.
Appendix A	RM0X Registers: Lists and explains all the RM0X registers.
Appendix B	RM0X Register Summary: Summarizes the hardware registers discussed in Appendix A.
Appendix C	RP0X Registers: Lists and explains all the RP0X registers.
Appendix D	RP0X Register Summary: Summarizes the RP0X hardware registers.

Other System Industries publications applicable to the 9900 Cache Bus CPA are as follows:

Publication Number	Title
PB9400-9021	SIDiag User's Guide
PB9400-9015	Overview Software Modifications User's Guide
PB9900-9001	9900 Disk Controller User's Guide
PB9901-9001	Disk Drive User's Guide

TABLE OF CONTENTS

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION 1
SYSTEM OVERVIEW

1.1 System Capability

The System Industries 9900 Series Disk Storage Subsystem interfaces from one to eight Storage Module Drives (SMDs) or SMD interface compatible drives to Digital Equipment Corporation (DEC)™ computers.

With the Cache Bus CPA the 9900 Controller supports the PDP-11/70™ on the internal cache bus.

DEC and PDP are trademarks of Digital Equipment Corporation

SECTION 2
PHYSICAL DESCRIPTION

2.1 9900 Cache CPA Major Components

The 9900 Cache Bus Computer Port Adapter (CPA) consists of four printed circuit boards:

- The UNIBUS control board (9400-61X4) measuring 9×16 inches (22.86 cm x 40.64 cm)
- Address and control board (9400-61X1) measuring 9×16 inches (22.86 cm x 40.64 cm)
- Data board (9400-61X3) measuring 9×6 inches (22.86 cm x 30.68 cm)
- Control buffer board (9400-61X2) measuring 9×12 inches (22.86 cm x 15.24 cm)

These boards occupy a four-slot, RH70 controller dedicated area in the DEC PDP-11/70.

The CPA is connected to the controller by two flat 40-conductor cables.

NOTE

Part numbers for parts in the 9900 model family may vary in the second to the last digit (e.g., cache bus CPA address and control boards may have part numbers 9400-6101 or 9400-6111). If a specific part is required for an application, a specific part number will be given.

SECTION 3
FUNCTIONAL DESCRIPTION

The Cache CPA provides the interface between the controller and the PDP-11/70 on both the internal cache bus for DMA transfers and the UNIBUS for register I/O and interrupt transactions. The CPA consists of the following:

- UNIBUS control board
- Address and control board
- Data board
- Control buffer board

The function of the CPA is to control the transfer of data between the controller and CPU memory.

3.1 UNIBUS Control Board

The UNIBUS control board interfaces between the PDP-11/70 UNIBUS and the controller microprocessor bus by means of a RAM register file and discrete registers that both the CPU and microprocessor can access. The RAM register file contains eight sets of drive registers. There is one set of these registers for each drive. The file also contains additional control registers for I/O and DMA operations.

3.2 Control Registers

These registers contain drive status, command and address parameters, I/O and DMA transfer information, and error messages. Additional logic allows an interrupt to be requested with an interrupt vector address presented to the CPU. Interrupt enable (IE) is bit 6 of RMCS1. It is a control bit that can be set only under program control. It must be set for the CPA to generate an interrupt request to the CPU.

3.3 Address and Control Board

The address and control board interfaces all the memory address and control lines between the cache bus and the UNIBUS control board. Its primary function is to control the buffer of the 32-bit data bus of the cache and the 16-bit data bus of the controller. This board is capable of doing 16-bit data transfers to the cache bus for start and finish addresses if necessary. A 22-bit address is sent from the UNIBUS control board with each data request. The board also sends back to the UNIBUS control board various status and error conditions. Actually there are 21 bits, since bit 0 is unused.

3.4 Data Board

The data board has two 16-bit buffers to interface the 32-bit cache bus and the 16-bit controller bus. When reading from memory, 32 bits of data are read and stored in the two buffers. The contents of the buffers are then sent to the controller. When writing to memory, 16 bits of data are sent from the controller and loaded into the first buffer. The next 16 bits are loaded into the second buffer and a write cycle is then initiated to the cache bus. The necessary actions are performed for 16-bit transfers to the cache bus if the start or finish address of the DMA transfer is an odd address.

3.5 Control Buffer Board

The control buffer board routes control and error signals between the address and control board and the data board. This board obviates wiring changes in the backplane of the PDP-11/70 CPU.

SECTION 4
INSTALLATION

This section contains the information required to install the 9900 Cache Bus CPA in a PDP-11/70 and to cable the CPA to the controller. The section contains the following information:

- Switch and jumper settings
- Physical installation of the CPA
- Cabling information and procedures
- Power requirements
- Power source check
- Power fail circuit

WARNING

Care should be exercised during the installation process to prevent damage to the system or personal injury. It is necessary to power down all or part of the computer system and to disconnect power cords from the AC power source to attach the CPA.

4.1 Visual Inspection

Before attempting to install this device, perform a visual inspection to verify the following:

- All components are undamaged, in place and secure.
- Connector pins are not bent or otherwise damaged.
- Cables are not kinked or cut.

4.2 Switch and Jumper Settings

Two switch settings and three jumper settings must be checked and, if necessary, reset for the CPA to operate correctly with the controller. The following paragraphs describe the switch and jumper settings necessary to configure the CPA.

4.2.1 UNIBUS Address

Set the UNIBUS address switch SW2 located at grid position 3E on the UNIBUS control board (9400-61X4). Refer to Table 4-1 for the switch settings and to Figure 4-1 for location of the switch. The switch settings in Table 4-1 represent the value of the secondary address (776300).

With SW2 set as indicated in Table 4-1, toggling the STD/ALT switch on the UNIBUS control board (located at grid position 5R) to the 'STD' position will select the value of the primary address (776700), and toggling it to the 'ALT' position will select the value of the secondary address (776300).

Nonstandard UNIBUS addresses may be selected by setting the appropriate UNIBUS address switches with the STD/ALT switch set to the 'ALT' position. A switch in the OFF position produces a logical 1 on the corresponding UNIBUS address line.

Table 4-1. UNIBUS Secondary Address (776300) Switch Settings

UNIBUS ADDRESS LINE	SWITCH NUMBER	SWITCH SETTING
5	1	NC
6	2	OFF
7	3	OFF
8	4	ON
9	5	ON
10	6	OFF
11	7	OFF
12	8	OFF

0 = ON
1 = OFF
NC = No connection

NOTE

If the user has selected a UNIBUS address other than the primary or secondary address (i.e., has set switch SW2 differently than indicated in Table 4-1), the 'ALT' mode of the STD/ALT toggle switch must be used. It will select the address set by switch SW2. The 'STD' mode must not be used.

4.2.2 Interrupt Vector

Set the interrupt vector switch SW1 located at grid position 3D on the UNIBUS control board. Refer to Table 4-2 for the switch settings and to Figure 4-1 for the board location of the switch. The switch settings in Table 4-2 represent the value of the secondary interrupt vector (150_8).

With SW1 set as in Table 4-2, toggling the STD/ALT switch (located at grid position 5R) to the 'STD' position will select the primary interrupt vector (254_8), and toggling it to the 'ALT' position will select the secondary interrupt vector (150_8).

Nonstandard interrupt vectors can be selected by setting the appropriate interrupt vector switches with the STD/ALT switch set to the 'ALT' position. A switch in the OFF position produces a logical 1 on the corresponding UNIBUS address line.

Table 4-2. Interrupt Vector Secondary Address (150) Switch Settings

UNIBUS ADDRESS LINE	SWITCH NUMBER	SWITCH SETTING
0	1	NC
1	2	NC
2	3	ON
3	4	OFF
4	5	ON
5	6	OFF
6	7	OFF
7	8	ON

0 = ON
1 = OFF
NC = No Connection

NOTE

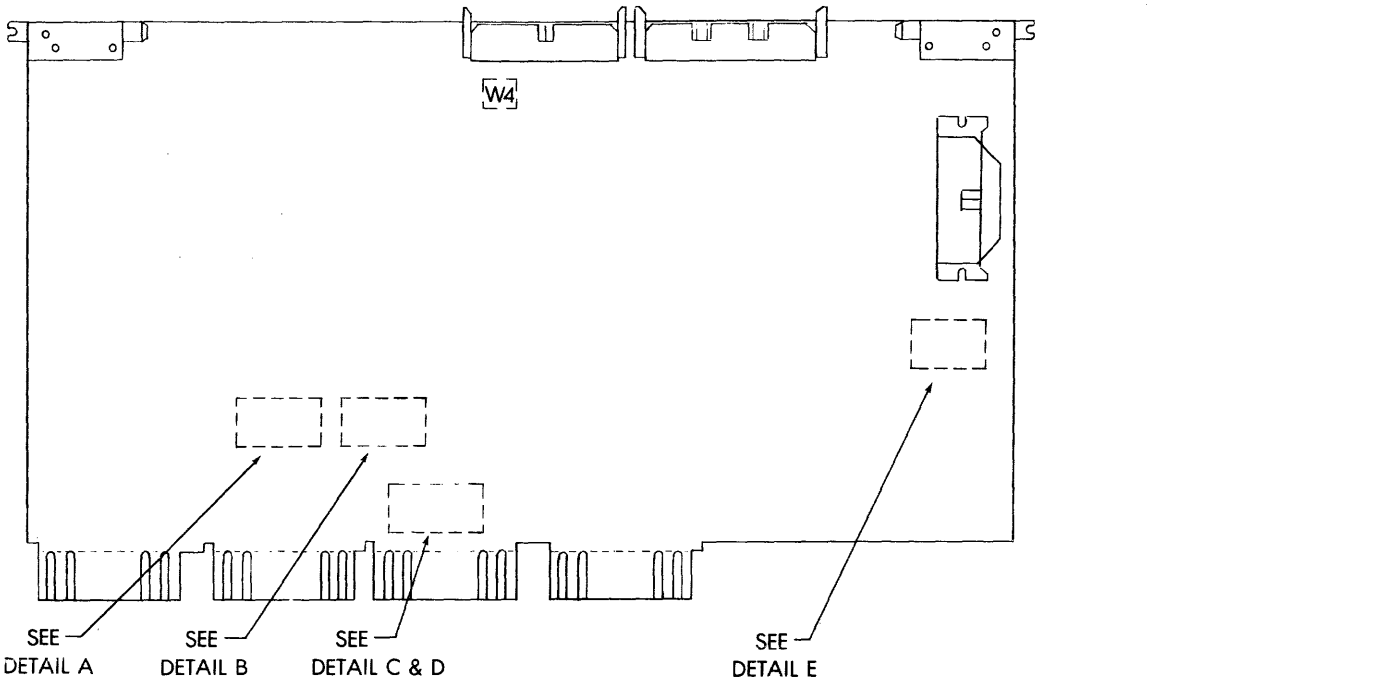
If the user has selected an interrupt vector address other than the primary or secondary address (i.e., has set switch SW1 differently than indicated in Table 4-1), the 'ALT' mode of the STD/ALT toggle switch must be used. It will select the address set by switch SW1. The 'STD' mode must not be used.

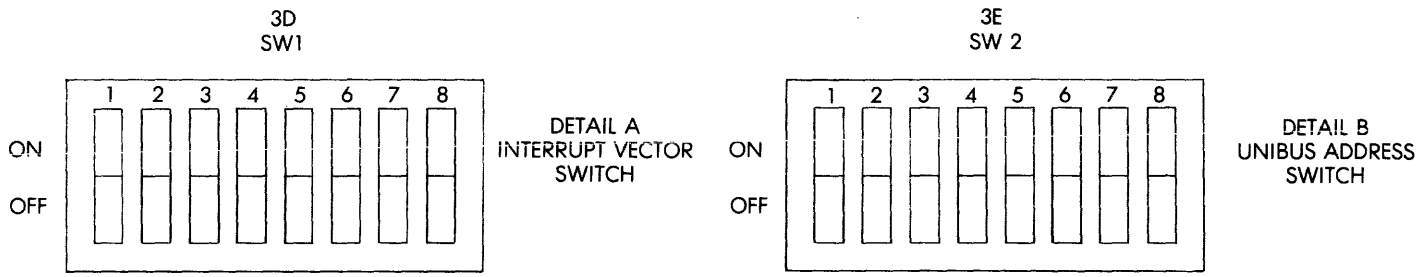
4.2.3 Bus Request Jumper

Verify that the bus request jumper W3 (in etch) located on the UNIBUS control board, is wired as in Figure 4-1. This configuration produces normal BR5 priority. Refer to Table 4-3 for additional bus request settings and to Figure 4-1 for the board location of the jumper.

Table 4-3. Bus Request Jumpers

BUS REQUEST PRIORITY LEVEL	JUMPER CONFIGURATION
BR4	W3 connected to E
BR5	W3 connected to F
BR6	W3 connected to G
BR7	W3 connected to H





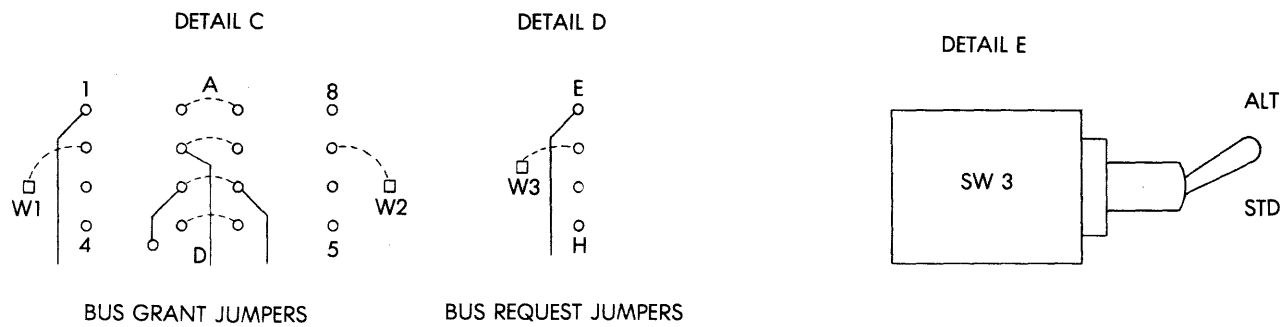


Figure 4-1. UNIBUS Control Board

4.2.4 Bus Grant Jumpers

Verify that the bus grant jumpers W1, W2, A, B, C, and D, (these jumpers are etched) located on the UNIBUS Control board, are wired as in Figure 4-1. This jumper configuration produces normal BG5 priority. Refer to Table 4-4 for additional bus grant settings.

Table 4-4. Bus Grant Jumper Settings

BUS GRANT PRIORITY LEVEL	JUMPER CONFIGURATION
BG4	W1 connected to 1 W2 connected to 8 A - out B,C,D - in
BG5	W1 connected to 2 W2 connected to 7 B - out A,C,D - in
BG6	W1 connected to 3 W2 connected to 6 C - out A,B,D - in
BG7	W1 connected to 4 W2 connected to 5 D - out A,B,C - in

NOTE

The bus grant and bus request jumpers must be set at the same priority level.

4.2.5 UNIBUS Control Board RM/RP Emulation Jumper

Verify that jumper W4, located on the UNIBUS control board, is removed for RM emulation. For RP emulation the jumper should be installed. The jumper location is shown in Figure 4-1.

4.3 Physical Installation

The four boards comprising the CPA are placed in one of the four-slot areas in the PDP-11/70 normally allocated for RH70 controllers (see Figure 4-2). Remove the bus grant continuity card in the UNIBUS control board slot before plugging in the UNIBUS control board. Table 4-5 lists the individual slot locations for the CPA boards in each of the four available areas.

Table 4-5. Slot Locations of the CPA Boards

RH70 DEDICATED AREA	9400-61X4 SLOT LOCATIONS	9400-61X1 SLOT LOCATIONS	9400-61X2 SLOT LOCATIONS	9400-61X3 SLOT LOCATIONS
A	27	26	25	24
B	31	30	29	28
C	35	34	33	32
D	39	38	37	36

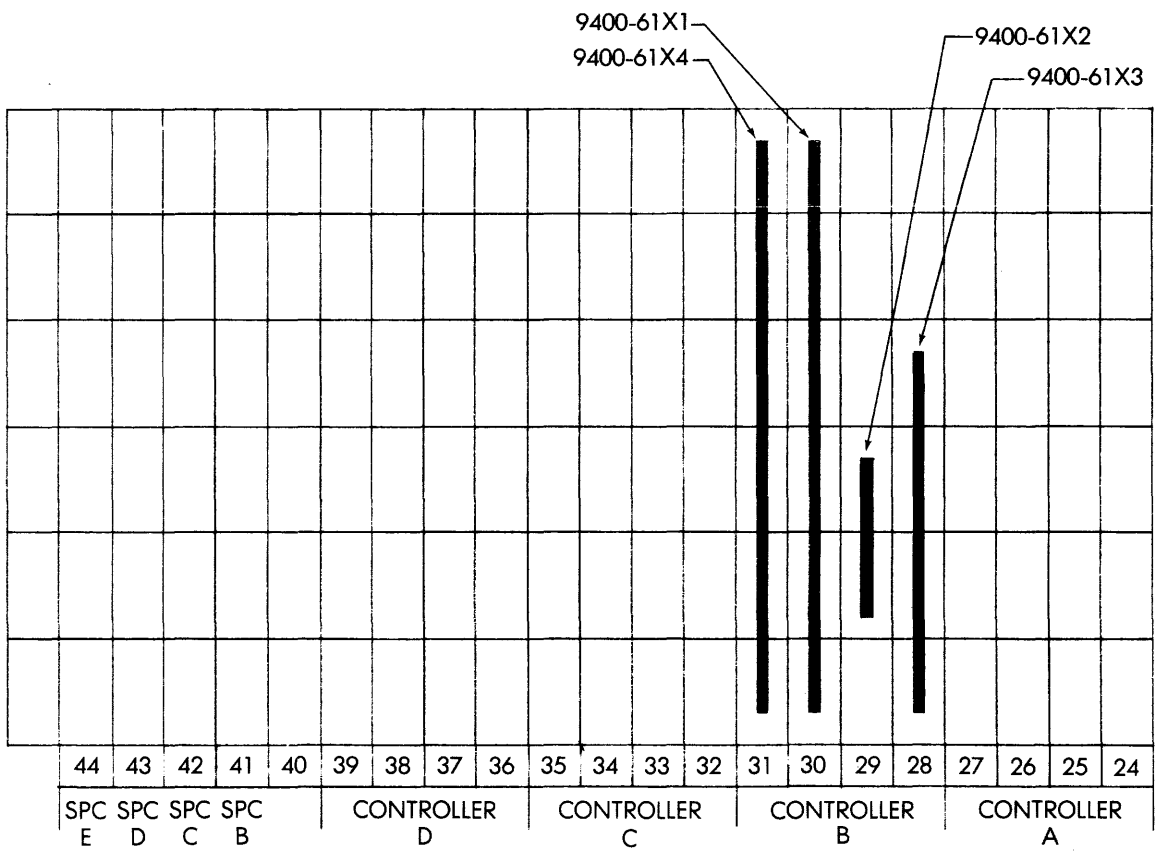


Figure 4-2. Cache Bus CPA Locations in the PDP-11/70

4.4 Cabling

The following paragraphs detail the cabling from CPA to controller and the internal cabling of the CPA.

4.4.1 CPA to Controller Cabling

The controller is connected to the CPA by two cables. Both are 40-conductor ribbon cables originating at the computer interface (CI) board (9400-60X7) located in the controller enclosure (See Figure 4-3).

The first cable (9400-7008 or 9400-7013) extends from connector J1 on the CI board to connector J1 on the UNIBUS control board (9400-61X4).

The second cable (9400-7217 or 9400-7218) provides a three-way interface, extending from connector J2 on the CI board to connector J1 on the data board (9400-61X3) and to connector J2 on the UNIBUS control board (9400-61X4).

4.4.2 Cabling Internal to the CPA

A 40-conductor ribbon cable (9400-7216) extends from connector J3 on the UNIBUS control board (9400-61X4) to connector J1 on the address and control board (9400-61X1). Refer to Figure 4-3.

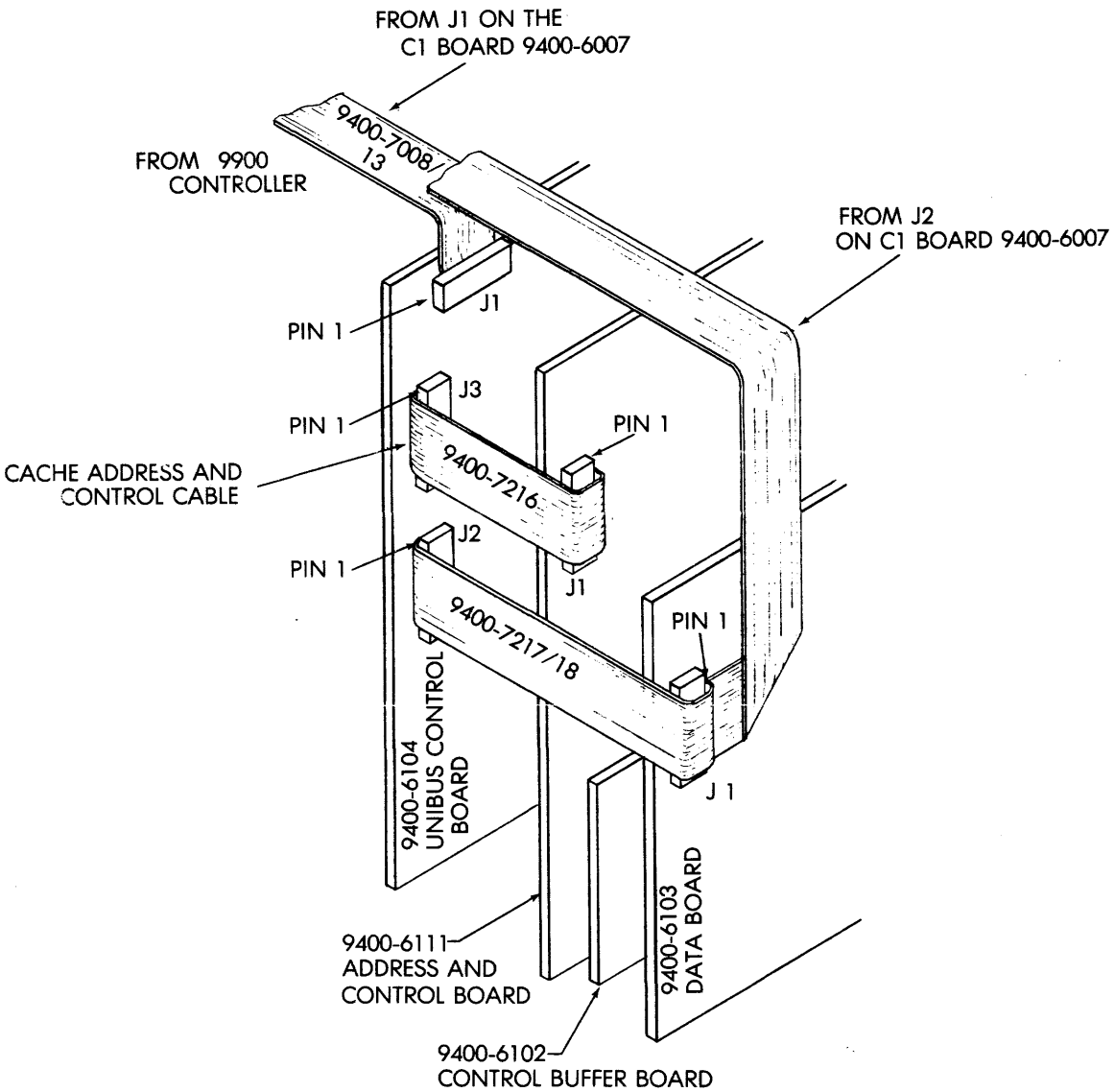


Figure 4-3. Cache Bus CPA Cabling

4.5 Power Requirements

The following voltage is required to operate the Cache Bus CPA:

+5VDC @ 7.5 Amps Maximum

It is obtained from the PDP-11/70 backplane.

4.6 Power Source Check

To ensure reliable operation of the CPA, the PDP-11/70 backplane voltage at each CPA printed circuit board must be checked, and, if necessary, adjusted after the boards have been installed. There are three +5VDC power supply regulators that supply the RH70 slots (see Table 4-6). With the boards in place, the +5VDC on the backplane of each slot, measured at pin FV1, must be within the range 5.00V to 5.10V.

If any of the regulators requires adjustment or replacement, contact the DEC field service representative for assistance.

Table 4-6. +5V Regulator Slots

+5V REGULATOR	RH70 SLOTS SUPPLIED
K	24 25 26 27 28
L	29 30 31 32 33 34 35
D	36 37 38 39

4.7 Power Fail Circuit

Certain CPAs have a CPA power fail circuit which works in conjunction with power-fail circuitry on the 9400-6017 or 9400-6027 computer interface (CI) board to prevent spurious commands from being recognized by the controller when a CPA power failure occurs. This feature was introduced on Cache Bus CPA boards with part number 9400-6104 and a date code of 129 or later. Further revisions of this board, e.g., 9400-6114, also have this circuit.

Boards with part numbers 9400-6104 and a date code earlier than 129 do not have this feature. For these boards it is necessary to disable the CI board power fail circuit by setting a switch. Refer to the 9900 Disk Controller User's Guide, PB9900-9001, for details of this procedure.

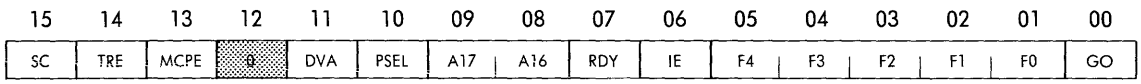
APPENDIX A
RM0X REGISTERS

RM03/05 Registers

Registers are referred to by their name and UNIBUS primary address.

Control and Status #1 Register (RMCS1) (776700)

RMCS1 can be read or written by program control and is used to store the current disk command function code and operational status of the 9900 Disk Controller.



Bit	Name	Function
15	Special Condition (SC)	Set when TRE (bit 14) or any drive's ATA bit (RMAS bits 07-00) is set. Cleared by clearing the TRE or ATA conditions.
14	Transfer Error (TRE)	Set when one or more of RMCS2 bits 15-08 (DLT, WCE, UPE, NED, NEM, PGE, MXF, MPDE) are set, or when a drive error occurs during a data transfer. Cleared by UNIBUS INIT, controller clear, by loading a data transfer command with GO (bit 00) set, or by writing a 1 into this bit causing an error clear.
13*	MASSBUS Control Bus Parity Error (MCPE)	Set to 0 by the controller.
12	Not Used	Set to 0 by the controller.
11*	Drive Available (DVA)	Always read as 1.
10*	Port Select (PSEL)	Used to direct a data transfer to a CI port other than the one corresponding to this CPA. When a data transfer command is initiated with PSEL set to 1, the data transfer will be directed to or from the CI port specified by bits 01-00 of RMOF. Note that the CPU connected to the alternate CPA must have previously loaded its RMBA and RMWC. Cleared by UNIBUS INIT, controller clear or by writing a 0 to this bit.
09-08	UNIBUS Address Extension Bits (A17-A18)	Upper extension bits of the RMBA register. Cleared by UNIBUS INIT, controller clear, or by writing 0's in these bits.
07	Ready (RDY)	Normally RDY = 1. During data transfers, RDY = 0. When a data transfer command code (51_8-73_8) is written into RMCS1, RDY is reset. At the termination of the data transfer, RDY is set.

*A register bit followed by an asterisk(*) indicates a bit whose function differs from DEC definitions.
MASSBUS is a trademark of Digital Equipment Corporation

RMCS1 (Continued)

Bit	Name	Function
06	Interrupt Enable (IE)	IE is a control bit that can be set only under program control. Setting IE enables an interrupt to occur when the following conditions are satisfied: 1. Upon termination of a data transfer if IE is set when RDY becomes asserted. 2. If SC (bit 15), IE, and RDY (bit 07) are all asserted. 3. If the program writes ones into IE and RDY at the same time. When a 0 is written into IE by the program, any pending interrupts are disabled. Cleared by UNIBUS INIT, controller clear or automatically cleared when an interrupt is recognized by the CPU.
05-00	F4-F0 and GO Bit	F4-F0 and the GO bit (00) function (command) code control bits (Table A-1):

Table A-1. Function Code Control Bits

F4	F3	F2	F1	F0	GO	Octal	
0	0	0	0	0	1	01	No operation
0	0	0	1	0	1	05	Seek
0	0	0	1	1	1	07	Recalibrate
0	0	1	0	0	1	11	Drive clear
0	0	1	0	1	1	13	Release
0	0	1	1	0	1	15	Offset
0	0	1	1	1	1	17	Return to centerline
0	1	0	0	0	1	21	Read-in-preset
0	1	0	0	1	1	23	Pack acknowledge
0	1	0	1	0	1	25	System reserve (extended mode only)*
0	1	0	1	1	1	27	System release (extended mode only)*
0	1	1	0	0	1	31	Search*
1	0	1	0	0	1	51	Write check data
1	0	1	0	1	1	53	Write check header and data
1	0	1	1	0	1	55	Call micro (extended mode only)*
1	1	0	0	0	1	61	Write data
1	1	0	0	1	1	63	Write header and data
1	1	0	1	0	1	65	Write micro (extended mode only)*
1	1	0	1	1	1	67	Autoformat (extended mode only)*
1	1	1	0	0	1	71	Read data
1	1	1	0	1	1	73	Read header and data
1	1	1	1	0	1	75	Read micro (extended mode only)*

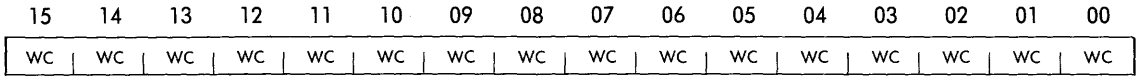
*SI Function

GO (bit 00) must be set to cause the controller to respond to a command. GO is reset by the controller after command execution.

Cleared by UNIBUS INIT or controller clear.

Word Count Register (RMWC) (776702)

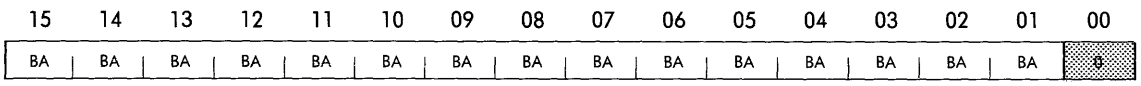
RMWC is loaded by the program with the two's complement of the number of words to be transferred. A maximum of 65,536 words can be transferred at one time.



Bit	Name	Function
15-00	Word Count (WC)	Set by the program to specify the number of words to be transferred (two's complement form). RMWC is updated by the controller at the completion of the DMA transfer. Cleared by writing zeros into these bits.

UNIBUS Address Register (RMBA) (776704)

RMBA is used to address the memory location in which a transfer is to take place. The RMBA forms the lower 16 bits of the address that combine with bits 05-00 of the Bus Address Extension Register (RMBAE) to create the 21-bit memory address (A17 and A16, RMCS1 bit 09 and 08, are also UNIBUS address extension bits and provide another means of reading or writing bits 17 and 16 of the extended UNIBUS address). The register is loaded with the starting memory address by the program. Each time a DMA transfer is made, the register is incremented by 2. If BAI (bus address increment inhibit, RMCS2 bit 03) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address.

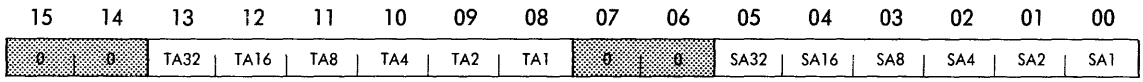


Bit	Name	Function
15-01	UNIBUS Address (BA)	Loaded by the program to specify the memory address of a transfer. RMBA is incremented by 2 after each transfer of a word to or from memory. Cleared by UNIBUS INIT, or by controller clear.
00	Not Used	Always read as 0.

Desired Sector/Track Address Register (RMDA) (776706)

RMDA register is used to address the sector and track on the disk to or from which a transfer is desired. RMDA is associated with the drive whose unit number appears in bits 02-00 of the Control and Status 2 register (RMCS2). Before a transfer, RMDA is loaded by the program with the address of the first block to be transferred. At the end of a transfer, RMDA contains the address of the block following the last block of the transfer.

The RMDA contains a 6-bit sector address field providing for 48 sectors per track (SI 9751 only). The register also contains a 6-bit track address field providing for up to 64 data tracks per cylinder.

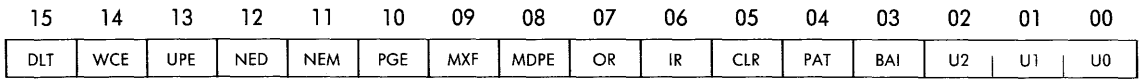


Bit	Name	Function
15-14*	Not Used	Set to 0 by the controller.
13-08*	Track Address (TA32-TA1)	Set by the program to specify the track on which a transfer is to start. Updated by the controller at the end of the transfer. Cleared by UNIBUS INIT.
07-05	Not Used	Set to 0 by the controller.
05-00*	Sector Address (SA32-SA1)	Set by the program to specify the sector on which a transfer is to start. Bit 5 is used if there is an SI 9751 in the system. Updated by the controller at the end of the transfer. Cleared by UNIBUS INIT.

*Function differs from DEC definition.

Control and Status #2 Register (RMCS2) (776710)

RMCS2 indicates the status of the controller and contains the drive unit number. The unit number specified in bits 02-00 of this register indicates which of the possible 8 logical drives is selected.



Bit	Name	Function
15*	Data Late (DLT)	Set to 0 by the controller.
14	Write Check Error (WCE)	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. WCE causes TRE (RMCS1 bit 14) to be set. If a mismatch is detected during a write-check command execution, the transfer terminates and WCE is set. The memory address displayed in RMBA (and RMBAE bits 05-00) is the address of the word following the one that did not match (if BAI, bit 03, is not set). The mismatched data word from the disk is displayed in RMDB. Cleared by UNIBUS INIT, controller clear, error clear, or loading a data transfer command with GO (RMCS1 bit 00) set.
13	UNIBUS Parity Error (UPE)	Set if any of RMCS3 bits 13, 14, or 15 (DPEE, DPE0, or APE) are set while the controller is performing a data transfer command. UPE sets TRE (RMCS1 bit 14). RMBA contains the address +2 of the memory location with the parity error. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RMCS1 bit 00) set.
12	Nonexistent Drive (NED)	Set when the program attempts a command on a drive that does not exist or is powered down. NED sets TRE (RMCS1 bit 14). Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RMCS1 bit 00) set.
11	Nonexistent Memory (NEM)	Set when the controller is performing a DMA transfer and the memory address specified in RMBA is nonexistent (does not respond to MSYN within 10 microseconds). NEM sets TRE (RMCS1 bit 14). RMBA contains the address +2 of the memory location causing the error. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RMCS1 bit 00) set.

*Function differs from DEC definition.

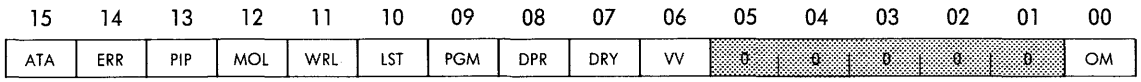
RMCS2 (Continued)

Bit	Name	Function
10	Program Error (PGE)	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. PGE sets TRE (RMCS1 bit 14). Cleared by UNIBUS INIT, controller clear, or error clear.
09*	Missed Transfer (MXF)	Set if the controller fails to detect an end of header or end of sector, or the data buffer fails to empty during a data transfer. MFX sets TRE (RMCS1 bit 14). Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RMCS1 bit 00) set.
08*	MASSBUS Data Bus Parity Error (MDPE)	Set to 0 by the controller.
07	Output Ready (OR)	Set by the controller to indicate a word is in RMDB.
06*	Input Ready (IR)	Set to 1 by the controller.
05	Controller Clear (CLR)	When a 1 is written into this bit, the controller and all drives are initialized. Always read as 0.
04*	Parity Test (PAT)	PAT has no effect on controller operation. Cleared by UNIBUS INIT or controller clear.
03	UNIBUS Address Increment inhibit (BAI)	When BAI is set, the controller will not increment the RMBA register during a data transfer. BAI bit cannot be modified while the controller is doing a data transfer (RDY, RMCS1 bit 07, negated). When set during a data transfer, all data words are read from or written into the same memory location. Cleared by UNIBUS INIT or controller clear.
02-00	Unit Select (U2-U0)	U2-U0 bits are written by the program to select a drive. The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. Cleared by UNIBUS INIT or controller clear.

*Function differs from DEC definition.

Drive Status Register (RMDS) (776712)

RMDS contains status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bits (02-00) of the RMCS2.



Bit	Name	Function
15	Attention Active (ATA)	An attention condition from a drive will set the ATA bit and the corresponding summary bit in RMAS. ATA is cleared by UNIBUS INIT, controller clear, drive clear, loading a command with GO bit (RMCS1 bit 00)set or, if no error conditions exist, by writing a 1 into the RMAS register bit corresponding to the drive's unit number. An attention condition is caused by: 1. Completion of seek, search, recalibrate, offset, or return to centerline. 2. MOL (bit 12) changing state.
14	Error (ERR)	Set when one or more error bits in the error registers (RMER1 or RMER2) for a selected drive is set, indicating a drive error has occurred. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing zeros into the set error bit(s) in the error registers.
13*	Positioning In Progress (PIP)	Always read as 0.
12	Medium On-line (MOL)	Set for the drive upon the successful completion of the start-up cycle. This bit is set when the unit ready line from the drive is asserted (indicating that the drive is up to speed, the heads are positioned over the recording tracks, and no fault condition exists within the drive), and is reset when the unit ready line is deasserted. Cleared when the drive is spun down or switched off.
11	Write Lock (WRL)	Set when the write protected line from the drive is asserted (as enabled by a switch located on the drive), indicating that the drive will not accept write commands. A write command issued on a write-locked drive will cause WLE (RMER1 bit 11) to be set.

*Function differs from DEC definition.

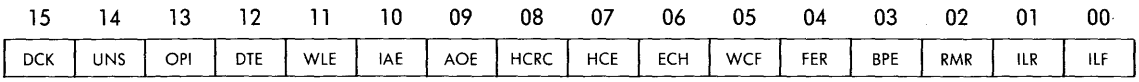
RMDS (Continued)

Bit	Name	Function
10	Last Sector Transferred (LST)	Set when last addressable sector on the disk pack has been read or written.
09*	Programmable (PGM)	Always read as 0.
08*	Drive Present (DPR)	Set if the drive is powered up.
07	Drive Ready (DRY)	Set at the completion of every command, data handling or mechanical motion. If this bit is reset, the program must not issue another command to this drive. When set, this bit indicates the readiness of the drive to accept a new command. DRY is the complement of GO (RMCS1 bit 00) except when the drive is nonexistent; then DRY is reset. Cleared at the initiation of a command.
06	Volume Valid (VV)	Set by the pack acknowledge or read-in preset command. When reset, VV bit indicates that the drive has been spun down and then up, and that a disk pack may have been changed. Cleared whenever drive spins up (i.e., when MOL, bit 12, becomes asserted) or when the CPU powers up.
05-01	Not Used	Always read as 0.
00	Offset Mode (OM)	Set when offset command is issued to a drive. When set, and a read command is received, the offset is performed prior to the execution of the read. Reset by any of the following actions: 1. Power-up 2. Mid-transfer seek 3. Write data or write header and data 4. Return to centerline 5. Recalibrate

*Function differs from DEC definition.

Error Register #1 (RMER1) (776714)

RMER1 contains the error status indicators for the drive whose unit number appears in bits 02-00 of RMCS2. The logical OR of all the error bits in the RMER1 and RMER2 registers is written into bit 14 of RMDS.



Bit	Name	Function
15	Data Check (DCK)	If ECI (RMOF bit 11) is 0, this bit will be set if an uncorrectable ECC error is detected (ECH, bit 06 is also set). If ECI is 1 and an ECC error is detected, no correction will be attempted and this bit will be set (the ECH bit will not be set). Cleared by UNIBUS INIT, controller clear, drive clear or by writing a 0 into the bit.
14	Unsafe (UNS)	Indicates a drive fault has been detected. Set when DVC (RMER2 bit 07) is set. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
13*	Operation Incomplete (OPI)	Set to 0 by the controller.
12	Drive Timing Error (DTE)	Set when more than one sector pulse occurs within a sector. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
11	Write Lock Error (WLE)	Set when the operating system attempts to issue a write command to a drive which has its write-protect switch on (WRL, RMDS bit 11, set). Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
10	Invalid Address Error (IAE)	Set when the address in RMDC or RMDA is invalid and a seek, search, or data transfer operation is initiated. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
09	Address Overflow Error (AOE)	Set when RMDC overflows during a read or write. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.

*Function differs from DEC definition.

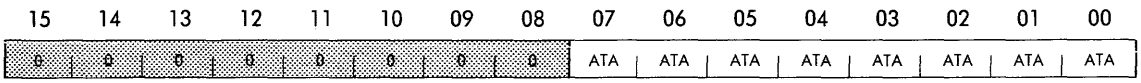
RMER1 (Continued)

Bit	Name	Function
08	Header CRC Error (HCRC)	Set by a CRC error in the header if HCI (RMOF bit 10) is reset. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
07	Header Compare Error (HCE)	If the sector counter is equal to the desired sector field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder and desired sector/track address, the header field is the required one. If HCI (RMOF bit 10) is reset and the header does not match the desired cylinder and sector/track address, HCE is set. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
06	ECC Hard Error (ECH)	Set by an uncorrectable ECC error. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
05*	Write Clock Fail (WCF)	Set to 0 by controller.
04*	Format Error (FER)	Set when the controller format switch is OFF and a write header and data command is attempted. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
03*	Buffer Parity Error (BPE)	Set when a controller buffer parity error is detected. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
02*	Register Modification Refused (RMR)	Set to 0 by the controller.
01*	Illegal Register (ILR)	Set to 0 by the controller.
00	Illegal Function (ILF)	Set when GO (RMCS1 bit 00) is set and the function code in the control register does not correspond to a valid command. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.

*Function differs from DEC definition.

Attention Summary Register (RMAS) (776716)

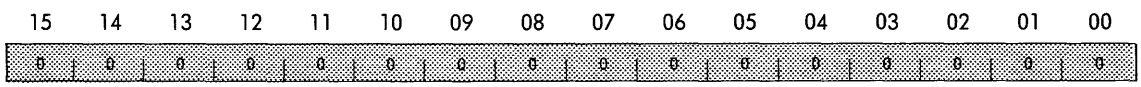
RMAS allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in the RMDS for the corresponding drive. When fewer than eight drives are attached to the controller, the bits corresponding to the missing drives are always 0.



Bit	Name	Function
15-08	Not Used	Always read as 0.
07-00	Attention Active (ATA)	Each ATA bit is set when the corresponding drive asserts its ATA bit. If any drive's ATA bit is set, bit 15 of RMDS will be set. Each drive also responds in the bit position of RMAS that corresponds to its unit number; e.g., drive 02 responds in bit position 02 of RMAS. All bits are cleared by UNIBUS INIT or controller clear. Individual bits are cleared by loading a function code with GO (RMCS1 bit 00) set in the corresponding drive or by writing a 1 into the ATA bit positions of this register. Writing a 0 has no effect.

Look-ahead Register (RMLA) (776720)

RMLA is not emulated.

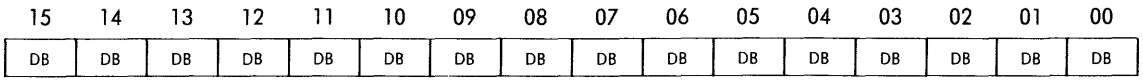


Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

*Function differs from DEC definition.

Data Buffer Register (RMDB) (776722)

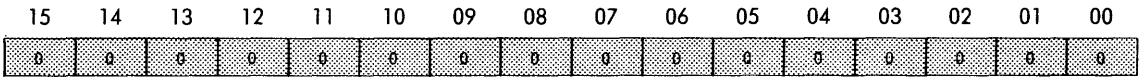
RMDB provides the bad data word resulting from a bad data compare operation.



Bit	Name	Function
15-00	Data Buffer (DB)	Contains the bad data word from a data compare operation.

Maintenance Register #1 (RMMR1) (776724)

RMMR1 is not emulated.

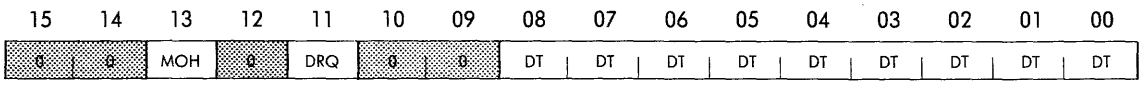


Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

*Function differs from DEC definiton.

Drive Type Register (RMDT) (776726)

RMDT register allows the program to distinguish between different types of drives.



Bit	Name	Function
15-14	Not Used	Set to 0 by the controller.
13	Moving Head (MOH)	Set to 1 by the controller since drives are moving head devices.
12	Not Used	Set to 0 by the controller.
11*	Drive Request Required (DRQ)	Set to 0 by the controller.
10-09	Not Used	Set to 0 by the controller.
08-00	Drive Type (DT)	These bits contain a code indicating the drive type being emulated. This is determined by the controller firmware (RM0X) reading switch 8 of the model byte switch bank on the DI board in the controller.

Table A-2. Drive Type Switch Settings.

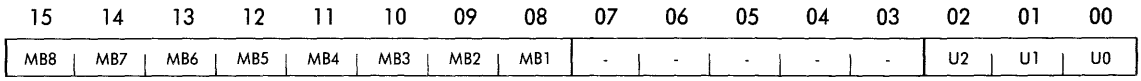
SWITCH NUMBER	DRIVE TYPE RM03	DRIVE TYPE RM05
8	1 24_8	0 27_8

1 = closed = ON.
0 = open = OFF.

*Function differs from DEC definition.

Serial Number Register (RMSN) (776730)

RMSN register is used to distinguish a drive from similar drives attached to the same controller. The serial number provides a means of distinguishing between different capacity drives with the same drive type code.

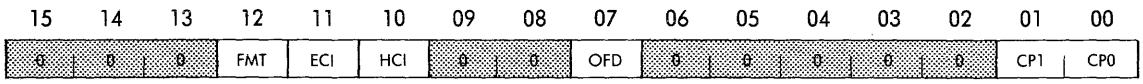


Bit	Name	Function
15-08*	Model Byte (MB8-MB1)	These bits contain a copy of the model byte switch setting on the radial drive interface board associated with the drive. See the 9900 Controller User's Guide for details of model byte switch settings for different drives and emulations.
07-03*	Undefined	Reserved to System Industries.
02-00*	Unit (U2-U0)	Contains a copy of the logical unit number of the drive.

*Function differs from DEC definition.

Offset Register (RMOF) (776732)

RMOF contains the positioner offset information supplied to the drive directly by the operating system prior to issuance of the offset command. The drive has the ability to offset the positioner approximately 200 micro-inches from the track centerline in either direction.

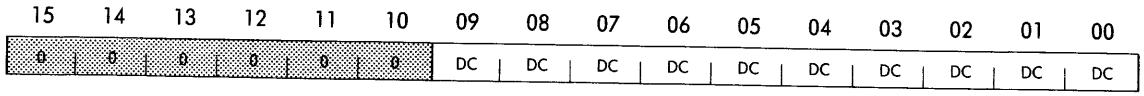


Bit	Name	Function
15-13	Not Used	Set to 0 by the controller.
12*	Format 16 (FMT)	The controller sets this bit to 1 and ignores any change in the setting.
11	Error Correction Inhibit (ECI)	Set when the software inhibits error correction. If an ECC error is detected and this bit is reset, the controller performs the ECC correction process at the end of the sector, provided the W7 jumper on the controller is set for internal ECC correction. If the error is correctable it will be corrected in the controller's buffer and the transfer will proceed (software transparent - no error indication). If the error is uncorrectable, the controller will set ECH and DCK (RMER1 bits 06 and 15). If ECI is already set, however, the error correction process will be inhibited, and DCK will be set (ECH bit will not be set). ECI is cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
10	Header Compare Inhibit (HCI)	Set when the software inhibits the reporting of header compare errors HCE and HCRC (RMER1 bits 07 and 08). When the controller detects this bit asserted, it will ignore the header compare logic and CRC check. With HCI set, the controller depends only on the hardware sector counter comparison for sector identification. If the sector counter is out of sequence, the wrong sector may be affected by the data transfer. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
09-08	Not Used	Set to 0 by the controller.
07	Offset Direction (OFD)	Set when the offset direction is toward the spindle. Reset when the offset direction is away from the spindle. The offset direction bit is valid if the following three conditions are met: 1. Read command is loaded into bits 05-00 of RMCS1. 2. GO (RMCS1 bit 00) is set. 3. OM (RMDS bit 00) is set.
06-02	Not Used	Set to 0 by the controller.
01-00	CI Port (CP1-CP0)	Used to specify the target CI port when PSEL (RMCS1 bit 10) is set.

*Function differs from DEC definition.

Desired Cylinder Register (RMDC) (776734)

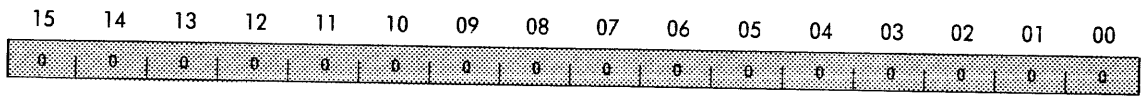
RMDC contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data handling command.



Bit	Name	Function
15-10	Not Used	Set to 0 by the controller.
09-00	Desired Cylinder (DC)	Set by the program to specify the required cylinder address. IAE (RMER1 bit 10) will be set if, when asserting GO for a data transfer, seek or search command, this register contains an address larger than the maximum cylinder address on the drive.

Holding Register (RMHR) (776736)

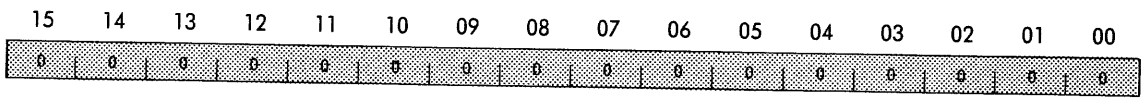
RMHR register is not emulated and is set to 0 by the controller.



Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

Maintenance Register #2 (RMMR2) (776740)

RMMR2 register is not emulated and is set to 0 by the controller.

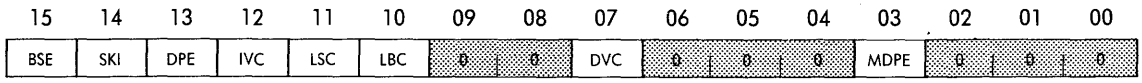


Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

*Function differs from DEC definition.

Error Register #2 (RMER2) (776742)

RMER2 contains detailed error status information and is primarily used for monitoring the electromechanical performance of the drive rather than the interface.

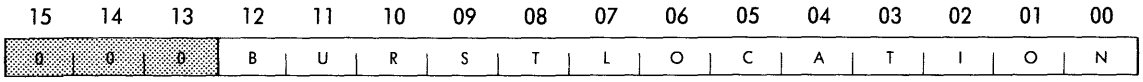


Bit	Name	Function
15	Bad Sector Error (BSE)	Set when the controller detects a 0 in bit 14 or 15 of the first header word and HCI (RMOF bit 10) is 0. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
14	Seek Incomplete (SKI)	Set when a seek operation fails to complete within 500 ms from a seek initiation. Cleared by UNIBUS INIT, controller clear, or by writing a 0 into this bit.
13*	Drive Plug Error (DPE)	Set to 0 by the controller.
12	Invalid Command (IVC)	Set when either VV or MOL (RMDS bits 6 and 12) are reset and any command other than read-in preset, pack acknowledge, drive clear or NO-OP is received. Cleared by UNIBUS INIT, drive clear, controller clear, or by writing a 0 into this bit.
11*	Loss of System Clock (LSC)	Set to 0 by the controller.
10*	Loss of Bit Clock (LBC)	Set to 0 by the controller.
09-08	Not Used	Set to 0 by the controller.
07	Device Check (DVC)	Set when drive fault line is asserted. Also sets UNS (RMER1 bit 14). Cleared by UNIBUS INIT, drive clear, controller clear, or by writing a 0 into this bit.
06-04	Not Used	Set to 0 by the controller.
03*	MASSBUS Data Parity Error (MDPE)	Set to 0 by the controller.
02-00	Not Used	Set to 0 by the controller.

*Function differs from DEC definition.

ECC Position Register #1 (RMEC1) (776744)

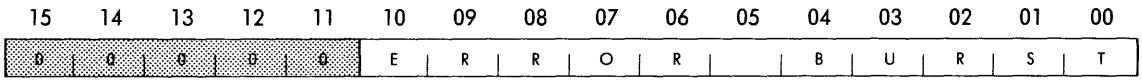
RMEC1 (Read Only)



Bit	Name	Function
15-13	Not Used	Set to 0 by controller.
12-00	Burst Location	These bits specify the location in the record of the first bit of the error burst in the error pattern register.

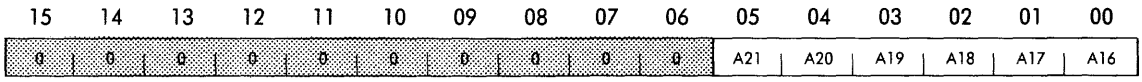
ECC Pattern Register #2 (RMEC2) (776746)

RMEC2 (Read Only)



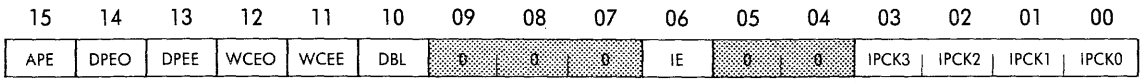
Bit	Name	Function
15-11	Not Used	Set to 0 by the controller.
10-00	Error Burst	These bits are the 11-bit error correction burst that the software uses to correct bad data in the record. The ECC position register specifies the starting bit position.

Bus Address Extension Register (RMBAE) (776750)



Bit	Name	Function
15-06	Not used	Always read as 0.
05-00	Bus Address Extension (A21-A16)	Loaded by the program to specify the starting memory address of a transfer. Cleared by UNIBUS INIT or controller clear.

Control and Status Register #3 (RMCS3) (776752)



Bit	Name	Function
15	Address Parity Error (APE)	Set if the address parity line indicates that the memory detected a parity error on address and control information during a memory transfer. When this bit becomes set, UPE (RMCS2 bit 13) is also set. Cleared by UNIBUS INIT, controller clear or by loading a data transfer command with GO set.
14	Data Parity Error Odd Word (DPEO)	Set if a parity error is detected on odd-word data read from memory during a write or write-check command. When this bit becomes set, UPE (RMCS2 bit 13) is also set. Cleared by UNIBUS INIT, controller clear or loading a data transfer command with GO (RMSC1 bit 00) set.
13	Data Parity Error Even Word (DPEE)	Set if a parity error is detected on even-word data read from memory during a write or write-check command. When this bit becomes set, UPE (RMCS2 bit 13) is also set. Cleared by UNIBUS INIT, controller clear or loading a data transfer command with GO (RMCS1 bit 00) set.
12*	Write Check Error Odd Word (WCEO)	Set to 0 by the controller.
11*	Write Check Error Even Word (WCEE)	Set to 0 by the controller.
10	Double Word (DBL)	Set if the last memory transfer was a double-word operation. Cleared by UNIBUS INIT, controller clear, or by loading a data transfer command with GO set.
09-07	Not Used	Set to 0 by the controller.

*Function differs from DEC definition.

RMCS3 (Continued)

Bit	Name	Function
06	Interrupt Enable (IE)	IE is a control bit that can be set only under program control and which enables an interrupt to occur when any one of the following conditions are satisfied: 1. Upon termination of a data transfer if IE is set when RDY becomes asserted. 2. If SC (RMCS1 bit 15), IE, and RDY (RMCS1 bit 07) are all asserted. 3. If the program writes ones into IE and RDY at the same time. When a 0 is written into IE by the program, any pending interrupts are cancelled. Cleared by UNIBUS INIT, controller clear or automatically cleared when an interrupt is recognized by the CPU.
05-04	Not Used	Set to 0 by the controller.
03-00*	Inverted Parity Check (IPCK3-0)	Set to 0 by the controller.

*Function differs from DEC definition.

APPENDIX B
RM0X REGISTER SUMMARY

Control and Status #1 Register (RMCS1) (776700)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

Word Count Register (RMWC)(776702)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

UNIBUS Address Register (RMBA)(776704)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	0

Desired Sector/Track Address Register (RMDA)(776706)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	TA32	TA16	TA8	TA4	TA2	TA1	0	0	SA32	SA16	SA8	SA4	SA2	SA1

Control and Status #2 Register (RMCS2)(776710)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

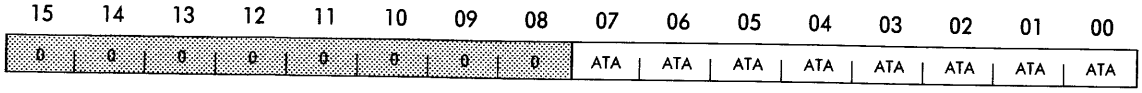
Drive Status Register (RMDS)(776712)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRU	VV	0	0	0	0	0	OM

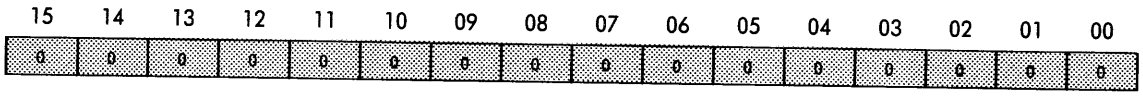
Error Register #1 (RMER1)(776714)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	BPE	RMR	ILR	ILF

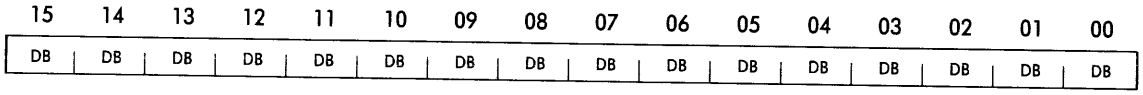
Attention Summary Register (RMAS)(776716)



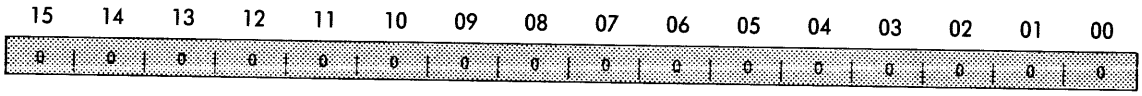
Look-ahead Register (RMLA)(776720)



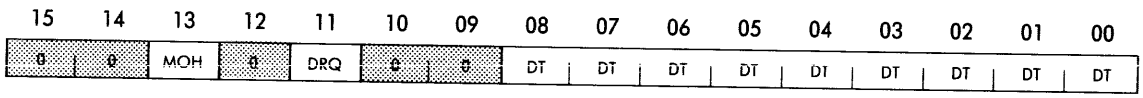
Data Buffer Register (RMDB)(776722)



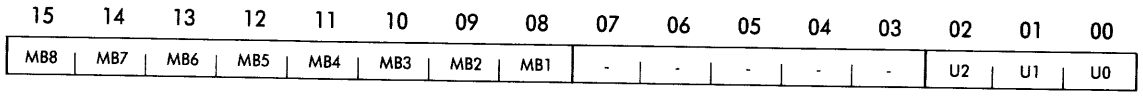
Maintenance Register #1 (RMMR1)(776724)



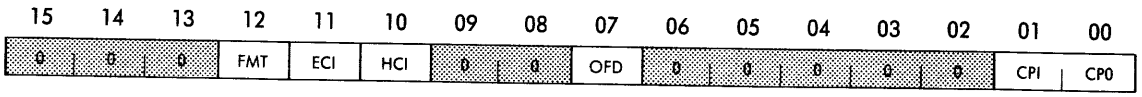
Drive Type Register (RMDT)(776726)



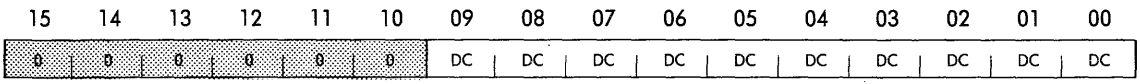
Serial Number Register (RMSN)(776730)



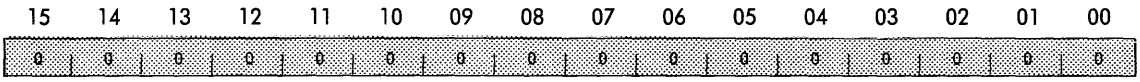
Offset Register (RMOF)(776732)



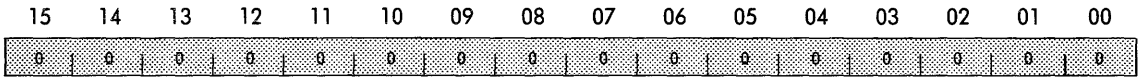
Desired Cylinder Register (RMDC)(776734)



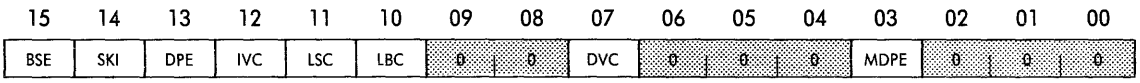
Holding Register (RMHR)(776736)



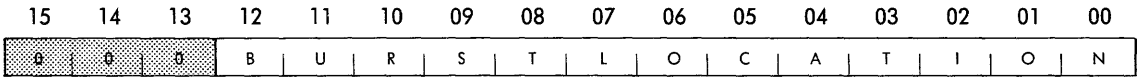
Maintenance Register #2 (RMMR2)(776740)



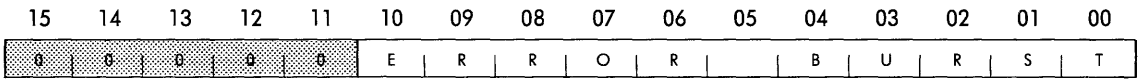
Error Register #2 (RMER2)(776742)



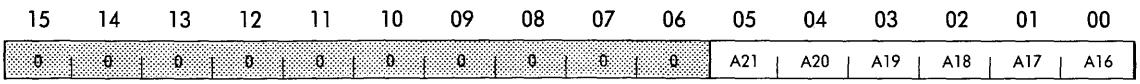
ECC Position #1 Register (RMCS1)(776744)



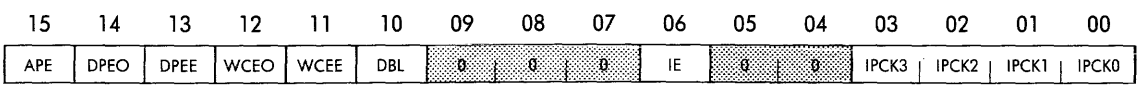
ECC Pattern Register #2 (RMEC2)(776746)



Bus Address Extension Register (RMBAE)(776750)



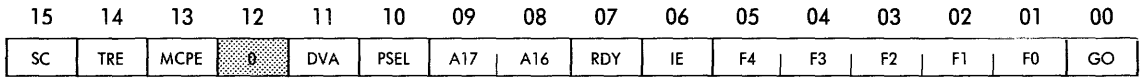
Control and Status Register #3 (RMCS3)(776752)



APPENDIX C
RP0X REGISTERS

Control and Status #1 Register (RPCS1) (776700)

RPCS1 register stores and current disk command function code and operational status of the 9900 Disk Controller.



Bit	Name	Function
15	Special Condition (SC)	Set when TRE or any drive's ATA bit is set. Cleared by clearing the TRE or ATA conditions.
14	Transfer Error (TRE)	Set when one or more of RPCS2 bits 15-08 (DLT, WLE, UPE, NED, NEM, PGE, MXF, MPDE) are set, or when a drive error occurs during a data transfer. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO set.
13*	MASSBUS Control Bus Parity Error (MCPE)	Set to 0 by the controller.
12	Not Used	
11*	Drive Available (DVA)	Always read as 1.
10*	Port Select (PSEL)	Set to 0 by the controller.
09-08	A17-A16 UNIBUS Address Extension Bits	Upper extension bits of the address of the RPBA register.
07	Ready (RDY)	Normally RDY = 1. During data transfers, RDY = 0. When a data transfer command code ($51\text{-}73_8$) is written into RPCS1, RDY is reset. At the termination of a data transfer, RDY is set.

RPCS1 (Continued)

Bit	Name	Function
06	Interrupt Enable (IE)	IE is a control bit that can be set only under program control and enables an interrupt to occur when the following conditions are satisfied: 1. Upon termination of a data transfer, if IE is set when RDY becomes asserted. 2. If SC (bit 14), IE, and RDY (bit 07) are all asserted. 3. If the program writes ones into IE and RDY at the same time. When a 0 is written into IE by the program, any pending interrupts are disabled. Cleared by UNIBUS INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU.
05-00	F4-F0 and GO Bit	F4-F0 and GO are function (command) code control bits (Table C-1):

Table C-1. Function Code Control Bits

F4	F3	F2	F1	F0	GO	Octal	
0	0	0	0	0	1	01	No operation
0	0	0	1	0	1	05	Seek
0	0	0	1	1	1	07	Recalibrate
0	0	1	0	0	1	11	Drive clear
0	0	1	0	1	1	13	Release
0	0	1	1	0	1	15	Offset
0	0	1	1	1	1	17	Return to centerline
0	1	0	0	0	1	21	Read-in-preset
0	1	0	0	1	1	23	Pack acknowledge
0	1	0	1	0	1	23	System reserve (extended mode only)*
0	1	0	1	1	1	27	System release (extended mode only)*
0	1	1	0	0	1	31	Search*
1	0	1	0	0	1	51	Write check data
1	0	1	0	1	1	53	Write check header and data
1	0	1	1	0	1	55	Call micro (extended mode only)*
1	1	0	0	0	1	61	Write data
1	1	0	0	1	1	63	Write header and data
1	1	0	1	0	1	65	Write micro (extended mode only)*
1	1	0	1	1	1	67	Auto format (extended mode only)*
1	1	1	0	0	1	71	Read data
1	1	1	0	1	1	73	Read header and data*
1	1	1	1	0	1	75	Read micro (extended mode only)*

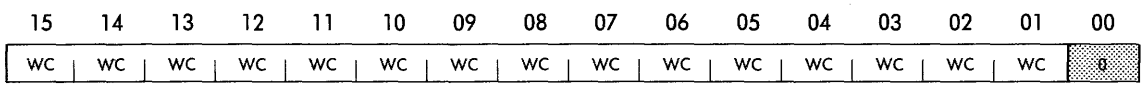
*SI function.

GO (bit 00) must be set to cause the controller to respond to a command. GO is reset by the controller after command execution.

Cleared by UNIBUS INIT or controller clear.

Word Count Register (RPWC) (776702)

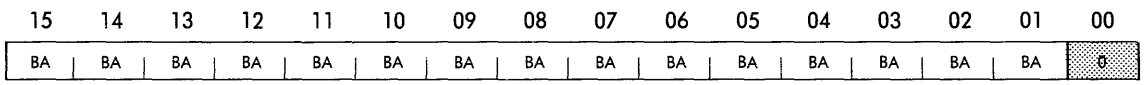
RPWC is loaded by the program with the two's complement of the number of words to be transferred. A maximum of 65,536 words can be transferred at one time.



Bit	Name	Function
15-01	Word Count (WC)	Set by the program to specify the number of words to be transferred (two's complement form). RPWC is updated by the controller at the completion of the DMA transfer. Cleared by writing zeros into these bits.
00	Not Used	Always read as 0.

UNIBUS Address Register (RPBA) (776704)

RPBA is used to address the memory location in which a transfer is to take place. RPBA forms the lower 16 bits of the address that combine with bits 05-00 of the Bus Address Extension Register (RPBAE) to create the 21-bit memory address (A17 and A16, RPCS1 bits 01 and 08, are also UNIBUS address extension bits and provide another means of reading or writing bits 17 and 16 of the extended UNIBUS address). The register is loaded with the starting memory address by the program. Each time a DMA transfer is made, the register is incremented by 2. If BAI (bus address increment inhibit, RPCS2 bit 03) is set, the incrementing of the register is inhibited and all transfers take place to or from the starting memory address.

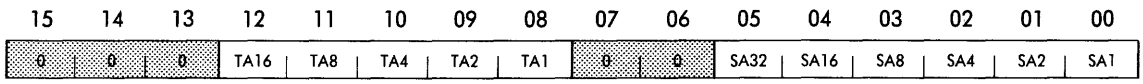


Bit	Name	Function
15-01	UNIBUS Address (BA)	Loaded by the program to specify the memory address of a transfer. The RPBA register is incremented by 2 after each transfer of a word to or from memory. Cleared by UNIBUS INIT or controller clear.
00	Not Used	Always read as 0.

Disk Address Register (RPDA) (776706)

RPDA register is used to address the sector and track on the disk to or from which a transfer is desired. RPDA is associated with the drive whose unit number appears in bits 02-00 of the Control and Status 2 register (RPCS2). Before a transfer, RPDA is loaded by the program with the address of the first block to be transferred. At the end of a transfer, RPDA contains the address of the block following the last block of the transfer.

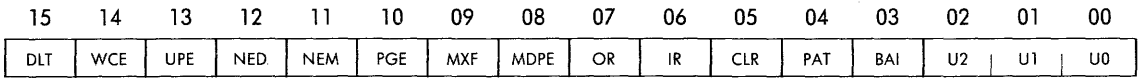
The RPDA contains a 6-bit sector address field providing for 64 sectors per track. The register also contains a 6-bit track address field providing for up to 32 data tracks per cylinder.



Bit	Name	Function
15-13	Not Used	Set to 0 by the controller.
12-08	Track Address (TA16-1)	Set by the program to specify the track on which a transfer is to start. Updated by the controller at the end of the transfer. Cleared by UNIBUS INIT.
07-06	Not Used	Set to 0 by the controller.
05-00	Sector Address (SA32-1)	Set by the program to specify the sector on which a transfer is to start. Updated by the controller at the end of the transfer. Cleared by UNIBUS INIT.

Control and Status #2 Register (RPCS2) (776710)

RPCS2 indicates the status of the controller and contains the drive unit number. The unit number specified in bits 02-00 of this register indicates which of the possible 8 logical drives is selected.



Bit	Name	Function
15*	Data Late (DLT)	Set to 0 by the controller.
14	Write Check Error (WCE)	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. WCE causes TRE (RPCS1 bit 14) to be set. If a mismatch is detected during a write-check command execution, the transfer terminates and WCE is set. The memory address displayed in RPBA (and RPBAE bits 05-00) is the address of the word following the one that did not match (if BAI, bit 03, is not set). The mismatched data word from the disk is displayed in RPDB. Cleared by UNIBUS INIT, controller clear, or loading a data transfer comand with GO (RPCS1 bit 00) set.
13	UNIBUS Parity Error (UPE)	Set if the UNIBUS parity lines indicate an error while the controller is performing a data transfer command. UPE sets TRE (RPCS1 bit 14). RPBA contains the address +2 of the memory location with the parity error. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RPCS1 bit 00) set.
12	Nonexistent Drive (NED)	Set when the program attempts a command on a drive that does not exist or is powered down. NED sets TRE (RPCS1 bit 14). Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RPCS1 bit 00) set.
11	Nonexistent Memory (NEM)	Set when the controller is performing a DMA transfer and the memory address specified in RPBA is nonexistent (does not respond to MSYN within 10 microseconds). NEM sets TRE (RPCS1 bit 14). RPBA contains the address +2 of the memory location causing the error. Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RPCS1 bit 00) set.

*Function differs from DEC definition.

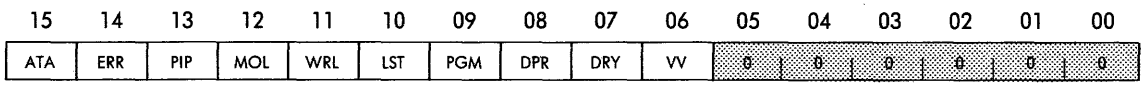
RPCS2 (Continued)

Bit	Name	Function
10	Program Error (PGE)	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. PGE sets TRE (RPCS1 bit 14). Cleared by UNIBUS INIT, controller clear, or error clear.
09*	Missed Transfer (MXF)	Set if the controller fails to detect an end of header or end of sector, or the data buffer fails to empty during a data transfer. MXF sets TRE (RPCS1 bit 14). Cleared by UNIBUS INIT, controller clear, error clear, or by loading a data transfer command with GO (RPCS1 bit 00) set.
08*	MASSBUS Data Parity Error (MDPE)	Set to 0 by the controller.
07	Output Ready (OR)	Set by the controller to indicate a word is in RPDB.
06*	Input Ready (IR)	Set to 1 by the controller.
05	Controller Clear (CLR)	When a 1 is written into this bit, the controller and all drives are initialized.
04*	Parity Test (PAT)	PAT has no effect on 9900 operation. Cleared by UNIBUS INIT or controller clear.
03	UNIBUS Address Increment Inhibit (BAI)	When BAI is set, the controller will not increment the RPBA during a data transfer. BAI bit cannot be modified while the controller is doing a data transfer (RDY, RPCS1 bit 07, negated). When set during a data transfer, all data words are read from or written into the same memory location. Cleared by UNIBUS INIT or controller clear.
02-00	Unit Select (U2-U0)	U2-U0 bits are written by the program to select a drive. The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. Cleared by UNIBUS INIT or controller clear.

*Function differs from DEC definition.

Drive Status Register (RPDS) (776712)

RPDS contains status indicators for the selected drive. The status indicators displayed are those of the drive that is specified by the unit select bits (02-00) of the RPCS2.



Bit	Name	Function
15	Attention Active (ATA)	An attention condition from a drive will set the ATA bit and the corresponding summary bit in RPAS. An attention condition is caused by: 1. Any error in the error registers if, a. GO set at completion of command. b. TO reset at occurrance of error. 2. Completion of seek, search, recalibrate, offset, or return to centerline. 3. MOL (RPDS bit 12) changing state. ATA is cleared by UNIBUS INIT, controller clear, error clear, by loading a command with GO bit (RPCS1 bit 00) set, or, if no error conditions exist, writing a 1 into the RPAS bit corresponding to the drive's unit number.
14	Error (ERR)	Set when one or more error bits in the error registers (RPER1 or RPER2) for a selected drive is set, indicating a drive error has occurred. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing zeros into the set error bit(s) in the error registers. Always read as 0.
13*	Positioning In Progress (PIP)	
12	Medium On-line (MOL)	Set for the drive upon the successful completion of the start up cycle. This bit is set when the unit ready line from the drive is asserted (indicating that the drive is up to speed, the heads are positioned over the recording tracks, and no fault condition exists within the drive), and is reset when the unit ready line is deasserted. Cleared when the drive is spun down or switch off.
11	Write Lock (WRL)	Set when the write protected line from the drive is asserted (as enabled by a switch located on the drive), indicating that the drive will not accept write commands. A write command issued on a write-locked drive will cause WLE (RPER1 bit 11) to be set.

*Function differs from DEC definition.

RPDS (Continued)

Bit	Name	Function
10	Last Sector Transferred (LST)	Set when last addressable sector on the disk pack has been read or written.
09*	Programmable (PGM)	Always read as 0.
08*	Drive Present (DPR)	Set if the drive is powered up.
07	Drive Ready (DRY)	Set at the completion of every command, data handling or mechanical motion. If this bit is reset, the program must not issue another command to this drive. When set, this bit indicates the readiness of the drive to accept a new command. DRY is the complement of GO (RPCS1 bit 00) except when the drive is nonexistent; then DRY is reset. Cleared at the initiation of a command.
06	Volume Valid (VV)	Set by the pack acknowledge or read-in preset command. When reset, VV bit indicates that the drive has been spun down and then up, and that a disk pack may have been changed. Cleared whenever drive spins up (i.e., when MOL, bit 12, becomes asserted) or when the CPU powers up.
05-00	Not used	Always read as 0.

*Function differs from DEC definition.

Error Register #1 (RPER1) (776714)

RPER1 contains the error status indicators for the drive whose unit number appears in bits 02-00 of RPCS2. The logical OR of all the error bits in the RPER1 and RPER2 registers is written into bit 14 of RPDS.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	BPE	RMR	ILR	ILF

Bit	Name	Function
15	Data Check (DCK)	If ECI (RPOF bit 11) is 0, this bit will be set if an uncorrectable ECC error is detected (ECH, bit 06 is also set). If ECI is 1 and an ECC error is detected, no correction will be attempted and this bit will be set (the ECH bit will not be set). Cleared by UNIBUS INIT, controller clear, drive clear or by writing a 0 into the bit.
14	Unsafe (UNS)	Set when a drive fault is detected. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
13	Operation Incomplete (OPI)	Set to 0 by the controller.
12	Drive Timing Error (DTE)	Set when more than one sector pulse occurs within a sector. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
11	Write Lock Error (WLE)	Set when the operating system attempts to issue a write command to a drive which has its write-protect switch on (WRL, RPDS bit 11, set). Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
10	Invalid Address Error (IAE)	Set when the address in RPDC or RPDA is invalid and a seek, search, or data transfer operation is initiated. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
09	Address Overflow Error (AOE)	Set when RPDC overflows during a read or write. Setting of this bit indicates that the desired cylinder address register has exceeded the maximum cylinder address. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.

*Function differs from DEC definition.

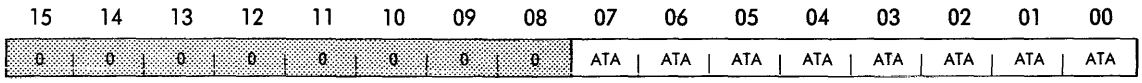
RPER1 (Continued)

Bit	Name	Function
08	Header CRC Error (HCRC)	Set by a CRC error in the header if HCI (RPOF bit 10) is reset. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
07	Header Compare Error (HCE)	If the sector counter is equal to the desired sector field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder and desired sector/track address, the header field is the required one. If HCI (RPOF bit 10) is reset and the header does not match the desired cylinder and sector/track address, HCE is set. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
06	ECC Hard Error (ECH)	Set by an uncorrectable ECC error. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
05*	Write Clock Fail (WCF)	Set to 0 by the controller.
04*	Format Error (FER)	Set when the 9900's format switch is OFF and a write header and data command is attempted. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
03*	Buffer Parity Error (BPE)	Set when a 9900 buffer parity error is detected. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
02*	Register Modification Refused (RPR)	Set to 0 by the controller.
01*	Illegal Register (ILR)	Set to 0 by the controller.
00	Illegal Function (ILF)	Set when GO (RPCS1 bit 00) is set and the function code in the control register does not correspond to a valid command. Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.

*Function differs from DEC definition.

Attention Summary Register (RPAS) (776716)

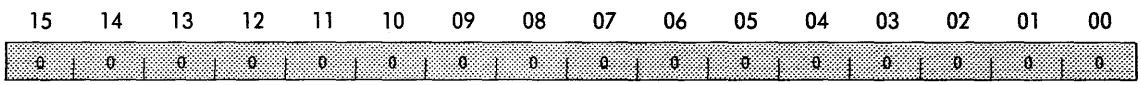
RPAS allows the program to examine the attention status of all the drives with only one register read operation. It also provides the means for resetting the attention logic in a selected group of drives. The bit displayed in each of the eight low-order positions of this register is identical to the ATA bit displayed in the RPDS for the corresponding drive. When fewer than eight drives are attached to the controller, the bits corresponding to the missing drives are always 0.



Bit	Name	Function
15-08	Not Used	Always read as 0.
07-00	Attention Active (ATA)	Each ATA bit is set when the corresponding drive asserts its ATA bit. If any drive's ATA bit is set, bit 15 of RPDS will be set. Each drive also responds in the bit position of RPAS that corresponds to its unit number, e.g., drive 02 responds in bit position 02 of RPAS. All bits are cleared by UNIBUS INIT or controller clear. Individual bits are cleared by loading a function code with GO (RPCS1 bit 00) set in the corresponding drive or by writing a 1 into the ATA bit positions of this register. Writing a 0 has no effect.

Look-ahead Register (RPLA) (776720)

RPLA is not emulated.

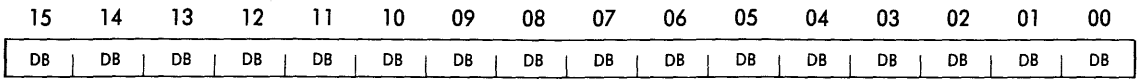


Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

*Function differs from DEC definition.

Data Buffer Register (RPDB) (776722)

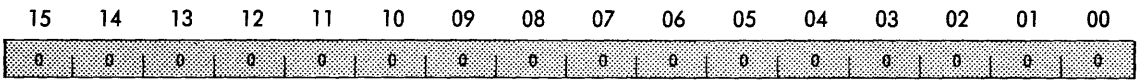
RPDB provides the bad data word resulting from a bad data compare operation.



Bit	Name	Function
15-00	Data Buffer (DB)	Contains the bad data word from a data compare operation.

Maintenance Register #1 (RPMR) (776724)

RPMR is not emulated.

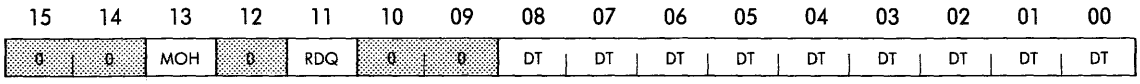


Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

*Function differs from DEC definiton.

Drive Type Register (RPDT) (776726)

RPDT register allows the program to distinguish between different types of drives.



Bit	Name	Function
15-14	Not Used	Set to 0 by the controller.
13	Moving Head (MOH)	Set to 1 by the controller since drives are moving head devices.
12	Not Used	Set to 0 by the controller.
11*	Drive Request Required (DRQ)	Set to 0 by the controller.
10-09	Not Used	Set to 0 by the controller.
08-00	Drive Type (DT)	These bits contain a code indicating the drive type being emulated. This is determined by the controller firmware (RP0X) and by switch settings in the controller as shown in Table C-2.

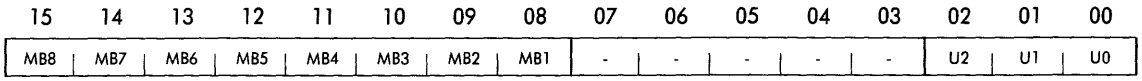
Table C-2. Drive Type Switch Settings

Drive Type	08	07	06	05	04	03	02	01	00	Octal
RP04	0	0	0	0	1	0	0	0	0	20
RP05	0	0	0	0	1	0	0	0	1	21
RP06	0	0	0	0	1	0	0	1	0	22

*Function differs from DEC definition.

Serial Number Register (RPSN) (776730)

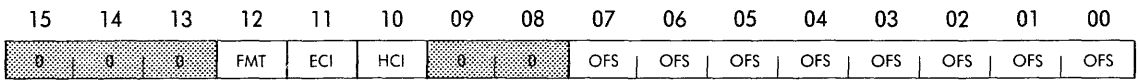
RPSN register is used to distinguish a drive from similar drives attached to the same controller. The serial number provides a means of distinguishing between different capacity drives with the same drive type code.



Bit	Name	Function
15-08	Model Byte (MB8-MB1)	These bits contain a copy of the model byte switch setting on the radial drive interface board associated with the drive (see 9900 Controller User's Guide for details of model byte switch settings for different drives and emulations.
07-03	Undefined	Reserved to System Industries.
02-00	Unit (U2-U0)	Contains a copy of the logical unit number of the drive.

Offset Register (RPOF) (776732)

RPOF contains the positioner offset information supplied to the drive directly by the operating system prior to issuance of the offset command. The drive has the ability to offset the positioner approximately 200 micro-inches from the track centerline in either direction.

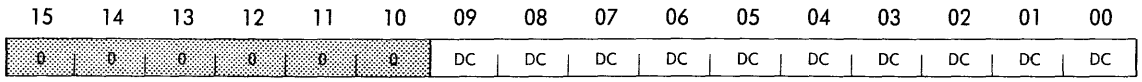


Bit	Name	Function
15-13	Not Used	Set to 0 by the controller.
12*	Format 16 (FMT)	Set to 1 by the controller.
11	Error Correction Inhibit (ECI)	Set when the software inhibits error correction. If an ECC error is detected and this bit is reset, the 9900 Controller begins the ECC correction process at the end of the sector. If the error is correctable, it will be corrected in the 9900's buffer and the transfer will proceed (software transparent -no error indication). If the error is uncorrectable, the controller will set ECH and DCK (RPER1 bits 15 and 06). If the ECC bit is already set, however, the error correction process will be inhibited and DCK will be set (ECH will not be set). Cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
10	Header Compare Inhibit (HCI)	Set when the software inhibits the repeating of header compare errors HCE and HCRC (RPER1 bits 07 and 08). When the 9900 Controller sees this bit asserted, it will ignore the header compare logic and CRC check. With HCI set, the controller depends only on the hardware sector counter comparison for sector identification. If the sector count is out of sequence, the wrong sector may be affected by the data transfer. HCI is cleared by UNIBUS INIT, controller clear, drive clear, or by writing a 0 into this bit.
09-08	Not Used	Set to 0 by the controller.
07-00	Offset (OFS)	When these bits become set, there is no effect on controller operation (RP0X offset command not emulated).

*Function differs from DEC definition.

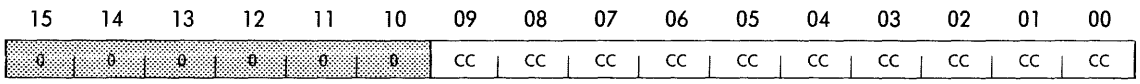
Desired Cylinder Register (RPDC) (776734)

RPDC contains the address of the cylinder to which the drive positioner moves the heads for a seek, search, or data handling command.



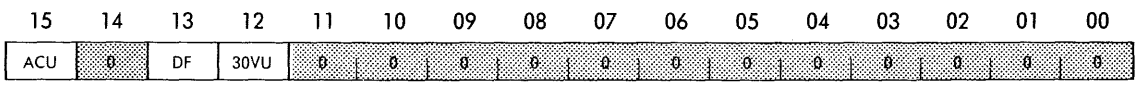
Bit	Name	Function
15-00	Not Used	Set to 0 by the controller.
09-00	Desired Cylinder (DC)	Set by the program to specify the required cylinder address. IAE (RPER1 bit 10) will be set if, when asserting GO (RPCS1 bit 00) for a data transfer, seek, or search command, this register contains an address larger than the maximum cylinder address on the drive.

Current Cylinder Register (RPCC) (776736)



Bit	Name	Function
15-10	Not Used	Set to 0 by the controller.
09-00	Current Cylinder (CC)	This register operates in conjunction with the desired cylinder address register. It is updated at the end of each operation, and contains the positioner location.

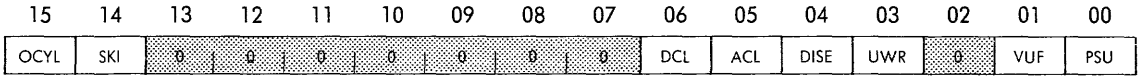
Error Register #2 (RPER2) (776740)



Bit	Name	Function
15	AC Unsafe (ACU)	Power low condition detected in the controller.
14	Not Used	Set to 0 by the controller.
13	Drive Fault (DF)	Set when a drive fault occurs.
12	30 Volts Unsafe (30VU)	Power low condition detected in the controller.
11-00	Not Used	Set to 0 by the controller.

Error Register #3 (RPER3) (776742)

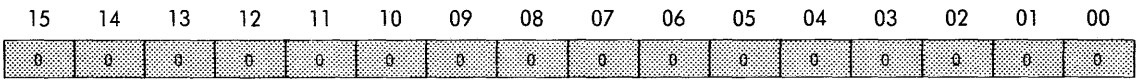
RPER3 contains detailed error status information and is primarily used for monitoring the electro-mechanical performance of the drive rather than the interface.



Bit	Name	Function
15*	Off Cylinder (OCYL)	Set to 0 by the controller.
14	Seek Incomplete (SKI)	Set when a seek operation fails to complete within 500ms from a seek initiation.
13-07	Not Used	Set to 0 by the controller.
06*	DC Low (DCL)	Power low condition detected in the controller.
05*	AC Low (ACL)	Power low condition detected in the controller.
04*	Disable Error (DISE)	Set to 0 by the controller.
03*	Any Unsafe (UWR)	Power low condition detected in the controller.
02*	Not Emulated	Set to 0 by the controller.
01*	Velocity Unsafe	Set to 0 by the controller.
00*	Pack Speed Unsafe (PSU)	Set to 0 by the controller.

ECC Position Register #1 (RPEC1) (776744)

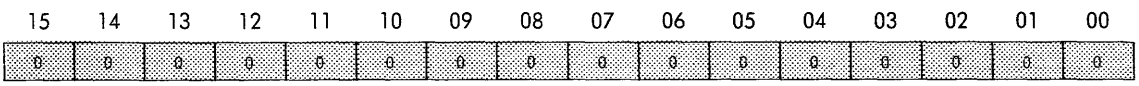
RPEC1 is not emulated.



Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

ECC Pattern Register #2 (RPEC2) (776746)

RPEC2 is not emulated.



Bit	Name	Function
15-00*	Not Emulated	Set to 0 by the controller.

*Function differs from DEC definition.

APPENDIX D
RP0X REGISTER SUMMARY

Control and Status Register #1 (RPCS1) (776700)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	0	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO

Word Count Register (RPWC) (776700)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC

UNIBUS Address Register (RPBA) (776704)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	0

Disk Address Register (RPDA) (776706)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	TA16	TA8	TA4	TA2	TA1	0	0	SA32	SA16	SA8	SA4	SA2	SA1

Control and Status Register #2 (RPCS2) (776710)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

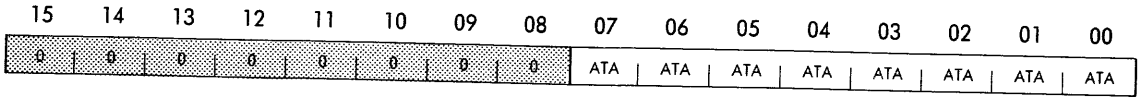
Drive Status Register (RPDS) (776712)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	0

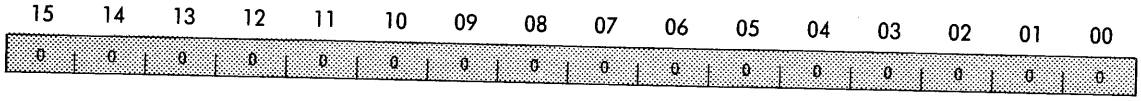
Error Register #1 (RPER1) (776714)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WLF	FER	BPE	RMR	ILR	ILF

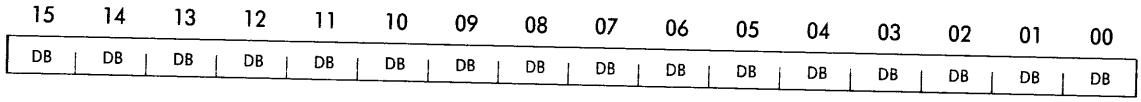
Attention Summary Register (RPAS) (776716)



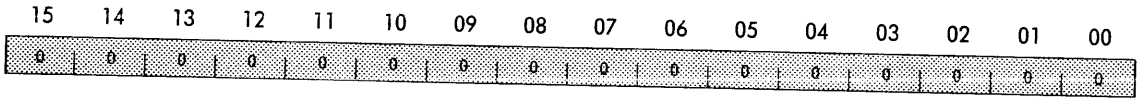
Look-Ahead Register (RPLA) (776720)



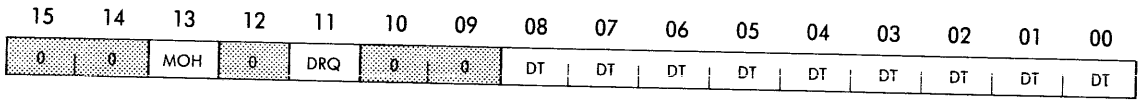
Data Buffer Register (RPDB) (776722)



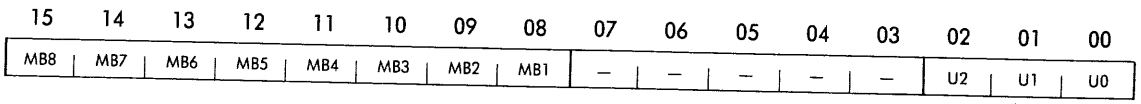
Maintenance Register (RPMR) (776724)



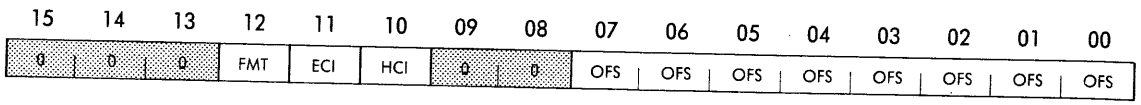
Drive Type Register (RPDT) (776726)



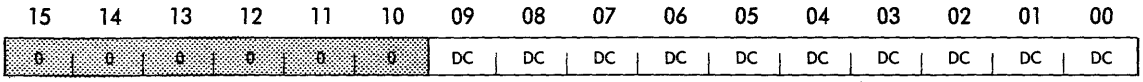
Serial Number Register (RPSN) (776730)



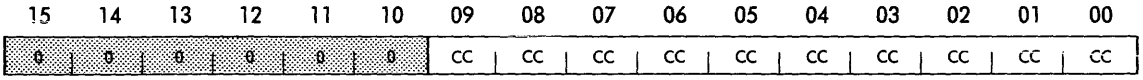
Offset Register (RPOF) (776732)



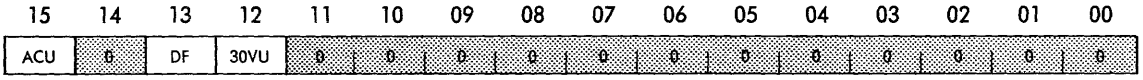
Desired Cylinder Register (RPDC) (776734)



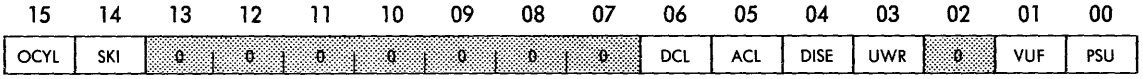
Current Cylinder Register (RPCC) (776736)



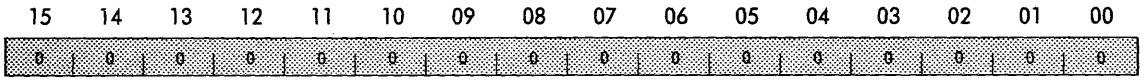
Error Register #2 (RPER2) (776740)



Error Register #3 (RPER3) (776742)



ECC Position Register #1 (RPEC1) (776744)



ECC Pattern Register #2 (RPEC2) (776746)