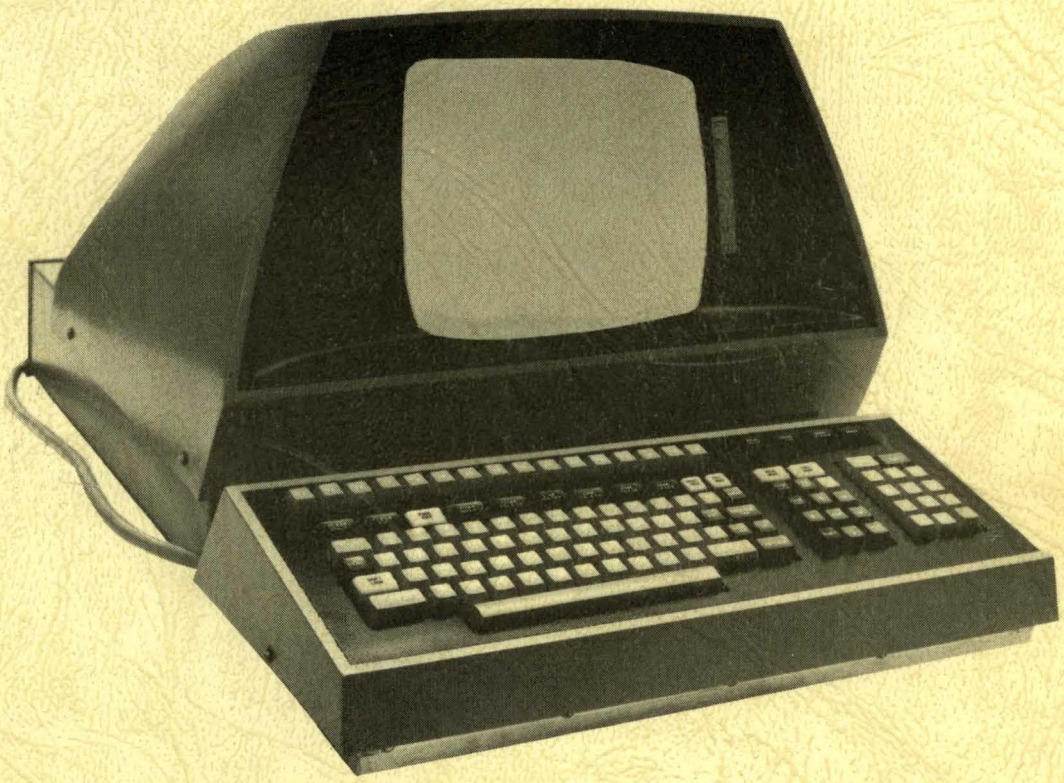
REFERENCE

MANUAL



T-5101

INTERACTIVE

DISPLAY

TERMINAL

Systematics General Corporation

National Scientific Laboratories Division

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SECTION I

T-5101 Specification

INTRODUCTION

The purpose of this manual is to provide operation and maintenance information for the T-5101 Interactive Display Terminal.

The scope of the material provided is sufficient in all aspects of operation and maintenance of the equipment.

The T-5101 consists of cable-interconnected assemblies. This unit is in turn connected to a computer by an additional interface cable.

The T-5101 Interface Display Terminal is shown in Figure 1-1.

Figure 1-1. T-5101 Interactive Display Terminal

T-5101 SPECIFICATIONS

Display

80 Character Lines	24
Character Positions	1920
Character Set	96 ASCII (Upper Case)
Screen Phosphor	White (P4)
Face Plate	Etched
Refresh Rate	60 Pages/Second
Protected Fields	Reduced Intensity
Status Displays	8
Control Characters Display	31
Blinking Field Rate	4 per second
Security Fields	Display Suppressed
Page Roll	Up

Cursor

Format	Reverse Video Block
Controls	Forespace, Backspace Upline, Downline, New Line, Return, Home, Tab Backtab, Position Addressing, Position Reading

Data Transmission

Code	Asynchronous ASCII 10 unit code
Parity	Even

Data Transmission

Interface	RS-232-C
Rates	110, 150, 300, 600, 1200, 2400, 4800, 9600 Baud
Duplex	Full and Half
Modes	Conversational Block Line, Page or Message (all or foreground)

Keyboard

Construction	Separate
Character and Control Keys	68
Cursor and Format Keys	14
Numeric Keys Pad	14
Function Keys	16
Transmission Send Control Keys	Page, Line, Message
Interlocking	Two Key rollover
Key Operation	2 ounce
Lighted Mode Keys	Shift Lock, Write Protect Program, Conversation, Page Edit

Memory

Storage Capacity	1920 Characters
Security Locations	Display Suppressed
Control Character Storage	Direct from Keyboard or Computer

Memory

Protected Fields	Character Protect Bit

Data Editing

Keyboard Editing	
Character	Type over, Insert, Delete
Line	Insert, Delete, Erase to End of line
Page	Clear all or foreground to Nulls or Spaces, Erase to End of Page (Replace All or Foreground with Nulls or Spaces)
Protected Fields	Reduced Intensity
Computer Controlled Editing	All of Above with Receipt of ESC Sequences

Tempest

Complies With NACSEM 5100, As Modified By AFNAG-9A

Physical Characteristics

Dimensions	
Display	14.12"H x 20.5"W x 18"L
Keyboard	4"H x 20.5"W x 9"L
Weight	55 lbs.
A-C Power Requirement	115 Volt, 60 Hz
Environment	5-50^{c}C; 41-122^{c}F 5-95% Relative Humidity without Condensation

SECTION II

MICROCONTROLLER PROGRAMMING

The organization of data transmission and control for the T-5101 interactive data display terminal is given in the data flow block diagram, Figure 2-1 below. A detailed description of control and programming for the microcontroller follows. Specific details of the terminal logic and control devices are contained in schematic drawing 129361, sheets 7-1 through 7-22, contained in Section 7.

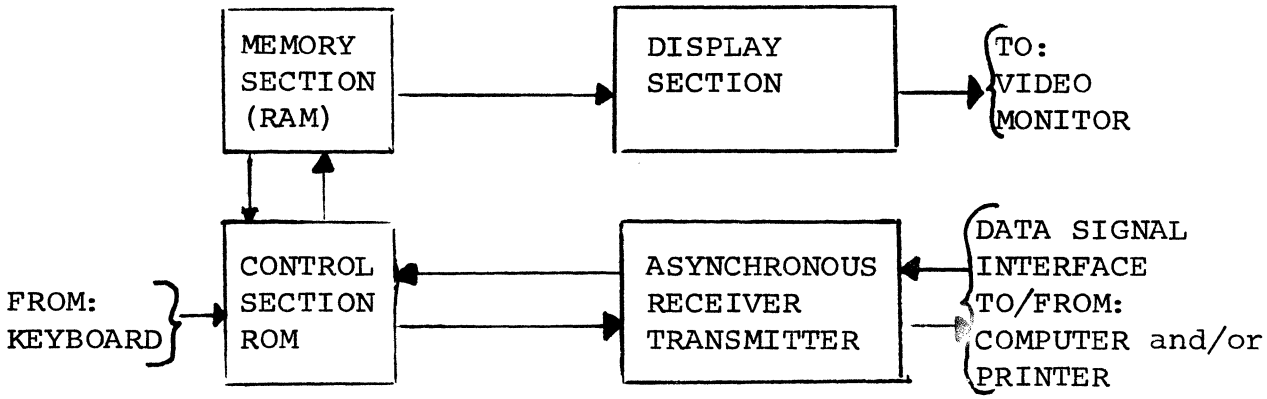


Figure 2-1. T-5101 Main Circuit Board
Data Flow Block Diagram

T-5101 Data organization is based on random access memory time sharing between control section and display section, with the display section given highest priority for the refresh function and the control section given secondary priority. The display function utilize random access memory 27% of the time leaving 73% for the control functions. This sharing organization provides the T-5101 with greater reliability of terminal operations since fewer components are required.

Data information and control commands are transferred internally between the various logic sections and components over a tri-state (memory, control, timing) bus.

Keystroke signals enter the main logic board as 8 bit parallel data codes, along with strobe signals. However, data received from an interfacing computer is received as ASCII seven bit serial data. The logic board has a serial-parallel converter to translate serial ASCII codes to parallel codes as well as a FIFO buffer to allow time for operations which are longer than inter character intervals in fast transmission rate environments.

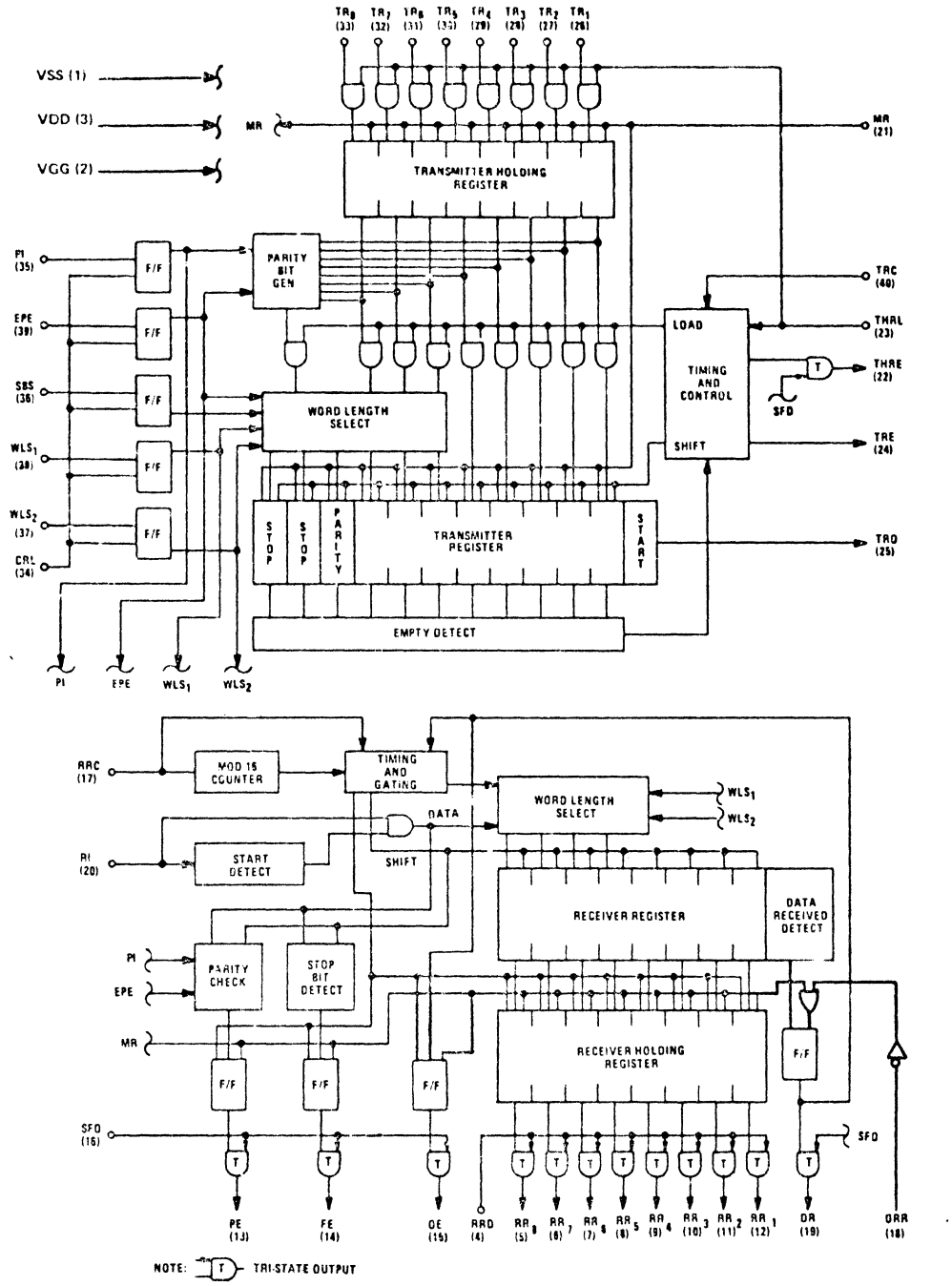
The transmitter/receiver is an LSI/UART chip which (1) accepts serial ASCII 10 or 11 unit codes (word structure option is strappable) from an RS-232-C standard interface or 20 ma current loop optional interface and (2) transmits an equivalent 8 bit parallel code as a data word to the control section. Furthermore, the universal asynchronous transmitter/receiver (UART) also decodes 8 bit words received from the T-5101 control section and transmits serial ASC II over the data signal interface. See Figure 2-2 for additional details of the UART.

Information transfer is controlled in the T-5101 by the microcontrol logic commanded by codes stored in a preprogrammed ROM. The standard T-5101 terminal functions are contained in four pages (256-8 bit words/pages) of microcode, with printer extension option requiring an additional page, and terminal polling option needing two pages.

The display memory section consists of 16 random access memory (RAM) chips, providing storage capacity of 2048 8-bit words. This memory provides useful character storage of 1920 characters, 24 lines of 80 characters each. The memory section also contains conversion logic necessary to monitor display cursor position.

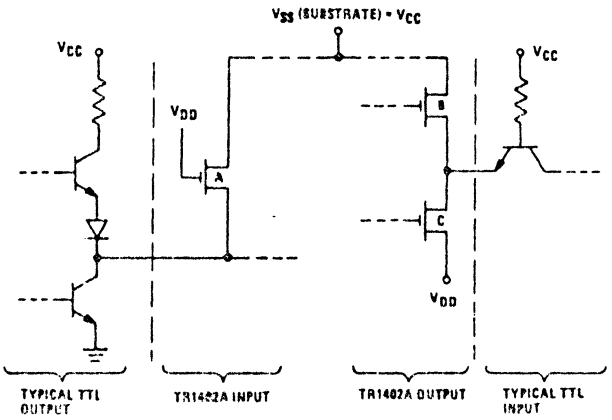
The display section consists of four main subsections, i.e., (1) Character Generator, (2) Row Refresh Logic, (3) Cursor Display Logic, and (4) Timing Control. In addition to the above functions, display section also provides control for reduced luminance (protected fields) and 8-status indicator displays.

Actual registers used in the T-5101 micro controller code are summarized and listed in Table 2-2.



INPUT STRUCTURE

MOS DEVICE "A" ACTS AS AN INTERNAL PULL-UP RESISTOR TO $V_{SS} = V_{CC}$ WHICH BIASES OFF THE CASCODE DEVICE OF THE TTL OUTPUT IN THE HIGH-LEVEL OUTPUT STATE. IN THE LOW-LEVEL OUTPUT STATE THE TTL OUTPUT DEVICE SINKS THE CURRENT SUPPLIED BY DEVICE "A".



OUTPUT STRUCTURE

DEVICES "B" & "C" COMPRISE A PUSH-PULL OUTPUT BUFFER. IN THE LOW-LEVEL STATE, OUTPUT TRANSISTOR "C" IS "ON" AND CASCODE DEVICE "B" IS OFF. IN THE HIGH-LEVEL STATE, THE OPPOSITE IS TRUE. IN THE DISCONNECTED STATE, BOTH "B" AND "C" ARE TURNED OFF CAUSING THE OUTPUT NODE TO FLOAT.

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART)

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 volts Supply
2	V_{GG} POWER SUPPLY	V_{GG}	-12 volts Supply
3	V_{DD} POWER SUPPLY	V_{DD}	Ground
4	RECEIVER REGISTER DISCONNECT	RRD	A high-level input voltage. V_{IH} applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8-RR_1 data outputs (pins 5-12).
5-12	RECEIVER HOLDING REGISTER DATA	RR_8 RR_1	The contents of the RECEIVER HOLDING REGISTER appear on these lines in parallel if a low-level input voltage, V_{IL}, is applied to RRD. Program control selection of a word length less than eight (8) bits will cause the most significant bits of the character to be forced to a low-level output voltage, V_{OL}. The character will be right justified. RR_1 (pin 12) is the least significant bit of the character.
13	PARITY ERROR	PE	The status of the parity verification circuit appears on this line, if a low-level input voltage, V_{IL}, is applied to the STATUS FLAGS DISCONNECT (pin 16) control line. Wired OR capability is provided on this line allowing PE lines from other arrays to be OR tied. A high level output voltage, V_{OH}, on this line (under the conditions above)

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART) (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
			indicates a PARITY ERROR in the received parity bit as programmed by the EVEN PARITY ENABLE control line (pin 39). The status is updated each time a character is transferred from the RECEIVER REGISTER to the RECEIVER HOLDING REGISTER.
14	FRAMING ERROR	FE	The status of the STOP bit detection circuit appears on this line if a low-level input voltage, V_{IL}, is applied to the STATUS FLAG DISCONNECT (pin 16) control line. Wired OR capability is provided on this line allowing FE lines from other arrays to be OR tied. A high-level output voltage, V_{OH}, indicates that the received character has no valid STOP bit, i.e., the bit following the parity bit is not a high-level input voltage, V_{IH}.
15	OVERRUN ERROR	OE	The status of the DATA RECEIVED circuit appears on this line of a low-level input voltage, V_{IL}, is applied to the STATUS FLAG DISCONNECT (pin 16) control line. Wired OR capability is provided on this line allowing OE lines from other arrays to be OR-tied. A high level output voltage, V_{OH}, indicates that the previously received character was not read (DR line not reset) before the present character was transferred to the RECEIVER HOLDING REGISTER.

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART)(Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE circuit outputs.
17	RECEIVER REGISTER CLOCK	RRC	This clock is sixteen (16) times faster than the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic after power turn-on. It resets all registers and sets the serial output line to a high-level output voltage, V_{OH}.
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output Voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART) (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage. V_{IL}, to a high level input voltage. V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage. V_{OH}. on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit DATA bits, PARITY bit, and STOP bit), are serially shifted out on this line. This line will remain at a high level output voltage, V_{OH}, when no data is being transmitted. A start of transmission is defined as the transition from a high-level output voltage, V_{OL}, of the start bit.

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART) (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
26-33	TRANSMITTER REGISTER DATA INPUTS	TR_1-TR_8	Parallel 8-bit characters are input on these lines into the TRANSMITTER HOLDING REGISTER with THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the least significant bits only are accepted. The character is right justified into the least significant bit. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V_{IH}, on the line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	PARITY INHIBIT	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits. The STOP bit(s) will immediately follow the last data bit on transmission if parity is uninhibited. A low-level input voltage, V_{IL}, enables the parity generation and verification circuits. PI will, when a high-level input voltage, V_{IH}, is applied, also clamp the $\overline{PE}$ line (pin 13) to a low-level output voltage, V_{OL}.
36	STOP BIT(S) SELECT	SBS	This line selects the number of STOP bits generated after the PARITY bit during transmission. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit.

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART) (Continued)

PIN NUMBER	NAME	SYMBOL	FUNCTION
37-38	WORD LENGTH SELECT	WLS_2 WLS_1	These two lines select the character length to be 5, 6, 7, or 8 bits.

WLS_2	WLS_1	WORD LENGTH
V_{IL}	V_{IL}	5 bits
V_{IL}	V_{IH}	6 bits
V_{IH}	V_{IL}	7 bits
V_{IH}	V_{IH}	8 bits

39	EVEN PARITY ENABLE	EPE	This line selects either even or odd PARITY to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRANSMITTER REGISTER CLOCK	TRC	This CLOCK is sixteen (16) times faster than the desired transmitter shift rate.

Figure 2-2. T-5101 Asynchronous Receiver/Transmitter (UART) (Continued)

Information is transferred between functional units by way of the tristate bus, TSB, under microprogram control. This information transfer consists of eight-bit characters transmitted in parallel between the following units.

TABLE 2-1. T-5101 FUNCTIONAL UNITS

Unit Mnemonic	Unit	
RCV	From	External Serial Source via UART Receiver
KEY	From	Keyboard
CPR	From	Cursor position row register
CPC	From	Cursor position character register
LIT	From/To	Eight bit literal register
RDR	From	Random access page buffer via the Read Data Register
WDR	To	Random access page buffer via the Write Data Register
LRC	From/To	Modulo 2 adder and accumulator (7 bits)
ADD	From	Switch (8 bits) internal, manually set
MACR	From/To	Random access page buffer row counter (address register high order five bits)
INPUT		Utility Register*
OUTPUT		Utility Register*
CMD		Utility Register*
MAR	From/To	Margin Register
IND	From/To	Indicator Register
CNTR	From/To	Counter Register

* Unused in Standard T-5101

TABLE 2-2. TABLE OF REGISTER USAGE

Register Symbol	Register Name	Description
WDR	Write Data Register	Eight bit character register contains characters to be written into the R.A.M. from tri state bus.
RDR	Read Data Register	Eight Bit register to contain characters read from the R.A.M. for transfer to tri state bus.
MACC	Memory Address Counter Character	Contains low order 7 bits of the R.A.M. address accessible to the tri state bus (column).
MACR	Memory Address Counter Row	Contains high order 5 bits of the R.A.M. address accessible to the tri state bus (row).
ARTO	Communications Interface UART	
ART1	Auxiliary Interface UART (printer, etc.)	
LIT	Literal (8 bit) Register	Used to transfer constants from ROM to tri state bus.
CPR	Cursor Row Position Register	
CPC	Cursor Character Position Register	
KEY	Keyboard Register	
LRC	Longitudinal Transmissions Check Register	For modulo 2 sum check of transmission characters.
RCV	Receiver	Receiver character register

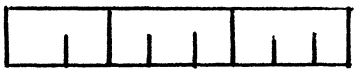
TABLE 2-2. TABLE OF REGISTER USAGE (Continued)

Register Symbol	Register Name	Description
ADD		Switches set manually inside cabinet
MAR	Margin Register	Eight bit utility register used for temporary holding of dynamic data.
CNTR	Counter Register	Eight bit utility register used for holding program counter during subroutine calls, and for incremented or decremented comparisons.
IND	Indicator Register	Eight bit register controls lighted indicators at right hand side of screen. 1 = lighted..
CMD	Command Register	Not used in standard MMDC.
OUTPUT	Output Register	Not used in standard MMDC.
INPUT	Input Register	Not used in standard MMDC.

INSTRUCTION SET FOR T-5101 MICRO CONTROLLER

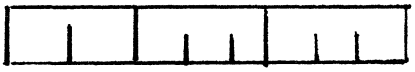
Instructions may be partitioned into two classes, those which occupy two eight bit bytes and those which occupy one eight bit byte. These can be represented as six or three octal digits, respectively, where the high order bit in each word is assumed to be zero. The implied ninth bit is, of course, not actually present in the eight bit hardware.

high order word



($D_{1,2}$ $D_{1,1}$ $D_{1,0}$)

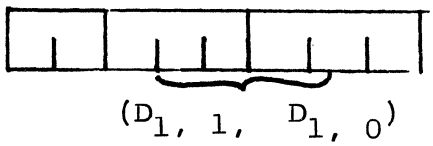
low order word (if required)



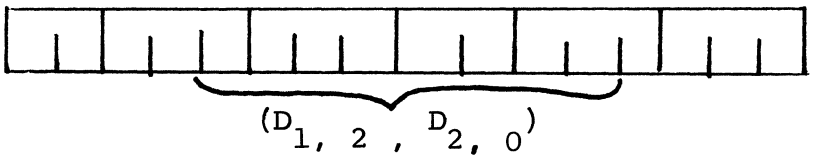
($D_{2,2}$ $D_{2,1}$ $D_{2,0}$)

Where $D_{i,j}$ is the j^{th} octal digit for the i^{th} 8 bit word.

Subfields of instructions will be indicated by only the high order and low order octal digits in parentheses, for example: Only high order word:



or both high and low order words:



Examples of terminal control functions written in the T-5101 mnemonic instruction set are given at the conclusion of this section.

TABLE 2-3. T-5101 INSTRUCTION SET

001	READ	072	CLR STB6	220	JFC OFLO
003	WRITE	073	SET STB6	221	JFC MAC=CPR
004	CLR WDR	074	CLR STB7	222	JFC OPT1
005	LOA WDR	075	SET STB7		
006	SET WPROT	076	CLR STB8	230	JFC RDR
007	CLR WPROT	077	SET STB8	231	JFC RPE
016	SET PROTM	100	JMP	232	JFC RFE
017	CLR PROTM	120	SEL ARTO	234	JFC THRE
020	CLR MACC	121	SET RTSO	235	JFC CTS
021	LOA MACC	122	CLR RTSO	236	JFC TRE
022	SET MACC	123	LOA ARTO	237	JFC NORS/OPT2
023	INC MACC	124	CLR ARTO	240	JFC PROTM
024	DEC MACC	130	SEL ART1	241	JFC PROT
027	LOA CPR	131	SET RTS1	242	JFC INTIN
030	CLR MACR	132	CLR RTS1	243	JFC FULL
031	LOA MACR	133	LOA ART1	243	JFC KEYST2
032	SET MACR	134	CLR ART1	244	JFC OPNC
033	INC MACR	150	LOA LIT	244	JFC RESET
034	DEC MACR	156	CLR LRC	245	JFC CONV
035	INH CUR	157	CLK LRC	246	JFC FDX
036	ENA CUR	160	TSB=RDR	247	
037	SET BEEP	161	TSB=KEY		
040	LOA OUTPUT	162	TSB=RCV	250	JFC MACC
042	LOA MAR	163	TSB=LIT	251	JFC NULL
044	LOA IND	164	TSB=CPC	252	JFC LIT7
045	CLR IND	165	TSB=CPR	253	JFC LIT8
046	LOA CMD	166	TSB=LRC	260	JFC STB1
051	LOA CNTR			261	JFC STB2
052	INC CNTR	170	TSB=ADD	262	JFC STB3
053	DEC CNTR	172	TSB=INPUT	263	JFC STB4
054	SET TIME	173	TSB=MAR	264	JFC STB5
055	SET BIN	174	TSB=IND	265	JFC STB6
056	CLR RTSEN	175	TSB=CNTR	266	JFC STB7
057	SET RTSEN	200	JFC TSB1	267	JFC STB8
060	CLR STB1	201	JFC TSB2	300	JTC TSB1
061	SET STB1	202	JFC TSB3	301	JTC TSB2
062	CLR STB2	203	JFC TSB4	302	JTC TSB3
063	SET STB2	204	JFC TSB5	303	JTC TSB4
064	CLR STB3	205	JFC TSB6	304	JTC TSB5
065	SET STB3	206	JFC TSB7	305	JTC TSB6
066	CLR STB4	207	JFC TSB8	306	JTC TSB7
067	SET STB4	210	JFC KEYSTR	307	JTC TSB8
070	CLR STB5	213	JFC CALL	310	JTC KEYSTR
071	SET STB5	214	JFC RTN	313	JTC CALL

TABLE 2-3. T-5101 INSTRUCTION SET (Continued)

314	JTC RTN	337	JTC NRST/OPT2	350	JTC MACC
320	JTC OFLO	340	JTC PROTM	360	JTC STB1
321	JTC MAC=CPR	341	JTC PROT	352	JTC LIT7
322	JTC OPT1	342	JTC INTIN	353	JTC LIT8
330	JTC RDR	343	JTC FULL	360	JTC STB1
331	JTC RPE	343	JTC KEYST2	361	JTC STB2
332	JTC RFE	344	JTC OPNC	362	JTC STB3
333	JTC ROE	344	JTC RESET	363	JTC STB4
334	JTC THRE	345	JTC CONV	364	JTC STB5
335	JTC CTS	346	JTC FDX	365	JTC STB6
336	JTC TRE	347		366	JTC STB7
				367	JTC STB8

TABLE 2-4. RANDOM ACCESS MEMORY CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
READ	001	Transfers the contents of the RAM location indicated by the contents of MACR, MACC into the RDR
WRITE	003	Transfers the contents of the WDR into the RAM location indicated by the contents of MACR, MACC
LOA WDR	005	Replaces the contents of the WDR with the contents currently on the TSB
CLR WDR	004	Clears the WDR
TSB=RDR	160	Sets the contents on the TSB equal to the contents of the RDR
SET WPROT	006	Sets the write protect bit on all words subsequently written into the RAM
CLR WPROT	007	Clears the write protect bit on all words subsequently written into the RAM
SET PROTM	016	Set the PROTM. This status bit is used as a global condition by the program to disable the over-writing of any characters in the RAM for which the WPROT bit is set
CLR PROTM	017	Clear the PROTM. This global condition enables the overwriting of write protected characters

TABLE 2-5. RAM ADDRESS CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
CLR MACC	020	Set character counter to left margin
CLR MACR	030	Set row counter to top row
LOA MACC	021	Set character counter to value on tri state bus
LOA MACR	031	Set row counter to value on tri state bus
LOA CPR	027	Sets contents of CPC and CPR equal to current contents of MACC and MACR, respectively
SET MACC	022	Set character counter to right margin
SET MACR	032	Set row counter to bottom row
INC MACC	023	* Move character counter right one position
INC MACR	033	* Move row counter down one line
DEC MACC	024	* Move character counter left one position
DEC MACR	034	* Move row counter up one line
SET BIN	055	This instruction, if followed immediately by LOA MACC or LOA MACR, will load the binary value of the (TSB) rather than the interpreted character value normally loaded.

* These operations will set OFLO if they cause character address to run off either margin or if they cause row address to run off top or bottom of page.

TABLE 2-6. ROM INSTRUCTION EXECUTION SEQUENCE CONTROL

Mnemonic	($D_{1,2}$ $D_{2,0}$)	Description
JMP	10P LLL	Causes next instructions to be taken from the location indicated by LLL on page P
JTC	3CC LLL	Causes next instructions to be taken from the location indicated by LLL on the local page if the condition indicated by CC is true. Instructions are taken in normal sequence otherwise. (See table of conditions for values of CC.) (See note below for CALL and RTN.)
JFC	2CC LLL	Causes next instructions to be taken from the location indicated by LLL on the local page if the condition indicated by CC is false. Instructions are taken in normal sequence otherwise. (See table of conditions for values of CC.) (See Note below for CALL and RTN.)
(NOTE: Transfer of control to subroutines on the same page are facilitated by the CALL and RTN conditions as follows:)		
JFC CALL	213	Causes contents of the program counter to be transferred to CNTR prior to transfer of control
JFC RTN	214	Causes contents of CNTR to replace contents of program counter. LLL is ignored. CNTR must be incremented prior to this operation

TABLE 2-7. TABLE OF CONDITIONS

Mnemonic	Condition Identifier	Description
TSB1	00	Tri State Bus Bit 1
2	01	Tri State Bus Bit 2
3	02	Tri State Bus Bit 3
4	03	Tri State Bus Bit 4
5	04	Tri State Bus Bit 5
6	05	Tri State Bus Bit 6
7	06	Tri State Bus Bit 7
8	07	Tri State Bus Bit 8
KEYSTER	10	Keyboard strobe
OFLO	20	MACC/MACR overflow or underflow
MAC=CPR	21	Set if MACR equals CPR
OPT1	22	Wire straps on main logic board
PROTM	40	Set if in character protection mode
PROT	41	Character protect bit in RAM and protect mode
CONV	45	Conversation mode
CALL	13	Subprogram call
RTN	14	Subprogram return
RDR	30	RCV Data ready
RPE	31	RCVR parity error
RFE	32	RCVR framing error

TABLE 2-7. TABLE OF CONDITIONS (Continued)

Mnemonic	Condition Identifier	Description
ROE	33	RCVR overflow
THRE	34	Transmitter holding register ready
CTS	35	Clear to sent (asynchronous transmission)
TRE	36	Transmitter register empty
$\overline{\text{RESET}}$/OPT2	37	Reset by OPT 2 (Strap)
INTIN	42	Extended memory option
KEYST2	47	Send Key Strobe Line (operation keys)
RESET	44	Reset key (also used with extended memory)
FDX	46	Full duplex
MACC	50	(TSB) equals (MACC)
NULL	51	(TSB) equals (NULL)
LIT7	52	(TSB) equals (LIT) seven bits only (1 through 7)
LIT8	53	(TSB) equals (LIT) eight bits
STB1	60	Status BIT 1
2	61	Status BIT 2
3	62	Status BIT 3
4	63	Status BIT 4
5	64	Status BIT 5

TABLE 2-7. TABLE OF CONDITIONS (Continued)

Mnemonic	Condition Identifier	Description
6	65	Status BIT 6
7	66	Status BIT 7
8	67	Status BIT 8

TABLE 2-8. TABLE OF CONDITION SIGNIFICANCE

Condition Mnemonic	Use or Action Resulting
WPROT	Write Protect bit copies into RAM each Write
PROTM	Write Protect mode
STB1	Status Bits set by microprogram for global control
2	Status Bits set by microprogram for global control
3	Status Bits set by microprogram for global control
4	Status Bits set by microprogram for global control
5	Status Bits set by microprogram for global control
6	Status Bits set by microprogram for global control
7	Status Bits set by microprogram for global control
8	Status Bits set by microprogram for global control

TABLE 2-8. TABLE OF CONDITION SIGNIFICANCE (Continued)

Condition Mnemonic	Use or Action Resulting
RTSO	Request to sent (Main ART)
RTS1	Request to send (Auxiliary ART)
TSB1	Tri State Bus Bits
2	Tri State Bus Bits
3	Tri State Bus Bits
4	Tri State Bus Bits
5	Tri State Bus Bits
6	Tri State Bus Bits
7	Tri State Bus Bits
8	Tri State Bus Bits
KEYSTR	Keyboard Strobe
CALL	Causes transfer of contents of program counter to CNTR when set
RTN	Causes transfer of contents of CNTR to program counter when set
RDR	Receiver Data Ready, set when receiver has assembled character
RPE	Received Parity Error, set if receiver detects parity error
THRE	Transmitter Holding Register, true when ready for next character
CTS	Clear to Send, remote device ready for text in asynchronous transmissions
TRE	Transmitter register empty indicator

TABLE 2-8. TABLE OF CONDITION SIGNIFICANCE (Continued)

Condition Mnemonic	Use or Action Resulting
KEYST2	Second key stroke true when depressed key is control function (clear, edit, etc.)
NRST	Reset key
FDX	True when in full duplex in conversational mode
MACC	True if contents of TSB equals contents of MACC
NULL	True if contents of TSB are null
LIT7	True if contents (7 bits) of TSB equals contents of LIT
LIT8	True if contents (8 bits) of TSB equals contents of LIT

Flag Control

Flags are set or cleared by the microprogram to either control certain hardward functions or set global conditions controlling the microprogram actions (see table of flags below). General instructions for flags are as follows:

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	ACTION
CLR	CAA	Clears the indicated flag. (See table flags for values of CAA.)
SET	CAA	Sets the indicated flag. (See table flags for value of CAA.)

TABLE 2-9. TABLE OF FLAGS

Mnemonic	Set	Clear	Description
WPROT	006	007	Write Protect
PROTM	016	017	Protect Mode
STB1	061	060	Program Global
STB2	063	062	Program Global
STB3	065	064	Program Global
STB4	067	066	Program Global
STB5	071	070	Program Global
STB6	073	072	Program Global
STB7	075	074	Program Global
STB8	077	076	Program Global
BEEP	037	(Clears automatically)	Causes one BEEP
RTSO	121	122	Communication Channel Request to Send
RTS1	131	132	Auxiliary Channel Request to Send
BIN	055	(Automatic after 1 cycle)	Modifies LOA and LOA MACR instructions

Literal Control

The literal register provides a means of entering a constant from the ROM onto the tri state bus (TSB). This command is:

MNEMONIC	$(D_{1,2}\ D_{1,0})$	$(D_{2,2}\ D_{2,0})$
LOA LIT	150	XXX

and causes the contents of LIT to be replaced by XXX.

NOTE: Content of LIT is changed by JMP instruction

Asynchronous Receiver/Transmitter Control

In addition to the main transmitter/receiver interface, normally associated with the computer, an additional transmitter/receiver interface is accommodated by the following instructions. This facilitates such optional devices as an auxiliary printer.

TABLE 2-10. ASYNCHRONOUS RECEIVER/TRANSMITTER CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
SEL ART0	120	Selects main receiver transmitter interface
SEL ART1	130	Selects auxiliary receiver transmitter interface
LOA ART0	123	Loads main transmitter from TSB
LOA ART1	133	Loads auxiliary transmitter from TSB
CLR ART0	124	Clear main data ready flag
CLR ART1	134	Clear auxiliary data ready flag

Transmission Longitudinal Checking

A 7-bit modulo 2 adder, LRC, is provided for transmission checking as follows:

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
CLR LRC	156	Clear LRC
CLK LRC	157	Replace each bit of the LRC with the Modulo 2 sum of its prior setting and the corresponding bit of the TSB.

Tri State Bus Control

The tri state bus contents are set equal to any one of the following registers by the indicated command. (See Table of Register Usage, Table 2-2.)

TABLE 2-11. TRI STATE BUS CONTROL

Mnemonic	($D_{1,2}$ $D_{1,0}$)	Description
TSB=RDR	160	Set the TSB contents equal to RDR
TSB=KEY	161	Set the TSB contents equal to KEY
TSB=RCV	162	Set the TSB contents equal to RCV
TSB=LIT	163	Set the TSB contents equal to LIT
TSB=CPC	164	Set the TSB contents equal to CPC
TSB=CPR	165	Set the TSB contents equal to CPR
TSB=LRC	166	Set the TSB contents equal to LRC
TSB=ADD	170	Set the TSB contents equal to ADD
TSB=INPUT	172	Set the TSB contents equal to INPUT
TSB=MAR	173	Set the TSB contents equal to MAR
TSB=IND	174	Set the TSB contents equal to IND
TSB=CNTR	175	Set the TSB contents equal to CNTR

Display Control

Several commands facilitate modifications of the screen display.

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
INH CUR	035	Inhibits display of cursor
ENA CUR	036	Enables display of cursor
LOA IND	044	A one (1) on TSB complements corresponding IND bit.
CLR IND	045	Clears IND

Utility Register Control

MNEMONIC	($D_{1,2}$ $D_{1,0}$)	DESCRIPTION
TSB=MAR	173	Sets TSB contents equal to that of the MAR
LOA MAR	042	Sets MAR contents equal to that of TSB
TSB=CNTR	175	Sets TSB contents equal to that of the CNTR
LOA CNTR	051	Sets CNTR contents equal to that of the TSB
INC CNTR	052	Increments contents of CNTR
DEC CNTR	053	Decrements contents of CNTR

T-5101 MICROCONTROLLER PROGRAM EXAMPLE

Page	ROM Address Octal	ROM Word Octal		Entry Point Label	Instruction	
0	0	124	260	RESET	CLR ARTO	
0	1	17	270	o	CLR PROTM	
0	2	100	280	o	JMP	RESET 10
0	3	104				
0	4	100	310	IDLE35X	JMP	IDLE 35
0	5	32				
0	6	37	320	BELL	SET BEEP	
0	7	261	330	IDLE	JFC STB2	IDLE 10
0	10	12				
0	11	124	340	o	CLR ARTO	

Page	ROM Address Octal	ROM Word Octal		Entry Point Label	Instruction	
0	12	62	350	IDLE10	CLR STB2	
0	13	120	360	o	SEL ARTO	
0	14	36	370	o	ENA CUR	
0	15	234	380	o	JFC THRE	IDLE 20
0	16	22				
0	17	236	390	o	JFC TRE	IDLE 20
0	20	22				
0	21	122	400	o	CLR RTSO	
0	22	222	410	IDLE20	JFC OPT1	IDLE30
0	23	26				
0	24	105	420	o	JMP	POLIDLE
0	25	0				
0	26	365	440	IDLE30	JTC STB6	PRINTINGO
0	27	114				
0	30	330	450	o	JTC RDR	RECEIVE
0	31	165				
0	32	310	460	IDLE35	JTC EKYSTR	IDLE40
0	33	50				
0	34	337	470	o	JTC NRST	IDLE
0	35	7				

T-5101 MICROCONTROLLER PROGRAM EXAMPLE (Continued)

Page	ROM Address Octal	ROM Word Octal		Entry Point Label	Instruction	
0	36	60	480	KRESET	CLR STB1	
0	37	174	490	o	TSB=IND	
0	40	206	500	o	JFC TSB7	KRESET 10
0	41	46				
0	42	150	510	o	LOA LIT	100
0	43	100				
0	44	163	520	o	TSB=LIT	
0	45	44	530	o	LOA IND	
0	46	102	540	KRESET10	JMP	KBDENBL
0	47	47				
0	50	161	550	IDLE40	TSB=KEY	
0	51	51	560	o	LOA CNTR	
0	52	35	570	o	DIS CUR	
0	53	207	580	o	JFC TSB8	IDLE50
0	54	57				
0	55	101	590	o	JMP	FKEY
0	56	174	600	IDLE50	TSB=IND	
0	60	300	610	o	JTC TSB1	IDLE
0	61	7				
0	62	347	620	o	JTC KEYST2	ESCL02

Page	ROM Address Octal	ROM Word Octal		Entry Point Label	Instruction	
0	63	206				
0	64	260	630	o	JFC STB1	IDLE60
0	65	71				
0	66	161	640	o	TSB=KEY	
0	67	101	650	o	JMP	ESCHAR
0	70	132				
0	71	150	660	IDLE60	LOA LIT	33
0	72	33				
0	73	175	670	o	TSB=CNTR	
0	74	352	680	o	JTC LIT7	IDLE70
0	75	100				
0	76	101	690	o	JMP	DATACHAR
0	77	0				
0	100	61	700	IDLE70	SET STB1	
0	101	5	710	o	LOA WDR	
0	102	100	720	o	JMP	IDLE
0	103					
0	104	15	730	RESET10	SET BLOCK	
0	105	320	740	o	JTC OFLO	RESET20
0	106	107				

T-5101 MICROCONTROLLER PROGRAM EXAMPLE (Continued)

Page	ROM Address Octal	ROM Word Octal		Entry Point Label	Instruction	
0	107	156	750	RESET20	CLR LRC	
0	110	166	760	o	TSB=LRC	
0	111	42	770	o	LOA MAR	
0	112	100	780	o	JMP	CLEAR 08
0	113	255				
0	114	337	790	PRINTING0	JTC NRST	PRINTING1
0	115	122				
0	116	66	800	o	CLR STB4	
0	117	71	810	o	SET STB5	
0	120	100	820	o	JMP	KRESET
0	121	36				

SECTION III

THEORY OF OPERATION

INTRODUCTION

The T-5101 interactive data display terminal is a modern, versatile microprogram controlled device designed to provide input/output access to an electronic computer. The T-5101 terminal is designed with four main functional modules:

a. Cathode Ray Tube Display and Monitor

b. Circuit Board with micro controller, memory and logic electronics

c. Power Supply

d. Keyboard with key encoding electronics

The terminal is assembled in an attractive, TEMPEST Modified housing together with necessary switches, hardware, cabling and cooling fan to accomplish display and memory functions. The keyboard is housed in its own enclosure, suitable for integral mounting with the T-5101 display housing or being located remotely (maximum of 5 ft.) from the display unit.

CATHODE RAY TUBE DISPLAY

The T-5101 displays alphanumeric data on the screen of a white CRT, through use of solid state monitor with raster scan. Data characters, either graphic or control, may be entered on the screen from the terminal keyboard or received from a remote computer for display.

Characters are displayed as a 5 x 9 dot matrix in a 7 x 11 dot field. Each character is alloted eleven raster lines, nine for accommodating either upper or lower case 5 x 7 characters and two for interline spacing. Horizontal intercharacter spacing is provided for the T-5101 display with two dot columns between characters.

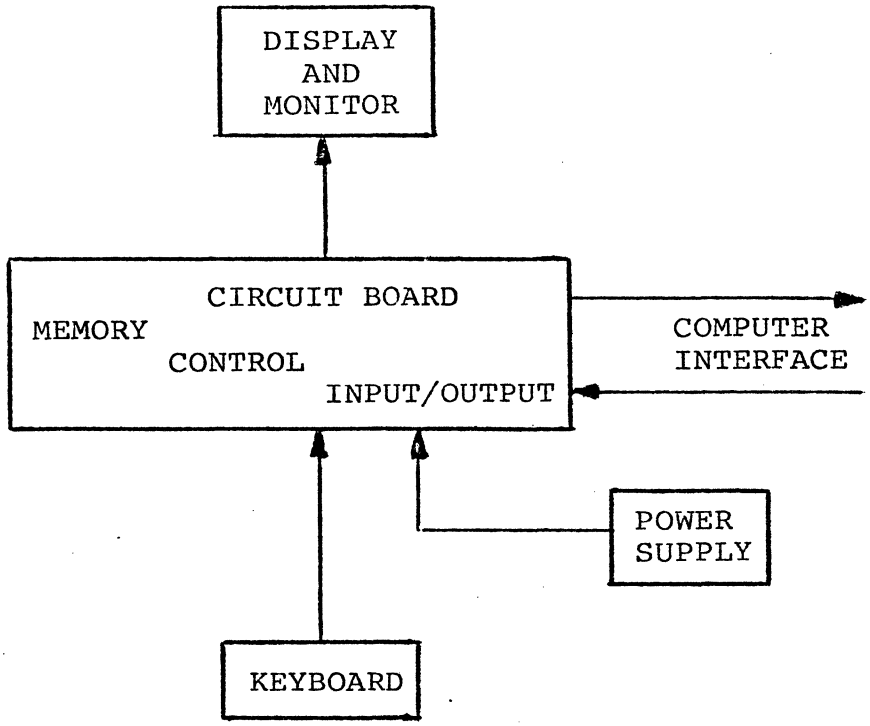


Figure 3-1.

T-5101
FUNCTIONAL BLOCK DIAGRAM

OPERATOR'S QUICK REFERENCE GUIDE

CONTROL

FUNCTION	SEQUENCE
CURSOR ←	CTRL / H
CURSOR ↓	CTRL / J
CURSOR ↑	CTRL / K
CURSOR →	CTRL / L
HOME	CTRL/ ^
SKIP	CTRL / I
NEW LINE	CTRL/—
*PROTECT ON	ESC &
*PROTECT OFF	ESC '
START WRITE PROTECT	ESC)
END WRITE PROTECT	ESC (
CLEAR ALL TO UNPROTECT SP	ESC +
SEND LINE UNPROTECT	ESC 4
SEND PAGE UNPROTECT	ESC 5
SEND LINE PROTECT	ESC 6
SEND PAGE PROTECT	ESC 7
CLEAR ALL TO NULL	ESC *
CLEAR PG TO NULL	ESC :
CLEAR PG TO SPACE	ESC ;
KEYBOARD ENABLE	ESC "
KEYBOARD DISABLE	ESC #
LOAD CURSOR	ESC =
READ CURSOR	ESC ?
ADM-1 MODE ON	ESC %
ADM-1 MODE OFF	ESC $
CHAR INSERT	ESC Q
CHAR DELETE	ESC W
LINE INSERT	ESC E
LINE DELETE	ESC R
LINE ERASE	ESC T
ERASE PAGE	ESC Y
PARTIAL SEND	ESC S
BACK TAB	ESC I
START/END BLINK FIELD	ESC ^
START/END BLANK FIELD	ESC _
*SET BLOCK MODE	ESC B
*SET CONVERSATION MODE	ESC C

*Use available key rather than escape sequence when making a keyboard entry. (PROT MODE, PAGE EDIT, CONV MODE)

ABSOLUTE CURSOR POSITIONING

X or Y	ASCII CODE	X or Y	ASCII CODE	X or Y	ASCII CODE
1	SPACE	28	;	55	V
2	!	29	<	56	W
3	"	30	=	57	X
4	#	31	>	58	Y
5	$	32	?	59	Z
6	%	33	@	60	[
7	&	34	A	61	\
8	'	35	B	62	]
9	(	36	C	63	^
10	)	37	D	64	_
11	*	38	E	65	`
12	+	39	F	66	a
13	,	40	G	67	b
14	—	41	H	68	c
15	.	42	I	69	d
16	/	43	J	70	e
17	0	44	K	71	f
18	1	45	L	72	g
19	2	46	M	73	h
20	3	47	N	74	i
21	4	48	O	75	j
22	5	49	P	76	k
23	6	50	Q	77	l
24	7	51	R	78	m
25	8	52	S	79	n
26	9	53	T	80	o
27	:	54	U		

TRANSMIT Y, THEN X.

BACK PAGE	ESC I	ERASE LINE TO NULL	ESC t
FORWARD PAGE	ESC K	ERASE PAGE TO NULL	ESC y
*SET PAGE EDIT	ESC N	SET STATUS 1	ESC c
CLEAR PAGE EDIT	ESC O	CLEAR STATUS 1	ESC b
PRINT PAGE	ESC P	SET STATUS 2	ESC e
UNFORMAT PRINT PAGE	ESC p	CLEAR STATUS 2	ESC d
SET PROGRAM MODE	ESC U	SET STATUS 3	ESC g
CLEAR PROGRAM MODE	ESC X	CLEAR STATUS 3	ESC f
SET COLUMN TAB	ESC V	SET STATUS 4	ESC <
		CLEAR STATUS 4	ESC >

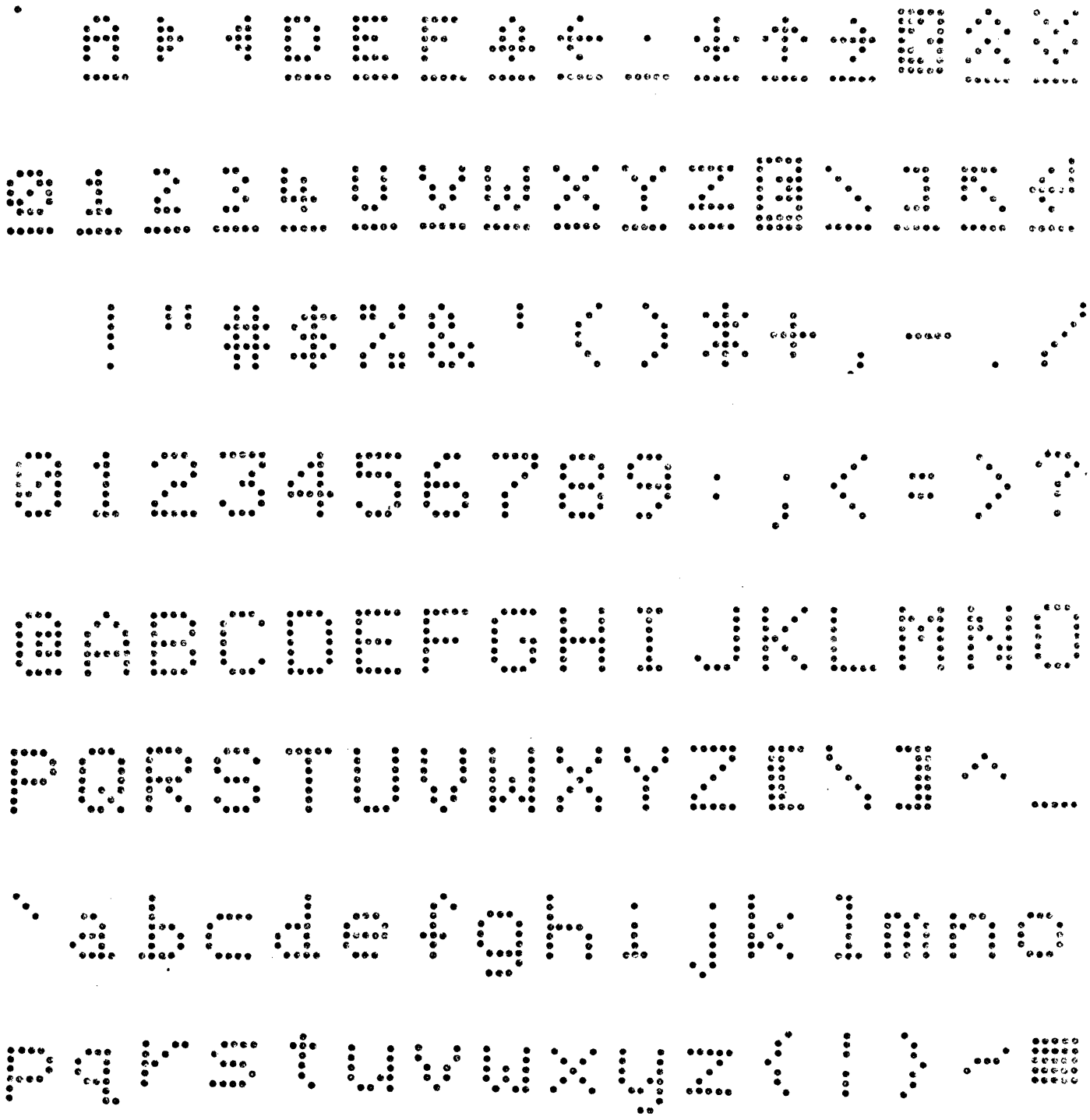


Figure 3-2. CHARACTER FORMAT (By Ascending ASCII Codes)

The standard display character set for the T-5101 is 96 characters ASCII. Control characters (32) can be displayed if: 1) preceded in transmission from computer or keyboard by ASCII ESC U code sequence or, 2) if terminal status is set to program mode.

Reverse image display is used if the cursor is positioned over data. Selected fields on the T-5101 display may be 1) caused to blink at 4 images/second, 2) protected from overwriting, characters of which are displayed with reduced intensity or 3) blanked by inhibiting the display of character stored in terminal memory locations corresponding to security fields. In addition, eight status indicators are displayable on the right of the screen, each as a full 14 x 9 dot block.

A complete page of characters in the T-5101 contains 24 character lines, each with 80 character positions, providing a total display capacity of 1920 characters per page. Display fields are refreshed at a rate set by a crystal oscillator synchronously with 60 Hz input power in the standard terminal. This rapid refresh rate generates flicker-free images and high contrast display even in bright ambient light.

Vertical and horizontal beam deflections for the display are generated by trigger signals derived from the T-5101 system clock and logic input to the monitor. The CRT monitor is a solid-state unit designed for reliability and high quality reproduction in industrial and commercial installations. The theory of operations of the monitor is detailed in Section IV of this reference manual.

MAIN CIRCUIT BOARD

All of the T-5101 terminal control functions are incorporated in a single printed circuit board mounted directly beneath the CRT display tube. Using a single circuit board eliminates interconnections and cabling, and increases terminal reliability. The board contains the microcontroller, display memory logic electronics, transmission rate control and data interface electronics. Discussion of the functions of the main circuit board is given in detail in Section III of this manual.

POWER SUPPLY

The T-5101 main logic board is supplied with 5 volts D.C. from a separate power supply module. The T-5101 D.C. power supply is rated at 12 amps and is equipped with its own solid state voltage regulator

and current limiter. Line and load regulation of .075% assures stable D.C. power availability for all T-5101 display terminal functions.

KEYBOARD

Your T-5101 terminal is equipped with a standard 118 key keyboard, capable of being located remotely up to 5' from the T-5101 display unit. Keys are positioned on 3/4" centers with 3/8" offset needing 2 oz. operating force, and have two key rollover feature such that if a key is depressed before a previously operated key is released, the second key code is transmitted upon release of the first key. The T-5101 Keyboard layout is depicted in Figure 3-3.

Normal Keyboard Operation

Single keystrokes or certain simultaneous multiple keystrokes are encoded into ASCII seven bit binary codes which are either stored in memory, displayed, and/or transmitted to the data interface depending upon the transmission or program mode of the T-5101. ASCII Control characters can be entered into memory and displayed on the screen while the terminal is in program mode. Terminal functions and keys used are given in Table 3-1.

The T-5101 standard keyboard encodes 96 ASCII characters for transmission and display, As an option, the T-5101 keyboard can be equipped to encode lower case alphabetic characters and the special characters ` , { , } , ¦ , ~ , for display.

The T-5101 keyboard can be enabled and disabled locally and remotely by computer control using the following sequence of keystrokes or equivalent ASCII codes:

ESC # disables all keyboard functions except RESET

ESC " enables the keyboard and restores keyboard control.

Since ESC # sequence may be accidentally initiated manually, the keyboard may need to be unlocked by depressing the RESET key.

SHIFT LOCK — Key provides a lock of the shift function that is cleared by operation of either shift key.

The "locked" shift does not perform the shift operation on the special function keys, PRINT key, SEND keys, CLEAR keys, EDIT keys or TAB keys.

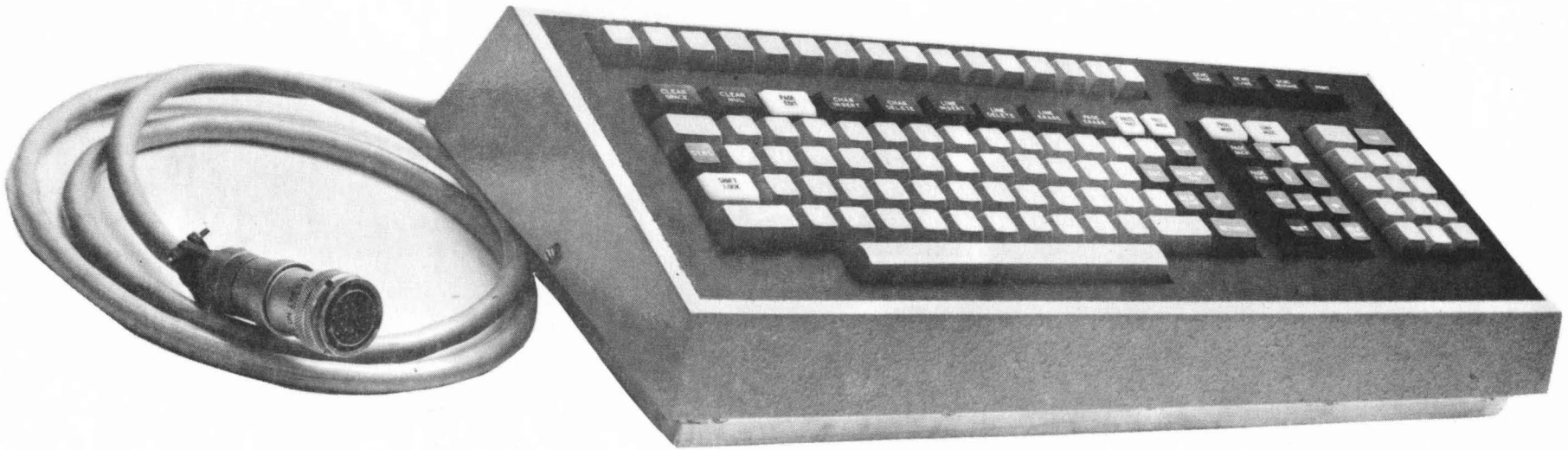


Figure 3-3. Keyboard

Table 3-1. KEYBOARD OPERATIONS

Operation	Keys Used
A. CHARACTER DISPLAY	
1. Alphabetic Upper Case	A to Z
2. Alphabetic Lower Case (Optional with SHIFT)	A to Z
3. Numeric	0 to 9 Main Keyboard or Numeric Pad
4. Special Characters	: - @ _ [ ] ; ^ \ , . /
5. Special Characters with SHIFT	! " # $ % & ' ( ) * = ` { } + ~ | < > ?
6. Special Characters with CTRL or CTRL/SHIFT	

ASCII CODE	DISPLAYED CHARACTER	KEYS USED
NULL		
SOH	A	CTRL/A
STX	▶	SHIFT/SOM-EOM, CTRL/B
ETX	◀	SOM-EOM, CTRL/C
EOT	D	CTRL/D
ENQ	E	CTRL/E
ACK	F	CTRL/F
BEEP	G	CTRL/G
BS	←	←, CTRL/H
HT	→	TAB, CTRL/I
LF	↓	LF, ↓, CTRL/J
VT	↑	↑, CTRL/K
FF	→	→ , CTRL/L
CR	◀	RETURN, CR, CTRL/M
SO	↑	CTRL/N
SI	↓	CTRL/O
DLE	P	CTRL/P
DC1	Q	CTRL/Q
DC2	R	CTRL/R
DC3	S	CTRL/S
DC4	T	CTRL/T
NAK	U	CTRL/U

Table 3-1. KEYBOARD OPERATIONS (Continued)

ASCII CODE	DISPLAYED CHARACTER	KEYS USED
SYN	V	CTRL/V
ETB	W	CTRL/W
CAN	X	CTRL/X
EM	Y	CTRL/Y
SUB	Z	CTRL/Z
ESC	■	ESC, CTRL/[
FS	\	CTRL/\
GS	]	CTRL/]
RS	^	HOME
US	↵	NEW LINE

Operation	Keys Used
7. No Display (ASCII SP)	SPACE
8. Protect Displayed Characters	PROT MODE, WRITE PROT
B. CURSOR CONTROL	
1. Cursor HOME	HOME
2. Position in Line	
a. Left margin of Same Line	RETURN, CR
b. Same Column of Next Line	LF
c. Left Margin of Next Line	NEW LINE
3. Position New Field	TAB SET, TAB, BACKTAB
4. Increment Up	↑
Down	↓
Left	←
Right	→

Table 3-1. KEYBOARD OPERATIONS (Continued)

Operation	Keys Used
C. TERMINAL CONTROL	
1. Reset	RESET
2. Break	BREAK
3. Clear Screen or Foreground to:	
a. Spaces	CLEAR SP
b. Null Codes	CLEAR NUL
4. Audible Tone	CTRL/G
5. Display Extended Memory Control (Optional)	PAGE FWD. PAGE BACK
D. DATA TRANSMISSION CONTROL	
1. Transmission Mode	BLOCK MODE. CONV MODE
2. Transmission Initiation (block mode)	SEND LINE. SEND MESSAGE. SEND PAGE
3. Send to Printer	PRINT
4. Transmitted Text Delimiters	SOM - EOM
5. Special Functions	F1 to F16

BINARY CODES

	CONTROL			GRAPHIC CHARACTER SET						ESCAPE SEQUENCE					
BITS	BITS	0	1	2	3	4	5	6*	7*	2	3	4	5	6	7
4321	765	000	001	010	011	100	101	110	111	010	011	100	101		
0000		NUL	DLE	SP	Ø	@	P	`	p				P PRINT PAGE		p UNFORMAT PRINT
0001		SOH	DC1	!	1	A	Q	a	q	!		A	Q INSERT CHAR		
0010		STX	DC2	"	2	B	R	b	r	" KBD ENA		B SET BLOCK	R DELETE LINE	b STATUS OFF	
0011		ETX	DC3	#	3	C	S	c	s	# KBD DISA		C SET CONV	S SEND MSG	c STATUS 1 ON	s SEND MSG ALL
0100		EOT	DC4	$	4	D	T	d	t	$ END MODE -1	4 SEND FG LINE	D	T ERASE LINE	d STATUS 2 OFF	t LINE TO NULL
0101		ENQ	NAK	%	5	E	U	e	u	% SET MODE -1	5 SENG FG PAGE	E INSERT LINE	U SET PGM MODE	e STATUS 2 ON	u CLR PGM MODE
0110		ACK	SYN	&	6	F	V	f	v	& SET PROTM	6 SEND ALL LINE	F	V SET TAB COLUMN	f STATUS 3 OFF	
0111		BEEP	ETB	'	7	G	W	g	w	' CLEAR PROTM	7 SEND ALL PAGE	G	W DELETE CHAR	g STATUS 3 ON	
1000		(←) BS	CAN	(	8	H	X	h	x	(CLEAR WPROT		H	X CLEAR PGM MODE		
1001		(SKIP) HT	EM	)	9	I	Y	i	y	) SET WPROT		I BACK TAB	Y ERASE PAGE	i TAB (SKIP)	y PAGE TO NULL
1010		LF (↓)	SUB	*	:	J	Z	j	z	* CLEAR ALL NULL	: CLEAR FG NULL	J PAGE BACK	Z		
1011		VT (↑)	ESC	+	;	K	[	k	{	+ CLEAR ALL SPACE	; CLEAR FG SPACE	K PAGE FWD	[		
1100		FF (→)	FS	,	<	L	\	l	¦		< STATUS 4 ON	L	\		
1101		CR	GS	-	=	M	]	m	}		= LOAD CURSOR	M	]		
1110		SO	(HOME) RS	.	>	N	^	n	~		> STATUS 4 OFF	N SET PAGE EDIT	^ START/END BLINK FIELD		
1111		SI	(NEW LINE) US	/	?	O	_	o	DEL		? READ CURSOR	O CLEAR PAGE EDIT	START/END BLANK FIELD		

*DISPLAYED AS UPPER CASE

Escape Sequences

ESCAPE sequences are initiated locally by using the ESC key or remotely by computer control to transmit an ASCII ESC code which enables the T-5105 under micro program control to interpret the next character or string of characters as special control instructions. The sequences are used for:

a. Keyboard enabling/disabling.

b. Formating; i.e. field protection, field security and field blinking.

c. Data Transmission Control; character, line, page or message.

d. Data Editing Control.

e. Absolute Cursor addressing/reading.

f. Selecting Special operation modes.

g. Controlling the serial printer (optional).

FORMATING AIDS

Numerous display and data entry formating aids are furnished as standard with the T-5105 terminal. These can be used under operator control from the T-5105 keyboard or activated by computer control. A summary list of these aids follow:

Table 3-4. FORMATING AIDS

Format Control	Keyboard Control	Computer Codes
Column Tab Set	TAB SET	ESC V
Tab	SHIFT-BACKTAB/TAB	ESC i, CTRL I
Back Tab	BACKTAB/TAB	ESC I
Security Field Start/End	ESC _	ESC _
Blinking Field Start/End	ESC ^	ESC ^
Protect Mode On	SHIFT-PROT MODE (lit)	ESC &
Protect Mode Off	PROT MODE (Unlit)	ESC /
Write Protect Start	SHIFT-WRITE PROT (lit)	ESC)
Write Protect End	WRITE PROT (Unlit)	ESC (

Column Tab Set (ESC V)

This control sets the protect mode and writes a vertical column of protected spaces in the column containing the cursor from the row in which cursor is positioned downward to display bottom row. Existing protected characters will not be overwritten. Cursor stops at the first unprotected position to the right of its original position. Tab set operation sets protect mode.

Tab (ESC i/CTRL I)

If MMDC is not in protect mode, actuation of TAB key will transmit (or write to memory if in block mode) an ASCII HT code.

When the terminal display is operated in protect mode, either operation of the TAB key or receipt of ASCII HT code will move the cursor rightward from its position to the first unprotected position following a protected field, continuing down the screen if necessary. If no protected positions are encountered, cursor will stop at home position.

Backtab (ESC I)

This operation causes the cursor to move leftward to the first character position of the unprotected field in which it resides. If the cursor already occupies the first position of an unprotected field it will continue to the first character of the preceding field, upscreen, line-by-line, continuing past home position, to the last unprotected position on the screen.

Blanked (Security) Fields (ESC_)

The operator may wish to designate certain fields in T-5105 character memory to be non-display for security reasons. The ESC _ sequence is provided to write a protected CAN character (CTRL X) as a field delimiter.

Blinking Field (ESC ∧)

Blinking display fields are established by using an ESC ∧ sequence to write a protected BEL delimit character. Blinking fields are blinked at a rate of four (4) images/second.

DATA EDITING OPERATIONS

Complete data editing capabilities are provided with the T-5105 terminal. The keyboard contains an ample arrangement of keys for single keystroke editing. Microprogram terminal control provides the T-5105 with ability to accommodate remote data editing with codes transmitted immediately after ASCII ESC. Editing operations have the following features:

Clear Foreground (ESC ;) or All (ESC +) to SPACES

The CLEAR-SPACES key will clear terminal foreground, i.e., all unprotected display fields and corresponding memory locations to unprotected space codes. Cursor is then positioned to the first unprotected position at or after HOME. Use of CLEAR-SPACES with SHIFT clears all fields, protected and unprotected, to unprotected spaces and positions the cursor to HOME.

The T-5105 display protect mode will be reset "off" with a CLEAR-SPACES (ALL) operation.

Clear Foreground (ESC :) or All (ESC *) to NULL

Use of the CLEAR-NUL key performs a virtually identical operation

as CLEAR-SPACES above, except that the foreground (or all locations) fields are replaced with unprotected NUL codes.

Page Edit (ESC N and ESC O)

The PAGE EDIT key will set (ESC N) and reset (ESC O) the T-5105 page editing mode which is used with character editing operations. This key is illuminated when page edit mode is on and unlit otherwise. Page edit mode provides additional capability for character and line editing as described below.

Character Insert (ESC Q)

Use of the CHAR INSERT key moves character under the cursor, and all characters to the right of the cursor, one space forward. If a protected field is in the same line as the cursor, no characters are moved into or over that protected field, and the rightmost character is lost. Similarly, a CHAR INSERT operation in a line of unprotected characters terminates rightward character movement in the 80th column, and the last character is lost.

Use of the PAGE EDIT mode key avoids loss of line data while CHARACTER INSERT operation occurs. If PAGE EDIT mode is on (PAGE EDIT key illuminated), use of CHAR INSERT key will move all characters rightward one space, wrapping around down screen, until either (1) a protected field is encountered (2) a NUL code is detected in the 80th position of any line, or (3) end of page is encountered, in which case only the last character on the page or within the field in which editing operation is being done is lost.

Character Delete (ESC W)

The CHAR DELETE key causes the character beneath the cursor to be overwritten with the character to the right of the cursor. All characters following on the right are moved one position leftward until end of line or a protected field is reached. The last position on a line or last unprotected position before a protected field is filled with an unprotected space.

If the T-5105 is in the PAGE-EDIT mode, the above sequence continues down screen, wrapping around line-by-line leftward to fill the position caused by character deletion until either a protected field or end of page is detected.

Line Insert (ESC E)

This key creates a line of spaces at the line position containing the cursor. The data on the line on which the cursor is located, and all on following lines move downward one line, causing the loss of data on the bottom line. Cursor does not move downward, but is positioned at the left margin of the inserted line of spaces. LINE INSERT is inhibited if T-5105 is in the protect mode.

Line Delete (ESC R)

The LINE DELETE key overwrites the line containing the cursor with the data on the line below, and moves all following data lines up one line. Cursor moves to the left margin of same line. The bottom line is written with unprotected spaces. LINE DELETE is inhibited in protect mode.

Erase Line to SPACES (ESC T) or NULS (ESC t)

Actuation of LINE ERASE key causes all unprotected characters on the same line under and to the right of the cursor to be erased to spaces or to nulls (LINE-ERASE with SHIFT). If T-5105 is in protect mode with write protect status on, the spaces or NUL will be written as protected characters. Cursor will remain at its original position or move to first rightward unprotected position, if the original position becomes protected.

Erase Page to SPACES (ESC Y) or NULS (ESC y)

The PAGE ERASE key replaces all unprotected characters from cursor to end of display with unprotected spaces. Used in combination with SHIFT, this key erases all unprotected characters from cursor to end of page, replacing them with NUL codes. The cursor does not move unless protect mode and write protect status is on, in which case it will move to the first unprotected position at or after HOME. The display protect mode, if set, will be cleared by this operation.

Cursor Addressing

The computer can position T-5105 cursor to any position by a four (4) character sequence:

ESC = Y X

where Y and X represent the row and column coordinates of the cursor

desired. The HOME position (top row, leftmost column) is addressed by ESC = SPACE SPACE, and successive positions (down for Y or to the right for X) use codes ascending in the ASCII character set as in Table 3-5.

TABLE 3-5. ABSOLUTE CURSOR POSITIONING

X or Y	ASCII Code	X	ASCII Code	X	ASCII Code
1	SPACE	28	;	55	V
2	!	29	<	56	W
3	"	30	=	57	X
4	#	31	>	58	Y
5	$	32	?	59	Z
6	%	33	@	60	[
7	&	34	A	61	\
8	'	35	B	62	]
9	(	36	C	63	^
10	)	37	D	64	_
11	*	38	E	65	`
12	+	39	F	66	a
13	'	40	G	67	b
14	-	41	H	68	c
15	.	42	I	69	d
16	/	43	J	70	e
17	0	44	K	71	f
18	1	45	L	72	g
19	2	46	M	73	h
20	3	47	N	74	i
21	4	48	O	75	j
22	5	49	P	76	k
23	6	50	Q	77	l
24	7	51	R	78	m
25	8	52	S	79	n
26	9	53	T	80	o
27	:	54	U		

After the 'X' coordinate is loaded, the position of the cursor is tested for protected status. If that position is protected, the cursor automatically skips to the first unprotected location in the forward direction.

Cursor Reading ESC ?

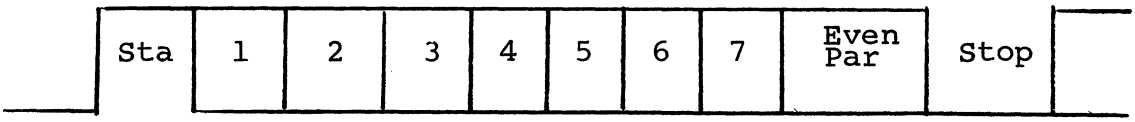
An ESC ? sequence causes the transmission of cursor position as YX

followed by CR code from the T-5105 to the data interface. This sequence cannot be initiated from the keyboard.

DATA INTERFACE

The MMDC transmits data to the computer or data set in accordance with EIA STandard RS-232-C.

The standard code for MMDC transmission is asynchronous serial ASCII ten bit code with even parity bit in the following format.



Other code formats are available as options for asynchronous serial data transmission. Please refer to Appendix A.6, Word Structure Options, in this manual.

In addition to the EIA RS232-C voltage level interface, a 20 ma. current loop interface is available for the transmit and receive data.

DATA TRANSMISSION

Two general data transmission modes, conversational and block are standard with the T-5105 interactive display terminal. Switching from block to conversational, or vice versa, is accomplished by using the CONV MODE pushbutton key, which is illuminated when conversational mode of transmission is selected, and unlit when the is in block transmission mode. Dynamic computer control of transmission mode provided with use of ESC B (Block Mode) and ESC C (Conversation Mode) sequences.

Data transmission rate is switch selectable with a thumb wheel switch on the Logic board of the T-5105. Baud rates and switch settings are as follows:

BAUD RATE	SWITCH SETTING
110	7
150	6
300	5
600	4
1200	3
2400	2
4800	1
9600	0

When the baud rate selector switch is set for 110 baud (pos. 7), a two (2) unit top code is transmitted.

A slide switch for selecting Half-duplex or Full-duplex is mounted on the Logic board.

Conversation Mode (Half Duplex)

Keyboard actuation of displayable character or control keys causes display of graphics or control action with transmission of code. Editing keys and command keys cause those operations to take place locally without transmission of code for that edit operation or command. Special function key (F1 through F16) code sequences are transmitted immediately with no terminal action until special function is deciphered by the computer.

Conversation Mode (Full Duplex)

In full duplex operation, graphic and control keys cause respective codes to be transmitted with the display enabled to receive echoed data from the computer.

Editing and command keys perform the indicated action with no transmission. Special function key actuation causes immediate transmission of its three (3) code sequence.

The T-5105 operates in a "roll" mode if the terminal display is not in protect mode. If a line advance code is keyed or received while the cursor is residing in the bottom line of the display, the entire display image moves upward one line. The bottom line is automatically filled with NUL codes, and the top line of information is lost.

Block Transmission

In block mode, operation of character keys, normal control keys, and editing keys perform local display and command functions without transmitting codes to the data interface. Data is transmitted to the computer in blocks or batches using any of several transmission control keys.

TABLE 3-6. BLOCK TRANSMISSION CONTROL

Transmission Block	Keys	Computer ESC Sequence
Special Function Command	F1 through F16	(none)
Defined Message (Foreground)	Send Message	ESC S
Defined Message (All)	Shift/Send Message	ESC s
Line (Foreground)	Send Line	ESC 4
Line (All)	Shift/Send Line	ESC 6
Page (Foreground)	Send Page	ESC 5
Page (All)	Shift/Send Page	ESC 7
Cursor Coordinates*	(See Note)	ESC ?
* Not Available to Operator,	Must be Requested by Computer	

Send Defined Message

The SEND MESSAGE key (ESC S) causes the cursor to back space until and ASCII STX code (generated by SHIFT-SOM-EOM key) is detected. Transmission then takes place until an ETX character is detected or until the end of the display is reached. As protected fields are encountered during transmission, an ASCII FS code is sent and cursor jumps to next unprotected character position. STX character displays as ▶ , EXT as ◀ symbol.

Using SEND MESSAGE with SHIFT (or equivalently, ESC s) will cause the cursor to back space until STX code detected, then transmit all the following characters as defined message until an ETX character is found.

Send Line

The SEND LINE key (ESC 4) moves cursor to first character position of line in which it resides, after recording actual cursor actual position. All foreground codes except NUL, are transmitted sequentially as the cursor moves forward to its original position.

As protected fields are encountered an ASCII FS code is transmitted. When the cursor returns to its original position, an ASCII CR is transmitted to signal end of LINE SEND. (See ADM-1 Emulation Mode below).

SEND LINE with SHIFT (or ESC 6) performs as above with two exceptions, (1) all codes except NUL codes are transmitted and (2) when protected fields are encountered, they are bracketed by ESC) and ESC(code sequences as they are transmitted.

Send Page

Actuation of the SEND PAGE key (ESC 5) positions the cursor to HOME. The cursor then moves forward, returning to its original position, while the T-5101 successively transmits unprotected non-NUL codes, with an ASCII FS code transmitted for each protected field, and an ASCII US code for each new line. When the cursor is at its original position, an ASCII CR is transmitted.

SPECIAL FUNCTION KEYS

Sixteen special functions keys are furnished as standard with the MMDC interactive display terminal. These keys enable the T-5101 operator to give concise three code responses to frequently recurring inquiries, and/or to direct the computer to access special programs or subroutines. Special function keys are identified as F1 through F16 from left to right at the keyboard top. (Table 3-7).

STATUS DISPLAYS

The T-5101 is equipped with eight status indicators which are displayed on the right hand side of the screen. A black on silver identification tape is available for taping on the display screen or the display housing to identify the indicators. NSL part number 1577 references the tape.

Status indicators are assigned as follows and are set and cleared with specific keys of ESC sequences from the computer and/or keyboard. (Table 3-8).

ADM-1 Emulation Mode

The T-5101 can be set to emulate an ADM-1 by using an ESC% sequence. If the T-5101, is emulating an ADM-1 with serial printer, unformated print must be requested by ESC p rather than ESC L. This mode is cleared by ESC $.

TABLE 3-7. SPECIAL FUNCTIONS

Special Function Key	Code Transmitted	
	Single Key	With Shift
F1	SOH @ CR	SOH \ CR
F2	SOH A CR	SOH a CR
F3	SOH B CR	SOH b CR
F4	SOH C CR	SOH c CR
F5	SOH D CR	SOH d CR
F6	SOH E CR	SOH e CR
F7	SOH F CR	SOH f CR
F8	SOH G CR	SOH g CR
F9	SOH H CR	SOH h CR
F10	SOH I CR	SOH i CR
F11	SOH J CR	SOH j CR
F12	SOH K CR	SOH k CR
F13	SOH L CR	SOH l CR
F14	SOH M CR	SOH m CR
F15	SOH N CR	SOH n CR
F16	SOH O CR	SOH o CR

TABLE 3-8. STATUS DISPLAYS

Status Indicator	Condition	Key	Set Status	Clear Status
1	Keyboard Lock		ESC #	ESC "
2	ADM-1 Mode		ESC %	ESC $
3	Unassigned		ESC c	ESC b
4	Unassigned		ESC e	ESC d
5	Unassigned		ESC g	ESC f
6	Message Waiting		ESC <	ESC >
7	Program Mode	Prog Mode	ESC U	ESC X
8	Page Edit Mode	Page Edit	ESC N	ESC O

SECTION IV

MONITOR DESCRIPTION

The TV monitor is a solid-state unit integral to the T-5105.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized. The synchronization circuits have been custom designed to accept vertical and horizontal drive signals thus enabling the interfacing of this monitor with industrial or simple sync sources. This feature simplifies the user's sync processing and mixing and allows the unit to operate without requiring composite sync. The electronic packaging has been miniatured to compatability with small volume requirements.

MONITOR ELECTRICAL SPECIFICATIONS

TABLE 4-1. INPUT DATA SPECIFICATIONS

	Video	Vertical Drive Signal	Horizontal Drive Signal
Pulse Rate or Width	Pulse Width: 100 nsec or greater	Pulse Rate: 47 to 63 pulses/ sec	Pulse Rate: 15,000 to 16,500 pulses /sec
Amplitude	Low= Zero $^{+0.4}_{-0.0}$ volts High=4 ± 1.5 volts		
Signal Rise and Fall Times (10% to 90% amplitude)	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec
Input Signal Format	See Figure 4-1		

DATA DISPLAY SPECIFICATIONS

Input Impedance

	Minimum Shunt Resistance	Maximum Shunt Capacitance
(a) Video Input:	3.3 k ohms	40 pF.
(b) Vertical Drive Input:	3.3 k ohms	40 pF.
(c) Horizontal Drive Input:	470 ohms	40 pF.

Video Amplifier

(a) Bandwidth:	12 MHz (-3 dB)
(b) Rise and Fall Times (10% to 90% amplitude):	Less than 35 nsec (linear mode)
(c) Storage Time:	15 nsec, maximum (linear mode)

Retrace and Delay Times

(a) Vertical:	900 μsec retrace, maximum
(b) Horizontal:	7 μsec retrace plus 4 μsec delay, maximum

TABLE 4-2. CATHODE RAY TUBE DISPLAY SPECIFICATIONS

Nominal Diagonal Measurement (inches)	Phosphor	*Resolution (TV Lines)	
		Center	Corner
12	P4	900 at 40 fL	800 at 40 fL

* Resolution is measured in accordance with EIA RS-375 except Burst Modulation (or Depth of Modulation) is adjusted for 100 percent.

Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within 1.5% of the rectangle height.

ENVIRONMENTAL SPECIFICATIONS

Temperature (Chassis or Custom Unit)

Operating Range:	5°C to 55°C Ambient
Storage Range:	-40°C to°65 C

Humidity

5 to 80 percent (Noncondensing)

Altitude

Operating Range:	Up to 10,000 feet

HUMAN FACTORS SPECIFICATIONS

X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78

CONTROLS

(1) Contrast, 500 ohm potentiometer carbon composition $\geq$ 1/8 Watt

(2) Brightness, 100 kilohm potentiometer $\geq$ 1/8 Watt

Optional: The Brightness Control can be mounted on the printed circuit board as an internal set up control.

Internal Set Up Controls

(1) Height

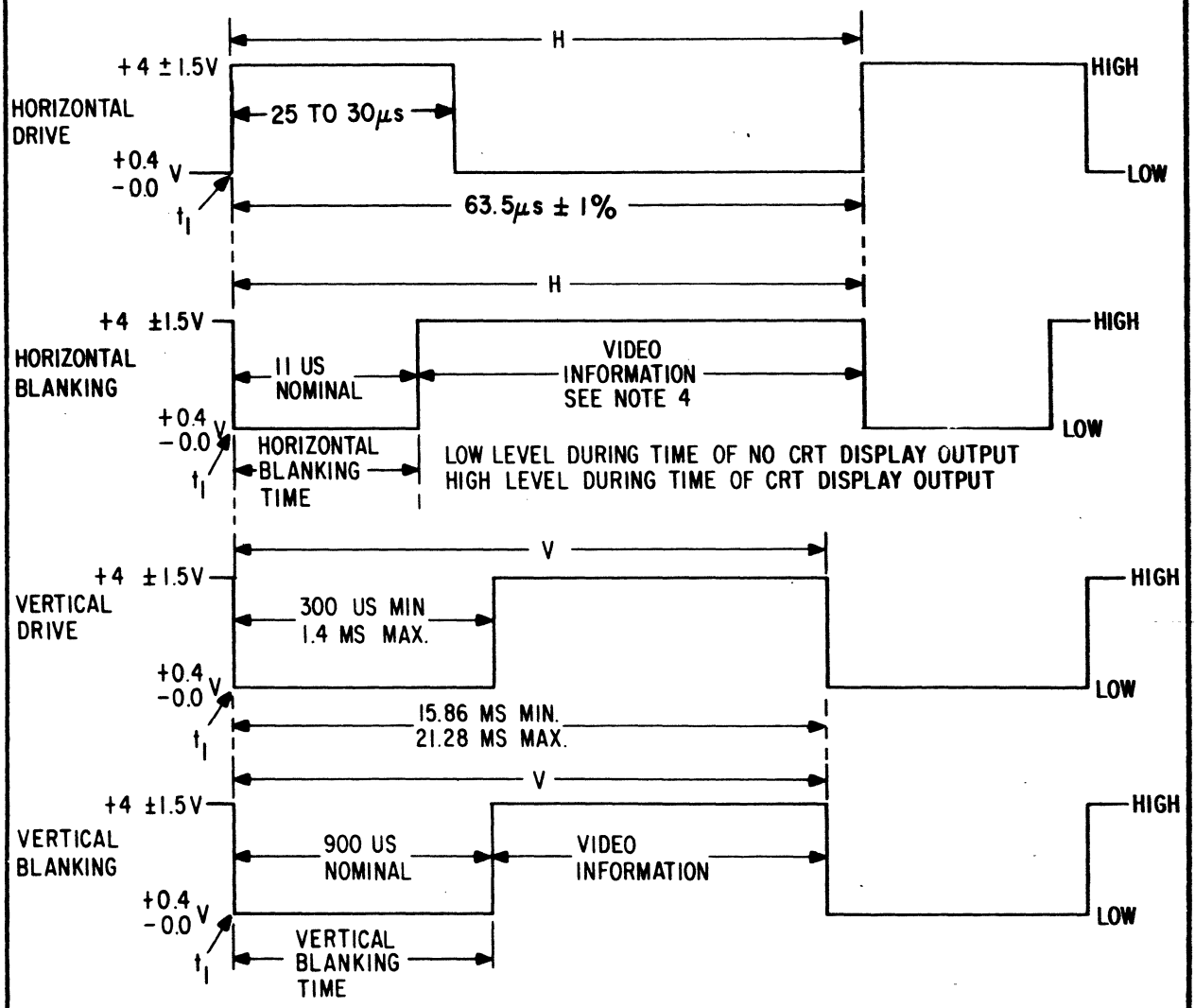
(2) Vertical Linearity

(3) Vertical Hold

(4) Focus

(5) Width

(6) Low Voltage Adjust



NOTES

1. The leading edges of Drive and Blanking waveforms must start at time t_1. Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

Figure 4-1. Synchronization and Blanking Generator Waveforms

THEORY OF OPERATION

Video Amplifier

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17. Q104, operating as a class B amplifier, remains cutoff until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

Vertical Deflection

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable resistor R116 and Capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gate "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward biased. This feature "programs" the

firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional unijunction transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104 and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102 is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola.

This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relatively high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the current through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

Horizontal Deflection

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (Section 1.2) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by C110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of the transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 kV (9 and 12 inches) or 9 kV (5 inches), "C" VDC and "B" VDC respectively. 12 kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier, Q101.

Low Voltage Regulated Supply

All models use a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener voltage of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201 where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection of current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are often used for this purpose; however, in the majority of cases, these devices are not fast enough to protect transistors.

SECTION V

MAINTENANCE AND FAILURE ANALYSIS

CARE OF THE T-5101

Your T-5101 Terminal with its solid state and modular electronics is easier to care for than an electric typewriter. Just give it a light cleaning from time to time, and it will remain as attractive as it is functional.

Lightly dust the unit using a brush or soft damp lint-free cloth. Paper towels are fine. Conventional spray cleaners work great for stubborn smudges and fingerprints. Do not use petroleum-base cleaners such as lighter fluids. These could harm the plastic or painted surfaces. Avoid wiping dust or lint into the keyboard area. If using spray cleaner, prevent excessive spraying which could run down between the keys.

EXTERNAL ADJUSTMENTS

External controls on the rear of the T-5101 include the following which are illustrated in Figure 5-1.

On-Off Switch

This two position switch controls the A.C. power to the unit and certain power-up and power-down sequences. Setting the switch to the ON position resets the circuitry within the T-5101, positions the cursor to home and clears the display memory to unprotected space codes.

Brightness

The monitor will be used to display alphanumeric or other black and white information. Usual video polarity produces white characters on a black background.

The brightness control should be adjusted at a point where the white raster is just extinguished. The CRT will then be at its cut off point, and a maximum contrast ratio can be obtained when a video signal is applied.

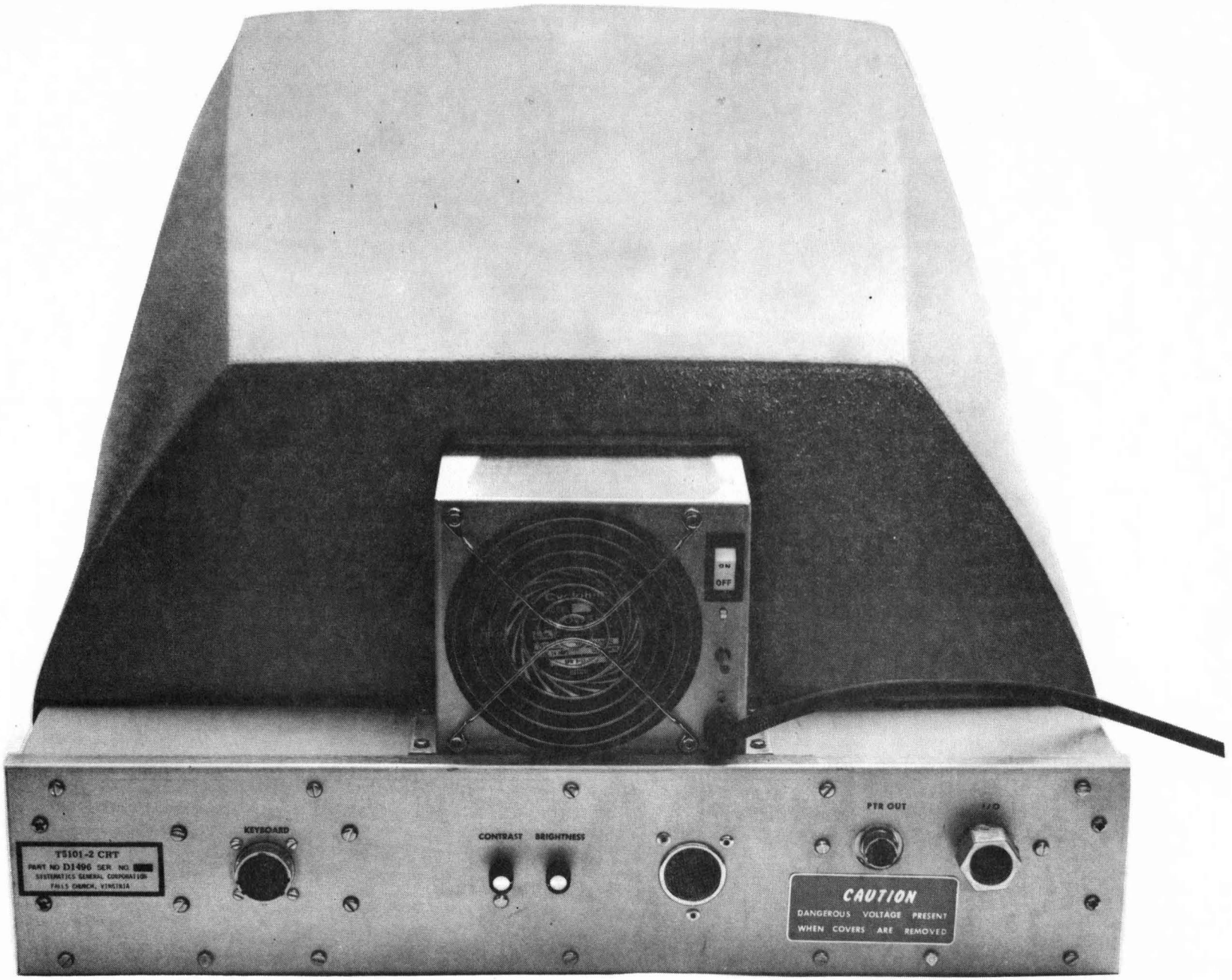


Figure 5-1. External Controls

Video Contrast

Q101 is designed to operate linearly when a +2.5 volt signal is applied to its base. The T-5101 incorporates an external contrast control to maintain this level. This control should be adjusted for a typical signal level of +2.5 volts peak-to-peak when measured at the video input terminal of the printed circuit board edge connector.

All other adjustments are internal to the T-5101 and require disassembly to the desired level.

DISASSEMBLY

1. Cover

   To detach gray and black molded cover, remove two screws on each side and one screw directly above fan on rear. Lift cover carefully to avoid damage to the screen.

2. Video Shield Cover

   To detach Video Shield Cover, remove 17 slotted screws designated by arrows in Figure 2-2.

3. Logic Assembly Adjustment Access

   Remove slotted screws designated by arrows in Figure 2-3. Grasp the cover and carefully slide the Logic Assembly out approximately 5 inches.

4. Logic Assembly Removal

   Refer to Figure 2-4.
   Slide out Logic Assembly as in Step 3 above. Unplug T-5101 Keyboard at KEYBOARD connector. Remove Data Interface Terminal Box cover and detach Interface cable, keylock wiring and SDU coax cables. Remove flexible conduit connections.

   Unplug: Logic Lower cable (P 1)
   Brightness Control cable (P 2)
   Contrast Control cable (P 3)
   Logic cables (P 4 and P 5)

   Carefully slide out Logic Assembly and remove.

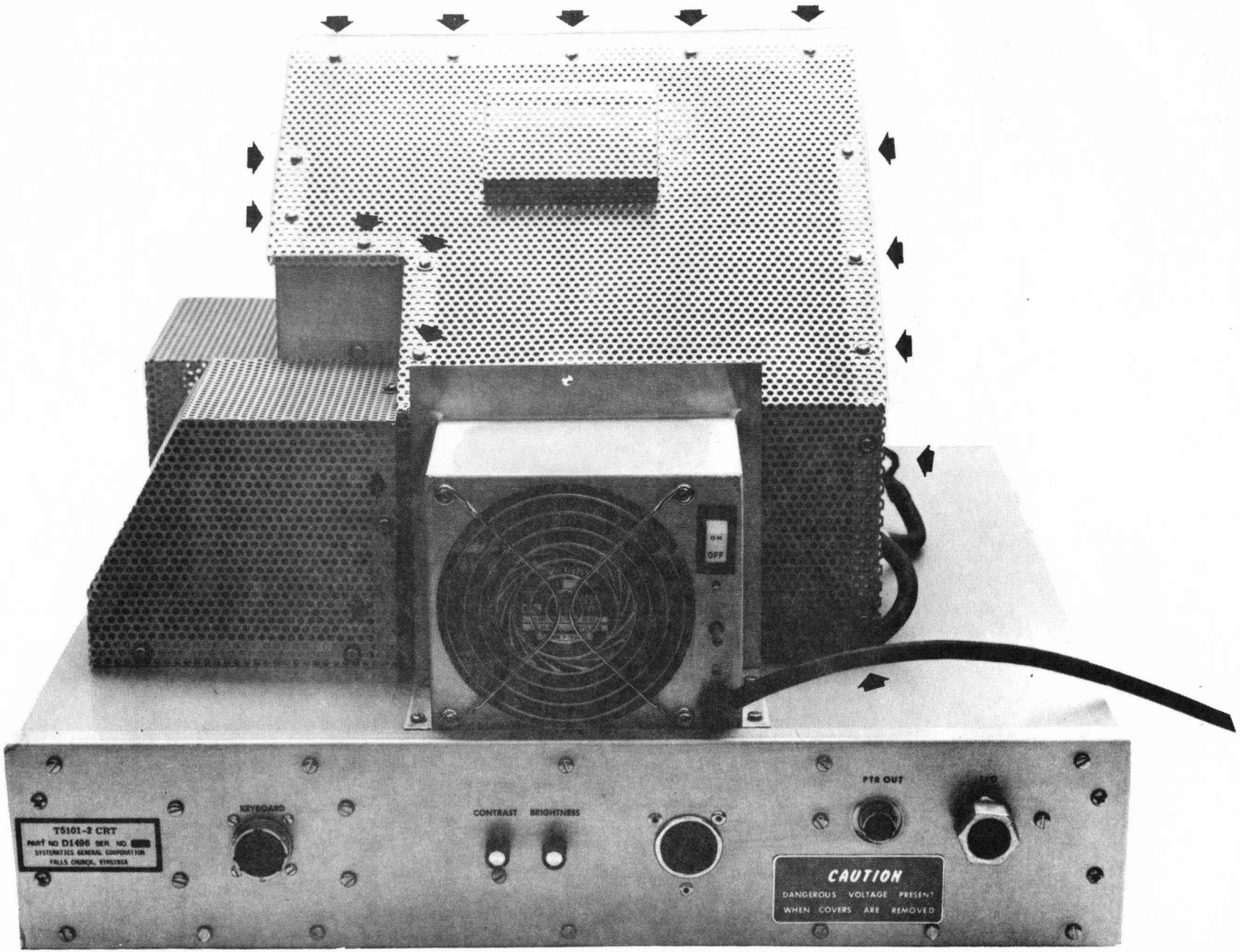


Figure 5-2. Video Shield Retaining Screws

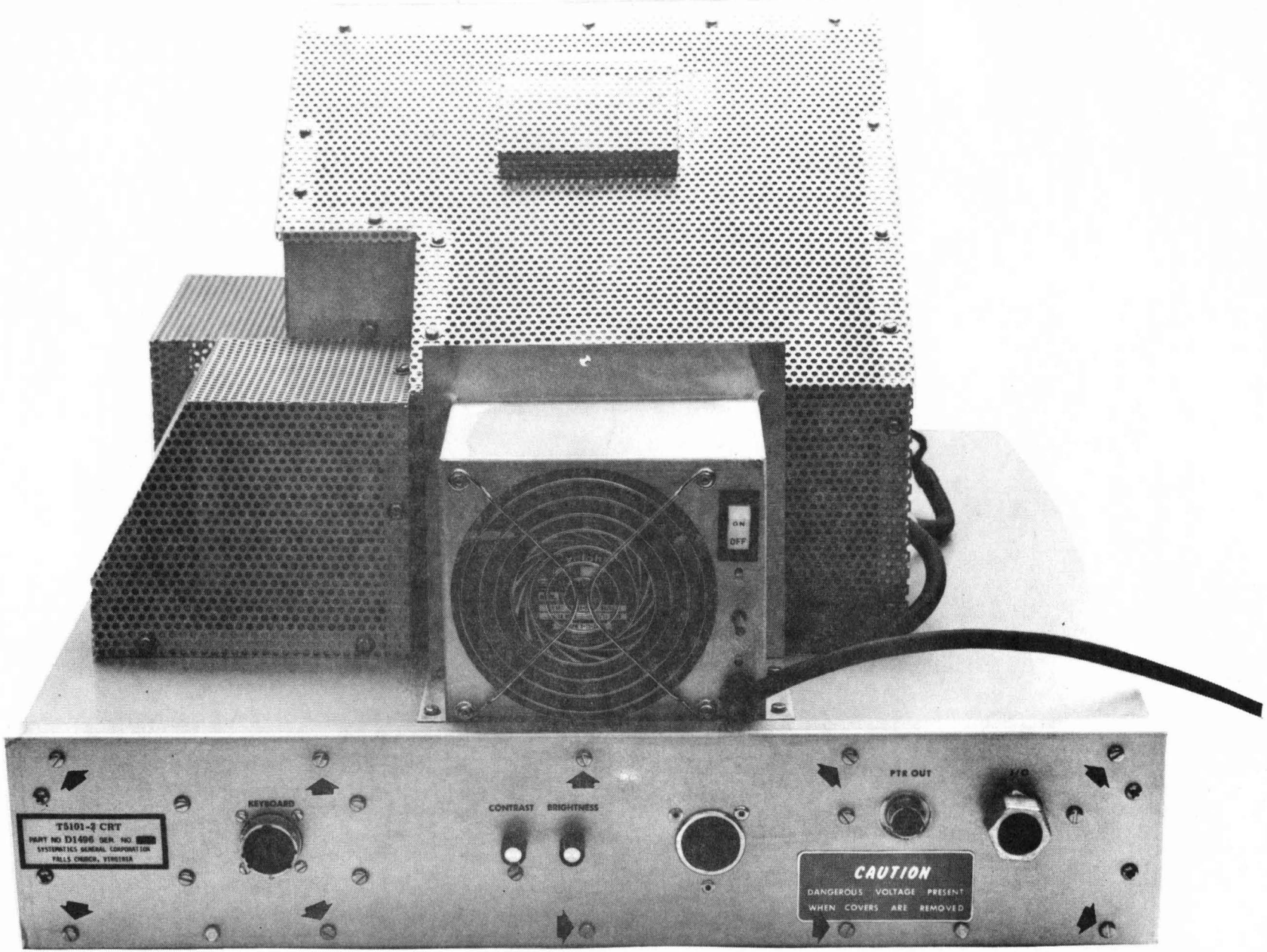


Figure 5-3. Rear Cover Retaining Screws

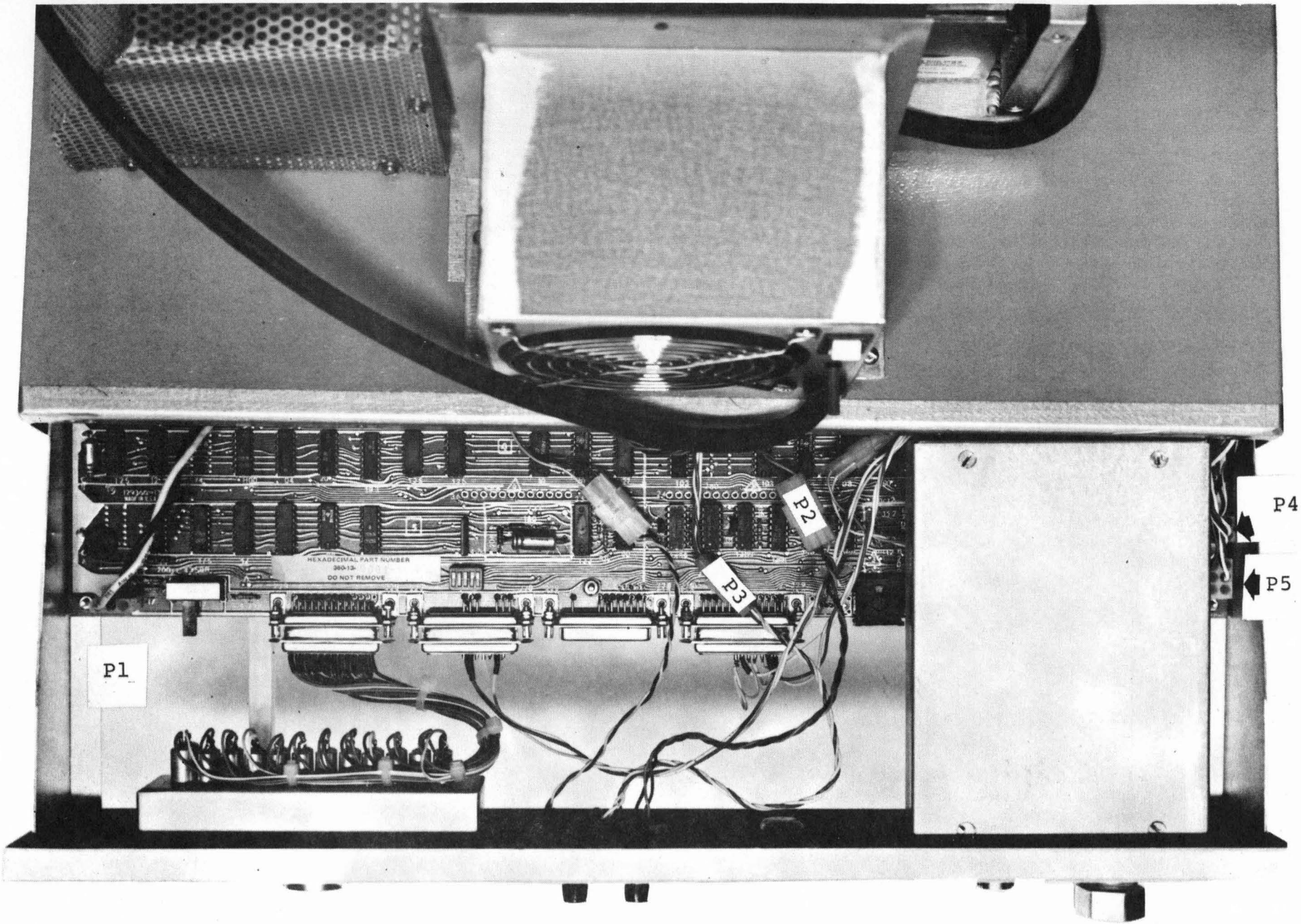


Figure 5-4. Logic Assembly Interconnections

5. Base plate

Invert the T-5101 and remove base plate retaining screws, base plate and shielding mesh. Store the mesh carefully to prevent damage.

6. Logic Power Supply

Remove Logic Power Supply Shields (Figure 5-5). Remove Logic Supply Mounting Screws (Figure 5-6). Unplug two (2) transformer cables. Loosen screw and remove transformer ground. Loosen screws and remove output cables. Remove power supply.

7. Transformer

Unsolder two (2) red wires at terminals 7 and 9. Unsolder black and white wires at terminals 1 and 2 respectively. Remove four (4) transformer retaining screws. Remove transformer.

8. Cathode Ray Tube

Support the Video Power Supply (Figure 5-7), invert chassis and remove the three (3) Power Supply Retaining Screws (Figure 5-8). Set chassis upright and unplug Power Supply cables. Remove Video Power Supply.

Unplug CRT socket and yoke cables (Figure 5-7). Support the CRT and remove four (4) CRT retaining screws on each side of Video Shield Figures 5-10, 5-11). Carefully lift the CRT up and out of Video Shield.

NOTE: Observe CRT handling precautions affixed to the CRT. Store carefully to prevent scratches or breakage.

9. Video Board

Refer to Figure 5-7. Remove Video Board edge card connector. Unplug Inductor cable. Remove four (4) corner screws and remove Video Board and spacers.

10. Composite Video Board

Remove mounting nut and washer from SDU BNC connectors in Interface Box and detach cables from box. Unsolder seven (7) wires connecting composite video board to logic board.

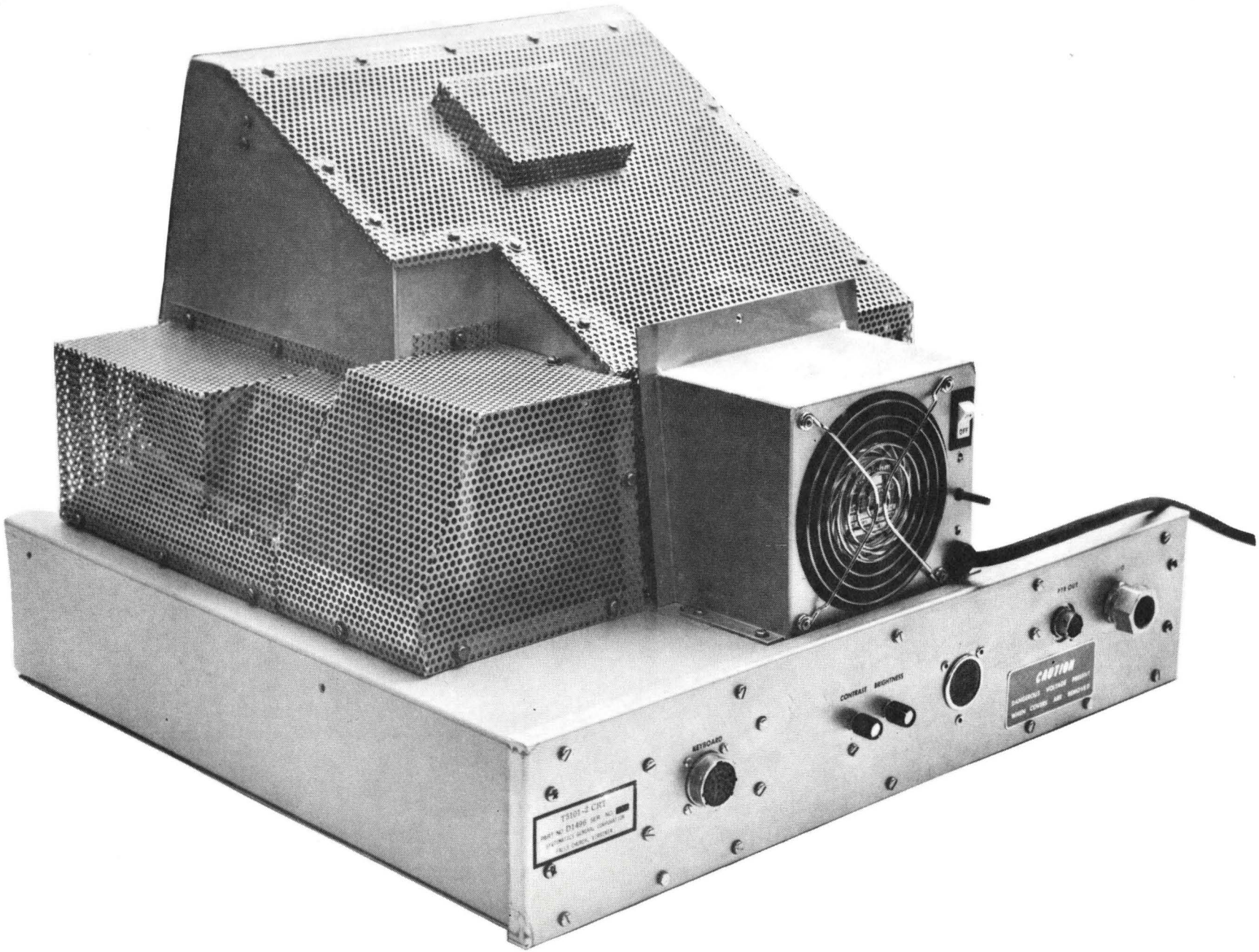


Figure 5-5. Logic Power Supply Shields

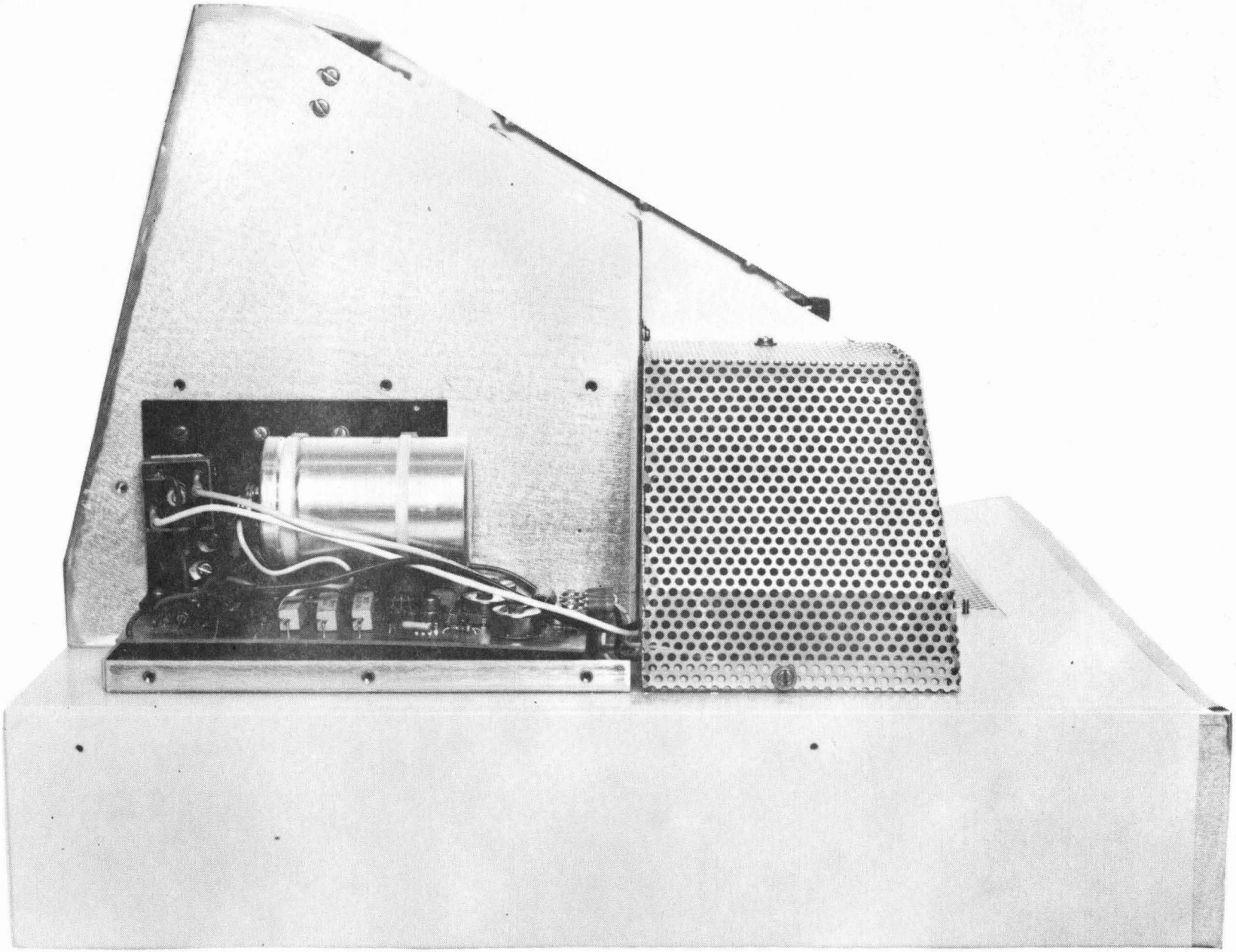


Figure 5-6. Logic Power Supply

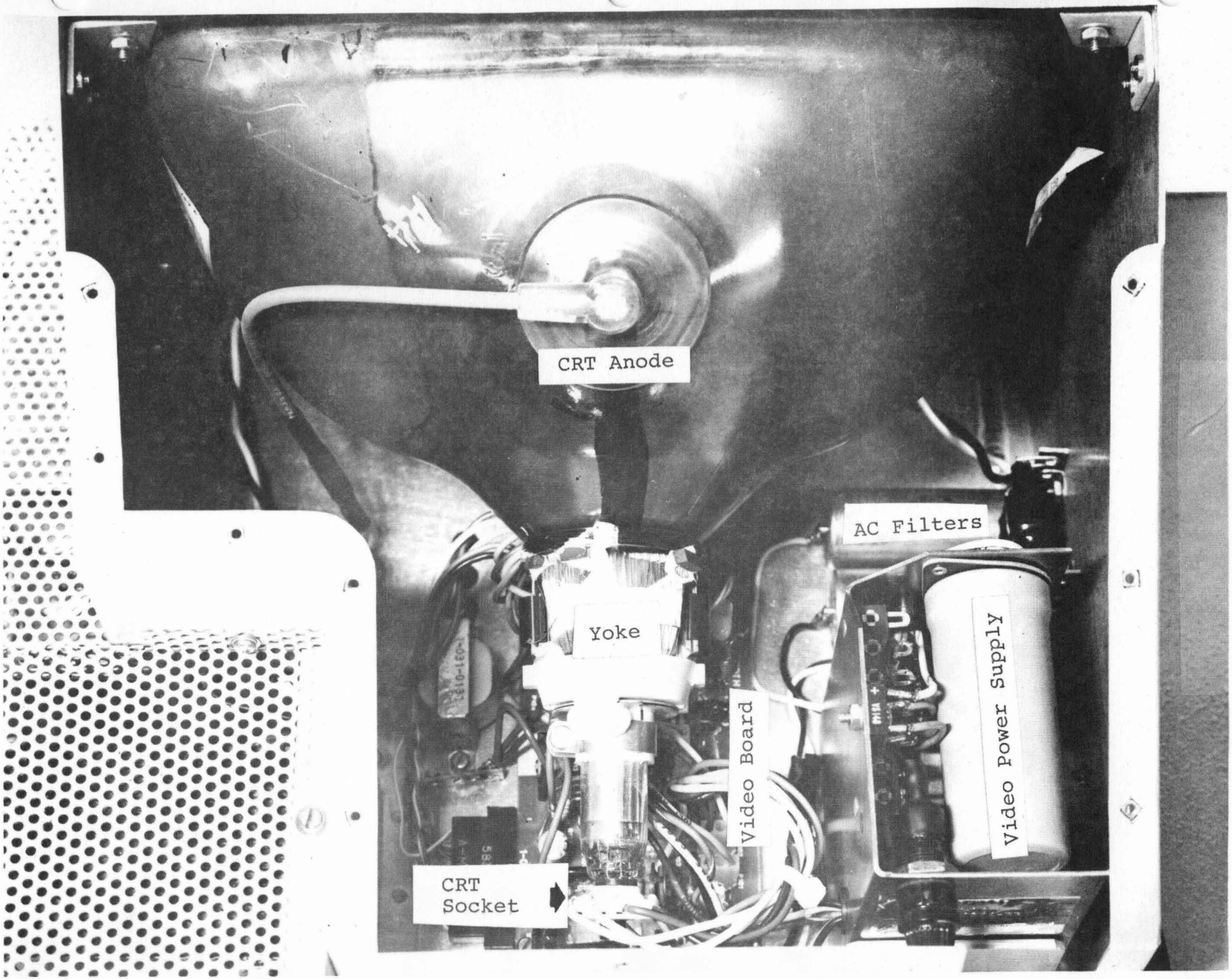


Figure 5-7. Video Enclosure

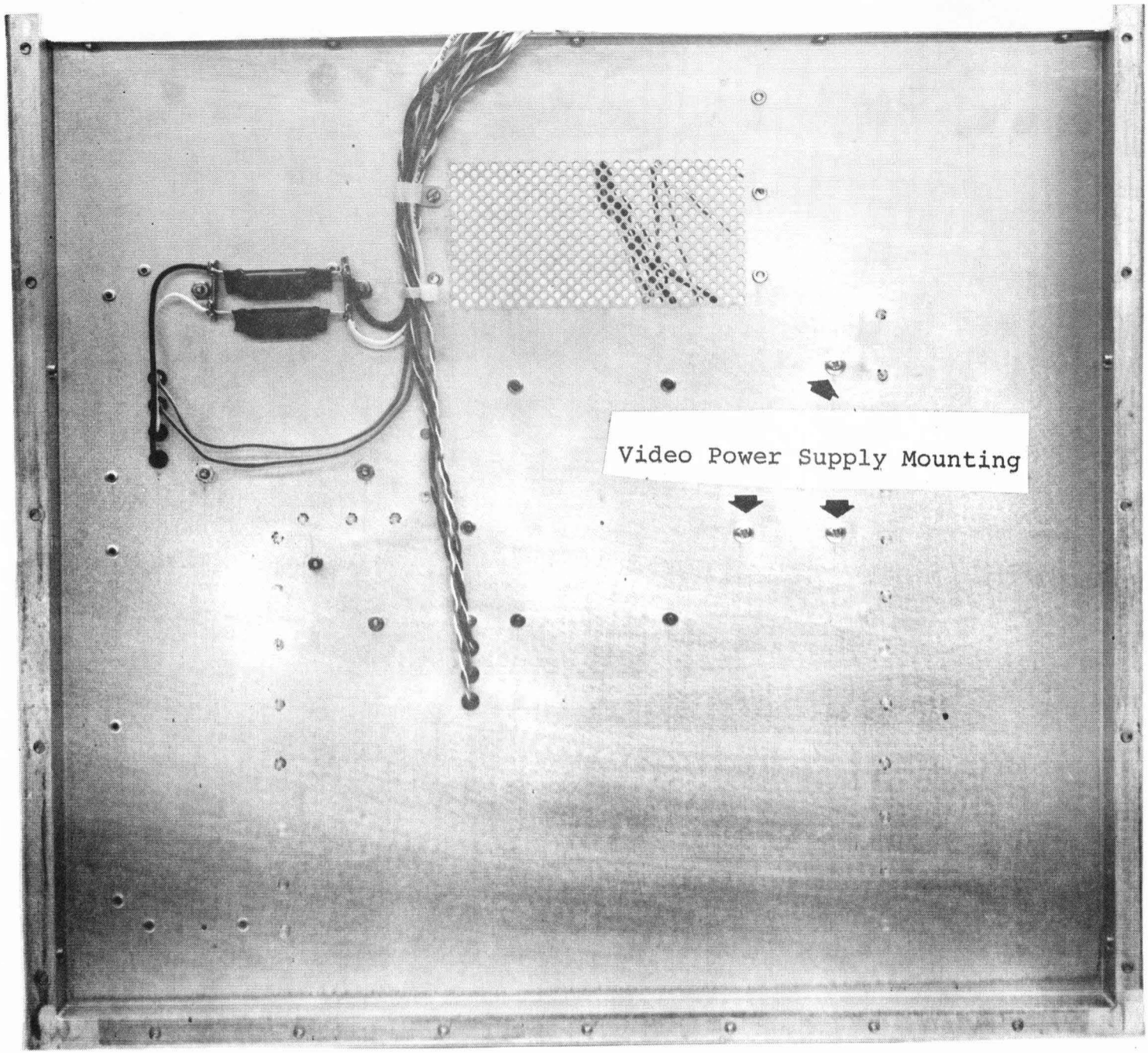


Figure 5-8. Chassis Cabling

Remove two (2) black nylon mounting nuts and detach composite video board and spacers.

11. Logic Board

Remove black nylon nuts and two (2) #4 hex nuts on front edge of board. Unplug Keyboard Interface connector and Data Interface connector and carefully lift logic board from base plate.

INTERNAL ADJUSTMENTS AND CONTROLS

The following adjustments and controls are accessible upon completion of Step 3 of the disassembly procedure. Refer to Figure 5-9.

Baud Rate Switch

The baud rate selector switch selects the desired baud rate. Table 5-1 gives the T-5101 switch settings for specific baud rates.

TABLE 5-1. BAUD RATE SELECTION

Baud Rate	Switch Setting	Baud Rate	Switch Setting
110	7	1200	3
150	6	2400	2
300	5	4800	1
600	4	9600	0

Mode Selector Switch

This thru position switch selects the duplex mode of operation in conversational mode. The F and H position select the full duplex and half duplex conversational mode respectively.

The following adjustments and controls are accessible upon completion of Step 1 and 2 of the disassembly procedure. Refer to Figure 5-11.

Vertical Adjustments

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

(1) Apply video and synchronization signals to the monitor.

(2) Set the vertical frequency control, R116, near the mechanical center of its rotation.

(3) Adjust the vertical height control, R124, for desired height.

(4) Adjust the vertical linearity control, R121, for best vertical linearity.

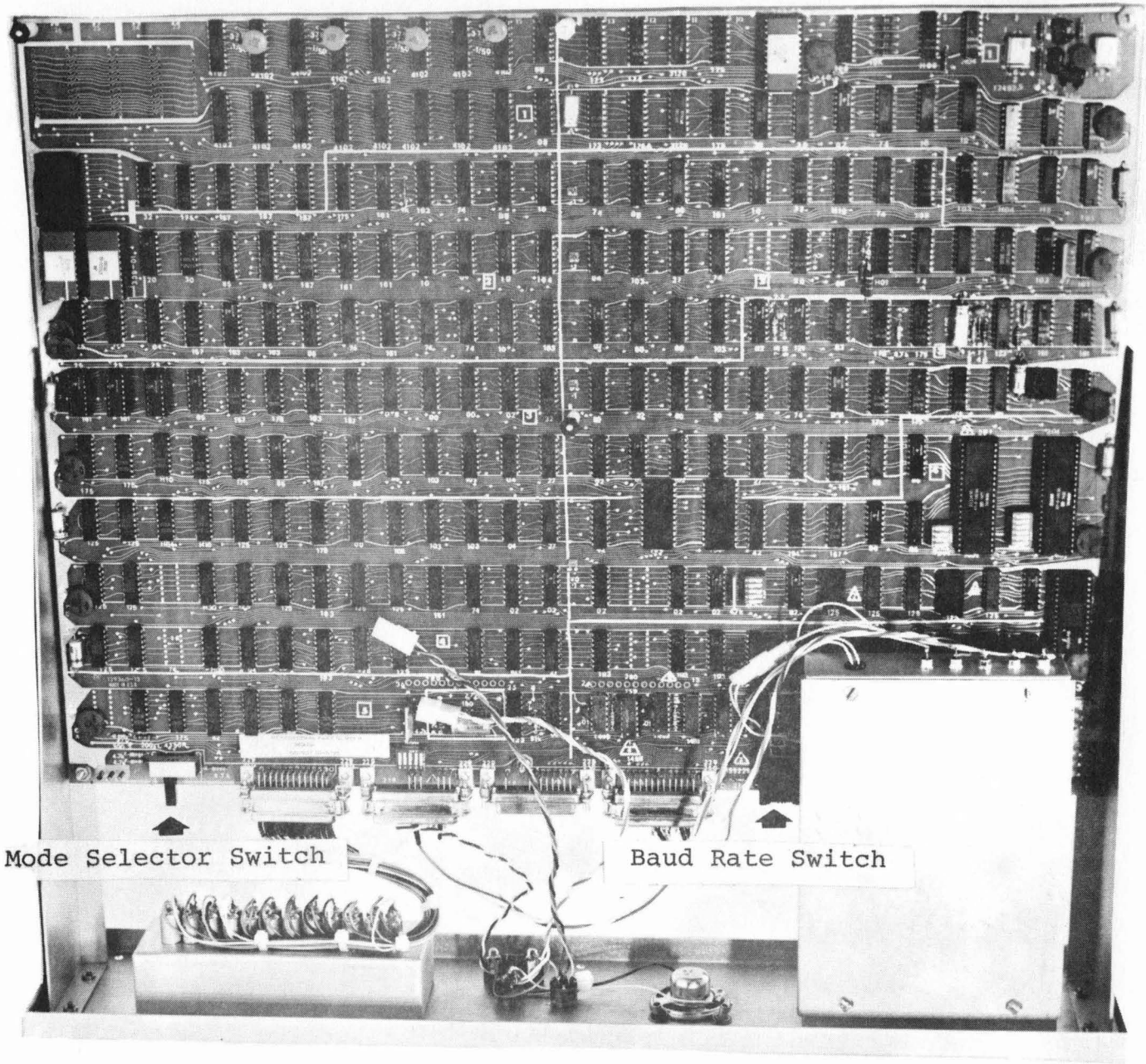


Figure 5-9. Internal Controls

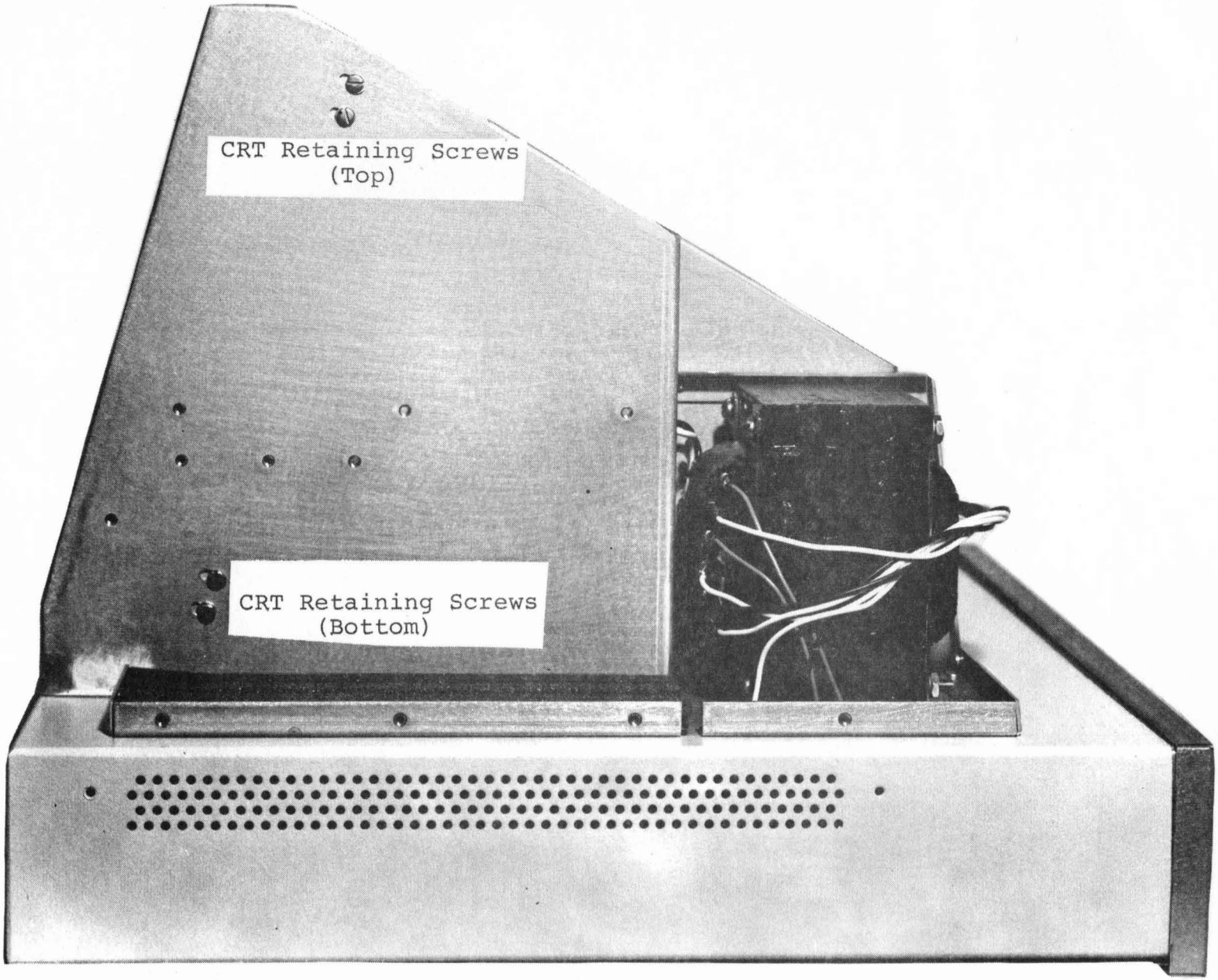


Figure 5-10. CRT Mounting (Right Side)

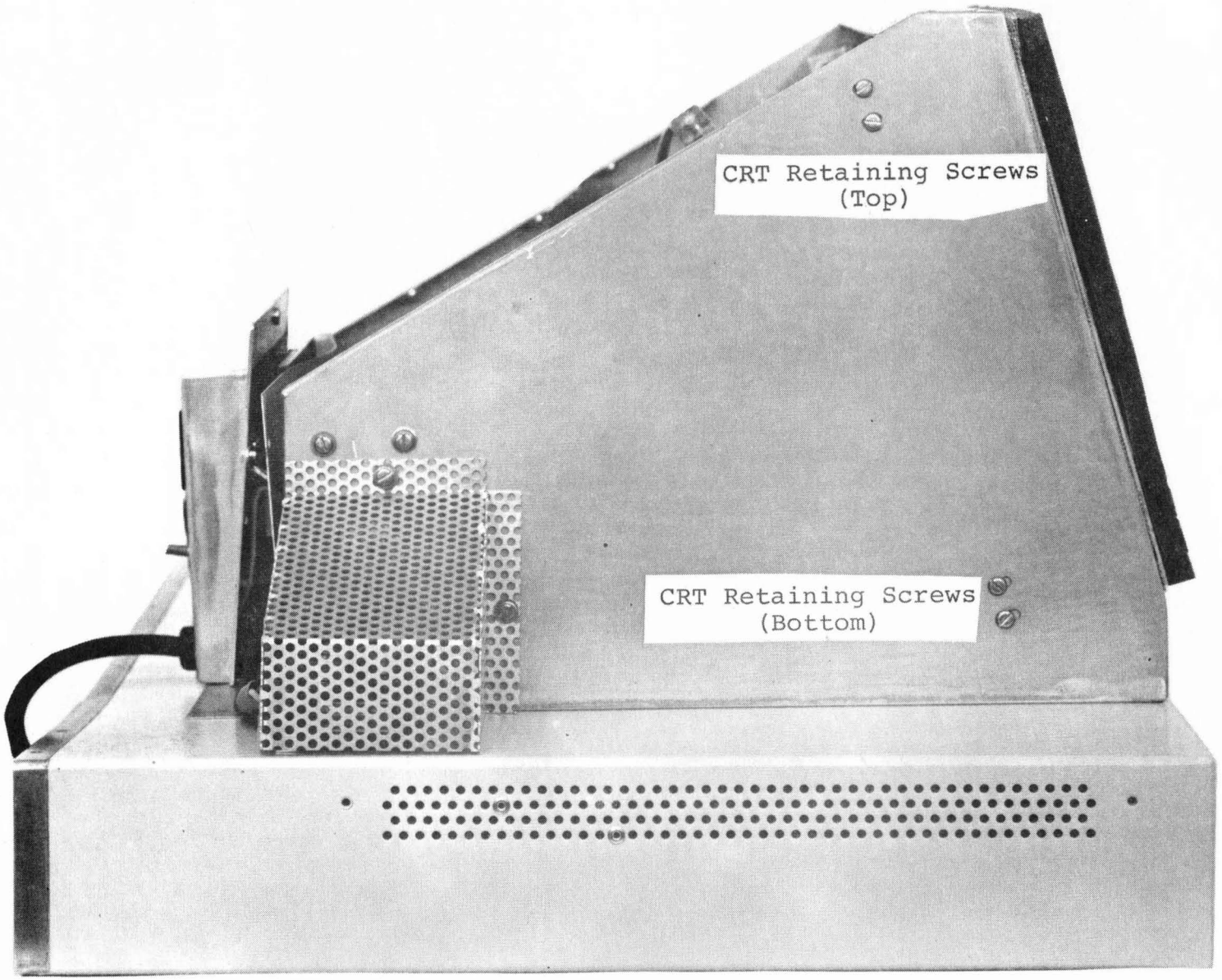


Figure 5-11. CRT Mounting (Left Side)

(5) Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

(6) Readjust the vertical frequency control, R116, until the picture rolls up slowly.

(7) Restore vertical drive to the monitor.

(8) Recheck height and linearity.

Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

(1) Apply video and synchronization signals to the monitor. Insert the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.) If the linearity sleeve is inserted farther than necessary, excessive power will be consumed, and the horizontal output circuitry could be overstressed.

(2) Adjust the horizontal width coil, L101, for the desired width.

(3) Insert the linearity sleeve farther under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

(4) Readjust L101 for proper width.

(5) Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor. The raster should be properly locked and centered when the horizontal drive signals as described above are used.

Focus Adjustment

The focus control, R107, provides an adjustment for maintaining best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large effect on focus.

Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

The ring magnets should not be used to offset the raster from its nominal center position because it would degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

PHILOSOPHY OF FAILURE ANALYSIS

Effective trouble shooting is accomplished in a minimum of time by following a series of logical steps. The ultimate aim is to effectively pinpoint the actual problems using all the information available.

Locating the malfunction is then the first logical step. The following is a suggested plan for effective casualty analysis.

(1) Investigate - record the state of the machine when the error occurred. Look for obvious symptoms including operator error, loose plugs or connectors, data set error, blown fuses or computer error.

(2) Isolation - Modular replacement is the quickest method of isolation where the replacement is available. Isolation to one of the following: circuit board, keyboard module, video monitor, power supply or inter-connecting wires should be the first step in isolation.

(3) Component Isolation - Isolation to a smaller component may be accomplished in some cases with the use of oscilloscope and multimeter.

(4) Replace the faulty module or component and retest by running the same operation in the same state the error occurred.

(5) Record for future reference the symptoms, cause and module or component isolation method used.

Failure Isolation

This section will explain briefly the approach to failure isolation and then describe a simple checkout procedure upon power turn-on.

The display terminal consists of a monitor assembly, power supply, logic board and keyboard. All assemblies are replaceable by simply disconnecting cables and removing attaching screws. To remove the cover for inspection or assembly replacement, remove the five screws on the side and back of the terminal.

The following will give you some helpful things to look and listen for which might indicate the problem area. Each assembly is described as to the function it performs along with a brief procedure to replace the assembly. At the end of this section is Table 5-2.

describing problems of symptoms and the most likely assembly to be at fault.

(1) Ensure the T-5101 power cord is plugged into a grounded A.C. outlet of the proper voltage and frequency.

(2) Set the ON/OFF Switch on the rear of the T-5101 to the "ON" position.

(3) Check to see if the fan starts when power is turned on. If it does not, check the power switch and push red circuit reset button.

(4) At turn on, listen for an audible 1 to 2 KHz tone that lasts approximately one second (only in units with beeper). If no tone is heard, look for cursor as in (5) below.

(5) If the cursor does not appear after a normal warm-up period, type the HOME key. If this fails to produce the cursor, reset the display by pressing the RESET key. If still no cursor, it is possible the brightness and/or contrast controls are misadjusted. They are adjusted as follows:

   (a) Set the contrast control to the middle of its range.

   (b) Turn the brightness control clockwise until the screen is bright, then reduce brightness slowly until the background is barely visible. The cursor should be present.

   (c) Adjust brightness and contrast for desired presentation.

   (d) If the cursor does not appear, check the power supply voltage; replace the monitor if necessary.

(6) If the problem is associated with transmitting and receiving of data to and from the computer, use the following procedure: Place the full-half duplex switch in full position. Remove the cable from the Interface Terminal block and jumper pins 4 and 5 on the terminal connector together. Now, whatever is typed on the keyboard should appear on the screen. This test checks the transmission of characters from the keyboard and display of those characters in non-BLOCK mode. To test the function of character storage in memory, run the cursor to the bottom of display and test page roll functioning of displayed characters roll upward as

expected, memory storage of characters is functional.

TABLE 5-2. T-5101 FAILURE ANALYSIS GUIDE

Type of Failure	Probably Location of Failure			
	Logic Board	Keyboard	Power Supply	Monitor
Audio Signal	1	2		
Clear Memory	1	2		
Clear Memory (Power Up)	1			
Cursor Control	1	2		
EDIT Control Option	1	2		
Parity Error	1			
Receive Data*	1			
Transmit Data*	1	2		
Video:				
Character/No Cursor	1			
No Character/Cursor	1			
No Character/No Cursor	3		2	1
Data/No Sync	2			1
Data Wave			1	2
Randomly Generated,				
Wrong Characters**	1	2		

* Check word structure specification and baud rate.

** Insure good connection of cable from keyboard to logic board.

TROUBLESHOOTING THE DISPLAY ASSEMBLY

The display received video and sync signals from the control board and performs normal TV functions. The high voltage for the display is generated from its own self-contained power supply. In addition, the display assembly includes its own low voltage (15V D.C.) power supply.

CAUTION

DISCHARGE HIGH VOLTAGE BEFORE ATTEMPTING

TO REMOVE DISPLAY ASSEMBLY.

Display Troubleshooting Guide

1.	Screen is dark	Check "A" bus Q106, Q105,
2.	Loss of video	CR 105, Q101
3.	Power consumption is too high	Check horizontal drive wavefore; check proper placement of horizontal linearity sleeve; Q105, Q106
4.	Low voltage bus incorrect (for units with a low voltage supply)	Q202, Q203, Q1 (Note: Low voltage supply will indicate low or "0" volts due to its current limiting action if a short is evident in the "A" volt line.

The voltage waveforms are shown in Figure 5-12.

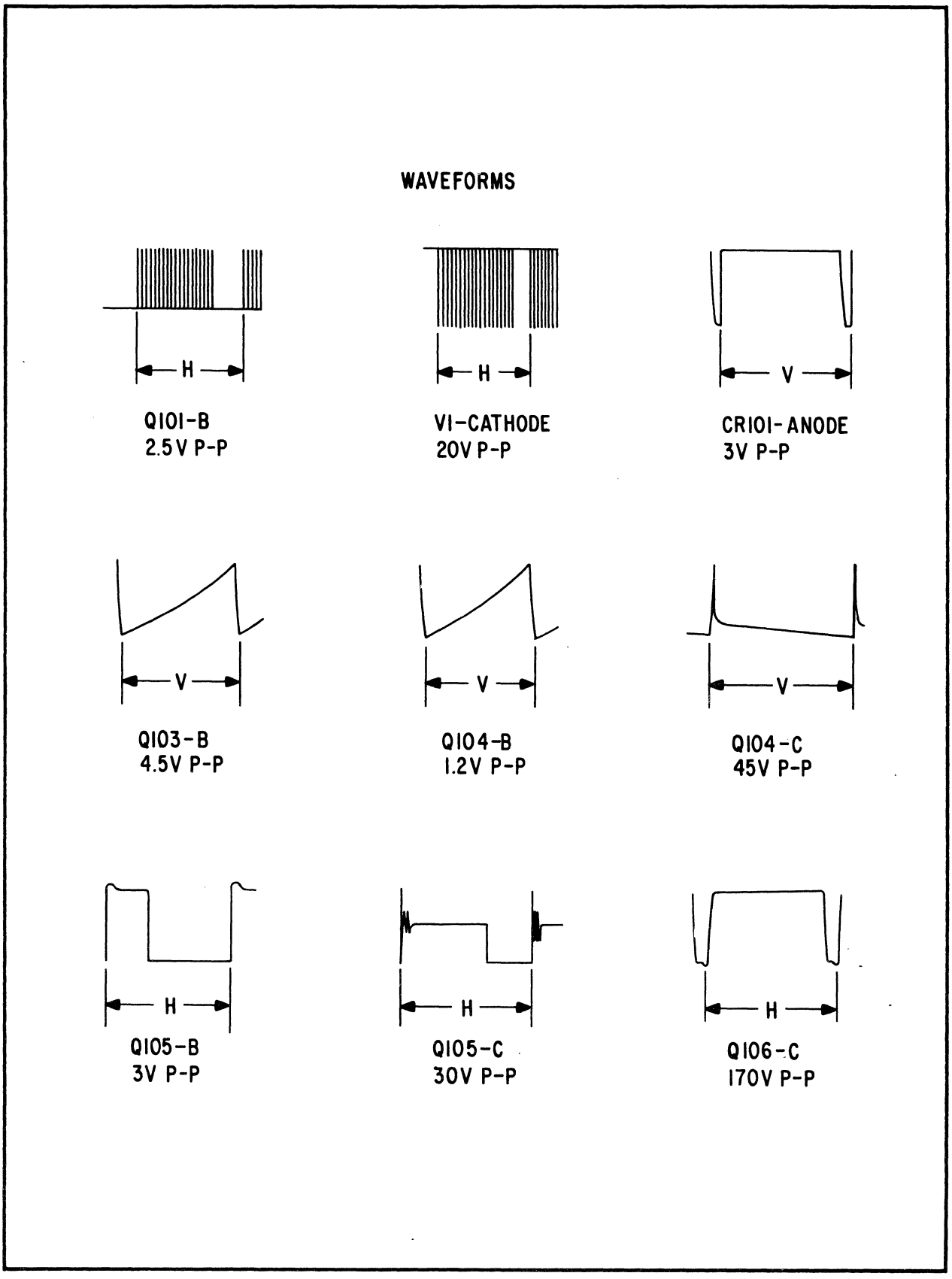


Figure 5-12 Voltage Waveforms for Display

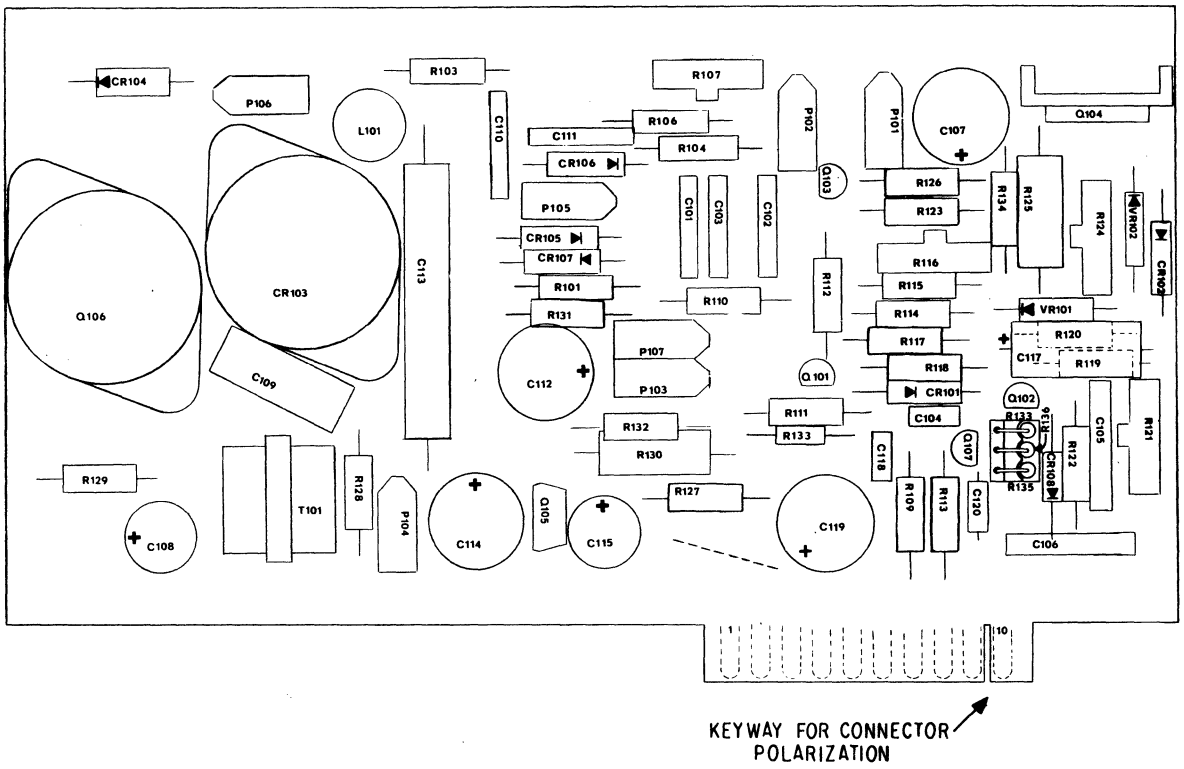


Figure 5-13. Video Circuit Board Components Location

MAINTENANCE OF MAIN LOGIC BOARD AND POWER SUPPLY

The main logic board is a self-contained functional unit with one exception: D.C. logic level +5 Volts is obtained from a separate POWERTEC power supply.

For maintenance and trouble shooting, refer to Table 5-3 for identification of connectors and terminals external to the main logic board and normal input-output signals.

Connector J1 is used for Data Signal interface connection to the main logic board. Connectors J2 and J3 are used for the same purpose

TABLE 5-3. MAIN LOGIC BOARD TERMINAL IDENTIFICATION CHART

Connector	Symbol	Pins	
RS232C Interface	J1	1-25	
RS232C Extension	J2		
		2	Transmit Data
		3	Receive Data
		4	Request to Send
		5	Clear to Send
		6	Data Set Ready
		8	Received Line Signal
		12	Secondary Received Line Signal
		19	Secondary Request to Send
Monitor I/O	J4	1	Brightness
		2	Brightness
		3	Brightness
		4	Contrast
		5	Chassis Ground
		6	Video and Vertical Ground
		7	Horizontal Ground
		8	Horizontal Drive
		9	Vertical Drive
Logic Board Power	J5	1	AC Feed 32 volts rms.
		2	AC Feed
		3	Equipment Ground
		4	Speaker
		5	Speaker
		6	D-C Feed (+5 volts)
Keyboard I/O	J6	1	CTRL
		2	RESET
		3	
		4	BIT 8
		5	BIT 6
		6	BIT 4
		7	BIT 2
		8	BIT 1
		9	BIT 3
		10	BIT 5
		11	BIT 7
		12	PAGE EDIT
		13	SHIFT

TABLE 5-3. MAIN LOGIC BOARD TERMINAL IDENTIFICATION CHART (Continued)

Connector	Symbol	Pins	
		15	STROBE L
		16	STROBE 0
		17	-20V POWER
		18	GROUND
		19	GROUND
		20	POWER +5 volts
		21	POWER
		22	PROTECT MODE
		23	CONVERSATIONAL MODE
		24	PROGRAM MODE

Bus Driver	129361 Sheet	TSB 1	2	3	4	5	6	7	8
RDR	14	L13-3	L13-4	L13-5	L13-6	M13-3	M13-4	M13-5	M13-6
KEY	19	C18-8	C18-6	C18-11	C18-3	B18-8	B18-6	B18-11	B18-3
RCV	20	C3-8	C3-6	C3-11	C3-3	B3-8	B3-6	B3-11	B3-3
LIT	13	D25-8	D25-6	D25-11	D25-3	D26-8	D26-6	D26-11	D26-3
CPC	15	C22-8	C22-6	C22-11	C22-3	D22-8	D22-6	D22-11	D22-3
CPR	15	C21-8	C21-6	C21-11	C21-3	D21-8	D21-6	D21-11	D21-3
LRC	15	C5-8	C5-6	C5-11	C5-3	B5-8	B5-6	B5-11	B5-3
ADD	17	C7-8	C7-6	C7-11	C7-3	B7-8	B7-6	B7-11	B7-3
MAR	10	C4-3	C4-4	C4-5	C4-6	B4-3	B4-4	B4-5	B4-6
IND	7	F6-8	F6-6	F6-11	F6-3	H6-8	H6-6	H6-11	H6-3
CNTR	18	C19-8	C19-6	C19-11	C19-3	B19-8	B19-6	B19-11	B19-3
CMA	9	B25-8	B25-6	B25-11	B25-3	B26-8	B26-6	B26-11	B26-3
OTSB	14	C2-9	C2-5	C2-12	C2-2	B2-9	B2-5	B2-12	B2-2
Bus Driven									
COND	17	A25-4	A25-3	A25-2	A25-1	A25-15	A25-14	A25-13	A25-12
WDR	14	K23-4	K24-5	K23-12	K23-13	K19-4	K19-5	K19-12	K19-13
ARTO	20	D1-26	D1-27	D1-28	D1-29	D1-30	D1-31	D1-32	D1-33
ART1	20	D3-26	D3-27	D3-28	D3-29	D3-30	D3-31	D3-32	D3-33
LRC	15	E5-9	E5-5	E5-12	E5-2	D5-9	D5-5	D5-12	D5-2
IND	7	E6-9	E6-5	E6-12	E6-2	D6-9	D6-5	D6-12	D6-2
CM	9	C25-9	C25-5	C25-12	C25-2	C26-9	C26-5	C26-12	C26-2

Table 5-4. Tri-State Bus Signal Locations

Bus Driven	129361 Sheet	TSB 1	2	3	4	5	6	7	8
	9	H25-9	H25-5	H25-2	H25-12	H26-9	H26-5	H26-2	H26-12
CNTR	18	C20-15	C20-1	C20-10	C20-9	B20-15	B20-1	B20-10	B20-9
COMPAR	18	F23-9	F23-11	F23-14	F23-1	E19-9	E19-11	E19-14	F18-10
MAR	10	C4-14	C4-13	C4-12	C4-11	B4-14	B4-13	B4-12	B4-11
MACC	12	H23-13	H23-10	H23-6	H23-3	F19-13	E18-9	F17-4	
MACR	12	H23-13	H23-10	H23-6	H23-3	F19-13			

Table 5-4. Tri-State Bus Signal Locations (Continued)

Connector J4 is used to supply output signals from the main logic board to the CRT monitor. If proper signals are present at terminals of connectors J5 and J6, examine the integrity of connector pins on P4. Examine for obvious faults on main logic board. It is strongly recommended that no involved repairs be attempted on this board. Instead, contact the factory or authorized service representative.

Connector J5 primarily handles power inputs to the main logic board. Therefore, the absence of proper inputs at terminals 1, 2, and 3 indicates failure in AC power feed. Likewise, lack of proper voltage at terminal 6 indicates problems with chassis mounted power supply or connector cable. Improper signals on terminals 4 and 5 indicate trouble with main logic board.

If noted signal levels are not present at terminals of connector J6 as keyboard is operated, examine keyboard assembly for obvious faults. Either repair or replace keyboard assembly.

Keyboard output levels are compatible with TTL circuits with logic "1" greater than +2.6V at .10 ma and logic "0" less than 0.4V. The outputs are bounce free so that only one signal will be generated for each key depression. Two-key rollover interlocking is provided for all encoded keys. If a key is depressed before a previous operated key is released, the second key code is transmitted after the first key is released. A strobe pulse is provided with each encoded key output.

Power Supply

D.C. Voltages of -5, +12 and -12 volts utilized within the main logic board are generated by regulator IC chips on that board. A separate +5 volt power supply for logic level voltage is mounted above the main circuit board on the chassis.

Recommended adjustment procedure for the separate power supply is as follows:

(1) Set current limit potentiometer for maximum current output (this is normal operating position).

CAUTION

DISCONNECT POWER SUPPLY OUTPUT LOAD BEFORE PROCEEDING THROUGH THE FOLLOWING STEPS.

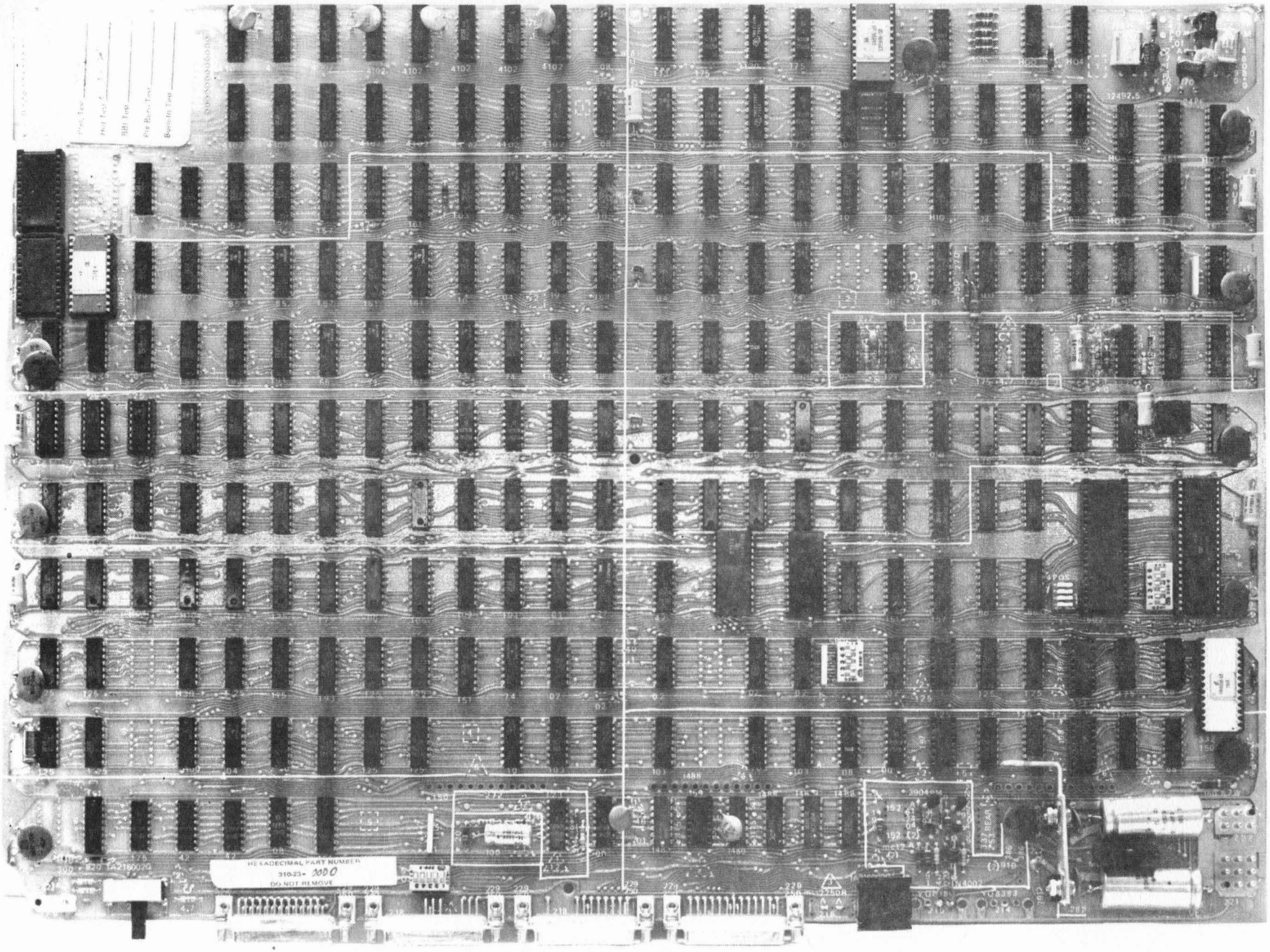


Figure 5-14. Main Logic Baord Layout

(2) Turn overvoltage protection potentiometer fully clockwise.

(3) Adjust output voltage to +6V DC (nominal).

(4) Adjust the overvoltage protection potentiometer counter clockwise to the point where output voltage is shut off.

(5) Turn output voltage fully counterclockwise, then slowly clockwise until the output voltage reaches +6V DC (nominal). The output should then fall to the overvoltage level, verifying correct overvoltage protection adjustment.

(6) Adjust the output voltage control to +5.2 volts D.C., which is the normal operating voltage.

Component Replacement

The replacement of a component on any printed circuit board requires care to prevent damage to circuit board etch. Clipping a component from the circuit board rather than unsoldering is the preferred method. Excessive heat from a soldering iron may result in damage to the component being replaced. The use of a soldering iron with a small copper alligator clip as a heat sink, and a delay between the soldering of individual pins of a chip are recommended.

In accordance with good maintenance practices, Lear Siegler does not recommend individual component replacement on any printed circuit board. Instead, it is recommended the factory be contacted relative to availability of special test equipment or factory rebuilt and tested replacement assemblies.

SECTION VI
SCHEDULED MAINTENANCE

Purpose. The purpose of the scheduled maintenance is to assure continued dependable operation of the T-5101 Control-Indicator, as the interactive display device functioning in an input/output capacity with the remote computer.

Scope. The scope of the scheduled maintenance is to test and adjust to validate the satisfactory operation of the T-5101 to meet its operational function.

Applicability. The scheduled maintenance instructions in this manual are cancelled when the Planned Maintenance System (PMS) is implemented for this equipment aboard your ship or station.

Scheduled Maintenance. The scheduled maintenance activity involves a weekly task and a monthly task. The weekly task requires external cleaning only. The monthly task requires a straight forward test and, if necessary, simple adjustment. In the event a malfunction does occur during testing, the regular trouble/failure sequence should be initiated.

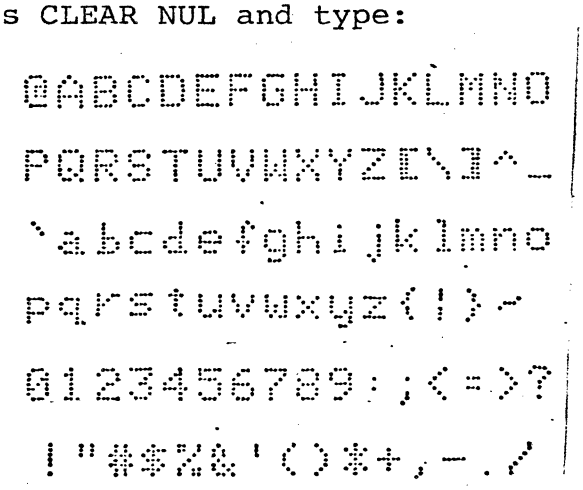
Weekly Maintenance. The T-5101 requires only light cleaning to maintain its normal finish. A light dusting using a soft brush or soft damp lin-free cloth/paper towel is acceptable.

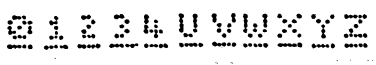
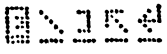
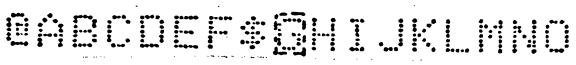
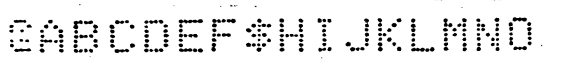
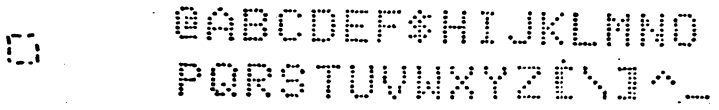
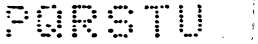
Conventional mild spray cleaners may be used for smudges and fingerprints. Harsh and petroleum based cleaners should not be used. Avoid excessive spraying or wiping dust or lint into the keyboard area.

Monthly Maintenance. The monthly maintenance activity will provide the operator with a well adjusted display and assurance of satisfactory operation.

Procedure.

Step	Item
1.	Plug in T-5101 to 117 volt AC, 60 hertz source.
2.	Turn on POWER switch on T-5101 and allow approximately 30 seconds for warm-up. SHIFT LOCK light on keyboard should be on.
3.	Cursor should appear. Check operation of BRIGHTNESS and CONTRAST controls.
	(a) Adjust BRICHTNESS control until raster just disappears.
	(b) Type A and adjust CONTRAST control to obtain a bright, but not smeared, character.
4.	Press CLEAR NUL and type:



Step	Item
5.	Press NEW LINE and PROG MODE. Type RUB, SPACE and CTRL a through o, which produces the following characters:  (Note: CTRL key must be depressed while typing lower case letters)
6.	Continuing as in Step 5, type CTRL p through z to display: 
7.	Type CTRL [\ ] HOME NEW LINE to display: 
8.	Using Cursor controls, position cursor on letter G obtained in Step 4. Press CHAR INSERT and $ to display:  Press CHAR DELETE to display:  Press ↓, the LINE INSERT to display:  Position cursor on letter V. Press LINE ERASE to display:  Press LINE DELETE to erase entire line. Position cursor on letter H. Press PAGE ERASE to erase all characters on display except those preceeding cursor. Press CLEAR NUL or CLEAR SPACE to erase rest of display.

Step	Item
9.	Check operation of the Keyboard lights. Depress following keys to turn on lamps, depress again to turn off lamps: PAGE EDIT PROG MODE CONV MODE PROT MODE SHIFT LOCK WRITE PROT (Depress while simultaneously depressing SHIFT key)
10.	Short between pins 2 and 3 of data interface connector. Set FBH switch to F, press PROG MODE and type: ESC=*C CTRL G RUB ESC) A ↓ M ESC (↑ ESC ^ 2 ESC ^ RETURN B →C NEW LINE D ESC E E ← ESC Q F ESC N ESC % HOME ↓ RUB RUB PROG MODE

Step	Item
	CONV MODE SEND LINE

The display obtained is shown in Figure 6-1. To reset the program, press CONV MODE, PAGE ERASE, PAGE EDIT, ESC $. Position cursor at end of program. Then press CONV MODE, SEND LINE.

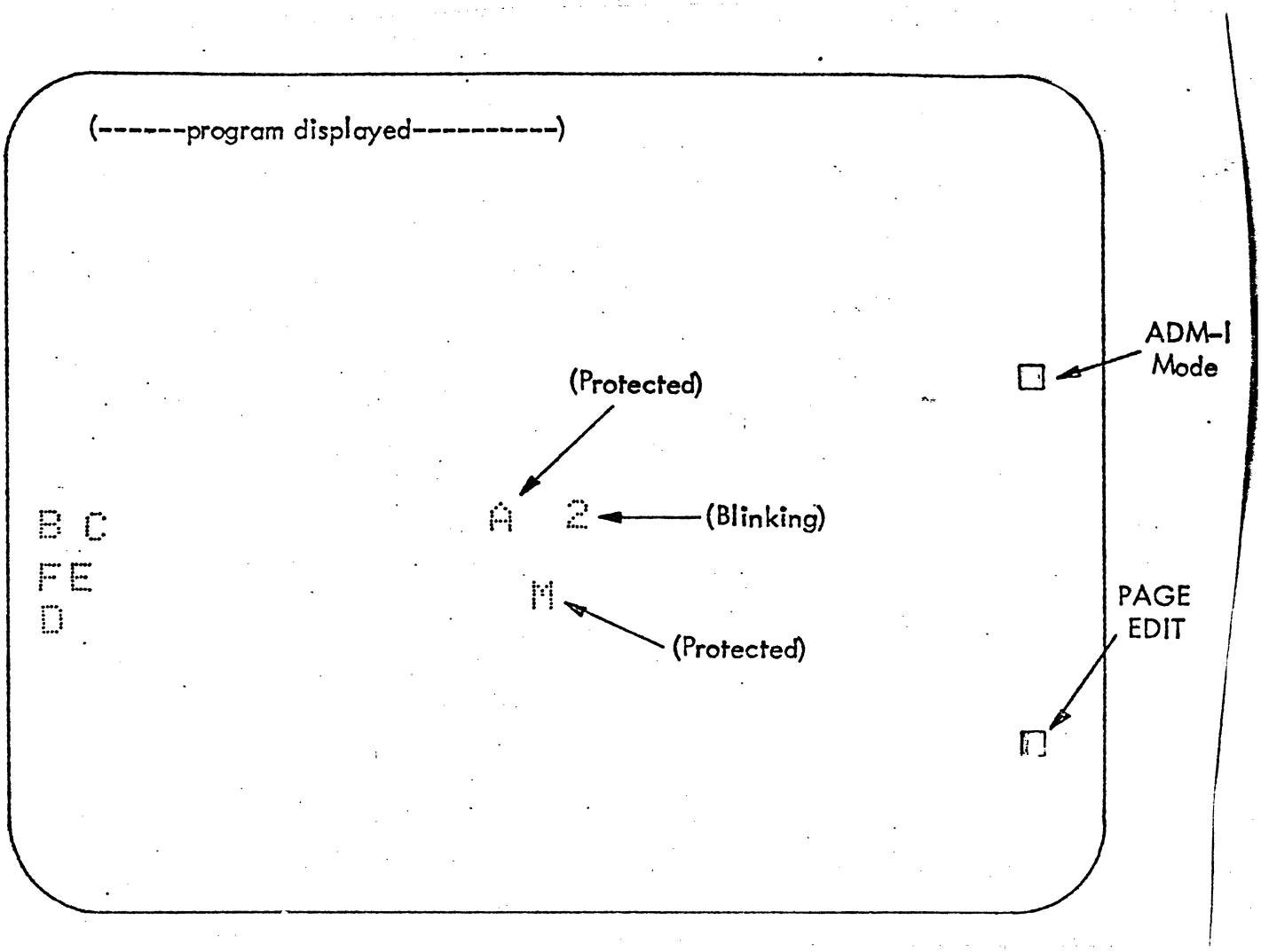


Figure 6-1.

Program Display

SAFETY PRECAUTIONS. The T-5101 Control-Indicator, has two shock potentials:

- 117 VAC, 60 Hz
- 12 KV, 2nd anode potential of CRT.

Each of these sources can produce a lethal or serious shock. Proper precautions must therefore be observed before handling any of the associated leads. Disconnect the AC power plug and discharge the AC power line filters to chassis ground before touching AC connections. Unplug the T-5101 from the AC power and discharge the 2nd anode lead to chassis ground before touching the red high voltage lead to the CRT 2nd anode, or the 2nd anode itself, or the flyback transformer attached to the read lead. Discharging circuits to chassis ground requires the use of an insulated test lead with a pointed tip on at least one end. First hold one end of the test lead onto the chassis and then touch the pointed end to the circuit connection to be discharged.

SECTION VII

T-5101 SCHEMATIC DRAWINGS AND DIAGRAMS

NOTE:

Figures 7-1 through 7-21 provide Logic Board schematics for the -7 configuration board.

Figures 7-22 through 7-44 provide Logic Board schematics for the -13 configuration board

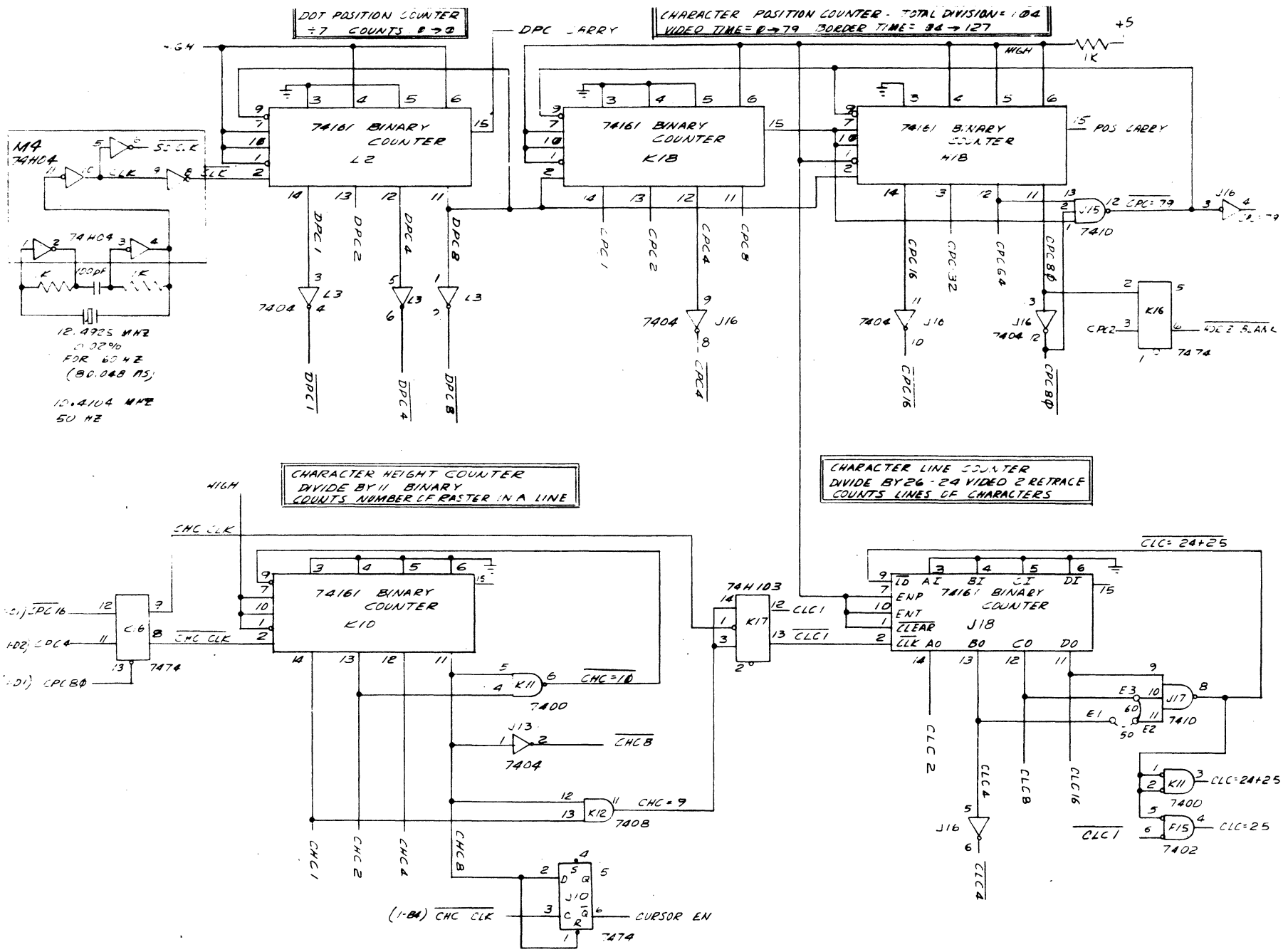

DOT POSITION COUNTER
÷7 COUNTS 0 → 6
DPC CARRY
CHARACTER POSITION COUNTER - TOTAL DIVISION = 104
VIDEO TIME = 0 → 79 BORDER TIME = 80 → 127
+5
1K
HIGH
74161 BINARY COUNTER
L2
K18
H18
POS CARRY
M4
74H04
50 C.K
CLK
CLC
100pf
12.4935 MHZ
± 32%
FOR 60 HZ
(80.048 NS)
12.4104 MHZ
50 HZ
DPC 1
DPC 2
DPC 4
DPC 8
7404
L3
J16
7410
J15
K16
7474
CPC=79
CHARACTER HEIGHT COUNTER
DIVIDE BY 11 BINARY
COUNTS NUMBER OF RASTER IN A LINE
CHARACTER LINE COUNTER
DIVIDE BY 26 - 24 VIDEO 2 RETRACE
COUNTS LINES OF CHARACTERS
CHC CLK
K10
C6
K11
7400
CHC=10
CHC B
J13
CHC=9
K12
7408
CHC 1
CHC 2
CHC 4
CHC B
J10
CURSOR EN
74H103
K17
CLC1
CLC=24+25
J18
E3
E1
E2
J17
F15
7402
CLC=25
CLC 2
CLC 4
CLC 8
CLC 16

Figure 7-1

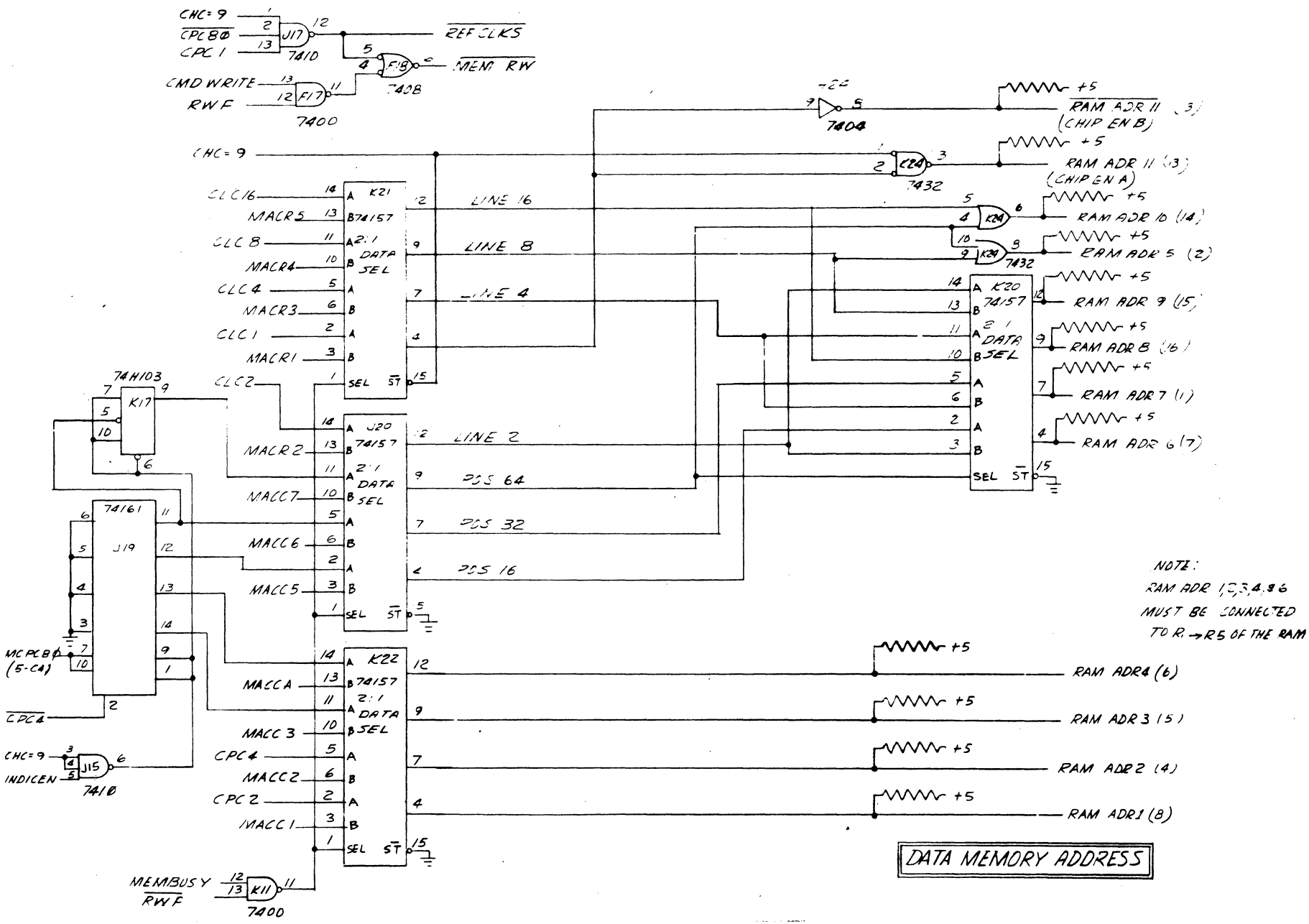

CHC=9
CPC80
CPC1
J17
7410
REF CLKS
F18
MEM RW
7408
CMD WRITE
RWF
F17
7400
CHC=9
CLC16
MACR5
CLC8
MACR4
CLC4
MACR3
CLC1
MACR1
CLC2
K21
74157
2:1 DATA SEL
LINE 16
LINE 8
LINE 4
74H103
K17
MACR2
MACC7
MACC6
MACC5
J20
LINE 2
DS 64
DS 32
DS 16
74161
J19
MCPC80 (5-C4)
CPC4
CHC=9
INDICEN
J15
7410
MACCA
MACC3
CPC4
MACC2
CPC2
MACC1
K22
RAM ADR4 (6)
RAM ADR3 (5)
RAM ADR2 (4)
RAM ADR1 (8)
MEMBUSY
RWF
K11
7400
7404
RAM ADR 11 (3) (CHIP EN B)
RAM ADR 11 (3) (CHIP EN A)
7432
K20
RAM ADR 10 (14)
RAM ADR 5 (2)
RAM ADR 9 (15)
RAM ADR 8 (16)
RAM ADR 7 (1)
RAM ADR 6 (7)
NOTE:
RAM ADR 1,2,3,4,8 6
MUST BE CONNECTED
TO R.→R5 OF THE RAM
DATA MEMORY ADDRESS

Figure 7-2

16 EA MOSTEK 4508-9P
1024 RAM

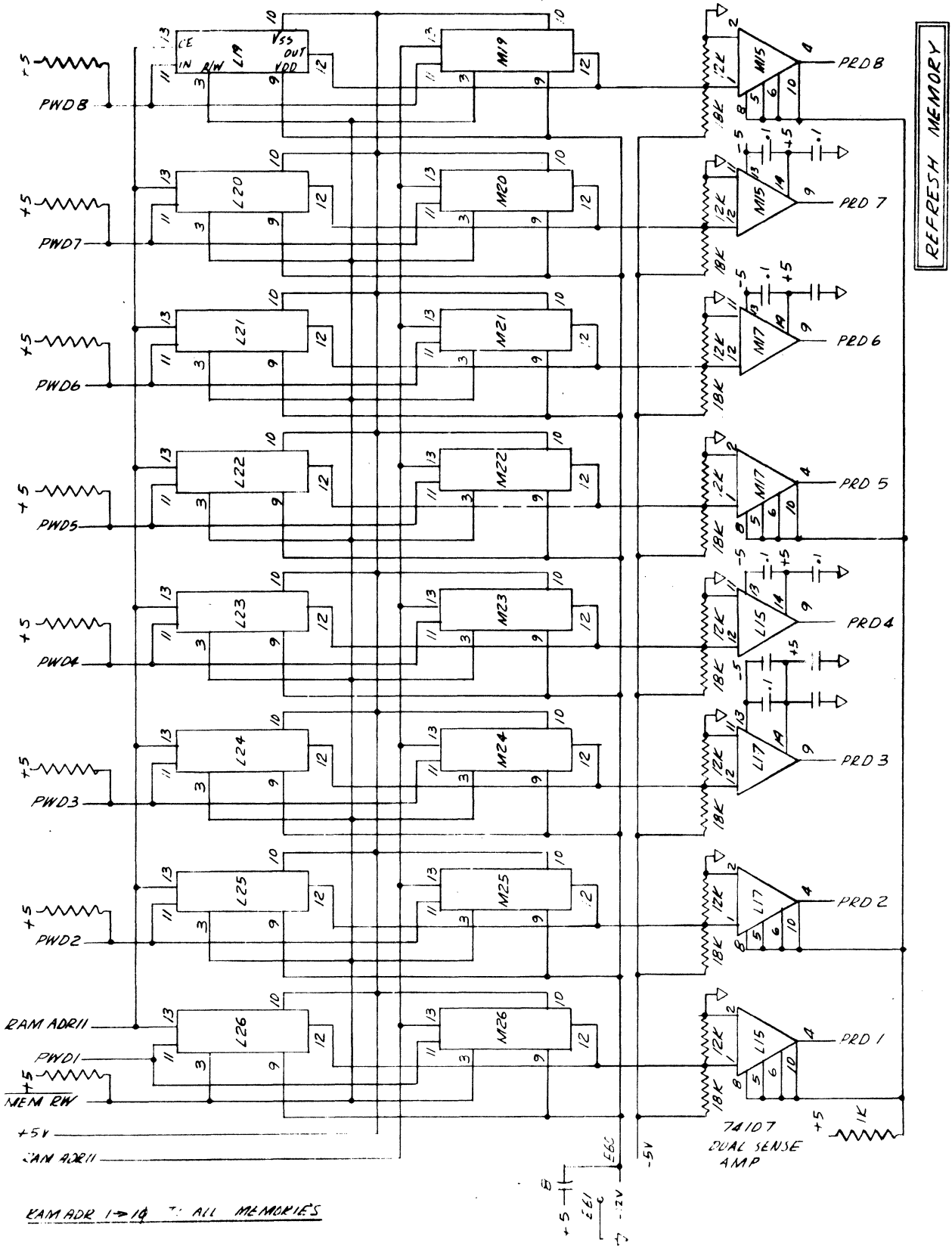


Figure 7-3

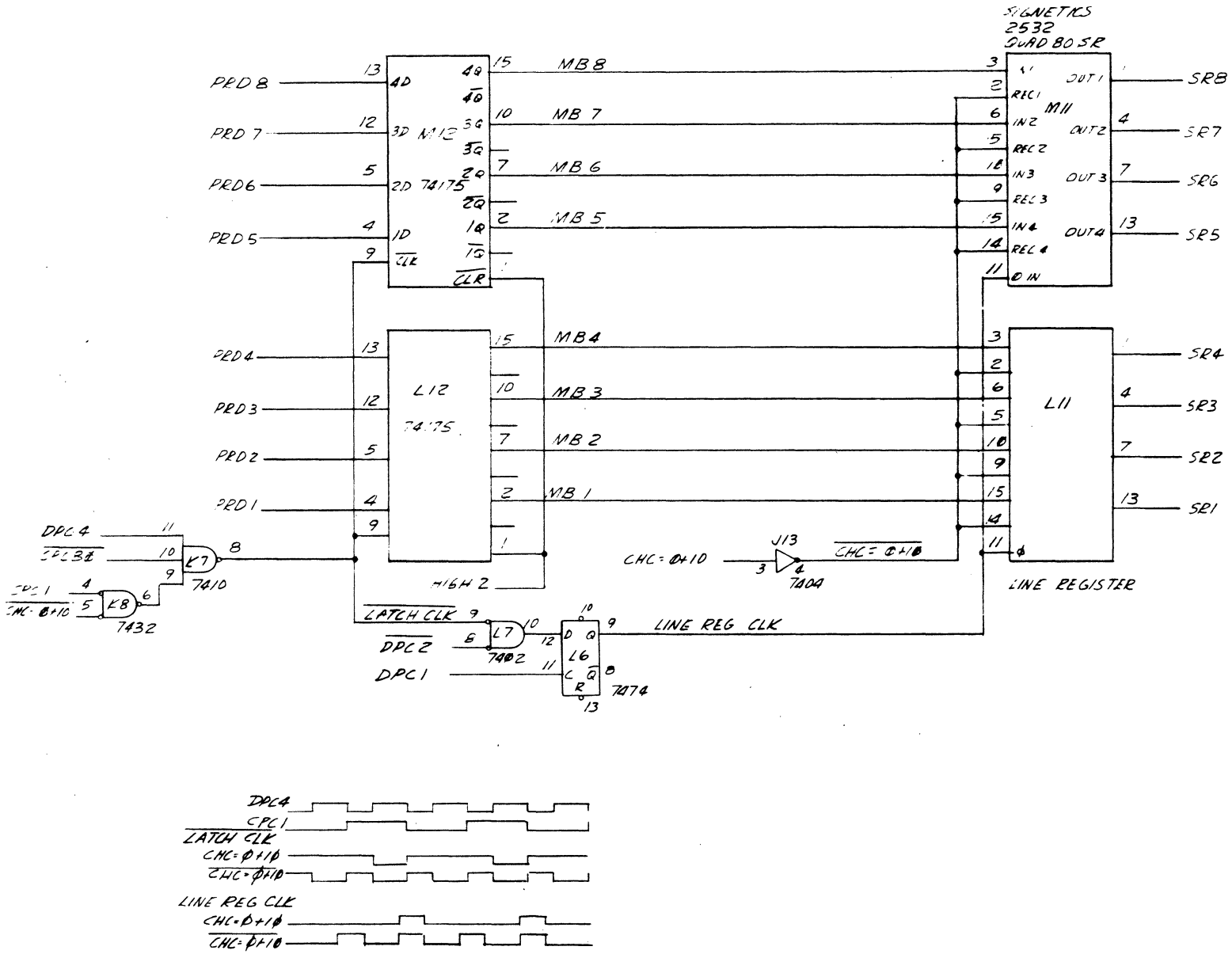

SIGNETICS
2532
QUAD 80 SR
M12
7475
L12
7475
M11
L11
LINE REGISTER
PRD 8
PRD 7
PRD 6
PRD 5
PRD 4
PRD 3
PRD 2
PRD 1
MB 8
MB 7
MB 6
MB 5
MB 4
MB 3
MB 2
MB 1
SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
DPC 4
CPC 1
CHC=Ø+1Ø
7410
7432
LATCH CLK
DPC 2
DPC 1
7402
7474
LINE REG CLK
CHC=Ø+1Ø
7404
DPC4
CPC1
LATCH CLK
CHC=Ø+1Ø
LINE REG CLK
CHC=Ø+1Ø

Figure 7-4

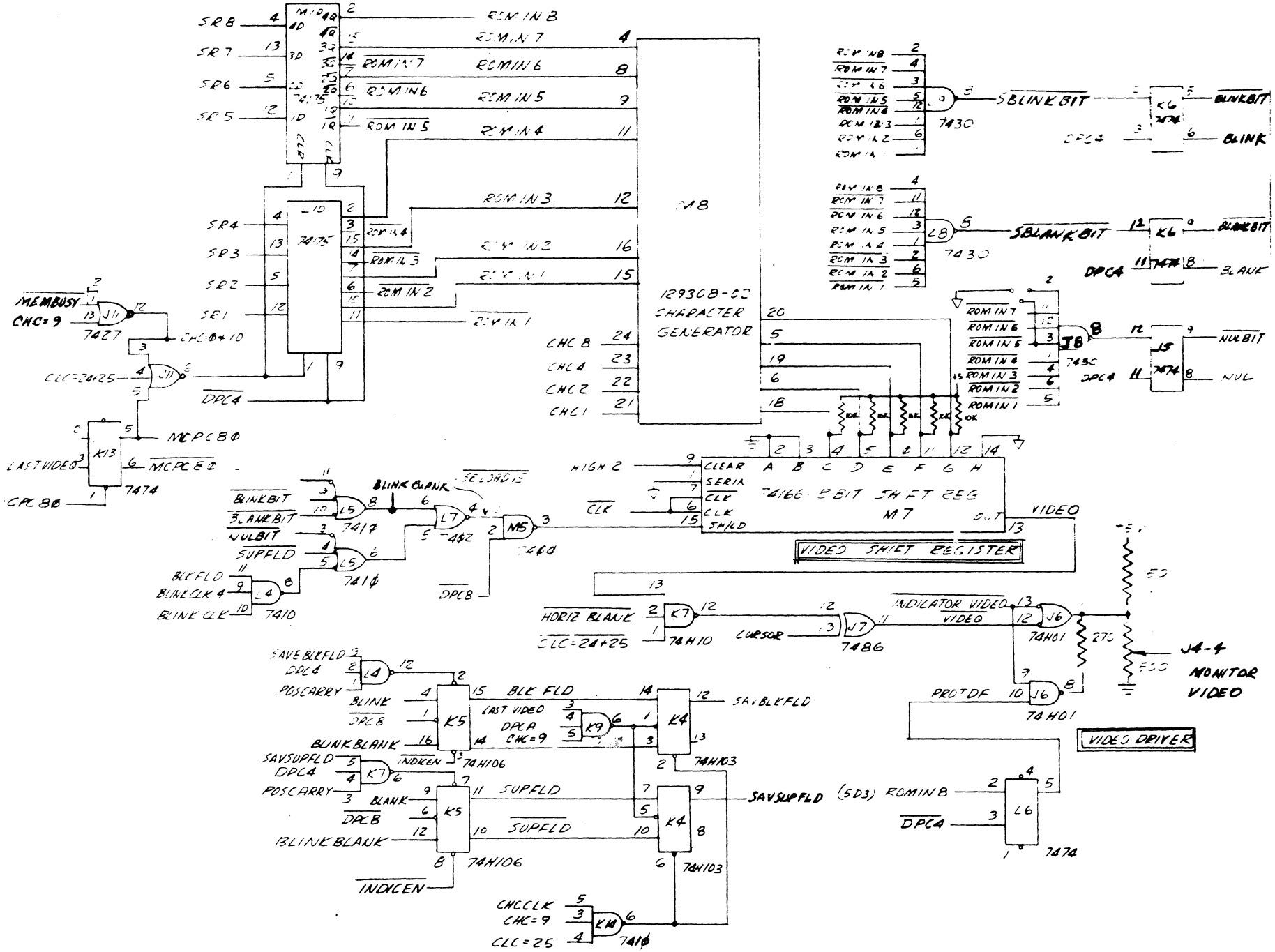

SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
ROM IN B
ROM IN 7
ROM IN 6
ROM IN 5
ROM IN 4
ROM IN 3
ROM IN 2
ROM IN 1
12930B-02
CHARACTER
GENERATOR
CHC 8
CHC 4
CHC 2
CHC 1
SBLINK BIT
SBLANK BIT
BLINK BIT
BLINK
BLANK BIT
BLANK
NUL BIT
NUL
MEMBUSY
CHC=9
CHC=24+25
DPCA
DPCB
MCPC80
MCPCE0
LAST VIDEO
CPC80
BLINK BLANK
BLINKBIT
BLANKBIT
NULBIT
SUPFLD
BLKFLD
BLINK CLK 4
BLINK CLK
SELOADIS
HIGH 2
CLK
74166 8 BIT SHIFT REG
M7
VIDEO
VIDEO SHIFT REGISTER
HORIZ BLANK
CURSOR
INDICATOR VIDEO
VIDEO
270
J4-4
MONITOR
VIDEO
PROTDF
VIDEO DRIVER
SAVE BLKFLD
POSCARRY
BLINK
BLK FLD
LAST VIDEO
SA1 BLKFLD
SAVSUPFLD
INDICEN
SUPFLD
(SD3) ROMIN B
CHCCLK
CLC=25

Figure 7-5

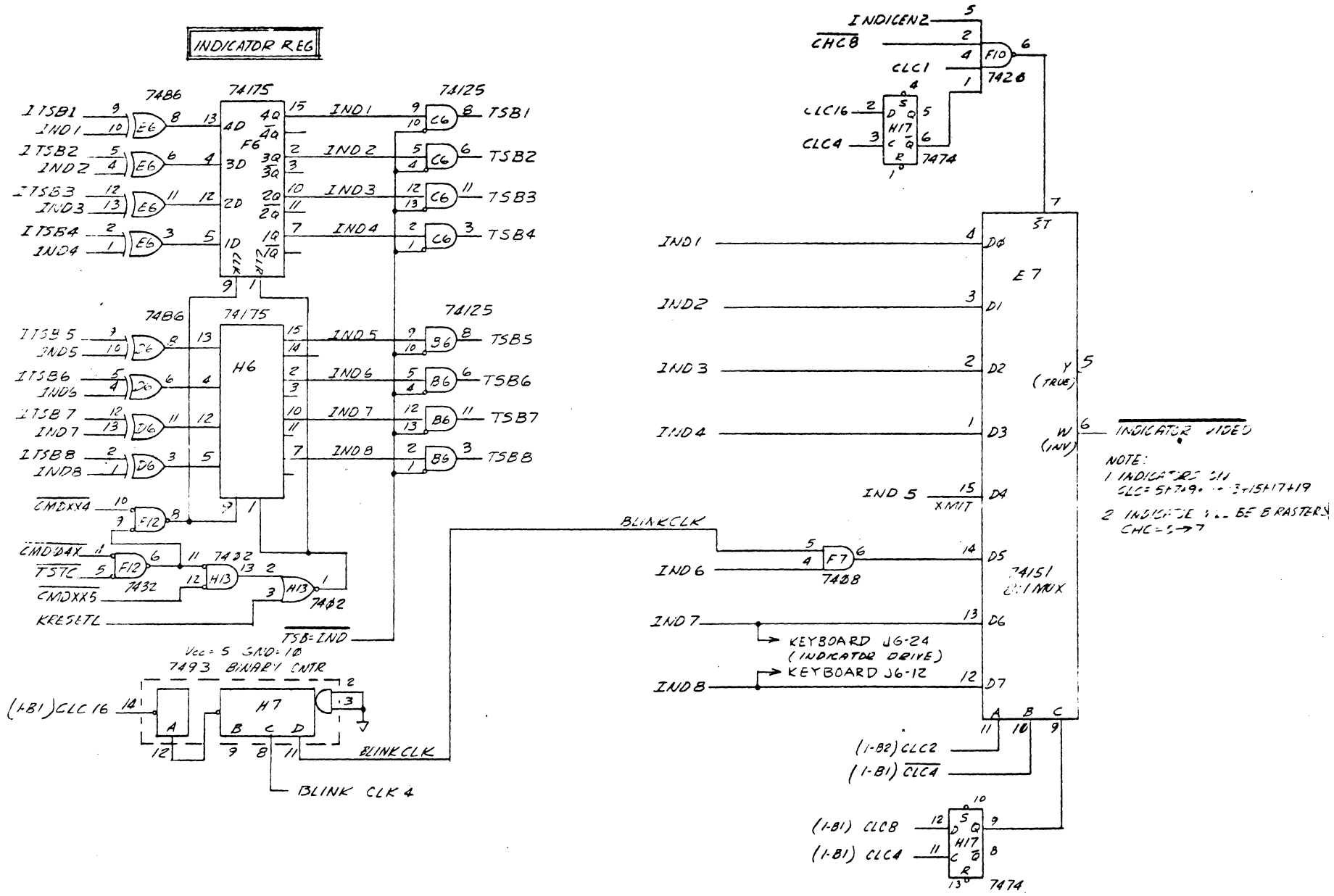

INDICATOR REG
7486
74175
74125
ITSB1
IND1
ITSB2
IND2
ITSB3
IND3
ITSB4
IND4
ITSB5
IND5
ITSB6
IND6
ITSB7
IND7
ITSB8
IND8
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
TSB8
CMDXX4
CMDDAX
TSTC
CMDXX5
KRESETL
7432
7402
TSB=IND
Vcc = 5 GND = 10
7493 BINARY CNTR
(1-B1)CLC16
BLINKCLK
BLINK CLK 4
INDICEN2
CHCB
CLC1
CLC16
CLC4
7474
IND1
IND2
IND3
IND4
IND5 XMIT
IND6
IND7
IND8
74151 8:1 MUX
KEYBOARD J6-24 (INDICATOR DRIVE)
KEYBOARD J6-12
(1-B2) CLC2
(1-B1) CLC4
(1-B1) CLCB
(1-B1) CLC4
INDICATOR VIDEO
NOTE:
1 INDICATORS 1,11
2 INDICATOR 1 ... BE BLANKED

Figure 7-6

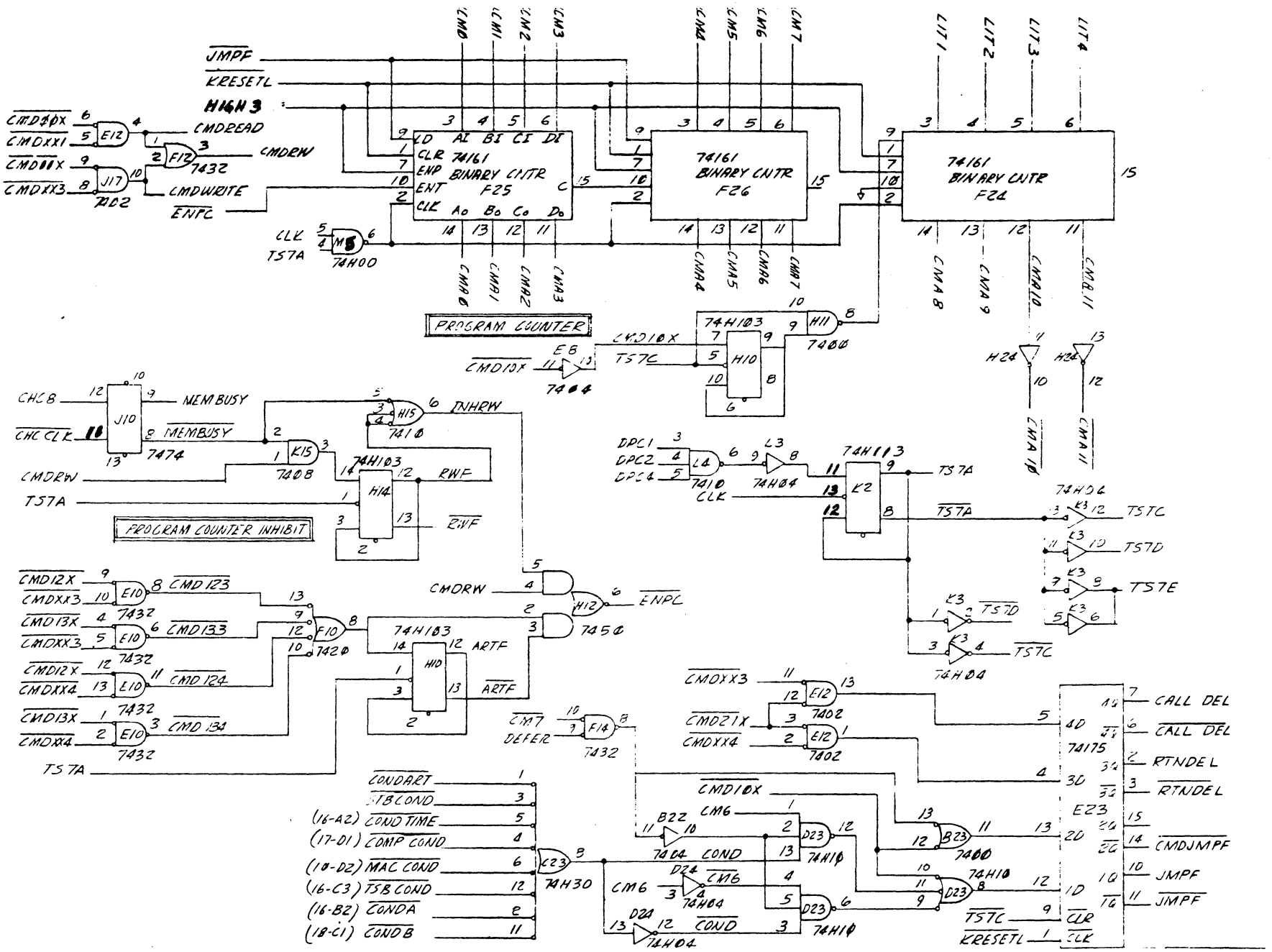

JMPF
KRESETL
HIGH 3
CMDRDX
CMDXX1
CMDWX
CMDXX3
CMDREAD
CMDRW
CMDWRITE
ENPC
CLK
TS7A
PROGRAM COUNTER
PROGRAM COUNTER INHIBIT
CMDIDX
TS7C
CHC B
CHC CLK
MEMBUSY
INHRW
CMDRW
TS7A
RWF
ZWF
DPC1
DPC2
DPC4
CLK
TS7A
TS7C
TS7D
TS7E
CMD12X
CMDXX3
CMD123
CMD13X
CMD133
CMD124
CMD134
TS7A
CMDRW
ENPC
74H103
ARTF
CONDART
STBCOND
(16-A2) CONDTIME
(17-D1) COMP COND
(18-D2) MAC COND
(16-C3) TSB COND
(16-B2) CONDA
(18-C1) CONDB
CMDIDX
CMDXX3
CMDZIX
CMDXX4
CMG
COND
CALL DEL
RTNDEL
CMDJMPF
JMPF
TS7C
KRESETL
CLR
CLK

Figure 7-7

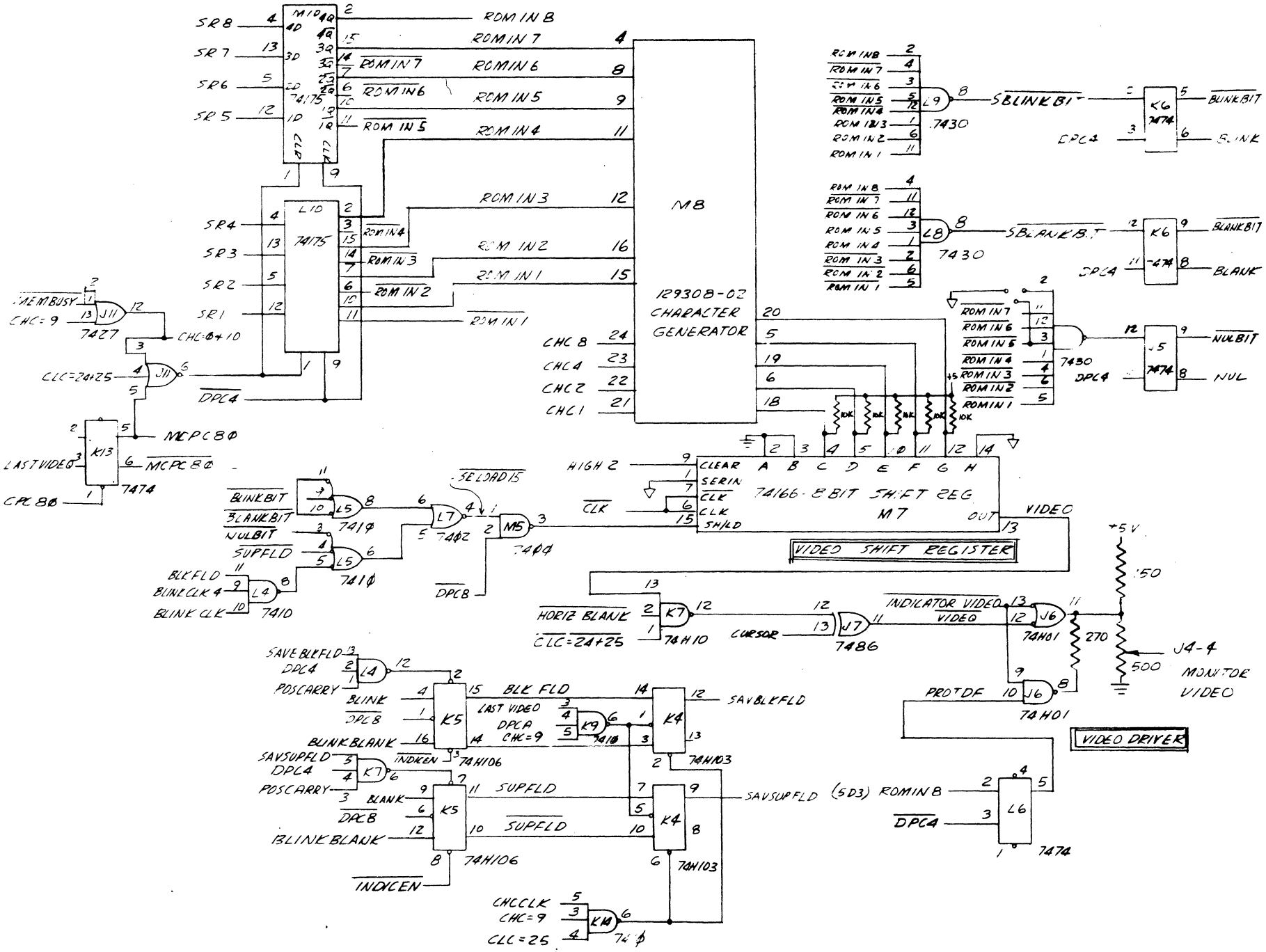

M8
12930B-02
CHARACTER
GENERATOR
ROM IN 8
ROM IN 7
ROM IN 6
ROM IN 5
ROM IN 4
ROM IN 3
ROM IN 2
ROM IN 1
SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
74175
CHC 8
CHC 4
CHC 2
CHC 1
DPC4
DPC8
MEMBUSY
CHC=9
7427
CHC=8+10
CLC=24+25
MCPC8Ø
LASTVIDEO
7474
CPC8Ø
BLINKBIT
BLANKBIT
NULBIT
SUPFLD
BLKFLD
BLINKCLK 4
BLINK CLK
7410
7400
7402
SELOAD15
HIGH 2
CLEAR
SERIN
CLK
SH/LD
74166 8 BIT SHIFT REG
M7
OUT
VIDEO
VIDEO SHIFT REGISTER
HORIZ BLANK
CLC=24+25
CURSOR
7486
INDICATOR VIDEO
VIDEO
74H01
+5V
150
270
500
J4-4
MONITOR
VIDEO
PROTDF
VIDEO DRIVER
SBLINKBI
SBLANKBI
BLINKBIT
BLANKBIT
NULBIT
BLINK
BLANK
NUL
7430
7474
SAVEBLKFLD
POSCARRY
BLINK
BLINKBLANK
SAVSUPFLD
INDXEN
BLK FLD
SUPFLD
SAVBLKFLD
SAVSUPFLD
74H106
74H103
(SD3) ROMINB
CHCCLK
CHC=9
CLC=25
74Ø

Figure 7-5

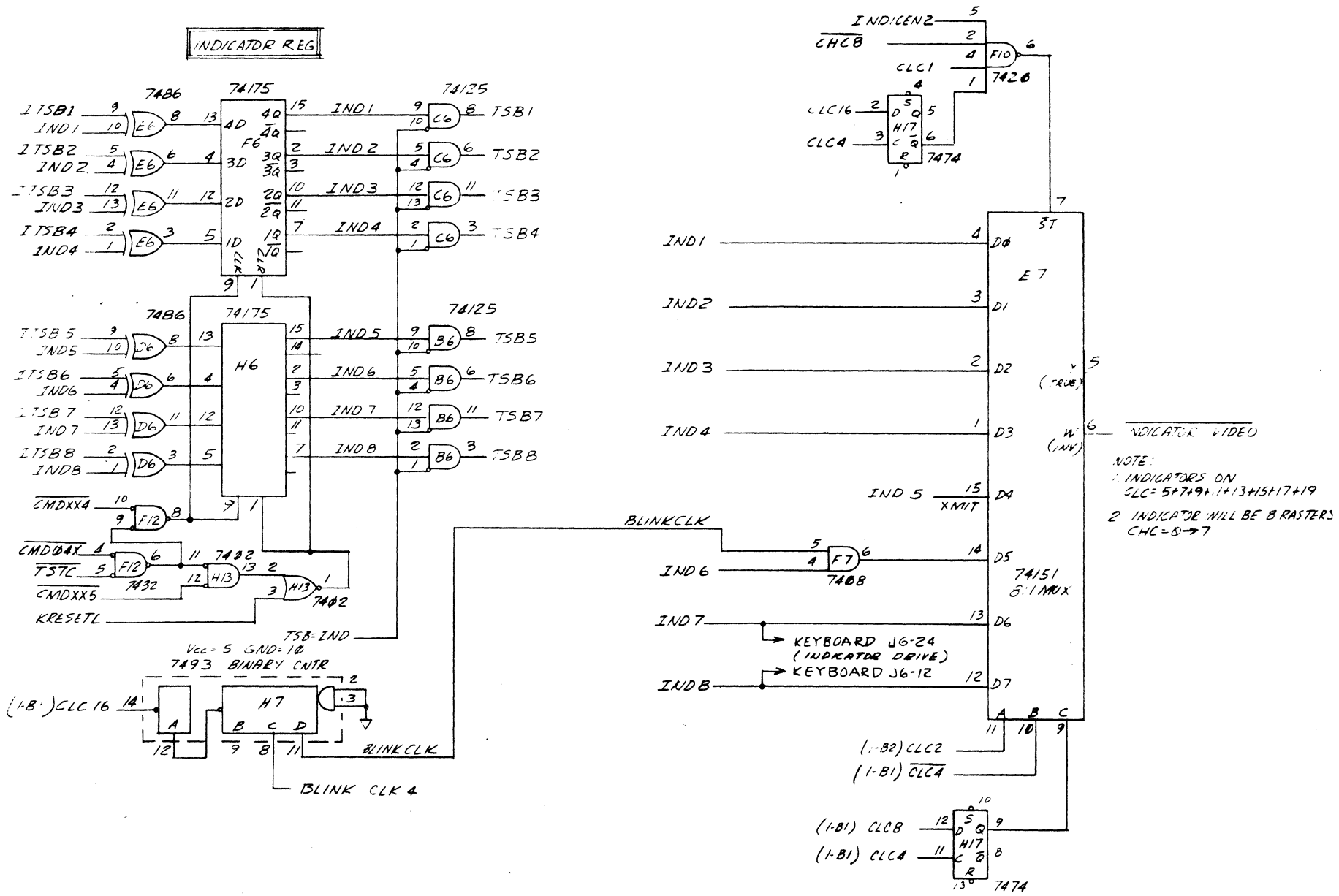

INDICATOR REG
7486
74175
74125
ITSB1
IND1
ITSB2
IND2
ITSB3
IND3
ITSB4
IND4
TSB1
TSB2
TSB3
TSB4
IND1
IND2
IND3
IND4
F6
H6
ITSB5
IND5
ITSB6
IND6
ITSB7
IND7
ITSB8
IND8
TSB5
TSB6
TSB7
TSB8
CMDXX4
CMDDATX
TSTC
CMDXX5
KRESETL
7432
7402
TSB=IND
Vcc=5 GND=10
7493 BINARY CNTR
(1-B') CLC16
H7
BLINK CLK 4
BLINKCLK
INDICEN2
CHC8
CLC1
CLC16
CLC4
7474
IND1
IND2
IND3
IND4
IND5
XMIT
IND6
IND7
IND8
E7
74151
8:1 MUX
(TRUE)
INDICATOR VIDEO
NOTE:
1. INDICATORS ON
CLC= 5+7+9+11+13+15+17+19
2 INDICATOR WILL BE 8 RASTERS
CHC=8→7
KEYBOARD J6-24
(INDICATOR DRIVE)
KEYBOARD J6-12
(1-B2) CLC2
(1-B1) CLC4
(1-B1) CLC8
(1-B1) CLC4

Figure 7-6

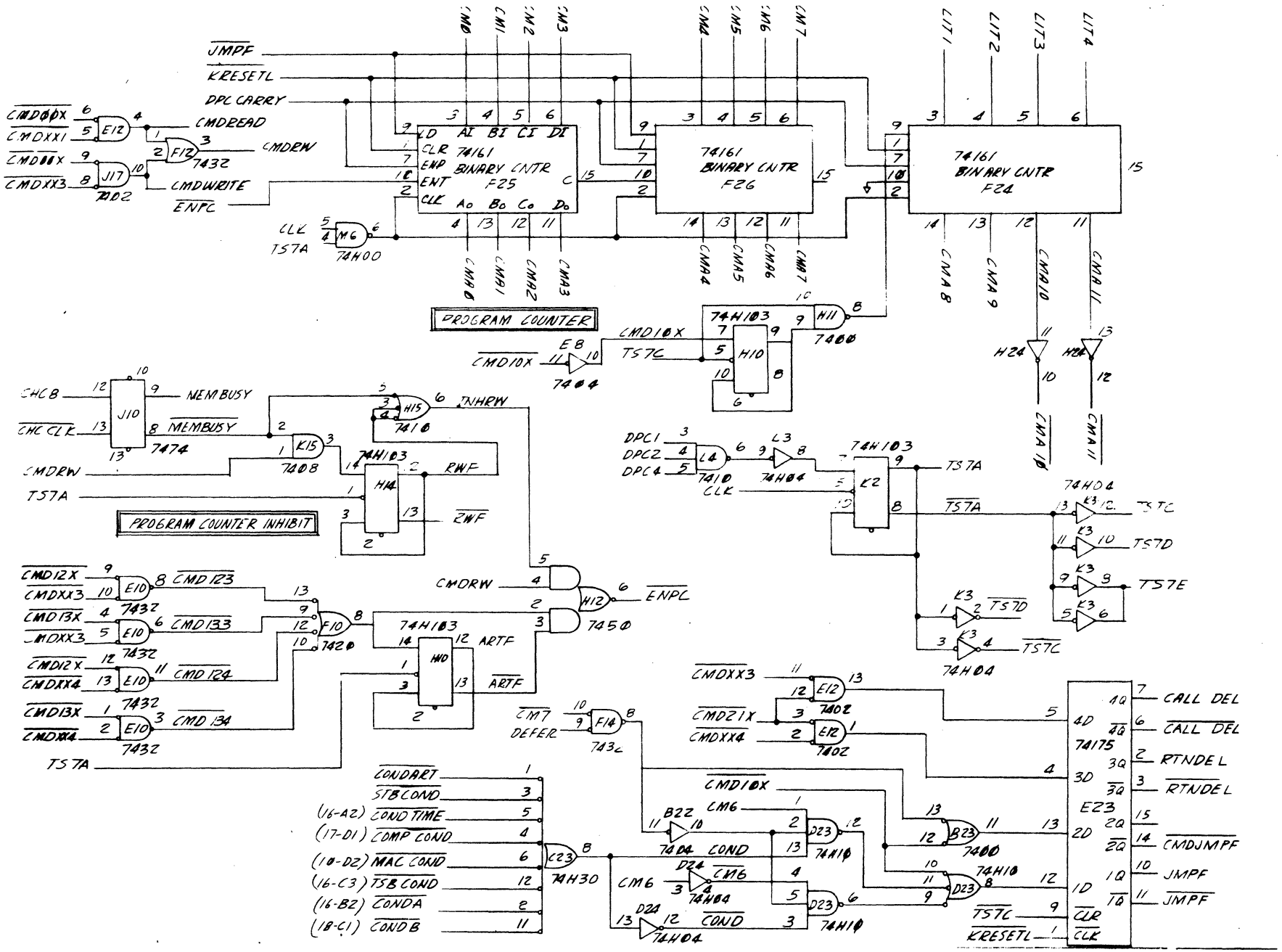
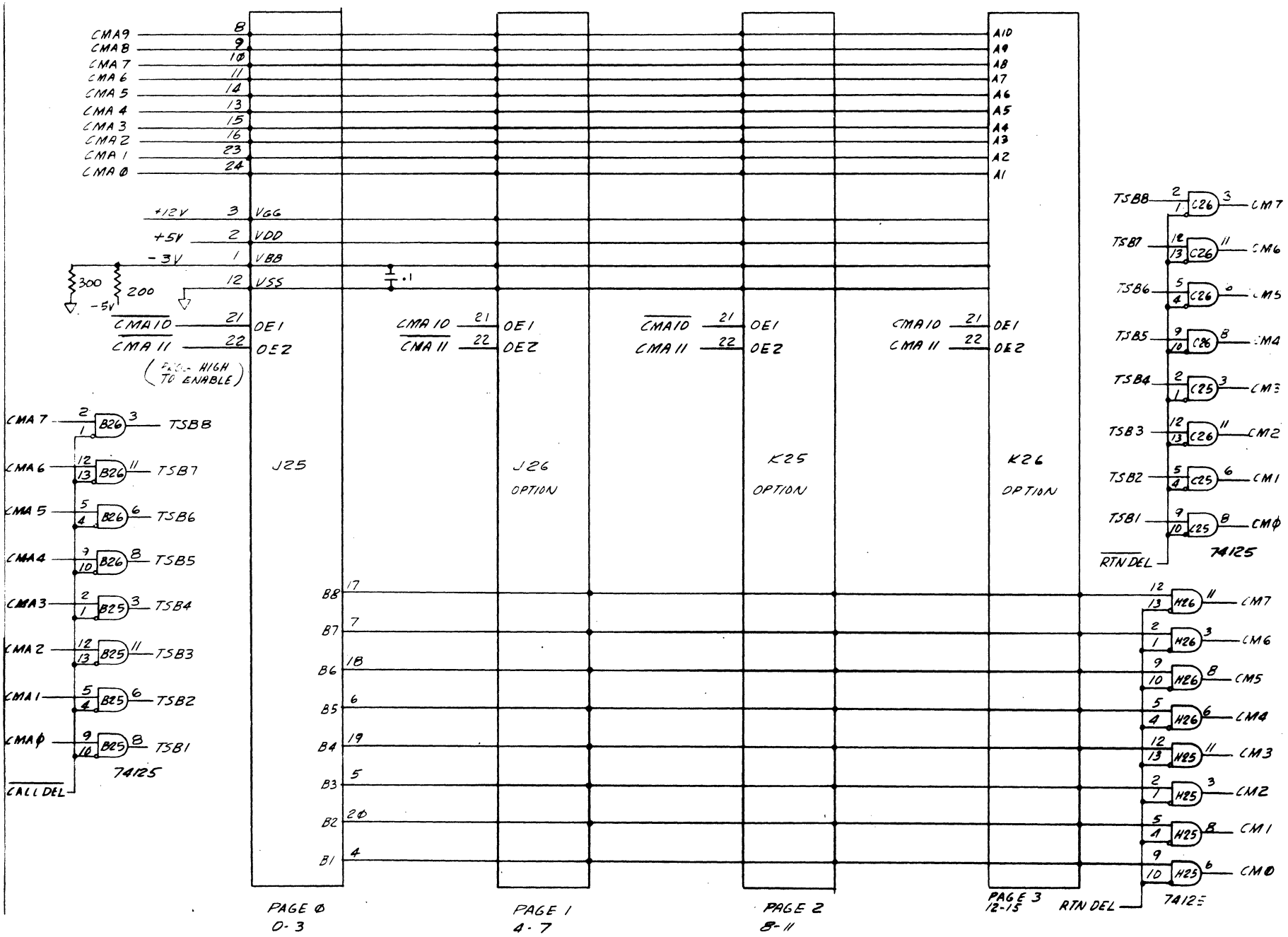

JMPF
KRESETL
DPC CARRY
CMD00X
CMDXX1
CMDREAD
CMDRW
CMD00X
CMDXX3
CMDWRITE
ENPC
E12
F12
7432
J17
7402
CLK
TS7A
M6
74H00
CM0
CM1
CM2
CM3
CM4
CM5
CM6
CM7
LIT1
LIT2
LIT3
LIT4
LD AI BI CI DI
CLR 74161
ENP BINARY CNTR
ENT F25
CLK A0 B0 C0 D0
74161
BINARY CNTR
F26
74161
BINARY CNTR
F24
CMA0
CMA1
CMA2
CMA3
CMA4
CMA5
CMA6
CMA7
CMA8
CMA9
CMA10
CMA11
PROGRAM COUNTER
CMD10X
E8
7404
74H103
H10
H11
7400
H24
H25
CMA10
CMA11
CHCB
CHC CLR
J10
7474
MEMBUSY
MEMBUSY
K15
7408
H15
7410
TXHRW
CMDRW
TS7A
H14
RWF
RWF
PROGRAM COUNTER INHIBIT
DPC1
DPC2
DPC4
L4
7410
CLK
L3
74H04
E2
TS7A
TS7A
74H04
K3
TS7C
TS7D
TS7E
TS7D
TS7C
CMD12X
CMDXX3
CMD13X
CMDXX3
CMD12X
CMDXX4
CMD13X
CMDXX4
E10
7432
CMD123
CMD133
CMD124
CMD134
F10
7420
74H103
H10
ARTF
ARTF
CMDRW
H12
7450
ENPC
CM7
DEFER
F14
7430
CMDXX3
CMDZ1X
CMDXX4
E12
7402
CONDART
STBCOND
(16-A2) COND TIME
(17-D1) COMP COND
(18-D2) MAC COND
(16-C3) TSB COND
(16-B2) CONDA
(18-C1) CONDB
C23
74H30
B22
7404
COND
CM6
D24
74H04
CMD10X
D23
74H10
B23
7400
TS7C
KRESETL
E23
74175
4D 1D 2D 3D
1Q 2Q 3Q 4Q
1CLR 2CLR 3CLR 4CLR
1CLK 2CLK 3CLK 4CLK
CALL DEL
CALL DEL
RTNDEL
RTNDEL
CMDJMPF
JMPF
JMPF

Figure 7-7



MOTOROLA MCM 6560L OPTIONA (102[illegible]E) ROM

Figure 7-8

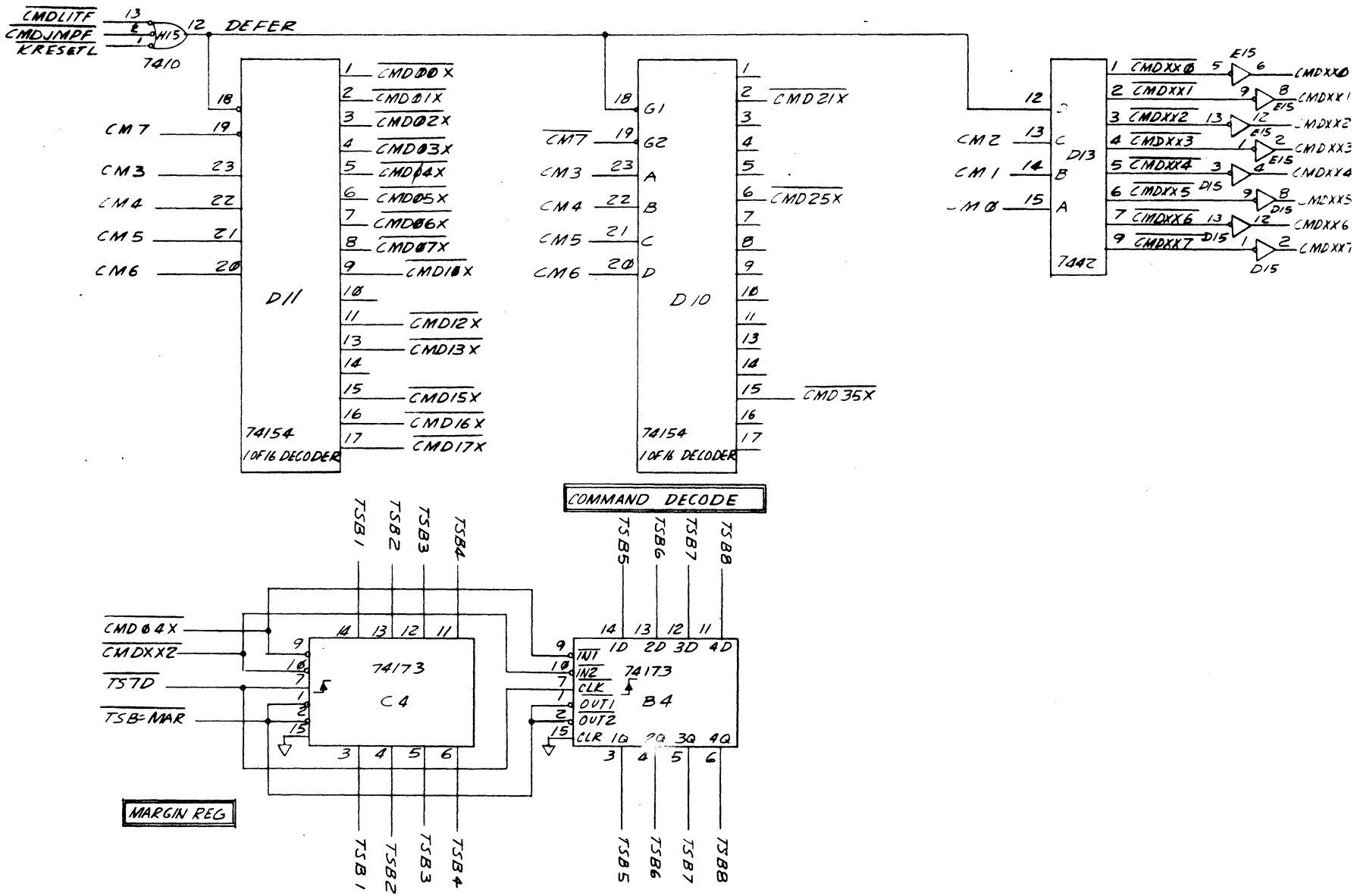

CMDLITF
CMDJMPF
KRESETL
7410
DEFER
D11
74154
1 OF 16 DECODER
D10
74154
1 OF 16 DECODER
D13
7442
CM7
CM3
CM4
CM5
CM6
CM2
CM1
CM0
CMD00X
CMD01X
CMD02X
CMD03X
CMD04X
CMD05X
CMD06X
CMD07X
CMD10X
CMD12X
CMD13X
CMD15X
CMD16X
CMD17X
CMD21X
CMD25X
CMD35X
CMDXX0
CMDXX1
CMDXX2
CMDXX3
CMDXX4
CMDXX5
CMDXX6
CMDXX7
COMMAND DECODE
MARGIN REG
74173
C4
74173
B4
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
TSB8
CMD04X
CMDXX2
TS7D
TSB=MAR

Figure 7-9

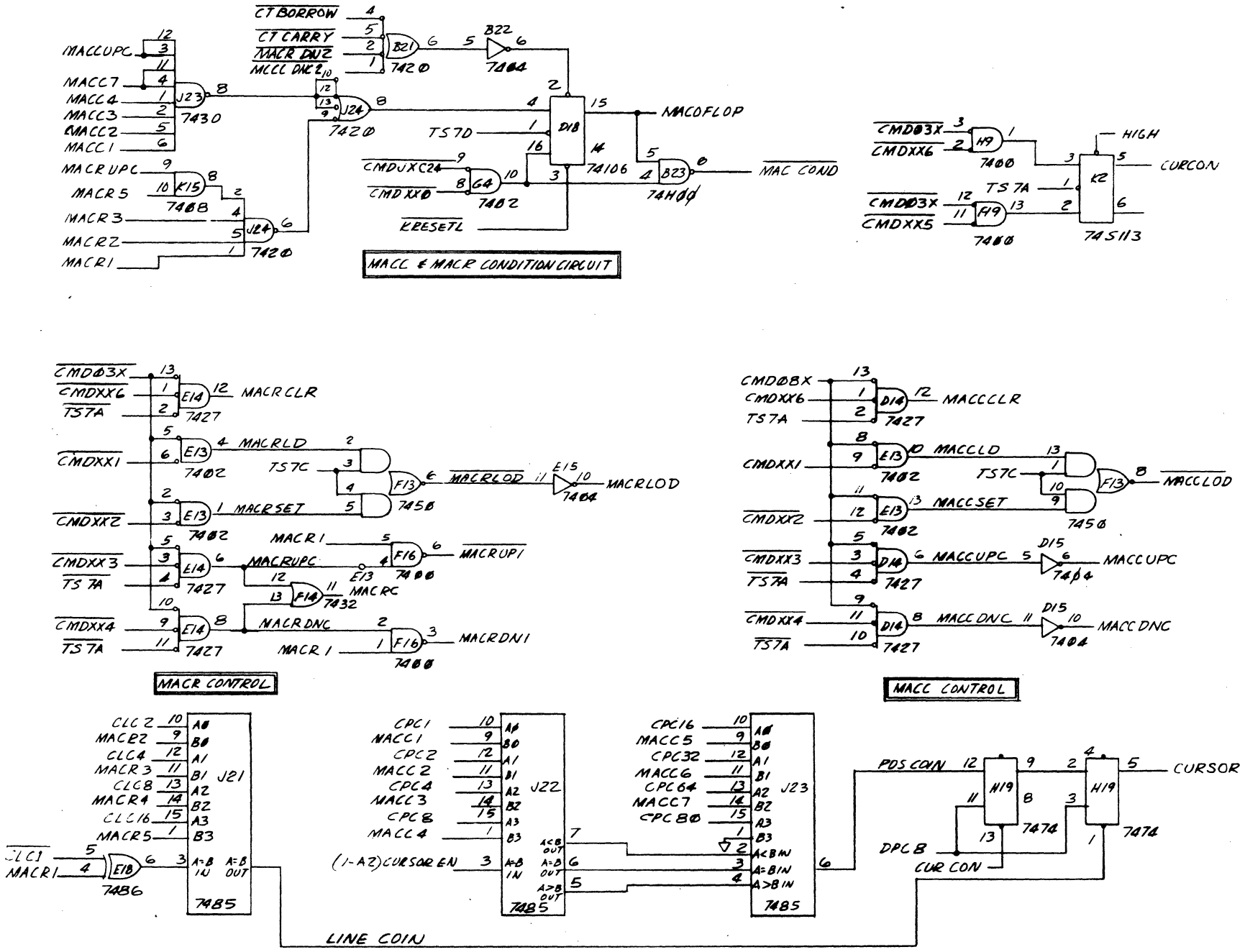

MACC & MACR CONDITION CIRCUIT
MACR CONTROL
MACC CONTROL
MACCUPC
MACC7
MACC4
MACC3
MACC2
MACC1
MACRUPC
MACR5
MACR3
MACR2
MACR1
CT BORROW
CT CARRY
MACR DNZ
MCCC ONE
MACOFLOP
TS7D
CMDUXC24
CMDXX0
RRESETL
MAC COND
CMD03X
CMDXX6
HIGH
CURCON
TS7A
CMDXX5
CMD0BX
MACCCLR
MACCLD
CMDXX1
MACCSET
CMDXX2
CMDXX3
MACCUPC
CMDXX4
MACCDNC
MACRCLR
MACRLD
MACRSET
MACRUPC
MACRC
MACRDNC
MACRLOD
MACRUPI
MACRDNI
CLC2
MACR2
CLC4
MACR3
CLC8
MACR4
CLC16
MACR5
CLC1
MACR1
CPC1
MACC1
CPC2
MACC2
CPC4
MACC3
CPC8
MACC4
(1-A2)CURSOR EN
CPC16
MACC5
CPC32
MACC6
CPC64
MACC7
CPC80
PDS COIN
DPC8
CUR CON
CURSOR
LINE COIN

Figure 7-10

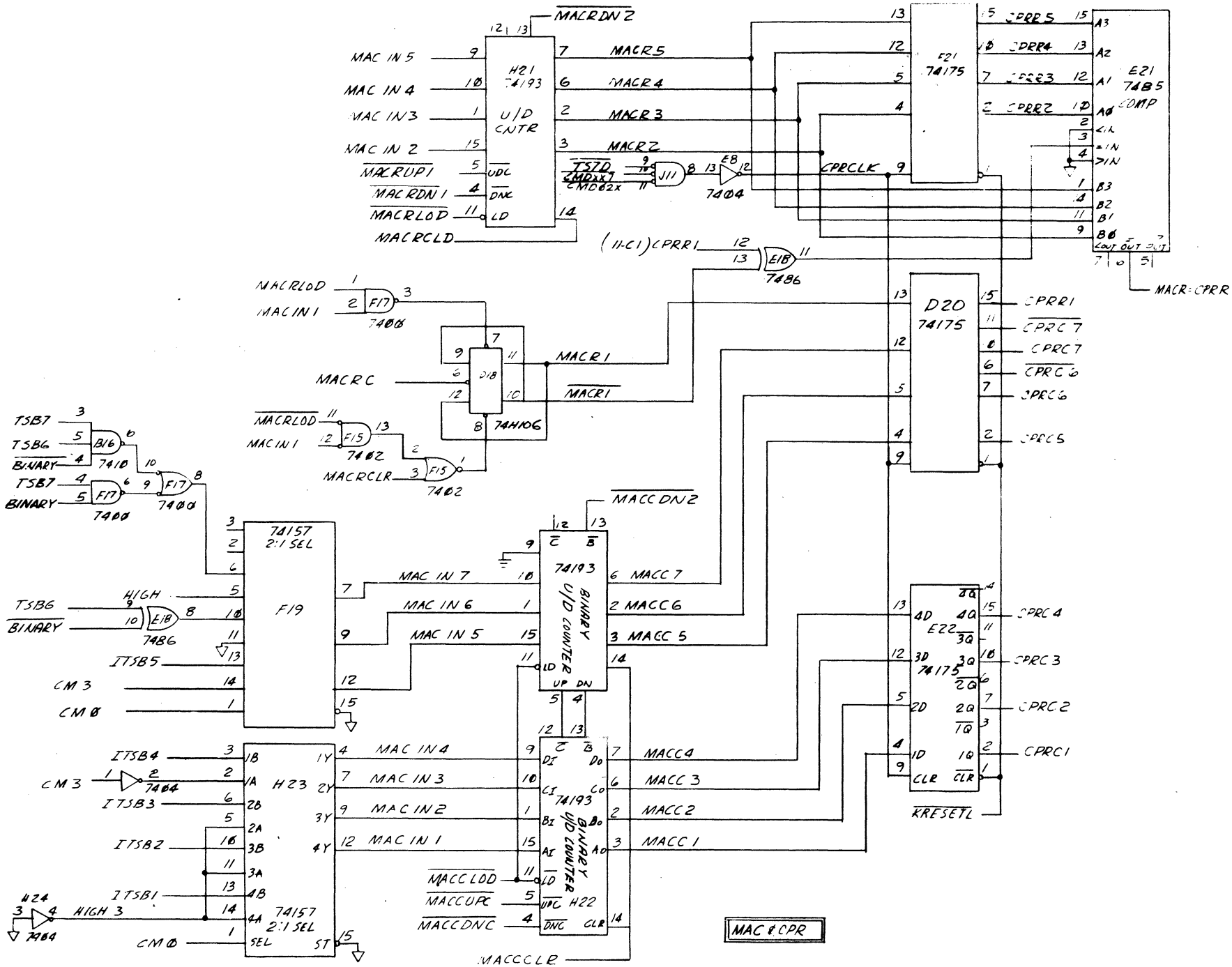

MACRDN2
MAC IN 5
MAC IN 4
MAC IN 3
MAC IN 2
MACRUP1
MACRDN1
MACRLOD
MACRCLD
H21
74193
U/D
CNTR
MACR5
MACR4
MACR3
MACR2
UDC
DNC
LD
TSTD
CMD02x
J11
E8
7404
CPRCLK
F21
74175
CPRR5
CPRR4
CPRR3
CPRR2
E21
7485
COMP
A>B
A=B
A<B
MACR=CPRR
(11-C1)CPRR1
E18
7486
MACRLOD
MAC IN 1
F17
7408
MACR C
D18
MACR1
MACR1
74H106
MACRLOD
MAC IN 1
F15
7402
MACRCLR
D20
74175
CPRR1
CPRC7
CPRC7
CPRC6
CPRC6
CPRC5
TSB7
TSB6
BINARY
B16
7410
TSB7
BINARY
F17
7408
7408
74157
2:1 SEL
F19
HIGH
TSB6
BINARY
E18
7486
ITSB5
CM 3
CM 0
MACCDN2
74193
U/D COUNTER
BINARY
UP DN
MAC IN 7
MAC IN 6
MAC IN 5
MACC7
MACC6
MACC5
E22
74175
CPRC4
CPRC3
CPRC2
CPRC1
KRESETL
ITSB4
CM 3
7404
ITSB3
ITSB2
ITSB1
H24
HIGH 3
7404
H23
74157
2:1 SEL
MAC IN 4
MAC IN 3
MAC IN 2
MAC IN 1
MACC4
MACC3
MACC2
MACC1
MACCLOD
MACCUP
MACCDNC
H22
MACCCLR
MAC & CPR

Figure 7-11

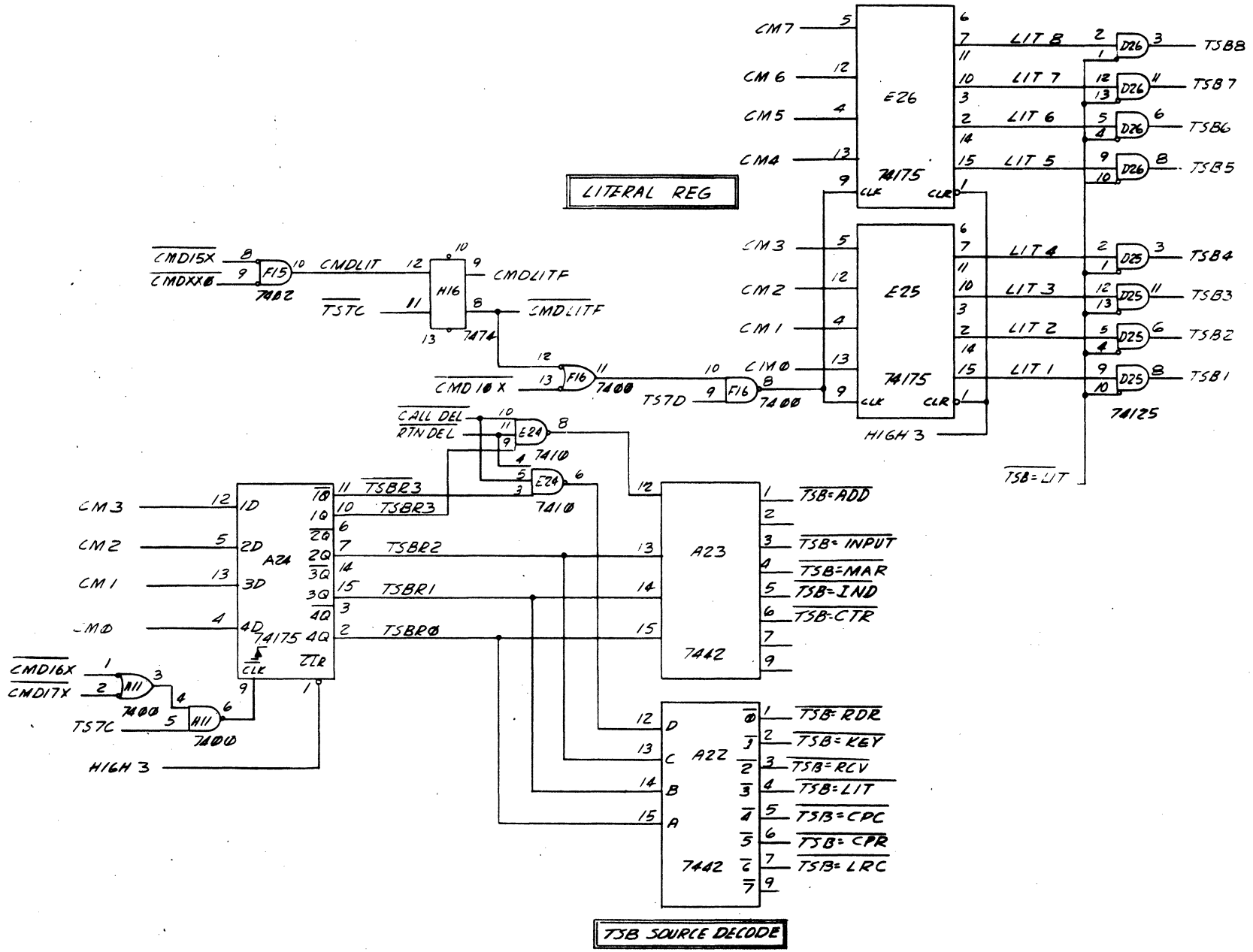

LITERAL REG
E26
74175
E25
74175
74125
LIT 8
LIT 7
LIT 6
LIT 5
LIT 4
LIT 3
LIT 2
LIT 1
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
HIGH 3
TSB=LIT
CMD15X
CMDXX0
CMDLIT
CMDLITF
TS7C
CMD10X
TS7D
CALL DEL
RTN DEL
A24
74175
TSBR3
TSBR2
TSBR1
TSBR0
CMD16X
CMD17X
A23
7442
TSB=ADD
TSB=INPUT
TSB=MAR
TSB=IND
TSB=CTR
A22
7442
TSB=RDR
TSB=KEY
TSB=RCV
TSB=LIT
TSB=CPC
TSB=CPR
TSB=LRC
TSB SOURCE DECODE

Figure 7-12

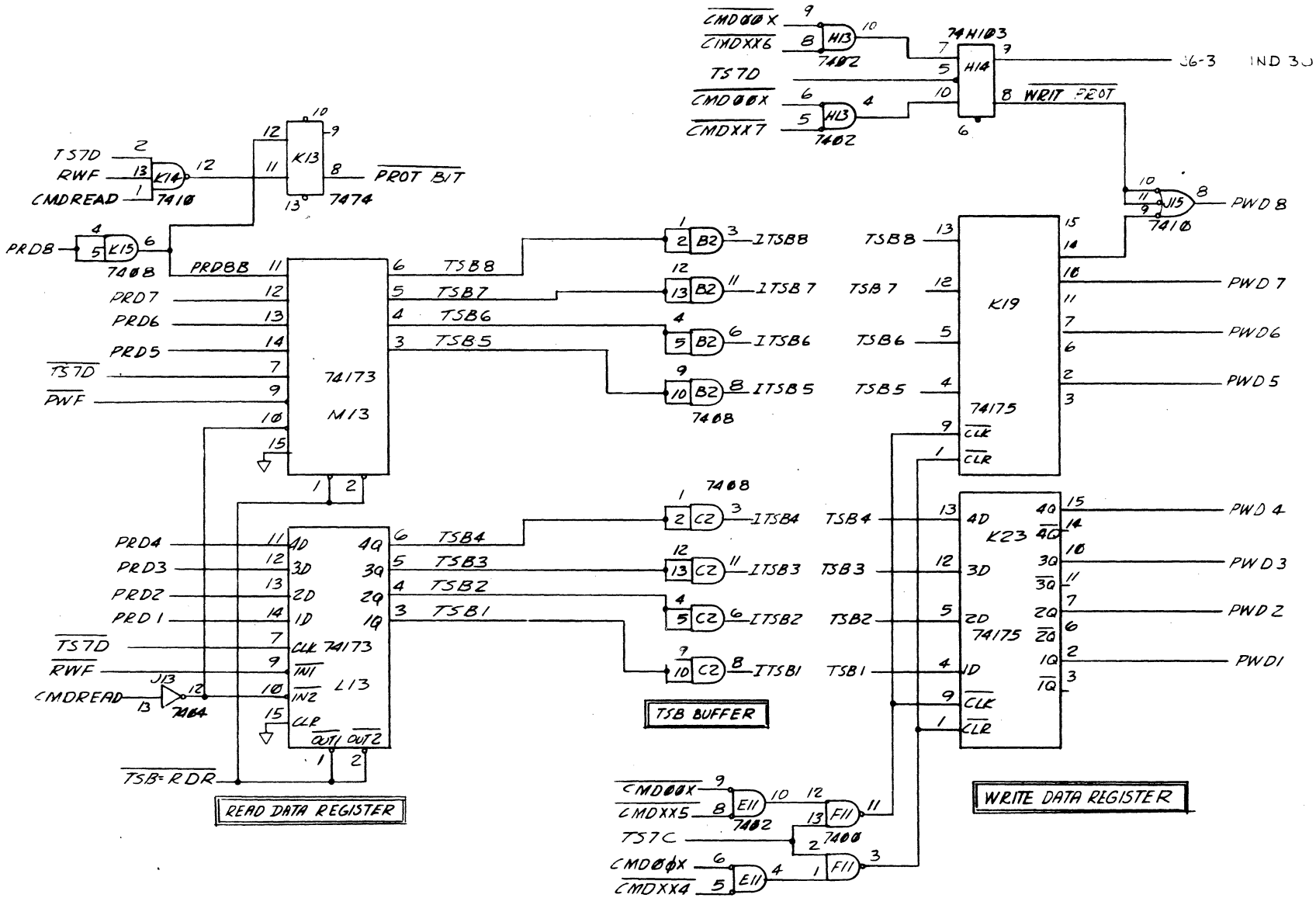

READ DATA REGISTER
WRITE DATA REGISTER
TSB BUFFER
74173
M13
L13
74175
K19
K23
PROT BIT
WRIT PROT
PWD 8
PWD 7
PWD6
PWD 5
PWD 4
PWD 3
PWD2
PWD1
TSB=RDR
CMDREAD
RWF
TS7D
PRDB
PRD7
PRD6
PRD5
PRD4
PRD3
PRDZ
PRD1
PWF
CMDXX6
CMDXX7
CMDXX5
CMDXX4
TS7C
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSBZ
TSB1
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSBZ
ITSB1
7408
7410
7474
7402
7400
7404
74H103
J6-3
IND 3

Figure 7-13

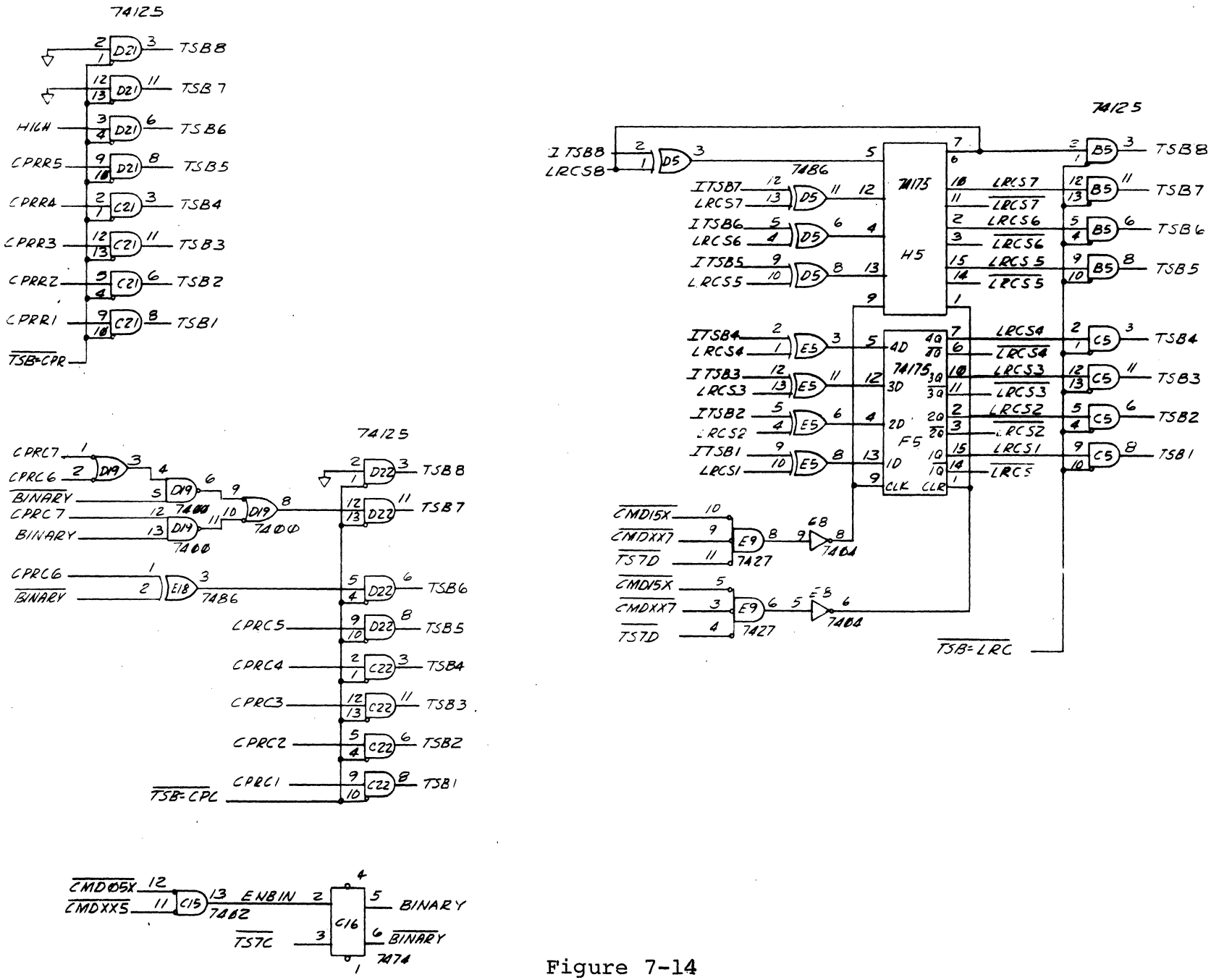

74125
TSB8
TSB7
HIGH
TSB6
CPRR5
TSB5
CPRR4
TSB4
CPRR3
TSB3
CPRR2
TSB2
CPRR1
TSB1
TSB=CPR
74125
CPRC7
CPRC6
BINARY
CPRC7
BINARY
7400
7400
7400
74125
TSB8
TSB7
CPRC6
BINARY
7486
TSB6
CPRC5
TSB5
CPRC4
TSB4
CPRC3
TSB3
CPRC2
TSB2
CPRC1
TSB1
TSB=CPC
CMD05X
CMDXX5
7402
ENBIN
BINARY
TS7C
BINARY
7474
I TSB8
LRCS8
7486
ITSB7
LRCS7
ITSB6
LRCS6
ITSB5
LRCS5
74175
H5
ITSB4
LRCS4
ITSB3
LRCS3
ITSB2
LRCS2
ITSB1
LRCS1
74175
F5
CMD15X
CMDXX7
TS7D
7427
7404
CMD15X
CMDXX7
TS7D
7427
7404
74125
LRCS7
LRCS6
LRCS5
LRCS4
LRCS3
LRCS2
LRCS1
LRCS
TSB=LRC
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1

Figure 7-14

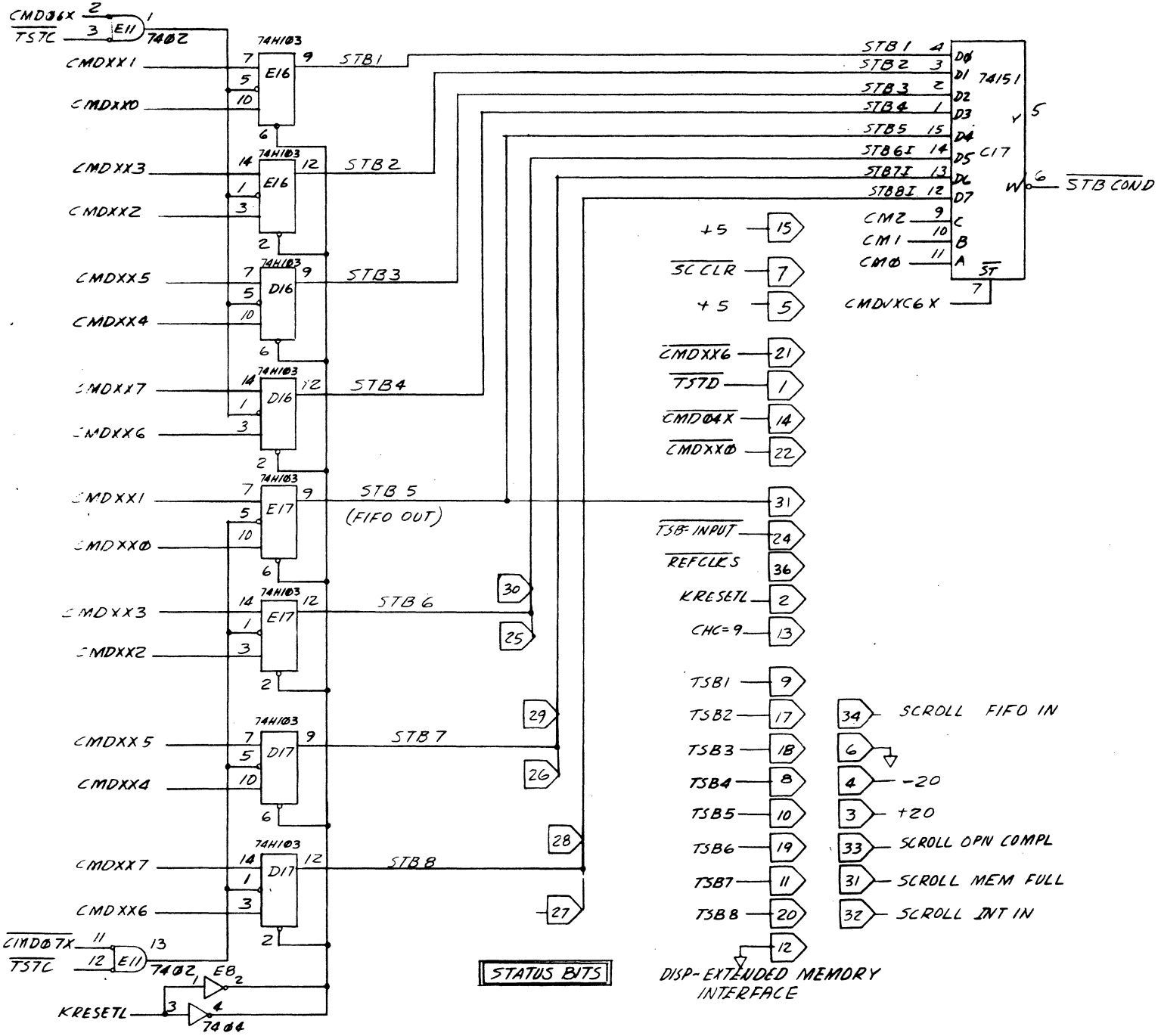

CMD06X
TST C
E11
74Ø2
74H1Ø3
E16
D16
E17
D17
CMDXX1
CMDXX0
CMDXX3
CMDXX2
CMDXX5
CMDXX4
CMDXX7
CMDXX6
STB1
STB2
STB3
STB4
STB 5
(FIFO OUT)
STB 6
STB 7
STB 8
CIMDØ7X
KRESETL
74Ø4
STATUS BITS
74151
C17
STB COND
CMDVXC6X
+5
SC CLR
CMDXX6
TSTD
CMDØ4X
CMDXXØ
TSB= INPUT
REFCLKS
CHC=9
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
TSB8
SCROLL FIFO IN
-20
+20
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
DISP-EXTENDED MEMORY INTERFACE

Figure 7-15

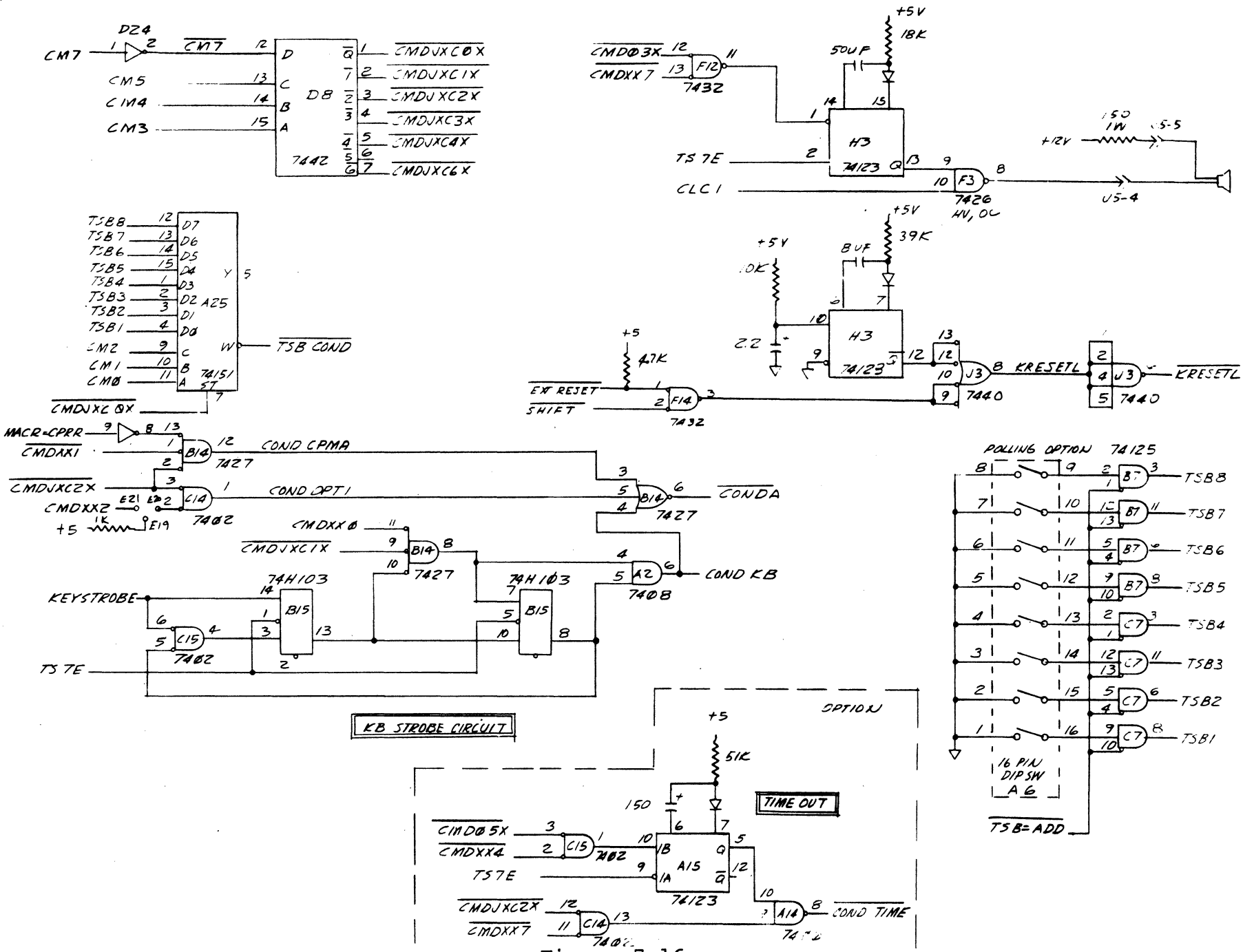

D24
CM7
CM5
CM4
CM3
D8
7442
CMDJXC0X
CMDJXC1X
CMDJXC2X
CMDJXC3X
CMDJXC4X
CMDJXC5X
CMDJXC6X
CMDØ3X
CMDXX7
7432
+5V
18K
50UF
H3
74123
TS7E
CLC1
F3
7426
HV, OC
150
1W
+12V
U5-5
U5-4
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
CM2
CM1
CM0
74151
A25
TSB COND
CMDJXC0X
39K
BUF
10K
22
4.7K
EXT RESET
SHIFT
F14
KRESETL
7440
MACR=CPRR
CMDAX1
CMDJXC2X
CMDXX2
E21
E19
1K
B14
7427
7402
COND CPMA
COND OPT1
CONDA
CMDXXØ
CMDJXC1X
74H103
B15
C15
KEYSTROKE
TS7E
A12
7408
COND KB
KB STROBE CIRCUIT
OPTION
51K
150
TIME OUT
CMDØ5X
CMDXX4
A15
CMDJXC2X
CMDXX7
A14
COND TIME
POLLING OPTION 74125
B7
C7
16 PIN DIP SW A6
TSB=ADD

Figure 7-16

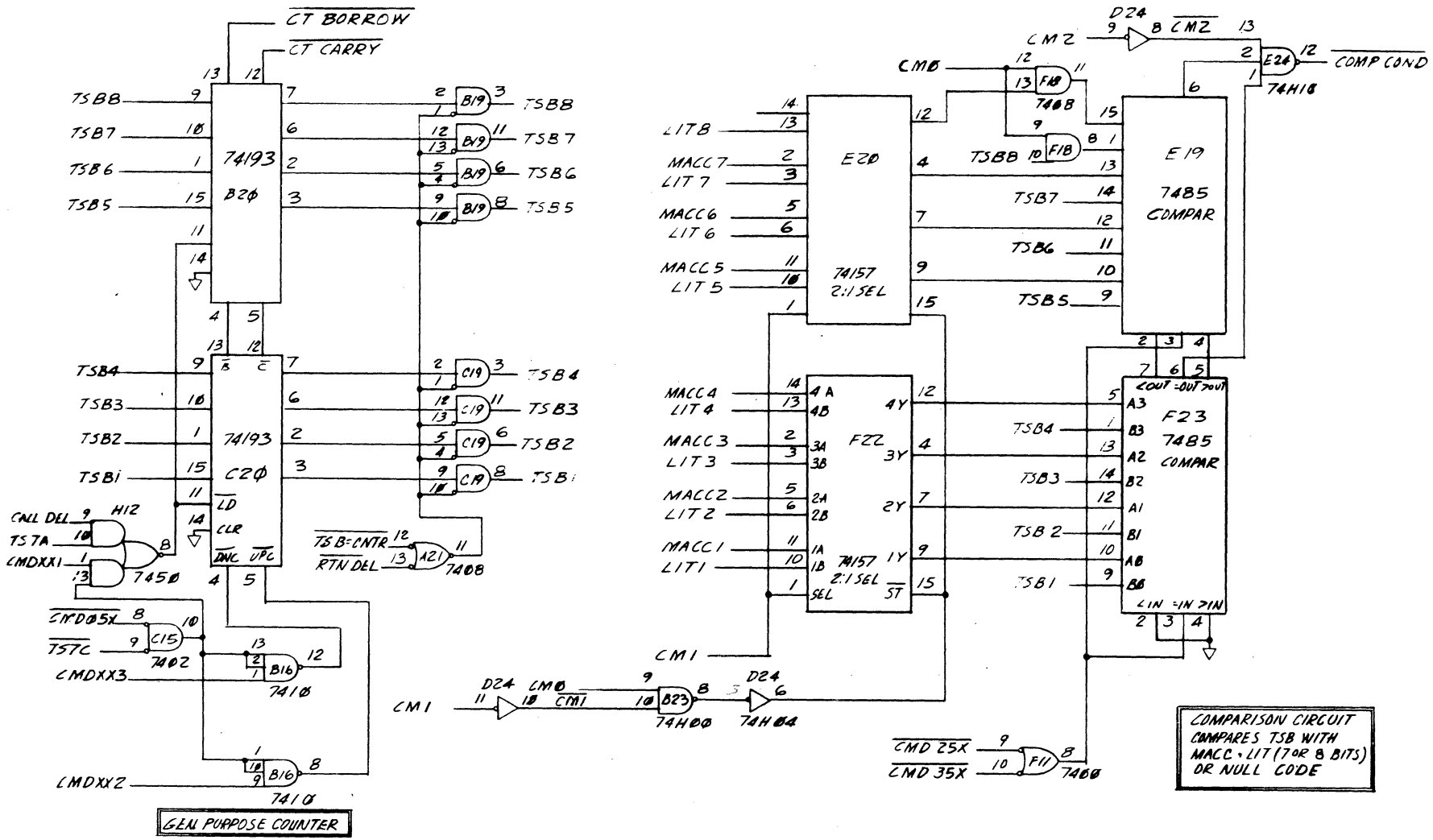

CT BORROW
CT CARRY
74193
B2Ø
C2Ø
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
LD
CLR
DNC
UPC
CALL DEL
TSTA
CMDXX1
H12
7450
CMDØ5X
TSTC
7402
CMDXX3
7410
CMDXX2
GEN PURPOSE COUNTER
TSB=CNTR
RTN DEL
7408
D24
CMØ
CMI
74HØØ
74H04
CM1
CM2
CMØ
CMD 25X
CMD 35X
7400
LITB
MACC7
LIT7
MACC6
LIT6
MACC5
LIT5
MACC4
LIT4
MACC3
LIT3
MACC2
LIT2
MACC1
LIT1
E2Ø
74157
2:1 SEL
F2Z
E19
7485
COMPAR
F23
COMP COND
74H10
COMPARISON CIRCUIT
COMPARES TSB WITH
MACC + LIT (7 OR 8 BITS)
OR NULL CODE

Figure 7-17

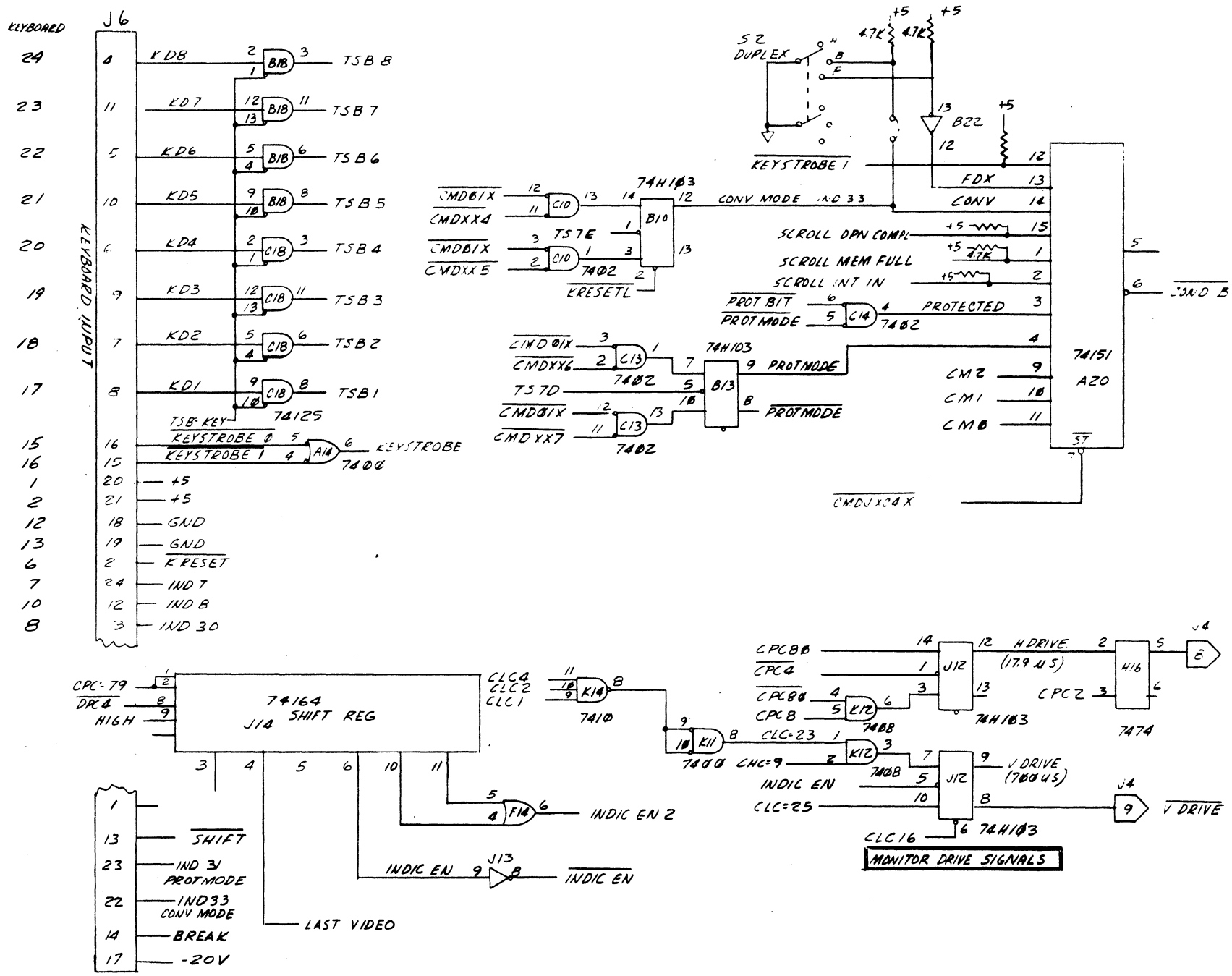

KEYBOARD
J6
KEYBOARD INPUT
KDB
KD7
KD6
KD5
KD4
KD3
KD2
KD1
TSB 8
TSB 7
TSB 6
TSB 5
TSB 4
TSB 3
TSB 2
TSB 1
74125
TSB KEY
KEYSTROBE Ø
KEYSTROBE 1
KEYSTROBE
74ØØ
+5
GND
KRESET
IND 7
IND 8
IND 30
SZ DUPLEX
4.7K
BZZ
KEYSTROBE 1
FDX
CONV
CONV MODE IND 33
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
PROT BIT
PROTMODE
PROTECTED
74Ø2
74H1Ø3
TS7E
TS7D
CMDXX4
CMDXX5
CMDXX6
CMDXX7
CMDØ1X
CMDØ2X
CMDØ3X
KRESETL
74151
A20
CM2
CM1
CM0
CMDJXC4X
IND B
CPC-79
DRC4
H16H
74164
J14 SHIFT REG
CLC4
CLC2
CLC1
7410
7400
7408
74H1Ø3
CPCBØ
CPC4
CPCB4
CPCB
CLC-23
CHC-9
INDIC EN
CLC-25
CLC16
H DRIVE
(17.9 µS)
CPC2
7474
V DRIVE
(700 µS)
MONITOR DRIVE SIGNALS
SHIFT
IND 31
PROTMODE
IND33
CONV MODE
BREAK
-20V
LAST VIDEO
INDIC EN 2
INDIC EN
J13
J4

Figure 7-18

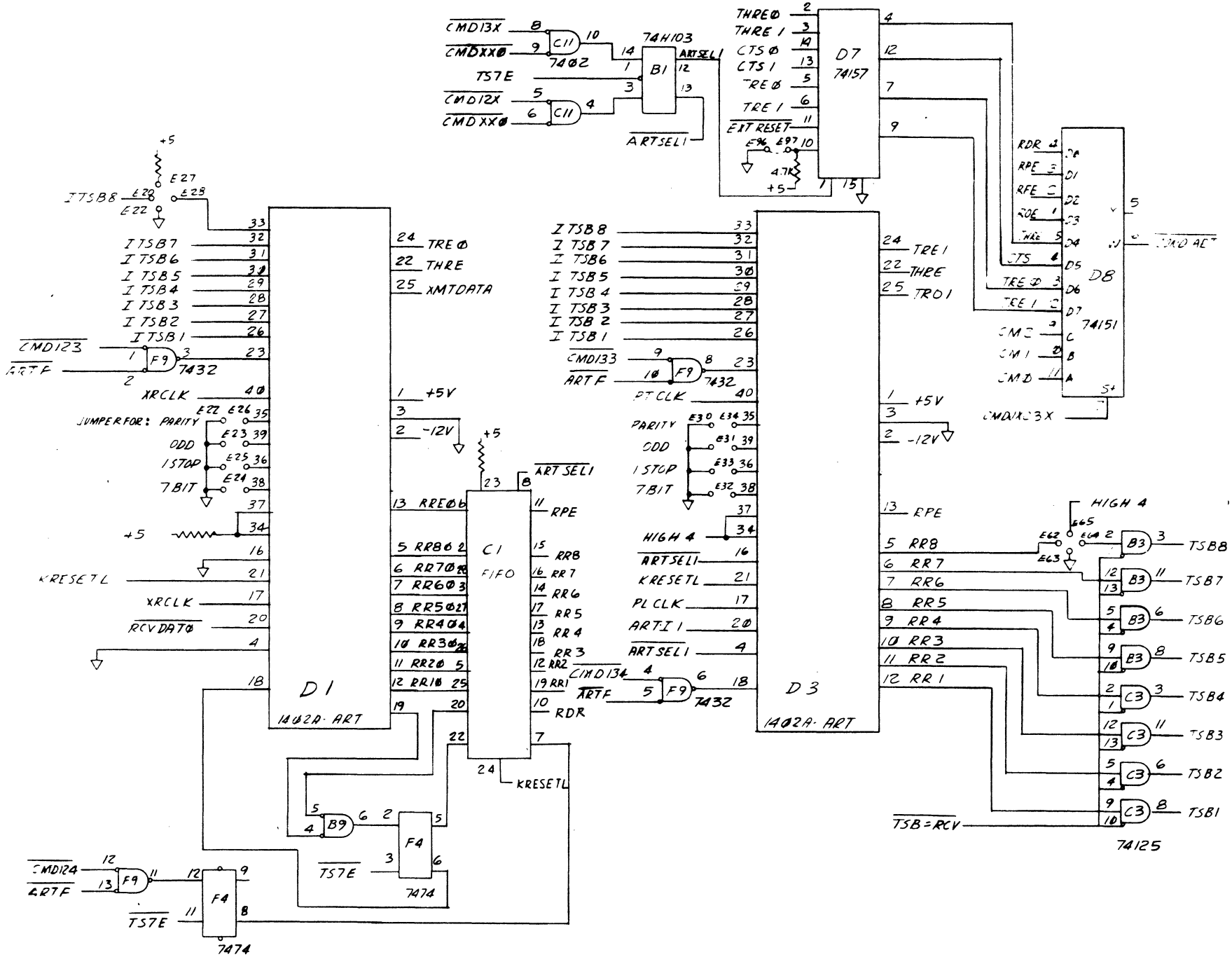

D1
1402A-ART
C1
FIFO
D3
1402A-ART
D7
74157
D8
74151
B1
74H103
C11
7402
F9
7432
B9
F4
7474
B3
C3
74125
CMD13X
CMDXX0
TST E
CMD12X
CMDXX0
ARTSEL1
THRE0
THRE 1
CTS0
CTS 1
TRE0
TRE 1
EXT RESET
4.7K
+5
RDR
RPE
RFE
ROE
THRE
CTS
TRE0
TRE 1
CMD
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
CMD123
ARTF
XRCLK
JUMPER FOR: PARITY
ODD
1STOP
7BIT
KRESETL
RCVDATA0
TRE0
THRE
XMTDATA
+5V
-12V
RRE0
RR80
RR70
RR60
RR50
RR40
RR30
RR20
RR10
RPE
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RDR
CMD134
CMD124
TSB=RCV
HIGH 4
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1

Figure 7-19

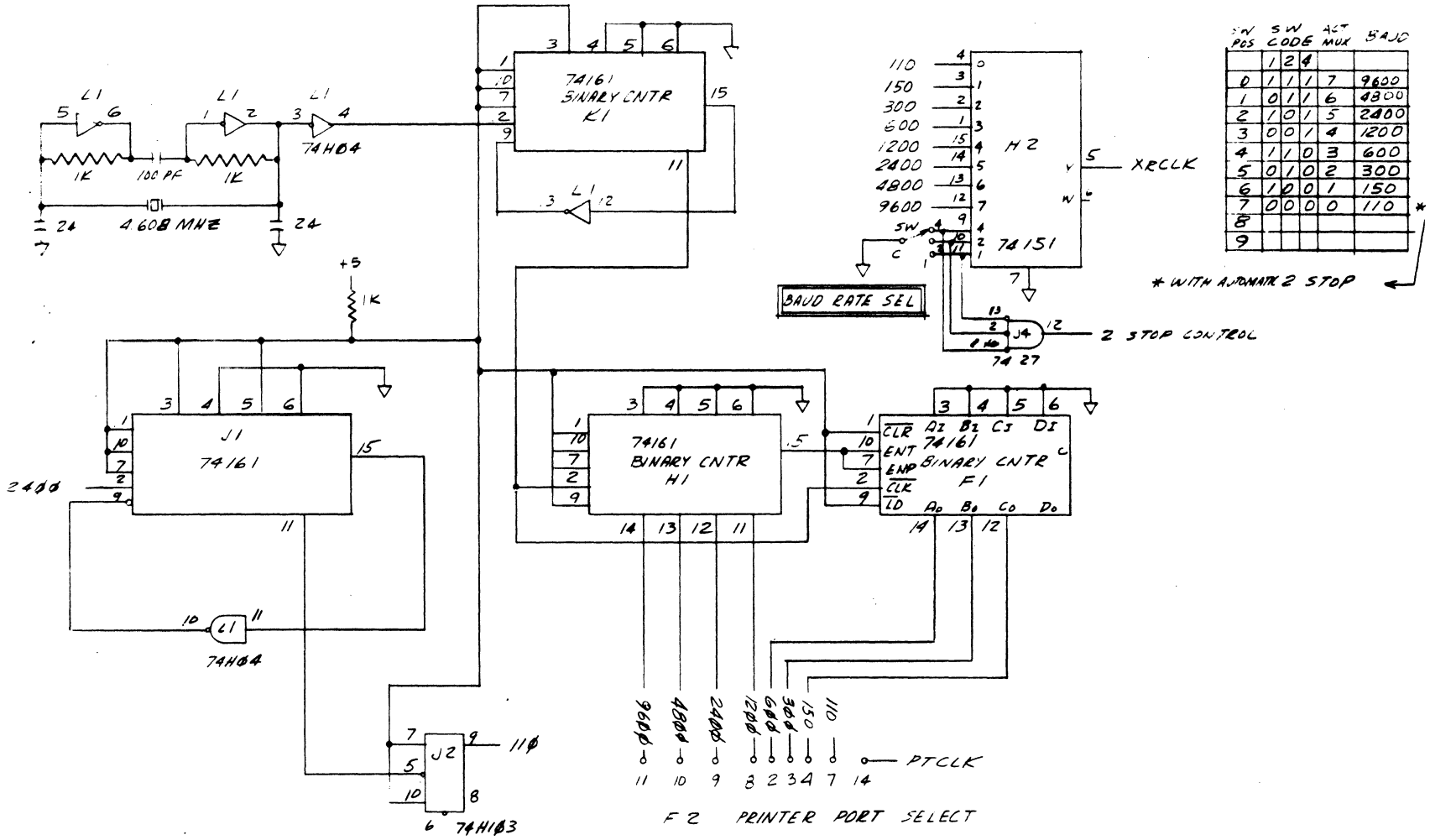
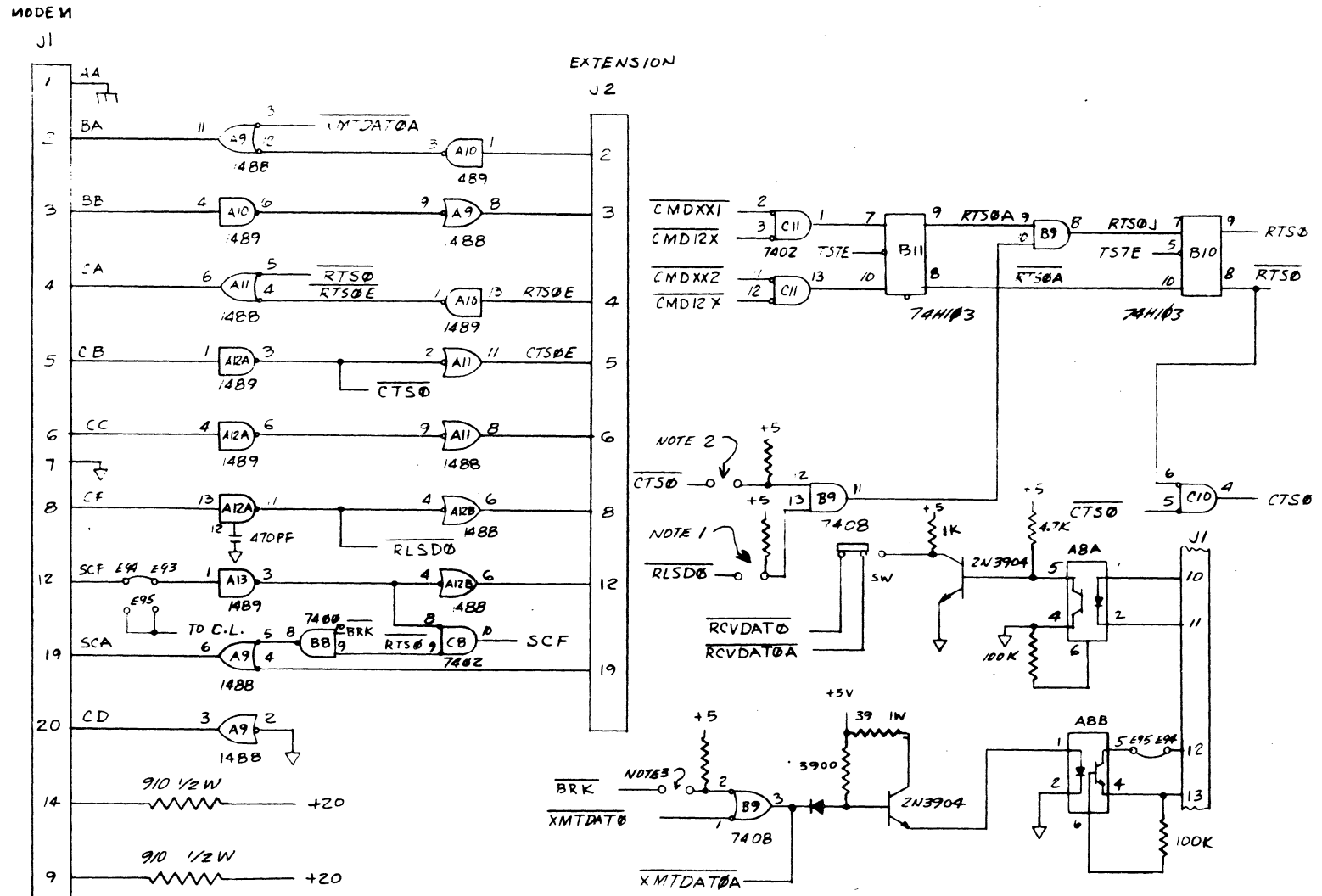

74161
BINARY CNTR
K1
74H04
1K
100 PF
1K
24
4.608 MHZ
24
+5
1K
J1
74161
2400
74161
BINARY CNTR
H1
74161
BINARY CNTR
F1
CLR A2 B2 C2 D2
ENT
ENP
CLK
LD A0 B0 C0 D0
74H04
J2
74H103
110
150
300
600
1200
2400
4800
9600
SW
M2
74151
XRCLK
BAUD RATE SEL
J4
74 27
2 STOP CONTROL
SW POS
SW CODE
ALT MUX
BAUD
* WITH AUTOMATIC 2 STOP
PTCLK
F2 PRINTER PORT SELECT

Figure 7-20



NOTES:

1. INSTALL JUMPER TO INHIBIT REQ TO SEND (CA) UNTIL RCVD LINE SIG DET(CF) FALLS- USED WITH 202 TYPE MODEM IN HALF DUPLEX MODE.
2. INSTALL JUMPER TO INHIBIT RTS(CA) UNTIL CTS='0' (CB)
3. INSTALL JUMPER FOR KEYBOARD BREAK SIGNAL

Figure 7-21

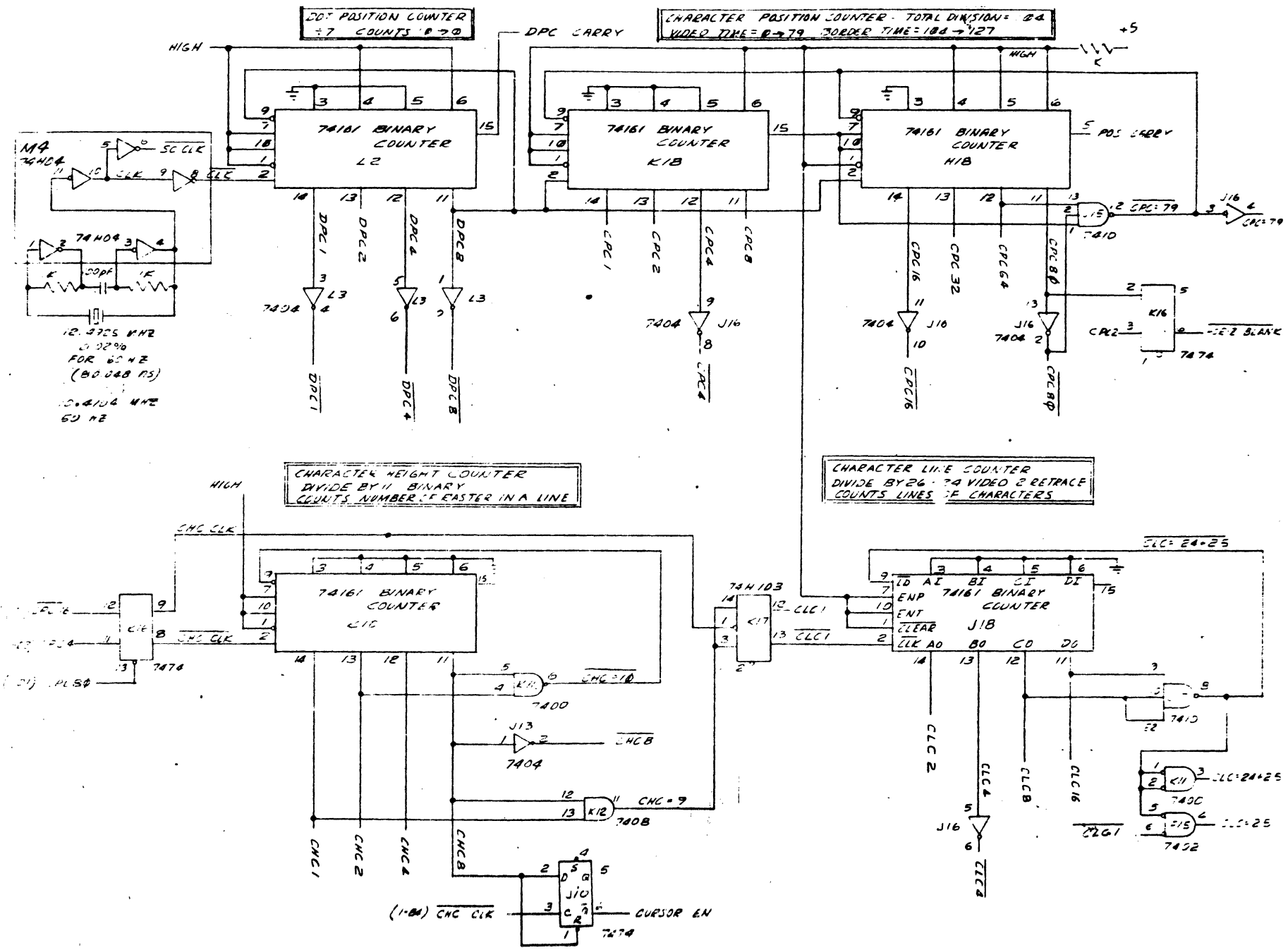

DOT POSITION COUNTER
÷7 COUNTS 0→0
DPC CARRY
CHARACTER POSITION COUNTER - TOTAL DIVISION = 84
VIDEO TIME = 0→79 BORDER TIME = 80→127
HIGH
+5
74161 BINARY COUNTER
L2
K18
H18
POS CARRY
M4
74H04
SC CLK
74H04
12.375 MHZ
0.02%
FOR 60 HZ
(80.808 NS)
10.4104 MHZ
60 HZ
DPC 1
DPC 2
DPC 4
DPC 8
CPC 1
CPC 2
CPC 4
CPC 8
CPC 16
CPC 32
CPC 64
CPC 80
7410
J16
CPC=79
7404
L3
K16
CPC2
SEE BLANK
7474
CHARACTER HEIGHT COUNTER
DIVIDE BY 11 BINARY
COUNTS NUMBER OF RASTER IN A LINE
CHARACTER LINE COUNTER
DIVIDE BY 26 - 24 VIDEO 2 RETRACE
COUNTS LINES OF CHARACTERS
CHC CLK
74161 BINARY COUNTER
J18
74H103
CLC 1
CLC 2
CLC 4
CLC 8
CLC 16
CLC 32
CLC=24+25
7400
7408
7402
J13
J10
CHC=10
CHC=9
CHC 1
CHC 2
CHC 4
CHC 8
CHCB
(1-8A) CHC CLK
CURSOR EN

Figure 7-22

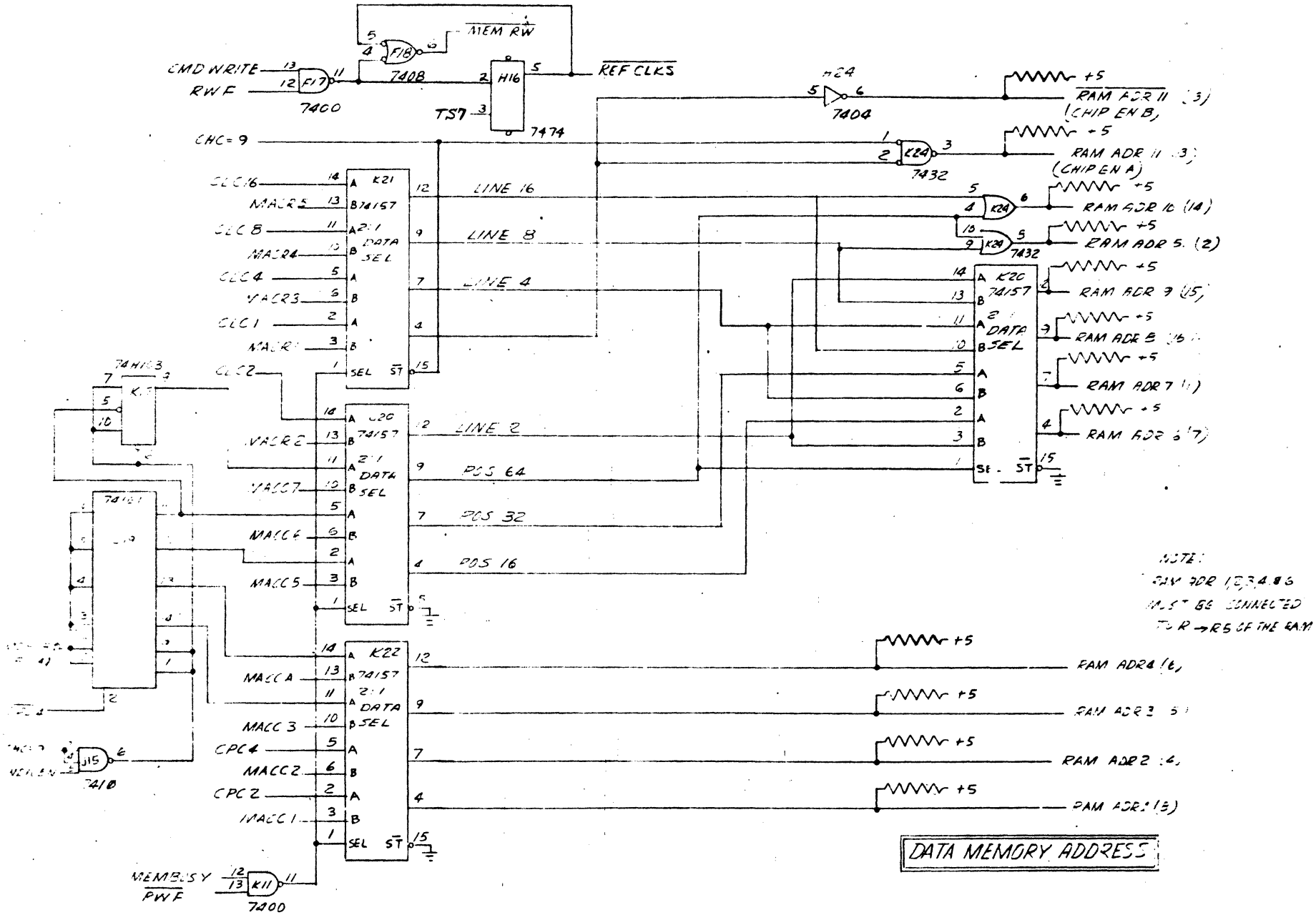
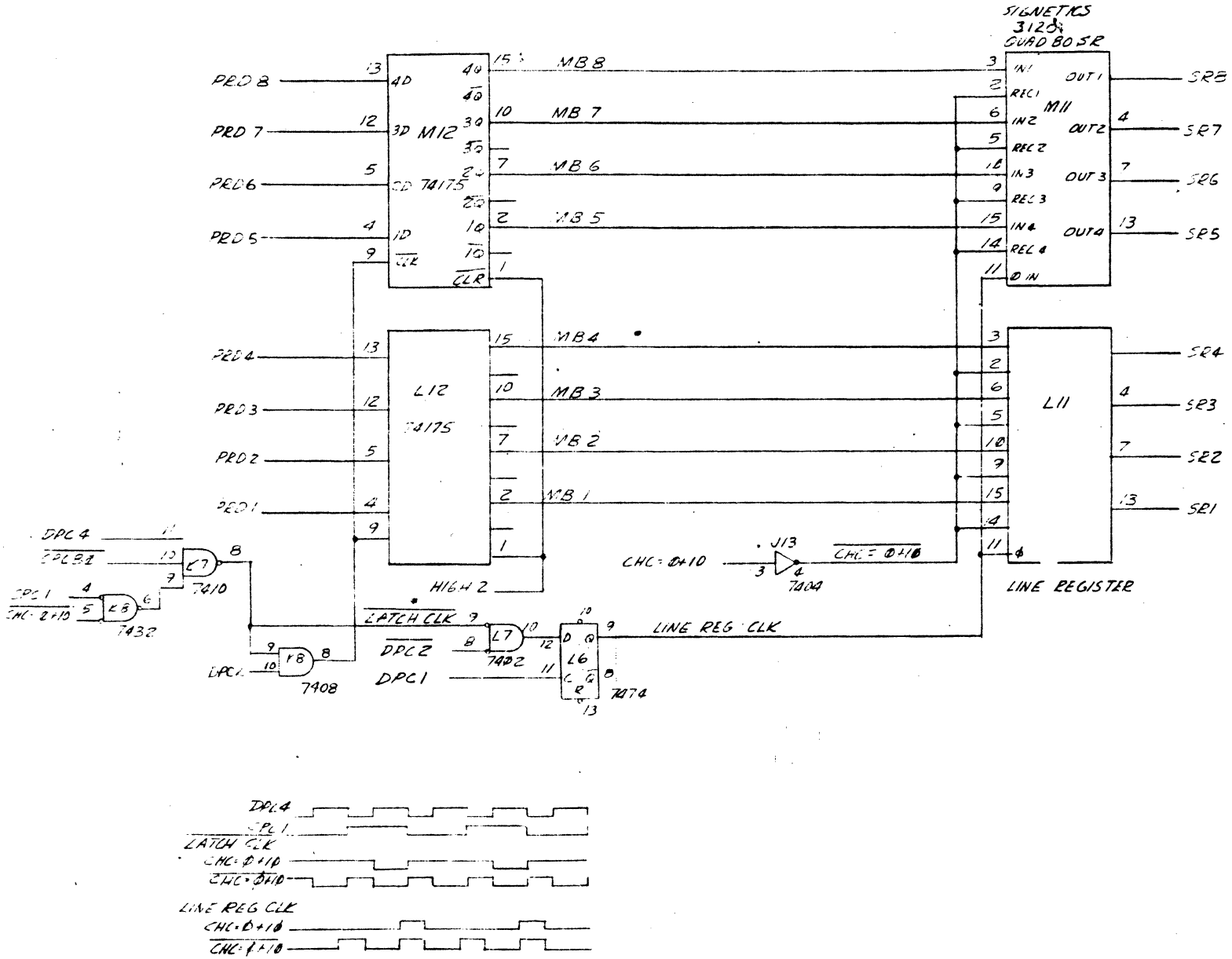

MEM RW
CMD WRITE
RWF
7400
7408
H16
7474
REF CLKS
TS7
CHC=9
LINE 16
LINE 8
LINE 4
LINE 2
POS 64
POS 32
POS 16
MACC7
MACC6
MACC5
MACC4
MACC3
MACC2
MACC1
CPC4
CPC2
CLC16
CLC8
CLC4
CLC2
CLC1
MACR5
MACR4
MACR3
MACR2
MACR1
K21
K20
K22
74157
2:1 DATA SEL
74H183
7410
7404
7432
MEMBUSY
PWF
7400
RAM ADR 11 (3) (CHIP EN B)
RAM ADR 11 (3) (CHIP EN A)
RAM ADR 10 (14)
RAM ADR 5 (2)
RAM ADR 9 (15)
RAM ADR 8 (1)
RAM ADR 7 (4)
RAM ADR 6 (7)
RAM ADR4 (6)
RAM ADR3 (5)
RAM ADR2 (4)
RAM ADR1 (3)
+5
DATA MEMORY ADDRESS

Figure 7-23

16 EA. 2102 RAM
PWD8
PWD7
PWD6
PWD5
PWD4
PWD3
PWD2
PWD1
RAM ADR11
MEM RW
+5V
RAM ADR 1->10 & A11 MNEMONICS
L22
L21
L20
L19
L18
L17
L16
L15
M22
M21
M20
M19
M18
M17
M16
M15
7406
PRD1
PRD2
PRD3
PRD4
PRD5
PRD6
PRD7
PRD8
REFRESH MEMORY

Figure 7-25


SIGNETICS
3120
QUAD BOSR
M11
M12
L12
L11
74175
PRD 8
PRD 7
PRD 6
PRD 5
PRD 4
PRD 3
PRD 2
PRD 1
MB 8
MB 7
MB 6
MB 5
MB 4
MB 3
MB 2
MB 1
SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
HIGH 2
LATCH CLK
LINE REG CLK
LINE REGISTER
DPC 4
DPC 1
DPC2
DPC1
CHC=0+10
CHC=0+10
J13
7410
7432
7408
7402
7404
7474

DPC4
DPC 1
LATCH CLK
CHC=0+10
CHC=0+10
LINE REG CLK
CHC=0+10
CHC=0+10

Figure 7-26

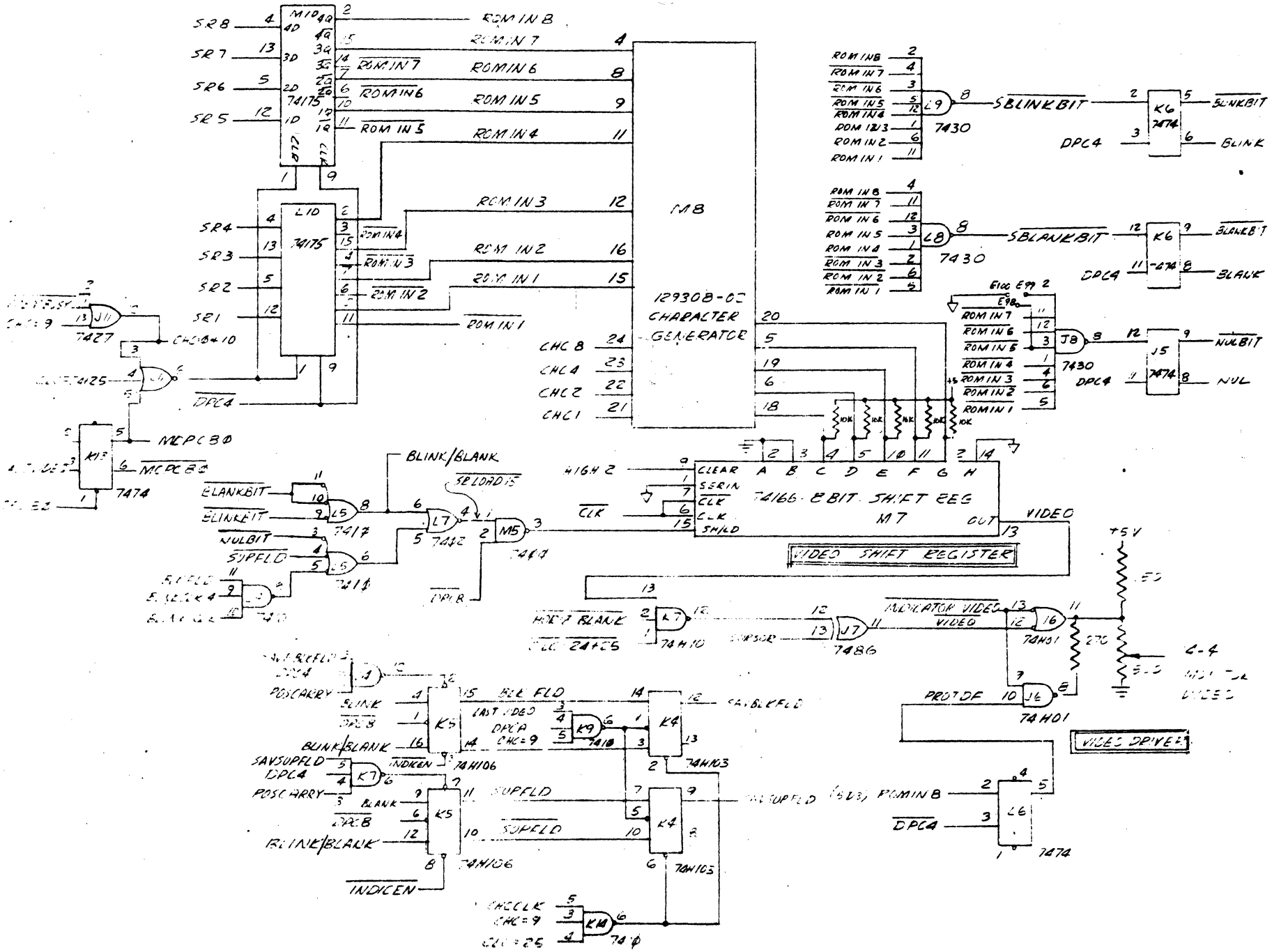

M8
12930B-02
CHARACTER
GENERATOR
74175
7430
7474
7427
7417
74166 8 BIT SHIFT REG
VIDEO SHIFT REGISTER
VIDEO
ROMIN8
ROMIN7
ROMIN6
ROMIN5
ROMIN4
ROMIN3
ROMIN2
ROMIN1
SR8
SR7
SR6
SR5
SR4
SR3
SR2
SR1
SBLINKBIT
SBLANKBIT
BLINKBIT
BLANKBIT
NULBIT
BLINK
BLANK
NUL
DPC4
BLINK/BLANK
SRLOAD15
CLK
MCPCB0
MCPCB8
ELANKBIT
ELINKBIT
NULBIT
SUPFLD
INDICEN
PROTDF
INDICATOR VIDEO
+5V
270

Figure 7-27

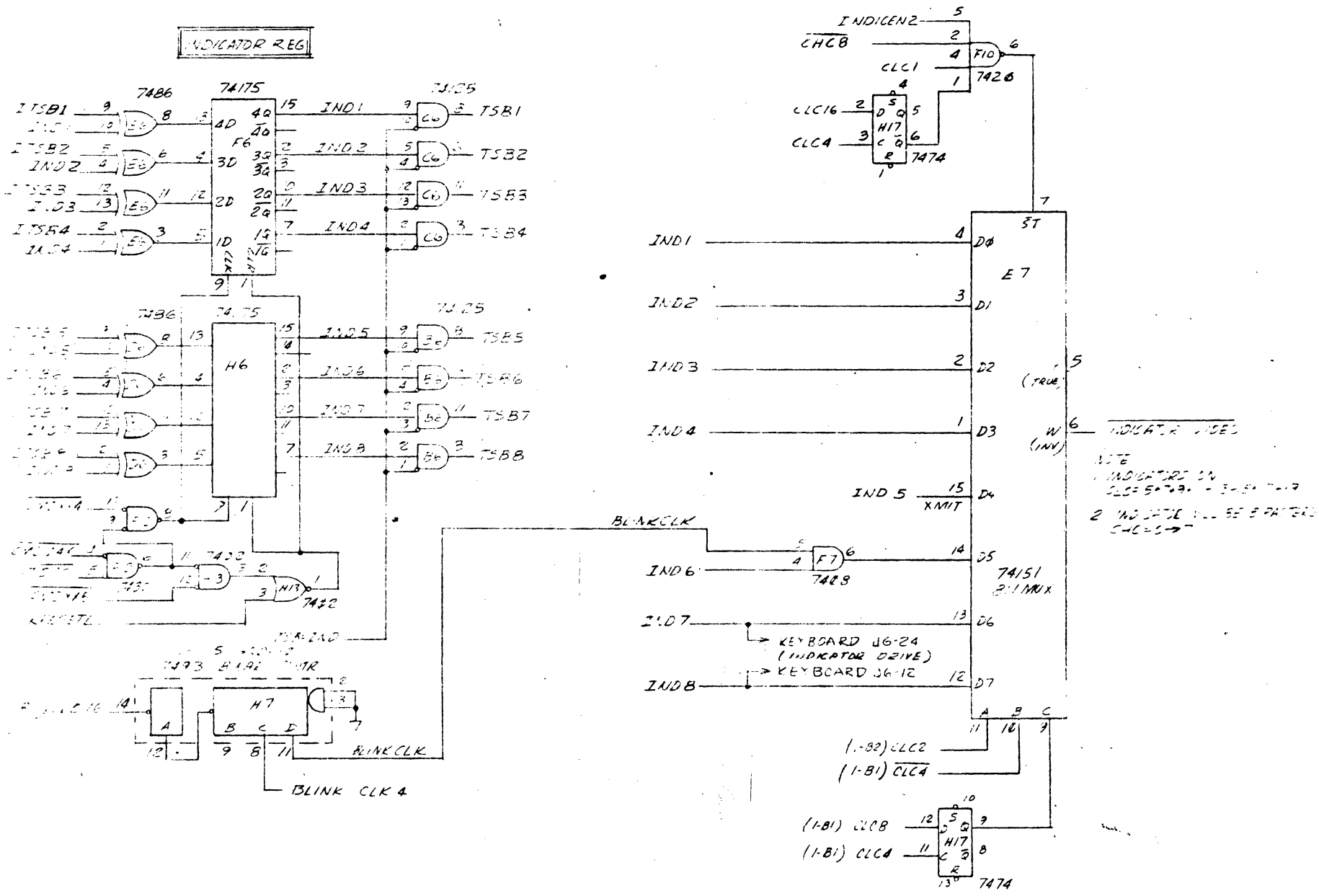

INDICATOR REG
7486
74175
F6
IND1
IND2
IND3
IND4
TSB1
TSB2
TSB3
TSB4
H6
IND5
IND6
IND7
IND8
TSB5
TSB6
TSB7
TSB8
7432
7402
H7
BLINKCLK
BLINK CLK 4
INDICEN2
CHCB
CLC1
CLC16
CLC4
F10
7426
H17
7474
E7
74151
8:1 MUX
IND 5
XMIT
F7
7408
KEYBOARD J6-24
(INDICATOR DRIVE)
KEYBOARD J6-12
(1-B2) CLC2
(1-B1) CLC4
(1-B1) CLC8
(TRUE)
(INV)

Figure 7-28

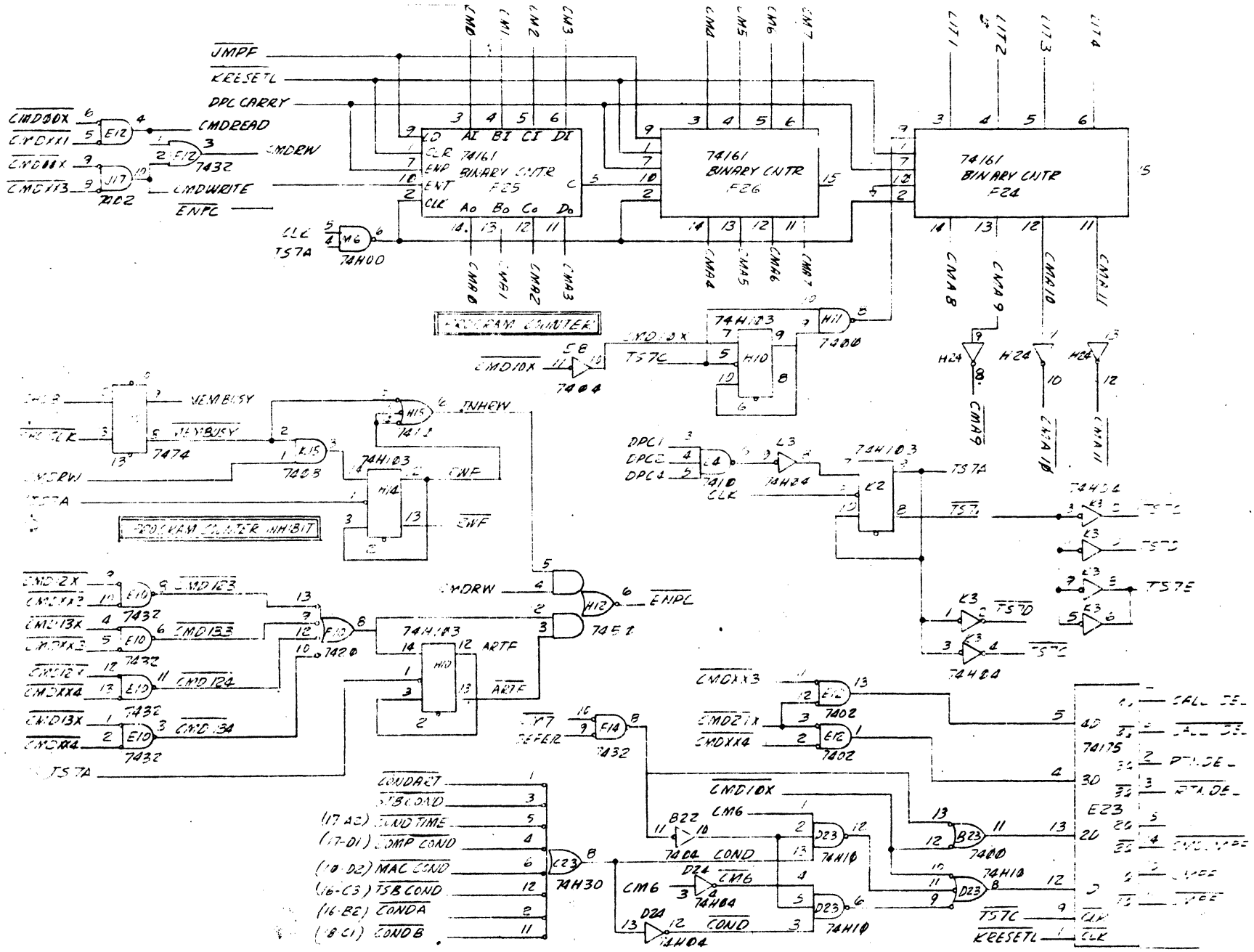
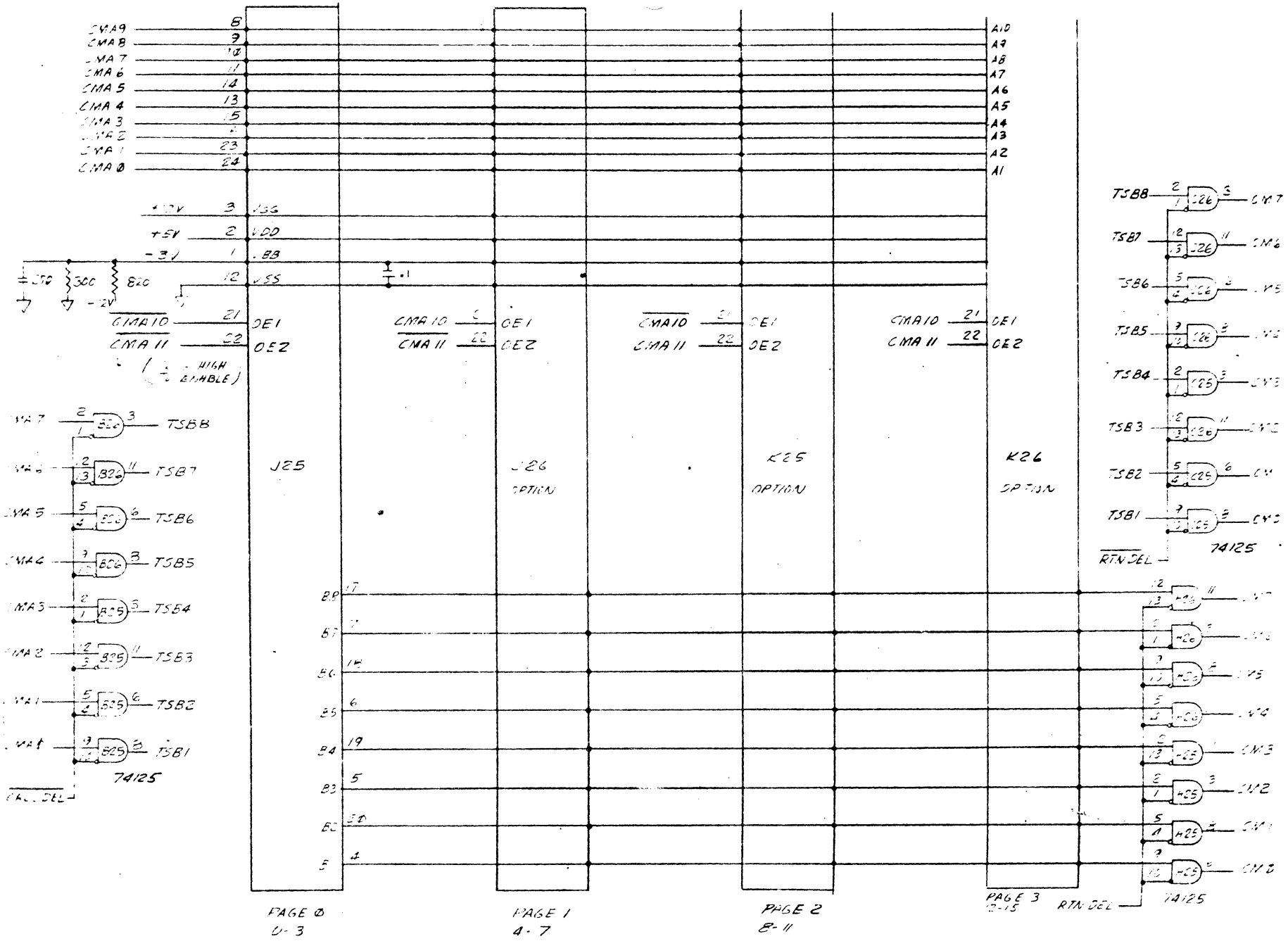

JMPF
KEESETL
DPC CARRY
CMDBOX
CMDXX1
CMDBOOX
CMDXX3
CMDBOOX
CMDXX3
CMDBEAD
CMDRW
CMDWRITE
ENPC
7432
7402
74161 BINARY CNTR F25
74161 BINARY CNTR F26
74161 BINARY CNTR F24
CLC
TS7A
74H00
PROGRAM COUNTER
74H103
7400
CMD10X
TS7C
7404
PROGRAM COUNTER INHIBIT
MEMBUSY
74H74
INHBUSY
INHFW
7408
74H15
74H03
CWF
DPC1
DPC2
DPC4
7410
74H24
74H08
TS7A
TS7
TS7D
TS7E
TS7C
CMDRW
ENPC
7451
CMD12X
CMDXX3
CMD123
CMD13X
CMDXX3
CMD133
CMD12X
CMDXX4
CMD124
CMD13X
CMDXX4
CMD134
7420
74H03
ARTF
DEFER
CMDXX3
CMDZ7X
CMDXX4
74175
CALL DE-
PTR DE-
CMD LOAD
LOAD
CLK
COUDACT
STBCOND
(17 A2) COND TIME
(17-D1) COMP COND
(10-D2) MAC COND
(16-C3) TSB COND
(16-B2) CONDA
(18 C1) CONDB
74H30
B22
B23
D23
D24
74H10
74H04
COND
CMD10X
CMD6
TS7C
KEESETL
CLK

Figure 7-29



MOTOROLA MCM 6560L - OPTIONA (1024 X 8) ROM

Figure 7-30

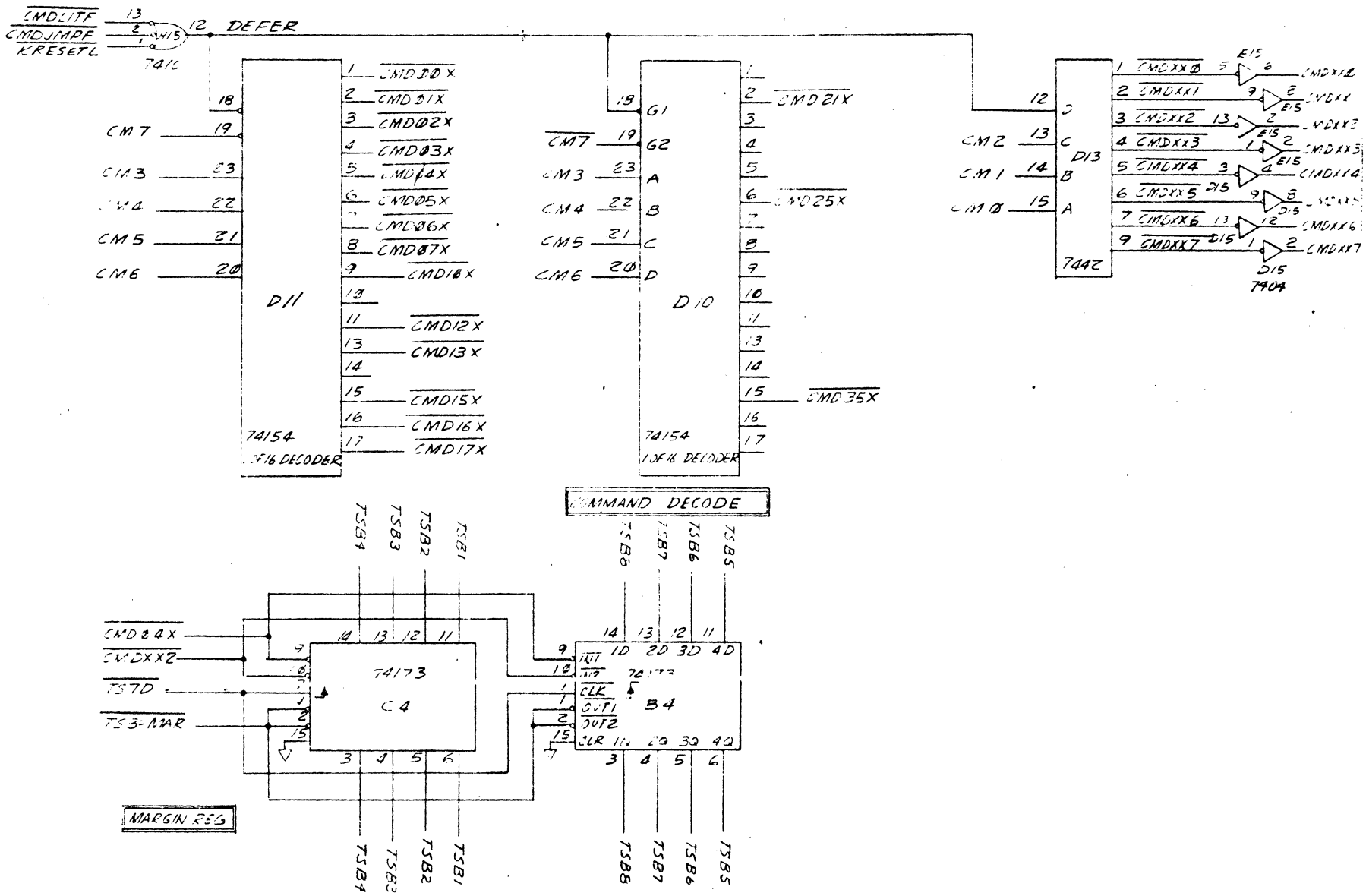

CMDLITF
CMDJMPF
KRESETL
DEFER
74LS15
74LS
D11
D10
D13
74154
1 OF 16 DECODER
7442
CM7
CM3
CM4
CM5
CM6
CM2
CM1
CM0
CMD00X
CMD01X
CMD02X
CMD03X
CMD04X
CMD05X
CMD06X
CMD07X
CMD10X
CMD12X
CMD13X
CMD15X
CMD16X
CMD17X
CMD21X
CMD25X
CMD35X
CMDXX0
CMDXX1
CMDXX2
CMDXX3
CMDXX4
CMDXX5
CMDXX6
CMDXX7
COMMAND DECODE
TSB4
TSB3
TSB2
TSB1
TSB8
TSB7
TSB6
TSB5
CMD24X
CMDXX2
TS7D
TS3-MAR
74173
C4
B4
MARGIN REG

Figure 7-31

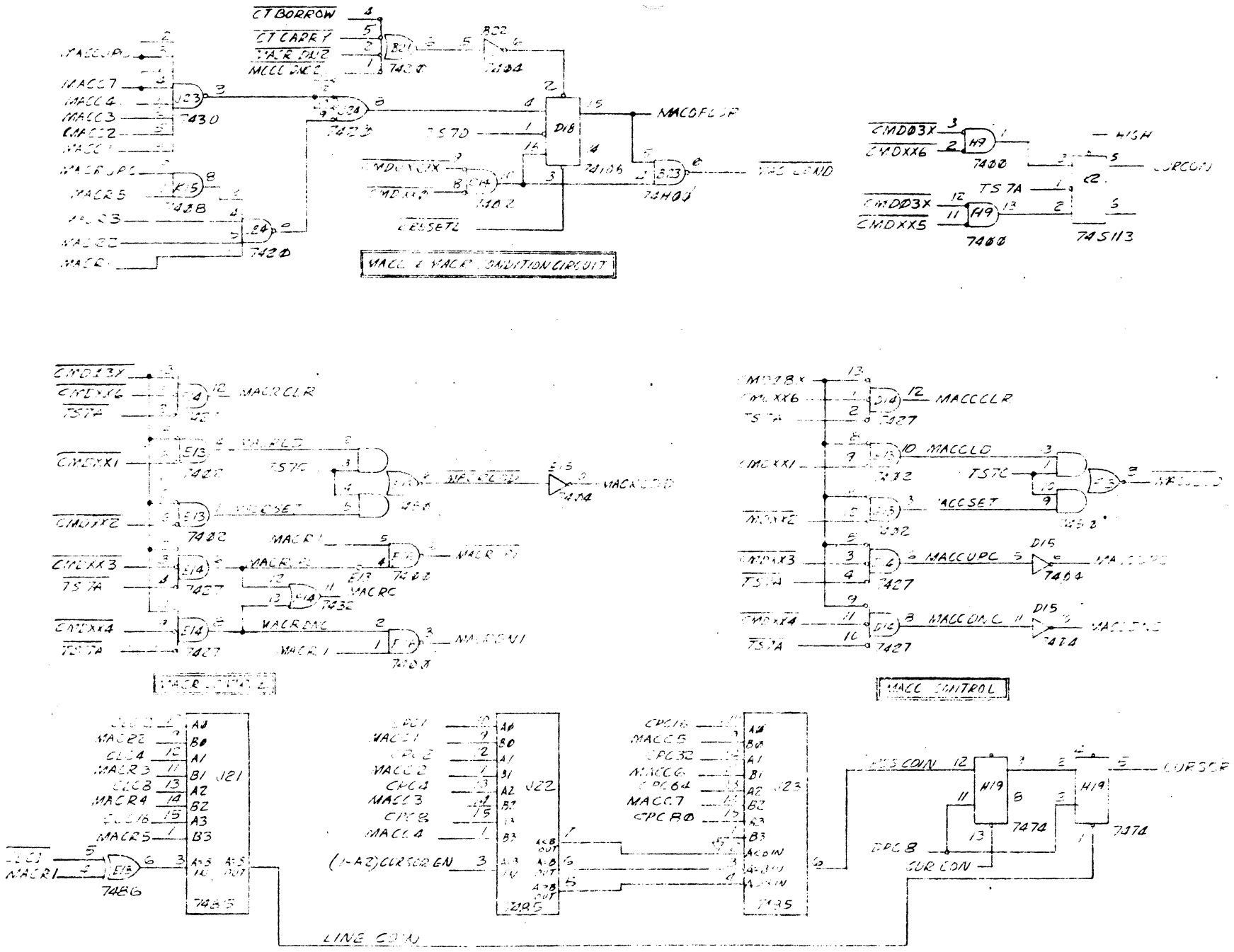

CT BORROW
CT CARRY
MACR OVF
MACC OVF
MACC7
MACC4
MACC3
MACC2
MACR7
MACR4
MACR3
MACR2
MACR1
MACR0
MACC & MACR VALIDATION CIRCUIT
CMD03X
CMDXX6
CMDXX5
HIGH
CURCON
TS7A
CMDXX1
CMDXX2
CMDXX3
CMDXX4
TS7C
TS7B
MACRCLR
MACCCLR
MACCLD
MACCSET
MACCUPC
MACCDAC
MACR CONTROL
MACC CONTROL
CURSCON
CPC8
LINE CONN

Figure 7-32

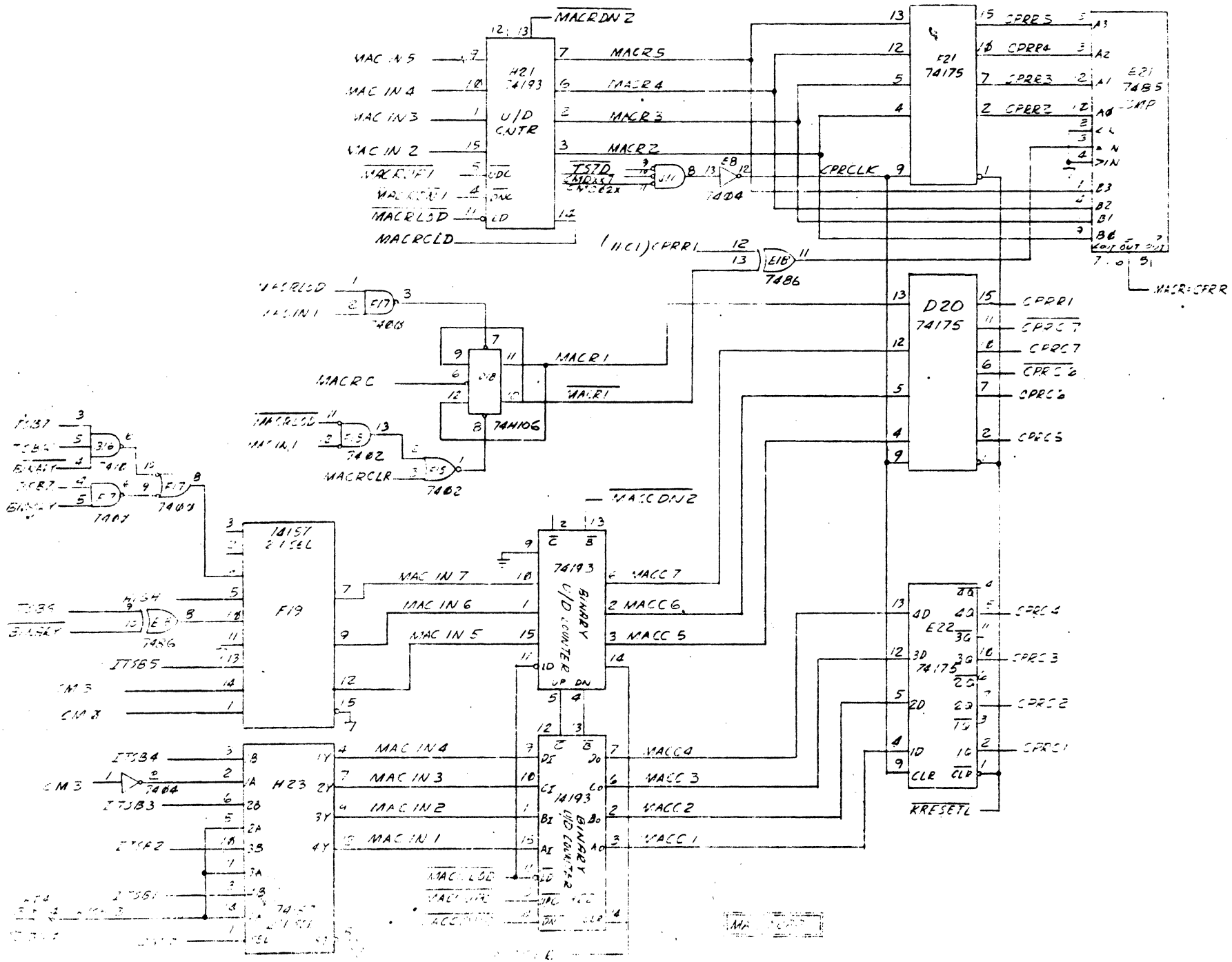

MACRDN2
MAC IN 5
MAC IN 4
MAC IN 3
MAC IN 2
MACRCNT1
MACRCNT0
MACRLOD
MACRCLD
U/D CNTR
MACR5
MACR4
MACR3
MACR2
MACR1
MACR0
CPRCLK
CPRR5
CPRR4
CPRR3
CPRR2
CPRR1
CPRC7
CPRC6
CPRC5
CPRC4
CPRC3
CPRC2
CPRC1
MACR=CPRR
MACRCLR
MACCDN2
MAC IN 7
MAC IN 6
MAC IN 5
MAC IN 4
MAC IN 3
MAC IN 2
MAC IN 1
MACC7
MACC6
MACC5
MACC4
MACC3
MACC2
MACC1
BINARY U/D COUNTER
KRESETL

Figure 7-33

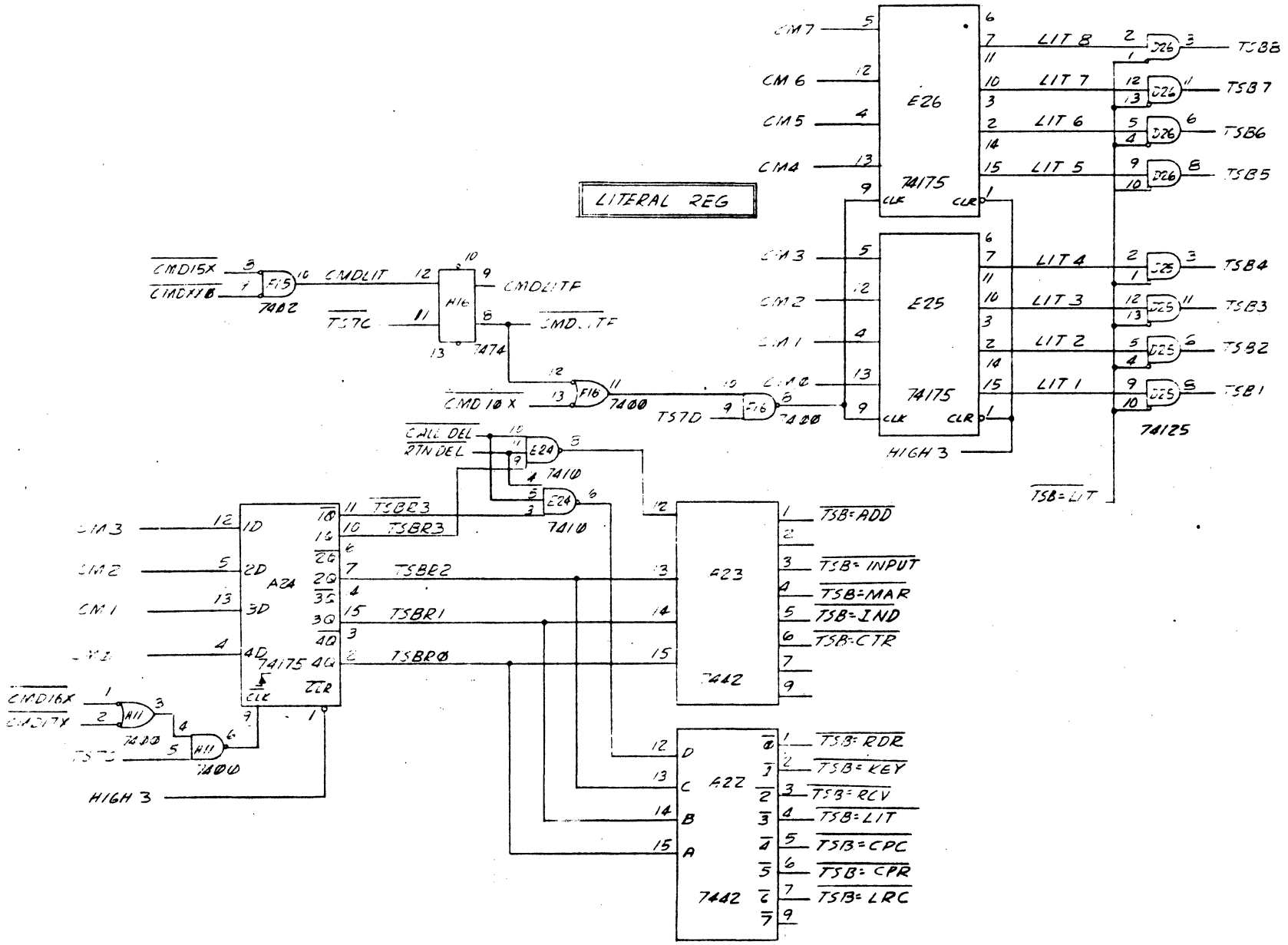


Figure 7-34 TSB SOURCE DECODE

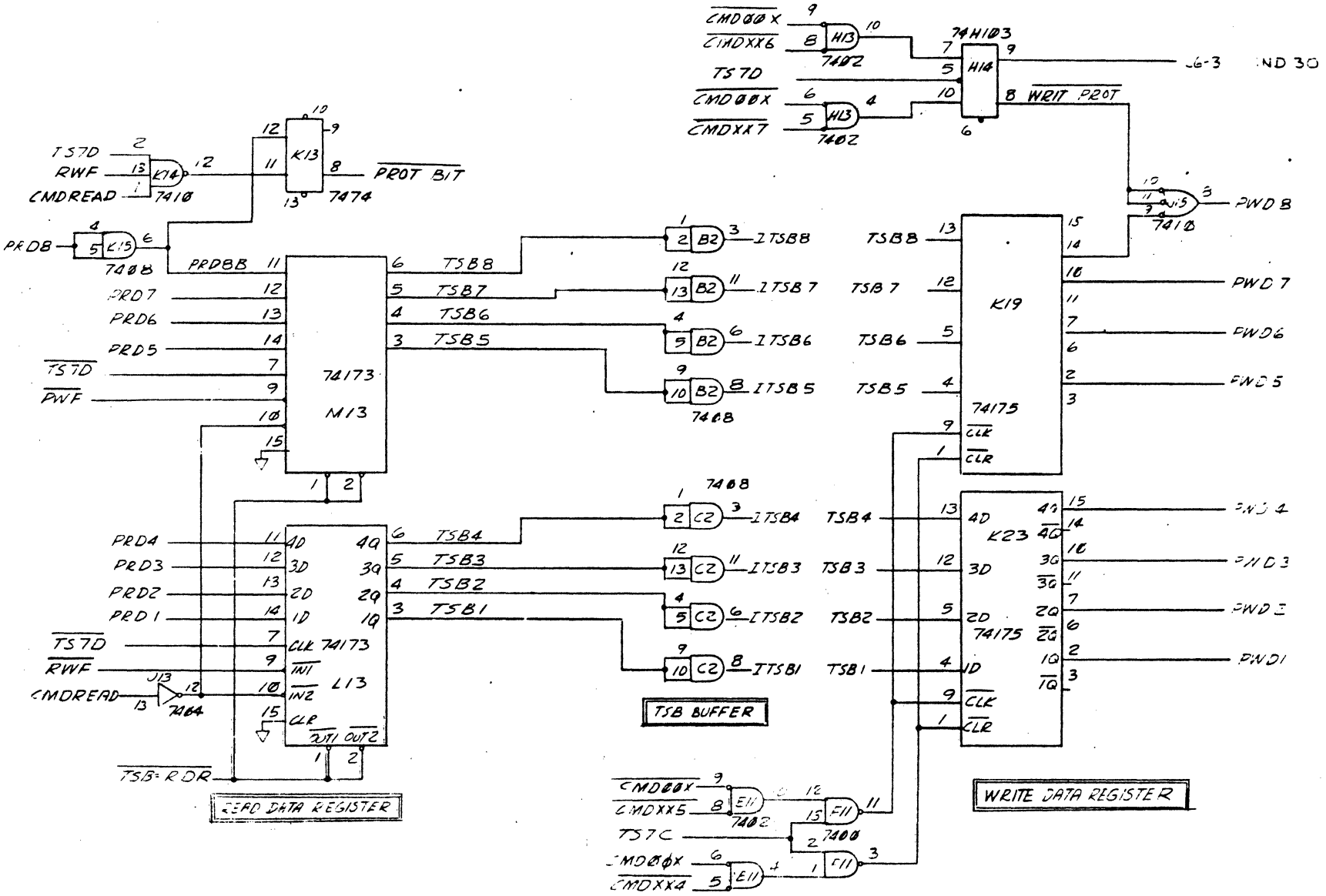

TS7D
RWF
CMDREAD
7410
PROT BIT
7474
PRD8
7408
PRD7
PRD6
PRD5
PRD4
PRD3
PRD2
PRD1
74173
M13
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
7408
ITSB8
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
TSB BUFFER
L13
7404
TSB-RDR
READ DATA REGISTER
CMDXX6
7402
WRIT PROT
PWD 8
PWD 7
PWD6
PWD 5
PWD 4
PWD 3
PWD 2
PWD1
K19
74175
K23
WRITE DATA REGISTER
CMDXX5
TS7C
CMDXX4
7400

Figure 7-35

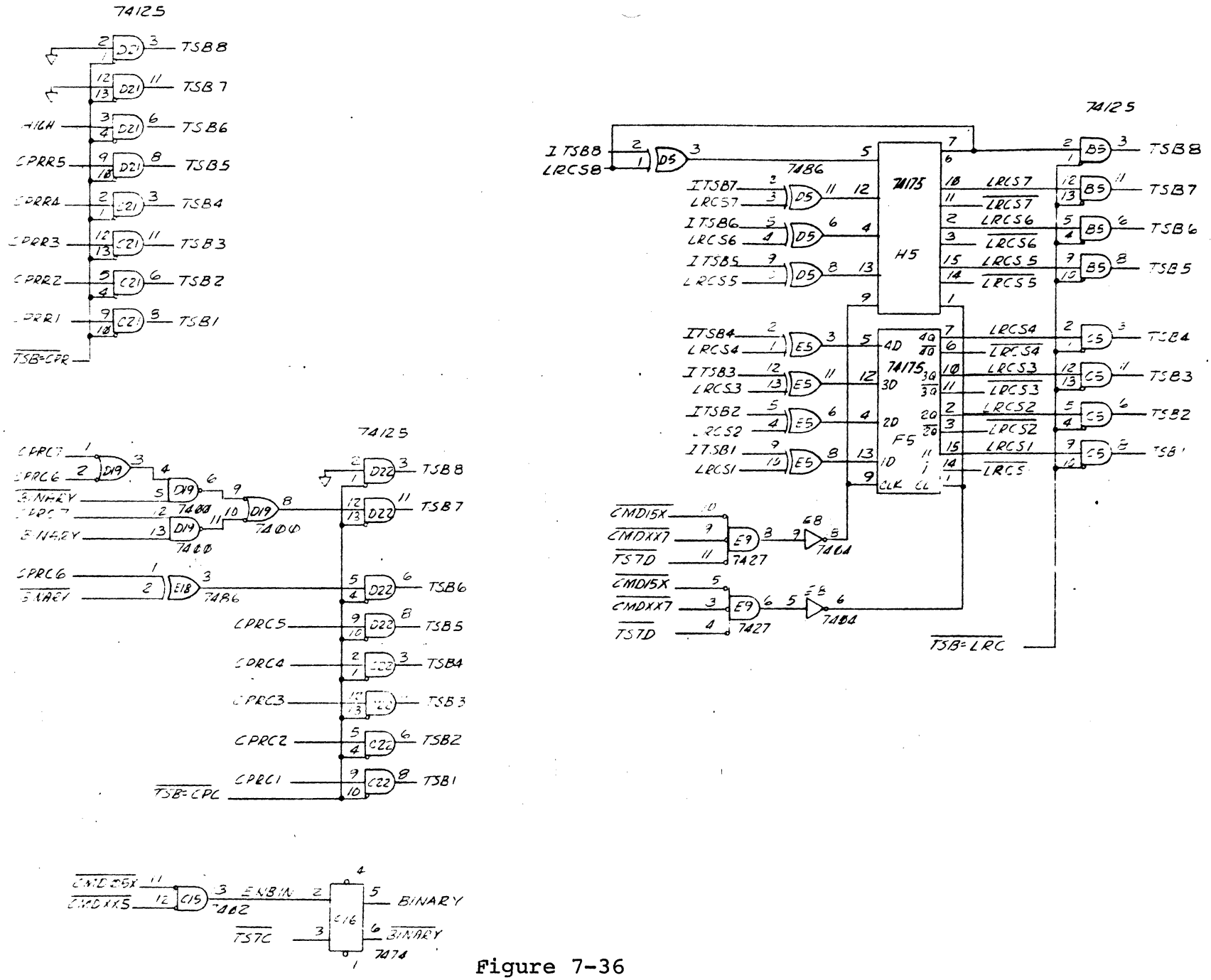

74125
TSB8
TSB7
HIGH
TSB6
CPRR5
TSB5
CPRR4
TSB4
CPRR3
TSB3
CPRR2
TSB2
CPRR1
TSB1
TSB=CPR
74125
CPRC7
CPRC6
BINARY
CPRC7
BINARY
7400
7400
7400
CPRC6
BINARY
7486
74125
TSB8
TSB7
TSB6
CPRC5
TSB5
CPRC4
TSB4
CPRC3
TSB3
CPRC2
TSB2
CPRC1
TSB1
TSB=CPC
CMDI5X
CMDXX5
7402
ENBIN
BINARY
TS7C
BINARY
7474
74125
ITSB8
LRCS8
7486
ITSB7
LRCS7
ITSB6
LRCS6
ITSB5
LRCS5
74175
H5
ITSB4
LRCS4
ITSB3
LRCS3
ITSB2
LRCS2
ITSB1
LRCS1
74175
F5
CLK
LRCS7
LRCS7
LRCS6
LRCS6
LRCS5
LRCS5
LRCS4
LRCS4
LRCS3
LRCS3
LRCS2
LRCS2
LRCS1
LRCS
74125
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
CMDI5X
CMDXX7
TS7D
7427
7404
CMDI5X
CMDXX7
TS7D
7427
7404
TSB=LRC

Figure 7-36

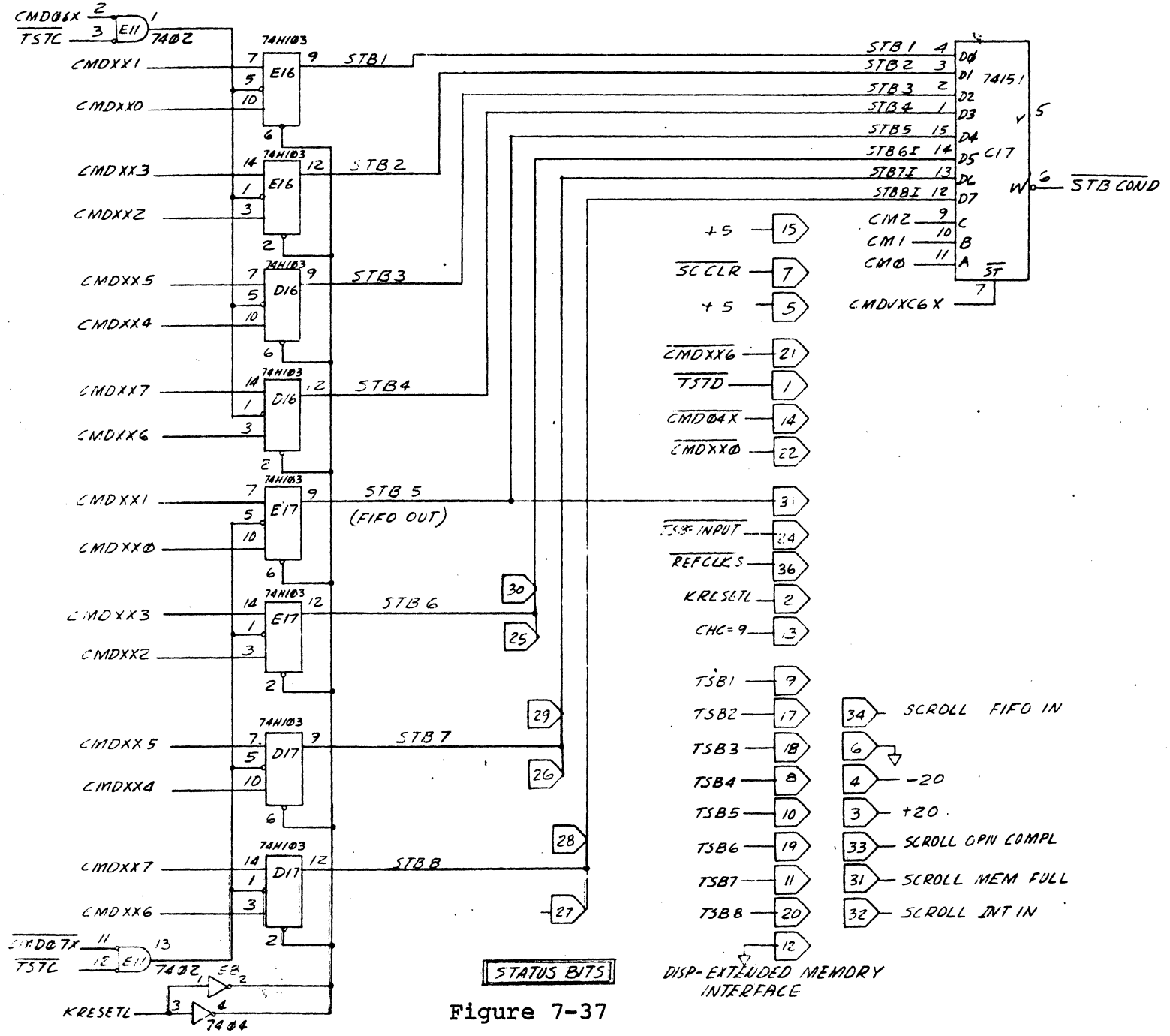

CMD06X
TSTC
E11
74Ø2
74H103
E16
CMDXX1
CMDXX0
STB1
CMDXX3
CMDXX2
STB2
D16
CMDXX5
CMDXX4
STB3
CMDXX7
CMDXX6
STB4
E17
CMDXX1
CMDXXØ
STB 5
(FIFO OUT)
CMDXX3
CMDXX2
STB 6
D17
CMDXX5
CMDXX4
STB 7
CMDXX7
CMDXX6
STB 8
CMDØ7X
TSTC
KRESETL
7404
STB 1
STB 2
STB 3
STB 4
STB 5
STB 6 I
STB 7 I
STB 8 I
74151
C17
CM2
CM1
CMØ
STB COND
CMDUXC6X
+5
SCCLR
CMDXX6
TSTD
CMD04X
CMDXXØ
INPUT
REFCLKS
KRCSETL
CHC=9
TSB1
TSB2
TSB3
TSB4
TSB5
TSB6
TSB7
TSB8
STATUS BITS
SCROLL FIFO IN
-20
+20
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
DISP-EXTENDED MEMORY INTERFACE

Figure 7-37

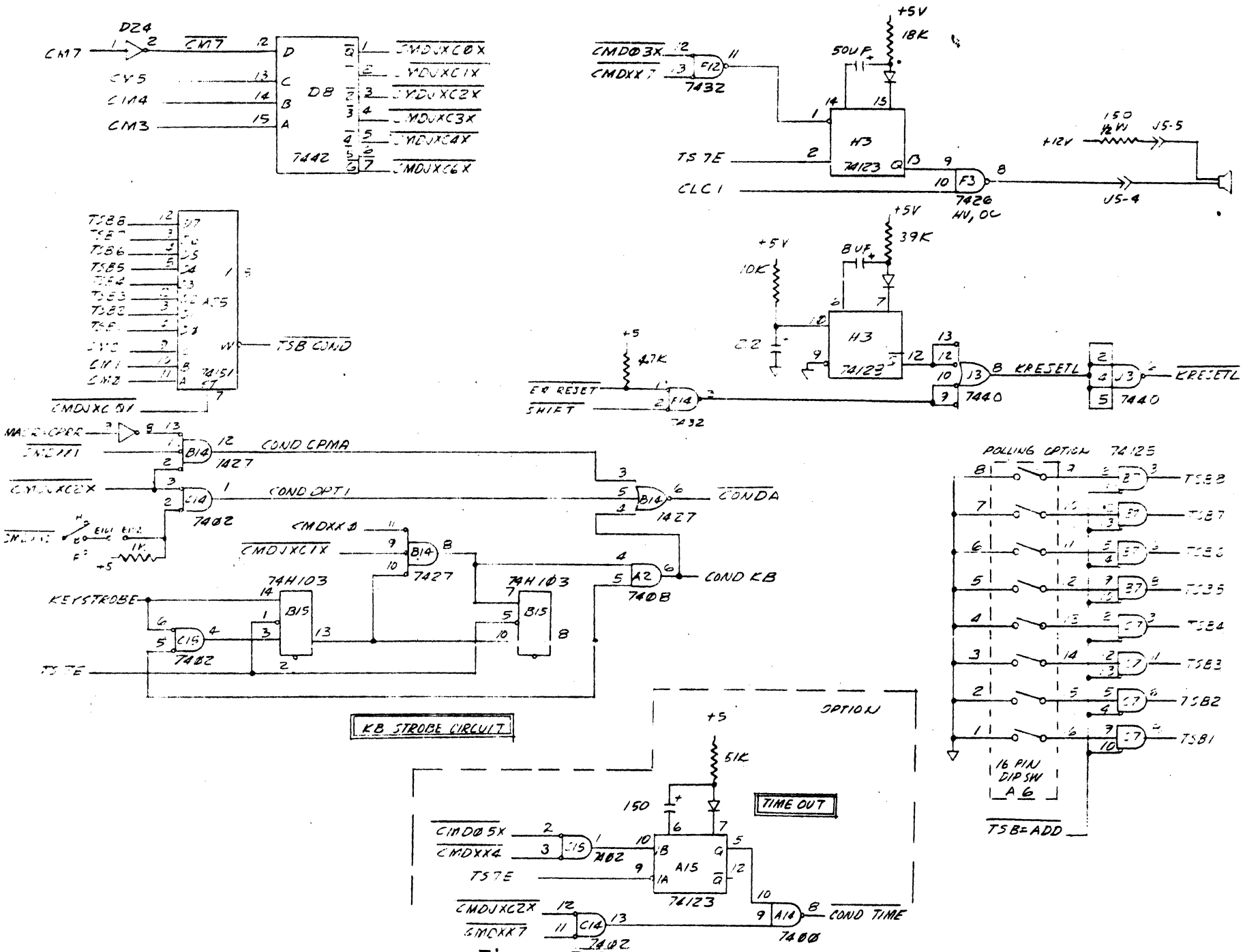

KB STROBE CIRCUIT
OPTION
TIME OUT
POLLING OPTION 74125
16 PIN DIP SW A6
TSB=ADD
COND CPMA
COND OPT1
COND KB
COND TIME
CONDA
TSB COND
KRESETL
74H103
7432
7402
7427
7408
7400
7440
7426 HV, OC
74123
74151
74125

Figure 7-38

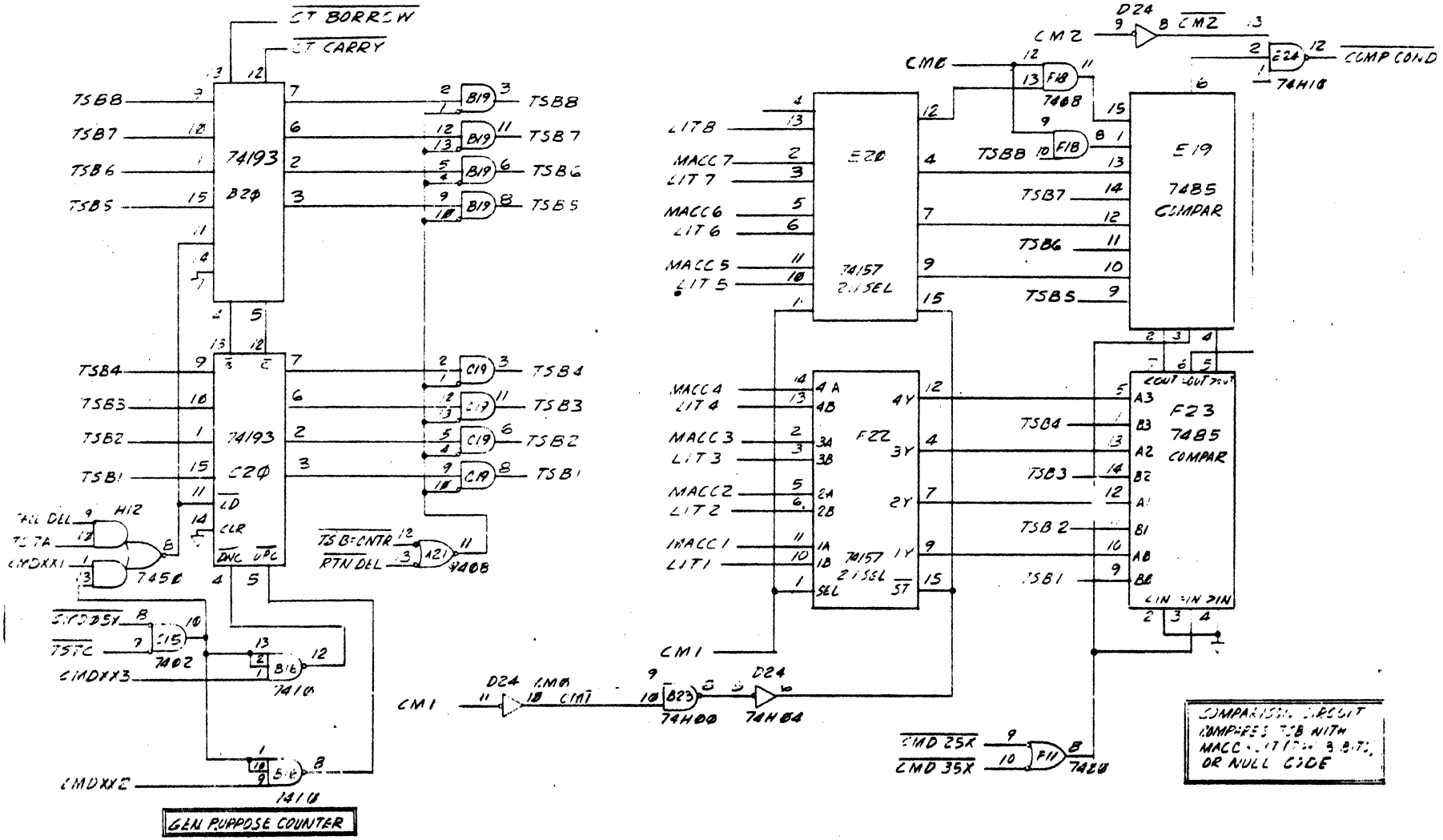

CT BORROW
CT CARRY
74193
B20
C20
LD
CLR
DNC
UPC
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
B19
C19
C17
C18
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
HI2
7450
CMDXX1
TSB=CNTR
RTN DEL
74H08
CMDXX3
CMDXXE
7402
7410
7400
GEN PURPOSE COUNTER
D24
CMZ
COMP COND
74H18
CMC
F18
E20
E19
7485
COMPAR
LIT8
MACC7
LIT7
MACC6
LIT6
MACC5
LIT5
74157
2:1 SEL
MACC4
LIT4
MACC3
LIT3
MACC2
LIT2
MACC1
LIT1
F22
4A
4B
3A
3B
2A
2B
1A
1B
SEL
4Y
3Y
2Y
1Y
ST
F23
A3
B3
A2
B2
A1
B1
A0
B0
CIN
COUT
CM1
74H00
74H04
CMD 25X
CMD 35X
F11
7420
COMPARISON CIRCUIT
COMPARES TSB WITH
MACC LIT (OR 8 BITS)
OR NULL CODE

Figure 7-39

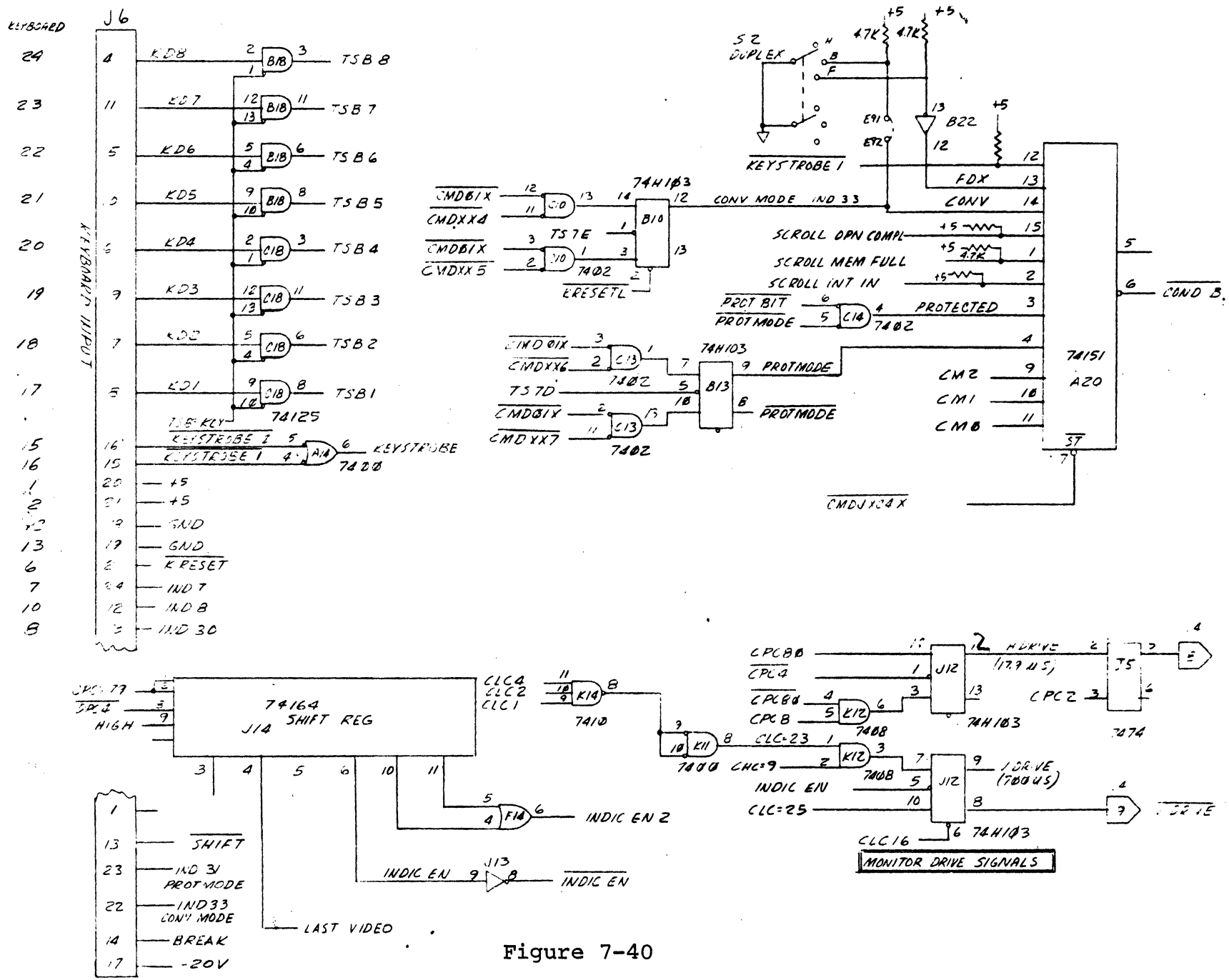

KEYBOARD
J6
KEYBOARD INPUT
KDB
KD7
KD6
KD5
KD4
KD3
KD2
KD1
TSB 8
TSB 7
TSB 6
TSB 5
TSB 4
TSB 3
TSB 2
TSB 1
74125
KEYSTROBE 2
KEYSTROBE 1
KEYSTROBE
7400
+5
+5
GND
GND
K RESET
IND 7
IND 8
IND 30
S2 DUPLEX
4.7K
4.7K
KEYSTROBE 1
B22
FDX
CONV
CONV MODE IND 33
74H103
CMDB1X
CMDXX4
CMDB1X
CMDXX5
TS7E
7402
KRESETL
SCROLL OPN COMPL
SCROLL MEM FULL
SCROLL INT IN
PROT BIT
PROTMODE
PROTECTED
7402
CMDB0IX
CMDXX6
TS7D
CMDB0IX
CMDYX7
7402
74H103
PROTMODE
PROTMODE
74151
A20
CM2
CM1
CM0
COND B.
CMDJXC4X
74164
J14
SHIFT REG
SPC 2
SPC 4
HIGH
CLC4
CLC2
CLC1
7410
CLC=23
CHC=9
7400
INDIC EN
CLC=25
CLC16
74H103
CPCB0
CPC4
CPCB0
CPC 8
7408
74H103
CPC 2
7474
H DRIVE
(17.7 μS)
J DRIVE
(700 μS)
MONITOR DRIVE SIGNALS
SHIFT
IND 31
PROTMODE
IND33
CONV MODE
BREAK
-20V
INDIC EN 2
INDIC EN
INDIC EN
LAST VIDEO

Figure 7-40

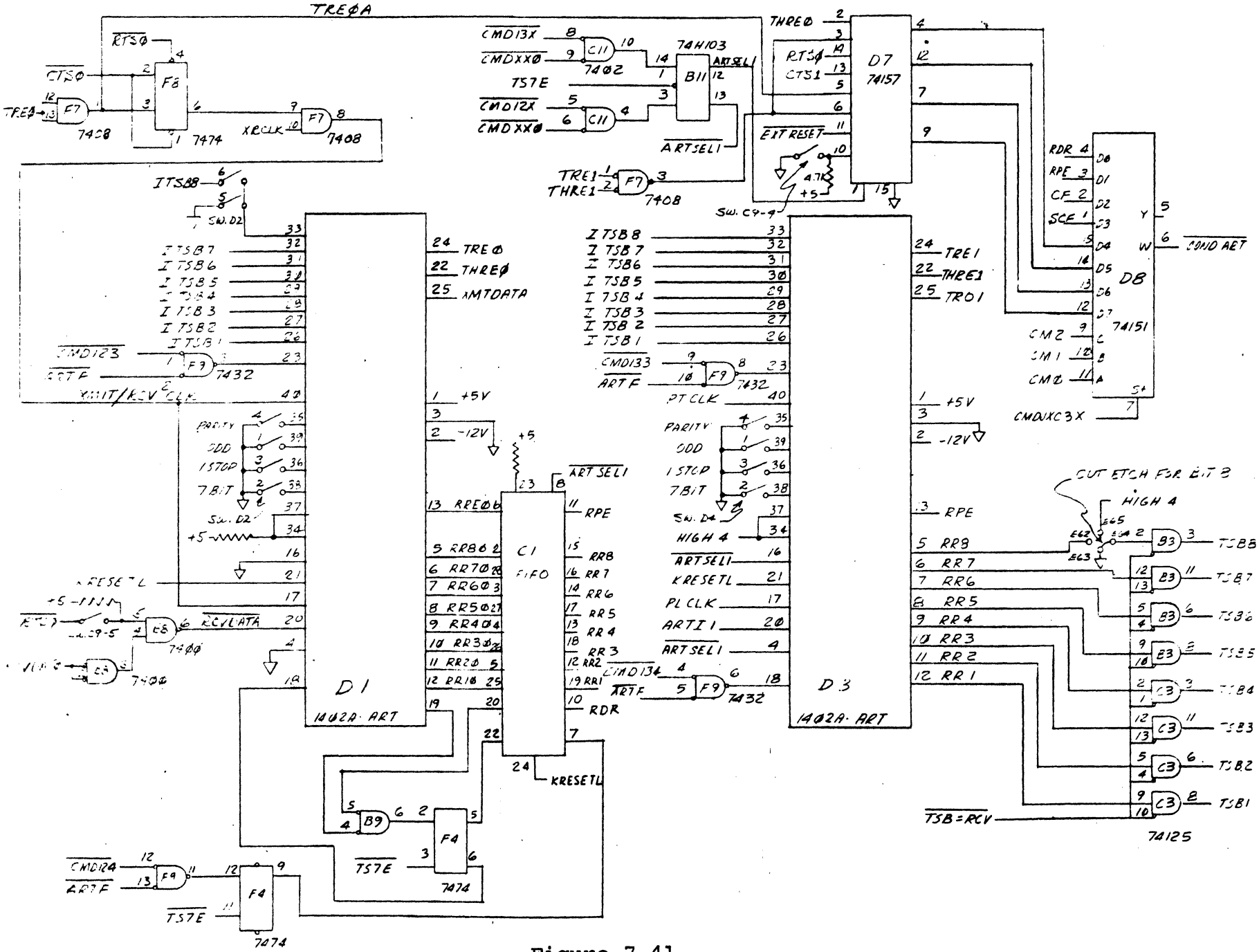

TREØA
RTSØ
CTSØ
TREØ
F8
F7
7408
7474
XRCLK
CMD13X
CMDXXØ
TS7E
CMD12X
CMDXXØ
C11
7402
74H103
B11
ARTSEL1
THREØ
RTSØ
CTS1
D7
74157
EITRESET
4.7K
+5
TRE1
THRE1
SW. C9-9
RDR
RPE
CF
SCE
D8
74151
CMD2
CMD1
CMDØ
CMDXC3X
ITSB8
SW. D2
ITSB7
ITSB6
ITSB5
ITSB4
ITSB3
ITSB2
ITSB1
CMD123
EITF
F9
7432
XMIT/RCV CLK
PARITY
ODD
1STOP
7BIT
SW. D2
+5
XRESETL
+5
SW. C9-5
EITF
C8
7400
RCVDATA
D1
1402A-ART
TREØ
THREØ
XMTDATA
+5V
-12V
RRE
RR8
RR7
RR6
RR5
RR4
RR3
RR2
RR1
RDR
C1
FIFO
ARTSEL1
KRESETL
B9
F4
7474
TS7E
CMD12A
ARTF
CMD13A
D3
TRE1
THRE1
TRO1
RPE
HIGH 4
CUT ETCH FOR EIT 2
EG5
EG4
EG2
EG3
B3
C3
74125
TSB8
TSB7
TSB6
TSB5
TSB4
TSB3
TSB2
TSB1
TSB=RCV

Figure 7-41

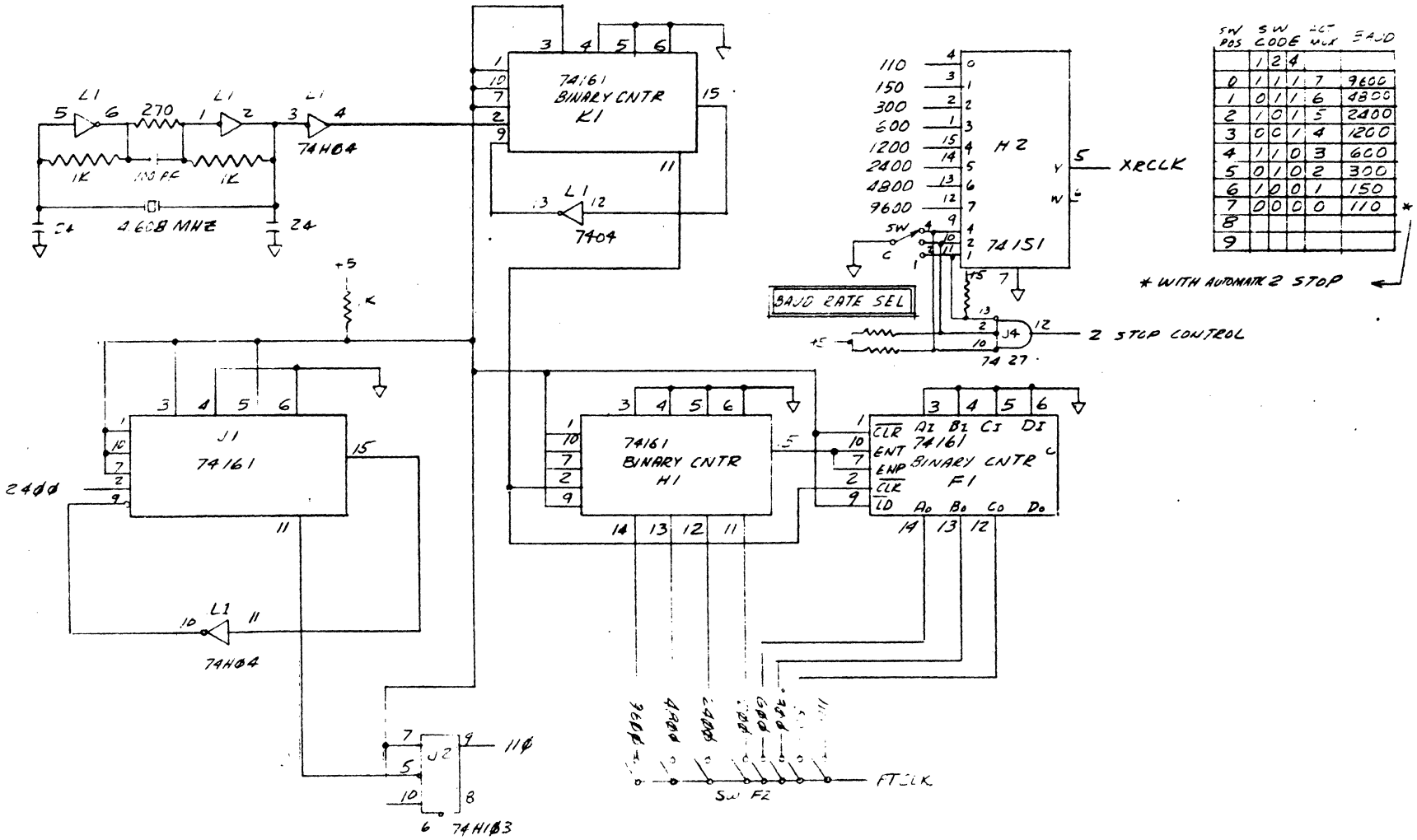
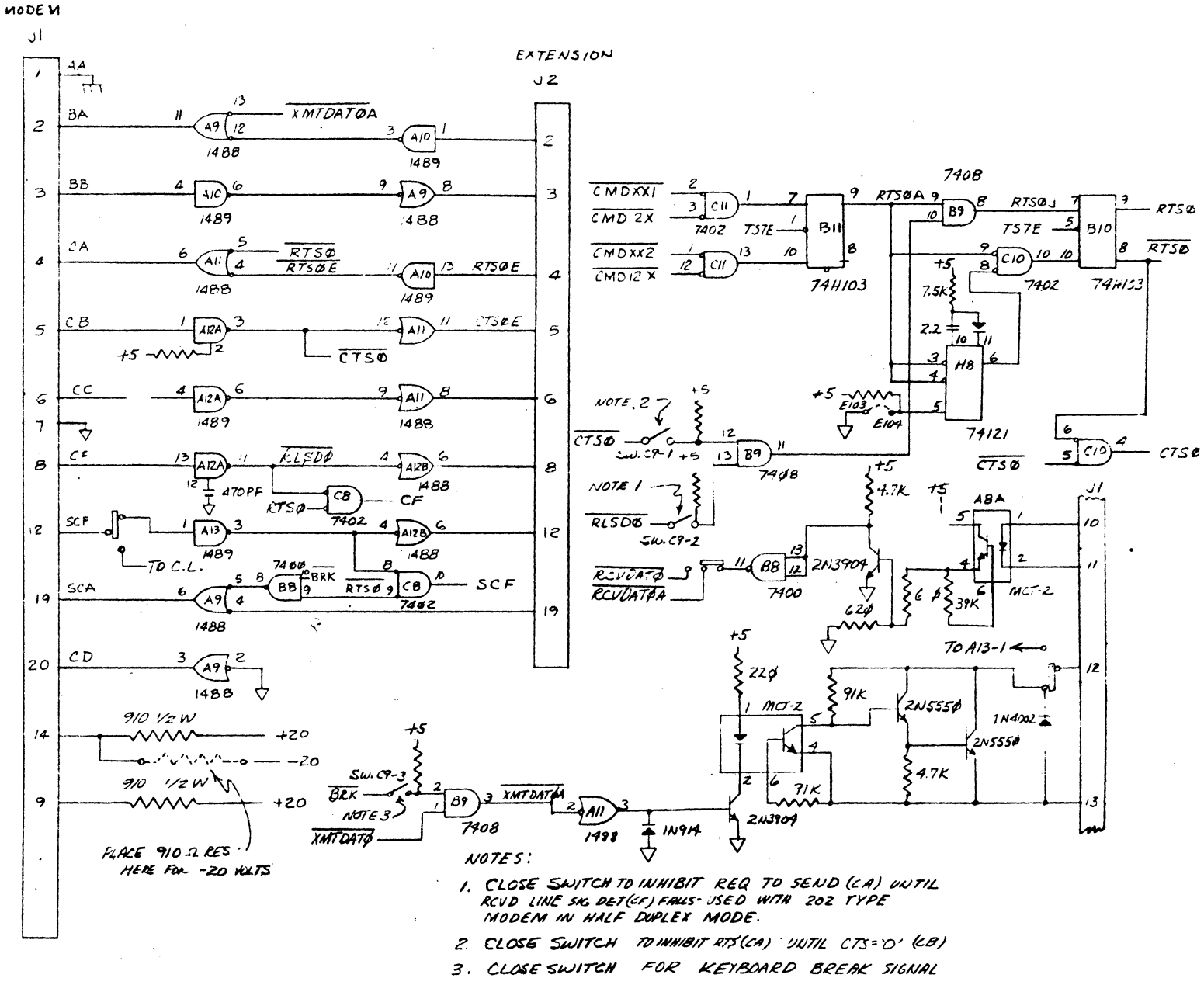

74161
BINARY CNTR
K1
74161
BINARY CNTR
H1
74161
BINARY CNTR
F1
J1
74161
74151
74H04
7404
74H03
270
1K
100 PF
4.608 MHZ
2400
BAUD RATE SEL
XRCLK
2 STOP CONTROL
74 27
* WITH AUTOMATIC 2 STOP
FTCLK
SW F2
110
150
300
600
1200
2400
4800
9600
SW POS
SW CODE
ACT BAUD
9600
4800
2400
1200
600
300
150
110

Figure 7-42



NOTES:

1. CLOSE SWITCH TO INHIBIT REQ TO SEND (CA) UNTIL RCVD LINE SIG DET (CF) FALLS. USED WITH 202 TYPE MODEM IN HALF DUPLEX MODE.
2. CLOSE SWITCH TO INHIBIT RTS (CA) UNTIL CTS = 'O' (CB)
3. CLOSE SWITCH FOR KEYBOARD BREAK SIGNAL

Figure 7-43

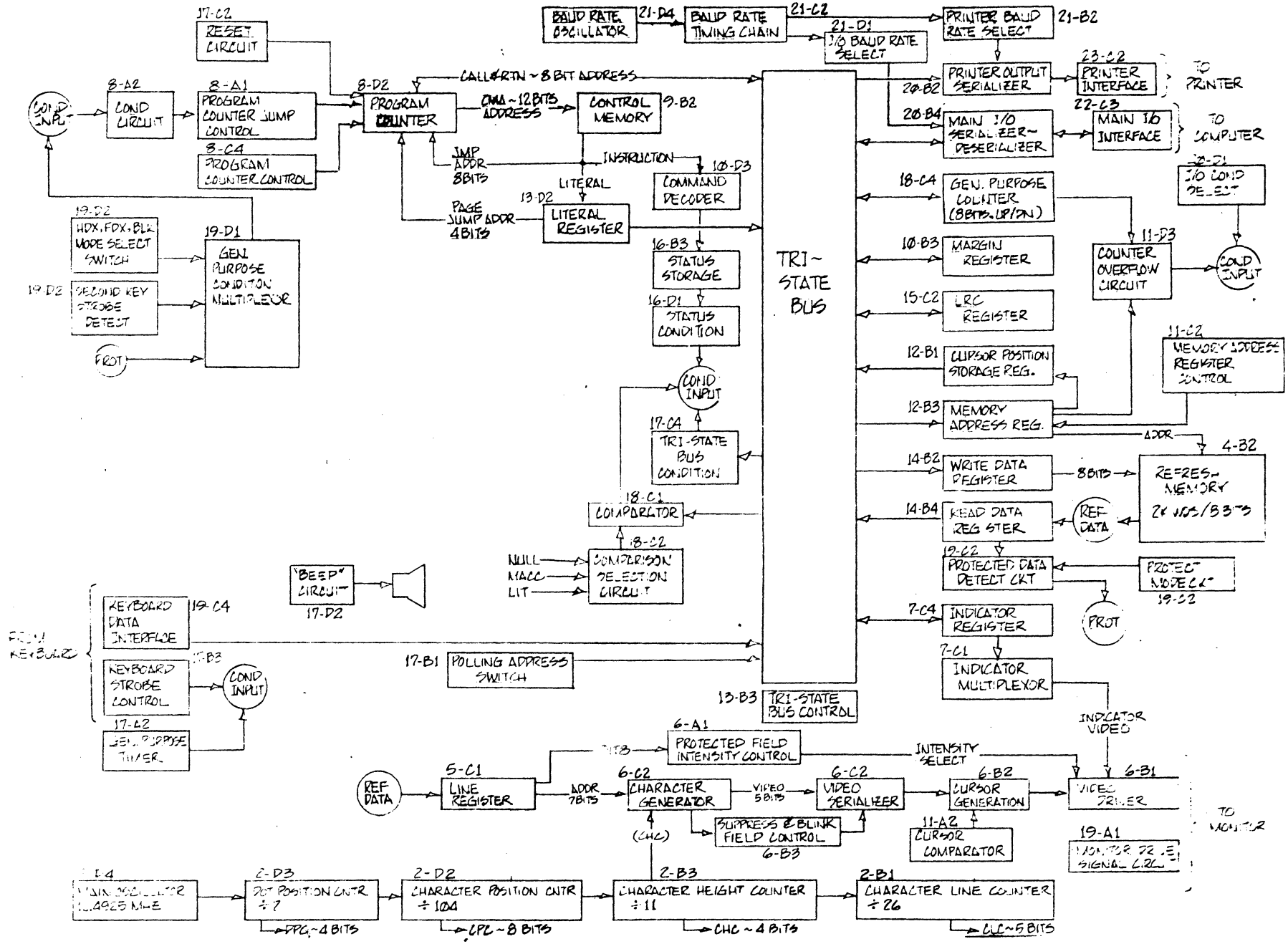

RESET CIRCUIT
17-C2
BAUD RATE OSCILLATOR
21-D4
BAUD RATE TIMING CHAIN
21-C2
21-D1
I/O BAUD RATE SELECT
PRINTER BAUD RATE SELECT
21-B2
COND INPUT
8-A2
COND CIRCUIT
8-A1
PROGRAM COUNTER JUMP CONTROL
8-C4
PROGRAM COUNTER CONTROL
8-D2
PROGRAM COUNTER
CALL & RTN ~ 8 BIT ADDRESS
CMA ~ 12 BITS ADDRESS
CONTROL MEMORY
9-B2
JMP ADDR 8BITS
INSTRUCTION
10-D3
COMMAND DECODER
LITERAL
13-D2
LITERAL REGISTER
PAGE JUMP ADDR 4BITS
19-D2
HDX, FDX, BLK MODE SELECT SWITCH
19-D2
SECOND KEY STROBE DETECT
PROT
19-D1
GEN PURPOSE CONDITION MULTIPLEXOR
16-B3
STATUS STORAGE
16-D1
STATUS CONDITION
COND INPUT
17-C4
TRI-STATE BUS CONDITION
18-C1
COMPARATOR
18-C2
COMPARISON SELECTION CIRCUIT
NULL
MACC
LIT
"BEEP" CIRCUIT
17-D2
KEYBOARD DATA INTERFACE
19-C4
KEYBOARD STROBE CONTROL
17-B3
COND INPUT
17-C2
GEN. PURPOSE TIMER
17-B1
POLLING ADDRESS SWITCH
TRI-STATE BUS
13-B3
TRI-STATE BUS CONTROL
PRINTER OUTPUT SERIALIZER
20-B2
PRINTER INTERFACE
23-C2
TO PRINTER
MAIN I/O SERIALIZER-DESERIALIZER
20-B4
MAIN I/O INTERFACE
22-C3
TO COMPUTER
I/O COND SELECT
12-D1
GEN. PURPOSE COUNTER (8BITS, UP/DN)
18-C4
MARGIN REGISTER
10-B3
COUNTER OVERFLOW CIRCUIT
11-D3
COND INPUT
LRC REGISTER
15-C2
CURSOR POSITION STORAGE REG.
12-B1
MEMORY ADDRESS REGISTER CONTROL
11-C2
MEMORY ADDRESS REG.
12-B3
ADDR
WRITE DATA REGISTER
14-B2
8 BITS
REFRESH MEMORY 2K WDS/8 BITS
4-B2
READ DATA REGISTER
14-B4
REF DATA
PROTECTED DATA DETECT CKT
19-C2
PROTECT MODE CKT
19-C3
INDICATOR REGISTER
7-C4
PROT
INDICATOR MULTIPLEXOR
7-C1
INDICATOR VIDEO
PROTECTED FIELD INTENSITY CONTROL
6-A1
INTENSITY SELECT
REF DATA
LINE REGISTER
5-C1
ADDR 7BITS
CHARACTER GENERATOR
6-C2
VIDEO 5 BITS
VIDEO SERIALIZER
6-C2
CURSOR GENERATION
6-B2
VIDEO DRIVER
6-B1
TO MONITOR
SUPPRESS & BLINK FIELD CONTROL
6-B3
(CHC)
CURSOR COMPARATOR
11-A2
MONITOR SYNC SIGNAL CKT
19-A1
CHARACTER POSITION CNTR ÷ 104
2-D2
CPC ~ 8 BITS
CHARACTER HEIGHT COUNTER ÷ 11
2-B3
CHC ~ 4 BITS
CHARACTER LINE COUNTER ÷ 26
2-B1
CLC ~ 5 BITS

Figure 7-44

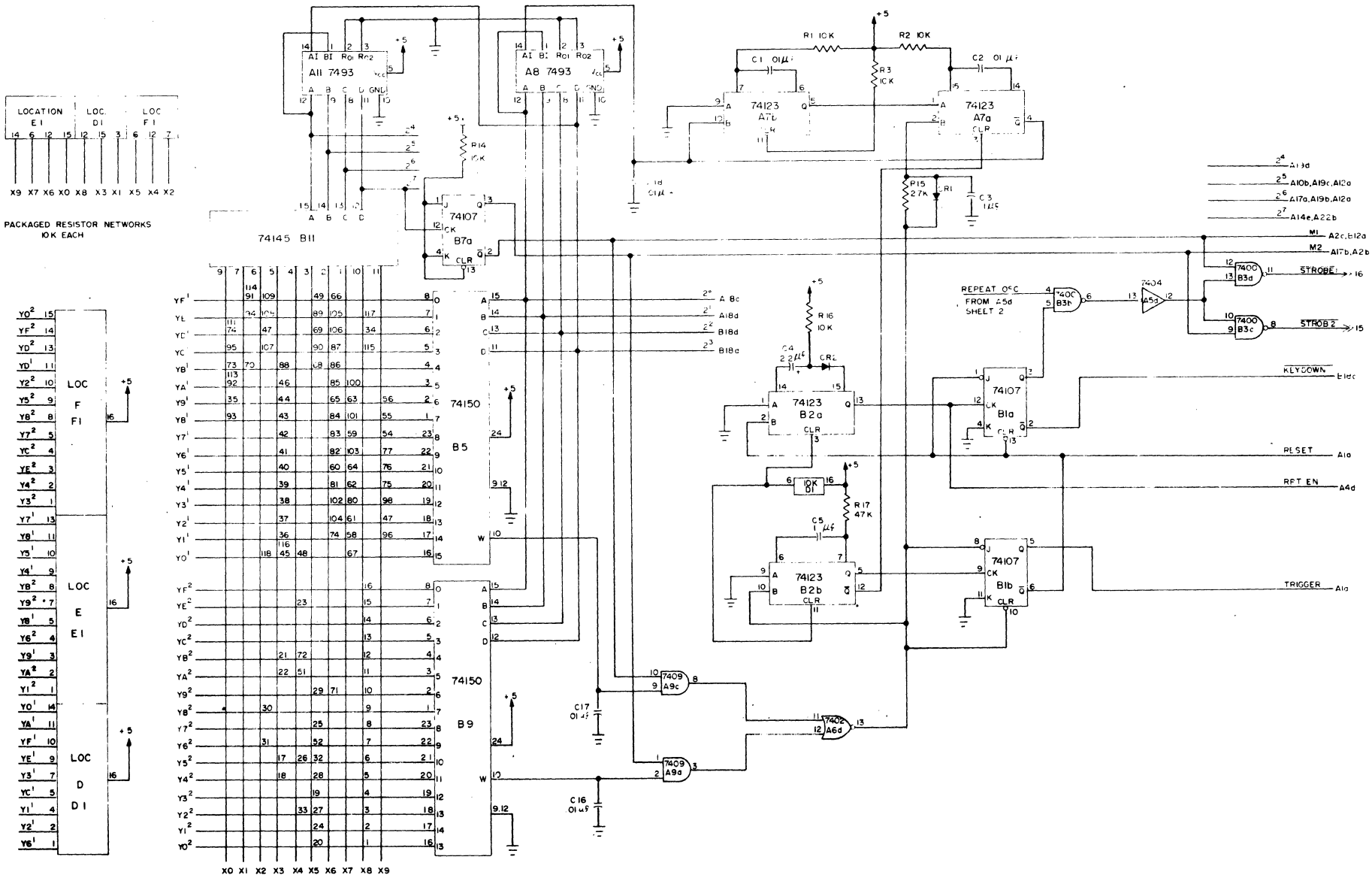


Figure 7-45 Keyboard Schematic

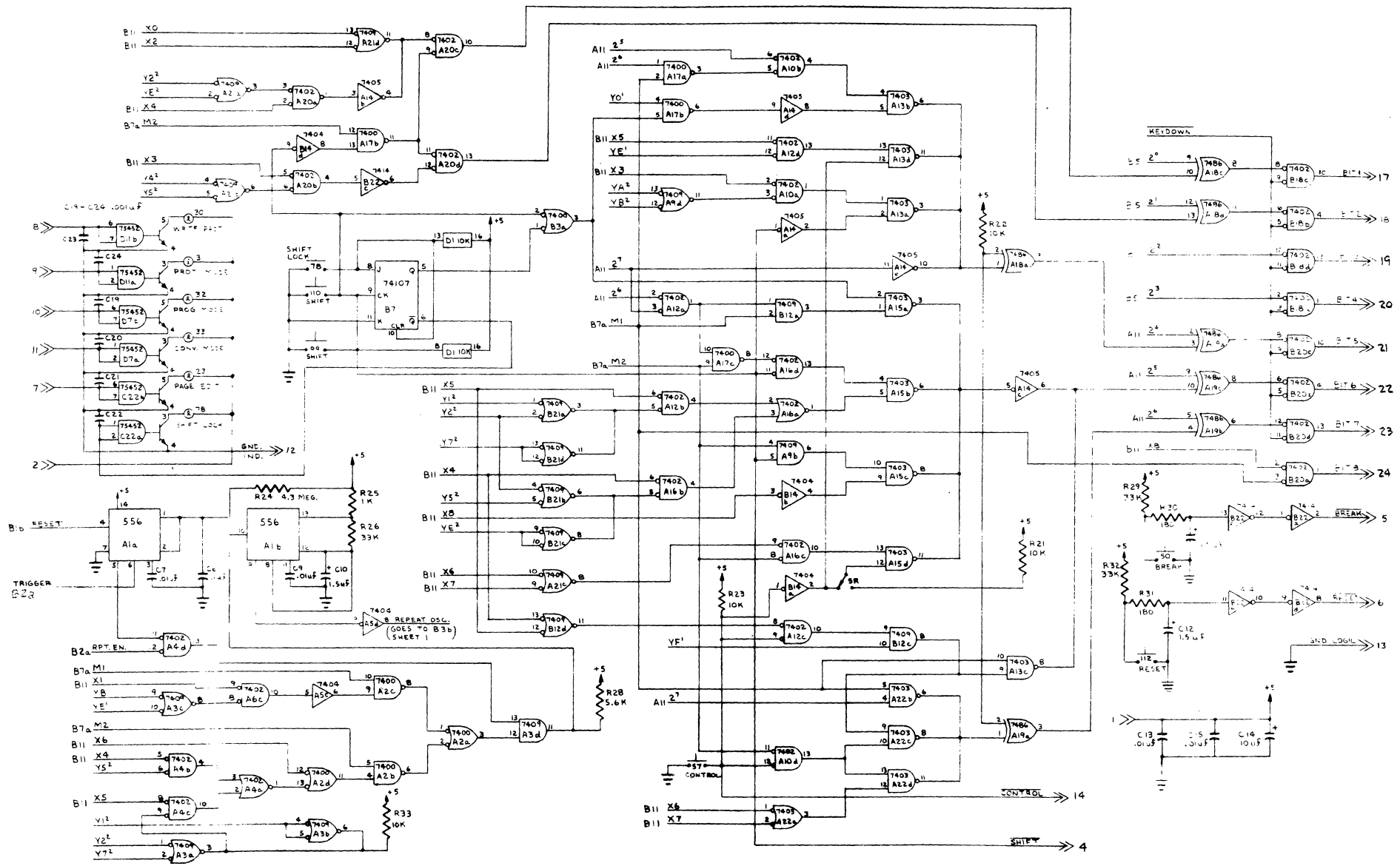
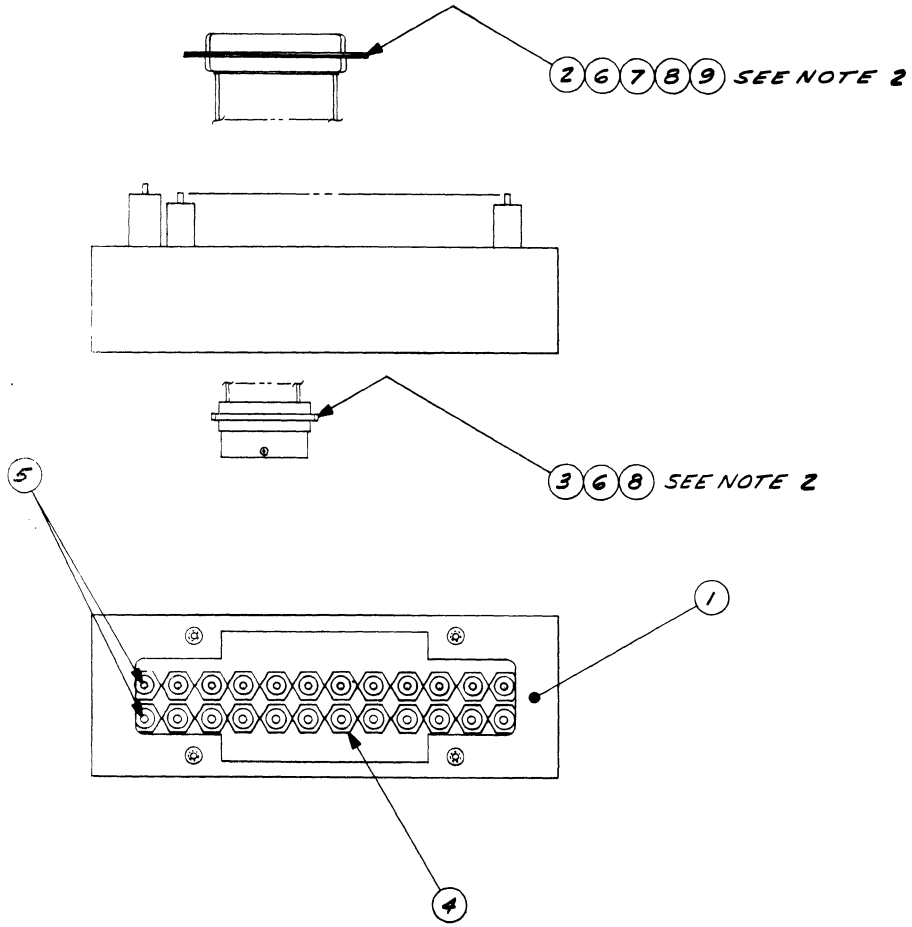


Figure 7-46 Keyboard Schematic (continued)



ZONE	LTR	DESCRIPTION	DATE	APPROVED

NOTES:
1. SOLDER PER MIL-STD-454 USING ITEM 8.
2. FOR COLOR AND DESTINATION OF WIRE REFER TO WIRING DIAGRAM, ITEM 10.

ITEM NO.	QTY REQ	CODE IDENT NO.	PART OR IDENT NO.	NOMENCLATURE OR DESCRIPTION	REF DES
10	REF		D-1604	WIRING DIAGRAM	
9	AR		AWG 22	TUBING, HEAT-SHRINKABLE	
8	AR		SN62NR1MAP2	SOLDER	
7	AR		MS3367-2-9	STRAP, TIE DOWN	
6	AR		AWG 22	WIRE, ELEC, INSUL	
5	2	23939	A-2859	CAPACITOR, FEED THRU	C47,48
4	22	23939	A-2858	CAPACITOR, FEED THRU	C25-46
3	1	77820	JTP0LRE16-26S	CONNECTOR	J2
2	1	02260	17-20260	CONNECTOR	P2
1	1			ENCLOSURE	

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES AND INCLUDE PLATING,
TOLERANCES ON: RMS √
FRACTIONS DECIMALS ANGLES
± — / — ± — ± —
REMOVE ALL SHARP EDGES
MATERIAL

CONTRACT NO.

		DATE
APPROVAL		
CHECKED		
DRAWN		10/17/76

NATIONAL SCIENTIFIC LABORATORIES, INC.
WASHINGTON, D.C.

KEYBOARD INTERFACE ENCLOSURE ASSY

SIZE	CODE IDENT NO.	DRAWING NO.	REV.
C	15119	C-1603	

SCALE 1/1 SHEET

C-1603

Figure 7-47

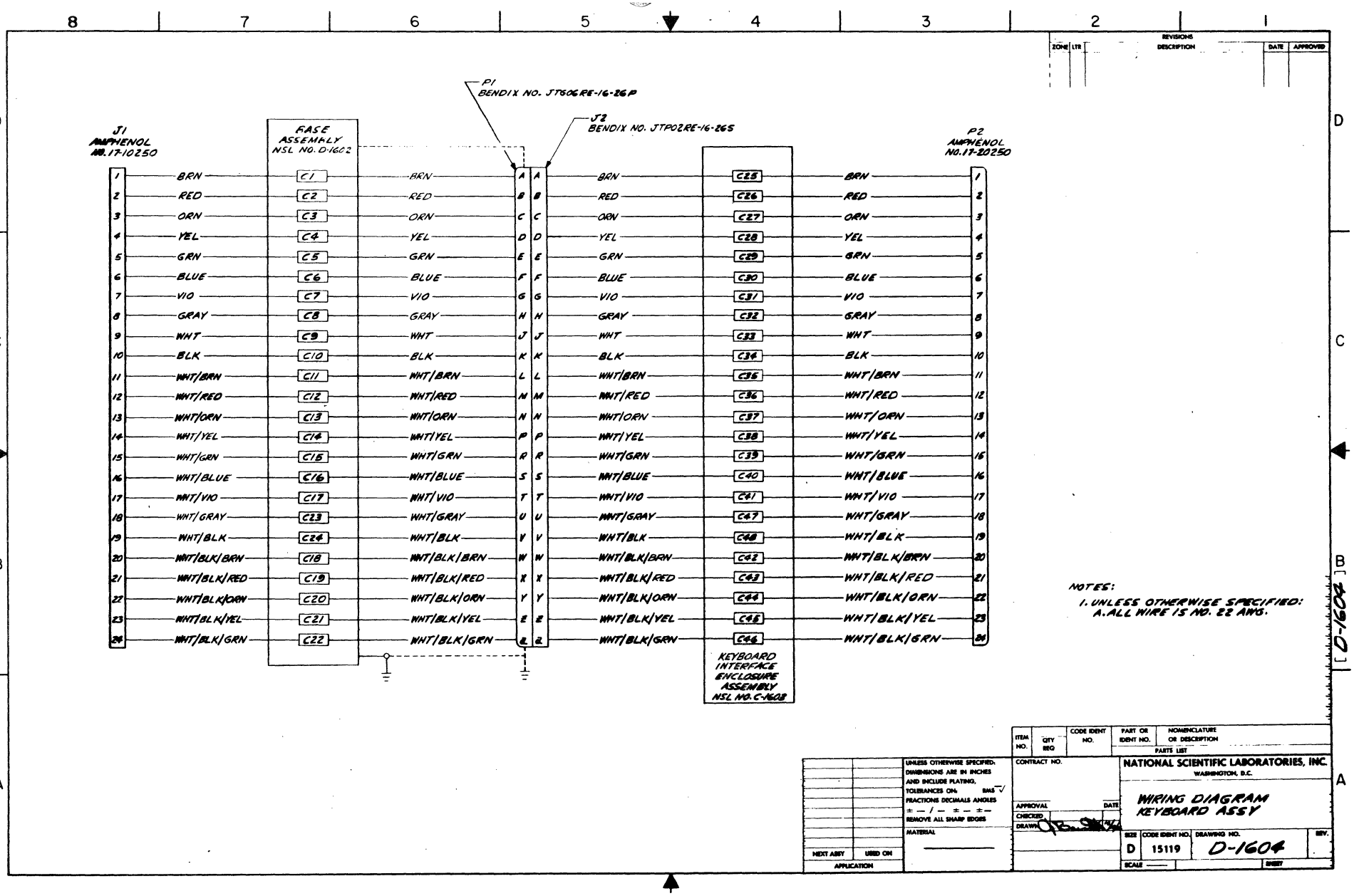
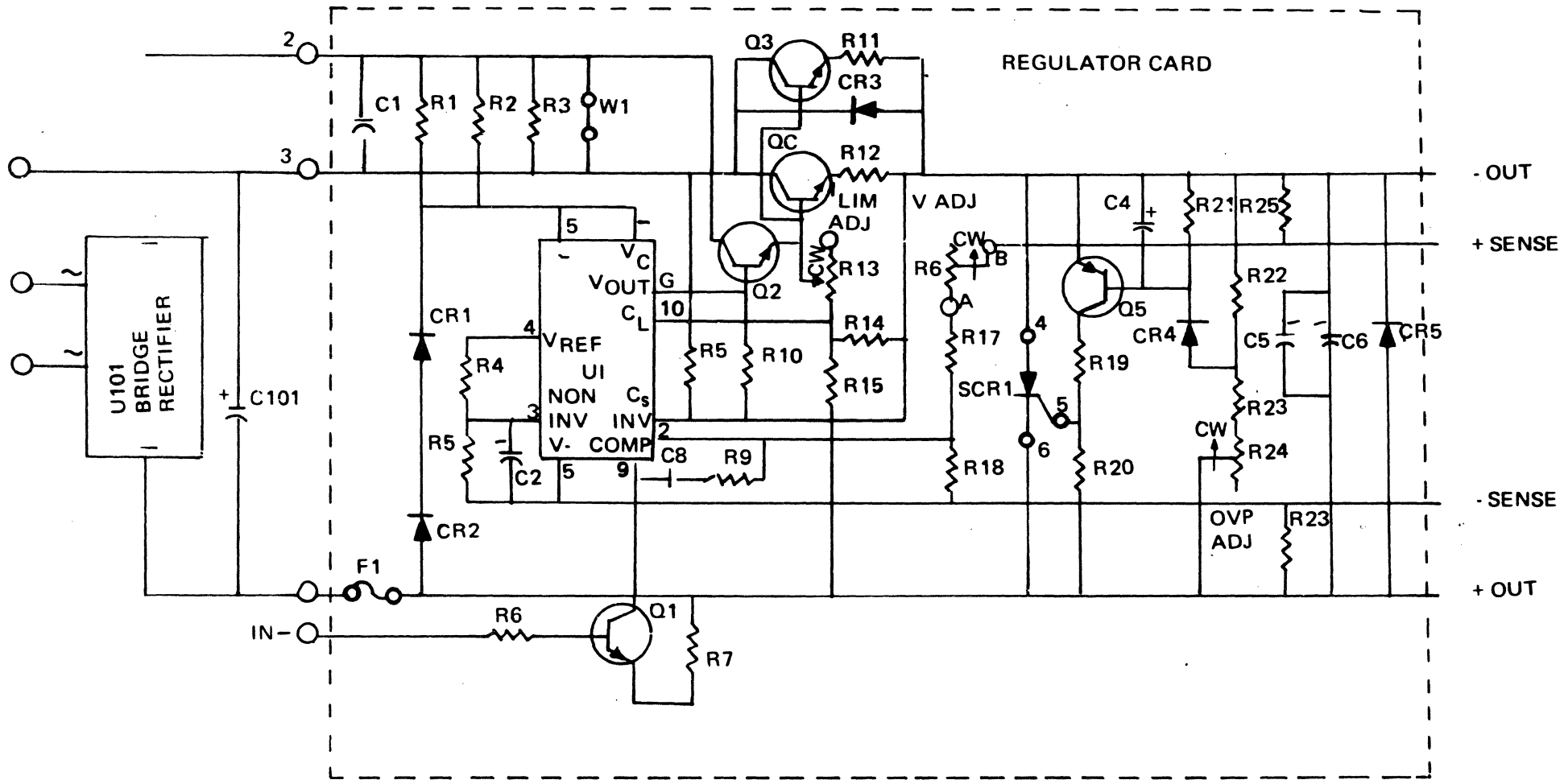

P1
BENDIX NO. JT06RE-16-26P
J2
BENDIX NO. JTP02RE-16-26S
J1
AMPHENOL
NO. 17-10250
BASE
ASSEMBLY
NSL NO. D-1602
P2
AMPHENOL
NO. 17-20250
KEYBOARD
INTERFACE
ENCLOSURE
ASSEMBLY
NSL NO. C-1603
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL WIRE IS NO. 22 AWG.
NATIONAL SCIENTIFIC LABORATORIES, INC.
WASHINGTON, D.C.
WIRING DIAGRAM
KEYBOARD ASSY
D
15119
D-1604

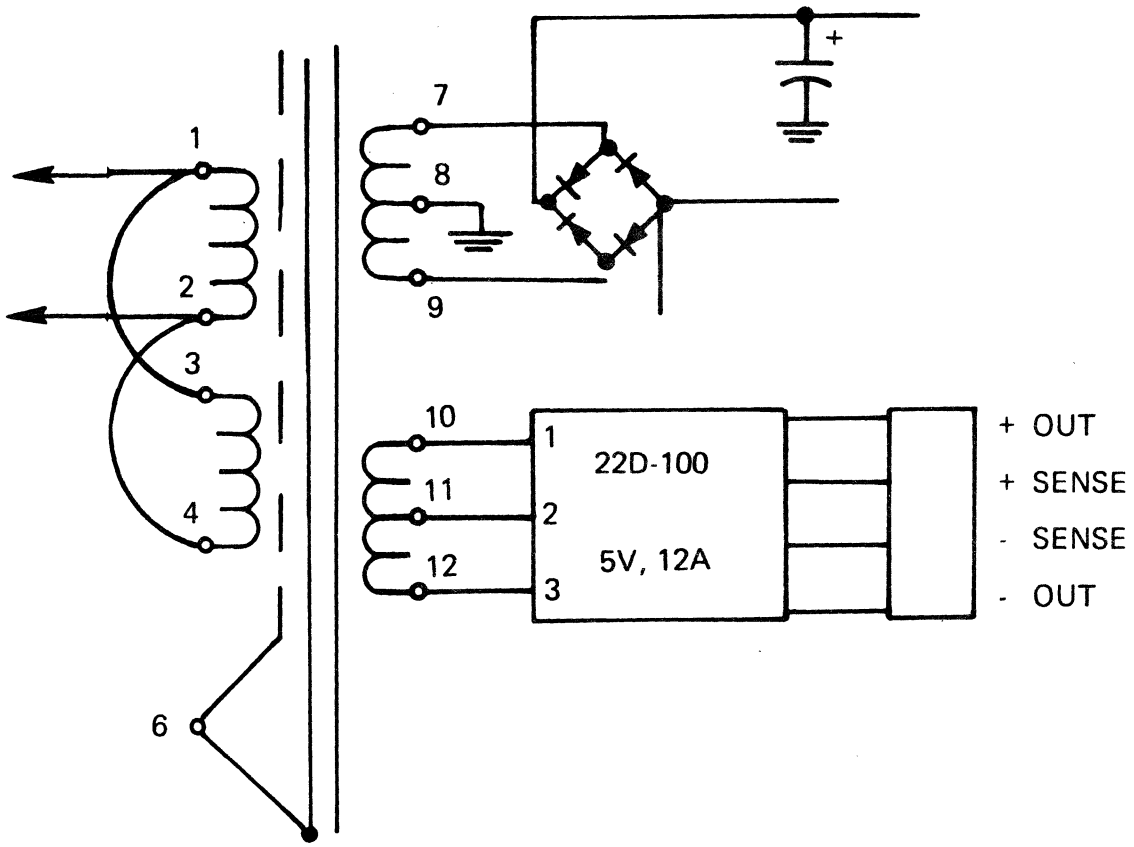
Figure 7-48

LOGIC POWER SUPPLY SCHEMATIC



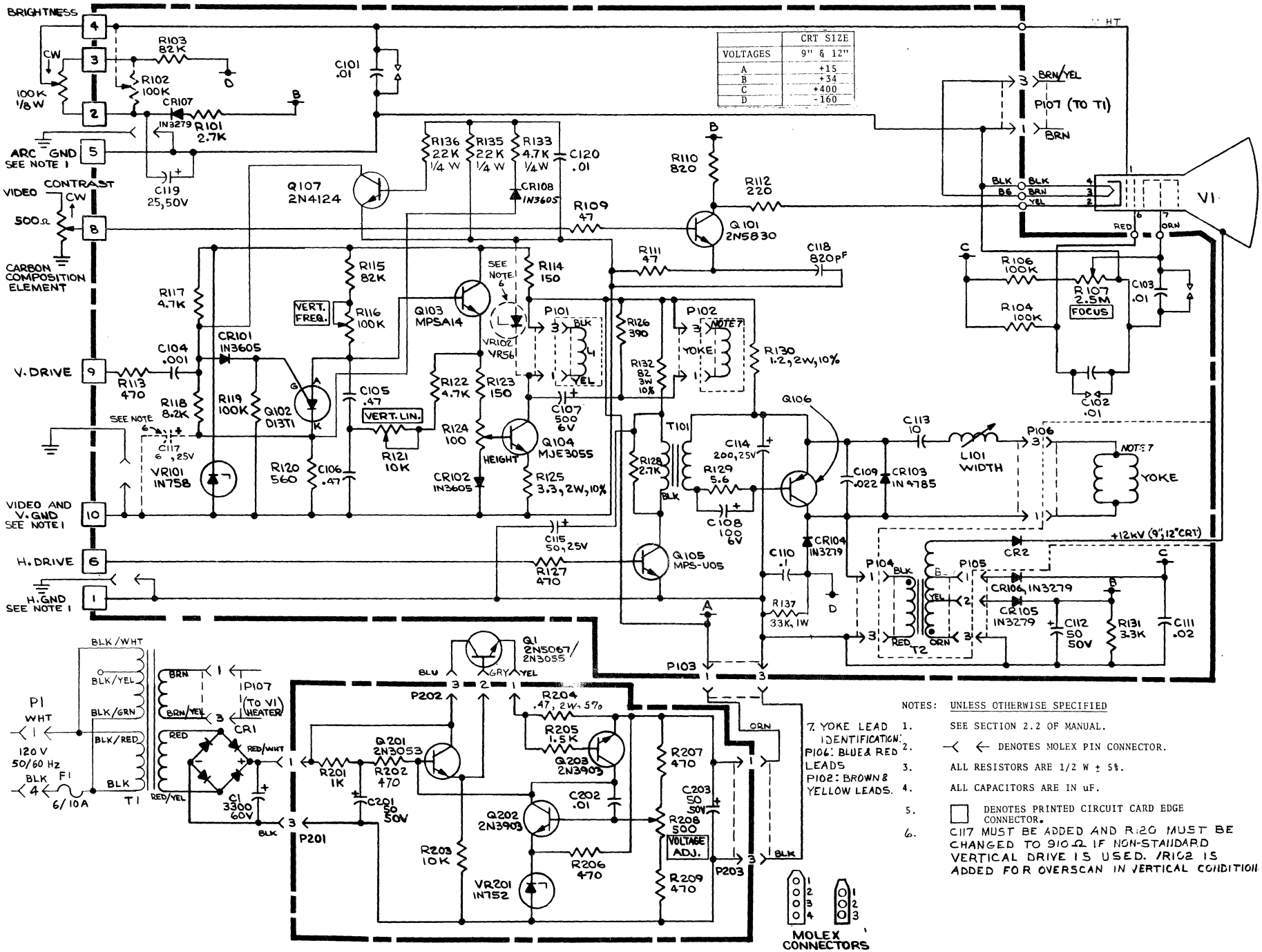
MODEL 22D-100 SCHEMATIC

Figure 7-49



WIRING DIAGRAM PK1112

Figure 7-50



VOLTAGES	CRT SIZE 9" & 12"
A	+15
B	+34
C	+400
D	-160

Figure 7-51

VIDEO BOARD WIRING

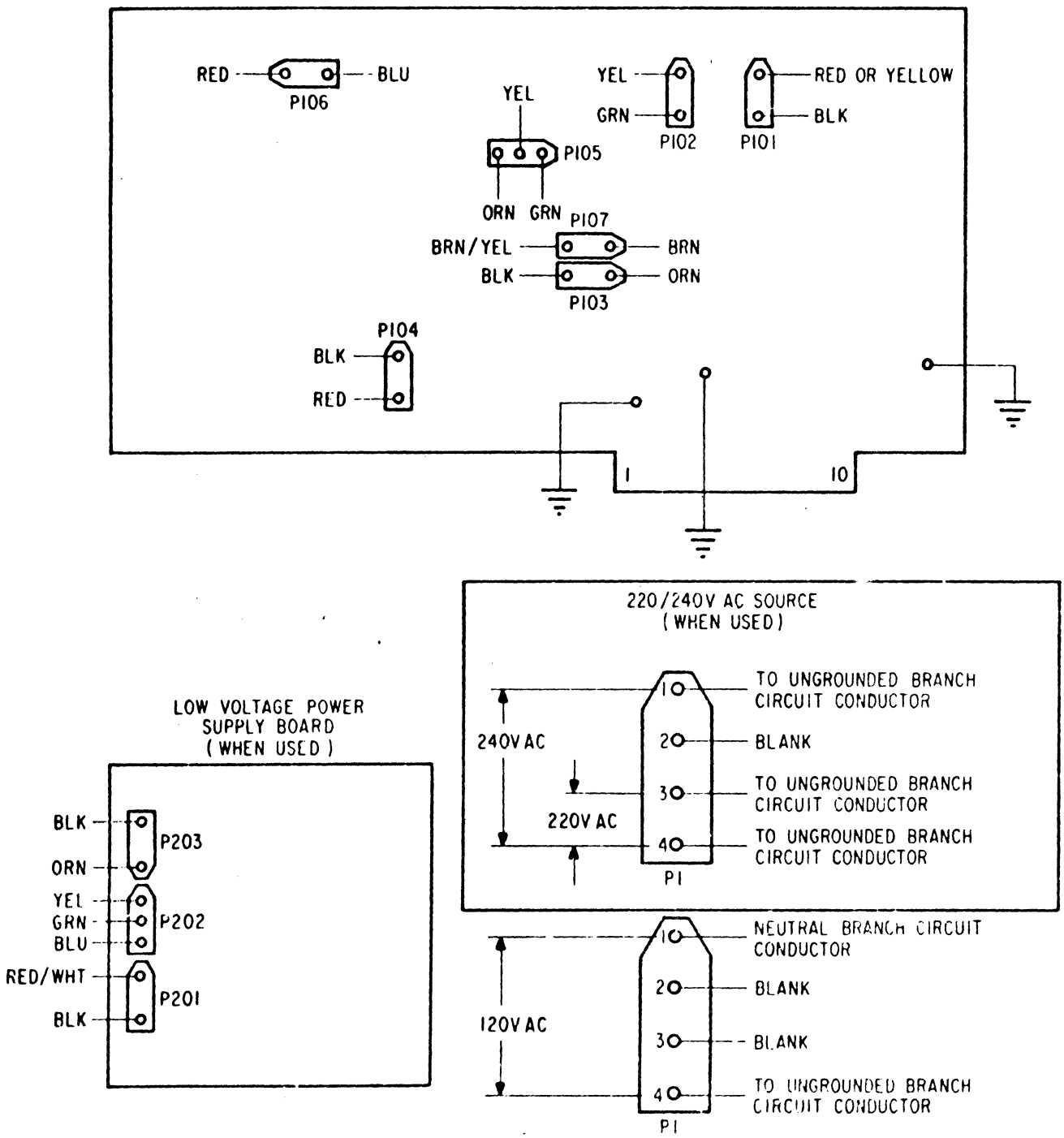
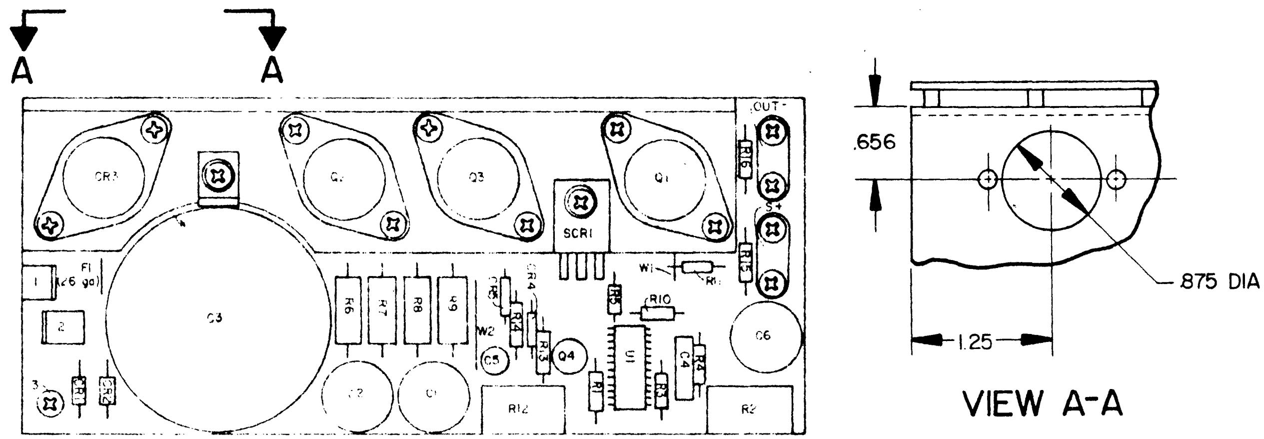


Figure 7-52



SUGGESTED SOURCE(S)	
VENDOR	P/N
LEAR/SIEGLER CODE IDENT 98438	129398-11

ALTERED PER VIEW A-A

Figure 7-53. Logic Power Supply Layout

VIII RENEWAL PARTS INFORMATION

MONITOR PARTS LIST

Symbol	Description	Mfg.	Mfg. Part Number
	Capacitor, Fixed: µF Unless Otherwise Stated		
C1	3300; 60V, Electrolytic	BBRC	1-012-2156
C101	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63
C102	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63
C103	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63
C104	0.001; ± 10% , 1000V, Ceramic Disc	ERIE	Type 801
C105	0.47 ± 10%, 100V, Mylar	PAK	MF830
C106	0.47 ± 10%; 100V, Mylar	PAK	MF830
C107	500; 6V, Electrolytic	BBRC	1-012-2158
C108	100; 6V, Electrolytic	BBRC	1-012-2160
C109	0.022 ± 10%, 400V, Mylar	SPRA	Type 225P
C110	.1 ± 10%; 200V, Mylar	PAK	MF580
C111	0.02 ± 20%; 1000V, Ceramic Disc	ERIE	Type 841
C112	50; 50V, Electrolytic	BBRC	1-012-2157
C113	10 ± 10%, 63V, Mylar	BBRC	1-012-1130
C114	200; 25V, Electrolytic	BBRC	1-012-2159
C115	50; 25V, Electrolytic	BBRC	1-012-2165
C116	20; 150V, Electrolytic	BBRC	1-012-1260
C117	6µf, 25V, Electrolytic	SPRA	TE1203
C118	820 pf ± 5%; 500V, Dipped Mica	ARCO	Type DM

MONITOR PARTS LIST (Continued)

Symbol	Description	Mfg.	Mfg. Part Number
C119	25; 50V, Electrolytic	BBRC	1-012-2193
C120	.01 = 20%; 1000 Ceramic Disc	ERIE	Type 811
C201	50; 50V, Electrolytic	BBRC	1-012-2157
C202	0.01 = 20%; 1000V, Ceramic Disc	ERIE	Type 841
C203	50;50V, Electrolytic	BBRC	1-012-2157
CR1	VS148, Bridge Rectifier	VARO	VS148
CR2q	H510, High Voltage Rectifier	VARO	H510
CR101	1N3605	SYL	1N3605
CR102	1N3605	SYL	1N3605
CR103	1N4785	RCA	1N4785
CR104	1N3279	DI	1N3279
CR105	1N3279	DI	1N3279
CR106	1N3279	DI	1N3279
CR107	1N3279	DI	1N3279
CR108	1N3605	SYL	1N3605
F1	Fuse, 0.6A-250V, 1/4 x 1-1/4, Slo-Blo	LF	Type AGC
or	Fuse, 0.6A-250V, 9/32x 1-1/4, Slo-Blo (TV-B12)	BUSS	Type MDM
F101	Fuse, 2A-125V, Picofuse	LF	276002
L1	Vertical Choke	BBRC	6-003-0321
L101	Coil, Width	BBRC	1-016-0303

MONITOR PARTS LIST (Continued)

Symbol	Description	Mfg	Mfg. Part Number
	TRANSISTOR		
Q1	2N3055	RCA	2N3055
Q101	2N5830	MOT	2N5830
Q102	D13T1	GE	D13T1
	Resistor, Film: 1/2W ± 5% Unless otherwise stated.		
R133	4.7K; 1/4W		
R134	Not Used		
R135	22K		
R136	22K		
R137	33K; 1W Composition		
R201	1K		
R202	1K		
R203	10K		
R204	0.68 ± 10%; 2W, Wirewound	IRC	Type BHW
R205	1.5K		
R206	470		
R207	470		
R208	Var; 500 ± 20%; 1/5W, Composition	CTS	Type 201
R209	470		

Symbol	Description	Mfg.	Mfg. Part Number
	TRANSFORMER		
T1	Power	BBRC	1-017-5390
T2	High Voltage (TV-12C, TV-A12, and TV-E12)	BBRC	6-003-0320
or	High Voltage (TV-B12, TV-TC12, and TV-C12)	BBRC	6-003-0325
or	High Voltage (TV-T12)	BBRC	6-003-0326
or	High Voltage (TV-D12)	BBRC	6-003-0326
T101	Horizontal Driver	BBRC	1-017-5338
VR101	1N758	T1	1N758
VR102	VR56	ST	VR56
	MISCELLANEOUS		
	Socker, CRT (TV 12)	BBRC	1-022-0427
	Fuseholder, Extractor Post, Fuse Size: 1/4 x 1-1/4	LF	342012
	Fuseholder, Extractor Post, Fuse Size: 9/32 x 1-1/4 (TV-B12 Only)	BUSS	Type HC M
	Low Voltage Circuit Board Assembly	BBRC	6-003-0459
	Main Chassis Circuit Board Assembly	BBRC	6-003-0500
	Main Chassis Circuit Board Assembly (TV-T12)	BBRC	6-002-0476
	Main Chassis Circuit Board Assembly (TV-TC12)	BBRC	6-002-0502

MONITOR PARTS LIST (Continued)

Symbol	Description	Mfg	Mfg. Part Number
	Main Chassis Circuit Board Assembly (TV-C12)	BBRC	6-002-0504
	Main Chassis Circuit Board Assembly (TV12), Tektronics)	BBRC	6-002-0506
	Cable Assembly; 8 inch	BBRC	6-004-0630
	Cable Assembly; 5 inch	BBRC	6-004-0631
	Power Supply Module (TV-12, 120VAC)	BBRC	6-003-0371
	Power Supply Module (TV-12, 220VAC)	BBRC	6-003-0372
	Power Supply Module (TV-B12, 120VAC)	BBRC	6-003-0368
	Power Supply Module (TV-B12, 220Vac)	BBRC	6-002-0370
	Deflection Coil Assembly	BBRC	6-004-0314
	Deflection Coil Assembly (TV-B12)	BBRC	6-004-0321
V1	CRT, 12Inch, P4 Phosphor	BBRC	1-014-0737
or	CRT, 12 Inch, P39 Phosphor	BBRC	1-014-0738
	Power Cable Assembly, 120VAC	BBRC	6-003-0645
	Power Cable Assembly, 220VAC	BBRC	6-003-0652

T-5105 DISPLAY ASSEMBLY PARTS LIST

Description	Mfg. Part No./ MIL Type Des.	Mfg. Code	Qty
MMDC Assembly w/o Keyboard	129350-1	LSI	1
Monitor	129302	LSI	1
Power Supply	129398-11	LSI	1
Printed Circuit Board Assembly	129360-1	LSI	1
Display Enclosure	129352-3	LSI	1
Wiring	129359	LSI	1
Top Chassis			1
Base Chassis			1
Rear Chassis			1
Fan Duct			1
Blower Bracket			1
Identification Plate			1
Blower	3-15-2450	HOWARD	1
Circuit Breaker	81504.5	LITTLEFUSE	1
Rocker Switch	TA101-TWB	CARLING	1
Pop Rivet	AD56ABS	USM	4
Pop Rivet	AD52ABS	USM	2
Pop Rivet	AD64ABS	USM	4
Nylon Spacer	Sp-73	WECKESSER	4
Nylon Nut	N-632-X	WECKESSER	4

T-5105 LOGIC BOARD PARTS LISTS

	Mfg. Part No./ MIL Type Des.	Mfg. Code	Qty.
Printed Circuit Board Assembly	129360-01	LSI	1
Printed Wiring Board	129360	LSI	1
Connector Bracket	128534-03	LSI	4
Voltage Reg Bracket	129389-04	LSI	1
Crystal	800-A4608.0 KHz	Standard	1
Crystal	800-A12492.5 KHz	Standard	1
Quad 2 NAND A14, B8, D19, F11, F16, F1y, H11, L5, K11	SN7400N	TI	9
QUAD 2 NAND B23, M5	SN74H00N	TI	2
QUAD 2 NAND (O.C) J6	SN74H0IN	TI	1
QUAD 2 NOR C8, C10, C11, C13, C14, C15, E11, E12, E12, F15, H9, H13, L7	SN7402N	TI	13
HEX 1 NAND B22, D15, E8, E15, H24, J13, J16	SN7404N	TI	7
HEX 1 NAND D24, K3, L3, M4	SN74H04N	TI	4
QUAD 2 AND A21, B2, B9, C2, F7, F18, K12, K15	SN7408N	TI	8
TRIPLE 3 NAND B16, H15, J15, J17, K9, K14, L4	SN7410N	TI	7

Description	Mfg. Part No./ MIL Type Des.	Mfg. Code	Qty
TRIPLE 3 NAND D23, E24, K7	SN74H10N	TI	3
DUAL 4 NAND B21, F10, J24	SN7420N	TI	3
HEX 1 NAND L1	SN74H04N	TI	1
QUAD 2 NAND (H.V.) F3	SN7426N	TI	1
TRIPLE 3 NOR B14, D14, E9, E14, J4, J11	SN7427N	TI	6
SINGLE 8 NAND J23, L8, L9	SN7430N	TI	3
SINGLE 8 NAND D23	SN74K30N	TI	1
QUAD 2 OR E10, F9, F12, F14, K8, K24	SN7432N	TI	6
DUAL 4 NAND BUFFER J3	SN74H40N	TI	1
ONE OF TEN DECODER S9, S13, A22, A23	SN7442N	TI	4
DUAL 2 AND/OR F13, H12	SN7451N	TI	2
DUAL D FLIP/FLOP C16, F4, H16, H17, H19, J10, K6, K13, K16, L6	SN7474N	TI	10
5 BIT COMPARATOR E19, E21, F23, H20 J21, J22	SN7485N	TI	6

Description	MFG. Part No. MIL Type Des.	Mfg. Code	Qty
QUAD 2 EXCLUSIVE OR D5, D6, E5, E6, E18, J7	SN7486N	TI	6
4 BIT BINARY COUNTER H7	SN7439N	TI	1
DUAL J-K FLIP/FLOP K2	SN74S113N	TI	1
DUAL J-K FLIP/FLOP B10, B11, B13, D16, D17, E16, E17, H10, H14, J2, J12, K4, K17	SN74H103N	TI	14
DUAL J-K FLIP/FLOP D18, K5	SN74H106N	TI	2
DUAL LINE RECEIVER L15, L17, M15, M17	SN75107AN	TI	4
DUAL ONE-SHOT A15, H3	SN74123N	TI	2
QUAD 1 BUFFER 3 STATE B3, B5, B6, B18, B19, B25, B26, C3, C5, C6, C18, C19 C21, C22, C25, C26, D21, D22, D25, D26, H25, H26	SN74125N	TI	22
DATA SELECTOR/ MULTIPLEXER A20, A25, C17, D8, E7, H2	SN74151N	TI	6
4 to 16 DECODER D10, D11	SN74154N	TI	2

T-5105 LOGIC BOARD PARTS LIST (Continued)

Description	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty
QUAD 2 to 1 LINE MULTIPLEXER D7, E20, F19, F22, H23 J20, K20, K21, K22	SN74157N	TI	9
4 BIT BINARY COUNTER F1, F24, F25, F26, H1, H18, J1, J18, J19, K1, K10, K18, L2	SN74161N	TI	13
8 BIT SHIFT REGISTER J14	SN74164N	TI	1
8 BIT SHIFT REGISTER M7	SN74166N	TI	1
QUAD D FLIP/FLOP 3-STATE L13, M13	SN74173N	TI	2
QUAD D FLIP/FLOP A24, D20, E22, E23, E25, E26, F5, F6, F21, H5, H6, K19, K23, L10, L12, M10, M12	SN7417SN	TI	17
4 BIT BINARY COUNTER B20, C20, F20, H21, H22	SN74193N	TI	5
QUAD LINE DRIVER A9, A11	MC1488L	MOTOROLA	2
QUAD LINE RECEIVER A10, A12A, A13	MC1489L	MOTOROLA	3
FIFO BUFFER C1	FR1502E	W DIGITAL	1
ASYNCH RECEIVER/ TRANSMITTER D1	TR1602B	W. DIGITAL	1

T-5105 LOGIC BOARD PARTS LISTS (Continued)

Description	Mfg. Part No./ MIL Type Des.	Mfg. Code	Qty.
QUAD 80 BIT SHIFT REGISTER L11, M11	2532B	SIGNETICS	2
RANDOM ACCESS MEMORY L19, L20, L21, L22, L23 L24, L25, L26, M19, M20, M21, M22, M23, M24, M25, M26	MK-4008-9P	MOSTEK	16
CHARACTER GENERATOR M8	129308-02	LSI	1
ROM J25	129309-01	LSI	1
POS. VOLT REG (+12)	MC7812P	MOTOROLA	1
NEG. VOLT REG (-5)	MC7905CP	MOTOROLA	1
NEG. VOLT REG (-12)	MC7912CP	MOTOROLA	1
PRINTED CIRCUIT BOARD	129390-21	LSI	1
BRIDGE	MDA 970-1	MOTOROLA	1
DIODE	IN914		
SOCKET STRIP	SB-25	ROBINSON-NUGENT	1
CAPACITOR			
24PF	DM-15-240	ELMENCO	
100PF	DM-15-101	ELMENCO	
.1μF	128518-104	LSI	14
.1μF, 50V	129329-104	LSI	2

T-5105 LOGIC BOARD PARTS LISTS (Continued)

Description	Mfg. Part No./ MIL Type Des.	Mfg. Code	Qty.
.1μF	128349-104	LSI	16
2.2μF	128518-225	LSI	1
8μF	128349-805	LSI	9
50μF	128349-506	LSI	1
150μF, 3V	TE-1061	SPRAGUE	1
1000μF, 35V	139329-108	LSI	2
RESISTOR			
150	128533-151	LSI	1
150 , 1/2 WATT	EB1515	A-B	1
200	128533-201	LSI	1
270	-271	LSI	1
300	-301	LSI	1
1K	-102	LSI	15
1.2K	-122	LSI	8
4.7K	-472	LSI	13
10K	128533-103	LSI	1
18K	-183	LSI	9
39K	-393	LSI	1
51K	-513	LSI	1
POTENTIOMETER			
100K	YQ383	CTS	1
500K	YQ384	CTS	1
SWITCH			
4P3T	MSS-4350R	ALCO	1
1P10T, BCD	1AZ 1600ZG	EECO	1
SOCKET			
CONNECTOR HOUSING J1, J6	17-304-01	AMPHENOL	2
SHORT, P.C.	17-1208	AMPHENOL	14
LONG, P.C.	17-1209	AMPHENOL	25
JACK	17-893	AMPHENOL	2
24 PIN	CA24S-10SD	CKT. ASSY	3

T-5105 LOGIC BOARD PARTS LIST (Continued)

Description	Mfg. Part No./ MIL Type Des.	Mfg. Code	Qty.
40 PIN	CA40S-10SD	CKT. ASSY	1
CONNECTOR			
WAFERCON, 9PIN, J4	09-18-5094	MOLEX	1
WAFERCON, 6 PIN, J5	09-18-5061	MOLEX	1
WAFERCON, 3 PIN, J7	09-18-5031	MOLEX	1
NUT			
HEX, STL, PLATED	4-40		8
Press	S0632-2	PEM	1
INSULATOR	43-77-2	THERM	2

T-5105 P.C. BOARD ASSEMBLY PARTS LIST

Qty.	Description	Part No.
	FIND NO. 1-13 Typical for All Assys.	
1	P.C. BOARD	-03
1	I.C.	128348-42
3	CAPACITOR .1μF	128349-104
3	CAPACITOR 8μF	128349-805
1	HEADER	WB-25-P
1	P-ROM 1R	129315-010
1	P-ROM 1L	129315-011
1	2R	-012
1	2L	-013
1	3R	-014
1	3L	-015
1	4R	-016
1	4L	-017
1	5R	-018
1	5L	-019
1	6R	-020
1	6L	-021
1	7R	-022
1	7L	-023
1	8R	-024

T-5105 P.C. BOARD ASSEMBLY PARTS LIST
(Continued)

Qty.	Description	Part No.
1	P-ROM 8L	129315-025
1	1R	-040
1	1L	-041
1	2R	-042
1	2L	-043
1	3R	-044
1	3L	-045
1	4R	-046
1	4L	-047
1	5R	-048
1	5L	-049
1	6R	-050
1	6L	-051
1	7R	-052
1	7L	-053
1	8R	-054
1	8L	-055
1	1R	-060
1	1L	-061
1	2R	-062
1	2L	-063

T-5105 P.C. BOARD ASSEMBLY PARTS LIST
(Continued)

Qty.	Description	Part No.
1	P-ROM-3R	129315-064
1	3L	-065
1	4R	-066
1	4L	-067