TEKTRONIX®

4051

GRAPHIC SYSTEM

SERVICE MANUAL

VOLUME 1

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

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CONTENTS

Section 1	INTRODUCTION	Page
	Purpose of Manual	1-1
	Standard Components	1-1
	4051 Graphic System	1-1
	Power Requirements	1-4
	Special Test Aids	1-6

Section 2	SPECIFICATIONS	Page
	Introduction	2-1
	Specifications	2-1
	Physical Measurements	2-1
	Environmental Specifications	2-2
	Power Specifications	2-2
	Operator Interface	2-3
	Alphanumeric Keyboard	2-4
	Line Editing Keys	2-6
	Program Development Keys	2-7
	Status Lights	2-7
	Display	2-8
	Magnetic Tape Unit	2-12
	Magnetic Tape Media	2-14
	Data Format and Recording Method	2-14
	Microprocessor System Specifications	2-16
	Motorola Devices	2-16
	Memory (ROM and Peripheral Devices)	2-17
	Memory (RAM for Program and Data Storage)	2-17
	Memory Address Allocation	2-17
	Bank Switch	2-19
	BASIC Language Format	2-19
	Line Number	2-19
	Keyword	2-20
	I/O Address	2-20
	General Purpose Interface Bus	2-24
	The GPIB Connector	2-24
	The GPIB Interfacing Concept	2-24
	GPIB Signal Definitions	2-26
	Data Bus	2-26
	Management Bus	2-26
	The Transfer Bus	2-27
	GPIB Data Formats	2-28
	Transferring ASCII Data	2-28
	Transferring Machine Dependent Binary Code	2-28
	Transferring One Data Byte at a Time	2-29

Section 2 SPECIFICATIONS (cont) Page

GPIB-to-IEEE Compatibility 2-29
Introduction 2-29
GPIB Interfacing Compatibility in Detail 2-30
General Purpose GPIB Commands 2-30

Section 3 MAINTENANCE Page
Routine Maintenance 3-1
General 3-1
Cleaning 3-1
Surface Cleaning 3-2
Cleaning the Fan Filter 3-2
Cleaning the Tape Head 3-2
Cleaning Electrical Contacts 3-3
System Verification Software 3-3
Cartridge Respooling 3-4
Static-Free Work Station 3-8
Disassembly/Assembly 3-11
Removing the Cover and Backpack 3-11
Keyboard Access 3-12
CRT Filter Access 3-16
CRT and Deflection Yoke Removal and Installation 3-17
CRT Removal 3-18
Deflection Yoke Replacement 3-21
CRT Installation 3-21
Power Supply Access 3-24
CPU Board/Memory Board Access 3-25
Display Board Access 3-25
Magnetic Tape Assembly Access 3-28

Section 4 4051 CALIBRATION Page
General 4-1
Power Supply 4-1
Display Calibration 4-4
Hard Copy Adjustments 4-7
Magnetic Tape Calibration 4-9

Section 5 TROUBLESHOOTING AIDS Page
General 5-1
4051 Troubleshooting Aids 5-2
Adjustment Locator Aids 5-5

Section 5 TROUBLESHOOTING AIDS (cont) Page

System Test Fixture 5-11
4051 Tests Using the System Test Fixture 5-12
System Test Fixture Switch Functions 5-12
4051 RAM Test 5-14
4051 ROM Test 5-18
4051 GPIB Test 5-21
4051 Display Test 5-25
4051 Tape Circuitry Test 5-27
Tape Tests—A Brief Description 5-31

Section 6 4051 CIRCUIT DESCRIPTION Page

System Architecture 6-1
System Addressing 6-7
4051 Timing 6-9
4051 Keyboard Operation 6-13
Indicator Lamps 6-17
Display Control 6-18
D/A Operation 6-20
Filter Operation 6-22
Long Vector Sense Circuit 6-23
Alphanumeric Display 6-24
Other Display Control Functions 6-24
Display Board 6-24
Display Board Blocks 6-27
Absolute Value Amplifiers 6-28
X^2 and Y^2 Amplifiers 6-29
Geometry Correction Multipliers 6-29
Deflection Amplifier 6-29
Storage and Erase Control Circuits 6-29
+175 Volt Supply 6-30
Erase Timing and CRT Voltage Levels 6-30
Target or Storage Backplate Control 6-31
Collimation Control 6-31
Flood Gun Control 6-32
High Voltage Circuits 6-32
High Voltage Regulator Oscillator 6-33
Focus Supply 6-33
Filament Supply 6-33
High Voltage Supply 6-33
Control Grid Supply 6-34
Intensity Control and Z Signal Amplifier 6-35

Section 6	4051 CIRCUIT DESCRIPTION (cont)	Page
	Hard Copy Operations	6-35
	Tape Unit	6-37
	General Purpose Interface Bus (GPIB)	6-46
	Power Supply Board	6-48
	Regulated Power Supplies	6-49
Section 7	BACKPACK CIRCUITS	Page
	Firmware Backpack (020-0147-00)	7-1
	Backpack Addressing	7-1
	Communications Backpack (021-0188-00)	7-4
	Communication Circuitry	7-4
	Communication Cable	7-8
	Self-Test Adapter	7-9
	Communication Interface Test "CMTEST"	7-9
Appendix A	INDEX OF SIGNAL NAMES	
Appendix B	MOTOROLA SPECIFICATIONS	
Appendix C	ASCII CODE CHART	
Index		
Change Information		

ILLUSTRATIONS

Figure	Illustration	Page
1-1	4051 Graphic System	1-3
1-2	Power Supply Transformer Shield	1-5
1-3	Replaceable power cords for the 4051	1-6
1-4	Special test aids for calibrating and troubleshooting the 4051 Graphic System	1-7
2-1	4051 Dimensions	2-1
2-2	Operator controls and system indicators	2-3
2-3	Default graphic coordinate limits	2-8
2-4	US ASCII Character Font (Upper Case Letters and Numbers)	2-9
2-5	US ASCII Character Font (Lower Case Letters)	2-10
2-6	US ASCII Character Font (Special Symbols)	2-11
2-7	NON-US ASCII Character Font (Special Symbols)	2-12
2-8	Standard data cartridge for the 4051	2-13
2-9	4051 magnetic tape cartridge recording format	2-15
2-10	4051 memory address space allocation map	2-18
2-11	GPIB connector(s) and pin assignments	2-25
2-12	GPIB bus structure diagram	2-26
2-13	Reading data from a device on the GPIB	2-31
2-14	Transmitting data to a device on the GPIB followed by the universal commands of UNTALK and UNLISTEN	2-32
2-15	A procedure to initiate data transfer between two GPIB devices and waiting until the data transfer is completed	2-33
3-1	Tape head and tape status light path	3-3
3-2	Cartridge assembly screws	3-5
3-3	Disassembling the tape cartridge	3-5
3-4	Tape positioning within the cartridge	3-6
3-5	Beginning the tape winding	3-7
3-6	Winding the tape	3-7
3-7	Assembling the tape cartridge	3-8
3-8	Typical static-free work station	3-9
3-9	Approved warning label for outside of shipping cartons	3-10
3-10	Cover mounting bolts	3-10
3-11	Cover removal	3-11

Figure	Illustrations (cont)	Page
3-12	Backpack removal.	3-12
3-13	Font coverplate removal to gain access to crt, keyboard, cpu board and memory board.	3-13
3-14	Keyboard screws.	3-14
3-15	Keyboard removal to gain access to cpu board and memory board.	3-15
3-16	CRT filter access and removal.	3-16
3-17	CRT neck shield, crt electrodes and yoke adjustment assembly.	3-18
3-18	CRT magnet ring location details.	3-19
3-19	Removing the crt faceplate mounting frame.	3-20
3-20	Lubrication and installation of the crt as part of the installation procedure.	3-22
3-21	Mounting the crt into the 4051.	3-23
3-22	Power supply removal procedure.	3-24
3-23	Screw pairs securing the cpu board.	3-26
3-24	Service layout for cpu board and memory board.	3-27
3-25	CRT writing gun connector removal.	3-27
3-26	Tape unit assembly with pointers to the mounting screws.	3-28
4-1	Remove the cover from the 4051 to gain access to most of the circuit adjustments.	4-2
4-2	Power supply check points and adjustments.	4-3
4-3	Display board check points and adjustments.	4-4
4-4	CRT shield with tag showing recommended electrode voltages. The deflection yoke adjustment rabs are also illustrated.	4-5
4-5	Intensity adjustments underneath the 4051.	4-6
4-6	Hard copy threshold with no information stored on the 4051 display.	4-8
4-7	Tape unit check points and adjustments.	4-10
4-8	Magnetic tape skew waveforms.	4-11
4-9	Magnetic tape signal for tape head height (right-to-left position) adjustments.	4-13
5-1	Test fixture for use with the 4051 Graphic System.	5-2
5-2	Rear panel check points and connectors.	5-5
5-3	Power supply check points and adjustments.	5-6
5-4	CRT electrodes, yoke adjustment and power line strapping tables.	5-7
5-5	Display board checkpoints and adjustments.	5-8
5-6	Cursor and character intensity adjustments.	5-9
5-7	Tape unit check points and adjustments.	5-10
5-8	4051 cpu board and memory board brought outside the system for component servicing.	5-11

Figure	Illustrations (cont)	Page
5-9	RAM test	5-15
5-10	RAM test	5-15
5-11	RAM test	5-15
5-12	RAM test	5-16
5-13	Random access memory (RAM) layout for the cpu board.	5-17
5-14	Random access memory (RAM) layout for the memory board.	5-17
5-15	ROM test	5-18
5-16	ROM test	5-19
5-17	ROM test	5-19
5-18	ROM test	5-19
5-19	GPIB test	5-21
5-20	GPIB test	5-22
5-21	GPIB test	5-22
5-22	GPIB test	5-23
5-23	Display test	5-25
5-24	Display test	5-25
5-25	Display test	5-26
5-26	Display test	5-26
5-27	Tape Test	5-27
5-28	Tape Test	5-29
5-29	Tape Test	5-29
5-30	Tape Test	5-29
6-1	4051 Graphic System block diagram.	6-2
6-2	Peripheral Interface Adapter (PIA) block diagram.	6-5
6-3	Asynchronous Communications Interface Adapter (ACIA) block diagram.	6-6
6-4	Memory allocation map for the 4051.	6-8
6-5	Block diagram of system timing circuits.	6-9
6-6	Processor timing.	6-10
6-7	Memory refresh timing.	6-11
6-8	Keyboard timing.	6-11
6-9	Tape write timing circuits—block diagram.	6-12
6-10	Tape timing for writing data to the tape.	6-12
6-11	Keyboard control circuitry block diagram.	6-13
6-12	Indicator board control circuitry.	6-18
6-13	Display control circuitry block diagram.	6-19
6-14	Typical D/A converter using proportioned resistors and a current summing amplifier.	6-20
6-15	Data and information flow through the X and Y digital-to-analog converters.	6-21

Figure	Illustrations (cont)	Page
6-16	Filter circuit to provide vector writing delay on the X axis.	6-22
6-17	Vector filtering response curves.	6-22
6-18	Long vector sense circuit.	6-23
6-19	Display board block diagram.	6-25
6-20	Direct view storage tape (DVST) crt schematic.	6-26
6-21	Transconductance amplifier for dynamic focus and geometry correction.	6-28
6-22	Erase timing and voltage waveforms.	6-30
6-23	A typical voltage doubler network.	6-33
6-24	Z axis control grid circuitry used to regulate the writing beam intensity.	6-34
6-25	Wavefrom used to establish the crt control grid voltage level.	6-34
6-26	Hard copy circuitry block diagram.	6-36
6-27	Block diagram of the 4051 tape drive control circuitry.	6-38
6-28	Magnetic tape recording format.	6-39
6-29	Timing signals for writing data to tape.	6-40
6-30	Tape drive read/write circuits on the tape drive board.	6-43
6-31	Peak detection amplifier operation.	6-44
6-32	Block diagram of tape status and motor drive circuitry.	6-45
6-33	Block diagram for general purpose interface bus (GPIB) circuitry on the 4051.	6-48
7-1	Block diagram of the Firmware Backpack circuitry.	7-2
7-2	Communication Interface Block Diagram.	7-5
7-3	Communication cable for the 4051 Communication Backpack.	7-8
7-4	Self-test adapters for use with the communication backpack.	7-9
7-5	Message displayed on the crt for "CMTEST" when no self test adapter is installed.	7-10
7-6	Active data lines, expected transitions and expected data during the first test in the "CMTEST" program.	7-11
7-7	Display output of "CMTEST" when the self-test adapter is used and no errors are present.	7-11

TABLES

Number	Name of Table	Page
2-1	Magnetic Tape Format Specifications	2-16
2-2	System Building Blocks	2-17
2-3	Bank Switch Data Word	2-19
2-4	Device Number Assignments	2-20
2-5	Internal Device Numbers	2-21
2-6	GPIB Primary Device Address Assignments	2-22
2-7	GPIB Secondary Address Assignments	2-23
5-1	Hexadecimal-to-Binary	5-12
5-2	Size of 4051 Systems	5-16
5-3	4051 Firmware Checksums	5-20
5-4	Checksums for Backpack ROMS	5-20
5-5	Communication Backpack	5-21
6-1	Data Equivalence For Decimal, Hexadecimal and Binary Codes	6-3
6-2	Key Codes (KC0 Thru KC6) For The 4051 Keyboard	6-14
6-3	Mag Tape Format Specifications	6-41
7-1	Bank Switch and Peripheral Control Addresses	7-1
7-2	Bank Switch Select Data	7-3
7-3	RS-232 Definitions	7-5
7-4	Oscillator Frequency	7-6
7-5	Frequency Dividing Counter	7-6
7-6	Baud Rate Selection	7-6
7-7	Bits 1-0 Specify Baud Rate Clock Division	7-7
7-8	Bits 4-2 Specify Parity Encoding/Decoding	7-7
7-9	Bits 6-5 Enable or Disable Transmit Buffer Empty Interrupt and Break—Spacing of Data Transmission	7-7
7-10	Bit 7 Controls the Read Buffer Full Interrupt	7-8

Fig. 1-1. 4051 Graphic System.

Section 1

INTRODUCTION

PURPOSE OF MANUAL

The purpose of this manual is to provide a service technician with the required data for performing routine maintenance on a 4051 Graphic System. It is also intended to be a guide for troubleshooting and repairing 4051 Graphic Systems that require service.

The service documentation is divided into two volumes. Volume 1 provides preventive maintenance information, calibration and adjustment procedures, troubleshooting and service information, specialized test procedures, and descriptions of circuit operation for the 4051. Portions of the text refer to schematics and diagrams found in Volume 2.

Volume 2 contains system block diagrams, timing diagrams, schematics, cross reference tables, wire lists, and replaceable parts lists for the 4051 Graphic System and attached devices. Service information for peripheral products is to be found in the appropriate manual written for the peripheral product.

STANDARD COMPONENTS

Standard components of the 4051 include the following:

(1) Full ASCII keyboard, plus calculator key pad, user-definable keys, and editing keys.

(2) 11" DVST (direct view storage tube) display with a capacity of 35 lines of alphunumeric characters, 74 characters per line. Vector resolution is approximately 120 points per inch.

(3) A magnetic tape unit, capable of storing 300K bytes of data and organized into a sequential-file structure. Tape format is programmable to support TEKTRONIX 4923-type tapes as well as 4051-type tapes.

(4) A GPIB bus connector, allowing interfacing to devices compatible with IEEEE standard #488-1975.

(5) Joystick connector, allowing the user to input graphic coordinates with optional joystick.

(6) Hard copy compatibility, allowing the user to obtain a copy of the displayed information via an optional TEKTRONIX 4631 or 4610 Hard Copy Unit.

4051 GRAPHIC SYSTEM

The TEKTRONIX 4051 (Fig. 1-1) is a desk-top unit that combines the visual display of a graphic terminal with the computational power of a scientific probrammable calculator. The 4051 can be used as a stand-alone programmable calculator, or, with the addition of the optional Communications Backpack, as an intelligent graphic terminal. The standard 4051 contains an eight-bit microprocessor, an 8K byte random access memory, an eleven-inch direct-view storage tube (with hardcopy compatibility), a built-in magnetic tape unit, and an extended BASIC language interpreter. The 4051 can handle the same processing functions normally handled by other computer-based computational systems.

The 4051 keyboard is the primary input device. The keyboard is similar to a TEKTRONIX 4012 terminal keyboard with a separate numeric keypad for data entry. Editing keys, peripheral control keys, and 10 user-definable keys are also included.

BASIC language statements are used to program the 4051. The 4051 BASIC language is an extended version of the Dartmouth College Timeshare BASIC (Beginner's All-purpose Symbolic Instruction Code) with extensions in the areas of graphic primitives, unified I/O handling of the General Purpose Interface Bus (GPIB), matrices, strings, and high level language interrupt handling.

Keyboard entries are displayed on an eleven-inch direct-view storage tube (DVST). Both upper and lower case letters are printed with a maximum of 72 characters per line. The display also features full graphic capability. Drawing lines (called vectors) on the screen is accomplished by typing BASIC graphic commands from the keyboard or executing BASIC statements under program control. The storage tube is hard copy compatible, which allows an attached hard copy unit to make a paper copy of displayed information. (The hard copy unit is optional.)

The 4051 memory is divided into a Random-Access Memory (RAM) and a Read Only Memory (ROM). The standard RAM has an 8K byte storage capacity of which 6K bytes are accessible by the user for storing programs and data. The RAM storage capacity can be increased up to 32K bytes by adding optional 8K byte memory increments.

The 4051 ROM has 36K locations that hold processor firmware, peripheral control addresses, and an 8K byte section for firmware bank swapping used by extended firmware modules (i.e., ROM packs). The Firmware Backpack or the optional Communications Backpack each provides the user with two slots for ROM packs. With the use of a device called a ROM Expander unit, the number of available ports for ROM packs can be increased to sixteen. The microprocessor has access to code in the ROM packs through use of a bank switch scheme.

Data and program instructions can be transferred onto magnetic tape and reentered into the RAM via a built-in magnetic tape unit. The storage medium is a standard data cartridge with approximately a 300K byte capacity depending upon the length of each data file.

Four rear panel connectors allow the 4051 to interface to a variety of peripherals. The General Purpose Interface Bus (GPIB) connector allows the 4051 to exchange data with devices such as disk storage units, digital X-Y plotters, and instrumentation systems. Data transfers over the GPIB are in byte-serial, bit parallel format (eight bits per byte). The GPIB is compatible with the IEEE Standard #488-1975.

Another rear panel connector is part of the optional Communications Backpack and is compatible with RS-232 devices (i.e., computer modems). This allows the 4051 to exchange data with devices such as computer terminals, printers, and modems. The RS-232 communications interface features asynchronous full-duplex or half-duplex operation. Data exchange rate is selectable by the user through program control for one of the following: 110, 150, 300, 600, 1200, or 2400 baud.

The other two connectors are utilized by an optional joystick and a Hard Copy Unit.

Power Requirements

The 4051 Graphic System will perform properly at 50 Hz or 60 Hz line frequencies using voltages of 120 Vac or 220 Vac. The 4051 is normally shipped from the factory strapped for 120 Vac operation. To convert the 4051 to 220 Vac operation, the cover of the 4051 must be removed; the transformer jumpers must be changed in accordance with a table inscribed on the transformer shield (Fig. 1-2); a 0.8 ampere line fuse must be installed; and a 220 volt power cable must be used (Fig. 1-3).

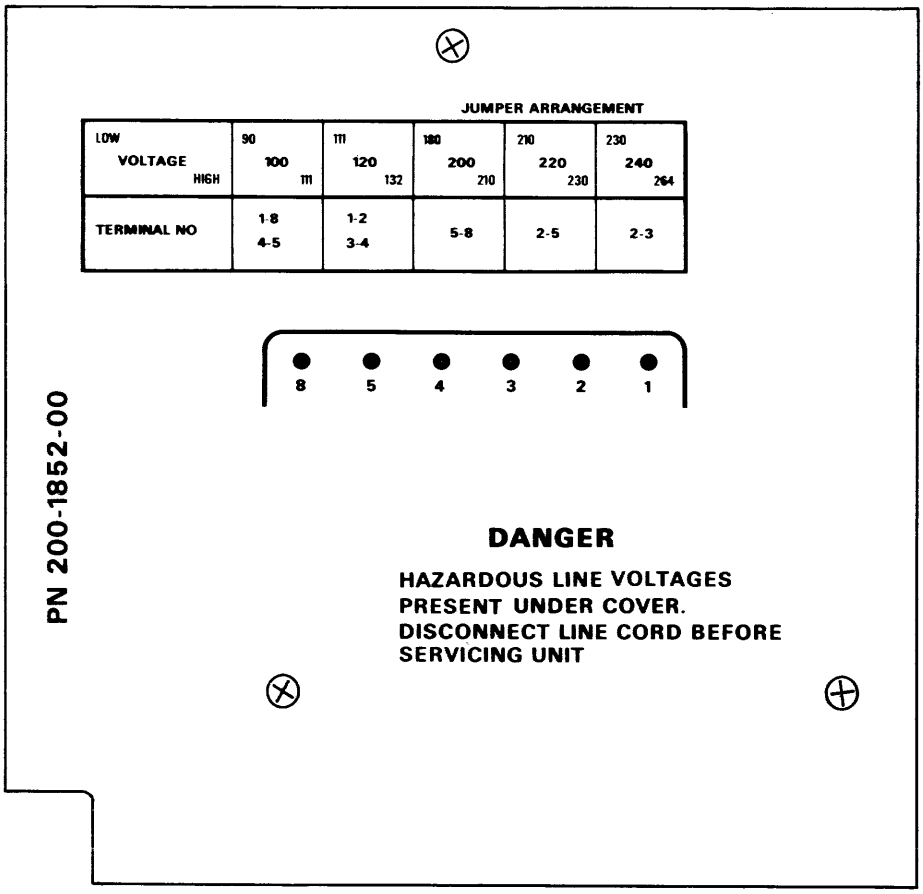


Fig. 1-2. Power Supply Transformer Shield.

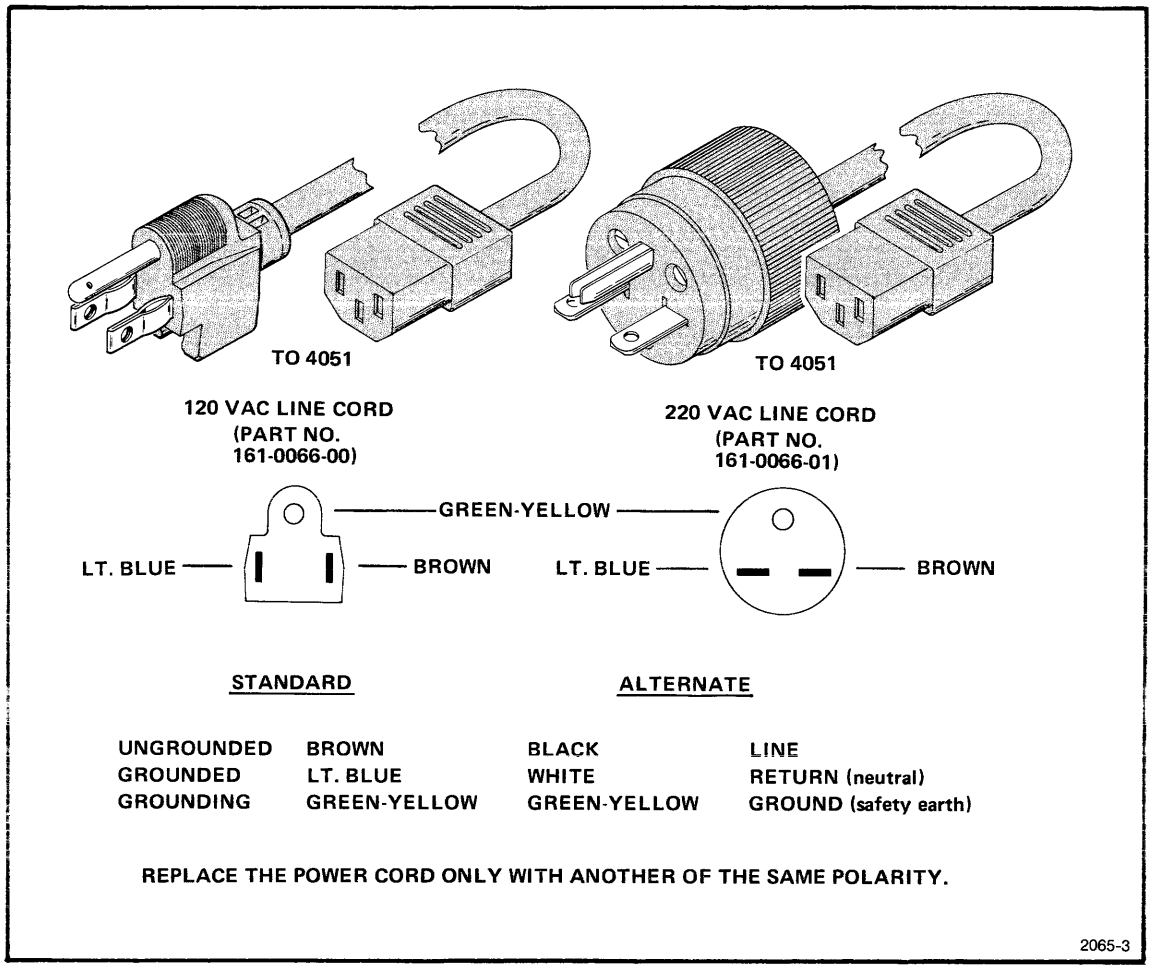


Fig. 1-3. Replaceable power cords for the 4051.

Special Test Aids

Most troubleshooting of 4051 electronics can be performed using standard general purpose test equipment found in most repair stations. A number of test and adjustment procedures require special test figures (Fig. 1-4) and devices; therefore, Tektronix has developed a calibration tape to help align and calibrate the magnetic tape unit, and a 4051 Test Fixture to exercise the Motorola 6800 microprocessor and perform tests on memory.

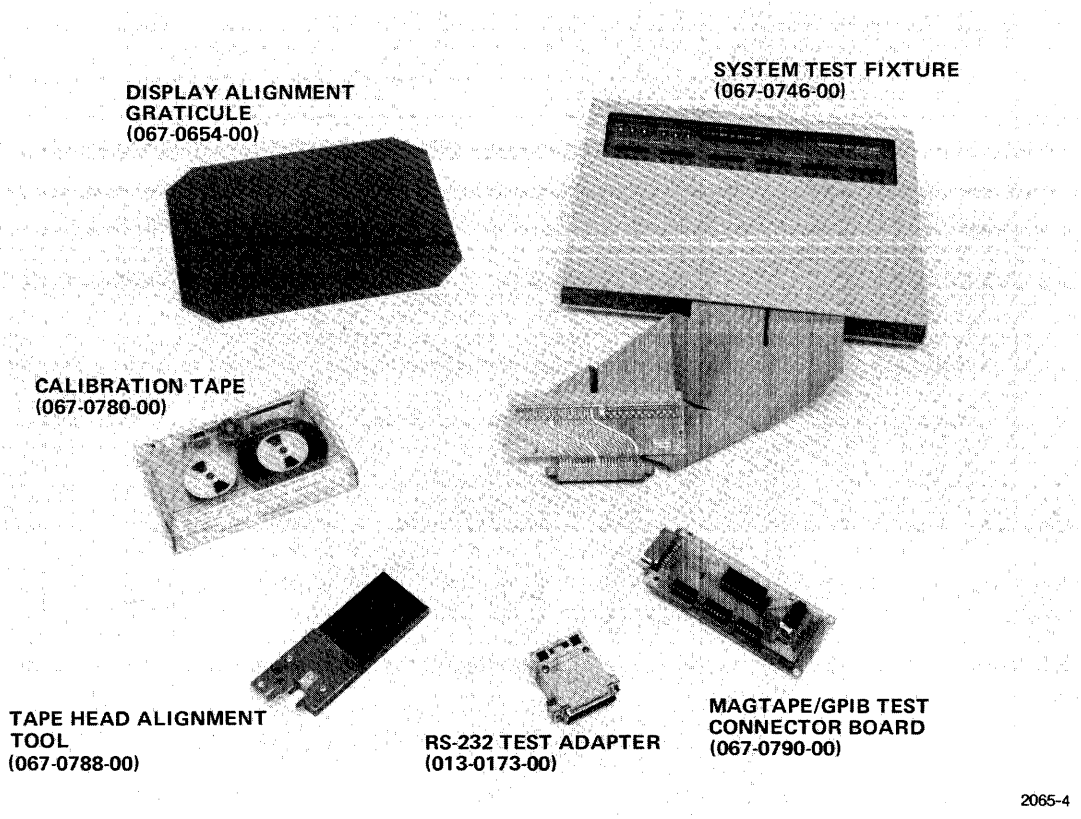


Fig. 1-4. Special test aids for calibrating and troubleshooting the 4051 Graphic System.

Section 2

SPECIFICATIONS

INTRODUCTION

This section gives a brief review of 4051 operations with special emphasis placed on physical and electrical specifications of the system. Hardware performance specifications are tabulated for quick reference. Some explanatory text is also incorporated. BASIC language statements are described in detail in the *4051 Graphic System Reference Manual*. Refer to the Reference Manual for detailed operation information. (Duplication of information is not the intent of the service documents.)

SPECIFICATIONS

PHYSICAL MEASUREMENTS

Dimensions (see Fig. 2-1)

Length	30.75 inches or 78.1 cm
Width	18.25 inches or 46.4 cm
Height	13.625 inches or 34.6 cm

Shipping Weight

80 pounds or 36.3 kg

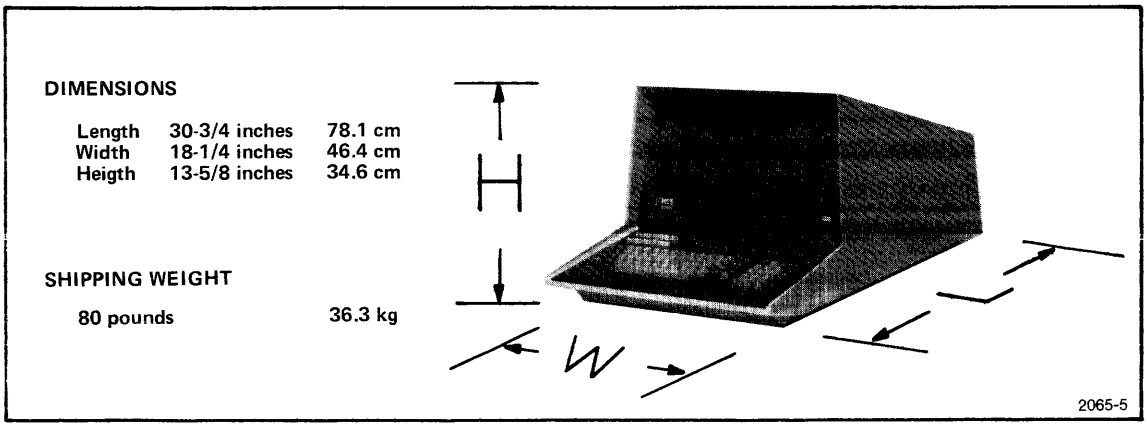


Fig. 2-1. 4051 dimensions.

ENVIRONMENTAL SPECIFICATIONS

Temperature

Operation	+10° C to +40° C
Storage	−40° C to +65° C (tape limited to +45° C)

Altitude

Operating	to 15,000 feet
Storage	to 50,000 feet

Humidity (maximum)

Operating	80% non-condensing (tape limited to 20% min. and 80% max.)
Storage	95% non-condensing (tape limited to 20% min. and 80% max.)

Shock

Non-operating	30 g's.

POWER SPECIFICATIONS

Line Voltages

Voltage	Fuse
100 V ±10%	1.6 A medium-blow
120 V ±10%	1.6 A medium-blow
200 V +5% −10%	0.8 A medium-blow
220 V ±5%	0.8 A medium-blow
240 V +10% −5%	0.8 A medium-blow

Maximum Line Voltage

132 Vac or 264 Vac

Line Frequency Range

48 Hz to 66 Hz

Power Comsumption

200 watts maximum

Dielectric Breakdown Greater than 2000 Vac RMS (60 Hz) between power line and accessible conductive components.

Power Supply Voltages

Voltage	Regulation	Ripple[1]	Current Demand	Current Limit
+5.1 V ±2%	±1%	5 mV	4.0 A	4.5 A
+12 V ±5%	±3%	5 mV	450 mA	1.0 A (temp. dep.)
+15 V ±1%	±0.2%	5 mV	200 mA	600 mA
+20 V	unreg.		3 A	3 A fused
+185 V	unreg.		100 mA	
+295 V	unreg.		50 mA	
−12 V ±2%	±0.5%	5 mV	250 mA	600 mA
−20 V	unreg.		3 A	3 A fused
40 V (−20 to +20) ±10%	unreg.		400 mA	

[1]**Note: Ripple is measured at the supply with X1 probe on 7A26 limited to 20 MHz, with probe GND connected to supply chassis, load was resistive dummy drawing at current demand specified from all supplies.**

OPERATOR INTERFACE

The front of the 4051 is divided into ten functional areas. These areas are illustrated by Fig. 2-2.

A display screen is used to present both graphic and alphanumeric or program information in a visible form.

The internal tape is used to store BASIC language program statements and data of various types on an industry-standard data cartridge.

The status indicator lights tell when power is applied to the system, when the system is busy doing calculations, when the system is performing input/output operations, and when waiting to stop at the end of the current BASIC language instruction in response to pressing the BREAK key.

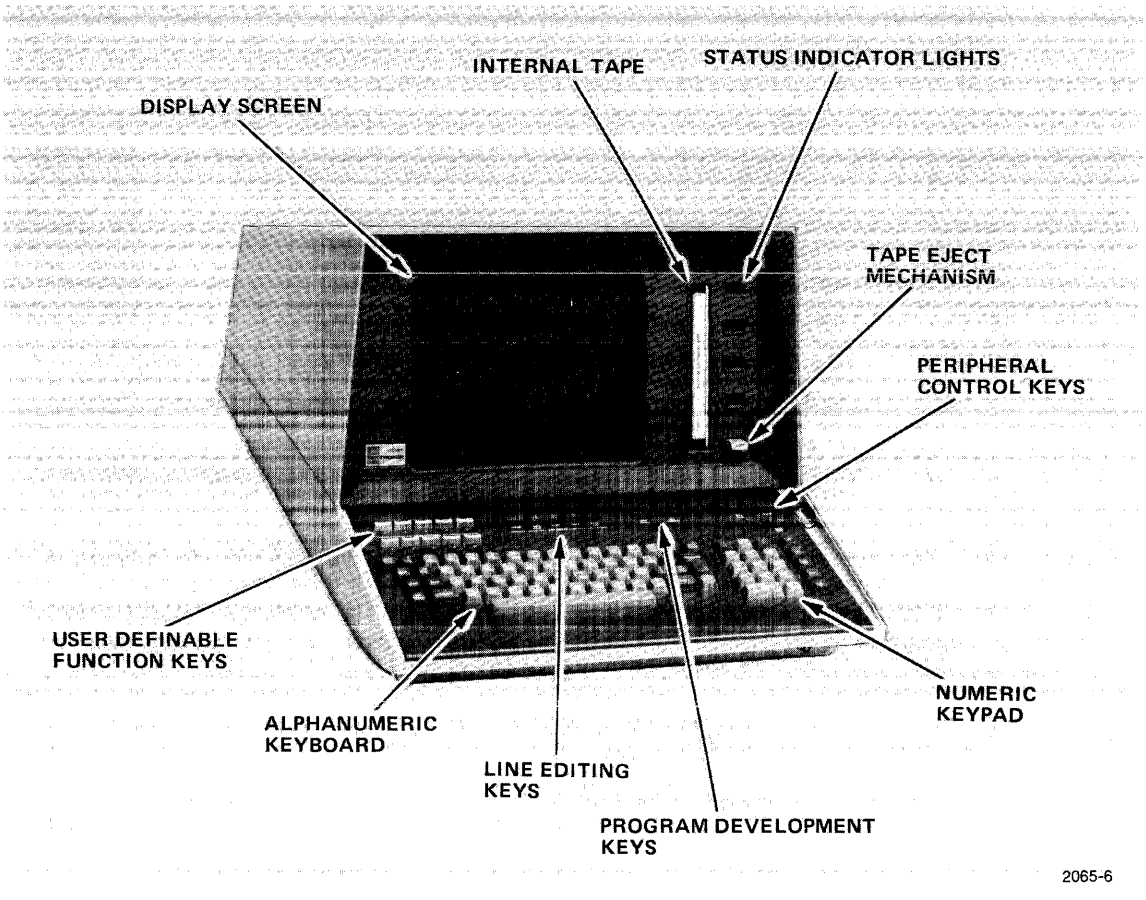


Fig. 2-2. Operator controls and system indicators for 4051 Graphic Systems.

The eject mechanism removes a tape cartridge from the 4051 Graphic System internal tape unit.

User-definable function keys allow the operator to branch to any of 20 specified BASIC program locations when pressing one of these keys. There are ten keys to specify ten program locations. Another ten locations are used if the keys are pressed in conjunction with holding down a SHIFT key.

The alphanumeric keyboard is used for entry of BASIC program language statements and data. If a communication backpack is installed on your 4051, these keys can be used for data entry into a host computer.

Line editing keys allow convenient editing of BASIC program statements without having to retype the entire command string.

Program development keys can be used to sequentially enter BASIC statement numbers when programs are being created or modified. They can also be used to debug or troubleshoot a BASIC language program.

The numeric keypad provides convenience when entering numeric data into the system. The basic calculator functions are also readily available. When used as a calculator without running a BASIC program, the RETURN key causes the calculated result to print on the display.

Peripheral control keys offer limited control of the tape unit and optional Hard Copy Unit.

ALPHANUMERIC KEYBOARD

ALPHANUMERIC KEYS	The alphanumeric keys (letters, numbers and symbols) are used to enter BASIC statements and generate ASCII control characters. Keys 0-9 can also be used to enter numeric data.
SPACE BAR	When the space bar is pressed, the display cursor moves one horizontal space to the right. No character is printed. If the cursor is at the right margin, no operation is performed.
SHIFT	This key is similar to the SHIFT key on a typewriter keyboard. It determines which one of two characters are printed when an alphanumeric key is depressed. If used alone, this key brings the display out of Hold Status.
TTY LOCK	Causes all lower case letters to be transformed to upper case when keyed.

TAB	When this key is pressed, the keyboard issues the ASCII control character TAB, regardless of the SHIFT key position. When the TAB function is executed, the display cursor moves to the right and stops in column 1, 19, 37, 55, 1, etc. TAB spacing can be modified if a PRINT USING statement is executed.
CTRL	When pressed in combination with a letter key and sometimes the SHIFT key, the keyboard issues an ASCII control character. At statement entry time, all control characters are echoed to the display as an underlined letter (except for CR and RUBOUT). At statement execution time, some control characters cause machine display functions to be executed.
ESC	When this key is pressed, the keyboard issues the ASCII control character ESC regardless of the SHIFT key position.
HOME PAGE	If pressed alone, the display is erased and the cursor returns to the Home position. If pressed in combination with the SHIFT key, the cursor returns to the Home position and the display is not erased.
BACK SPACE	Moves the cursor to the left by one space.
RETURN	Pressing this key generates an ASCII control character CR (Carriage Return). The display cursor returns to the left margin and moves one vertical space down. This key causes the machine to evaluate the information on the previous line. If the line contains a line number, the statement is entered into memory and is not executed. If the statement does not contain a line number, it is executed immediately.
RUBOUT	Pressing RUBOUT usually causes the display cursor to move one space to the left and write a full 5 x 8 dot matrix over any character in that location. The character underneath the cursor is logically removed from memory and replaced by the space character. The next time the line is printed, a space appears instead of the 5 x 8 matrix. If the cursor is over a non-blank character, the cursor does not move but rubs out the present position.
BREAK	The first time the BREAK key is pressed, the BREAK indicator on the front panel lights up and the machine stops program execution after the present line is completed. This is referred to as a "BREAK pending" condition. The indicator goes out when the program halts. If the BREAK key is depressed while the BREAK light is on, program execution is aborted immediately and the program line pointer returns to the starting position.

LINE EDITING KEYS

The five program line editing keys at the top center of the keyboard are each dual purpose. The primary function is lettered below each key while the secondary function is printed above each key.

The primary function is performed by pushing the key directly. The secondary function is performed by pressing the key and at the same time holding the SHIFT key. All operations are performed on the current line which is stored in a 72-character line buffer.

EXPAND	This key is used for insert operations. All characters to the right of the cursor, including that character where the cursor is positioned, are moved to the extreme right of the line buffer. On the screen, the line appears to split into left and right portions separated by a gap. The cursor finishes at the extreme left of the gap. Characters may now be inserted.
COMPRESS	This key (actually the simultaneous pushing of the EXPAND key and SHIFT key), is the inverse of EXPAND. COMPRESS removes adjacent spaces to the right. The portion of line to the right of the screen is shifted to the current position of the cursor.
BACKSPACE	This key moves the cursor one character position to the left.
RUBOUT ←	This key is equivalent to pressing RUBOUT.
SPACE	This key is equivalent in function to the SPACE bar on the main keyboard and is provided in this set for convenience. The cursor is positioned one character space to the right until the right margin is reached.
RUBOUT →	This key is equivalent to RUBOUT except it moves to the right instead of to the left.
CLEAR	CLEAR empties the contents of the current line buffer without affecting information already stored in RAM.
REPRINT	This key duplicates the current contents of the line buffer one position below the current display. The position of the cursor relative to the buffer is unchanged. This is a useful key to use when, due to overwriting, the storage display is difficult to read.
RECALL LINE	This key recalls a program line previously stored in RAM. The number of the line to be recalled is entered prior to pushing this key. The line is called and the cursor finishes one position beyond it.
RECALL NEXT LINE	This key is similar in function to the RECALL LINE, but instead of calling the line with the line number currently in the display, the line with the next greater number is called.

PROGRAM DEVELOPMENT KEYS

AUTO NUMBER

The AUTO NUMBER function is provided as an operator convenience during program statement entry time. Pressing the key once places the 4051 in a mode where line numbers are automatically provided for each BASIC statement entry from the keyboard. The first time the key is pressed, line number 100 is placed in the line buffer and appears on the display. The operator enters a BASIC statement and presses the RETURN key. The machine then places line number 110 in the line buffer for the next statement entry. The line number increment is automatically set at 10. To start the auto number sequence with a line number other than 100, the line number is entered into the line buffer from the keyboard and then the AUTO NUMBER key is pressed. The 4051 then provides line numbers from that starting point in increments of 10. To exit the auto number mode, the operator presses the AUTO NUMBER key again.

STEP PROGRAM

The STEP PROGRAM key causes the 4051 to execute the current BASIC program one step at a time. Each time the key is pressed, one line in the program is executed. This feature allows the keyboard operator to monitor the execution sequence of the program during debugging operations. Normally, the program starts one step execution from the beginning; however, the program line counter can be set to any line in the program by using the GOTO statement and then pressing the STEP PROGRAM key causes one step execution from that point. For example, entering GOTO 500 and pressing the RETURN key sets the program line counter to line number 500. The program can then execute one step at a time from that point by pressing the PROGRAM STEP key again and again.

AUTO LOAD

The AUTO LOAD key causes the internal magnetic tape unit to rewind and load a BASIC program from the magnetic tape cartridge into the Random Access Memory. There must be a valid ASCII program stored on the tape, otherwise an error occurs.

REWIND

Pressing the REWIND key causes the 4051 to rewind the tape cartridge in the internal magnetic tape unit. Pressing the REWIND key is the same as executing the BASIC statement FIND 0.

MAKE COPY

Pressing the MAKE COPY key causes an attached Hard Copy Unit to make a paper copy of the information on the 4051 display. Pressing this key is the same as executing the BASIC statement COPY.

STATUS LIGHTS

BUSY

4051 is busy transferring or processing data.

I/O

Input/output operations are in progress.

BREAK	A break in program execution is pending. The BREAK light goes out after program execution halts at the end of the current line.
POWER	Indicates that power is supplied to the 4051.

DISPLAY

The display is an 11 inch Direct View Storage Tube (DVST) crt.

HOLD STATUS	Reduced intensity after 90 seconds of no display activity occurs to maintain the currently stored image for redisplay.
AUTOMATIC ERASE	After 30 minutes of idle machine time, the crt erases.
GRAPHICS	Coordinates are specified by a pair of decimal fractions. The default coordinate limits are 0—100 on the vertical (Y) axis and 0—130 on the horizontal (X) axis (Fig. 2-3). Vectors are drawn using MOVE and DRAW commands to move the writing beam to a specified coordinate location or to draw a line from the current beam reference position to the indicated coordinate location. The coordinate limits can be changed by executing the WINDOW command. Resolution is approximately 120 points per inch.

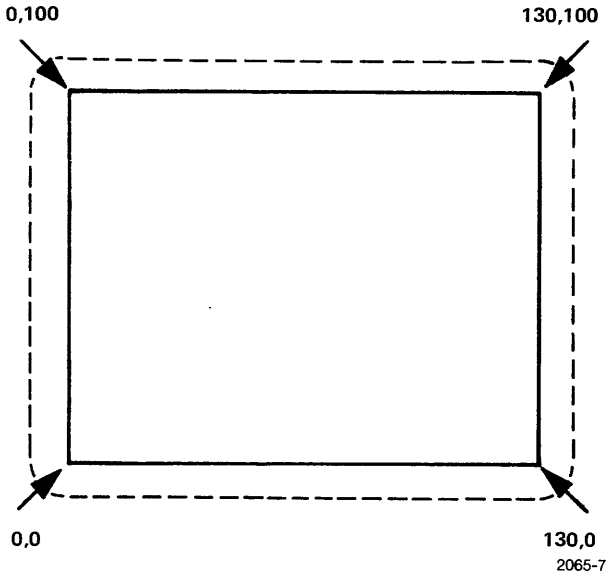


Fig. 2-3. Default graphic coordinate limits.

ALPHANUMERIC CHARACTERS	Full ASCII 96 printable characters set (upper and lower case) printed using a 5 X 8 dot matrix (see Figures 2-4, 2-5, 2-6 and 2-7). 72 characters/line 35 lines/display 2590 characters/display Automatic return and linefeed (CR-LF) at the right margin to display lines longer than 72 characters in length.

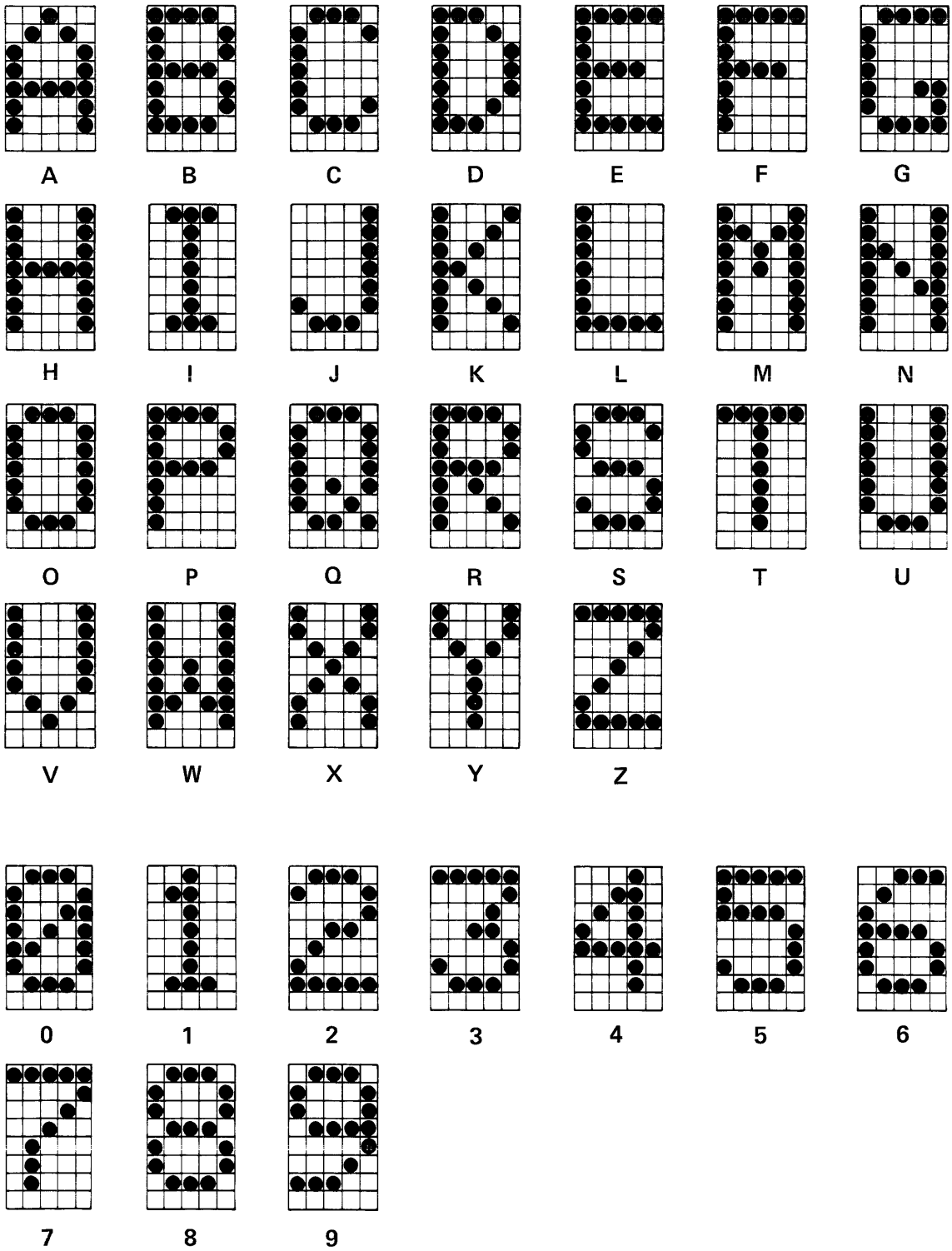


Fig. 2-4. US ASCII Character Font (Upper Case Letters and Numbers).

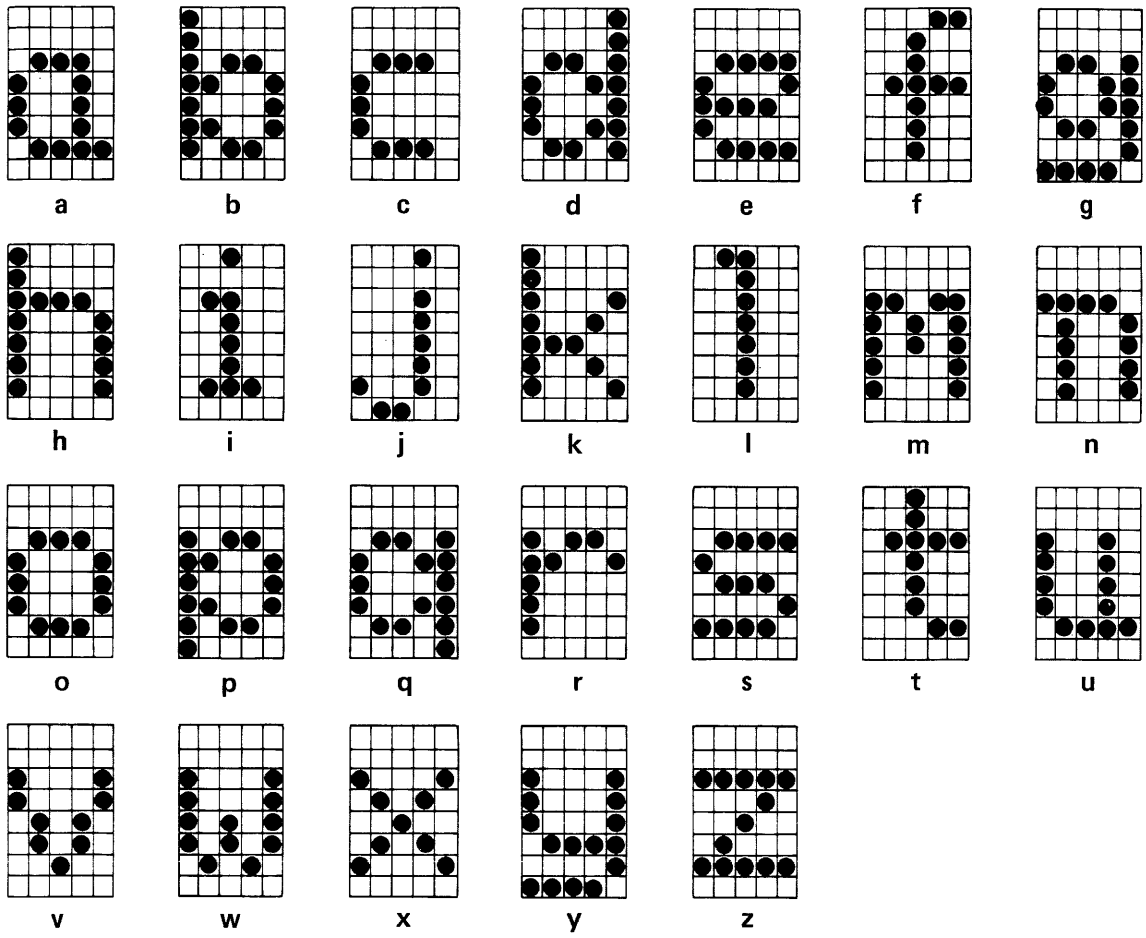


Fig. 2-5. US ASCII Character Font (Lower Case Letters).

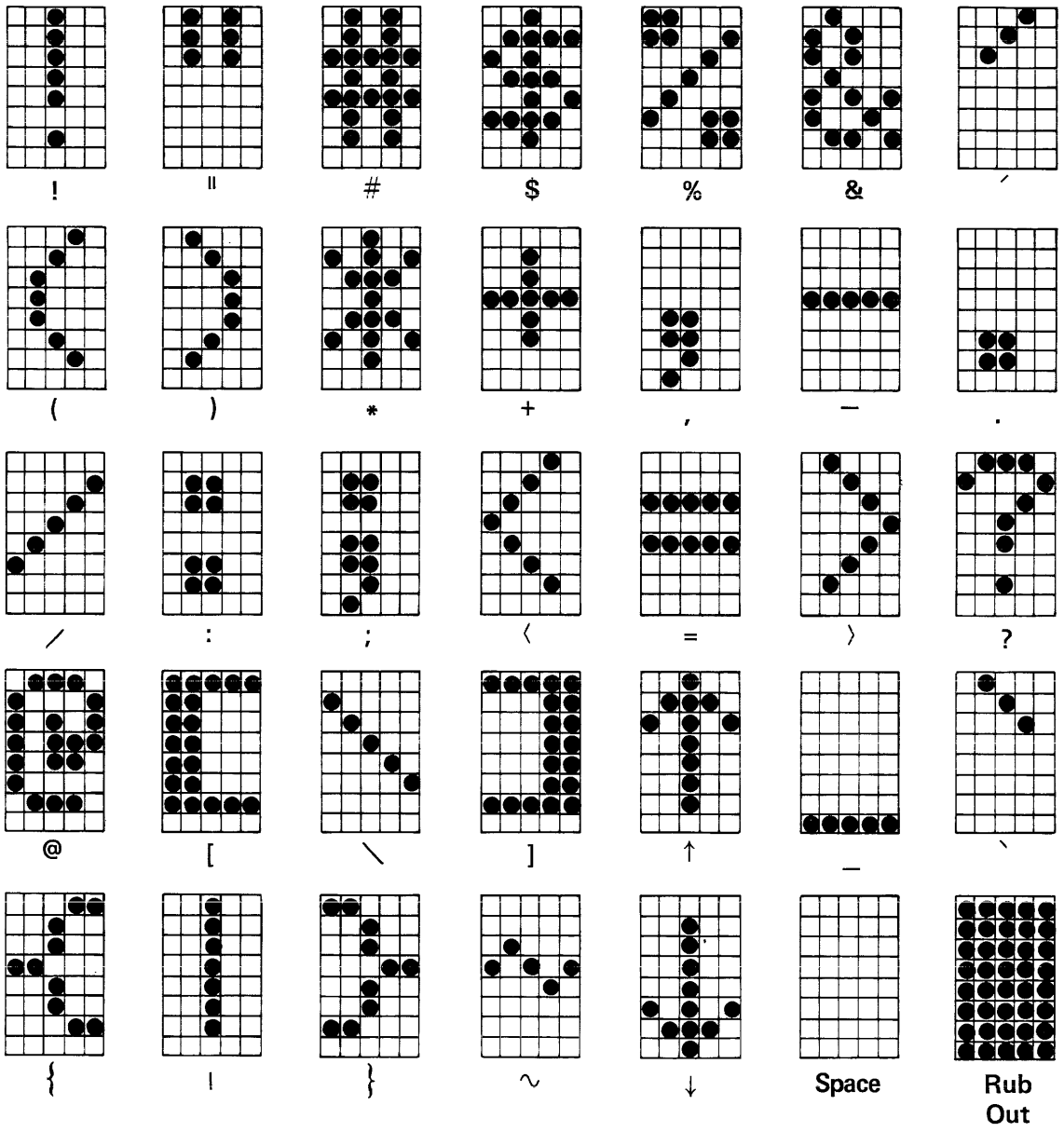


Fig. 2-6. US ASCII Character Font (Special Symbols).

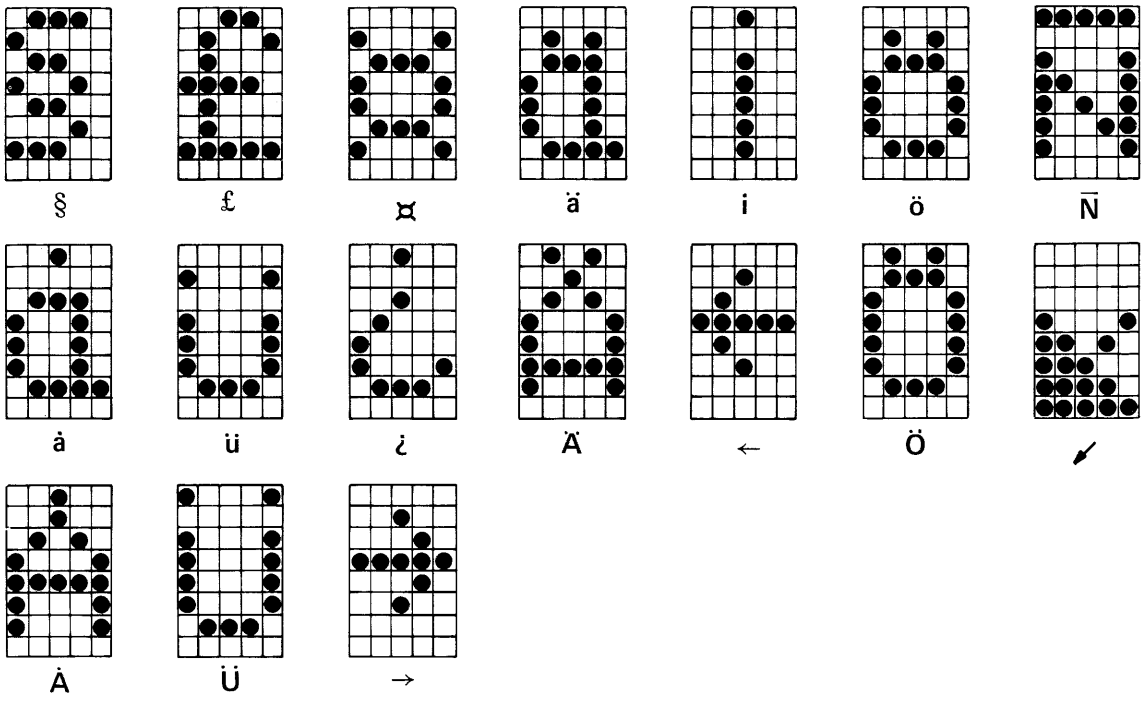


Fig. 2-7. NON-US ASCII Character Font (Special Symbols).

MAGNETIC TAPE UNIT (Built In Unit)

The tape unit uses an industry standard data cartridge with approximately 300 feet of 1/4 inch computer grade tape having a storage capacity of 300K bytes of data (Fig. 2-8).

Input/output operations with the tape unit are normally performed by executing the BASIC language commands FIND, OLD, SAVE, APPEND, INPUT, OUTPUT, PRINT, READ, and WRITE. Many of the commands require the tape unit address @32. Two keyboard keys, REWIND and AUTO LOAD, provide minimal control of tape operations. Magnetic tape operations are defined in detail in the *4051 Graphic System Reference Manual*.

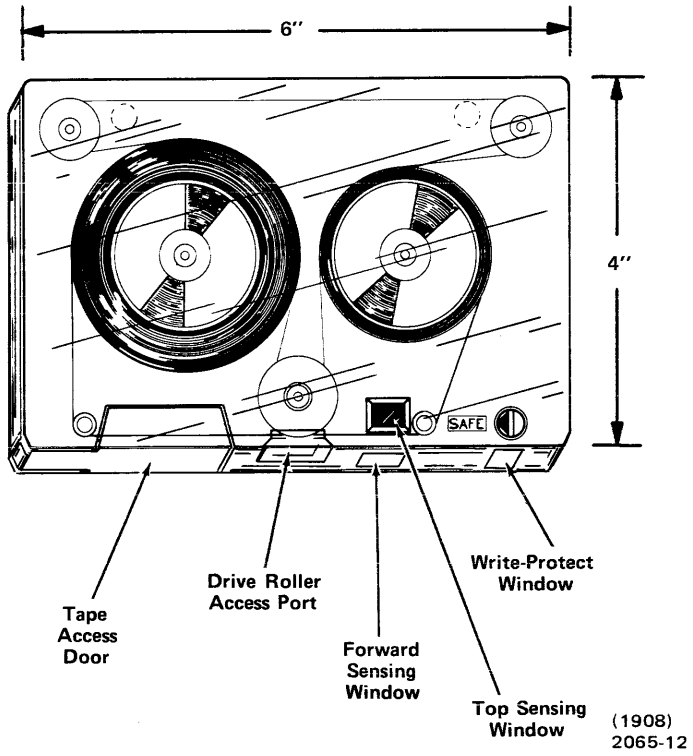


Fig. 2-8. Standard data cartridge for the 4051.

Recording Method	NRZ self clocking (NRZ = Non Return to Zero)
Bit Density	1600 bits per inch
Tracks	2
Head Type	Single 2-track read/write head

	Tape Speed	Accel/Decel Time	Accel/Decel Tape Dist.
Normal Read/Write	30 ips 76.2 cm/s	25 ms	0.375 in ±10%
Fast Forward/Reverse	90 ips 228.6 cm/s	90 ms	1.125 in ±10%
Rewind	90 ips 228.6 cm/s	90 ms	1.125 in ±15%

Life Expectancy Drive Motor and Tape Head	≥1000 hours of read/write operation.
Operating Time Between Head Cleanings	6 hours of tape drive read/write activity, or every 1000 hours of standard 4051 usage.

MAGNETIC TAPE MEDIA

The tape units use an industry standard data cartridge.

	3M Company type: DC 300 A Tektronix Part Number 119-0680-00
Data Capacity	300K bytes
Minimum Life	5000 passes
Tape Markers (See Diagram)	B.O.T. (Beginning Of Tape) Load Point Early Warning Point E.O.T. (End Of Tape)

DATA FORMAT AND RECORDING METHOD

The data format is determined by 4051 system firmware (Fig. 2-9). Data timing is tabulated in Table 2-1. Information on the tape is divided into files that contain a minimum of 3 records. The standard record length is 256 bytes of data characters, but a 128 character format may be selected using the PRINT @33,0: statement. The 128 character format is compatible with standard 4923 tape unit operations.

The tape formatting process occurs with the MARK *n,m* statement where *n* is the number of files to be marked and *m* is the number of bytes per file. Areas of the tape are demarcated by means of record marks and file marks.

Binary data bits are represented as reversals in flux direction (magnetic domain boundaries) on either the 1 track or 0 track. In reading the tape, the tape head is sensitive to flux reversals. The determination of a 1 or 0 depends upon which track had the flux reversal. This is the NRZ data recording system.

Special Data Sequences	Data is held at zero during record and file marks. Flux reversals occur only on track zero for these sequences.
Record Mark	4 flux reversals separated by intervals about three times longer than data bit separations. The longer intervals are called intercharacter gaps. The shorter intervals are interbit gaps.
File Mark	8 flux reversals separated by intervals about three times longer than data bit separations.

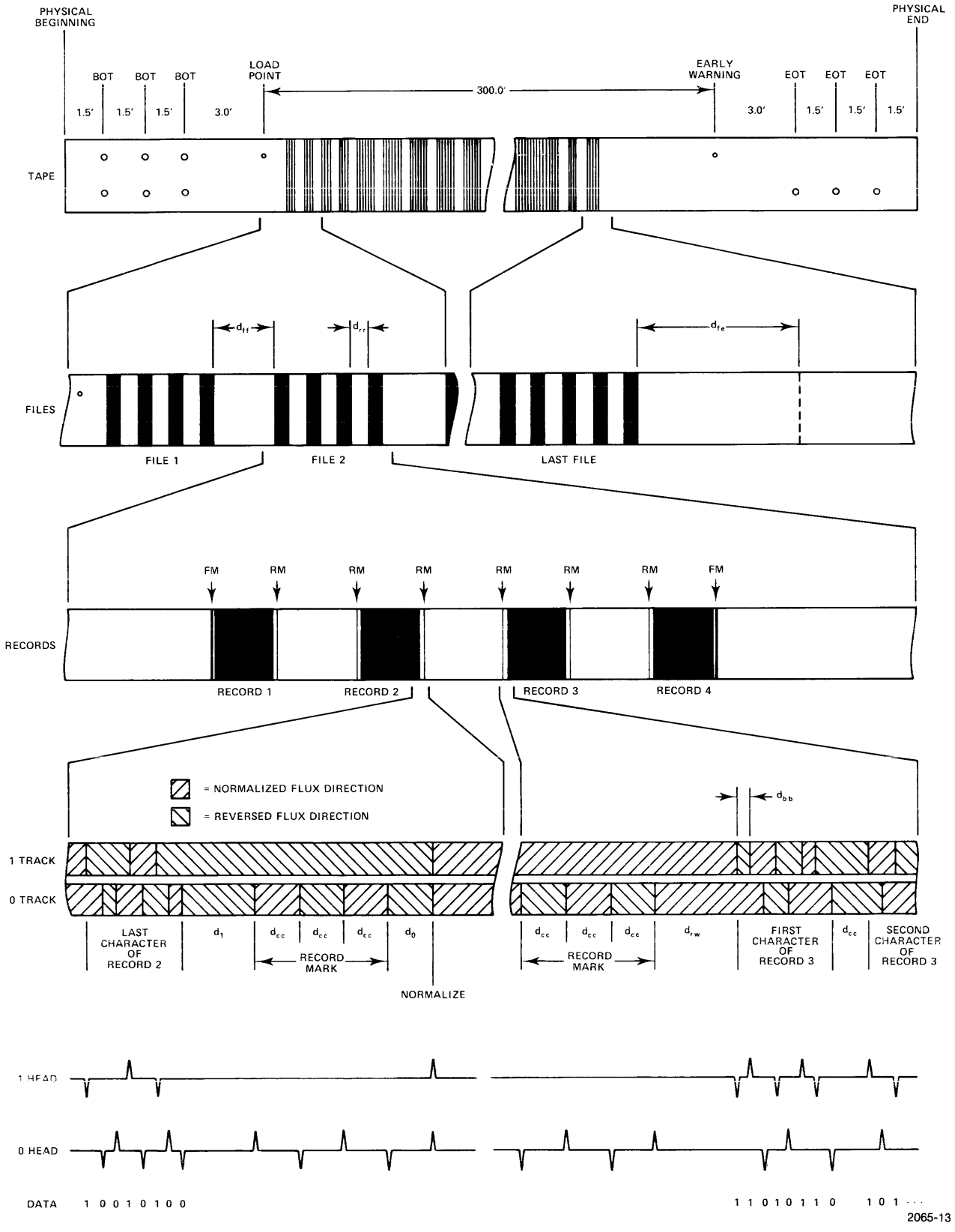


Fig. 2-9. 4051 magnetic tape cartridge recording format. See table 2-1 for timing and distance specifications.

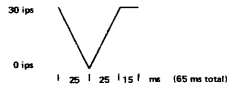
Table 2-1

MAGNETIC TAPE FORMAT SPECIFICATIONS

Characteristic	Symbol	Distance				Time (at 30 ips max.)			
		min.	nom.	max.	units	min.	nom.	max.	units
erase after last file	d_{fe}	9	-	-	in	300	-	-	ms
interfile gap	d_{ff}	3.17	3.60	4.03	in	172	195	218	ms[2]
interrecord gap	d_{rr}	1.06	1.20	1.34	in	57	65	73	ms[3]
read-to-write gap	d_{rw}	4.35	8.18	12.00	mil	145	272	400	μs
first intercharacter gap after record data	d_i	1.50	-	3.90	mil	50	-	130	μs
intercharacter gap	d_{cc}	1.50	2.25	3.00	mil	50	70	100	μs
normalizing gap after EOR mark	d_o	-	-	3.00	mil	-	-	100	μs
interbit gap	d_{bb}	.57	.65	.73	mil	19	21	24	μs

[2]**Speed is not constant at 30 ips during the interfile gap (Fig. 2-9).**

[3]**Speed is not constant at 30 ips during the interrecord gap (Fig. 2-9).**



MICROPROCESSOR SYSTEM SPECIFICATIONS

MOTOROLA DEVICES

The 4051 Graphic System is based on a Motorola 6800 microcomputer system. Specific system building blocks are listed in Table 2-2.

Table 2-2

SYSTEM BUILDING BLOCKS		
Microprocessing Unit (MPU)	MC6800	Used as mainframe central processing unit.
Peripheral Interface Adapter (PIA)	MC6820	Used as peripheral device controllers (i.e., tape control, keyboard control, display control, joystick control, GPIB controls, Bank Switch control, etc.)
Asynchronous Communications Interface Adapter (ACIA)	MC6850	Used for RS-232 communications interface.
Read Only Memory (ROM)	MCM6832L	Mask programmable ROM used in all 4051 firmware and firmware products.
Random Access Memory RAM)	MCM6605L	Dynamic Random Access Memory used for temporary program and data storage within the 4051 mainframe.

For detailed specifications on each of these devices, see the appendix that incorporates reprinted Motorola specification sheets.

MEMORY (ROM and Peripheral Devices)

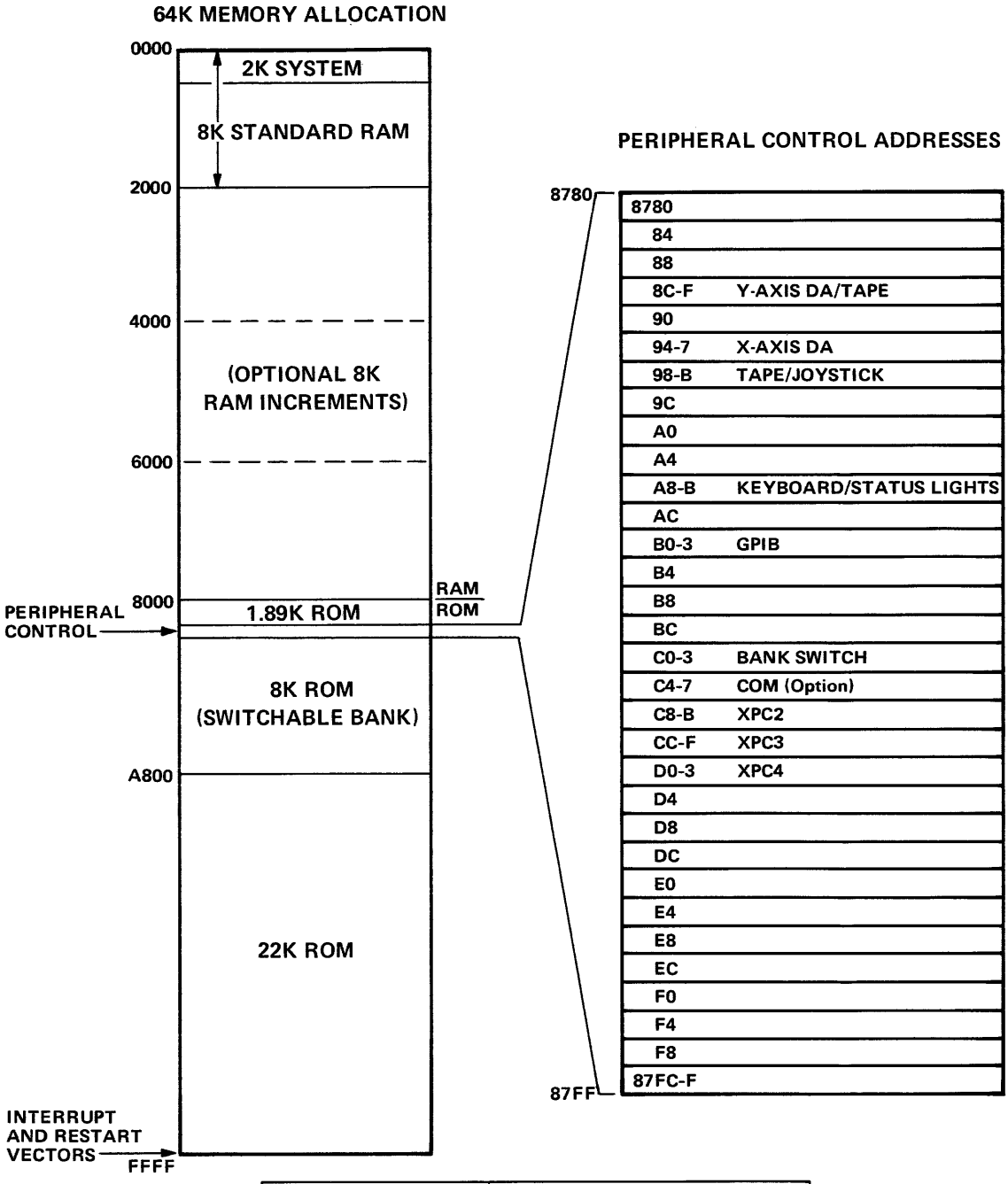
36K bytes for firmware and peripheral control addresses. Included are 8K bytes for a switchable firmware bank.

MEMORY (RAM for Program and Data Storage)

8K bytes minimum (2K of which are used by system tables). Additional 8K byte increments may be added up to a maximum address space of 32K.

MEMORY ADDRESS ALLOCATION

Figure 2-10 is a map of the 4051 memory address space. The total address space comprises 64K memory locations. The lower 32K is reserved for random access memory (RAM). The upper 32K is predominently read only memory (ROM) with a few addresses reserved for interfaces, most of which are peripheral interface adapters (PIAs).



DIVISION	ADDRESS BOUNDARIES
Standard RAM	0000-1FFF
Optional RAM	2000-7FFF
1.89K ROM	8000-877F
Peripheral Control	8780-87FF
8K Switchable Bank	8800-A7FF
22K ROM	A800-FFF7
Interrupt Vector	FFF8-FFF9
Restart Vector	FFFE-FFFF

2286-11

Fig. 2-10. 4051 Memory address space allocation map.

BANK SWITCH

Of the ROM addresses available to the 4051, there is a bank of 8K that is switch selectable. The particular 8K bank that is selected to reside in the switchable address space is determined by data stored in a bank switch register. Table 2-3 shows the meaning of the 8-bit data to be stored into the bank switch register or memory location. The letter X defines a don't care condition. The letter D defines ROM Expander Unit data.

Table 2-3

BANK SWITCH DATA WORD

76	543	210	
XX	000	XXX	RBC (ROM Bank Control)
XX	001	XXX	BSOFL (Bank Switch Overflow—Select Overflow ROMs)
XX	010	XXX	BSCOM (Bank Switch Communication—Select Communication ROM)
XX	011	XXX	—
XX	100	XXX	BS(L) (Bank Switch Left—Select Left ROM Pack)
XX	101	XXX	BS(R) (Bank Switch Right—Select Right ROM Pack)
XX	110	DDD	BSX(L) (Bank Switch Expander—Select Left ROM Expander Unit)
XX	111	DDD	BSX(R) (Bank Switch Expander—Select Right ROM Expander Unit)

DDD = ROM EXPANDER SLOT ADDRESS

BASIC LANGUAGE FORMAT

(Line Number) KEYWORD $\left(\begin{matrix}\% \\ @\end{matrix}\right)$ (I/O Addresses:)

LINE NUMBER

The line number determines the order of statement execution. If a line number is present, the statement is executed when the system is placed under program control. If the line number is not present, the statement is executed as soon as the statement is entered into the line buffer and the RETURN key is pressed.

KEYWORD

The KEYWORD is an alphabetical code that tells the BASIC interpreter what function to perform. This code represents a set of instructions for the BASIC interpreter only and is never seen by the peripheral device involved in the transfer. A list of operations for each BASIC keyword can be found in the *4051 Graphic System Reference Manual*.

I/O ADDRESS

The I/O address is a two-part numeric code that presents instructions to the peripheral device. The I/O address is sent to the peripheral device before the data transfer begins.

The I/O address follows the keyword in the statement and is specified as an "at" sign (@) or a percent sign (%), followed by a primary address, followed by a comma, followed by a secondary address, and terminated with a colon (:).

The "at" sign (@) or the percent sign (%) specifies which delimiters are to be used during the I/O operation. Some applications involving GPIB input/output operations use the percent sign (%) to logically disconnect the 4051 from the GPIB. Refer to the *4051 Graphic System Reference Manual* for details.

The primary address is specified as a peripheral device number between 1 and 255. When the statement is executed, the peripheral device number is converted to a primary talk address or a primary listen address, whichever is appropriate for the keyword, and issued to the specified peripheral device. The primary address tells the peripheral device that it has been selected to either send data to or receive data from the random access memory. Peripheral device numbers for the system are divided into categories as shown in Table 2-4.

Table 2-4

DEVICE NUMBER ASSIGNMENTS

Device Number	Peripheral Device
0	System Disc (mass storage device)
1-30	External peripheral devices on the General Purpose Interface Bus
31-39	Internal peripheral devices connected directly to the microprocessor bus lines
40-255	Reserved for future use

Internal peripheral devices are preassigned the following peripheral device numbers:

Table 2-5

INTERNAL DEVICE NUMBERS

Device Number	Peripheral Device
31	GS keyboard
32	GS display
33	Magnetic Tape Unit
34	DATA Statement
35	Unassigned
36	Unassigned
37	Processor Status
38	Unassigned
39	Unassigned

Peripheral device numbers can be specified as a numeric expression in a statement as long as the BASIC interpreter can reduce the expression to a numeric constant and round the constant to an integer within the range 1 to 255. This means that the primary address can be specified as a numeric variable; by changing the value assigned to the variable, different peripheral devices can be selected as the input source or output destination without changing the BASIC statement itself.

The secondary address in an I/O address is issued immediately after the primary address and tells the peripheral device what the data transfer is all about. Since the peripheral device never sees the keyword in the statement, the secondary address provides the only way to tell the peripheral device what function is being performed by the BASIC interpreter. A secondary address is specified as a number from 0 through 32. Each number has a predefined meaning. For example, secondary address 12 means that the BASIC interpreter is executing a PRINT statement; secondary address 13 means that the BASIC interpreter is executing an INPUT statement, and secondary address 0 means that the BASIC interpreter is sending status information. The following table lists the secondary address assignments for each I/O function performed by the BASIC interpreter.

Table 2-6

GPIB PRIMARY DEVICE ADDRESS ASSIGNMENTS

PERIPHERAL DEVICE	PRIMARY LISTEN ADDRESS									PRIMARY TALK ADDRESS								
	DECIMAL VALUE	DIO BUS								DECIMAL VALUE	DIO BUS							
		8	7	6	5	4	3	2	1		8	7	6	5	4	3	2	1
Device 0	32	0	0	1	0	0	0	0	0	64	0	1	0	0	0	0	0	0
Device 1	33	0	0	1	0	0	0	0	1	65	0	1	0	0	0	0	0	1
Device 2	34	0	0	1	0	0	0	1	0	66	0	1	0	0	0	0	1	0
Device 3	35	0	0	1	0	0	0	1	1	67	0	1	0	0	0	0	1	1
Device 4	36	0	0	1	0	0	1	0	0	68	0	1	0	0	0	1	0	0
Device 5	37	0	0	1	0	0	1	0	1	69	0	1	0	0	0	1	0	1
Device 6	39	0	0	1	0	0	1	1	0	70	0	1	0	0	0	1	1	0
Device 7	39	0	0	1	0	0	1	1	1	71	0	1	0	0	0	1	1	1
Device 8	40	0	0	1	0	1	0	0	0	72	0	1	0	0	1	0	0	0
Device 9	41	0	0	1	0	1	0	0	1	73	0	1	0	0	1	0	0	1
Device 10	42	0	0	1	0	1	0	1	0	74	0	1	0	0	1	0	1	0
Device 11	43	0	0	1	0	1	0	1	1	75	0	1	0	0	1	0	1	1
Device 12	44	0	0	1	0	1	1	0	0	76	0	1	0	0	1	1	0	0
Device 13	45	0	0	1	0	1	1	0	1	77	0	1	0	0	1	1	0	1
Device 14	46	0	0	1	0	1	1	1	0	78	0	1	0	0	1	1	1	0
Device 15	47	0	0	1	0	1	1	1	1	79	0	1	0	0	1	1	1	1
Device 16	48	0	0	1	1	0	0	0	0	80	0	1	0	1	0	0	0	0
Device 17	49	0	0	1	1	0	0	0	1	81	0	1	0	1	0	0	0	1
Device 18	50	0	0	1	1	0	0	1	0	82	0	1	0	1	0	0	1	0
Device 19	51	0	0	1	1	0	0	1	1	83	0	1	0	1	0	0	1	1
Device 20	52	0	0	1	1	0	1	0	0	84	0	1	0	1	0	1	0	0
Device 21	53	0	0	1	1	0	1	0	1	85	0	1	0	1	0	1	0	1
Device 22	54	0	0	1	1	0	1	1	0	86	0	1	0	1	0	1	1	0
Device 23	55	0	0	1	1	0	1	1	1	87	0	1	0	1	0	1	1	1
Device 24	56	0	0	1	1	1	0	0	0	88	0	1	0	1	1	0	0	0
Device 25	57	0	0	1	1	1	0	0	1	89	0	1	0	1	1	0	0	1
Device 26	58	0	0	1	1	1	0	1	0	90	0	1	0	1	1	0	1	0
Device 27	59	0	0	1	1	1	0	1	1	91	0	1	0	1	1	0	1	1
Device 28	60	0	0	1	1	1	1	0	0	92	0	1	0	1	1	1	0	0
Device 29	61	0	0	1	1	1	1	0	1	93	0	1	0	1	1	1	0	1
Device 30	62	0	0	1	1	1	1	1	0	94	0	1	0	1	1	1	1	0
UNLISTEN/UNTALK	63	0	0	1	1	1	1	1	1	95	0	1	0	1	1	1	1	1

Table 2-7

GPIB SECONDARY ADDRESS ASSIGNMENTS

Secondary Address	Predefined Meaning	Decimal Value	Data Bus 8	7	6	5	4	3	2	1
0	"STATUS"	96	0	1	1	0	0	0	0	0
1	SAVE	97	0	1	1	0	0	0	0	1
2	CLOSE	98	0	1	1	0	0	0	1	0
3	OPEN	99	0	1	1	0	0	0	1	1
4	OLD/APPEND	100	0	1	1	0	0	1	0	0
5	CREATE	101	0	1	1	0	0	1	0	1
6	TYPE	102	0	1	1	0	0	1	1	0
7	KILL	103	0	1	1	0	0	1	1	1
8	UNIT	104	0	1	1	0	1	0	0	0
9	DIRECTORY	105	0	1	1	0	1	0	0	1
10	COPY	106	0	1	1	0	1	0	1	0
11	RELABEL	107	0	1	1	0	1	0	1	1
12	PRINT	108	0	1	1	0	1	1	0	0
13	INPUT	109	0	1	1	0	1	1	0	1
14	READ	110	0	1	1	0	1	1	1	0
15	WRITE	111	0	1	1	0	1	1	1	1
16	ASSIGN	112	0	1	1	1	0	0	0	0
17	"ALPHASCALE"	113	0	1	1	1	0	0	0	1
18	"ALPHAFONT"	114	0	1	1	1	0	0	1	0
19	LIST/TLIST	115	0	1	1	1	0	0	1	1
20	DRAW/RDRAW	116	0	1	1	1	0	1	0	0
21	MOVE/RMOVE	117	0	1	1	1	0	1	0	1
22	PAGE	118	0	1	1	1	0	1	1	0
23	HOME	119	0	1	1	1	0	1	1	1
24	GIN	120	0	1	1	1	1	0	0	0
25	"ALPHAROTATE"	121	0	1	1	1	1	0	0	1
26	COMMAND	122	0	1	1	1	1	0	1	0
27	FIND	123	0	1	1	1	1	0	1	1
28	MARK	124	0	1	1	1	1	1	0	0
29	SECRET	125	0	1	1	1	1	1	0	1
30	"ERROR"	126	0	1	1	1	1	1	1	0
31	undefined	127	0	1	1	1	1	1	1	1

GENERAL PURPOSE INTERFACE BUS (GPIB)

THE GPIB CONNECTOR

The GPIB connector is a 24-pin connector located on the rear panel of the 4051 Graphic System main chassis. This connector allows external peripheral devices to be connected to the system. The devices must conform to the IEEE Standard #488-1975 which describes a byte-serial, bit-parallel interface system for programmable instrumentation. The GPIB connector is a standard 24-pin connector with sixteen active signal lines and eight interlaced grounds. The cable attached to the GPIB connector must be no longer than 20 meters maximum with a maximum number of fifteen peripheral devices. The connector pin arrangement and signal line nomenclature is shown in Fig. 2-11.

THE GPIB INTERFACING CONCEPT

The GPIB is functionally divided into three component buses; an eight-line Data Bus, a three-line Transfer Bus, and a five line Management Bus for a total of sixteen active signal lines. This bus structure is shown in Fig. 2-12.

The transfer rate over the Data Bus is a function of the slowest peripheral device taking part in a transfer at any one time. The bus operates asynchronously with a maximum transfer rate of one megabyte/second. Both peripheral addresses and data are sent sequentially over the Data Bus. Once peripheral addresses are established for a particular transfer, successive data bytes may be transmitted in a burst for higher effective data rates.

Peripheral Devices on the GPIB are designated as talkers and listeners. The Graphic System microprocessor acts as the controller to assign peripheral devices on the bus as listeners and talkers. The Graphic System microprocessor assumes that it is the only controller on the bus and it has complete control over the direction of all data transfers. There is no provision in the Graphic System for other devices on the GPIB with controller capability to take turns with the microprocessor as controller-in-charge.

A talker is a device capable of transmitting information on the Data Bus. There can be only one talker at a time. The Graphic System microprocessor has the ability to assume the role of the talker when it elects to do so.

A listener is a device capable of receiving information transmitted over the Data Bus. There may be up to fourteen listeners taking part in an I/O operation at any one time. The Graphic System microprocessor has the ability to assume the role of a listener any time it elects to do so.

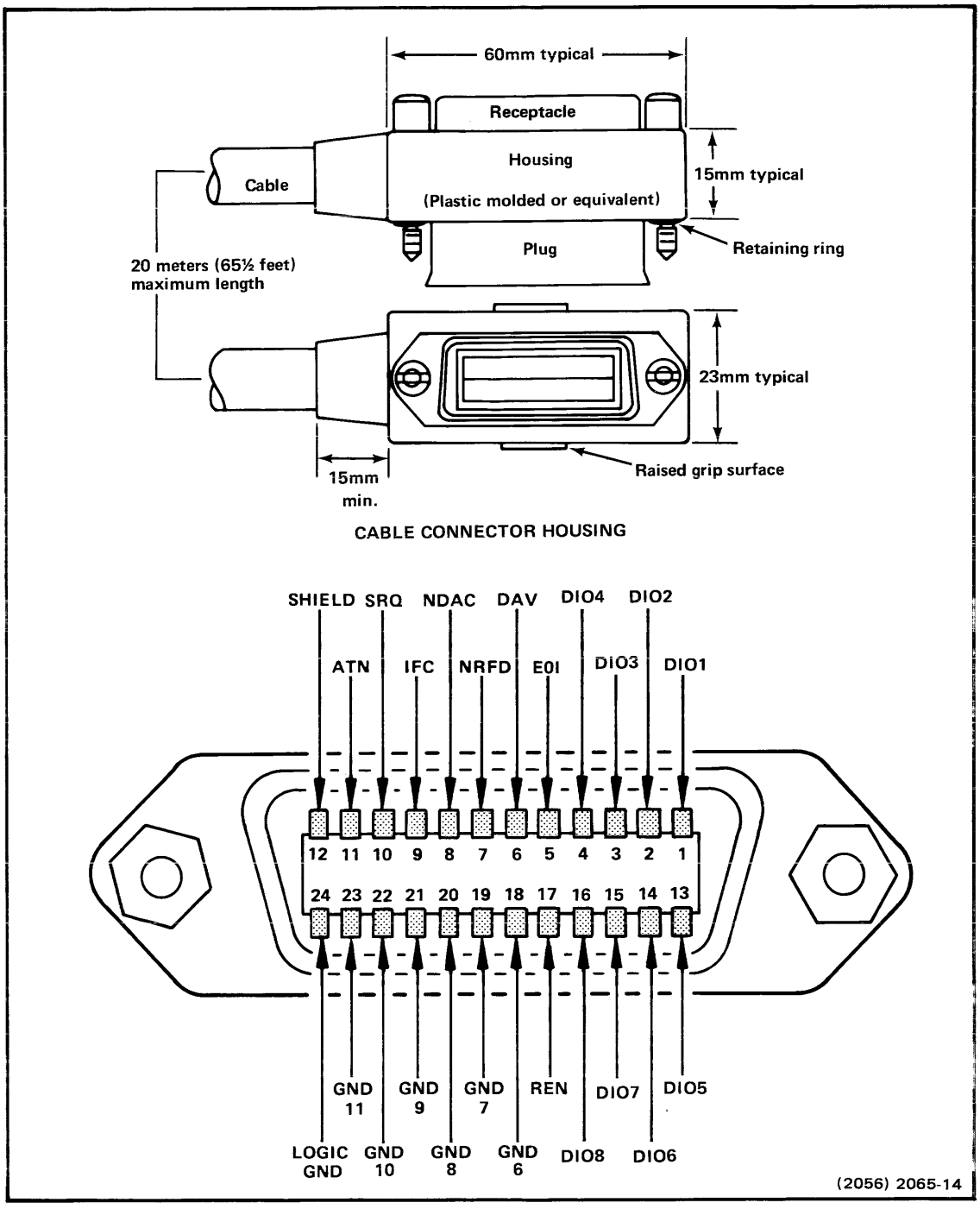


Fig. 2-11. GPIB connector(s) and pin assignments.

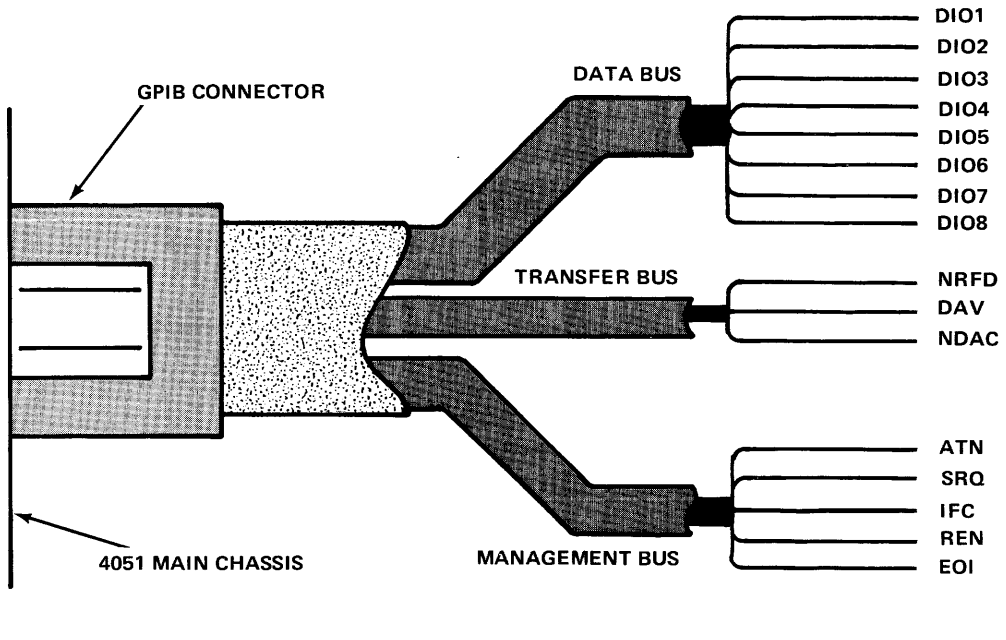


Fig. 2-12. GPIB bus structure diagram.

GPIB SIGNAL DEFINITIONS

Data Bus

The Data Bus contains eight bidirectional active-low signal lines, DIO1 through DIO8. One byte of information (eight bits) is transferred over the bus at a time. DIO1 represents the least significant bit in the byte; DIO8 represents the most significant bit in the byte. Each byte represents a peripheral address (either primary or secondary), a control word, a digit in a numeric data item, or a character in an alphanumeric character string. Data bytes can be formatted in ASCII code, with or without parity, or they can be formatted in machine dependent binary code.

Management Bus

The Management Bus is a group of five signal lines that are used to control data transfers over the Data Bus. The signal definitions for the Management Bus are as follows:

Signal	Definition
ATTENTION (ATN)	This signal line is activated by the controller when peripheral devices are being assigned as listeners and talkers. Only peripheral addresses and control messages can be transferred over the Data

	Bus when ATN is active low. After ATN goes high, only those peripheral devices which are assigned as listeners and talkers can take part in the data transfer. The Graphic System microprocessor assumes it is the only source of this signal.
SERVICE REQUEST (SRQ)	Any peripheral device on the GPIB can request the attention of the controller by setting SRQ active low. The controller responds by setting ATN active high and executing a serial poll to see which device is requesting service. This response is generated by the SRQ ON Unit instruction that is executed in the BASIC program. The serial poll is taken when a POLL statement is executed in the BASIC program. After the peripheral device requesting service is found, BASIC program control is transferred to a service routine for that device. When the service routine is finished executing, program control returns to the main program. The SRQ signal line is reset to an inactive state when the device requesting service is polled.
INTERFACE CLEAR (IFC)	The IFC signal line is activated by the controller when it wants to place all interface circuitry in a predetermined quiescent state. The 4051 Graphic System microprocessor assumes that it is the only source of this signal. IFC is activated each time the INIT statement is executed in a BASIC program and each time an error occurs in program execution.
REMOTE ENABLE (REN)	The REN signal line is activated whenever the system is operating under program control. REN causes all peripheral devices on GPIBs to ignore their front panel controls and operate under remote control via signals and control messages received over the GPIB.
End or Identify (EOI)	The EOI signal can be used by the talker to indicate the end of a data transfer sequence. The talker activates EOI as the last byte of data is transmitted. When the controller is listening, it assumes that a data byte received is the last byte of the transmission, if EOT is activated. When the controller is talking, it always activates EOI as the last byte is transferred.

The Transfer Bus

A handshake sequence is executed by the talker and the listeners over the Transfer Bus each time a data byte is transferred over the Data Bus. The Transfer Bus signal lines are defined as follows:

Signal	Definition
Not Ready for Data (NRFD)	An active low NRFD signal line indicates that one or more assigned listeners are not ready to receive the next data byte. When all of the assigned listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. This tells the talker to place the next data byte on the Data Bus.
Data Valid (DAV)	The DAV signal line is activated by the talker shortly after the talker places a valid data byte on the Data Bus. An active DAV signal tells each listener to capture the data byte presently on the Data Bus. The talker is inhibited from activating DAV when NRFD is active low.
Data Not Accepted (NDAC)	The NDAC signal line is held active low by each listener until the listener captures the data byte currently being transmitted over the Data Bus. When all listeners have captured the data byte, NDAC goes inactive high. This tells the talker to take the byte off the Data Bus.

GPIB DATA FORMATS

Any series of bit patterns can be transmitted over the GPIB. This allows both numeric data and alphanumeric data to be transmitted in either ASCII code or machine dependent binary code.

Transferring ASCII Data

ASCII data is transferred from the read/write random access memory to a peripheral device on the GPIB using the PRINT statement. ASCII transfers in the opposite direction are executed using the INPUT statement. ASCII numeric data can be transferred in either standard (free) format or scientific format, and must be transmitted most significant digit first. Valid ASCII characters are digits 0 through 9,E,e,+,−, and decimal point. ASCII character strings can be transmitted as any sequence of valid ASCII characters except Carriage Return. Carriage Return is used as the string delimiter. All ASCII data transfers, both numeric and alphanumeric, are terminated with a Carriage Return character or by activating the EOI signal line on the Management Bus, or both. (Refer to the INPUT and PRINT statements in the Input/Output Operations section of the *4051 Graphic System Reference Manual* for detailed information on ASCII data transfers over the GPIB.)

Transferring Machine Dependent Binary Code

The term "machine dependent binary code" refers to the internal binary format used to store data within the 4051 Graphic System. Communication between the BASIC interpreter and an external peripheral device in machine dependent binary code is usually faster because the time it takes to convert the internal binary format to ASCII format is eliminated. Transfers between the random access memory and a peripheral device in machine dependent binary code implies that the peripheral device is able to understand the internal binary format.

Normally, transfers of this nature are carried on between the random access memory and an external mass storage device that doesn't have to understand the code or between the random access memory and a peripheral device specifically built for the system by Tektronix.

Information transfers to and from a peripheral device on the GPIB are carried on via the WRITE statement and the READ statement. Each data item transmitted is preceded by a two byte header which identifies the data type (numeric or alphanumeric) and the length of the data item (in bytes). (Refer to the READ statement and the WRITE statement in the I/O Operations section of the *4051 Graphic System Reference Manual* for details.

Transferring One Data Byte at a Time

Direct access to the GPIB from the 4051 keyboard is made available through the WBYTE (Write Byte) statement and the RBYTE (Read Byte) statement. These two statements allow you to send any eight bit pattern over the GPIB. Also, the WBYTE statement allows you to activate the ATN signal line to tell peripheral devices that the byte you're sending is a peripheral address or a control word and it gives you complete control over the activation of the EOI signal line except when a binary 0 is explicitly transferred by WBYTE-0. (Refer to the WBYTE and RBYTE statement in the Input/Output Operations section of the *4051 Graphic System Reference Manual* for details.) To send binary zero with EOI activated the program should specify a value between zero and −0.5 that rounds to the integer zero in the WBYTE statement.

GPIB-to-IEEE COMPATIBILITY

INTRODUCTION

The following text describes the interfacing compatibility of the 4051 Graphic System's General Purpose Interface Bus with the IEEE Standard #488-1975 which describes a byte-serial, bit-parallel interface system for programmable instrumentation.

In general, the Graphic System microprocessor acts as a standard talker, listener, and controller. The controller function does not have the ability to conduct a parallel poll; it does however, have the ability to conduct a serial poll. Serial polls are taken each time the POLL statement is executed.

The Graphic System microprocessor does not have the ability to transfer control to another device on the GPIB with controller capability. Therefore, the Graphic System microprocessor assumes that it is the only controller on the GPIB.

GPIB INTERFACING COMPATIBILITY IN DETAIL

Reference: IEEE Standard #488-1975

The 4051 Graphic System GPIB falls into the following interface function subsets as defined in the IEEE Standard #488-1975 document:

Section 2.3 SH (Source Handshake Function)
SH1 — completely compatible

Section 2.4 AH (Acceptor Handshake Function)
AH1 — completely compatible

Section 2.5 T (Talker Function)
TE3 — basic extended talker, however, the microprocessor addresses itself internally and not over the GPIB.

Section 2.6 L (Listener Function)
LE1 — basic extended listener, however, the microprocessor addresses itself internally and not over the GPIB.

Section 2.7 SR (Service Request Function)
SR0 — no capability to issue SRQ

Section 2.8 RL (Remote Local)
RL0 — no capability

Section 2.9 PP (Parallel Poll Function)
PP0 — no capability

Section 2.10 DC (Device Clear Function)
DC0 — no capability

Section 2.11 DT (Device Trigger Function)
DT0 — no capability

Section 2.12 C (Controller Function)
C1 — System Controller
C2 — Send IFC and take charge
C3 — Send REN
C4 — Respond to SRQ
C28 — Send Interface Messages

GENERAL PURPOSE GPIB COMMANDS

GPIB device addresses can be issued as illustrated in Fig. 2-13 followed by a command to read data. When the WBYTE @70,109: statement is executed in a BASIC program, the @ sign causes the ATN line to be activated, 70 is the primary talk address for device number 6 and 109 is the secondary address normally interpreted by the 4051 BASIC Language Interpreter as an

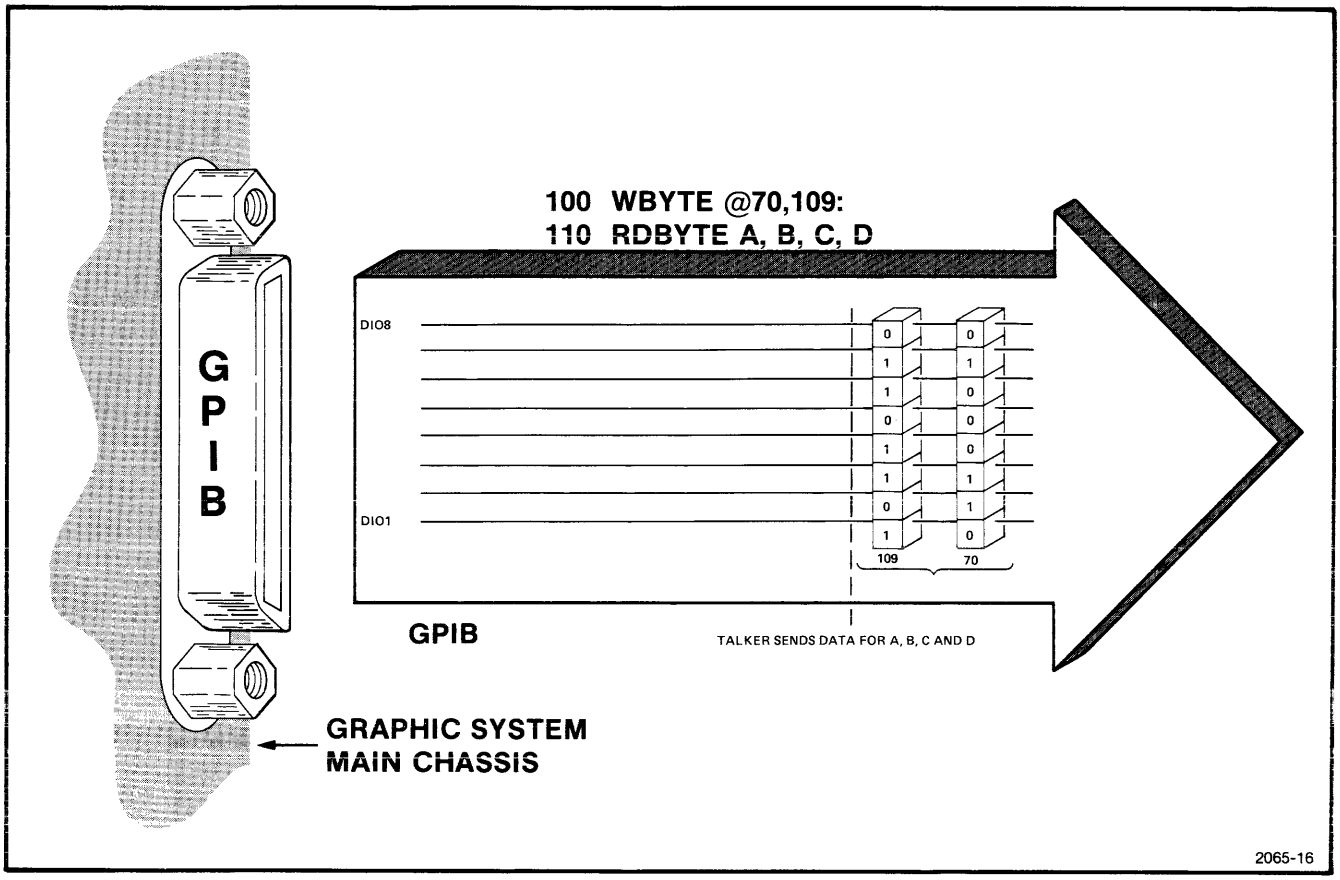


Fig. 2-13. Reading data from a device on the GPIB. 70 is the primary talk address for device 6 and 109 is the secondary address associated with the INPUT command statement.

INPUT command. The WBYTE statement enables secondary device addresses to be transmitted without activating contradictory data processing firmware within the 4051. The RDBYTE statement can then be used to read data from the assigned talker. The RDBYTE statement receives one or more data bytes from a peripheral device on the GPIB and assigns each data byte to a numeric variable.

In the example of Fig. 2-14 a primary address of 44 and secondary address os 108 are transmitted to the peripheral device. Data is sent to the peripheral device corresponding to the binary bytes associated with the numbers 65 and 66. The minus sign on −66 activates the EOI line during the last byte of data transferred. WBYTE @63,95: transmits the universal commands UNTALK and UNLISTEN over the GPIB.

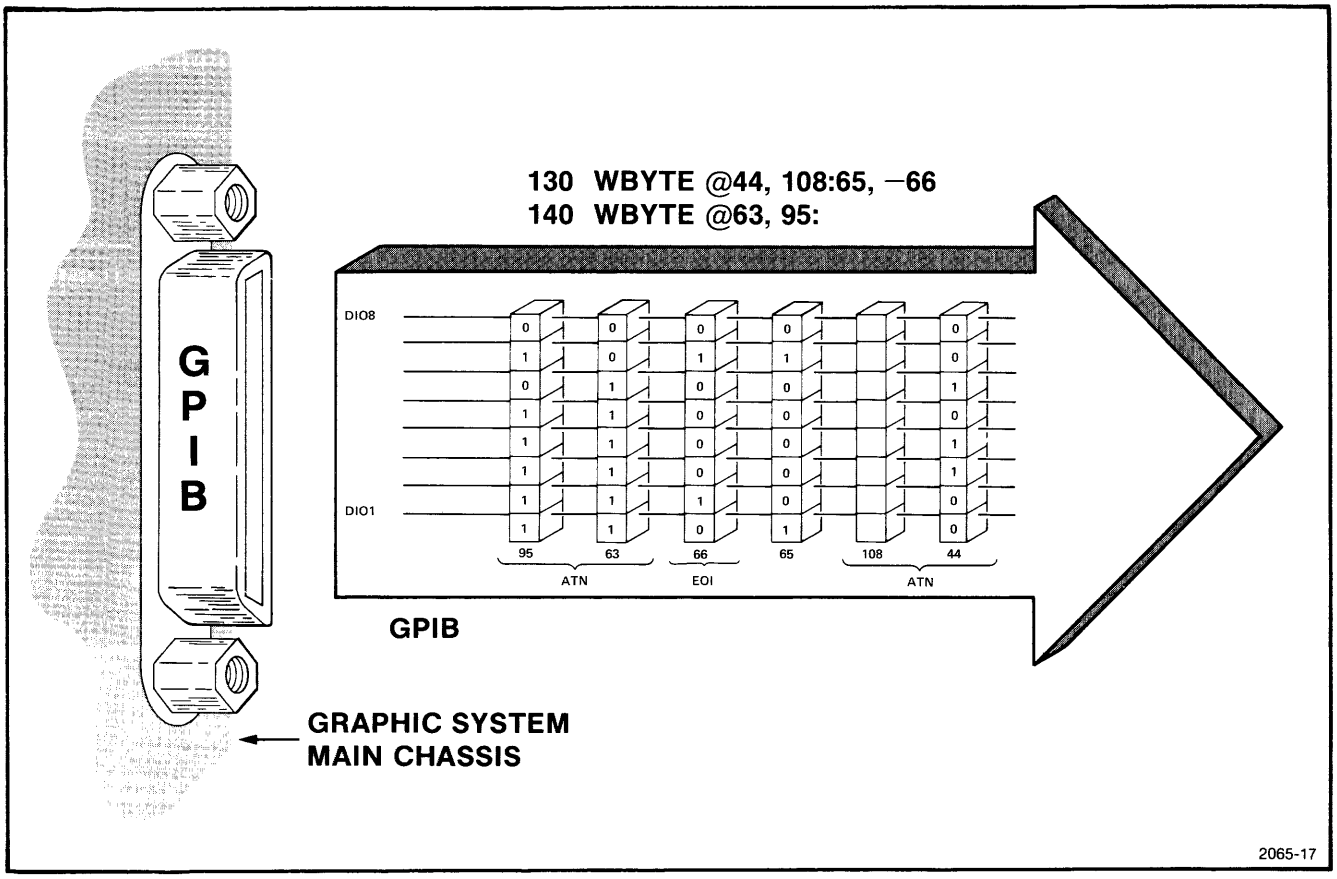


Fig. 2-14. Transmitting data to a device on the GPIB followed by the universal commands of UNTALK and UNLISTEN.

To cause one peripheral device to transfer information to another device on the bus, the listeners and talker must be addressed. The BASIC statement WBYTE % (arguments) must have the percent sign to remove the 4051 from the GPIB as in Fig. 2-15. The 4051 then executes a WAIT statement to halt the current instruction stream until EOI is received. The ON EOI THEN 18Ø statement causes control to pass to line 180 when device-to-device data transfer is complete.

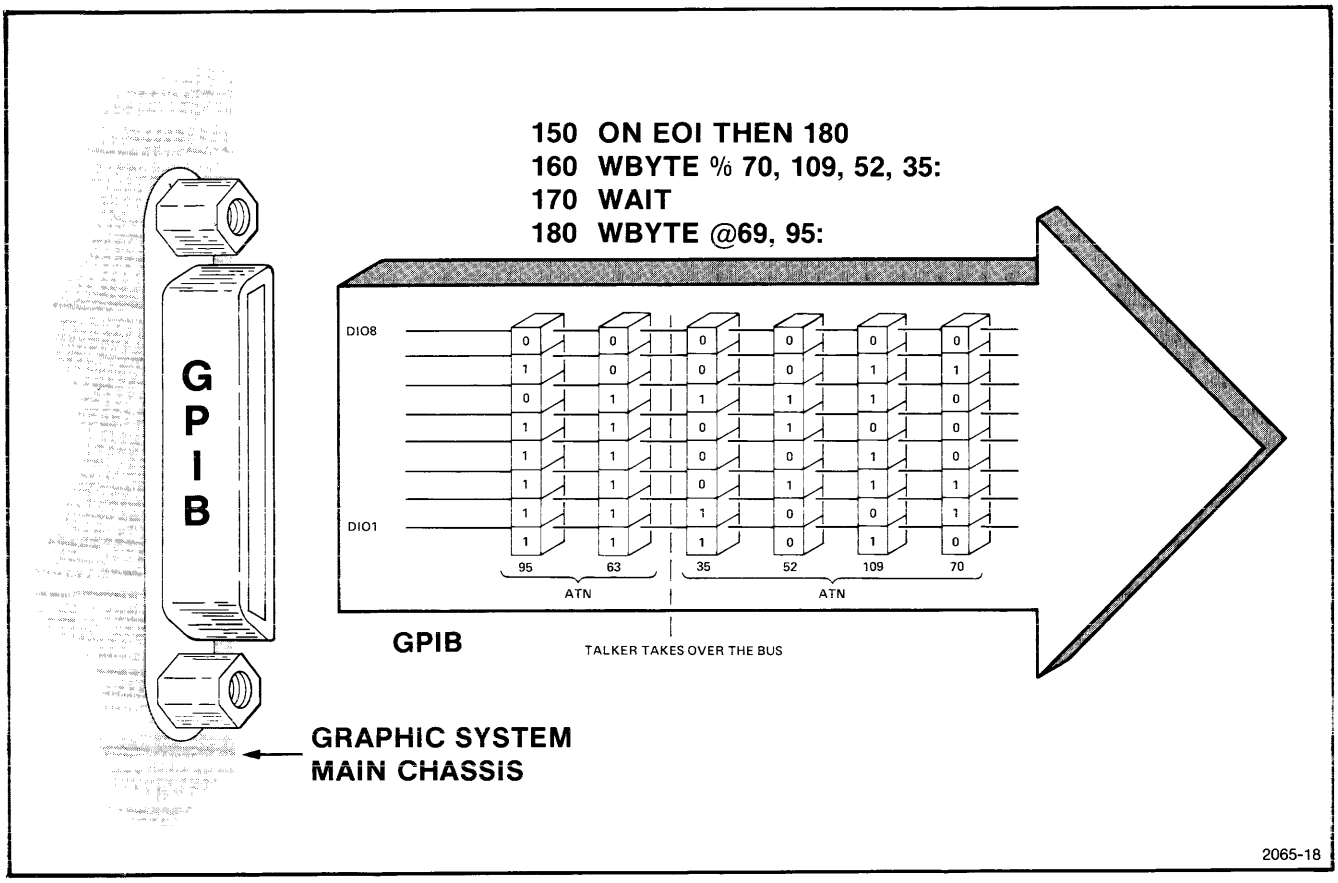


Fig. 2-15. A procedure to initiate data transfer between two GPIB devices and waiting until the data transfer is completed.

Section 3

MAINTENANCE

ROUTINE MAINTENANCE

GENERAL

Beyond the need for occasional cleaning there is virtually little need for routine maintenance of the system. It has no lubrication points and, with the exception of the crt, no vacuum tubes. The solid state components provide stable operation with little need for routine adjustment. However, a routine maintenance schedule and procedure is recommended. The frequency depends upon your operating environment and the amount of time the 4051 is used. Along with routine maintenance you should include running the System Software and Firmware Verification programs found on the PLOT 50: SYSTEM SOFTWARE TAPE. First, read the following text; then establish a routine maintenance schedule.

Routine service procedures that should be performed at regular intervals on your 4051 Graphic System include the following:

1) Clean the outer surfaces of the unit.
2) Clean the air filter when dirty.
3) Clean the tape heads every 6 hours of tape drive operation, 1000 hours of 4051 operation, or whenever tape errors begin to occur. Tape errors can be identified as the tape does a backup operation to read a record of data for another time.

Note that all motors and bearings in the 4051 are permanently lubricated and should not need oil or other lubrication. The solid-state components provide stable operation with little need for routine adjustment. If a routine schedule for circuit adjustment and calibration is desired, a one-year interval is recommended. Material in this section should be referred to as necessary.

This section contains preventive maintenance information and system disassembly/reassembly procedures.

CLEANING

CAUTION

Avoid the use of chemical cleaning agents which may damage the plastics in this instrument. Avoid chemicals which contain benzene, toluene, xylene, acetone, or similar solvents.

Surface Cleaning

To clean the face of the display crt and the exterior of the system, use a soft cloth dampened with a mild detergent and water solution.

Cleaning the Fan Filter

The cooling fan filter on the backpanel should be checked periodically and cleaned as required to ensure optimum cooling air flow through the system. Before cleaning the fan filter, disconnect the power cord from the power source.

The air filter can be removed by removing the filter bracket from the back of the 4051. After removal, shake loose as much dust as possible (or vacuum), then thoroughly clean in a mild detergent and water solution. Be sure the filter is thoroughly dry before installing it back in the system.

Cleaning the Tape Head

The surface of the tape head (see Fig. 3-1) must be kept clean in order to accurately read and write data to and from the tape. Oxide from the tape, along with other foreign matter, may be deposited on the head during tape operation. This results in data errors and must be corrected as required by cleaning the head, using the following procedure.

1. Inspect the head by shining a light, such as a penlight, across the surface of the head at an angle. This reveals accumulations of foreign material. If the head is dirty, clean the head according to the remaining instructions.

2. Use a cotton swab moistened with isopropyl alcohol or a quality magnetic tape head cleaner to rub off accumulated matter. Light accumulations of oxide will probably be readily removable, while heavy accumulations may require more alcohol and clean swabs.

3. After removing the oxides and other foreign matter, use a clean, dry cotton swab to polish the head and remove alcohol residue.

4. At this time you may elect to run the System Verification Software to check magnetic tape unit operation.

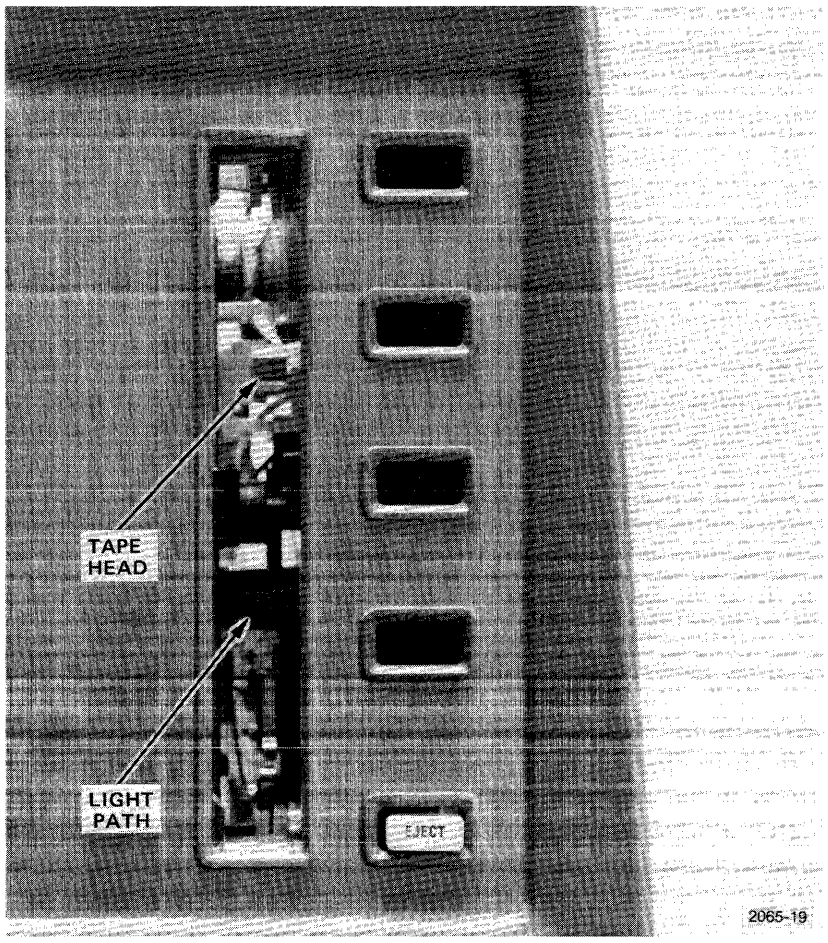


Fig. 3-1. Tape head and tape status light path.

Cleaning Electrical Contacts

Freon TF (trichlorotrifluroethane) and combinations with isoproply alcohol are suitable electrical contact cleaners (i.e., Miller-Stephenson MS-160 or FREON TP-35). Avoid using these chemical solvents near the tape motor and fan; they readily remove lubrication from motor bearings. Avoid the use of chemicals that damage plastic parts within the instrument.

SYSTEM VERIFICATION SOFTWARE

There are two verification programs on the PLOT 50: SYSTEM SOFTWARE TAPE: a software program and a firmware program.

The Software Verification Program checks out system internal peripherals; that is, the keyboard, the graphic system display, and the data transfer to and from the internal magnetic

tape unit. You and the 4051 Graphic System act as a team in this checkout. You press keys in response to system requests, and the system responds with various statements and test patterns.

The Firmware Verification Program checks the 4051's random access memory (RAM). The system does all the work in this program in about one minute.

To test the system read-only memories (ROM) that hold the BASIC interpreter, a System Test Fixture is required. Test fixture operations and the special tests performed are documented later in this manual.

The Software Verification Program and the Firmware Verification Program are stored on two separate tape files for your convenience. It is suggested, however, that both verification programs found on the PLOT 50: SYSTEM SOFTWARE TAPE be run during equipment checkout.

The verifications programs are on the PLOT 50: SYSTEM SOFTWARE TAPE. Insert the tape cartridge into the system. Press the AUTO LOAD key. When tape movement stops, the Plot 50 Master Menu will appear on the display screen. Notice that menu selection 6 is the Software Verification Program. Press the 6 key, then press the RETURN key. This will take you to the Software Verification Program.

When the Software Verification Program is completed, the system returns to the master menu automatically. Notice that the 7th selection on the menu is for the Firmware Verification Program. Press the 7 key, then press the RETURN key to go to that program. When it is completed, turn off the 4051 Graphic System or press the AUTO LOAD key and return to the master menu.

CARTRIDGE RESPOOLING

The data cartridge used in the 4051 Graphic System is open-ended; that is, the tape ends are not secured to either of the spools. The magnetic tape unit relies on light-sensing of small holes at either end of the tape to stop motion before the physical end of the tape is reached. Under certain conditions, such as a possible circuit failure, a burned-out lamp, or an obstruction in the light path (such as a soiled cartridge or lamp-detector assembly) the tape may fail to stop in time, resulting in a tape end coming off the spool. If you suspect the cause is a circuit failure or a burned-out lamp, the cause must be determined and corrected. Refer to the Circuit Description section for circuit information. In any event, you will want to wind the tape back onto the empty spool. Use the following procedure.

1. Remove the four screws that attach the metal base to the plastic cover (see Figs. 3-2 and 3-3).

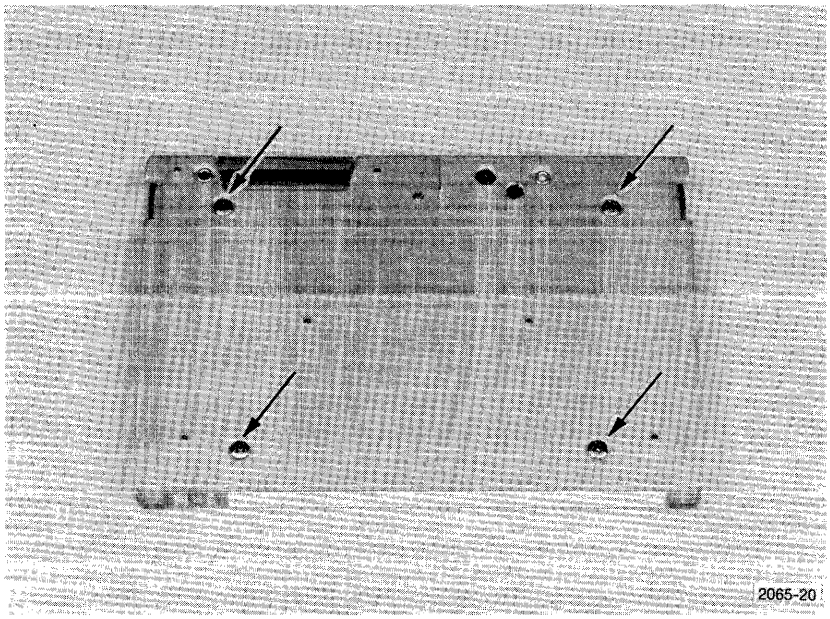


Fig. 3-2. Cartridge assembly screws.

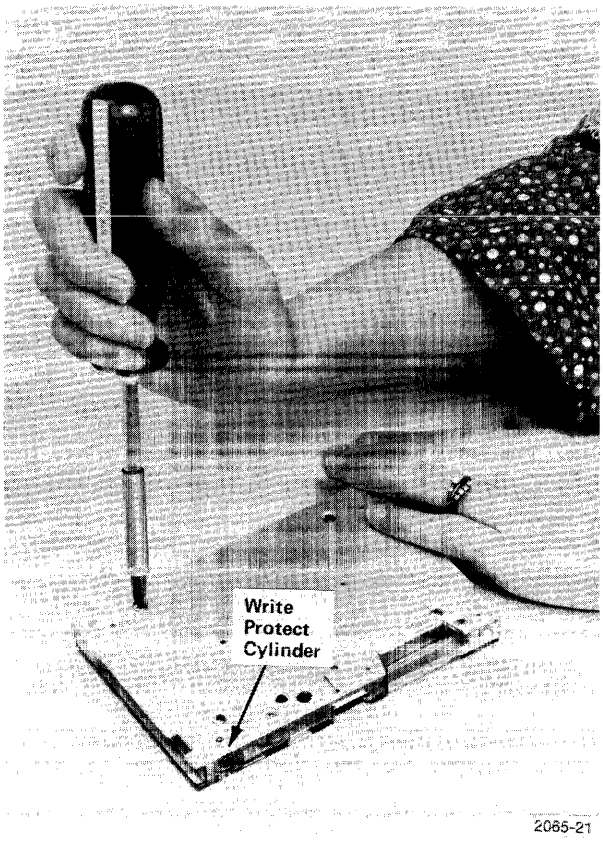


Fig. 3-3. Disassembling the tape cartridge.

2. Carefully remove the metal base plate, using caution not to lose the write-protect cylinder or the small metal spring between the cylinder and the metal base (Fig. 3-3).

3. Place the loose end of the tape across the front of the cartridge, threading it through in front of the two guide posts. Now, keeping light tension on the tape, place the loose end of the tape around the outside edge of the take-up spool, to the point where the spool meets the tension band (Fig. 3-4).

4. Rotate the spool, causing the tape to pass around the spool, with the loose end passing through the inside edge of the spool (Fig. 3-5). Do not press down on the full spool.

5. Hold the loose end of the tape against the spool, and continue to rotate until the loose end passes under the continuing length of tape, then continue to rotate for a few more turns, until the first set of sensing holes are reached (Fig. 3-6). Make certain that these first windings stay evenly within the spool edges.

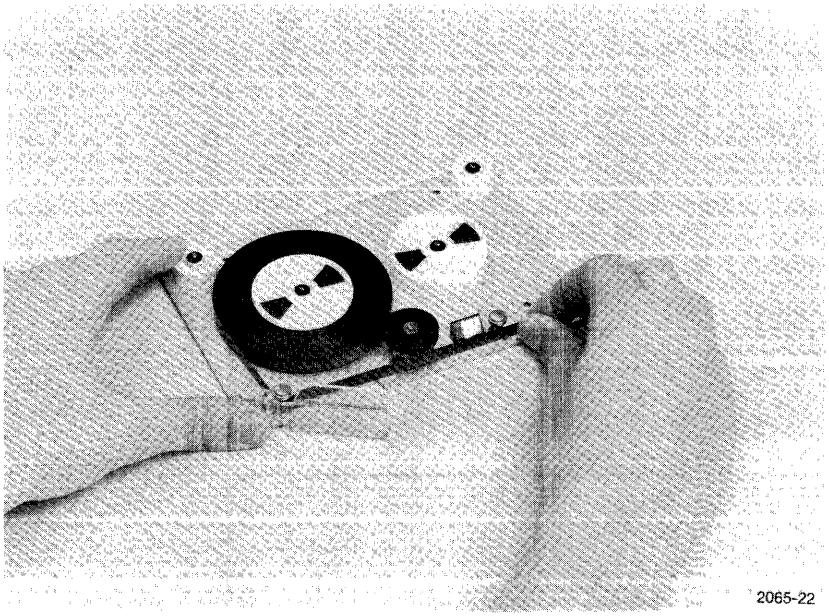


Fig. 3-4. Tape positioning within the cartridge.

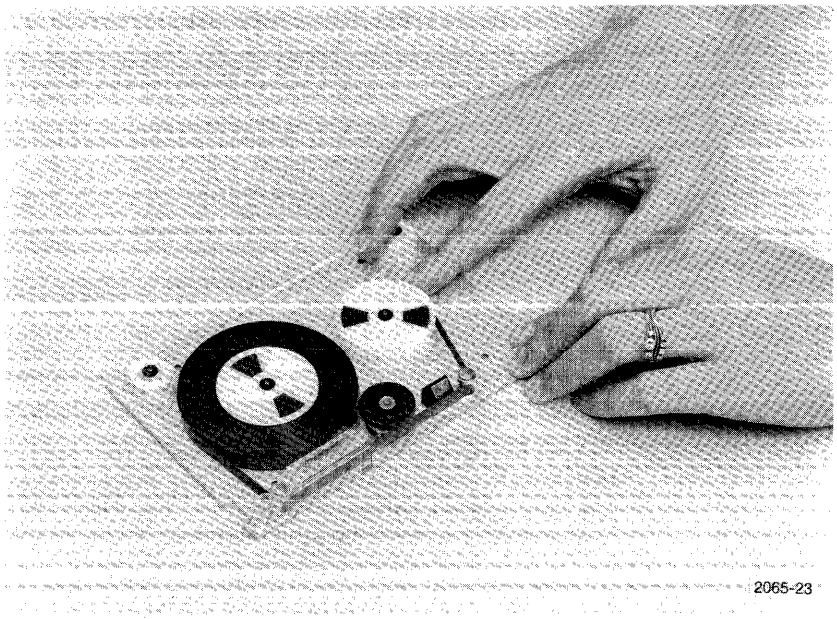


Fig. 3-5. Beginning the tape winding.

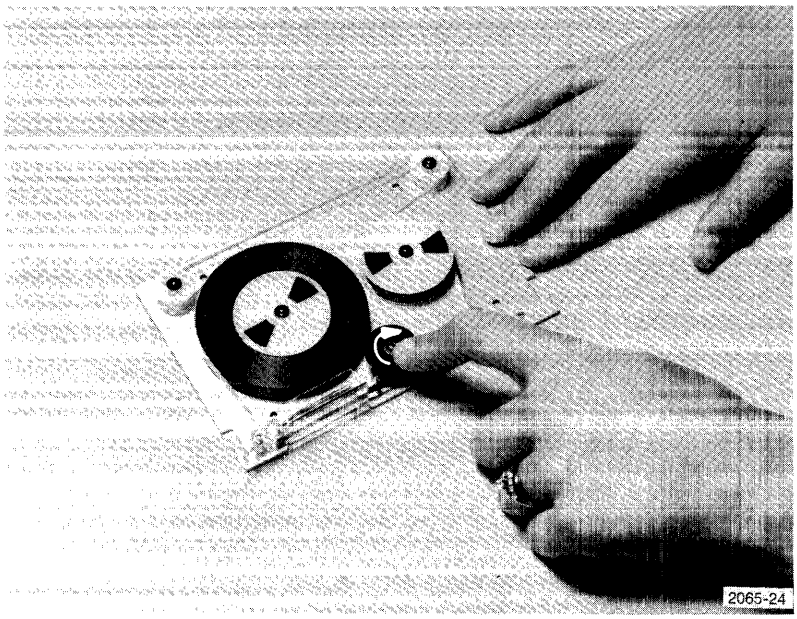


Fig. 3-6. Winding the tape.

6. Make certain that the write-protect cylinder is in position, with the spring washer between the cylinder and the metal cartridge base. Position the metal cartridge base over the plastic cover. Be careful not to catch and wrinkle the tape with the plastic case (Fig. 3-7).

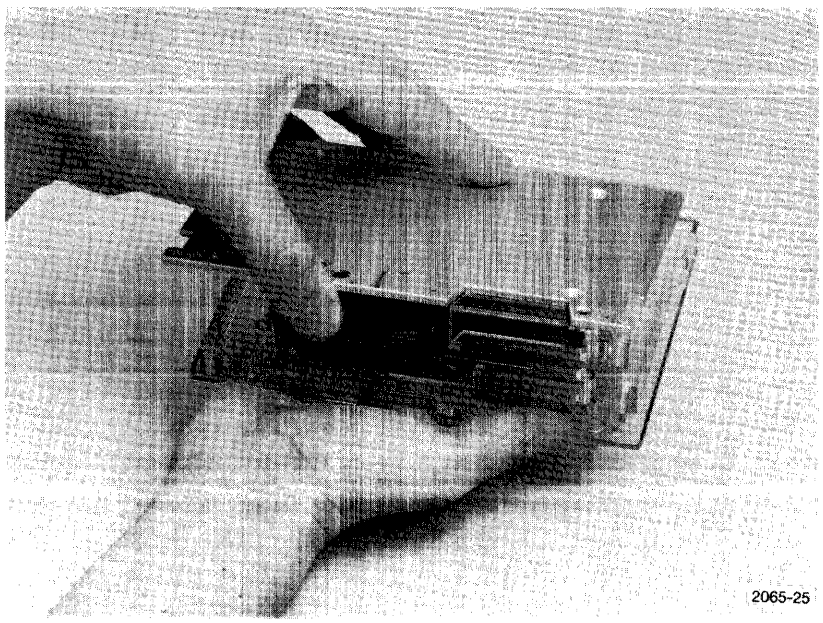


Fig. 3-7. Assembling the tape cartridge.

7. Holding the cartridge together, install the four screws that attach the plastic case to the metal base.

8. Check the light path (refer back to Fig. 3-1) and remove any obstructions (lint, dust, etc.) in the light path. Install the tape cartridge and run a couple of tape exercises (such as REWIND, TLIST, etc.) to ensure that the tape problem does not recur. If the problem recurs and you have checked the light sensing assemblies and removed any obstructions, then the system probably has a circuit failure. Refer to the Circuit Description section of this manual.

STATIC-FREE WORK STATION

Some of the devices within the 4051 are highly susceptible to small electrostatic voltages. Therefore, special precautions should be taken to avoid circuit damage during the handling of naked or unprotected circuit boards. Our replacement circuit boards are packed in special bags that are made of electrically-conductive polyethylene. Boards that are shipped back to regional Tektronix field offices or to the manufacturing facilities in Oregon require the same electrostatic protection afforded by these special bags.

It is recommended that servicing the 4051 be performed at a static-free work station by qualified personnel.

A typical static-free work station (Fig. 3-8) consists of a table with an electrically conductive top. The surface material should be resistive, such as carbon or treated polyethylene, instead of being highly conductive as in the case of metals. The table top should be grounded through a resistor of approximately 200 kΩ to 500 kΩ. The service technician should wear a conductive wrist strap that is tied to the table top by 100 kΩ of series resistance. All test equipment should be grounded. No implements capable of generating or holding a static charge should be allowed on the work surface—this includes most note paper.

An approved warning label to be used on shipping cartons is illustrated in Fig. 3-9.

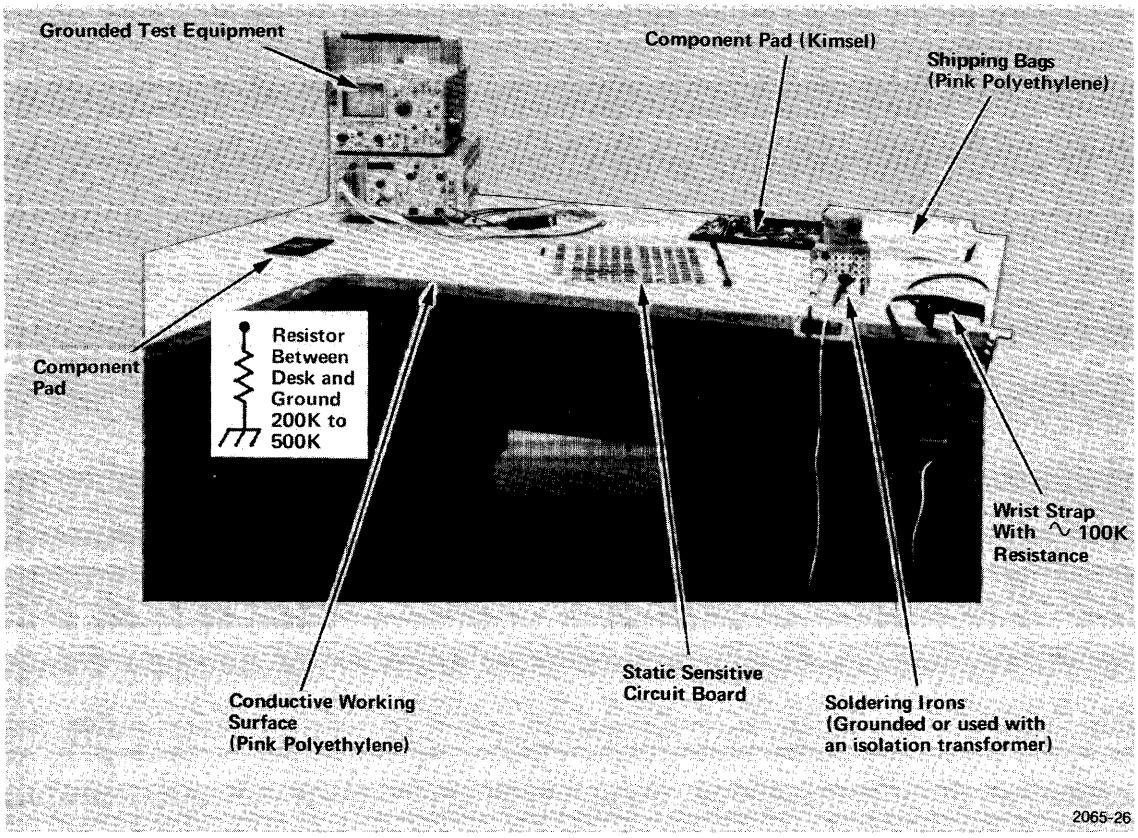


Fig. 3-8. Typical static-free work station.

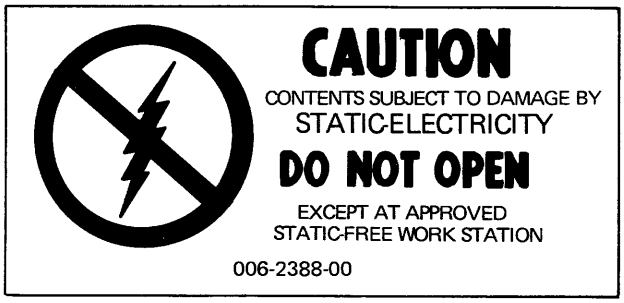


Fig. 3-9. Approved warning label for outside of shipping cartons.

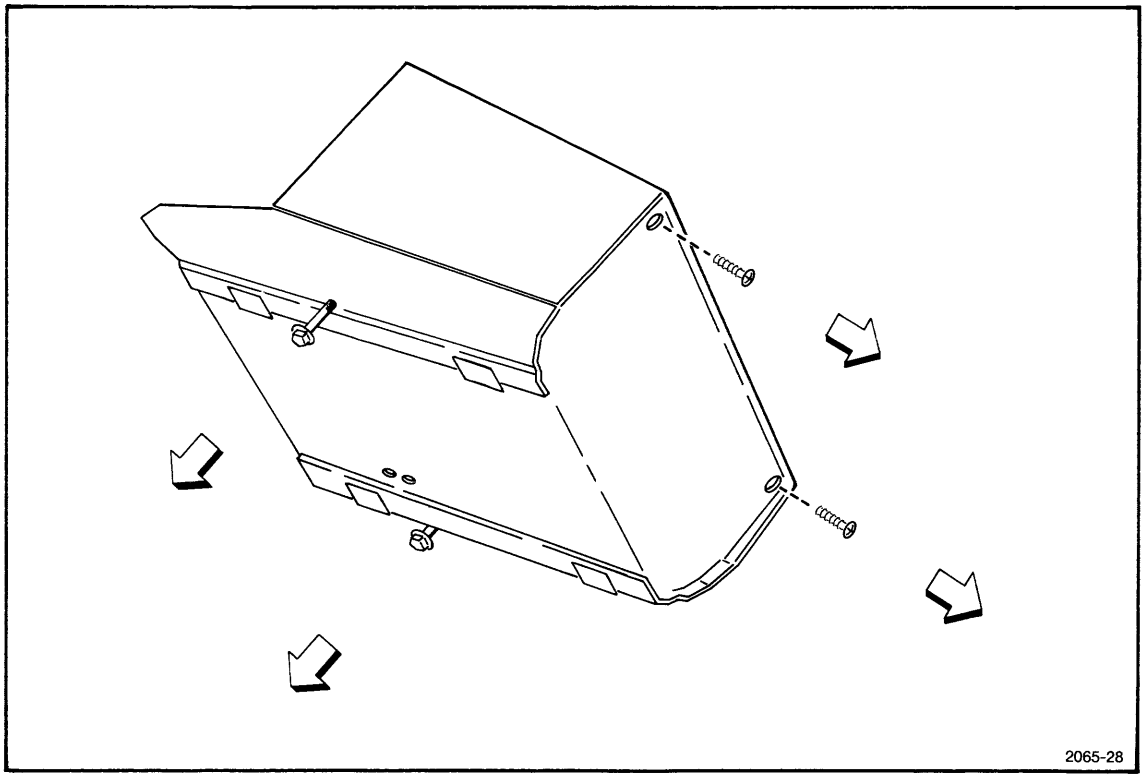


Fig. 3-10. Cover mounting bolts.

DISASSEMBLY/ASSEMBLY

REMOVING THE COVER AND BACKPACK

1. Removal of the cover provides access to most test points and system adjustments.

2. Remove the power cord from the rear of the 4051. Using a 5/16" hex driver, loosen the two bolts on the lower sides of the 4051. Using a #2 Phillips screwdriver, remove the two rear bolts that secure the 4051 cover (Fig. 3-10).

3. The cover can then be removed as shown in Fig. 3-11. To replace the cover, the rear corners are seated first, then the front of the cover is lowered.

4. Remove the backpack by removing four Phillips screws (Fig. 3-12) and then pull gently near the bottom of the backpack to separate the edge card connectors. Note that the shorter screws were removed from the top of the backpack.

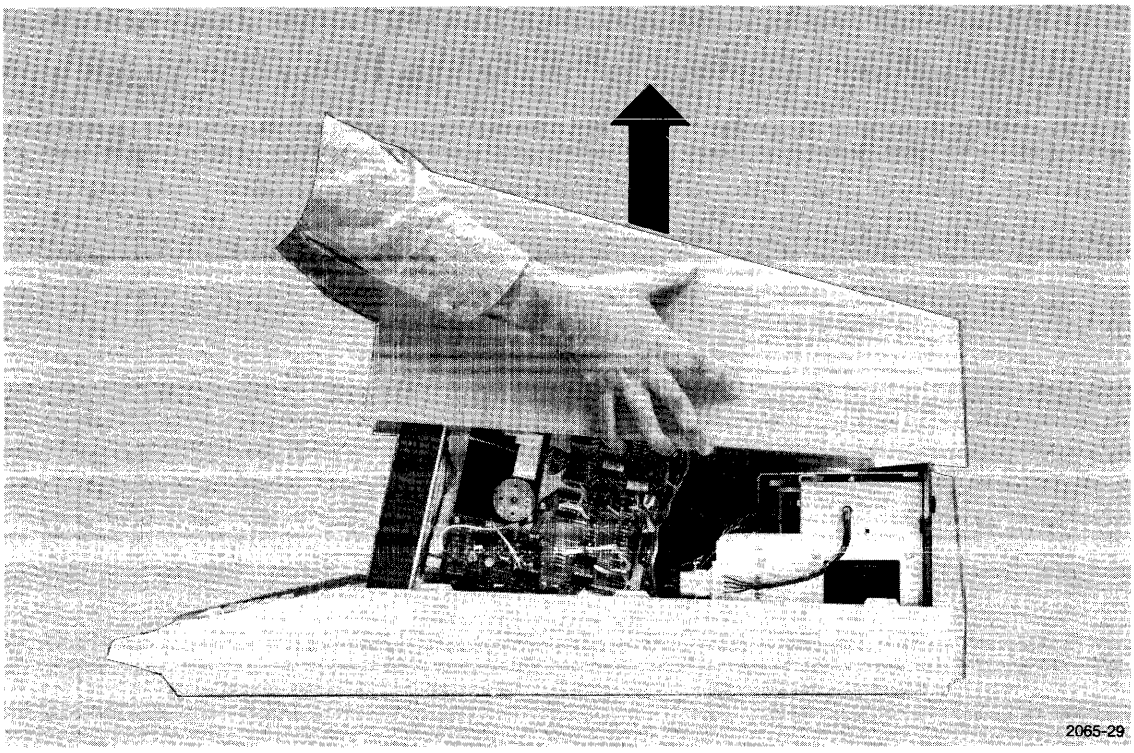


Fig. 3-11. Cover removal.

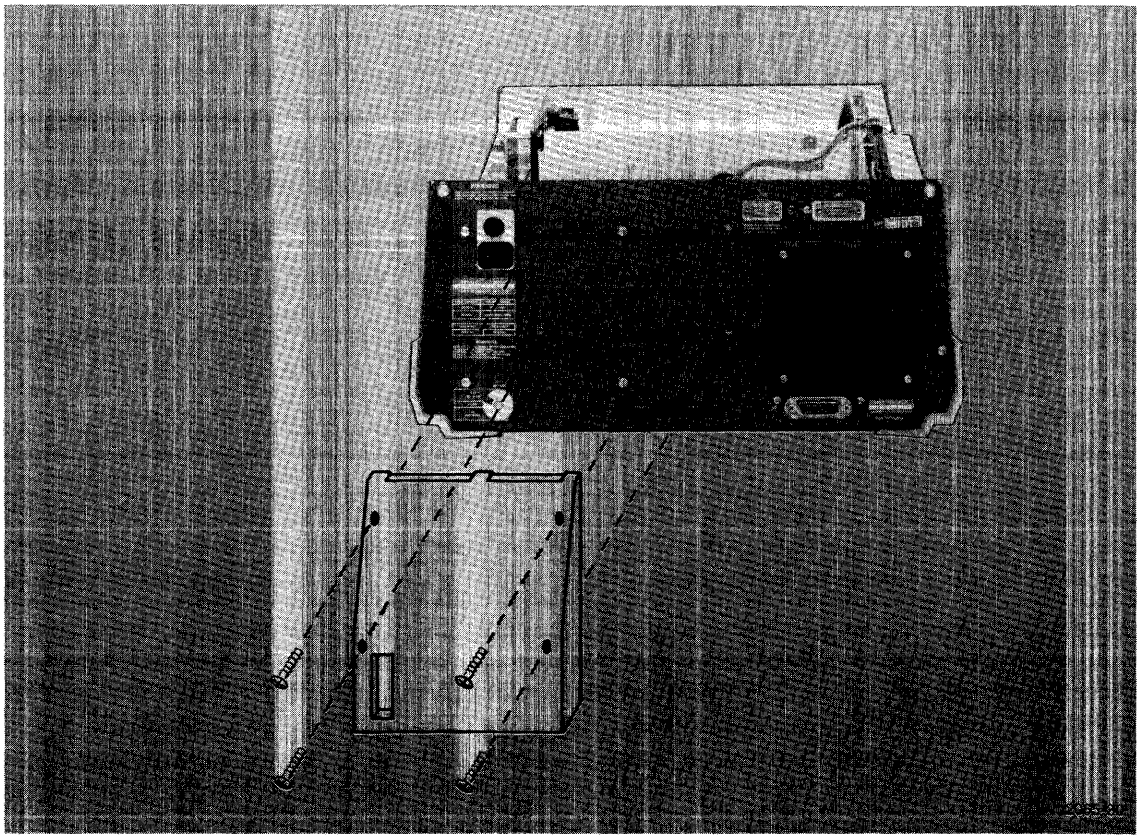


Fig. 3-12. Backpack removal.

KEYBOARD ACCESS

1. Make sure there is no tape cartridge in the system.

2. Remove the front coverplate that frames the crt face, indicator lights and EJECT button. This is done by lifting on the top flange of the coverplate and then pulling forward (Fig. 3-13). You may have to help it over the EJECT button.

3. Using the Phillips screwdriver, remove the bolts that secure the keyboard (Fig. 3-14).

4. Use the pushing motion shown in Fig. 3-15 to force the keyboard against the display. Pull up on the right top corner, and hold. With the other hand, lift up on the right edge of the keyboard starting at the top. Slide your lift motion forward until the bottom edge comes free

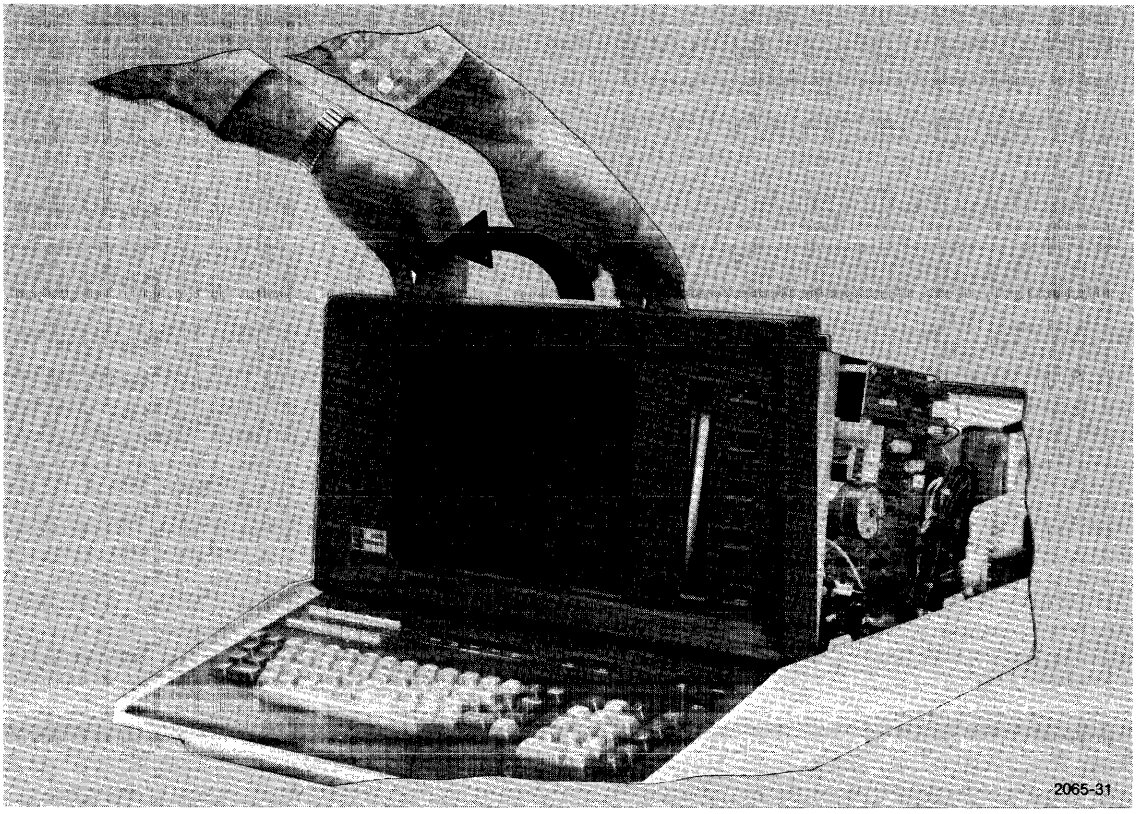


Fig. 3-13. Front coverplate removal to gain access to crt, keyboard, cpu board and memory board.

from its retainer groove. Slide both hands around to the bottom and lift, pulling towards you. A flat-blade screwdriver is helpful to lift the front of the keyboard from the cabinet.

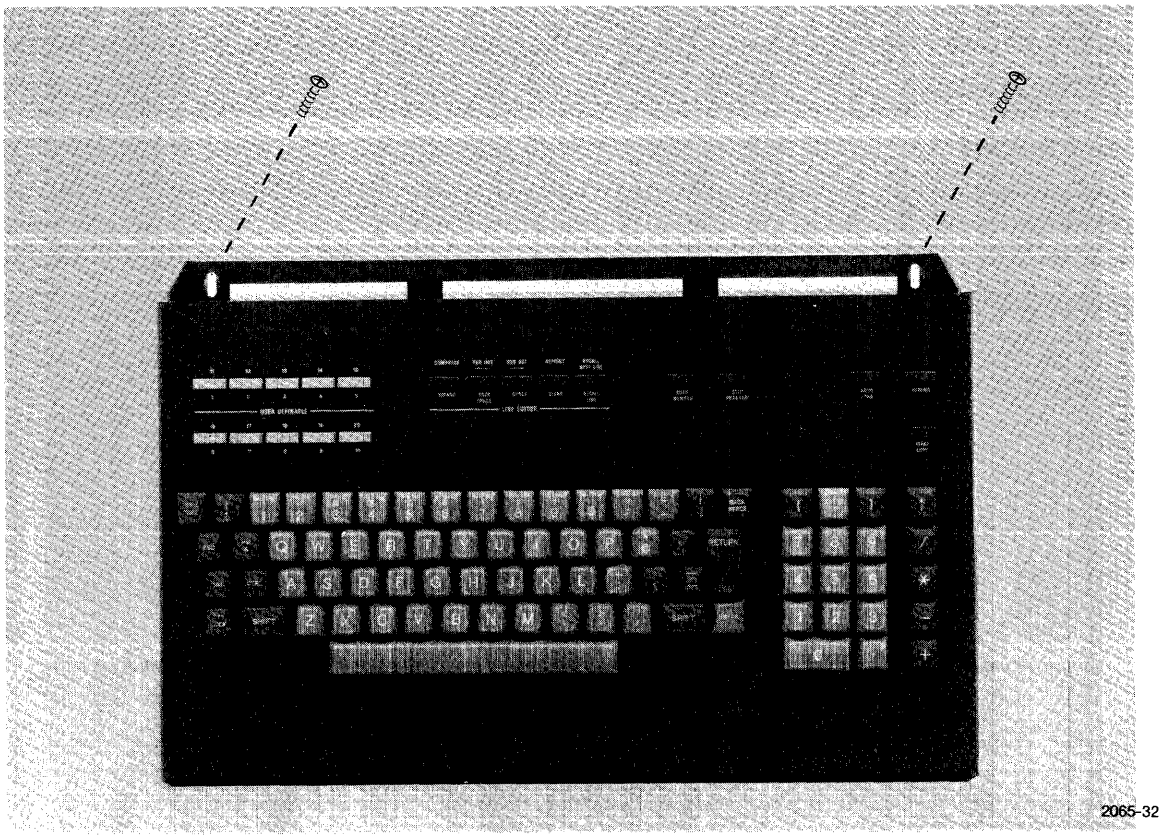


Fig. 3-14. Keyboard screws.

5. Either disconnect the two keyboard connectors (J30 and J31) and remove the assembly, or place an insulating pad (e.g., computer print-out sheets) on the top of the crt shield and rest the keyboard on it.

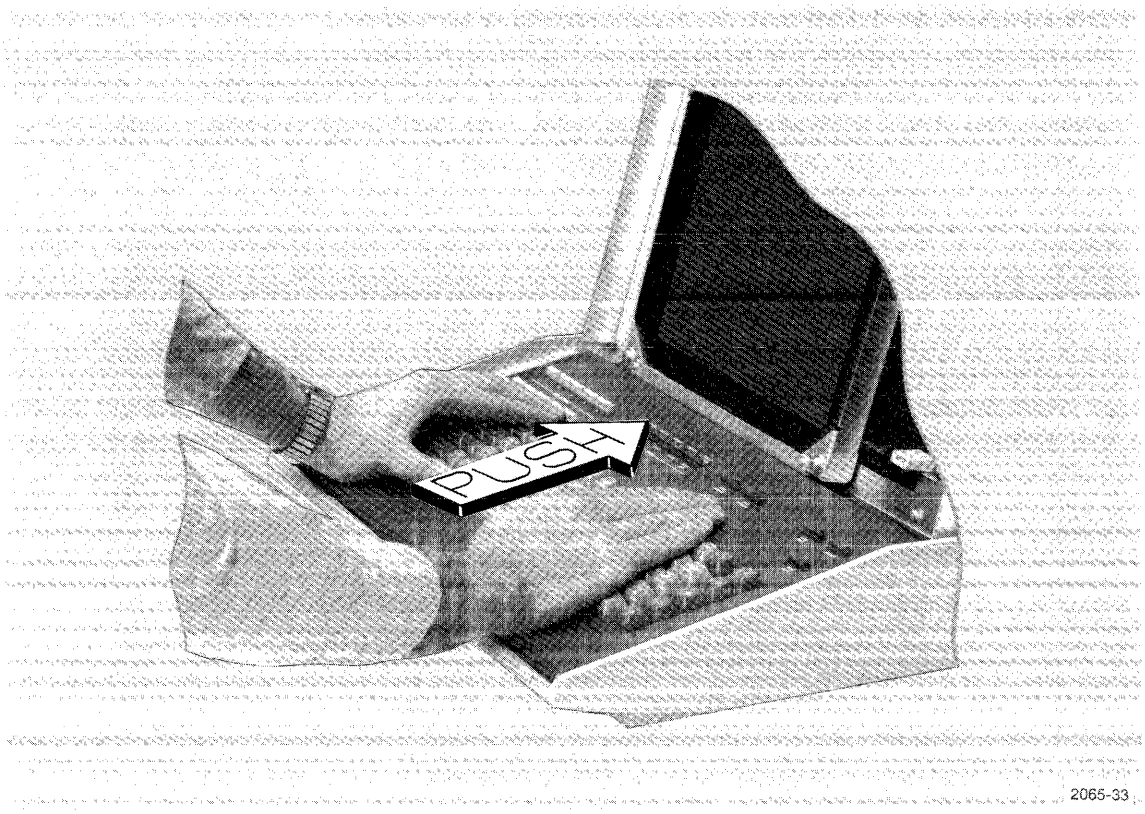


Fig. 3-15. Keyboard removal to gain access to cpu board and memory board.

6. Further disassembly of the keyboard module is accomplished by removing the 12 Phillips screws that secure the circuit board.

CRT FILTER ACCESS

1. The front coverplate and keyboard should be removed as previously described.

2. The crt filter has a foil strip around the outer surface to provide an electrical barrier to control electromagentic inteference. This foil strip will be used as a reference during replacement. If a new filter is to be installed, the foil strip goes toward the face of the crt. The filter side affording the least amount of reflection should be placed outward when installed in the 4051.

3. Remove the top angle bracket from the crt mounting assembly (Fig. 3-16), after removing the two screws, one on each end. Loosen the screws on the lower angle bracket.

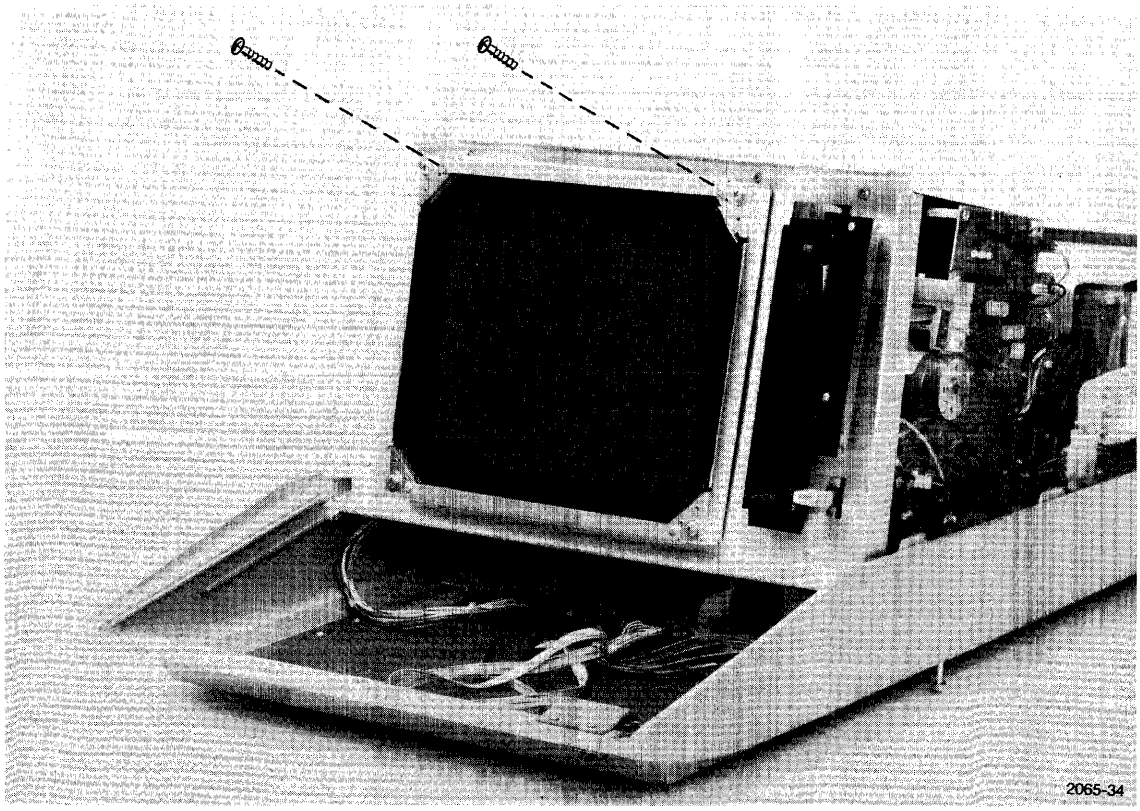


Fig. 3-16. CRT filter access and removal.

4. Remove the filter from the crt mounting bracket. Use caution to avoid scratching or breaking the filter.

5. Cleaning. Clean the face of the crt and the under-side of the filter using a soft cloth and a mild soap and water solution. Note that the under-side can be distinguished from the outer surface by the masking tape if the original is being reinstalled. If the old filter is being replaced with a new one, the under-side can be determined by comparing it with the old filter. Note that less glare from reflected light is apparent on the outer surface than on the under surface of the filter.

6. Installation. Put the filter in place in the recess in the neoprene mounting ring. The outer surface should be flush with the edge of the frame when properly installed. It may be necessary to use a non abrasive device (such as a toothpick) to work the filter into place.

7. Install the angle brackets and fastening screws.

CRT AND DEFLECTION YOKE REMOVAL AND INSTALLATION

WARNING

The crt may implode if it is scratched or struck severly. Do not handle the crt by its neck. Wear protective clothing and a face shield when handling the crt. Use glycerin for a crt neck lubricant.

CRT Removal

1. Remove the cover and crt faceplate as previously described.

2. Remove the writer gun connector from the base of the crt's neck (Fig. 3-17).

3. Remove the crt nect shield then replace the nuts on the yoke adjustment without the shield.

4. The crt may or may not have one or two magnet rings installed on its neck (Fig. 3-18b). If rings were installed, note that the ring positions are marked as in Fig. 3-18a and then slide the ring(s) off the neck of the tube. If the rings are not removed, they may fall onto the circuit boards and damage some components.

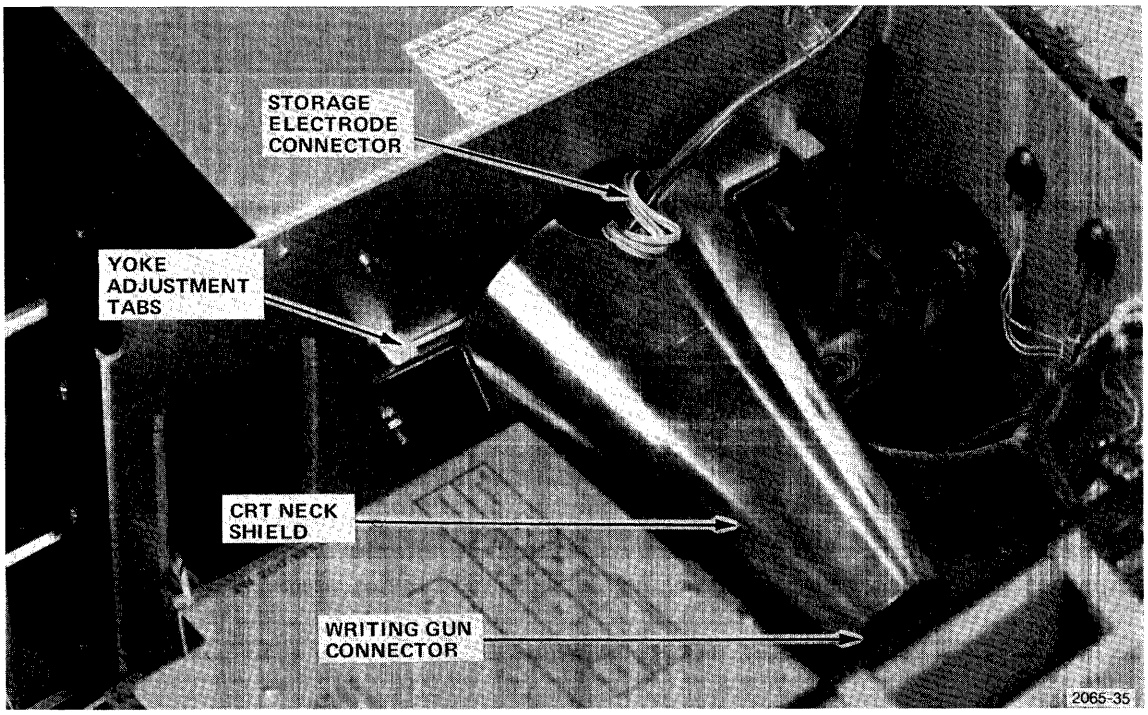
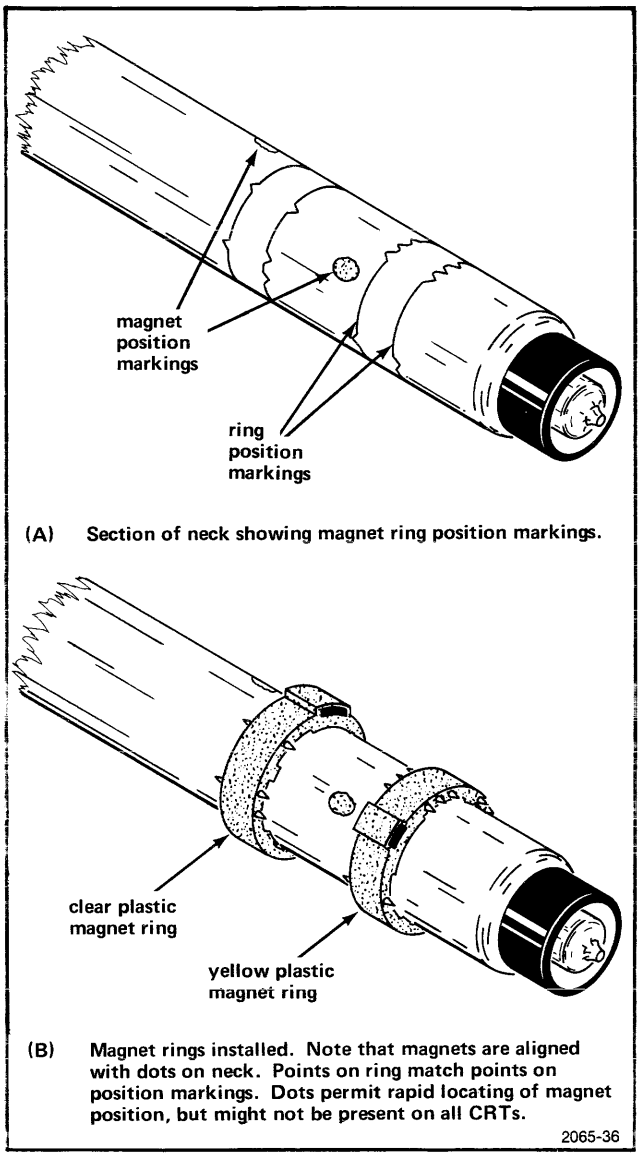


Fig. 3-17. CRT neck shield, crt electrodes and yoke adjustment assembly.



(A) Section of neck showing magnet ring position markings.

(B) Magnet rings installed. Note that magnets are aligned with dots on neck. Points on ring match points on position markings. Dots permit rapid locating of magnet position, but might not be present on all CRTs.

2065-36

Fig. 3-18. CRT Magnet ring location details. The magnet rings should be used only when supplied with the CRT.

5. Remove the four screws from the frame that holds the face of the crt in place. Then remove this metal frame (Fig. 3-19).

6. Apply *glycerin* lubricant sparingly to the nect of the crt using a cotton swab. DO NOT DROP LUBRICANT ONTO THE CIRCUIT BOARDS:

7. Slide the crt out the front of the unit using a rotating motion (not a sideways motion) about the neck axis. The rotating motion enables crt removal from the yoke—the neoprene ring in the yoke tends to bind otherwise. DO NOT PLACE SIDE PRESSURE ON THE NECK. DO NOT HOLD BY THE NECK.

8. Remove the storage electrode from the body of the crt near the neck.

9. After crt removal, place the crt on a firm but padded surface. The neoprene sleeve around the neck and the larger ring around the screen can be removed at this time. Water or *glycerin* may be used to assist removal of the small neoprene ring (yoke sleeve).

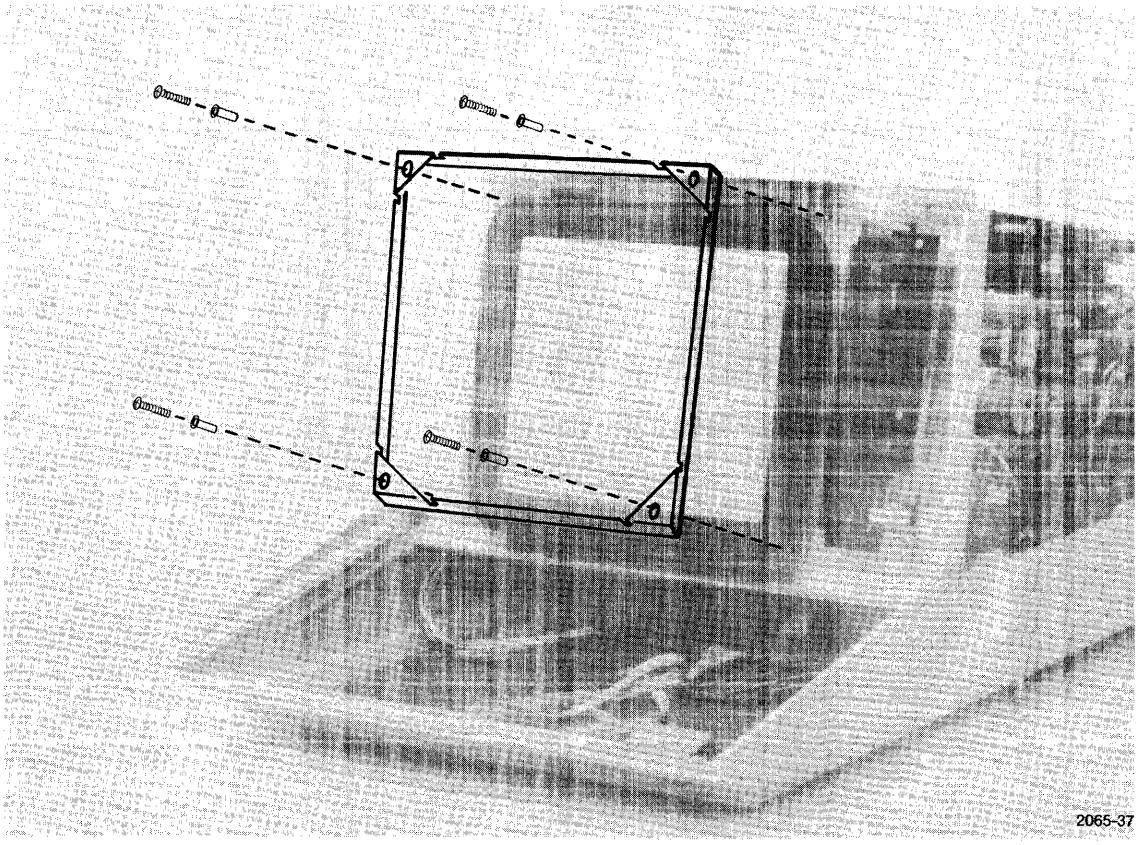


Fig. 3-19. Removing the crt faceplate mounting frame.

Deflection Yoke Replacement

1. Remove the crt as previously described.

2. The yoke may now be replaced. Note that the adjustment tabs of the yoke assembly must be upward.

3. Mount the new yoke in the instrument without the neck shield. Loosen, but do not remove the screws that hold the yoke to the adjustment fixture. The adjustment fixture and yoke must be free to move.

4. Replace the crt.

CRT Installation

1. Make sure the yoke is mounted and the nuts on the adjustment assembly are loosened but not removed.

2. Insert the small neoprene ring (yoke sleeve) into the deflection yoke and lubricate the inner surface with *glycerin*. Use a swab and *avoid getting any lubricant onto the circuit boards* in the base of the 4051. Very little glycerin is required (Fig. 3-20).

3. Place the large neoprene ring around the screen of the crt that is to be placed into the system.

4. Use *glycerin* to lubricate the nect of the crt so it may slide freely through the neoprene sleeve in the deflection yoke. Very little *glycerin* is needed.

5. Place the neck shield behind the deflection yoke to accommodate the neck of the crt.

6. Carefully insert the crt into the front of the instrument. Connect the storage electrodes to the crt before placing the neck into the deflection yoke.

7. Place the neck into the deflection yoke and slide the crt into the instrument. STOP if binding occurs at the neck; then use a rotating motion to remove the crt; lubricate the neck elements with *glycerin* and try again to install the crt.

8. Place the metal mounting frame around the rubber collar at the face of the crt and secure it to the chassis (Fig. 3-21). Be careful to tighten the screws evenly to avoid sideways movement of the crt's neck. The light metal pieces of the mounting frame should not be deformed by the rubber collar. The collar may have to be manipulated slightly during assembly to ensure proper seating of the mounting frame.

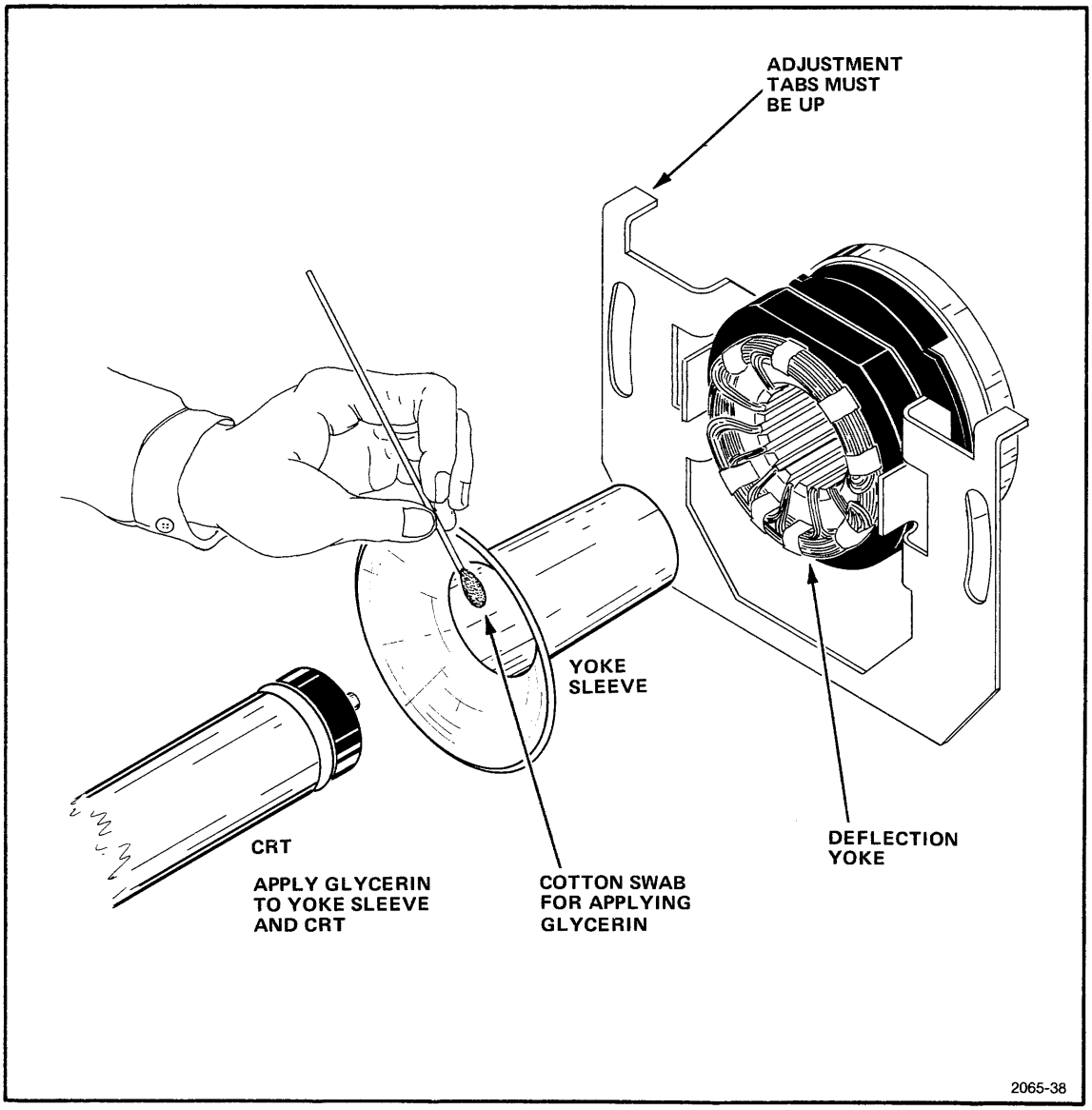


Fig. 3-20. Lubrication and installation of the crt as part of the installation procedure.

9. After fastening the mounting frame to the chassis, replace the magnets (Fig. 3-18) if any are required on the crt neck.

10. The deflection yoke is to be pressed firmly against the body of the crt and the screws holding it to the adjustment fixture tightened.

11. Remount the neck shield to the deflection ajdustment assembly with the two nuts provided (Fig. 3-17).

12. Attach the writing gun connector to the base of the crt.

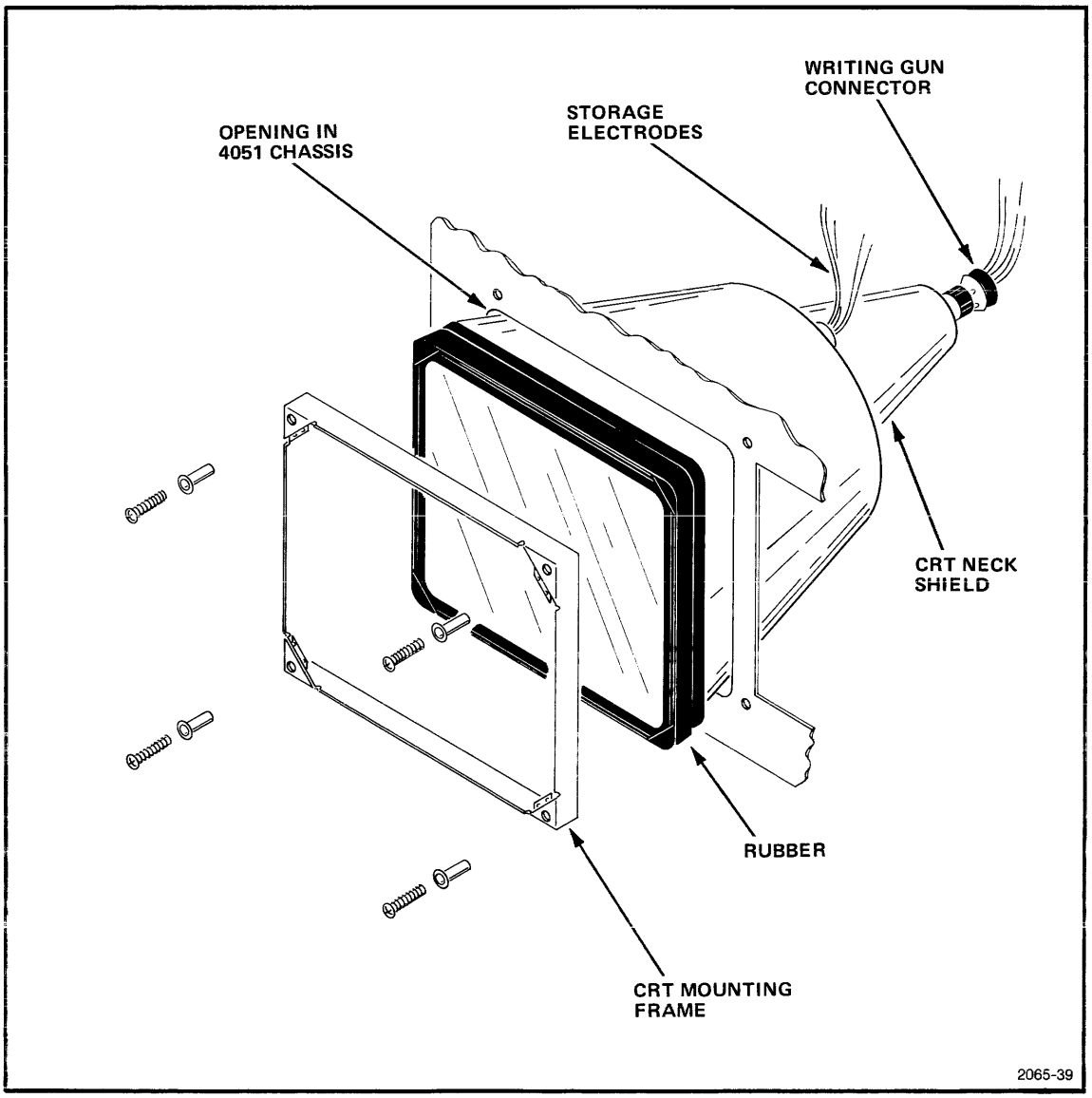


Fig. 3-21. Mounting the crt into the 4051.

13. Replace the crt faceplate shield or filter over the screen of the crt.

14. Reassemble the instrument to a working configuration and perform the display adjustment procedures found in the Calibration section of this manual.

POWER SUPPLY ACCESS

1. Remove the backpack and cover to the 4051 as previously described.

2. Remove all connectors and Phillips screws as shown in Fig. 3-22. The screw to be removed last is marked in the illustration.

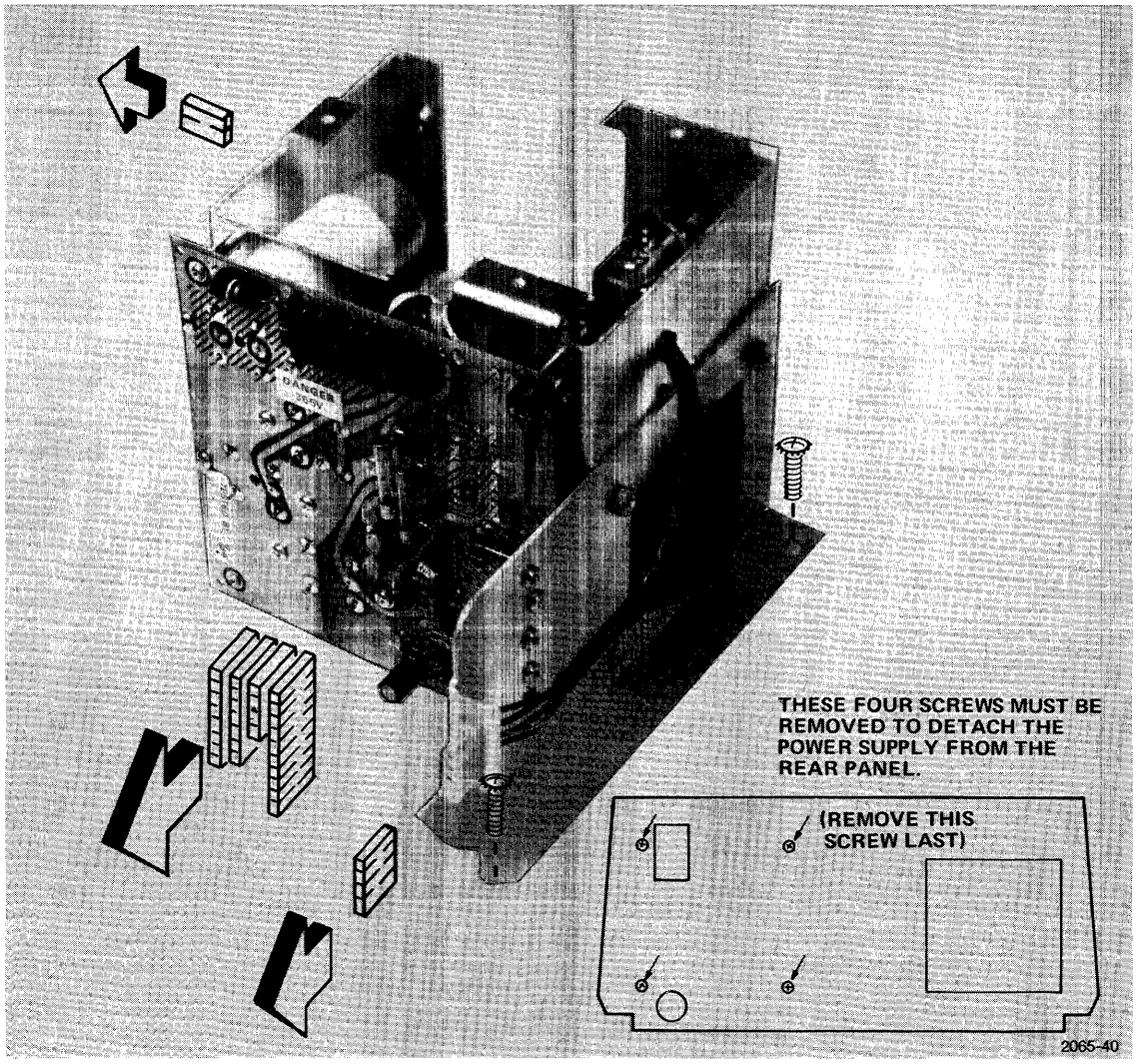


Fig. 3-22. Power supply removal procedure.

3. The power supply module can now be lifted up and out. Be careful to not wipe off the silicon gel on the bottom flange. Further disassembly of the power supply module is accomplished with the Phillips screwdriver. In order to remove the etched circuit board, the six heat-sinked transistors must be unscrewed from the mounting bracket.

CPU BOARD/MEMORY BOARD ACCESS

1. Memory boards and cpu boards have devices that are highly susceptible to low electrostatic voltages. It is recommended that assembly and disassembly procedures be performed at a static-free work station. Devices that are mounted in the boards are not as susceptible to static as are unmounted circuit components.

2. Note the polarities of and remove the three connectors from the front of the cpu board: harmonica connectors J3 and J4 and ribbon connector J2.

3. Remove the six Phillips screws that secure the cpu board to the chassis (Fig. 3-23). Note that screws holding the display board chassis may have to be removed in order to properly replace the cpu board.

4. Pull the cpu board out gently, by its supporting rails. The memory board is mounted on top of the cpu board, so exercise care in removing the two. Both boards are susceptible to electrostatic discharges.

5. Remove the six Phillips screws that hold memory and cpu boards together.

6. For cpu board or memory board service, place an insulating pad (e.g., a pink polyethylene shipping bag or a carbon impregnated cushion) over the front lip of the 4051 chassis (Fig. 3-24). Paper can develop dangerous electrostatic charges and should *not* be used for the insulating pad. Place the memory board alongside. Reconnect J2, J3 and J4, observing polarity.

DISPLAY BOARD ACCESS

1. Display board test points and connectors are accessible once the 4051 cover is removed.

2. Detach the high voltage protective shield by removing three Phillips screws to gain access to high voltage test points and adjustments.

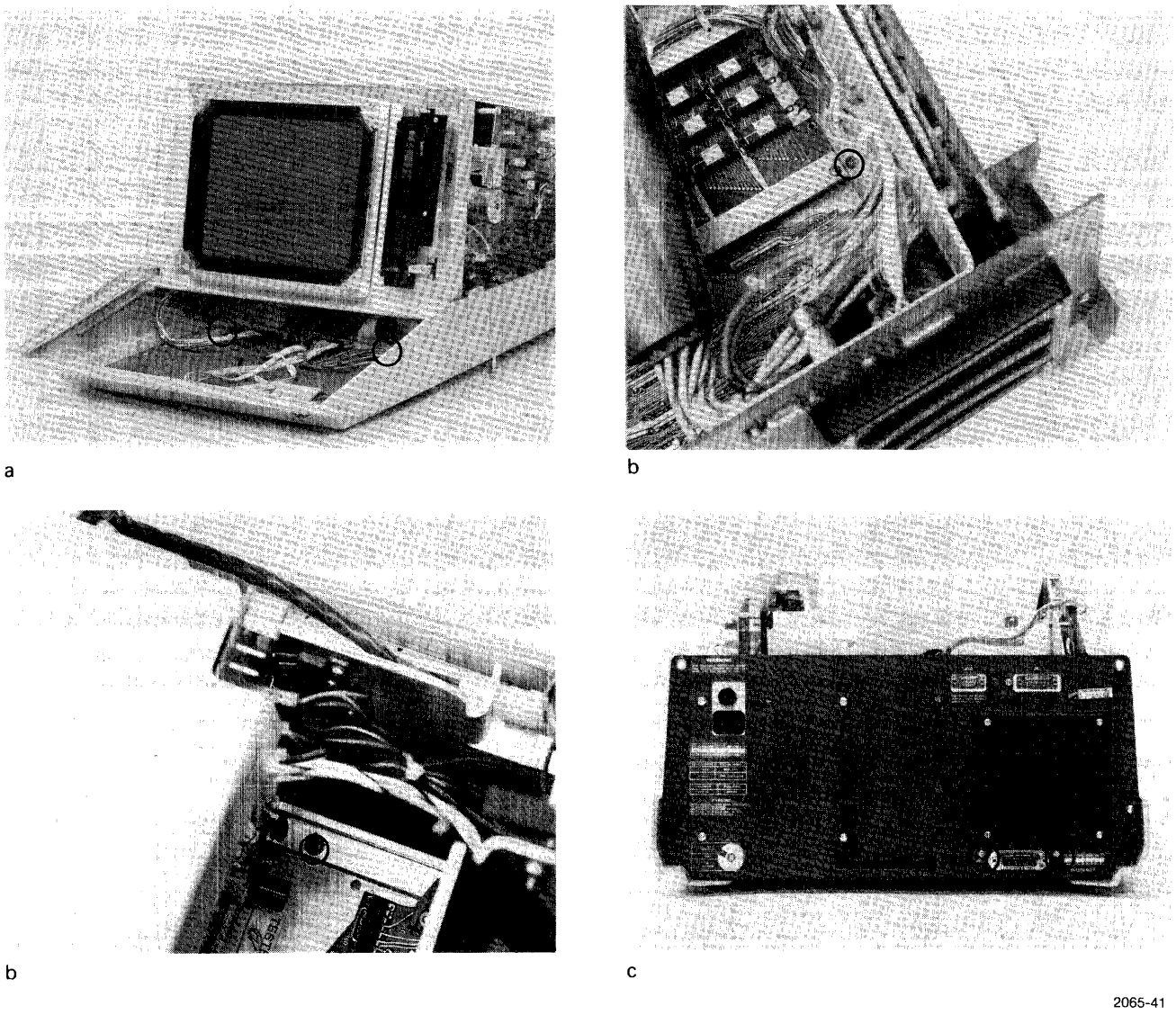


Fig. 3-23. Screw pairs securing the cpu board; (a) front (b) top and (c) rear views.

3. Remove the six Phillips screws and two teflon screws that secure the display board.

4. Remove the nine connectors to heatsinked transistors directly under the board, as well as all other connectors. The crt gun connector is an octal-type which is detached with a gentle pull on the wires that exit the rear of the crt neck shield (Fig. 3-25).

5. Remove or replace the display board. Use extreme caution in replacing all connectors just as they were removed.

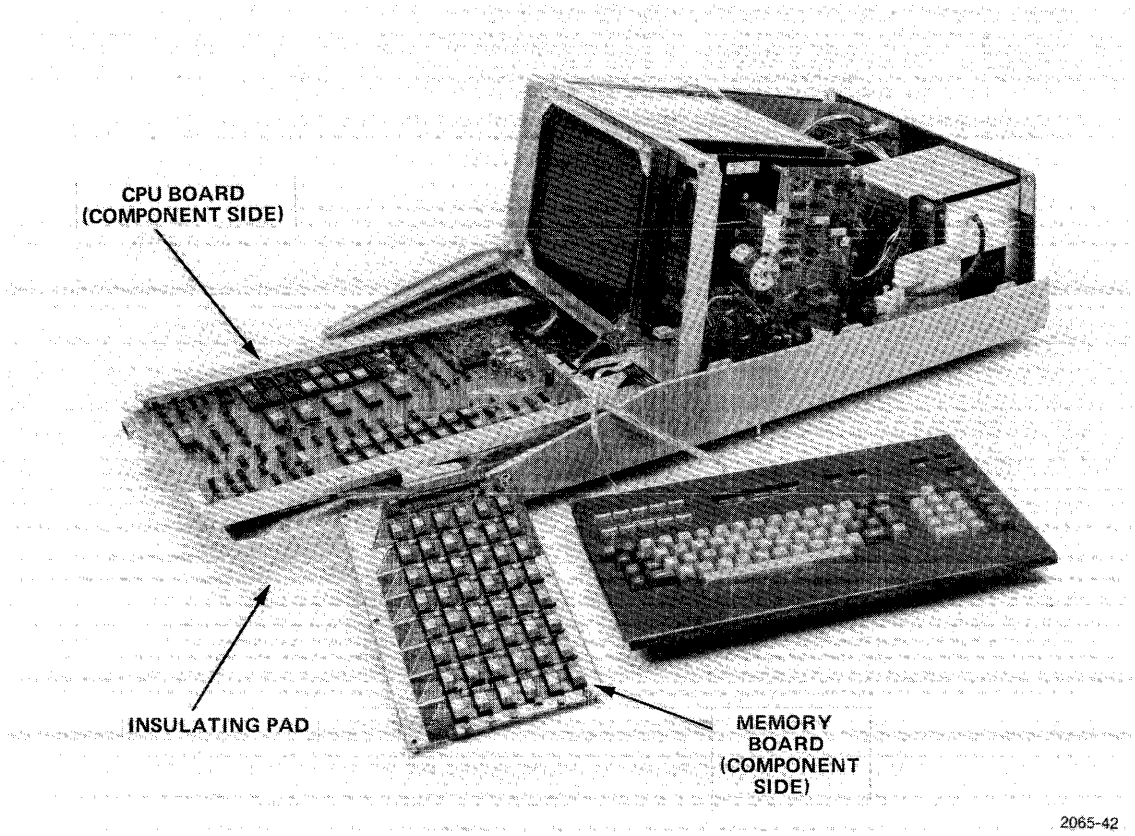


Fig. 3-24. Service layout for cpu board and memory board. The insulating pad is to be pink polyethylene or a carbon impregnated foam to protect the circuit components from dangerous electrostatic voltages.

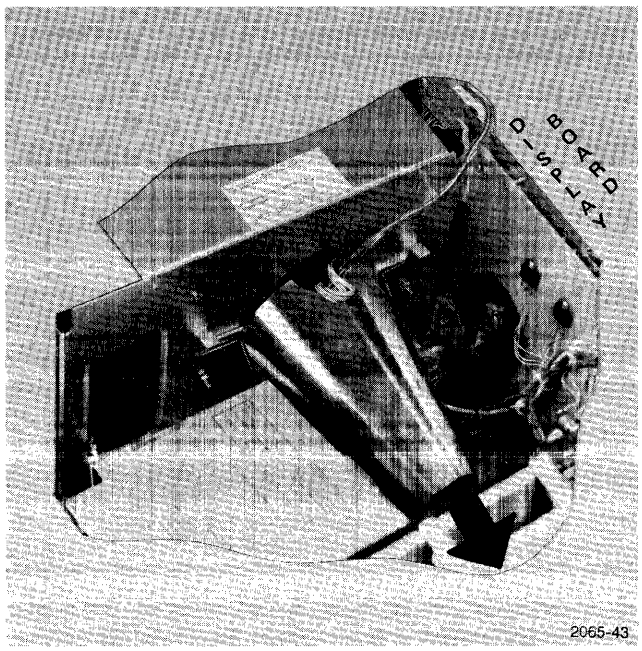


Fig. 3-25. CRT writing gun connector removal.

MAGNETIC TAPE ASSEMBLY ACCESS

1. Access to the magnetic tape drive board is obtained by removal of the 4051 cover. For complete disassembly or replacement, use the following procedure:

2. Remove the two Phillips screws on the right front of the 4051, one just above the BUSY indicator light, the other just below the EJECT button (Fig. 3-26).

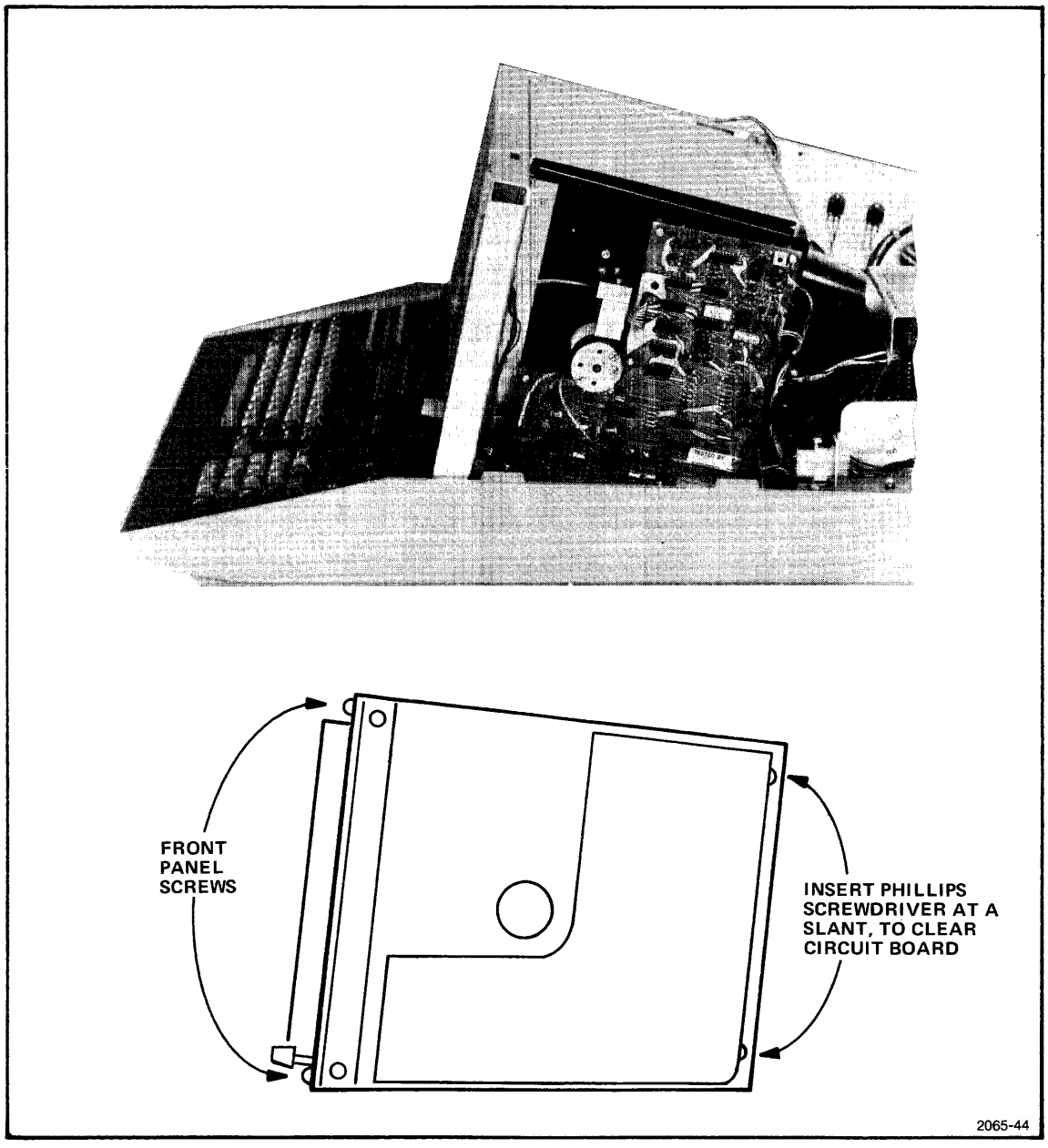


Fig. 3-26. Tape unit assembly with pointers to the mounting screws.

3. Remove the two Phillips screws on the mag tape assembly (also shown in Fig. 3-26). Remove all connectors, and then slide the unit back and up, allowing the EJECT button to be drawn through the front panel.

4. Further disassembly, as for replacement of mechanical parts or circuit boards, proceeds as follows: remove the 8 Phillips screws that secure the tape drive board to the assembly, and remove connectors.

Section 4

4051 CALIBRATION

GENERAL

This procedure covers all 4051 potentiometer settings. If a unit is fully calibrated but still does not perform to specifications, then the troubleshooting aids of Section 5 should be used.

EQUIPMENT REQUIRED

Phillips screwdrivers #1 and #2 points
5/16", 11/32" Hex drivers
Small shaft (1/8") standard blade screwdriver
Insulated alignment tool (1/8" or smaller blade)
3/32" Allen wrench
Digital counter (DC 501 or equivalent)
Voltmeter (DM 510 or equivalent)
High Voltage probe for 4 kV
Calibration tape cartridge (067-0781-00)
15 MHz Dual trace oscilloscope (DS 502 or equivalent)
Deflection alignment graticule (067-0654-00)

With power off, remove the 4051 cover (Fig. 4-1) to gain access to most of the circuit adjustments. Take care not to catch the circuit components with the cover.

POWER SUPPLY

1. Check the power supply strapping on the transformer and set it for the line voltage range at which the 4051 is to be operated. Then rotate the yellow indicator ring on the back of the system to indicate the strapped voltage range of the system. Replace the transformer shield.

2. Check the power line fuse and replace it with the appropriate value: 1.6 A medium-blow for 120 volt operation, 0.8 A medium-blow for 220 volt operation.

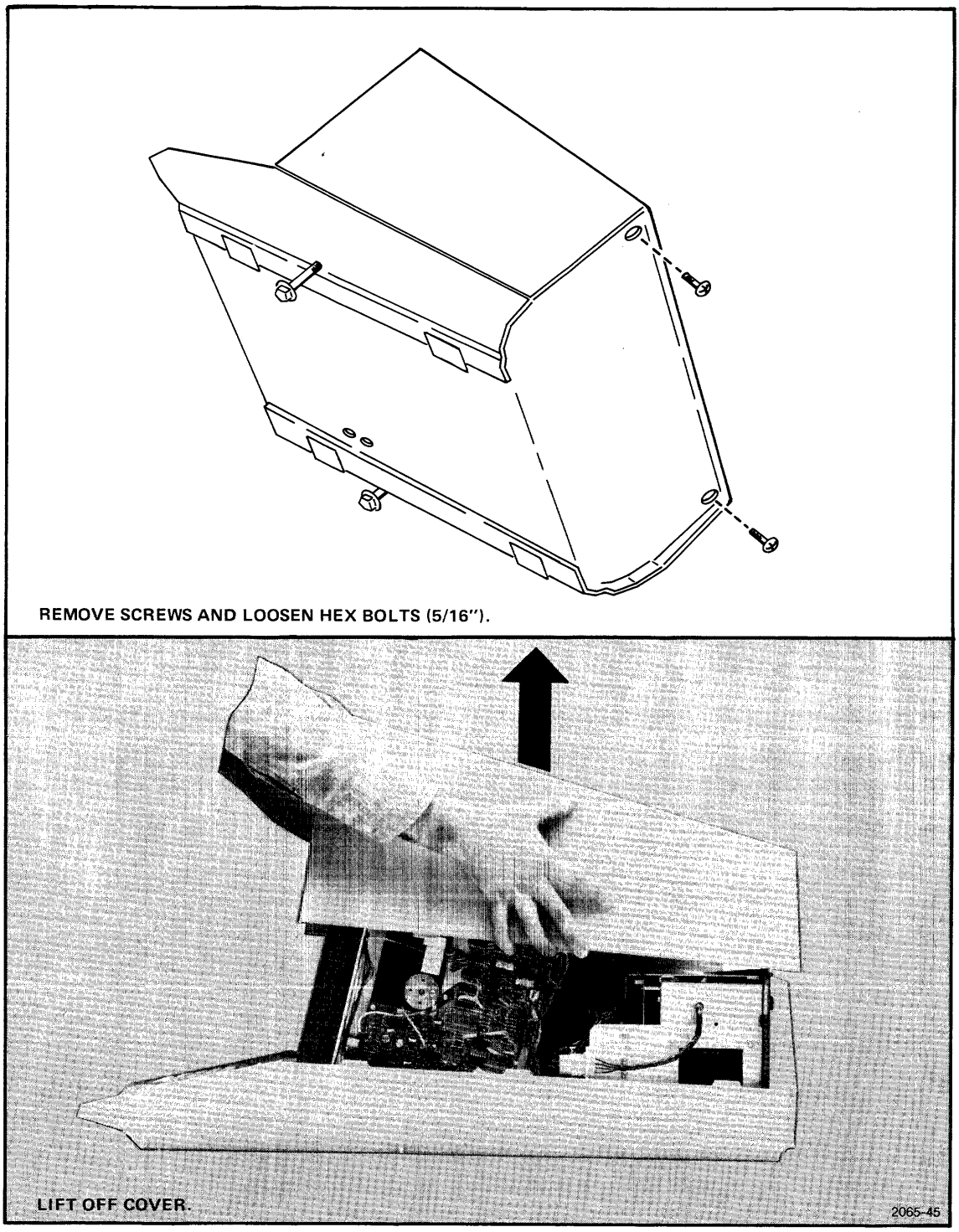


Fig. 4-1. Remove the cover from the 4051 to gain access to most of the circuit adjustments.

3. Adjust the +15 volt supply by placing a voltage meter on the +15 volt test point (TP51) and power up (Fig. 4-2). A ground pin (TP50) lies adjacent to the +15 volt test location. Adjust R51 for +15 volts (limits are: 14.85, 15.15).

4. Check the regulated supplies at J21.
   +12 volts (11.64, 12.36)
   −12 volts (−12.06, −11.94)
   +5 volts (4.90, 5.10)

5. Figure 4-2 also points to several other components that should be checked if problems are encountered.

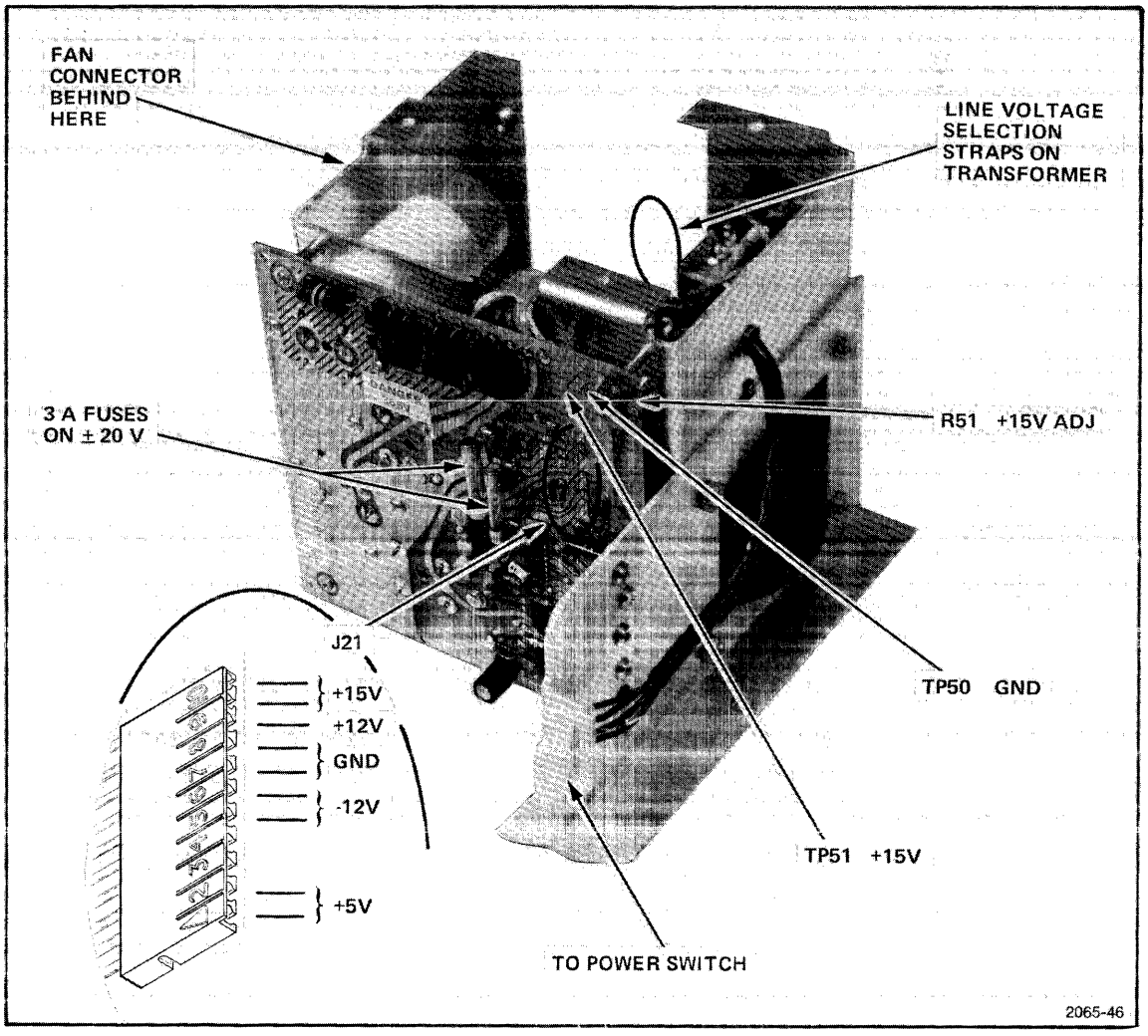


Fig. 4-2. Power supply check points and adjustments.

DISPLAY CALIBRATION

1. Power down. Remove the high voltage shield and connect a negative high voltage probe to TP102 on the rear of the display board (Fig. 4-3). Ground the meter to chassis or to the power supply ground pin. Power up, and adjust R224 for approximately −3850 V. Power down, and remove the probe.

2. Remove J50, which will disable the high voltage generator. Place a voltage probe to J58-3. Power up, and adjust R359 for a collimation electrode voltage of about 85 V, or as specified on the crt shield (Fig. 4-4).

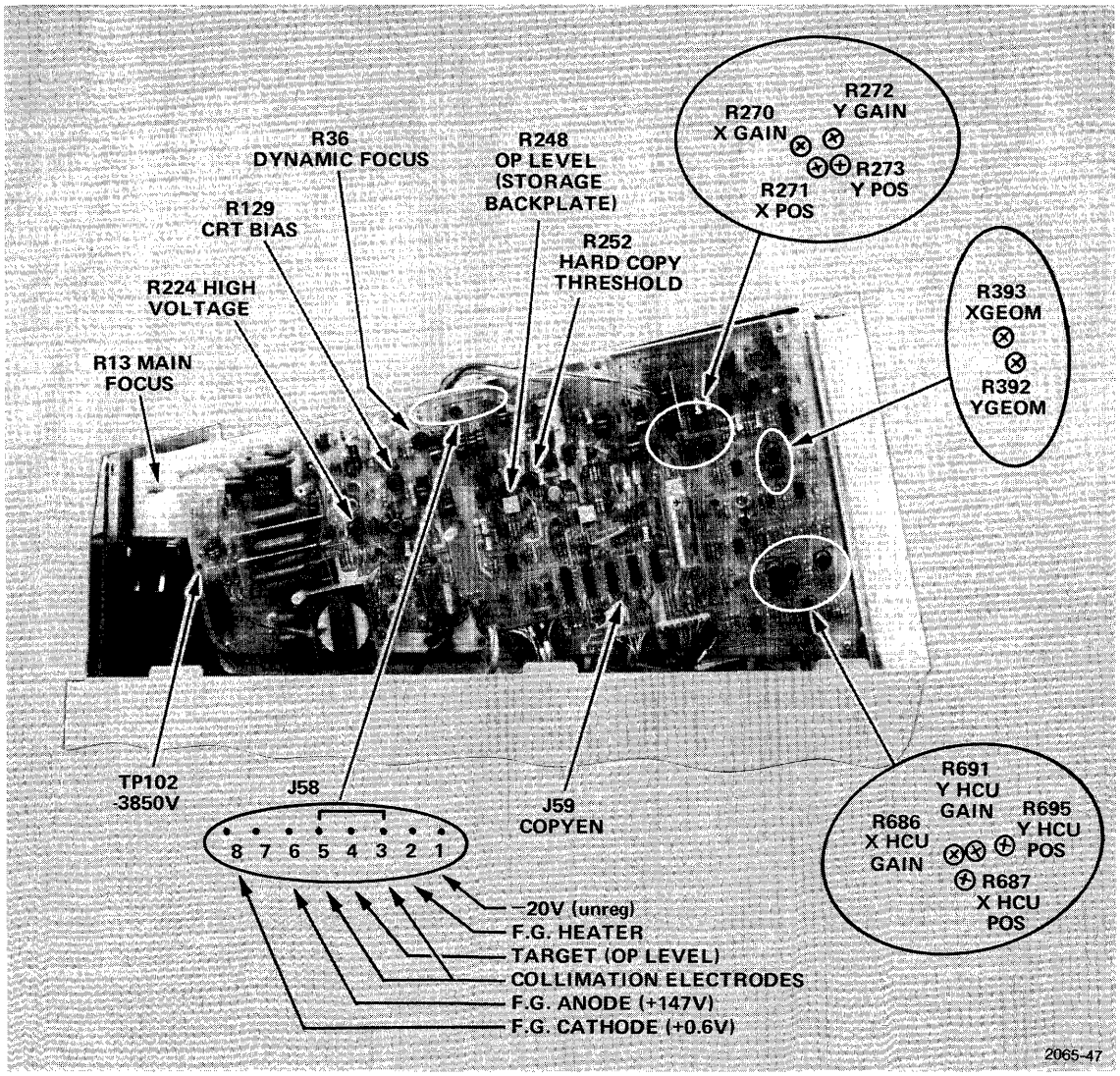


Fig. 4-3. Display board check points and adjustments.

3. Move the probe to J58-4 (Fig. 4-3) and adjust R248 for proper storage backplate voltage (op level). This level should be about 200 V (or as specified on the crt shield).

4. Power down. Reconnect J50. Power up. Adjust R129, the bias level, until a dot is seen in the upper left of the display during a page cycle. Hold down the keyboard PAGE key and back off R129 until the dot just disappears.

5. Tilting the 4051 up on its side, adjust cursor intensity (R683 in Fig. 4-5) until the cursor does not store. To check for storage, press the space key of the Line Editor set while adjusting intensity. This spot is accessed with a screwdriver or insulated alignment tool inserted through the hole in the bottom left of the instrument. There are two holes—use the one towards the *REAR*. (If the cursor remains stored, recheck the crt BIAS and OP LEVEL adjustments).

6. Key in this short program to check focus:

```
SET KEY
4 PRINT "@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@"
5 RETURN
```

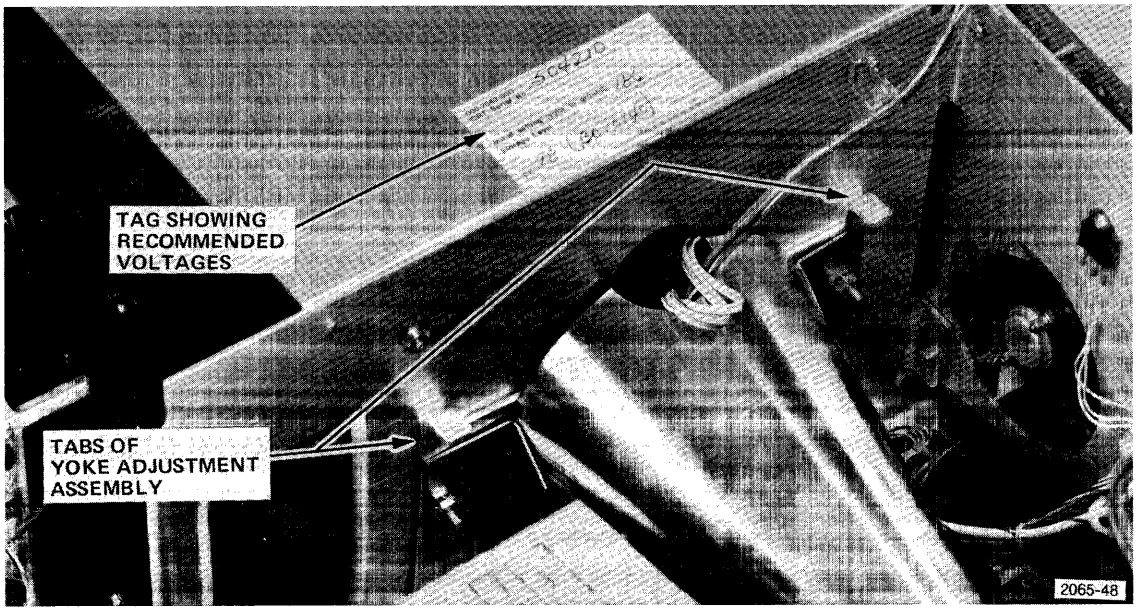


Fig. 4-4. CRT shielded with tag showing recommended electrode voltages. The deflection yoke adjustment tabs are also illustrated.

7. Now push Page. Hold down on User-Definable Key 1 and observe successive lines of @ – signs printed. Adjust the main focus, at the rear of the display board (R13) as lines are printing, until optimum focus is achieved.

8. Page and repeat the previous step, this time adjusting Dynamic Focus (R35). This adjustment affects the difference in focus between that at the center and that in a corner of the screen.

9. Page and repeat the previous procedure of printing @ – signs. This time adjust the character intensity (R685) located under the chassis and just forward from the cursor intensity pot (Fig. 4-5).

   Characters should store, yet not fill in. Some readjustment of the op level may be necessary (see step 3).

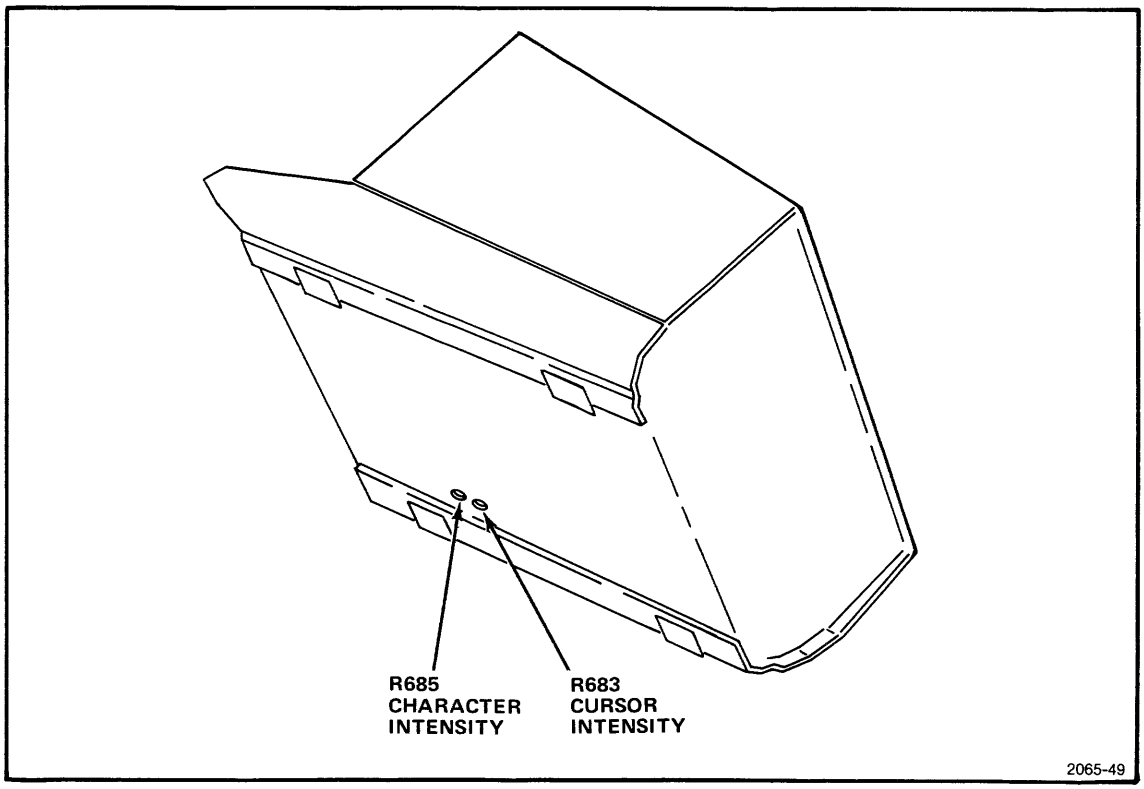


Fig. 4-5. Intensity adjustments underneath the 4051.

10. Before adjusting deflection, enter the following from the keyboard:

```
DEL ALL

100 MOVE 0, 0
120 DRAW 130, 0
130 DRAW 130, 100
140 DRAW 0, 100
150 DRAW 0, 0
160 MOVE 65, 0
170 DRAW 65, 100
180 MOVE 0, 50
190 DRAW 130, 50
200 GOTO 100
PAGE
RUN
```

    You should see a rectangle divided into four equal, smaller rectangles.

11. Now, move the origin shift strap option (located just above J56) to the CAL position. If the display pattern is tilted, the yoke must be rotated. This is done by loosening the two 11/32" Hex nuts which secure the yoke (Fig. 4-4). By means of the two tabs (one projecting from either side of the yoke) rotate the yoke while running the alignment program just keyed. After proper alignment, fasten the nuts, being careful to not disturb the yoke position in doing so.

12. While running the alignment programs, adjust X position, X gain, Y position and Y gain pots (R271, R270, R273, R272 respectively) to obtain a rectangle having dimensions of 19 cm by 14 cm on the display. Adjust for centering, and note that position and gain are interactive.

13. Adjust X Geom and Y Geom (R393 and R392, respectively) to make the vectors in the test pattern straight. Readjustment of position and gain may be needed. For most accurate deflection settings, you should use a 4010 alignment graticule (067-0654-00) and adjust to place the edge of the test pattern into the "racetrack" on the graticule.

14. Replace the origin shift jumper strap of step 11 to the GND position unless hard copy adjustments are to be performed.

HARD COPY ADJUSTMENTS

1. These adjustments can be ignored if no hard copy unit is to be used with this 4051 system.

2. Connect a 4610 or 4631 Hard Copy Unit to the 4051.

3. Disable the paper drive or remove the Hard Copy Paper from the Hard Copy Unit.

4. Place the origin shift jumper strap on the display board to the CAL position.

5. Run the display alignment test pattern program.

   Stop the program, and press the Make Copy key. Adjust X Hard Copy Ramp position (X HCP, R687) and X Hard Copy Ramp Gain (X HCG, R686) to overlay the test pattern by .5 cm on left and right sides. Repeat this step as often as necessary.

6. Adjust Y HCP (R695) and Y HCG (R691) to achieve the same 0.5 cm overlap in the vertical direction.

7. Make another copy, and this time adjust the intensity of the scanning line to a point just below storage. Adjust R224 on the rear panel of the 4051, adjacent to the Hard Copy Unit jack.

8. Connect the scope probes to TP255 and TP257 (Fig. 4-3). Set vertical deflection to 0.5 V/cm, non-inverted. Set sweep rate to 0.5 ns/cm. Set both inputs to ground and position both traces to the second horizontal graticule line from the bottom. Switch both inputs to dc.

9. Connect external trigger probe to the Hard Copy Interrogate signal on J52-5 or U557-9. Press Page, then Make Copy and check for a display resembling Fig. 4-6).

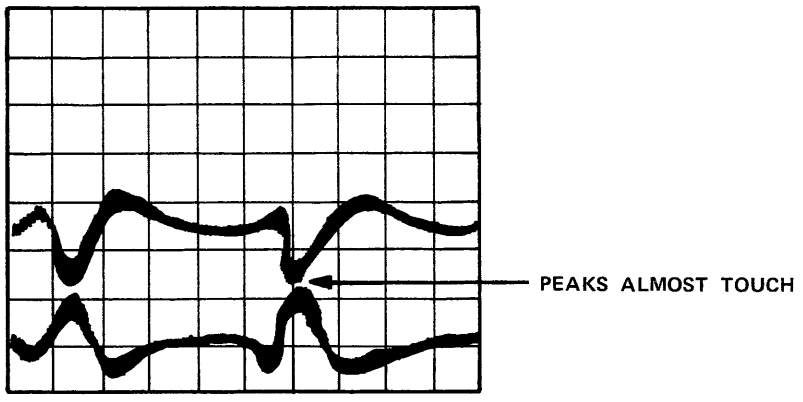


Fig. 4-6. Hard copy threshold with no information stored on the 4051 display.

10. Adjust the threshold pot (R252) until the peaks almost touch, but no overlapping of the two traces occurs.

11. Either enable the paper drive in the Hard Copy unit if it was disabled in step 3 or make sure there is good paper in the Hard Copy Unit.

12. Place a test figure or a page of characters on the display and make a hard copy. Final adjustment of the threshold using a blank screen should be made after inspection of the copy for noise, appearing as black specks.

13. Power down and replace the origin shifter strap to "GND". Replace the cover—calibration is complete.

MAGNETIC TAPE CALIBRATION

This portion of the Calibration Procedure describes adjustments on the tape drive board. There are 4 post and 3 mechanical adjustments, as shown in Fig. 4-7.

1. With no tape inserted, place voltmeter probe to TP591. Adjust Servo Zero Pot (R573) for 0 V ±50 mV. There should be no motor movement.

2. Move the voltmeter probe to TP21. Set the U21 Offset Adjustment (R8) for 0 V ±50 mV.

3. Move the voltmeter probe to TP22. Set the U121 Offset Adjustment (R9) for 0 V ±50 mV. Remove probe.

4. Connect the oscilloscope probes: Channel 1 to TP21, Channel 2 to TP22. Connect the Digital Counter probe to TP231.

   Insert calibration tape and press the AUTOLOAD button. The tape will move at 30 inches per second for approximately 2 minutes.

   Recorded on the first half of the tape is a continuous 10 kHz signal using both channels (observable on scope). The second half is recorded with bursts of 10 kHz, separated by erased zones.

5. Motor speed is adjusted during the *first* half of the calibration tape. Set the motor speed pot for 10 kHz ±1% (9.9—10.1 kHz) as measured on the counter.

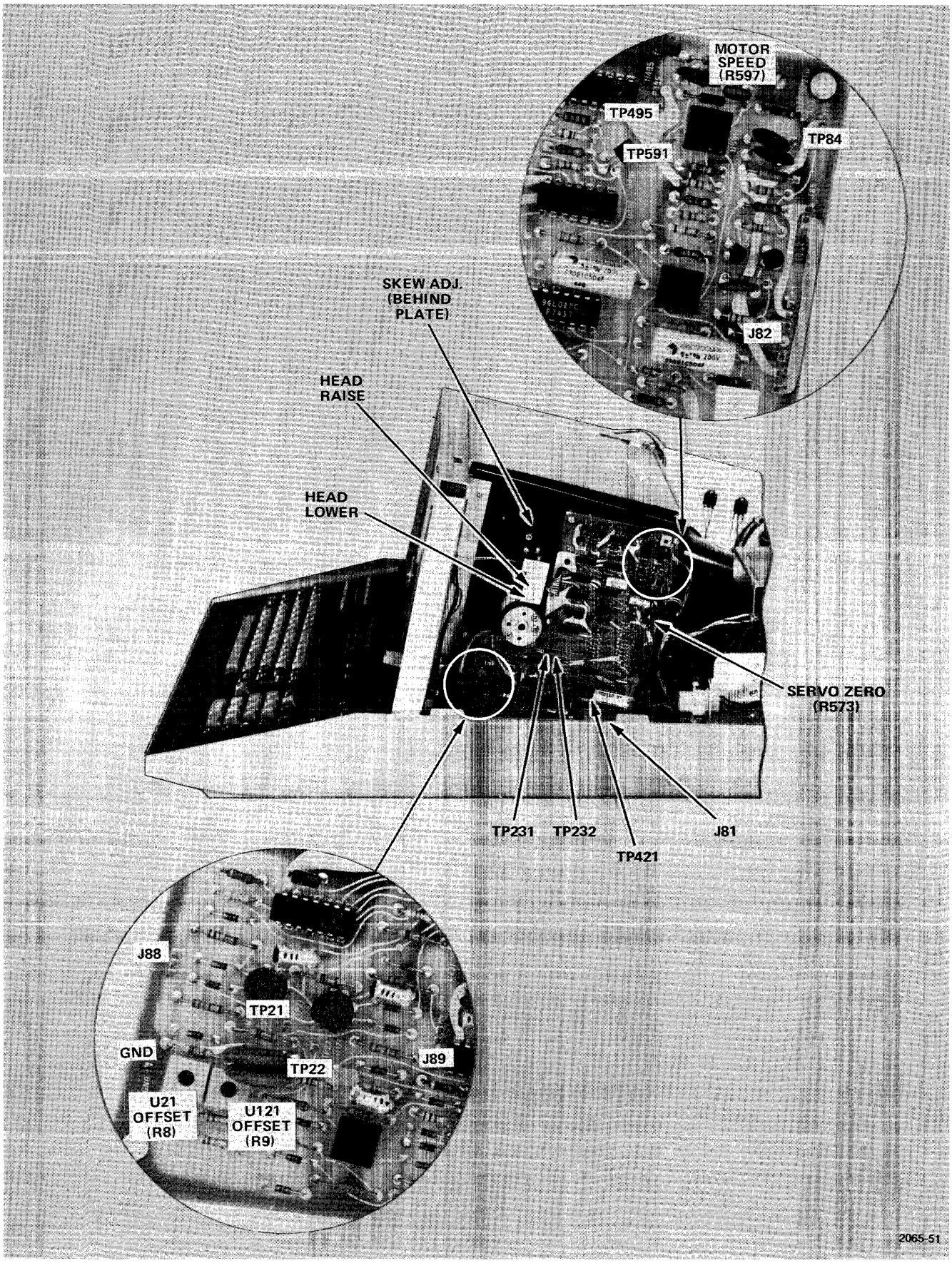


Fig. 4-7. Tape unit check points and adjustments.

If the tape should reach halfway (a burst pattern then appears on the oscilloscope) before completion of this step, the tape must be rewound and started again. Rewinding occurs automatically when the end of the tape is reached, or can be expedited by ejecting and then inserting the tape and pushing the "REWIND" button. To start the tape forward again, push "AUTOLOAD".

6. Head skew is also set during the *first* half of the calibration tape, and procedures for replaying this continuous 10 kHz segment are the same as previously described.

   As the tape is running at 30 ips, set the scope for 1 ns/cm, 2 V/cm, trigger on negative edge channel 1. Adjust skew with Allen wrench until the skew waveforms of Fig. 4-8 are aligned.

7. Turn off the power and swap connectors J88 and J89 that go to the tape head. Turn on the power and check to see if the skew pulses are still aligned. The differences in alignment between step 6 and step 7 are caused by electronically induced skew. If this induced skew is greater than 1 μs, replace the tape unit, otherwise adjust for half the skew difference (less than $\pm$500 ns).

8. Turn off power and restore J88 and J89 to their original locations. Skew adjustments and head height (right to left positioning) are interactive and both procedures may have to be performed several times.

9. Head height is set during the *second* half of the calibration tape, which contains alternate zones of 10 kHz and erased tape.

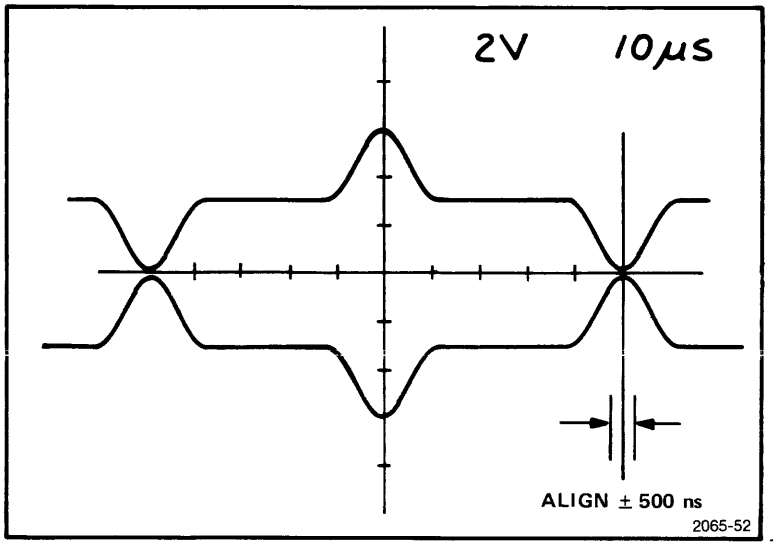


Fig. 4-8. Magnetic tape skew waveforms.

Move the scope probes: CH. 1 to TP21, remove CH. 2 (Fig. 4-7). Set the oscilloscope to 2 V/cm, 5 ms/cm and observe the burst pattern of Fig. 4-9.

Adjust delayed sweep if available on your oscilloscope to view the low-level region that follows the 10 kHz burst. (Set the delayed sweep rate to 100 ns/cm and the vertical sensitivity to 100 mV/cm.)

Loosen the head height raise screw about 3 turns (Fig. 4-7). Adjust the head lower screw for minimum amplitude during erased interval (Fig. 4-9).

It may be necessary to overcompensate height, as the height raise screw will, when tightened, affect the setting.

10. Height and skew are interactive adjustments, and 2 or 3 readjustments may be necessary before both are optimized. (Repeat steps 6 thru 9.)

11. When skew and height are optimized, and the height raise screw is tight, the calibration procedure is complete.

Routine maintenance procedures should now be followed, cleaning the head with isopropyl alcohol and a swab every 1000 hours of average 4051 use (or 6 hours of continuous tape operation).

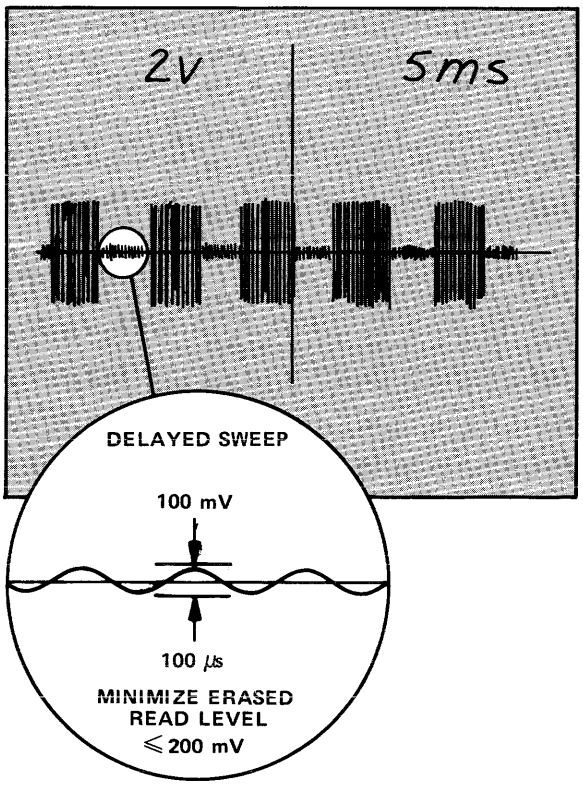


Fig. 4-9. Magnetic tape signal for tape head height (right-to-left position) adjustments.

Section 5

TROUBLESHOOTING AIDS

GENERAL

This section contains a short troublehsooting guide that is intended to lead a technician towards finding a faulty board or circuit assembly.

Adjustment locator aids are figures that are intended to help an experienced service technician readily locate a needed check point or adjustment. Detailed adjustment procedures are found in the calibration section of this manual.

This section also contains special tests that can be used to help isolate problem areas on the cpu board and optional memory boards. These tests require the System Test Fixture (part number 067-0746-00) that is designed to exercise Motorola 6800 microprocessors and system-related circuits. One of the standard tests contained in a programmable read only memory (PROM) within the text fixture performs a checksum validity test on the 4051 read only memory (ROM) devices. Another test verifies random access memory (RAM) data locations and then performs some pattern sensitivity analysis to help isolate transient memory-error conditions.

Two other tests use the System Test Fixture and also require a special connector board to check GPIB hardware and magnetic tape control hardware on the cpu board. This special connector board is given Tektronix part number 067-0790-00.

A brief description of System Test Fixture operations is also included to allow service personnel to construct their own specialized test procedures.

Motorola 6800 microcomputer system specifications have been reprinted by permission of Motorola Semiconductor, Inc. as an appendix in this manual for your convenience.

Figure 5-1 shows the test fixtures manufactured or provided by Tektronix, Inc. to help service 4051 Graphic Systems. The Calibration Tape is used to align the magnetic tape head of the 4051 tape drive and to adjust tape motor speed. The Display Alignment Graticule is used for precise display deflection alignment of the crt writing beam. Uses of the System Test Fixture and the Test Connector board are as previously described. The RS-232 Test Adapter is used by the Communication Backpack to verify the communication circuitry.

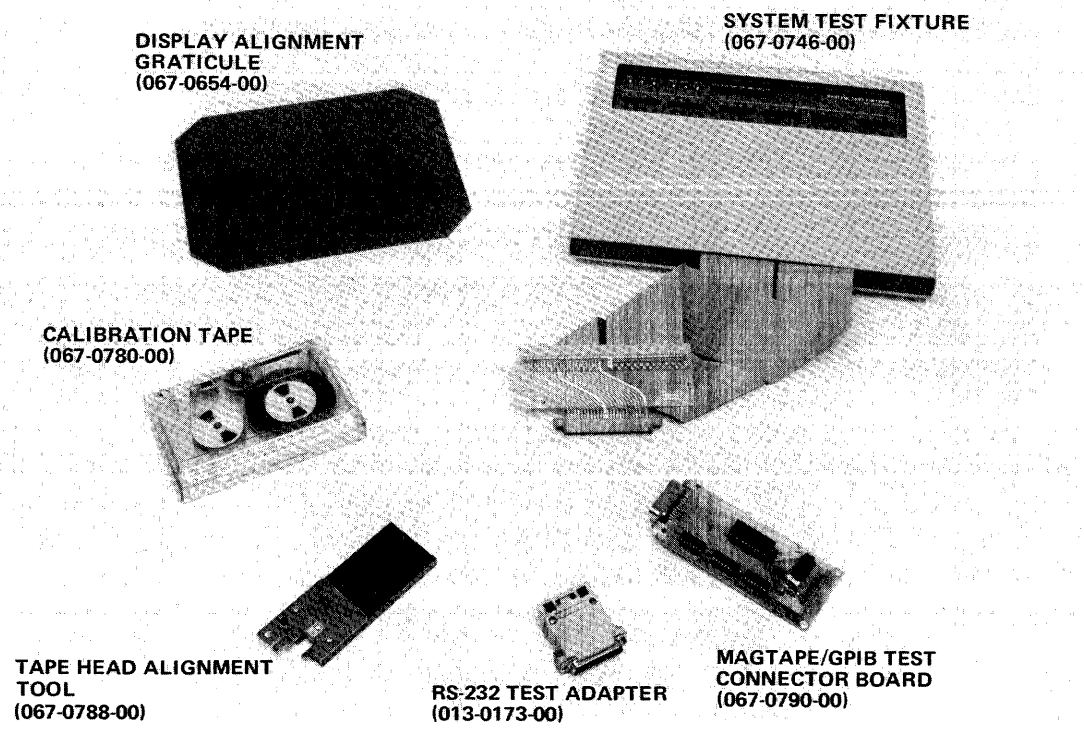


Fig. 5-1. Test fixtures for use with the 4051 Graphic System.

4051 TROUBLESHOOTING GUIDE

1. Check power cord, switch, fuse and line voltage setting. Be sure the indicator ring corresponds to the line voltage strapping within the instrument.

2. With a tape in the tape drive, turn on the power.
   a. The POWER light should turn on.
   b. The BUSY, I/O, and BREAK lights should be off.
   c. The fan should turn on.
   d. The tape should rewind and position at the load point.
   e. The alphanumeric cursor should appear in the upper-left corner of the screen.
   f. Peripherals on the GPIB should be initialized.
   g. After 90-120 seconds, the screen should become dim.

3. Absence of POWER light may be caused by:
   a. Burnt-out lamp.
   b. Blown line fuse.
   c. Absence of +12 volt supply.

4. The BUSY, I/O and BREAK lights being lit indicates a microprocessor system problem.
   a. Check the firmware and 6800 microprocessor.

5. Absence of fan motion may be caused by:
   a. Unplugged fan.
   b. Bad fan.
   c. Blown line fuse.
   d. Bad power transformer.

6. Absence of tape motion may be caused by:
   a. Bad power supplies.
   b. Bad tape motors.
   c. Bad tape status lamp (LOHOLE and UPHOLE).
   d. Bad status microswitch (LOAD SW).
   e. Bad tape control logic.
   f. Bad firmware.

7. Deformed cursor can be caused by:
   a. Bad display deflection circuitry.
   b. Maladjusted crt voltages.
   c. Bad logic feeding the D/A converters.
   d. Bad firmware.

8. Absence of cursor may be caused by:
   a. Maladjusted high voltage circuits.
   b. Bad deflection circuitry.
   c. Absence of microprocessor RESTART on the +5 volt supply.
   d. Bad digital-to-analog hardware.
   e. Bad firmware.

9. Inability to initialize GPIB peripherals may be due to:
   a. Bad +5 volt supply or RESTART signal.
   b. Bad microprocessor firmware.

10. Unable to witness VIEW/HOLD display functions can result from:
    a. Bad flood gun circuitry.
    b. Bad high voltage supplies.
    c. Bad Flood Gun Heater voltage and +150 volts anode voltage.
    d. Bad view control circuitry on the cpu board.

11. Press PAGE to erase the screen. Inability to erase the screen may be due to:
    a. Bad high voltage supplies.
    b. Bad erase control circuitry (display board storage circuits).
    c. Bad display control logic.
    d. Bad firmware.

12. Place the PLOT 50: SYSTEM SOFTWARE TAPE into the 4051 tape drive and press the AUTO LOAD key.

13. Failure to read the first tape file may be caused by:
    a. Bad tape or dirty tape head.
    b. Bad tape head alignment.
    c. Bad tape control circuitry (not properly adjusted).
    d. Bad power supplies.
    e. Bad firmware and system logic.
    f. Bad motor.

14. If the file read correctly, run the Software Verification program and the Firmware Verification program. Errors identified by these programs indicate system problems. The Firmware Verification program checks the usability of random access memory (RAM) in a 4051. A special test using the System Test Fixture is necessary to verify the firmware in read-only memory (ROM) devices. When replacing ROM, it is advisable to replace all devices required to update the system to the most recent firmware level. Replace a firmware version or level tag on the rear of the 4051 Graphic System if necessary.

15. If the 4051 power supplies are OK and nothing else works:
    a. Check the system cabling.
    b. Check for broken or heat-damaged components.
    c. Perform special system tests using the System Test Fixture.

16. Check the power supply usage chart to assist in isolating bad boards.

+320 volts	Display Board, Power Supply
+185 volts	Display Board, Power Supply
+175 volts	Display Board
+150 volts	Display Board
Flood Gun Heater	Display Board, Power Supply
+20 volts	Display Board, Tape Board, Power Supply
+15 volts	All except the backpacks and keyboard
+12 volts	CPU Board, Memory Board, Backpacks, ROM Packs, Power Supply
+5 volts	All boards
−5 volts	CPU Board, Memory Board
−11.5 volts	CPU Board
−12 volts	All boards except the keyboard, tape status and indicator lights
−20 volts	CPU Board, Tape Board, Power Supply

ADJUSTMENT LOCATOR AIDS

Figures 5-2 thru 5-7 are provided as a quick reference to all the major adjustment and check point locations in the 4051 Graphic System. If you are not familiar with these adjustments, please review the calibration procedures in the previous section. There are circuits having high voltages and dangerous currents that can be harmful if not handled with proper care. Disassembly procedures that necessitate the removal of circuit boards should be performed at a static-free work station to protect the high-impedance integrated circuits from electrostatic discharges. Disassembly procedures are documented in the maintenance section of this manual.

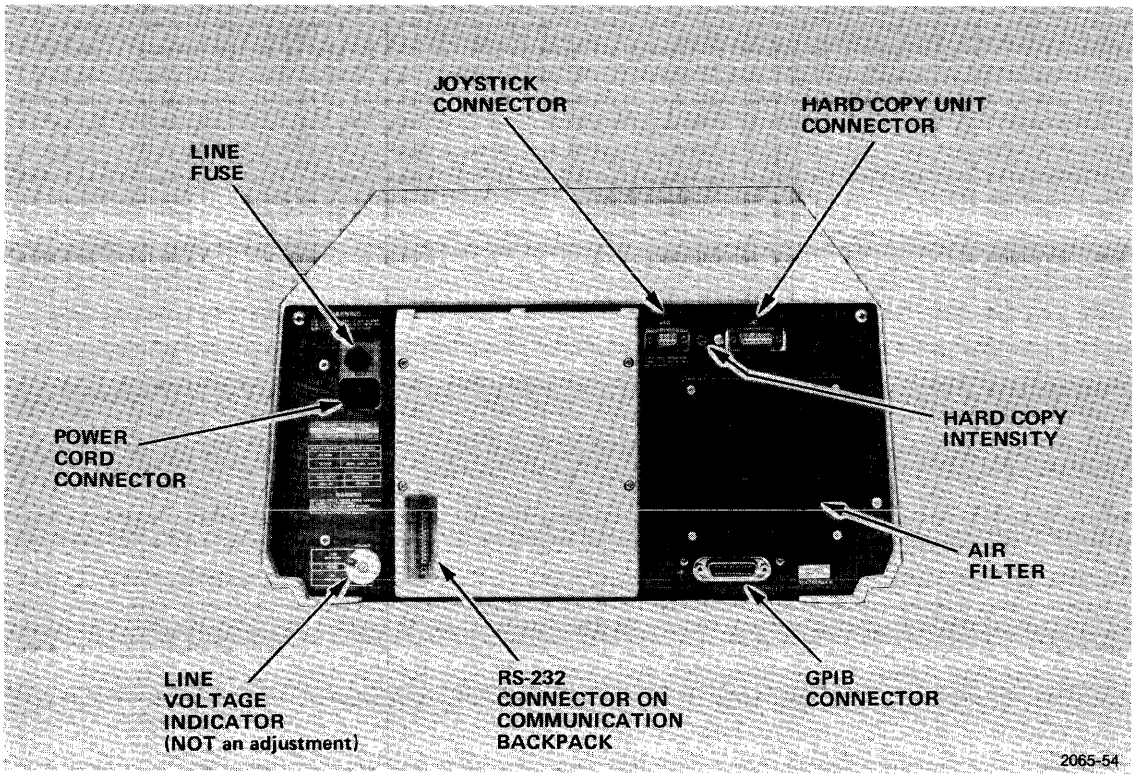


Fig. 5-2. Rear panel check points and connectors.

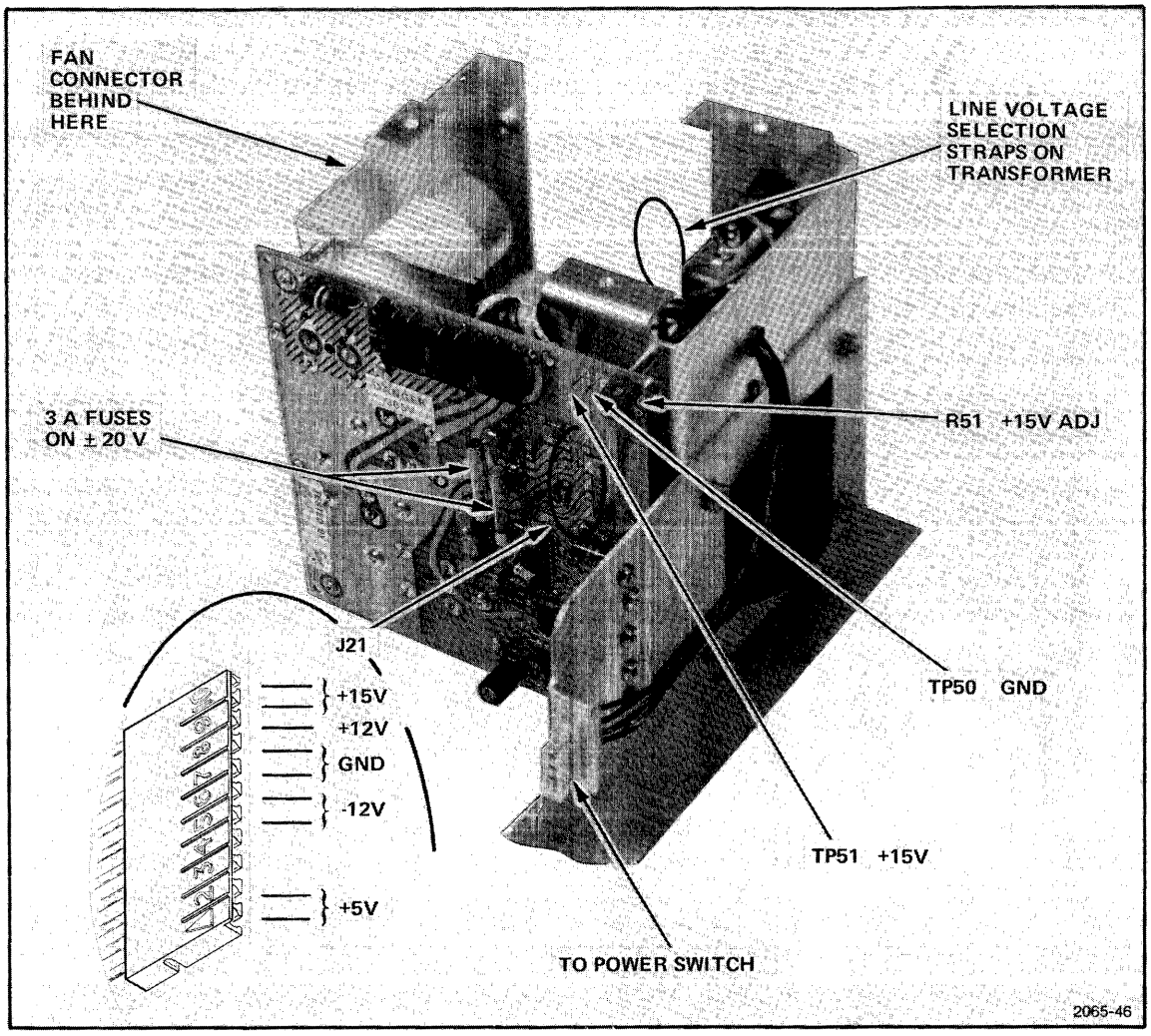


Fig. 5-3. Power supply check points and adjustments.

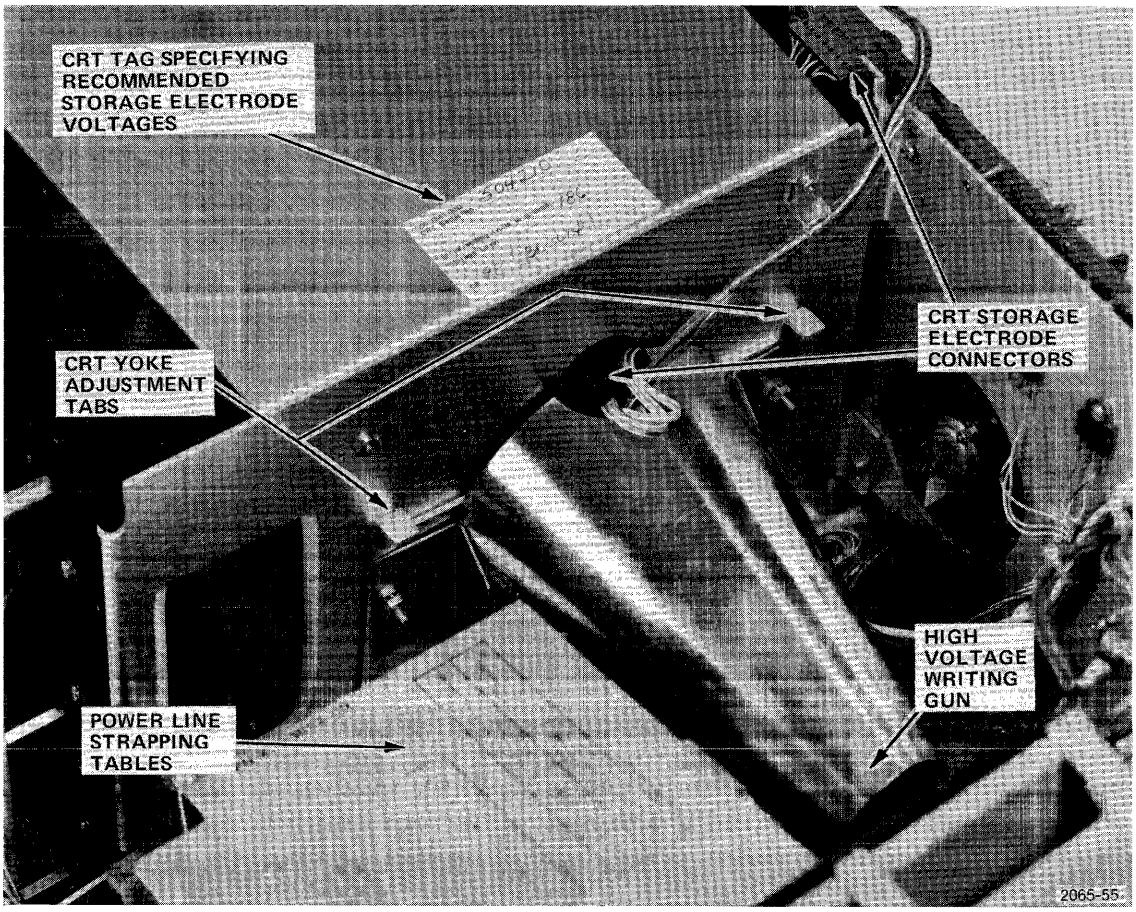


Fig. 5-4. CRT electrodes, yoke adjustment and power line strapping tables.

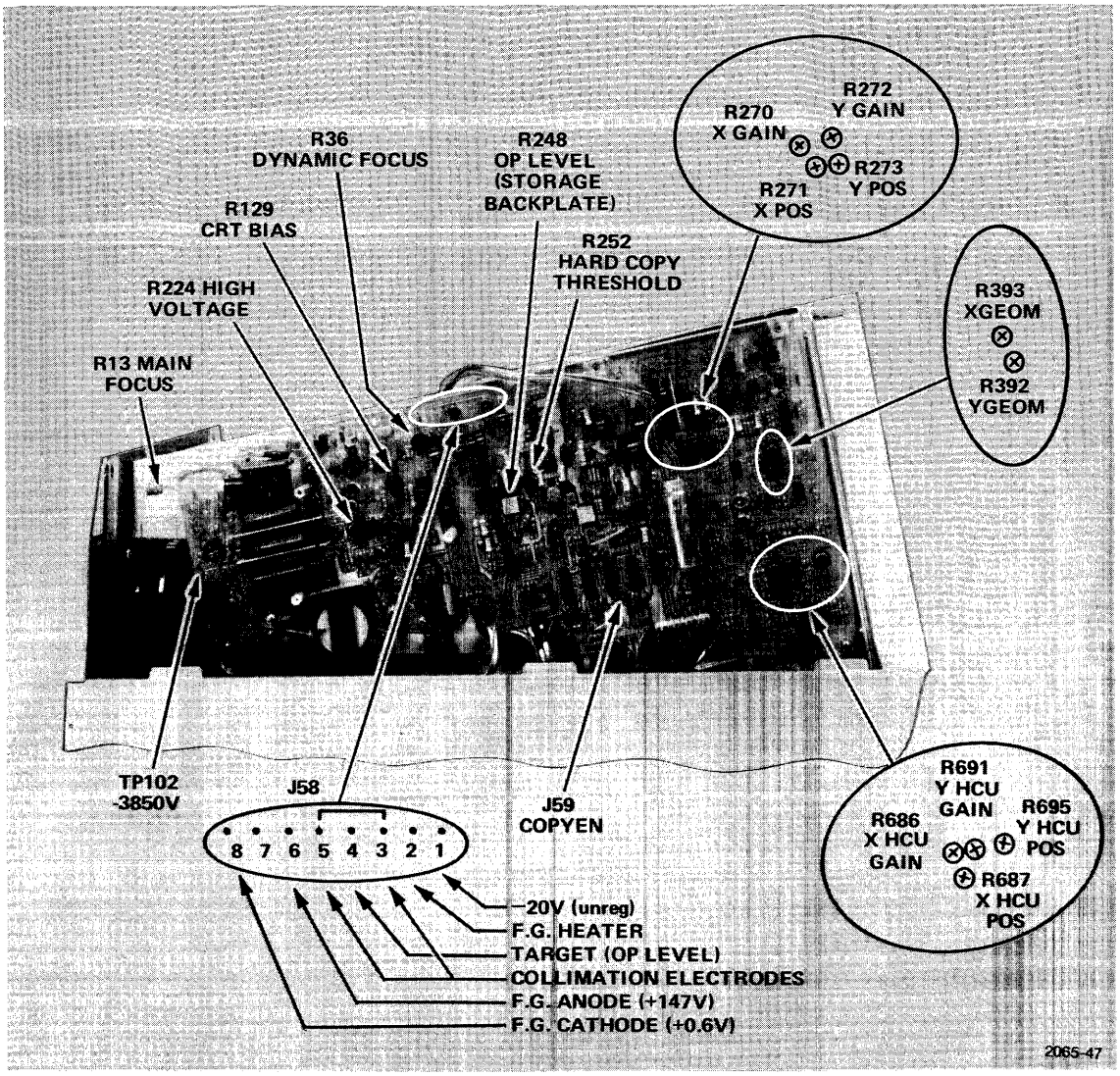


Fig. 5-5. Display board checkpoints and adjustments.

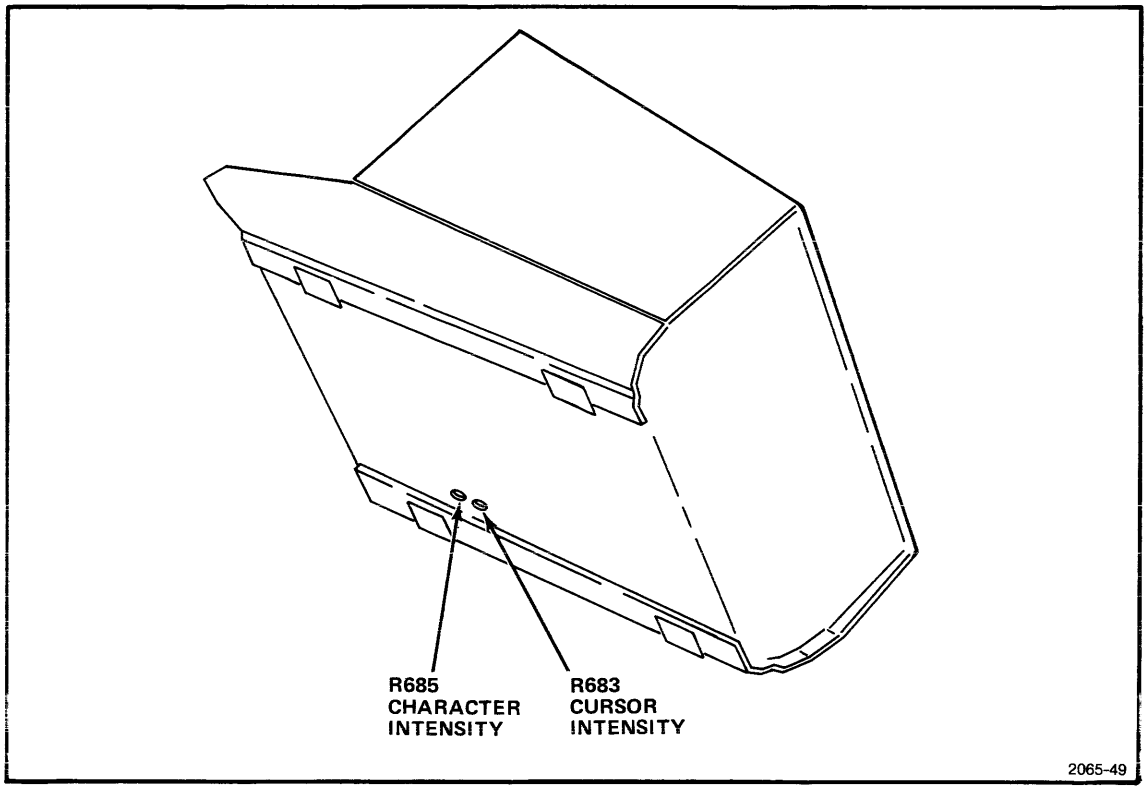


Fig. 5-6. Cursor and character intensity adjustments.

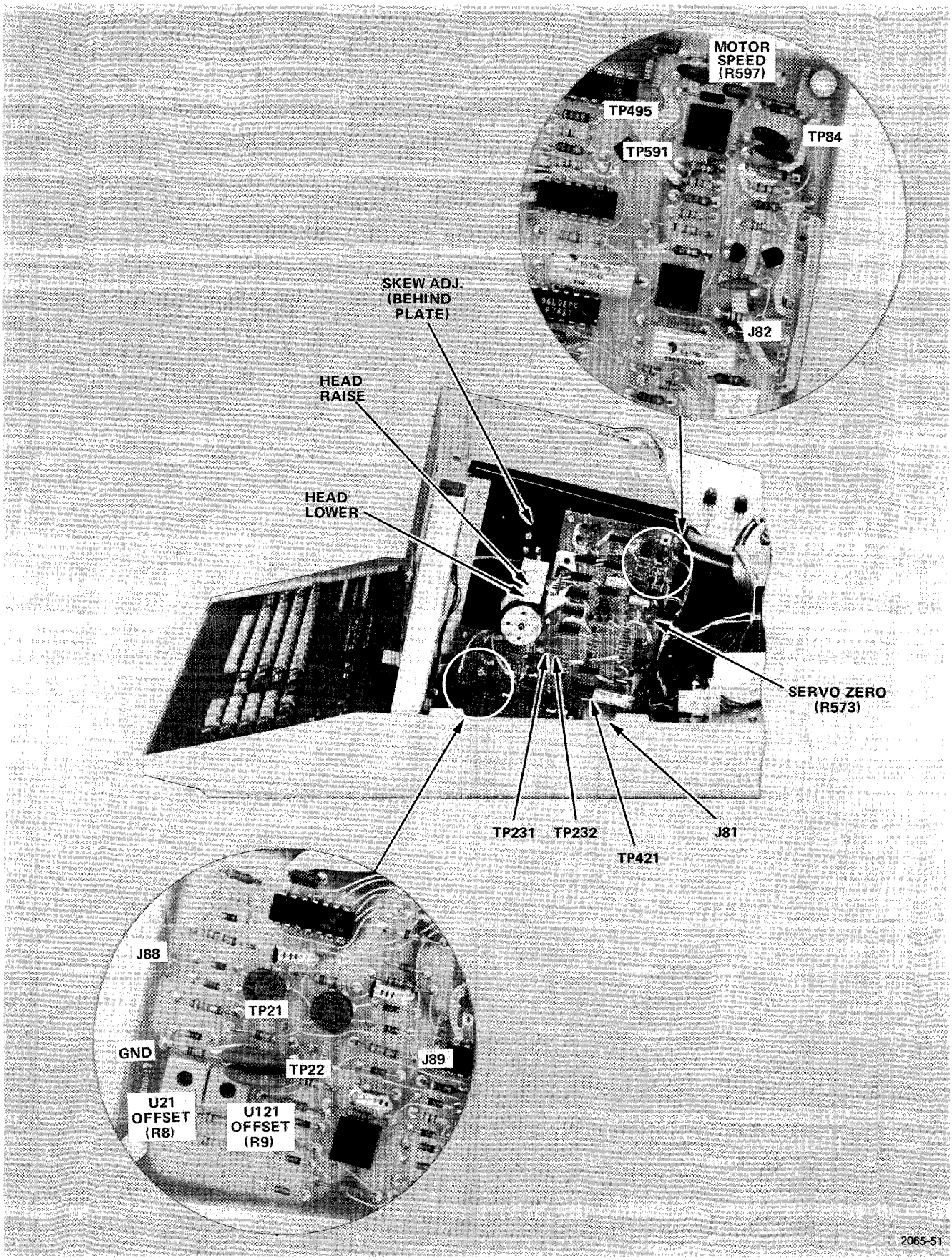


Fig. 5-7. Tape unit check points and adjustments.

SYSTEM TEST FIXTURE

The System Test Fixture (067-0746-00) is an instrument capable of exercising the Motorola 6800 bus in the 4051, and all devices (RAM, ROM, PIA, ACIA) connected to the bus within the 4051. Backpack circuitry cannot be exercised unless a special interconnect board is obtained. (This special board was not available when this manual was printed.)

The System Test Fixture connects to J5 at the rear of the 4051 cpu board. The fixture ribbon cable terminates in a 50-pin connector mounted on a fiber-glass circuit board. The side of this board marked "A" must correspond to the non-component side of the 4051 cpu board. When the fixture is used with the cpu board inside the 4051, the "A" side should face up. When the fixture is used on a CPU board brought outside the 4051, then cpu components will face up (Fig. 5-8); consequently, the test fixture connector "A" side will face down.

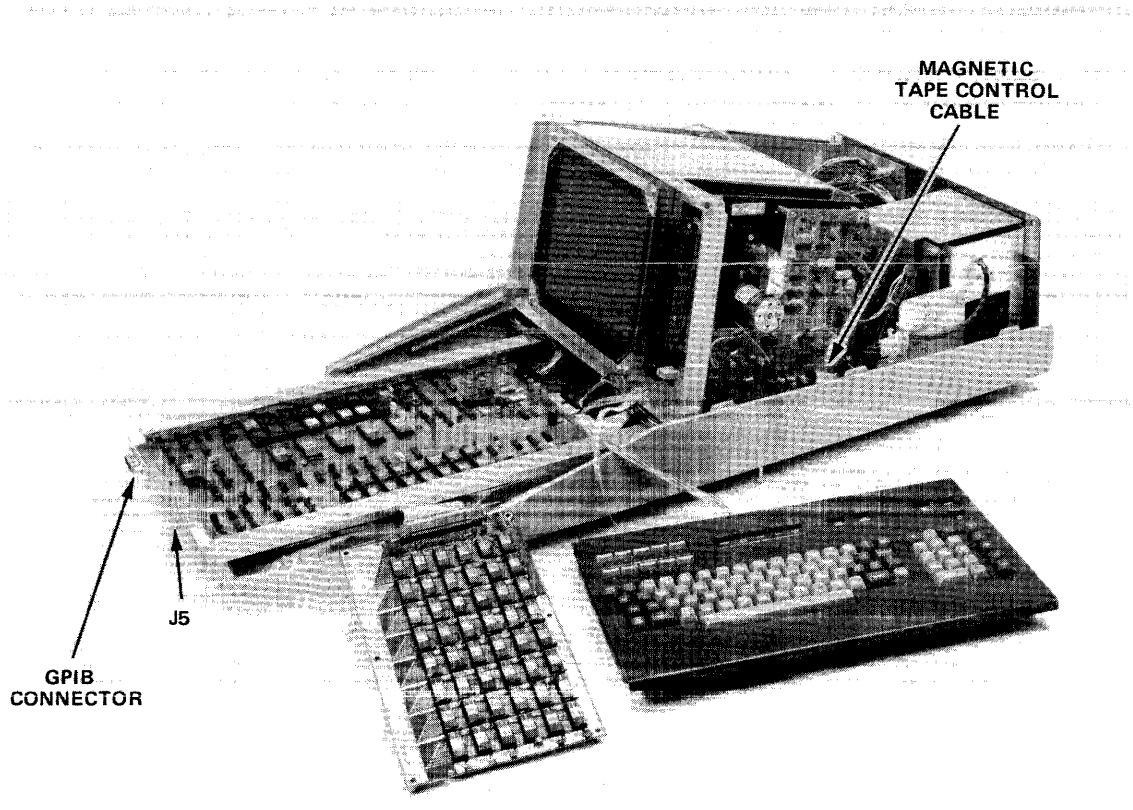


Fig. 5-8. 4051 cpu board and memory board brought outside the system for component servicing.

4051 TESTS USING THE SYSTEM TEST FIXTURE

There are five tests coded into programmable read-only memory located in the System Test Fixture. These are 1) a RAM test, 2) a ROM test, 3) a GPIB circuit test, 4) a display test, 5) a tape control circuitry test. Table 5-1 is a conversion between binary notation and hexadecimal notation. The lights (LEDs) on the System Test Fixture present information in binary format while the following test procedures specify the required binary data in hexadecimal notation.

Table 5-1

HEXADECIMAL-TO-BINARY	
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

SYSTEM TEST FIXTURE SWITCH FUNCTIONS

16 Address Switches — These switches provide key entry of memory address locations. (UP=1, DOWN=0). The switches are in groups of four (AB15-AB0, left to right) for hexadecimal address entry (binary equivalent).

8 Data Switches — These switches provide key entry of data. (UP=1, DOWN=0). The switches are in two groups of four to facilitate hexadecimal data entry. (DB7-DB0, left to right).

STOP — Pressing this switch will drop the GO/HALT line to the 6800 microprocessor. The ABA LED should turn on to indicate that the microprocessor (MPU) has stopped and that the address bus is available for test fixture use.

START — Pressing this switch will release the GO/HALT line and allow the MPU to begin executing coded instructions.

STEP	Each time this switch is pressed, the GO/HALT line is pulsed to allow the MPU to execute a single instruction. One instruction may occupy one, two or three bytes of memory.
ABA LED	The Address Bus Available LED will be on each time the MPU is halted or is in a wait state.
EXAMINE	Pressing this switch, when the processor is halted, will cause the data residing at the memory address location specified by the Address Switches to be displayed on the Data LEDs.
DEPOSIT	Pressing this switch, when the processor is halted, will cause the data specified by the Data Switches to be loaded into the memory location specified by the Address Switches.
RESTART	Pressing this switch will drop the RESET line to the MPU and cause it to perform a vectored restart operation. The MPU restart vector resides in memory locations FFFE-FFFF.
LATCH DATA	When this switch is up and the MPU addresses the memory location specified by the Address Switches, the data written to or read from that memory location will be displayed on the Data LEDs.
LATCH ADDR	When this switch is up and the MPU writes data specified by the Data Switches into any memory location the address of that memory location into which data was written will be displayed on the Address LEDs.
FIXTURE PROM	When this switch is up, firmware code located in programmable read-only memory (PROM) devices in the System Test Fixture can be addressed. The RBC line is dropped to disable ROM in the 4051 that shares the same memory addresses.
FIXTURE RAM	When this switch is up, 32 bytes of RAM in the System Test Fixture are switched to occupy memory addresses FFE0-FFFF. This enables selected interrupt vecotrs and restart vectors to be keyed or generated by the System Test Fixture.
DATA BREAK	When this switch is up and the MPU writes data specified by the Data Switches, the GO/HALT line will drop allowing the MPU to execute only one more instruction.
ADDR BREAK	When this switch is up and the MPU addresses the location specified by the Address Switches, the GO/HALT line will drop. The MPU will generally execute one more instruction unless the address is that of the instruction being executed, at which time the MPU will usually halt at the end of the current instruction.

INSTR CYCLE

When this switch is up, the OP CODE of the instruction being executed will be latched into the Data LEDs if the LATCH DATA switch is down; the address of the OP CODE will be latched into the Address LEDs if the LATCH ADDR switch is down.

When this switch is down, the last byte of the instruction being executed will be latched into the Data LEDs if the LATCH DATA switch is down; the address of the last instruction byte will be latched into the Address LEDs if the LATCH ADDR switch is down.

4051 RAM Test

1. Power down the 4051.
2. Attach the System Test Fixture to J5 (Fig. 5-8).
3. Power up the 4051.
4. Set the seven control switches to the positions indicated in Fig. 5-9.
5. Data is loaded into a memory location by keying the memory address into the Address switches and the data into the Data switches. Pressing the DEPOSIT switch transfers the data to the memory register indicated by the Address switches. Pressing the EXAMINE switch causes data appearing in the register indicated by the Address switches to be displayed on the Data LEDs.

   Load 90 into address register FFFE (Fig. 5-10).

   Load 00 into address register FFFF (Fig. 5-11).

   This causes the starting address for the test routine to be loaded into the processor's restart vector address.

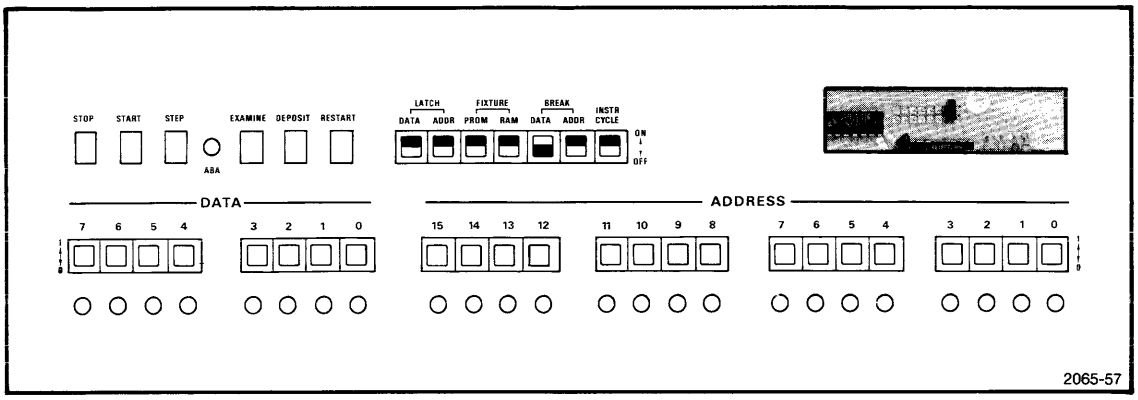


Fig. 5-9.

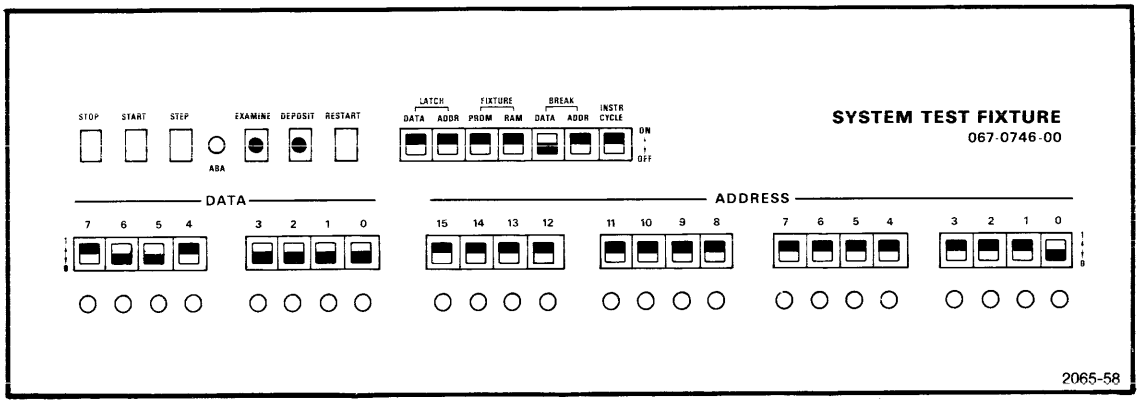


Fig. 5-10.

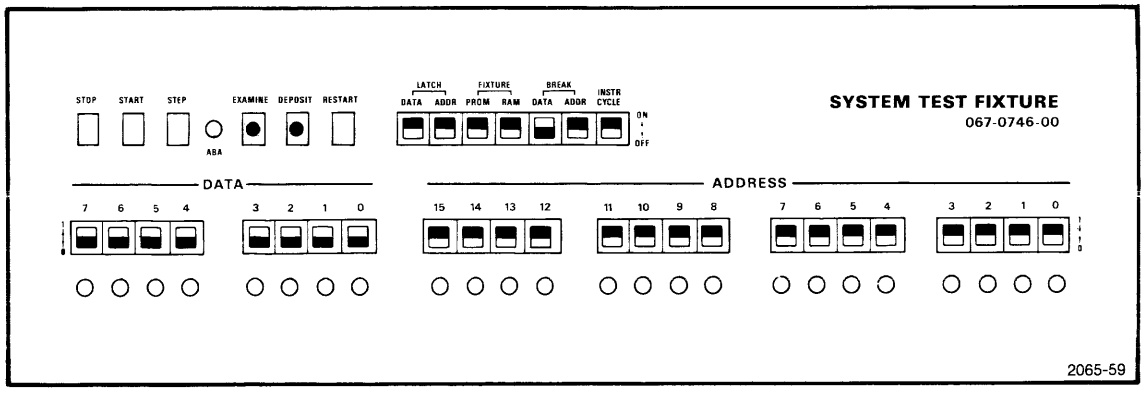


Fig. 5-11.

6. Place 00 into the Data switches and FFFD into the Address switches. Press RESTART and then START to begin program execution (Fig. 5-12).

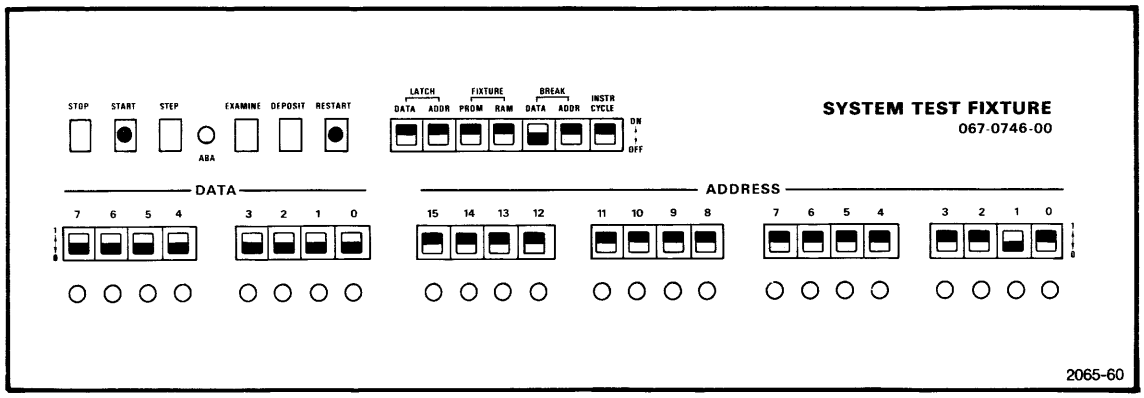


Fig. 5-12.

7. When the program stops, the ABA LED turns on and the Address LEDs will either indicate a bad memory location or the maximum amount of RAM in the 4051. See Table 5-2. The Data LEDs indicate the bad bit(s) in the data byte addressed. Refer also to Figures 5-13 and 5-14 for memory chip locations referenced by memory address and data bit.

Table 5-2

SIZE OF 4051 SYSTEMS

8K of RAM	Address LEDs indicate 2000
16K of RAM	Address LEDs indicate 4000
24K of RAM	Address LEDs indicate 6000
32K of RAM	Address LEDs indicate 8000

8. If the address of step 7 is correct, press START twice to start the test procedures that perform pattern sensitivity analysis. An 8K machine takes the least time and a 32K machine will take the most, almost 2 hours.

   If the test runs to completion without error, the ABA LED will be on, the Data LEDS will all be on, and the Address LEDs will show FFFC.

9. If an error is detected, ABA LED will be on, the Address LEDs will show the bad address and the Data LEDs will show the bad bit(s) by turning on the LEDs corresponding to the bad bits. Refer to Figures 5-13 and 5-14 for locating memory chips.

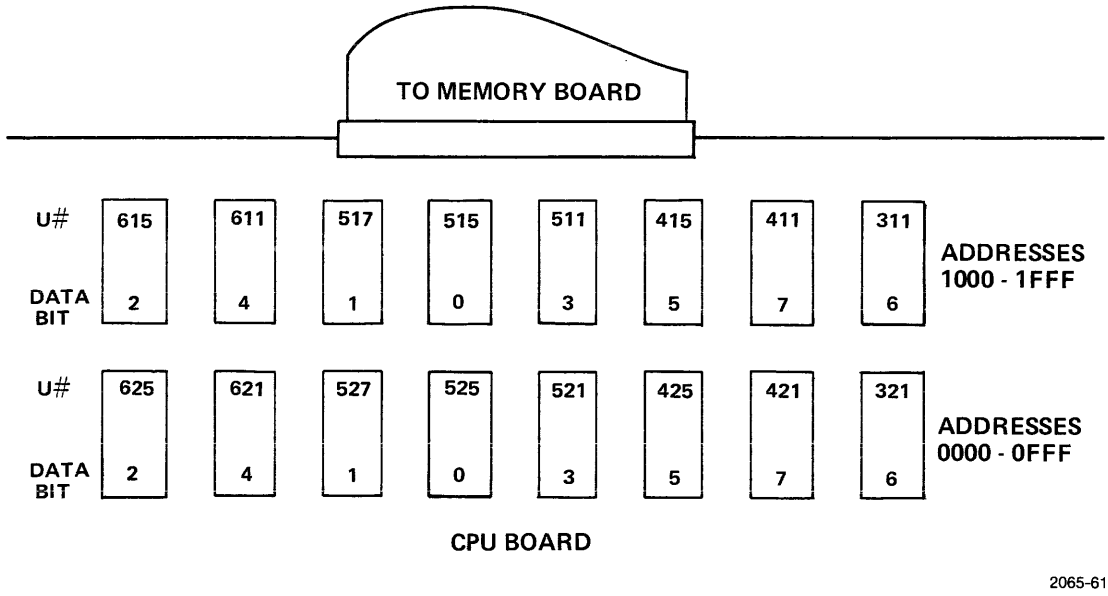


Fig. 5-13. Random access memory (RAM) layout for the cpu board.

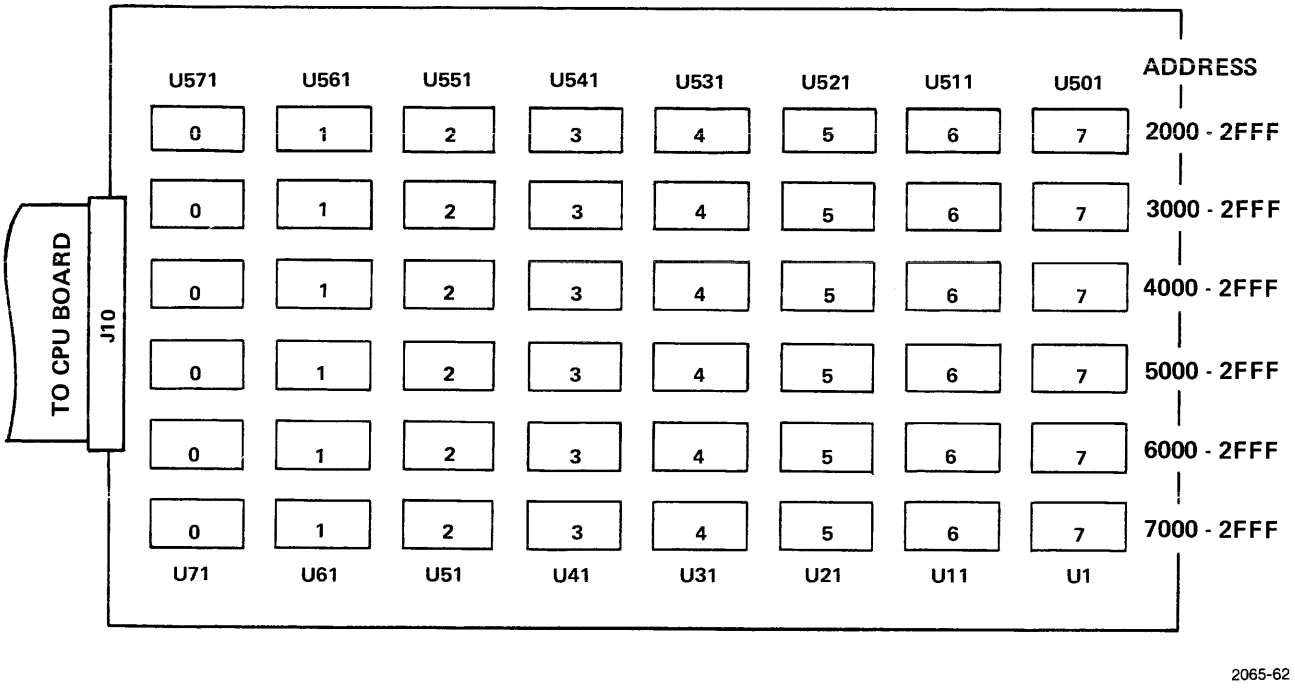


Fig. 5-14. Random access memory (RAM) layout for the memory board.

4051 ROM Test

1. Power down the 4051.

2. Attach the System Test Fixture to J5 (Fig. 5-8).

3. Power up the 4051.

4. Set the seven control switches to the positions indicated in Fig. 5-9.

5. Data is loaded into a memory location by keying the memory address into the Address switches and the data into the Data switches. Pressing the DEPOSIT switch transfers the data to the memory register indicated by the Address switches. Pressing the EXAMINE switch causes data appearing in the register indicated by the Address switches to be displayed in the Data LEDs.

   Load 91 into address register FFFE (Fig. 5-15).

   Load 00 into address register FFFF (Fig. 5-16).

6. Place 00 into the Data switches and FFFD into the Address switches.

   Press RESTART and then START to begin program execution (Fig. 5-17). This program segment causes the next program segment to be executed to be transferred into RAM. After the transfer is complete, the microprocessor stops with the ABA LED turned on.

7. Change the Address switches to 00FD (Fig. 5-18).

   Turn off the PROM and RAM switches.

   Press START.

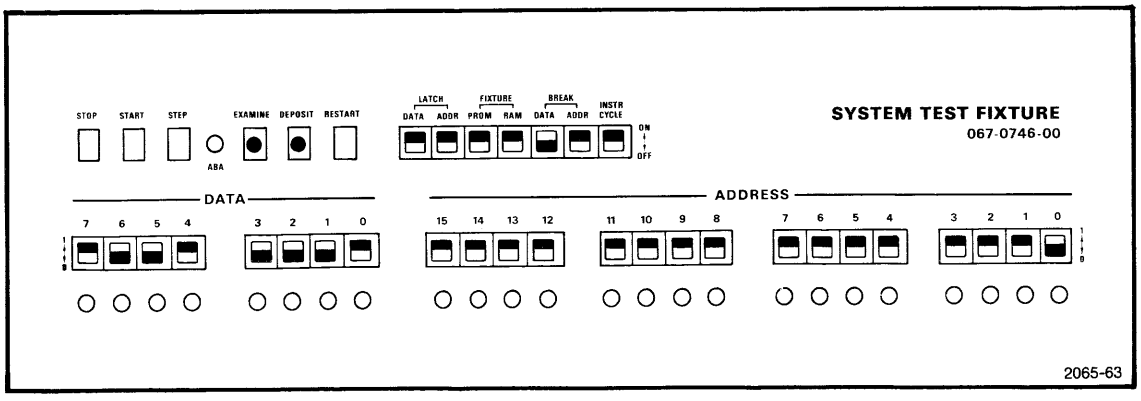


Fig. 5-15.

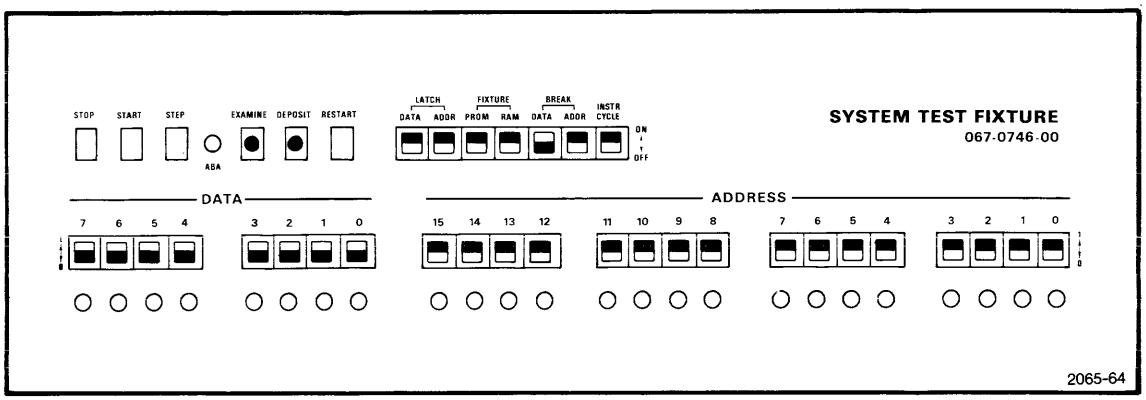


Fig. 5-16.

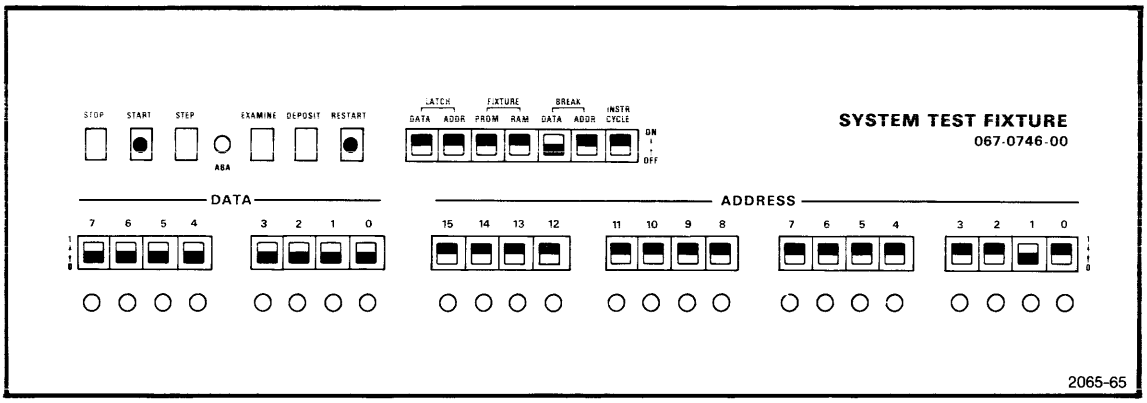


Fig. 5-17.

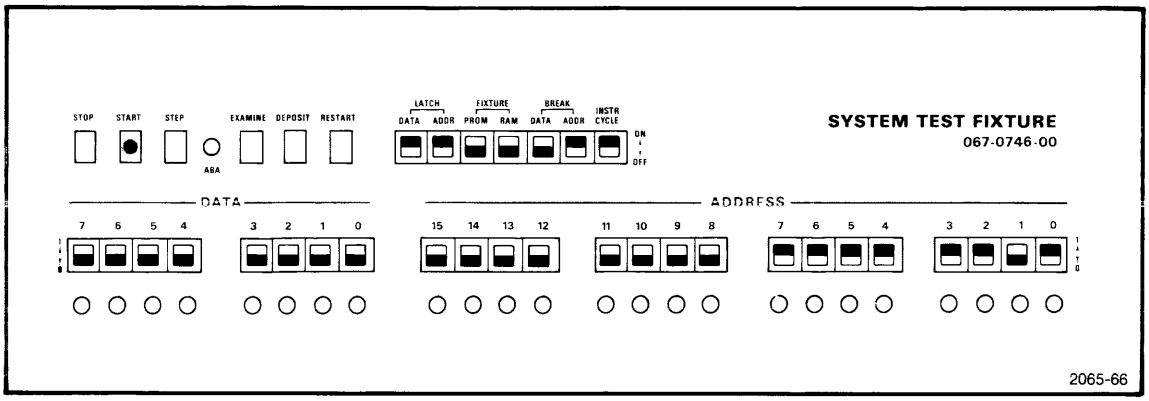


Fig. 5-18.

8. The Address LEDs now show the address of the ROM being tested and the Data LEDs show the computed checksum. Compare this checksum against the list of correct checksums for the version of 4051 firmware being tested. These checksums are found in Table 5-3.

9. Press START to continue the test to the next ROM address. Cycle through steps 8 and 9 until all ROM devices have been checked.

10. To check backpack ROM devices, remove the ROM chips from the backpack and substitute them for ROMs on the cpu board and repeat steps 1 thru 9. Substitute the checksums in tables 5-4 and 5-5 for the ROM locations replaced. DO NOT REPLACE U585 ON THE CPU BOARD FOR THIS TEST. The numbers in parentheses are part number suffix indicators.

Table 5-3

4051 FIRMWARE CHECKSUMS

Part Number	Circuit Number	Starting Address	Version 1	Version 2	Version 3	Version 4	Version 5
156-0659-XX	U585	8000	FF(-01)	7D(-02)	7D(-02)	7D(-02)	7D(-02)
156-0660-XX	U581	8800	E0(-01)	E0(-01)	E0(-01)	E0(-01)	E0(-01)
156-0661-XX	U487	9000	5B(-01)	5B(-01)	5B(-01)	5B(-01)	5B(-01)
156-0662-XX	U485	9800	1C(-01)	1C(-01)	1C(-01)	1C(-01)	1C(-01)
156-0663-XX	U481	A000	8A(-01)	8A(-01)	8A(-01)	8A(-01)	8A(-01)
156-0664-XX	U385	A800	AF(-01)	53(-02)	53(-02)	53(-02)	53(-02)
156-0665-XX	U381	B000	B2(-01)	B2(-02)	B2(-02)	B2(-02)	B2(-02)
156-0666-XX	U285	B800	4D(-01)	4D(-01)	4D(-01)	4D(-01)	4D(-01)
156-0667-XX	U595	C000	BE(-01)	BE(-02)	BE(-02)	BE(-02)	BE(-02)
156-0668-XX	U591	C800	42(-01)	42(-01)	42(-02)	42(-02)	42(-01)
156-0669-XX	U497	D000	E2(-01)	E2(-01)	E2(-01)	E2(-01)	E2(-01)
156-0670-XX	U495	D800	F4(-01)	F4(-01)	F4(-01)	F4(-01)	F4(-01)
156-0671-XX	U491	E000	E2(-01)	E2(-02)	E2(-02)	E2(-02)	E2(-02)
156-0672-XX	U395	E800	59(-01)	59(-01)	AD(-02)	AD(-02)	AD(-02)
156-0673-XX	U391	F000	10(-01)	CE(-02)	CE(-02)	CE(-03)	CE(-03)
156-0674-XX	U295	F800	F4(-01)	F4(-02)	F4(-02)	F4(-02)	F4(-02)

Table 5-4

CHECKSUMS FOR BACKPACK ROMS

Firmware/Communications (Overflow ROMS)	Version 1	Version 2
U101/U1 (156-0747-XX)		EA(-01)
U201/U11 (156-0748-XX)		38(-01)

Table 5-5

COMMUNICATION BACKPACK
(Communication ROMS)

Overflow ROMS	Version 1	Version 2
U101 (156-0712-XX)	29(-00)	29(-01)
U111 (156-0713-XX)	43(-00)	93(-01)
U121 (156-0714-XX)	80(-00)	C1(-01)
U131 (156-0715-XX)	EA(-01)	EA(-01)

4051 GPIB Test

1. Power down the 4051.

2. Attach the System Test Fixture to J5 (Fig. 5-8). Attach the test connector board (067-0790-00) to the GPIB connector on the 4051. Place a jumper between any +5 volt power source on the 4051 and the +5 volt pin on the test connector board.

3. Power up the 4051.

4. Set the seven control switches to the positions indicated in Fig. 5-19.

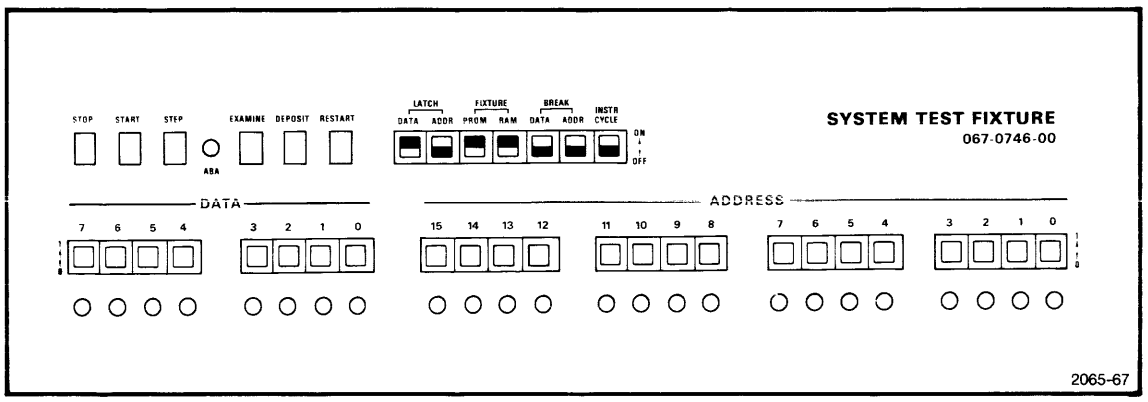


Fig. 5-19.

5. Data is loaded into a memory location by keying the memory address into the Address switches and the data into the Data switches. Pressing the DEPOSIT switch transfers the data into the memory register indicated by the Address switches. Pressing the EXAMINE switch causes data appearing in the register indicated by the Address switches to be displayed on the Data LEDs.

   Load 92 into address register FFFE (Fig. 5-20).

   Load 00 into address register FFFF (Fig. 5-21).

6. Place 00 into the Data switches and FFFD into the Address switches.

   Press RESTART and then START to begin program execution (Fig. 5-22).

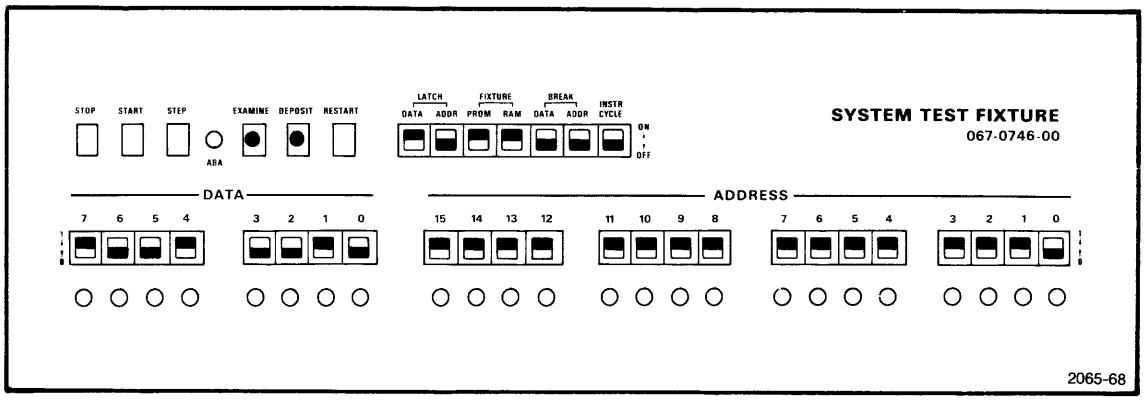


Fig. 5-20.

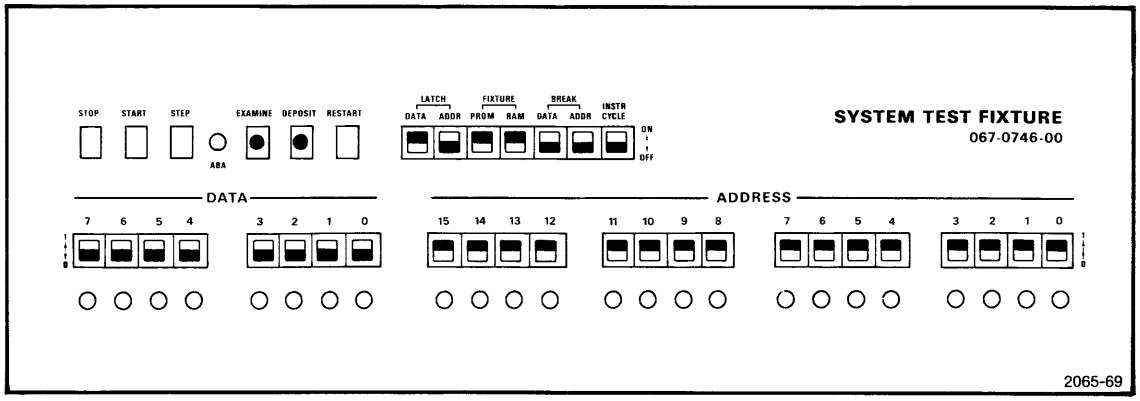


Fig. 5-21.

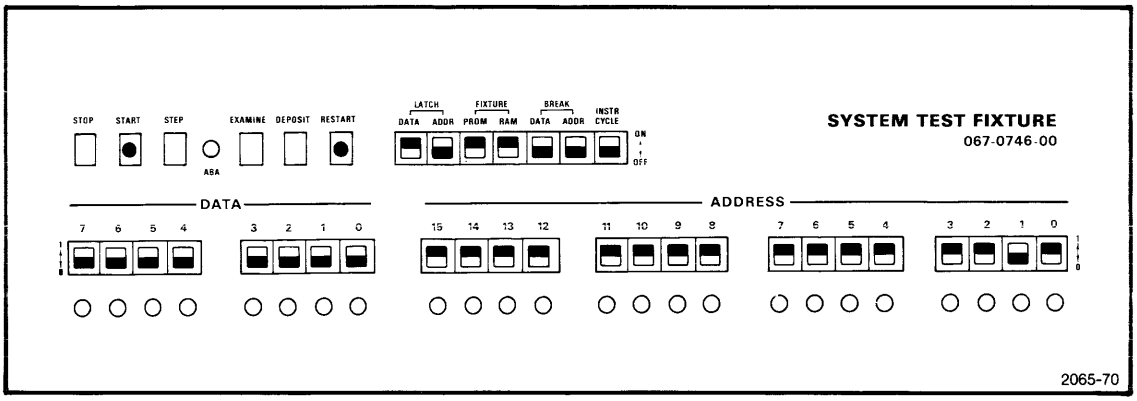


Fig. 5-22.

7. If all four tests in this program are passed, 80 is displayed in the Data LEDs. Otherwise the output should correspond to one of the following error codes.

The error codes are in hexadecimal notation as they appear on the Data LEDs. The GPIB test procedure performs a sequence of three tests.

Test A:

When one of the following error codes is displayed, check TALK=Hi (U265-pin 19) U281-pin 13,NTALK=Lo at U193-pin 14 and DAV (out)=Lo (U265-pin 39)

ER1: (EO1-SRQ) Check (U265-pin10, (U191-pin2), (U265-pin15), (U461-pin14)
ER2: (IFC-NRFD) Check (U265-pin11), (U191-pin7), (U265-pin14)
ER3: (REN-DAV) Check (U265-Pin12), (U191-pin15), (U265-pin16), or
Check U461-pin17 (BUSY-REN), (U121-pin1), (U191-pin15), (U265-pin16)
ER4: (ATN-NDAC) (U265-pin13), (U191-pin9), (U265-pin17)
ER5: (EOI-FLAG) Check (U191-pin3), (U265-pin40)
ER6: (SRQ-FLAG) Check (U91-pin3), (U165-pin18)

After the error code is displayed on the Data LEDs, pulses appear at the test points for each error code.

Test B:

This test examines NDAC, NRFD, and DAV as output by reading DIO1-DIO3. If one of the following errors is indicated check TALK=Lo at U281-pin 13 and U281-pin14, NTALK=Hi at U193-pin4, and U265-pin10=Hi.

ER7: (NDAC problem as output) Check (U265-pin17), (U193-pin10), (U91-pin9), (U181-pin3), (U265-pin2)
ER8: (NRFD problem as output) Check (U265-pin14), (U193-pin13), (U91-pin7), (U181-pin14), (U183-pin7), (U265-pin4)
ER9: (DAV problem as output) Check (U265-pin39), (U91-pin15), (U181-pin6), (U183-pin5), (U265-pin1)

After the error code is displayed, pulses appear at the test points for each error code.

Test C:

This is a data test for DIO1-DIO8.

If an error is displayed, check for a TALK pulse at (U265-pin19) and (U265-pin10).

ER10: (DIO1 problem) Check (U265-pin2), (U181-pin2) for TALK mode. Also check (U181-pin2), (U183-pin2), (U183-pin3), (U265-pin2) for LISTEN mode.
ER11: (DIO2 problem) Check (U265-pin3), (U181-pin7) for TALK mode. Also check (U181-pin7), (U183-pin4), (U183-pin5), (U265-pin3) for LISTEN mode.
ER12: (DIO3 problem) Check (U265-pin4), (U181-pin15) for TALK mode. Also check (U181-pin15), (U183-pin6), (U183-pin7), (U265-pin4) for LISTEN mode.
ER13: (DIO4 problem) Check (U265-pin5), (U181-pin9) for TALK mode. Also check (U181-pin9), (U183-pin10), (U183-pin9), (U265-pin5) for LISTEN mode.
ER14: (DIO5 problem) Check (U265-pin6), (U81-pin2) for TALK mode. Also check (U81-pin2), (U281-pin2), (U281-pin3), (U265-pin6) for LISTEN mode.

After the error code is displayed, pulses appear at the test points for each error code.

4051 Display Test

1. Power down the 4051.

2. Attach the System Test Fixture to J5 (Fig. 5-8).

3. Power up the 4051.

4. Set the seven control switches to the positions indicated in Fig. 5-23.

5. Data is loaded into a memory location by keying the memory address into the Address switches and the data into the Data switches. Pressing the DEPOSIT switch transfers the data into the memory register indicated by the Address switches. Pressing the EXAMINE switch causes data appearing in the register indicated by the Address switches to be displayed on the DATA LEDs.

   Load 93 into address register FFFE (Fig. 5-24).

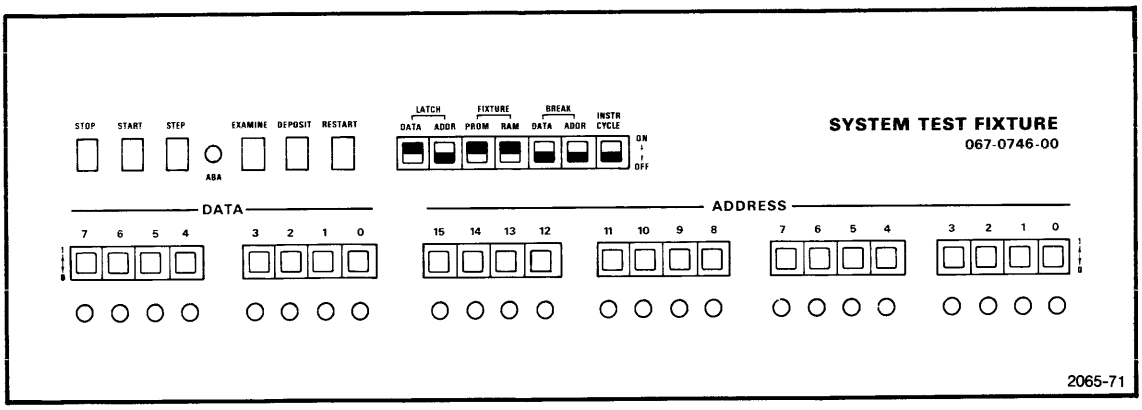


Fig. 5-23.

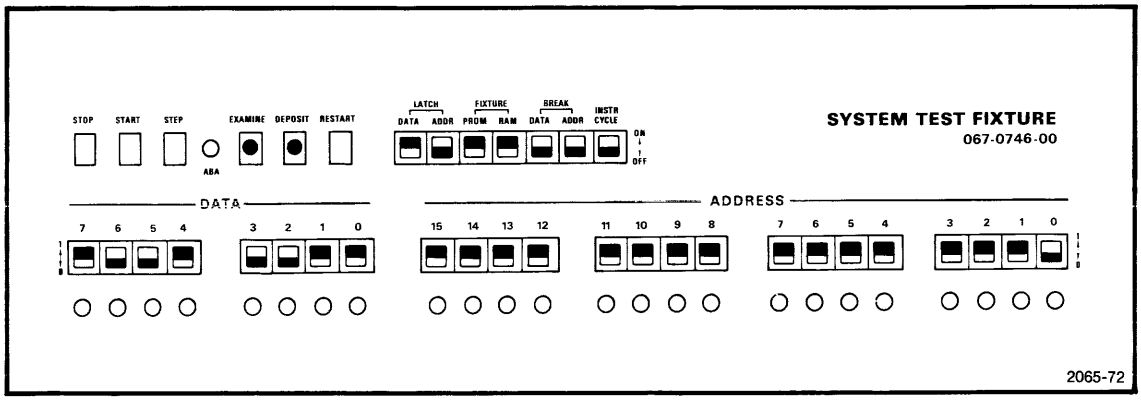


Fig. 5-24.

Load 00 into address register FFFF (Fig. 5-25).

6. Place 00 into the Data switches and FFFD into the Address Switches.

   Press RESTART and then START to begin program execution (Fig. 5-26).

   This program causes vectors to be continually drawn to the extremes of X axis and Y axis deflection. Output from the deflection amplifiers for each axis is approximately ±8.0 volts at the cpu board. The result is a bright 45° line going from bottom-left to upper-right of the display. (Don't worry if both directions of vector drawing do not close for the deflection magnitude may be well out of the linear range of display deflection parameters.)

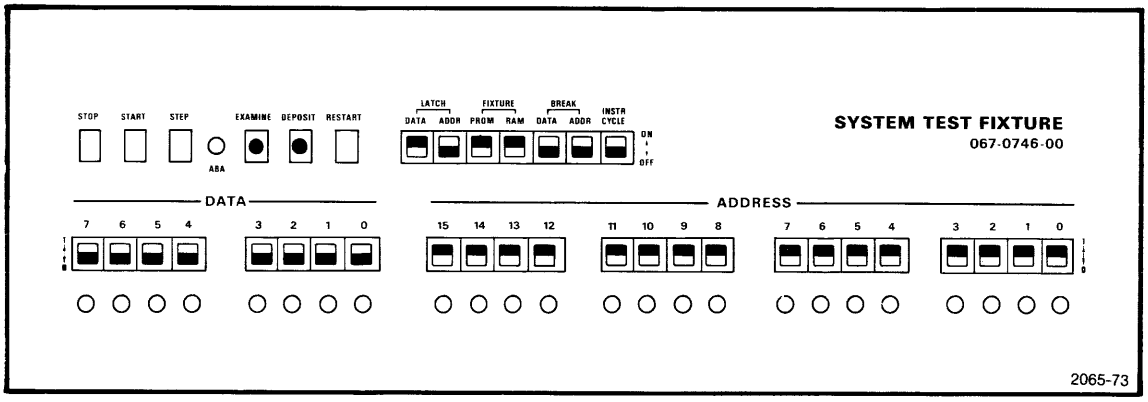


Fig. 5-25.

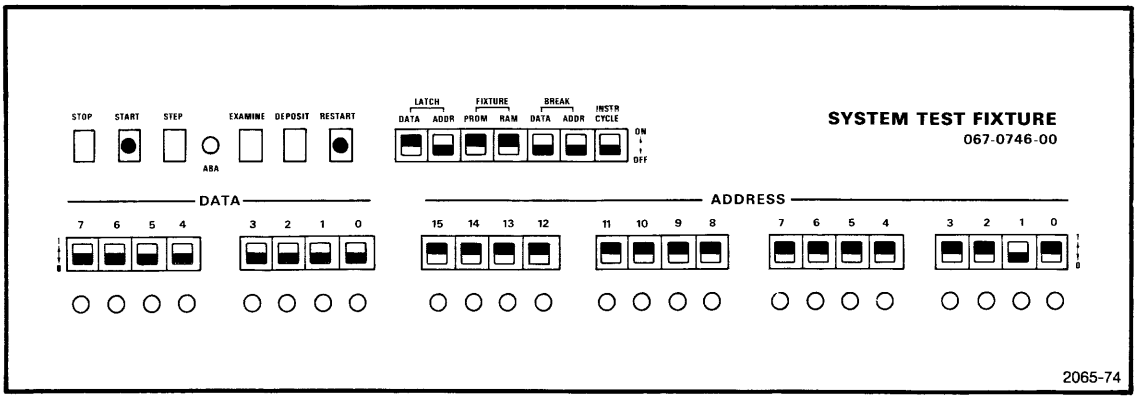


Fig. 5-26.

4051 Tape Circuitry Test

1. Power down the 4051.

2. Attach the System Test Fixture to J5 (Fig. 5-8). Detach the tape control cable from the tape drive board and attach the test connector board (067-0790-00) to the end of the cable. Remove the J82 connector from the tape drive board to disconnect ±20 V power.

3. Power up the 4051.

4. Set the seven control switches to the positions indicated in Fig. 5-27.

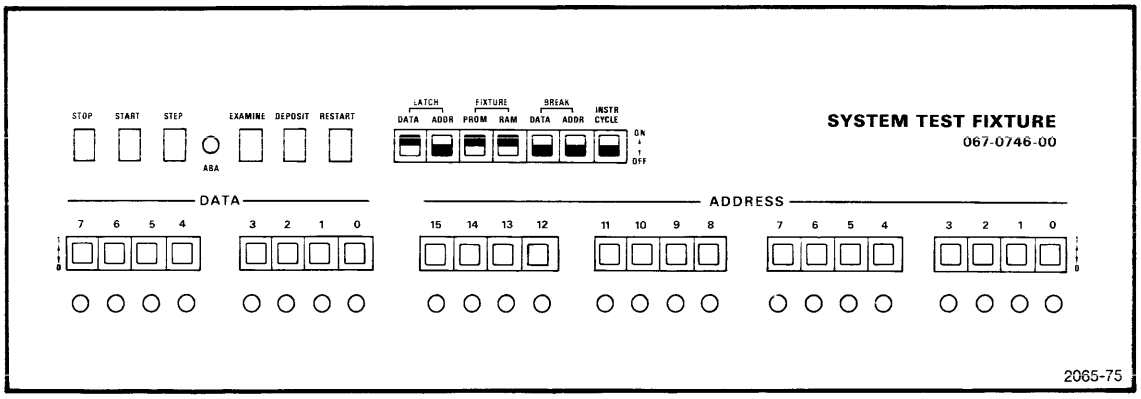


Fig. 5-27.

5. Data is loaded into a memory location by keying the memory address into the Address switches and the data into the Data switches. Pressing the DEPOSIT switch transfers the data into the memory register indicated by the Address switches. Pressing the EXAMINE switch causes data appearing in the register indicated by the Address switches to be displayed on the Data LEDs.

   Load 94 into the address register FFFE (Fig. 5-28).

   Load 00 into the address register FFFF (Fig. 5-29).

6. Place 00 into the Data switches and FFFD into the Address switches.

   Press RESTART and then START to begin executing the first tape test (Fig. 5-30).

7. If no errors occur for test 1, the Data LEDs show a value of 80 after which you have 30 seconds to prepare for test 2 without turning off power to the 4051.

8. Prepare for test 2 by the following steps.

   a) Remove the test connector board from the tape control cable.
   b) Place the tape control cable back on the 4051 tape drive board (J81).
   c) Replace the ±20 volt power connector (J82).
   d) Have NO tape cartridge in the tape drive.

9. If there are no errors for the first part of test 2, the Data LEDs show a value of 40.

10. Begin the second part of test 2 by placing a tape into the 4051 tape drive. The tape cartridge must be previously marked (formatted on a working 4051) and must NOT be SAFE.

    The following activity then occurs:

    09 is placed into the Data LEDs and remains unchanged unless an error occurs.

    The Load Point hole is read 5 times.

    The test proceeds to test 3 and continuously reads data on the tape.

11. EJECT the tape to stop the test. If the test is left running, the cartridge will *not* stop at end of tape.

12. Analyze errors. Data in the Data LEDs if other than 00 or 09 indicates that tape errors have occurred. The Data LEDs show accurately up to 255 errors. The total number of errors can be found in memory locations 9 and A.

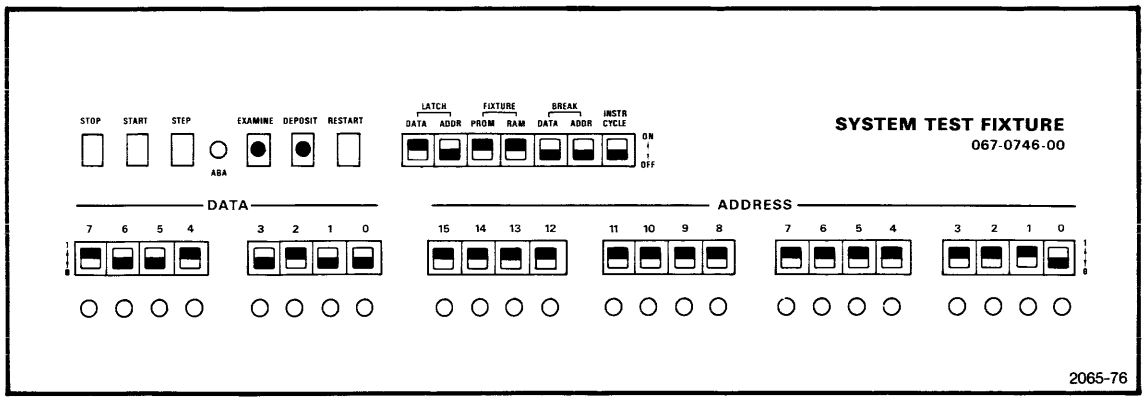


Fig. 5-28.

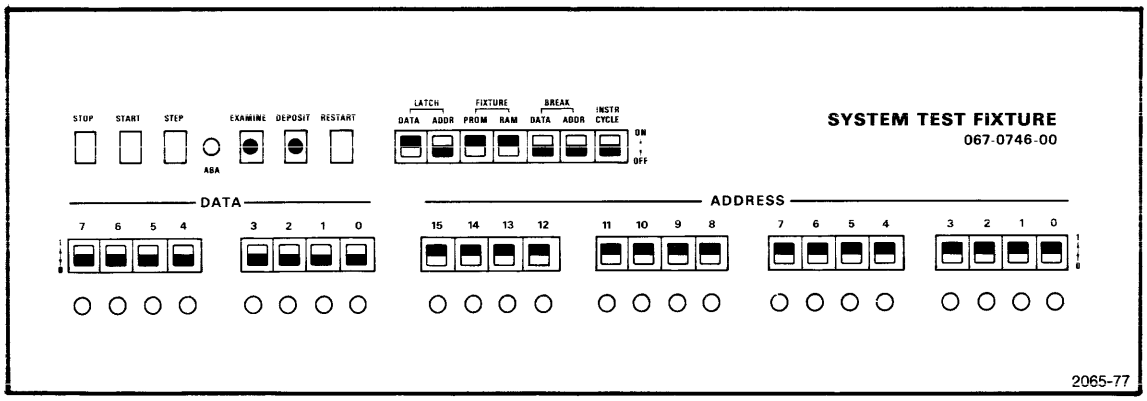


Fig. 5-29.

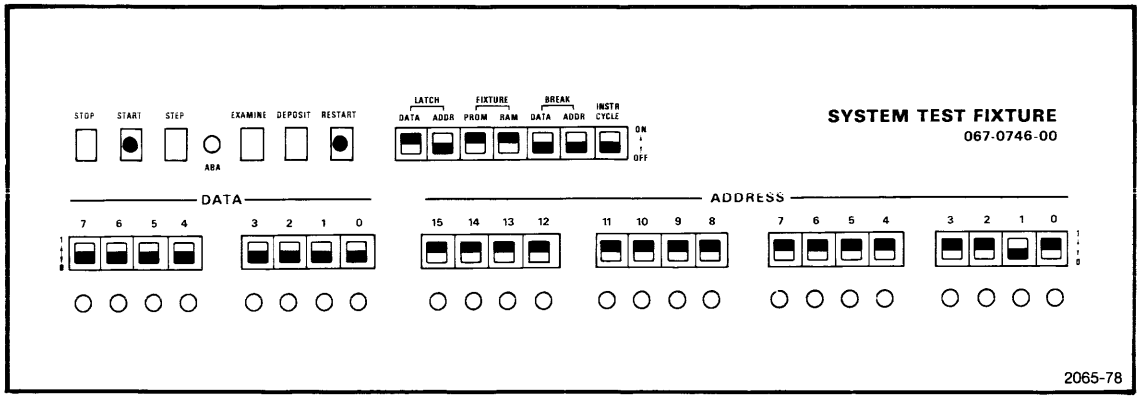


Fig. 5-30.

13. To begin tape test 4, load 97DF into the restart vector at memory locations FFFE-FFFF. Press RESTART and START. The 7 control switches are to be set the same as for tape test 1.

    Test 4 begins execution by rewinding the tape then reading the tape, pausing after each record.

    The Data LEDs read zero if no errors occur. The Data LEDs record up to 256 errors. Memory locations 7 and 8 record up to 65,535 errors.

    To stop the test, EJECT the tape, otherwise the tape may run past the end of tape marks.

The following is a listing of the magnetic tape error messages in hexadecimal notation.

ERROR NO.	MESSAGES
2	"DELAY OUT" = 0 (U481 on the tape drive board)
3	"DELAY OUT" = 0 (U481 on the tape drive board)
4	"TUTS" = 1 or "TNIM" = 0 (U495 on the tape drive board)
5	"TUTS" = 1 or "TNIM" = 1 when the motor runs (U495 on the tape drive board)
6	"TUTS" = 0 or "TNIM" = 1 after 60 ms (U495 on the tape drive board)
7	"TUTS" = 1 or "TNIM" = 0 60 ms after the motor is stopping (U495 on the tape drive board)
8	"LOADED" = 1 without cartridge (tape drive board)
9	"SAFE" = 0 for safe mode (tape drive board)
A	"MDATA" = 0 no WCLOCK, U823, U713, U711, U721 (on cpu board or cable)
B	"RBYTE" = 0 U825, U815 (on cpu board or cable) or bad write clock (21.6 μs)
C	WDATA, RDATA error (cpu board or cable), U761, U711, U751, U561
D	NO "REMARK" U815, U561, U721, U715, U711 (on cpu board or cable)
E	No "FMARK" (on cpu board or cable)
F	No "RMARK" Flag is set because U825-pin8 does not reset U821 (on cpu board or cable)

ERROR NO.	MESSAGES
10	"FILEFND" = 0 (U815-pin9 or U361-pin8)
11	"FILEFND" = 1 (cpu board or cable)
12	No "FILEFND" U361-pin39 or U815-pin9 (cpu board or cable)
13	Errors in "DELAY OUT" — "READ/WRITE", "TUTS" — "FAST" "TNIM", "REV", "SAFE", "DRTAPE" (cpu board or cable)
14	"UPHOLE", "LOHOLE" flags never set
15	"LOADED" problem or "DELAY IN" problem (cpu board or cable)
16	"LOADED" = 0 (cpu board or cable)

Detail About The Test Connector Board (Tape Connector)

"DELAY OUT" (26) is connected to "READ/WRITE" (29). "TUTS" (23) is connected to "FAST" (31). "TNIM" (25) is connected to "REV" (32) and "LOHOLE" (28). "SAFE" (27) is connected to "DRTAPE" (33) and "UPHOLE" (30). "LOADED" (19) is connected to "DELAY IN" (34). "WCLOCK" (21) is tied to one-shot (74121) input. "RCLOCK" (20) is tied to the Q output of the one-shot. "WDATA" (24) is connected to "RDATA" (22).

Tape Tests—A Brief Description

Tape Test 1 (Start 9400)

This test uses the test connector board to verify the tape control circuitry on the cpu board. Errors are displayed on the Data LEDs and can be looked up in the list of error codes. If there is an error, the test program loops at the bad location so that a voltage can be measured on an oscilloscope.

Tape Test 2 (Start 95C4)

Part one requires that the tape drive be empty of any cartridge and that the control and power connections be correct on the tape drive board. Hardware being tested corresponds to DELAY, LOADED and SAFE signals. 40 is displayed in the Data LEDs if this part tests without error. See error codes for errors.

Part two requires that a previously marked tape be inserted into the tape drive. The cartridge must NOT be SAFE. The tape rewinds and reads the load point 5 times. Afterwards, tape data is continuously read. EJECT the tape to stop the test.

If the Data LEDs show data other than 09, an error has occurred. The DATA LEDs count up to 255 errors. Memory locations 7 and 8 store an error count up to 65,535 errors. Memory locations 9 and A store the number of passes.

Tape Test 3 (Start 96A5)

This test rewinds and then continuously reads data on a previously marked tape. The tape should NOT be SAFE. Data LEDs count up to 255 errors (00 or 09 is displayed if no errors exist). Memory locations 7-8 contain an error count up to 65,535 errors. Memory locations 9 and A store the number of passes.

Tape Test 4 (Start 97DF)

This test is the same as tape test 3 except that the tape pauses at the end of each record as data is read.

Section 6

4051 CIRCUIT DESCRIPTION

SYSTEM ARCHITECTURE

The TEKTRONIX 4051 Graphic System is a computational graphics tool based on a Motorola 6800 microcomputer system (Fig. 6-1). The motorola 6800 microprocessor unit (MPU) provides control logic, data manipulation and computation capability to the 4051 Graphic System. The MPU uses contents of read-only memory (ROM) to specify how the system is to perform. An extended BASIC computer language interpreter is implemented as code stored in the system ROM devices. Temporary data and results of computations can be stored in random-access memory (RAM). Data in RAM can also be MPU instructions, but is more often BASIC language program instructions and computational data.

Bit patterns in ROM specify the type of activity to be performed by the MPU. These instructions (bit patterns) cause various operations to be performed.

1) Read the data at a specified address location and place it in an MPU register.
2) Write the data from an MPU register to a specified addressable location. The addressable location may be RAM, PIAs, or ACIAs.[1]
3) Perform computational or data comparison procedures on specified data.
4) Jump or branch to a location other than the next successive memory location to retrieve the next instruction for program execution. These jump or branch operations are often determined by interrogating the result or status of an arithmetic or logical computational operation.
5) Stop and wait for interrupt.
6) Branch to and return from subroutines.
7) Branch to a vectored routine to service interrupts and system restart operations.

[1]**MPU = Microprocessing Unit**
ROM = Read Only Memory
RAM = Random Access Memory
PIA = Peripheral Interface Adapter
ACIA = Asynchronous Communications Interface Adapter

The Motorola 6800 MPU uses a 64K address space. The lower 32K is dedicated for RAM devices (0000-7FFF in hexadecimal notation). The upper 32K is dedicated for ROM and peripheral interface devices such as PIAs and ACIAs.

The various elements that share the 64K address space possess unique attributes.

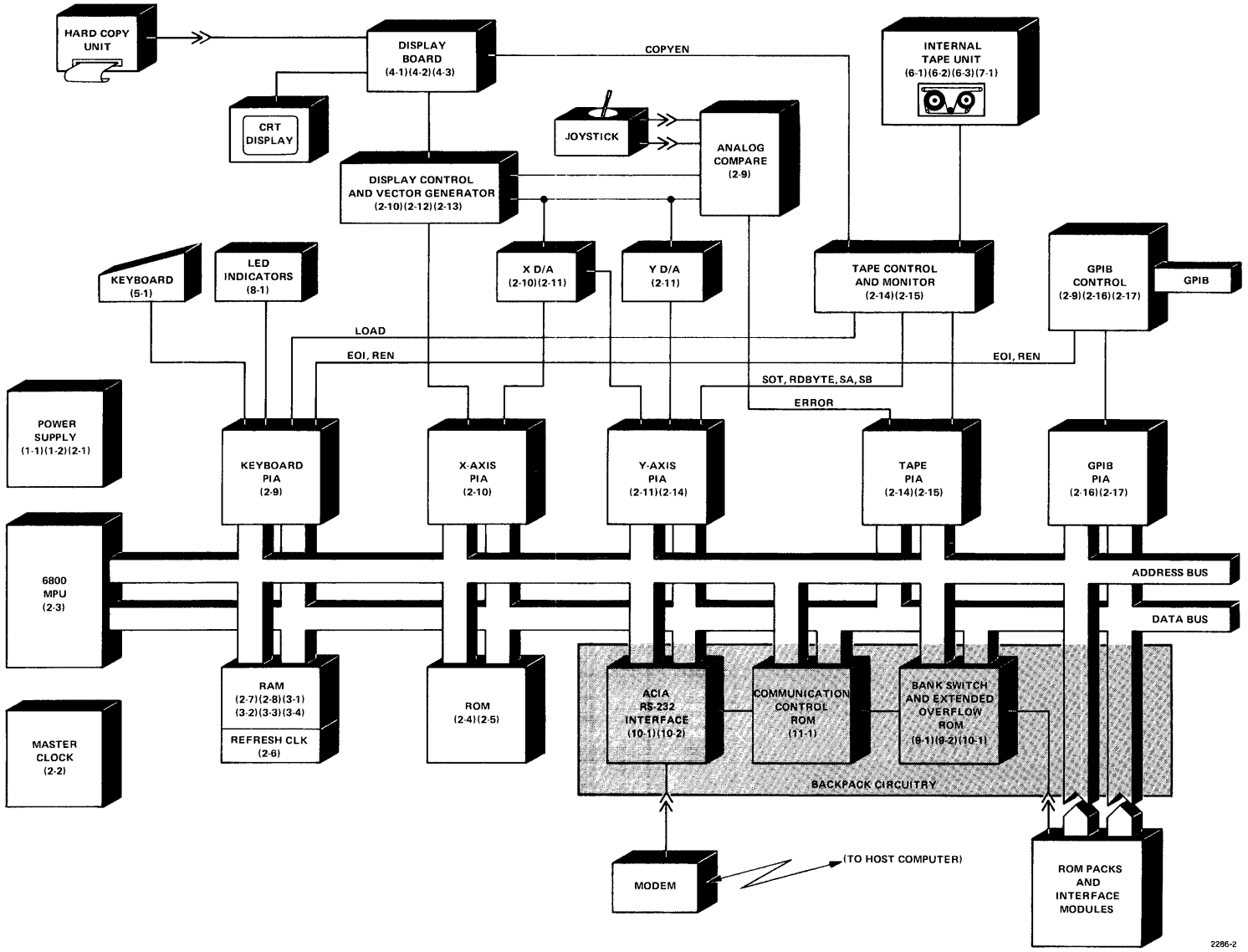


Fig. 6-1. 4051 Graphic System block diagram.

ROM (READ-ONLY MEMORY)

Data in read-only memory devices are placed in the devices during the manufacturing process. This data cannot be changed by functions of the MPU. Thus data in these devices becomes a set of permanent programs and data for the MPU that cannot be changed without placing a new programmed ROM device into the electrical circuits.

RAM (RANDOM-ACCESS MEMORY)

Data in random-access memory devices is meaningless when power is initially applied to the system. Data can be placed in the RAM address locations for later use by the MPU as either computational data or instructions. The process for storing data into RAM requires that the MPU perform a data storage or write operation to a specified RAM address location for each byte of data to be stored. Direct memory access by other devices, accommodated by the Motorola 6800 microprocessor is not implemented in the 4051 Graphic System.

Table 6-1

DATA EQUIVALENCE FOR DECIMAL, HEXADECIMAL AND BINARY CODES

DECIMAL	HEXADECIMAL	BINARY
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

PIA

(PERIPHERAL INTERFACE ADAPTER)

Peripheral interface address locations are used to pass data bytes of information between the MPU and device control circuitry. Device control circuitry can either be devices external to the 4051 Graphic System such as printers and plotters, logical system control devices such as memory bank switch circuitry, or system data handling devices such as the keyboard, display magnetic tape unit, joystick interface and general purpose interface bus (GPIB). Peripheral interface address locations are addressed like any other memory location in the 4051 Graphic System,

Each PIA has six internal registers (Fig. 6-2) and requires four contiguous memory addresses. There are two control registers, two data direction registers and two peripheral data buffers in each PIA. Interrupt logic protocol is determined, in part, by data placed into the control registers. Also, one bit of the data in control registers determines which of two registers is addressed by a common address—a data direction register or a peripheral data buffer.

Before performing any I/O operation to a peripheral device using a PIA, the following procedure, or a similar procedure, must be performed.

1. Place data into a control register to enable addressing a data direction register.

2. Place data into a data direction register to establish proper data direction transfer (send or receive) for each of eight peripheral data lines.

3. Place data into the control register to initialize the appropriate interrupt protocol for the CA and CB device control lines. The same data byte must also allow the peripheral data buffer to be addressed.

4. Data communications via the peripheral data bus can now be performed.

When processing an interrupt request, the appropriate control register must be read. This resets any active processor interrupt status after transmitting the current interrupt status to the MPU.

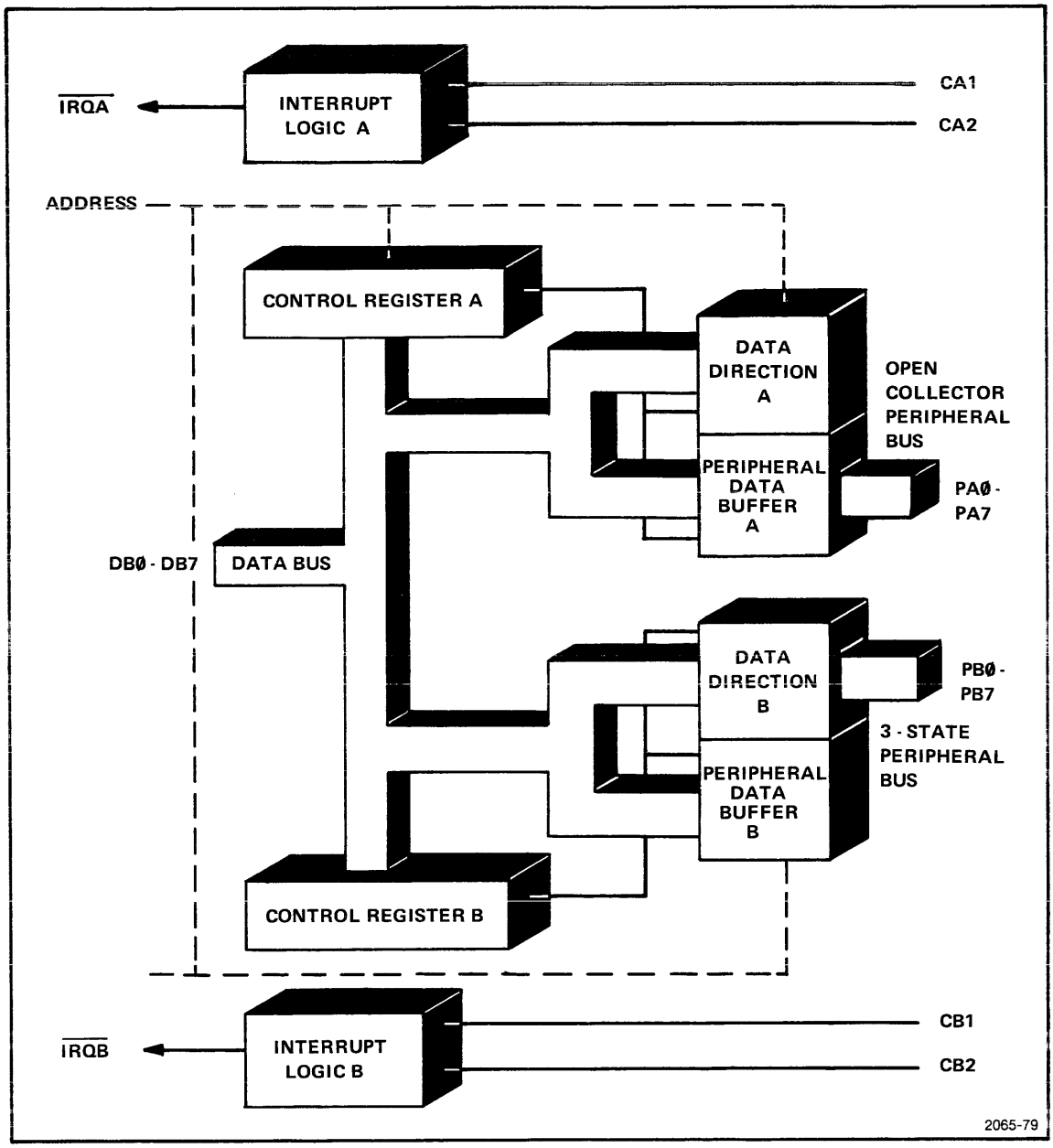


Fig. 6-2. Peripheral Interface Adapter (PIA) block diagram.

ACIA

(ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER)
The ACIA is used in asynchronous serial data communications. It takes a byte of data and converts it to a string of digital pulses for serial data transmission to a modem, with or without parity attached. The ACIA can also take a string of data and convert it to 8-bit parallel binary data to be made available to the MPU. Parity can be checked if 9 bits of data (including parity) are transmitted or received. Timing for ACIA serial data transmission is provided by external clock inputs — one for transmit and one for receive. The MPU interface timing is the same as for any standard memory cycle.

There are four registers in an ACIA requiring only two address locations (Fig. 6-3). Each register is interrogated by an address in conjunction with a read or write operation. Memory write operations, as performed by the MPU can load data into either the control register or the transmit data register. Read operations receive data from either the status register or the receive data register.

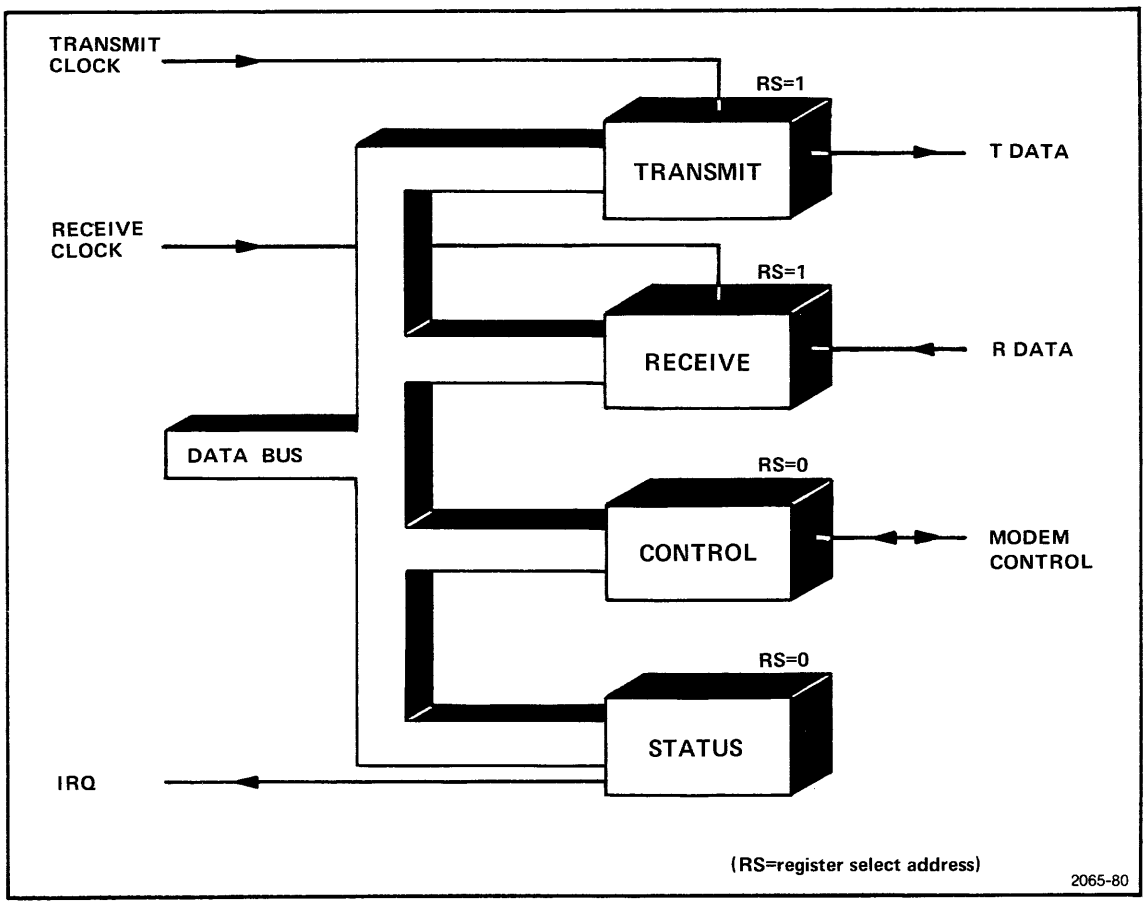


Fig. 6-3. Asynchronous Communications Interface Adapter (ACIA) block diagram.

For a detailed analysis of Motorola 6800 microcomputer operation, refer to specification sheets and documentation provided by Motorola Semiconductor, Inc. for the following devices.

MPU = XC6800
RAM = MCM6605L
ROM = MCM6832L
PIA = SC6820
ACIA = SC6850

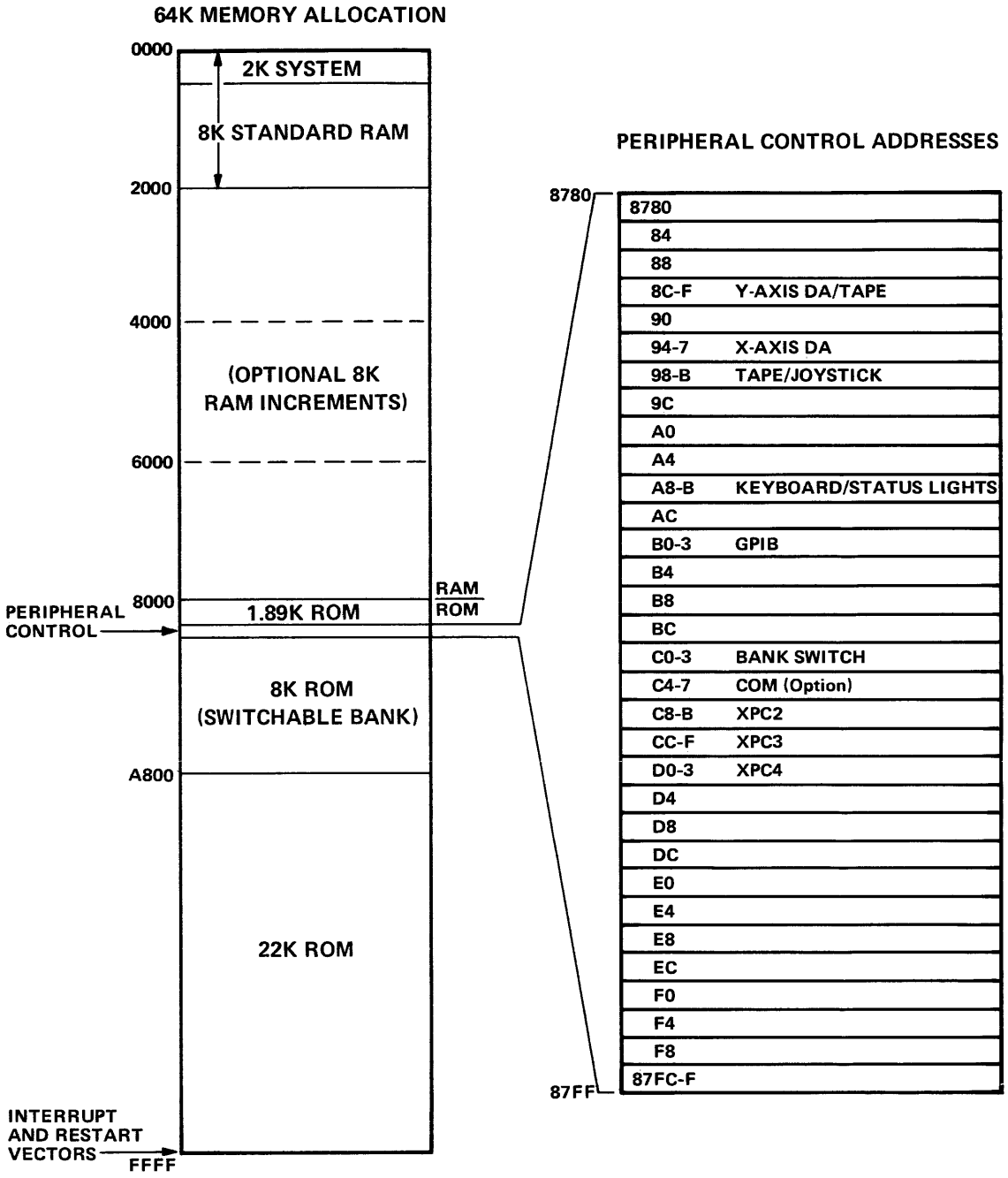
SYSTEM ADDRESSING

All read-only memories (ROM), random-access memories (RAM), and device interface circuits reside in the addressable memory space of the Motorola 6800 microprocessor (MPU). Standard device interface circuits are of two types. The most common is the peripheral interface adapter (PIA). The other is the asynchronous communication interface adapter (ACIA). Other interface circuitry can be built of discrete logic elements.

The Motorola memory address space is 64K bytes or 65,536 memory address locations (Fig. 6-4). The lower 32K bytes (0 through 32,767 in decimal notation or 0000 through 7FFF in hexadecimal notation) are dedicated for system RAM devices. Into these locations, the MPU stores temporary system data, BASIC program language statements, computational data, and system configuration tables identifying available ROM packs and external device interfaces.

The upper 32K bytes of memory (8000 through FFFF) are used for ROM devices and device interface circuitry. The BASIC computer language interpreter and device control programs are stored as unchangeable data in read only memory device. Refer to the address allocation table for system address assignments.

An 8K memory bank is used by the ROM packs. This memory bank occupies address locations 8800-A800. Memory bank switching is accomplished by transmitting a data byte to a special bank switch address (87C0). This special location is the bank switch register. In the Firmware Backpack, the bank switch register is generated by discrete logic. In the Communications Backpack, the bank switch register is a peripheral data buffer or register in a PIA. Data placed in the bank switch register is used to logically connect or select an 8K byte ROM bank or external peripheral interface. This logical connection allows the selected bank to respond to addresses in the switchable bank address region. External PIAs respond to XPC2, XPC3 or XPC4 addresses if their ROM address bank is selected.



DIVISION	ADDRESS BOUNDARIES
Standard RAM	0000-1FFF
Optional RAM	2000-7FFF
1.89K ROM	8000-877F
Peripheral Control	8780-87FF
8K Switchable Bank	8800-A7FF
22K ROM	A800-FFF7
Interrupt Vector	FFF8-FFF9
Restart Vector	FFFE-FFFF

2286-11

Fig. 6-4. Memory allocation map for the 4051.

4051 TIMING

Most of the 4051 timing circuitry is shown on schematic sheet 2-2 in the 4051 schematics section in Volume 2 of the 4051 Service Manual with additional timing on sheets 2-6 and 2-14. Timing requirements of the Motorola 6800 microprocessor system devices are reproduced as specification documents in the appendix on Motorola specifications. Figure 6-5 is a block diagram showing how the various timing pulses are generated.

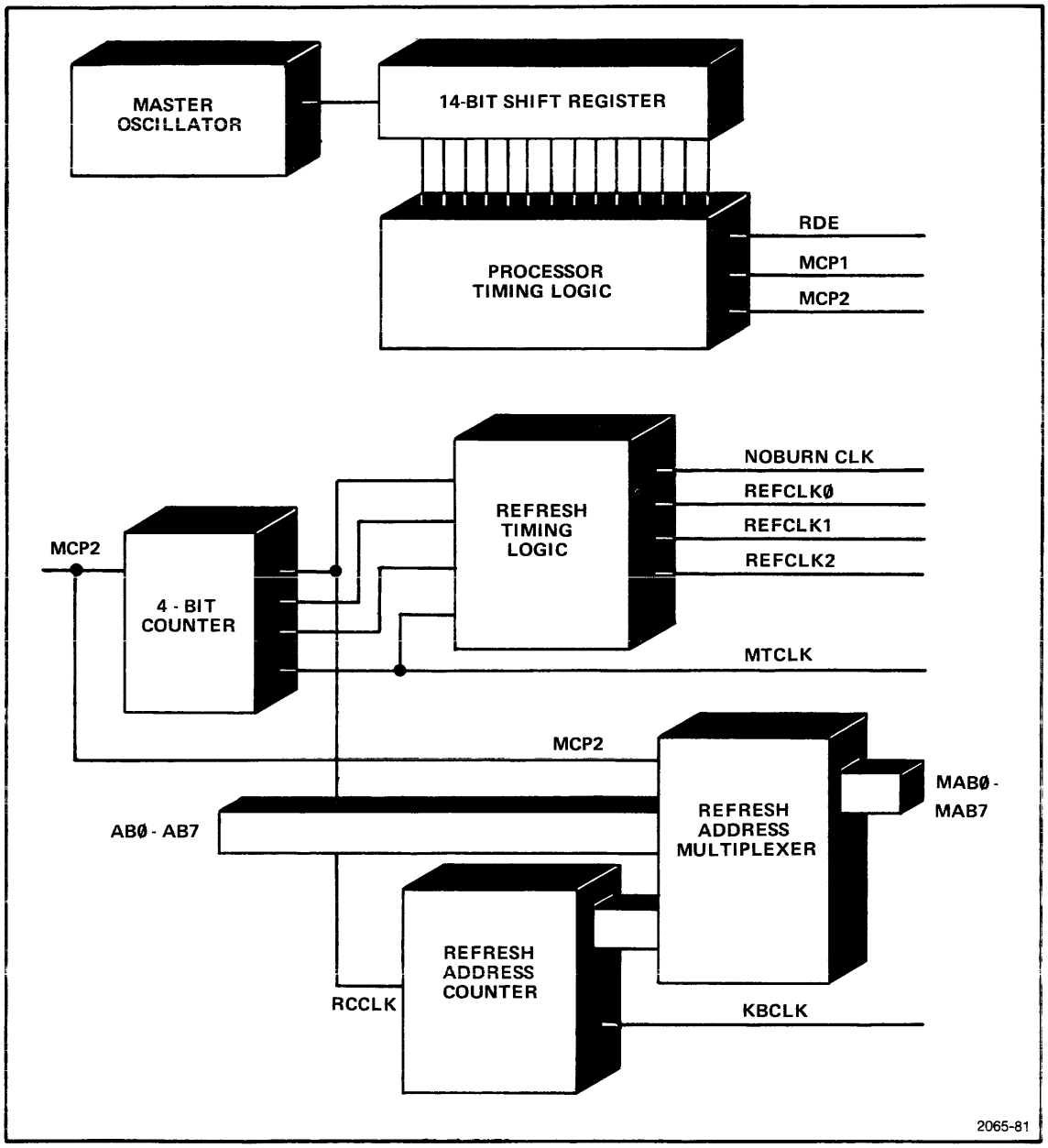


Fig. 6-5. Block diagram of system timing circuits.

Figures 6-6, 6-7, and 6-8 are timing diagrams showing the timing relationships between the various timing signals in the 4051. The master oscillator has a frequency of 12.5 MHz or a cycle time of 80 ns. A 14-bit shift register is clocked by the oscillator output and drives combinatorial logic to provide MCP1, MCP2, and RDE. MCP1 and MCP2 are the master clock phase one and phase two signals respectively. They are used to clock the microprocessor and all 6800 system devices. The read enable (RDE) signal and memory refresh clocks (REFCLKn) are generated to provide memory refresh and data read/write timing.

Memory refresh timing circuitry uses a 4-bit counter clocked by MCP2, the output of which drives combinatorial logic to generate NOBURN CLK (used to prevent phosphor burns on the crt during the draw of short vectors, REFCLKn (used to provide refresh activity for a selected bank of random access memory), MTCLK (used as a source clock for magnetic tape timing control) and RCCLK (used to provide a memory refresh address and generate timing keyboard switch decoding).

Figure 6-9 shows a brief block diagram of magnetic tape timing circuitry for writing data to tape. The reading of data from tape, using the self-clocking NRZ data format of data on the tape, is described in detail later. Figure 6-10 shows the important timing relationships between the various signals responsible for magnetic tape timing. The schematic reference for the circuitry is sheet 2-14 of the 4051 Schematics in Volume 2 of the 4051 Service Manual.

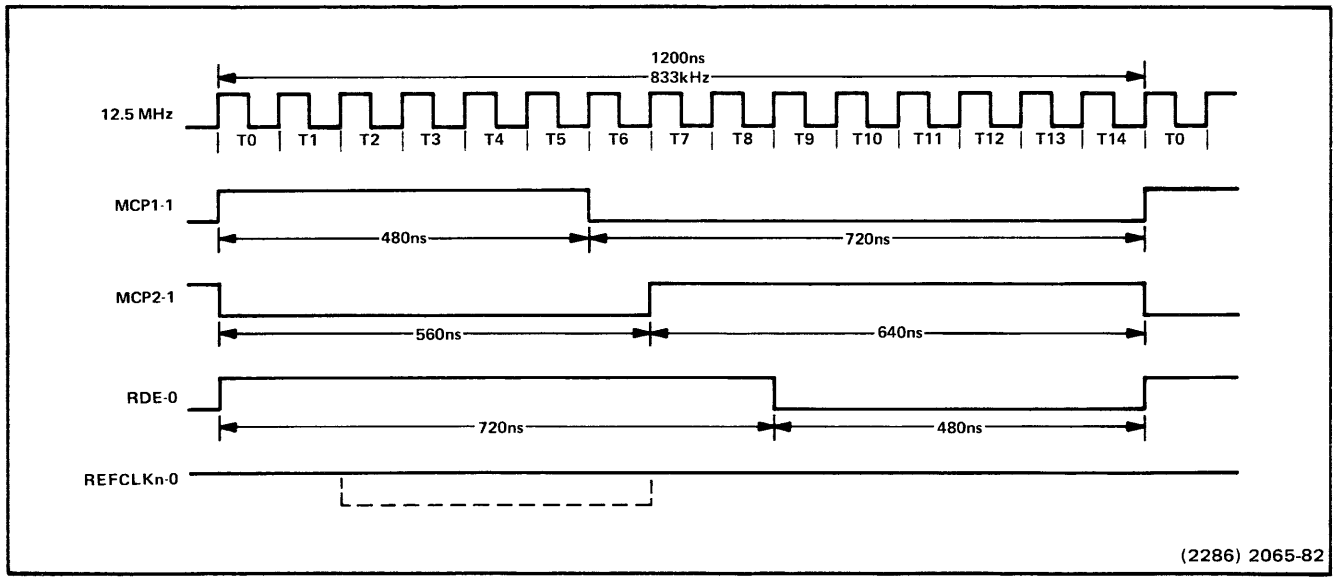


Fig. 6-6. Processor timing.

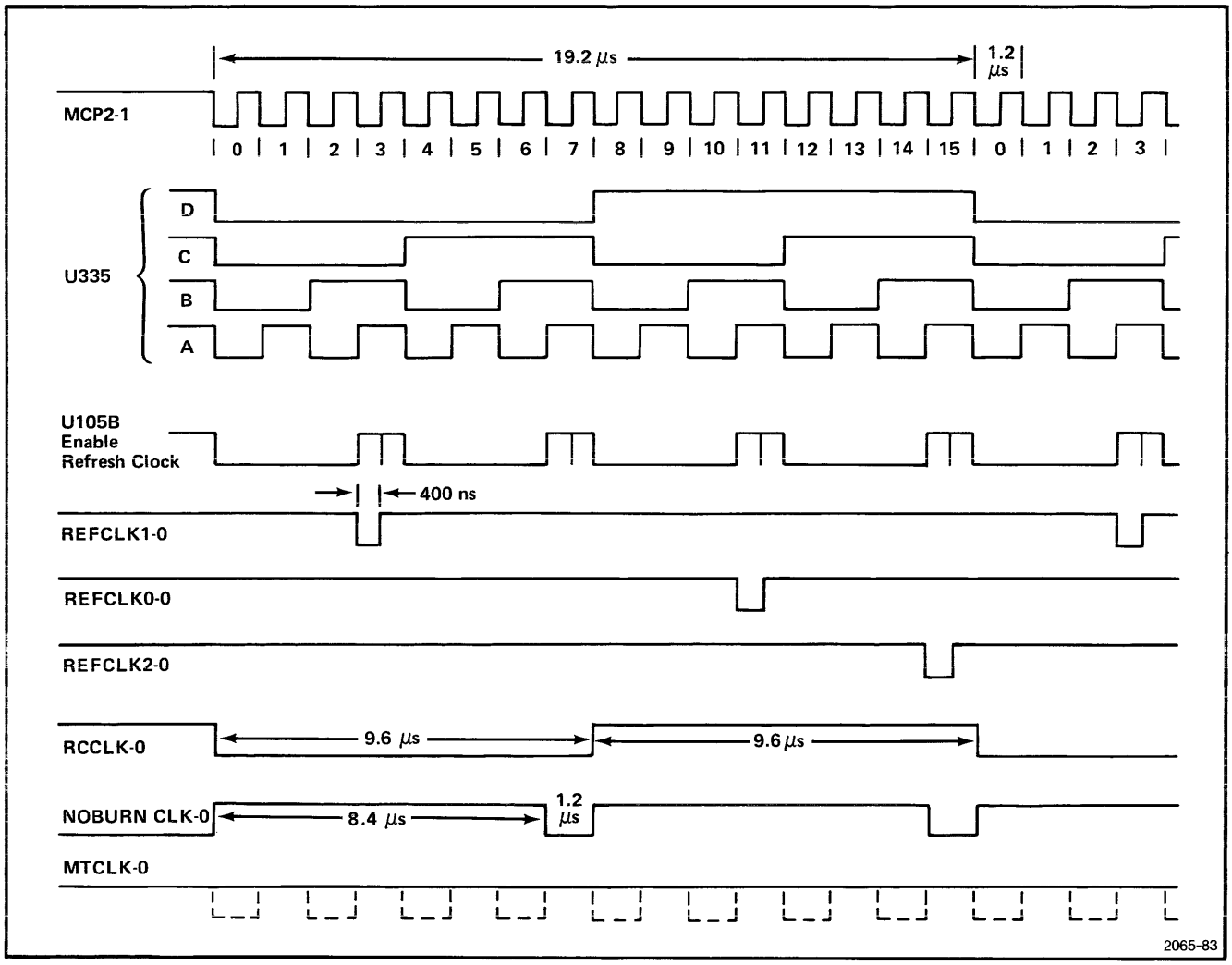


Fig. 6-7. Memory refresh timing.

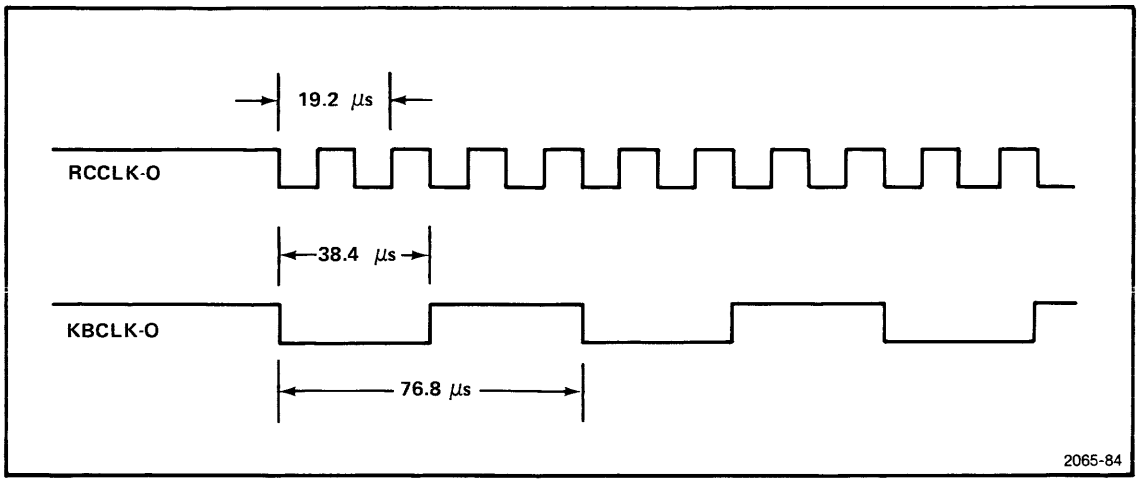


Fig. 6-8. Keyboard timing.

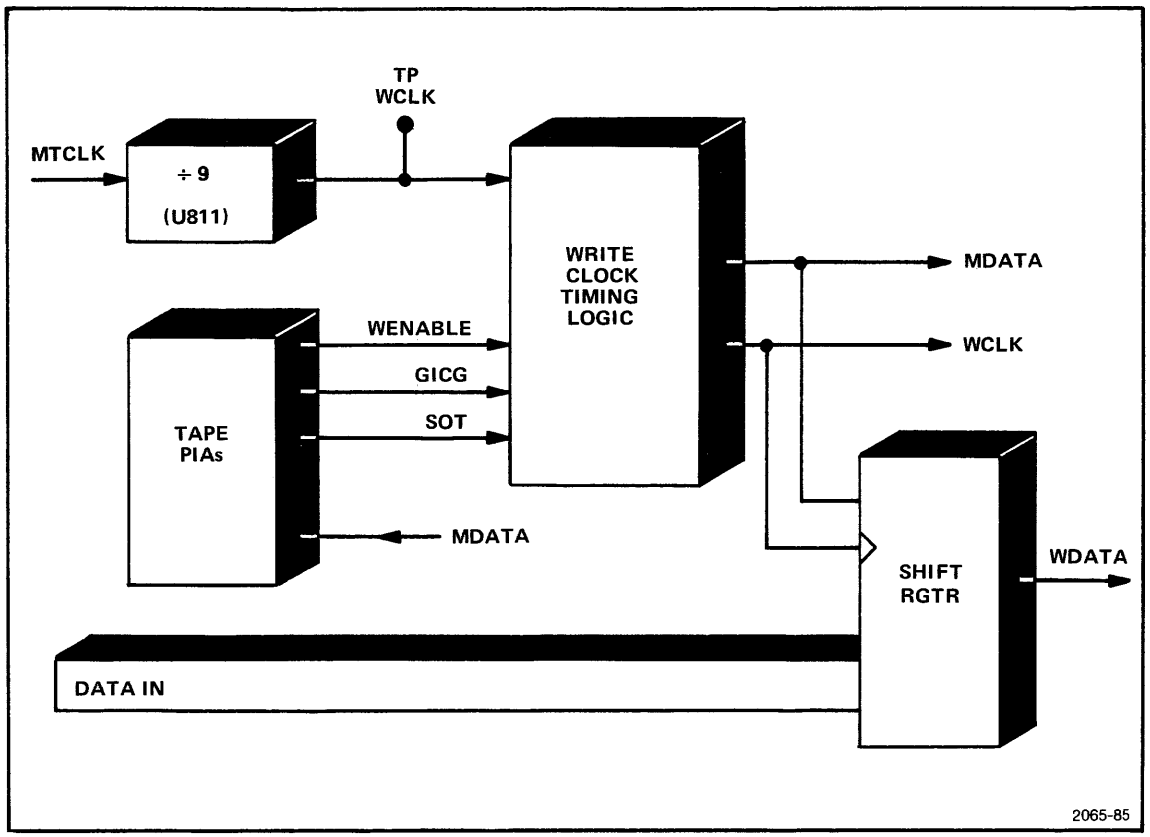


Fig. 6-9. Tape write timing circuits—block diagram.

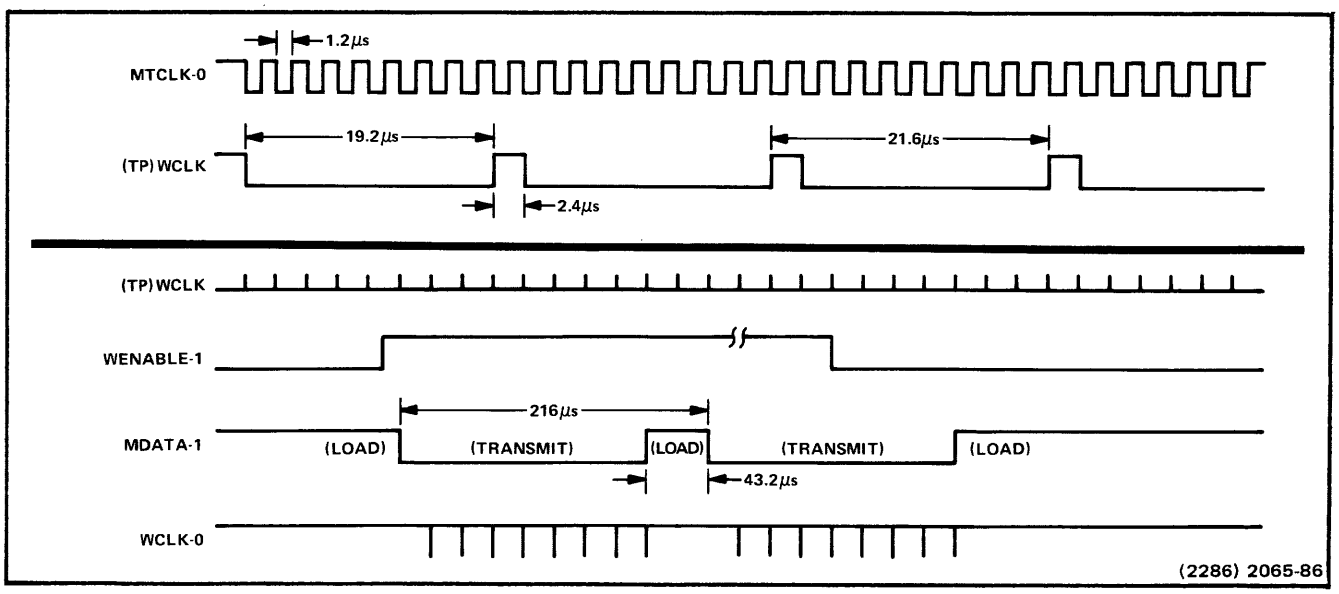


Fig. 6-10. Tape timing for writing data to the tape.

4051 KEYBOARD OPERATION

Refer to the block diagram (Fig. 6-11) and 4051 schematic sheet 5-1. The MPU causes the KBHALT-1 device control line to be lowered. This enables the KBCLK-0 keyboard clock signal to increment a key position decoding counter. The decoding counter causes each of 128 positions in the keyboard matrix to be interrogated. At the end of the 128 position cycle, the KEY-1 signal is placed into the high state via the J-K flip flops of U5A and U5B. If a key closure is encountered in the keyboard matrix, then the J-K flip flops are reset causing KEY-1 to remain high until the next KBCLK-0 signal occurs, at which time KEY-1 goes low and the key closure data on lines KC0 through KC6 can be read. The actual key closure position is equal to the data on lines KC0 through KC6 minus one. The key closure data is valid for only76.8 μs unless the KBHALT-1 device control line is made high during the 76.8 μs time frame.

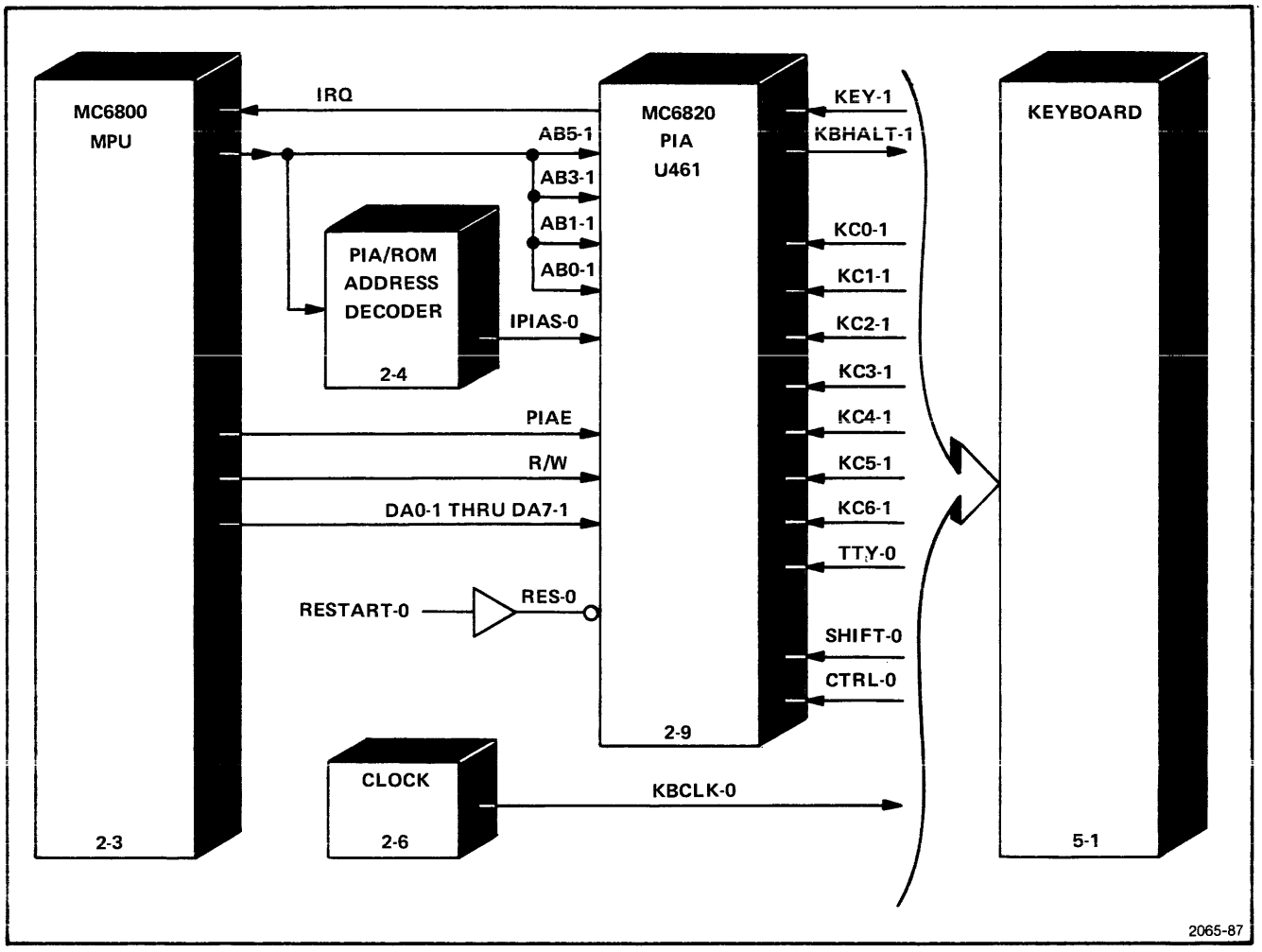


Fig. 6-11. Keyboard control circuitry block diagram.

The SHIFT keys, CONTROL key, and TTY LOCK key do not provide a microprocessor interrupt. Microprocessor interrupts are generated when KEY-1 goes low. The status of the SHIFT-0 and CTRL-0 signals are read on separate data lines to tell the software how to interpret the KC0 through KC6 data. See Table 6-2.

System operation where the SHIFT key causes the display to resume view mode is handled by circuitry shown on 4051 schematic 2-13. This schematic shows that the SHIFT-0 signal automatically triggers the display view state.

Table 6-2

KEY CODES (KC0 THRU KC6)
FOR THE 4051 KEYBOARD

ALPHANUMERIC
TERMINAL KEYS

KC	6	5	4	3	2	1	0	HEX
A	1	0	0	0	0	0	1	41
B	1	0	0	0	0	1	0	42
C	1	0	0	0	0	1	1	43
D	1	0	0	0	1	0	0	44
E	1	0	0	0	1	0	1	45
F	1	0	0	0	1	1	0	46
G	1	0	0	0	1	1	1	47
H	1	0	0	1	0	0	0	48
I	1	0	0	1	0	0	1	49
J	1	0	0	1	0	1	0	4A
K	1	0	0	1	0	1	1	4B
L	1	0	0	1	1	0	0	4C
M	1	0	0	1	1	0	1	4D
N	1	0	0	1	1	1	0	4E
O	1	0	0	1	1	1	1	4F
P	1	0	1	0	0	0	0	50
Q	1	0	1	0	0	0	1	51
R	1	0	1	0	0	1	0	52
S	1	0	1	0	0	1	1	53
T	1	0	1	0	1	0	0	54

ALPHANUMERIC TERMINAL KEYS

KC	6	5	4	3	2	1	0	HEX (cont)
U	1	0	1	0	1	0	1	55
V	1	0	1	0	1	1	0	56
W	1	0	1	0	1	1	1	57
X	1	0	1	1	0	0	0	58
Y	1	0	1	1	0	0	1	59
Z	1	0	1	1	0	1	0	5A
0	0	1	1	0	0	0	0	30
1	0	1	1	0	0	0	1	31
2	0	1	1	0	0	1	0	32
3	0	1	1	0	0	1	1	33
4	0	1	1	0	1	0	0	34
5	0	1	1	0	1	0	1	35
6	0	1	1	0	1	1	0	36
7	0	1	1	0	1	1	1	37
8	0	1	1	1	0	0	0	38
9	0	1	1	1	0	0	1	39
PAGE	1	1	0	1	0	1	0	6A
[	1	0	1	1	0	1	1	5B
:	0	1	1	1	0	1	0	3A
—	0	1	1	1	1	0	1	3D
]	1	0	1	1	1	0	1	5D
BK SPACE	0	0	0	1	0	0	0	08
ESC	0	0	1	1	0	1	1	1B
^	1	0	1	1	1	1	0	5E
@	1	0	0	0	0	0	0	40
LF	0	0	0	1	0	1	0	0A
RETURN	0	0	0	1	1	0	1	0D
TAB	0	0	0	1	0	0	1	09
CTRL	-	-	-	-	-	-	-	
;	0	1	1	1	0	1	1	3B
/	1	0	1	1	1	0	0	5C
RUBOUT	1	0	1	1	1	1	1	5F
TTY LOCK	-	-	-	-	-	-	-	
SHIFT(L)	-	-	-	-	-	-	-	
SHIFT(R)	-	-	-	-	-	-	-	
,	0	1	1	1	1	0	0	3C
.	0	1	1	1	1	1	0	3E
/	0	1	1	1	1	1	1	3F
BREAK	1	1	0	1	0	1	1	6B
SPACE	0	0	1	0	0	0	0	10

NUMERIC KEY PAD

KC	6	5	4	3	2	1	0	HEX
0	0	1	0	0	0	0	0	20
.	0	1	0	1	1	1	0	2E
1	0	1	0	0	0	0	1	21
2	0	1	0	0	0	1	0	22
3	0	1	0	0	0	1	1	23
4	0	1	0	0	1	0	0	24
5	0	1	0	0	1	0	1	25
6	0	1	0	0	1	1	0	26
7	0	1	0	0	1	1	1	27
8	0	1	0	1	0	0	0	28
9	0	1	0	1	0	0	1	29
(	1	1	1	1	1	0	1	7D
E	1	1	1	1	1	1	1	7F
)	1	1	1	1	1	1	0	7E
Λ	1	1	1	1	1	0	0	7C
/	0	1	0	1	1	1	1	2F
*	0	1	0	1	0	1	0	2A
-	0	1	0	1	1	0	1	2D
+	0	1	0	1	0	1	1	2B

FUNCTION KEYS

KC	6	5	4	3	2	1	0	HEX
FK1	1	1	0	0	0	0	0	50
FK2	1	1	0	0	0	0	1	51
FK3	1	1	0	0	0	1	0	52
FK4	1	1	0	0	0	1	1	53
FK5	1	1	0	0	1	0	0	54
FK6	1	1	0	0	1	0	1	55
FK7	1	1	0	0	1	1	0	56
FK8	1	1	0	0	1	1	1	57
FK9	1	1	0	1	0	0	0	58
FK10	1	1	0	1	0	0	1	59

LINE EDITING

KC	6	5	4	3	2	1	0	HEX
EXPAND	1	1	1	0	0	0	0	70
BK SPACE	1	1	1	0	0	0	1	71
SPACE	1	1	1	0	0	1	0	72
CLEAR	1	1	1	0	0	1	1	73
RECALL	1	1	1	0	1	0	0	74

TAPE CONTROL

KC	6	5	4	3	2	1	0	HEX
AUTO LOAD	1	1	1	0	1	1	1	77
REWIND	1	1	0	1	1	0	0	5C
MAKE COPY	1	1	0	1	1	0	1	5D

PROGRAM CONTROL

KC	6	5	4	3	2	1	0	HEX
AUTO NUM	1	1	1	0	1	0	1	75
STEP PROG	1	1	1	0	1	1	0	76

INDICATOR LAMPS

The 4051 schematics of sheets 2-9 and 8-1 are printed in part as Fig. 6-12. The +12 volt power supply provides power to the circuitry on the circuit board containing the indicator lights. The lights are activated by the microprocessor writing a data byte to the B data register of the keyboard PIA (peripheral interface adapter). If a data bit (D5, D6, or D7) is zero, the corresponding lamp turns on. An audio tone is generated by the MPU writing data bytes to the data register and alternating the state of data bit 7.

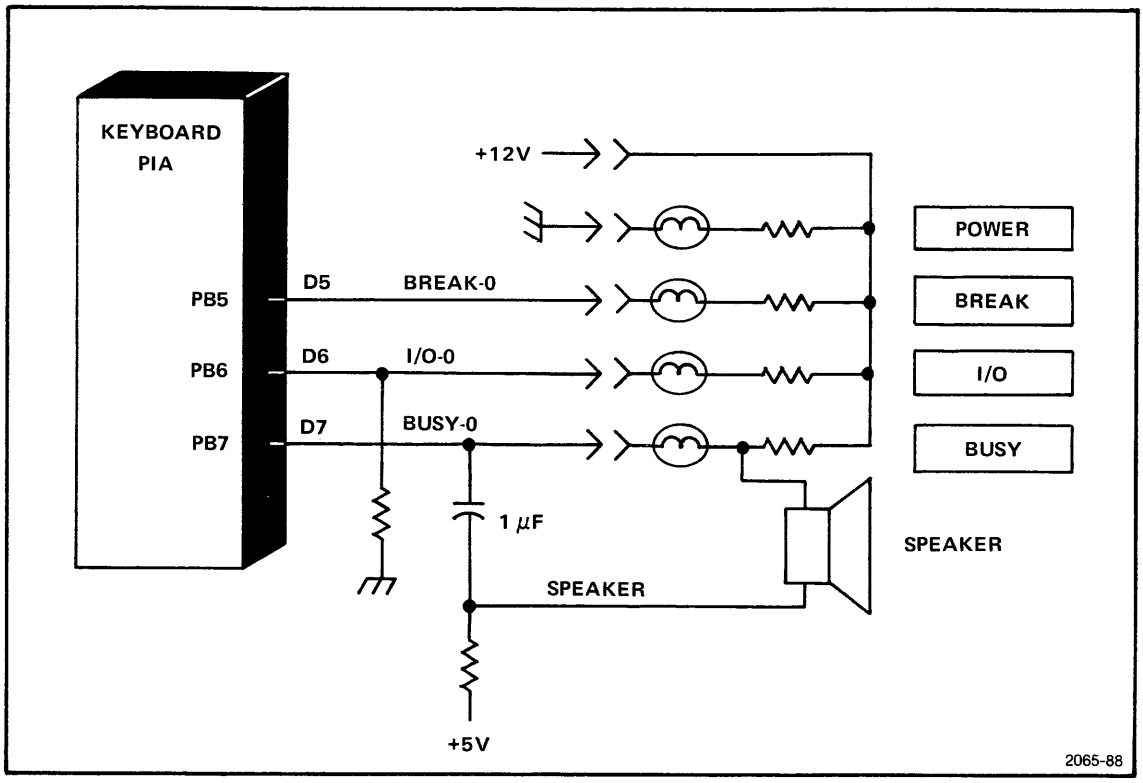


Fig. 6-12. Indicator board control circuitry.

DISPLAY CONTROL

The bulk of 4051 display operations require the drawing of vectors, the printing of dot matrix characters and the display of a refresh cursor character. Refer to the set of 4051 schematics in Volume 2, sheets 2-10 through 2-13. See also the display control block diagram (Fig. 6-13).

The Motorola 6800 microprocessor (MPU) communicates to the display control circuitry through a set of peripheral interface adapters (PIAs). The PIA output lines are programmed to control the display circuitry in a manner dictated by MPU instruction sequences in read only memory (ROM).

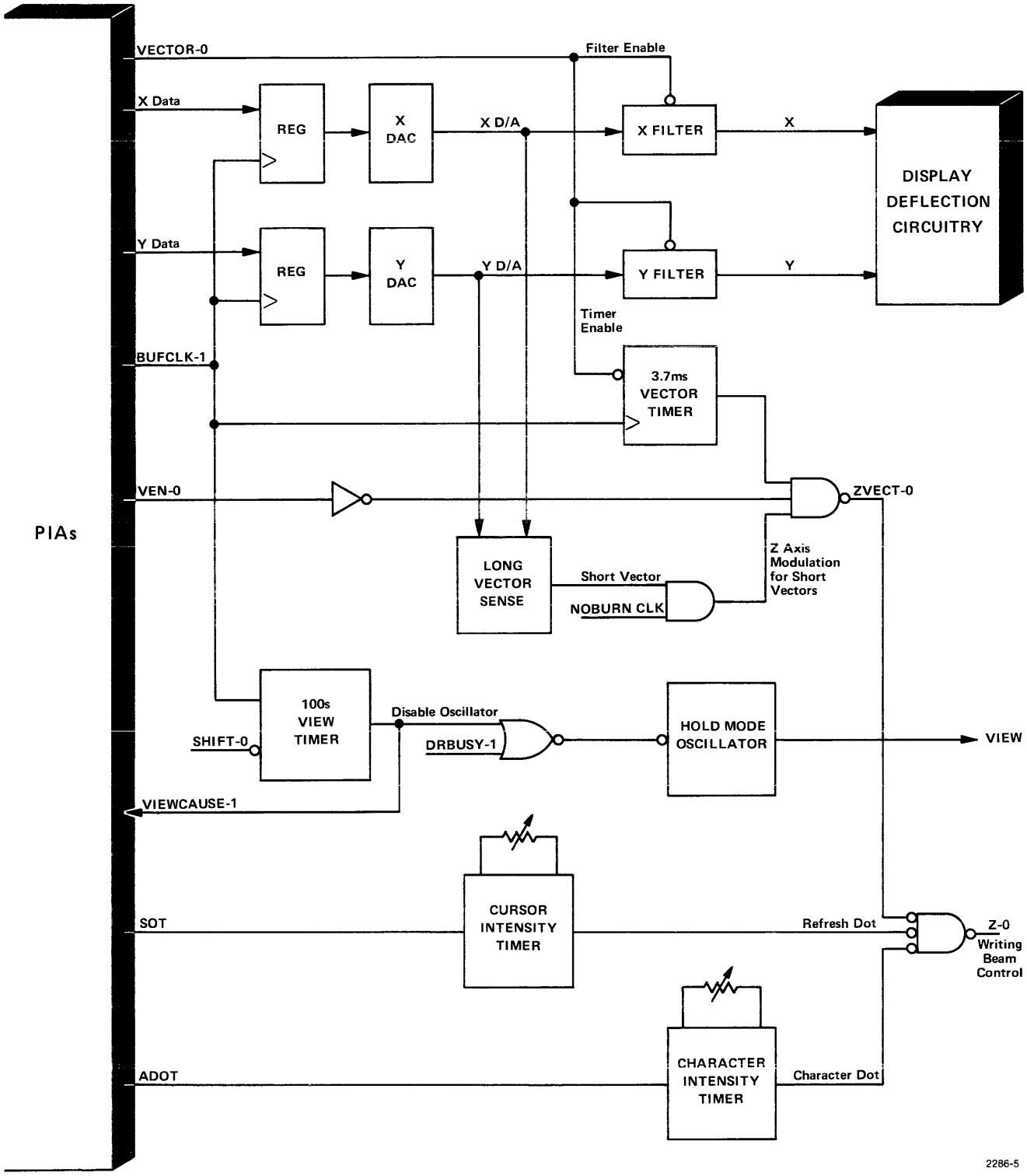


Fig. 6-13. Display control circuitry block diagram.

D/A OPERATION

Refer to the diagram (Fig. 6-14). See also 4051 schematics 2-10 and 2-11. The transistors are the outputs of TTL logic. Resistors that are binary fractions of R (R, R/2, R/4, R/8) are current programming resistors. Current through R/8 is eight times greater than current through R. Current through these resistors either goes through the transistor logic or through the current summing resistor Rb.

When transistor logic is on, output low, the transistor takes current from its current programming resistor, preventing current summing. The BIAS must be such that the disconnect diode has reverse bias when the switching transistor is on.

When the transistor logic is off, output high, the transistor either provides high impedance or reverse biases its source diode, thus causing the programmed current to be summed by the amplifier.

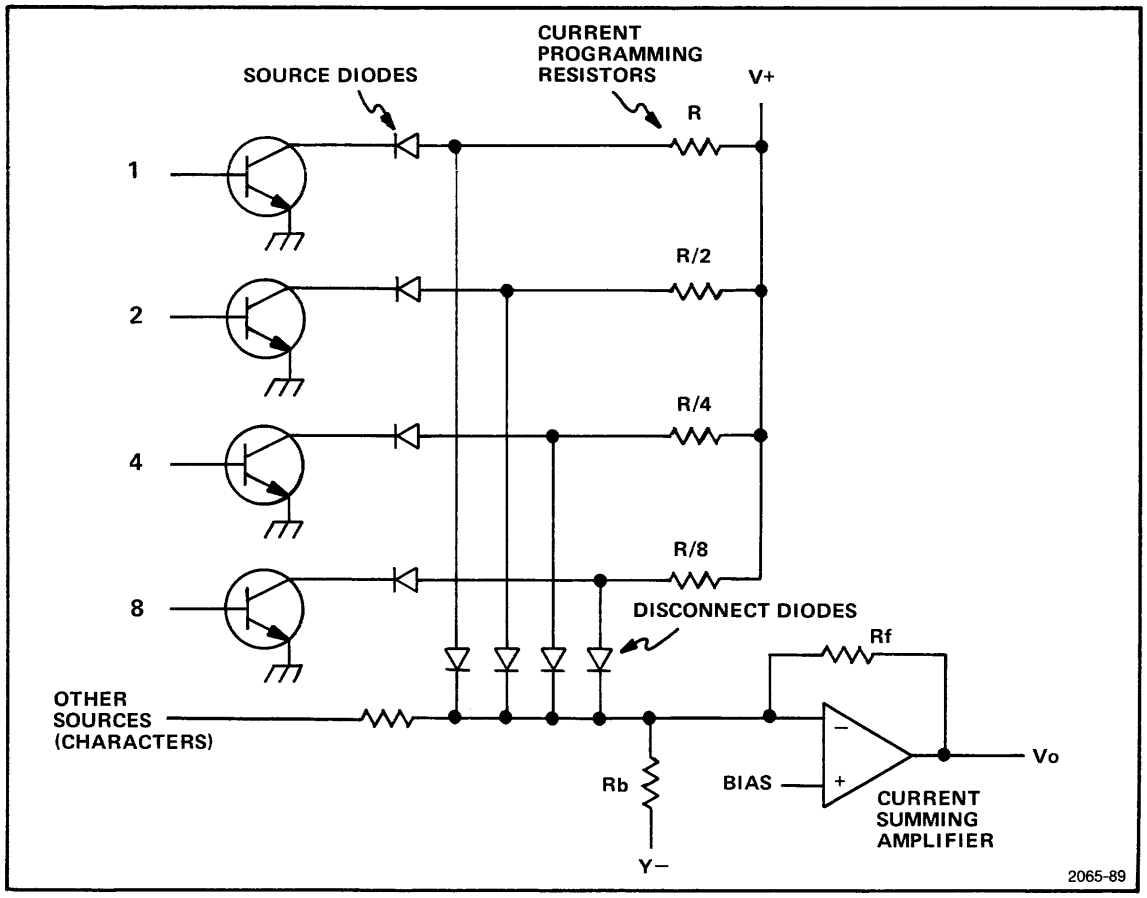


Fig. 6-14. Typical D/A converter using proportioned resistors and a current summing amplifier.

The current summing amplifier has the following operation. When no current comes through the disconnect diodes or other sources, the current through Rf is equal to the current through Rb. The junction voltage betweed Rf and Rb is determined by and is equal to the BIAS applied to the operational amplifier. As current comes through the disconnect diodes or other sources, the current through Rf is decreased by the total sum of input currents. Current through Rf may even reverse if the sum of input currents becomes large in order to maintain the junction voltage between Rf and Rb at the BIAS level.

Figure 6-15 shows the information flow through D/A converters in the 4051. The X Data and Y Data blocks are resistance networks like those previously described in Fig. 6-14.

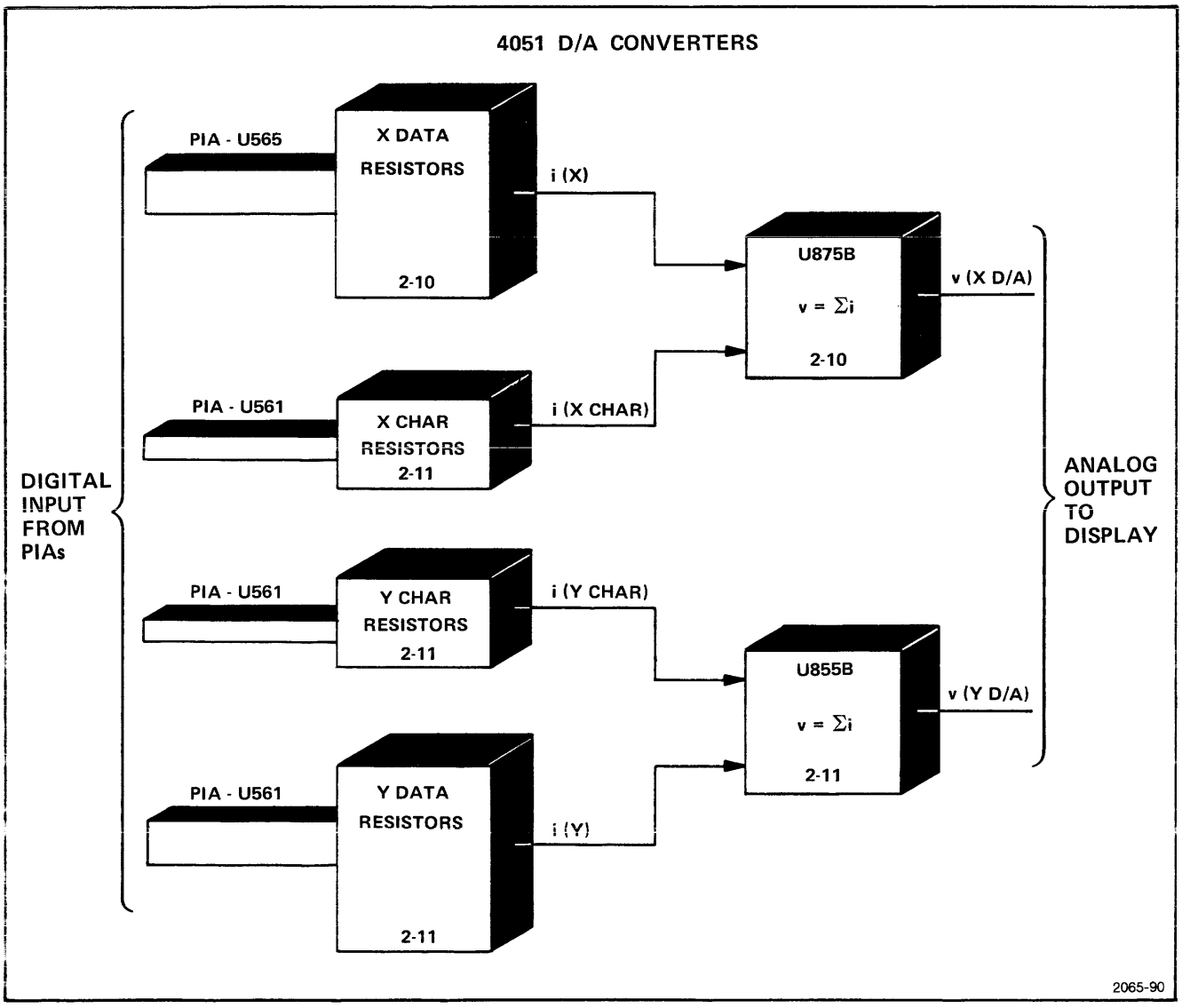


Fig. 6-15. Data and information flow through the X and Y digital-to-analog converters.

FILTER OPERATION

Filtering is provided by the distributed resistance and capacitance on the positive input of the operational amplifier (Fig. 6-16). See also 4051 schematic 2-12. When the FET (field effect transistor) switch is in the on state, the filter network is given a ground reference and is therefore able to provide exponenetial filtering of the D/A signal (Fig 6-17a). When the FET is off, the filter is disabled causing the output voltage to directly follow the input (Fig. 6-17b). Straight vectors can be drawn because both filters for the X and Y axes have matched exponential filtering characteristics.

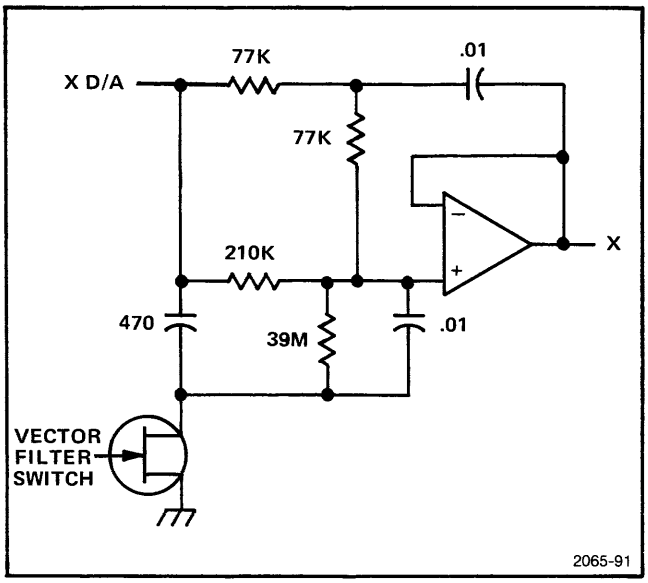


Fig. 6-16. Filter circuit to provide vector writing delay on the X axis.

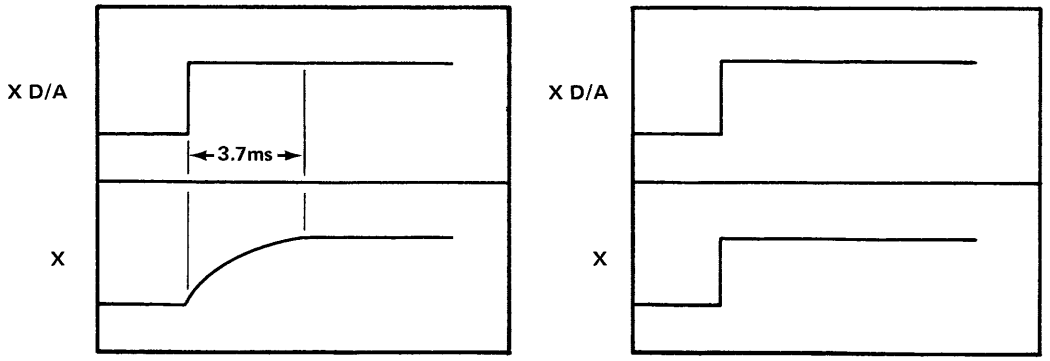


Fig. 6-17. Vector filtering response curves.

LONG VECTOR SENSE CIRCUIT

The long vector sense circuit on the 4051 schematics (page 2-12) is shown also in Fig. 6-18. For appropriate values and component numbers, refer to the schematic on the 4051 schematics page 2-12.

This circuit, during static operation, has an output voltage of near +5 volts. All transistors are in their off state. A voltage change of more than ±0.7 volts on either X D/A or Y D/A line will cause one of the four transistors to conduct and cause the output voltage to drop to zero. The active transistor will either ground the +5 volt line or the −12 volt line. If the −12 volt line is brought up to zero, the FET goes into conduction to lower the +5 volt line.

The output pulse for long vectors is only momentary due to the small .001 μF capacitors. Therefore, the output is saved by a nand gate flip-flop during a vector drawing period. The presence of a long vector causes the NOBURN CLK-0 signal to be disabled before its affect reaches the ZVECT-0 signal line. The ZVECT-0 signal is used to control the Z axis writing beam during a vector draw operation.

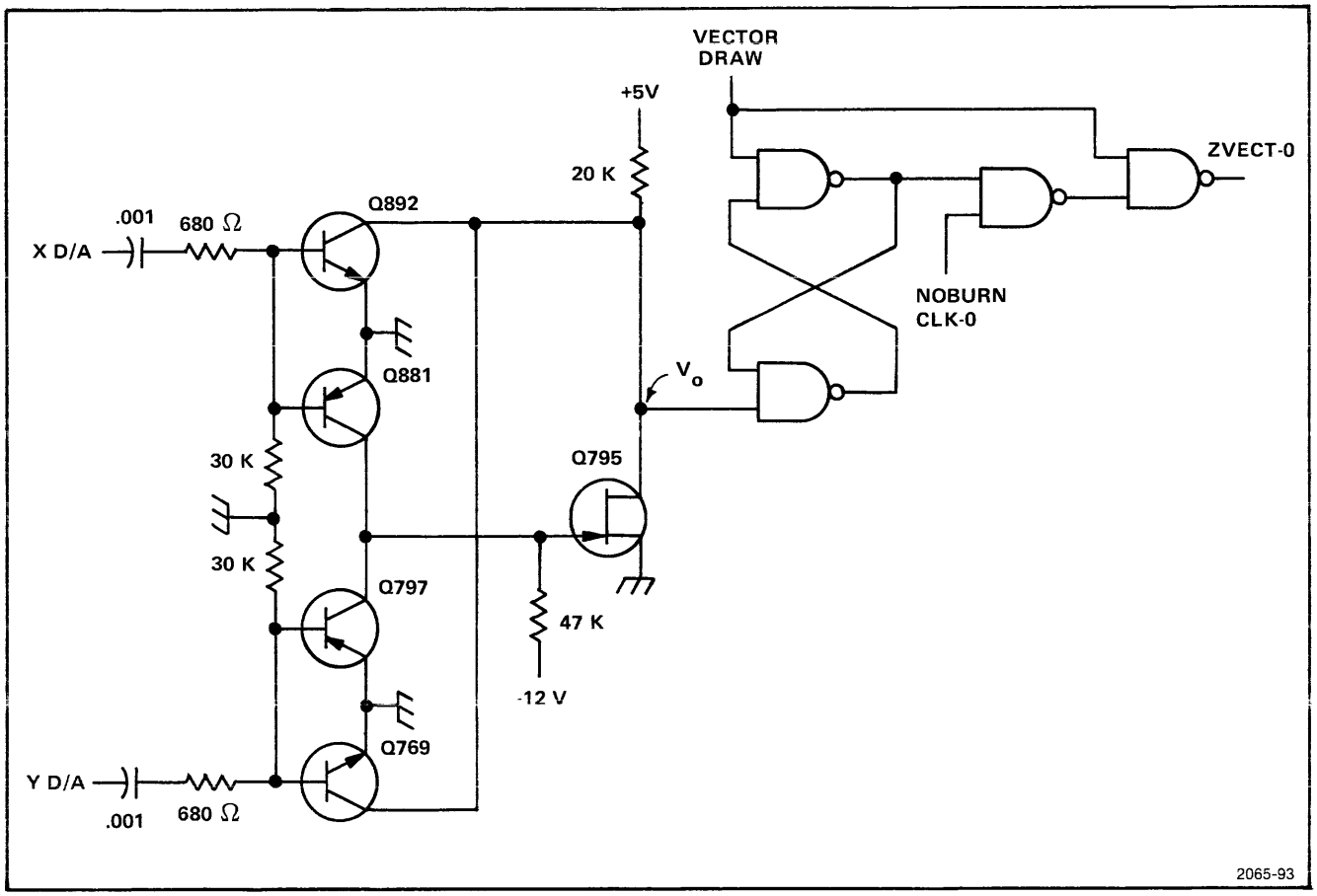


Fig. 6-18. Long vector sense circuit.

ALPHANUMERIC DISPLAY

Refer to the display control block diagram (Fig. 6-13). The display coordinate position is generated through the digital-to-analog converters (X DAC and Y DAC) and fed through the filter circuitry with the filtering disabled. A short time later, either SOT is activated to print a cursor refresh dot or ADOT is activated to print a stored character dot. The timers for cursor intensity and character intensity are adjustable by potentiometers accessible through the bottom of the assembled instrument.

OTHER DISPLAY CONTROL FUNCTIONS

Refer to the display control block diagram (Fig. 6-13). View mode is active when the VIEW signal is logically true. A 100 second view timer keeps the 4051 in View mode for 100 seconds following either the closure of the keyboard SHIFT key or the display of any new information on the crt. The View mode timer disables the Hold mode oscillator. During Hold mode operations, the VIEW signal is activated by a square wave having a 12.3% duty cycle. The screen goes dark, but the stored information is retained on the crt phosphors for later viewing.

Hard copy operations are initiated when COPY-0 goes low. During hard copy activity, DRBUSY becomes true to ensure the VIEW flood guns are on during the time a hard copy is being made.

Erasing the screen is accomplished by lowering the ERASE-0 line.

DISPLAY BOARD

There are two versions of the display board. Early instruments have discrete component implementation for the analog multiplexer, dynamic focus and geometry correction circuits. Later versions of the board incorporated these circuits into custom hybrid integrated circuits. The boards built with discrete geometry correction and dynamic focus circuitry are described here. Reading this information will also help give understanding to the internal operation of the new boards having special integrated circuits to provide the same analog correction functions.

The display board takes deflection and control information from the cpu board and processes these signals into a form usable by the direct view storage tube (DVST crt). The display board also uses signals from an optional Hard Copy Unit to copy the display information on the storage tube to a piece of paper.

Refer to the block diagram of the display board (Fig. 6-19) and crt schematic (Fig. 6-20). Display deflection amplifiers and other analog crt control circuitry are found on the 4051 display board. The display board schematics are found in Volume 2 of the 4051 Service Manual, 4051 schematics section, sheets 4-1 through 4-4. The display board is divided into three operational sections:

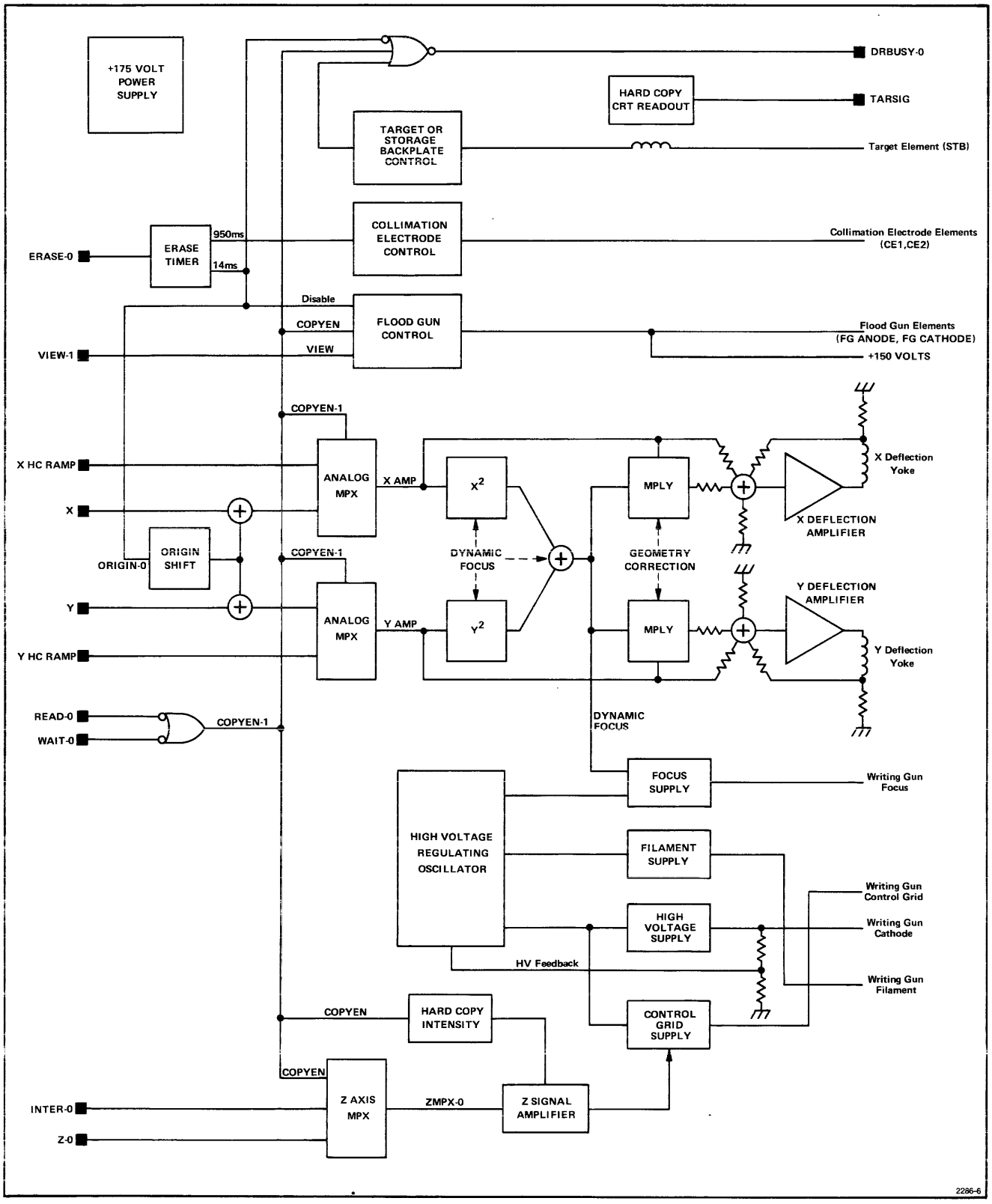


Fig. 6-19. Display board block diagram.

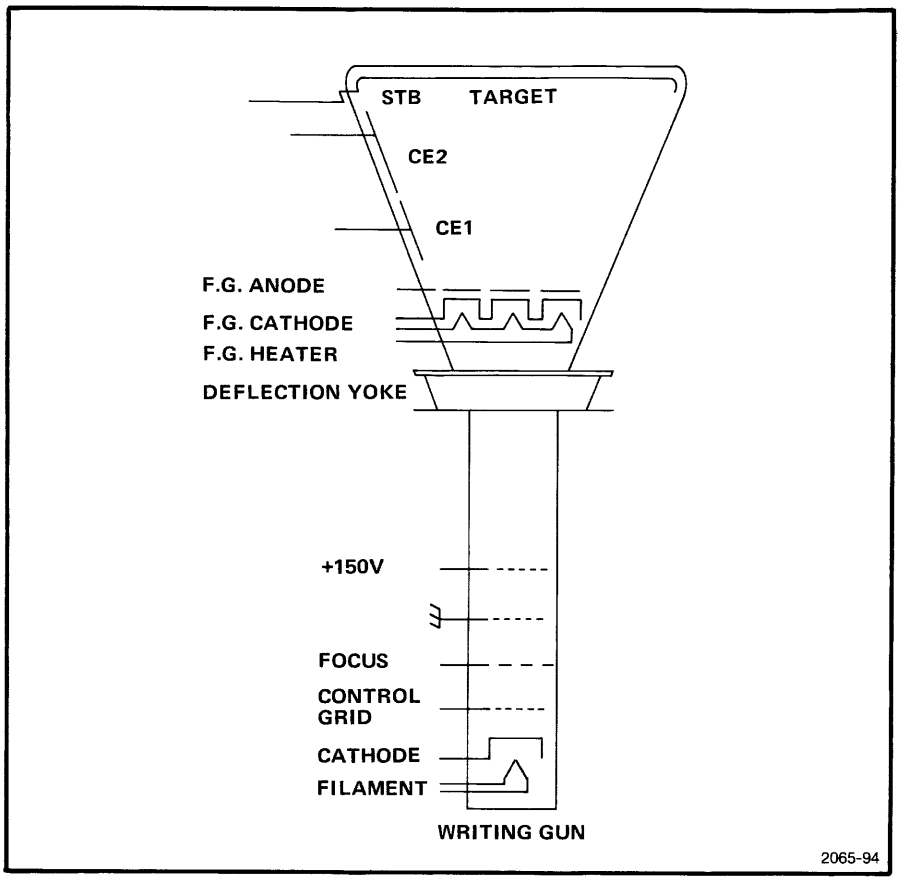


Fig. 6-20. Direct view storage tube (DVST) crt schematic.

1. Deflection Amplifier circuitry (sheets 4-1, 4-3).
2. Storage, View and Erase circuitry (sheet 4-2).
3. High Voltage and Focus circuitry (sheet 4-4).

Schematic sheets 4-5, 4-6 and 4-7 pertain to the modified version of display boards using customized hybrid circuits for much of the Deflection Amplifier circuitry.

Inputs to the display board are from display control circuitry on the cpu board. Outputs from the display board are to the various crt electrodes and to the deflection yoke.

Hard copy signals are also processed by the display board. Hard copy circuitry is activated only if an optional Hard Copy Unit has been purchased and is attached to the system. Hard copy operations, which produce a copy of crt display information, are described later.

Order of presentation will be in the following order of 4051 schematics: 4-1, 4-3, 4-2 and 4-4.

Refer to schematic page 4-1. Circuitry on this schematic provides the selection of hard copy deflection ramp signals (X HC RAMP and Y HC RAMP) if hard copy operation is activated, or the selection of display deflection signals (X and Y) form the cpu board during normal system operation. Hard copy operation is asserted by an optional Hard Copy Unit when either the READ-0 or WAIT-0 lines are brought low, thus activating the COPYEN-1 signal. The presence of COPYEN-1 being high causes the outputs of Q552 and Q551 to be high. These high level voltages (approximately +15 volts) cause the X and Y amplifiers U777A and U577A to go into saturation and the outputs of U777B and U577B to control the X AMP and Y AMP deflection lines. During standard operation, COPYEN-1 is low to cause the X and Y amplifiers to have output control of the X AMP and Y AMP deflection lines. The BIAS line from schematic 4-3 causes transistors Q674 and Q473 to be constant current sources, each sinking approximately 4.5 milliamperes of current. On schematic sheet 4-5, hard copy selection is performed by U585.

Detailed hard copy operations are described later in this text.

Origin shift circuitry (sheet 4-1) consists of a 3-bit binary counter and a small-range digital-to-analog converter to supply minute amounts of current to the X axis and Y axis deflection signals. The counter is incremented each time the crt is erased. At the beginning of each page erasure, the ORIGIN-0 signal goes low for approximately 14 milliseconds. On schematic sheet 4-5, origin shift functions are performed by U585.

Refer to the 4051 schematic sheet 4-3. The deflection amplifier circuitry can be logically separated into three circuit sections: dynamic focus, geometry correction, and deflection amplifiers. In this circuitry, the X AMP and Y AMP signals are the primary deflection signal components. The other signals provide for focus and geometry correction.

The DYNAMIC FOCUS signal provides a focus correction component to the focus circuitry on schematic sheet 4-4. The DYNAMIC FOCUS signal compensates for magnetic deflection effects and crt geometry effects on writing beam focus. On schematic sheet 4-5, dynamic focus and geometry correction components are generated by U485.

Outputs of the geometry correction multipliers provide writing beam deflection correction to compensate for magnetic deflection and flat crt target geometries, thus eliminating a pin-cushion effect. The pin-cushion effect is likened to a rectangle drawn on the crt that has rounded sides instead of straight sides.

The deflection amplifiers are high-gain current amplifiers designed to provide the necessary current in a deflection coil to establish the proper magnetic field for writing beam deflection. The magnetic field produced is directly proportional to the current in the deflection coil or yoke.

DISPLAY BOARD BLOCKS

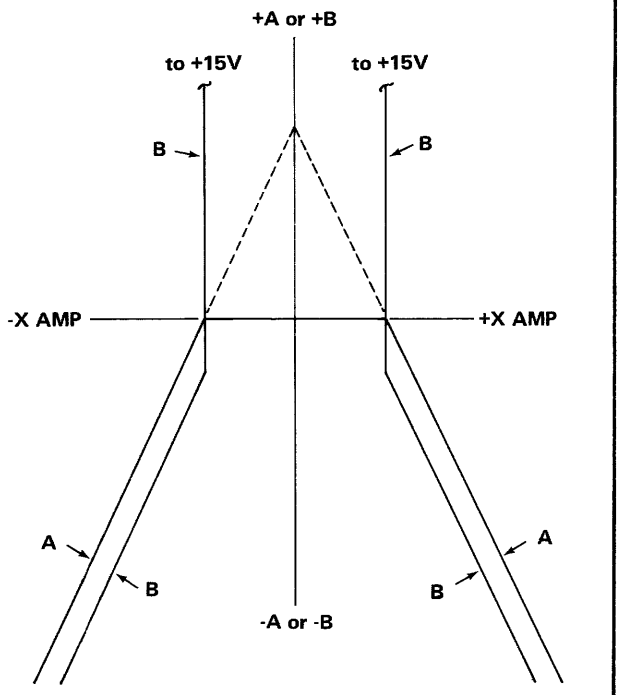
Refer to schematic sheet 4-3. Dynamic focus circuitry consists of absolute value amplifiers ($|X|$ and $|Y|$) followed by multiplier circuits for X^2 and Y^2 again followed by a current summing amplifier.

Absolute Value Amplifiers

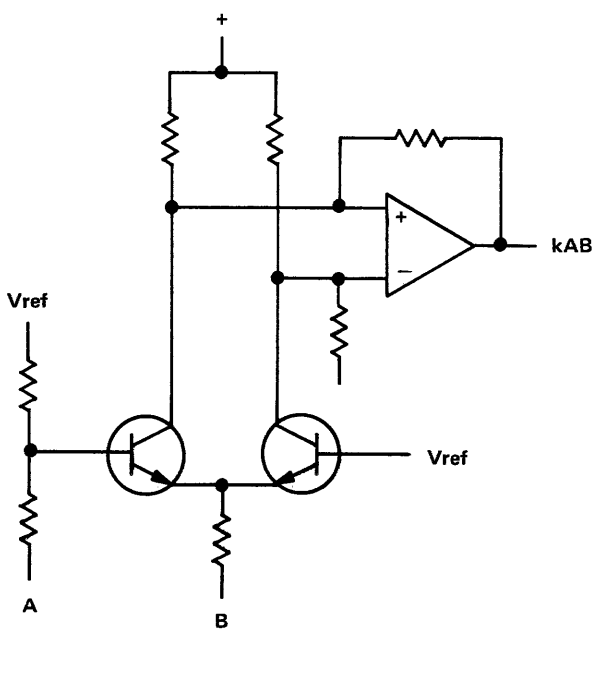
The X amplifier consists of U496A and the associated resistors and diodes. A chart of |X| voltages versus the X AMP voltage is given in Fig. 6-21. When XAMP is less than 2 volts, both CR593 and CR597 have forward bias, the U496A amplifier is almost a unity gain linear amplifier with a positive offset voltage.

In the region between −2 volts and +2 volts on X AMP, a positive feedback voltage at the anode of CR395 is required for regulation of U496A. Since there is no voltage source above signal ground at the anode of CR395, the diode looses its forward bias causing the negative amplifier input to be less than the positive input, thus causing the amplifier output to go into positive saturation.

When the X AMP signal is greater than 2 volts, R592 and R493 provide a negative unity gain amplifier biased at 0.9 volt at their junction. CR597 is reverse biased.



Absolute value amplifier voltages. Output voltages A and B with respect to input voltage XAMP.



A typical transconductance multiplier circuit.

2065-95

Fig. 6-21. Transconductance amplifier for dynamic focus and geometry correction.

X^2 and Y^2 AMPLIFIERS

The X^2 amplifier is a transconductance multiplier circuit composed of Q491, R482, R483, and R485. A typical transconductance multiplier circuit is shown in Fig. 6-21. The difference in current through the transistor collectors is equal to the scaled product of the input voltages (A and B) with respect to the voltage reference, provided that the amplifier is operated in its active region. In the case of the X^2 amplifier, A and B are essentially the same signal separated only be a diode voltage drop. During the portion of the X AMP voltage curve when B is near +15 volts, the X^2 amplifier has a differential output of zero.

Currents from the X^2 and Y^2 amplifiers are added at the transistor collectors. The total is converted to a voltage ($X^2 + Y^2$) at the output of U381A. This voltage is used for DYNAMIC FOCUS and also as a component for geometry correction of writing beam deflection.

Geometry Correction Multipliers

Geometry correction multipliers are also transconductance multipliers. These multipliers take the $X^2 + Y^2$ voltage on the emitters of U296A and U296B, multiply this voltage by a deflection voltage (X AMP or Y AMP) and add the result to the inputs of the deflection amplifier circuits.

Deflection Amplifier

The X deflection amplifier and Y deflection amplifier have identical operation. Inputs to the operational amplifier (U184A) represent the weighted sum of all parameters incorporated into writing beam deflection. R281 passes the primary deflection signal X AMP. Resistors R282 and R287 provide the geometry correction. The X POS adjustment provides a position bias to U184A. And the X GAIN adjustment establishes the feedback voltage magnitude from the coil current sensing resistors. Output from U194A drives a complementary pair of cascaded current amplifiers.

In the cascaded amplifiers, Q186 is a constant current source that provides 8.8 milliamperes of current. Activation of power transistors is dependent upon current supplied by Q84. Current greater than 8.8 milliamperes causes Q1069 to go into conduction. Current less than 8.8 milliamperes causes Q1074 to conduct. Q1069 forces current into the X deflection coil. Q1074 draws current from the same deflection coil.

Storage And Erase Control Circuits

Refer to the 4051 schematic sheet 4-2. The backplate control, collimation control, and flood gun control circuits are switchable high voltage sources. Depending upon the state of a logic input signal, the output voltage acquires one of two stable voltage levels. The target or storage backplate control circuitry has a 10 μF timing capacitor that is used during the crt erase cycle causing the target (STB) voltage to be slowly restored.

The hard copy crt readout amplifier circuit senses a current change in the target electrode by amplifying a voltage developed across transformer windings. The amplified signal is then filtered for noise. The result triggers a 400 nanosecond monostable device that provides a clean digital pulse back to a Hard Copy Unit.

+175 Volt Supply

The +175 volt supply uses the +15 volt supply for a voltage reference. A voltage divider using 130K and 6.19K resistors provides an 8 volt feedback voltage to U445 thus regulating the supply.

Erase Timing And CRT Voltage Levels

Erase timing is controlled by the erase timer monostable devices. Refer to the erase timing diagram of Fig. 6-22. The first monostable provides a 14 millisecond pulse that is used to write up the screen by increasing the flood gun current. The 950 millisecond monostable is then triggered to erase the screen and restore the crt operating level without again writing the phosphors. If the target voltage increases too fast, the face of the crt will go to the bright written state.

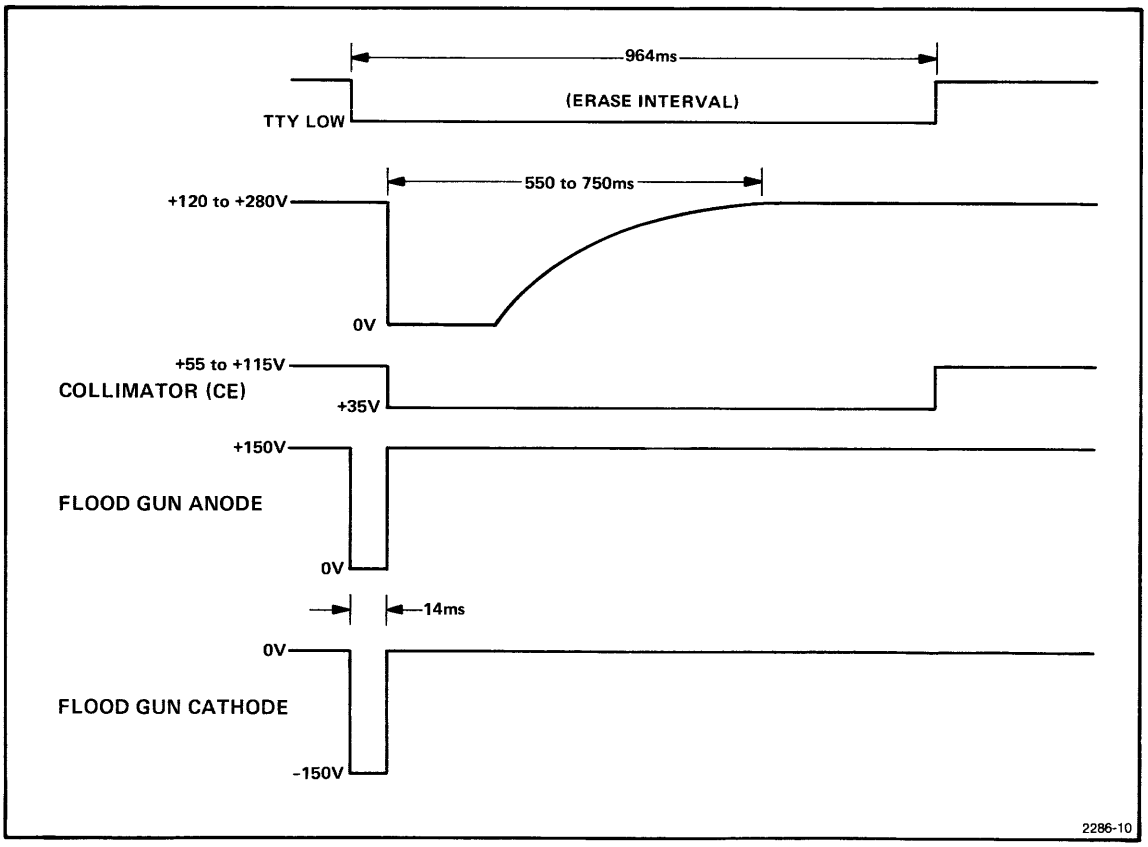


Fig. 6-22. Erase timing and voltage waveforms.

The crt operation level, as established by the target or storage backplate control circuitry, causes crt write-up or fade-positive effects if set too high. Information dropout occurs if the crt operating level is set too low. The operating voltages for the particular crt in the instrument is specified on a service tag within the instrument. In the case of a new crt, the operating voltages may be specified in the accompanying shipping literature.

Collimation operating level, as established by the collimation control circuitry, determines the linearity of flood gun intensity across the face of the crt. If the voltage is too high, the outer portions of the crt will tend to write up and excessive display power will be used. If the voltage is too low, the center of the crt will tend to write up and information on the outside edges will tend to show information dropout.

Target or Storage Backplate Control

Normal output of inverter U561A is grounded. During the erase cycle, the output goes to an open collector state placing the positive timing capacitor lead at +9 volts through diode CR450. During normal operation, the voltage across the timing capacitor (C353) is approximately zero. During the erase cycle, the positive side of the capacitor is lifted to +9 volts and the negative lead charges toward zero through R352. Q251 buffers the voltage from the timing circuit and provides the necessary current to the voltage regulating circuitry. At the end of the erase cycle, the positive capacitor lead is brought to zero and the negative lead discharges to ground through diode CR350.

The erase cycle beginning causes about a +5 volt change on the OP LEVEL adjustment resistor causing Q143 to turn on hard, grounding the STB electrode on the crt. The STB electrode remains grounded until the timing voltage through Q251 drops sufficiently for regulating feedback (through R148) to again cause a voltage rise — Q143 again biased in the active region.

Two transistors are required to drive the STB line. They are biased in such a way that their electrical breakdown voltages are not exceeded when reaching for the +320 volt unregulated supply.

Collimation Control

Normal operating range is established by the CE adjustment. Q361 is normally off and Q362 is normally on.

During the erase cycle, Q361 turns on and bypasses the CE adjustment. As a result, the output voltage on CE1 and CE2 drops to +35 volts.

During hard copy operations, Q362 turns off forcing CE1 and CE2 to go towards +250 volts. Since the voltage on the +185 volt unregulated supply is all that is available, that supply voltage becomes the voltage at CE1 and CE2.

Flood Gun Control

Normal operation has the VIEW-1 signal at a high voltage level. This causes both Q459 and Q366 to be off allowing the flood gun anode to have a voltage of +150 volts regulated by zener diodes. The flood gun cathode is near zero.

Hold mode operation causes the VIEW-1 signal to oscillate between TTL true and TTL false voltage levels. When VIEW-1 is in the low voltage state, both Q459 and Q366 are turned on, thus placing the flood gun anode voltage at −20 volts. Since the cathode voltage remains near zero, the flood guns are turned off.

During erase operations, the transistor Q364 is turned on for 14 milliseconds. This grounds the positive lead of the 50 μF capacitor and forces the negative lead to −150 volts. This increases the voltage potential between the flood gun electrodes and the crt TARGET (STB) by 150 volts. This increased potential causes the flood guns to write the crt to saturation brilliance due to increased flood gun current.

HIGH VOLTAGE CIRCUITS

The high voltage circuits are shown on the 4051 schematic sheet 4-4 in Volume 2 of the Service Manual.

The high voltage circuits provide voltages for the focus electrodes and writing gun electrodes of the crt. The writing gun elements operate at −4,000 volts dc. Power to the high voltage circuits is generated using a flyback transformer and driven by a regulated blocking oscillator.

Z axis control is provided by coupling a voltage through a capacitor to turn on the writing beam. During normal operation the writing beam is biased off.

High Voltage Regulator Oscillator

The high voltage regulator oscillator is a regulated blocking oscillator. A typical blocking oscillator circuit is provided by transistor Q432 and transformer windings 5-4 and 6-3. The transformer operates as a flyback transformer. The oscillator transistor (Q432) momentarily forces current through the primary winding 5-4 and then opens to provide a high impedance to the established current. Winding 6-3 provides positive feedback for sustained oscillations. Regulating voltage feedback is provided by a voltage divider in the high voltage supply. Phase control feedback is provided at winding 2-1. The feedback control signals are then amplified by a series of transistors and applied to the base of the oscillating transistor for duty cycle control. This duty cycle control provides for the necessary voltage regulation.

Focus Supply

The focus supply consists of an adjustable gain amplifier for dynamic focus and an isolated focus supply from the high voltage flyback transformer. The isolated supply uses as its voltage reference, the output of the dynamic focus amplifier. A fixed negative value as determined by the FOCUS adjustment is subtracted from the dynamic focus amplifier output before driving the crt focus electrode. The gain of the dynamic focus amplifier is determined by the DYNAMIC FOCUS adjustment.

Filament Supply

Voltage reference for the writing beam filament supply is the −4,000 volt cathode voltage. The filament supply therefore provides alternating current to the filaments at a voltage centered about the high voltage cathode.

High Voltage Supply

The source voltage for the high voltage supply is winding 10-2 of the flyback transformer. This ac voltage is fed through a voltage doubler network of capacitors and diodes. A typical voltage doubler network is shown in Fig. 6-23. High voltage feedback bias is determined by the HV ADJ resistor and the associated resistance network. The result is fed back to the high voltage oscillator to establish the cathode voltage at −4,000 volts dc.

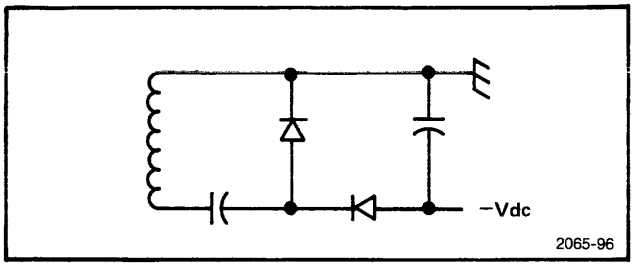


Fig. 6-23. A typical voltage doubler network.

Control Grid Supply

A simplified diagram of the control grid supply is shown in Fig. 6-24. The schematic containing the circuitry is the 4051 schematic sheet 4-4. The supply voltage driving the rectifier circuitry of the control grid supply is a clamped waveform as shown in Fig. 6-25. The 1.2 megohm resistor enables the clamping process to occur by limiting available current from the transformer. The Z axis voltage is normally at the off state. The BIAS voltage is adjusted to ensure there is

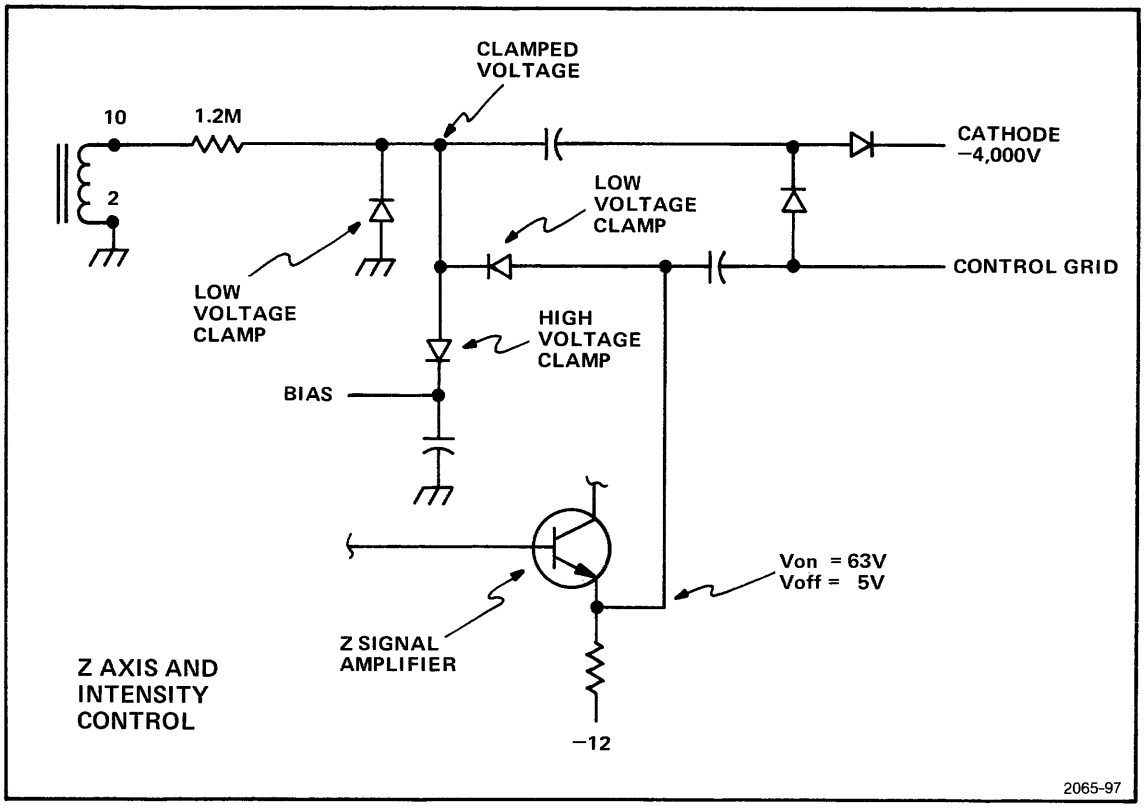


Fig. 6-24. Z axis control grid circuitry used to regulate the writing beam intensity.

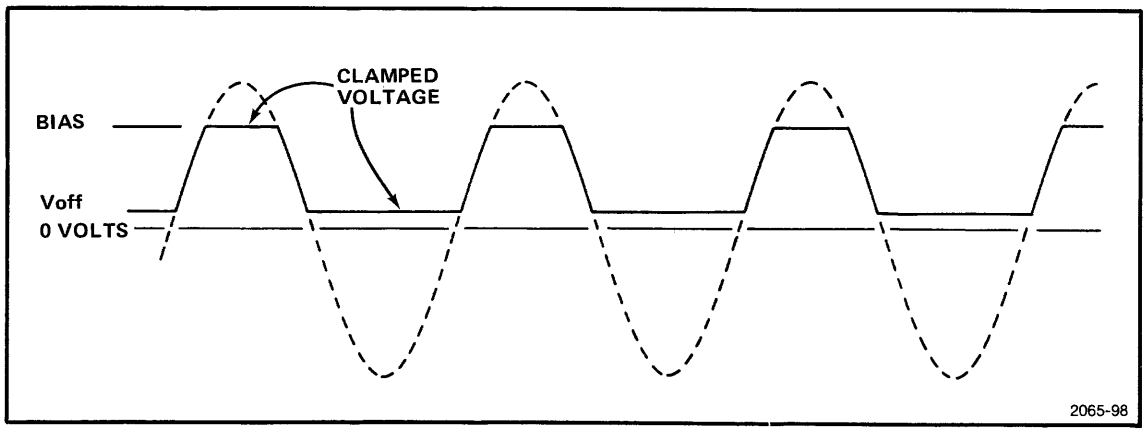


Fig. 6-25. Waveform used to establish the crt control grid voltage level.

enough negative potential on the control grid to keep the writing beam turned off when the Z axis is not active. When the Z axis turns on, a positive voltage change is coupled through a capacitor to the control grid, thus causing writing beam current in the crt.

Intensity Control and Z Signal Amplifier

Refer to the 4051 schematic sheet 4-4. Intensity control circuitry is a regulated voltage source having reference to the +175 volt regulated power supply. Output of the supply at transistor Q231 is normally at 63 volts. During hard copy operations, the voltage is less as determined by the HARD COPY INTENSITY adjustment.

The Z signal amplifier normally has an output of 5 volts. The Z MPX-0 signal is at a TTL high voltage. When Z MPX-0 goes low to turn on the writing beam, Q123 turns off and the current established in the coil L27 causes the output transistor voltage to immediately assume the voltage established by the intensity control amplifier, normally 63 volts.

HARD COPY OPERATIONS

Hard copy signals and their influence are shown in the block diagram of Fig. 6-26. The related schematics are found in the 4051 schematics in Volume 2 of the 4051 Service Manual. Figure 6-19 in this section references the appropriate schematic diagrams.

Hard copy operations can be started any of three ways:

1) Press the MAKE COPY button on the keyboard.
2) Execute a COPY command.
3) Press the COPY button on the Hard Copy Unit.

In any case, the MAKE COPY-0 signal is asserted. When an attached Hard Copy Unit receives the MAKE COPY-0 signal, it issues a READ-0 or WAIT-0 to the calling device. READ means that the Hard Copy Unit is busy making a copy of the display. WAIT means that the Hard Copy Unit has a multiplexer option and is currently busy making a copy from another display device.

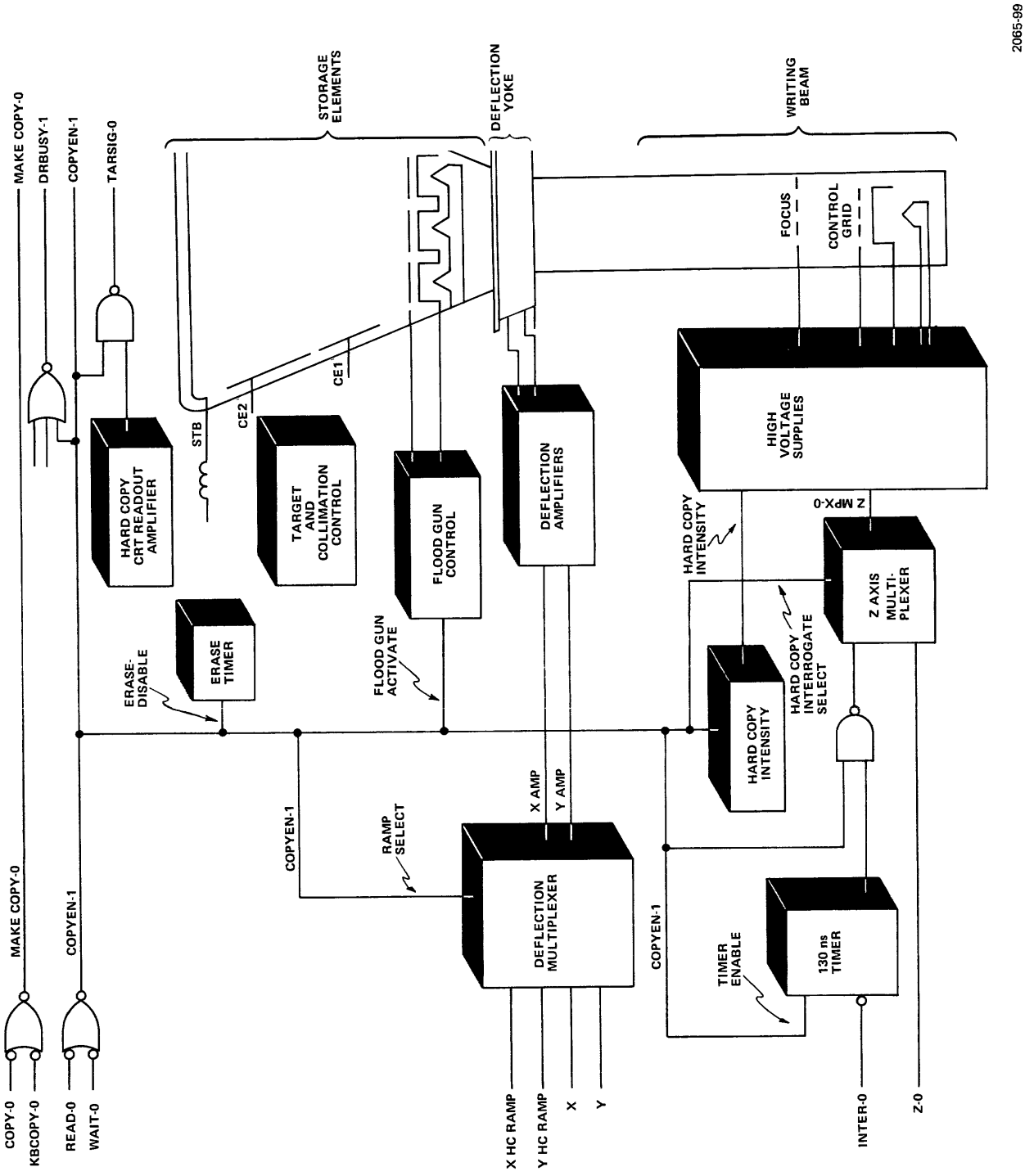


Fig. 6-26. Hard copy circuitry block diagram.

Upon receiving READ-0 or WAIT-0 from a Hard Copy Unit, the copy enable (COPYEN-1) siganl is activated — sent high. The COPYEN signal sends a display busy condition (DRBUSY) back to the microprocessor. It also prevents the display from being erased. It causes the HC RAMP signals to provide the writing beam deflection voltage. It establishes a writing beam intensity used for display interrogation pulses. And it enables Z axis display interrogation pulses (INTER-0) to be received from the Hard Copy Unit.

Hard copy information is read from the face of the crt by means of a pulsed writing beam of low intensity. Whenever the writing beam touches the target or storage backplate (screen) of the crt, there is an increase in current. This current is sensed as a differential voltage on the output of a pulse transformer and amplified by the hard copy crt readout amplifier circuitry. Target signal information is then placed on the TARSIG signal line. Bright display areas generate more target current than areas that are not written; therefore the crt readout amplifiers can discriminate between bright and dark areas of the display.

The THRESHOLD adjustment determines the signal level used to discriminate between bright and dark portions of the crt.

TAPE UNIT

The block diagram of Fig. 6-27 shows the tape control interface lines at the peripheral interface adapters. Schematic numbers are given in parentheses to reference the source and receiving circuits. Figure 6-28 illustrates the data recording format on 4051 magnetic tape cartridges with related parameters in Table 6-3.

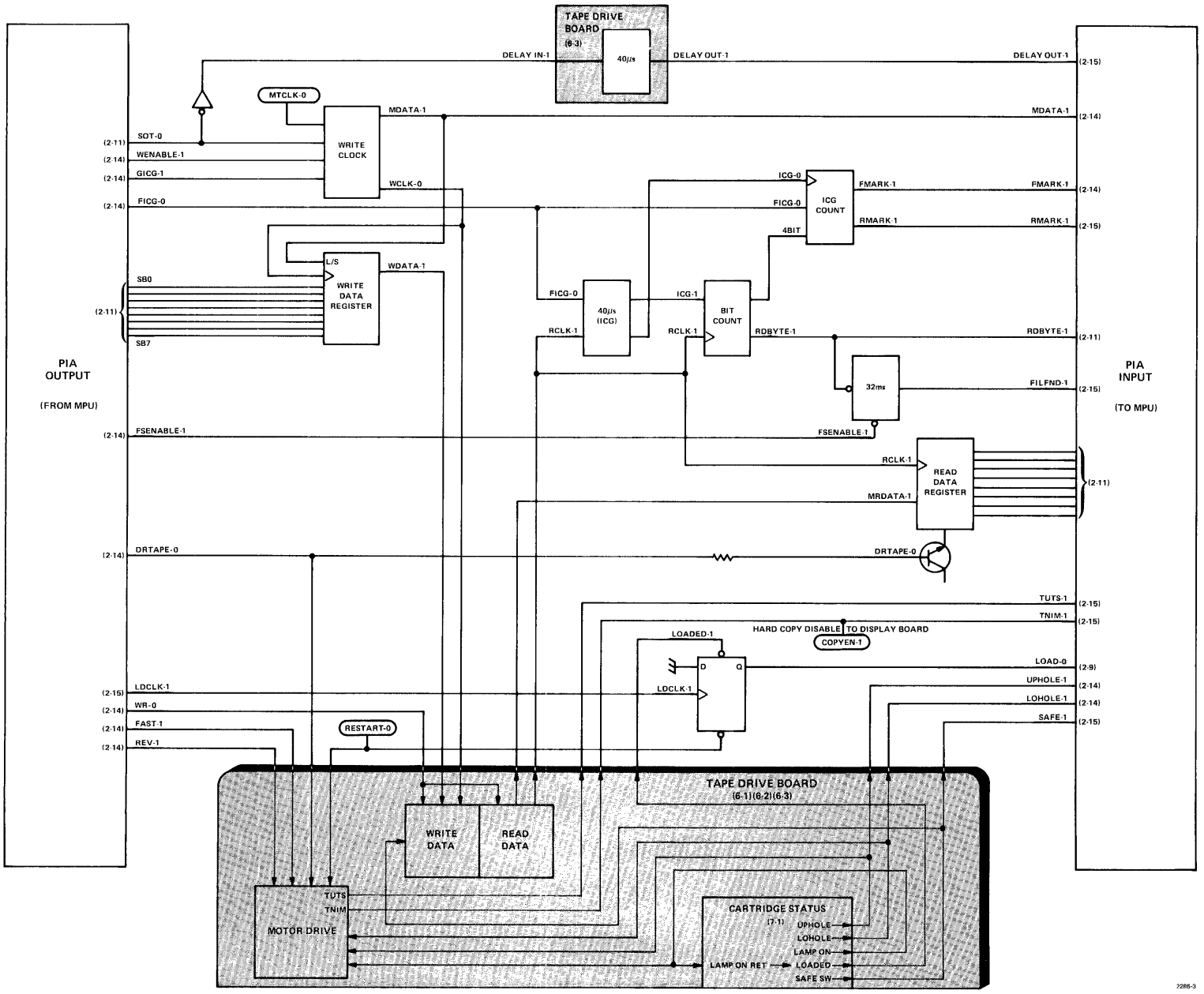


Fig. 6-27. Block diagram of the 4051 tape drive control circuitry.

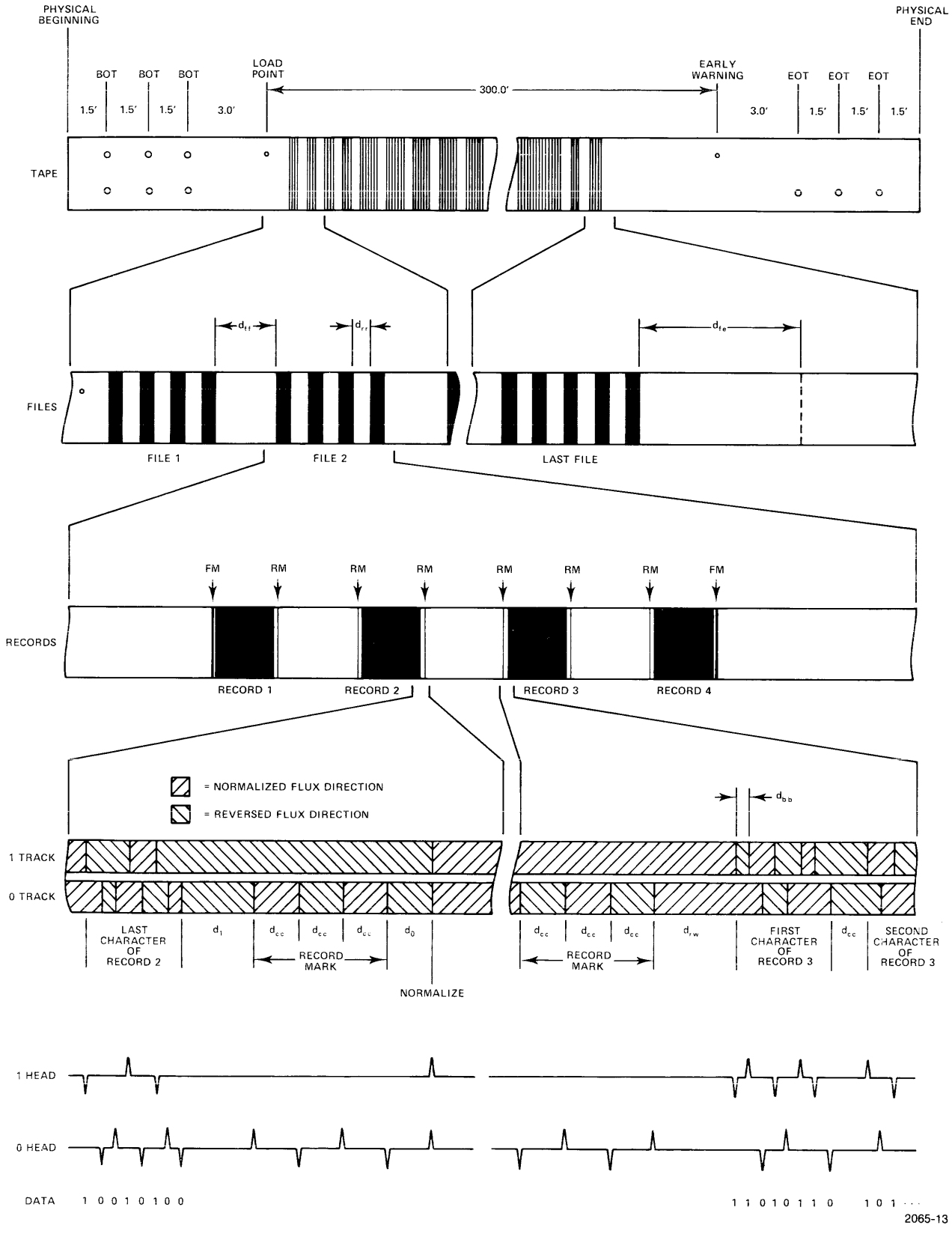


Fig. 6-28. Magnetic tape recording format.

Due to limited power, the display deflection circuitry should not be active while the tape is in motion. A COPYEN-1 signal is produced to inhibit all hard copy activity at the display board during tape drive operations. Before the tape motors are started, 4051 firmware places the display writing beam near the center of the screen and later restores the beam position after tape operations are complete.

Data to the tape drive is bit-serial. The write enable line WENABLE-1 triggers the write clock circuitry to load the write data register followed by a timed serial shift for 8-bits of data output to the Tape Drive board. The parallel data (SB0 through SB7) comes from the Y axis D/A peripheral interface adapter (PIA).

Refer to schematic 2-14. Data to be written to the tape is loaded into a shift register (write data register) and then shipped bit-serial to the tape head circuitry. WDATA-1 is this serial data. The write clock circuitry is driven by the MTCLK-0 signal generated from the system clock circuits. Write clock outputs are (TP) WCLK, WCLK-0, and MTCLK-0 (see Fig. 6-29). Shift register data is latched on the positive-going edge of MDATA-1; the shift register is then shifted eight times by WCLK-0, once for each positive edge. The bit-serial data goes out over the WDATA-1 line.

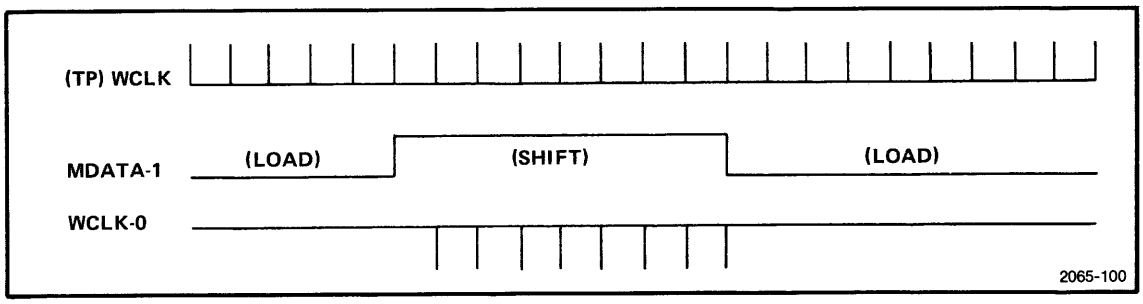


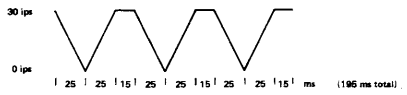
Fig. 6-29. Timing signals for writing data to tape.

Table 6-3

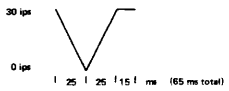
MAG TAPE FORMAT SPECIFICATIONS

Characteristic	Symbol	Distance				Time (at 30 ips max.)			
		min.	nom.	max.	units	min.	nom.	max.	units
erase after last file	d_{fe}	0	-	-	in	300	-	-	ms
interfile gap	d_{ff}	3.17	3.60	4.03	in	172	195	218	ms[a]
interrecord gap	d_{rr}	1.06	1.20	1.34	in	57	65	73	ms[b]
read-to-write gap	d_{rw}	4.35	8.18	12.00	mil	145	272	400	μs
first inter-character gap after record data	d_{1}	1.50	-	3.90	mil	50	-	130	μs
intercharacter gap	d_{cc}	1.50	2.25	3.00	mil	50	70	100	μs
normalizing gap, after EOR mark	d_{o}	-	-	3.00	mil	-	-	100	μs
interbit gap	d_{bb}	.57	.65	.73	mil	19	21	24	μs

[a]Speed is not constant at 30 ips during the interfile gap:



[b]Speed is not constant at 30 ips during the interrecord gap:



Refer to schematic 2-15. The read clock signal, RCLK-1, is the result of timing data recorded on the tape. This read clock signal shifts bit-serial data into the read data shift register. The register output is in 8-bit parallel form for PIA usage.

The read clock timing circuits interrogate the RCLK-1 timing sequences to decode end of record (RMARK), end of file (FMARK) and beginning of data information. The monostable device set at 40 microseconds times out if a data gap equal to or larger than an intercharacter gap is encountered. The bit counter places the RDBYTE-1 signal low during data read operations. After the last data byte is loaded into the read data register, RDBYTE-1 again goes high. The ICG counter circuit interprets four consecutive intercharacter gaps as a record mark and eight intercharacter gaps as a file mark.

Finding file boundaries (interfile gaps) when the magnetic tape drive is operating at high speed is the responsibility of a 32 millisecond monostable device. The monostable device is reset by FINDCLK-0 and triggered by RDBYTE-1. The output, FILFND-1, goes high after the 32 milliseconds elapses.

To generate an intercharacter gap, GICG-1 is first made high, afterwards SOT-0 is sent low and high again. SOT-0 also activates a DELAY IN signal that passes through a 40 μs monostable device to produce DELAY OUT. DELAY OUT can be used by firmware as a general purpose timing signal.

Refer to Fig. 6-27 for schematic references and a block diagram showing an overview of tape drive operations. The tape read and write circuits of the tape drive board are shown in Fig. 6-30. The detailed schematic diagram is sheet 6-1 of the 4051 schematics in Volume 2 of the Service Manual.

Write operations are performed when the WR-0 line goes low (Fig. 6-30). This causes the diodes on the inputs of the flux sensing amplifiers to become forward biased. Write current is then forced through the tape heads at a direction determined by the J-K flip flops and their output gates. Data representing a one causes the J-K flip flop on the number one track to change state, thus forcing a flux reversal on that track. Data representing a zero causes the other J-K flip flop to force a flux reversal on the zero track.

There are several factors that can prevent write current from being established on the tape heads. One factor occurs when the SAFE SW signal is low meaning that the tape is write protected. Another is that RESTART-0 is low to prevent tape data from being changed when the 4051 is being powered up or restarted.

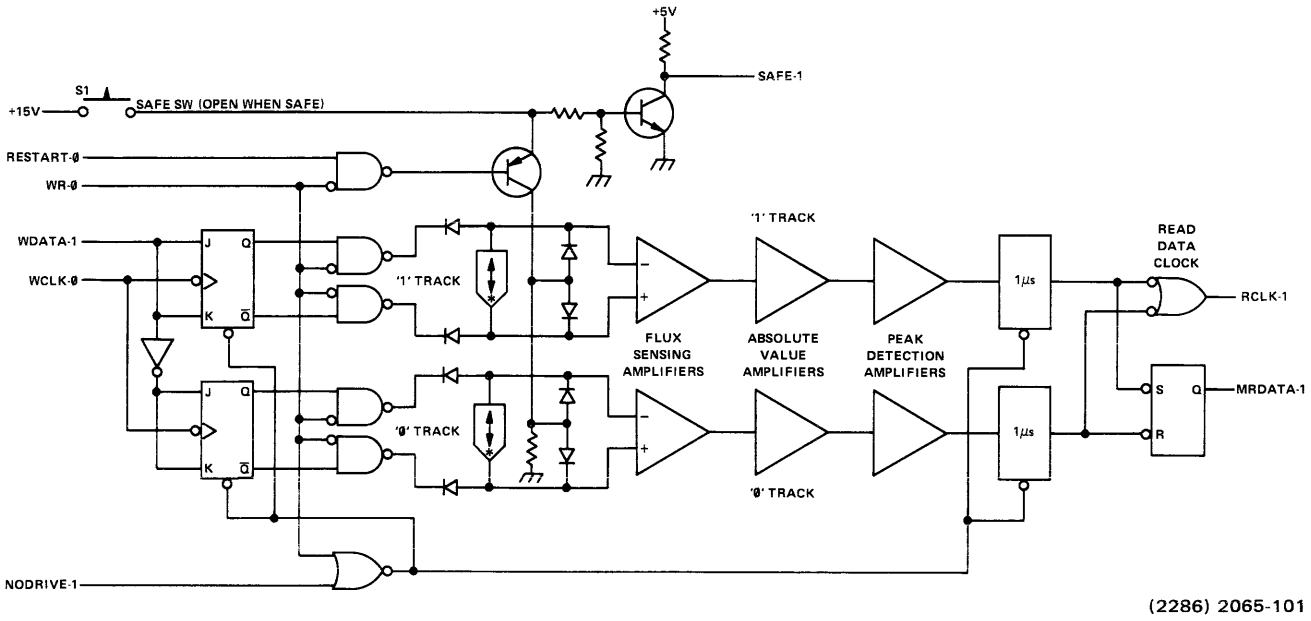


Fig. 6-30. Tape drive read/write circuits on the tape drive board.

Read operations occur when the WR-0 signal is high causing the writing diodes to have reversed bias. The diodes on the inputs of the flux sensing amplifiers have their anodes at zero. Flux changes on the magnetic tape cause a voltage to be generated at the tape heads. This voltage is then amplified by the flux sensing amplifiers and passed through absolute value amplifiers in order to activate the peak detection amplifiers for data detection (Fig. 6-31). One microsecond monostable devices are triggered by the output from the peak detection amplifiers. These one microsecond pulses are the interface to the world of digital electronics by generating a read clock pulse, RCLK-1, each time a flux reversal is encountered on the tape and clocks an R-S flip flop to select the associated one or zero data bit (MRDATA-1).

Some operations prohibit read operations by preventing the one microsecond monostable devices from being triggered. One occurs when there is no command available to cause tape motion. Another occurs when WR-0 is low to perform a write operation.

The peak detection amplifier operation is illustrated in Fig. 6-31. The schematic is sheet 6-1 of the 4051 schematic set. During the positive rise of input voltage, the capacitor charges through R1 as illustrated in part a. When the input voltage starts to drop, the capacitor charging diode becomes reversed causing an equivalent circuit shown as part b. As the input voltage continues to drop, the voltage at the junction of R2 and R3 drops below the stored capacitor voltage. This causes the output voltage to go negative and the equivalent circuit changes to that shown in part c. The capacitor in part c discharges through R1 until the input voltage starts to rise, at which time the discharge diode becomes reverse biased. The equivalent circuit again becomes that of part b. As the rising input voltage forces the junction of R2 and R3 above the capacitor voltage, the output again goes positive and the equivalent circuit again becomes that of part a.

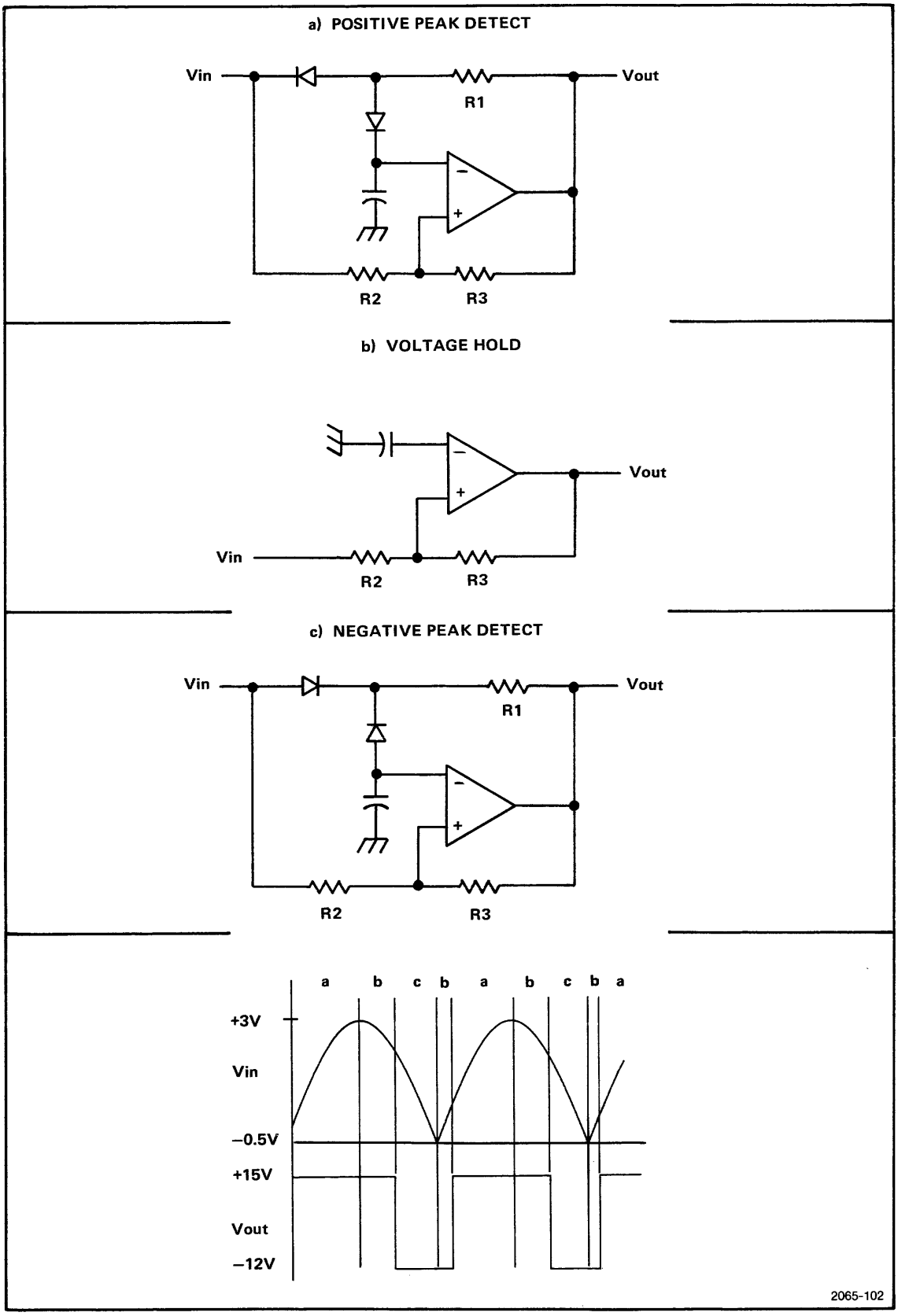


Fig. 6-31. Peak detection amplifier operation.

Refer to Fig. 6-32 and schematic sheet 6-2. The emergency stop circuitry removes the drive enable signal under the following conditions:

1) When the tape is in reverse and the beginning of tape is encountered.
2) When DRTAPE-0 goes high under microprocessor control.
3) When the tape cartridge is removed.
4) When the status lamp burns out.

The rate amplifier is a saturating amplifier having an output voltage clamped with zener diodes at +8 volts or −8 volts or regulated output near zero. For ramp generation, the zener regulated voltages provide a constant input to the integrator until the ramp has reached its excursion limit. Feedback from the integrator forces the rate amplifier output to zero when the proper ramp (motor speed) voltage is reached. RAMP-1 voltage is approximately 1 volt for each 10 inches per second of tape velocity.

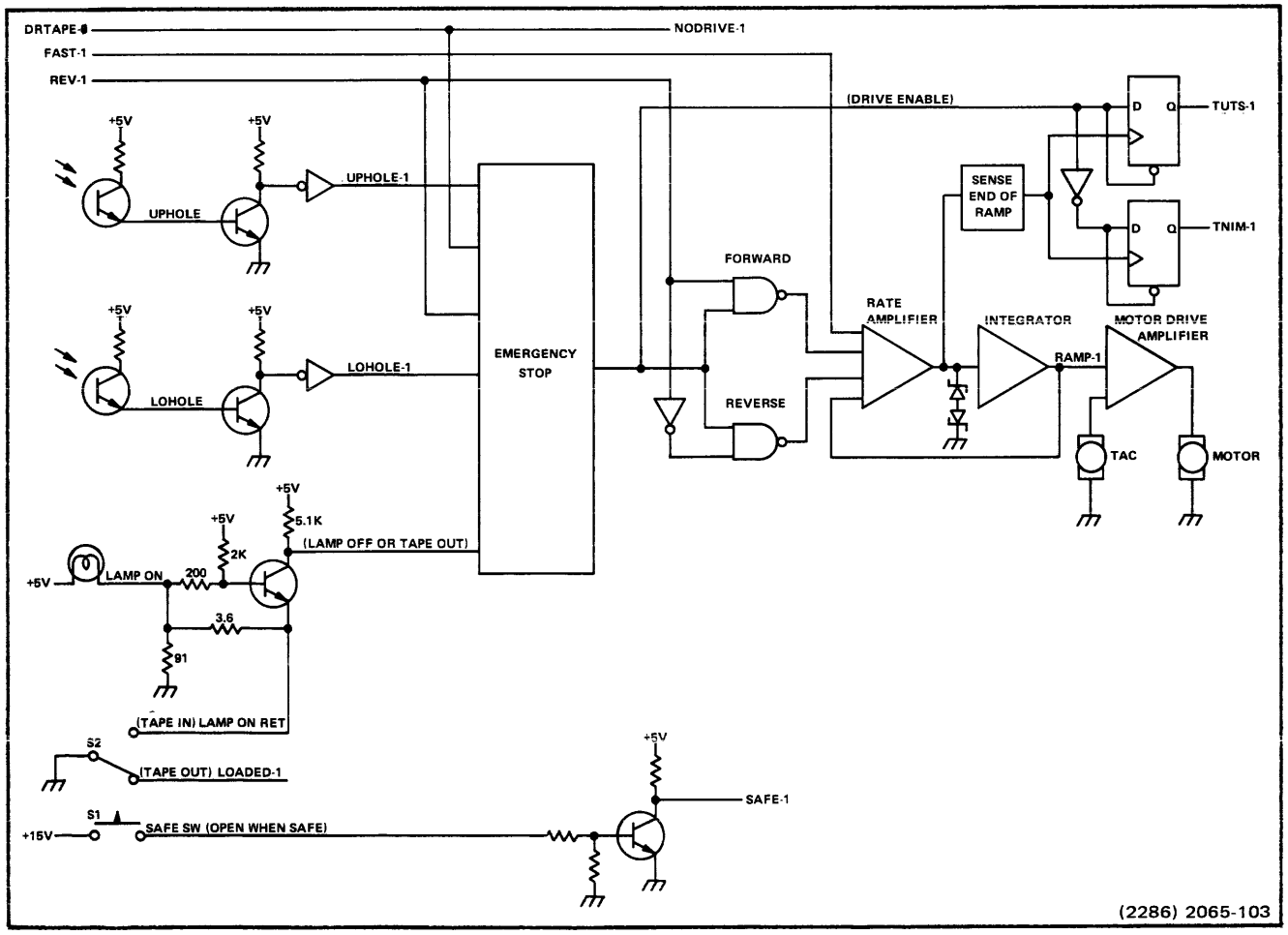


Fig. 6-32. Block diagram of tape status and motor drive circuitry.

Output of the rate amplifier is also conditioned to trigger a 15 millisecond monostable device at the termination of a ramp voltage. This provides a settling delay time before either the tape-up-to-speed (TUTS-1) or tape-not-in-motion (TNIM-1) indicator is made true.

The rate amplifier also provides a switch that alters the attenuation of the limiting feedback signal from the integrator. When the FAST-1 signal is false, the FET limit switch is turned off allowing the RAMP-1 signal to attain voltage levels of ±3 volts. When FAST-1 is true, the FET switch conducts and allows the RAMP-1 signal to limit at ±9 volts.

The motor drive amplifier circuitry is shown on schematic sheet 6-3. This is a high gain current amplifier that uses complementary darlington transistors to drive a dc controlled motor. The motor uses a tachometer to provide voltage feedback to regulate the motor drive amplifier. There is also other feedback in the amplifier circuits to stabilize motor speed variations by limiting the maximum gain of the amplifier circuits. R587, R591 and R593 are resistors in three of the noise suppression loops.

The Zero Motion adjustment establishes a bias to provide no motor drive current when the tape is to be stopped.

The Motor Speed adjustment is set to provide 30 or 90 inches per second tape velocity when the full ramp votage has stabilized.

GENERAL PURPOSE INTERFACE BUS (GPIB)

Figure 6-33 is a block diagram of General Purpose Interface Bus (GPIB) circuitry. The numbers in parentheses in the figure refer to the appropriate 4051 schematic sheet in Volume 2 of the Service Manual.

The GPIB conforms to the IEEE Standard 488-1975, A Standard Digital Interface For Programmable Instrumentation. The current implementation does not allow the use of other controllers on the bus; therefore the 4051 must be a primary system controller. The 4051 firmware does *not* support the following functions:

1) The passing of control between system and task controllers.
2) The ability to request service of another device (i.e., another controller).
3) Parallel Poll operations.

Operation of the GPIB electronics is straight forward. The TALK signal goes true whenever the 4051 wishes to send data to devices on the General Purpose Interface Bus. When the TALK signal is true, data on the data lines can pass to the external data bus through the bus driver circuitry. Data external to the 4051 cannot be received. Also, when TALK is true, the receive handshake signals NRFD and NDAC cannot be activated by 4051 circuitry; the state of these lines can only be read by the 4051.

When the TALK signal is false, data can be received through the bus driver circuitry and the handshake signals NRFD and NDAC can be interrogated by the talking or transmitting device.

Bus drivers on all the other interface lines are constantly enabled to provide signal paths as defined by arrows in the block diagram of Fig. 6-33.

The hardware used is primarily open collector TTL logic where the output is active low and passive high. Wired OR logic causes a low signal to override all the other high signals. An active output transistor will lower the collector voltage of all passive or non-conducting output transistors.

Handshake sequences and message protocol as defined by the IEEE Standard 488-1975 specification document is implemented by firmware and software programming in the 4051. For a complete description of GPIB timing and performance limitations, refer to the *4051 GPIB Hardware Support* manual.

POWER SUPPLY BOARD

The Power Supply schematics are found in the 4051 schematics section of Volume 2 of the 4051 Service Manual. The schematics are sheets 1-1 and 1-2.

4051 Graphic Systems are shipped from the factory strapped for 120 volts ac.

Filtered line voltage is supplied to a power transformer strapped for one of several line voltage ranges (100 V, 120 V, 200 V, 220 V, or 240 V ac). Voltage selection jumpers are located on the power transformer. Access is obtained by removing the top cover from the 4051, then the line voltage protection shield. Outputs of this transformer pass through conventional diode bridge networks to provide power for the unregulated power supplies: +320 V, +195 V, +20 V, −20 V, and source for +5 V regulated.

Note that when measuring voltages of unregulated voltage supplies with a voltmeter, the meter reading will be somewhat higher than the indicated supply voltage. Under the maximum specified load conditions, these unregulated voltages should not drop below the indicated value.

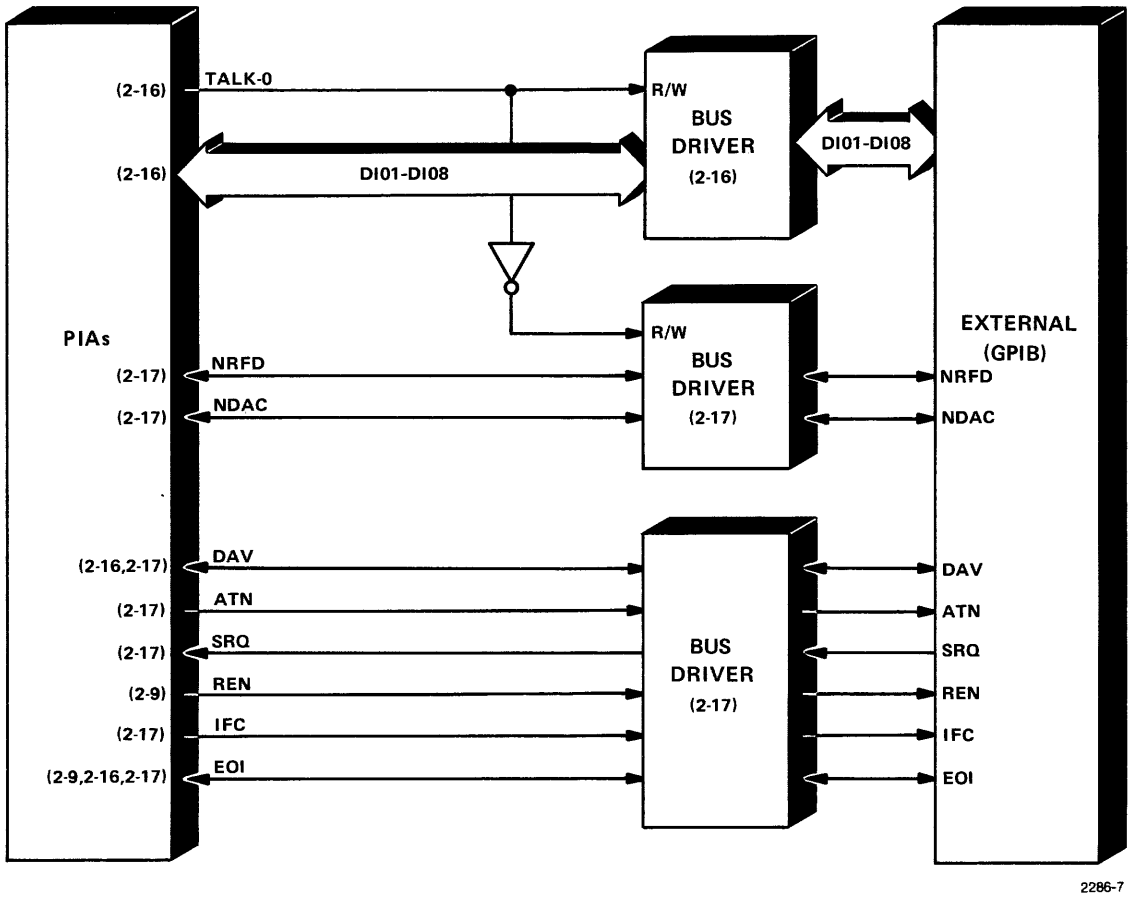


Fig. 6-33. Block diagram for general purpose interface bus (GPIB) circuitry on the 4051.

REGULATED POWER SUPPLIES

Refer to sheets 1-1 and 1-2 of the 4051 schematics.

The flood gun heater (F.G. HEATER) supply is a zener regulated voltage of 43 V with reference to the −20 V unregulated supply. A darlington transistor provides the flood gun voltage at its emitter and obtains its power from the +20 V unregulated supply.

The +15 volt regulated supply also derives its power from the +20 V unregulated source. Regulation is provided by an IC regulator circuit. This regulator circuit has its own internal zener voltage reference, an operational amplifier, and current limiting circuitry built in. Voltage determination is established by tapping a +5 volt reference from the zener voltage reference using the +15 V adjustment potentiometer. The +15 V output voltage is passed through a resistive divider to place +5 volts on the negative or regulating input of the voltage regulator. Transistor Q451 provides the current necessary to maintain the +15 volt power source. Current is drawn from the +20 V supply.

The +12 volt regulated supply is determined by circuitry contained entirely within the U352 regulator package. With no power transistor for output, the available current on this supply is severely restricted.

The −12 volt regulated supply uses a voltage divider between the output voltage and the +15 volt regulated supply to provide a feedback voltage near zero to a regulating amplifier (U442). The reference input to this amplifier is at ground potential. Q452 and Q453 act as a Darlington transistor to power the −12 volt supply by driving current from this supply and feeding it to the −20 V system. Current limit is affected by Q454 in conjunction with the 1 Ω resistor, R341, when the voltage drop across R341 becomes greater than 0.6 volt.

The +5 volt regulated power supply has a power-up delay provided by capacitor C552 and the distributed circuit resistances. This delay is enough to give the RESTART-0 signal enough time to initialize 4051 electronics and programming. The regulating amplifier is U541A feeding a series-pass power Darlington Q552. Current limiting is provided by transistor Q551 in conjunction with the resistance network on its base. Overvoltage protection is afforded by the Q251 SCR, VR251, and R251. When the output voltage causes R251 to see an appropriate positive voltage, the SCR triggers and shunts the power supply to ground.

Section 7

BACKPACK CIRCUITS

FIRMWARE BACKPACK (020-0147-00)

A block diagram of the Firmware Backpack circuitry is shown in Fig. 7-1. The circuit diagrams can be found among the Backpack Schematics in Volume 2 of the 4051 Service Manual. The Firmware Backpack circuitry provides an extension of the microprocessor data and address busses to external circuitry. It also provides a bank switch register to select specific hardware circuitry that is placed on the external lines. The external circuitry can be 8K ROM Packs or special interfaces.

Refer to the Firmware Backpack block diagram of Fig. 7-1. Circuit operation is basically the passage of address and data lines from the 4051 to an external bus structure. There are also some control lines that are passed such as MCP2 for timing, IRQ for interrupt requests, RWOC to initiate read and write output commands, EPIAS to strobe external PIAs, and PIAE to enable a PIA address. There are several control lines generated in the backpack to facilitate reduced electronics in external circuit modules. These lines are decoded external peripheral control lines XPC2, XPC3 and XPC4; also BS(L) and BS(R) that logically connect ROM devices in either of two backpack slots to the address and data busses. BSOFL performs functions similar to BS(L) and BS(R) but enable an overflow ROM set within the backpack. BSX(L) and BSX(R) enable ROM devices within the slots found in an optional ROM Expander Unit. A ROM bank control signal (RBC) is generated to disable an 8K ROM bank that resides on the cpu board within the 4051 whenever an auxiliary ROM bank is activated (i.e., external ROM Packs or overflow ROM within the backpack).

BACKPACK ADDRESSING

Table 7-1

BANK SWITCH AND PERIPHERAL CONTROL ADDRESSES

Memory Address	Function
87C0	Load Bank Switch (LBS)
87C0-87C3[a]	Communications PIA
87C4-87C7[a]	Communications ACIA
87C8-87CB	External PIA 2 (XPC2)
87CC-87CF	External PIA 3 (XPC3)
87D0-97D3	External PIA 4 (XPC4)
8800-A7FF	Switched 8K ROM Bank

[a]These addresses and bank switch data values are used by the Communications Backpack.

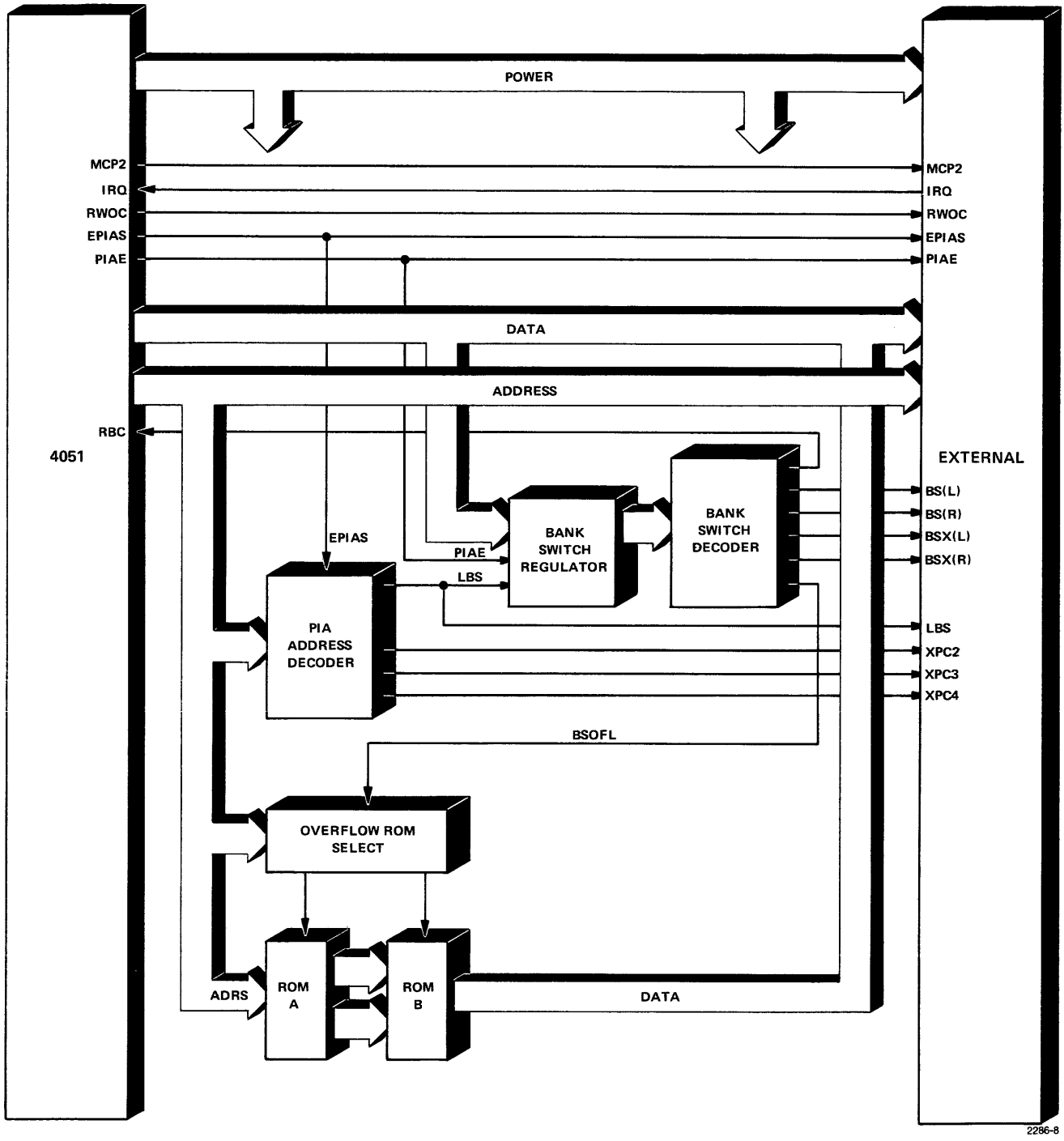


Fig. 7-1. Block diagram of the Firmware Backpack circuitry.

Table 7-2

BANK SWITCH SELECT DATA

Bank Switch Data (with LBS) 7 6 5 4 3 2 1 0	Function
X X 0 0 0 X X X	RBC
X X 0 0 1 X X X	BSOFL
X X 0 1 0 X X X [a]	BSCOM
X X 0 1 1 X X X	-----
X X 1 0 0 X X X	BS(L)
X X 1 0 1 X X X	BS(R)
X X 1 1 0 D D D	BSX(L)
X X 1 1 1 D D D	BSX(R)

X = Don't Care Bit
DDD = ROM Expander Unit Slot Address
(L) = Left Backpack Slot
(R) = Right Backpack Slot

[a] **These addresses and bank switch data values are used by the Communications Backpack.**

Table 7-1 shows the memory addresses that activate the bank switch and peripheral control lines. Table 7-2 shows the interpretation of data loaded into a bank switch register. Several elements in these tables refer to circuitry available in the optional Communications Backpack.

Bank switch operations are simply the writing of a data byte to the bank switch register(s) located at memory location '87C0'. The optional ROM Expander Unit has its own bank switch register to decode one of eight slots. Data in the bank switch register is decoded to enable ROM banks and external interfaces that occupy the specified backpack slot or location. The device remains enabled until the bank switch data is changed by another write operation to the bank switch register.

On 4051 power-up, the firmware in the 4051 sequentially loads all possible bank switch data locations to scan the available backpack slots for ROM packs and optional interfaces. During a search for valid ROM packs, the microprocessor tries to read data from the first ROM locations in the switch register and match the data to a standard data string. A data match means that a valid ROM pack is installed in the specified slot. Special purpose interfaces must have an identification ROM installed. This ROM may also house the firmware necessary to operate the special interface.

COMMUNICATIONS BACKPACK (021-0188-00)

The Communications Backpack provides the same functions as the Firmware Backpack and includes an RS-232 asynchronous communications interface. The RS-232 interface allows the 4051 to emulate a TEKTRONIX 4012 Display Terminal as well as provide formatted line communications with a host computer in much the same manner as an intelligent computer terminal. The Firmware Backpack writeup describes much of the Communications Backpack circuitry. Primary differences include a bank of communications control ROM, an asynchronous communications interface adapter (ACIA) and a communications peripheral interface adapter (PIA). The bank switch register is the 'A' data register or peripheral output register within the communications PIA instead of a discrete register as found in the Firmware Backpack. There are two circuit boards within the Communications Backpack. One houses the interface control circuitry and RS-232 interface lines while the other houses the overflow ROM bank and the communications ROM bank.

For detailed operation of the RS-232 interface found on the Communications Backpack, refer to the *4051 Option 1 Data Communications Interface 021-0188-00* manual. That manual specifies the various modes of operation as well as the BASIC language statements that implement the modes. The following text describes the interface circuitry rather than all the firmware control functions.

COMMUNICATION CIRCUITRY

Refer to the Communication Backpack (Interface) schematic in Volume 2 of the 4051 Service Manual and the communication interface block diagram of Fig. 7-2. RS-232 signal name definitions are given in Table 7-3. The operational status of the RS-232 communications lines is sensed by the peripheral interface adapter (PIA). This PIA also controls data on the CTS and STX lines to initiate transmission line turn-around operations — especially in half-duplex supervisor protocol situations. The output connector looks like the lines from a data communications modem. The communications cable that is used transposes the following lines when the 4051 is connected to modem data communications equipment: RDATA-TDATA, STX-SRX, RTS-CTS, DSR-DTR.

Table 7-3

RS-232 DEFINITIONS	
TDATA	Transmitted Data
RDATA	Receive Data
STX	Secondary Transmit Data
SRX	Secondary Receive Data
DCD	Data Carrier Detect
DSR	Data Set Ready
RTS	Request To Send
CTS	Clear To Send

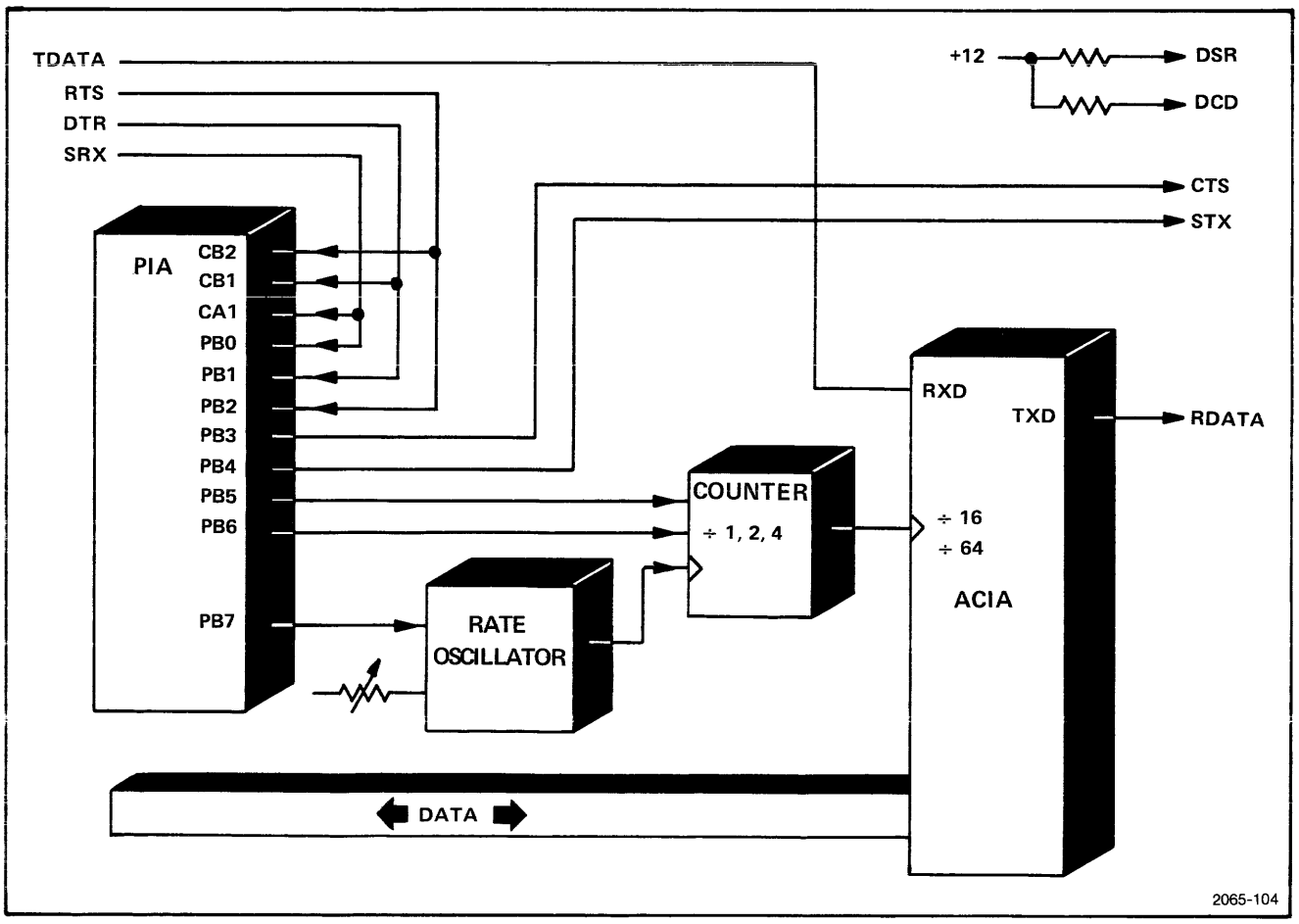


Fig. 7-2. Communication Interface Block Diagram.

Data rate selection (baud rate) is determined by data bytes sent from the 6800 microprocessor to both the ACIA and the PIA. Data sent to the ACIA determines whether the clock signals are divided by 16 or 64 pulses per data bit interval. The oscillator transmits a frequency of 38,4000 Hz or 28,160 Hz depending on bit 7 (PB7) of a data byte sent to the 'B' peripheral register in the PIA. The counter is programmed as a divide by one, two, or four by PIA data bits PB6 and PB5. There is no method available to utilize an external synchronous data clock signal or to provide an external synchronous clock signal in the Communication Backpack.

The oscillator frequency is shown in Table 7-4. The frequency division of the counter is shown in Table 7-5. And the state of the system for each available baud rate is shown in Table 7-6.

Table 7-4

OSCILLATOR FREQUENCY

PB7	
0	38,400 Hz
1	28,160 Hz

Table 7-5

FREQUENCY DIVIDING COUNTER

PB6	PB5	
0	0	÷1
0	1	÷1
1	0	÷4
1	1	÷2

Table 7-6

BAUD RATE SELECTION

Baud Rate	Oscillator	Divider	ACIA
2400	38,400	÷1	÷16
1200	38,400	÷2	÷16
600	38,400	÷1	÷64
300	38,400	÷2	÷64
150	38,400	÷4	÷64
110	28,160	÷4	÷64

Data addressed to the ACIA data registers (address 87C5 or 87C7) is for data transmitted over or received by the interface.

Data addressed to the ACIA control register (address 87C4 or 87C6) has the format as specified in the following tables.

Table 7-7

BITS 1-0 SPECIFY BAUD RATE CLOCK DIVISION

Bit 1	Bit 0	
0	0	÷1 (not used)
0	1	÷16
1	0	÷64
1	1	Master Reset

Table 7-8

BITS 4-2 SPECIFY PARITY ENCODING/DECODING

Bit 4	Bit 3	Bit 2	
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Table 7-9

BITS 6-5 ENABLE OR DISABLE TRANSMIT BUFFER EMPTY INTERRUPT AND BREAK — SPACING OF DATA TRANSMISSION.

Bit 6	Bit 5	
0	0	Transmit Interrupt Disabled
0	1	Transmit Interrupt Enabled
1	0	Transmit Interrupt Disabled
1	1	Transmit Interrupt Disabled — Send BREAK

Table 7-10

BIT 7 CONTROLS THE READ BUFFER FULL INTERRUPT

Bit 7	
0	Receive Interrupt Disabled
1	Receive Interrupt Enabled

PIA data register addressing relies upon previously setting a specific bit (bit 2) in the associated PIA control register. To address a peripheral register or peripheral data bus, the control register bit 2 must be set to a one. A zero in bit 2 causes the data direction register to be addressed by the same memory address.

COMMUNICATION CABLE

The backpack output has a female connector that corresponds to EIA RS-232 standards for data communication equipment (modem pinouts). To use the 4051 as data terminal equipment, a special cable is provided that interchanges the line pairs 2-3, 4-5 and 8-20. All other control lines go directly through the cable, pin for pin. See Fig. 7-3.

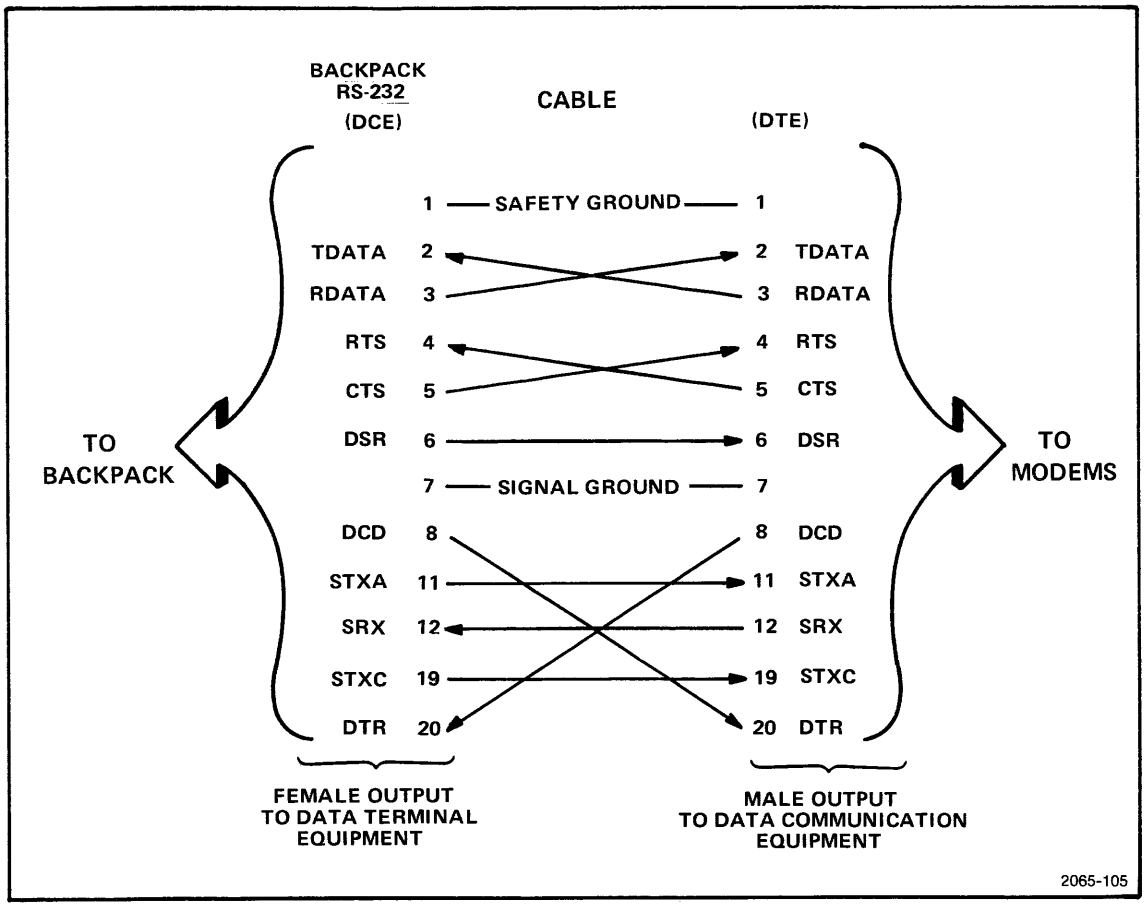


Fig. 7-3. Communication cable for the 4051 Communication Backpack.

SELF-TEST ADAPTER

For reliable execution of the communication interface test program, CALL "CMTEST", be sure to have the communication cable removed from the backpack and a self-test adapter installed. Cross-talk and reflected data in a non-terminated cable may cause unexpected test results. Wiring for the adpater is shown in Fig. 7-4.

COMMUNICATION INTERFACE TEST "CMTEST"

The Communication Interface Test is initiated by typing the CALL "CMTEST" command sequence on the 4051 keyboard. The test is performed in three parts. The test is generally performed with a Self-Test Adapter attached to the RS-232 communication lines at the backpack.

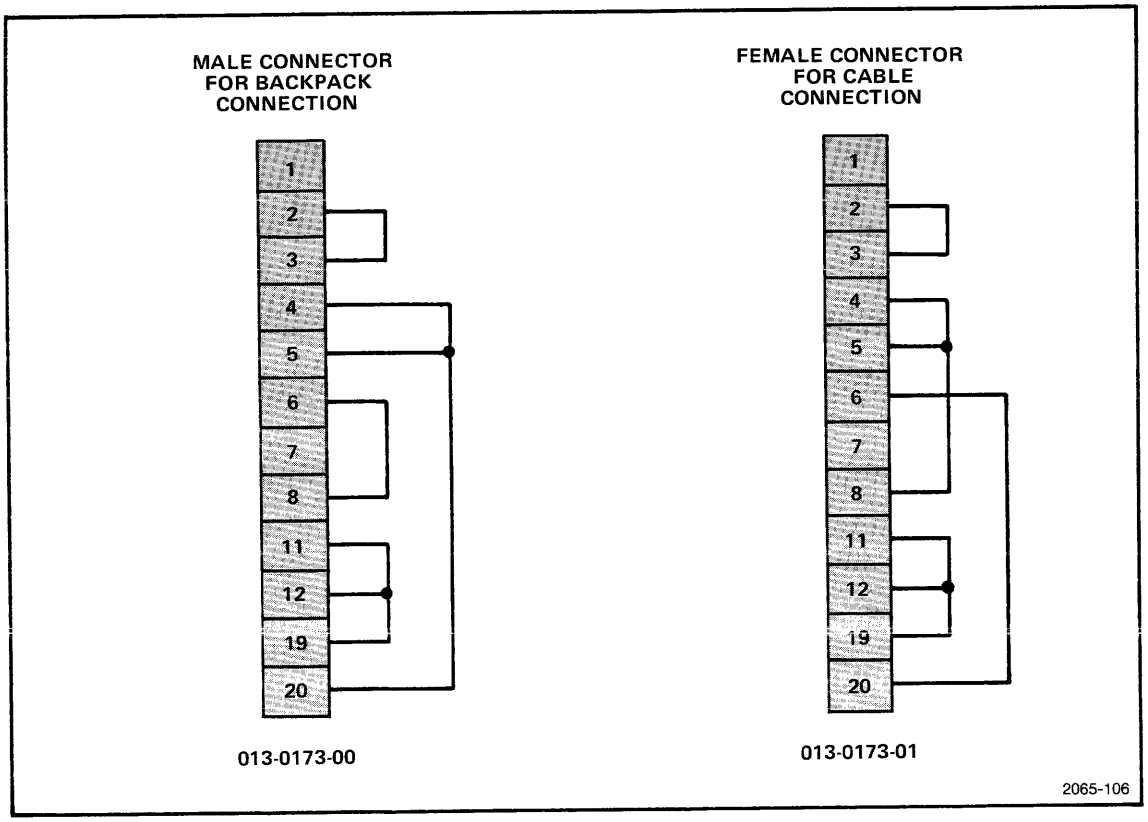


Fig. 7-4. Self-test adapters for use with the communication backpack. Use of the male connector (013-0173-00) is preferred.

Part 1 tests the communication control lines in the RS-232 interface. If the self-test adapter is not installed, the error messages look like those of Fig. 7-5. The expected state transitions and data levels are shown in Fig. 7-6. If there is a mismatch between the expected transition state or data level, an output to the display shows a 1 — otherwise a 0 is displayed to show the absence of error as in Fig. 7-7.

Part 2 tests the data lines by receiving a line of data as it is being transmitted.

Part 3 tests the timing circuitry. Pin 3 of the RS-232 connector on the back of the backpack provides a square wave signal that has a frequency equal to half of the baud rate. Unless the baud rate has changed by the CALL "RATE" command, the received square wave should be 150 Hz. If not, the callibration adjustment should be reset.

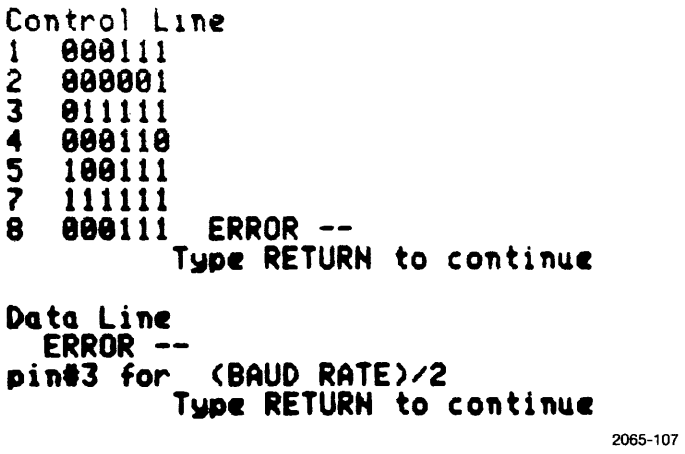


Fig. 7-5. Message displayed on the crt for "CMTEST" when no self test adapter is installed. This pattern indicates no error.

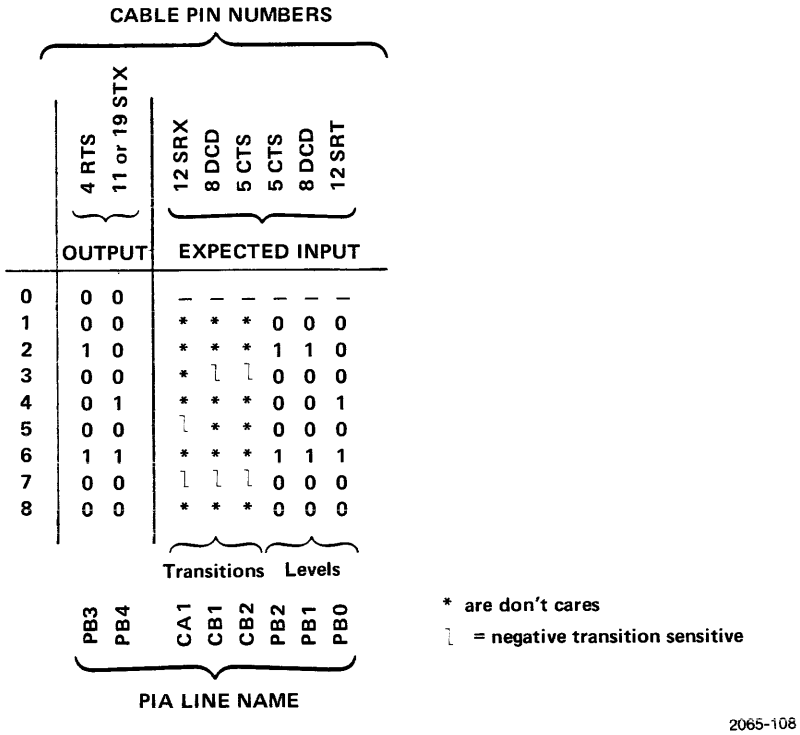


Fig. 7-6. Active data lines, expected transitions and expected data during the first test in the "CMTEST" program.

```
Control Line
Data Line
HIJKL
NOHIJKL
NOXYZ[\]↑_XYZ[\]↑_()*+,-./()*+,-./89:;<=>?89:;<=>?HIJKLMNOHIJKLMNOXYZ[\]
↑_XYZ[\]↑_hijklmnohijklmnoxyz{|}~↓xyz{|}~↓  ERROR --
pin#3 for  (BAUD RATE)/2
         Type RETURN to continue
```

2065-109

Fig. 7-7. Display output of "CMTEST" when the self test adapter is used and no errors are present.

Appendix A

INDEX OF SIGNAL NAMES

Interpretation of true and false logic states on the schematic diagrams uses this convention. Whenever a signal is followed by a dash one (NAME-1), the voltage is logically *high* for the signal to be true. Whenever a signal is followed by a dash zero (NAME-0), the voltage is logically *low* for the signal to be true.

AB0 thru AB15	ADDRESS BUS LINES These lines comprise the address bus. Data on the address bus determines which memory location or peripheral interface is to be activated.
ABA	ADDRESS BUS AVAILABLE This signal is the buffered bus available signal from the microprocessor. The true state specifies that the microprocessor is not using the address bus and that any other device may use the bus at this time. Memory refresh activity occurs at times when ABA is true. The 4051 system test fixture uses this signal to enable memory input/output operations when the microprocessor is halted.
ADOT	ALPHANUMERIC DOT This signal causes the display of a stored dot in the drawing of a printable character on the crt.
ANODE	ANODE This is a voltage line controlling the flood guns. When the display is in view mode, the anode voltage is +150 volts dc. When the display is in hold mode, the anode voltage alternates between +150 volts and zero volts, turning the flood guns on and off, to maintain the display of information on the crt.
ATN	ATTENTION This signal is activated by the 4051 when it is transmitting multiline interface messages over the General Purpose Interface Bus (GPIB). Only an active controller (4051 assumes it is the only controller) asserts ATN. When ATN is true, data on the data lines DIO1 thru DIO8 is interpreted as a talk address, listen address, untalk, unlisten,

or any other multiline interface message specified in the IEEE Standard 488-1975 (IEEE Standard Digital Interface for Programmable Instrumentation. When ATN is false, the assigned talker can send device dependent information over the data lines DIO1 thru DIO8.

BIAS

BIAS
This voltage is generated by deflection amplifier circuitry on the display board to establish four constant current sources for proper display operation. Two of the current sources enable operation of the deflection amplifier outputs. The other two enable the multiplexing of crt deflection control between the cpu board and an optional Hard Copy Unit.

BIAS

BIAS
This voltage is generated in the digital-to-analog circuitry on the cpu board to bias the current summing amplifiers of the digital-to-analog converters in their active region.

BREAK

BREAK
This signal is used to light the BREAK light. This light being on indicates that program execution will halt at the completion of the current BASIC program language statement, at which time the BREAK light will go out.

BSCOM

BANK SWITCH COMMUNICATION
This signal is generated by the banks switch data decoder to enable an 8K bank of read only memory (ROM) that contains code to govern RS-232 communication activity. To activate BSCOM, the hexadecimal data (10) must be loaded into the bank switch data register. LBS is active when the bank switch data register is addressed. The bank switch data register is located in the backpack.

BS(L)

BANK SWITCH LEFT
This signal is generated by the bank switch data decoder to enable an 8K bank of read only memory (ROM) residing in the left backpack slot. The bank switch data register is located in the backpack.

BS(R)

BANK SWITCH RIGHT
This signal is generated by the bank switch data decoder to enable an 8K bank of read only memory (ROM) residing in the right backpack slot. The bank switch data register is located in the backpack.

BSX(L)

BANK SWITCH EXPANSION LEFT
This signal is generated by the bank switch data decoder to enable an 8K bank of read only memory (ROM) that resides in any of 8 slots in an optional ROM Expander Unit. The particular expander slot is determined by the 3 least significant bits of data loaded into a bank switch register.

BSX(R)

BANK SWITCH EXPANSION RIGHT
This signal is generated by the bank switch data decoder to enable an 8K bank of read only memory (ROM) that reside in any of 8 slots in an optional ROM Expander Unit. The particular expander slot is determined by the 3 least significant bits of data loaded into a bank switch register.

BUFCLK

BUFFER CLOCK
This signal is used to strobe data into the digital-to-analog converter data registers. It restarts a 90 second view mode timer. And, if vectors are to be drawn, it initiates a 3.7 millisecond pulse (VPULSE) used to time vector draws.

BUSY

BUSY
This signal lights the BUSY light to indicate that the 4051 is busy transferring or processing data. BUSY is also driven by a programmed square wave to cause an audio tone at the speaker.

CBACIA

COMMUNICATION BACKPACK ACIA
This signal is a line from an address asynchronous communication interface adapter is being addressed.

CTRL

CONTROL
This signal is generated by pressing the CONTROL or CTRL key on the keyboard.

COPY

COPY
This signal is generated by programming to initiate hard copy activity. It is also asserted when the MAKE COPY key on the keyboard is pressed.

COPYEN

COPY ENABLE
This signal is generated by the OR of READ and WAIT signals from an optional Hard Copy Unit enabling the Hard Copy Unit to control circuitry on the display board. When the COPYEN signal is true, the Hard Copy Unit is either producing a hard copy or waiting to produce a hard copy of information on the crt.

COPYEN is driven false whenever the internal magnetic tape drive is in motion, preventing the Hard Copy Unit from simultaneously controlling the display circuitry. Since both the crt display and tape drives are large consumers of energy, and that there is limited power from the power supply, a requirement exists that the display deflection amplifiers and tape motors cannot be simultaneously active.

CS — CHIP SELECT
This signal is generated by the MCP2 clock to select random access memory (RAM) circuits for read and write operations only when MCP2 is true. When MCP2 is false, memory refresh operations may occur. CS is the inverse of MCP2.

CTS — CLEAR TO SEND
When the 4051 acts as a data set, the signal transmitted at pin 5 of the RS-232 interface on the Communication Backpack enables a computer terminal to send data to the 4051.

When the 4051 acts as a data terminal, CTS becomes **Request To Send** on pin 4 of the RS-232 communication cable. It then notifies data communication equipment that the 4051 wishes to transmit data.

DAV — DATA VALID
The true state of this signal specified that data on the general purpose interface bus (GPIB) data lines (DIO1 thru DIO8) is valid. The 4051 places a true signal on DAV whenever data or remote interface messages are placed on the data lines by the 4051. DAV should remain asserted until NDAC goes false.

The 4051 cannot issue DAV if NRFD is true. A true on NRFD does not remove an already valid DAV signal.

The 4051 cannot issue DAV if it is a listener on the GPIB.

DB0 thru DB7 — DATA BUS
These are the bi-directional data bus lines between the microprocessor and all memory and interface devices in the 4051.

DBE — DATA BUS ENABLE
This signal is an input to the microprocessor to enable the microprocessor to output information on the data bus. DBE is actually the phase two microprocessor clock MCP2. When high, the microprocessor can write data to the data bus, when low, memory refresh activity and other data functions can make use of the data bus.

DCD	DATA CARRIER DETECT When the 4051 acts as a data set, the signal transmitted at pin 8 of the RS-232 interface on the Communication Backpack enables a remote terminal to send and receive data on the interface. When the 4051 acts as a data terminal, DCD becomes **Data Terminal Ready** on pin 20 of the RS-232 communication cable. It tells data communication equipment that the 4051 is ready to send or receive data over the RS-232 interface.
DELAY IN	DELAY INPUT This is a general purpose trigger signal derived from the selected operation trigger (SOT) signal. DELAY OUT is triggered by DELAY IN going high. DELAY OUT remains high for 40 microseconds after being triggered by DELAY IN.
DELAY OUT	DELAY OUTPUT This signal is a general purpose timing pulse of 40 microseconds in duration generated by a one shot on the tape drive board. DELAY OUT is triggered by the DELAY IN signal from the cpu board.
DIO1 thru DIO8	DATA IN AND OUT BUS These are the bi-directional data lines found on the general purpose interface bus (GPIB).
DRBUSY	DIRECT READOUT BUSY This signal goes true any time the display is busy (during an erase cycle or creating a hard copy). DRBUSY notifies the microprocessor that the cpu is involved in a time-consuming task. It also ensures that the flood guns are active when performing a page erase function or a hard copy operation.
DRTAPE	DRIVE TAPE This signal is generated by the microprocessor through a peripheral interface adapter to turn the tape unit motor on and off. When true, the tape motor is turned on; when false, the tape motor is turned off.
DSR	When the 4051 acts as a data set, the DSR signal transmitted on pin 6 of the RS-232 connector on the Communication Backpack tells the terminal that the 4051 is powered up and ready to operate. When the 4051 acts as a data terminal, the passive high has no affect on the DSR signal transmitted by the data communication equipment. DSR is ignored.

DTR	DATA TERMINAL READY When the 4051 acts as a data set, the signal received on pin 20 of the RS-232 connector of the Communication Backpack tells the 4051 that a data terminal is powered up and ready for operation. When the 4051 acts as a data terminal, DTR becomes **Data Carrier Detect** on pin 8 of the RS-232 communication cable. It then notifies the 4051 that a data set is powered up and that a communication link has been established.
DYNAMIC FOCUS	DYNAMIC FOCUS This analog voltage is generated by the deflection amplifiers on the display board to provide correction to compensate for the physical characteristics of the crt. The correction voltage is proportional to (X deflection)^2 + (Y deflection)^2.
EMI0 thru EMI7	EXPANDED MEMORY INPUTS These signal lines are an extension of the bi-directional data bus used to provide data to be written into random access memory (RAM) devices on the expanded memory board within the 4051.
EMO0 thru EMO7	EXPANDED MEMORY OUTPUTS These signal lines are the output data bus from the random access memory (RAM) devices. During RAM read operations, data on the expanded memory output lines is strobed onto the 4051's bi-directional data bus.
EOI	END OR IDENTIFY This signal is sent true by an assigned talker on the general purpose interface bus (GPIB) to signal the end of data. Since parallel poll operations are not implemented in the 4051, the identify function of EOI is not implemented. During normal bus operation, EOI accompanies the last data byte to be transmitted.
EPIAS	EXTERNAL PERIPHERAL INTERFACE ADAPTER SELECT This signal is generated by the read only memory (ROM) page decoder and goes true whenever data on the address bus specifies that a valid external peripheral address may be present. External peripheral interface adapters (PIAs) are optional interfaces in ROM Pack cartridges that are inserted into backpack slots.
ERASE	ERASE This signal is generated on the cpu board to initiate an erase cycle on the display board.

FAST	FAST This signal is generated on the cpu board to determine the operating speed of the tape drive motor. When FAST is true, a tape speed of 90 inches per second is enabled. When FAST is false, the normal read/write tape speed of 30 inches per second is enabled.
FICG	FIND INTERCHARACTER GAP This signal enables the intercharacter gap (ICG) detecting circuitry during magnetic tape read operations. A true state enables the detection of file marks and record marks when the tape is operating at normal speed.
FILFND	FILE FOUND This signal is interrogated to indicate the presence of an interfile gap when the tape is operating in a fast search mode of 90 inches per second. FSENABLE is the signal that enables a timing one-shot that generates FILFND.
F.G. HEATER	FLOOD GUN HEATER VOLTAGE The flood gun heater voltage is a zener regulated voltage of +40 volts above the −20 volt unregulated supply. It is used to heat the filaments in the crt flood guns.
FMARK	FILE MARK This signal is generated by the intercharacter gap (ICG) counter when reading the tape and a file mark has been encountered. A file mark consists of 8 consecutive intercharacter gaps separated by flux reversals on track 0 — one reversal between each ICG.
FSENABLE	FAST SEARCH ENABLE This signal, when true, enables the detection of an interfile gap when the tape is operating in a fast search mode of 90 inches per second.
GICG	GENERATE INTERCHARACTER GAP This signal enables the selected operation trigger (SOT) to become the magnetic tape write clock (WCLK) when generating intercharacter gaps. GICG also forces a data write to track zero by holding WDATA false.
GND	GROUND This is the electrical common or zero potential (chassis voltage) in the 4051.

HALT	HALT This signal is generated by the 4051 system test fixture to stop the operation of the microprocessor. When the microprocessor is stopped, VMA is false, BA is true, and the three-state signals, R/W, address lines and data lines are at a high impedance state. HALT is also used by the 4051 system test fixture to single-step through microprocessor instructions.
IFC	INTERFACE CLEAR This general purpose interface bus (GPIB) signal is asserted by the 4051 to force all devices on the bus to a predetermined quiescent state. The INIT statement in the 4051 BASIC language will cause the IFC line to become active. The 4051, being the only controller and therefore the system controller, is the only source for this signal.
INTER	INTERROGATE This signal is produced by an optional Hard Copy Unit to strobe the crt writing beam (Z axis) while generating a copy of the displayed image. Each time the strobed writing beam lands on a written portion of the crt image, a target signal (TARSIG) is generated and transmitted back to the Hard Copy Unit.
I/O	INPUT/OUTPUT INDICATOR This signal is used to turn on the I/O signal light anytime a device input/output operation (data transfer) is performed.
IPIAS	INTERNAL PERIPHERAL INTERFACE ADAPTER SELECT This signal is generated by the read only memory (ROM) page decoder and goes true whenever data on the address bus specifies that a valid internal peripheral address may be present. Internal peripheral interface adapters (PIAs) are located on the cpu board.
IRQ	INTERRUPT REQUEST This line is a maskable interrupt request line to the microprocessor.
KBCLK	KEYBOARD CLOCK This signal increments a data decoding counter used to interrogate and decode the particular alphanumeric key being pressed. The clock is generated as an output from the random access memory (RAM) refresh counter.
KBCOPY	KEYBOARD COPY This signal is used only by the 4006-1 Display Terminal to initiate a hard copy request.

KBHALT	KEYBOARD HALT This is a signal generated by the keyboard interface to stop the keyboard decoding counter until its contents can be read. The count is placed on the key code lines (KC0 through KC6) to specify which key has been pressed. After the microprocessor has read the key code, the KBHALT line again goes false.
KC0 thru KC6	KEY CODE LINES Data found on these lines specifies which keyboard key has been pressed. Data on these lines becomes stable when the microprocessor issues a KBHALT command to the keyboard. Data on KC0 thru KC6 is converted into ASCII format by the microprocessor for BASIC data processing.
KEY	KEY DOWN This signal goes true whenever a key on the keyboard is pressed.
LAMP ON	LAMP ON This signal is used to turn on the tape sensing lamp when the tape cartridge is inserted into the instrument. Illumination from the lamp is used to activate phototransistors that generate UPHOLE and LOHOLE signals.
LAMP ON RETURN	LAMP ON RETURN This signal is used by logic to sense that a cartridge tape unit has been inserted into the 4051. The tape drive motor is disabled unless the sensing lamp is on and a tape cartridge is inserted into the sstem.
LBS	LOAD BANK SWITCH This signal is generated whenever the bank switch memory location is addressed. Data written into the bank switch register indicates which 8K ROM bank is selected to use the shared ROM address space. The data also determines which of several possible external interfaces may be activated.
LDCLK	LOAD CLOCK This signal is activated whenever the 4051 wishes to perform tape input/output operations and the LOAD line is false. A false on the LOAD line indicates that there is no tape in true only if a tape cartridge has been loaded into the 4051. The LOAD line will remain true until the tape cartridge is removed.

LOAD	LOAD This signal is used by the microprocessor through the keyboard PIA to determine if a tape cartridge is loaded and available to perform input/output operations.
LOADED	LOADED This signal is generated by a microswitch in the 4051 to indicate that a tape cartridge is currently in the system.
LOHOLE	LOWER HOLE INDICATOR This signal is generated by a phototransistor as light shines through the lower magnetic tape hole, right side of tape. LOHOLE is used to decode beginning of tape (BOT) and end of tape (EOT).
MAB0 thru MAB11	MULTIPLEXED ADDRESS BUS These signal lines are outputs from the random access memory (RAM) refresh multiplexer. When MCP2 is false, a memory refresh address is on the MAB address lines. When MCP2 is true, memory data address from the microprocessor (or 4051 system test fixture) is on the MAB address lines. The MAB address lines are used to address the contents of random access memory (RAM) devices and also to provide RAM refresh addressing.
MAKE COPY	MAKE COPY This signal is generated on the display board and is sent to an optional Hard Copy Unit whenever a copy is to be made.
MCP1	MASTER CLOCK PHASE 1 This is the phase 1 clock for the microprocessor. It is generated as a fixed number of pulses from a crystal oscillator.
MCP2	MASTER CLOCK PHASE 2 This is the phase 2 clock for the microprocessor. It is also used for peripheral timing and memory timing operations. MCP2 is generated as a fixed number of pulses from a crystal oscillator.
MDATA	MORE DATA This signal is generated by the tape cartridge clocking circuitry to request more data to be written to the tape. It is also used to enable the load and shift operations of a parallel-in serial-out shift register.
MTCLK	MAGNETIC TAPE CLOCK This signal is generated by a counter in the master timing circuits. MTCLK is used to drive the clock control circuitry that writes data to the magnetic tape cartridge.

NDAC	NOT DATA ACCEPTED This is a handshake control line on the general purpose interface bus (GPIB). Its true state indicates that data is not accepted. Listener devices cause this line to go false to signal an acceptance of data in response to DAV.
NMI	NON-MASKABLE INTERRUPT This is a high priority interrupt used by the cartridge tape control logic to request service of the microprocessor. This interrupt cannot be disabled within the microprocessor.
NOBURN CLK	NO BURN CLOCK This is a 12.5% duty cycle clock signal used to reduce writing beam energy when the 4051 draws short vectors. This prevents phosphor burns resulting from concentrated writing energy. The NOBURN CLK signal is generated by the system timing circuits.
NODRIVE	NO TAPE DRIVE This signal is the inverse of DRTAPE to indicate that the magnetic tape motor is not being driven. It is used to disable the writing circuits when the tape is not moving.
NRFD	NOT READY FOR DATA This is a handshake signal used by the general purpose interface bus (GPIB) to indicate that a listener is not ready for data. The false state indicates that a listener is ready to receive more data.
OFA	OVERFLOW A This signal is generated in the Firmware Backpack whenever the first overflow read only memory device is addressed.
OFB	OVERFLOW B This signal is generated in the Firmware Backpack whenever the second overflow read only memory device is addressed.
ORIGIN	ORIGIN SHIFT CLOCK This signal line is pulsed each time the page (or crt display) is erased. ORIGIN clocks a counter that determines the zero address offset for a new page of displayed information.
PIAE	PERIPHERAL INTERFACE ADAPTER ENABLE This signal is true when both VMA from the microprocessor and MCP2 from the master clock circuits are true. PIAE is used as a timing or enable pulse for peripheral interfaces such as PIAs and ACIAs.

PIAS	PERIPHERAL INTERFACE ADAPTER SELECT This signal goes true whenever the address on the address bus lies within the peripheral interface address space. This decoded address signal is used to generate IPIAS and EPIAS.
RAMP	RAMP The voltage on this analog signal line determines the speed of the tape motor and therefore the cartridge tape velocity. The RAMP voltage is determined by an integrator circuit on the motor drive board. Tape velocity is approximately 10 inches per second for each volt of RAMP voltage.
RAMS0 thru RAMS7	RANDOM ACCESS MEMORY SELECT Each of the RAMS lines is generated by an address decoder. Each line enables 4K bytes of random access memory composed of eight 4K RAM chips. RAM blocks 0 and 1 are on the cpu board. RAM blocks 2 thru 7 are on the expanded memory board.
RAMW	RANDOM ACCESS MEMORY WRITE This signal causes a write operation to be performed on random access memory (RAM) devices within the 4051. It goes true whenever a write operation is commanded on R/W from the microprocessor and MCP2 is true. It also goes true if the 4051 system test fixture issues a write command, RWOC, during MCP2.
RBC	ROM BANK CONTROL This signal is generated by the bank switch data decoder in a backpack to disable the 8K ROM bank on the cpu board whenever another ROM bank that shares the same address space is selected.
RCCLK	RANDOM ACCESS MEMORY COUNTER CLOCK This signal is generated by the master clock circuitry to periodically advance the random access memory refresh address counter. The counter cycles the refresh addresses associated with address lines MAB0 thru MAB5.
RCE0 thru RCE7	RAM CHIP ENABLE Each RCE line goes to chip enable inputs of a 4K block of RAM and is activated at the appropriate time for input/output operations and memory refresh operations. During RAM input/output operations, only one of the eight RCE lines is active. During memory refresh, REFCLK0 activates RCE0 and RCE1, REFCLK1 activates RCE2 thru RCE4, and REFCLK2 activates RCE5 thru RCE7.

RCLK

READ CLOCK
This signal is generated by data being read from the internal magnetic tape. RCLK is used to clock the serial tape data into the serial-to-parallel shift register. It is also interrogated by one shots to decode the various tape formatting patterns (i.e., intercharacter gaps, record marks, file marks and interfile gaps).

MRDATA

MAGNETIC READ DATA

This signal is serial data recovered from the tape during a read operation. On the cpu board it is converted to 8-bit parallel data for use by the microprocessor.

RDATA

RECEIVE DATA
When the 4051 acts as a data set, the signal transmitted at pin 3 of the RS-232 connector on the Communication Backpack is data to be received by a data terminal.

When the 4051 acts as a data terminal, RDATA becomes **Transmit Data** on pin 2 of the RS-232 communication cable. This data is sent to data communication equipment.

RDBYTE

READ BYTE
This signal goes true during a magnetic tape read operation when 8 bits of data have been loaded into the read data register, a serial-in parallel-out shift register. RDBYTE informs the microprocessor to read the data currently in the read data register.

RDE

RAM DECODE ENABLE
This signal is generated by the master timing circuitry to enable the decoding of a random access memory (RAM) address during a specified time period (the last 480 nanoseconds of MCP2).

READ

READ
This signal is generated by an optional Hard Copy Unit and goes true whenever the Hard Copy Unit is making a copy of the image on the crt.

REFCLK0
REFCLK1
REFCLK2

REFRESH CLOCK SIGNALS
These clock signals are generated by the master clock circuits to time the refresh activity for random access memory (RAM) devices. Each clock signal initiates refresh activity for a bank of RAMs.

REN

REMOTE ENABLE
The 4051 places this signal on the general purpose interface bus (GPIB) whenever the BUSY light is lit. This signal places all devices on the GPIB under control of the 4051, causing these devices to ignore their front panel controls.

RES

RESET
This signal is a buffered data line from the RESTART signal. This signal resets all interface devices and restarts the microprocessor programming.

RESTART

RESTART
This signal is generated by the +5 volt power supply during 4051 power-up operations. It can also be generated by the 4051 system test fixture.

REV

REVERSE
This signal controls the direction of tape drive operation. When true, the tape travels in the backward direction when the tape unit is ordered into motion. When false, the tape travels in the forward direction.

RMARK

RECORD MARK
This signal interprets the pulses from the intercharacter gap counter to determine when a record mark on tape has been read. A record mark is four successive intercharacter gaps separated only by flux reversals on track 0. There is one flux reversal between each intercharacter gap.

ROMDIS

READ ONLY MEMORY DISABLE
This signal is generated by the 4051 system test fixture to disable the ROME15 signal. When ROMDIS is true, the address space associated with ROME15 is used by memory devices within the 4051 system test fixture.

RTS

REQUEST TO SEND
The 4051 cannot act as a half-duplex data set. RTS is a half-duplex control signal received on pin 4 of the RS-232 connector on the Communication Backpack.

When the 4051 acts as a half-duplex data terminal, RTS becomes **Clear To Send** on pin 5 of the RS-232 communication cable. CTS is transmitted as **Request To Send** whenever the 4051 needs to transmit data. RTS is received as **Clear To Send** whenever it is ok for the 4051 to transmit data. This is half-duplex normal operation.

R/W	READ/WRITE This signal is generated by the microprocessor to control direction of data flow on the data bus. When R/W is true, the microprocessor reads data that has been placed on the data bus by peripheral interfaces or memory. When R/W is false, the microprocessor places data on the data bus to be written into memory or a peripheral interface.
RWIC1 and RWIC2	READ-WRITE INPUT COMMAND These signals are contained entirely within an integrated circuit chip. They are used to place random access memory (RAM) output data onto the data bus whenever a RAM read operation is performed.
RWOC	READ-WRITE OUTPUT COMMAND This signal is the buffered R/W line from the microprocessor. It is used by all devices that are inserted into the backpack slots. The 4051 system text fixture also activates this line when the microprocessor is halted to examine or deposit data in memory locations within the 4051.
SA0 thru SA7	SELECTED DATA BUS A This data bus is used to receive data from the magnetic tape. The bus consists of the PA data lines on the Y axis D/A peripheral interface adapter.
SAFE	SAFE This signal is generated by the magnetic tape microswitch that indicates whether the tape cartridge is write protected. The true state of the SAFE signal prevents data from being written to the tape cartridge.
SAFE SW	SAFE SWITCH This switch is open when a tape cartridge is write-protected. This switch is closed to attach the +15 V_1 supply voltage to the tape writing circuits.
SB0 thru SB7	SELECTED DATA BUS B This data bus is used to send data bytes to the magnetic tape. The bus consists of the PB data lines on the Y axis D/A peripheral interface adapter.
SHIFT	SHIFT This signal is generated by the keyboard whenever the SHIFT key is pressed.

SOT

SELECTED OPERATION TRIGGER
This signal is generated by a peripheral interface adapter to implement several timing functions.

1. SOT triggers a refreshed dot during the display of a cursor or refreshed character on the crt.

2. SOT becomes the WCLK signal whenever an intercharacter gap (GICG) is to be written to the magnetic tape.

3. SOT triggers a 40 microsecond timer on the tape drive board by activating the DELAY IN signal. After initiating SOT, the microprocessor can monitor DELAY OUT to determine when 40 microseconds has elapsed. The 40 microsecond timer is used to control functions such as generating intercharacter gaps on magnetic tape, line turn-around timing in half-duplex communications and status response timing in 4012 Display Terminal emulation.

SPEAKER

SPEAKER
This is a filtered return line for the BUSY signal as it passes through a speaker for generating an audio tone.

SRQ

SERVICE REQUEST
This is a control line that is activated by a peripheral device on the general purpose interface bus (GPIB) to request service from the microprocessor (system controller). The 4051 responds to SRQ by performing a serial poll of devices on the GPIB.

SRX

SECONDARY RECEIVED LINE SIGNAL DETECTOR

This signal is found on pin 12 of the RS-232 connector on the Communication Backpack. It is also on pin 12 of the RS-232 communication cable. When the 4051 acts as a half-duplex data terminal using supervisor communications, the signal received on SRX indicates that the computer or data set is listening for data. When SRX goes false, the computer or data set wishes to send data to the 4051.

STXA
STXC

SECONDARY REQUEST TO SEND (RS-232-A)
SECONDARY REQUEST TO SEND (RS-232-C)
STXA is transmitted by the 4051 on pin 11 of the RS-232 connector on the Communication Backpack or the end of the communication cable. STXC is transmitted by the 4051 on pin 19 of the RS-232 connector on the Communication Backpack or the end of the

communication cable. When the 4051 acts as a half-duplex data terminal using supervisory communications, the signal transmitted on STXA or STXC is true whenever the 4051 is listeneing for data. STXA or STXC is false whenever the 4051 wishes to transmit data. When STXA or STXC is false, the 4051 must wait for SRX to become true before transmitting data. This is half-duplex supervisory communications.

TALK

TALK
This signal goes true whenever the 4051 wishes to transmit data over the general purpose interface bus (GPIB). TALK goes false whenever the 4051 listens to data on the GPIB. TALK provides an enable signal for line buffers on the data lines (DIO1 thru DIO8) and handshake lines (DAV, NRFD and NDAX).

TARSIG

TARGET SIGNAL
This signal is generated by the crt readout amplifier when a hard copy is being created by an optional Hard Copy Unit. During hard copy operation, the crt writing beam is being strobed. Whenever the writing beam lands on a stored (written) portion oof the display, TARSIG momentarily goes true and is used by the Hard Copy Unit to indicate the presence of displayed information at any given location.

TDATA

TRANSMIT DATA
When the 4051 acts as a data set, the signal received on pin 2 of the RS-232 connector on the Communication Backpack is serial data transmitted from a computer terminal to the 4051.

When the 4051 acts as a data terminal, TDATA becomes **Receive Data** on pin 3 of the RS-232 connector on the RS-232 communication cable. It is used to receive data from a computer or data communication equipment.

TNIM

TAPE NOT IN MOTION
This signal is generated by the magnetic tape motor drive circuits to indicate that the tape has stopped.

TTY

TELETYPE LOCK
This signal is generated by the TTY LOCK key on the keyboard. When the TTY LOCK key is down TTY is true and an abbreviated ASCII character set is selected. TTY being false indicates that the TTY LOCK key is up and the full printable ASCII character set is enabled. Decoding of ASCII characters is performed by the microprocessor.

TUTS	TAPE UP TO SPEED This signal is generated by the motor drive circuitry to indicate that the tape motor is up to operating speed of 30 or 90 inches per second.
UPHOLE	UPPER HOLE This signal is generated by a phototransistor as light shines through the upper magnetic tape hole, left side of tape. UPHOLE is used to decode beginning of tape (BOT), the tape load point and the early warning hole near the end of tape.
VECTOR	VECTOR This signal is generated by data from a peripheral interface adapter to enable vector generation. When true, VECTOR activates the filters on the digital-to-analog converter outputs. VECTOR also enables the VPULSE one shot.
VEN	VECTOR ENABLE This signal is generated by data from a peripheral interface adapter to enable the drawing of a vector on the crt. VEN disables the alphanumeric timing one shots and enables the writing beam (Z axis) to turn on during vector generation.
VIEW	VIEW This signal is generated on the cpu board to control the crt flood gun anode voltage. When VIEW is true, the flood gun anode is at +150 volts. When false, the flood gun anode is at zero volts. When the cpu board asserts view mode operation, VIEW is true. When the cpu board asserts hold mode operation, VIEW is activated by a low duty-cycle square wave.
VIEWCAUSE	VIEW CAUSE SIGNAL This signal is generated by a 100 second view timer on the cpu board. VIEWCAUSE is triggered each time the shift key is pressed or each time data is loaded into the digital-to-analog converter circuits.
VMA	VALID MEMORY ADDRESS This signal is generated by the microprocessor when a memory address is placed on the address bus.
VPULSE	VECTOR PULSE This is a 3.7 millisecond pulse that provides the vector drawing time signal. The signal goes true whenever a vector is being generated regardless if it is displayed or not.

WAIT	WAIT This signal is generated by Hard Copy Units that have a multiplexer option. The signal goes true whenever a Hard Copy Unit is currently making a copy from another crt display when the 4051 initiates a copy request. The WAIT signal is used to hold display modification activity until a hard copy has been made of the crt in the 4051.
WCLK	WRITE CLOCK This signal is generated by the magnetic tape write control circuitry driven by MTCLK on the cpu board. WCLK is used to clock data onto the magnetic tape within the 4051.
WDATA	WRITE DATA This is serial data to be written to the internal magnetic tape. This data is unpacked from a parallel-in serial-out shift register on the cpu board and is strobed onto the magnetic tape by the write clock, WCLK.
WENABLE	WRITE ENABLE This signal is generated as data from a peripheral interface adapter to enable magnetic tape writing activity. WENABLE determines whether the write clock signal (WCLK) can be generated and whether data can be loaded into the write data shift register.
WR	WRITE This signal is generated as data from a peripheral interface adapter to select the read/write circuits on the tape drive board. When WR is true, data may be written or stored onto a tape cartridge. When WR is false, data may be read from a tape cartridge.
X	X AXIS ANALOG SIGNAL This signal is the X axis deflection voltage from the filter whose input is X D/A. If vectors are to be drawn, then X D/A is passed through an active RC filter network before becoming X. X voltage range is approximately +8 volts at the left of the screen and −8 volts at the right of the screen.
X AMP	X AXIS AMPLITUDE This signal is generated by the display multiplexer circuits on the display board. Inputs to the circuitry are X HC RAMP IN from a Hard Copy Unit and X from the cpu board. X AMP is used to drive the deflection amplifiers and the correction circuitry for geometry and focus.

X CHAR D/A	X CHARACTER DIGITAL TO ANALOG Character positioning is determined by a primary digital-to-analog converter while column selection within a character is determined by X CHAR D/A.
X D/A	X DIGITAL TO ANALOG This signal is the output from the X axis digital-to-analog converter amplifier. X D/A is selectively filtered to determine writing beam deflection and is used directly as a voltage comparison with a Joystick output voltage.
XERR	X AXIS JOYSTICK ERROR This signal is generated by a comparison amplifier using X D/A and X JOY as input voltages. The state of XERR is examined by the microprocessor to determine the location referenced by the Joystick.
X HC RAMP IN	X AXIS HARD COPY RAMP INPUT This signal is generated by an optional Hard Copy Unit to drive the X axis writing beam deflection while creating a hard copy of the image displayed on the crt.
X JOY	X JOYSTICK VOLTAGE This signal line has a position reference voltage generated by an optional Joystick that can be used for graphic input applications.
XPC2 thru XPC4	EXTERNAL PERIPHERAL CONTROL LINES Each line is a decoded address of a possible external peripheral interface adapter (PIA). These lines can be used to address special interfaces placed into backpack slots or ROM Expander Unit slots. In order for an interface in a backpack slot to be activated, its slot should be previously selected by bank switch circuitry.
Y	Y AXIS ANALOG SIGNAL This signal is the Y axis deflection voltage from the filter whose input is Y D/A. If characters are drawn, the filter is disabled and Y becomes Y D/A. If vectors are to be drawn, then Y D/A is passed through an active RC filter network before becoming Y. Y voltage range is approximately +8 volts at the top of the screen and −8 volts at the bottom of the screen.
Y AMP	Y AXIS AMPLITUDE This signal is generated by the display multiplexer circuits on the display board. Inputs to the circuitry are Y HC RAMP IN from a Hard Copy Unit and Y from the cpu board. Y AMP is used to drive the deflection amplifier and correction circuitry for geometry and focus.

Y CHAR D/A	Y CHARACTER DIGITAL TO ANALOG Character positioning is determined by a primary digital-to-analog converter while row selection within a character is determined by Y CHAR D/A.
Y D/A	Y DIGITAL TO ANALOG This signal is the output from the Y axis digital-to-analog converter amplifier. Y D/A is selectively filtered to determine writing beam deflection and is used directly as a voltage comparison with a Joystick output voltage.
YERR	Y AXIS JOYSTICK ERROR This signal is generated by a comparison amplifier using Y D/A and Y JOY as input voltages. The state of YERR is examined by the microprocessor to determine the location referenced by the Joystick.
Y HC RAMP IN	Y HARD COPY RAMP INPUT This signal is generated by an optional Hard Copy Unit to drive the Y axis writing beam deflection while creating a hard copy of the image displayed on the crt.
Y JOY	Y JOYSTICK VOLTAGE This signal line has a position reference voltage generated by an optional Joystick that can be used for graphic input applications.
Z	Z AXIS SIGNAL This signal is generated by the cpu board to control the state of the writing beam. Z becomes Z MPX on the display board if a hard copy is not being made. If Z is true, the writing beam of the crt will turn on. If false, the writing beam will remain off.
Z MPX	Z AXIS MULTIPLEXED SIGNAL This signal is generated on the display board to drive the writing beam circuits (Z axis amplifier). When a hard copy is to be generated, Z MPX is triggered by INTER. Otherwise, Z MPX is equal to Z.
Z VECT	Z VECTOR DRAW This signal is generated by vector generation circuitry on the cpu board to turn on the writing beam for the duration of a vector draw. The Z signal is controlled by Z VECT as well as outputs of character dot one shots.

Appendix B

MOTOROLA SPECIFICATIONS

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6800
(0 to 70°C; L or P Suffix)
MC6800C
(-40 to 85°C; L Suffix only)

MICROPROCESSING UNIT (MPU)

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

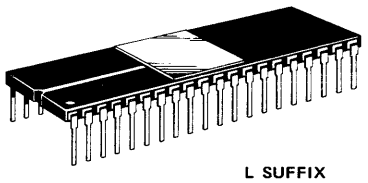
The MC6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65K Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved In Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

MOS

(N-CHANNEL, SILICON-GATE)

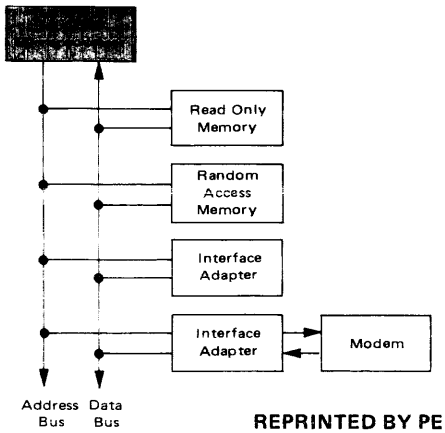
MICROPROCESSOR



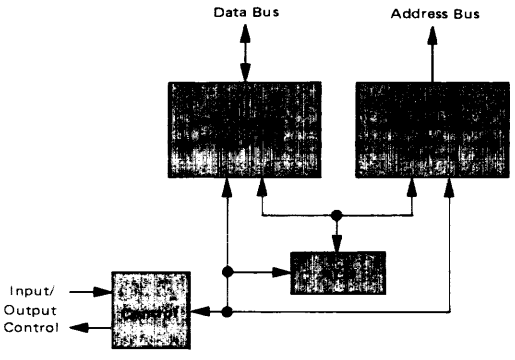
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 711

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6800 MICROPROCESSOR BLOCK DIAGRAM



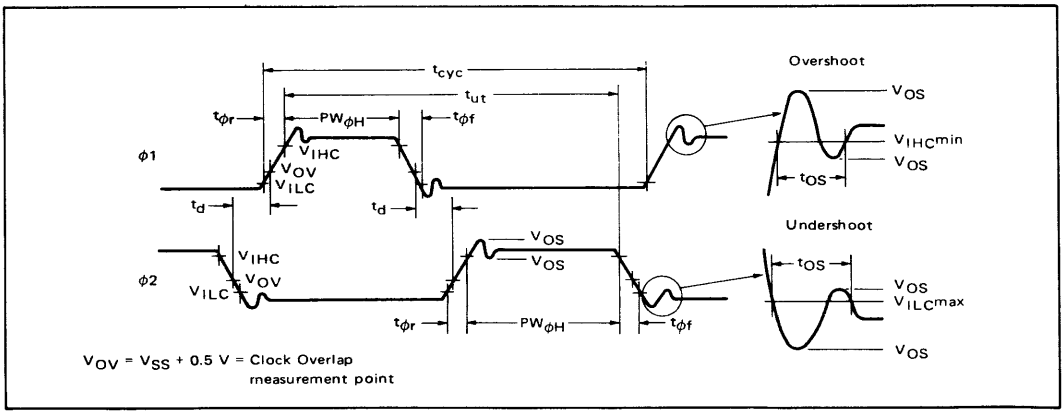
MC6800

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic	V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
	$\phi1,\phi2$	V_{IHC}	V_{CC} – 0.3	–	V_{CC} + 0.1	
Input Low Voltage	Logic	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	Vdc
	$\phi1,\phi2$	V_{ILC}	V_{SS} – 0.1	–	V_{SS} + 0.3	
Clock Overshoot/Undershoot – Input High Level		V_{OS}	V_{CC} – 0.5	–	V_{CC} + 0.5	Vdc
– Input Low Level			V_{SS} – 0.5	–	V_{SS} + 0.5	
Input Leakage Current		I_{in}				μAdc
(V_{in} = 0 to 5.25 V, V_{CC} = max)	Logic*		–	1.0	2.5	
(V_{in} = 0 to 5.25 V, V_{CC} = 0.0 V)	$\phi1,\phi2$		–	–	100	
Three-State (Off State) Input Current	D0-D7	I_{TSI}	–	2.0	10	μAdc
(V_{in} 0.4 to 2.4 V, V_{CC} = max)	A0-A15,R/W		–	–	100	
Output High Voltage		V_{OH}				Vdc
(I_{Load} = –205 μAdc, V_{CC} = min)	D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = –145 μAdc, V_{CC} = min)	A0-A15,R/W,VMA		V_{SS} + 2.4	–	–	
(I_{Load} = –100 μAdc, V_{CC} = min)	BA		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, V_{CC} = min)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Power Dissipation		P_D	–	0.600	1.2	W
Capacitance #	$\phi1,\phi2$	C_{in}	80	120	160	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	TSC		–	–	15	
	DBE		–	7.0	10	
	D0-D7		–	10	12.5	
	Logic Inputs		–	6.5	8.5	
	A0-A15,R/W,VMA	C_{out}	–	–	12	pF
Frequency of Operation		f	0.1	–	1.0	MHz
Clock Timing (Figure 1)						
Cycle Time		t_{cyc}	1.0	–	10	μs
Clock Pulse Width		$PW_{\phi H}$				ns
(Measured at V_{CC} – 0.3 V)	$\phi1$		430	–	4500	
	$\phi2$		450	–	4500	
Total $\phi1$ and $\phi2$ Up Time		t_{ut}	940	–	–	ns
Rise and Fall Times	$\phi1,\phi2$	$t_{\phi r}$, $t_{\phi f}$	5.0	–	50	ns
(Measured between V_{SS} + 0.3 V and V_{CC} – 0.3 V)						
Delay Time or Clock Separation		t_d	0	–	9100	ns
(Measured at V_{OV} = V_{SS} + 0.5 V)						
Overshoot Duration		t_{OS}	0	–	40	ns

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3 kΩ pullup load resistors for wire-OR capability at optimum operation.
#Capacitances are periodically sampled rather than 100% tested.

FIGURE 1 – CLOCK TIMING WAVEFORM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

READ/WRITE TIMING Figures 2 and 3, f = 1.0 MHz, Load Circuit of Figure 6.

Characteristic	Symbol	Min	Typ	Max	Unit
Address Delay	t_{AD}	–	220	300	ns
Peripheral Read Access Time $t_{acc} = t_{ut} - (t_{AD} + t_{DSR})$	t_{acc}	–	–	540	ns
Data Setup Time (Read)	t_{DSR}	100	–	–	ns
Input Data Hold Time	t_H	10	–	–	ns
Output Data Hold Time	t_H	10	25	–	ns
Address Hold Time (Address, R/W, VMA)	t_{AH}	50	75	–	ns
Enable High Time for DBE Input	t_{EH}	450	–	–	ns
Data Delay Time (Write)	t_{DDW}	–	165	225	ns
Processor Controls*					
Processor Control Setup Time	t_{PCS}	200	–	–	ns
Processor Control Rise and Fall Time	t_{PCr}, t_{PCf}	–	–	100	ns
Bus Available Delay	t_{BA}	–	–	300	ns
Three State Enable	t_{TSE}	–	–	40	ns
Three State Delay	t_{TSD}	–	–	700	ns
Data Bus Enable Down Time During $\phi 1$ Up Time (Figure 3)	$t_{\overline{DBE}}$	150	–	–	ns
Data Bus Enable Delay (Figure 3)	t_{DBED}	300	–	–	ns
Data Bus Enable Rise and Fall Times (Figure 3)	t_{DBEr}, t_{DBEf}	–	–	25	ns

*Additional information is given in Figures 12 through 16 of the Family Characteristics – see pages 17 through 20.

FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

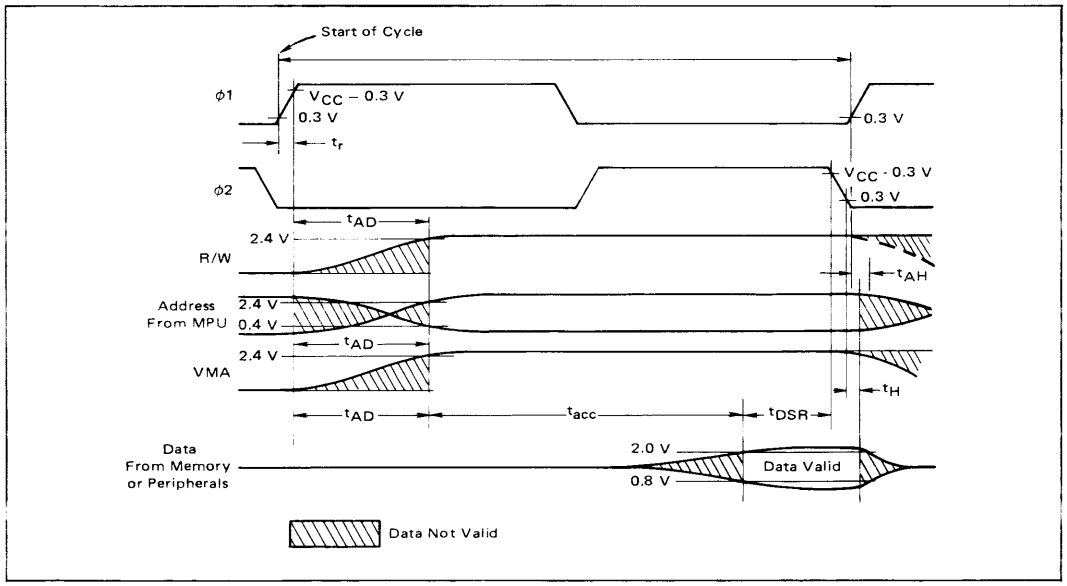


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FIGURE 3 – WRITE IN MEMORY OR PERIPHERALS

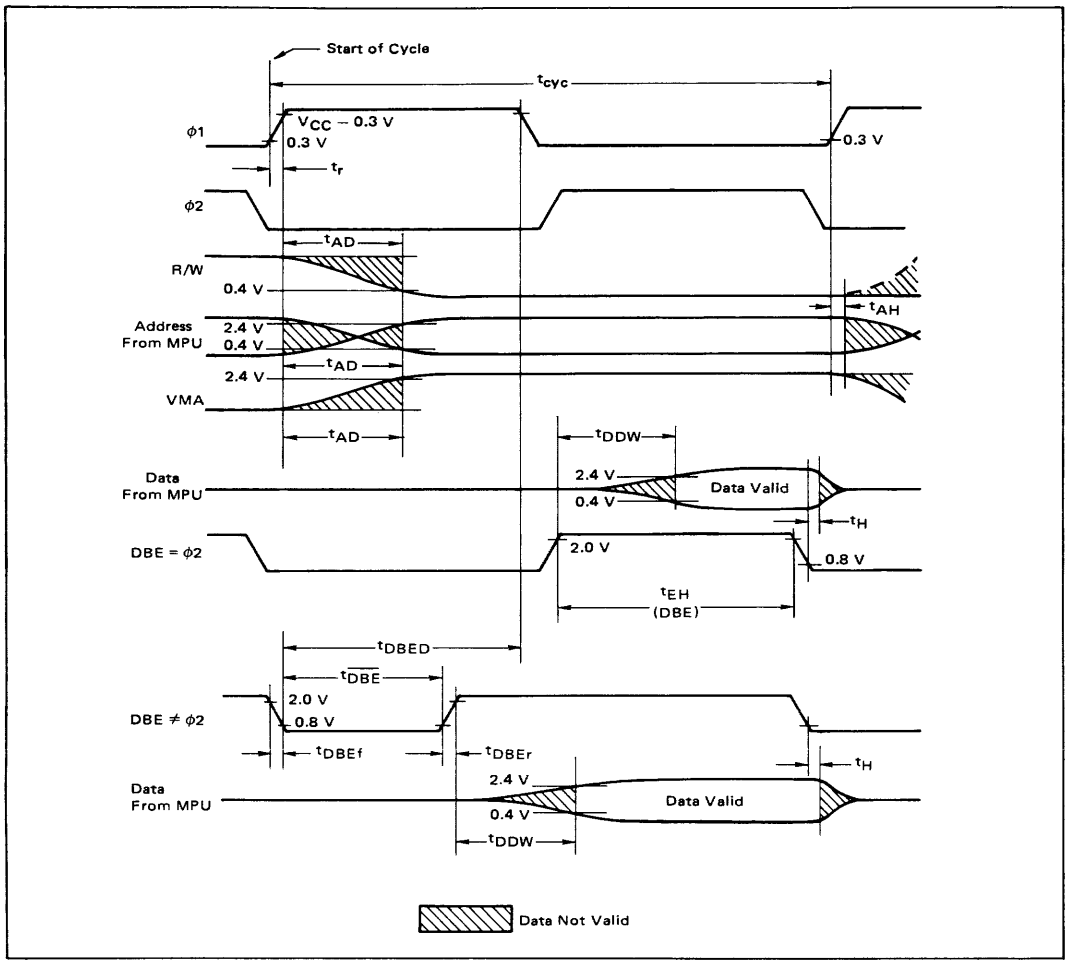

FIGURE 4 – TYPICAL DATA BUS OUTPUT DELAY versus CAPACITIVE LOADING

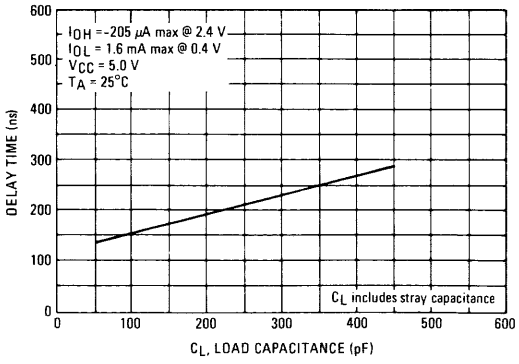

FIGURE 5 – TYPICAL READ/WRITE, VMA, AND ADDRESS OUTPUT DELAY versus CAPACITIVE LOADING

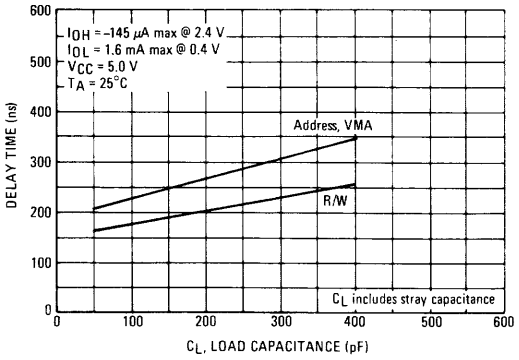

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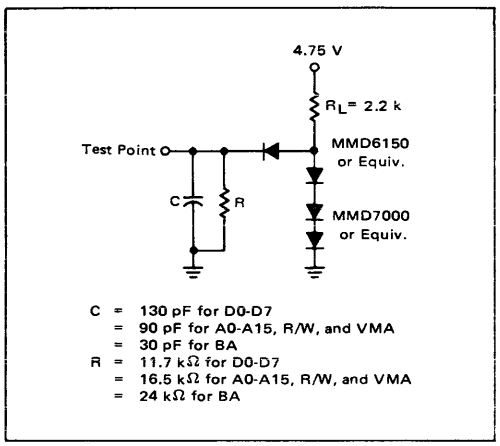
FIGURE 6 – BUS TIMING TEST LOAD



C = 130 pF for D0-D7
= 90 pF for A0-A15, R/W, and VMA
= 30 pF for BA
R = 11.7 kΩ for D0-D7
= 16.5 kΩ for A0-A15, R/W, and VMA
= 24 kΩ for BA

TYPICAL POWER SUPPLY CURRENT

FIGURE 7 – VARIATIONS WITH FREQUENCY

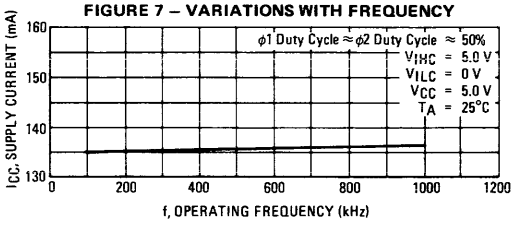
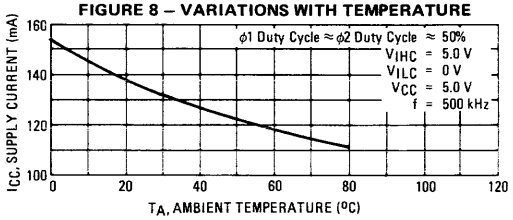
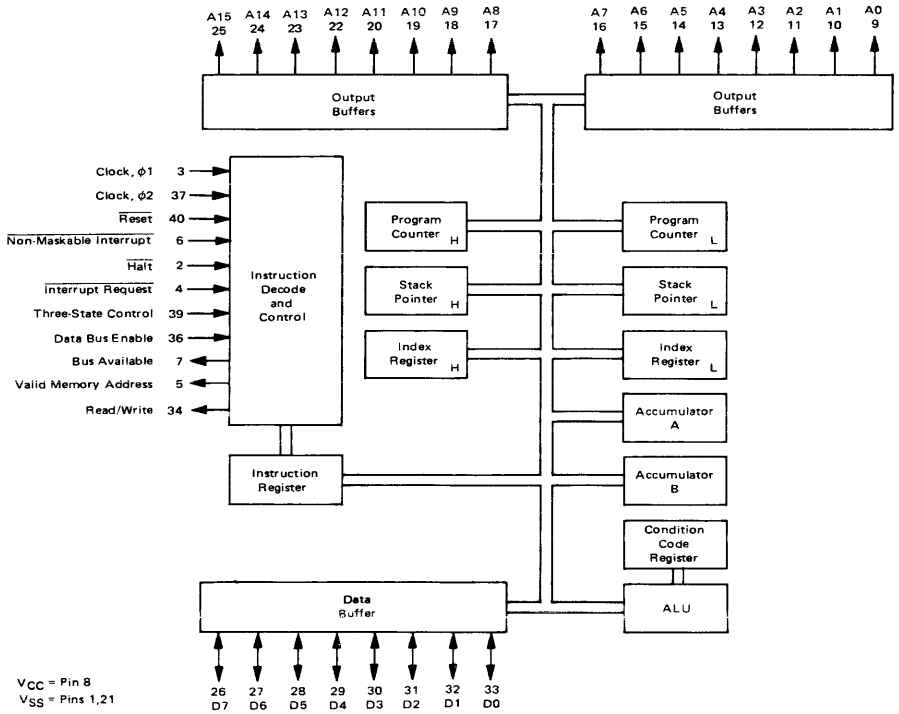


FIGURE 8 – VARIATIONS WITH TEMPERATURE



EXPANDED BLOCK DIAGRAM



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MPU SIGNAL DESCRIPTION

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor.

Clocks Phase One and Phase Two (ϕ1, ϕ2) – Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.

Address Bus (A0-A15) – Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.

Data Bus (D0-D7) – Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130 pF.

$\overline{\text{Halt}}$ – When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Clock cycle.

Three-State Control (TSC) – This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 700 ns after TSC = 2.0 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The ϕ1 clock must be held in the high state and the ϕ2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 4.5 μs or destruction of data will occur in the MPU.

Read/Write (R/W) – This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 90 pF.

Valid Memory Address (VMA) – This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90 pF may be directly driven by this active high signal.

Data Bus Enable (DBE) – This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it would be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.

Bus Available (BA) – The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$) – This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{Halt}}$ is low.

The $\overline{\text{IRQ}}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{\text{Reset}}$ – This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$.

Figure 9 shows the initialization of the microprocessor after restart. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts. If $\overline{\text{Reset}}$ goes high prior to the leading edge of $\phi 2$, on the next $\phi 1$ the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

Non-Maskable Interrupt ($\overline{\text{NMI}}$) – A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

Figure 10 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

FIGURE 9 – INITIALIZATION OF MPU AFTER RESTART

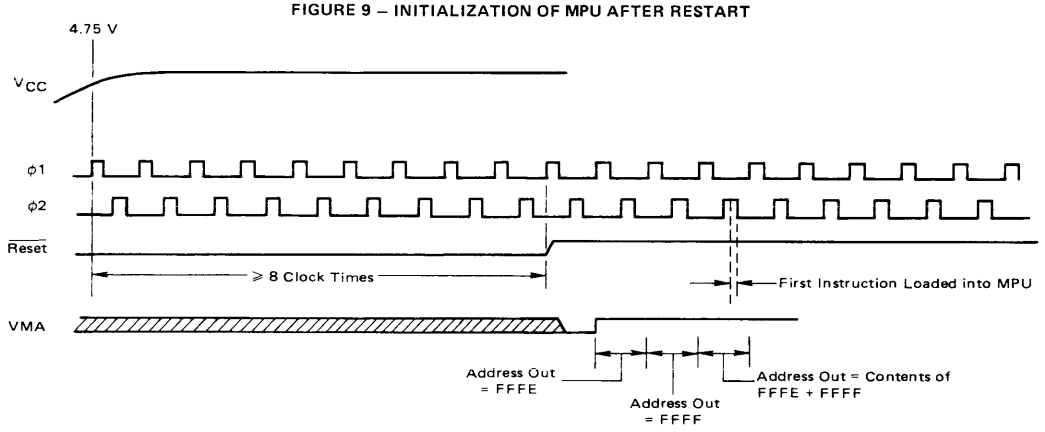
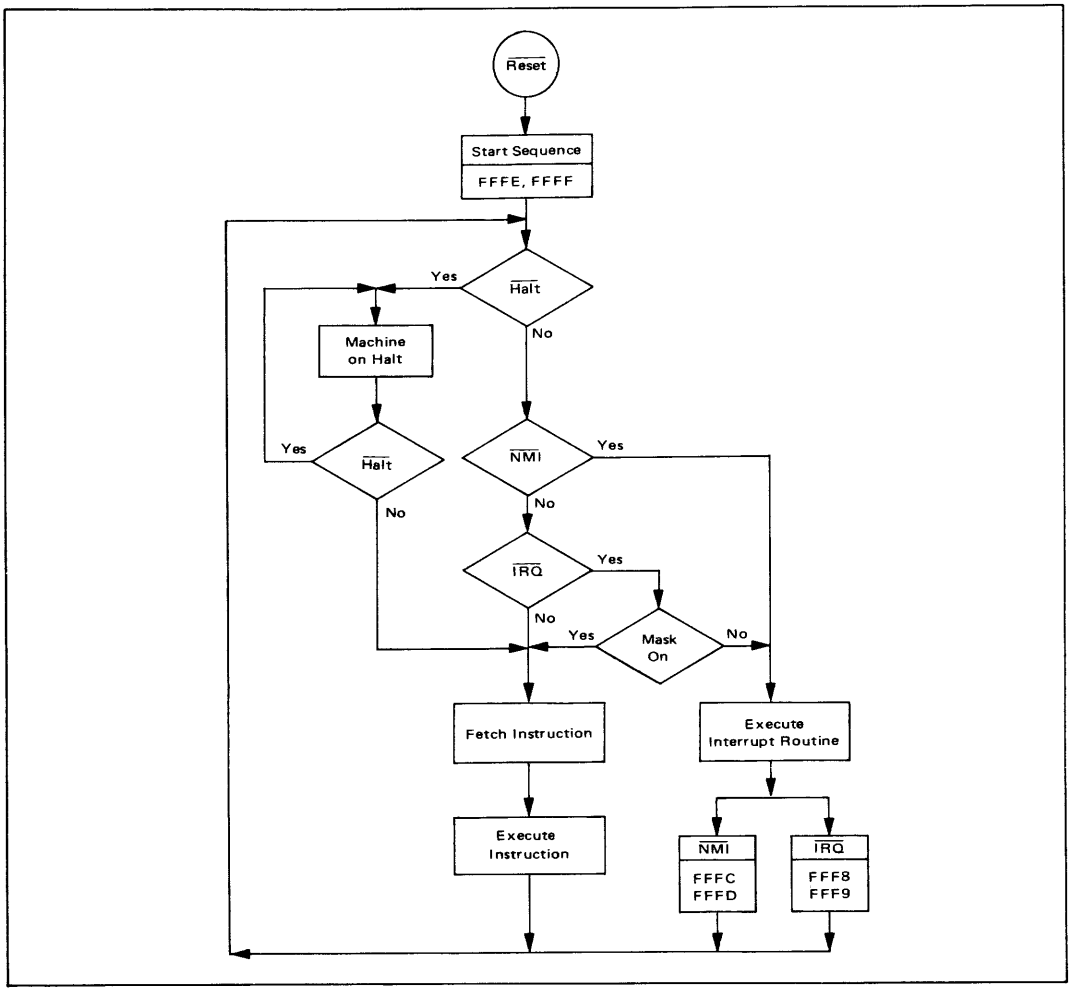


TABLE 1 – MEMORY MAP FOR INTERRUPT VECTORS

Vector MS	Vector LS	Description
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF8	FFF9	Interrupt Request

FIGURE 10 – MPU FLOW CHART



MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 11).

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

FIGURE 11 – PROGRAMMING MODEL OF THE MICROPROCESSING UNIT

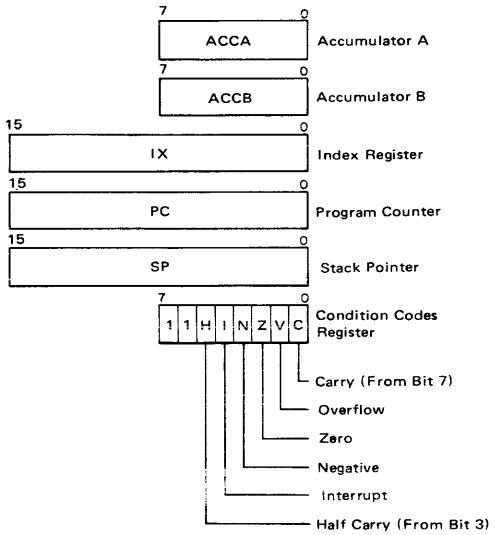
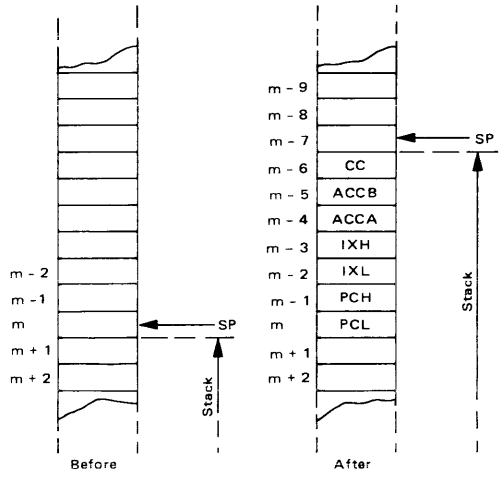


FIGURE 12 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits



Condition Code Register – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

Figure 12 shows the order of saving the microprocessor status within the stack.

MPU INSTRUCTION SET

The MC6800 has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions (Tables 2 thru 6).

MPU ADDRESSING MODES

The MC6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 7 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

Accumulator (ACCX) Addressing – In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing – In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MPU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing – In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

Extended Addressing – In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing – In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MPU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing – In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

Relative Addressing – In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of -125 to +129 bytes of the present instruction. These are two-byte instructions.

TABLE 2 – MICROPROCESSOR INSTRUCTION SET – ALPHABETIC SEQUENCE

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

TABLE 3 – ACCUMULATOR AND MEMORY INSTRUCTIONS

OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED =	DIRECT OP	DIRECT ~	DIRECT =	INDEX OP	INDEX ~	INDEX =	EXTND OP	EXTND ~	EXTND =	IMPLIED OP	IMPLIED ~	IMPLIED =	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	3B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				M̄ → M	•	•	↕	↕	R	S
	COMA													43	2	1	Ā → A	•	•	↕	↕	R	S
	COMB													53	2	1	B̄ → B	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 − M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 − A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 − B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M − 1 → M	•	•	↕	↕	④	•
	DECA													4A	2	1	A − 1 → A	•	•	↕	↕	④	•
	DECB													5A	2	1	B − 1 → B	•	•	↕	↕	④	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → M_{SP}, SP − 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B (C b7 b0)	•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A (C b7 b0)	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑦	↕
	ASLA													48	2	1	A (C b7 b0 0)	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A (b7 b0 C)	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A (0 b7 b0 C)	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A − M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B − M → B	•	•	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A − B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A − M − C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	F2	5	2	F2	4	3				B − M − C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test: Zero or Minus	TST							6D	7	2	7D	6	3				M − 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A − 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B − 00	•	•	↕	↕	R	R
																		H	I	N	Z	V	C

LEGEND:

OP Operation Code (Hexadecimal);
~ Number of MPU Cycles;
= Number of Program Bytes;
+ Arithmetic Plus;
− Arithmetic Minus;
· Boolean AND;
+ Boolean Inclusive OR;
⊕ Boolean Exclusive OR;
M̄ Complement of M;
→ Transfer Into;
0 Bit = Zero;
00 Byte = Zero;
M_{SP} Contents of memory location pointed to be Stack Pointer;

Note: Accumulator addressing mode instructions are included in the column for IMPLIED addressing.

CONDITION CODE SYMBOLS:

H Half-carry from bit 3;
I Interrupt mask
N Negative (sign bit)
Z Zero (byte)
V Overflow, 2's complement
C Carry from bit 7
R Reset Always
S Set Always
↕ Test and set if true, cleared otherwise
• Not Affected

TABLE 4 – INDEX REGISTER AND STACK MANIPULATION INSTRUCTIONS

		IMMED			DIRECT			INDEX			EXTND			IMPLIED				COND. CODE REG.					
																		5	4	3	2	1	0
POINTER OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BOOLEAN/ARITHMETIC OPERATION	H	I	N	Z	V	C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑧	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

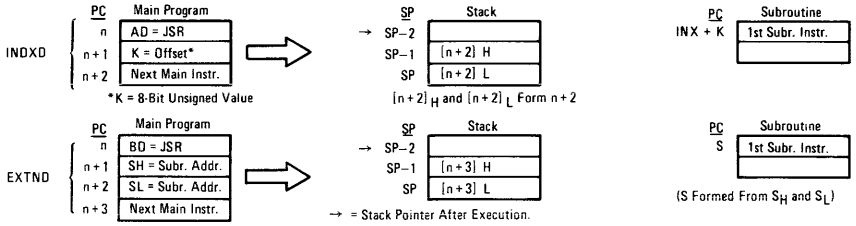
TABLE 5 – JUMP AND BRANCH INSTRUCTIONS

		RELATIVE			INDEX			EXTND			IMPLIED				COND. CODE REG.						
															5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BRANCH TEST	H	I	N	Z	V	C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										$N \oplus V = 0$	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										$Z + (N \oplus V) = 0$	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										$C + Z = 0$	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										$Z + (N \oplus V) = 1$	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										$C + Z = 1$	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										$N \oplus V = 1$	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		———		⑩			———
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait for Interrupt*	WAI										3E	9	1		•	⑪	•	•	•	•

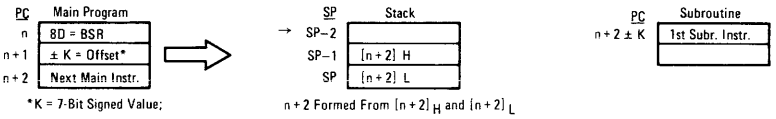
*WAI puts Address Bus, R/W, and Data Bus in the three-state mode while VMA is held low.

SPECIAL OPERATIONS

JSR, JUMP TO SUBROUTINE:

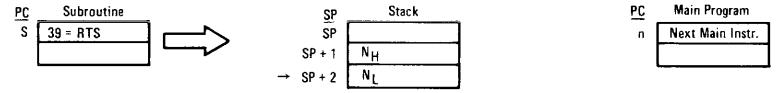


BSR, BRANCH TO SUBROUTINE:



JMP, JUMP:

RTS, RETURN FROM SUBROUTINE:



RTI, RETURN FROM INTERRUPT:

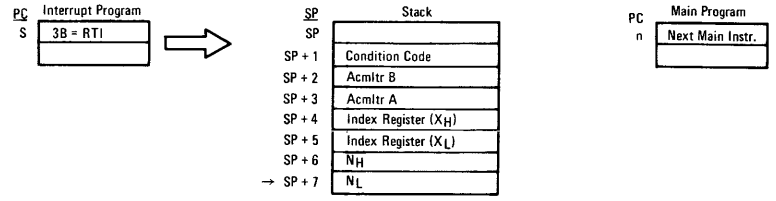


TABLE 6 – CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

		IMPLIED				COND. CODE REG.					
						5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	BOOLEAN OPERATION	H	I	N	Z	V	C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	A → CCR	——— (12) ———					
CCR → Acmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise)

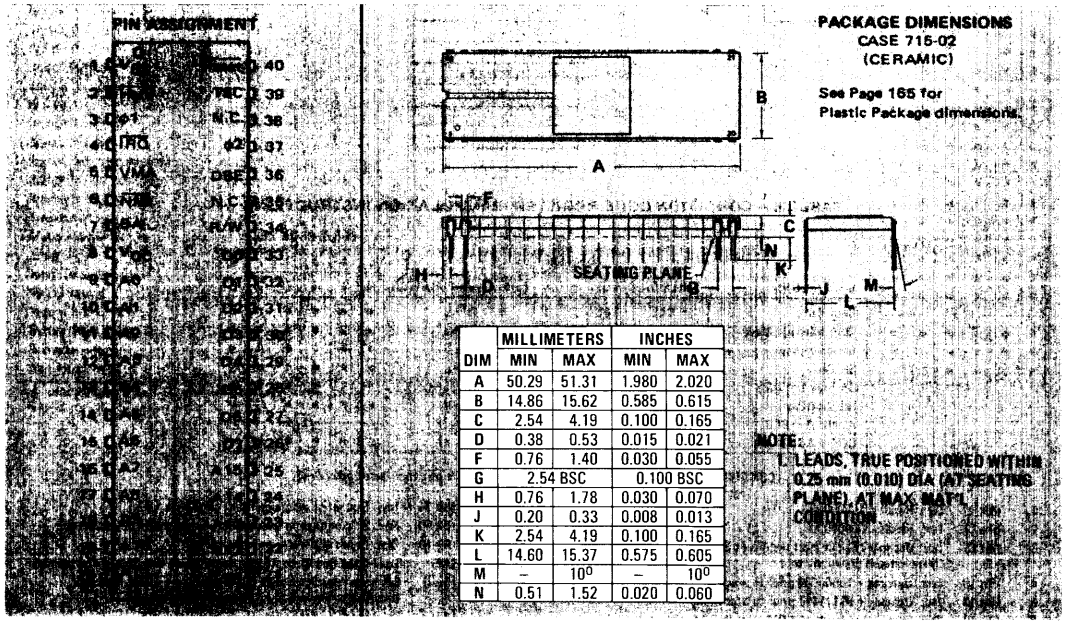
1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

TABLE 7 – INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES
(Times in Machine Cycles)

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied	Relative
ABA		•	•	•	•	•	2	•
ADC	x	•	2	3	4	5	•	•
ADD	x	•	2	3	4	5	•	•
AND	x	•	2	3	4	5	•	•
ASL		2	•	•	6	7	•	•
ASR		2	•	•	6	7	•	•
BCC		•	•	•	•	•	•	4
BCS		•	•	•	•	•	•	4
BEA		•	•	•	•	•	•	4
BGE		•	•	•	•	•	•	4
BGT		•	•	•	•	•	•	4
BHI		•	•	•	•	•	•	4
BIT	x	•	2	3	4	5	•	•
BLE		•	•	•	•	•	•	4
BLS		•	•	•	•	•	•	4
BLT		•	•	•	•	•	•	4
BMI		•	•	•	•	•	•	4
BNE		•	•	•	•	•	•	4
BPL		•	•	•	•	•	•	4
BRA		•	•	•	•	•	•	4
BSR		•	•	•	•	•	•	8
BVC		•	•	•	•	•	•	4
BVS		•	•	•	•	•	•	4
CBA		•	•	•	•	•	2	•
CLC		•	•	•	•	•	2	•
CLI		•	•	•	•	•	2	•
CLR		2	•	•	6	7	•	•
CLV		•	•	•	•	•	2	•
CMP	x	•	2	3	4	5	•	•
COM		2	•	•	6	7	•	•
CPX		•	3	4	5	6	•	•
DAA		•	•	•	•	•	2	•
DEC		2	•	•	6	7	•	•
DES		•	•	•	•	•	4	•
DEX		•	•	•	•	•	4	•
EOR	x	•	2	3	4	5	•	•

	(Dual Operand)	ACCX	Immediate	Direct	Extended	Indexed	Implied
INC		2	•	•	6	7	•
INS		•	•	•	•	•	4
INX		•	•	•	•	•	4
JMP		•	•	•	3	4	•
JSR		•	•	•	9	8	•
LDA	x	•	2	3	4	5	•
LDS		•	3	4	5	6	•
LDX		•	3	4	5	6	•
LSR		2	•	•	6	7	•
NEG		2	•	•	6	7	•
NOP		•	•	•	•	•	2
ORA	x	•	2	3	4	5	•
PSH		•	•	•	•	•	4
PUL		•	•	•	•	•	4
ROL		2	•	•	6	7	•
ROR		2	•	•	6	7	•
RTI		•	•	•	•	•	10
RTS		•	•	•	•	•	5
SBA		•	•	•	•	•	2
SBC	x	•	2	3	4	5	•
SEC		•	•	•	•	•	2
SEI		•	•	•	•	•	2
SEV		•	•	•	•	•	2
STA	x	•	•	4	5	6	•
STS		•	•	5	6	7	•
STX		•	•	5	6	7	•
SUB	x	•	2	3	4	5	•
SWI		•	•	•	•	•	12
TAB		•	•	•	•	•	2
TAP		•	•	•	•	•	2
TBA		•	•	•	•	•	2
TPA		•	•	•	•	•	2
TST		2	•	•	6	7	•
TSX		•	•	•	•	•	4
TSX		•	•	•	•	•	4
WAI		•	•	•	•	•	9

NOTE: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

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SUMMARY OF CYCLE BY CYCLE OPERATION

Table 8 provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the control program is executed. The information is categorized in groups according to Addressing Mode and Number of Cycles per instruction. (In general, instructions with the same Addressing Mode and Number of Cycles execute in the same manner; exceptions are indicated in the table.)

TABLE 8 – OPERATION SUMMARY

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data
CPX LDS LDX	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data (High Order Byte)
		3	1	Op Code Address + 2	1	Operand Data (Low Order Byte)
DIRECT						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data
CPX LDS LDX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data (High Order Byte)
		4	1	Operand Address + 1	1	Operand Data (Low Order Byte)
STA	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address
		3	0	Destination Address	1	Irrelevant Data (Note 1)
		4	1	Destination Address	0	Data from Accumulator
STS STX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	0	Address of Operand	1	Irrelevant Data (Note 1)
		4	1	Address of Operand	0	Register Data (High Order Byte)
		5	1	Address of Operand + 1	0	Register Data (Low Order Byte)
INDEXED						
JMP	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data
CPX LDS LDX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data (High Order Byte)
		6	1	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)

MC6800

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INDEXED (Continued)						
STA	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Current Operand Data
		6	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		7	1/0 (Note 3)	Index Register Plus Offset	0	New Operand Data (Note 3)
STS STX	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data (High Order Byte)
		7	1	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
JSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Index Register	1	Irrelevant Data (Note 1)
		8	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
EXTENDED						
JMP	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	1	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data
CPX LDS LDX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data (High Order Byte)
		5	1	Address of Operand + 1	1	Operand Data (Low Order Byte)
STA A STA B	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	1	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	0	Operand Destination Address	1	Irrelevant Data (Note 1)
		5	1	Operand Destination Address	0	Data from Accumulator
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Current Operand Data
		5	0	Address of Operand	1	Irrelevant Data (Note 1)
		6	1/0 (Note 3)	Address of Operand	0	New Operand Data (Note 3)

MC6800

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
EXTENDED (Continued)						
STS STX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	0	Address of Operand	1	Irrelevant Data (Note 1)
		5	1	Address of Operand	0	Operand Data (High Order Byte)
		6	1	Address of Operand + 1	0	Operand Data (Low Order Byte)
JSR	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	1	Subroutine Starting Address	1	Op Code of Next Instruction
		5	1	Stack Pointer	0	Return Address (Low Order Byte)
		6	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		7	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		8	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		9	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
INHERENT						
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
DES DEX INS INX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Previous Register Contents	1	Irrelevant Data (Note 1)
		4	0	New Register Contents	1	Irrelevant Data (Note 1)
PSH	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Accumulator Data
		4	0	Stack Pointer – 1	1	Accumulator Data
PUL	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Operand Data from Stack
TSX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	0	New Index Register	1	Irrelevant Data (Note 1)
TXS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	0	Index Register	1	Irrelevant Data
		4	0	New Stack Pointer	1	Irrelevant Data
RTS	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Address of Next Instruction (High Order Byte)
		5	1	Stack Pointer + 2	1	Address of Next Instruction (Low Order Byte)

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MC6800

TABLE 8 – OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INHERENT (Continued)						
WAI	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6 (Note 4)	1	Contents of Cond. Code Register
RTI	10	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Contents of Cond. Code Register from Stack
		5	1	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	1	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	1	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	1	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	1	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	1	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 1)
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer – 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer – 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer – 4	0	Contents of Accumulator A
		8	1	Stack Pointer – 5	0	Contents of Accumulator B
		9	1	Stack Pointer – 6	0	Contents of Cond. Code Register
		10	0	Stack Pointer – 7	1	Irrelevant Data (Note 1)
		11	1	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	1	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE						
BCC BHI BNE BCS BLE BPL BEQ BLS BRA BGE BLT BVC BGT BMI BVS	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		4	0	Branch Address	1	Irrelevant Data (Note 1)
BSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer – 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer – 2	1	Irrelevant Data (Note 1)
		7	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		8	0	Subroutine Address	1	Irrelevant Data (Note 1)

Note 1. If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.
Note 2. Data is ignored by the MPU.
Note 3. For TST, VMA = 0 and Operand data does not change.
Note 4. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low; Address Bus, R/W, and Data Bus are all in the high impedance state.

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MC6820
(0 to 70°C; L or P Suffix)
MC6820C
(-40 to 85°C; L Suffix only)

PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

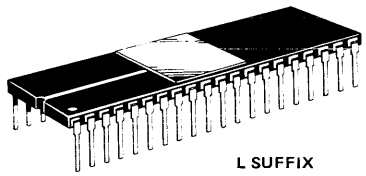
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines

MOS

(N-CHANNEL, SILICON-GATE)

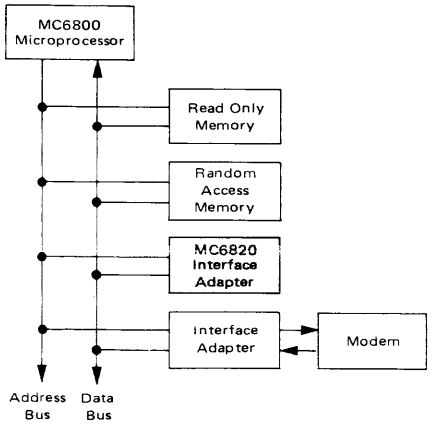
PERIPHERAL INTERFACE ADAPTER



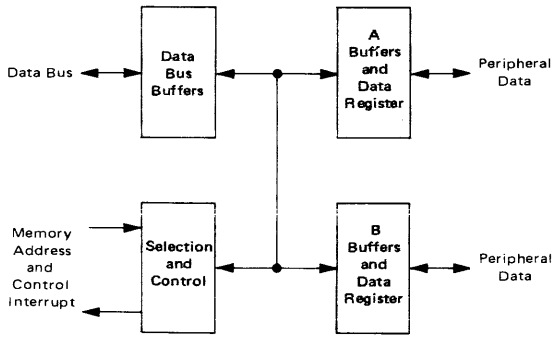
L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 711

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6820 PERIPHERAL INTERFACE ADAPTER BLOCK DIAGRAM



MC6820

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage — Enable	V_{IH}	V_{SS} + 2.4	–	V_{CC}	Vdc
Input High Voltage — Other Inputs		V_{SS} + 2.0	–	V_{CC}	
Input Low Voltage — Enable	V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.4	Vdc
Input Low Voltage — Other Inputs		V_{SS} -0.3	–	V_{SS} + 0.8	
Input Leakage Current (R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable) (V_{in} = 0 to 5.25 Vdc)	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (D0-D7, PB0-PB7, CB2) (V_{in} = 0.4 to 2.4 Vdc)	I_{TSI}	–	2.0	10	μAdc
Input High Current (PA0-PA7, CA2) (V_{IH} = 2.4 Vdc)	I_{IH}	-100	-250	–	μAdc
Input Low Current (PA0-PA7, CA2) (V_{IL} = 0.4 Vdc)	I_{IL}	–	-1.0	-1.6	mAdc
Output High Voltage	V_{OH}				Vdc
(I_{Load} = -205 μAdc, Enable Pulse Width < 25 μs) D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs) Other Outputs		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width < 25 μs)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc) D0-D7		-205	–	–	μAdc
Other Outputs		-100	–	–	μAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2		-1.0	-2.5	-10	mAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Output Leakage Current (Off State) ($\overline{IRQA}$, $\overline{IRQB}$) (V_{OH} = 2.4 Vdc)	I_{LOH}	–	1.0	10	μAdc
Power Dissipation	P_D	–	–	650	mW
Input Capacitance — Enable	C_{in}	–	–	20	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7		–	–	12.5	
PA0-PA7, PB0-PB7, CA2, CB2		–	–	10	
R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1		–	–	7.5	
Output Capacitance ($\overline{IRQA}$, $\overline{IRQB}$)	C_{out}	–	–	5.0	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) PB0-PB7		–	–	10	
Peripheral Data Setup Time (Figure 1)	t_{PDSU}	200	–	–	ns
Delay Time, Enable negative transition to CA2 negative transition (Figure 2, 3)	t_{CA2}	–	–	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition (Figure 2)	t_{RS1}	–	–	1.0	μs
Rise and Fall Times for CA1 and CA2 input signals (Figure 3)	t_r,t_f	–	–	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition (Figure 3)	t_{RS2}	–	–	2.0	μs
Delay Time, Enable negative transition to Peripheral Data valid (Figures 4, 5)	t_{PDW}	–	–	1.0	μs
Delay Time, Enable negative transition to Peripheral CMOS Data Valid (V_{CC} – 30% V_{CC}, Figure 4; Figure 12 Load C) PA0-PA7, CA2	t_{CMOS}	–	–	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition (Figure 6, 7)	t_{CB2}	–	–	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition (Figure 5)	t_{DC}	20	–	–	ns
Delay Time, Enable positive transition to CB2 positive transition (Figure 6)	t_{RS1}	–	–	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals (Figure 7)	t_r,t_f	–	–	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition (Figure 7)	t_{RS2}	–	–	2.0	μs
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$ (Figure 8)	t_{IR}	–	–	1.6	μs
Reset Low Time* (Figure 9)	t_{RL}	2.0	–	–	μs

*The Reset line must be high a minimum of 1.0 μs before addressing the PIA.

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MC6820

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BUS TIMING CHARACTERISTICS

READ (Figures 10 and 12)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

WRITE (Figures 11 and 12)

Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Setup Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

FIGURE 1 – PERIPHERAL DATA SETUP TIME
(Read Mode)

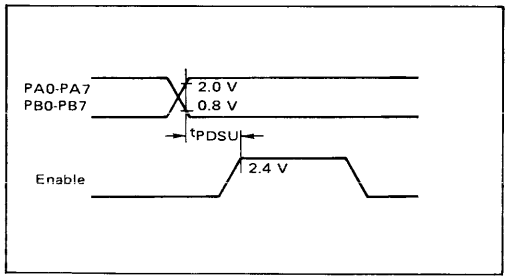
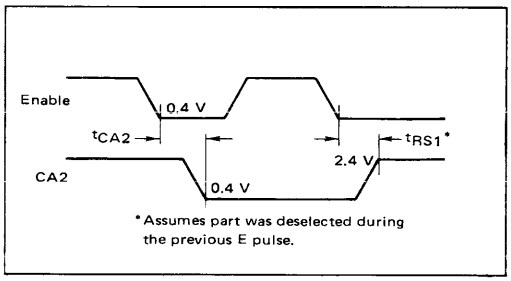


FIGURE 2 – CA2 DELAY TIME
(Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 3 – CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

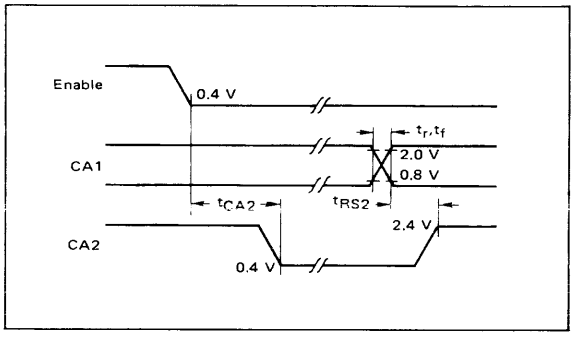


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FIGURE 4 – PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

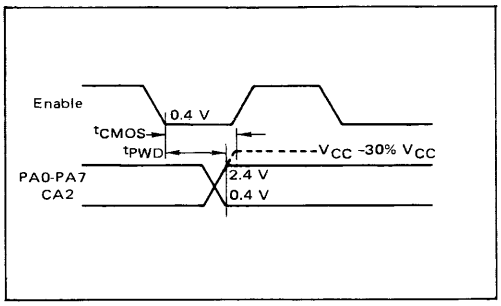

FIGURE 5 – PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

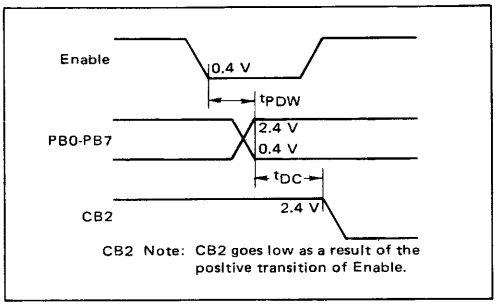

FIGURE 6 – CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

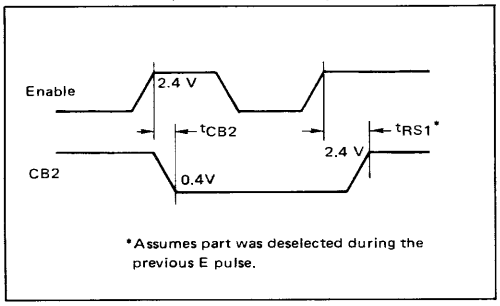

FIGURE 7 – CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)

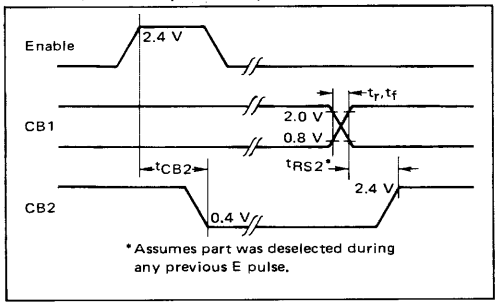

FIGURE 8 – $\overline{IRQ}$ RELEASE TIME

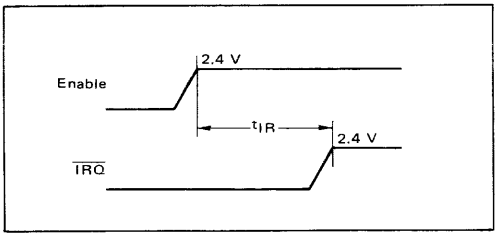

FIGURE 9 – $\overline{RESET}$ LOW TIME

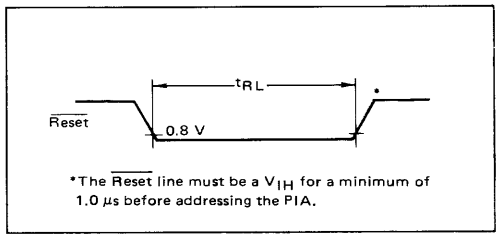

FIGURE 10 – BUS READ TIMING CHARACTERISTICS
(Read Information from PIA)

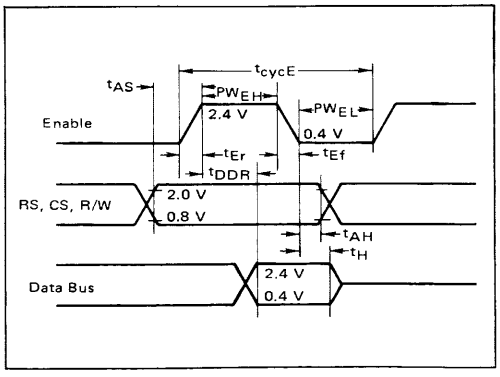

FIGURE 11 – BUS WRITE TIMING CHARACTERISTICS
(Write Information into PIA)

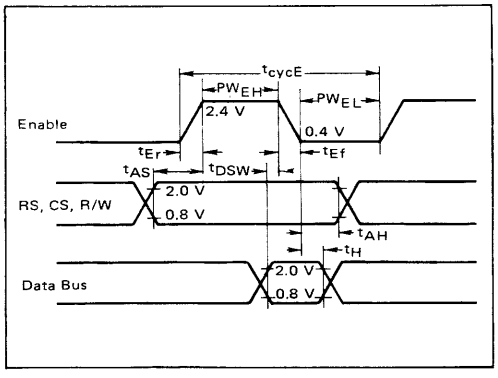

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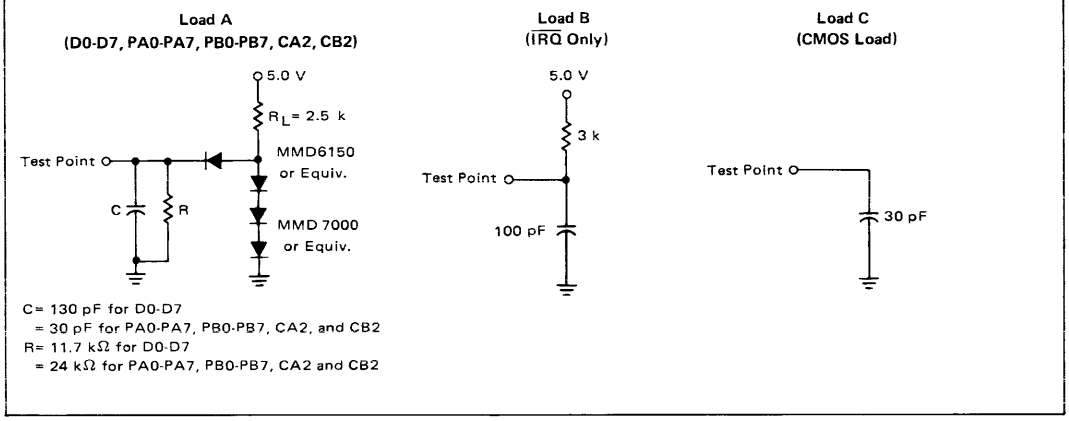
FIGURE 12 – BUS TIMING TEST LOADS



PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the MC6800 MPU with an eight-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the PIA. VMA should be utilized in conjunction with an MPU address line into a chip select of the PIA.

PIA Bi-Directional Data (D0-D7) – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.

PIA Enable (E) – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock.

PIA Read/Write (R/W) – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

$\overline{\text{Reset}}$ – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

PIA Chip Select (CS0, CS1 and $\overline{\text{CS2}}$) – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

PIA Register Select (RS0 and RS1) – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) – The active low $\overline{\text{Interrupt Request}}$ lines ($\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

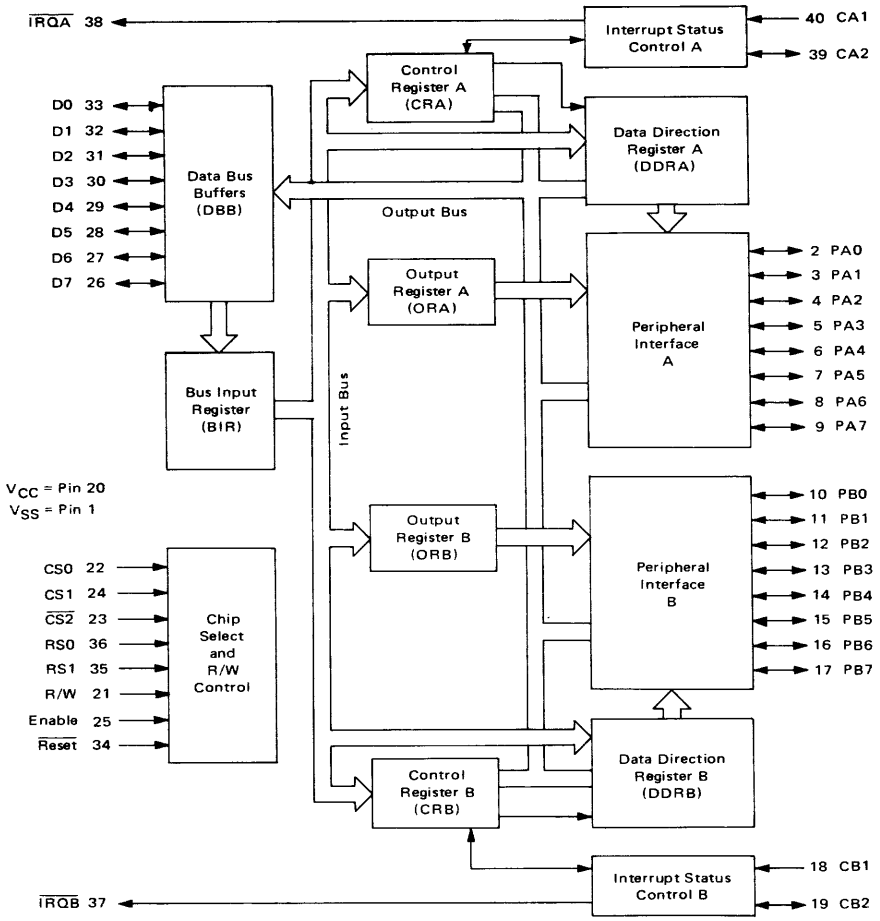
Each $\overline{\text{Interrupt Request}}$ line has two internal interrupt flag bits that can cause the $\overline{\text{Interrupt Request}}$ line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an

MC6820

EXPANDED BLOCK DIAGRAM



MOTOROLA Semiconductor Products Inc.

MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bi-directional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0-PA7) – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0-PB7) – The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) – Peripheral Input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

NOTE: It is recommended that the control lines (CA1, CA2, CB1, CB2) should be held in a logic 1 state when $\overline{\text{Reset}}$ is active to prevent setting of corresponding interrupt flags in the control register when $\overline{\text{Reset}}$ goes to an inactive state. Subsequent to $\overline{\text{Reset}}$ going inactive, a read of the data registers may be used to clear any undesired interrupt flags.

INTERNAL CONTROLS

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Details of possible configurations of the Data Direction and Control Register are as follows.

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. A Data Direction Register bit set at "0" configures the corresponding peripheral data line as an input; a "1" results in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

Notes: 1. ↑ indicates positive transition (low to high)

2. ↓ indicates negative transition (high to low)

3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.

4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-0 (CRB-0) is written to a "one".

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) – The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

Notes: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs after CRA-3 (CRB-3) is written to a "one".

TABLE 5 – CONTROL OF CB2 AS AN OUTPUT
CRB-5 is high

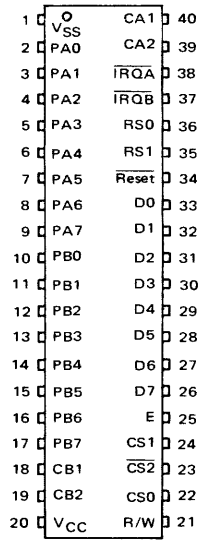
CRB-5	CRB-4	CRB-3	CB2 Cleared	CB2 Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal.
1	0	1	Low on the positive transition of the first E pulse after an MPU Write "B" Data Register operation.	High on the positive edge of the first "E" pulse following an "E" pulse which occurred while the part was deselected.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU Write into Control Register "B".

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 6 – CONTROL OF CA-2 AS AN OUTPUT
CRA-5 is high

CRA-5	CRA-4	CRA-3	CA2 Cleared	CA2 Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High when the interrupt flag bit CRA-7 is set by an active transition of the CA1 signal.
1	0	1	Low on negative transition of E after an MPU Read "A" Data operation.	High on the negative edge of the first "E" pulse which occurs during a deselect.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write to Control Register "A".	Always low as long as CRA-3 is low. Will go high on an MPU Write to Control Register "A" that changes CRA-3 to "one".
1	1	1	Always high as long as CRA-3 is high. Will be cleared on an MPU Write to Control Register "A" that clears CRA-3 to a "zero".	High when CRA-3 goes high as a result of an MPU Write to Control Register "A".

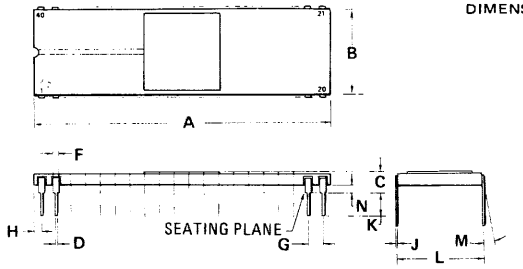
PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 715-02
(CERAMIC)

SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS.



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.60	15.37	0.575	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX. MAT'L CONDITION.

MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC6850

(0 to 70°C; L or P Suffix)

MC6850C

(-40 to 85°C; L Suffix only)

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

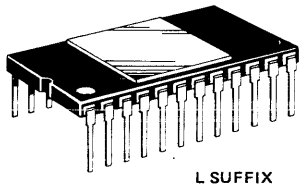
The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- Eight and Nine-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500 kbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One or Two Stop Bit Operation

MOS

(N-CHANNEL, SILICON-GATE)

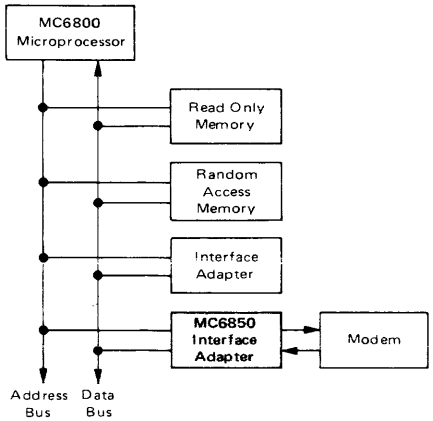
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER



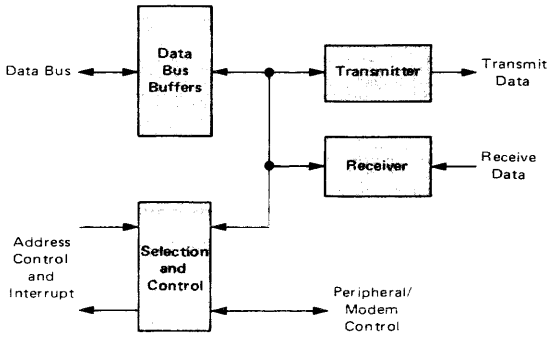
L SUFFIX
CERAMIC PACKAGE
CASE 716

NOT SHOWN: **P SUFFIX**
PLASTIC PACKAGE
CASE 709

M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Thermal Resistance	θ_{JA}	82.5	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	R/W,CS0,CS1,$\overline{CS2}$,Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc)	D0-D7	I_{TSI}	–	2.0	10	μAdc
Output High Voltage	D0-D7	V_{OH}				Vdc
(I_{Load} = -205 μAdc, Enable Pulse Width <25 μs)			V_{SS} + 2.4	–	–	
(I_{Load} = -100 μAdc, Enable Pulse Width <25 μs)	Tx Data, $\overline{RTS}$		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width <25 μs)		V_{OL}	–	-	V_{SS} + 0.4	Vdc
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	μAdc
Power Dissipation		P_D	–	300	525	mW
Input Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7		–	10	12.5	
	E, Tx Clk, Rx Clk, R/W, RS, Rx Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$		–	7.0	7.5	
Output Capacitance	$\overline{RTS}$, Tx Data	C_{out}	–	–	10	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	$\overline{IRQ}$		–	–	5.0	
Minimum Clock Pulse Width, Low (Figure 1)	÷16, ÷64 Modes	PW_{CL}	600	–	–	ns
Minimum Clock Pulse Width, High (Figure 2)	÷16, ÷64 Modes	PW_{CH}	600	–	–	ns
Clock Frequency	÷1 Mode	f_C	–	–	500	kHz
	÷16, ÷64 Modes		–	–	800	
Clock-to-Data Delay for Transmitter (Figure 3)		t_{TDD}	–	–	1.0	μs
Receive Data Setup Time (Figure 4)	÷1 Mode	t_{RDSU}	500	–	–	ns
Receive Data Hold Time (Figure 5)	÷1 Mode	t_{RDH}	500	–	–	ns
$\overline{Interrupt\ Request}$ Release Time (Figure 6)		t_{IR}	–	–	1.2	μs
$\overline{Request\text{-}to\text{-}Send}$ Delay Time (Figure 6)		t_{RTS}	–	–	1.0	μs
Input Transition Times (Except Enable)		t_r,t_f	–	–	1.0*	μs

*1.0 μs or 10% of the pulse width, whichever is smaller.

BUS TIMING CHARACTERISTICS

READ (Figures 7 and 9)

Characteristic	Symbol	Min	Typ	Max	Unit
Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Delay Time	t_{DDR}	–	–	320	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

WRITE (Figure 8 and 9)

Enable Cycle Time	t_{cycE}	1.0	–	–	μs
Enable Pulse Width, High	PW_{EH}	0.45	–	25	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	–	μs
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	–	ns
Data Setup Time	t_{DSW}	195	–	–	ns
Data Hold Time	t_H	10	–	–	ns
Address Hold Time	t_{AH}	10	–	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	–	25	ns

MOTOROLA Semiconductor Products Inc.

MC6850

FIGURE 1 – CLOCK PULSE WIDTH, LOW-STATE

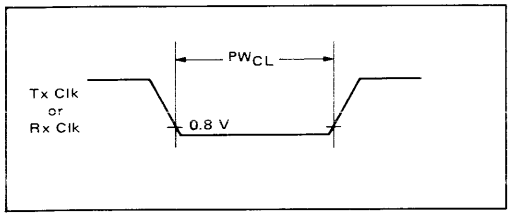


FIGURE 2 – CLOCK PULSE WIDTH, HIGH-STATE

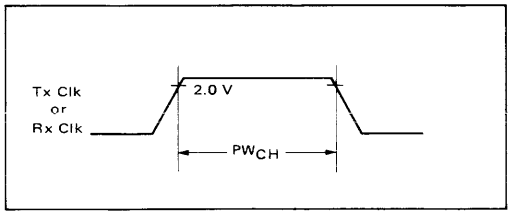


FIGURE 3 – TRANSMIT DATA OUTPUT DELAY

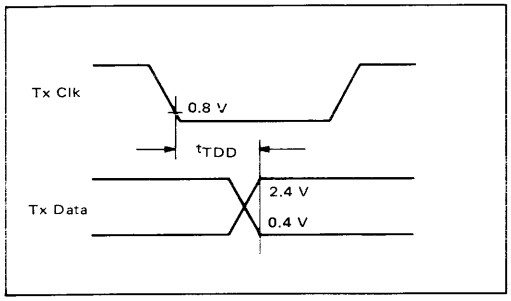


FIGURE 4 – RECEIVE DATA SETUP TIME
(÷1 Mode)

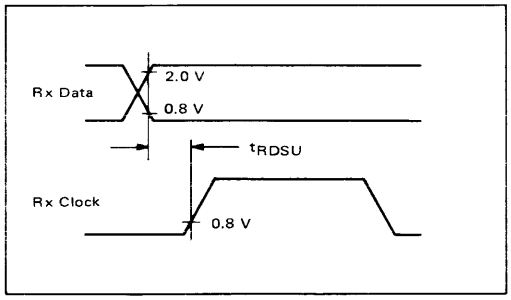


FIGURE 5 – RECEIVE DATA HOLD TIME
(÷1 Mode)

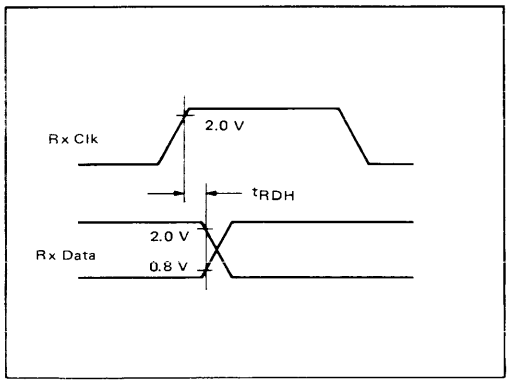


FIGURE 6 – $\overline{\text{REQUEST-TO-SEND}}$ DELAY AND $\overline{\text{INTERRUPT-REQUEST}}$ RELEASE TIMES

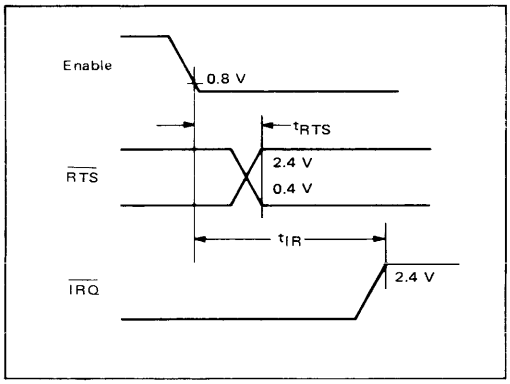


FIGURE 7 – BUS READ TIMING CHARACTERISTICS
(Read information from ACIA)

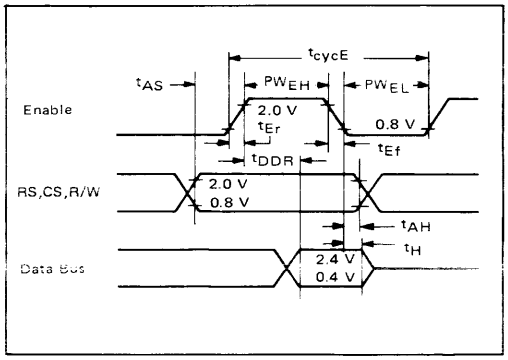


FIGURE 8 – BUS WRITE TIMING CHARACTERISTICS
(Write information into ACIA)

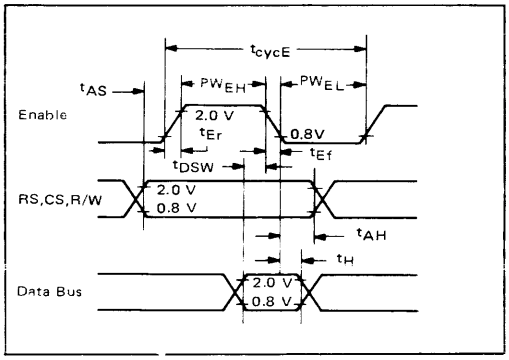


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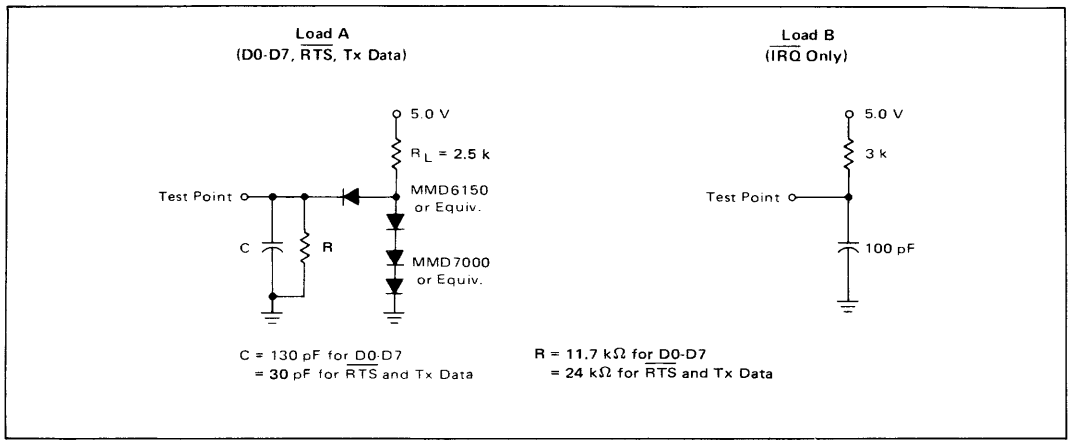
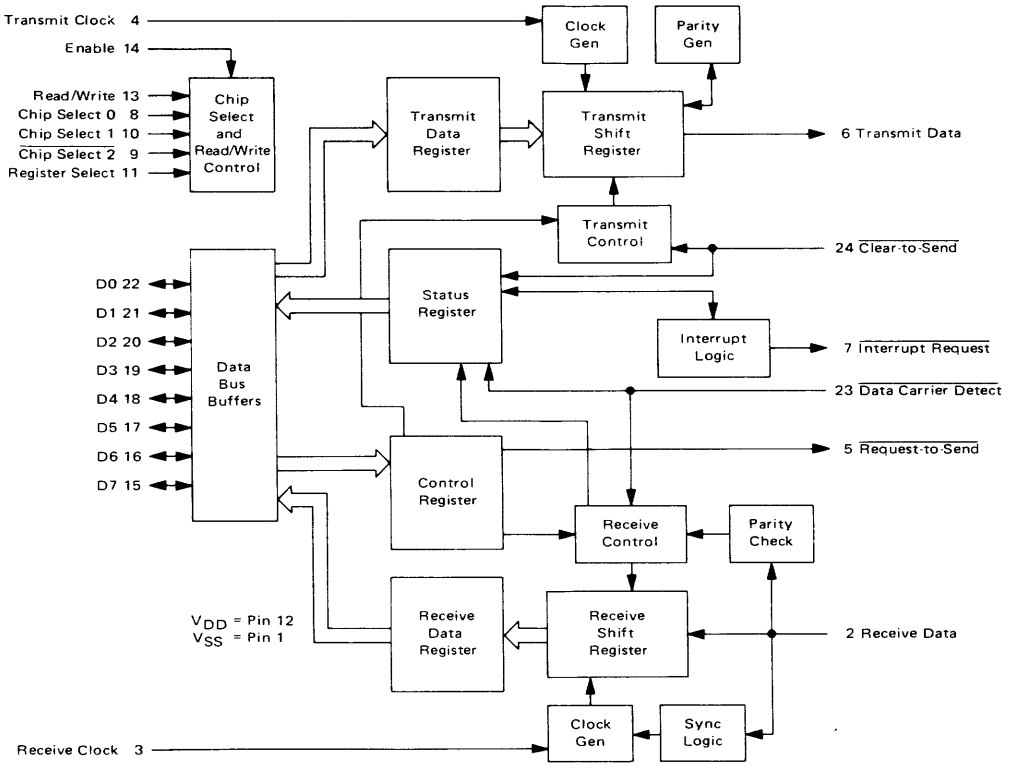
FIGURE 9 – BUS TIMING TEST LOADS



EXPANDED BLOCK DIAGRAM



DEVICE OPERATION

At the bus interface, the ACIA appears as two addressable memory locations. Internally, there are four registers: two read-only and two write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and three peripheral/modem control lines.

POWER ON/MASTER RESET

The master reset (CR0, CR1) should be set during system initialization to insure the reset condition and prepare for programming the ACIA functional configuration when the communications channel is required. Control bits CR5 and CR6 should also be programmed to define the state of $\overline{RTS}$ whenever master reset is utilized. The ACIA also contains internal power-on reset logic to detect the power line turn-on transition and hold the chip in a reset state to prevent erroneous output transitions prior to initialization. This circuitry depends on clean power turn-on transitions. The power-on reset is released by means of the bus-programmed master reset which must be applied prior to operating the ACIA. After master resetting the ACIA, the programmable Control Register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none), etc.

TRANSMIT

A typical transmitting sequence consists of reading the ACIA Status Register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmit Data Register if the status read operation has indicated that the Transmit Data Register is empty. This character is transferred to a Shift Register where it is serialized and transmitted from the Transmit Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the Data Register, the Status Register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted (because of double buffering). The second character will be automatically transferred into the Shift Register when the first character transmission is completed. This sequence continues until all the characters have been transmitted.

RECEIVE

Data is received from a peripheral by means of the Receive Data input. A divide-by-one clock ratio is provided for an externally synchronized clock (to its data) while the divide-by-16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide-by-16 and 64 modes is initiated by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the Status Register along with framing error, overrun error, and Receive Data Register full. In a typical receiving sequence, the Status Register is read to determine if a character has been received from a peripheral. If the Receiver Data Register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. When parity has been selected for an 8-bit word (7 bits plus parity), the receiver strips the parity bit (D7 = 0) so that data alone is transferred to the MPU. This feature reduces MPU programming. The Status Register can continue to be read again to determine when another character is available in the Receive Data Register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

INPUT/OUTPUT FUNCTIONS

ACIA INTERFACE SIGNALS FOR MPU

The ACIA interfaces to the MC6800 MPU with an 8-bit bi-directional data bus, three chip select lines, a register select line, an interrupt request line, read/write line, and enable line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the ACIA.

ACIA Bi-Directional Data (D0-D7) – The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation.

ACIA Enable (E) – The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the MC6800 $\phi 2$ Clock.

Read/Write (R/W) – The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), ACIA output drivers are turned on and a selected register is read. When it is low, the ACIA output drivers are turned off and the MPU writes into a selected register. Therefore, the Read/Write signal is used to select read-only or write-only registers within the ACIA.

Chip Select (CS0, CS1, $\overline{CS2}$) – These three high impedance TTL compatible input lines are used to address the ACIA. The ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from the ACIA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) – The Register Select line is a high impedance input that is TTL compatible. A high level is used to select the Transmit/Receive Data Registers and a low level the Control/Status Registers. The Read/Write signal line is used in conjunction with Register Select to select the read-only or write-only register in each register pair.

Interrupt Request ($\overline{IRQ}$) – $\overline{\text{Interrupt Request}}$ is a TTL compatible, open-drain (no internal pullup), active low

output that is used to interrupt the MPU. The $\overline{IRQ}$ output remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set. The IRQ status bit, when high, indicates the $\overline{IRQ}$ output is in the active state.

Interrupts result from conditions in both the transmitter and receiver sections of the ACIA. The transmitter section causes an interrupt when the Transmitter Interrupt Enabled condition is selected (CR5 · $\overline{CR6}$), and the Transmit Data Register Empty (TDRE) status bit is high. The TDRE status bit indicates the current status of the Transmitter Data Register except when inhibited by Clear-to-Send ($\overline{CTS}$) being high or the ACIA being maintained in the Reset condition. The interrupt is cleared by writing data into the Transmit Data Register. The interrupt is masked by disabling the Transmitter Interrupt via CR5 or CR6 or by the loss of $\overline{CTS}$ which inhibits the TDRE status bit. The Receiver section causes an interrupt when the Receiver Interrupt Enable is set and the Receive Data Register Full (RDRF) status bit is high, an Overrun has occurred, or Data Carrier Detect ($\overline{DCD}$) has gone high. An interrupt resulting from the RDRF status bit can be cleared by reading data or resetting the ACIA. Interrupts caused by Overrun or loss of $\overline{DCD}$ are cleared by reading the status register after the error condition has occurred and then reading the Receive Data Register or resetting the ACIA. The receiver interrupt is masked by resetting the Receiver Interrupt Enable.

CLOCK INPUTS

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data. Clock frequencies of 1, 16 or 64 times the data rate may be selected.

Transmit Clock (Tx Clk) – The Transmit Clock input is used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock.

Receive Clock (Rx Clk) – The Receive Clock input is used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver samples the data on the positive transiton of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data) – The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

Transmit Data (Tx Data) – The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are in the range of 0 to 500 kbps when external synchronization is utilized.

PERIPHERAL/MODEM CONTROL

The ACIA includes several functions that permit limited control of a peripheral or modem. The functions included are Clear-to-Send, Request-to-Send and Data Carrier Detect.

Clear-to-Send ($\overline{CTS}$) – This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem Clear-to-Send active low output by inhibiting the Transmit Data Register Empty (TDRE) status bit.

Request-to-Send ($\overline{RTS}$) – The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The $\overline{RTS}$ output corresponds to the state of the Control Register bits CR5 and CR6. When CR6 = 0 or both CR5 and CR6 = 1, the $\overline{RTS}$ output is low (the active state). This output can also be used for Data Terminal Ready ($\overline{DTR}$).

Data Carrier Detect ($\overline{DCD}$) – This high impedance TTL compatible input provides automatic control, such as in the receiving end of a communications link by means of a modem Data Carrier Detect output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receive Interrupt Enable bit is set.

ACIA REGISTERS

The expanded block diagram for the ACIA indicates the internal registers on the chip that are used for the status, control, receiving, and transmitting of data. The content of each of the registers is summarized in Table 1.

TRANSMIT DATA REGISTER (TDR)

Data is written in the Transmit Data Register during the negative transition of the enable (E) when the ACIA has been addressed and RS · R/$\overline{W}$ is selected. Writing data into the register causes the Transmit Data Register Empty bit in the Status Register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)

Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receive Data Register Full bit (RDRF) in the status buffer to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receive Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although

TABLE 1 – DEFINITION OF ACIA REGISTER CONTENTS

Data Bus Line Number	Buffer Address			
	RS • R/W Transmit Data Register (Write Only)	RS • R/W Receive Data Register (Read Only)	RS • R/W Control Register (Write Only)	RS • R/W Status Register (Read Only)
0	Data Bit 0*	Data Bit 0	Counter Divide Select 1 (CR0)	Receive Data Register Full (RDRF)
1	Data Bit 1	Data Bit 1	Counter Divide Select 2 (CR1)	Transmit Data Register Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Select 1 (CR2)	Data Carrier Detect (DCD)
3	Data Bit 3	Data Bit 3	Word Select 2 (CR3)	Clear-to-Send (CTS)
4	Data Bit 4	Data Bit 4	Word Select 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Transmit Control 1 (CR5)	Receiver Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Transmit Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Receive Interrupt Enable (CR7)	Interrupt Request (IRQ)

* Leading bit = LSB = Bit 0
** Data bit will be zero in 7-bit plus parity modes.
*** Data bit is "don't care" in 7-bit plus parity modes.

the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receive Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

CONTROL REGISTER

The ACIA Control Register consists of eight bits of write-only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send peripheral/modem control output.

Counter Divide Select Bits (CR0 and CR1) – The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a master reset for the ACIA which clears the Status Register (except for external conditions on CTS and DCD) and initializes both the receiver and transmitter. Master reset does not affect other Control Register bits. Note that after power-on or a power fail/restart, these bits must be set high to reset the ACIA. After reseting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷ 16
1	0	÷ 64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4) – The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6) – Two Transmitter Control bits provide for the control of the interrupt from the Transmit Data Register Empty condition, the Request-to-Send (RTS) output, and the transmission of a Break level (space). The following encoding format is used:

CR6	CR5	Function
0	0	RTS = low, Transmitting Interrupt Disabled.
0	1	RTS = low, Transmitting Interrupt Enabled.
1	0	RTS = high, Transmitting Interrupt Disabled.
1	1	RTS = low, Transmits a Break level on the Transmit Data Output. Transmitting Interrupt Disabled.

Receive Interrupt Enable Bit (CR7) – The following interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7): Receive Data Register Full, Overrun, or a low to high transistion on the Data Carrier Detect (DCD) signal line.

MC6850

STATUS REGISTER

Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This read-only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of the Transmit Data Register, the Receive Data Register and error logic, and the peripheral/modem status inputs of the ACIA.

Receive Data Register Full (RDRF), Bit 0 – Receive Data Register Full indicates that received data has been transferred to the Receive Data Register. RDRF is cleared after an MPU read of the Receive Data Register or by a master reset. The cleared or empty state indicates that the contents of the Receive Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE), Bit 1 – The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect (DCD), Bit 2 – The Data Carrier Detect bit will be high when the $\overline{DCD}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated when the Receive Interrupt Enable is set. It remains high after the $\overline{DCD}$ input is returned low until cleared by first reading the Status Register and then the Data Register or until a master reset occurs. If the $\overline{DCD}$ input remains high after read status and read data or master reset has occurred, the interrupt is cleared, the $\overline{DCD}$ status bit remains high and will follow the $\overline{DCD}$ input.

Clear-to-Send ($\overline{CTS}$), Bit 3 – The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{CTS}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master reset does not affect the Clear-to-Send Status bit.

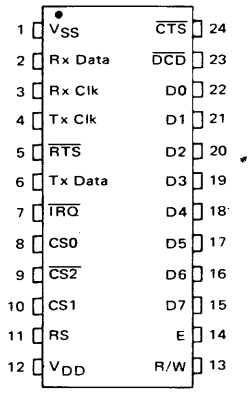
Framing Error (FE), Bit 4 – Framing error indicates that the received character is improperly framed by a start and a stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receive data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN), Bit 5 – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receive Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until the Overrun is reset. Character synchronization is maintained during the Overrun condition. The Overrun indication is reset after the reading of data from the Receive Data Register or by a Master Reset.

Parity Error (PE), Bit 6 – The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

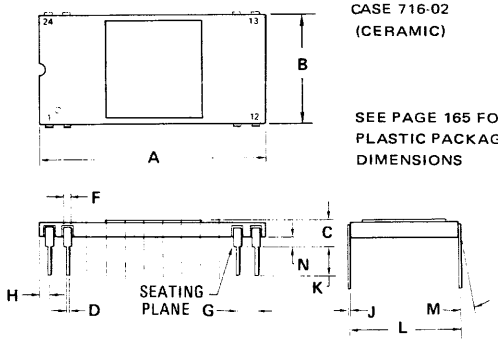
Interrupt Request (IRQ), Bit 7 – The IRQ bit indicates the state of the $\overline{IRQ}$ output. Any interrupt condition with its applicable enable will be indicated in this status bit. Anytime the $\overline{IRQ}$ output is low the IRQ bit will be high to indicate the interrupt or service request status. IRQ is cleared by a read operation to the Receive Data Register or a write operation to the Transmit Data Register.

PIN ASSIGNMENT



PACKAGE DIMENSIONS

CASE 716-02
(CERAMIC)



SEE PAGE 165 FOR PLASTIC PACKAGE DIMENSIONS

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	29.97	30.99	1.180	1.220
B	14.88	15.62	0.585	0.615
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.88	15.37	0.585	0.605
M	–	10^0	–	10^0
N	0.51	1.52	0.020	0.060

NOTE:
1. LEADS TRUE POSITIONED WITHIN 0.25mm (0.010) DIA (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.

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Appendix C

ASCII CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	COMMAND		LISTEN ADDRESS		TALK ADDRESS		SECONDARY ADDRESS	
	ADRSD	UNIV						
Ø Ø Ø Ø	NUL (0)	DLE (16)	SP LA0 (32)	0 LA16 (48)	@ TA0 (64)	P TA16 (80)	\ SA0 (96)	p SA16 (112)
Ø Ø Ø 1	SOH GTL (1)	DC1 LLO (17)	! LA1 (33)	1 LA17 (49)	A TA1 (65)	Q TA17 (81)	a SA1 (97)	q SA17 (113)
Ø Ø 1 Ø	STX (2)	DC2 (18)	" LA2 (34)	2 LA18 (50)	B TA2 (66)	R TA18 (82)	b SA2 (98)	r SA18 (114)
Ø Ø 1 1	ETX (3)	DC3 (19)	# LA3 (35)	3 LA19 (51)	C TA3 (67)	S TA19 (83)	c SA3 (99)	s SA19 (115)
Ø 1 Ø Ø	EOT SDC (4)	DC4 DCL (20)	$ LA4 (36)	4 LA20 (52)	D TA4 (68)	T TA20 (84)	d SA4 (100)	t SA20 (116)
Ø 1 Ø 1	ENQ PPC (5)	NAK PPU (21)	% LA5 (37)	5 LA21 (53)	E TA5 (69)	U TA21 (85)	e SA5 (101)	u SA21 (117)
Ø 1 1 Ø	ACK (6)	SYN (22)	& LA6 (38)	6 LA22 (54)	F TA6 (70)	V TA22 (86)	f SA6 (102)	v SA22 (118)
Ø 1 1 1	BEL (7)	ETB (23)	' LA7 (39)	7 LA23 (55)	G TA7 (71)	W TA23 (87)	g SA7 (103)	w SA23 (119)
1 Ø Ø Ø	BS GET (8)	CAN SPE (24)	(LA8 (40)	8 LA24 (56)	H TA8 (72)	X TA24 (88)	h SA8 (104)	x SA24 (120)
1 Ø Ø 1	HT TCT (9)	EM SPD (25)	) LA9 (41)	9 LA25 (57)	I TA9 (73)	Y TA25 (89)	i SA9 (105)	y SA25 (121)
1 Ø 1 Ø	LF (10)	SUB (26)	* LA10 (42)	: LA26 (58)	J TA10 (74)	Z TA26 (90)	j SA10 (106)	z SA26 (122)
1 Ø 1 1	VT (11)	ESC (27)	+ LA11 (43)	; LA27 (59)	K TA11 (75)	[TA27 (91)	k SA11 (107)	{ SA27 (123)
1 1 Ø Ø	FF (12)	FS (28)	, LS12 (44)	< LA28 (60)	L TA12 (76)	\ TA28 (92)	l SA12 (108)	¦ SA28 (124)
1 1 Ø 1	CR (13)	GS (29)	- LA13 (45)	= LA29 (61)	M TA13 (77)	] TA29 (93)	m SA13 (109)	} SA29 (125)
1 1 1 Ø	SO (14)	RS (30)	. LA14 (46)	> LA30 (62)	N TA14 (78)	^ TA30 (94)	n SA14 (110)	~ SA30 (126)
1 1 1 1	SI (15)	US (31)	/ LA15 (47)	? UNL (63)	O TA15 (79)	_ UNT (95)	o SA15 (111)	RUBOUT (DEL) (127)

THIS CHART ALSO CONTAINS GPIB COMMAND AND ADDRESS INFORMATION.

INDEX

+175 Volt Supply 6-30

4051 Graphic System 1-2
4051 Option 1 7-4

Absolute Value Amplifiers 6-28
ACIA 6-6
Addressing 6-7
Adjustment Locator Aids 5-5
Alphanumeric Display 6-24
Alphanumeric Keyboard 2-4
Analog Filter 6-22
ASCII Code Chart C-1

Backpack Addressing 7-1
Backpack Circuits 7-1
Backpack Removal 3-11
Bank Switch 1-2, 2-19, 7-3
BASIC Language 1-2
BASIC Language Format 2-19
BASIC Line Length 1-2
Baud Rate Select 7-6

Calibration 4-1
Calibration—Display 4-4
Calibration—Hard Copy 4-7
Calibration—Power Supply 4-1
Calibration—Tape Unit 4-9
Calibration Equipment 4-1
Cartridge Respooling 3-4
Circuit Description 6-1
Cleaning 3-1
Cleaning—Electrical Contacts 3-3
Cleaning—Fan Filter 3-2
Cleaning—Surface 3-2
Cleaning—Tape Head 3-2
Collimation Control 6-31
Communication Backpack 1-2, 7-4
Communication Cable 7-8
Communication Interface 7-4
Communication Interface Test 7-9
Communication Self-Test Adapter 7-9
Communications ACIA 7-7

Index (cont) Page

Control Grid Supply 6-34
Cover Removal 3-11
CPU Board Access 3-25
CRT Filter Access 3-16
CRT Installation 3-21
CRT Removal 3-18
CRT Voltage Levels 6-30

D/A Operation 6-20
Data Rate Select 7-6
Data Storage—Magnetic Tape 1-4
Deflection Amplifiers 6-26, 6-29
Deflection Yoke Replacement 3-21
Device Numbers 2-20
Disassembly/Assembly 3-11
Display 1-1, 2-8, 4-4
Display Board 6-24
Display Board Access 3-25
Display Board Blocks 6-27
Display Control 6-18, 6-24
Display Test 5-25

Electrical Contacts—Cleaning 3-3
Environmental Specifications 2-2
Erase Circuits 6-26, 6-29
Erase Timing 6-30

Fan Filter—Cleaning 3-2
Filament Supply 6-33
Filter—Analog 6-22
Firmware 1-2
Firmware Backpack 1-2, 7-1
Firmware Checksums 5-20
Flood Gun Control 6-32
Focus Circuits 6-26
Focus Supply 6-33

General Purpose Interface Bus 2-24
General Purpose Interface Bus (GPIB) 6-46
Geometry Correction Multipliers 6-29

Index (cont) Page

GPIB 1-1, 2-24
GPIB ASCII Data 2-28
GPIB Binary Data 2-28
GPIB Commands 2-30
GPIB Concepts 2-24
GPIB Connector 2-24
GPIB Data Bus 2-26
GPIB Data Format 2-28
GPIB Device Numbers 2-21
GPIB Management Bus 2-26
GPIB Signal Definitions 2-26
GPIB Single Byte Transfer 2-29
GPIB Test 5-21
GPIB Transfer Bus 2-27
GPIB—IEEE Compatibility 2-29

Hard Copy Adjustments 4-7
Hard Copy Compatibility 1-2
Hard Copy Operations 6-24, 6-35
High Voltage Circuits 6-26, 6-32
High Voltage Regulator Oscillator 6-33
High Voltage Supply 6-33

I/O Address Code 2-20
Index of Signal Names A-1
Indicator Lamps 6-17
Intensity Control 6-35
Internal Device Numbers 2-21

Joystick Connector 1-1

Key Codes 6-14
Keyboard 1-1, 1-2, 6-13
Keyboard Access 3-12
Keyboard Operation 6-13
Keyboard Timing 6-10
Keyword 2-20

Line Editing Keys 2-6
Long Vectors 6-23

Index (cont) Page

Magnetic Tape Data Format 2-14
Magnetic Tape Media 2-14
Magnetic Tape Specifications 2-12
Magnetic Tape Unit 2-12, 4-9
Magnetic Tape Unit Access 3-28
Maintenance 3-1
Memory 1-2
Memory—RAM 2-17, 6-3
Memory—ROM 6-3
Memory—ROM and Peripheral Devices 2-17
Memory Address Allocation 2-17, 6-7
Memory Board Access 3-25
Memory Refresh Timing 6-10
Microcomputer Building Blocks 2-17
Microcomputer System 2-16, 6-1
Microprocessor 1-2, 2-16, 6-1
Motorola Devices 2-16

Noburn Circuit 6-23

Operator Interface 2-3

Peak Detection Amplifier 6-43
Peripheral Control 1-2
Peripheral Device Numbers 2-21
Peripheral Interface Adapter (PIA) 6-4
Physical Measurements 2-1
PIA 6-4
Power Requirements 1-4
Power Specifications 2-2
Power Supply 4-1
Power Supply Access 3-24
Power Supply Board 6-48
Processor Timing 6-10
Program Development Keys 2-7
Purpose—Volume 1 1-1
Purpose—Volume 2 1-1

RAM Test 5-14
Random-Access Memory (RAM) 1-2, 6-3
Read-Only Memory (ROM) 1-2, 6-3
Regulated Power Supplies 6-49

Index (cont) Page

Removal—Backpack 3-11
Removal—Cover 3-11
Removal—CPU Board 3-25
Removal—CRT 3-18
Removal—CRT Filter 3-16
Removal—Deflection Yoke 3-21
Removal—Keyboard 3-12
Removal—Memory Board 3-25
Removal—Power Supply 3-24
Removal—Tape Unit 3-28
ROM Checksums 5-20
ROM Expander Unit 1-2
ROM Test 5-18
RS-232 Interface 7-4

Service Equipment 4-1
Software—Verification 3-3
Special Test Aids 1-6
Specifications 2-1
Specifications—Environmental 2-2
Specifications—Magnetic Tape 2-12
Specifications—Microcomputer System 2-16
Specifications—Physical 2-1
Specifications—Power 2-2
Standard Components 1-1
Static Warning Label 3-10
Static-Free Work Station 3-8
Status Lights 2-7
STB (Storage Backplate) Control 6-31
Storage Circuits 6-26, 6-29
System Addressing 6-7
System Architecture 6-1
System Building Blocks 2-17
System Connectors 1-4
System Test Aids 1-6
System Test Fixture 5-11
System Test Fixture—see Test Fixture 5-11

Tape Cartridge Respooling 3-4
Tape Control Test 5-27
Tape Data Format 6-37

Index Page

Tape Head—Cleaning 3-2
Tape Read Operations 6-42
Tape Speed Control 6-45
Tape Test Connector 5-31
Tape Timing 6-10, 6-40
Tape Unit 1-1, 6-37
Tape Unit Access 3-28
Tape Unit Calibration 4-9
Tape Unit Control 6-37
Tape Write Operations 6-42
Target Control 6-31
Test Fixture—Display Test 5-25
Test Fixture—GPIB Test 5-21
Test Fixture—RAM Test 5-14
Test Fixture—ROM Checksums 5-20
Test Fixture—ROM Test 5-18
Test Fixture—Tape Tests 5-27, 5-31
Test Fixture Switches 5-12
Test Fixture Tests 5-12
Test Fixtures 1-6
Timing 6-9
Timing—Keyboard 6-10
Timing—Memory Refresh 6-10
Timing—Processor 6-10
Timing—Tape 6-10
Transconductance Multiplier 6-29
Troubleshooting 5-1
Troubleshooting Aids 5-1
Troubleshooting Guide 5-2

Vector Generation 6-22
Verification Software 3-3
View Circuits 6-26

X^2 and Y^2 Amplifiers 6-29

Z Signal Amplifier 6-35

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MANUAL CHANGE INFORMATION

PRODUCT 4051 SERVICE
VOLUMN I 070-2065-00

CHANGE REFERENCE C1/677
DATE 6-2-77

CHANGE:	DESCRIPTION

EFF SN B082623 TEXT CORRECTIONS

REPLACE: Fig. 4-3 and Fig. 5-5 with both the following A and B versions.

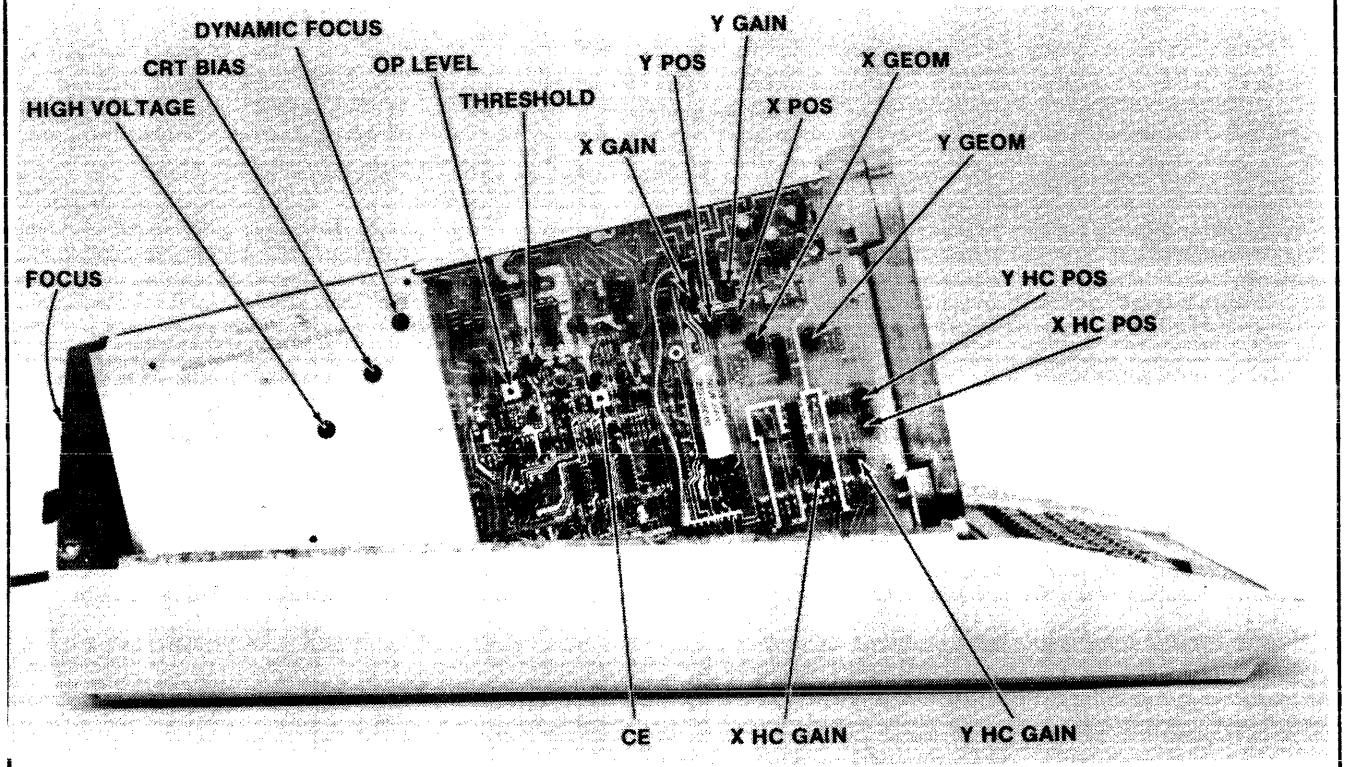

Fig. A. 672-0546-05 and above Display board adjustments.

CHANGE:	DESCRIPTION

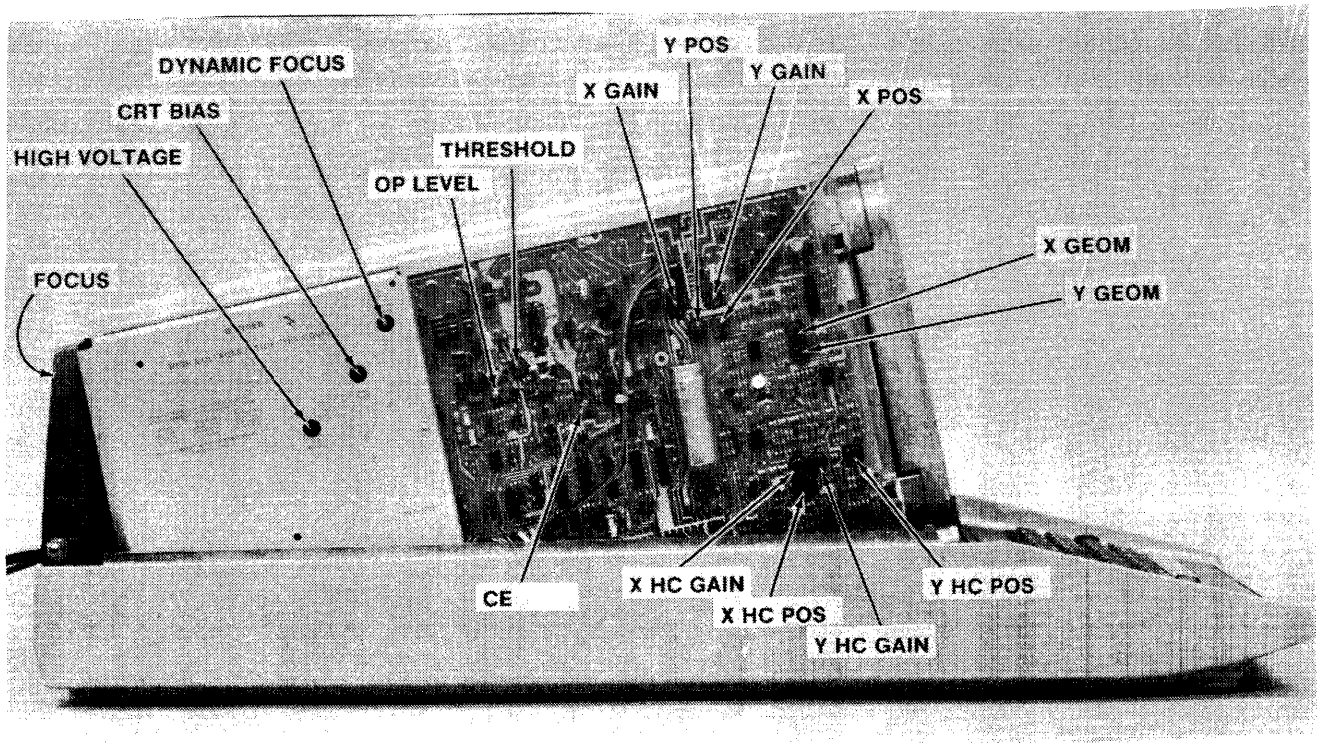

Fig. B. 672-0546-04 and below Display board adjustments.

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MANUAL CHANGE INFORMATION

PRODUCT 4051 SERVICE
VOLUMN 1 070-2065-00
CHANGE REFERENCE C2/877
DATE 8-5-77

CHANGE:	DESCRIPTION

Page 1-6 Fig. 1-4

CALIBRATION TAPE Replaced by 067-0781-01

RS-232 TEST ADAPTER Replaced by 013-0173-01

Page 4-1 Calibration tape cartridge (067-0781-01)