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4052/4054
&
4052A/4054A
TECHNICAL DATA
SERVICE MANUAL

Tektronix, Inc.
P.O. Box 500
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MANUAL PART NO.

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

MANUAL REVISION STATUS

PRODUCT: 4054/4054A Options 30 and 31 Dynamic Graphics

This manual supports the following versions of this product: 4052: B010100 and up
4054: B010100 and up
4052A: B010100 and up
4054A: B010100 and up

REV DATE	DESCRIPTION
SEP 1979	Original Issue
MAY 1980	Revised pages
JUL 1981	Revised to include information on 4054 Option 31. Manual Part No. changed to 070-2840-01.
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NOV 1982	Revised to include 4052A and 4054A; Manual Part Number changed to 070-2840-03.

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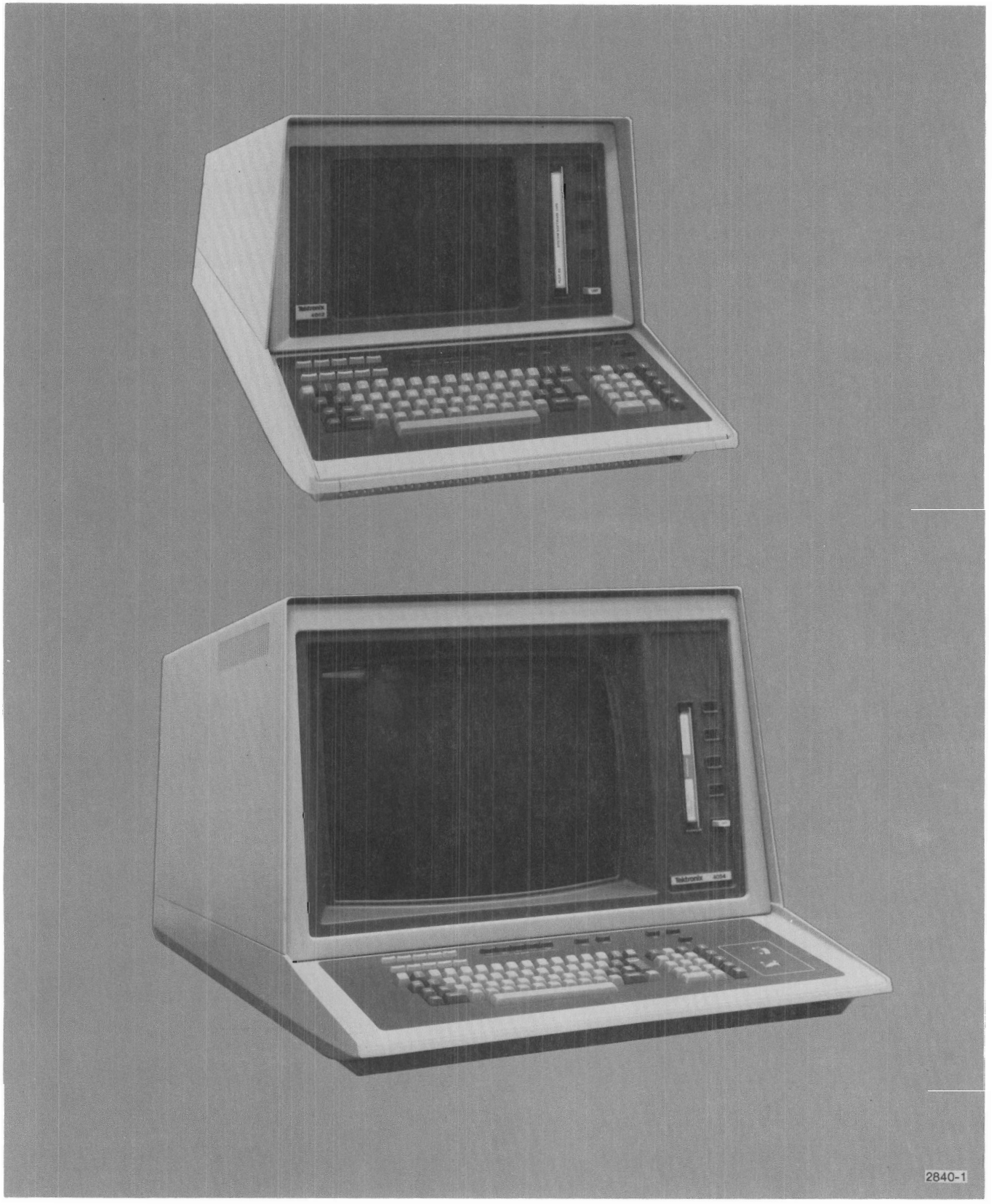


Figure 1-1. 4052 and 4054 Graphic Computing Systems.

Section 1

INTRODUCTION

PURPOSE OF MANUAL

This manual, in conjunction with the appropriate Parts and Schematics Manual, provides a service technician with the necessary information for performing routine maintenance, for troubleshooting, and for repairing the 4052/4052A and 4054/4054A Graphic Computing Systems.

This manual is part of a service documentation package which consists of the following Service Manuals:

- 4052/4052A & 4054/4054A Technical Data Service Manual
- 4052/4052A Parts and Schematics Service Manual
- 4054/4054A Parts and Schematics Service Manual
- 4054/4054A Options 30 and 31 Dynamic Graphics Service Manual

In this documentation package, references to the 4052 and 4054 apply to the 4052A and 4054A also, unless specifically stated otherwise. All versions of the circuit boards you are likely to encounter are documented in this service package. Whenever multiple versions of boards exist, verify that the information you are reading matches the board in your instrument.

The 4052/4054 Technical Data Service Manual (this manual) provides maintenance information, calibration procedures, troubleshooting information, and circuit descriptions for the 4052 and the 4054.

The 4052 Parts and Schematics Service Manual contains 4052 block diagrams, schematics, cross reference tables, signal name definitions, wire lists, and replaceable parts lists for the 4052 Graphic Computing System, 4052 Backpacks, and 4052 ROM Packs. It also contains a short form calibration procedure.

The 4054 Parts and Schematics Service Manual contains 4054 block diagrams, schematics, cross reference tables, signal name definitions, wire lists, and replaceable parts lists

for the 4054 Graphic Computing System, 4054 Backpacks, and 4054 ROM Packs. It also contains a short form calibration procedure.

Additional service test procedures for the 4052 and the 4054 are found in the 067-0900-00 Diagnostic Rom Pack Instruction Manual.

4052/4054 STANDARD COMPONENTS

Standard components that are common to the 4052 and the 4054 include the following:

- The 4052/4054 Processor, consisting of the following three circuit boards: ALU Board (Arithmetic Logic Unit); MCP Board (Memory Command Processor); MAS Board (Memory Array Sequencer). The 4052/4054 Processor does the computation, controls the I/O, and contains memory storage for the 4052 and the 4054. The processor is described in Section 6, 4052/4054 General Theory of Operation and Section 7, ALU, MCP, and MAS Theory of Operation.

- Full ASCII keyboard, plus calculator key pad, user-definable keys, and editing keys. (See Section 8, 4052/4054 Keyboard Theory of Operation.)

- A magnetic tape unit, capable of storing 300K bytes of data and organized into a sequential-file structure. Tape format is programmable to support TEKTRONIX 4923 and 4924 type tapes, as well as 4050-Series type tapes. Refer to Section 9, 4052/4054 Tape Unit Theory of Operation.

- A GPIB bus connector, allowing interfacing to devices compatible with IEEE standard #488-1975. (See Section 10, 4052/4054 General Purpose Interface Bus Theory of Operation.)

- Joystick connector, allowing the user to input graphic coordinates with the optional joystick.

- Hard copy compatibility, allowing the user to obtain a copy of the displayed information via an optional TEKTRONIX 4631 or 4610 Hard Copy Unit.

- A two-slot Firmware Backpack, capable of holding two optional ROM Packs.

4052 Standard Components

The following standard component is used in the 4052:

- 11" DVST (direct view storage tube) display with a capacity of 35 lines of alphanumeric characters, 72 characters per line (74 characters per line in communications, terminal mode). Vector resolution is approximately 120 points per inch.

4054 Standard Components

The following standard components are used in the 4054:

- In addition to the standard keyboard there are thumb wheels for moving crosshairs on the display.
- 19" DVST (direct view storage tube) display with four character sizes, dashed lines in graphics, keyboard input of 72 characters per line (74 characters per line in communications, terminal mode). The maximum number of characters per line depends on character size. The characters are written with vectors and not with dots. Vector resolution is approximately 290 points per inch.

4052 GRAPHIC COMPUTING SYSTEM

The 4052 can be used as a stand-alone programmable calculator, or, with the addition of the optional Communications Backpack, as an intelligent graphic terminal. The standard 4052 contains a 16-bit ALU unit, a 32K byte random access memory, an 11-inch direct-view storage tube (with hard copy compatibility), a built-in magnetic tape unit, and an extended BASIC language interpreter. The 4052 handles the same processing functions normally handled by other computer-based computational systems.

The 4052 keyboard is the primary input device. The keyboard has standard full ASCII keys with a separate numeric keypad for data entry. Editing keys, magnetic tape control keys, hard copy keys, and 10 user-definable keys are also included.

BASIC language statements are used to program the 4052. The 4050 Series BASIC language is an extended version of the Dartmouth College Timeshare BASIC (Beginner's All-purpose Symbolic Instruction Code) with extensions in the areas of graphics primitives, unified I/O handling of the General Purpose Interface Bus (GPIB), matrices, strings, and high level language interrupt handling. Basic programs written for the TEKTRONIX 4051 can be run on the 4052.

Keyboard entries are displayed on the DVST. Both upper and lower case letters are printed, with a maximum of 72 characters per line (74 characters with the optional communications terminal mode). The display also features full graphics capability. Drawing lines (called vectors) on the screen is accomplished by typing BASIC graphic commands from the keyboard or executing BASIC statements under program control. The storage tube is hard copy compatible, which allows an attached hard copy unit to make a paper copy of displayed information. (The hard copy unit is optional.)

The 4052 memory is divided into a random-access memory (RAM) and a read only memory (ROM). The standard 4052 has a 32K-byte storage capacity, of which 30.5K bytes are accessible by the user for storing programs and data. The RAM storage capacity can be increased to 56K bytes.

The 4052 ROM has 46K locations that hold processor firmware, peripheral control addresses, and a 16K byte section used by extended firmware modules (i.e., ROM packs). The Firmware Backpack or the optional Communications Backpack each provides the user with two slots for ROM packs. By replacing the two-slot backpacks (firmware or communications) with an optional four-slot backpack (firmware or communications), the number of available ports for ROM packs can be increased to four. The processor has access to code in the ROM packs through a bank switch.

Data and program instructions can be transferred onto magnetic tape and re-entered into RAM via a built-in magnetic tape unit. The tape is in a standard data cartridge with approximately a 300K-byte capacity, depending upon the length of each data file.

Four rear panel connectors allow the 4052 to interface to a variety of peripherals. The General Purpose Interface Bus (GPIB) connector allows the 4052 to exchange data with devices such as disk storage units, X-Y plotters, and instrumentation systems. Data transfers over the GPIB are in byte-serial, bit-parallel format (eight bits per byte). The GPIB is compatible with the IEEE Standard #488-1975.

Another rear panel connector is part of the optional Communications Backpack and is compatible with RS-232 devices (e.g., computer modems). This allows the 4052 to exchange data with devices such as computer terminals, printers, and modems. The RS-232 communications interface features asynchronous full-duplex or half-duplex operation. Data exchange rate is selectable by the user through program control for one of the following: 110, 150, 300, 600, 1200, 2400, 4800, or 9600 baud.

The other two connectors are utilized by the optional joystick and hard copy unit peripherals.

4054 GRAPHIC COMPUTING SYSTEM

The TEKTRONIX 4054 is similar to the 4052 except that it has a 19-inch crt, graphic input thumbwheels, stroke-drawn characters in four sizes, and solid line or dotted vectors. Keyboard entries are displayed on the 19-inch direct-view storage tube (DVST). Both upper and lower case letters are printed, with a maximum of 72 characters per line in entry mode. Four character sizes are available. The 4054 uses stroke drawn characters instead of the dot matrix characters used by the 4051 and the 4052. The display also features full graphics capability. Drawing lines or vectors on the screen is accomplished by typing BASIC graphic commands from the keyboard or executing BASIC statements under program control. The vectors can be drawn either as solid lines or as dashed lines. The storage tube is hard copy compatible, which allows an attached hard copy unit to make a paper copy of displayed information.

4052/4054 POWER REQUIREMENTS

The 4052 and 4054 operate at 50 Hz or 60 Hz line frequencies using voltages of 100 Vac, 120 Vac, 220 Vac,or 240 Vac. The 4052 or 4054 is normally shipped from the factory strapped for 120 Vac operation. To change the operating voltage, refer to Section 4, 4052 Calibration, or to Section 5, 4054 Calibration.

4052/4054 TEST AIDS

The following test aids are available for the 4052/4054:

Diagnostic ROM pack	067-0900-00
Diagnostic Test Tape	067-0901-00
Self Test Adapter (used with communications option)	013-0173-01
Alignment Tape Cartridge	067-0781-01
Mag Tape/GPIB Test Fixture	067-0790-00
Tape Head Alignment Tool	067-0788-00
Display Test Graticule (4052)	067-0654-00
Display Test Graticule (4054)	067-0818-00
DVST Display Exerciser (4054)	067-0807-XX
Flexible Extender (4054)	067-0817-XX

Section 2

SPECIFICATIONS

INTRODUCTION

This section gives a brief review of 4052/4054 operations with special emphasis placed on physical and electrical specification of the system. Hardware performance specifications are tabulated for quick reference. Some explanatory text is also incorporated. BASIC language statements are described in detail in the 4050 Series Graphic System Reference Manual. Refer to the Reference Manual for detailed operation information.

SPECIFICATIONS

Physical Measurements

Dimensions(4052)

Length	31.75 in (80.64 cm)
Width	18.25 in (46.4 cm)
Height	14.25 in (36.2 cm)

Dimensions (4054)

Length	34.75 in (88.3 cm)
Width	26.3 in (66.8 cm)
Height	20.5 in (52.0 cm)

Weight 4052 (70 lbs 31.8 kg)

Weight 4054 (145 lbs 65.9 kg)

Environmental Specifications

Temperature

Operation	+10 to +40 degrees C
Storage	-40 to +65 degrees C (tape limited to +45 degrees C)

Altitude

Operating	to 15,000 feet

Humidity

Storage	95% non-condensing (tape limited to 20% min and 80% max.)

Shock (Non-operating)

4052	30 g's, 11 ms duration
4054	20 g's, 11 ms duration

Power Specifications

	4052	4054
Line Voltage	90 to 132Vac 198 to 250Vac	90 to 132Vac 198 to 250Vac
Fuse 115VAC 230VAC	 3A Fast Blow 3A Fast Blow	 5A Fast Blow 3A Slow Blow
Line Frequency	48 to 66 Hz	48 to 66 Hz
Power Consumption (Approximate)	230W (780BTU)	360W (1225BTU)

Dielectric breakdown greater than 2000VAC RMS (60Hz) between power line and accessible conductive components.

OPERATOR INTERFACE

The front of the 4052 or the 4054 Graphic Computing System is divided into ten functional areas. These areas are illustrated in Figure 2-1 and Figure 2-2.

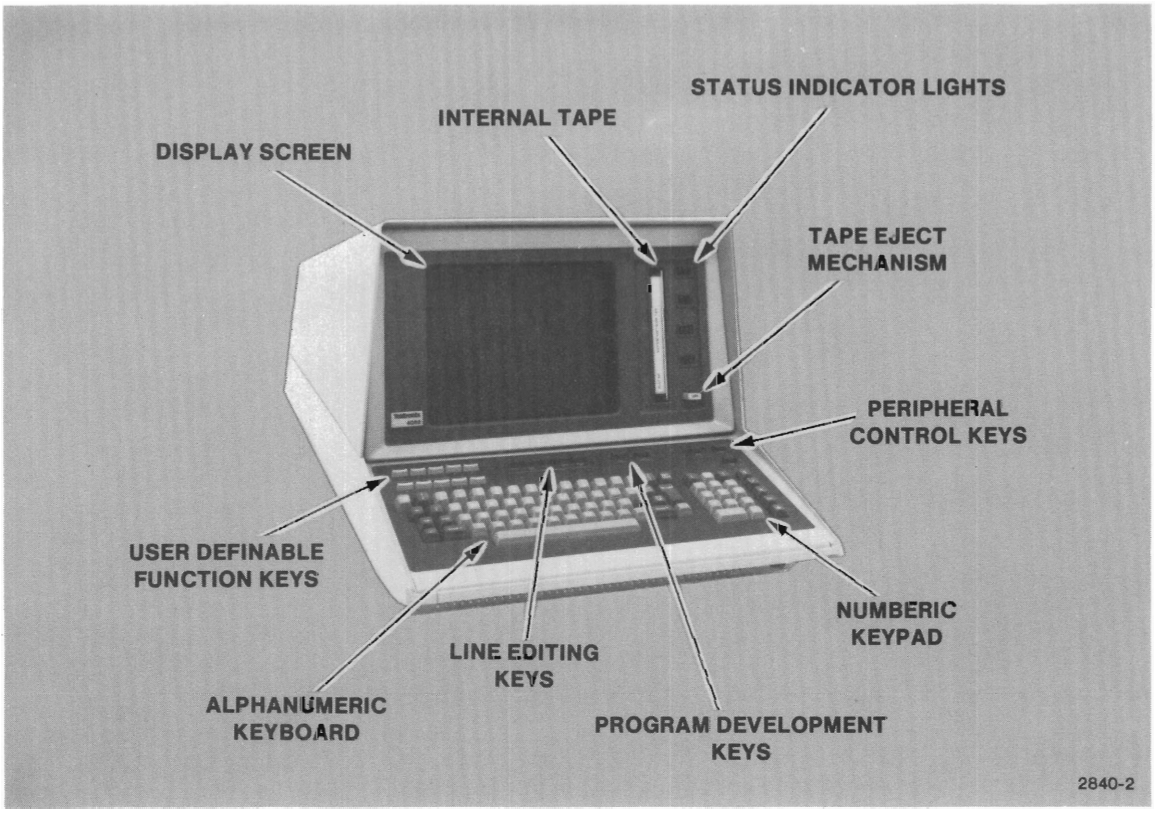


Figure 2-1. 4052 Front Panel Controls and Indicator Lights.

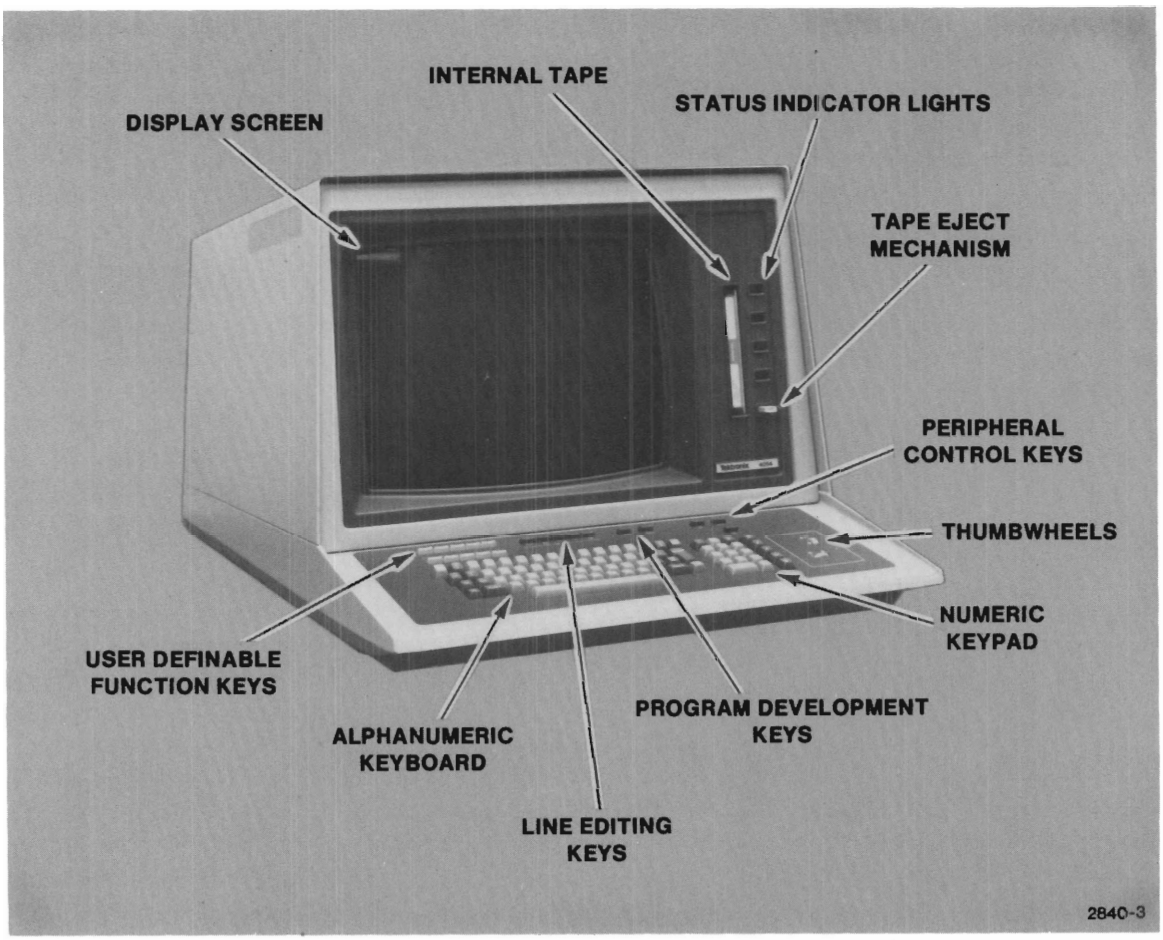


Figure 2-2. 4054 Front Panel Controls and Indicator Lights.

A crt screen is used to display both graphic and alphanumeric information.

The internal tape unit is used to store BASIC language program statements and data of various types on a standard magnetic tape cartridge.

The status indicator lights tell when power is applied to the system, when the system is performing input or output operations, and when it is waiting to stop after the BREAK key has been pressed.

The eject mechanism removes a tape cartridge from the Graphic Computing System internal tape unit.

User-definable function keys allow the operator to branch to any of 20 specified BASIC program locations by pressing one of these keys. There are ten keys to specify ten program locations. Another ten locations are available if the keys are pressed while holding down a SHIFT key.

The alphanumeric keyboard is used for entry of BASIC program language statements or data. If a communication backpack is installed on the 4052/4054, these keys can be used for data entry into a host computer.

Line editing keys allow editing of BASIC statements, without having to retype the entire statement.

Program development keys can be used to enter BASIC statement numbers sequentially when programs are being created or modified. They can also be used to debug or troubleshoot a BASIC program.

The numeric keypad is for entering numeric data into the system. Calculator functions are also available. When the 4052/4054 is used as a calculator without a BASIC program, the RETURN key causes the calculated result to be displayed.

Peripheral control keys control the tape unit and optional hard copy unit.

Alphanumeric Keyboard

ALPHANUMERIC KEYS	The alphanumeric keys (letters, numbers and symbols) are used to enter BASIC statements and generate ASCII control characters. Keys 0-9 can also be used to enter numeric data.
SPACE BAR	When the space bar is pressed, the display cursor moves one space to the right. No character is printed. If the cursor is at the right margin, nothing happens.

SHIFT	These keys are similar to the SHIFT keys on a typewriter keyboard. Either key determines which one of two characters is printed when an alphanumeric key is pressed. If used alone, this key brings the display out of Hold Status.
TTY LOCK	This key causes all lower case letters to be transformed to upper case when entered.
TAB	When this key is pressed, the keyboard issues the ASCII control character TAB. The TAB character prints on the display as an underlined I. When the TAB function is executed, the display cursor moves to the right and stops in column 19, 37, 55,1, etc. TAB spacing can be modified if a PRINT USING statement is executed. The 4054 tab settings are also spaced every 18 columns. The number of TAB columns available varies with the print size.
CTRL	When pressed in combination with a letter key and sometimes the SHIFT key, the keyboard issues an ASCII control character. At statement entry time, all control characters are echoed to the display as an underlined letter (except CR and RUBOUT). At statement execution time, some control characters cause machine display functions to be executed.
ESC	When this key is pressed. the keyboard issues the ASCII control character ESC.
HOME PAGE	If pressed alone, the display is erased and the cursor returns to the Home position. If pressed in combination with the SHIFT key, the cursor returns to the Home position and the display is not erased.

BACK SPACE	Pressing this key moves the cursor to the left by one space. If the line buffer is empty, the cursor does not move.
RETURN	Pressing this key generates an ASCII control character CR (Carriage Return). The display cursor returns to the left margin and moves down one line. This key causes the machine to evaluate the information on the previous line. If the line contains a line number, the statement is entered into memory and is not executed. If the statement does not contain a line number it is executed immediately.
RUBOUT	If the display cursor is over a blank, pressing RUBOUT moves the display cursor one space to the left and writes the cursor over any character in that location. The character underneath the cursor is logically removed from memory and replaced by the space character. The next time the line is printed, a space appears instead of the cursor. If the cursor is over a non-blank character, the cursor does not move but rubs out the character.
BREAK	The first time the BREAK key is pressed, the BREAK indicator on the front panel lights up. This is referred to as a "BREAK pending" condition. The machine stops program execution after the present line is completed and the indicator goes out. If the BREAK key is pressed while the BREAK light is on, program execution is aborted immediately and the program line pointer returns to the starting position.

Line Editing Keys

The five program line editing keys at the top center of the keyboard are each dual purpose. The primary function is printed below each key, while the secondary function is printed above each key.

The primary function is performed by simply pushing the key. The secondary function is performed by pressing the key while holding down the SHIFT key. All operations are performed on the current line which is stored in a 72-character line buffer.

EXPAND	This key is used for insert operations. All characters to the right of the cursor, including that character where the cursor is positioned, are moved to the extreme right of the line buffer. On the screen, the line splits into left and right portions, separated by a gap. The cursor finishes at the extreme left of the gap. Characters can now be inserted
COMPRESS	This key (actually the simultaneous pushing of the EXPAND key and SHIFT key), is the inverse of EXPAND. The portion of line to the right of the screen is shifted to the current position of the cursor, and intervening spaces are removed.
BACKSPACE	This key moves the cursor one character position to the left. It performs the same function as the ASCII BACKSPACE key on the keyboard.
RUBOUT	This key is the same as pressing RUBOUT.
SPACE	This key is the same as the SPACE bar on the main keyboard and is provided here for convenience. The cursor moves one character space to the right.

RUBOUT	This key is the same as RUBOUT except it moves the cursor to the right instead of to the left.
CLEAR	CLEAR empties the contents of the current line buffer without affecting information already stored in RAM.
REPRINT	This key duplicates the current contents of the line buffer one position below the current display. The position of the cursor relative to the buffer is unchanged. This is a useful key to use when the storage display is written over and difficult to read.
RECALL LINE	This key recalls a program line previously stored in RAM. You must enter the number of the line to be recalled before pushing this key. The line is called and the cursor appears one space beyond the last character in the line.
RECALL NEXT LINE	This key is similar in function to RECALL LINE, but instead of calling the line with the line number currently in the display, the line with the next greater number is called.

Program Development Keys

AUTO NUMBER

The AUTO NUMBER function is provided as an operator convenience during program statement entry time. Pressing the key once automatically provides line numbers for each BASIC statement entry from the keyboard. The first time the key is pressed, line number 100 is placed in the line buffer and appears on the display. The operator enters a BASIC statement and presses the RETURN key. The machine then places line number 110 in the line buffer for the next statement entry. The line number increment is automatically set at 10. To start the auto number sequence with a line number other than 100, the line number is entered into the line buffer from the keyboard and then the AUTO NUMBER key is pressed. The 4052/4054 provides line numbers from that starting point in increments of 10. To exit the auto number mode, press the AUTO NUMBER key again.

STEP PROGRAM

The STEP PROGRAM key causes the 4052/4054 execute the current BASIC program one step at a time. Each time the key is pressed, one line in the program is executed. This feature allows the keyboard operator to monitor the execution sequence of the program during debugging operations. Normally, the program starts one step execution from the beginning; however, the program line counter can be set to any line in the program by using the GOTO statement and then pressing the STEP PROGRAM key causes one step execution from that point. For example, entering GOTO 500 and pressing the RETURN key sets the program line counter to line number 500. Then you can execute one step at a time from that point by pressing the PROGRAM STEP key again and again.

AUTO LOAD	Pressing the AUTO LOAD key causes the cartridge in the magnetic tape unit to rewind and load the first BASIC program from the cartridge into the Random Access Memory. There must be a valid ASCII program stored on the tape, otherwise an error occurs.
REWIND	Pressing the REWIND Key causes the 4052/4054 to rewind the tape cartridge in the internal magnetic tape unit. Pressing the REWIND key is the same as executing the BASIC statement FIND 0.
MAKE COPY	Pressing the MAKE COPY key causes an attached hard copy unit to make a paper copy of the information on the 4052/4054 display. Pressing this key is the same as executing the BASIC statement COPY.
THUMBWHEELS	(4054 only) The thumbwheels are located on the right side of the keyboard section. They position the crosshair cursor that is displayed in GIN (Graphic Input) Mode.

Status Lights

BUSY	The system is busy transferring or processing data.
I/O	Input/Output operations are in progress.
BREAK	A break in program execution is pending. The BREAK light goes out after program execution halts at the end of the current line.
POWER	Indicates that power is supplied to the 4052/4054.

Display

The display is a direct view storage tube (DVST) crt.

HOLD STATUS	Reduced intensity after approximately 100 seconds of no display activity. Maintains the currently stored image for re-display.
AUTOMATIC ERASE	After about 30 minutes of idle machine time, the crt erases.
GRAPHICS	Coordinates are specified by a pair of decimal fractions. The default coordinate limits are 0 to 100 on the vertical (Y) axis and 0 to 130 on the horizontal (X) axis. Vectors are drawn using MOVE and DRAW commands. The coordinate limits can be changed by executing the WINDOW command. Resolution is approximately 120 points per inch for the 4052 and 290 points per inch for the 4054 (see Figure 2-3).
ALPHANUMERIC CHARACTERS	(4052) Full ASCII 96 printing character set (upper and lower case) printed using a 5 x 8 dot matrix. 72 characters per line 35 lines per display 2520 characters per display, (2590 Option 1) (4054) The full ASCII printing character set is available using stroke-drawn characters. There are four character sizes, with maximum 72, 79, 119, and 132 characters per line, respectively. To change character size on the 4054, use:Print@32,17:N (N=1, 2, 3, or 4) or CHA 1, CHA 2, etc.

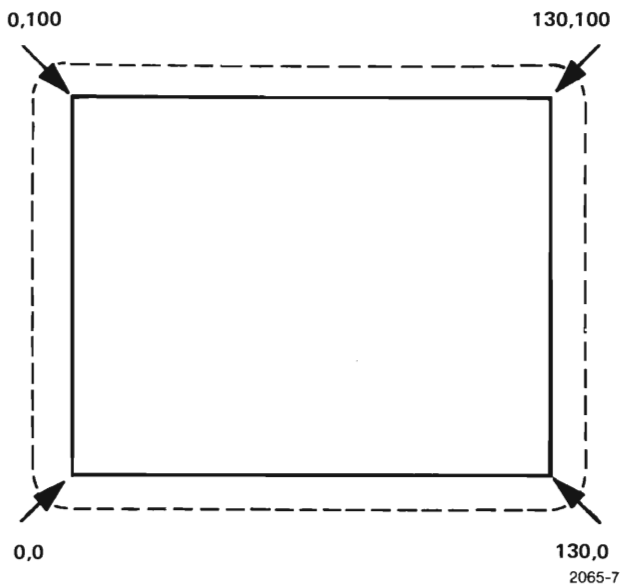


Figure 2-3. Default Graphic Coordinate Limits.

Magnetic Tape Unit (Built In Unit)

The tape unit uses a standard data cartridge with approximately 300 feet of 1/4 inch computer-grade magnetic tape. Each tape has a storage capacity of 300K bytes of data.

Input/Output operations with the tape unit are normally performed by executing the BASIC language commands FIND, OLD, SAVE, APPEND, INPUT, OUTPUT, PRINT, READ, and WRITE. The system's operator can also transfer machine binary code with BSAVE, BOLD, etc. Many of the commands require the tape unit address @33. Two keyboard keys, REWIND and AUTO LOAD, provide minimal control of tape operations. Magnetic tape operations are defined in detail in the 4050 Series Graphic System Reference Manual.

Tape Unit Specifications

The tape units use a standard data cartridge.

	Tektronix Part Number 119-0680-01
Data Capacity	300K bytes(Depending on the number of files)
Minimum Life	5000 passes
Tape Markers	B.O.T. (Beginning of Tape) Load Point Early Warning Point E.O.T. (End of Tape)

Data Format and Recording Method

The data format is determined by 4052/4054 system firmware. Data timing is tabulated in Section 9. Information on the tape is divided into files that contain a minimum of 3 records. The standard record length is 256 bytes of data characters, but a 128 character format may be selected using the PRINT @33.0: statement. The 128 character format is compatible with standard 4923 Digital Cartridge Tape Recorder operations.

The tape formatting process occurs with the MARK **n**, **m** statement where **n** is the number of files to be marked and **m** is the number of bytes per file. Areas of the tape are separated by record marks and file marks.

Binary data bits are represented as reversals in flux direction (magnetic domain boundaries) on either the 1 track or 0 track. In reading the tape, the tape head is sensitive to flux reversals. The determination of a 1 or 0 depends upon which track had the flux reversal. This is the NRZ data recording system.

Special Data Sequences	Data is held at zero during record and file marks. Flux reversals occur only on track zero for these sequences.

Record Mark	Four flux reversals separated by intervals about three times longer than data bit separations. The longer intervals are called intercharacter gaps. The shorter intervals are interbit gaps.
File Mark	Eight flux reversals separated by intervals about three times longer than data bit separations.

Basic Language I/O Format

(Line Number) KEYWORD ( ) (I/O Addresses:)

Line Number

The line number determines the order of statement execution. If a line number is present, the statement is executed when the system is placed under program control. If the line number is not present, the statement is executed as soon as the statement is entered into the line buffer and the RETURN key is pressed.

Keyword

The KEYWORD is an alphabetical code that tells the BASIC interpreter what function to perform. This code represents a set of instructions for the BASIC interpreter only and is never seen by the peripheral device involved in the transfer. A list of operations for each BASIC keyword can be found in the 4050 Series Graphic System Reference Manual.

I/O Address

The I/O address is a two-part numeric code that presents instructions to the peripheral device. The I/O address is sent to the peripheral device before the data transfer begins.

The I/O address follows the keyword in the statement. It consists of an "at" sign (@) or a percent sign (%), followed by a primary address, followed by a comma, followed by a secondary address, and terminated with a colon (:).

The "at" sign (@) or the percent sign (%) specifies which delimiters are to be used during the I/O operation. Some applications involving GPIB input/output operations use the percent sign (%) to logically disconnect the 4052/4054 from the GPIB. Refer to the 4050 Series Graphic System Reference Manual for details.

The primary address is specified as a peripheral device number between 1 and 255. When the statement is executed, the peripheral device number is converted to a primary talk address or a primary listen address, and issued to the specified peripheral device. The primary address tells the peripheral device that it has been selected either to send data to or receive data from the random access memory. Peripheral device numbers for the system are divided into categories as shown in Table 2-1.

Table 2-1

DEVICE NUMBER ASSIGNMENTS

Device Number	Peripheral Device
0	System Disc (mass storage device)
1-30	External peripheral devices on the General Purpose Interface Bus
31-39	Internal peripheral devices connected directly to the microprocessor bus lines
40-255	Reserved for future use

Internal peripheral devices are preassigned the peripheral device numbers listed in Table 2-2.

Table 2-2

INTERNAL DEVICE NUMBERS

Device Number	Peripheral Device
31	GS keyboard
32	GS display
33	Magnetic Tape Unit
34	DATA Statement
35	Unassigned
36	Unassigned
37	Processor Status
38	Unassigned
39	Unassigned

Peripheral device numbers can be specified as a numeric expression in a statement, as long as the BASIC interpreter can reduce the expression to a numeric constant and round the constant to an integer within the range 1 to 255. This means that the primary address can be specified as a numeric variable; by changing the value assigned to the variable, different peripheral devices can be selected as the input source or output destination without changing the BASIC statement itself. The secondary address in an I/O address is issued immediately after the primary address and tells the peripheral device what the data transfer is all about. Since the peripheral device never sees the keyword in the statement, the secondary address provides the only way to tell the peripheral device what function is being performed by the BASIC interpreter. A secondary address is specified as a number from 0 through 32. Each number has a predefined meaning. For example, secondary address 12 means that the BASIC interpreter is executing a PRINT statement; secondary address 13 means that the BASIC interpreter is executing an INPUT statement, and secondary address 0 means that the BASIC interpreter is sending status information. The secondary address assignments for each I/O function performed by the BASIC interpreter are listed in the GPIB Section 10 of this manual.

Section 3

4052 AND 4054 ROUTINE MAINTENANCE

There is little need for routine maintenance of the Graphic Computing System except for occasional cleaning. There are no lubrication points and no vacuum tubes except for the crt. The solid state components provide stable operation with little need for routine adjustment. A routine maintenance schedule is recommended however. The frequency depends on how much the system is used and where it is used.

Routine service procedures that should be followed include the following:

- Clean the outer surface of the unit.
- Clean the tape heads every 6 hours of tape drive operation, 1000 hours of system operation, or whenever tape errors occur. Tape errors can be identified when the tape does a backup operation in an attempt to reread a record of data without error.
- The fan filter on the 4054 should be inspected monthly and washed with mild soap and water when dirty. Do not reinstall it while it is wet.

All motors and bearings in the Graphic Computing System are permanently lubricated and should not need lubrication. If a routine schedule for circuit adjustment and calibration is desired, a one-year interval is recommended. Refer to this section and the calibration procedure as necessary.

This section contains maintenance information, system disassembly and system reassembly procedures.

CLEANING

CAUTION

Avoid the use of benzene, toulene, xylene, acetone, or similar solvents which may damage the plastics in this instrument.

Surface Cleaning

Use a soft cloth dampened with a mild detergent and water to clean the display surface of the crt and the exterior of the cabinet.

Cleaning the Tape Head

The surface of the tape head (Figure 3-1) must be kept clean in order to read and write tape data accurately. Oxide from the tape and other foreign matter may be deposited on the head during tape operation. Use the following procedure:

Inspect the head by shining a light across the surface of the head. If the head is dirty, clean it as described below:

Use a cotton swab moistened with isopropyl alcohol or a magnetic head cleaner to rub off the accumulated matter on the head.

After removing the oxides and other accumulations from the head, use a clean dry cotton swab to polish the head and remove alcohol residue.

Cleaning Electrical Contacts

Freon TF (trichlorotrifluroethane) or isopropyl alchohol are suitable electrical contact cleaners. Don't use these solvents on the tape motor or fan motor; they may wash away the bearing lubrication.

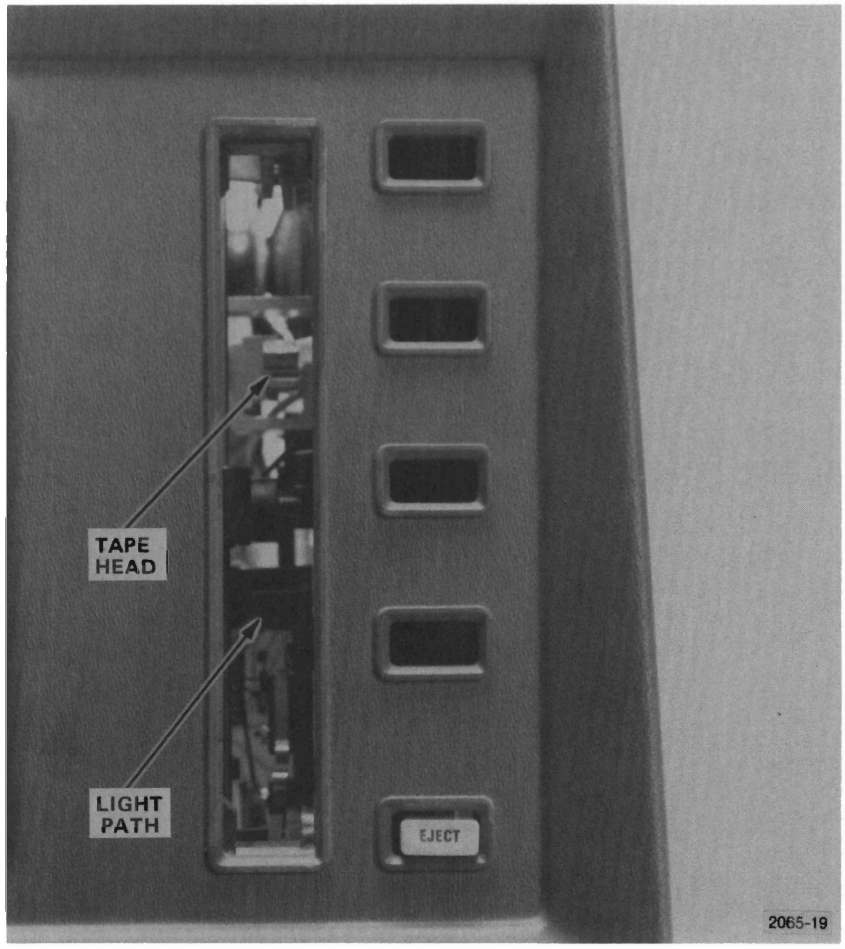


Figure 3-1. Tape Head and Tape Status Light Path.

CARTRIDGE RESPOOLING

The tape in the data cartridge used in the Graphic Computing Systems is not fastened at either end of the spool. The magnetic tape unit relies on light-sensing of small holes at either end of the tape to stop motion before the end of the tape is reached. Sometimes a circuit failure, a burned out lamp, or an obstruction in the light path may allow the tape to run off of the end of the spool. If you suspect a circuit failure or a burned out lamp, refer to the tape drive circuit description. To wind the tape back on the spool, use the following procedure:

1. Remove the four screws that attach the plastic cover to the metal plate (Figure 3-2).

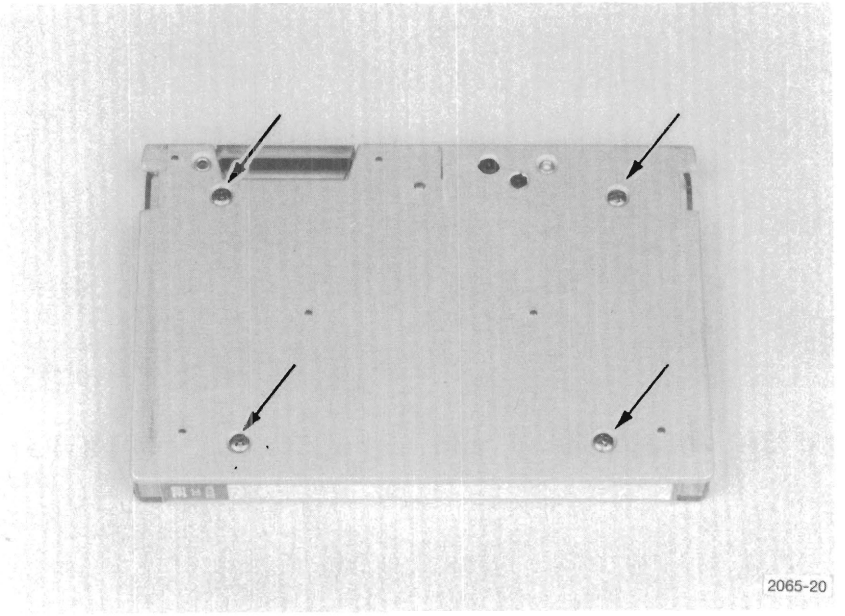


Figure 3-2. Cartridge Assembly Screws.

2. Carefully remove the metal plate. Be careful not to lose the write-protect cylinder or the small spring between the cylinder and the metal plate (Figure 3-3).

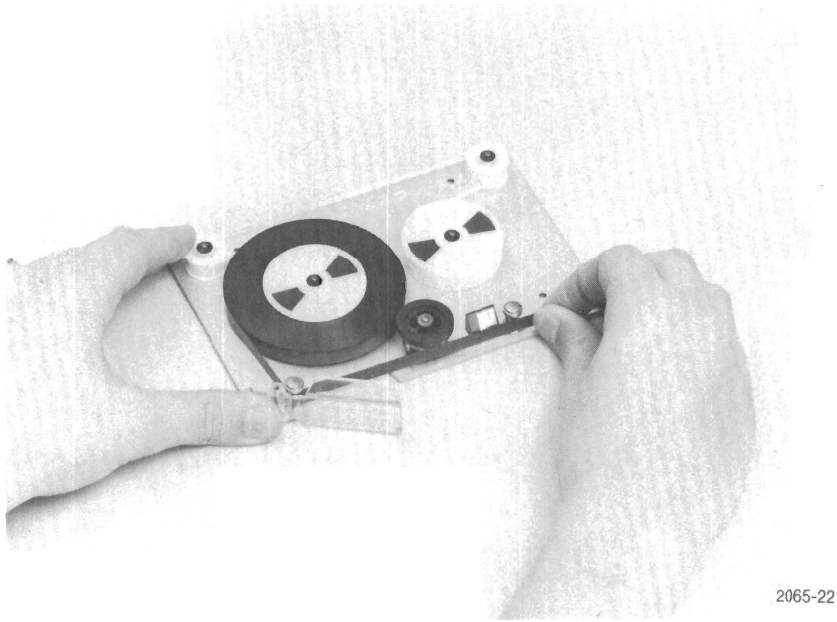


Figure 3-3. Positioning Tape.

3. Place the loose end of the tape across the front of the cartridge. Thread it through the front of the two guide posts. Keeping light tension on the tape, place the loose end of the tape around the outside of the take-up spool at the point where the spool meets the small tension band (Figure 3-4).

Figure 3-4. Beginning the Tape Winding.

4. Rotate the spool. Make the tape go around the spool with the loose end continuing around the inside of the spool (Figure 3-5). Do not press down on the tape on the full spool.

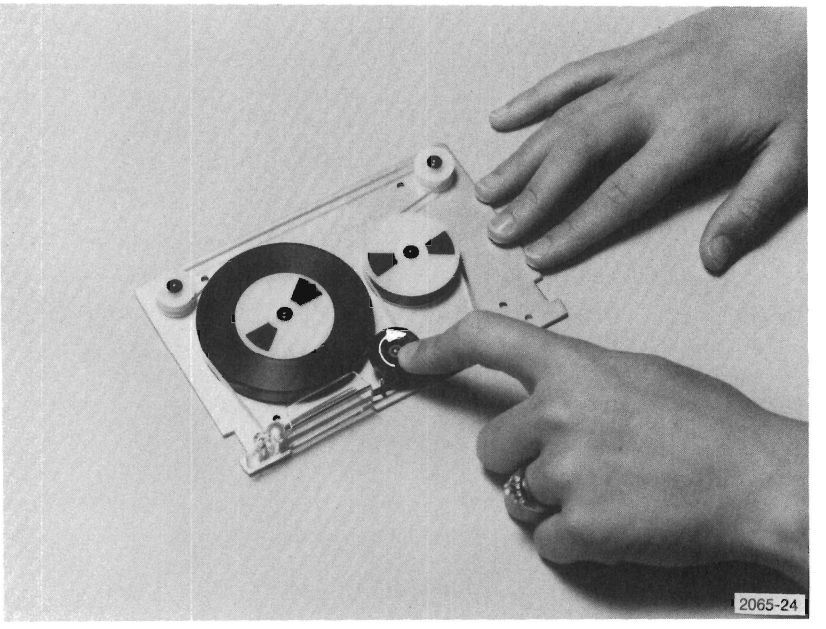


Figure 3-5. Winding the Tape.

5. Hold the loose end of the tape against the spool and continue to rotate until the loose end passes under the continuing length of tape. Continue the rotation for a few turns until the first set of sensing holes is reached. Make certain that these first windings stay evenly within the spool edges (Figure 3-5).

6. Make certain that the write-protect cylinder is in position with the spring washer between the cylinder and the metal cartridge base. Position the metal cartridge base over the plastic cover. Be careful not to catch or wrinkle the tape (Figure 3-6).

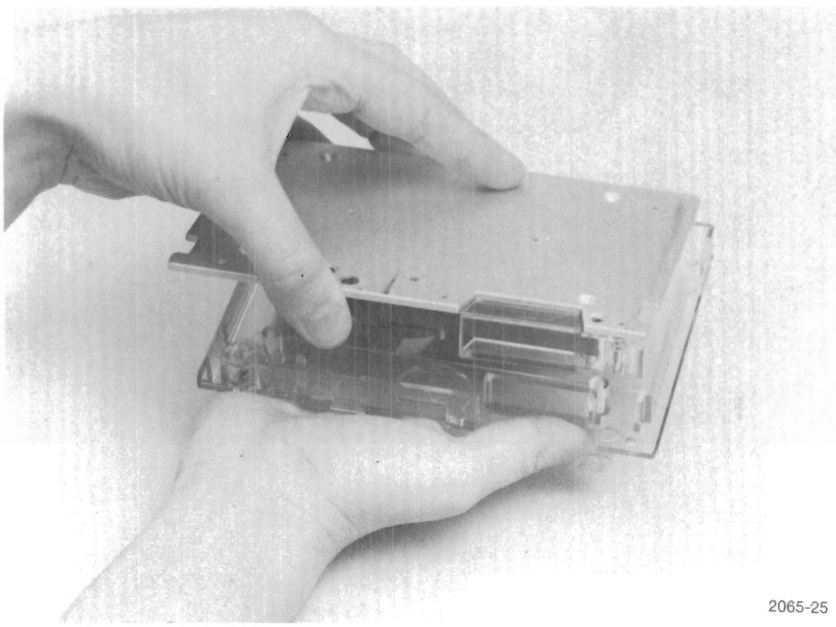


Figure 3-6. Assembling the Tape Cartridge.

7. Holding the cartridge together, install the four screws that attach the plastic case to the metal case.

8. Check the light path to see that it is free from obstructions. Refer back to Figure 3-1. Install the cartridge and run a few tape exercises such as TLIST or MTPACK to ensure that the problem does not come back. If it does return, try another tape to determine if the problem is the tape or a circuit problem.

STATIC-FREE WORK STATION

CAUTION

Some of the devices in the 4052 and the 4054 can be damaged by electrostatic voltages. Special precautions should be taken to avoid circuit damage during the handling of unprotected circuit boards and components.

Servicing of the Graphic Computing System should be done by qualified personnel at a static-free work station.

Replacement circuit boards are shipped in special bags of electrically conductive material. Boards should be shipped in these same bags to protect them.

A typical static-free work station (Figure 3-7) consists of a table with and electrically conductive top coating. The surface material should be resistive, such as carbon or treated polyethylene, instead of being highly conductive like a metal surface. The table top should be grounded through a resistor of approximately 200 k to 500 k ohms. The service technician should wear a conductive wrist strap that is tied to the table top with 100 k of series resistance. All test instruments should be grounded. No implements capable of generating or holding a static charge should be allowed on the work surface. This includes most paper.

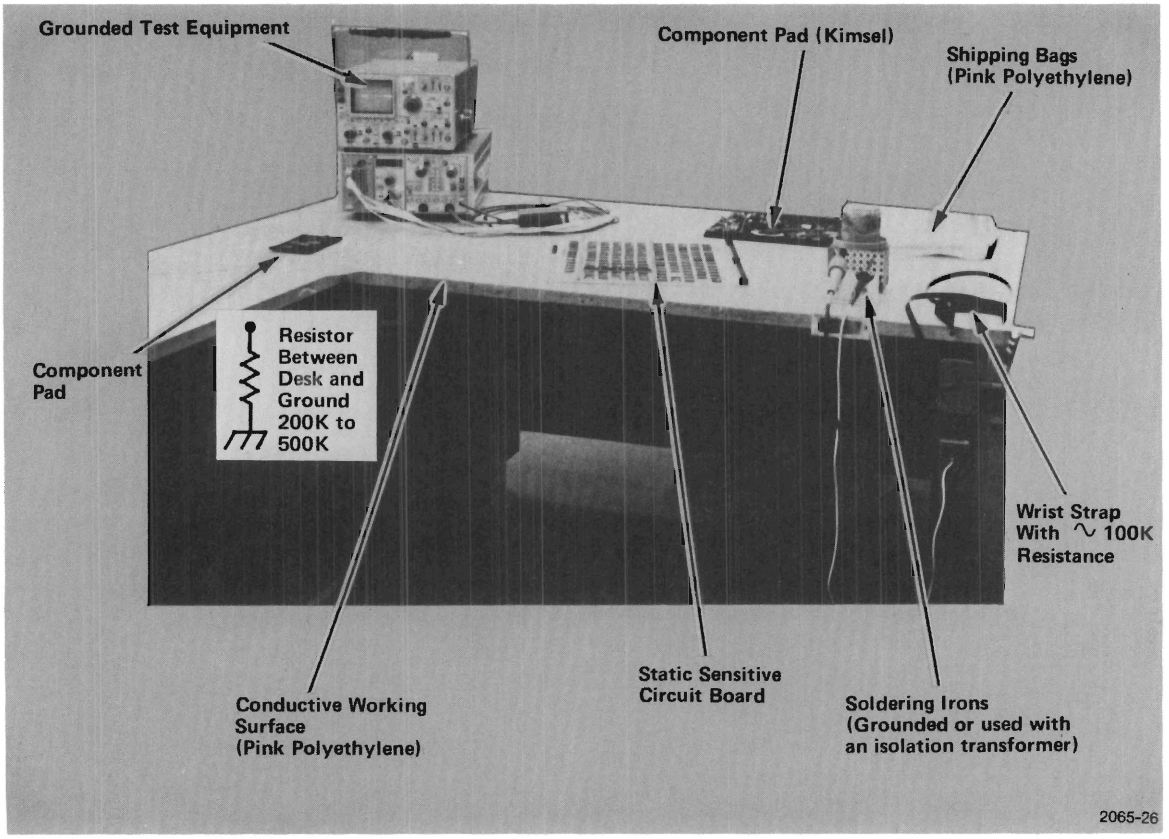


Figure 3-7. Static-Free Work Station Example.

An approved warning label to be used on shipping cartons is shown in Figure 3-8.

Figure 3-8. Warning Label for Shipping Cartons.

4052 DISASSEMBLY/ASSEMBLY

Removing the Cover and Backpack

1. Remove the cover to reach the test points and system adjustments.

2. Unplug the power cord (Figure 3-9). Loosen the two bolts on the lower sides the 4052 using a 5 6" hex driver. Remove the two rear screws that secure the cover. Use a # 2 Phillips screwdriver.

3. Remove the cover. To replace the cover, seat the rear corners first, then lower the front of the cover.

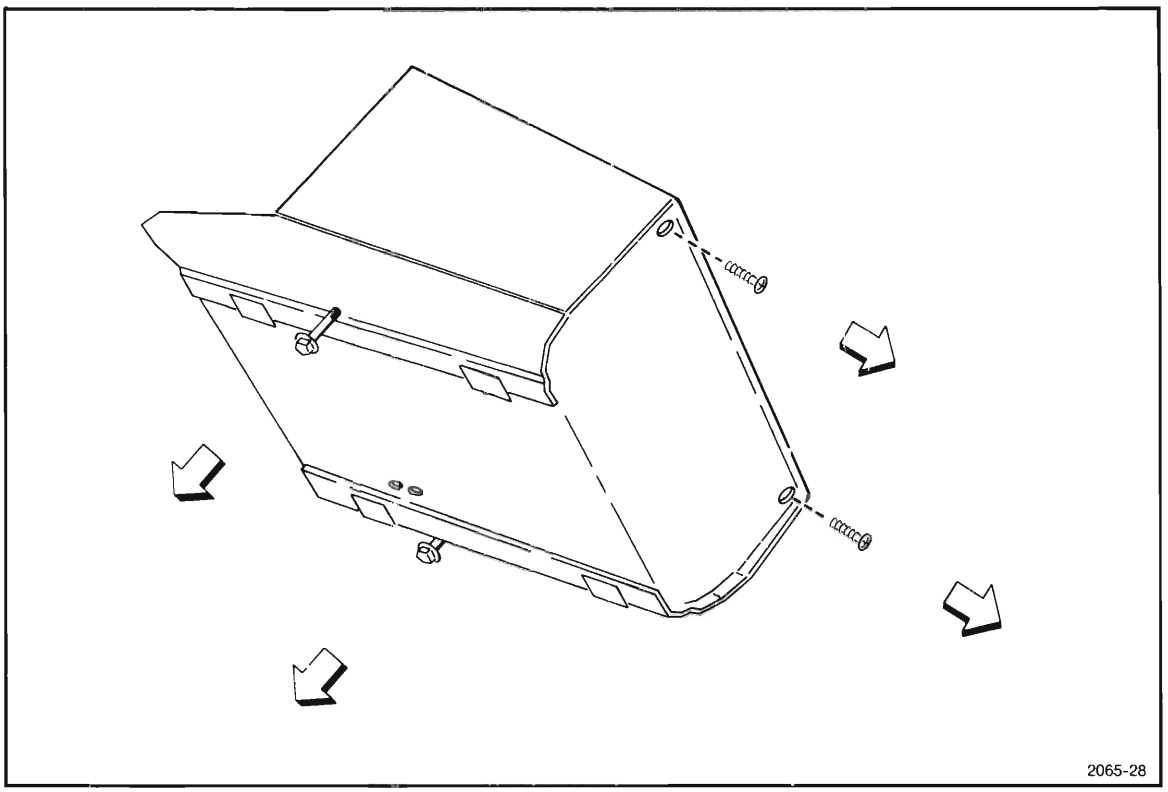


Figure 3-9. 4052 Cover Mounting Bolts.

4. Remove four Phillips screws to free the backpack (Figure 3-10). Pull gently near the bottom of the backpack to separate the edge card connectors. The shorter screws go in the top of the backpack.

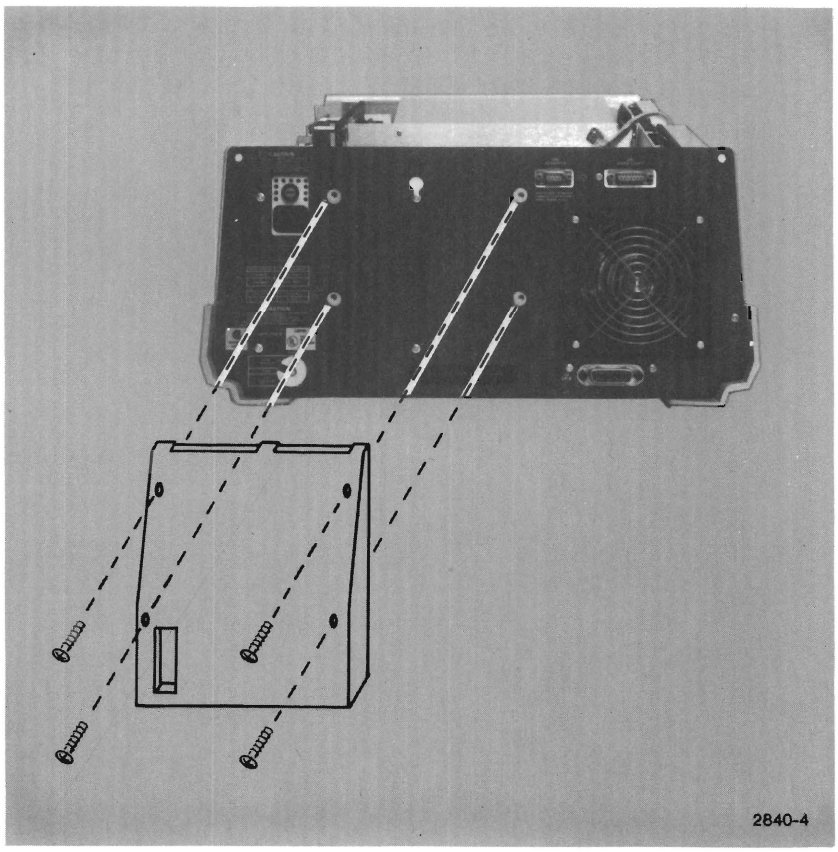


Figure 3-10. Backpack Removal.

Keyboard Access

1. Remove any tape cartridge from the system.

2. Remove the bezel that frames the crt face, indicator lights, and EJECT button (Figure 3-11). Lift the top flange of the bezel and then pull it forward. You may have to help it over the EJECT button.

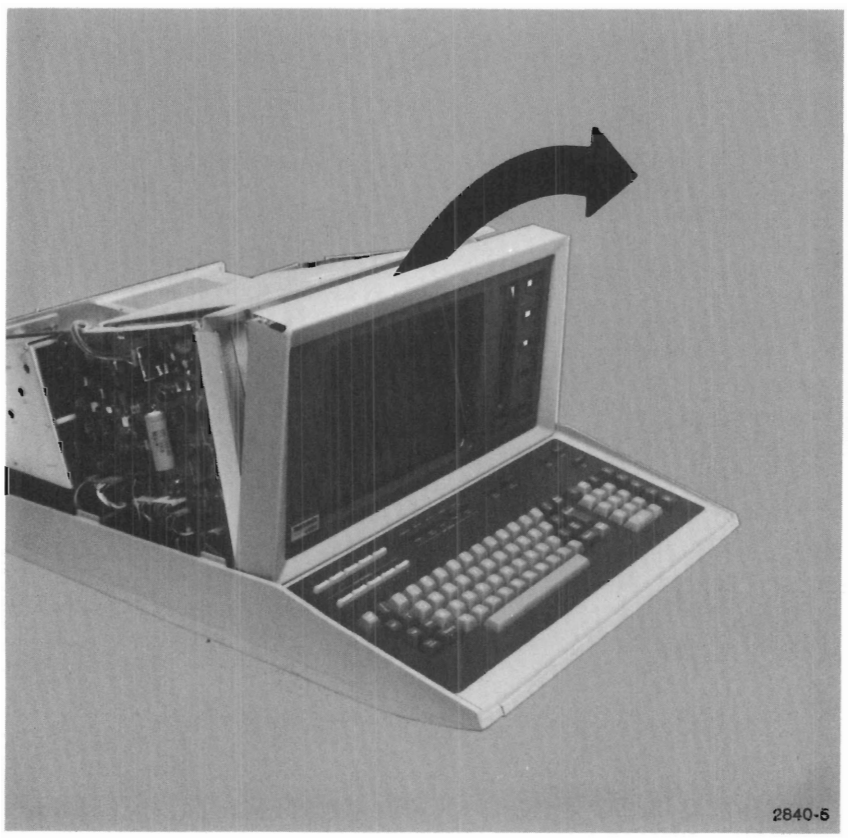


Figure 3-11. Front Bezel Removal.

3. Use the Phillips screwdriver to remove the screws that secure the keyboard (Figure 3-12).

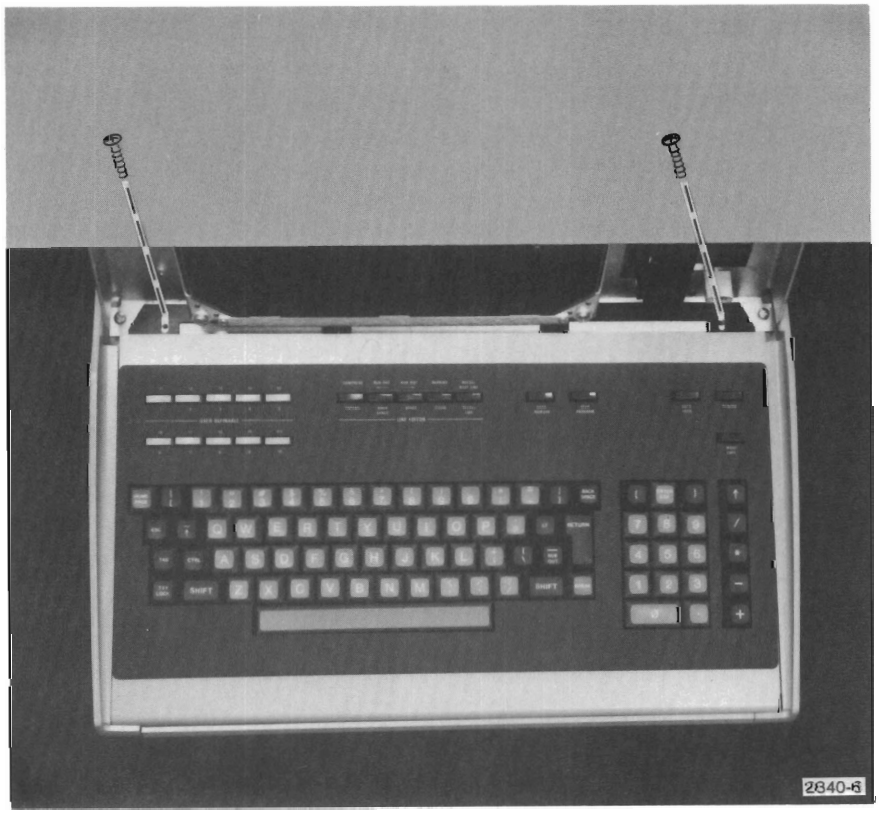


Figure 3-12. Keyboard Screw Removal.

4. Push the keyboard towards the display as shown in Figure 3-13. Push it towards the instrument until the bottom edge of the keyboard comes free from its retaining groove. Lift the keyboard out of the instrument.

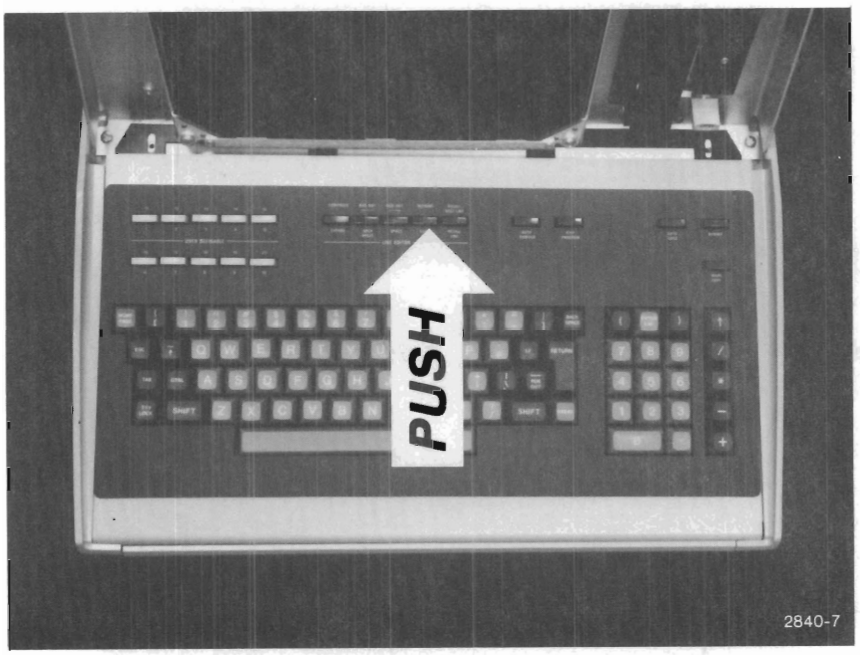


Figure 3-13. Keyboard Removal.

5. Either disconnect the two keyboard connectors, J30 and J31, and remove the assembly or place the keyboard on an insulating pad to one side of the instrument or on the top of the crt shield.

6. To further disassemble the keyboard, remove the 12 Phillips screws that secure the circuit board.

CRT Filter Access

1. The front bezel amd keyboard should be removed as previously described.

2. The crt filter has a foil strip around the outer surface to provide an electrical barrier to control electromagnetic interference. If a new filter is installed, the foil strip goes toward the face of the crt. The filter side that has the least amount of reflection should be placed outward when installed on the 4052.

3. Remove the top angle bracket from the crt mounting assembly (Figure 3-14). After removing one screw from each end, loosen the screws on the lower angle bracket.

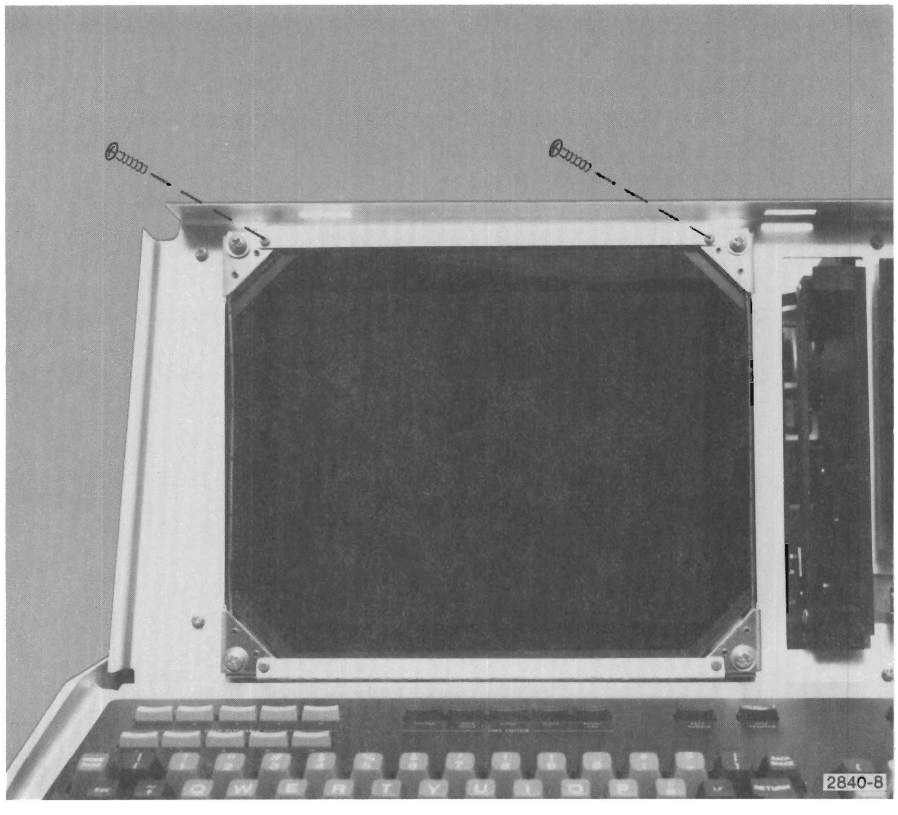


Figure 3-14. CRT Filter Access and Removal.

4. Remove the filter from the crt mounting bracket. Be careful not to scratch or break the filter.

5. Clean the face of the crt and the underside of the filter using a soft cloth and a mild soap and water solution.

6. To install the filter, place it in the recess in the neoprene mounting ring. The outer surface should be flush with the edge of the frame. It may be necessary to use a non-abrasive device like a toothpick to work the filter into place.

CRT and Deflection Yoke Removal and Replacement

WARNING

The crt may implode if it is handled roughly. Do not handle the crt by the neck. Wear protective clothing and a face shield when handling the crt.

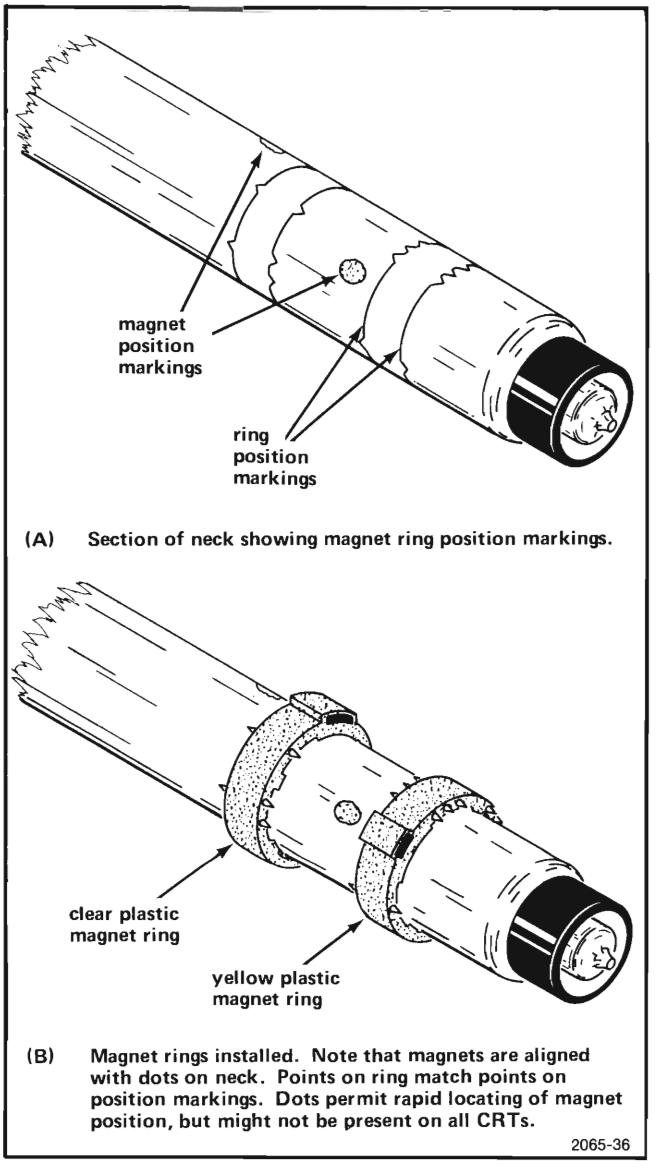
CRT Removal

1. Remove the cover and faceplate as previously described.

2. Remove the writing gun socket connector from the crt neck.

3. Remove the crt neck shield. Replace the nuts on the yoke adjustment without the shield.

4. The crt may have one or two magnet rings installed on its neck. If there are rings, mark their positions as in Figure 3-15. Next slide the ring(s) off the neck of the tube. If the rings are not removed, they may fall onto the circuit boards and cause damage.



(A) Section of neck showing magnet ring position markings.

(B) Magnet rings installed. Note that magnets are aligned with dots on neck. Points on ring match points on position markings. Dots permit rapid locating of magnet position, but might not be present on all CRTs.

Figure 3-15. CRT Magnet Ring Location Details.

5. Remove the four screws that hold the face of the crt in place. Next remove the metal frame. Figure 3-16.

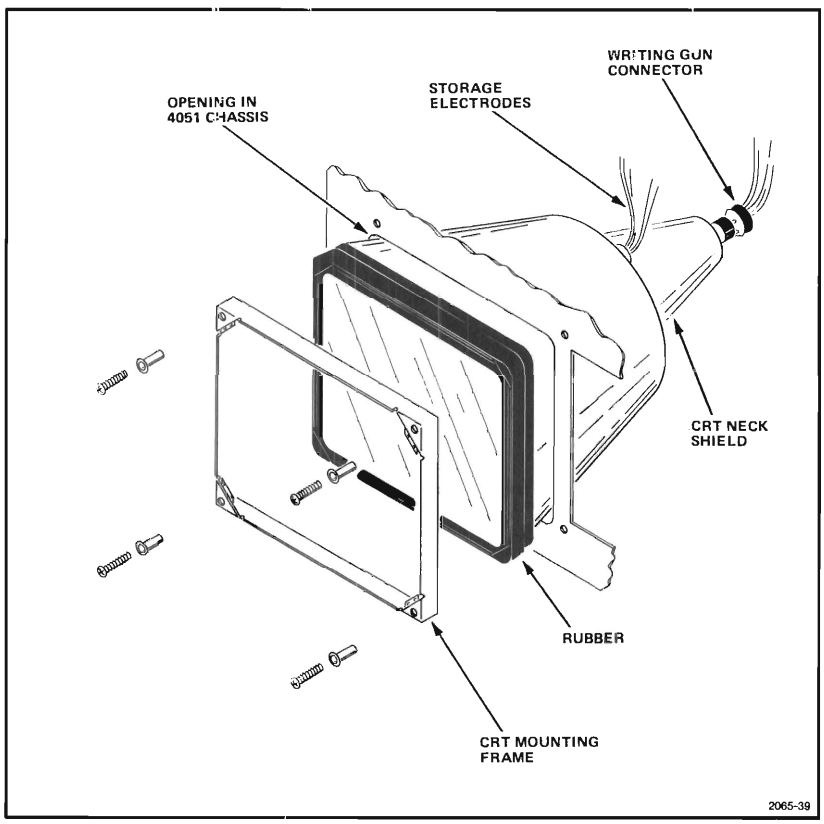


Figure 3-16. CRT Mounting Detail.

6. Apply glycerin lubricant sparingly to the neck of the crt using a cotton swab as shown in Figure 3-17.

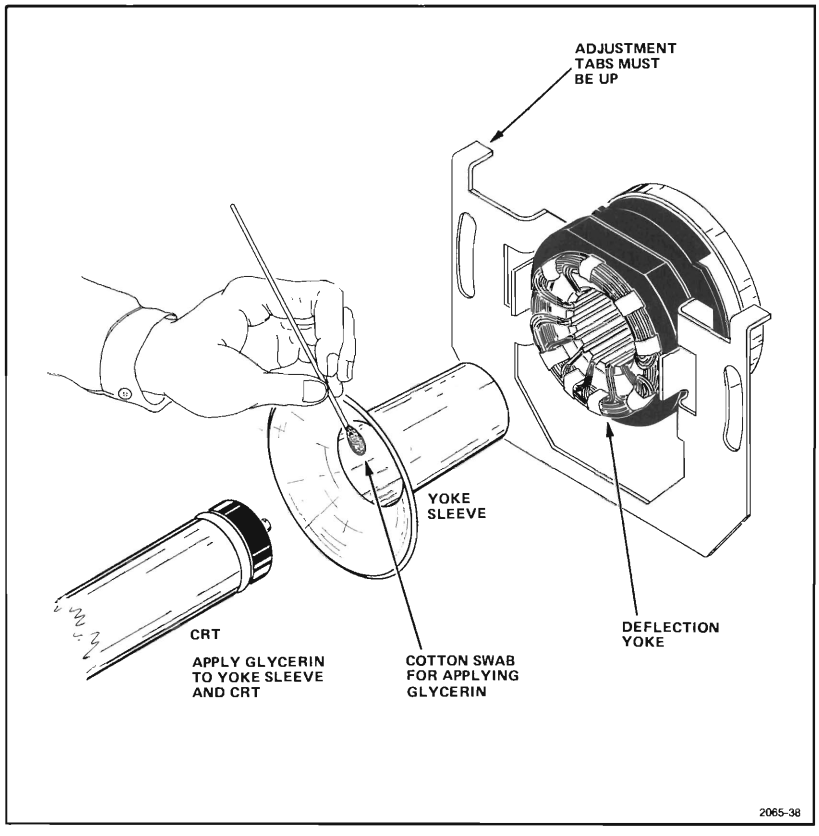


Figure 3-17. CRT Installation/Removal Detail.

CAUTION

Do not drop lubricant onto the circuit boards. Do not place side pressure on the crt neck.

7. Slide the crt out of the front of the unit using a rotating motion, not a sideways motion. The rotating motion makes it easier to remove the neoprene ring in the yoke.

8. Remove the storage electrode from the body of the crt near the neck.

9. After crt removal, place the crt on firm padded surface. The neoprene sleeve around the neck and the larger ring around the screen can now be removed. Water or glycerin may be used to help remove the small neoprene yoke sleeve ring.

Power Supply Access

1. Remove the cover of the 4052 as previously described.

2. Remove all of the connectors and Phillips screws as shown in Figure 3-18. The screw to be removed last is marked in the illustration.

3. The power supply module can now be lifted up and out. Be careful not to wipe off the silicon gel on the bottom flange. The silicon gel is used to increase heat transfer to the instrument frame.

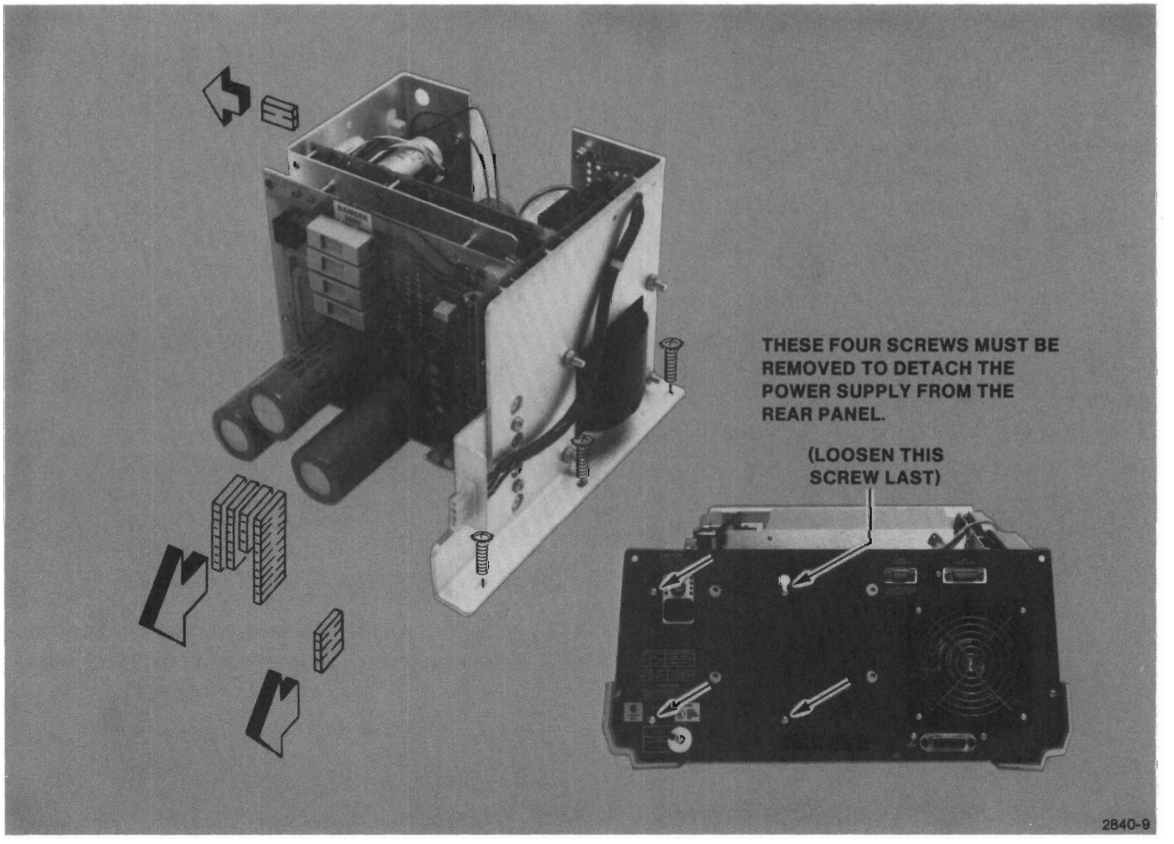


Figure 3-18. Power Supply Removal.

ALU and Memory Board Removal

CAUTION

The ALU and Memory Boards have devices that can be damaged by electrostatic voltages. It is recommended that the instrument be worked on at a static-free work station. Devices mounted in the boards are not as susceptible to static charges as unmounted components.

1. It is necessary to remove the keyboard to allow the ALU/Memory Board set to be removed from the front of the instrument.

2. Note the polarities and remove the three connectors from the front of the board set.

3. Remove the six Phillips screws that secure the board set to the chassis (Figure 3-19).

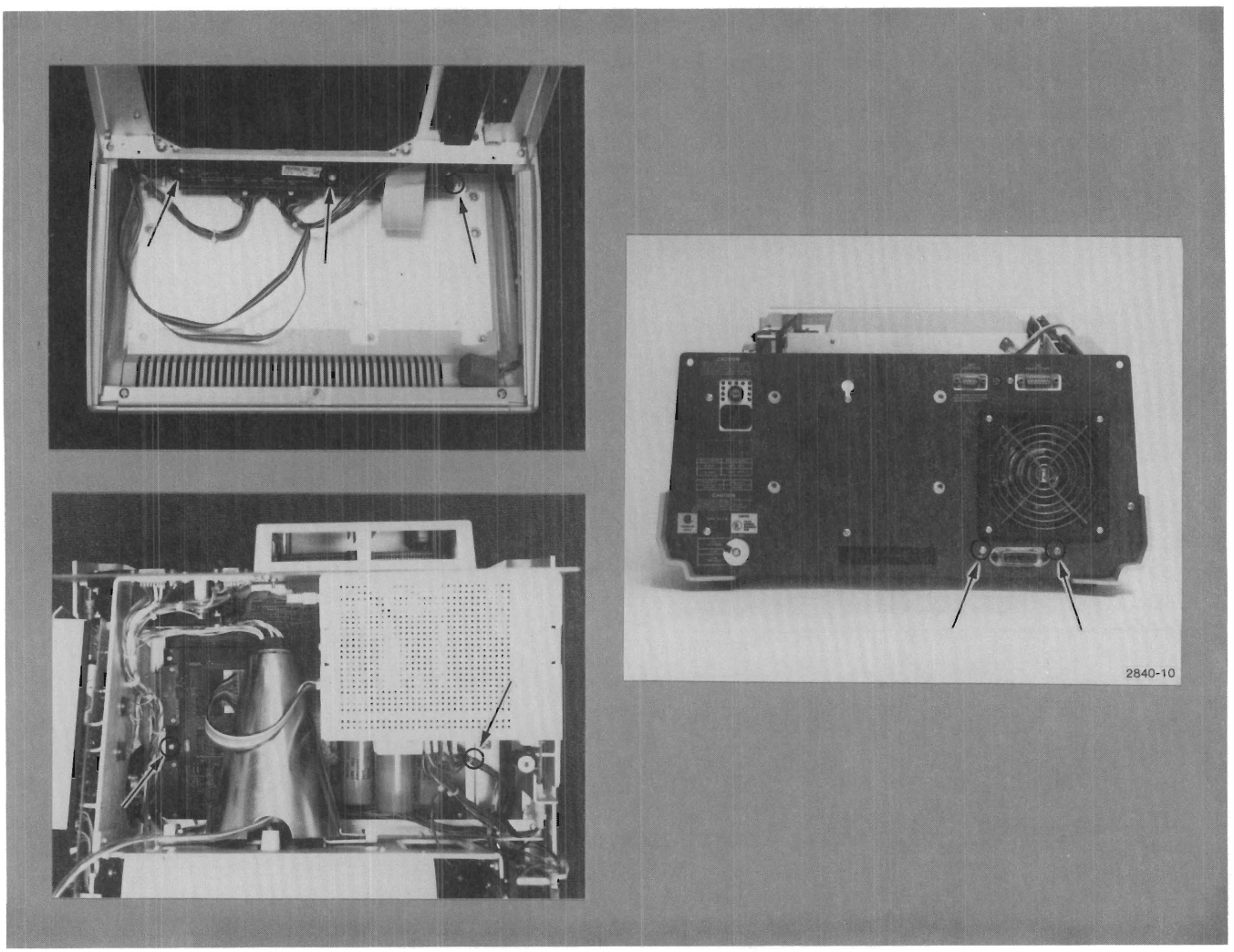


Figure 3-19. ALU/Memory Board Removal.

4. Pull the board set out carefully by its supporting rails. There are two layers of boards and they can be damaged by static charges.

5. Remove the 14 screws that hold the two layers of boards together.

6. To service the boards, place an insulating pad over the front lip of the 4052 chassis to keep the boards from shorting to the chassis. See Figure 3-20. Use a pink polyethylene shipping bag or similar material material that doesn't develop electrostatic charges. Paper can develop dangerous charges and should not be used. Unfold the boards, keeping the interconnecting cables connected and place them alongside on insulating material. Reconnect the cables from the 4052.

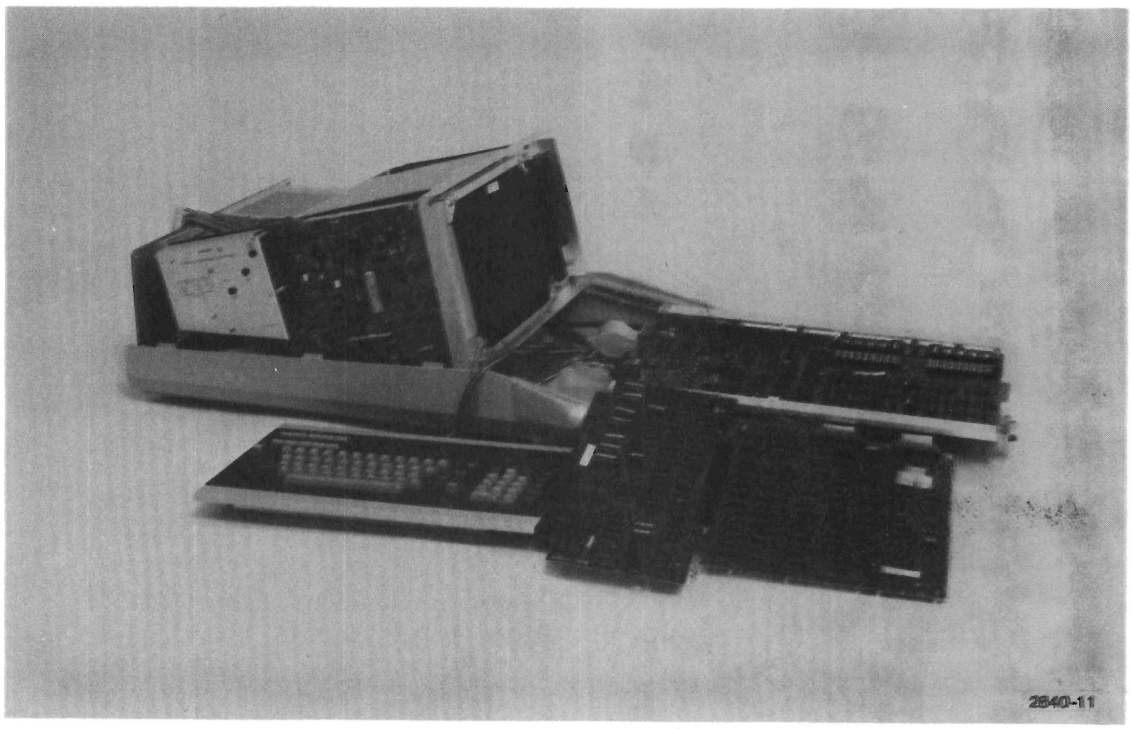


Figure 3-20. Service Layout for CPU Board and Memory Board.

Display Board Replacement

1. Remove the intrument cover to reach the Display Board.
2. To reach the high voltage test points and adjustments, remove the three Phillips head screws that hold the protective shield.
3. Remove the six Phillips screws and two Teflon screws that secure the Display Board.
4. Remove the nine connectors to heat-sinked transistors directly under the board and all other connectors. The crt gun connector is an octal connector which may be detached with a gentle pull on the wires that come out from the rear of the crt neck shield.
5. When the Display Board is replaced, be careful to replace the connectors just the same as they were removed.

Magnetic Tape Assembly Replacement

To remove or replace the Magnetic Tape Drive Board, use the following procedure:

1. After the instrument cover is removed, remove the two Phillips head screws on the right front of the 4052. One screw is just above the BUSY indicator light, the other is just below the EJECT button (Figure 3-21).
2. Remove the two Phillips screws on the rear of the mag tape assembly. Remove all connectors and then slide the unit back and up, allowing the EJECT button to be drawn through the front panel.
3. To further disassemble the unit, remove the eight Phillips screws that secure the Tape Drive Board to the assembly and remove the connectors.

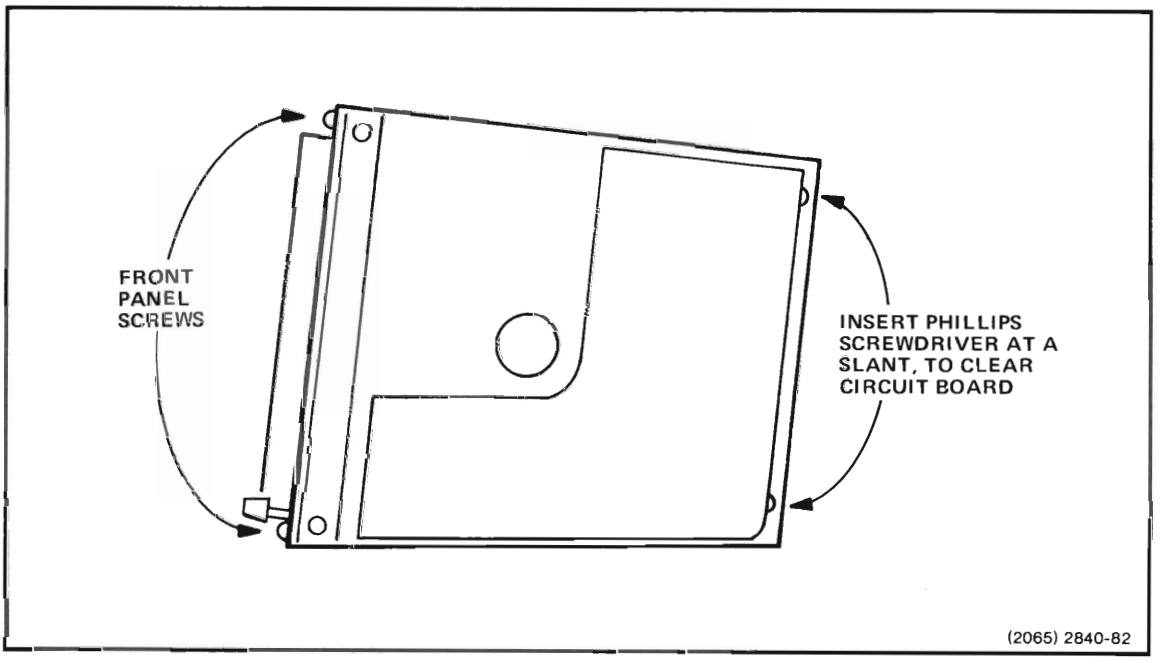


Figure 3-21. Tape Unit Mounting Screws.

4054 DISASSEMBLY/ASSEMBLY

Removing the Cover and Backpack

The cover must be removed to reach most of the test points and system adjustment points.

1. Unplug the power cord from the rear of the 4054. Using a 5 6" hex driver, loosen the two bolts on the lower sides of the 4054. Use a #2 Phillips screwdriver to remove the four rear bolts that hold the 4054 cover (Figure 3-22).

2. The cover can then be removed. To replace the cover, seat the rear corners first, then lower the front of the cover.

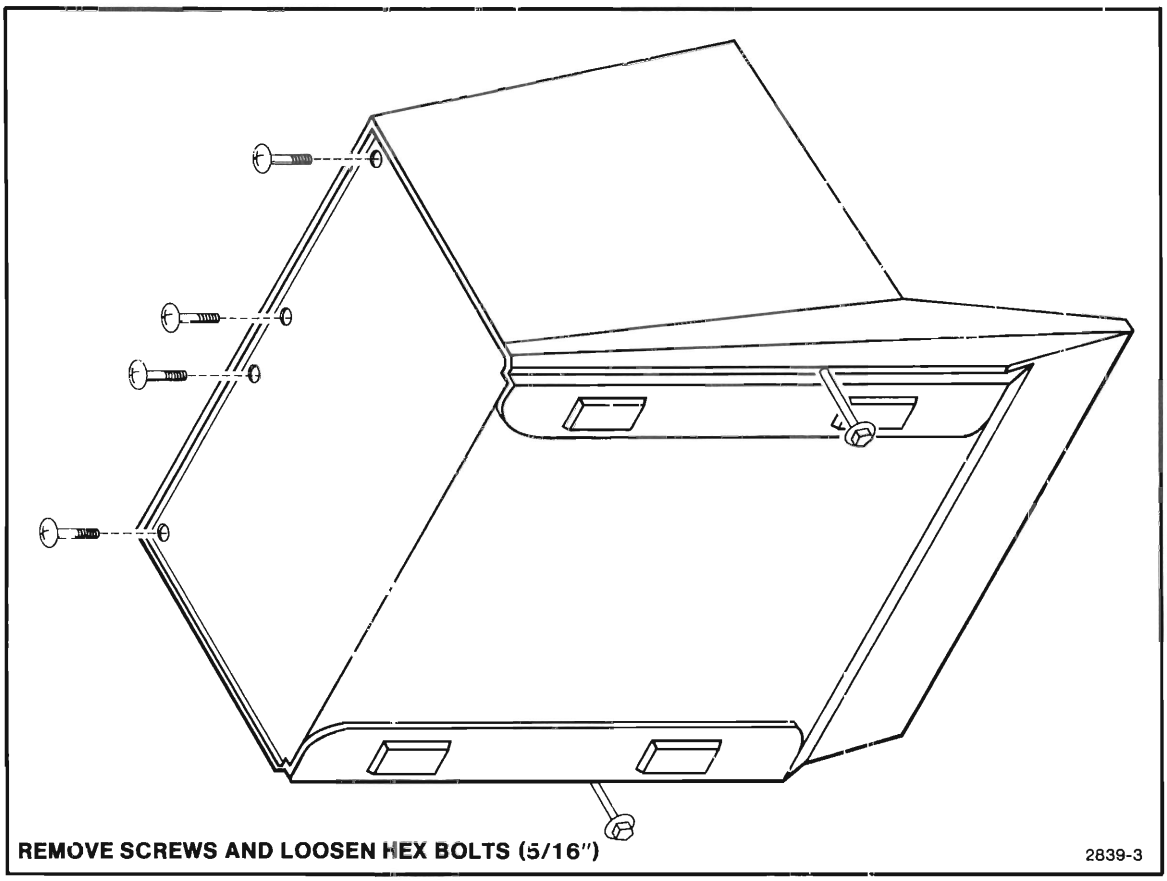


Figure 3-22. 4054 Cover Removal.

3. The backpack is removed by unscrewing the four Phillips screws (Figure 3-23). Next pull gently near the bottom of the backpack to separate the card edge connectors. Note that the shorter screws were removed from the top of the backpack.

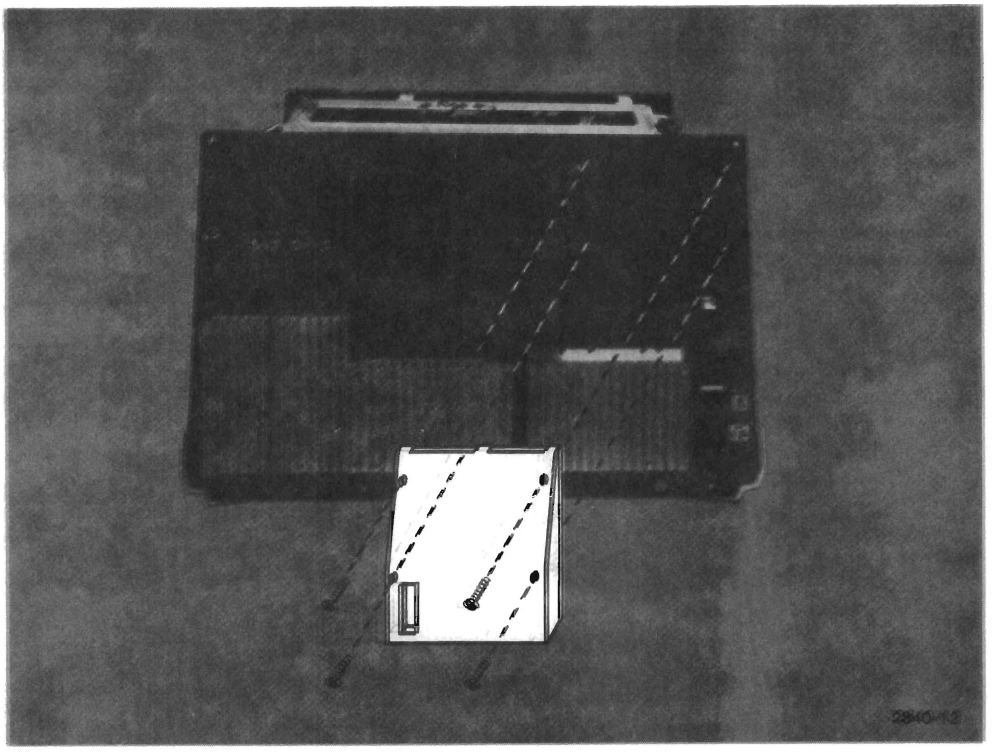


Figure 3-23. 4054 Backpack Removal.

Keyboard Access

1. Remove any tape cartridge from the system.

2. Remove the front bezel of the instrument. This is done by pressing the two springs at the top and tipping the bezel forward at the top. You may have to help it past the EJECT button. Next lift it clear from the instrument.

3. Use the Phillips screwdriver to remove the bolts that hold the keyboard in place.

4. Use the pushing motion shown in Figure 3-24 to force the keyboard against the display until the bottom edge comes free from its groove. Now lift the keyboard out of the instrument.

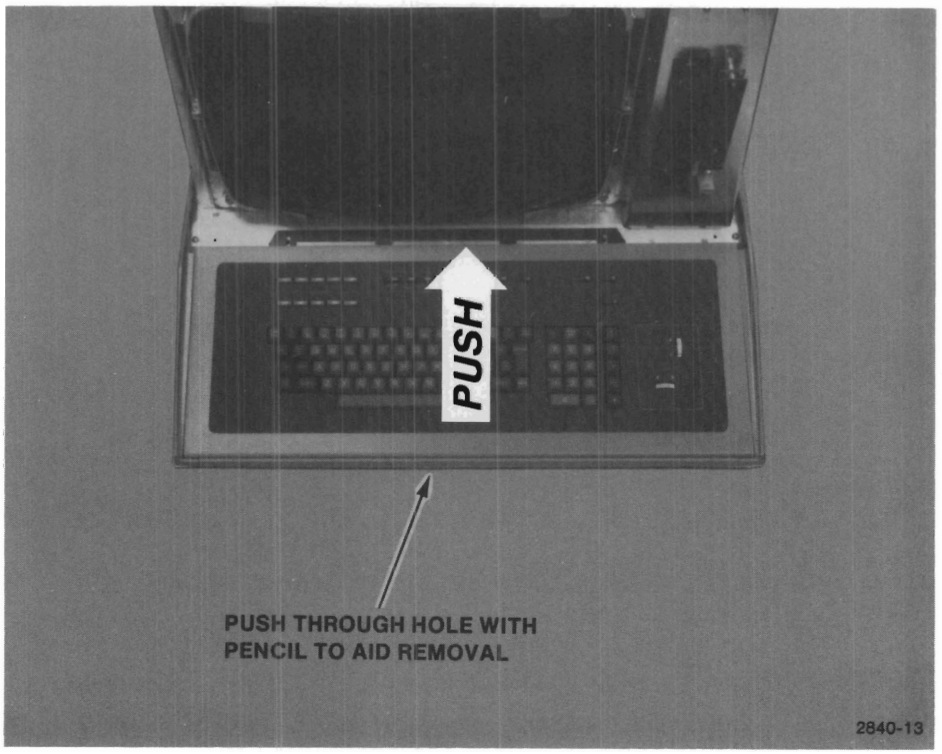


Figure 3-24. Keyboard Removal.

5. The keyboard connectors can now be removed or the assembly can be placed on an insulating pad.

6. Further disassembly of the keyboard module can be done by removing the 12 Phillips screws that secure the circuit board.

Light Filter Cleaning or Replacement

CAUTION

The light filter is fragile and can be cracked by rough handling. Don't force it into position.

1. Loosen and pull out the lower light filter clamps. See Figure 3-25.

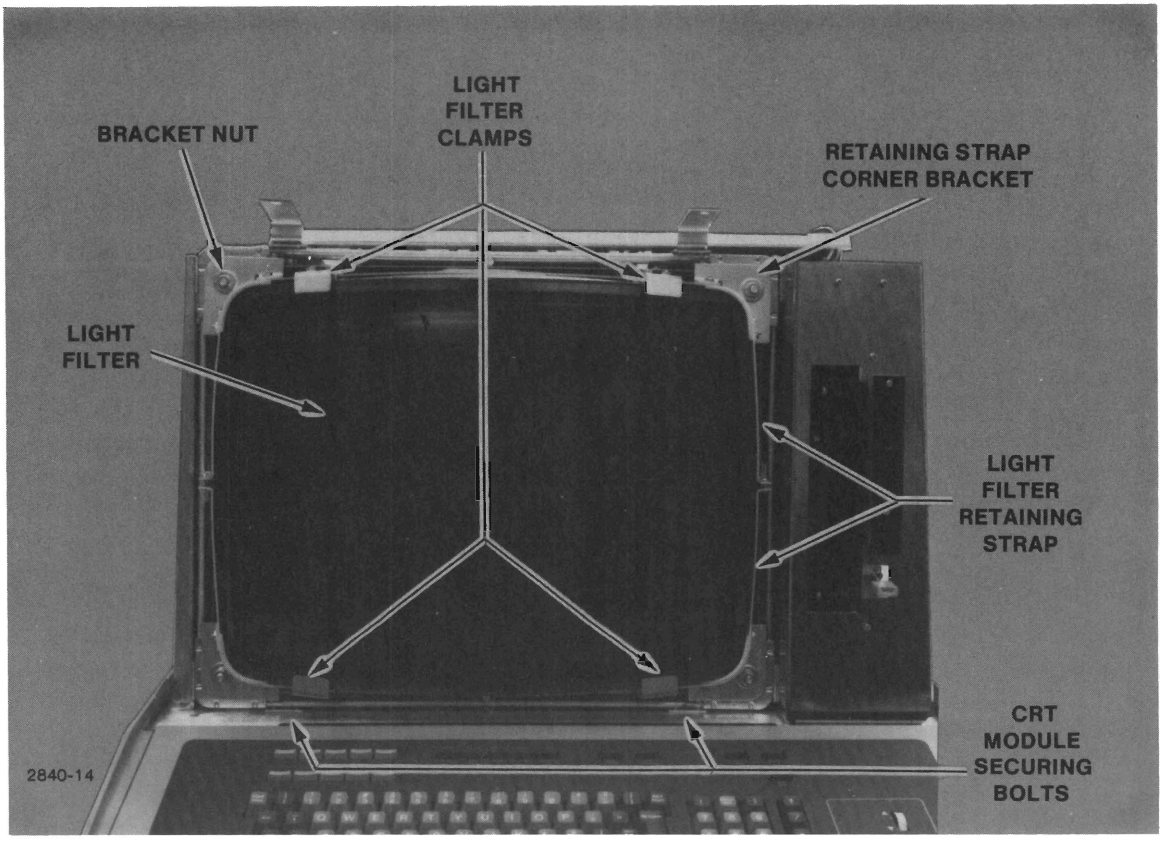


Figure 3-25. Light Filter Brackets and Hardware.

2. Loosen the upper light filter clamps. Loosen the light filter retaining strap, then loosen the retaining strap corner brackets. Move the corner brackets out of the way to free the light filter.

3. When the light filter is free, remove the upper light filter brackets and remove the light filter.

4. Clean the crt face and the under side of the light filter with a soft cloth and a solution of mild detergent and water. Dry with a soft cloth.

5. Reverse the removal process to reinstall the filter.

CRT Replacement

WARNING

The crt module is heavy. It requires two people to handle it and guide the cables through the holes. Do not put undue pressure on the crt neck as it may implode. Wear protective clothing while handling any crt.

1. Unplug the power cord.

2. Remove the light filter according to the previous instructions. Retighten the light filter retaining strap and the corner brackets. Reinstall the light filter clamps.

3. Remove the crt socket, the deflection cable from the Deflection Amplifier Board, and the storage cables from the Hard Copy Interface Board.

4. Remove two crt module securing clamps from the chassis bulkhead under the crt module. See Figure 3-26.

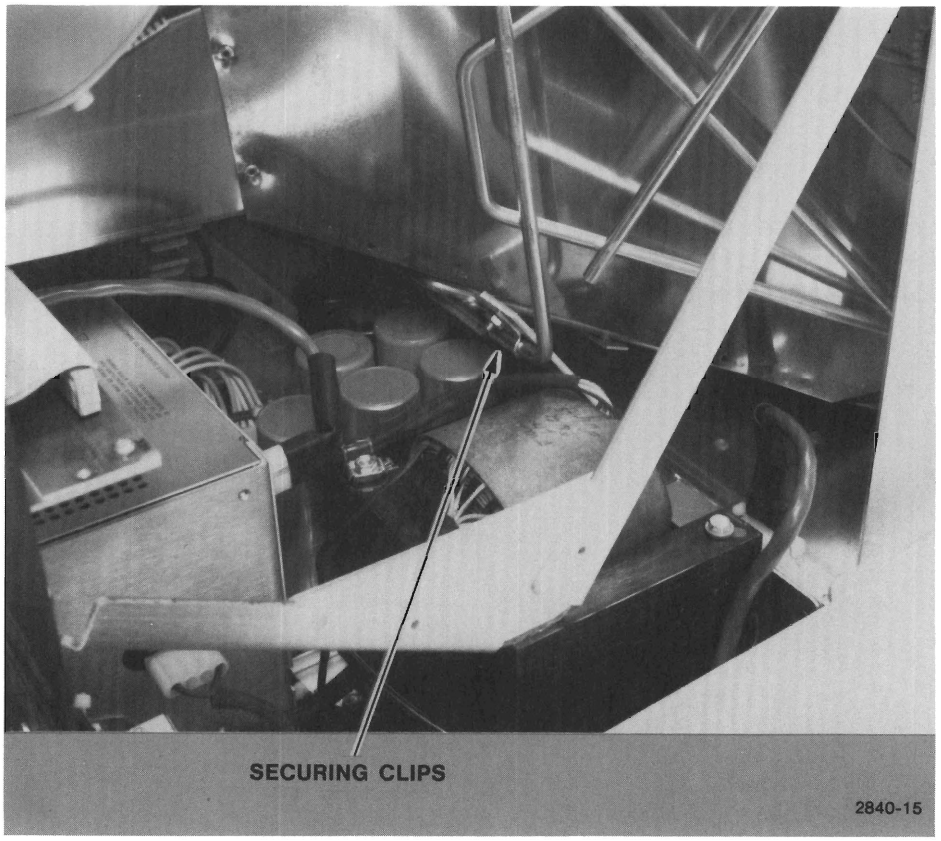


Figure 3-26. Side View Showing Securing Clamps.

5. Remove two securing bolts from the chassis just under the lower edge of the crt screen. See Figure 3-25.

6. Place a soft foam pad or a cushion on the work surface in front of the monitor to receive the removed CRT module.

7. Remove the last eight securing bolts from the upright brackets holding the crt module. (Four bolts are on each side.) Roll the crt module, face down, onto the pad.

8. Remove the securing nuts from the light filter retaining strap corner brackets (Figure 3-27). Disconnect the small ground lug located on one side of the crt module.

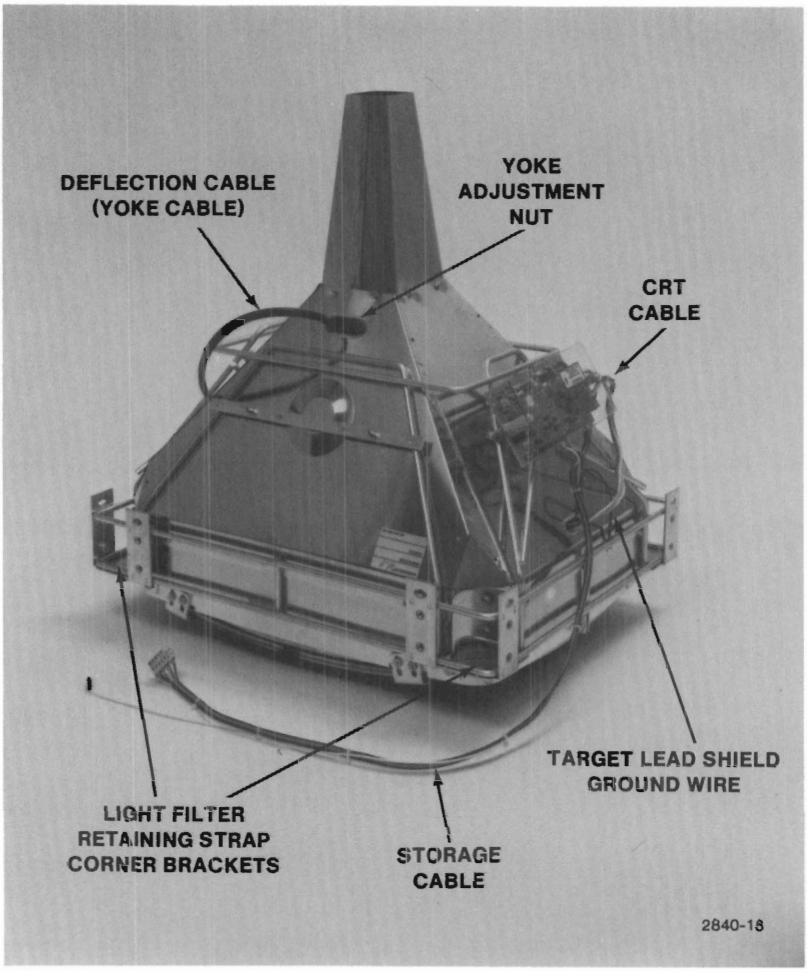


Figure 3-27. CRT Module.

9. Check to see that module is free of the crt, then pull the module straight up from the crt while guiding the deflection leads and the storage cables through their openings in the module.

10. Note the orientation of the crt cables and ground lug. Place the new crt on the cushion with its cables and ground lug oriented in the same way. Transfer the yoke to the new crt.

11. Lower the crt module down over the new crt while feeding the cables through their holes. Attach the ground lug.

Perform the removal steps in reverse order to complete the reinstallation of the new crt. Now refer to the Calibration Procedure for crt adjustments.

Rotating the CRT

When a residual pattern is noticed on the crt after repeated erasings, the crt life can be extended by rotating the crt as follows:

1. Remove the crt, as described previously.

2. Rotate the crt module 180 degrees as it sits on the foam pad.

3. The Hard Copy Amplifier Board will be on the opposite side of the crt module but the cables are long enough to reach to the new position.

4. Remove the connectors on J206 and J203 on the Deflection Amplifier Board. Twist each connector 1/2 turn and reconnect each to its respective jack.

5 V Switching Power Supply Removal

There are two large thumbscrews at the bottom right hand of the rear panel. Loosen these screws, remove the three connector plugs from the power supply and remove the bracket on the top of the supply. Now take the switching power supply out of the rear of the instrument for servicing.

ALU/Memory Board Set Removal.

1. This board set is held in place by two bolts through the crt module bracket and two hinge pins at the back. To gain access to much of the rest of the instrument, remove the front two bolts and fold the boards back out of the way. See Figure 3-28.

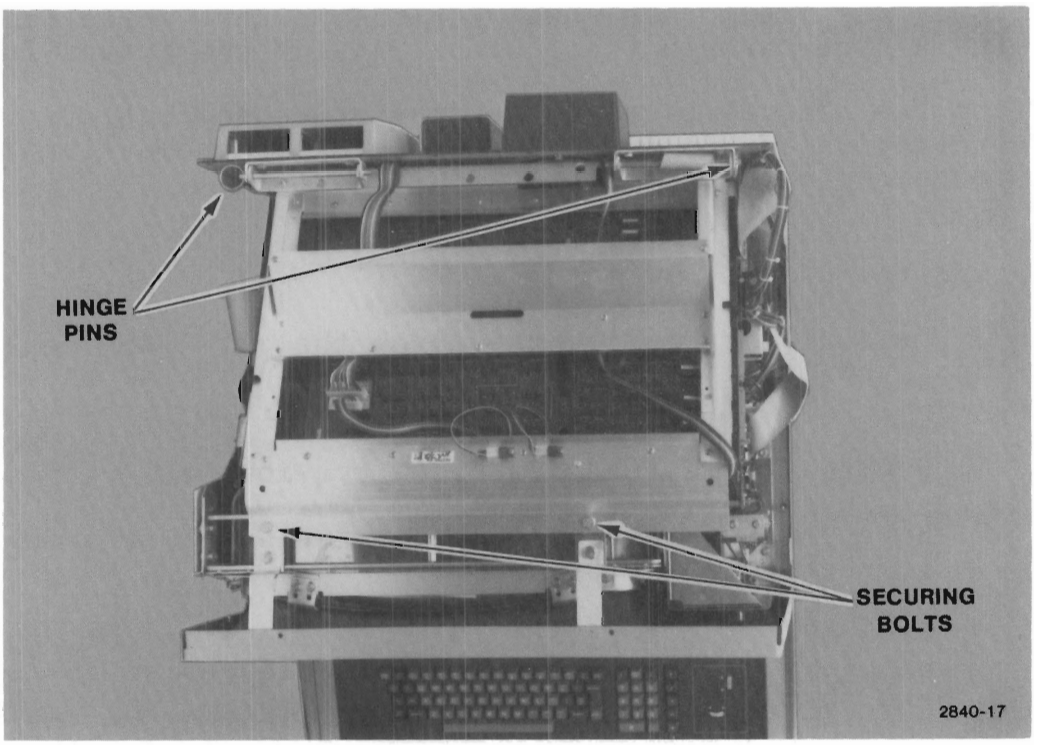


Figure 3-28. ALU/Memory Board Set Removal.

2. To remove the board set, remove the connecting cables. Remove the two retaining bolts on the front edge of the board set. Remove the two hinge pins by pulling outward on the rings on their ends. Lift the board set free from the instrument.

Low Voltage Power Supply Board Removal

The Low Voltage Power Supply Board is difficult to remove. Remove all connecting plugs (Figure 3-29). Unscrew the 4 Phillips head screws securing the board to the chassis. Leave the rear edge of the board in place and lift the front edge of the board. Guide the tops of the capacitors past the crt bracket and remove the board.

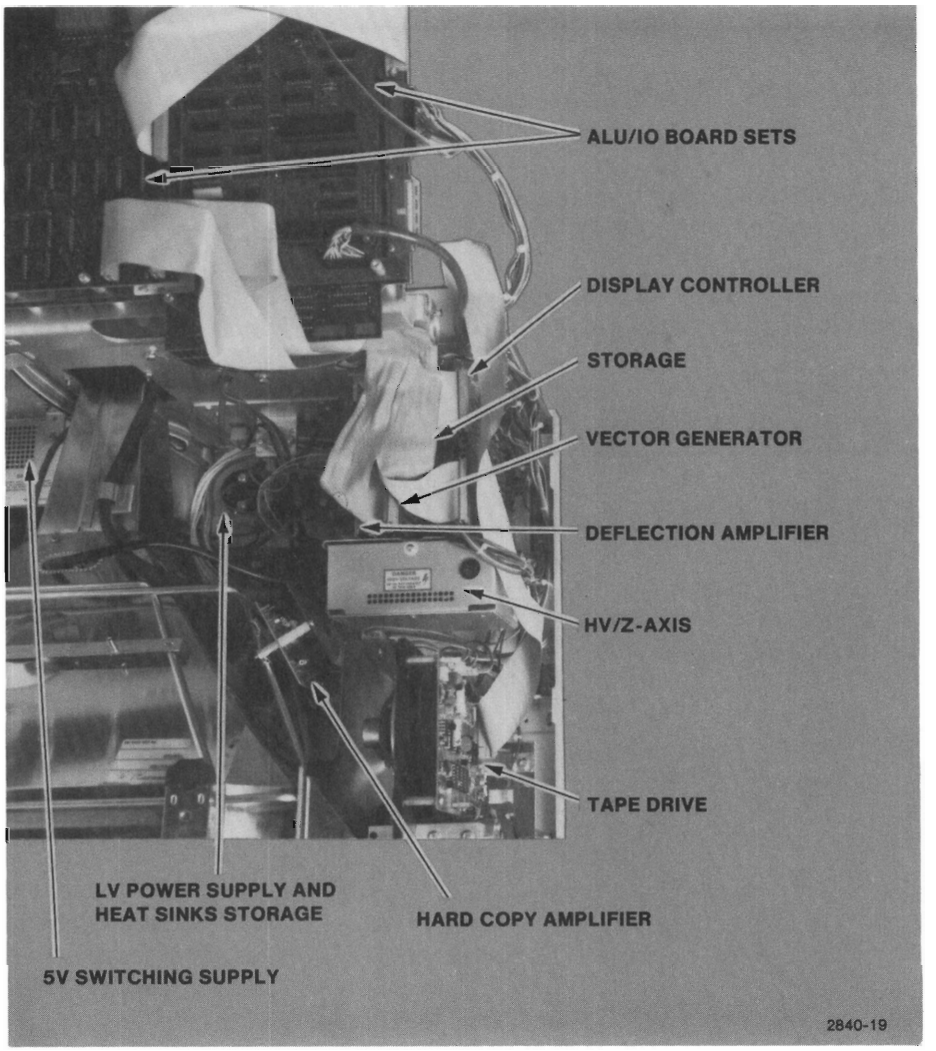


Figure 3-29. Board Placement.

Removal of Vector Generator or Display Controller Boards

The Vector Generator or Display Controller Boards may be removed from the instrument by folding back the large board set on top, removing the connecting cables on the top of the boards and pulling up on them to remove them from the instrument.

Removal of High Voltage/Z Axis Board.

The High Voltage/Z Axis board can be removed by the following steps:

1. Remove the crt base cover on the rear panel and unplug the cable from the crt base.
2. Remove the retaining screw from the top of the HV/Z Axis board and pull up on the board to remove it.

Deflection Board Removal

In order to remove the Deflection board, first remove the back panel from the instrument. Figure 3-30 shows which screws hold the back panel in place. Several cables from the back panel have to be unplugged. The board can now be pulled up and unplugged from the instrument for replacement or repair.

Storage Board Removal

In order to remove the Storage Board, first remove the back panel from the instrument. Figure 3-30 shows which screws hold the back panel in place. After the back panel is removed and its connecting cables are unplugged, the Storage Board can be pulled up to unplug it and the board removed for replacement or repair.

Tape Drive Mechanism Removal

The tape drive mechanism used in the 4054 is the same as that used in the 4052. Refer to the 4052 section of the maintenance instructions for removal information.

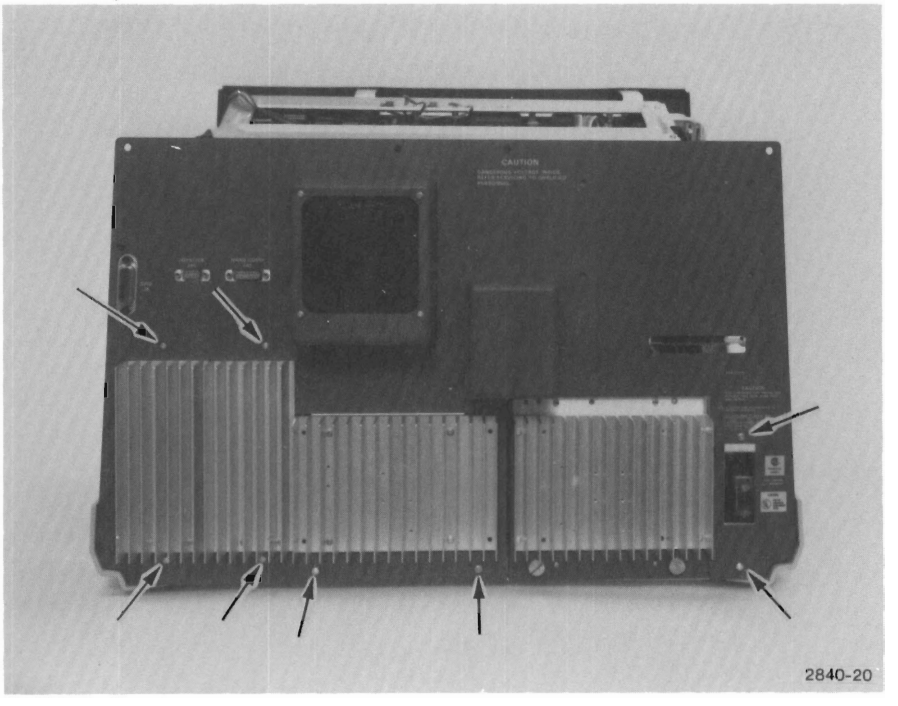


Figure 3-30. Rear Panel Securing Screws.

Section 4

4052 AND 4052A CALIBRATION PROCEDURE

GENERAL INFORMATION

This calibration procedure is for both the 4052 and the 4052A. In general most of the procedures are the same. Whenever a difference exists, it will be noted. Unless it is indicated otherwise, the terms 4052 and 4052A may be used interchangeably.

This calibration procedure is intended for use by a qualified person who is familiar with both digital and analog circuitry and knows how to use the necessary test equipment.

Equipment Required

Phillips screwdrivers, #1 and #2 points.
5/16" and 11/32" hex nut drivers
Small shaft (1/8") standard blade screwdriver
Insulated alignment tool (1/8" or smaller blade
3/32" and 1/16" Allen wrenches
Digital frequency counter (TEKTRONIX DC501 or equivalent)
Voltmeter (TEKTRONIX DM510 or equivalent)
High Voltage Probe for 4 kV
Calibration Tape Cartridge 067-0781-02
15 mHz Dual Trace Oscilloscope (TEKTRONIX T935A or equivalent)
Deflection Alignment Graticule (067-0654-01)

Cabinet Removal

WARNING

If you don't unplug the power cord, you may touch parts of the circuitry with the cover as you remove it. You could receive a dangerous shock. The instrument could also be damaged. Turn off the power and refer to Figure 4-1 for the location of the screws that hold the cover on. Remove the screws and lift off the cover carefully. Be careful not to hit circuit components during removal.

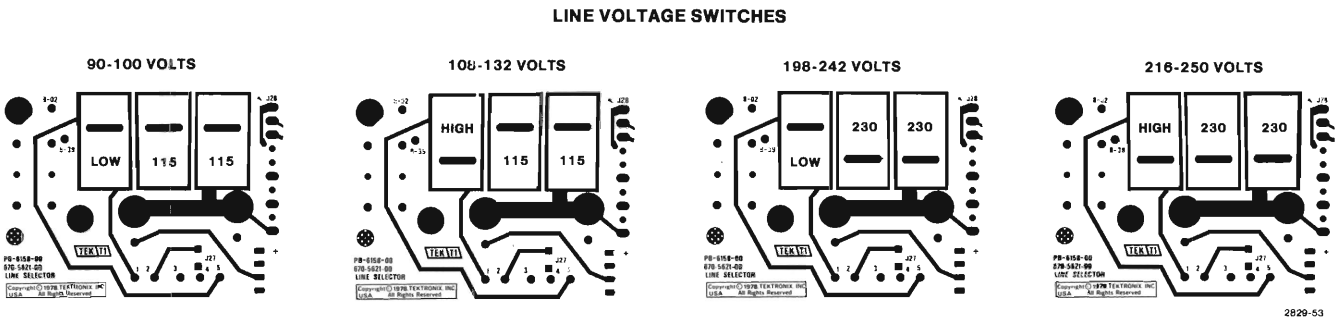


Figure 4-1. Line Voltage Selector Switches.

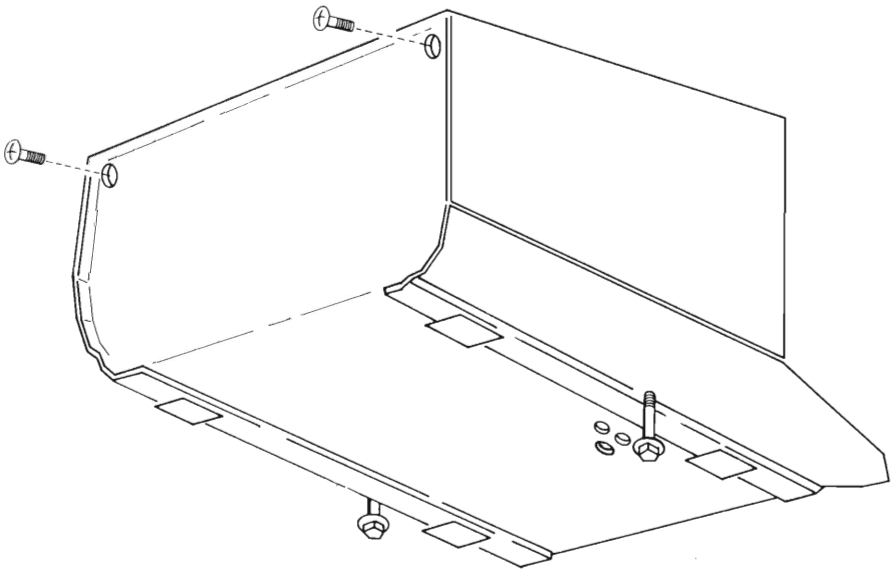
Power Line Voltage Selection

The power line input voltage is selected by setting three switches. The switches are located under the power supply cover on the left side as viewed from the back of the 4052.

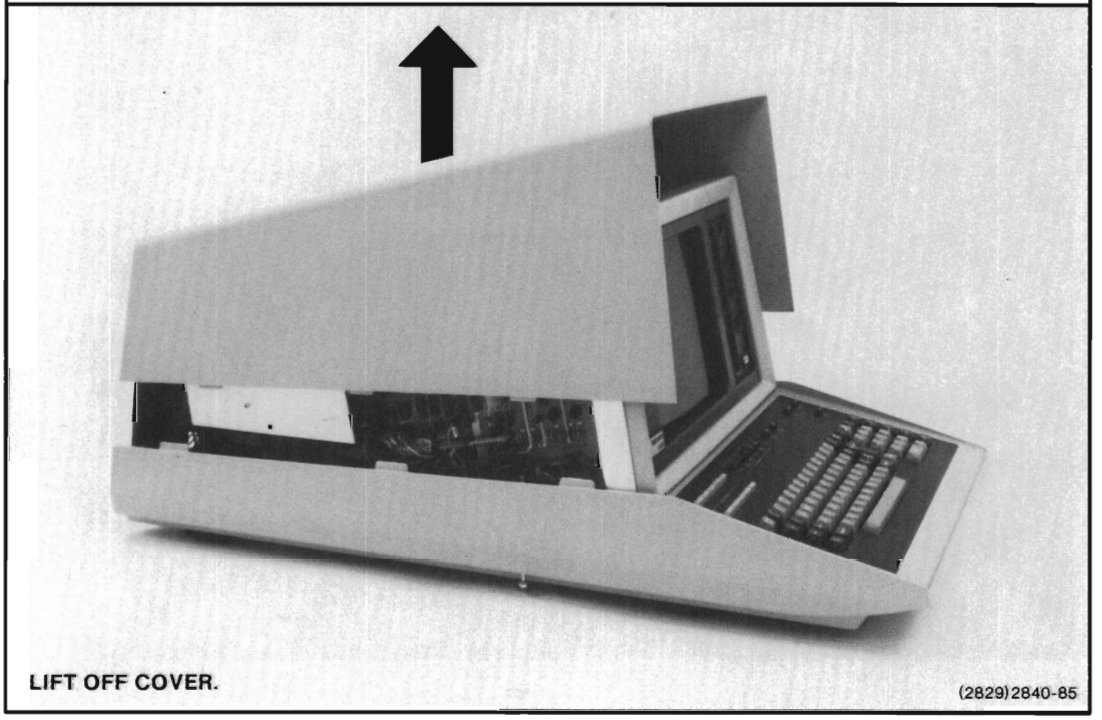
The input power ranges are 90-110 volts, 108-132 volts, 198-242 volts, and 216-250 volts. The appropriate range is set by placing the switches in the desired position (Figure 4-2).

WARNING

Any other switch combination is not valid and may cause damage to the power supply or the 4052 system. The system must have the right power cord for the selected input line voltage.



REMOVE SCREWS AND LOOSEN HEX BOLTS (5/16").



LIFT OFF COVER.

(2829)2840-85

Figure 4-2. Cover Removal Procedure.

POWER SUPPLY CALIBRATION

Adjust the power supplies or check them by placing a voltage meter between TP51 (+15 V) and TP50 (Ground). Refer to Figure 4-3 for adjustments and measurement points. The regulated voltages should fall within these ranges:

+15 V +/-1%
+12 V +/-5%
-12 V +/-2%
+5.05 V +/-1.5%

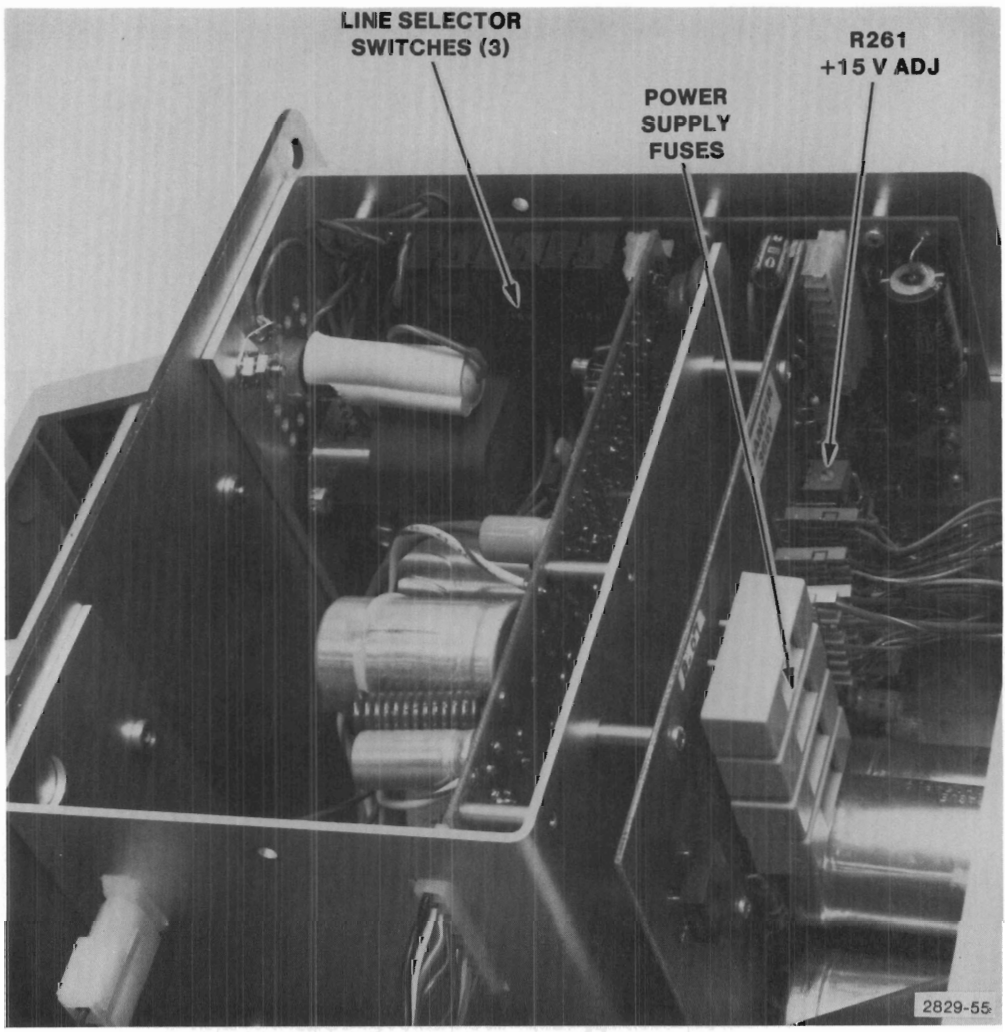


Figure 4-3. Power Supply Checkpoints.

DISPLAY CALIBRATION

Refer to Figure 4-4 for locations of the following adjustments.

1. High Voltage Adjustments.

   Turn off the power. Remove the high voltage shield. Connect a high voltage probe to TP102, and turn on the power. Adjust R224 for approximately -3850 V.

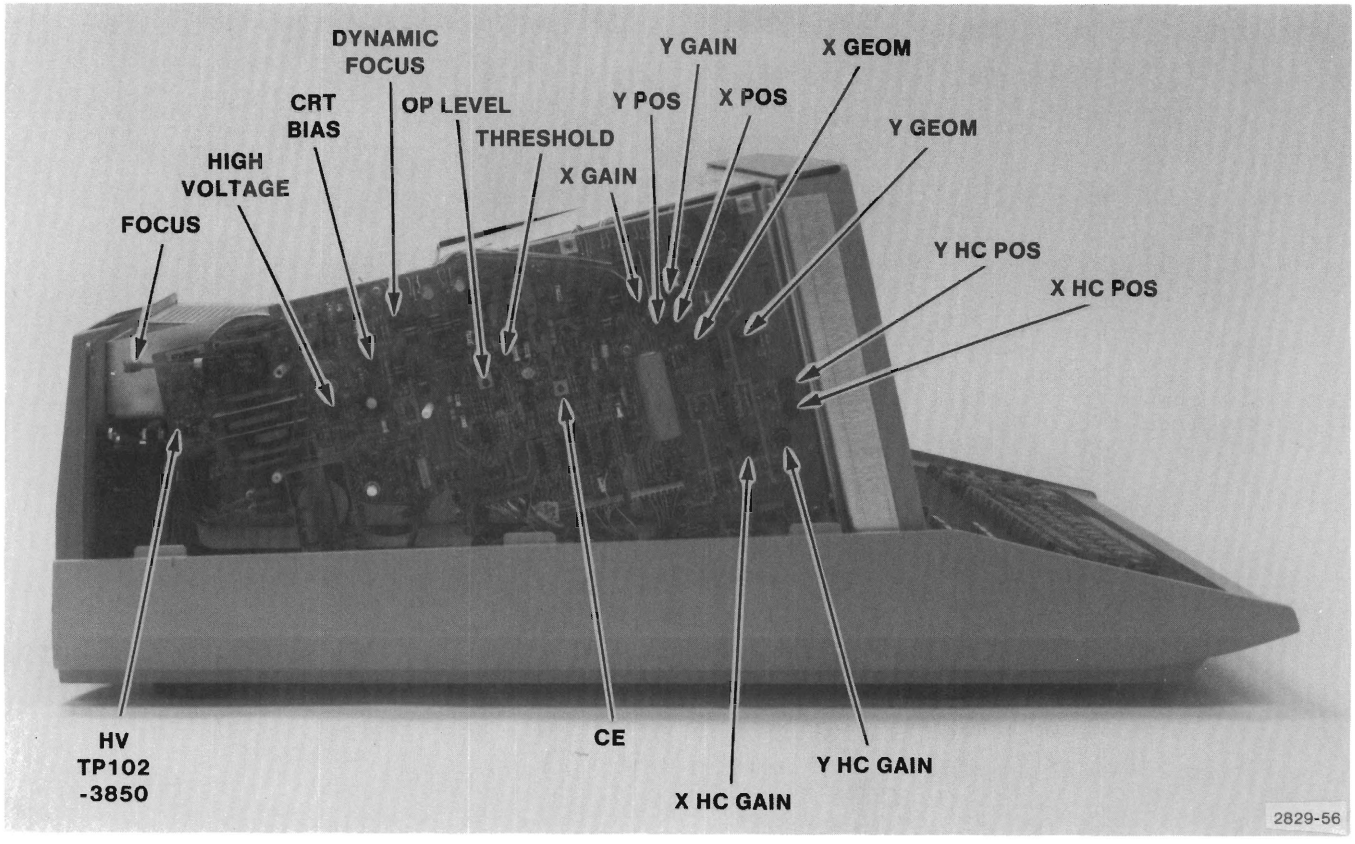


Figure 4-4. Display Board Checkpoints and Adjustments.

2. Collimation Voltage Adjustments

Turn the power off and then remove J50. This disables the high voltage. Place the voltmeter probe on J58-3. Turn the power on and adjust R359 for the voltage specified on the crt shield (Figure 4-5). This will be about 85 V.

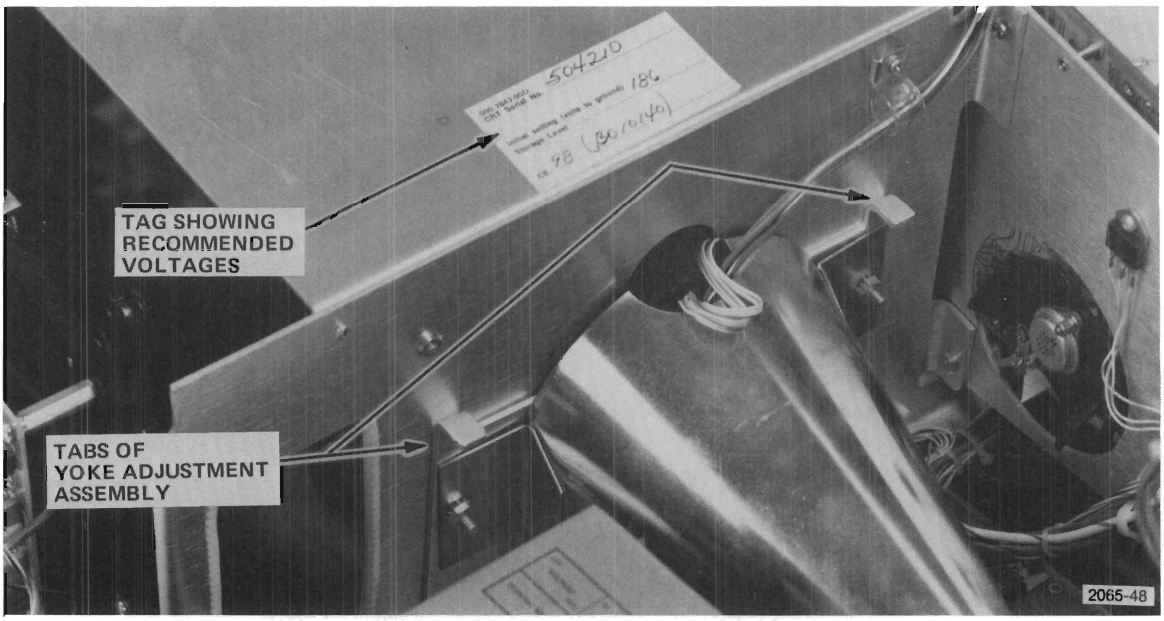


Figure 4-5. CRT Voltage Tag and Yoke Adjustments.

3. Storage Backplate Voltage

Move the voltmeter probe to J58-4 and adjust R248 for the voltage specified on the crt shield.

4. Bias Level adjustment

Turn the power off. Reconnect J50. Adjust R129 until a dot is just visible in the upper left corner of the screen just after the screen is paged. Hold down the HOME PAGE key and adjust R129 to the point where the dot just disappears.

CAUTION

A dot that is too bright may burn the crt.

5. Cursor Intensity

The location of R683, the cursor intensity adjustment, is shown in Figure 4-6. Tilt the 4052 on its side and adjust R683 until the cursor does not store. To check for storage, move the cursor across the crt with the space bar while making the adjustment.

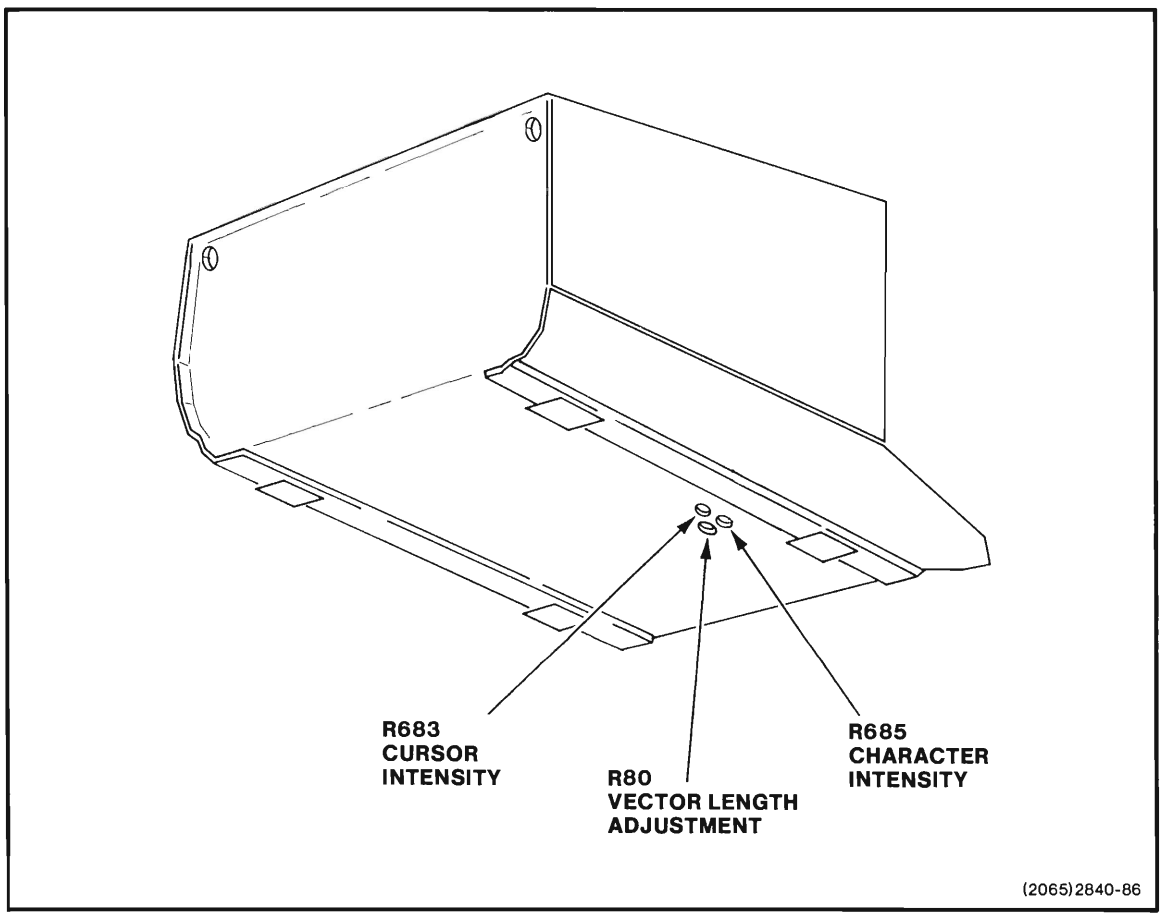


Figure 4-6. External Adjustments.

6. Focus Adjustment

Key in this program:

```
4 PRINT "8";
5 RUN
```

Now push User Definable Key #1 and you will get repeating lines of 8's. Adjust the main focus (R13) at the rear of the display board for the best focus in the center of the display. Page the display as needed. Page the screen and now adjust the Dynamic Focus (R36). This adjustment affects the difference between the center and edge focus of the display. Adjust for the best overall focus of the display. To stop the lines of 8's, push the BREAK key. To resume the program, push User Definable Key #1.

7. Character Intensity

Repeat the procedure of printing 8's as in Step 6. This time adjust the character intensity control (R865) located under the chassis just forward from the cursor intensity control. See Figure 4-6 for the location of the control. The characters should store but not fill in for a minute after storage.

8. Deflection Adjustment

Before adjusting the deflection, enter the following display alignment test pattern from the keyboard:

```
100 MOVE 0,0
110 DRAW 130,0
120 DRAW 130,100
130 DRAW 0,100
140 DRAW 0,0
150 DRAW 0,50
160 DRAW 130,50
170 MOVE 65,100
180 DRAW 65,0
190 GO TO 100
PAGE
RUN
```

You should now see a rectangle divided into four equal smaller rectangles. Now move the origin shift strap (located just to the rear of R686) to the CAL position.

9. Yoke Adjustment

If the display is tilted, the yoke must be rotated. To do this, loosen the two 11/32 in hex nuts which secure the yoke. Then rotate the yoke by means of the two tabs projecting from either side of the yoke. Rotate the yoke, while running the program just keyed, to the proper position and retighten the nuts.

10. Position and Size Adjustment

Remove the bezel and install the test graticule. While running the alignment program, adjust X position (R271), X gain (R270), Y position (R273), and Y gain (R272) to obtain a rectangle having the dimensions of 19 cm by 14 cm (7.48" by 5.5") centered on the display.

11. Geometry Adjustment

Adjust the X and Y geometry (R393 and R392) to make the lines in the test pattern straight. Readjustment of position and gain may be needed. Replace the origin shift jumper strap to the GND position if hard copy adjustments are not going to be made. Remove the test graticule and reinstall the bezel.

12. Vector Length Adjustment (4052A only)

Key in (or OLD from tape) the following program:

```
4   GOTO 100
100 PRINT "13.7 MS VECTOR TIMER ADJUSTMENT PATTERN"
110 PRINT "ADJUST FOR MINIMAL OVER AND UNDERSHOOT"
120 FOR L1  TO 50 STEP 5*0.128
130 MOVE L1,100-L
140 DRAW L1,L1
150 DRAW 130-L1,L1
160 DRAW 130-L1,100-L1
170 DRAW L1,100-L1
180 NEXT L1
190 RETURN
```

Adjust R80, Vector Length Adjustment (R80 is accessible from beneath the instrument, see Figure 4-6), so the ends of the vectors just close without any overshoot after the program has run.

HARD COPY ADJUSTMENTS

SKIP THESE ADJUSTMENTS IF NO HARD COPY UNIT IS USED WITH THIS 4052.

1. Preliminary Settings

   Connect a hard copy unit to the 4052. Remove the paper from the paper feeding mechanism in the hard copy unit if you want to save paper. Place the origin shift jumper on the Display Board to the CAL position. (Located to the rear of R686) Run the display alignment test pattern listed in the display calibration section.

2. Hard Copy Scan Adjustments

   Stop the program by pressing the BREAK key and then press the MAKE COPY key. Adjust the X HCP position (R687) and the X HCP gain to overlay the test pattern by 0.5 cm (0.2") on the left and right sides. Adjust the Y HCP (R695) and Y HCG (R691) to achieve the same 0.5 cm (0.2") overlap at the top and bottom of the display. Push the MAKE COPY key again and adjust the intensity of the scanning line to a point just below storage. The adjustment (R224) is located on the rear panel of the 4052 near the hard copy unit connector.

3. Hard Copy Threshold Adjustments

   Connect the scope probes to TP255 and TP22 (Figure 4-4). Set the vertical deflection to 0.5 V/cm. Set the sweep rate to 0.5 us/cm. Set both traces to the second horizontal graticule line from the bottom. Switch both inputs to DC. Connect an external trigger probe to the Hard Copy Interrogate signal on J52-5 or U557-9. Press PAGE and then MAKE COPY.Check for a display resembling Figure 4-7. Adjust the threshold control (R252) until the peaks almost touch, but do not overlap. Enable the paper in the hard copy unit, if it was disabled, or make sure it is ready to make copies. Place a test pattern on the screen (the focus test pattern of 8's will do) and make a copy. Final adjustment of the threshold should be made with a blank screen. Inspect a copy for noise which appears as random black spots on the copy. Slight adjustment of the threshold may be necessary to eliminate these. Turn off the power and replace the origin shifter strap to "GND".

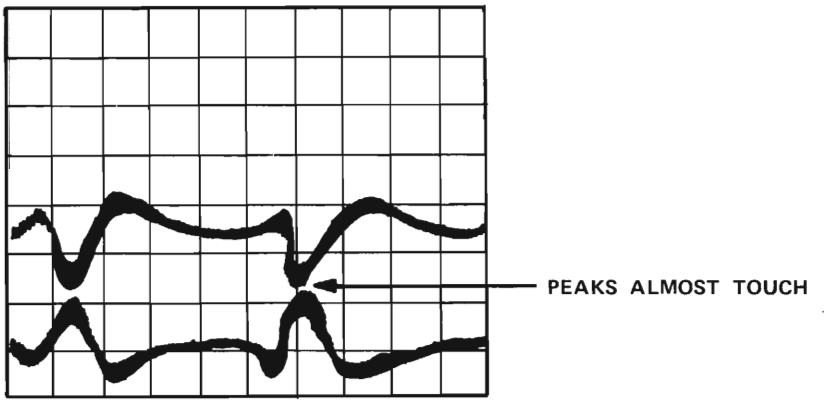


Figure 4-7. Hard Copy Threshold Adjustments with No Information Stored on the 4052 Display.

TAPE DRIVE CALIBRATION

This section of the calibration procedure describes the adjustments on the Tape Drive Board. Locations of adjustments are shown in Figure 4-8.

Be careful not to drop the head adjustment tape. Dropping it may misalign the mechanical parts and make it inaccurate. This applies to any of the tapes used with the system.

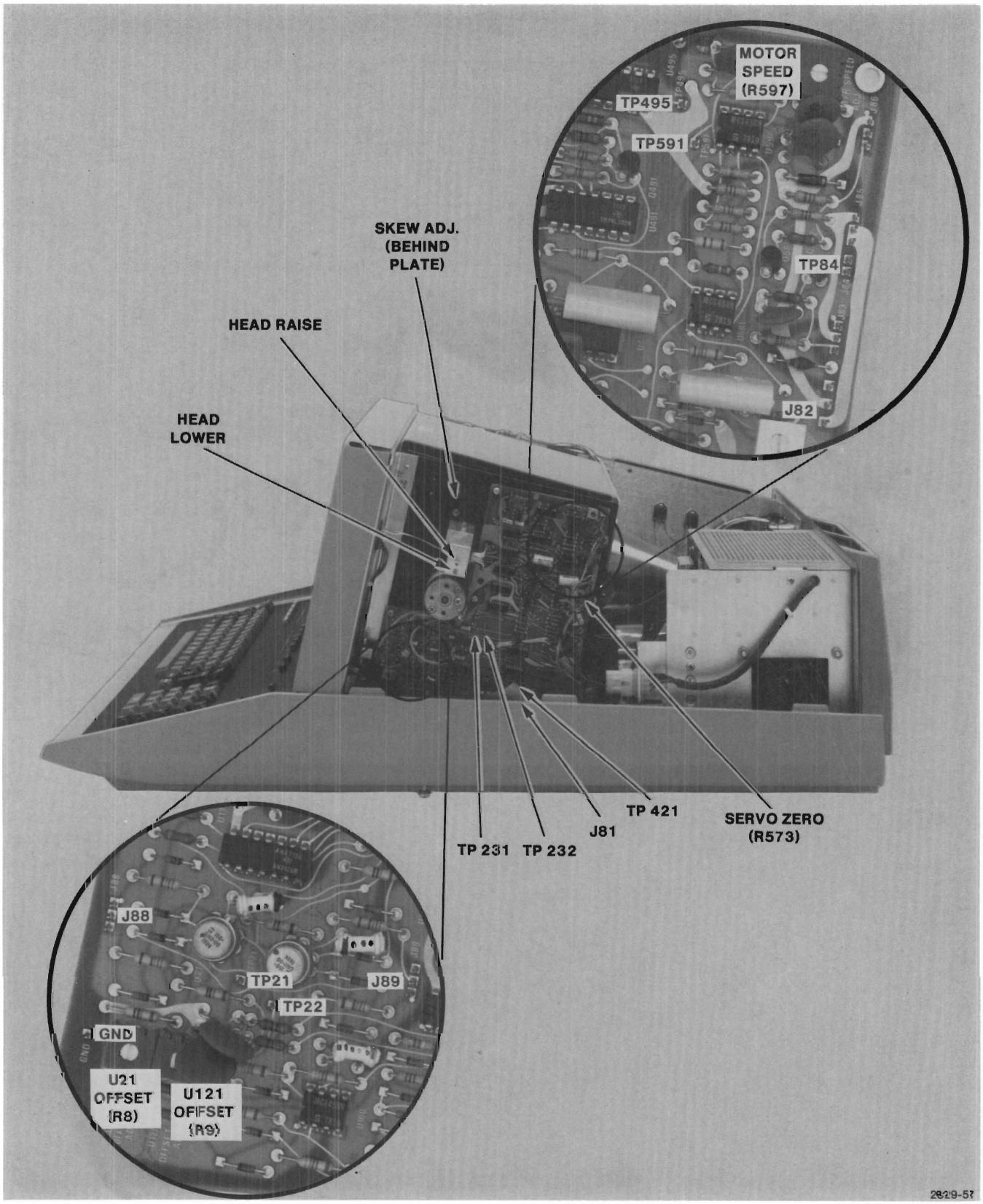


Figure 4-8. Tape Unit Checkpoints and Adjustments.

Always spool the test tape from one end to the other before making any head adjustments. Increased accuracy is also obtained by tilting the 4052 15 to 30 degrees to the right while adjusting the tape drive.

1. Amplifier DC Ajustments.

   With no tape inserted, place the voltmter probe on TP591. Adjust Servo Zero (R573) for 0 V +/- 50 mV. There should be no motor movement.

   Move the voltmeter probe to TP12. Set U21 offset adjustment (R8)for 0 V +/-50 mV.

   Move the voltmeter probe to TP22. Set U121 offset adjustment (R9) for 0 V +/-50 mV.

2. Motor Speed Adjustment

   Insert the calibration tape (067-0781-01) and press the AUTOLOAD button. The tape will move at 30 inches per second for approximately 2 minutes. A continuous 10 kHz on both channels is recorded on the last half of the tape. The first half of the tape is recorded with bursts of 10 kHz separated by erased zones. Motor speed should be adjusted during the last half of the calibration tape while the 10 kHz is continuous.

   Set the motor speed pot (R597) for 10 kHz +/- 1.0% (9.9-10.1 kHz) as measured on the frequency counter at TP231. Do not set the speed during the 10 kHz burst section of the tape. Rewinding occurs automatically when the end of the tape is reached, or can be expedited by ejecting the tape and reinserting it, then pushing the REWIND button. To start the tape forward again, push AUTOLOAD.

3. Head Skew and Height Adjustments

   Head skew should be set during the second half of the calibration tape. Procedures for replaying this continuous 10 kHz section are the same as previously described.

Connect the channel 1 probe to TP21 and the channel 2 probe to TP22. As the tape is running, set the scope for 10 usec, 2 V/cm. Trigger on the negative edge of the channel 1 waveform. Adjust skew with an Allen wrench until the waveforms are aligned as in Figure 4-9. Turn off the power and exchange connectors J88 and J89 that go to the tape head. Turn on the power and check to see if the skew pulses are still aligned. The differences in alignment between these two measurements are caused by electronically induced skew. This induced skew should not be more than one microsecond. Adjust for half of the skew difference. Move the probes to TP231 and TP232 to check that the skew at that point is less than +/-500 ns.

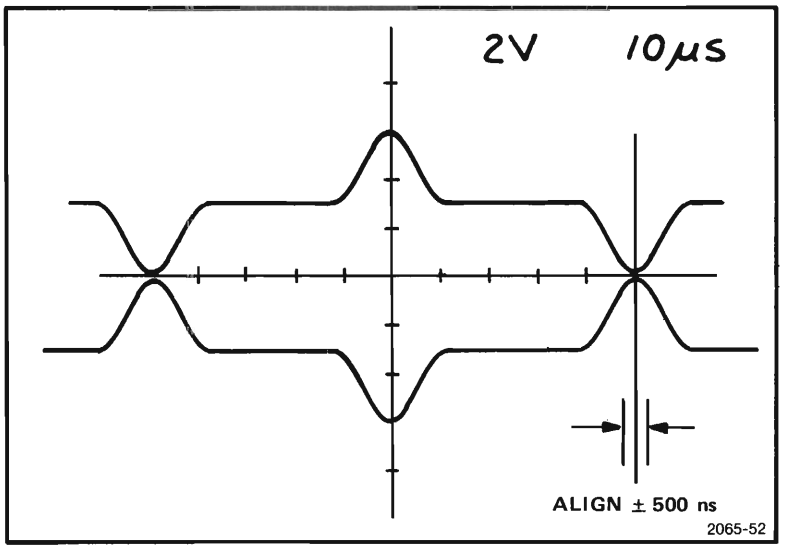


Figure 4-9. Magnetic Tape Skew Waveforms.

Turn the power off and restore J88 and J89 to their original positions. (The grey plug with the red wires goes to J88.) Skew adjustments and head height (right and left positioning) affect each other, and the adjustments may have to be rechecked.

Head height is set during the first half of the calibration tape which contains alternate zones of 10 kHz and erased tape. The head is set for minimum noise on the erased sections. This centers the head over the erased section of the tape.

Move the Channel 1 probe to TP21; remove Channel 2 probe (Figure 4-8). Set the oscilloscope to 2 V/cm, 5 ms/cm and observe the burst pattern of Figure 4-10.

Adjust the delayed sweep, if it is available on your oscilloscope, to display the low-level region between the 10 kHz bursts. (Set the delayed sweep rate to 100 us/cm and the vertical sensitivity to 100 mV/cm).

Loosen the head height raise screw about three turns (Figure 4-8). Adjust the head lower screw for minimum amplitude during the erased interval (Figure 4-10). Head skew and height adjustments interact and may have to be readjusted before both are optimized. Tighten the screws and the calibration is complete.

Routine maintenance procedures are to clean the head with isopropyl alcohol and a swab every 1000 hours of average use or every six hours of continuous tape operation.

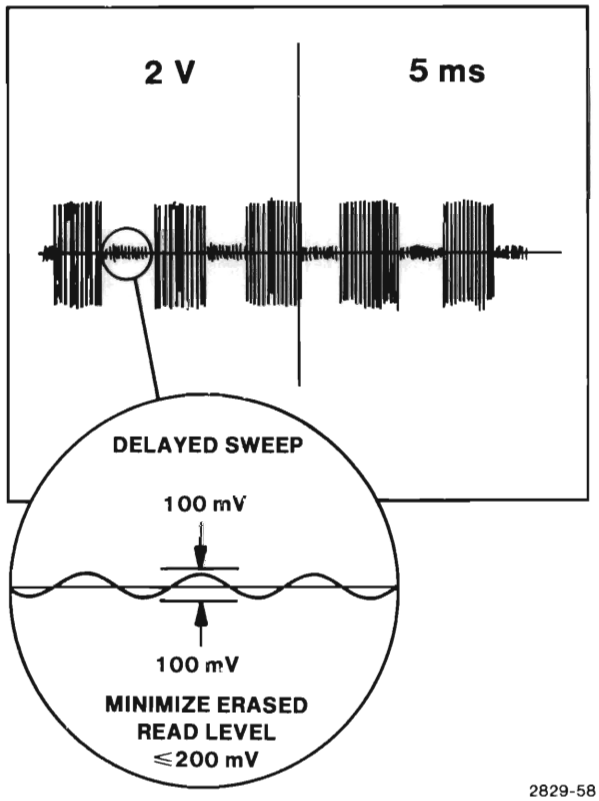


Figure 4-10. Magnetic Tape Signal for Tape Head Height Adjustments.

Section 5

4054 AND 4054A CALIBRATION PROCEDURE

GENERAL INFORMATION

This calibration procedure is for both the 4054 and the 4054A. In general most of the procedures are the same. Whenever a difference exists, it will be noted. Unless it is indicated otherwise, the terms 4054 and 4054A may be used interchangeably.

The calibration procedure for the 4054/4054A Option 31 is nearly the same as that for a standard 4054/4054A. There are no new adjustments, since the circuit boards are functionally the same. Any differences in this procedure between the standard 4054/4054A and the 4054/4054A Option 31 are specifically noted. Wherever the reference numbers to adjustments refer to different reference numbers both sets of reference numbers may be found.

This calibration procedure is intended for use by a qualified person who is familiar with both digital and analog circuitry and knows how to use the necessary test equipment.

Equipment Required

The following equipment is required for the calibration procedure. Numbers shown in parenthesis are Tektronix part numbers.

Phillips screwdrivers, #1 and #2 points
5 6" and 11 2" hex nut drivers
Small shaft (1 ") standard blade screwdriver
7 1 " insulated shaft screwdriver (003-0001-00)
3 2" and 1 6" Allen Wrench
Digital frequency counter (TEKTRONIX DC501 or equivalent)
Voltmeter (TEKTRONIX DM510 or equivalent)
High Voltage Probe for 6500V
Calibration Tape Cartridge (067-0781-01)
100MHz Dual Trace Oscilloscope (TEKTRONIX 465 or equivalent)
Cal Fixture, crt scale (067-0948-00)

LINE VOLTAGE SELECTION

The line voltage is selected by a small printed circuit board in the line selector. See Figure 5-1. The voltage that you see on the circuit card is the line voltage currently selected for the instrument.

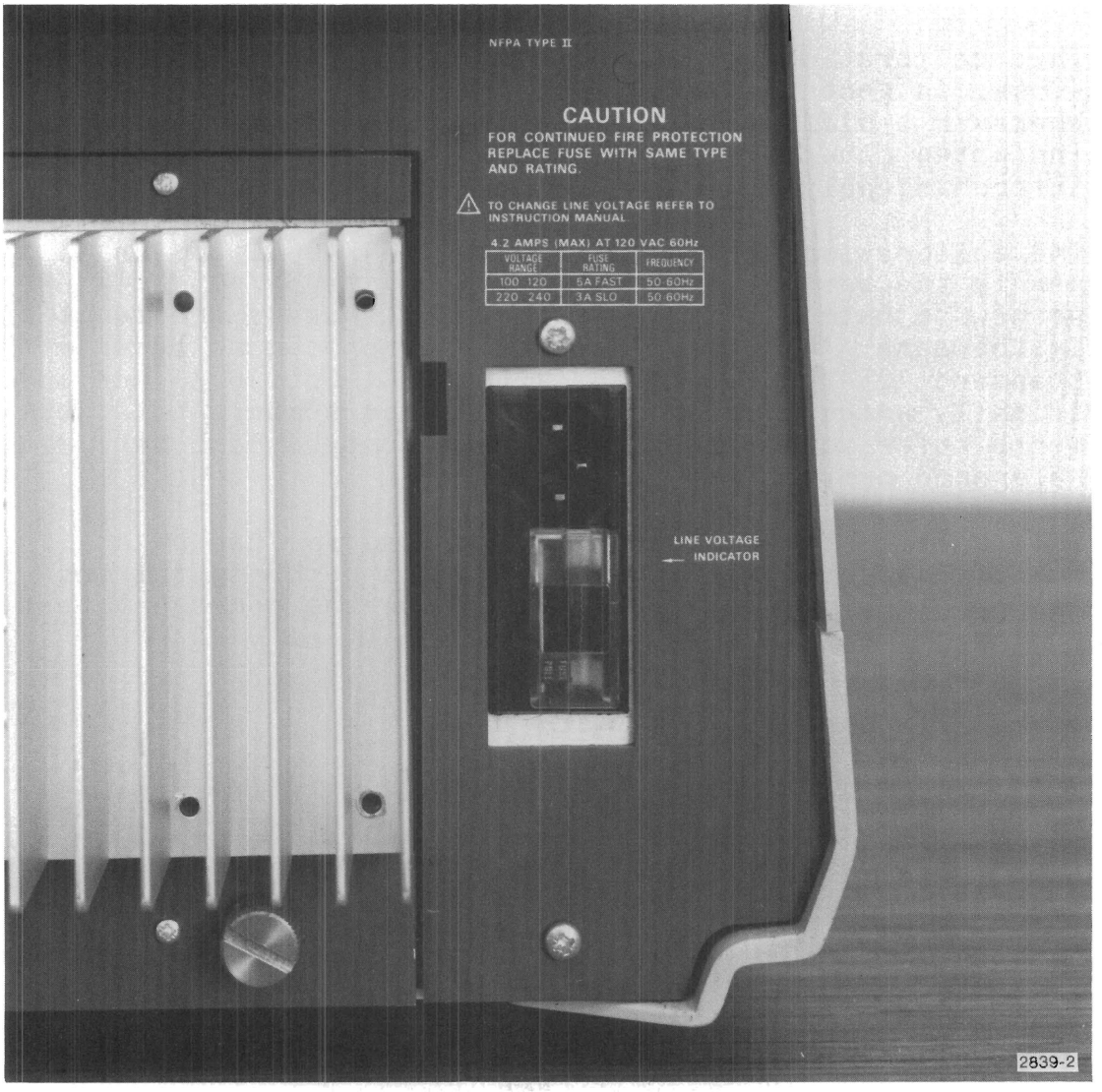


Figure 5-1. Line Voltage Selector.

WARNING

Do not try to defeat the fail-safe features of this voltage changing device. Attempting to change it may cause a fatal electrical shock.

To change the line voltage:

1. Remove the power cord.
2. Slide the plastic cover upwards.
3. Pull the fuse removal lever upwards and outwards to remove the fuse.
4. Remove the small printed circuit card with long nose pliers.
5. Reinstall the card with the desired line voltage showing in the small cut out beside the fuse.
6. Check the fuse size label above the connector and reinstall the correct size fuse for the new line voltage.
7. Slide the plastic cover down in place.
8. Reinstall the power cord.

Cabinet Removal

WARNING

Make certain that the power cord is disconnected before you remove the cover. If you don't you may touch parts of the circuitry with the cover and receive a dangerous shock. The instrument could also be damaged.

Turn off the power and refer to Figure 5-2 for the location of the screws that secure the cover. Remove the screws and lift the cover off. Be careful not to hit circuit parts while removing the cover.

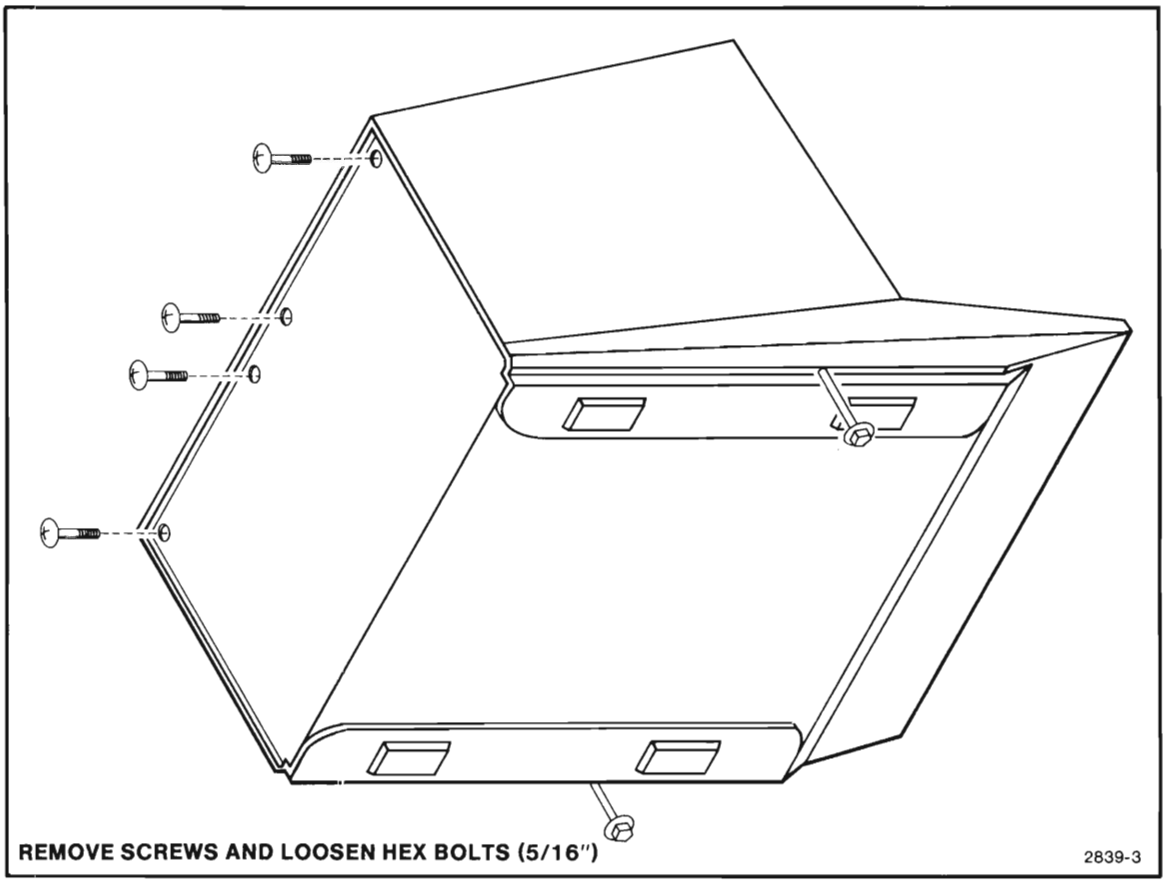


Figure 5-2. 4054 Cover Removal Procedure.

PERFORMANCE CONDITIONS

The following conditions must be met before the 4054 display characteristics and performance specifications are valid:

1. The display must be adjusted at room temperature (68 to 86 degrees Fahrenheit or 20 to 30 degrees Celsius).

2. The display must have power applied for at least 30 minutes.

Inspection Procedure

WARNING

Hazardous voltages are present in the 4054 circuitry. Only qualified service technicians should perform the following inspection procedure. BEFORE DOING THIS PROCEDURE, DISCONNECT THE POWER CORD AND WAIT 60 SECONDS; FAILURE TO DO SO MAY RESULT IN LETHAL ELECTRICAL SHOCK.

1. Check for loose, damaged, or improperly mounted hardware.
2. Make sure that circuit boards are installed in the correct slots.
3. Make sure that board level numbers are correct and that circuit modifications are installed correctly.
4. Check the crt and shield for foreign material and scratches.
5. Make sure the crt ground straps are screwed tightly to the chassis.
6. Check all wiring and harmonica connectors for proper installation.
7. Check edge connectors and Interconnect board pins for damage.
8. Check the crt filter for proper installation; make sure the ground clips are securely fastened.
9. Make sure that the crt socket is properly connected.

10. (4054 Standard Instrument) Check the strap settings on the High Voltage/Z-Axis board. Make sure both Z-Axis jumpers are set to the Z-0 position (toward U115). See Figure 5-3.

    (4054 Option 31) Check the strap settings on the High Voltage/Z-Axis board. Make sure the settings are as follows:

Jumper	**Position**
Z-Axis jumper	Z-0 position (inner position)
90/100 jumper	100 position (middle position)
75/93/50 jumper	93 position (outer position)
J611	Jumpered between pins 2 and 3
J512	Jumpered between pins 1 and 2
J511	Jumpered between pins 1 and 2

    Make sure that the board has a 1A fast blow fuse in place. See Figure 5-4.

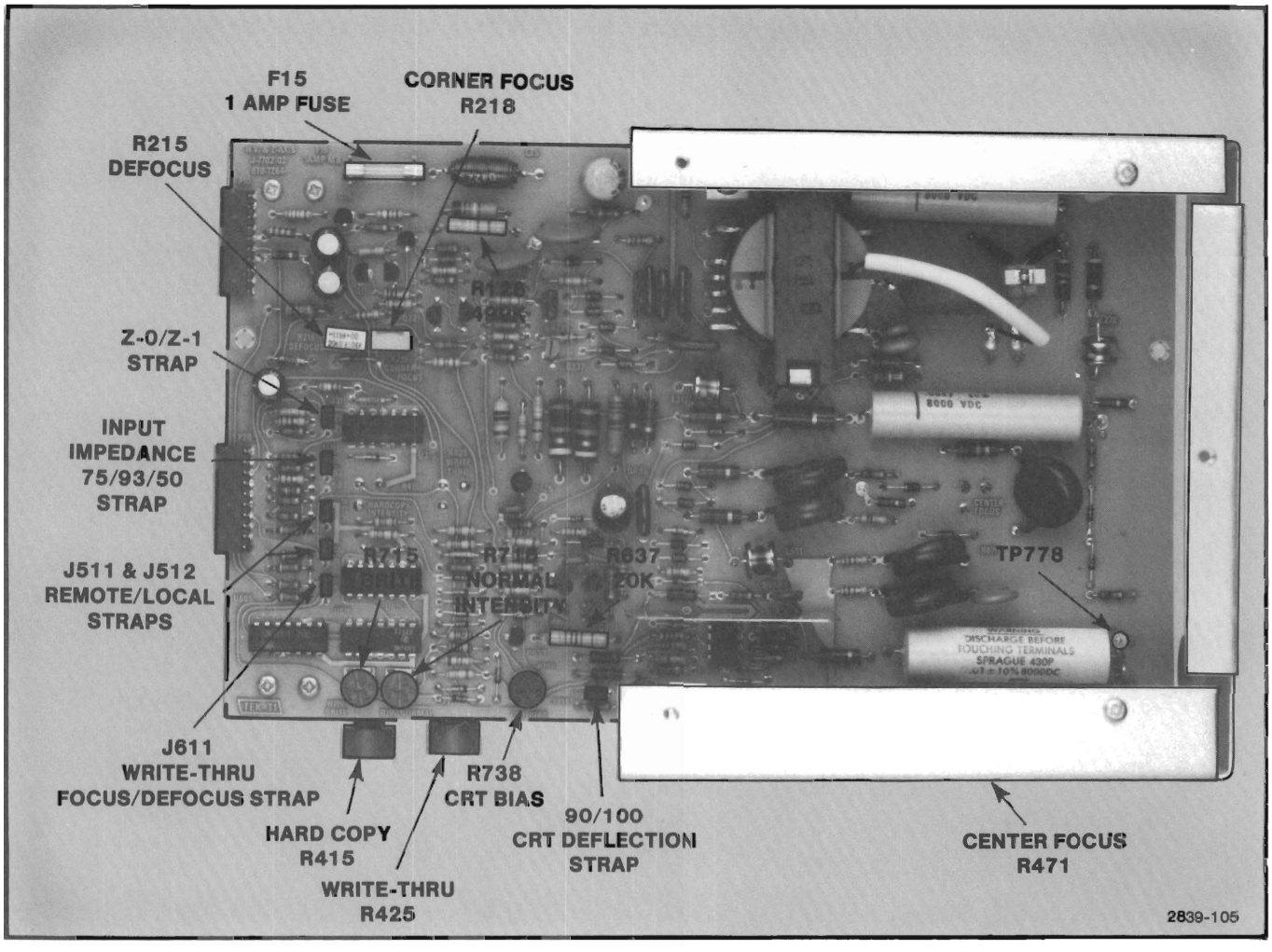


Figure 5-3. High Voltage/Z-Axis Board Strap Settings and Adjustments (Standard 4054).

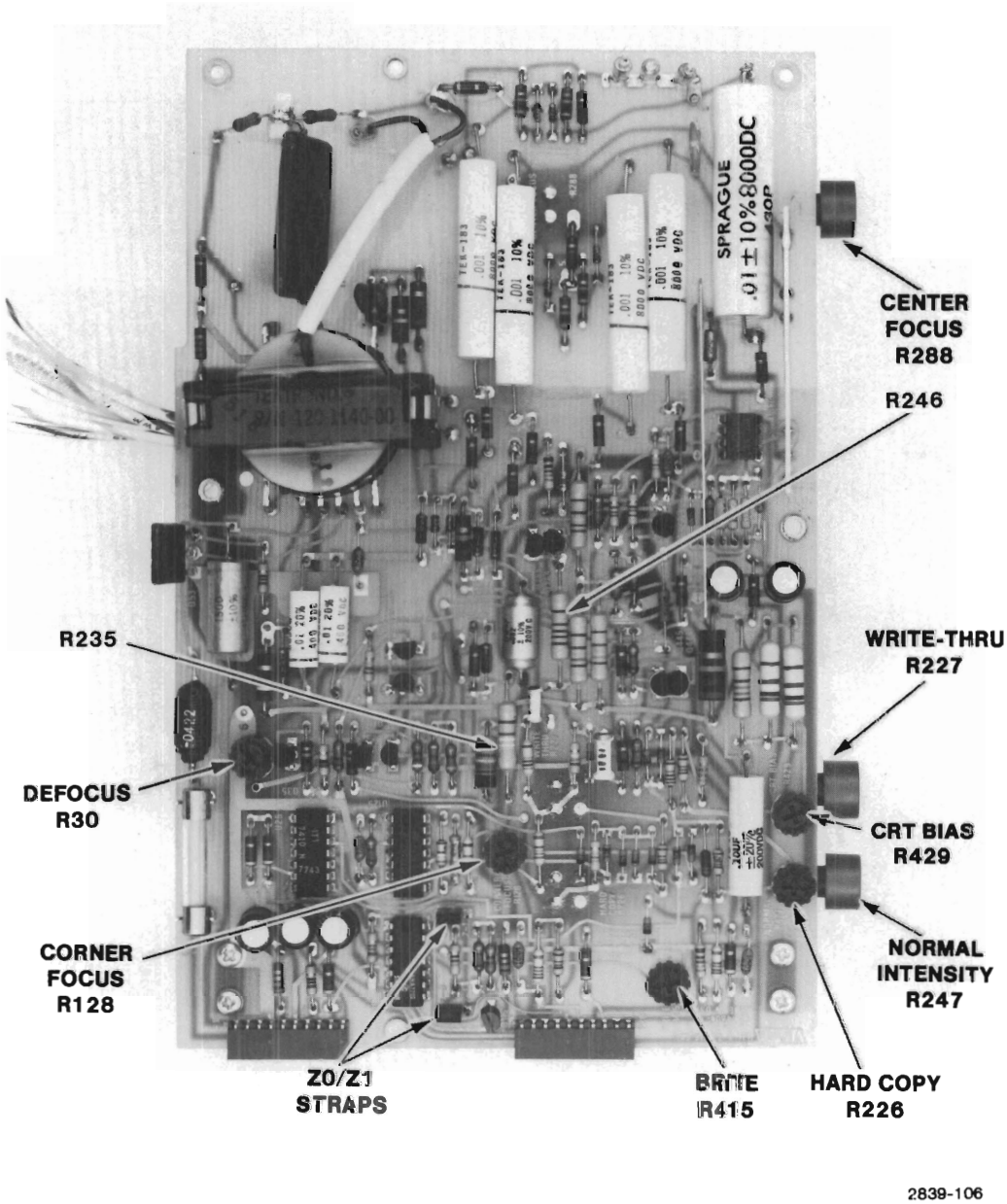


Figure 5-4. High Voltage/Z-Axis Board (4054 Option 31).

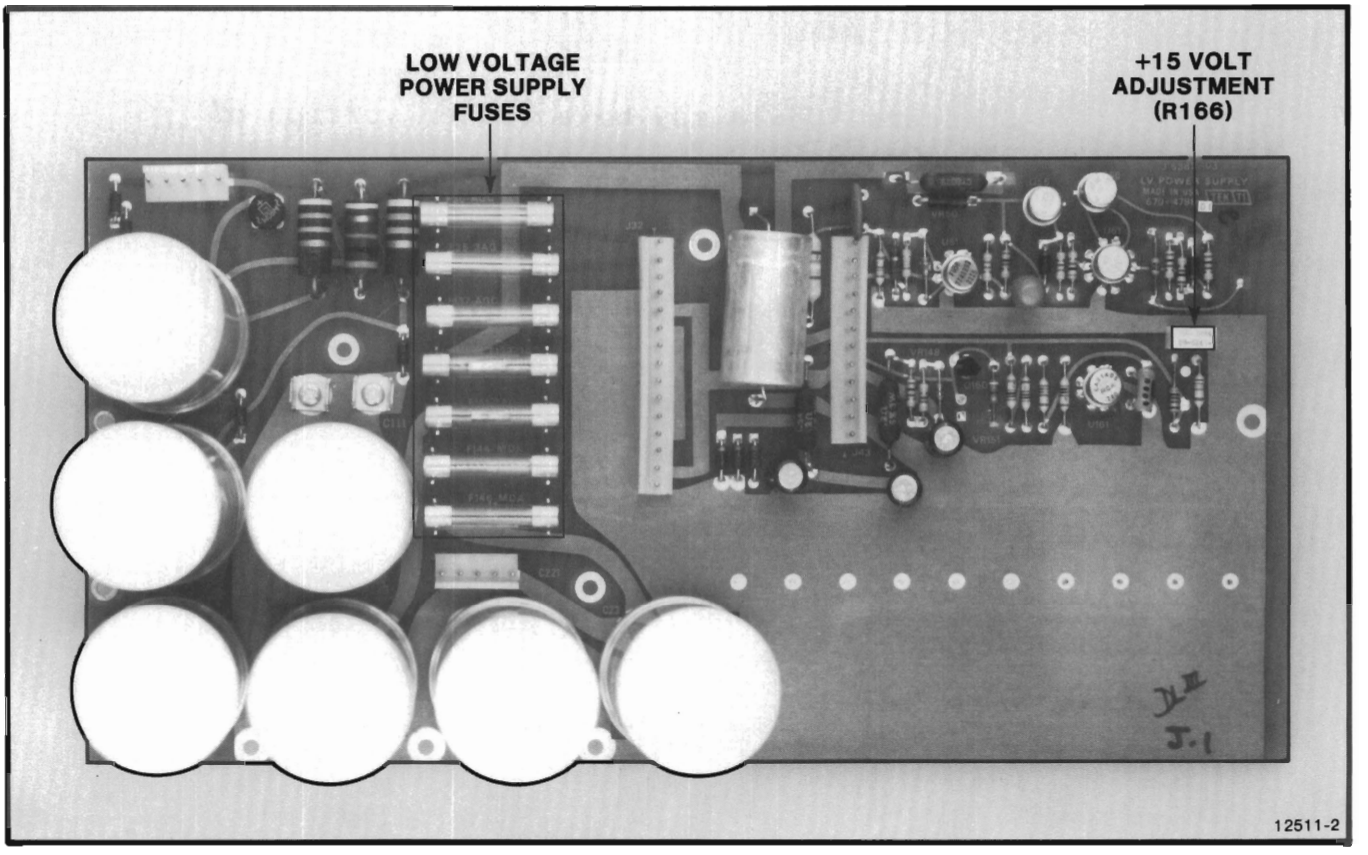


Figure 5-5. Low Voltage Power Supply Fuses and Adjustments.

11. Perform the following checks on the Low Voltage Power Supply (LVPS) board. Check the cables from the power supply to the Interconnect board for defects. Make sure that all wiring is fastened securely. Make sure that the line fuse is securely seated. Also, make sure that the following fuses have the correct ratings and are installed properly. The location of these fuses is shown in Figure 5-5. The ratings are as follows:

Standard 4054		4054 Option 31/Standard 4054	
F30	.15A fast	F30	.15A fast
F35	.25A fast	F35	.25A fast
F137	.15A fast	F137	.15A fast
F139	2.0A fast	F139	2.0A fast
F141	2.0A fast	F141	2.0A fast
F144	5.0A slow	F144	6.0A fast
F146	4.0A slow	F146	5.0A fast

NOTE

Standard 4054's may have either version of the Low Voltage Power Supply board.

12. Check the strap settings on the Storage board. Make sure that the VIEW RESET jumper is set to the GB (lower) position and also that the Z-TRU-Z jumper is set to the TRU-Z (lower) position. Set the NORMAL/TEST jumper to the "N" (top) position. Figure 5-6 shows the location of these straps.

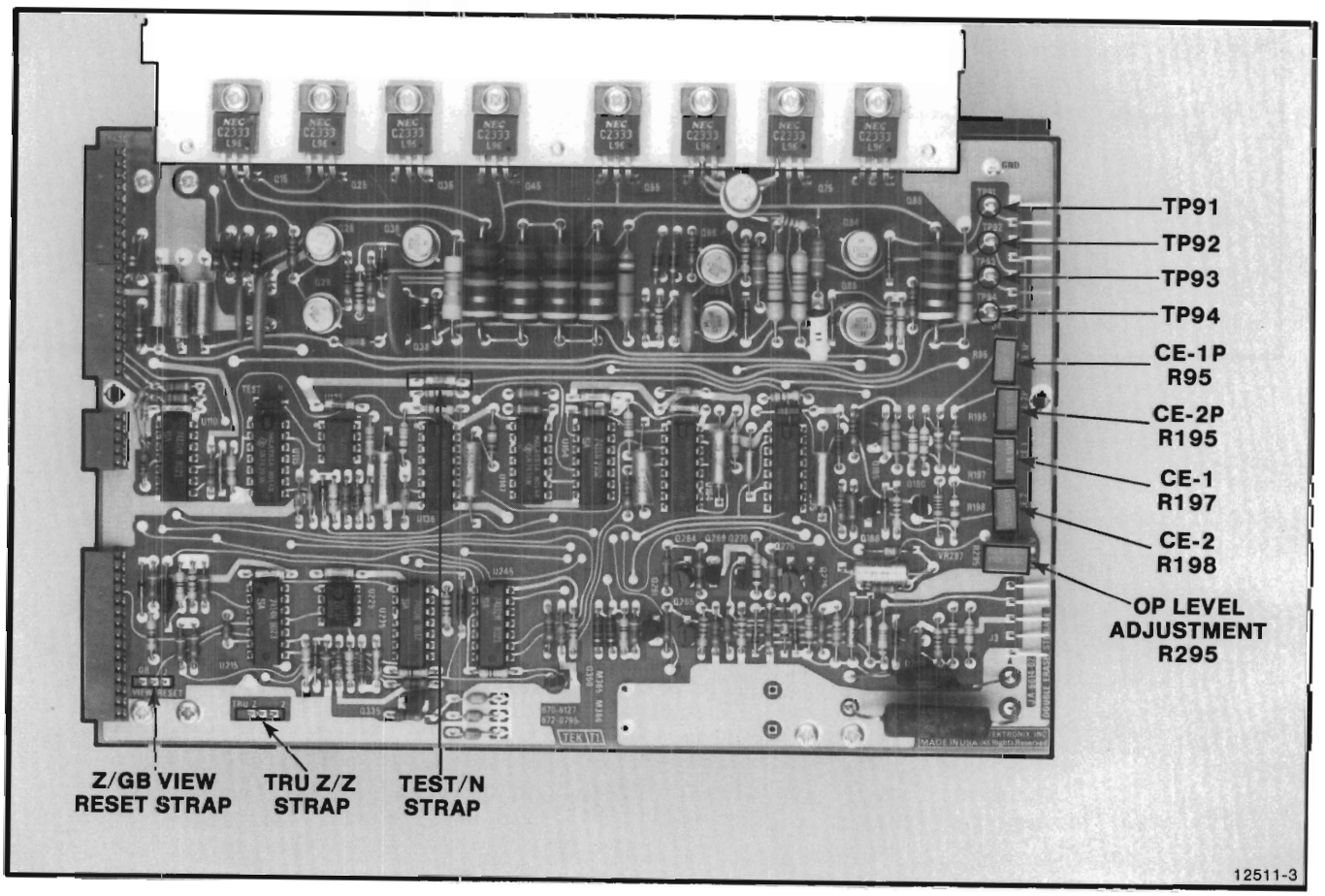


Figure 5-6. Storage Board Adjustments, Straps and Test Points.

13. Set the ANTI-BURN jumper to the IN (lower) position on the Deflection board (Figure 5-7).

14. Make sure that the harmonica plugs are correctly installed on the Hard Copy board, and that no parts are shorted together. Also, make sure that the Danger Warning is in place on the plastic shield. Check that the attaching screws are secure.

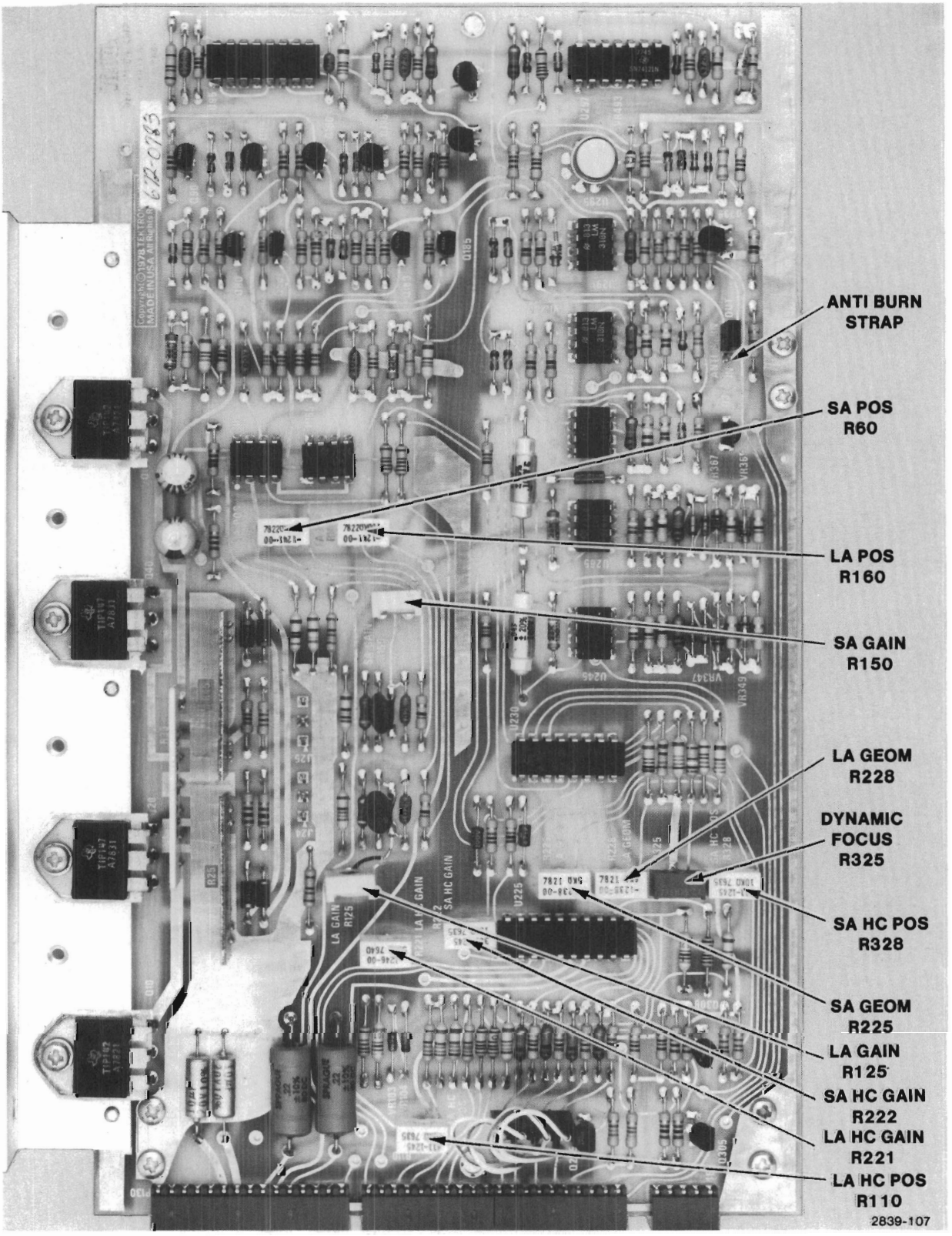


Figure 5-7. Deflection Amplifier Board Adjustment Points.

POWER SUPPLY CALIBRATION

WARNING

Use care in making these adjustments; it is possible to receive a dangerous shock from parts of the circuitry. It is also possible to damage the instrument by accidentally shorting parts of the circuitry together or to ground.

Low Voltage Power Supply

1. Connect the power cord to the ac voltage source.
2. Turn the 4054 POWER switch on.

CAUTION

Observe the crt for the first minute to insure that the beam does not remain in one spot with high intensity for more than a few seconds. This could cause a permanent deterioration of the crt phosphor in that spot. If a bright spot appears, turn off the 4054 immediately and refer to the crt bias adjustment.

3. Erase the crt by pressing the PAGE key.
4. Adjust the power supplies or check them by connecting a voltmeter between J65 (ground) and the pins on the Interconnect board called out in the following steps. The easiest place to measure some of the voltages is on the wide circuit runs directly behind J65 (Figure 5-8).
5. Adjust R166 (Figure 5-9) for a reading of 14.97 to 15.03V at J530 pin 12.

6. Check the 5V test point (Figure 5-8) for a reading of 4.85 to 5.15V at J530 pin 13.

NOTE

It is necessary to remove the front two securing bolts and fold back the hinge mounted circuit boards on the top of the instrument to adjust or check the two 12V supplies.

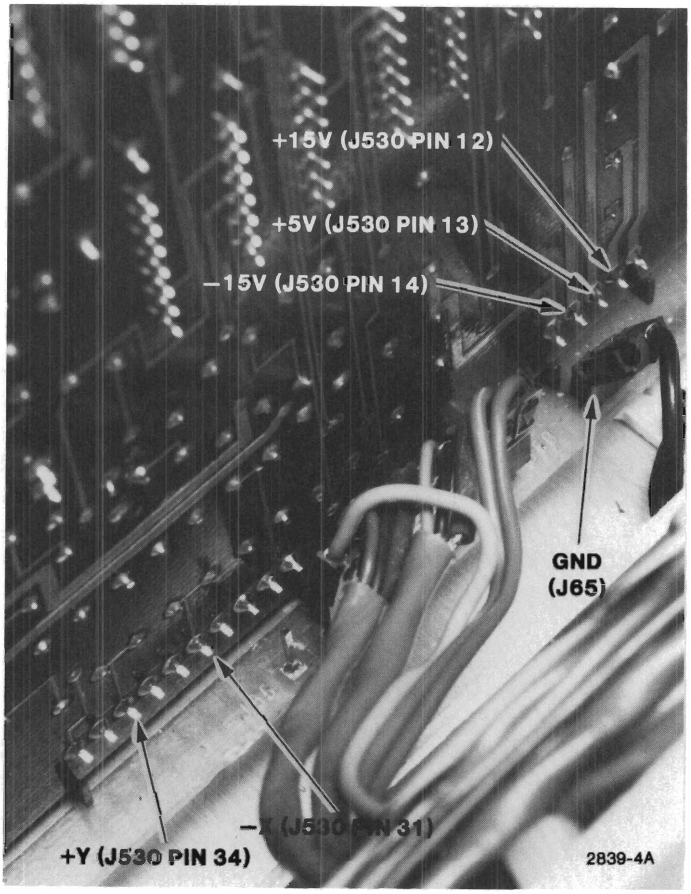


Figure 5-8. Power Supply Checkpoints.

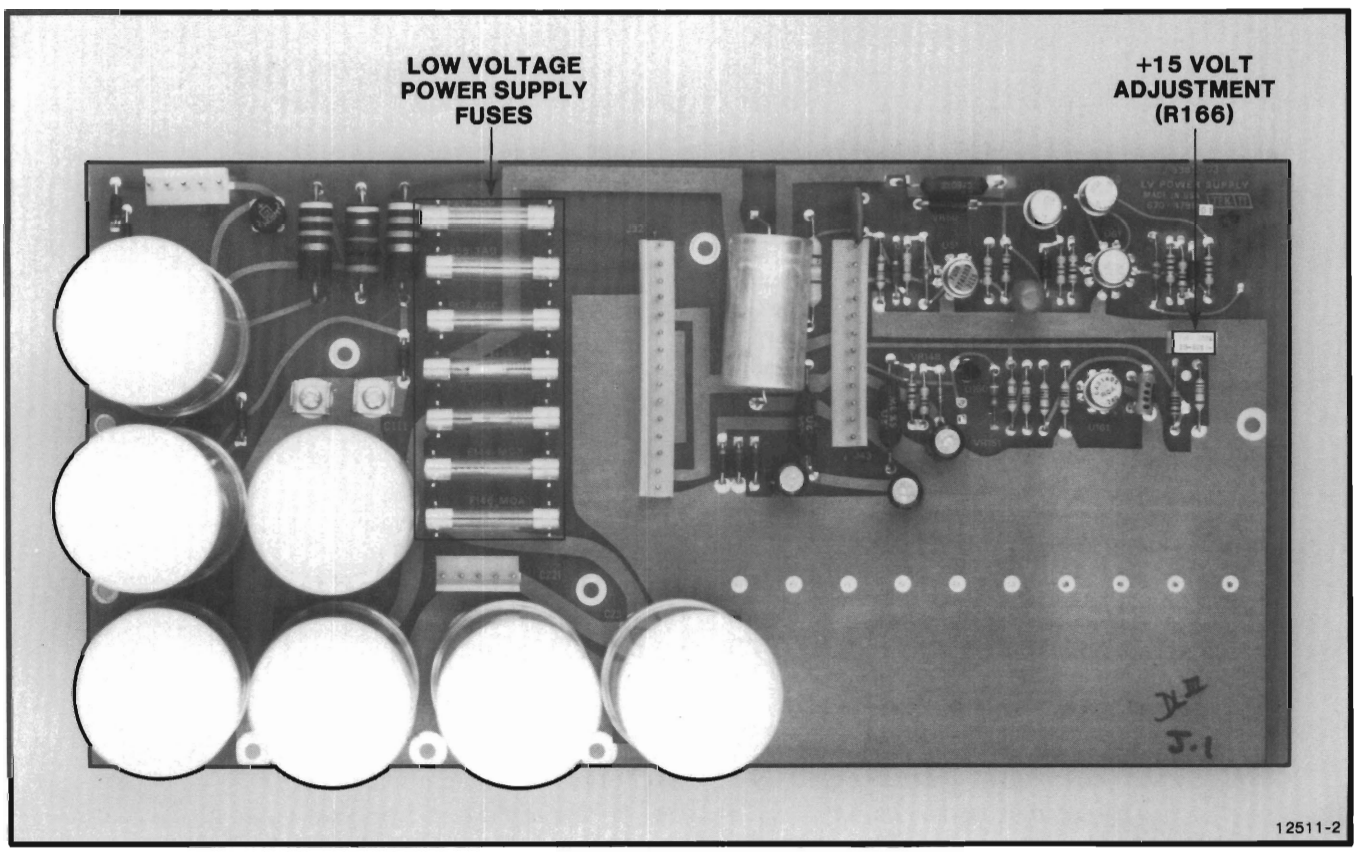


Figure 5-9. +15V Adjustment Point.

7. Check the voltages on J119 on the I/O board for the tolerances listed below. J119 is located next to the voltage adjustment potentiometer (Figure 5-10).

J119 pin	Voltage
1 & 2	+12 Vdc ±1.5% (11.82 to 12.18V)
3	-12 Vdc ±1.5% (-11.82 to -12.18V)
4	GND

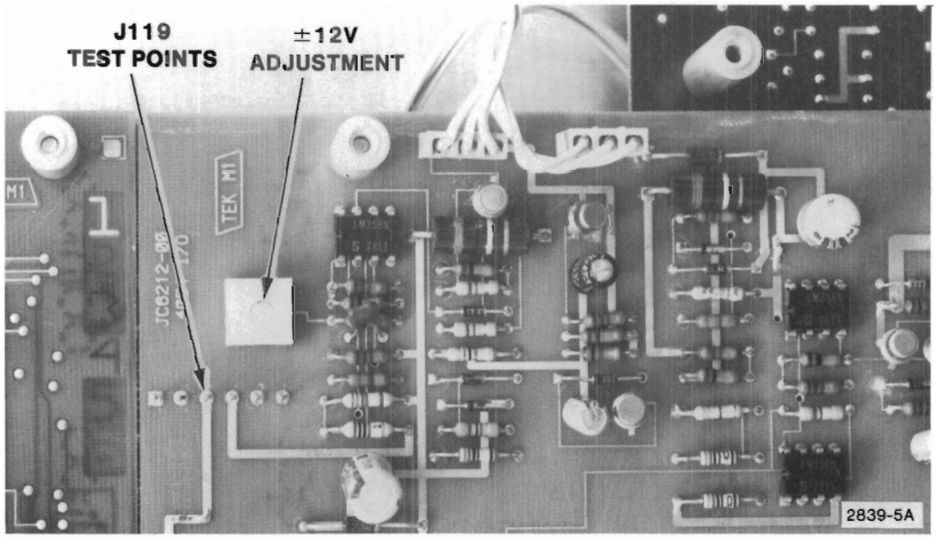


Figure 5-10. I/O Voltage Points.

8. Check the remaining voltage test points on the Interconnect board (Figure 5-11) for the following values:

Test Point	Value
J530 pin 14 (-15V reg.)	-14.85V to -15.15V
J530 pin 9 (+12V unreg.)	no tolerance (about +9V)
J530 pin 10 (-12V unreg.)	no tolerance (about -9V)
J530 pin 7 (+20V unreg.)	no tolerance
J530 pin 8 (-20V unreg.)	no tolerance
J10 pin 3 (+175V unreg.)	no tolerance
J10 pin 2 (+290V reg.)	+287.10V to +292.90V
J80 pin 1 (+490V unreg.)	no tolerance

9. Set up the oscilloscope to 0.5V/div, 10us/div, ac coupled; check to see that the following ripple voltages are within range. These are measured at the same Interconnect board test points as the dc voltages.

Test Point	Value
+15V (reg.)	5mV p-p max
-15V (reg.)	5mV p-p max
+5V (reg.)	10mV p-p max
+12V (unreg.)	1.5V p-p max
-12V (unreg.)	1.5V p-p max
+20V (unreg.)	1.2V p-p max
-20V (unreg.)	1.2V p-p max
+175V (unreg.)	7.0V p-p max
+290V (reg.)	100mV p-p max
+490V (unreg.)	5V p-p max

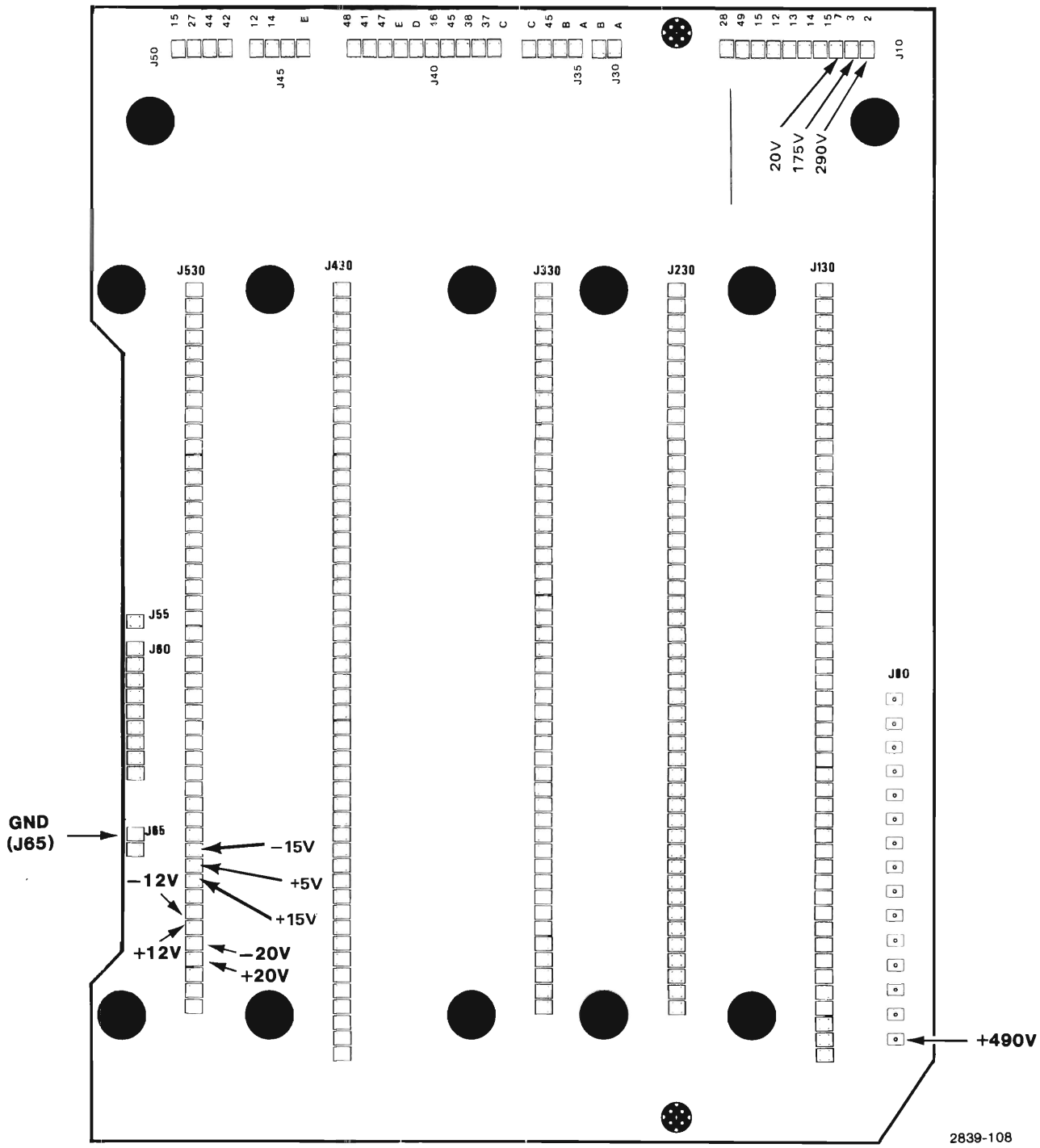


Figure 5-11. Interconnect Board.

High Voltage Check

WARNING

The following measurement involves a potentially lethal voltage. Use extreme care when making this measurement.

1. Turn the ac power source off.
2. Using a voltmeter capable of measuring 6500 Vdc, connect the positive lead of the voltmeter to ground (J65 on the Interconnect Board).
3. Connect the negative lead to the lead of C475 (standard 4054) or to TP778 (Option 31). This connection point is accessible through the top hole in the high voltage shield. See Figures 5-3 and 5-4.

NOTE

For the standard 4054, use a sharp probe tip to penetrate the insulation on the capacitor lead.

4. Turn on the instrument.
5. Check the high voltage; it must be between -5700V and -6300V or you will have difficulty in making the display adjustments.

DISPLAY CALIBRATION

NOTE

Because the High Voltage/Z-Axis board is different for the Option 31, refer to Figures 5-3 and 5-4 for potentiometer locations. The potentiometer number (R#) for the standard 4054 always appears first in the following procedure. It is followed by the number for the new High Voltage/Z-Axis board. The format is: R# standard 4054 / R# Option 31.

Storage Board Adjustments

All the test points and adjustments on the Storage board are located across the top edge of the Storage board (Figure 5-6).

1. Set the digital voltmeter to 200 Vdc range.
2. Connect the digital voltmeter probe to TP91 (the flood gun anode).
3. Check for a voltage of 142.5V to 157.5V.
4. Connect the digital voltmeter probe to TP94.

NOTE

Overhead lighting may affect how bright the crt seems to the viewer during the following adjustment.

5. Adjust R295 (the OP LEVEL adjustment at the top edge of the Storage board) so that the crt gets bright but does not store.

6. Note this voltage as the OP LEVEL voltage.

7. Remove the digital voltmeter probe from TP94 and connect it to TP93 (CE-2).

8. Adjust R198 (the CE-2 adjustment at the top edge of the Storage board) so that the flood gun pattern is within 1/4 inch from the crt target edge (edge of the phosphor).

9. Note this voltage (the CE-2 voltage); remove the probe from TP93 and attach it to TP92.

10. Adjust R197 (the CE-1 adjustment at the top edge of the Storage board) to illuminate the target background uniformly. Make sure the corners of the crt screen are at the same level of brightness as the center.

11. Check for oscillation in the background illumination. If background oscillation is present, readjust CE-1. CE-1 is typically 5 to 10V higher than CE-2. Note that there may be some interaction between R198 and R197.

12. Connect the digital voltmeter probe to TP91 (the flood gun anode).

13. Press the PAGE key. This should erase the screen.

14. Make sure that the flood gun anode voltage does not change during an erase of the screen.

Storage Board Erase Waveforms

1. Set the oscilloscope as follows:

1. V/DIV	50V/DIV
2. TIME/DIV	0.1 SEC/DIV
3. TRIGGER SOURCE	CH1 (using 10X probe)
4. TRIGGER MODE	NORMAL
5. TRIGGER LEVEL	+
6. AC/GND/DC	DC

WARNING

Always disconnect the ac power cord and wait at least 60 seconds before moving the test jumper on the Storage board or moving any jumpers on any boards. The capacitors on the Low Voltage Power Supply board discharge to a safe level in 60 seconds or more. As an added safety measure, it is a good idea to watch the +490 or the +290V supplies discharge using the DVM while the display is unplugged.

2. Turn off the 4054, disconnect the ac power cord, and wait at least 60 seconds before continuing.

3. Remove the test jumper (on the bottom of the Storage board) from the "N" position and place the jumper in the "TEST" position. The jumper may be left in the TEST position while making oscilloscope waveform checks on the Storage board but must be moved back to the "N" position when making voltage checks with the digital voltmeter. If the jumper is not used in the TEST position, the crt screen must be erased for each waveform check.

4. Reconnect the ac power cord and turn the 4054 on.

5. Note that the crt goes into Hold mode and erases every three seconds.

6. Set the oscilloscope trigger mode to "AUTO".

7. Adjust the oscilloscope vertical positioning so that ground reference is lined up with the second graticule line from the bottom of the oscilloscope screen.

8. Set the trigger mode to "NORMAL".

9. Connect the oscilloscope probe to TP94.

10. Refer to the target erase waveform (Figure 5-12) and do the following:

    a. Verify that the second positive-going ramp (c) is between 600 and 900ms long.

    b. Verify that the most negative portion of the waveform falls between 0V and +25V.

    c. Verify that the pulse height (a) is 135V to 165V above the OP LEVEL. For example, if the OP LEVEL is 150V, the pulse height must be between 285V and 315V.

11. Set the oscilloscope time/div adjustment to 20 ms/div.

12. Observe the first ramp shown as (b) in Figure 5-12.

13. Refer to Figure 5-13, which shows the first ramp of the target erase waveform in more detail.

    a. Verify that the time between pulses is 85ms to 115ms.

    b. Verify that the ramp time is a minimum of 65ms. Also make sure that the end of the ramp is not less than 80% of the OP LEVEL value. For example, if the OP LEVEL is 150V, the end of the first ramp should not fall below 120V (0.8 x 150V).

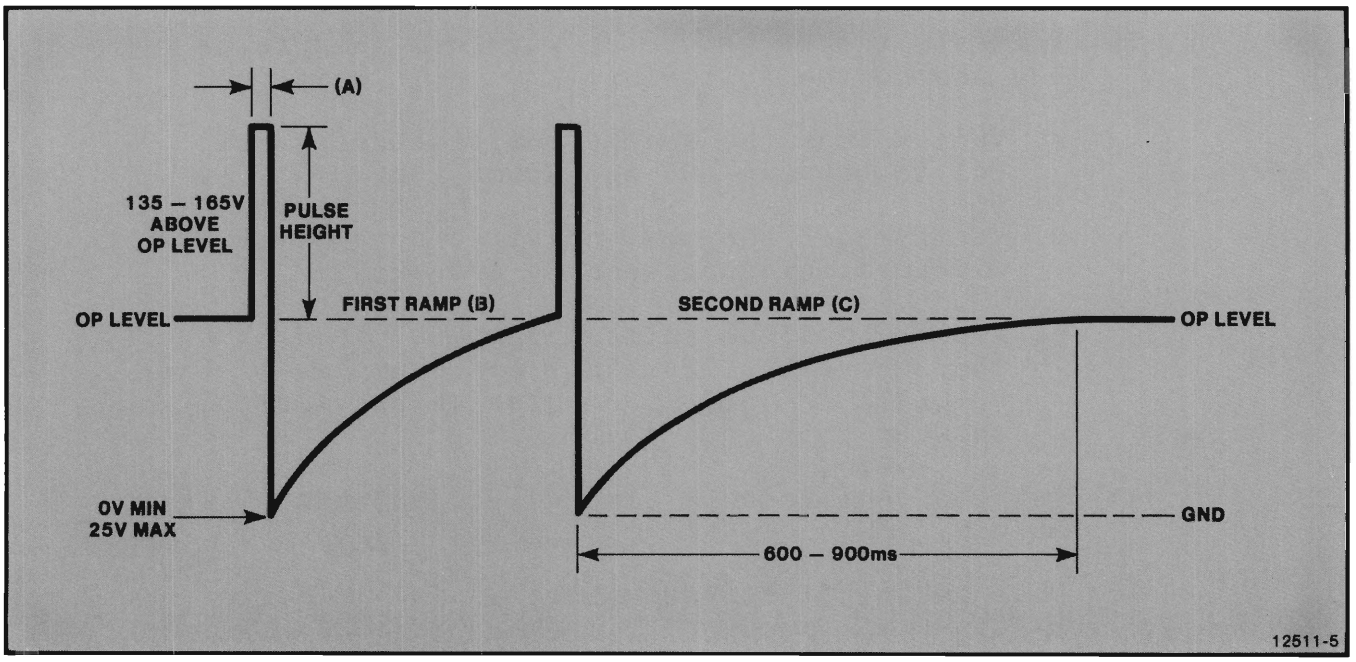


Figure 5-12. Target Erase Waveform.

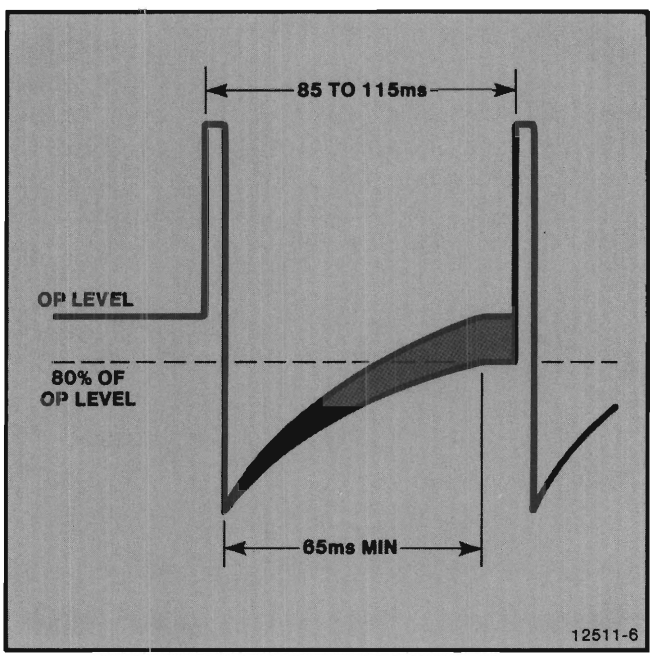


Figure 5-13. First Ramp of Target Erase Waveform.

14. Set the oscilloscope time/div adjustment to 0.5 ms/div.

15. Adjust the oscilloscope so that the OP LEVEL trace is at the center of the oscilloscope graticule.

16. Observe the pulse waveform shown in Figure 5-14. This waveform is also indicated as (a) in Figure 5-12.

17. Verify that the pulse, as measured from half way up its rising and falling edges, has from 1.7ms to 2.3ms pulse width. (This check measures both positive pulses).

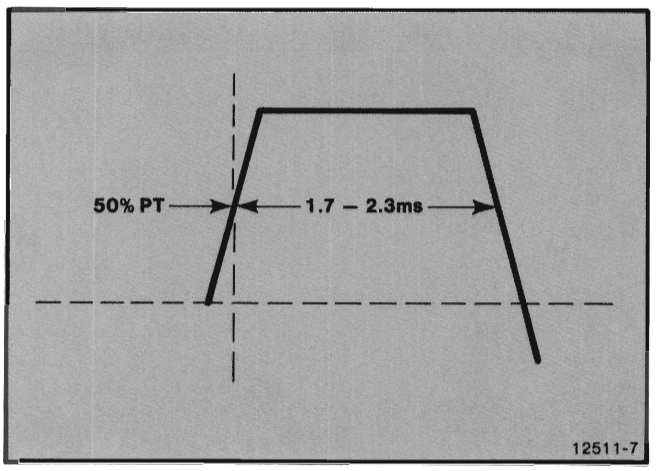


Figure 5-14. Target Erase Pulse Waveform.

18. Connect the oscilloscope probe to TP93.

19. Set the oscilloscope time/div adjustment to 50 ms/div.

20. Do the following using the waveform in Figure 5-15:

    a. Verify that the first ramp time is greater than 70ms. Also, make sure that the end of the ramp is at least 75% of the CE-2 level. For example, if the CE-2 level is 60V, the end of the first ramp should not fall below 45V (0.75 x 60V).

    b. Verify that the second ramp is 70 to 120ms long.

    c. Verify that the beginning of both ramps is between 0V and +15V.

    d. Verify that the time between pulses is 85ms to 115ms.

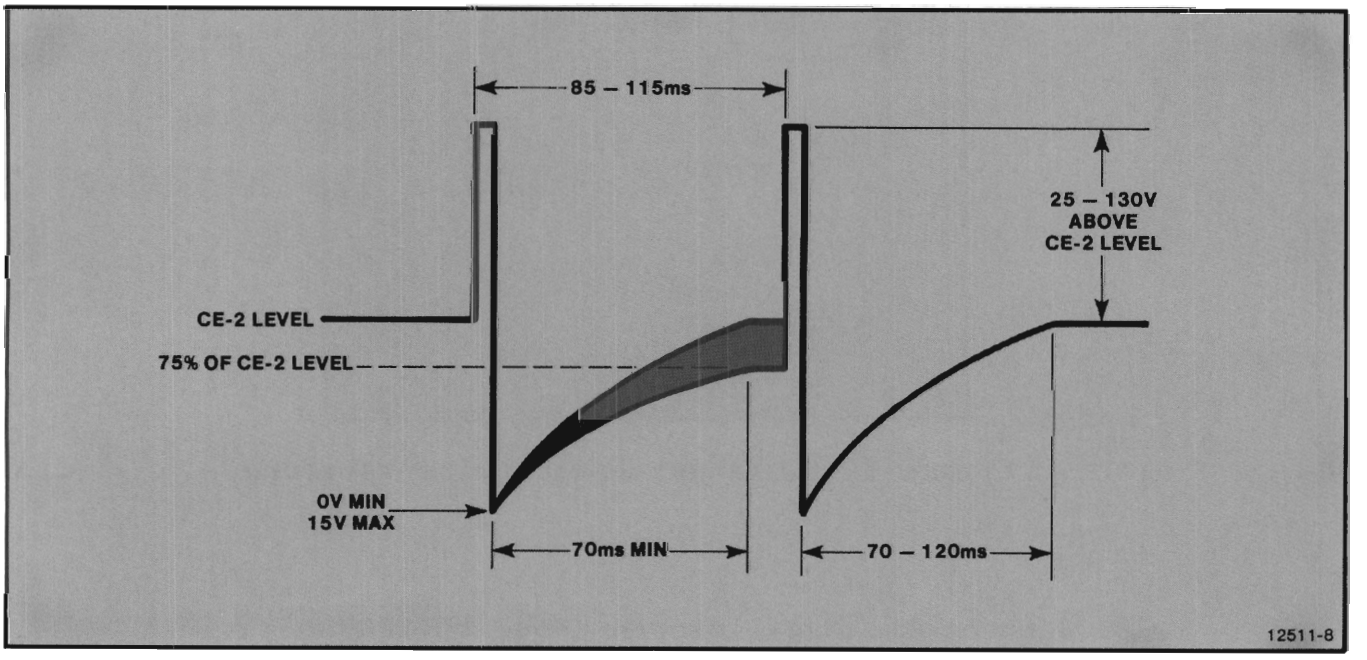


Figure 5-15. CE-2 Waveform.

21. Connect the oscilloscope probe to TP92.

22. Set the oscilloscope time/div adjustment to 20 ms/div.

23. Observe the waveform in Figure 5-16 and make sure that the time from the beginning of the first pulse to the beginning of the second pulse is 85 to 115ms.

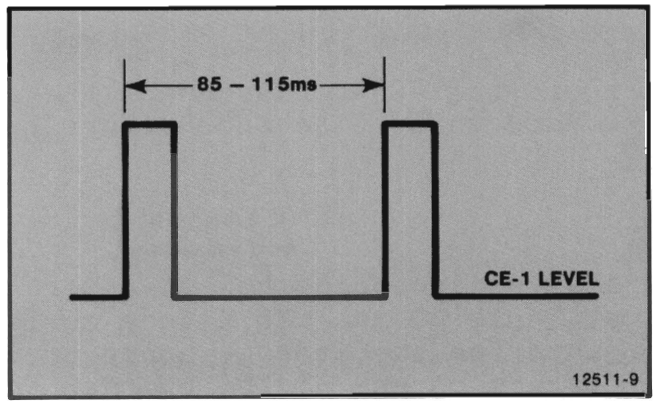


Figure 5-16. CE-1 Waveform.

24. Adjust R95 (CE-1 pulse control on the top edge of the Storage board) while erasing the crt and observe the edges of the crt for full coverage. Usually, the erase covers the full screen when R95 is turned fully clockwise or very close to fully clockwise. If no change is noticed during this adjustment, leave R95 adjusted at 90% clockwise.

25. Adjust R195 (CE-2 pulse control at the top edge of the Storage board) while erasing. At the same time, make sure that the erase extends fully to the corners of the screen.

NOTE

The OP LEVEL, CE-1, and CE-2 adjustments interact. Because of this, slight readjustment of the OP LEVEL, CE-1 level, CE-2 level, and CE-2 pulse may be required to make the crt screen look right. Readjust if necessary for proper background appearance, full screen target coverage, and full screen erasing.

26. Turn off the 4054, disconnect the ac power cord, and wait 60 seconds before continuing.

WARNING

Always disconnect the ac power cord and wait at least 60 seconds before moving the test jumper on the Storage board or moving any jumpers on any of the boards. The capacitors on the Low Voltage Power Supply board discharge to a safe level in 60 seconds or more. As an added safety measure, it is a good idea to watch the +490 or the +290V supplies discharge using the DVM while the display is unplugged.

27. Remove the test jumper from the "TEST" position and reinstall it in the "N" position.

28. Reconnect the ac power cord and apply power to the 4054.

Flood Gun Anode

1. Connect the oscilloscope probe to TP91 on the Storage board.

2. Set the oscilloscope time/div adjustment to 2 ms/div.

3. Press the PAGE key. This restarts the Hold mode timer.

4. Verify that the terminal enters Hold mode 90 to 135 seconds after pressing the PAGE key.

5. Refer to the waveform in Figure 5-17 while the crt is in Hold mode.

NOTE

Timing specifications will appear in the following format: standard 4054/4054 Option 31.

a. Verify that the positive pulse is 10 to 15% / 12 to 16% of the period of the waveform. This represents a duty cycle of 10-15% / 12-16%. It may be easier to see if the time/div. on the oscilloscope is taken out of the calibrated position and the positive and negative transitions of the waveform are aligned with the graticule of the oscilloscope. The period of the waveform, however, must have a real time of 8.3 to 12.5ms / 7 to 15ms.

b. Verify that the most negative part of the waveform is -15V.

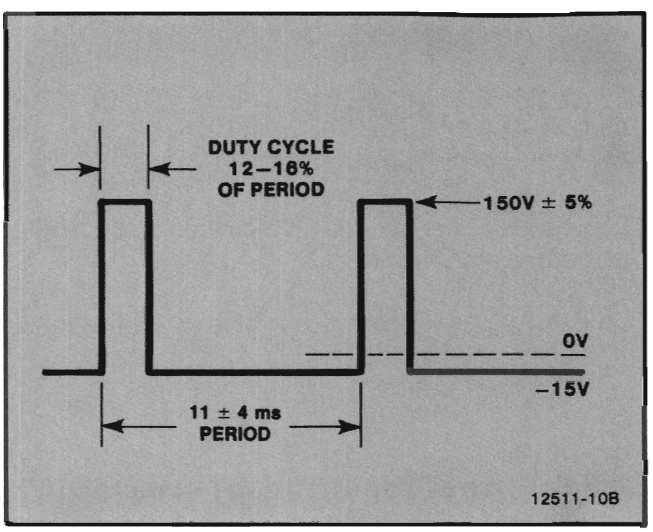


Figure 5-17. Flood Gun Anode Waveform.

6. Connect the digital voltmeter probe to Pin 43 "DBUSY" on the Interconnect board (see Figure 5-11).

7. Check for less than 0.8V (TTL low) during Hold mode.

8. Remove the oscilloscope probe from the Storage board.

Crt Bias Adjustment (R429/R738)

WARNING

Always disconnect the ac power cord and wait at least 60 seconds before moving the ANTI-BURN strap on the Deflection Amplifier board or moving any jumpers on any of the boards. The capacitors on the Low Voltage Power Supply board discharge to a safe level in 60 seconds or more. As an added safety measure, it is a good idea to watch the +490 or the +290V supplies discharge using the DVM while the display is unplugged.

1. Disconnect the ac power cord and wait 60 seconds before continuing.

2. Change the ANTIBURN strap on the Deflection Amplifier board from the "IN" position to the "OUT" position. See Figure 5-7.

3. Reconnect the ac power cord and reapply power to the 4054.

4. Use the cursor for the following adjustments.

NOTE

For the location of the following High Voltage/Z-Axis board adjustments, refer to Figures 5-3 and 5-4.

CAUTION

Do not allow a bright bias dot to burn the crt!

5. Adjust R429/R738 (the CRT BIAS adjustment in the middle right of the High Voltage/Z-Axis board) slowly clockwise until a low intensity dot appears in one corner of the cursor.

6. Readjust R429/R738 until the dot just disappears. Erase the display if the dot stores while making the CRT BIAS adjustment.

FOCUS ADJUSTMENT

Key in this program:

```
100 INIT
110 PAGE
120 DELETE L1,L2,T1,T2
130 RESTORE 140
140 DATA 0,100,0,0,16,25,0,16,25,100,32.5,100,32.5,0,48.75,0,48.75,100
150 DATA 65,100,65,0,81.25,0,81.25,100,97.5,100,97.5,5,0,113.75,0
160 DATA 113.75,100,130,100,130,0
170 DATA 0,0,0,16.67,130,16.67,130,33.33,0,33.33,0,50,130,50
180 DATA 130,66.67,0,66.67,0,83.33,130,83.33,130,100,0,100
190 DATA 0,0,130,0,130,100,0,100
200 DELETE T1
210 DIM T1(70)
220 READ T1
230 MOVE 0,100
240 PRINT @32,30:3
250 PRINT @32,20:T1
260 PRINT @32,30:1
270 PRINT @32,20:T1
280 GO TO 240
```

Run the program and a 6 by 8 grid will be displayed.

CAUTION

Do not display the 6 by 8 grid pattern for extended lengths of time; screen phosphor damage may occur.

1. Center focus

   a. Using the 6 by 8 grid pattern adjust center focus using R288/R471 on the High Voltage board for sharp center lines.

2. Corner focus

   a. Adjust R128/R218 on the High Voltage board for sharp corner lines.

3. Dynamic focus

   a. Set the scope as follows:

1. CH1	10V/DIV.
2. TIME/DIV	10ms/DIV.
3. VERT MODE	CH1
4. TRIGGER SOURCE	CH1
5. TRIGGER MODE	AUTO

   b. Put the scope probe on the upper end of R26 on the High Voltage board.

   c. Adjust the corner focus pot (R128/R218) on the High Voltage board and adjust dynamic focus R325 on the Deflection Amp. board so the voltage level at the bottom of the waveform does not change and is not clipped.

   d. Increase the sensitivity of the scope to 5V/div and the TIME/DIV to .2 sec/div.

   e. Repeat step (c) until the corner focus adjustment has no effect on the center focus portion (the bottom of the waveform) when corner focus is adjusted from one stop to the other.

4. Repeat center and corner focus procedure, trying to make all the lines equally sharp and thin as possible.

Normal Intensity (R427/R716)

Connect a 10X probe to the upper end of R246/R637 on the High Voltage/Z-Axis board (see Figure 5-3 and 5-4). Run the program for dynamic focus and adjust the pulse at this point to an amplitude of 60V with the normal intensity control.

Brite Intensity (R415/R715)

Adjust the pulse that appears at the upper end of R246/R637 to 10V higher than the Normal Intensity setting. Press BREAK to stop the program.

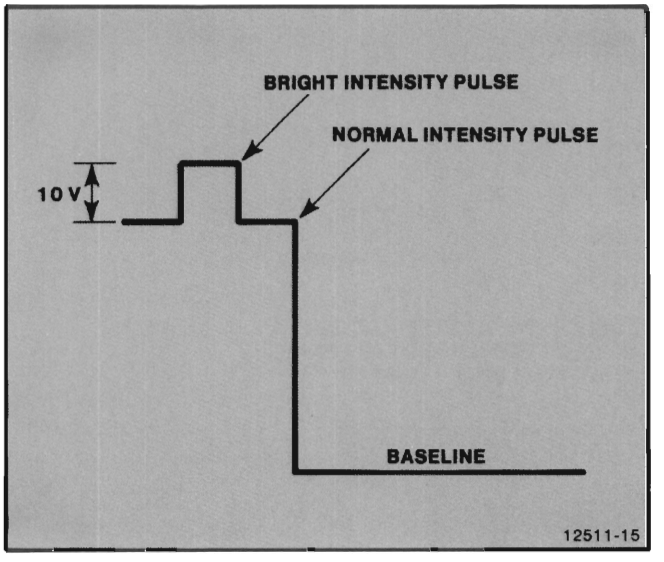


Figure 5-18. Brite Intensity Pulse.

DEFOCUS AND WRITE THRU INTENSITY

Key this program into the 4054:

```
4 F5=1
5 F6=0
6 GO TO 100
8 F5=0
9 F6=1
10 GO TO 100
100 PAGE
110 RINIT
120 IF F6=0 THEN 310
130 PRINT @32,30:0
140 T2=55
150 T3=44
160 PRINT @32,21:T2,T3
170 PRINT @32,3:1
180 PRINT @32,1:1,0
190 FOR L1=0 TO 294*0.032 STEP 4*0.032
200 PRINT @32,21:T2,T3+L1
210 PRINT @32,20:T2+294*0.032,T3+L1
220 NEXT L1
230 PRINT @32,21:T2+12,T3
240 FOR L1=0 TO 294*0.032 STEP 5*0.032
250 PRINT @32,21:T2+12,T3+L1
260 PRINT @32,20:T2+12+294*0.032,T3+L1
270 NEXT L1
280 PRINT @32,2:1
290 PRINT @32,1:1,1
300 END
310 PRINT @32,30:0
320 T1=0
330 FOR L1=70 TO 20 STEP -18*10*0.032
340 T1=NOT(T1)
350 PRINT @32,21:0,L1+2.7
360 IF T1=0 THEN 390
370 PRINT "          NO BRIDGING ALLOWED!"
380 GO TO 400
390 PRINT "            BRIDGING REQUIRED!"
400 IF T1=0 THEN 420
410 T1=2
420 FOR L2=0.32 TO 0 STEP -0.032
430 PRINT @32,21:30,L1+L2*(8+T1)
440 PRINT @32,20:100,L1+L2*(8+T1)
450 NEXT L2
460 NEXT L1
470 END
```

1. Defocus Adjustment for Standard Display:

   Push USER DEFINABLE key 1 and adjust R34 until fine lines merge, and coarse lines do not merge. Press USER DEFINABLE key 1 to repeat.

2. Defocus Adjustment for Option 31 Display:

   Push USER DEFINABLE key 2 and adjust the R215 Defocus pot until fine lines merge, and coarse lines do not merge. Press USER DEFINABLE key 2 to repeat. Adjust Write Thru intensity R425 down if pattern stores, and repeat.

3. Write Thru Intensity Adjustment:

   Break the program, press the PAGE key and key in the following:

   ```
   POINTER X,Y,Z$
   ```

   Adjust Write Thru adjustment just below keyboard (next to power switch) to mid-range. Adjust Write Thru Intensity adjustment pot (R227/R425) for maximum write thru intensity without storing. You may have to adjust the thumbwheels to position the cursor on the screen.

Origin Shift Check

Press the PAGE key repeatedly and note the cursor moves in eight small steps. The cursor moves back to the original starting point once in every eight pages of the screen.

Vector Generator Adjustments

Key this program into the 4054:

```
4 GO TO 100
100 INIT
110 MOVE 0,100
120 DRAW 130,100
130 DRAW 130,0
140 DRAW 0,0
150 DRAW 0,100
160 DRAW 0,50
170 DRAW 130,50
180 DRAW 130,0
190 DRAW 65,0
200 DRAW 65,100
210 GO TO 100
```

Press USER DEFINABLE Key 1. A rectangle with lines crossing in the center will appear.

(4054 Only) Connect a 10X probe to Pin 31 of J530 (-X as shown on Figure 5-8) on the back side of the Display Controller Board. The vertical deflection signal that appears here should have an amplitude of 10V p-p with the horizontal line in the center of the waveform at 0Vdc. R421 on the Vector Generator Board sets the waveform amplitude, and R321 sets the center dc level.

Move the 10X probe to Pin 34 of J530 (+Y) on the back side of the Display Controller Board. The horizontal deflection signal seen here should have an amplitude of 7.5V p-p. The horizontal line in the center of the waveform should be at 0Vdc. R621 on the Vector Generator Board sets the waveform amplitude, and R715 sets the dc level.

(4054A Only) Only the Y axis is adjustable on the 4054A. Connect a 10X probe to Pin 34 of J530 on the back side of the Display Controller Board. Adjust R727 so that the horizontal line in the center of the waveform is at 0Vdc.

Deflection Amplifier Adjustments (Figure 5-7)

Install the calibration graticule. The Bezel will have to be removed to install the graticule.

WARNING

Use the insulated screwdriver for making these adjustments. If you accidentally drop an uninsulated srewdriver on the Interconnect board, you can cause damage to the instrument.

Adjust LA POS (R160) and SA POS (R60) to align the center of the displayed pattern to the center of the graticule. It may be necessary to loosen the yoke clamp and rotate it to align the center vertical and horizontal lines with the graticule.

Adjust the LA GEOM (R228) and SA GEOM (R225) LA GAIN (R125) and SA GAIN (R150) to get the pattern to align with the test graticule. These adjustments interact and may have to be adjusted several times.

Vector Start and Stop Adjustments (R455 & R355)

These two adjustments are at the top edge of the display controller board. Position the cursor to near the center of the screen. Adjust these two controls to close the corners of the cursor box, but not to overlap. Overlap makes bright dots at the cursor corners. If a bright dot appears beneath the cursor, readjust the CRT bias until it just disappears.

Dropout

Key in this program:

```
4 PRINT "8";
5 RUN
```

NOTE

This will be referred to as the hard copy pattern.

1. Display the hard copy pattern using the program above; wait 2 1/2 minutes. This allows the display to drop into Hold Mode.

2. Bring the display out of Hold Mode by pressing the SHIFT key.

3. Increase the OP LEVEL adjustment or the Normal Intensity adjustment or both in 5V increments if breaks occur in the hard copy pattern. Page the screen to repeat the hard copy pattern for the best picture with a minimum number of breaks. An example of drop out is shown in Figure 5-19.

4. Check Focus again if Normal Intensity adjustments are made.

5. Check the CE-1, CE-2, display gain, and positioning adjustments if OP LEVEL adjustments are made.

CAUTION

Do not allow more than 70V p-p for Normal Intensity. Brite Intensity is always set at 10V above Normal Intensity.

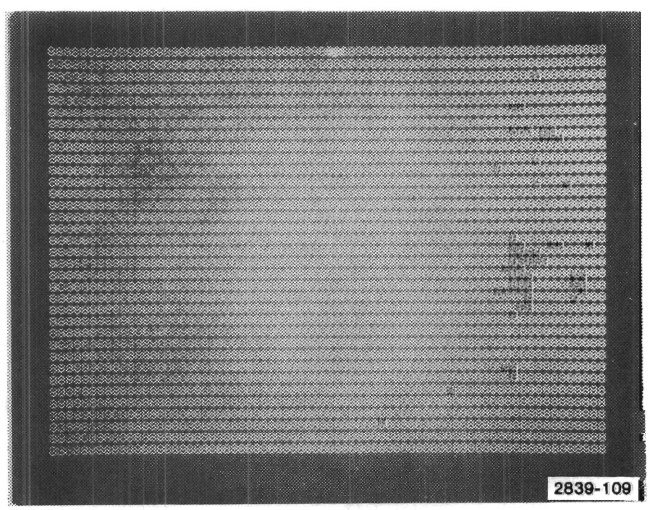


Figure 5-19. Display Conditions.

6. Set scope as follows:

   1. CH1 20V/DIV
   2. TIME/DIV 10ms/DIV
   3. VERT MODE CH1
   4. TRIGGER SOURCE CH1
   5. TRIGGER MODE AUTO

7. When the display goes into Hold mode, put the scope probe on J4 pin 6 and verify the view hold waveform for a period of 8.3ms to 12.5ms / 7ms to 15ms.

8. Decrease the TIME/DIV to 50us/div and check for a 12 to 16% pulse duty cycle.

9. Press SHIFT key to return display back to View Mode. Check and verify that there is no drop out, fade out or flood up.

HARD COPY ADJUSTMENTS

(This section of the adjustment procedure is not necessary if no hard copy unit is used.)

Hard Copy Intensity

Connect a hard copy unit to J41 (on back of 4054) and allow the unit to warm up.

Display the hard copy pattern using the program above. When the screen screen is full of 8's, press the MAKE COPY key on the 4054. As the line crosses the screen, adjust the Hard Copy Intensity control for a line intensity just below the storage level. The control is located near the power switch below the keyboard. The Hard Copy Intensity control located on the High Voltage/Z-Axis board should be left at mid-range.

Hard Copy Position Controls (Figure 5-7)

Press the 4054 MAKE COPY key and adjust the LA HC POS (R110) and the SA HC POS (R328) for full display coverage by the hard copy sweep, both horizontally and vertically. These controls are on the Deflection Amplifier board. The SA HC GAIN (R222) and the LA HC GAIN (R221) may also have to be adjusted to achieve complete display coverage. It may be necessary to press MAKE COPY several times to complete the adjustments.

Hard Copy Threshold

Press the BREAK key to stop the hard copy pattern. Key in from the keyboard CHA 1 to get the smallest size letters.

Press USER DEFINABLE key 1 to fill the screen with 8's and adjust R26 (Hard Copy Amplifier board) for the best copy of the pattern. The smallest characters should be easily readable. Page the screen and make a copy with nothing stored on the screen. Look for black dots (noise) on the blank areas of the paper and adjust R26 for minimum noise with good copy.

Tape Drive Calibration

The 4054 tape drive is the same as the 4052. Refer to the tape drive section of the 4052 calibration procedure (Section 4) for instructions.

Section 6

4052/4054 GENERAL THEORY OF OPERATION

INTRODUCTION

The 4052/4054 General Theory of Operation Section covers the software explanation for the 4052/4054 Graphic Computing Systems. (For the hardware theory of operation refer to the appropriate hardware section.) Some of the subjects covered in this section are:

- 4052/4054 address allocation (RAM, ROM, PIAs, GPIB, etc.)
- User language (BASIC) storage.
- Firmware (BASIC interpreter) storage and control.
- Micro Code (hardware control) storage and control.
- Data and firmware instruction transfer.

4052/4054 ADDRESS ALLOCATION

The 4052/4054 memory space (128K bytes total) is divided into two spaces; ROM space (64K bytes) and RAM space (64K bytes).

ROM space (Figure 6-1) contains 46K bytes of firmware (BASIC intrepreter), 16K bytes in a switchable bank (ROM packs), and 2K bytes of patch ROM used for firmware fixes of the 46K ROM area and of the 8K data ROM area in RAM space.

RAM space (Figure 6-1) contains 256 bytes used for I/O addresses, 8K data ROM used for firmware constants, 32K bytes of standard RAM, and 24K bytes of optional RAM. The standard RAM area and the optional RAM area are used to store BASIC language programs during execution. Approximately 1.5K bytes of the standard RAM area is used for firmware variables, leaving 31.5K bytes or 54.5K bytes for user programs.

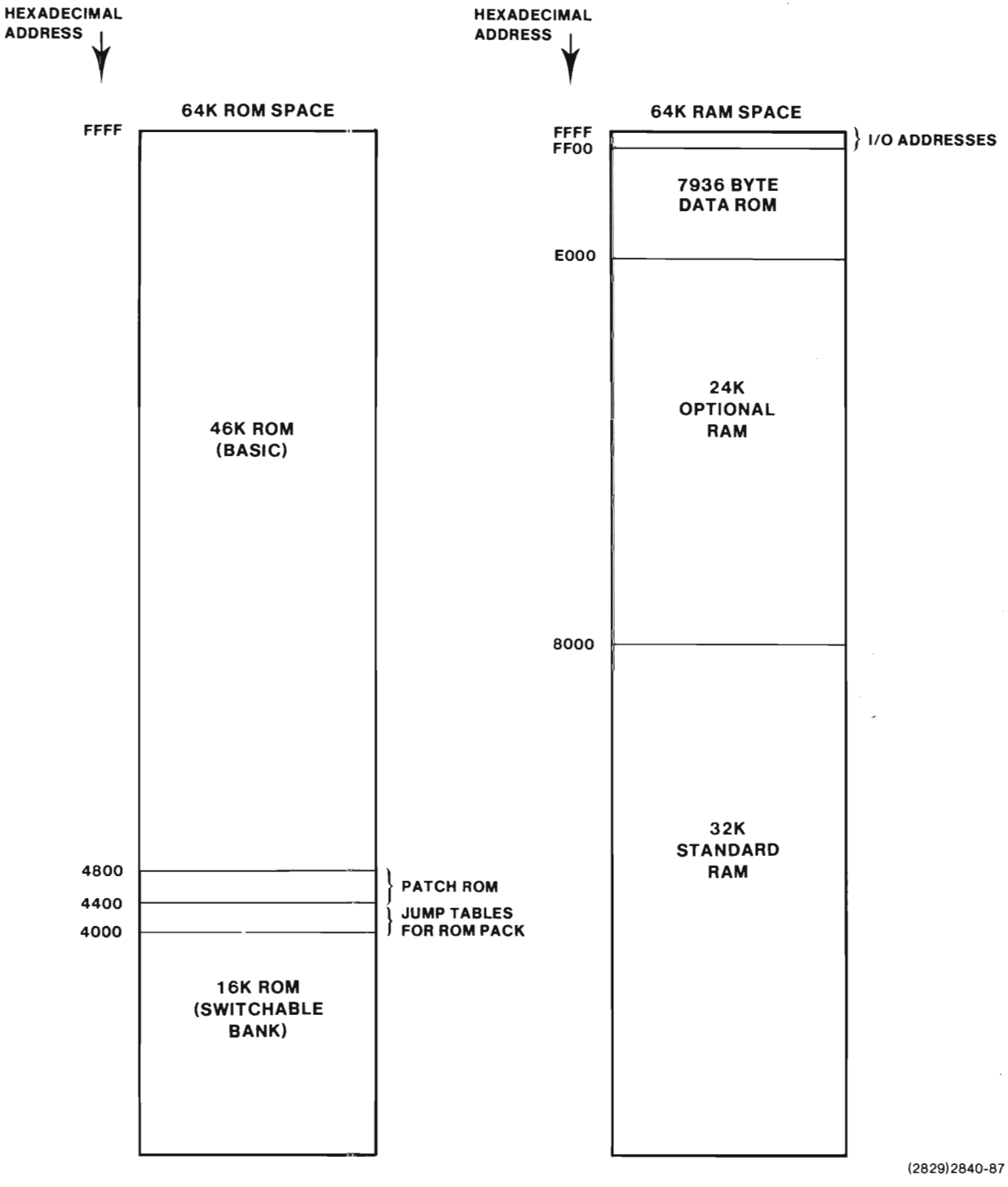


Figure 6-1. 4052/4054 Memory Address Allocation.

The 4052 I/O addressing is shown in Figure 6-2 and the 4054 I/O addressing is shown in Figure 6-3. The only difference in the 4052 and the 4054 I/O addressing is in the display area. The 4052 uses PIAs for the display data and control. The 4054 uses registers for the display data and control.

4052 I/O ADDRESS ALLOCATION MAP

I/O SECTION	SCHEMATIC PAGE	ADDRESS HEX
GPIB	5-5	FF00-FF05
Y AXIS PIA/MAG TAPE DATA	5-3	FF0C-FF0F
X AXIS PIA	5-3	FF14-FF17
MAG TAPE PIA	5-2	FF18-FF1B
KEYBOARD PIA	5-6	FF28-FF2B
COMMUNICATIONS PIA	12-1 OR 13-2	FF40-FF43
COMMUNICATIONS ACIA	12-1 OR 13-2	FF44-FF45

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Figure 6-2. 4052 I/O Address Allocation Map.

I/O SECTION	SCHEMATIC PAGE	ADDRESS HEX
GPIB	p. 5-4	FF00-FF05
DISPLAY CONTROL REGISTER	p. 5-3	FF08
DATA TO DISPLAY VECTOR GENERATOR	p. 5-3	FF09-FF0A
MAG TAPE DATA	p. 5-2	FF0C-FF0F
DISPLAY STATUS REGISTER	p. 5-2	FF10
DATA FROM DISPLAY VECTOR GENERATOR	p. 5-3	FF11-FF12
MAG TAPE PIA	p. 5-2	FF18-FF1B
KEYBOARD PIA	p. 5-3	FF28-FF2B
COMMUNICATIONS PIA	p. 5-2	FF40-FF43
COMMUNICATIONS ACIA	p. 5-1	FF44-FF45

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Figure 6-3. 4054 I/O Address Allocation Map.

4052/4054 USER (BASIC) PROGRAMMING

A user program is placed into the RAM area of memory from the keyboard or a storage device (previously written programs). The program is stored on and retrieved from the internal tape drive, an external device on the GPIB (General Purpose Interface Bus) or a host by using a Communications option (four-slot or two-slot backpack). The firmware interprets the user programs (executes BASIC language statements).

4052/4054 FIRMWARE

The same firmware is used in both the 4052 and the 4054 to interpret user programs, to transfer data, and to control the I/O devices (internal tape drive, display, keyboard, and GPIB). The firmware is located in ROM space and the Data ROM (system constants) in RAM space.

A firmware instruction is one, two, or three bytes in length. The first byte of each firmware instruction is the operation code (opcode). The second byte or the second and third bytes are the operand (data) or address of the operand (Figure 6-5).

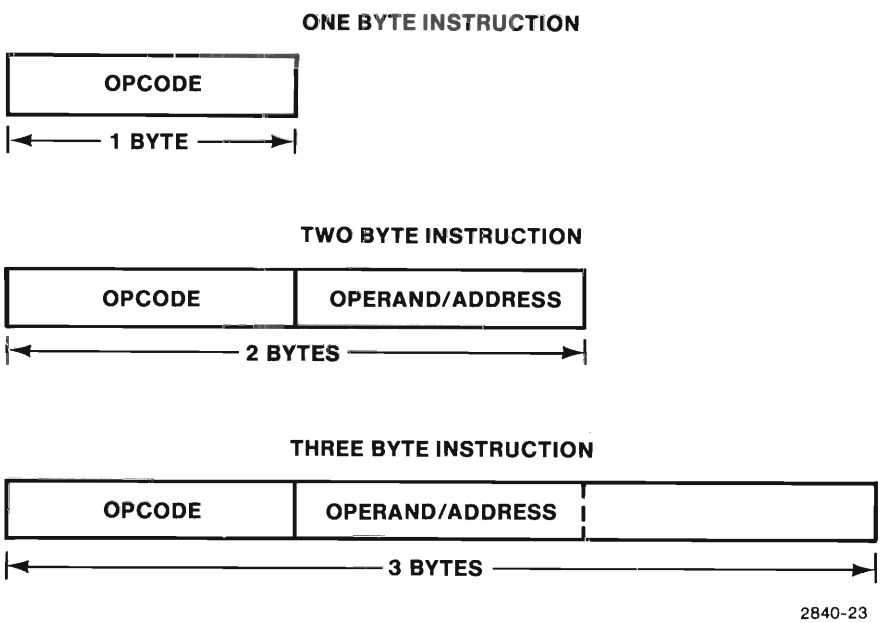


Figure 6-5. Firmware Instruction Format.

The 4052/4054 firmware addressing modes are as follows:

- ACCUMULATOR ADDRESSING. In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

- IMMEDIATE ADDRESSING. In immediate addressing, the operand is contained in the second byte or the second and third bytes of the instruction. The operand is data to be used by the RALU (Register Arithmetic Logic Unit) on the ALU Board. These are two or three-byte instructions.

- DIRECT ADDRESSING. In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing accesses the lowest 256 bytes of RAM space or ROM space. Data space is determined by the CCRD bit in the condition code register. These are two-byte instructions.

- EXTENDED ADDRESSING. In extended addressing, the second byte of the instruction is used as the higher eight bits of the operand address. The third byte of the instruction is used as the lower eight bits of the operand address. This address is the absolute address of the operand in RAM space or ROM space. Data space is determined by the CCRD bit in the Condition Code Register. These are three-byte instructions.

- INDEXED ADDRESSING. In indexed addressing , the address contained in the second byte of the instruction is added to the index register's lower byte. The upper byte added to the index register upper byte is all zeros. The offset is in the range of 0 to 255. These are two-byte instructions.

- IMPLIED ADDRESSING. In the implied addressing mode the instruction indicates the address (i.e., stack pointer, index register). These are one-byte instructions.

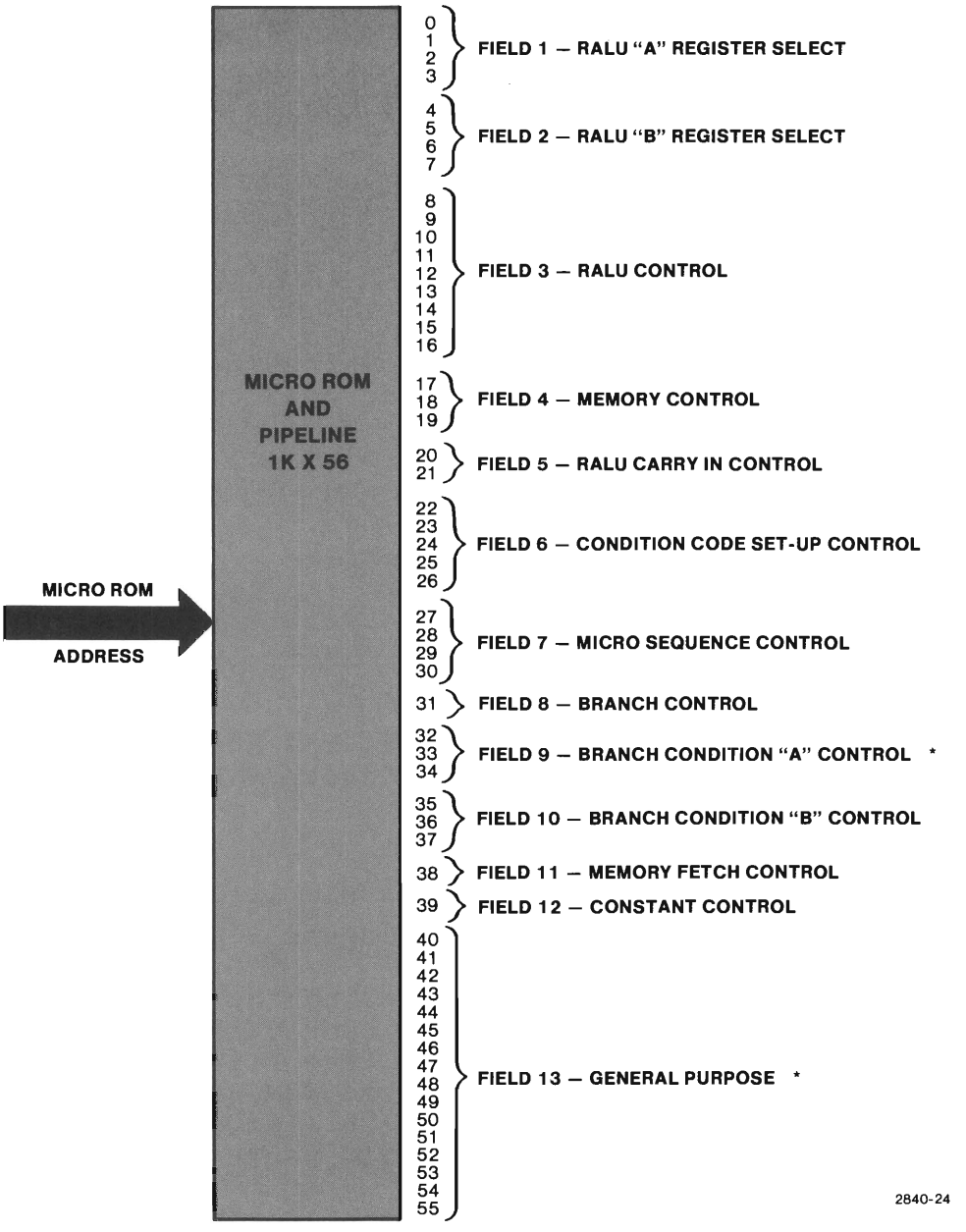
- RELATIVE ADDRESSING. In relative addressing, the second byte of the instruction is added to the program counter's lower eight bits. If Bit 7 in the second byte is a one, the upper byte added to the program counter is set to all ones. If Bit 7 is a zero, the upper byte added to the program counter is set to all zeros. The offset is in twos complement. These are two-byte instructions.

4052/4054 MICROCODE

The 4052/4054 microcode is a ROM array of 1K words with 56 bits per word (Figure 6-6). One or more microcode instructions are executed for each firmware instruction. The microcode instructions are the machine (board logic) control of operations. Each microcode word is divided into fields, and each field has a different function. The 13 fields of the microcode word are as follows:

- Field 1 - RALU "A" Register Select.
- Field 2 - RALU "B" Register Select.
- Field 3 - RALU Control.
- Field 4 - Memory Control.
- Field 5 - RALU Carry in Control.
- Field 6 - Condition Code Set-up Control.
- Field 7 - Micro Sequence Control.
- Field 8 - Branch Control.
- Field 9 - Branch Condition "A" Control.(1)
- Field 10 - Branch Condition "B" Control.
- Field 11 - Memory Fetch Control.
- Field 12 - Constant Control.
- Field 13 - General Purpose.(1)

(1) Function of output depends on the output of field 12.



*FUNCTION OF OUTPUT DEPENDS ON FIELD 12

Figure 6-6. Micro ROM Output Fields.

Field 3 RALU Control

Field 3 controls the data source, operation, and data destination of the RALU (Figure 7-2). The data source is controlled by the lower three bits of field 3. The sources are the "A" port, the "B" port, data from the ALUIN0 through ALUIN15 lines, "Q" register (multiply or divide), and zero (register load). The sources input to the RALU's arithmetic logic unit "R" port and "S" port. The "R" port data source comes from either data, "A" port, or zero. The "S" port data source comes from either "Q" register, "B" port, "A" port, or zero. The Table 6-2 gives the source selections.

Table 6-2

RALU SOURCE OPERAND CONTROL

Micro Code			Octal	RALU Source Operations	
I2	I1	I0	Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

A= Port "A"
B= Port "B"
D= Data input (ALUIN0 thru ALUIN15)
Q= "Q" Register
0= Zero

The middle three bits of field 3 controls the RALU function of the "R" and "S" ports. The result is at the "F" port. Table 6-3 shows the code and functions.

Table 6-3

RALU FUNCTION CONTROL

Micro Code			Octal Code	RALU Function
I5	I4	I3		
L	L	L	0	R Plus S
L	L	H	1	S Minus R
L	H	L	2	R Minus S
L	H	H	3	R OR S
H	L	L	4	R AND S
H	L	H	5	(NOT R) AND S
H	H	L	6	R EX-OR S
H	H	H	7	R EX-NOR S

R= "R" port
S= "S" port

The last three bits of field 3 determine the destination of the RALU (Figure 7-2) resultant output from the "F" port. Table 6-4 shows the destination control for the RALU.

Table 6-4

RALU DESTINATION CONTROL

Micro Code			Octal	Register Function		Q Register Function		ALUOUT	Register Shifter		Q Register Shifter	
I8	I7	I6	Code	Shift	Load	Shift	Load	Source	LSB	MSB	LSB	MSB
L	L	L	0	X	NONE	NONE	F->Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F->B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F->B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2->B	DOWN	Q/2->Q	F	F(LSB)	IN(MSB)	Q(LSB)	IN(MSB)
H	L	H	5	DOWN	F/2->B	X	NONE	F	F(LSB)	IN(MSB)	Q(LSB)	X
H	H	L	6	UP	2F->B	UP	2Q->Q	F	IN(LSB)	F(MSB)	IN(LSB)	Q(MSB)
H	H	H	7	UP	2F->B	X	NONE	F	IN(LSB)	F(MSB)	X	Q(MSB)

F= Function result output ("F" port)
X= Don't care or three-state, high-impedance
B= The register addressed by field 2 ("B" register select)
A= The register addressed by field 1 ("A" register select)
MSB= The most significant bit (bit 7 or bit 15)
LSB= The least significant bit (bit 0)

Field 4 Memory Control

Field 4 is for the microcode control of memory data transfers (Table 6-5). This field indicates the operation to be performed by the MCP Board.

Table 6-5

MEMORY CONTROL

Micro Code			Octal	Memory
PLMC2	PLMC1	PLMC0	Code	Function
L	L	L	0	NOP
L	L	H	1	INC PC by 1
L	H	L	2	PC TO ALU
L	H	H	3	ALU TO PC[a]
H	L	L	4	XFER 8[b]
H	L	H	5	XFER 16
H	H	L	6	R ADDR
H	H	H	7	W ADDR

PC= Program Counter
ALU= ALU Board
XFER 8= Transfer 8 bits To/From D Space
XFER 16= Transfer 16 bits To/From D Space
R ADDR= Read Address in D Space
W ADDR= Write Address in D Space

[a] **Also sets "Actual" Fetch space equal to CCR Bit F.**

[b] **Top byte is undefined.**

Field 5 RALU Carry-in Control

Field 5 is the control of the carry input to the RALU during register shifts (Table 6-6).

Table 6-6

RALU CARRY-IN CONTROL

Micro Code		Octal	
CRYC1	CRYC2	Code	Function
L	L	0	Carry-in= 0
L	H	1	Carry-in= 1
H	L	2	CCRC
H	H	3	Inverse of CCRC

CCRC= The present state of the CCRC bit out of the Condition Code Register.

Field 6 Condition Code Set-up Control

Field 6 (Figure 6-7) is used to select the RALU conditions and the data space selection (RAM or ROM) for the Condition Code Register. The firmware instructions require various sets of conditions to be active during instruction executions.

HEX CODE	CONDITION CODE EFFECTED								
	C	V	Z	N	I	H	D	F	
00									
01	↕	↕	↕	↕	•	↕	•	•	
02	↕	↕	↕	↕	•	•	•	•	
03	•	↕	↕	↕	•	•	•	•	
04	S	R	↕	↕	•	•	•	•	
05	~	↕	↕	↕	•	•	•	•	① CARRY NOT
06	•	↕	↕ 16	↕ 16	•	•	•	•	
07	•	•	↕ 16	•	•	•	•	•	16 BIT ZERO
08	•	R	↕ 16	↕ 16	•	•	•	•	
09	•	R	↕	↕	•	•	•	•	
0A	A0	*	+	C	•	•	•	•	ROR, V= N ⊕ C
0B	•	•	↕	•	•	•	•	•	8 BIT ZERO
0C	A0	*	↕	R	•	•	•	•	LSR, V= N ⊕ C
0D	↕ 16	↕ 16	↕ 16	↕ 16	•	•	•	•	
0E	A0	*	•	•	•	•	•	•	ASR, V= N ⊕ C
0F	•	•	B	•	•	•	•	•	BY BRMUX2 STATE
10	•	•	•	B	•	•	•	•	BY BRMUX2 STATE
11	•	B	•	•	•	•	•	•	BY BRMUX2 STATE
12	B	•	•	•	•	•	•	•	BY BRMUX2 STATE
13	•	•	•	•	B	•	•	•	BY BRMUX2 STATE
14	•	•	•	•	•	B	•	•	BY BRMUX2 STATE
15									
16									
17									
18	•	•	•	•	•	•	R	•	DATA ROM
19	•	•	•	•	•	•	•	R	FETCH RAM
1A	A0	A1	A2	A3	A4	A5	A6	A7	ALU → C.C.R.
1B									
1C	•	•	•	•	•	•	S	•	DATA RAM
1D	•	•	•	•	•	•	•	S	FETCH ROM
1E									
1F	•	•	•	•	•	•	•	•	NO CHANGE

⊕ = EX–OR
• = NOT CHANGED
S = SET (1)
8 = 8 BIT (assumed)
R = RESET(0)
16 = 16 BITS
↕ = SELECTED CONDITION
C = OLD CARRY
* = N + C
+ = (UNDEFINED)
~ = NEGATED CONDITION
B = BRMUXZ OUTPUT
An = ALUOUT BIT n

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Figure 6-7. Condition Code Set-up Control.

Field 7 Micro Sequence Control

Field 7 controls the function of the Micro ROM Sequencer (Table 6-7). The Micro ROM Sequencer sets up the address of the next microcode instruction to be executed.

Table 6-7

MICRO SEQUENCE CONTROL

Micro Code				Hex	
SEQ3	SEQ2	SEQ1	SEQ0	Code	Function
L	L	L	L	0	
L	L	L	H	1	Call
L	L	H	L	2	Not used
L	L	H	H	3	Go to
L	H	L	L	4	Do
L	H	L	H	5	Branch (to)
L	H	H	L	6	Not used
L	H	H	H	7	Not used
H	L	L	L	8	Not used
H	L	L	H	9	Not used
H	L	H	L	A	Return
H	L	H	H	B	Go to (pop)
H	H	L	L	C	Load branch counter
H	H	L	H	D	Loop
H	H	H	L	E	Continue (default)
H	H	H	H	F	Finish

Field 8 Branch Control

Field 8 determines the condition of agreement with the selected branch condition by Field 8 or Field 9 (only one field is active at any given time). Field 8 is a one line control. If Field 8 is low, the branch is taken when the condition is true. If Field 8 is high, the branch is taken when the condition is false.

Field 9 Branch Condition "A" Control

Field 9 has two functions: branch condition select when Field 12 is low and data to the RALU when Field 12 is high (Table 6-8).

Table 6-8

FIELD 9 BRANCH CONDITION "A" CONTROL

Micro Code			Hex	Function	
BRMUX2	BRMUX1	BRMUX0	Code	Field 12 = 0	Field 12 = 1
L	L	L	0	Always false	Field 13 to RALU
L	L	H	1	CCRC	CCR to RALU
L	H	L	2	CCRN	
L	H	H	3	CCRV	Clear INT (a)
H	L	L	4	CCRN EX-OR CCRV	Set CCR bit(b)
H	L	H	5	CCRH	
H	H	L	6	Not used	
H	H	H	7	Not used	

(a) Clears the NMI and HDWFAIL interrupts

(b) BRXMU2 equals 1 sets the selected Condition Code Register bit and BRMUX2 equals 0 clears the Condition Code Register bit dependeing on Field 6 selection.

Field 10 Branch Condition "B" Control

Field 10 selects the branch conditions for the Micro Sequencer (Table 6-9). Field 9 and Field 10 are used together for conditional branching.

Table 6-9

FIELD 10 BRANCH CONDITION "B" CONTROL

Micro Code			Hex	
BRMUX5	BRMUX4	BRMUX3	Code	Function
L	L	L	0	Always false
L	L	H	1	CCRZ
L	H	L	2	Any Interrupt
L	H	H	3	HDWFAIL interrupt
H	L	L	4	Counter = 16
H	L	H	5	Not used
H	H	L	6	Not used
H	H	H	7	Not used

Field 11 Memory Fetch Control

Field 11 is a control line to the MCP Board. This line is used to initiate a fetch of the next instruction when the Micro Code is finished with the last instruction. Field 11 is also used by the MCP Board as the number of bits in the write address (Field 4-WADDR) or read address (Field 4-RADDR).

Field 12 Constant Control

Field 12 is a control line used during loading of the RALU with either a constant from the Micro Code Field 13 or the contents on the Condition Code Register. Field 12 changes the functions of Field 13 and Field 9.

Field 13 General Purpose

Field 13 supplies a 16-bit constant to the RALU when Field 12 equals 1. When Field 12 equals 0 the output of Field 13 is used for shift control and Micro ROM branching address (Figure 6-8).

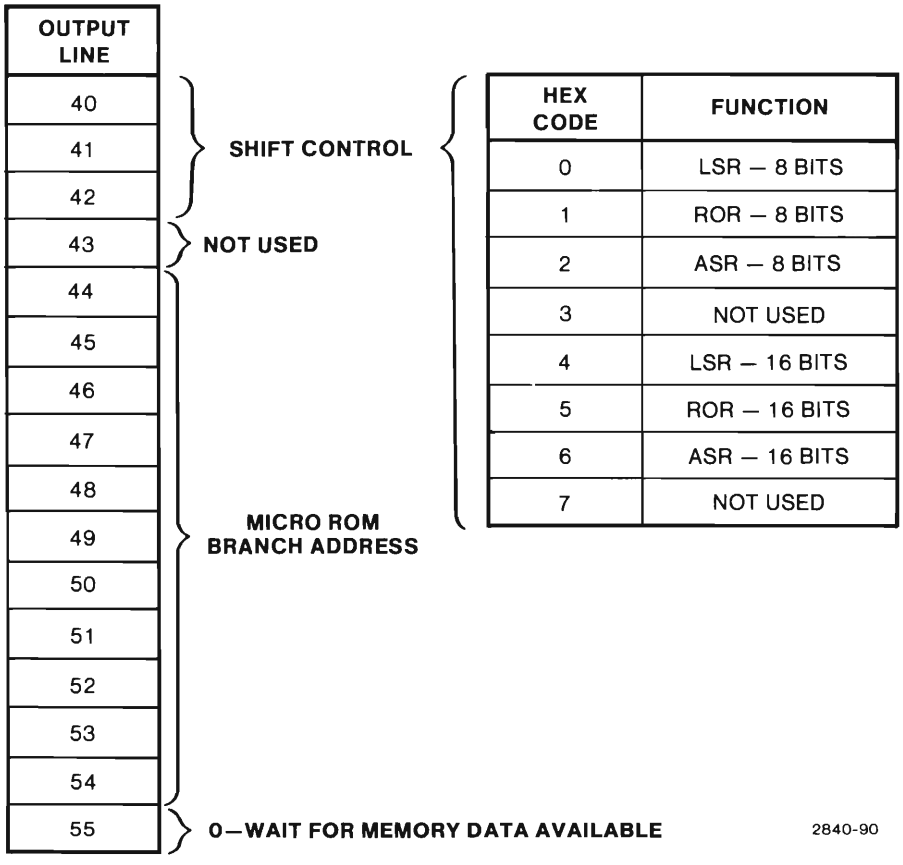


Figure 6-8. Field 13 - General Purpose (Field 12 = 0).

4052/4054 SYSTEM BLOCK DESCRIPTION

The description presented here is a general overview of the 4052 and 4054 systems. For a detailed description refer to Section 7 (ALU, MCP, AND MAS CIRCUIT BOARDS THEORY OF OPERATION) or to the I/O sections (keyboard, mag tape unit, display, or GPIB). Refer to Figure 6-9 and Figure 6-10 for the following description. The only difference between the 4052 and the 4054 systems is the display circuitry.

4052/4054 System Overview

The 4052/4054 system consists of the I/O units (display, keyboard, backpacks, internal mag tape unit, and GPIB) and the processor boards (ALU, MCP, and MAS Boards). The I/O Board interfaces the processor boards to the I/O units. The functions of the processor boards and I/O Board can be summarized as follows:

- ALU - Arithmetic Logic Unit. This is the microprogrammed processor board containing the arithmetic logic units (RALUs). The system microcode, the major processor registers (accumulators, index register, stack pointer, etc.), and master clock circuitry. This board, through the mircroprograms and related hardware, controls the fundamental system operations and execution of firmware (macro) level instructions.

- MCP - Memory Command Processor. Directing memory operations, the MCP plays a major role in the execution of firmware instructions and coordinating data transfers between the ALU and memory. Some of its' primary functions are: determining the source and destination of address/data information being passed to the Memory Access Sequencer, relaying information on the number of bytes involved in a memory transfer or which memory space is involved in the operation, and upkeep of the firmware level program counter (the only processor-related register not contained on the ALU). It also is involved in the operation of the MBUS (main 16-bit bus between the MCP and MAS).

- MAS - Memory Access Sequencer. Under the direction of the MCP, the MAS performs the actual memory accesses for read/write operations. Besides containing the timing logic for these operations, the MAS also holds address decoding logic for accessing the I/O and ROM Pack address spaces. All system RAM and ROM (firmware) are located on this board.

- I/O - Input/Output. Providing the interface to the outside world, the I/O board generates the necessary timing for the operation of the keyboard, magtape, display, GPIB, and peripheral/ROMPACK circuitry.

There are four types of data carriers in the 4052/4054 system:

- ADDRESS AND DATA. The 16-bit data or the 16-bit memory space address is carried on this bus between the MCP Board and the MAS Board.

- ADDRESS ONLY. The 16-bit address from the MCP Board is split into two 16-bit address busses on the MAS Board: an even address bus and an odd address bus. The even address bus is used for even RAM and ROM addressing, for external addressing of the backpacks, and for the I/O Board addressing. The odd address bus is used for odd RAM and ROM.

- DATA ONLY. The 16-bit data between the MCP Board and the MAS Board is split into two 8-bit busses: an even data bus and an odd data bus. The even data bus is for even RAM and ROM data, and for external data for the backpacks and the I/O Board. The odd data bus is for the odd RAM and ROM data and 16-bit external data (first external byte).

- OTHER.The rest consists of Micro ROM addressing, timing signals, control lines, I/O data, and handshaking between the circuit boards.

The Micro ROM on the ALU Board performs a partial system check during power up (refer to 4052/4054 MICROCODE). When finished with the power up operation, the microcode is controlled by firmware instructions from the MAS Board or Backpacks. The firmware instruction is latched into the Instruction Register. The Instruction Register is decoded and the microcode sequence for the firmware instruction is executed. During each microcode instruction the microcode word is latched into the Pipeline Register. This allows the ALU Board control to set up the address of the next microcode word to be executed.

Data between the ALU Board and the MCP Board is transfered over two 16-bit busses: one for data to the RALU and one for data from the RALU. The RALU and Condition Code Logic consist of 16 registers, an arithmetic logic unit, Condition Code Register, and shift logic.

Part of the microcode controls the operation and data-address transfer between the MAS Board, the MCP Board, and the ALU Board. The MCP Board has a Program Counter, Zero High/Sign Extended, ALU input and output latches, and a Memory Byte Latch. The Program Counter is used for addressing of the firmware instruction. The ALU input and output latches are used to store RALU data. The Memory Byte Latch and the Zero High/Sign Extended are used together during firmware instruction fetching and execution.

The MCP Board controls the address and read or write of data on the MAS Board. The address from the MCP Board is received by the Address Bus Logic. For non-external addressing the address is put on the odd address bus, and the address plus one is put on the even address bus. For external addressing, the address is put on the even address bus and on the external address lines. If only one byte is needed the external addressing is finished, but if two bytes are needed the even address is incremented and the external address is enabled again for the second byte. When 16 bits of data from external are read, the first byte is latched and put on the odd data bus, while the second byte is placed on the even data bus.

The data to and from the MCP Board to the MAS Board splits into an 8-bit odd data bus and an 8 bit even data bus on the MAS Board. Depending on the operation and the address (Figure 6-11), even data is active on either the low byte or the high byte of MCP Board 16-bit data but not to both bytes. The odd data is active on the byte not used by the even data. The Data Bus Logic can cross the data bytes between the MAS Board and the MCP Board.

The I/O Board contains the external interface to the internal mag tape drive, the keyboard, the display, and the GPIB Interface.

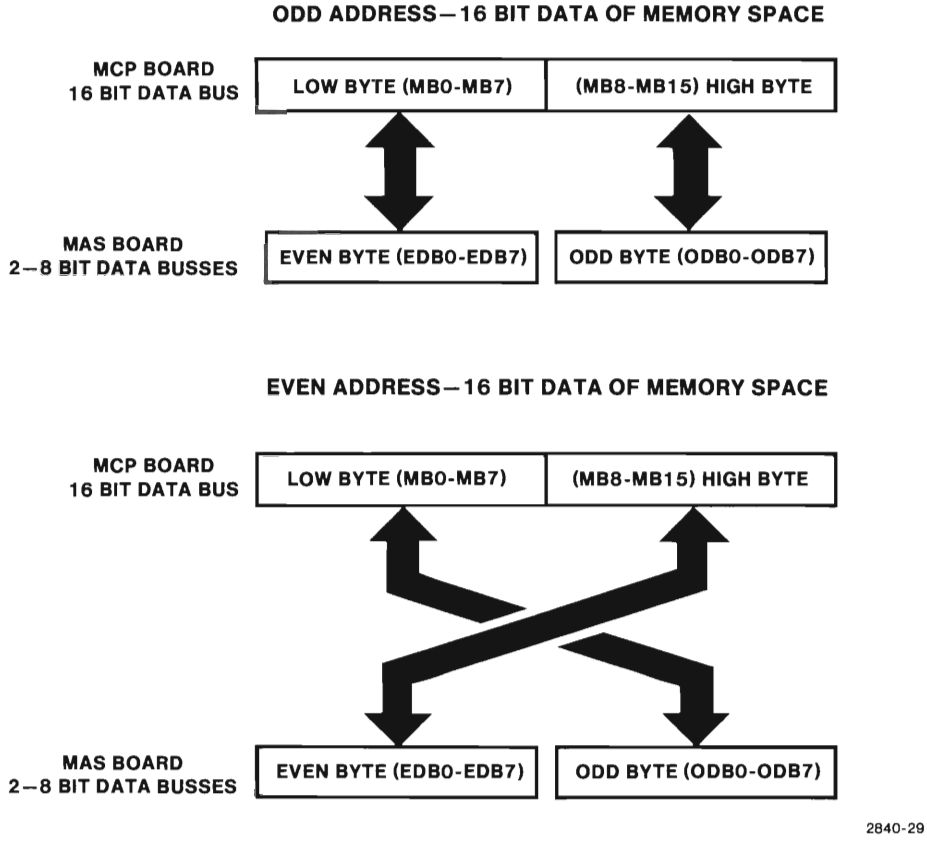


Figure 6-11. MCP Board and MAS Board Data Bytes Transfer.

4052/4054 FIRMWARE INSTRUCTION DATA TRANSFER

The 4052/4054 firmware instructions are processed by the processor in the following sequence:

- Fetch firmware instruction.
- Decode instruction.
- Execute the instruction.
- Honor pending interrupts.
- Go back to fetch.

The address and data flow for the firmware instructions vary depending on the type of addressing used: immediate (one or two bytes data), direct, extended, indexed, implied, or relative. (Refer to the firmware part of this section.)

Firmware Instruction Fetch

The fetch cycle is started when the microcode pulls the MHOLD-0 control line to the MCP Board low (Figure 6-12). The MCP Board enables the output of the Program Counter to the MB15-MB0 bus. The address is applied to the Even and Odd ROM (external to the Backpacks, if the address is a Backpack address). Two bytes of data are always fetched. The high byte of data (MB15-MB8) is loaded into the Instruction Register. The low byte of data is loaded into the Memory Byte Latch for use during two-byte firmware instruction execution. If the instruction is a one-byte instruction, the low byte of the fetch is not used since it is the opcode for the next firmware instruction. The Program counter is incremented for the next firmware instruction or the operand of the present firmware instruction. If the instruction is a three-byte firmware instruction, this stored byte is discarded. The second and third byte of the instruction are fetched together (refer to three-byte immediate and extended instructions).

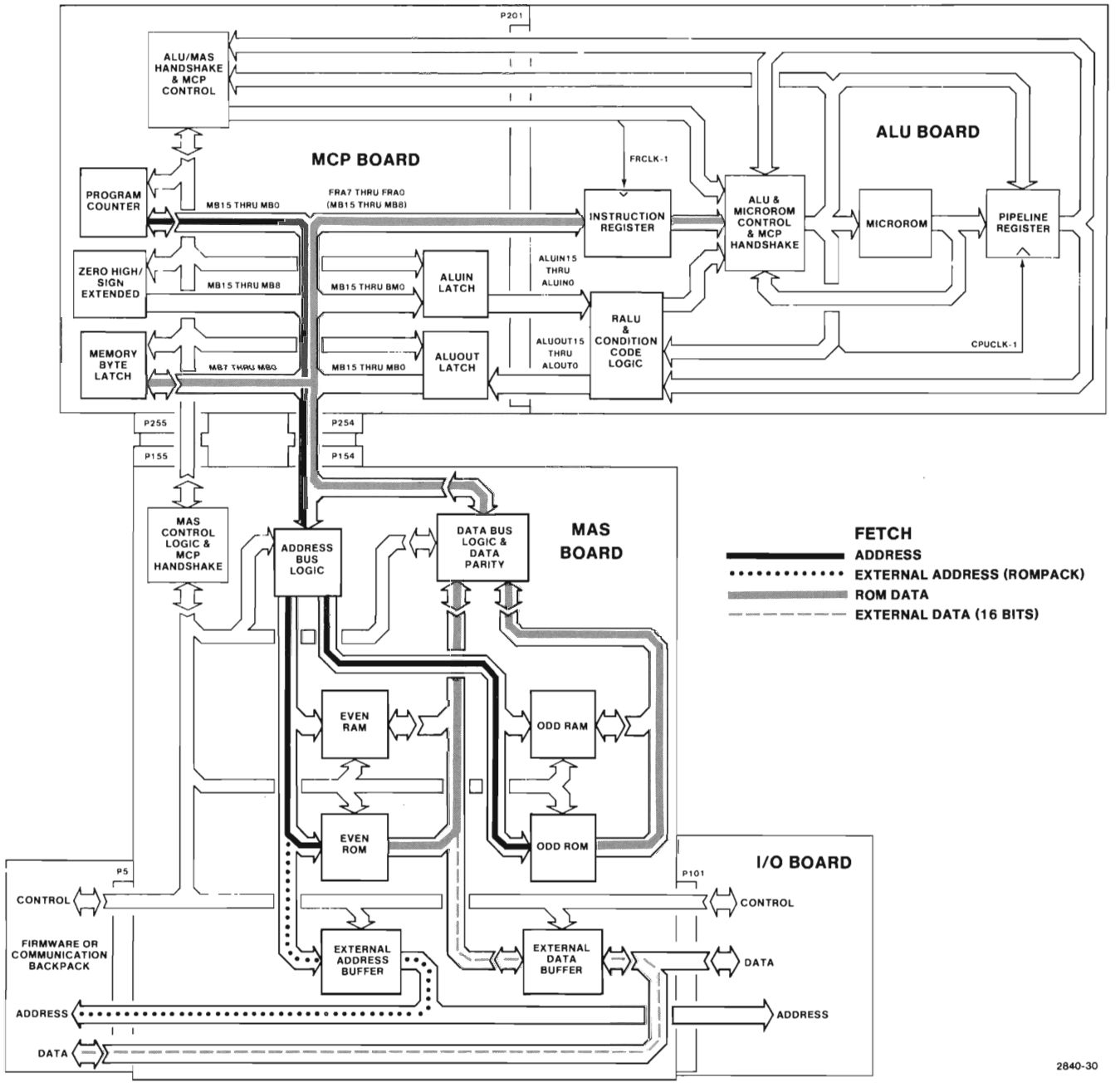


Figure 6-12. 4052/4054 Firmware Instruction Fetch.

Two-Byte Immediate Firmware Instruction

Two-byte immediate firmware instructions require no futher memory access after a fetch. The byte stored in the Memory Byte Latch and a zero byte from the Zero High/Sign Extended is transfered to the Aluin Latch and then to the RALU (Figure 6-13). At the end of the transfer the Progran counter is incremented by one for the next firmware instruction to be executed.

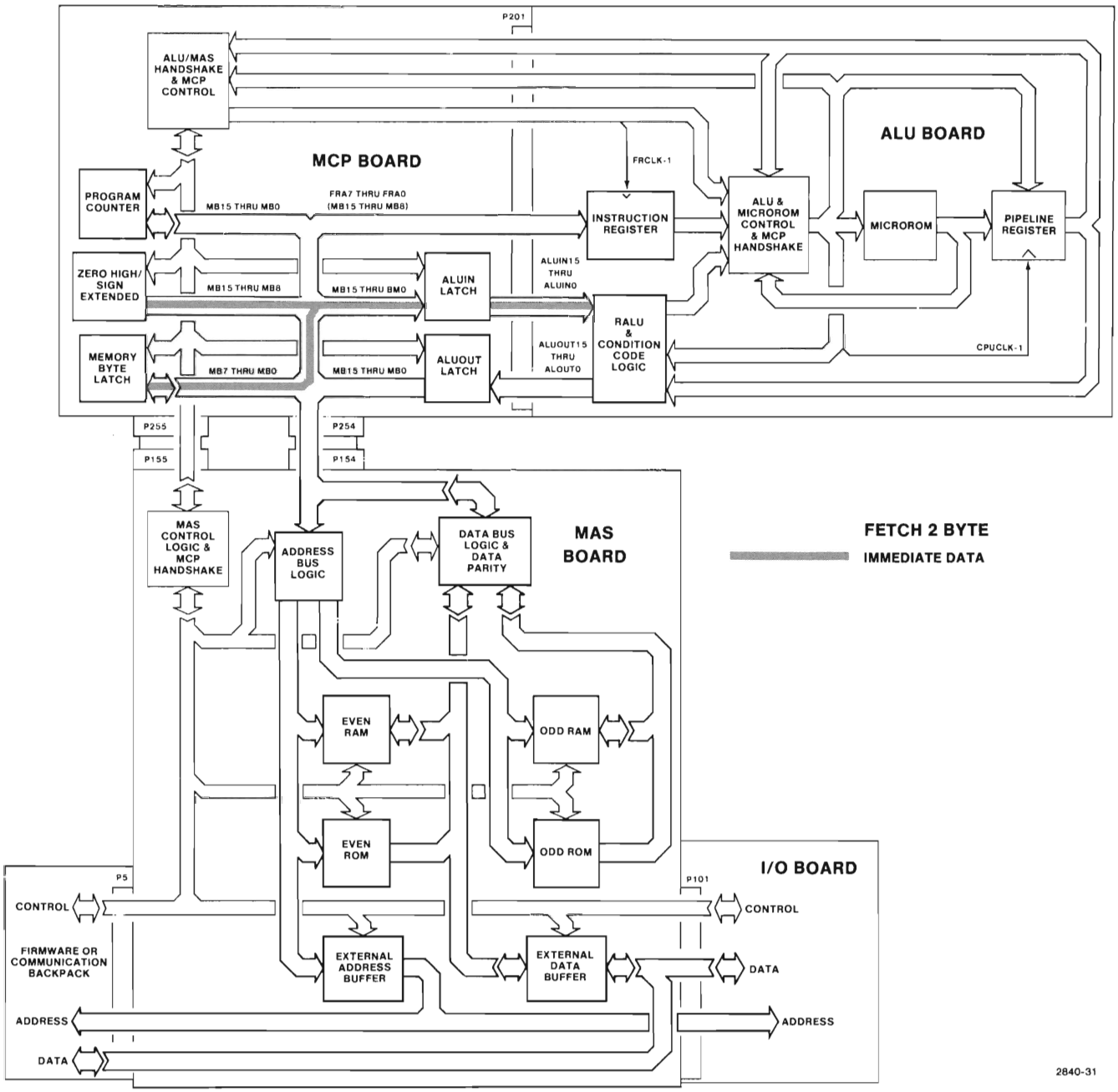


Figure 6-13. 4052/4054 Two-Byte Immediate Firmware Instruction.

Three-Byte Immediate Firmware Instructions

Three-byte firmware instructions require an additional memory access. The byte stored in the Memory Byte Latch is not used. The Program Counter supplies the address to the MAS Board. Sixteen bits of data are returned from the MAS Board. The data is latched in the Aluin Latch and then to the RALU. At the end of the memory fetch the Program Counter is incremented by two for the next firmware instruction.

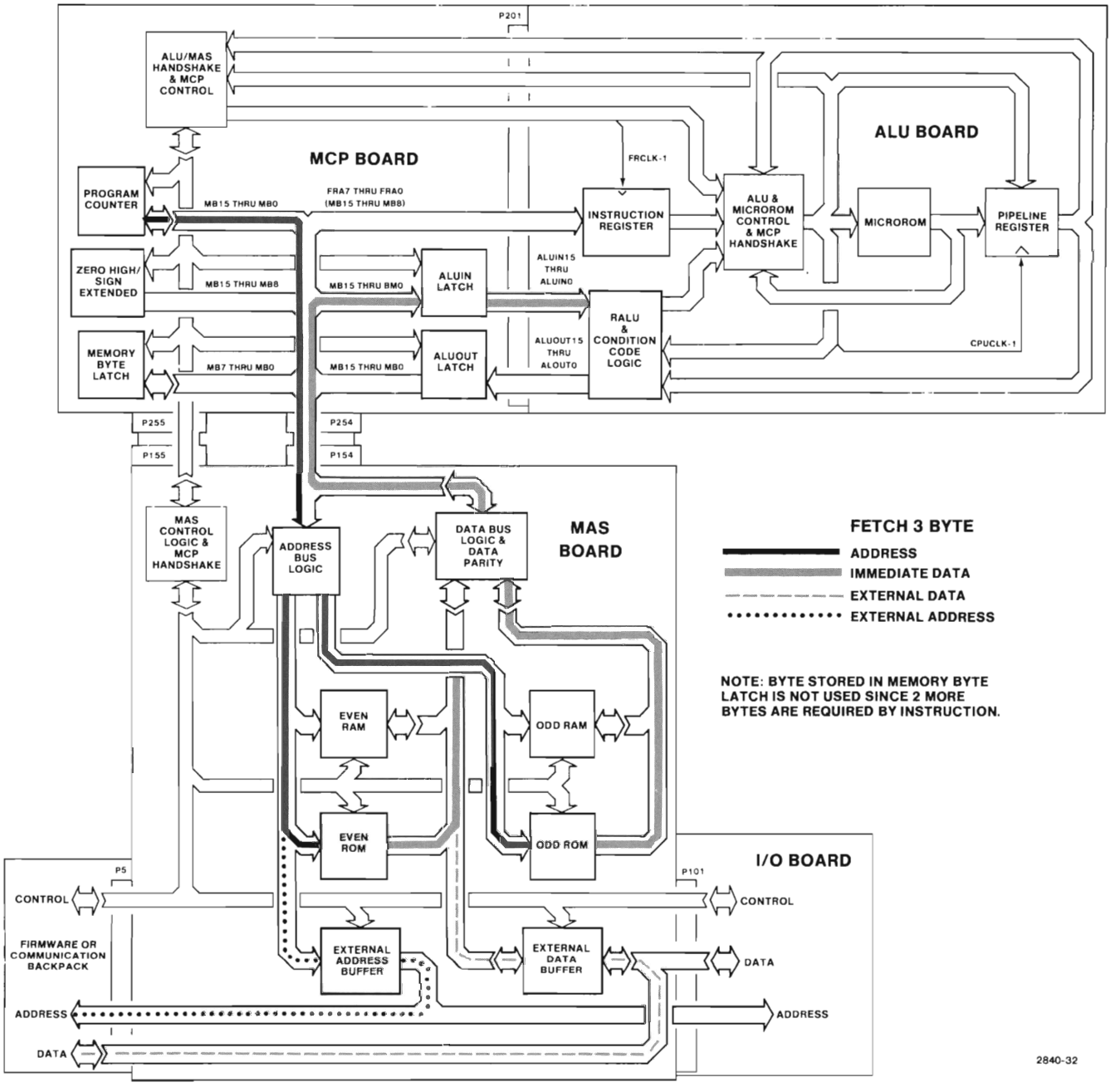


Figure 6-14. 4052/4054 Three-Byte Immediate Firmware Instruction.

Direct Firmware Instruction

Direct firmware instructions are two-byte instructions. The second byte is used for addressing the first 256 bytes of RAM Space or ROM Space, depending on the state of the CCRD bit in the Condition Code Register. The second byte was stored in the Memory Byte Latch during the fetch cycle. The second byte combined with a zero byte from the Zero High/Sign Extended buffer is the address sent to the MAS Board. If the direct address is a write, the data is transferred from the RALU to the Aluout Latch, and then to the MAS Board to be stored in RAM space. If the direct address is a read, the data is transferred from the MAS Board to the Aluin Latch and then to the RALU. At the end of the firmware instruction, the Program Counter is incremented by one for the next memory fetch.

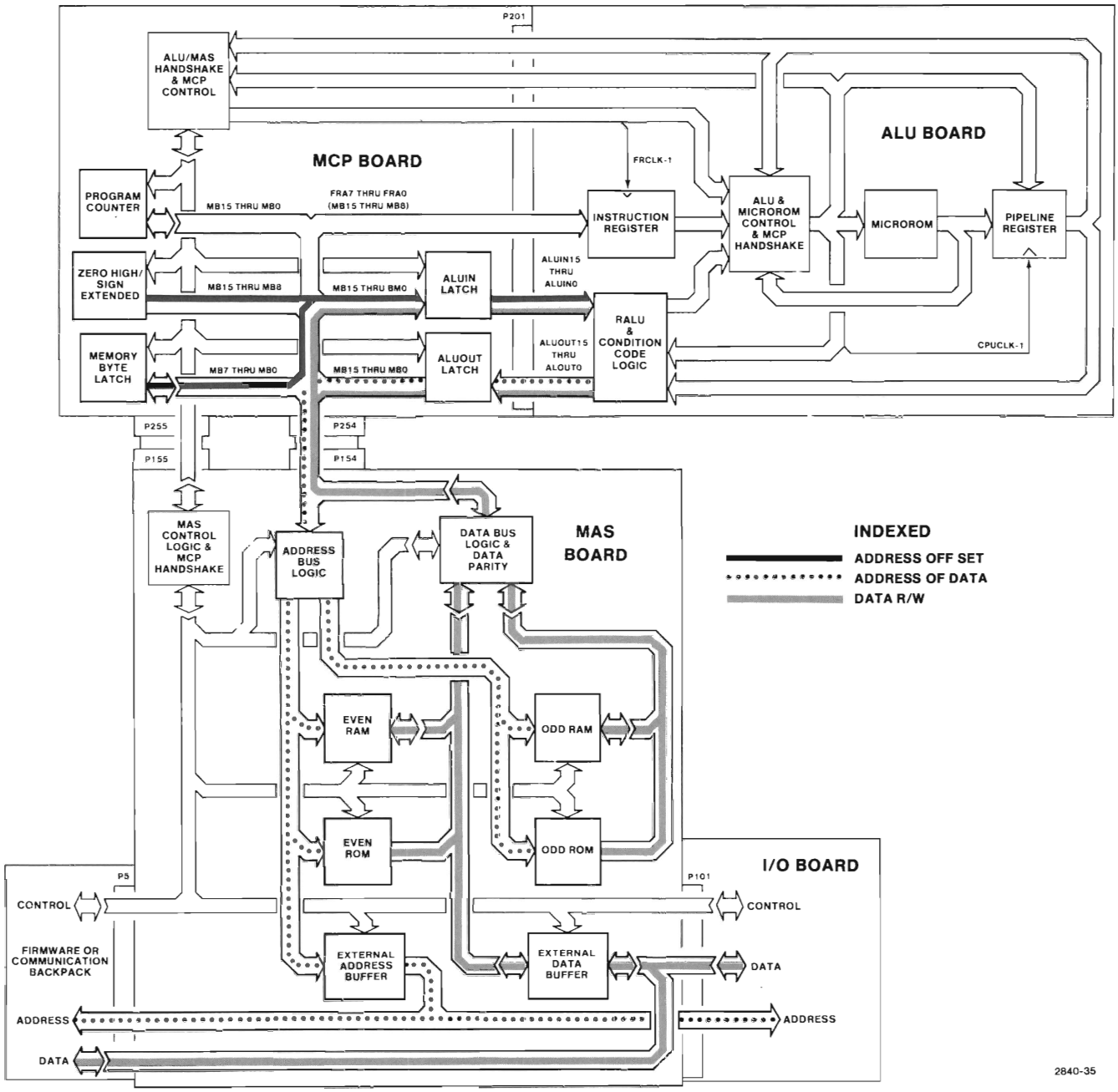


Figure 6-15. 4052/4054 Direct Firmware Instruction.

Extended Firmware Instructions

Extended firmware instructions require an additional memory access. The byte stored in the Memory Byte Latch is not used. After the Program Counter supplies the address to the MAS Board, the operand is sent directly back to the MAS Board by the MCP Board to be used as the data address. Write data for the second memory access comes from the RALU to the Aluout Latch and then to the MAS Board. Read data for the second memory access is latched into the Aluin Latch and then to the RALU. At the end of the last memory cycle the Program Counter is incremented by two for the next fetch cycle.

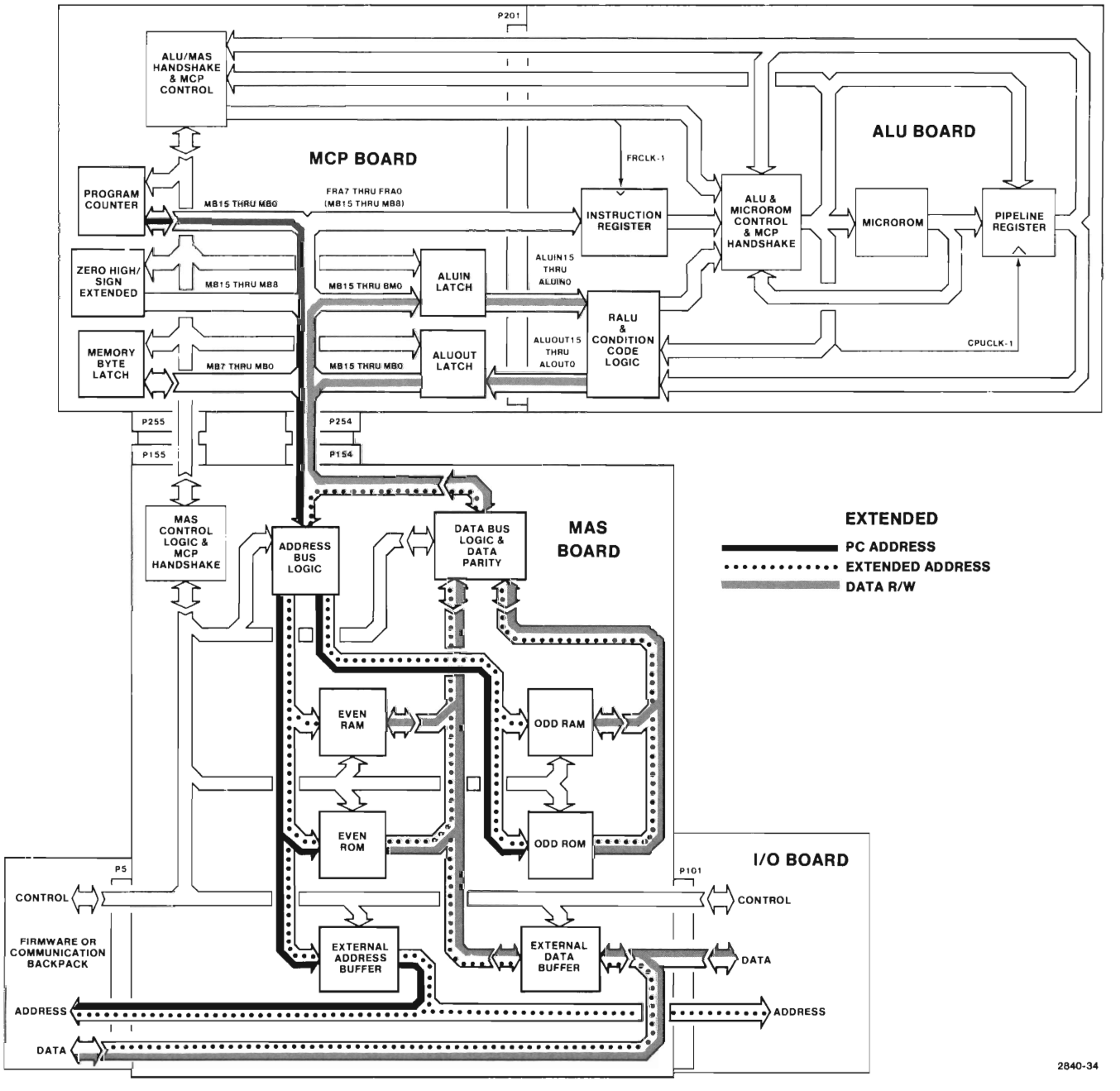


Figure 6-16. 4052/4054 Extended Firmware Instruction.

Indexed Firmware Instructions

Indexed firmware instructions use the byte stored in the Memory Byte Latch as an offset to the index register. The offset is in unsigned binary (0 to 255). The Memory byte Latch (MB7) is used to supply the upper byte os all zeros. The two bytes are latched into the Aluin Latch and then to the RALU. In the RALU the offset is added to the index register. The content of the index register is not changed. The result is latched into the Aluout Latch and supplied to the MAS Board as the address of the required data. Read data is transfered to the Aluin Latch and then to the RALU. Write data is transfered from the RALU to the Aluout Latch and then to the MAS Board. At the end of the address transfer the Program Counter is incremented by one for the next firmware instruction fetch.

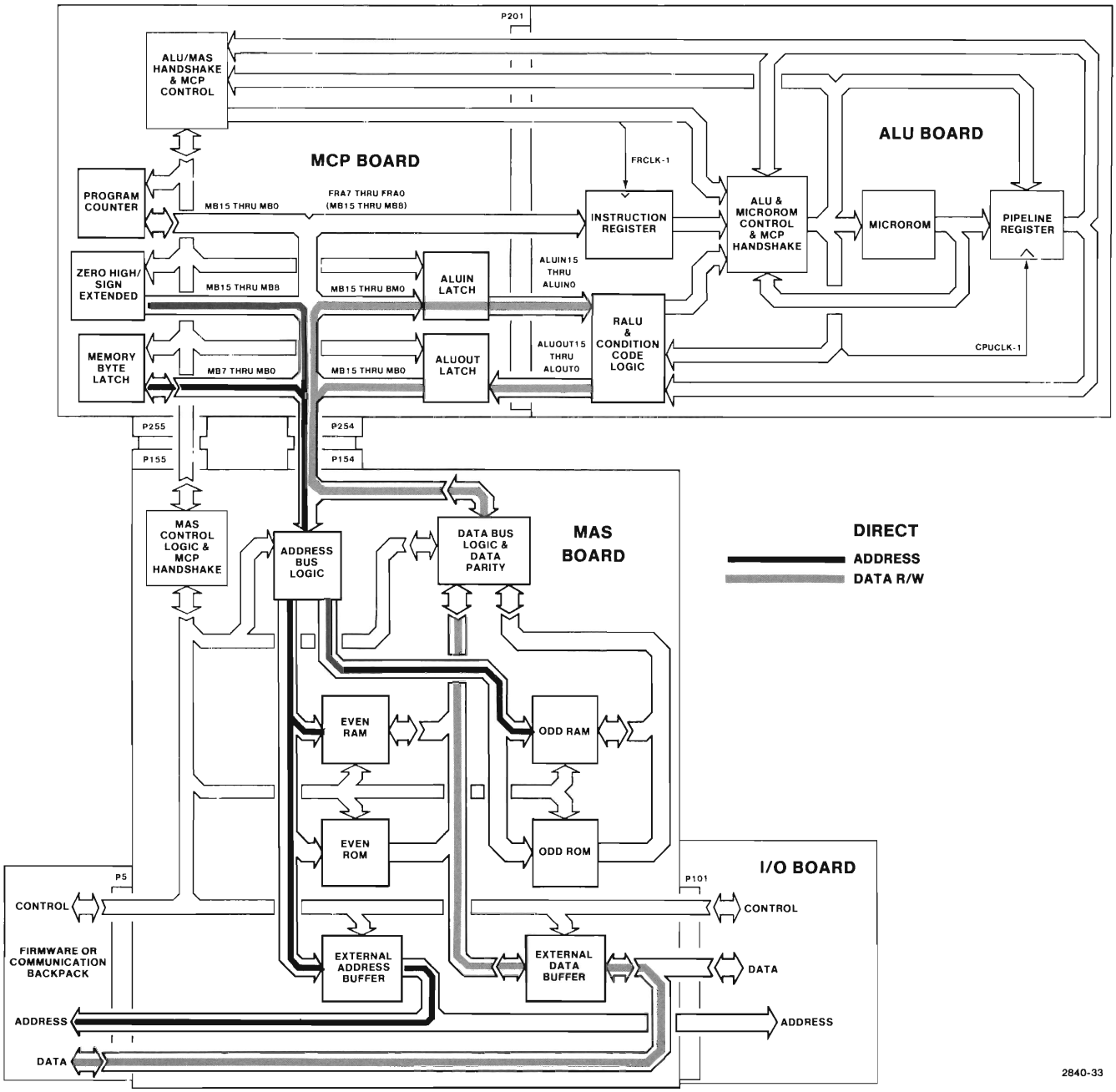


Figure 6-17. 4052/4054 Indexed Firmware Instruction.

Implied Firmware Instructions

Implied firmware instructions use the index register or the stack pointer as the memory address of the data. The address comes from the RALU and is latched into the Aluout Latch. The MCP Board supplies the address to the MAS Board. Read data is transferred from the MAS Board, latched in the Aluin Latch, and then to the RALU. Write data comes from the RALU to the Aluout Latch and then to the MAS Board for storage. Since implied instructions are one byte instructions, the Program counter is not incremented and the stored byte in the Memory Byte Latch is discarded.

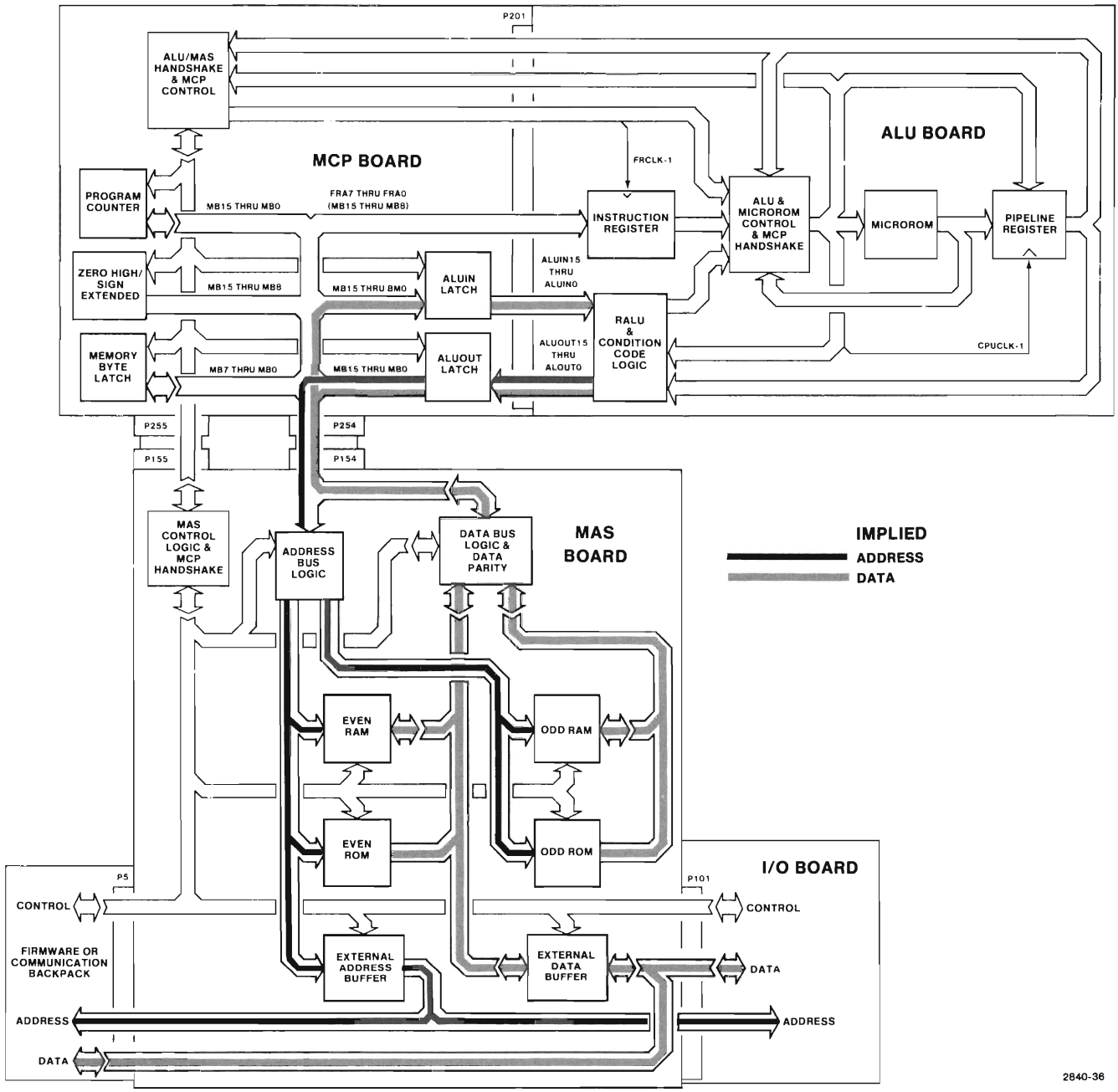


Figure 6-18. 4052/4054 Implied Firmware Instruction.

Relative Firmware Instructions

Relative firmware instructions use the Program Counter and the byte stored in the Memory Byte Latch for the memory address for branches taken. If the branch is not taken the Program Counter is incremented by one and the MCP Board executes a opcode fetch of the next firmware instruction. If the branch is taken, the Program Counter is transferred to the Aluin Latch, then to the RALU. The upper bit (MB7) controls the output of the Zero High/Sign Extended. If the bit is a one, the output of the upper byte is all ones. If the bit is a zero, the output of the upper byte is all zeros. The RALU adds the output of the Memory Byte Latch Latch and Zero High/Sign Extended to the stored Program Counter address. The final address is latched in the Aluout Latch, then transferred to the Program Counter. The Program Counter now contains the next firmware instruction to be executed. The MCP Board is enabled to do a firmware instruction fetch.

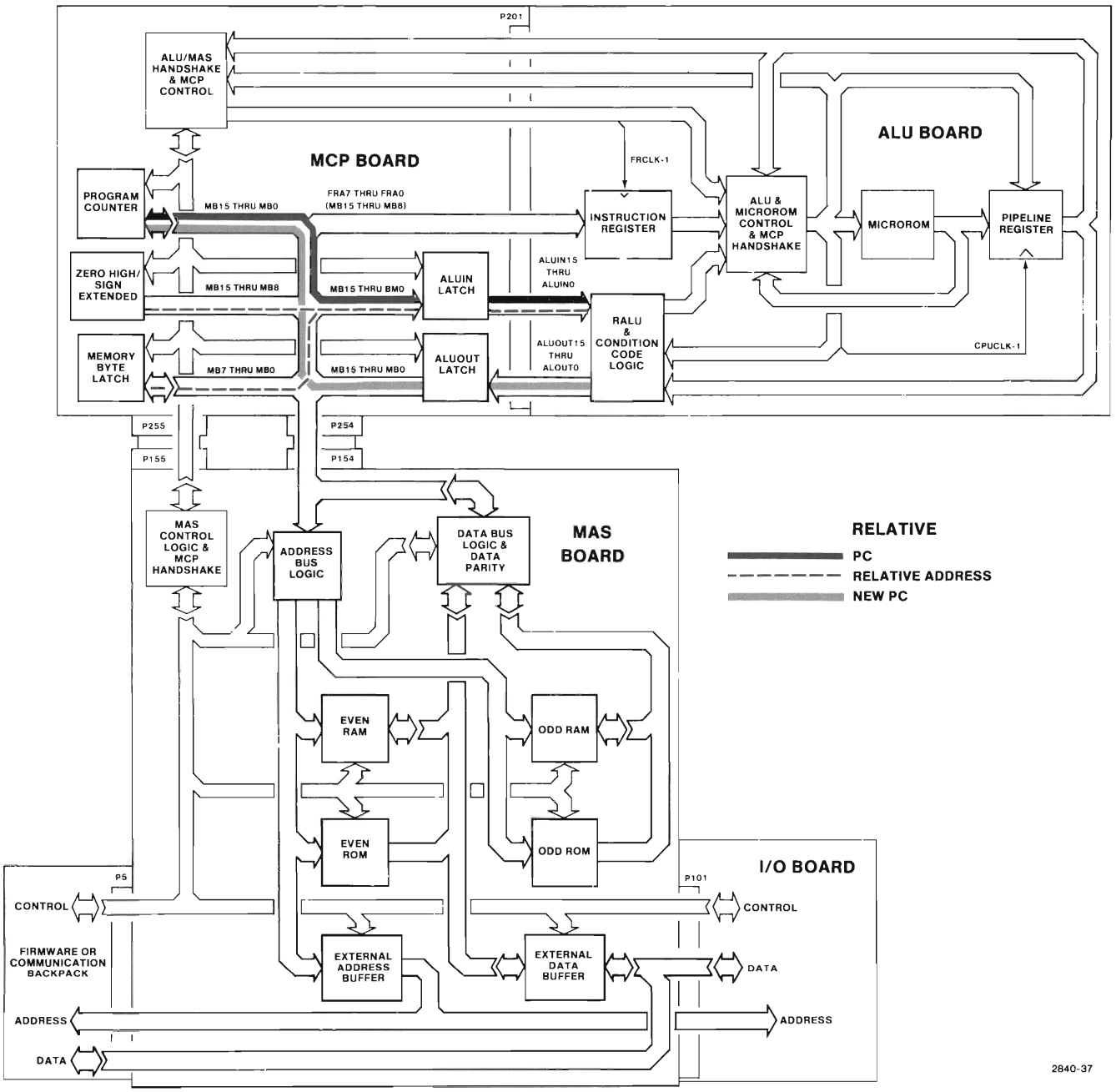


Figure 6-19. 4052/4054 Relative Firmware Instructions.

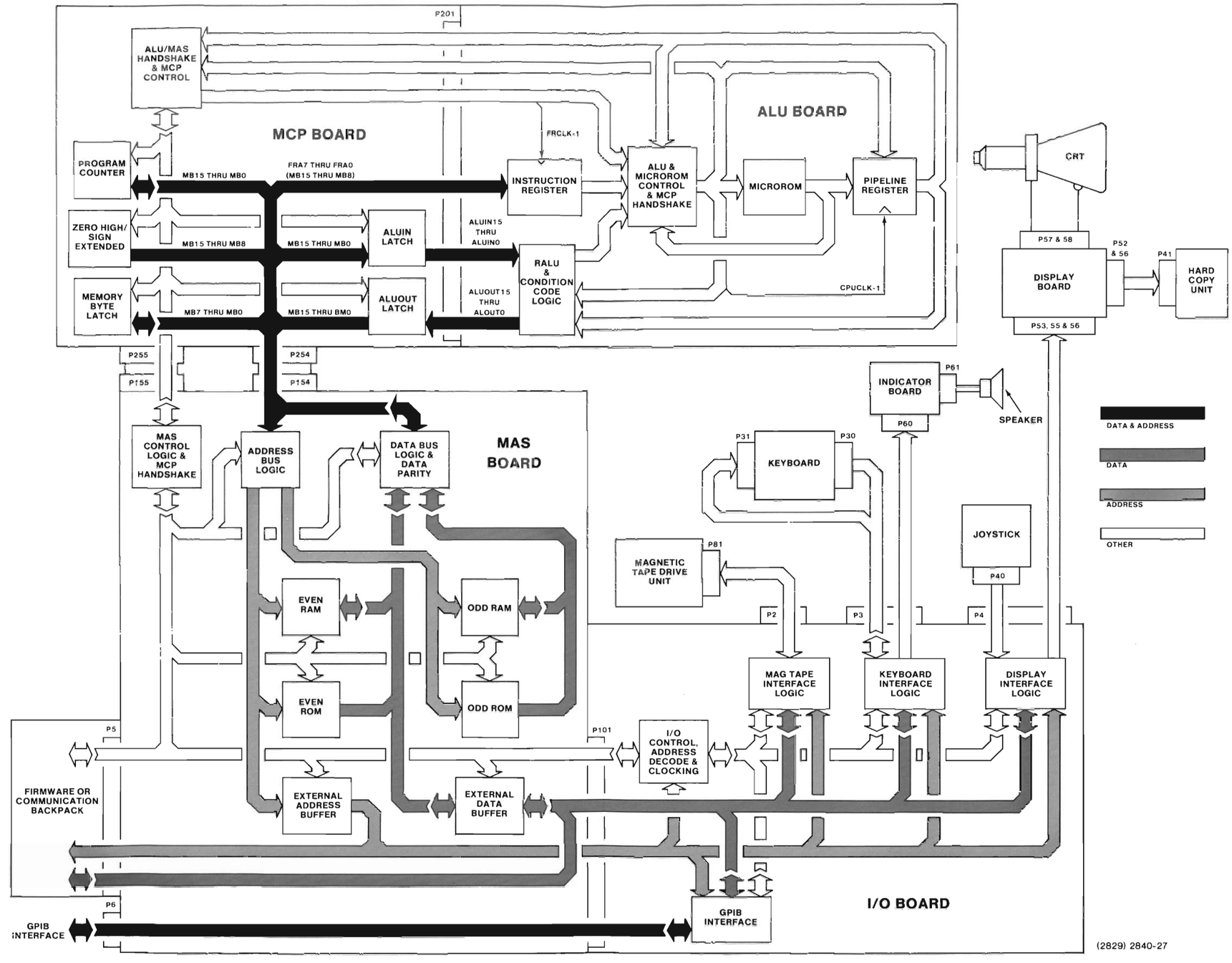


Figure 6-9. 4052/4052A System Block Diagram.

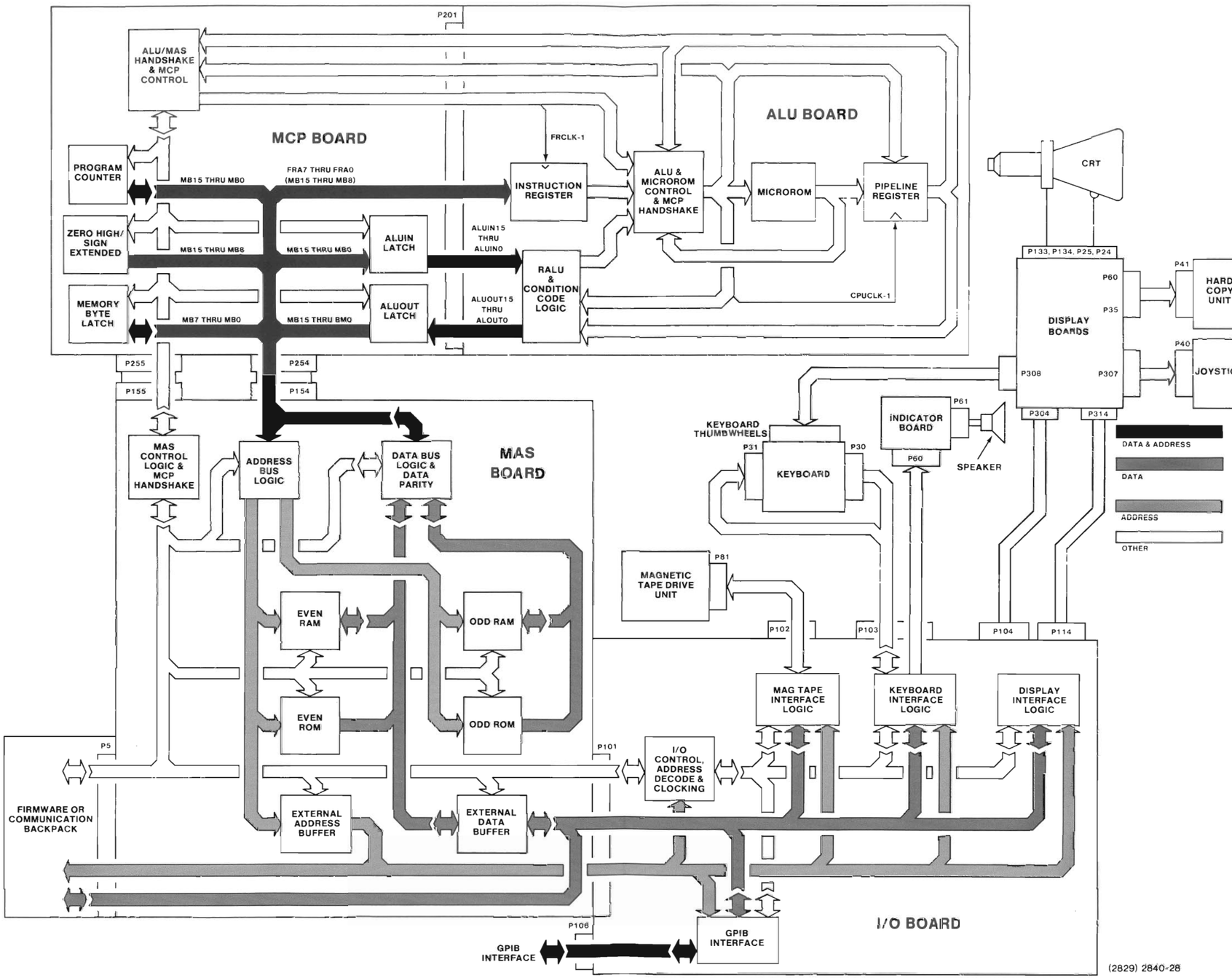


Figure 6-10. 4054/4054A System Block Diagram.

Section 7

ALU, MCP, MAS, AND I/O CIRCUIT BOARDS THEORY OF OPERATION

INTRODUCTION

The ALU Board, MCP Board, and MAS Board are the processor and memory for the 4052/4052A and 4054/4054A Desktop Computers. This section covers the theory of operation and general timing of these three circuit boards. Although the 4052, 4052A, 4054, and 4054A all use different I/O Boards, their operation is quite similar. For details as to operation of the I/O Board, see Section 8, Keyboard Theory of Operation, Section 9, Tape Unit Theory of Operation, and Section 10, GPIB Theory of Operation.

This manual covers the different boards used in the 4052 and 4054 and the 4052A and 4054A Desktop Computers. Each board is commented so you will be able to identify the correct board for your computer system.

You should refer to the following in order to fully understand and use this section:

- Section 6 and Appendix A of this manual
- 4052/4052A Parts and Schematics Service Manual
- 4054/4054A Parts and Schematics Service Manual

ALU BOARD

Two major versions of the ALU Board are used. They differ only in the clock circuitry. The latest version of the ALU Board uses a modular clock, while the earlier version uses a clock built of discrete components.

The ALU Board (Figure 7-1) contains the arithmetic logical unit, firmware instruction decode-execution, interrupt control, and system registers (except for the Program Counter which resides on the MCP Board). The ALU Board interfaces to the MCP Board and is connected to the interrupt lines from the rest of the computer system. The ALU Board contains the following functional units:

- Instruction Register
- Fetch Control
- Wait Control
- Memory Controller Handshake
- Clocks
- Sequence Instruction Branch
- Sequence Micro ROM Branch
- Interrupt Generator
- Micro Sequencer Branch Control
- RALU
- RALU Constant Load
- Shift Control
- Condition Code Set-up and Register
- Micro ROM
- Micro ROM Sequencer
- Pipeline Register

Instruction Register

The Instruction Register is a clocked latch used to store the firmware instruction opcode. The opcode is latched into the register at the rise of FRCLK-1 from the MCP Board. The opcode is supplied by the FRA0 thru FRA7 lines (MB8 thru MB15 are the same lines). The output of the Instruction Register is used by the Fetch Control ROM and the Sequence Instruction Branch.

Fetch Control

The Fetch Control is a ROM addressed by the output of the Instruction Register. The ROM decodes the firmware instruction opcode for use by the MCP Board during the instruction execution. The WONFI-0 and WONFO-0 are used by the Wait Control to delay the ALU Board operation during certain firmware instructions.

Sequence Instruction Branch

The Sequence Instruction Branch is a tri-state buffer used as a source of a Micro ROM address for the Micro ROM Sequencer. The Micro ROM starting address for a firmware instruction is X '3XX', where "XX" is the hexadecimal value of the firmware opcode. The NEXT-0 control line from the Micro Sequencer Branch Control enables output of the buffer when the firmware instruction is to be executed.

Sequence Micro ROM Branch

The Sequence Micro ROM Branch is a tri-state buffer used as a source of a Micro ROM address for the Micro ROM Sequencer. The address comes from the Pipeline Register (latched Micro ROM output). This allows the Micro ROM to supply the next Micro ROM address. The LSABR-0 control line from the Micro Sequence Branch Control enables the output of the buffer when the Micro ROM branch is taken.

Interrupt Generator

The Interrupt Generator uses four interrupt input lines. The order of interrupt line priority from highest to lowest is HWDFAIL-0, NMI-0, IRQ-0, AND DSPINT-0. The HWDFAIL-0 and NMI-0 interrupt lines are latched if there is a transition of a high to a low state. The interrupt is not lost during execution of a firmware instruction. IRQ-0 and DSPINT-0 are lost if they are not low when CPCLK-1 goes high. IRQ-0 and DSPINT-0 are maskable interrupts. When the Condition Code Register bit CCRI-1 is high, IRQ-0 and DSPINT-0 are disabled. They can not produce an interrupt until CCRI-1 goes low.

CPCLK-1 goes high at the start of each micro instruction cycle latching all active interrupts into the storage latch (U62). If an interrupt was latched, INTREQ-1 goes high. INTREQ-1 is used by the Micro Sequence Branch Control for interrupt branching at the end of a firmware instruction. INTREQ-1 is also used to prevent the MCP Board from fetching the next firmware instruction.

Interrupts are honored at the end of each firmware instruction. If there is no interrupt, the MCP Board fetches the next firmware instruction to be executed. If there is an interrupt, the Interrupt Generator supplies a Micro ROM address to the Micro ROM Sequencer. The Micro ROM address is enabled by LSAVEC-0 from the Micro Sequence Branch Control.

Micro Sequence Branch Control

The Micro Sequence Branch Control supplies control lines for the Micro ROM Sequencer, selects the active inputs for conditional branching, controls which micro code address is active to the Micro ROM Sequencer, and controls the Micro ROM constant to the RALU.

The Micro Sequence Branch Control consists of a ROM (U235), a counter (U175), two data selectors (U100 and U108), and a decoder (U185). The ROM is addressed by Field 7 Micro ROM Sequence control (SEQ0 thru SEQ3) and by the branch true line (BRANCH-1). DO1 thru DO4 of the ROM controls the Micro ROM Sequencer. DO5 of the ROM controls the loading of data from the RALU (ALUOUT0 thru ALUOUT3) into the counter. The counter is used for Micro ROM instruction looping. DO6 of the ROM controls when the counter increments. DO7 and DO8 of the ROM addresses one-half of the decoder. The output of the decoder determines where the next Micro ROM branch address is from: Sequence Instruction Branch (NEXT-0); Sequence Micro ROM Branch (LSABR-0); or Interrupt Generator (LSAVEC-0). The other half of the decoder is addressed by BRMUX0-1 and BRMUX1-1 from the Micro ROM instruction and enabled by the inverse of LMODE-1. The output of the decoder is used for the loading (LCNST-0) of a constant from the Micro ROM or transferring (TPA-0) the Condition Code Register to the RALU. The two data selectors are addressed by BRMUX0-1 thru BRMUX5-0 from the Micro ROM instruction. The data lines supply the conditions to be selected. The outputs of the two data selectors are OR-ed together (U110A) and EX-OR-ed (U165B) with BROT-0 from the Micro ROM instruction. When BROT-0 is low, the selected condition is not inverted. When BROT-0 is high, the selected condition is inverted.

Micro ROM Sequencer

The Micro ROM Sequencer addresses to the Micro ROM. On power up, the SEQZER-0 line goes low. The Micro ROM Sequencer outputs an address of all zeros. The Micro ROM starts a system check from this address. During the power up check, the Micro ROM address is supplied by either the sequencers internal counter or by the BRA0 thru BRA11 lines from the Sequence Micro ROM Branch. When the power up sequence is finished, the Micro ROM Sequencer also gets addresses from the Sequence Instruction Branch (firmware instruction execution) and the Interrupt Generator (system interrupt acknowledge).

Micro ROM

The Micro ROM contains all the micro instructions for power up and firmware instruction execution. The Micro ROM contains 1K words of 56 bits per word. For explanation of the Micro ROM output refer to the Micro Code part of Section 6 of this manual.

The Micro ROM address is supplied by the Micro ROM Sequencer. The output of the Micro ROM is latched into the Pipeline Register. Two output lines UROM39-1 and UROM55-1 are used by the Wait Control.

Pipeline Register

The Pipeline Register stores the Micro ROM data while it is being used by the processor. Storage of the micro instruction allows the Micro ROM to be addressed for the next Micro ROM output before the present micro instruction is finished.

At reset the SEQ0 thru SEQ3 section of the Pipeline Register is cleared by CPINIT-0 to ensure no false control of the Micro ROM Sequencer. The Micro ROM data is latched on the rise of CPCLK-1 during each micro instruction cycle.

RALU Constant Load

The RALU Constant Load is a buffer that allows the transfer of 16 bits of data from the Micro ROM instruction to the ALUIN0 thru ALUIN15 lines. The buffers are enabled when LCNST-0 is low. The data comes from the Pipeline Register lines (AES0 thru AES2 and PLR43 thru PLR55).

RALU

The RALU consists of four 2901-type, 4-bit slices and a carry look-ahead generator. The RALU Block Diagram (Figure 7-2) shows the flow of data within the 2901s and the relationship of the RALU to the Shift Control and the Condition Code Set-up and Register. The control of the RALU is from the Micro ROM instruction (AECI0 thru AECI8, AECA0 thru AECA3, and AECB0 thru AECB3). Refer to the micro code description in Section 6 for the internal operation control.

Data to the RALU is on the ALUIN0 thru ALUIN15 lines and data out is on the ALUOUT0 thru ALUOUT15 lines. Both 8-bit and 16-bit conditions are supplied to the Condition Code Set-up and Register.

Shift Control

The Shift Control is controlled by AECI7, CRYC0 thru CRYC1 and AES0 thru AES2 from the Micro ROM instruction. The Shift Control selects the lines that are active during shifts. The Shift Control selects the carry input to the RALU ("0", "1", CCRC-1, and CCRC-1 inverted).

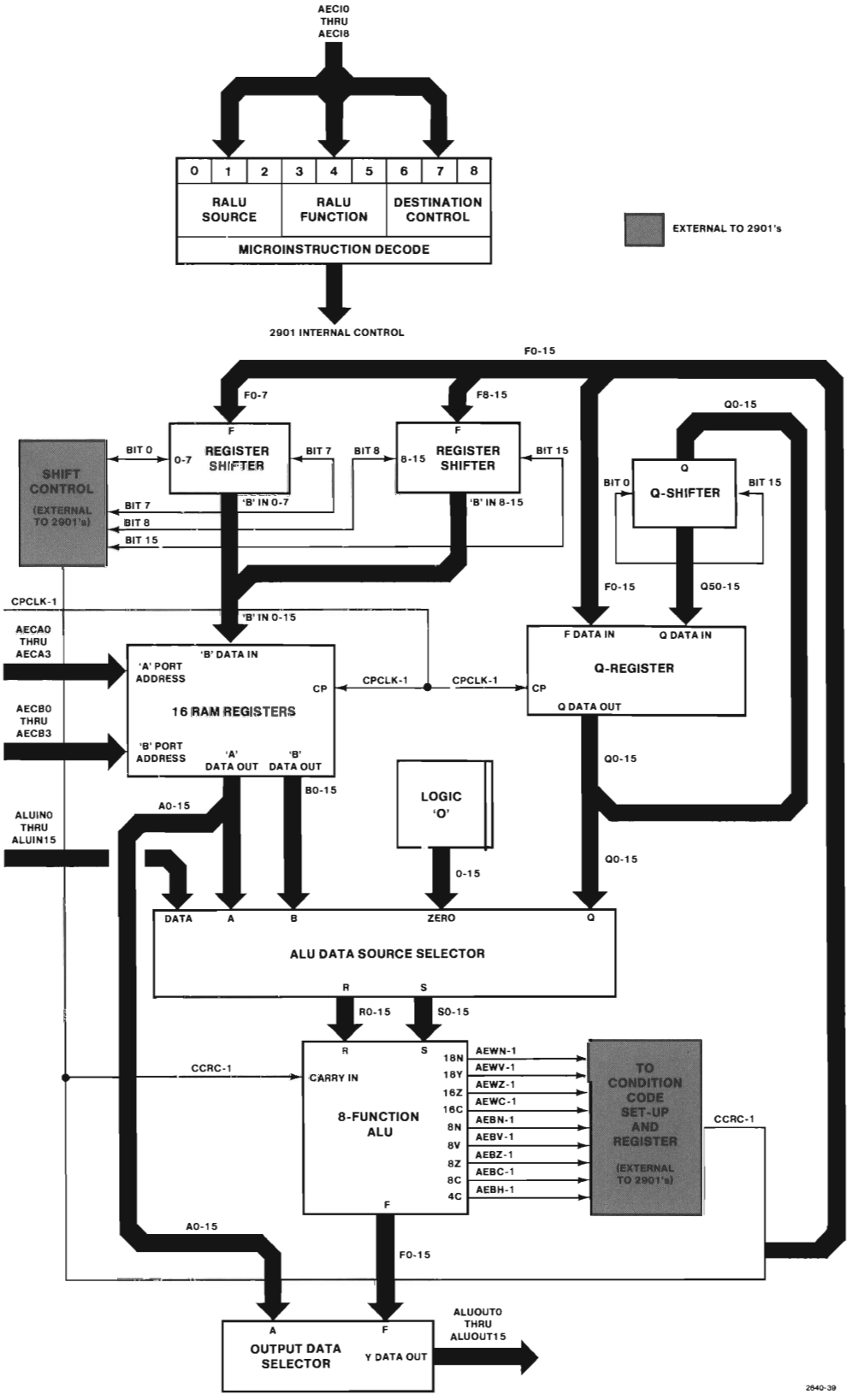


Figure 7-2. RALU Block Diagram.

Condition Code Set-up and Register

The Condition Code Set-up selects the conditions that change the Condition Code Register. Two ROMs (U170 and U172) are addressed by the Micro ROM instruction (CCC0 thru CCC4). The outputs of the ROMs address data selectors, one selector for each bit of the Condition Code Register. The CCRD and CCRF selectors are addressed directly by the CCC0 thru CCC4 lines. The selected conditions are latched into the Condition Code Register (U385) at the rise of CPCLK-1.

The contents of the Condition Code Register are transferred to the RALU when TPA-0 is low. The output of the Condition Code Register also is used by the Micro Instruction Branch Control and the Interrupt Generator.

Clocks

The original version of the ALU Board uses a discrete clock circuit built from two transistors, associated passive components and TTL buffers. This circuit has been replaced on later boards by a hybrid oscillator which performs the same function.

The system clock is a 49.152 MHz clock (approximately 20 ns) divided by two by U15A (Figure 7-3). The 25 MHz (40 ns) clock is the main clock used by the 4052/4054 system. The 25MHz clock is divided by 10 (U20) to supply communications clocking on the I/O Board and the communications backpack.

The ALU Board cycle starts on the first rise of U15A-5 after the rise of U117B-6. The flip-flop timing in Figure 7-3 follows the states and holds in the initial state until U117B-6 goes high again. U117B-6 goes high on reset, when the MCP Board is finished, or when an ALU Board only operation is finished. CPUCLK-1 and CPCLK-1 go high at the fall of U25B-9 and fall when the data from the RALU is ready and stable.

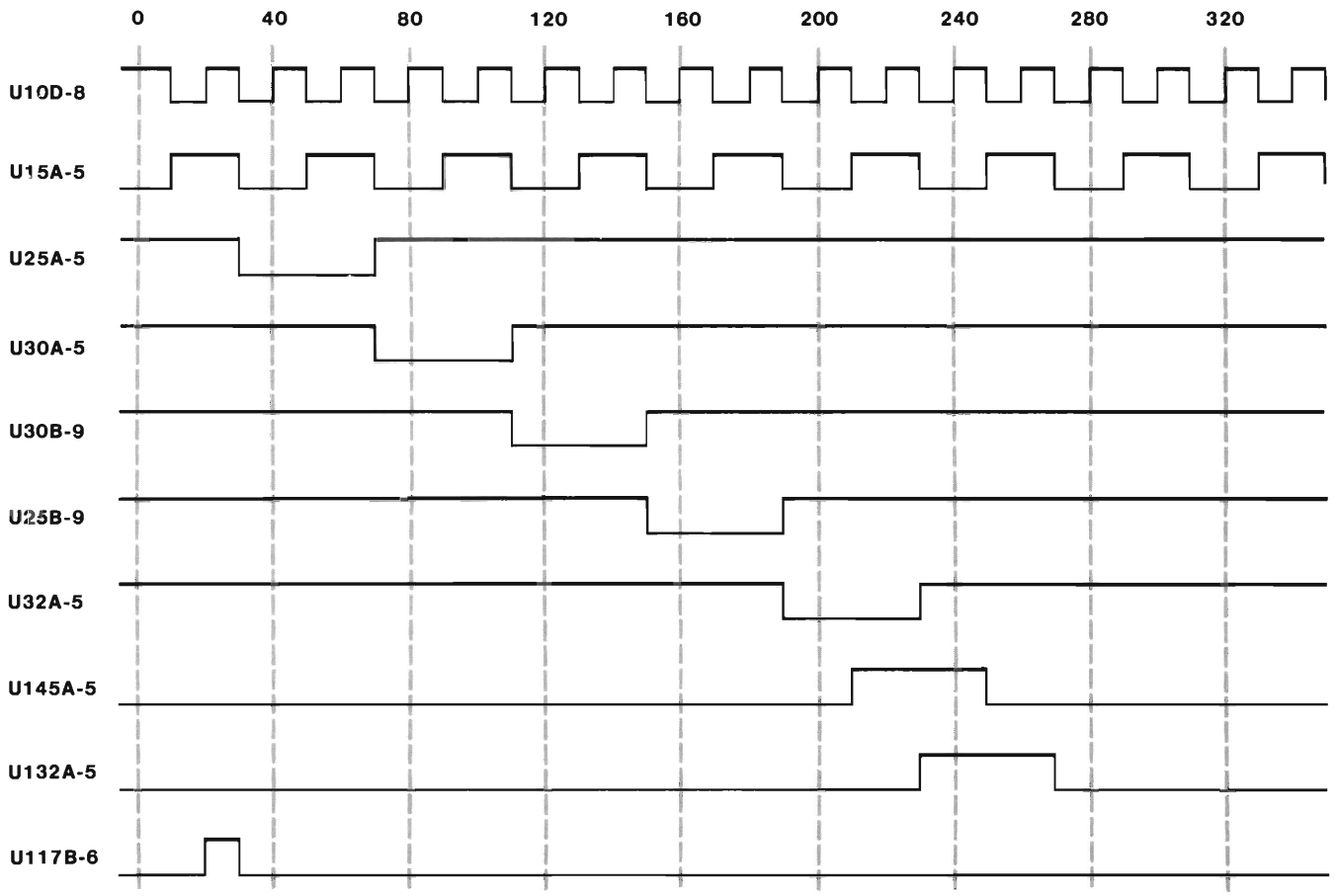


Figure 7-3. ALU Timing-Clocks.

Memory Control Handshake

The Memory Control Handshake controls the data and address transfer between the ALU Board and the MCP Board. During a fetch of the firmware opcode, FRCLK-1 goes high. FRCLK-1 latches the opcode into the Instruction Register and clocks U60A, sending FRBSY-1 high. FRBSY-1 stays high until the opcode has been decoded. FRCLR-1 goes high during a fetch cycle when U30A-5 goes low and goes low when U30A-5 goes high. FRCLR-1 indicates to the MCP Board that the ALU Board has accepted the firmware instruction opcode. PLRDY-0 outputs a high pulse starting when CPUCLK-1 goes high. On the fall of PLRDY-0, the Pipeline Register lines are stable to the MCP Board. When data is requested by the ALU Board, the ALU Board cycle holds until MCPDAV-1 goes high. When data is sent to the MCP Board, the ALU Board holds until ALUACPT-1 goes high.

Wait Control

The Wait Control decodes the operation of the ALU Board and sets up wait controls. The Wait Control is used during firmware instruction opcode fetching and data transfer between the ALU Board and the MCP Board. When waiting for data from the MCP Board, CPUCLK-1 is held high until MCPDAV-1 goes high. When data is transferred to the MCP Board, the ALU Board pauses with CPUCLK-1 low until ALUACPT-1 goes high. The Wait Control supplies the SEQZER-0 signal to start the power up sequence of the micro code.

MCP BOARD

The MCP Board (Figure 7-4) controls the data and address between the ALU Board and the MAS Board. The MCP Board contains the Program Counter used during execution of firmware instructions. The MCP Board contains the following blocks:

- Aluin Latch
- Aluout Latch

- Memory Byte Latch
- High Zero/Sign Extended
- Program Counter
- Request Generator
- MAS Control
- Timing
- ALU Handshake
- Instruction Decode
- Mbus Enable

Aluin Latch

The Aluin Latch consists of 16 D-type latches (U451 and U551) used to hold the data from the MB0 thru MB15 lines. The data from the Aluin Latch to the ALU Board is on the ALUIN0 thru ALUIN15 lines. The data is latched when ALUINHI-1 and ALUINLO-1 goes high. ALUINHI-1 clocks the upper byte (MB8 thru MB15) into the latch (U451). ALUINLO-1 clocks the low byte (MB0 thru MB7) into the latch (U551). The data output is controlled by LMODE-0 from the ALU Board micro instruction. When LMODE-0 is high the Aluin Latch is active on the ALUIN0 thru ALUIN15 lines.

Aluout Latch

The Aluout Latch consists of 16 D-type latches (U441 and U541) used to hold the data from the ALUOUT0 thru ALUOUT15 lines. The Aluout Latch output is to the MB0 thru MB15 lines. The data is latched when CPUCLK-0 goes high. The data is enabled to the MB0 thru MB15 lines when ALUOUT-0 is low.

Memory Byte Latch

The Memory Byte Latch is used during firmware instruction opcode fetch operations. The lower byte (MB0 thru MB7) is stored in the latch (U515) and the upper byte (MB8 thru MB15) is stored in the Instruction Register on the ALU Board. MB8 thru MB15 are the same lines as FRA0 thru FRA7. The data is stored in the latch when MBLIN-1 goes high. The data is enabled to the MB0 thru MB7 lines when MBLOUT-0 is low.

High Zero/Sign Extended

The High Zero/Sign Extended has two functions: it supplies a high byte of all zeros or all ones during +/- offset addressing (relative), and it supplies a high byte of all zeros during one-byte data transfer.

During a fetch operation the upper bit (MB7-1) stored in the Memory Byte Latch is clocked into a D-type latch (U681A) by MBLIN-1 going high. The D-type latch is cleared if the data in the Memory Byte Latch is to be used for 8-bit immediate, a direct address, or 8-bit data from the MAS Board to the ALU Board. The output of the D-type latch (U681A-5) is supplied to all eight inputs of a buffer (U415). The buffer output is enabled by ZEROOUT-0.

Program Counter

The Program Counter consists of a 16-bit counter (U425, U435, U525, and U535), output buffer (U421 and U521), and load-increment timing logic. The Program Counter supplies the firmware instruction address.

To load the Program Counter, LDPC-1 goes high, clocking a D-type filp-flop (U635A). The Q-not output of the flip-flop (U635A-6) enables the load line to the counter. The delay produced by the next D-type flip-flop (U635B) allows the data and load lines to settle. The last D-type flip-flop (U625A) is used to clock the counter and clear U635A.

The Program Counter is incremented by one or by two. The same configuration of flip-flops used for loading the counter is used to increment the counter. The increment-by-two flip-flop set has the last two flip-flops repeated to get the second increment pulse. The increment-by- one flip-flops are started by the INCPC/1-1 line. The increment-by-two flip-flops are started by the INCPC/2-1 line. At the time the counter is being clocked the PCBUSY-0 line is low.

The load data to the counter is from the MB0 thru MB15 lines. The counter output to the MB0 thru MB15 lines is enabled by the PCOUT-0 line to the buffers (U421 and U521).

Request Generator

The Request Generator generates three types of requests: a fetch request (FREQ-1 is high); an implied request (IMPREQ-1 is high); and pipeline request (PLREQ-0 is low). A fetch request is when a firmware instruction opcode is being fetched from the MAS Board or the backpacks. An implied request is used for two and three-byte firmware instructions. An implied request follows the firmware instruction fetch and enables the MCP Board to process the additional firmware instruction bytes (immediate, direct, extended, or relative addressing). A pipeline request provides a means by which the ALU Board has control of the MAS Board from the micro code (PLMC0 thru PLMC2) for power-up and firmware instructions that require more than an implied request.

MAS Control

The MAS Control supplies the handshaking between the MCP Board and the MAS Board. When an address is available on the MB0 thru MB15 lines, ADDRVALID-0 is low. When write data is available on the MB0 thru MB15 lines, DATAVALID-0 is low. When the address has been accepted by the MAS Board, ADRACPT-0 goes low and ADDRVALID-0 goes high. Data between the MAS Board and the MCP Board is confirmed by DCNFRM-0 going low. During a memory read operation, DCNFRM-0 going low indicates that the data is available from the MAS Board on the MB0 thru MB15 lines. During a memory write operation, DCNFRM-0 going low indicates that the data has been received by the MAS Board.

Timing

The Timing block is used for the MCP Board cycles and buffers the system clock (25MHZ-1, MCP40NSCLK-1, and M40NSCLK-1) on the MCP Board and to the MAS Board.

ALU Handshake

The ALU Handshake tells the ALU Board that the data from the ALU Board has been accepted by the MCP Board (ALUACPT-1 goes high).

Instruction Decode

The Instruction Decode takes the three request types (fetch request - FREQ-1 high; implied request - IMPLREQ-1 high; and pipeline request - PLREQ-0 low) and decodes the type of operation the MCP Board is to execute for the selected request.

The active output lines depend on which request is active. Only one type of request can be active at any one time. Most of the outputs are used by the Mbus Enable block to control data and address transfer on the MB0 thru MB15 lines.

Mbus Enable

The Mbus Enable decodes the outputs of the Instruction Decode to control the buffers and registers that are connected to the MB0 thru MB15 lines. PCOUT-0 enables the output of the Program Counter to the MB0 thru MB15 lines. MBLOUT-0 enables the Memory Byte Latch to the MB0 thru MB7 lines. ZEROOUT-0 enables the High Zero/Sign Extended to the MB8 thru MB15 lines. ALUOUTEN-0 enables the Aluout Latch to the MB0 thru MB15 lines. The MSPACE-1 output is the control line to the MAS Board. MSPACE-1 indicates the memory space (RAM or ROM) the MAS Board uses for the memory operation. If MSPACE-1 is high, RAM space is used. If MSPACE-1 is low, ROM space is used (see Figure 7-5).

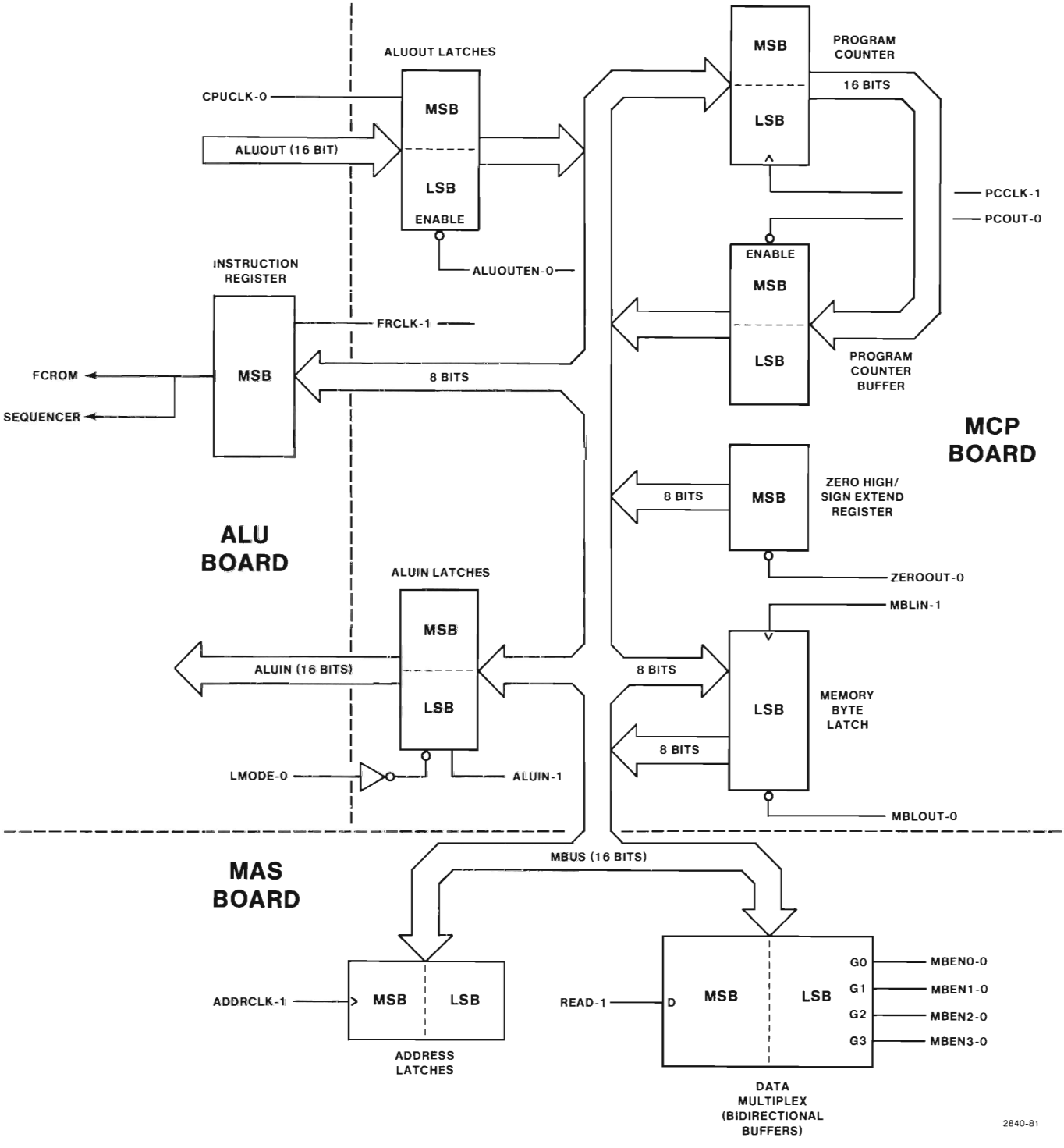


Figure 7-5. MBUS Block Diagram.

MAS BOARD

A different MAS Board is used in the 4052A and 4054A. The "A" series MAS board differs from the older MAS Board in several ways:

- The mask programmed ROMs, Patch FPLAs, and Patch ROM used on the older MAS Board are replaced by 2764 type EPROMS.
- An internal bank select register and associated timing circuitry has been added.
- Two additional EPROMs (selected by the new internal bank select register) add firmware space.

The MAS Board (Figure 7-6, foldcut) contains the RAM and ROM memory, memory addressing, address decode, and data transfer control (transfer between the MCP Board and the I/O Board and backpacks [external address and data space]). The MAS Board contains the following functional blocks:

- Data Bus
- Address Bus
- External Address Decode
- External Address Buffer
- Parity Generating and Checking
- Parity Error Latch
- RAM Control
- RAM Arrays (Odd and Even)
- ROM Control
- ROM Arrays (Odd and Even) and Patch FPLAs for the older version board
- Internal Timing Control
- External Timing Control
- Address Decode and Data Control
- Memory Request Sequencer
- Status Control
- Internal Bank Select Register (newer MAS Board only)

Data Bus

The Data Bus provides the data path between the internal data registers and the internal (system ROM and RAM) or external (I/O Board or backpack) memory space. Data direction is controlled by the READ-1 line. When READ-1 is low (memory write) the data is transferred from the MB0 through MB15 to the EDB0 through EDB15 and ODB0 through ODB15 lines. WHen READ-1 is high (read memory) the data goes in the other direction.

The memory spaces are divided into even and odd addressing of data bytes. Data transfer between the MAS Board and the MCP Board is two bytes or one byte (Figure 7-7). When one byte is transferred, MB0 thru MB7 is active with EDB0 thru EDB7 (U195) for even addresses and with ODB0 thru ODB7 (U165) for odd addresses. External one-byte data transfers are between EXD0 thru EXD7 and EDB0 thru EDB7 (U495) for both even and odd external addresses (EDB0 thru EDB7 is active with MB0 thru MB7). During an odd address or an external (even and odd addresses read only, write to external is one-byte only) two-byte data transfer, MB0 thru MB7 is active with EDB0 thru EDB7 (U185); MB8 thru MB15 is active with ODB0 thru ODB7 (U170). The first external byte (EXD0 thru EXD7) is latched in U160 and output to ODB0 thru ODB7. The second external byte is transfered from EXD0 thru EXD7 to EDB0 thru EDB7 (U495). When two bytes of data at an even address are transferred, MB0 thru MB7 is active with ODB0 thru ODB7 (U165) and MB8 thru MB15 is active with EDB0 thru EDB7 (U185). The MBEN0 thru MBEN3 control lines control these data transfers.

The ODB0 thru ODB7 lines are buffered to the odd RAM and ROM (ORB0 thru ORB7) by U270. The EDB0 thru EDB7 lines are buffered to the even RAM and ROM (ERB0 thru ERB7) by U395.

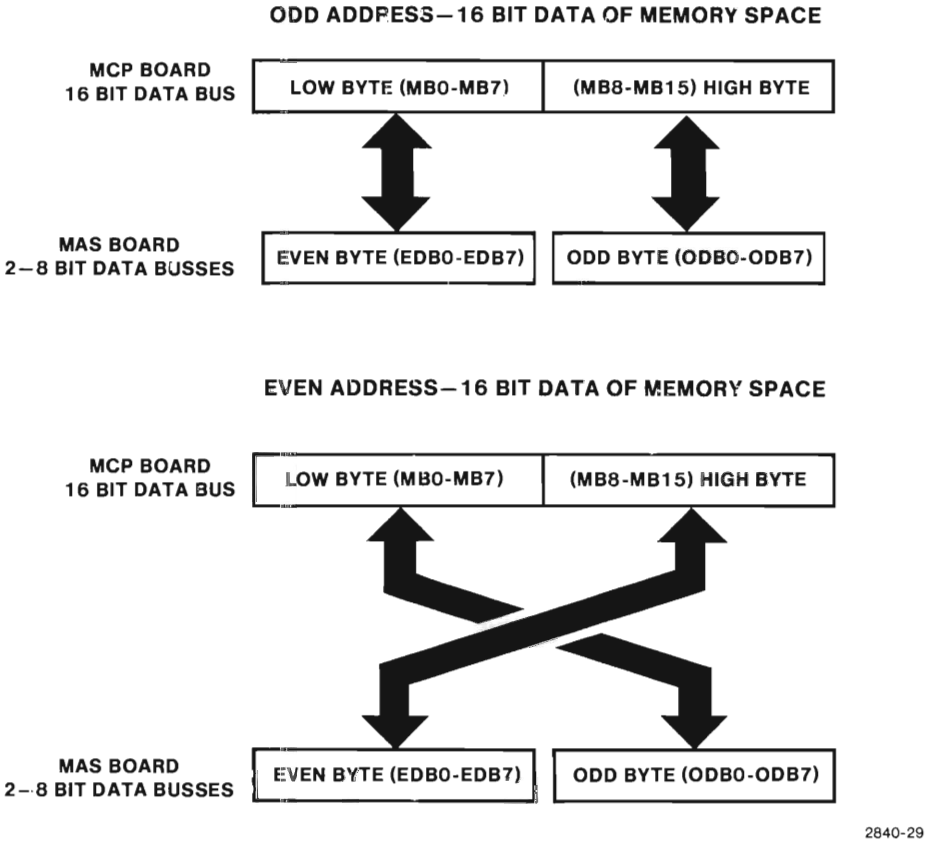


Figure 7-7. Data Byte Transfer.

Address Bus

The Address Bus latches the address from the MCP Board, buffers the destination of the address, and supplies the address counting for dynamic RAM refresh. The address from the MB0 through MB15 lines is latched (via U180 and U190) and supplied to the OAB0 through OAB15 lines.

Internal memory (both ROM and RAM is arranged into two banks, an Odd Bank and and Even Bank. These two banks are addressed by the lines EAB1 through EAB15 (Even Address Bank 1-15) and OAB1 through OAB15 (Odd Address Bank 1-15). An adder consisting of U385, U390, and U480 increments the EAB0 through EAB15 lines for odd word addresses and two-byte external addresses. The input to the adder is from OAB0 through OAB15 and the output of the adder is sent to lines EAB0 through EAB15.

Single Byte Operations

During single byte operations, the addresses present on the EAB1-15 lines and the addresses present on the OAB1-15 lines are identical. Selection of the odd or even memory bank is done by line OAB-0.

Word (Two-byte) Operations

During word or two-byte operations, both banks are addressed regardless of the state of OAB-0. When the first byte of a two-byte operation is located at an even address (on MB0-15), the addresses on the two banks will be the same. However, when the first byte of the two-byte operation is located at an odd address, the EAB1-15 address is the OAB1-15 address incremented by the adder (the value of OAB1-15 + 1).

External Addressing

A two-byte external address is sent to the External Address Buffer on the EAB0-15 lines in two memory cycles. During the first cycle, the address from the latches (U180 and U190) is placed onto the bus and also into the adder. During the second memory cycle, the adder increments the address by one (INCADD-1 goes high).

RAM Refresh Addressing

The dynamic RAM memory is refreshed by periodically cycling through the OAB0-7 lines. A counter (U295) is incremented whenever the line RFSHLATE-1 goes high. The output of the counter is buffered by U290, and whenever RFSHEARLY-0 goes low, the buffered address is placed on the OAB0-7 lines.

Dynamic RAM Addressing

The dynamic RAMs are addressed through buffers U460 and U465 from lines OAB1-14 to lines ORAB1-7 and buffers U430 and U435 from lines EAB1-14 to lines ERAB1-7.

External Address Decode

The External Address Decode enables the external space for access. The MEXT-0 line is low for RAM space address (MSPACE-1 is high) X'FF00' to X'FFFF' and for ROM space address (MSPACE-1 is low) X'0000' to X'3FFF'. The RAM space of external is used for the I/O Board addressing. The ROM space of external is used for the switchable backpack address (16K).

External Address Buffer

The External Address Buffer is enabled at all times. The input to the buffers (U485 and U490) is from the EAB0 thru EAB15 lines. The output is to the AEA0 thru AEA15 lines. The AEA0 thru AEA15 lines address the I/O Board and the backpacks.

Parity Generating and Checking

The Parity Generating and Checking consists of two parity generating intergrated circuits, one for even RAM space (U285) and one for odd RAM space (U260). The data is from the ODB0 thru ODB7 (odd RAM space) and EDB0 thru EDB7 (even RAM space). During a RAM space write, the generators create an even parity output to OPDIN-1 and EPDIN-1 for storage in RAM space. During a read of data, the generators input the data with the parity stored during write and create an output. If there is an error OPARITY-1 or EPARITY-1 goes high.

Parity Error Latch

The Parity Error Latch is used to generate a HWDFAIL-0 interrupt. The conditions required for the interrupt are a read operation of the RAM Array (U345A-3 is high) and either an odd parity error (OPARITY-1 is high) or an even parity error (EPARITY-1 is high). During one-byte memory read, only the RAM space addressed parity is active (odd or even). The LED, DS15, is turned on by a parity error.

RAM Control

The RAM Control does the decoding for one or two-byte access, read/write control, row addressing (RAS) control, and column addressing (CAS) control. WORD-0 controls the one and two-byte memory access. When WORD-0 is low, both even and odd RAM arrays are active (two-byte read/write). When WORD-0 is high, OAB0-1 selects the active RAM array (one-byte read/write). WRITE-1 controls the reading and writing of both RAM arrays. WRITE-1 high is a write operation. Each RAM bank (even and odd) is divided into two 16K-byte sections. EAB15-1 selects the active 16K section of the Even RAM Array. OAB15-1 selects the active 16K section of the Odd RAM Array. Row address select (RAS) is activated for refresh by RFRSHEARLY-0 going low and for memory access by EAB15-1 and OAB15-1. RFRSHEARLY-0 activates all four 16K sections of RAM. Column address select (CASCLK-1) goes high to select the RAMs for read/write addressing.

RAM Arrays (Odd and Even)

The Even RAM Array and the Odd RAM Array functions exactly the same; therefore, only one is described here. Each RAM array is divided into two 16K by 9 bit sections. Eight bits are used for data, and the ninth bit is used for storing the parity. The control and selection is from the RAM Control. The address is supplied in two 7-bit parts from the ERAB1 thru ERAB7 lines. The row address (RAS) input is used for refresh of memory and data access addressing. The row address is latched into the RAMs, and then the column address (CAS) is supplied to the RAMs. Column address is not used for the RAM refresh.

ROM Control

The ROM Control selects the ROMs addressed by the computer system. These may be the Odd ROM array, the Even ROM Array, or in the case of the older boards, the Patch ROMs.

The address decoders, U420 and U470, select the active ROM. The address decoders are enabled by SPACER-1, OBYTE-1, and EBYTE-1 when ROMCLK-0 goes low. CONSTROM-0 selects the constant ROMs.

On the older boards using FPLAs and Patch ROMs, the FPLAs are used to detect patch addresses. The flag outputs (U863-19 and U845-19) are used to disable the address decoders when the FPLAs detect a patch address. The FPLAs supply the byte or bytes at the trap memory address. The FPLAs' flag output also disables the constant ROMs (U810 and U893) to allow patching of constants.

On the newer boards, the ROM Control can be disabled by placing a strap at J419.

The Even ROM Array and Even Patch FPLA, and the Odd ROM Array and Odd Patch FPLA are functionally the same; therefore, only one is described here. The Patch FPLA looks at all addresses. When a memory patch address has been received, the flag output (pin 19) goes low. The FPLA outputs a data byte to the data bus instead of the ROMs. In each ROM array there are four 8K by 8-bit ROMs. Three ROMs are used for firmware instructions, and one is used for constant data. The constant ROM has an address in the lower 8K of RAM space. The patch ROMs are either 512 by 8-bit ROMs or 256 by 8-bit ROMs. The patch ROMs are used for patching large sections of memory and are accessed by instructions executed from the FPLAs.

Internal Timing Control

The Internal Timing Control develops the RAM and ROM timing signals needed for memory access, and provides timing for system handshake signals needed four internal memory operations. The timing is developed by a series of flip-flops. At the beginning of a memory operation, each flip-flop in the series is clocked, in succession, to a logical 1. Then the series is sequentially clocked to a logical 0 until all flip-flops have been zeroed. Combination of the flip-flop's outputs supplies the MAS Board with the signals used to control the Data and Address Busses, the RAM and ROM clocks, and the system handshake signals.

External Timing Control

The External Timing Control supplies the timing signals when an external access is required. When high, the WORD-1 signal sets up the timing for two-byte external access by setting U102A. When U102A is set, it forces the I/O board to complete two cycles by placing the external timing control into a mode which requires two DAX-0 pulses before EXTREQ-0 is removed.

Address Decode and Data Control

The Address Decode and Data Control supplies the selection of memory space (RAM, ROM, constant ROM, or external), the read/write control lines (for the MAS Board and the I/O Board), and the Data Bus buffer selection. The memory select control lines are SPACER-1, RAMADDR-0, CONSTROM-0, and EXT-0. The read/write control lines are R-1/W-0, WRITE-1, and READ-1. The Data Bus buffer lines (MBEN0 thru MBEN3) are supplied from a ROM (U250).

Memory Request Sequencer

The Memory Request Sequencer starts the memory access and controls the dynamic RAM refresh cycles. The MAS Board starts a memory access when ADDRVALID-0 goes low, MINDRECT-0 goes low, or there is a refresh request from U12CB-9. ADDRVALID-0 is the control line used for address from the MCP Board. MINDIRECT-0 is used during an extended addressing mode (the data out of the MAS Board is the address of the next memory access). The control lines used for refresh are RFRSHEARLY (-1 and -0) and RFRSHLATE (-1 and -0).

Status Control

The Status Control latches information to perform the memory accesses. The following information is latched in U225: read/write (MREAD-1 is high for read operations); one or two-byte data (MWORD-1 is high for two bytes); RAM or ROM space (MSPACE-1 is high for RAM space); and external access (MEXT-0 is low for an external access).

External Bank Select (New Board Only)

The External Bank Select is a single bit addressed register which is written to in parallel with the ROM Pack Bank Select Register. When bit six is high, U380B is set. This disables external memory accesses in ROM space and enables EPROMs U863 and U845. When U380B is cleared, normal external memory accesses are again enabled.

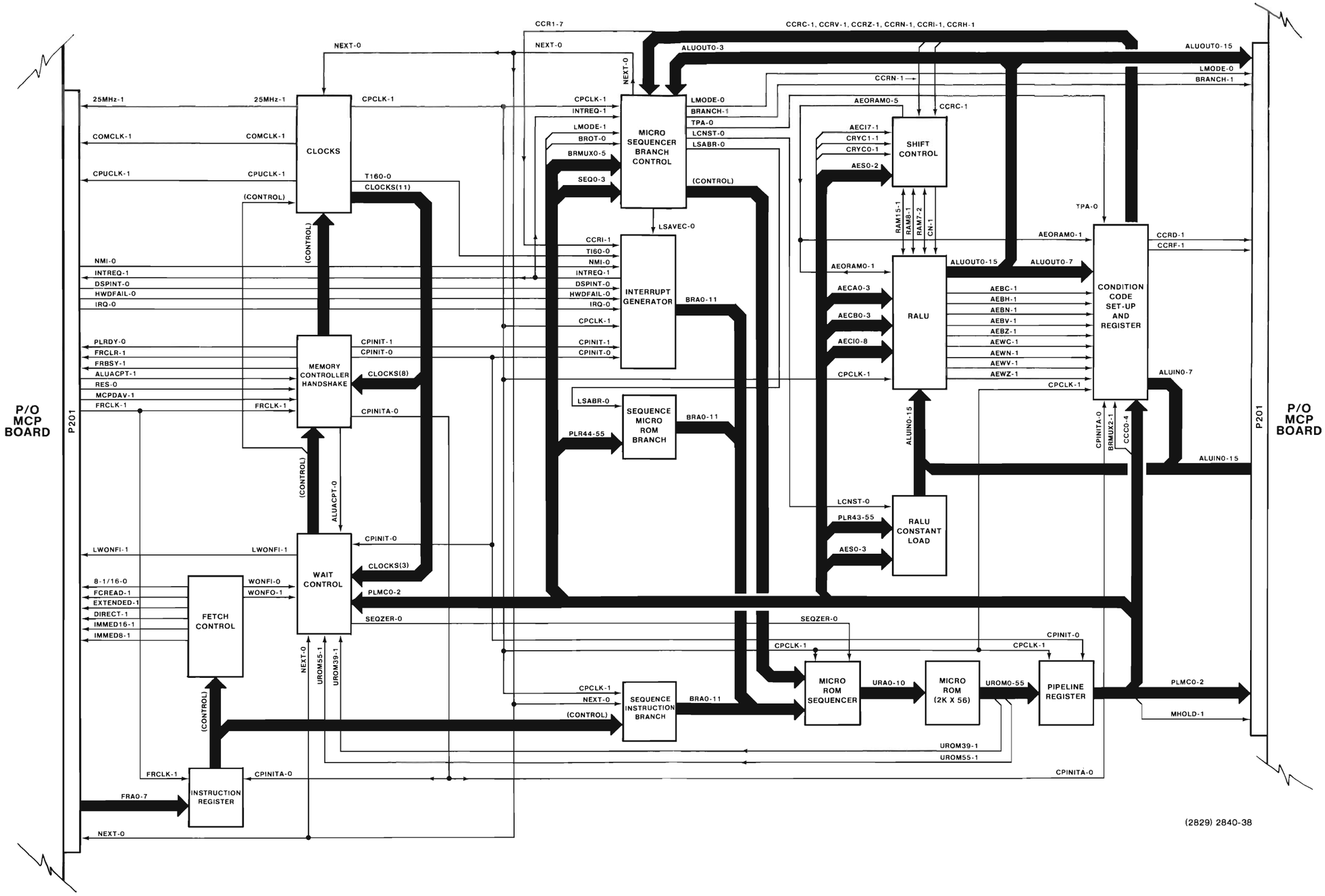
I/O BOARD

The I/O Board contains the following functional areas:

- o I/O Control, Address Decode, and Clocking
- o Magnetic Tape Interface Logic
- o Keyboard Interface Logic
- o Display Interface Logic
- o GPIB Interface

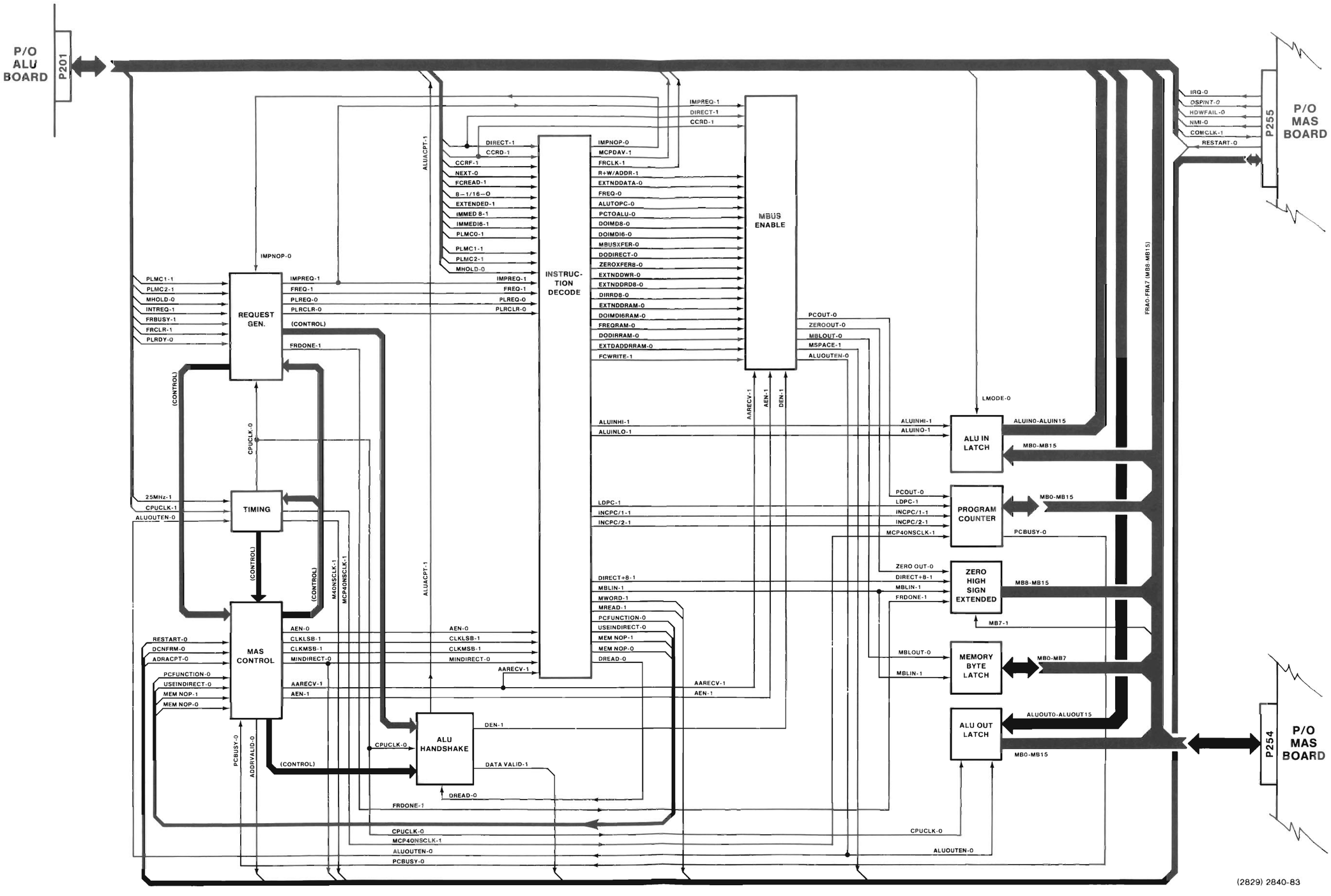
Two versions of the I/O Board exist for the 4052/4052A and two for the the 4054/4054A. They differ in that the newer board has the GPIB control performed by a single integrated circuit.

General interfacing is done through PIAs and discrete logic located on the I/O Board. You should be familiar with the Manufacturer's Data sheets before attempting to diagnose or repair problems involving PIAs or the GPIB Interface circuit.



(2829) 2840-38

Figure 7-1. ALU Block Diagram.



(2829) 2840-83

Figure 7-4. MCP Block Diagram.

MCP BOARD P154
MB0-15
DATA BUS
INTBUF-1
ERB0-7
ORB0-7
EXD0-7
EDB0-7
EXLATCLK-1
MBEN0-3
EXTBUF-1
ODB0-7
READ-1
EXTERNAL ADDRESS BUFFERS
AEA0-15
J5 BACKPACKS
P101 I/O BOARD
ADDRESS BUS
ERAB1-7
ORAB1-7
EAB0-15
OAB0-15
QC-1
QC-0
ADDRCLK-1
RFRSH LATE-1
RFRSH EARLY-1
RFRSH EARLY-0
INCADD-1
EVEN RAM ARRAY
ODD RAM ARRAY
EVEN ROM ARRAY & EVEN PATCH FPLA
ODD ROM ARRAY & ODD PATCH FPLA
(CONTROL)
EPDIN-1
EPDOUT-1
OPDIN-1
SPACER-1
EAB1-15
OAB1-15
EXTREQ-0
OACLK-0
RESTART-0
WORD-1
CLK2-1
EXTERNAL TIMING CONTROL
2NDEXTBYTE-0
WRITE-1
READ-1
EXTERNAL ADDRESS DECODE
MB8-15
MSPACE-1
OAB0-1,13-15
MEXT-0
EAB10-15
OAB10-15
ROM CONTROL
OBYTE-1
EBYTE-1
CONSTROM-0
ROMCLK-0
INTERNAL TIMING CONTROL
CLK1-0
QA-1
QA-0
CLK2-0
RFRSHLATE-0
QB-1
RAMADDR-1
QF-0
QE-1
CASCLK-1
CQ-0
MBEN0-3
EAB15-1
OAB0-1
OAB15-1
QB-1
RFRSHEARLY-0
WORD-0
WRITE-1
RAM CONTROL
ADDRESS DECODE & DATA CONTROL
EXTEN-0
PIAE-1
RAMADDR-0
CONSTROM-0
I/O BOARD P101
MCP BOARD P155
PARITY GENERATING & CHECKING
EDB0-7
ODB0-7
READ-1
EPDOUT-1
OPDOUT-1
EPARITY-1
OPARITY-1
EPDIN-1
OPDIN-1
PARITY ERROR LATCH
HWDFAIL-0
DATA CONFIRM-0
ADDRACPT-0
RESTART-0
DATA VALID-0
MSPACE-1
MREAD-1
MWORD-1
STATUS CONTROL
MINDIRECT-0
ADDRVALID-0
M40NSCLK-1
MEMORY REQUEST SEQUENCER
QE-1
MEMDONE-1
QACLH-0
ADDRCLK-1
RFRSHLATE-1
RFRSHEARLY-1
RFRSHEARLY-0
DATA CONFIRM-0
ADDRACPT-0
40NSCLK-1
CLK1-0
QA-1
QA-0
CLK2-0
RFRSHLATE-0
ROMCLK-0
MYMEM-1
MEMDONE-1
WORD-1
EXT-0
R-1/W-0
J5 BACK PACKS
40NSCLK-1
(2829) 2840-84

Figure 7-6. MAS Block Diagram.

Section 8

KEYBOARD THEORY OF OPERATION

The keyboard allows the operator to put information directly into the Graphic Computing System. Two signals come into the keyboard circuit (Figure 8-1): KBCLK (Keyboard Clock), and KBHALT (Keyboard Halt).

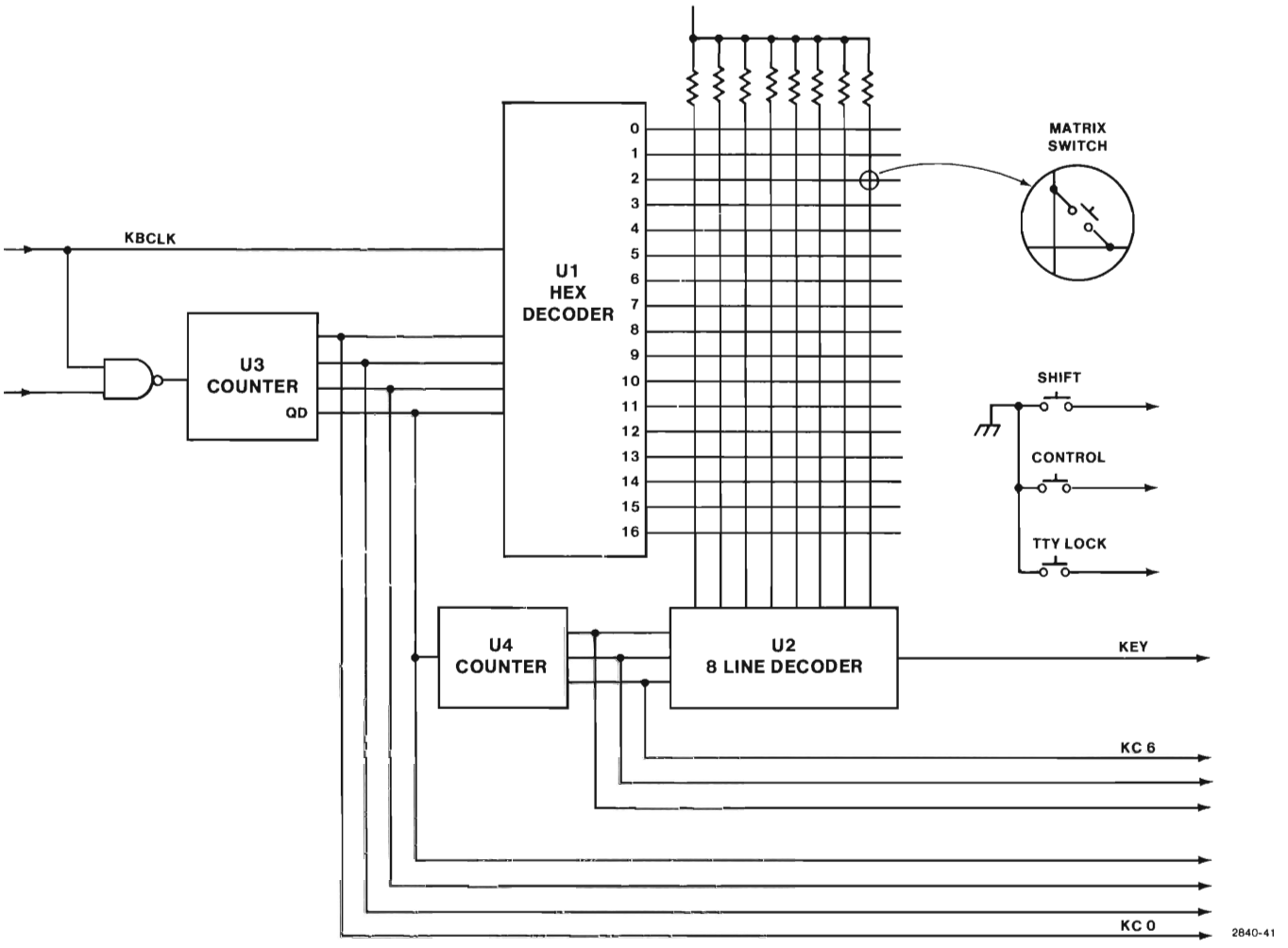


Figure 8-1. Simplified Keyboard Circuitry.

The KBCLK (Keyboard Clock) signal controls the two decoder-multiplexer chips that scan the keyboard lines. When a key is pressed, the decoding PIA on the I/O board detects the output from the keyboard and generates KBHALT. This stops the keyboard scanning until the keyboard position is decoded.

There are two basic outputs from the keyboard to the PIA. One output is seven lines of information, KC0 to KC6, that tell which lines are being scanned. A second output, KEY, tells when a key is pressed.

Three additional keys, SHIFT, CONTROL, and TTY, also go to the PIA to control the output from the PIA.

The KBCLK signal enables a decoder (U1) and also clocks a ripple counter (U3). The ripple counter output turns on one of the sixteen lines from the decoder at a time. After a scan of the sixteen lines has been completed, an output pulse goes from the QD output of the counter(U3) to a second ripple counter, U4. The second counter advances the eight line decoder(U2) to the next line. It requires eight complete scans of the sixteen line decoder to increment the second counter-decoder combination through its complete scan and cover all 128 keys.

When the eight input multiplexer detects a keyboard input, KEY goes high. The decoding PIA on the I/O Board then issues KBHALT which stops KBCLK until the PIA has time to decode the position of the key pushed. After the KBHALT signal terminates, the KBCLK signal starts again, and the key positions are scanned until the next key is pushed.

Section 9

TAPE UNIT THEORY OF OPERATION

The circuitry for the 4052 and the 4054 tape drives are the same, and the same circuit board is used for each. The circuit board contains the tape read/write circuitry and the motor control servo circuitry. Refer to Figure 9-1 for a block diagram of the tape read and write section. The detailed schematic diagram is in the Parts and Schematics Manual.

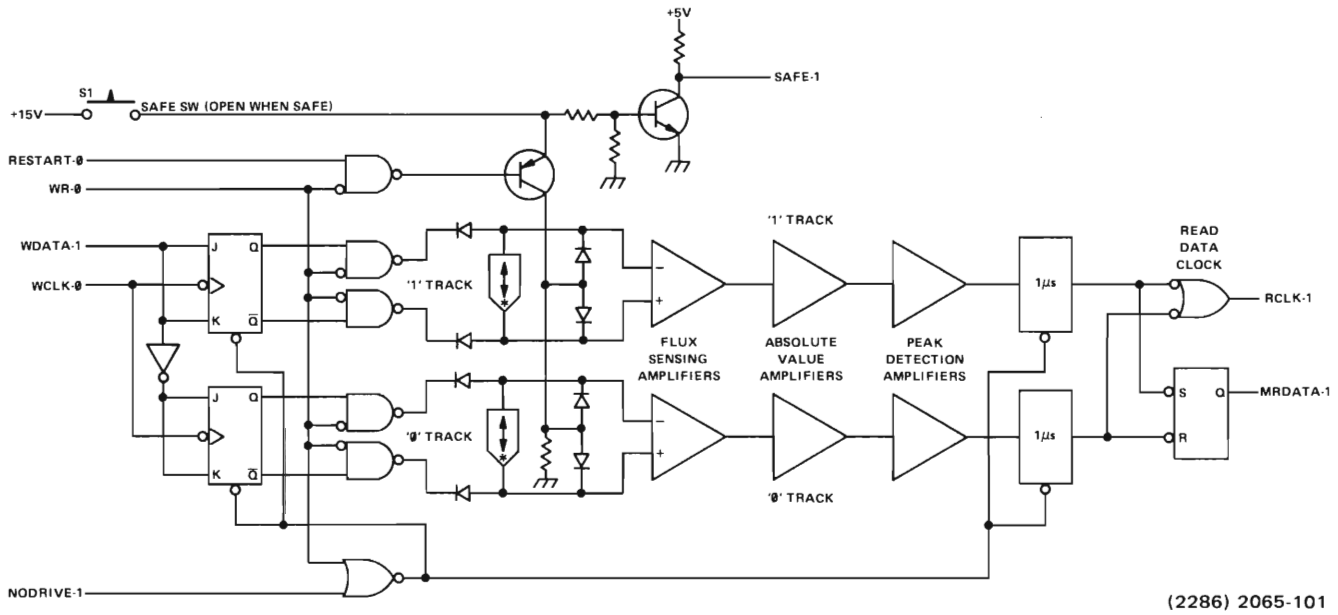


Figure 9-1. Tape Drive Board Read/Write Circuits.

Write operations are performed when the WR-0 line goes low. This causes the diodes on the inputs of the flux-sensing amplifiers to become forward biased. Write current is then forced through the tape heads in a direction determined by the J-K flip-flops and their output gates. A one causes the J-K flip-flop on the number one track to change state, thus forcing a flux reversal on that track. A zero causes the other J-K flip-flop to force a flux reversal on the zero track.

There are two signals that can keep the tape heads from writing. When the SAFE SW signal is low, indicating that the tape is write protected, the tape cannot be written. While the 4052/4054 is being powered up or restarted and RESTART-0 is low, tape data cannot be changed.

Read operations occur when the WR-0 signal is high, causing the writing diodes to have reversed bias. The diodes on the inputs of the flux-sensing amplifiers have their anodes at zero. Flux changes on the magnetic tape cause a voltage to be generated at the tape heads. This voltage is then amplified by the flux-sensing amplifiers and passed through absolute value amplifiers in order to activate the peak detection amplifiers for data detection (Figure 9-2). One microsecond monostable devices are triggered by the output of the peak detection amplifiers. These one microsecond pulses generate a read clock pulse, RCLK-1, each time a flux reversal is encountered on the tape and clock an R-S flip-flop to select the one or zero data bit (MRDATA-1).

Certain conditions prohibit read operations by preventing the one microsecond monostable devices from being triggered. One such condition occurs when there is no command available to cause tape motion. Another occurs when WR-0 is low to perform a write operation.

The peak detection amplifier operation is illustrated in Figure 9-2. The detailed schematic is in the Parts and Schematics Manual. During the positive rise of input voltage, the capacitor charges through R1 as illustrated in part a). When the input voltage starts to drop, the capacitor-charging diode becomes reverse biased. This results in an equivalent circuit as shown in part b). As the input voltage continues to drop, the voltage at the junction of R2 and R3 drops below the stored capacitor voltage. This causes the output voltage to go negative, and the equivalent circuit changes to that shown in part c). The capacitor in part c) discharges through R1 until the input voltage starts to rise. Now the discharge diode becomes reverse biased. The equivalent circuit again becomes that of part b). As the rising input voltage forces the junction of R2 and R3 above the capacitor voltage, the output again goes positive, and the equivalent circuit becomes that of part a). The waveshape at the bottom of the figure illustrates the input and output waveshapes during each part of the cycle.

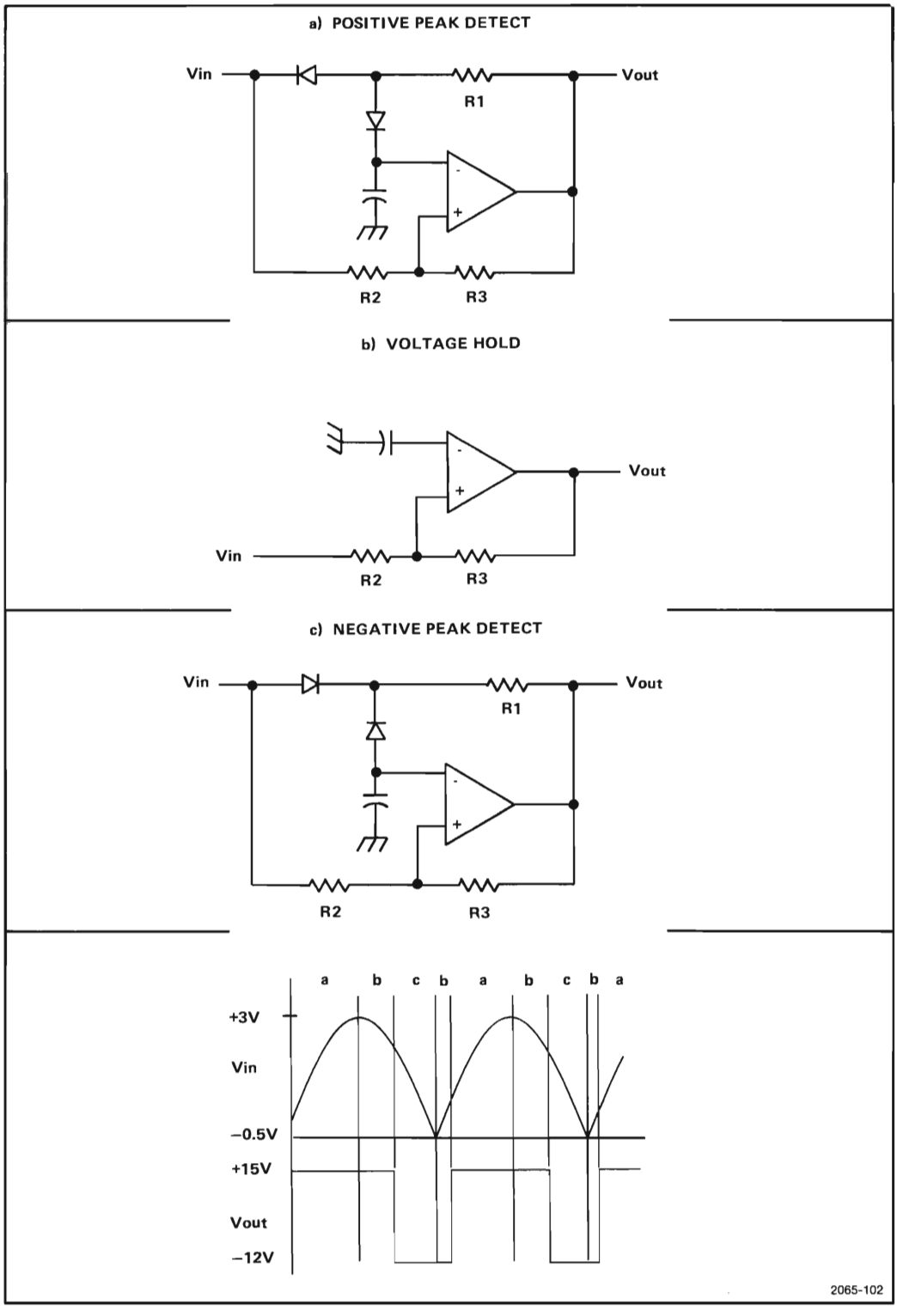


Figure 9-2. Peak Detection Amplifier Operation.

The tape motor control circuitry is shown in Figure 9-3. This circuitry controls motor speed, direction, and emergency stop functions.

The emergency stop circuitry removes the drive enable signal when:

- The tape is in reverse and the beginning of tape is encountered,
- DRTAPE-0 goes high under microprocessor control,
- The tape cartridge is removed, or
- The status lamp burns out.

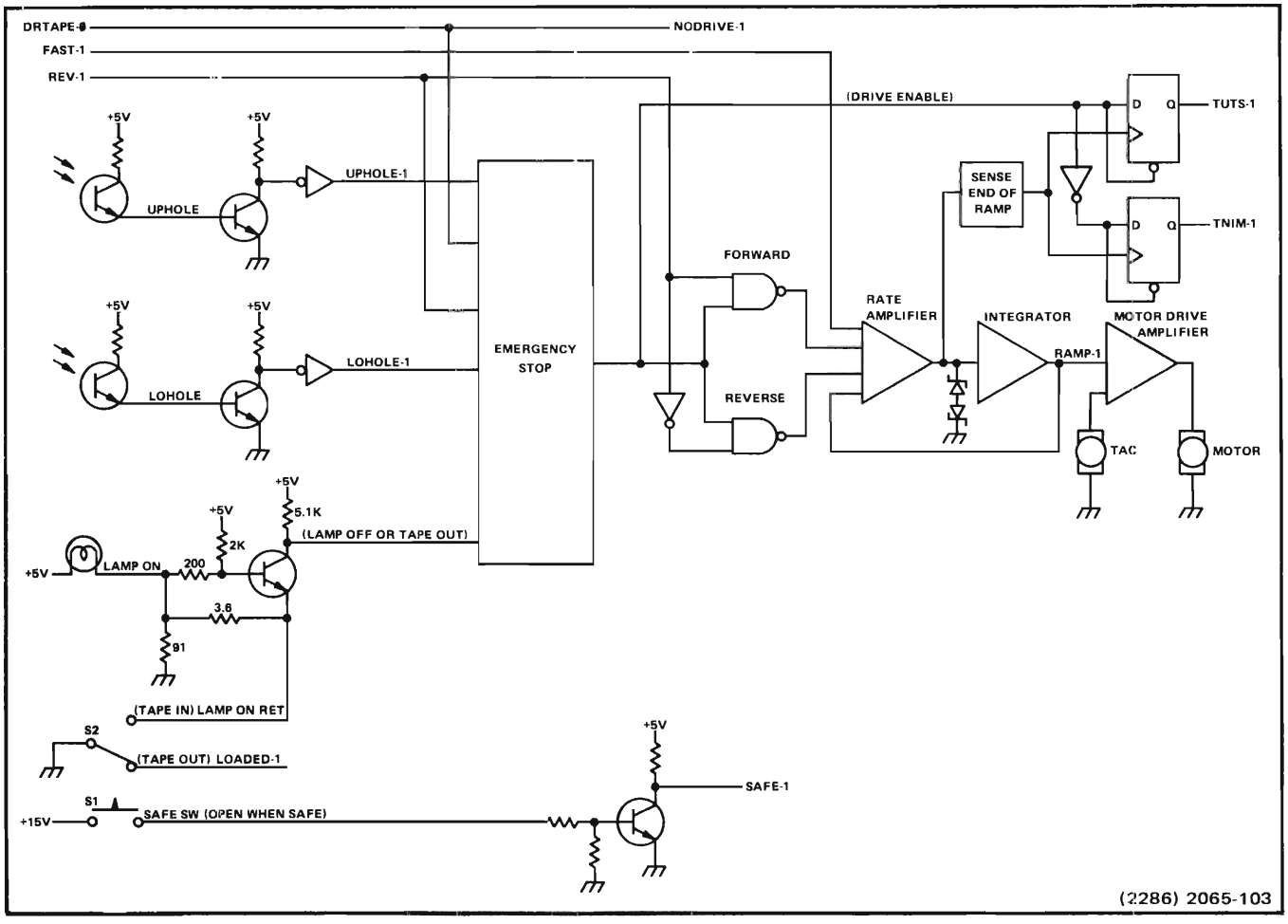


Figure 9-3. Block Diagram of Tape Status and Motor Drive Circuitry.

The rate amplifier controls the motor speed. The tachometer output is compared with a ramp output from the rate amplifier circuitry. The rate amplifier is a saturating amplifier having an output voltage clamped with zener diodes at +8 volts or -8 volts, with a regulated output near zero volts. For ramp generation, the zener-regulated voltages provide a constant input to the integrator until the ramp has reached its excursion limit. Feedback from the integrator forces the rate amplifier to zero when the ramp (motor speed) voltage is reached. RAMP-1 voltage is approximately 1 volt for each 10 inches per second of tape velocity.

The output of the rate amplifier also triggers a 15 millisecond monostable device at the termination of a ramp voltage. This provides a settling delay time before either the tape-up-to-speed (TUTS-1) or tape-not-in-motion (TNIM-1) indication is made true.

The rate amplifier also provides a switch that alters the attenuation of the limiting feedback signal from the integrator. When the FAST-1 signal is false, the FET limit switch is turned off, allowing the RAMP-1 signal to reach voltage levels of +/- 3 volts. When FAST-1 is true, the FET switch conducts and allows the RAMP-1 signal to limit at +/- 9 volts.

The motor drive amplifier circuitry is shown in the Parts and Schematics Manual. This high gain current amplifier uses complementary Darlington transistors to drive a dc motor. The motor uses a tachometer to provide feedback to regulate the motor drive amplifier. Other feedback in the amplifier circuitry limits the maximum gain of the amplifier circuits to stabilize motor speed.

When the tape is stopped, the Zero Motion adjustment is set for no motor drive current.

The Motor Speed adjustment is set to provide normal tape velocity of 30 inches per second.

Table 9-1

MAGTAPE FORMAT SPECIFICATIONS

Characteristic	Symbol	Distance				Time (at 30 ips max.)			
		min.	nom.	max.	units	min.	nom.	max.	units
erase after last file	d_{fe}	0	-	-	in	300	-	-	ms
interfile gap	d_{ff}	3.17	3.60	4.03	in	172	195	218	ms[a]
interrecord gap	d_{rr}	1.06	1.20	1.34	in	57	65	73	ms[b]
read-to-write gap	d_{rw}	4.35	8.18	12.00	mil	145	272	400	μs
first inter-character gap after record data	d_{i}	1.50	-	3.90	mil	50	-	130	μs
intercharacter gap	d_{cc}	1.50	2.25	3.00	mil	50	70	100	μs
normalizing gap, after EOR mark	d_{o}	-	-	3.00	mil	-	-	100	μs
interbit gap	d_{bb}	.57	.65	.73	mil	19	21	24	μs

[a]Speed is not constant at 30 ips during the interfile gap:

[b]Speed is not constant at 30 ips during the interrecord gap:

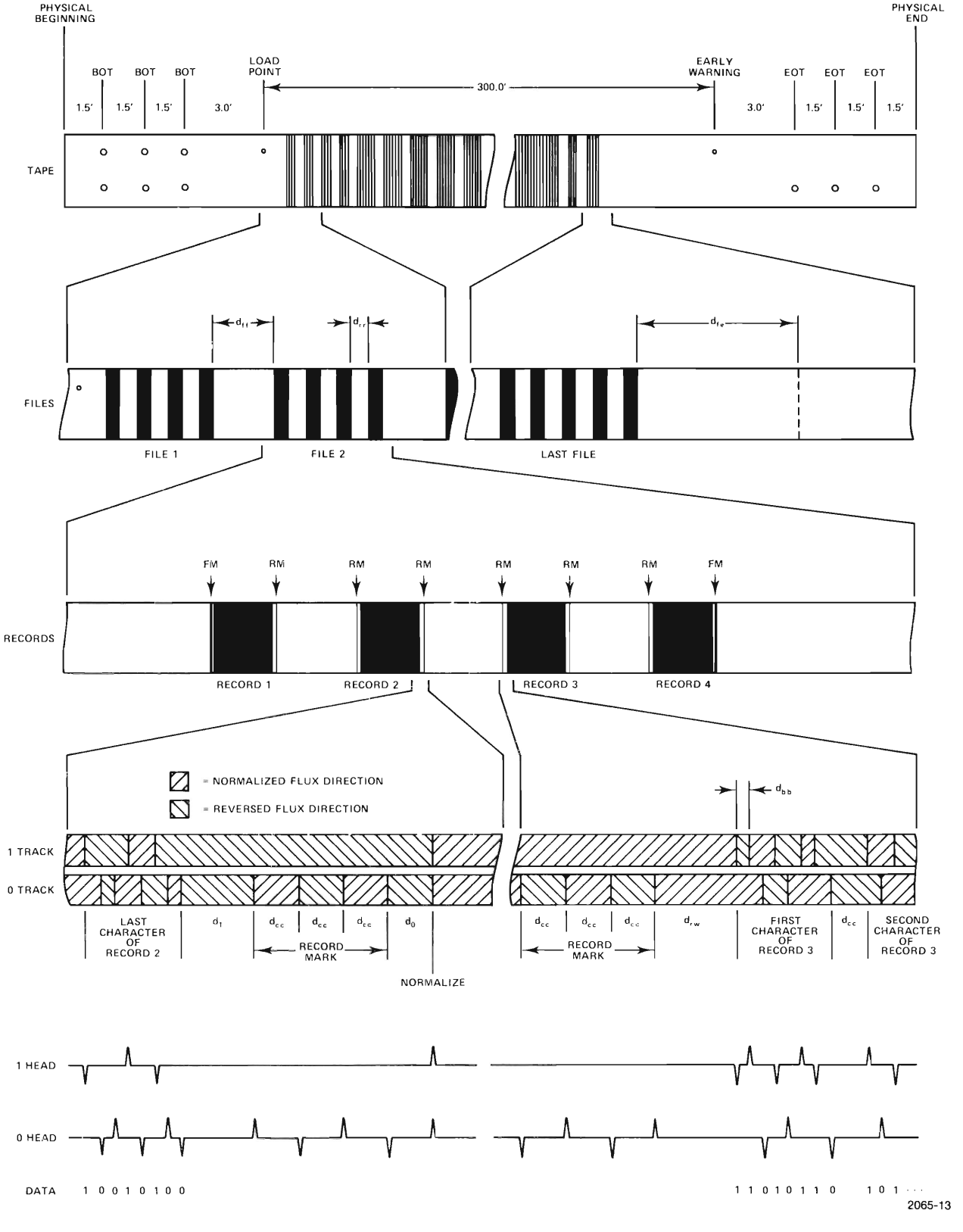


Figure 9-4. Magnetic Tape Recording Format.

Section 10

4052/4054 GENERAL PURPOSE INTERFACE BUS THEORY OF OPERATION (GPIB)

Figure 10-1 is a block diagram of the GPIB (General Purpose Interface Bus) circuitry. The GPIB conforms to the IEEE Standard 488-1975, A Standard Digital Interface For Programmable Instrumentation.

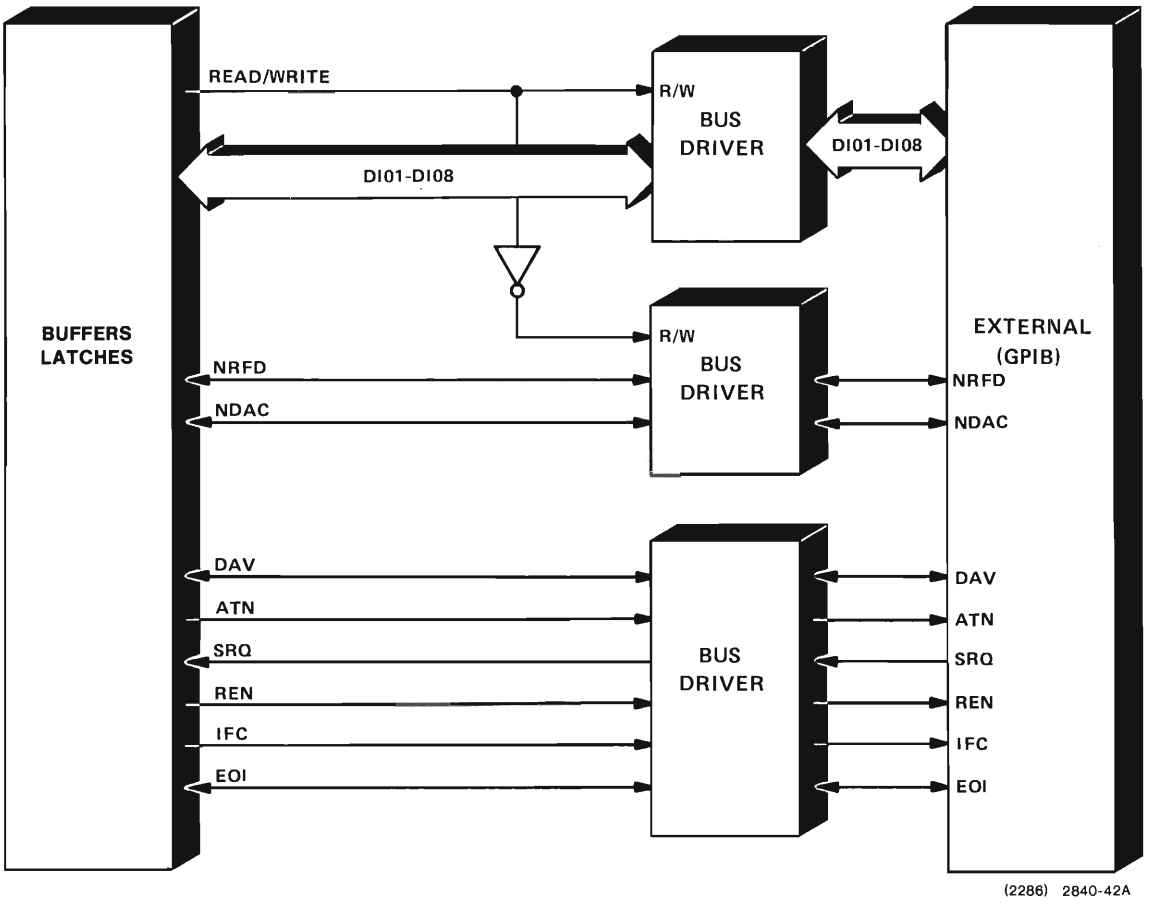


Figure 10-1. GPIB Circuitry Block Diagram.

GPIB READ/WRITE OPERATIONS

The Graphic Computing System must be the primary system controller, therefore other controllers are not allowed on the bus. The Graphic Computing System firmware does not support the following operations:

1. The passing of control between system and task controllers.

2. The ability to request service of another controller.

3. Parallel poll operations.

In the operation of the GPIB the R/W (Read/Write) signal goes true whenever the Graphic Computing System wishes to send data to devices on the GPIB. When the R/W signal is true (Write), data on the data lines can pass to the external data bus through the bus driver circuitry. Data external to the system cannot be received. When the R/W line is true for writing, the receive handshake signals NRFD (Not Ready For Data). Then NDAC (Data Not Accepted) can be read but not activated by the Graphic Computing System.

When the R/W signal is false (Read), data can be recieved through the bus driver circuitry, and the handshake signals NRFD and NDAC can be activated by the Graphic Computing System and read by the talking or transmitting device.

Bus drivers on all other interface lines are constantly enabled to provide signal paths as defined by arrows on Figure 10-1.

THE GPIB CONNECTOR

The GPIB connector is a 24-pin connector located on the rear panel of the 4052/4054 Graphic System main chassis. This connector allows external peripheral devices to be connected to the system. The devices must conform to the IEEE Standard #488-1975 which describes a byte-serial, bit-parallel interface system for programmable instrumentation. The GPIB connector has sixteen active signal lines and eight interlaced grounds. The cable attached to the GPIB connector must be no longer than 20 meters maximum, with a maximum of fifteen peripheral devices attached. The connector pin arrangement and signal line nomenclature is shown in Figure 10-2.

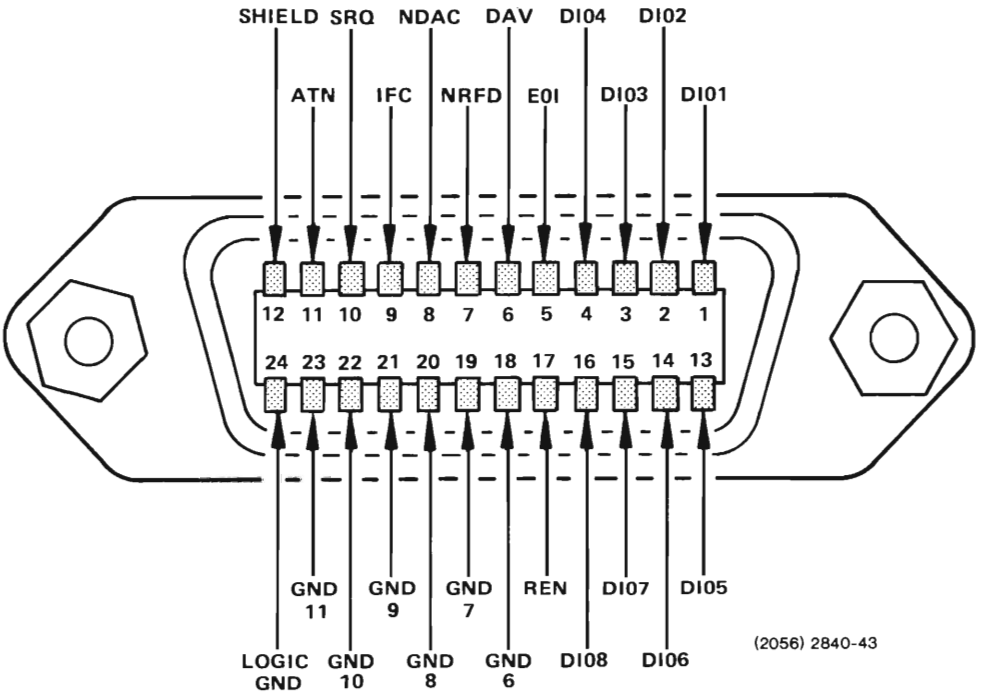


Figure 10-2. GPIB Pin Assignments.

THE GPIB INTERFACING CONCEPT

The GPIB is actually three busses; an eight-line Data Bus, a three-line Transfer Bus and a five-line Management Bus. This bus structure is shown in Figure 10-3.

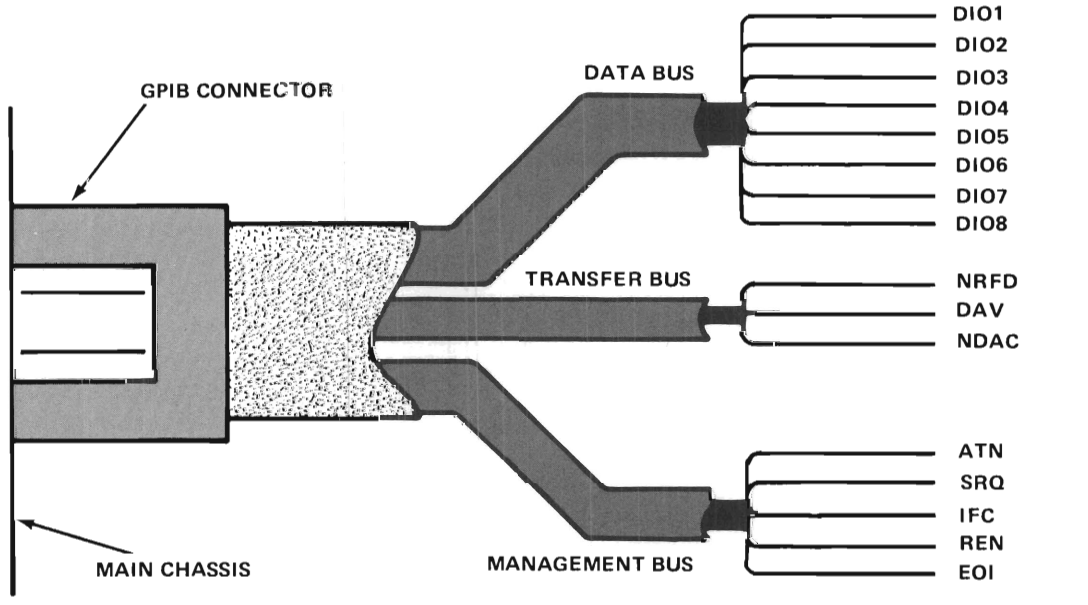


Figure 10-3. GPIB Bus Structure.

The transfer rate over the GPIB is a determined by the slowest peripheral device taking part in a transfer at any one time. The bus operates asynchronously with a maximum transfer rate of one megabyte/second. Both peripheral addresses and data are sent sequentially over the Data Bus. Once peripheral addresses are established for a particular transfer, successive data bytes may be transmitted in a burst for higher effective data rates.

Peripheral devices on the GPIB are designated as talkers and listeners. The 4052/4054 processor acts as the controller to assign peripheral devices on the bus as listeners and talkers. It assumes that it is the only controller on the bus, and it has complete control over the direction of all data transfers. There is no provision for other devices on the GPIB with controller capability to to take turns with the Graphic Computing System as controller-in-charge.

A talker is a device capable of transmitting information on the Data Bus. There can be only one talker at a time. The Graphic Computing System can be the talker when the operator wants it to be.

A listener is a device that receives data on the Data Bus. There may be up to fourteen listeners taking part in an I/O operation at a time. The Graphic Computing System can be a listener any time it elects to do so.

GPIB SIGNAL DEFINITIONS

Data Bus

The Data Bus contains eight bidirectional active-low signal lines, DIO1 through DIO8. One byte of information (eight bits) is transferred over the bus at a time. DIO1 represents the least significant bit in the byte. DIO8 represents the most significant bit in the byte. Each byte represents a peripheral address (either primary or secondary), a control word, a digit in a numeric data item, or a character in an alphanumeric character string. Data bytes can be formatted in ASCII code, with or without parity, or they can be formatted in machine-dependent binary code. See Tables 10-1 and 10-2.

Table 10-1

GPIB PRIMARY DEVICE ADDRESS ASSIGNMENTS

PERIPHERAL DEVICE	PRIMARY LISTEN ADDRESS									PRIMARY TALK ADDRESS								
	DECIMAL VALUE	DIO BUS								DECIMAL VALUE	DIO BUS							
		8	7	6	5	4	3	2	1		8	7	6	5	4	3	2	1
Device 0	32	0	0	1	0	0	0	0	0	64	0	1	0	0	0	0	0	0
Device 1	33	0	0	1	0	0	0	0	1	65	0	1	0	0	0	0	0	1
Device 2	34	0	0	1	0	0	0	1	0	66	0	1	0	0	0	0	1	0
Device 3	35	0	0	1	0	0	0	1	1	67	0	1	0	0	0	0	1	1
Device 4	36	0	0	1	0	0	1	0	0	68	0	1	0	0	0	1	0	0
Device 5	37	0	0	1	0	0	1	0	1	69	0	1	0	0	0	1	0	1
Device 6	39	0	0	1	0	0	1	1	0	70	0	1	0	0	0	1	1	0
Device 7	39	0	0	1	0	0	1	1	1	71	0	1	0	0	0	1	1	1
Device 8	40	0	0	1	0	1	0	0	0	72	0	1	0	0	1	0	0	0
Device 9	41	0	0	1	0	1	0	0	1	73	0	1	0	0	1	0	0	1
Device 10	42	0	0	1	0	1	0	1	0	74	0	1	0	0	1	0	1	0
Device 11	43	0	0	1	0	1	0	1	1	75	0	1	0	0	1	0	1	1
Device 12	44	0	0	1	0	1	1	0	0	76	0	1	0	0	1	1	0	0
Device 13	45	0	0	1	0	1	1	0	1	77	0	1	0	0	1	1	0	1
Device 14	46	0	0	1	0	1	1	1	0	78	0	1	0	0	1	1	1	0
Device 15	47	0	0	1	0	1	1	1	1	79	0	1	0	0	1	1	1	1
Device 16	48	0	0	1	1	0	0	0	0	80	0	1	0	1	0	0	0	0
Device 17	49	0	0	1	1	0	0	0	1	81	0	1	0	1	0	0	0	1
Device 18	50	0	0	1	1	0	0	1	0	82	0	1	0	1	0	0	1	0
Device 19	51	0	0	1	1	0	0	1	1	83	0	1	0	1	0	0	1	1
Device 20	52	0	0	1	1	0	1	0	0	84	0	1	0	1	0	1	0	0
Device 21	53	0	0	1	1	0	1	0	1	85	0	1	0	1	0	1	0	1
Device 22	54	0	0	1	1	0	1	1	0	86	0	1	0	1	0	1	1	0
Device 23	55	0	0	1	1	0	1	1	1	87	0	1	0	1	0	1	1	1
Device 24	56	0	0	1	1	1	0	0	0	88	0	1	0	1	1	0	0	0
Device 25	57	0	0	1	1	1	0	0	1	89	0	1	0	1	1	0	0	1
Device 26	58	0	0	1	1	1	0	1	0	90	0	1	0	1	1	0	1	0
Device 27	59	0	0	1	1	1	0	1	1	91	0	1	0	1	1	0	1	1
Device 28	60	0	0	1	1	1	1	0	0	92	0	1	0	1	1	1	0	0
Device 29	61	0	0	1	1	1	1	0	1	93	0	1	0	1	1	1	0	1
Device 30	62	0	0	1	1	1	1	1	0	94	0	1	0	1	1	1	1	0
UNLISTEN/UNTALK	63	0	0	1	1	1	1	1	1	95	0	1	0	1	1	1	1	1

Table 10-2

GPIB SECONDARY ADDRESS ASSIGNMENTS

Secondary Address	Predefined Meaning	Decimal Value	Data Bus 8	7	6	5	4	3	2	1
0	"STATUS"	96	0	1	1	0	0	0	0	0
1	SAVE	97	0	1	1	0	0	0	0	1
2	CLOSE	98	0	1	1	0	0	0	1	0
3	OPEN	99	0	1	1	0	0	0	1	1
4	OLD/APPEND	100	0	1	1	0	0	1	0	0
5	CREATE	101	0	1	1	0	0	1	0	1
6	TYPE	102	0	1	1	0	0	1	1	0
7	KILL	103	0	1	1	0	0	1	1	1
8	UNIT	104	0	1	1	0	1	0	0	0
9	DIRECTORY	105	0	1	1	0	1	0	0	1
10	COPY	106	0	1	1	0	1	0	1	0
11	RELABEL	107	0	1	1	0	1	0	1	1
12	PRINT	108	0	1	1	0	1	1	0	0
13	INPUT	109	0	1	1	0	1	1	0	1
14	READ	110	0	1	1	0	1	1	1	0
15	WRITE	111	0	1	1	0	1	1	1	1
16	ASSIGN	112	0	1	1	1	0	0	0	0
17	"ALPHASCALE"	113	0	1	1	1	0	0	0	1
18	"ALPHAFONT"	114	0	1	1	1	0	0	1	0
19	LIST/TLIST	115	0	1	1	1	0	0	1	1
20	DRAW/RDRAW	116	0	1	1	1	0	1	0	0
21	MOVE/RMOVE	117	0	1	1	1	0	1	0	1
22	PAGE	118	0	1	1	1	0	1	1	0
23	HOME	119	0	1	1	1	0	1	1	1
24	GIN	120	0	1	1	1	1	0	0	0
25	"ALPHAROTATE"	121	0	1	1	1	1	0	0	1
26	COMMAND	122	0	1	1	1	1	0	1	0
27	FIND	123	0	1	1	1	1	0	1	1
28	MARK	124	0	1	1	1	1	1	0	0
29	SECRET	125	0	1	1	1	1	1	0	1
30	"ERROR"	126	0	1	1	1	1	1	1	0
31	undefined	127	0	1	1	1	1	1	1	1

Management Bus

The Management Bus is a group of five signal lines that are used to control data transfers over the Data Bus. The signal definitions for the Management Bus are as follows:

Signal	Definition
ATTENTION (ATN)	This signal line is activated by the controller when peripheral devices are being assigned as listeners and talkers. Only peripheral addresses and control messages can be transferred over the Data Bus when ATN is active low. After ATN goes high, only those peripheral devices which are assigned as listeners and talkers can take part in the data transfer. The 4052/4054 assumes it is the only source of this signal.
SERVICE REQUEST (SRQ)	Any peripheral device on the GPIB can request the attention of the controller by setting SRQ active low. The controller may respond by setting ATN active high and executing a serial poll to see which device is requesting service. The serial poll is taken when a POLL statement is executed in the BASIC program. After the device requesting service is found, BASIC program control is transferred to a service routine for that device. When the service routine is finished executing, program control returns to the main program. The SRQ signal line is reset to an inactive state when the device requesting service is polled.

Signal	Definition
INTERFACE CLEAR (IFC)	The IFC signal line is activated by the controller when it wants to place all interface circuitry in a predetermined quiescent state. The 4052/4054 assumes that it is the only source of this signal. IFC is activated each time the INIT statement is executed in a BASIC program and each time an error occurs in program execution.
REMOTE ENABLE (REN)	The REN signal line is activated whenever the system is turned on. REN causes all peripheral devices on the GPIB to ignore their front panel controls and operate under remote control via signals and control messages received over the GPIB.
END OR IDENTIFY (EOI)	The EOI signal can be used by the talker to end a data transfer sequence. When the controller is listening and EOI is activated by the talker, the controller assumes that a data byte received is the last byte of the transmission. When the controller is talking, it always activates EOI as the last byte is transferred.

The Transfer Bus

A handshake sequence is executed by the talker and the listeners over the Transfer Bus each time a data byte is transferred over the Data Bus. The Transfer Bus signal lines are defined as follows:

Signal	Definition
NOT READY FOR DATA (NRFD)	An active low NRFD signal line indicates that one or more addressed listeners are not ready to receive the next data byte. When all of the addressed listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. This tells the talker to place the next data byte on the Data Bus.
DATA VALID (DAV)	The DAV signal line is activated by the talker shortly after the talker places a valid data byte on the Data Bus. An active DAV signal tells each listener to capture the data byte presently on the Data Bus. The talker is inhibited from activating DAV when NRFD is active low.
DATA NCT ACCEPTED (NDAC)	The NDAC signal line is held active low by each listener until the listener captures the data byte currently being transmitted over the Data Bus. When all listeners have captured the data byte, NDAC goes inactive high. This tells the talker to take the byte off the Data Bus.

GPIB DATA FORMATS

Any series of bit patterns can be transmitted over the GPIB. This allows both numeric data and alphanumeric data to be transmitted in either ASCII code or machine-dependent binary code.

Transferring ASCII DATA

ASCII data may be transferred from the read/write random access memory to a peripheral device on the GPIB using the PRINT, WBYTE, or WRITE statements. ASCII transfers in the opposite direction are executed using the INPUT statement. ASCII numeric data can be transferred in either standard (free) or scientific format, and must be transmitted most significant digit first. Valid ASCII characters are digits 0 through 9,E,e,+, =, and decimal point. ASCII character strings can be transmitted as any sequence of valid ASCII characters except Carriage Return. Carriage Return is used as the string delimiter. All ASCII data transfers, both numeric and alphanumeric, are terminated with a Carriage Return character or by activating the EOI signal line on the Management Bus, or both. (Refer to the INPUT and PRINT statements in the Input/Output Operations section of the 4050 Series Graphic System Reference Manual for detailed information on ASCII data transfers over the GPIB.)

Transferring Machine Dependent Binary Code

The term "machine-dependent binary code" refers to the internal binary format used to store data within the 4052/4054 Graphic System. Communication between the BASIC interpreter and an external peripheral device using machine-dependent binary code is usually faster because no time is needed to convert the internal binary format to ASCII format. Transfers between the random access memory and a peripheral device in machine dependent binary code implies that the peripheral device is able to understand the internal 4050 series binary format.

Normally, transfers of this nature are carried on between the random access memory and an external mass storage device that doesn't have to understand the code, or between the random access memory and a peripheral device specifically built for the system by Tektronix.

Information transfers to and from a peripheral device on the GPIB are carried on via the WRITE statement and the READ statement. Each data item transmitted is preceded by a two byte header which identifies the data type (numeric or alphanumeric) and the length of the data item in bytes. Refer to the READ statement and the WRITE statement in the I/O Operations section of the 4050 Series Graphic System Reference Manual for details.

Transferring One Data Byte at a Time

Direct access to the GPIB from the 4052/4054 keyboard uses the WBYTE (Write Byte) statement and the RBYTE (Read Byte) statement. These two statements let you send any eight bit pattern over the GPIB. The WBYTE statement also allows you to activate the ATN signal line to tell peripheral devices that the byte you're sending is a peripheral address or a control word. WBYTE controls the EOI signal line, except when a binary 0 is explicitly transferred by WBYTE-0. (Refer to the WBYTE and RBYTE statements in the Input/Output Operations section of the 4050 Series Graphic System Reference Manual for details.) To send binary zero with EOI activated the program should specify a value between zero and -0.5 that rounds to the integer zero in the WBYTE statement.

GPIB-TO-IEEE COMPATIBILITY

Introduction

The following text describes the interfacing compatibility of the Graphic System's General Purpose Interface Bus with the IEEE Standard #488-1975.

In general, the 4052/4054 acts as a standard talker, listener, and controller. The controller function does not have the ability to conduct a parallel poll; it does, however, have the ability to conduct a serial poll. Serial polls are taken each time the POLL statement is executed.

The 4052/4054 does not have the ability to transfer control to another device on the GPIB with controller capability. Therefore, the 4052/4054 assumes that it is the only controller on the GPIB.

GPIB Interfacing Compatibility in Detail

Reference: IEEE Standard #488-1975

The 4052/4054 Graphic System GPIB supports the following interface function subsets as defined in the IEEE Standard # 488-1975 document.

Section 2.3 SH (Source Handshake Function)
SH1 -- completely compatible

Section 2.4 AH (Acceptor Handshake Function)
AH1 -- completely compatible

Section 2.5 T (Talker Function)
TE3 -- basic extended talker. However, the processor addresses itself internally and not over the GPIB.

Section 2.6 L (Listener Function)
LE1 -- basic extended listener, however, the processor addresses itself internally and not over the GPIB.

Section 2.7 SR (Service Request Function)
SR0 -- no capability to issue SRQ

Section 2.8 RL (Remote Local)
RL0 -- no capability

Section 2.9 PP (Parallel Poll Function)
PP0 -- no capability

Section 2.10 DC (Device Clear Function)
DC0 -- no capability

Section 2.11 DT (Device Trigger Function)
DT0 -- no capability

Section 2.12 C (Controller Function)
C1 -- System Controller
C2 -- Send IFC and take charge
C3 -- Send REN
C4 -- Respond to SRQ
C28 -- Send Interface Messages

General Purpose GPIB Command

GPIB device addresses can be issued as illustrated in Figure 10-4 followed by a command to read data. When the **WBYTE @70, 109:** statement is executed in a BASIC program, the @ sign causes the ATN line to be activated, 70 is the primary talk address for device number 6 and 109 is the secondary address normally interpreted by the 4050 Series BASIC Language Interpreter as an INPUT command. The WBYTE statement enables secondary device addresses to be transmitted without activating contradictory firmware within the 4052/4054. The RBYTE statement can then be used to read data from the assigned talker. The RBYTE statement receives one or more data bytes from a peripheral device on the GPIB and assigns each data byte to a numeric variable.

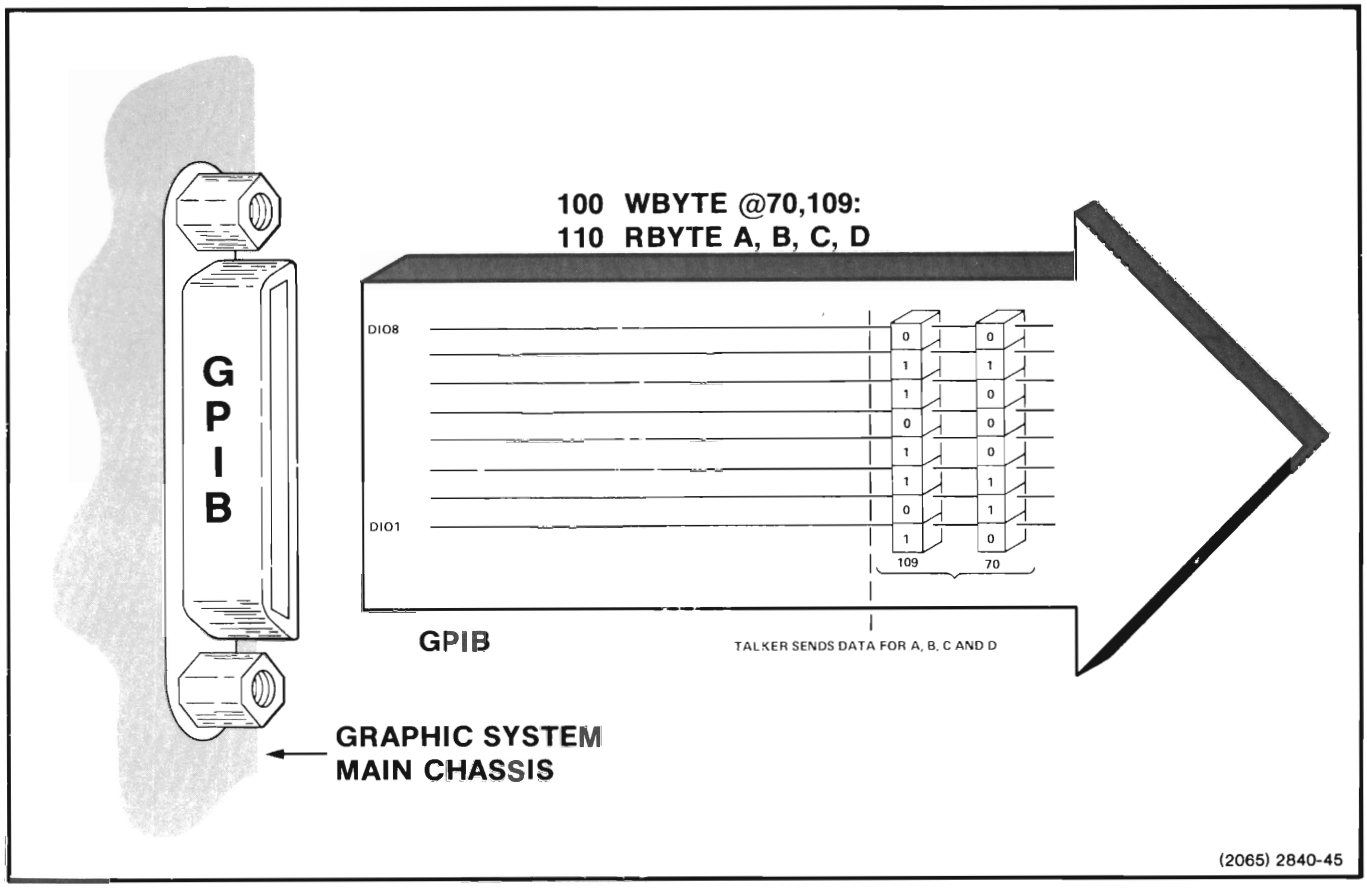


Figure 10-4. Reading Data From a Device on the GPIB. 70 is the primary talk address for device 6 and 109 is the secondary address associated with the INPUT command statement.

In the example of Figure 10-5 a primary address of 44 and secondary address of 108 are transmitted to the peripheral device. Data is sent to the peripheral device corresponding to the binary bytes associated with the numbers 65 and 66. The minus sign on -66 activates the EOI line during the last byte of data transferred. WBYTE @63, 95: transmits the universal commands UNTALK and UNLISTEN over the GPIB.

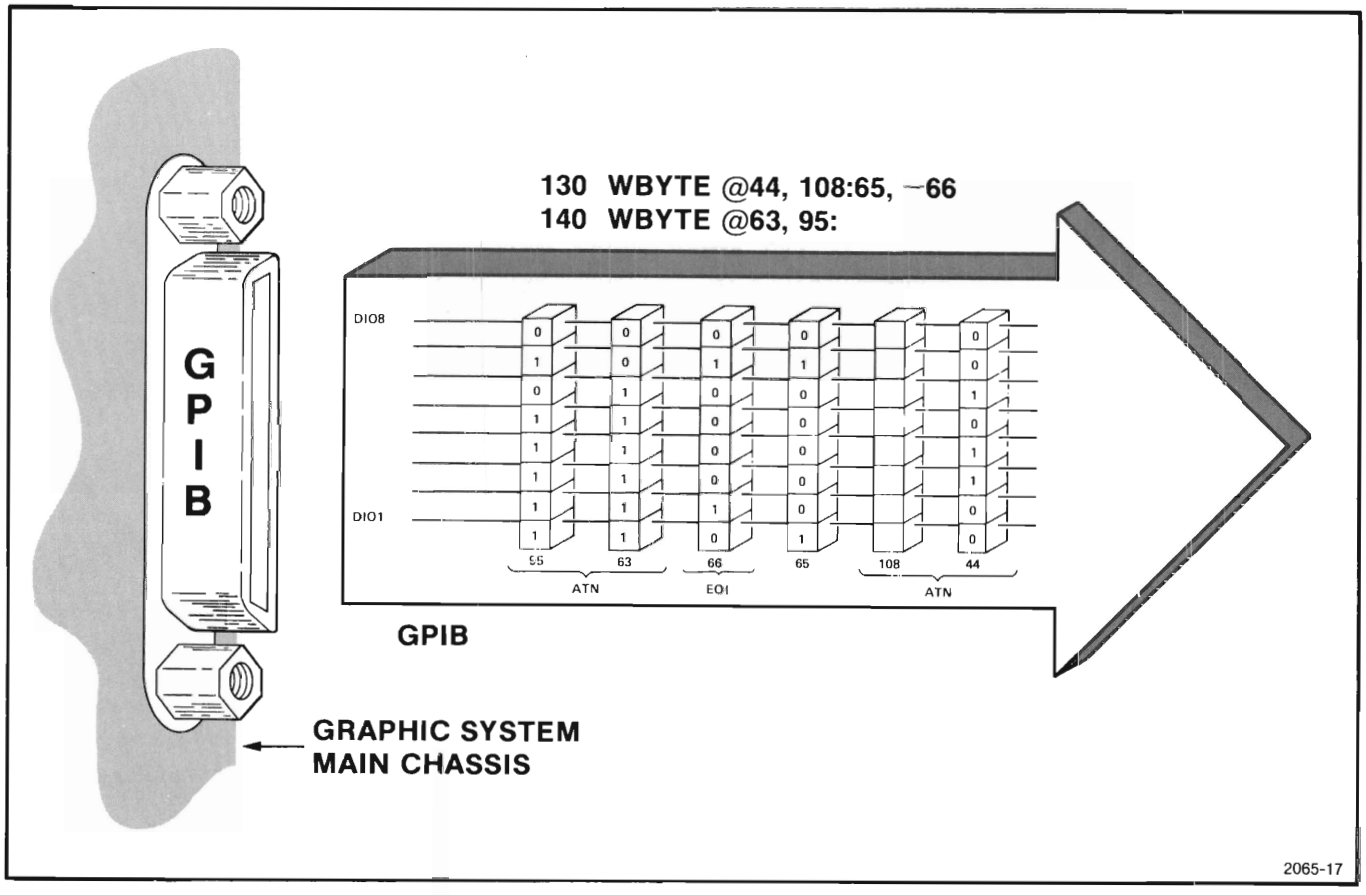


Figure 10-5. Transmitting Data to a Device on the GPIB Followed by the Universal Commands of UNTALK and UNLISTEN.

To cause one peripheral device to transfer information to another device on the bus, the listeners and talker must be addressed. The BASIC statement WYBTE % (arguments) must have the percent sign to remove the 4052/4054 from the GPIB as in Figure 10-6. The 4052/4054 then executes a WAIT statement to halt the current program until EOI is received. The ON EOI THEN 180 statement causes control to pass to line 180 when device-to-device data transfer is complete.

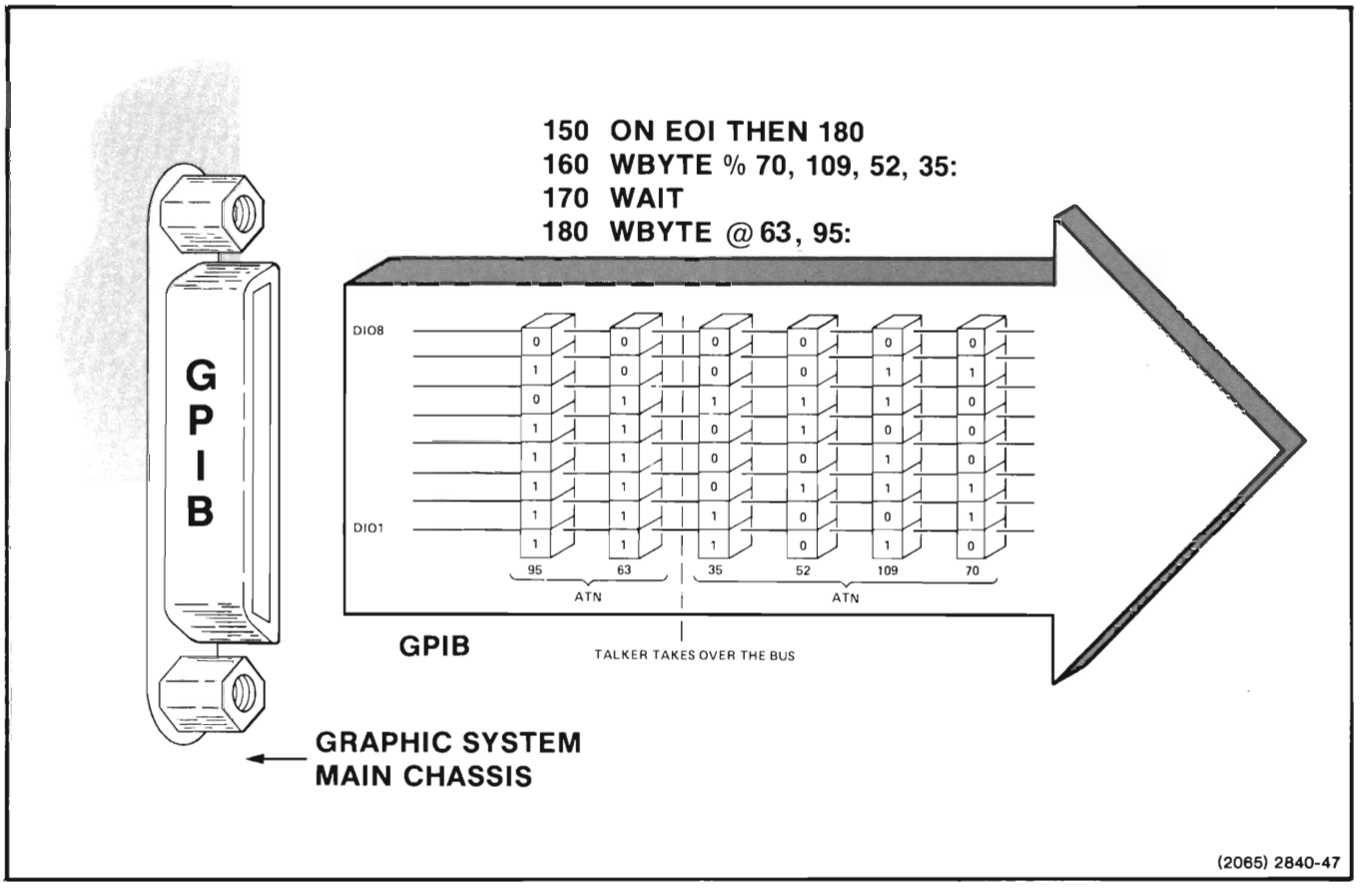


Figure 10-6. A Procedure to Initiate Data Transfer Between Two GPIB Devices and Waiting Until the Data Transfer is Completed.

Section 11

4052 DISPLAY THEORY OF OPERATION

DISPLAY CONTROL

Display operations of the 4052 require the drawing of vectors, the printing of dot matrix characters and the display of a refreshed cursor. Refer to the 4052 Parts and Schematics Manual and also the display control block diagram for the following descriptions. (Figure 11-1)

The circuitry shown in Figure 11-1 is located on the I/O Board.

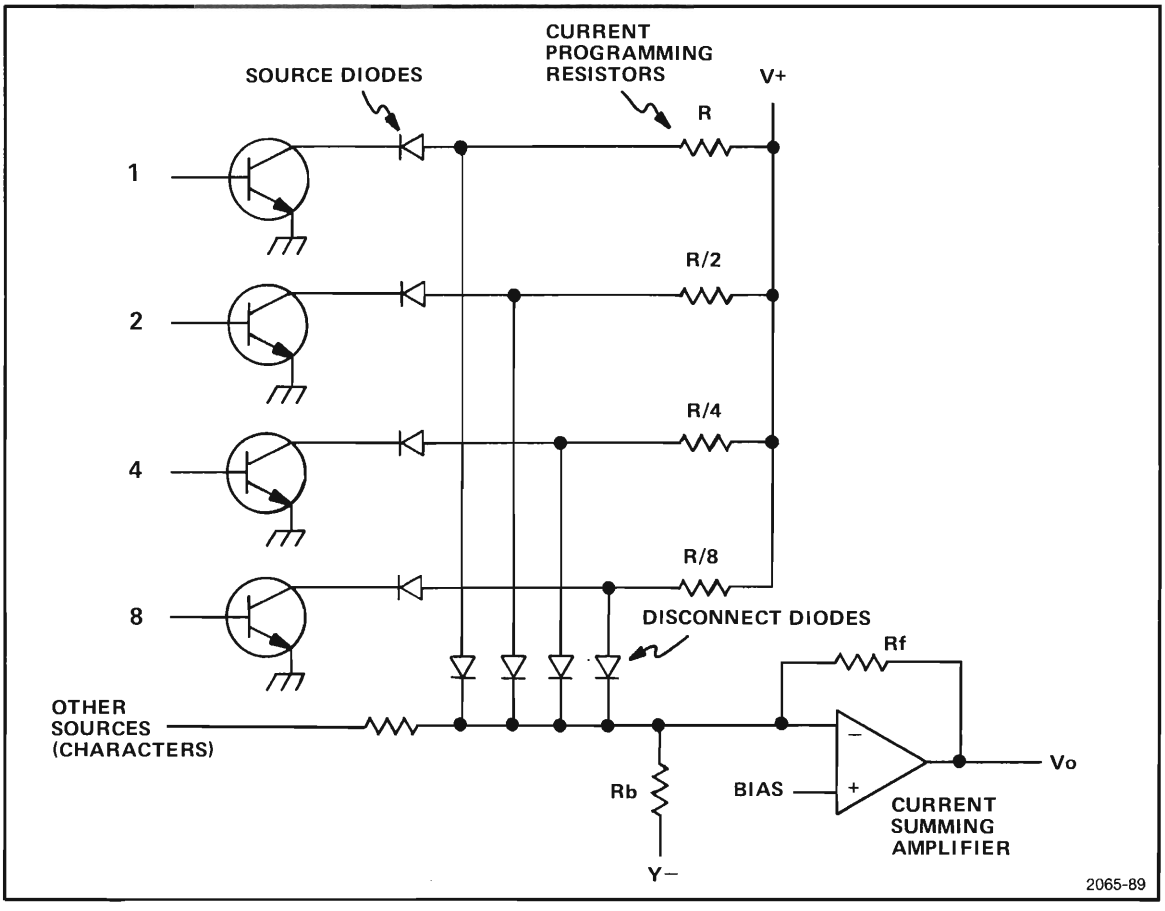


Figure 11-1. D/A Converter Using Proportioned Resistors and a Current Summing Amplifier.

The 4052 Processor communicates with the display control circuitry through a set of peripheral interface adapters (PIAs). The PIA output lines are programmed to control the display circuitry as directed by firmware instruction sequences contained in ROM (read only memory).

The output from the PIAs is changed from digital information to analog information to drive the deflection circuitry of the 4052. The writing beam of the crt is deflected by this analog information while other signals from the PIAs turn the beam on and off to form the written pattern on the crt face.

D/A Operation

The D/A converters change the digital output data from the system to analog signals for use by the display section.

Refer to the diagram (Figure 11-1). The transistors are the outputs of TTL logic. Resistors that are binary fractions of R (R, R/2, R/4, R/8) are current-programming resistors. Current through R/8 is eight times greater than current through R. Current through these resistors has two possible paths, through the transistor logic or through the current summing resistor Rb.

When transistor logic is on, output low, the transistor takes the current from its current programming resistor, removing the current from the summing amplifier input. The disconnect diode has reverse bias when the switching transistor is on.

When the transistor logic is off, output high, the transistor provides high impedance and reverse biases its source diode. This causes the programming resistor current to be summed by the amplifier.

The output voltage from the amplifier is proportional to the input current. When no current comes through the disconnect diodes or other sources, the current through Rf is equal to the current through to the operational amplifier. As current comes through the disconnect diodes or other sources, the current through Rf is decreased by the total sum of input currents. Current through Rf may even reverse in order to maintain the junction voltage between Rf and Rb at the BIAS level.

Figure 11-2 shows the information flow through D/A converters in the 4052.

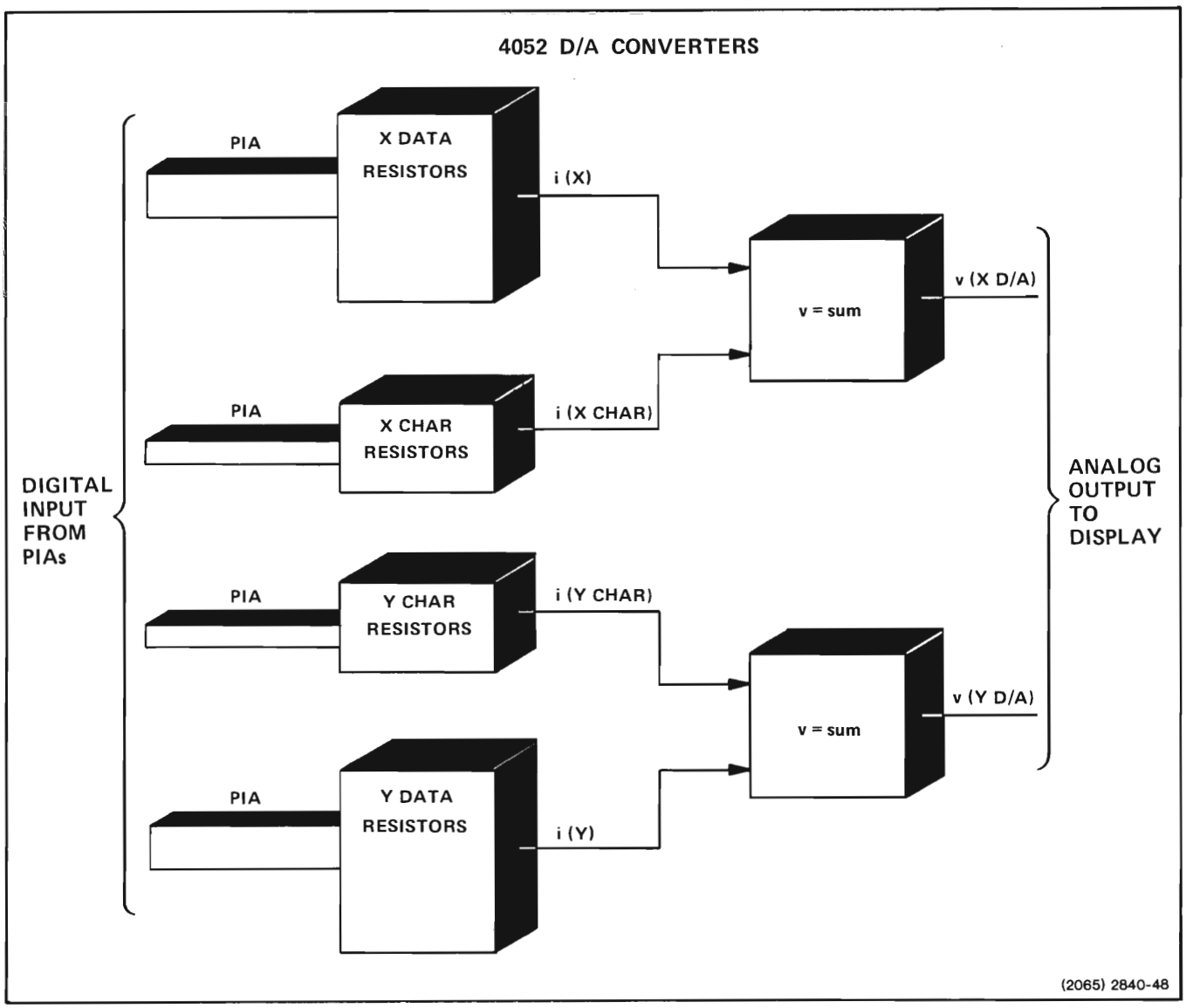
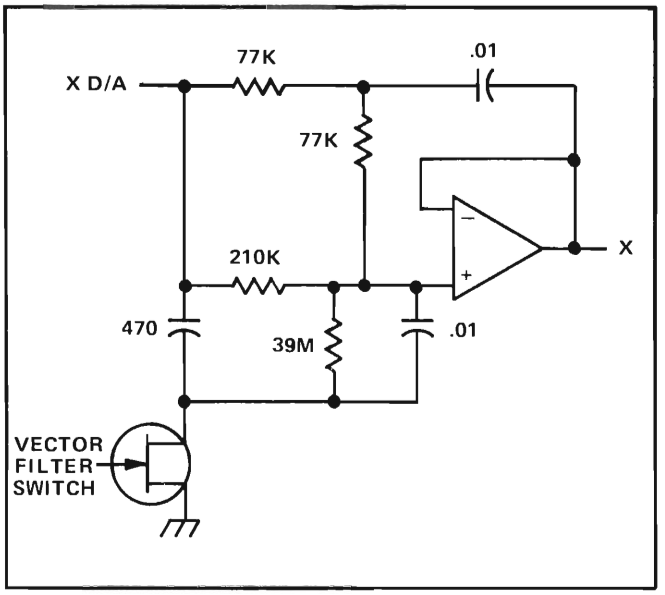


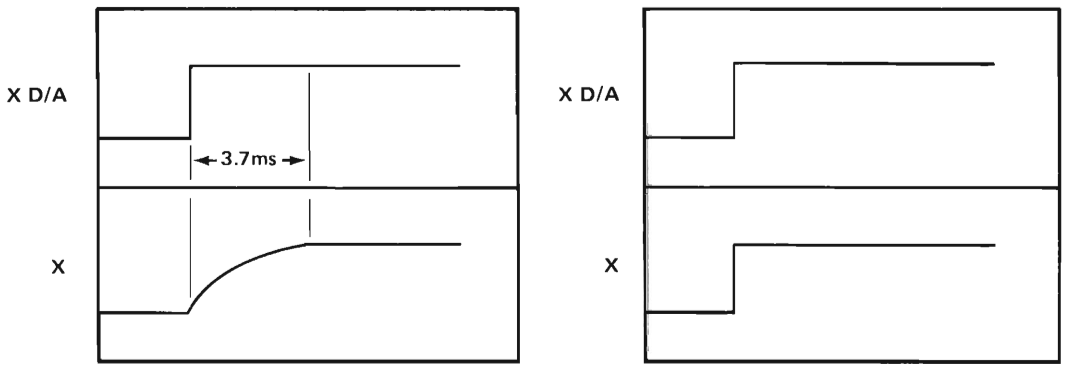
Figure 11-2. Data and Information Flow Through the X and Y Digital-to-Analog Converters.

Filter Operation

When the D/A converters switch the current source resistors in and out, the output signal contains small variations that need to be filtered out. Filtering is provided by the R/C filter at the positive input of the operational amplifier (Figure 11-3). Also see the appropriate 4052 schematic. When the FET (field effect transistor) is conducting, the filter network is given a ground reference and is able to filter the D/A signal. When the FET is off, the filter is disabled causing the output voltage to directly follow the input (Figure 11-4B). Straight vectors can be drawn because both filters for the X and Y axes have matched filtering characteristics.



FILTER CIRCUIT TO PROVIDE VECTOR WRITING DELAY ON THE X AXIS.



FILTER ENABLED FOR VECTORS.

FILTER DISABLED FOR CHARACTERS.

(2065) 2840-49

Figure 11-3. Vector Filtering Response Curves.

Long Vector Sense Circuit

The long vector sense circuit is shown in Figure 11-4. For specific parts values and component numbers, refer to the 4052 Parts and Schematics Manual.

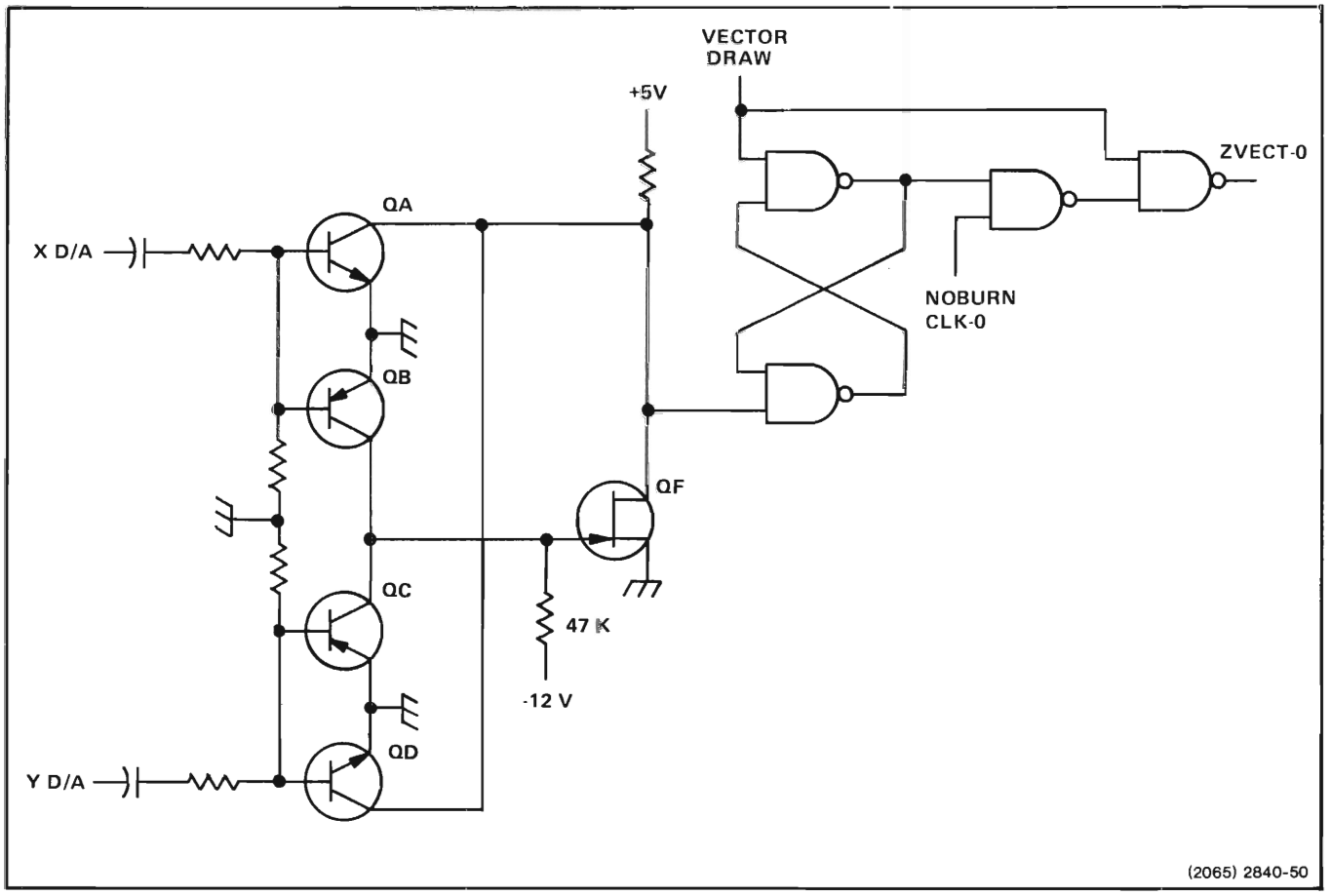


Figure 11-4. Long Vector Sense Circuit.

This circuit, during static operation, has an output voltage of near +5 volts. None of the transistors are conducting. A voltage change of more than -0.7 volts on either X D/A or Y D/A line will cause one of the four transistors (QA - QF) to conduct, and the output voltage will drop to zero. The active transistor will either ground the end of the resistor coming from the +5 volt line or the end of the resistor coming from the -12 volt line. If the input from the -12 volt line is brought up to zero, the FET, QF, goes into conduction to lower the input from the +5 volt line.

Since the output pulse for long vectors is only momentary due to the small .001 uf capacitors, Ca and Cb, the output is saved by a nand gate flip-flop during a vector drawing period. The presence of a long vector causes the NOBURN CLK-0 signal to be disabled before its effect reaches' the ZVECT-0 signal line. The ZVECT-0 signal is used to control the Z axis writing beam during a vector draw operation.

Alphanumeric Display

Refer to the display control block diagram (Figure 11-5). The display coordinate position is generated through the digital-to-analog converters (X DAC and Y DAC) and fed through the filter circuitry with the filtering disabled. A short time later, either SOT (Selected Operation Trigger) or ADOT (Alphanumeric Dot) is activated. SOT writes the refreshed cursor. ADOT prints a stored character. The timers for cursor and character intensity are adjustable by potentiometers accessible through the bottom of the instrument.

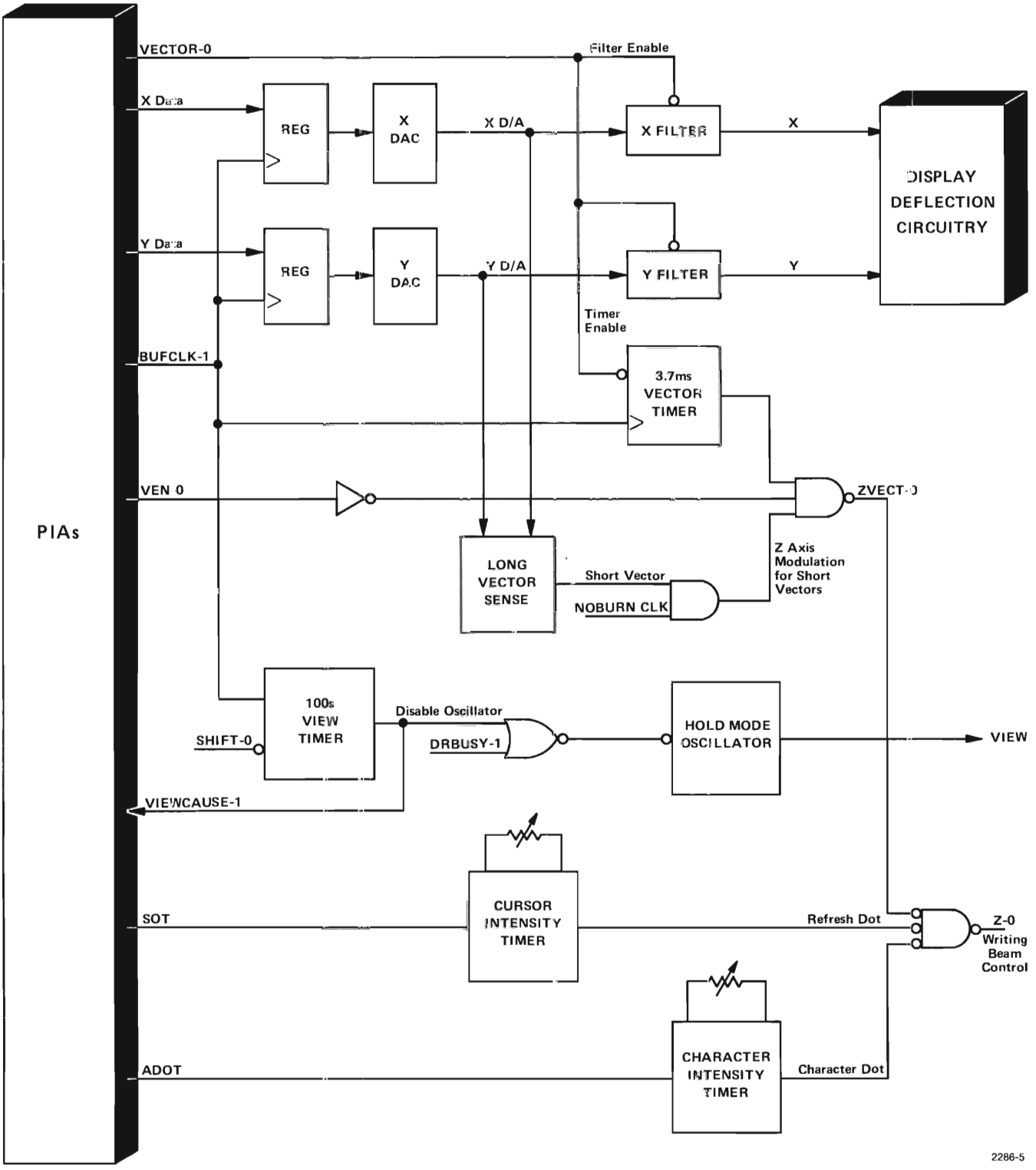


Figure 11-5. Display Control Circuitry Block Diagram.

Other Display Control Functions

Refer to the display control block diagram (Figure 11-5). View mode is active when the VIEW signal is logically true. A View Mode Timer keeps the 4052 in View Mode for 100 seconds following either the closure of the keyboard SHIFT key or the display of any new information on the crt. The View Mode Timer disables the Hold Mode Oscillator. During Hold Mode operations, the VIEW signal is activated by a square wave having a 12.3% duty cycle. The screen goes dark, but the stored information is retained on the crt phosphor for later viewing. If the system remains in hold mode for more than thirty minutes, the screen is automatically erased.

During hard copy activity, DRBUSY becomes true to be sure that the View flood guns are on during the time a hard copy is being made.

Erasing the screen is accomplished by lowering the ERASE-0 line.

DISPLAY BOARD

The Display Board takes deflection and control information from the I/O Board and changes these signals into a form usable by the direct view storage tube (DVST). The Display Board also uses signals from an optional hard copy unit to copy the display information from the storage tube to paper.

Refer to the block diagram of the Display Board (Figure 11-6) and crt schematic (Figure 11-7). Display deflection amplifiers and other analog crt control circuitry are on the 4052 Display Board. The Display Board schematics are in the Parts and Schematics Manual. The Display Board is divided into three operational sections:

- Deflection Amplifier circuitry
- Storage, View and Erase circuitry
- High Voltage and Focus circuitry

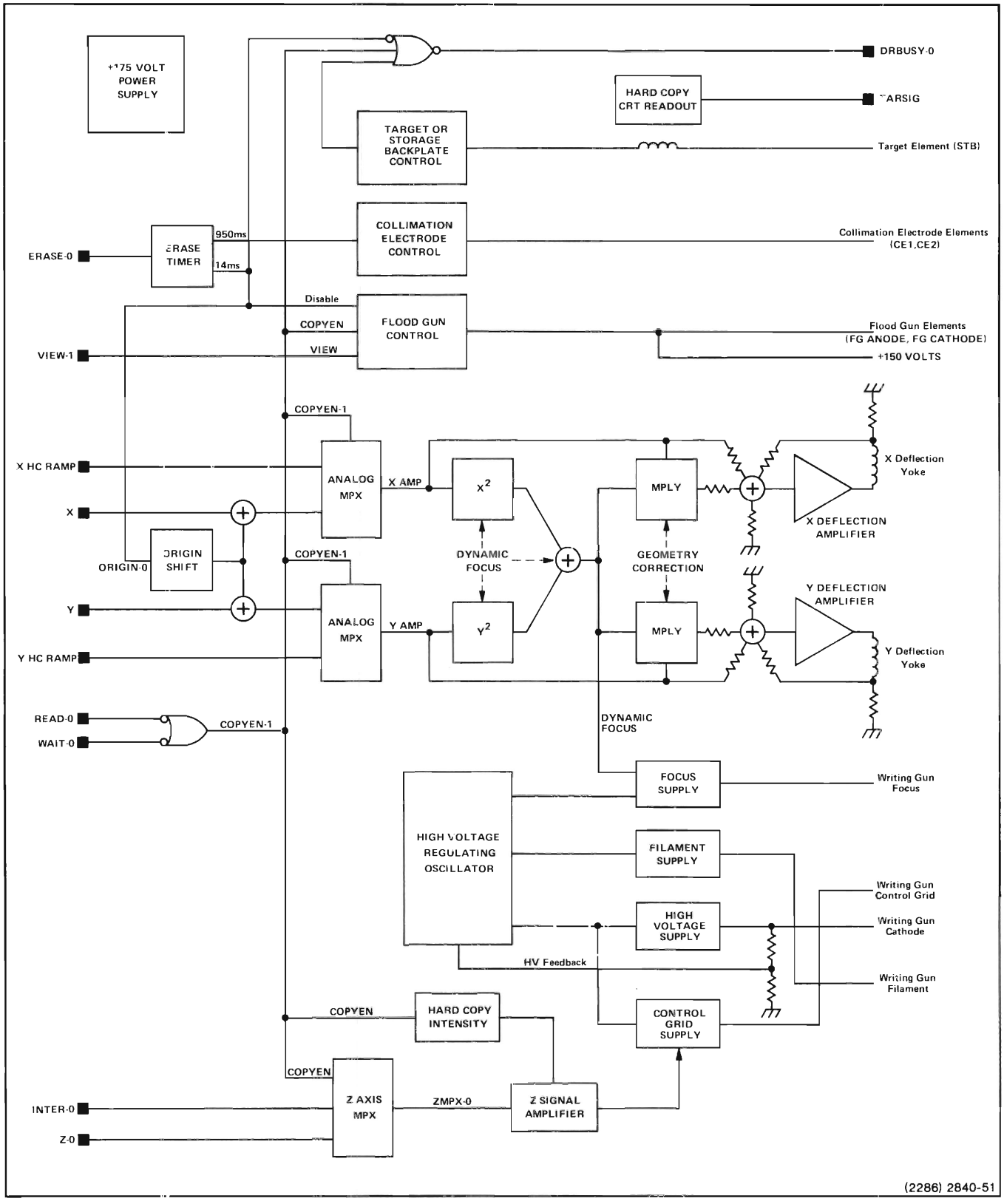


Figure 11-6. Display Board Block Diagram.

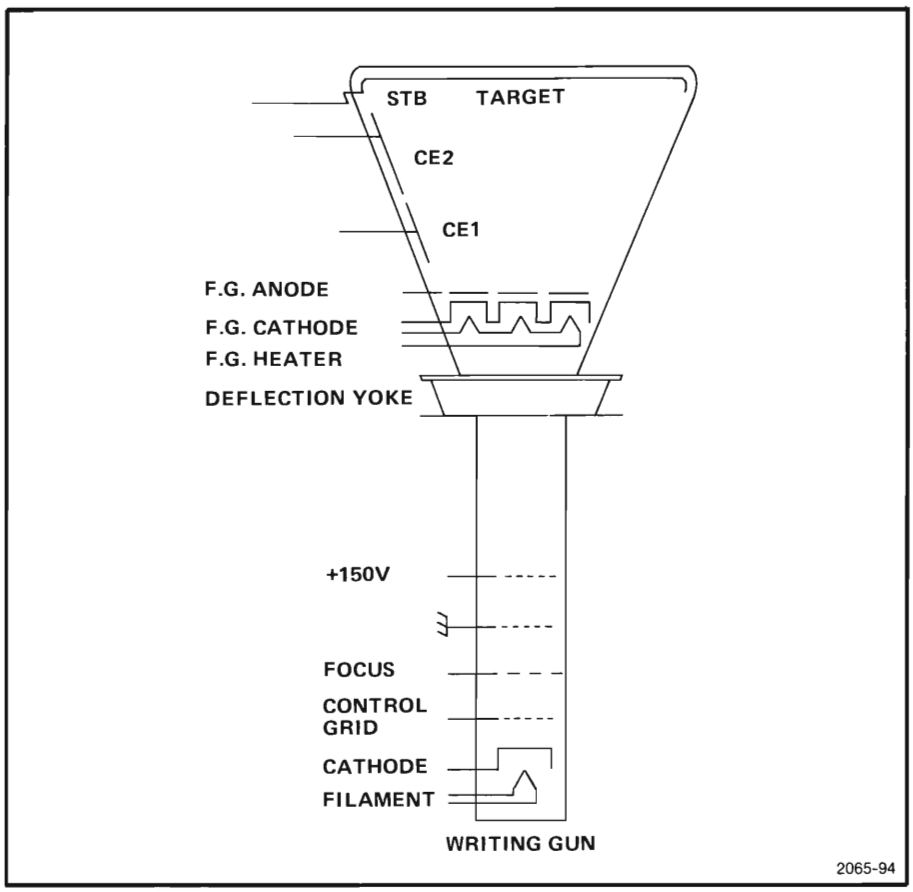


Figure 11-7. Direct View Storage Tube (DVST) Crt Schematic.

Input to the Display Board is from display control circuitry on the I/O Board. Outputs from the Display Board are to the crt electrodes and to the deflection yoke.

Refer to the Display Board Block Diagram, Figure 11-6, along with the Deflection Amplifier Circuitry description. The Amplifier input circuitry provides the selection of hard copy deflection signals (X HC RAMP and Y HC RAMP) if hard copy operation is activated, or the selection of display deflection signals (X and Y) from the I/O Board during normal system operation.

Refer to the 4052 Display Block Diagram. The deflection amplifier circuitry has three circuit sections: dynamic focus, geometry correction, and deflection amplifiers. In this circuitry, the X AMP and Y AMP signals are the primary deflection signal components.

The Geometry Correction section provides a correction component to the deflection circuitry. It compensates for the pincushion distortion seen on electromagnetic deflection systems. The amount of correction is set by external resistors.

Another amplifier generates an error (Dynamic Focus) signal which is used to correct for defocusing. The defocusing is due to changes in the length of the writing beam as it is deflected.

The deflection amplifiers are high-gain current amplifiers designed to provide the necessary current in the deflection coils to deflect the writing beam. The magnetic field produced is directly proportional to the current in the deflection coil or yoke.

Deflection Amplifier

The deflection amplifiers are composed of an operational amplifier driving a complementary pair of cascaded current amplifiers. The X deflection amplifier and Y deflection amplifier have identical operation. Inputs to the operational amplifier are the sum of all input signals incorporated into writing beam deflection, the primary deflection signal, geometry correction, position adjustment and gain adjustment. The GAIN adjustment provides a feedback voltage from the coil current sensing resistors to set the amplifier gain.

An origin shift circuit is included to make certain that the screen is not continually written in the same spots. To keep this from happening, the writing area is shifted slightly each time the screen is erased. The origin shift circuitry is made up of a three-bit binary counter and a small range digital to analog converter. It supplies small amounts of current to the X and Y axis deflection signals. The counter is incremented each time the screen is erased. The origin shift circuitry is part of the input multiplexer chip.

Storage and Erase Control Circuits

Refer to the Display Board Block Diagram (Figure 11-6). Target control, collimation control, and flood gun control circuits are switchable high voltage sources. Depending upon the state of a logic input signal the output voltage acquires one of two stable voltage levels. One level erases the screen and the other level allows the screen to be written on.

Erase Timing and CRT Voltage Levels

Erase timing is controlled by the erase timer monostable devices. Refer to the erase timing diagram of Figure 11-8. The first monostable provides a 14 millisecond pulse that writes the entire screen by increasing the flood gun current. The 950 millisecond multivibrator is then triggered to erase the screen and restore the crt operating level without writing the phosphor again. If the target voltage increases too fast, the face of the crt will go to the bright written state.

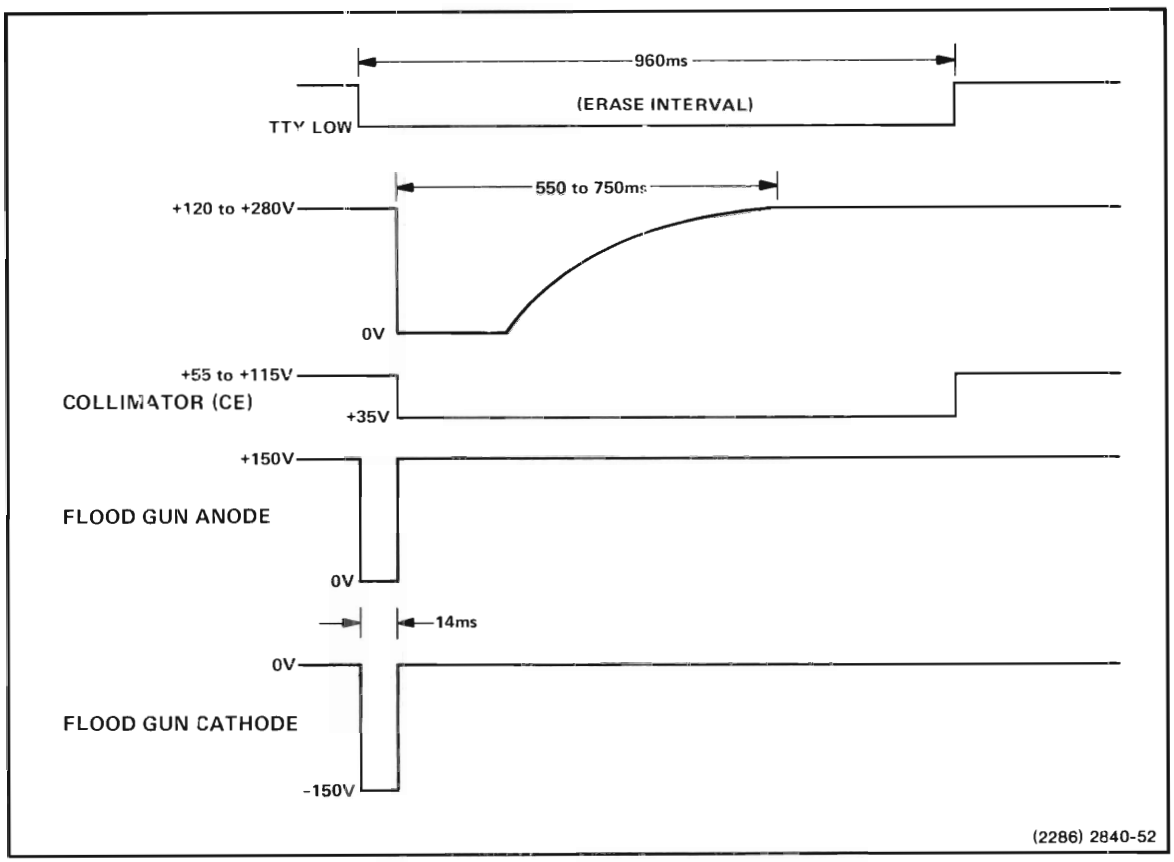


Figure 11-8. Erase Timing and Voltage Waveforms.

The crt operation level, as established by the target control circuitry, causes crt information to run together when set too high. Information fades away if the crt operating level is set too low. The operating voltages for the particular crt in the instrument are specified on a service tag within the instrument. The operating voltages for a new crt will be specified in the accompanying information.

Collimation operating level, as established by the collimation control circuitry, determines the uniformity of flood gun intensity across the face of the crt. If the voltage is too high, information on the outer portions of the crt will tend to run together and excessive display power will be used. If the voltage is too low, information at center of the crt will run together and information on the outside edges will tend to fade away.

Storage Backplate Control

The Storage Backplate Control amplifier controls the voltage at the storge backplate of the crt. (The Backplate is also called the Target.) A simplified circuit is shown in Figure 11-9. Normal output of inverter U1 is grounded. During the erase cycle, the output goes to an open collector state placing the positive timing capacitor lead at +9 volts through diode CR4. During normal operation, the voltage across the timing capacitor (C3) is approximately zero. During the erase cycle, the positive side of the capacitor is lifted to +9 volts and the negative lead charges toward zero through R2. Q1 buffers the voltage from the timing circuit and provides the necessary current to the voltage regulating circuitry. At the end of the erase cycle, the positive capacitor lead is brought to zero and the negative lead discharges to ground through diode CR5.

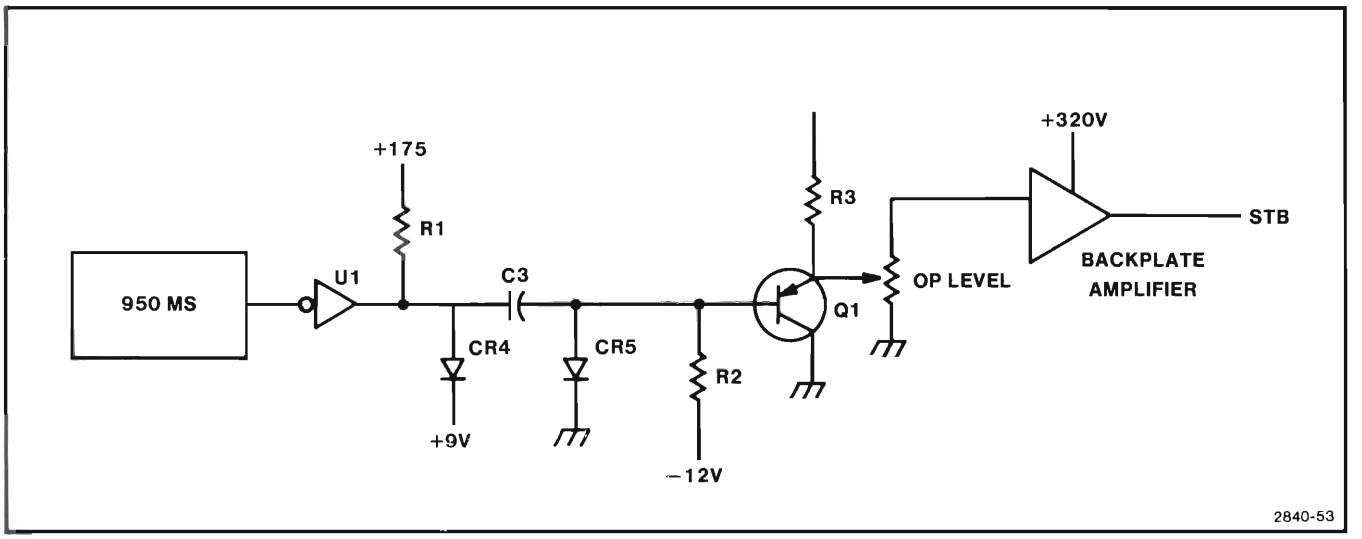


Figure 11-9. Simplified Backplate Amplifier.

The beginning of the erase cycle makes about a +5 volt change on the OP LEVEL adjustment resistor. This causes U3 to turn on hard, grounding the STB electroce on the crt. The STB electrode remains grounded until the timing current through Q1 drops enough to allow the output voltage from U3 to rise again.

Two transistors,(U3), are required to drive the STB line. They are biased so that their electrical breakdown voltages are not exceeded by the +320 volt unregulated supply.

Collimation Control

Normal Collimation Control operating range is established by the CE adjustment. During the erase cycle, the collimation amplifier turns on and the output voltage on CE1 and CE2 drops to +5 volts.

During hard copy operations, the collimation amplifier conduction is turned off, allowing CE1 and CE2 to go positive. The amplifier supply is the +185 volt unregulated supply, so that voltage appears at CE1 and CE2.

Flood Gun Control

Normal operation has the VIEW-1 signal at a high voltage level. This causes the flood gun controllers, Q3 and Q4, to be off (Figure 11-10). The flood gun anode then has a voltage of +150 volts regulated by zener diodes. The flood gun cathode is near zero.

Hold mode operation causes the VIEW-1 signal to oscillate between TTL true and TTL false voltage levels. When VIEW-1 is in the low voltage state, the flood gun controllers are turned on. This places the flood gun anode voltage at -20 volts. Since the cathode voltage remains near zero, the flood guns are turned off.

During erase operations, Q1 grounds the positive lead of the 50 ufd capacitor for 14 milliseconds. This forces the negative lead to -150 volts. The voltage potential between the flood gun electrodes and the crt TARGET (STB) increases by 150 volts. The increased potential causes the flood guns to write the crt completely and erase the written areas.

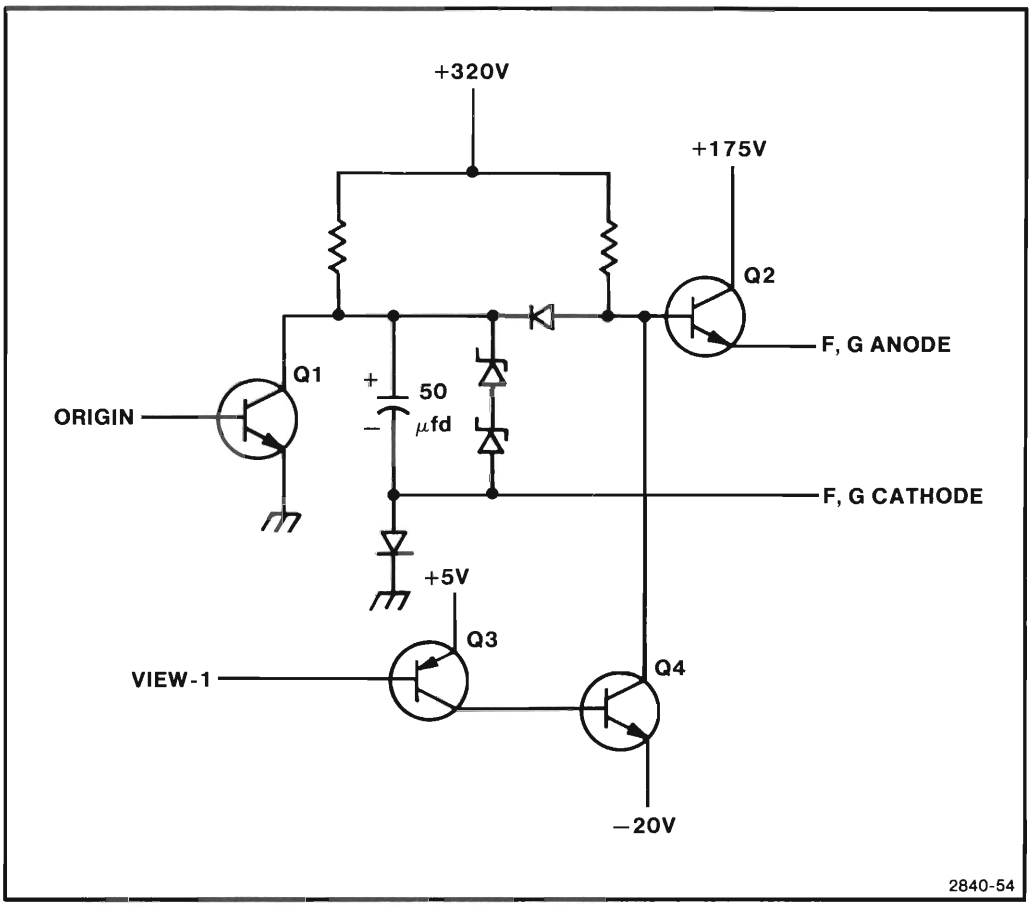


Figure 11-10. Simplified Flood Gun Control.

HIGH VOLTAGE CIRCUITS

The high voltage circuits provide voltages for the focus electrodes and writing gun electrodes of the crt. The writing gun elements operate at -4,000 volts dc. Power to the high voltage circuits is generated using a flyback transformer driven by a regulated blocking oscillator.

Z axis control is provided by coupling a voltage through a capacitor to turn on the writing beam. With no Z axis input, the writing beam is biased off.

High Voltage Regulator Oscillator

The high voltage regulator oscillator is a regulated blocking oscillator. A typical blocking oscillator circuit is provided by transistor Q2 and transformer windings 5 and 4 (Figure 11-11). The transformer operates as a flyback transformer. The oscillator transistor (Q2) momentarily draws current through the primary winding 5-4 and then turns off to provide a high impedance to the established current. Winding 6-3 provides positive feedback for sustained oscillations. Regulating voltage feedback is provided by a voltage divider (R1 and R2) in the high voltage supply. The feedback control signals are then amplified by a series of transistors and applied to the base of the oscillating transistor for duty cycle control. This duty cycle control provides voltage regulation.

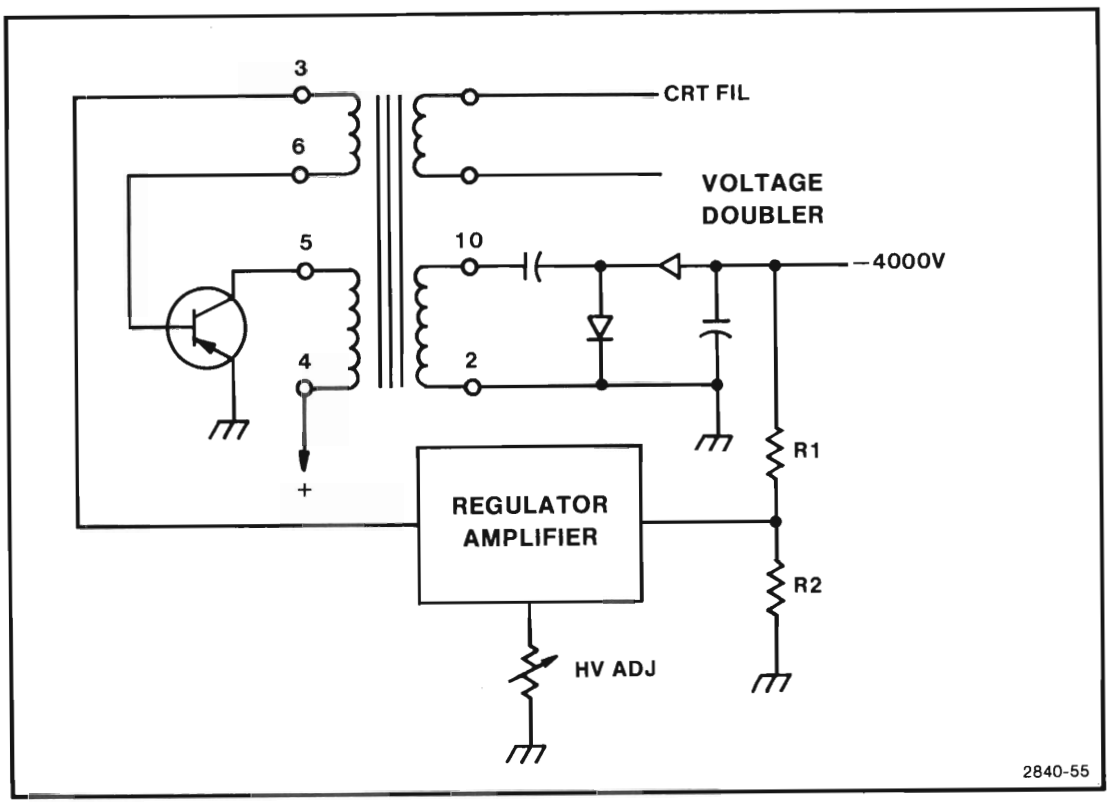


Figure 11-11. High Voltage Oscillator.

High Voltage Supply

The source for the high voltage supply is winding 10-2 of the flyback transformer. This ac voltage goes to a voltage doubler, as shown in Figure 11-11. High voltage feedback bias is determined by the HV ADJ resistor and the associated resistance network. The output from this divider is fed back to the high voltage oscillator to establish the cathode voltage at -4000 V.

Focus Supply

The focus supply consists of an adjustable gain amplifier for dynamic focus and an isolated focus supply from the high voltage flyback transformer. The isolated supply uses the output of the dynamic focus amplifier as its voltage reference. A fixed negative value as determined by the FOCUS adjustment is subtracted from the dynamic focus amplifier output before driving the crt focus electrode. The gain of the dynamic focus amplifier is determined by the DYNAMIC FOCUS adjustment.

Filament Supply

Voltage reference for the writing beam filament supply is the -4,000 volt cathode voltage. The filament supply provides alternating current to the filaments from a winding on the high voltage transformer. This winding is elevated to -4000 volts.

Control Grid Supply

A simplified diagram of the control grid supply is shown in Figure 11-12. The supply voltage driving the rectifier circuitry of the control grid supply is a clamped waveform as shown in Figure 11-13. The 1.2 megohm resistor enables the clamping process to occur by limiting available current from the transformer. The BIAS voltage is adjusted to ensure there is enough negative potential on the control grid to keep the writing beam turned off when the Z axis is not active. When the Z axis turns on, a positive voltage is coupled through a capacitor to the control grid, turning on the crt writing beam.

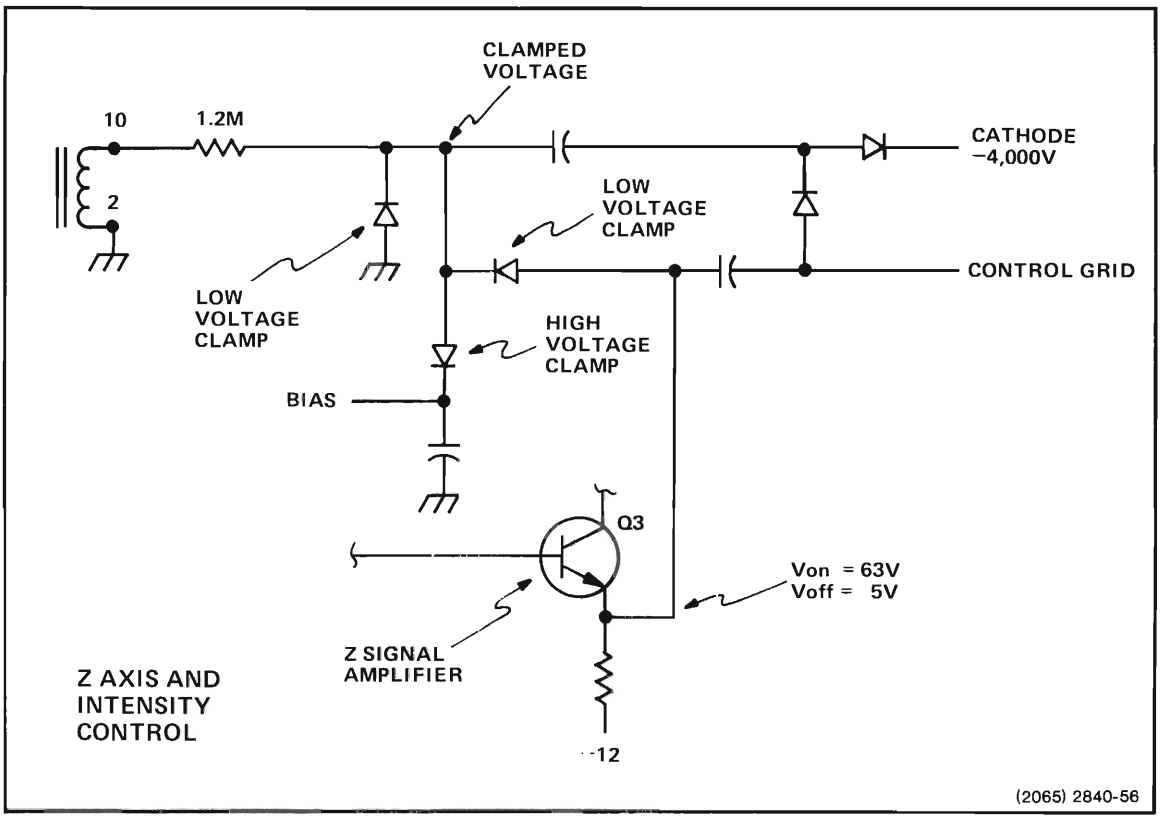


Figure 11-12. Z Axis Control Grid Circuitry Used to Regulate the Writing Beam Intensity.

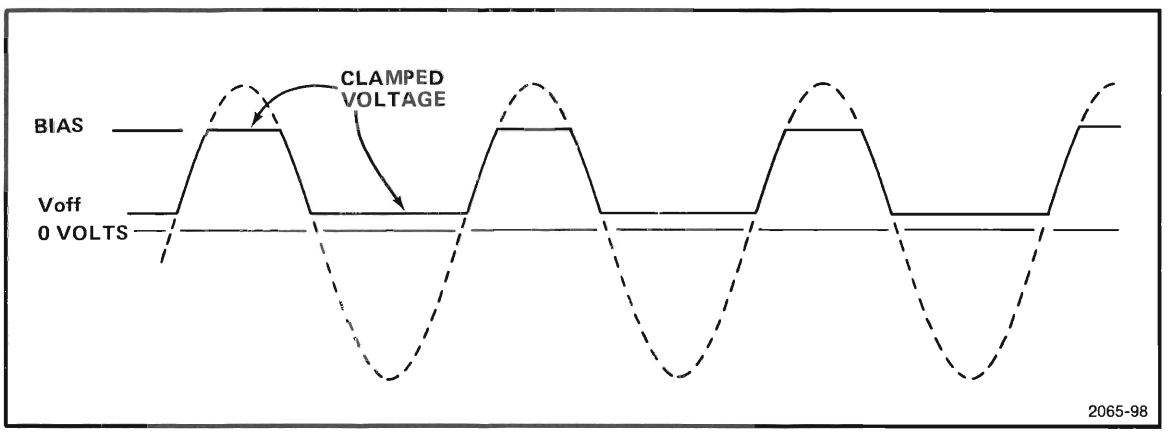


Figure 11-13. Waveform Used to Establish the CRT Control Grid Voltage Level.

Intensity Control and Z Signal Amplifier

Refer to the Simplified Z Axis and Intensity Control Diagram (Figure 11-12). Intensity Control Circuitry is a regulated voltage source referenced to the +175 volt power supply. Output of the supply at transistor Q3 is normally 63 volts. During hard copy operations, the voltage is determined by the HARD COPY INTENSITY adjustment.

The Z signal amplifier normally has an output of 5 volts. The Z MPX-0 signal is at a TTL high voltage. When Z MPX-0 goes low to turn on the writing beam, Q3 turns off and causes the output voltage to go to the voltage established by the intensity control amplifier, normally 63 volts.

HARD COPY OPERATIONS

Hard copy signals and their influence are shown in the block diagram of Figure 11-14. The related schematics are found in the 4052 Parts and Schematics Manual.

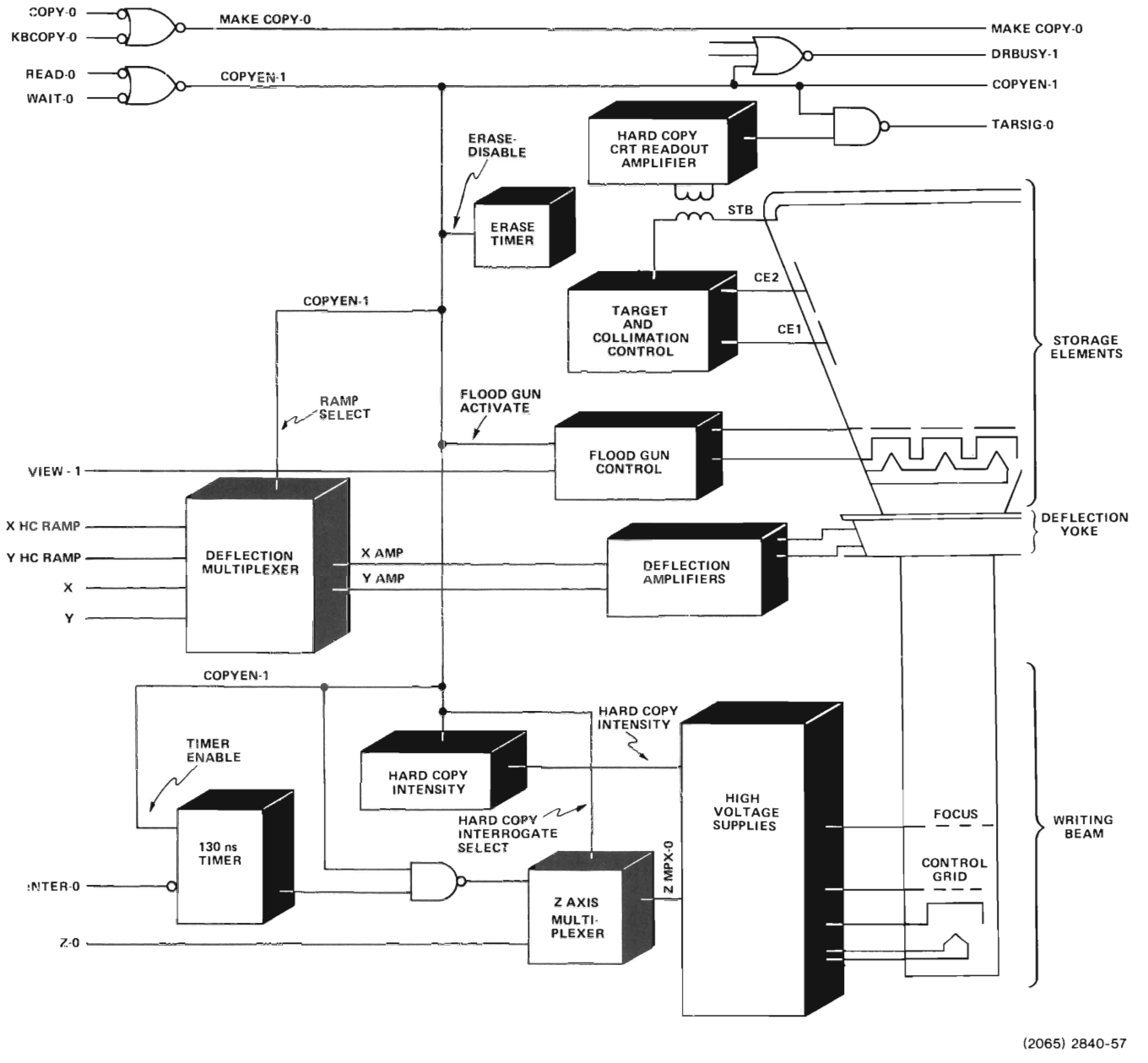


Figure 11-14. Hard Copy Circuitry Block Diagram.

Hard copy operations can be started any of three ways:

1) Press the MAKE COPY button on the keyboard.

2) Execute a COPY command.

3) Press the COPY button on the hard copy unit.

In each case, the MAKE COPY-0 signal is asserted. When an attached hard copy unit receives the MAKE COPY-0 signal, it issues a READ-0 or WAIT-0 to the calling device. READ means that the hard copy unit is busy making a copy of the display. WAIT means that the hard copy unit has a multiplexer option and is currently busy making a copy from another display.

Upon receiving READ-0 or WAIT-0 from a hard copy unit, the Copy Enable (COPYEN-1) signal is sent high. The COPYEN signal sends a display busy condition (DRBUSY) back to the Graphic Computing System. It also prevents the display from being erased. The HC RAMP signals provide the writing beam deflection voltage. The COPYEN signal establishes the writing beam intensity used for display interrogation pulses. It also enables Z axis display interrogation pulses (INTER-0/C) to be received from the hard copy unit.

Hard copy information is read from the face of the crt by using a pulsed writing beam of low intensity. Whenever the writing beam touches a written area of the storage backplate (target) of the crt, there is an increase in current. This current is sensed as a differential voltage on the output of a pulse transformer and amplified by the hard copy Amplifier circuitry. Target signal information is then placed on the TARSIG signal line.

The THRESHOLD adjustment determines the signal level used to discriminate between bright and dark portions of the crt.

Section 12

4054 DISPLAY THEORY OF OPERATION

INTRODUCTION

This section provides information to enable the technician to isolate most of the problems to a block of circuitry on a specific board. The problem then can be traced to a specific component using the schematics as a guide.

GENERAL INFORMATION

Figure 12-1 is a block diagram of the 4054 display circuitry.

The display circuitry is contained on six circuit boards, with an Interconnect Board connecting five of them to each other.

The writing circuitry of the display includes the Deflection Amplifier Board, the deflection yoke, the High Voltage and Z Axis Board, and the writing components of the crt.

The storage circuitry includes the Storage Board and the storage components of the crt, the flood guns, the collimation electrodes, and the crt target.

Hard copy operation is controlled by circuitry located on the Deflection Amplifier Board, the Storage Board, High Voltage and Z Axis Board, and the Hard Copy Amplifier Board.

The digital signals coming into the display are converted to analog signals by the Display Controller and the Vector Generator. The Display Controller also connects the Joystick and Thumbwheel inputs to the display.

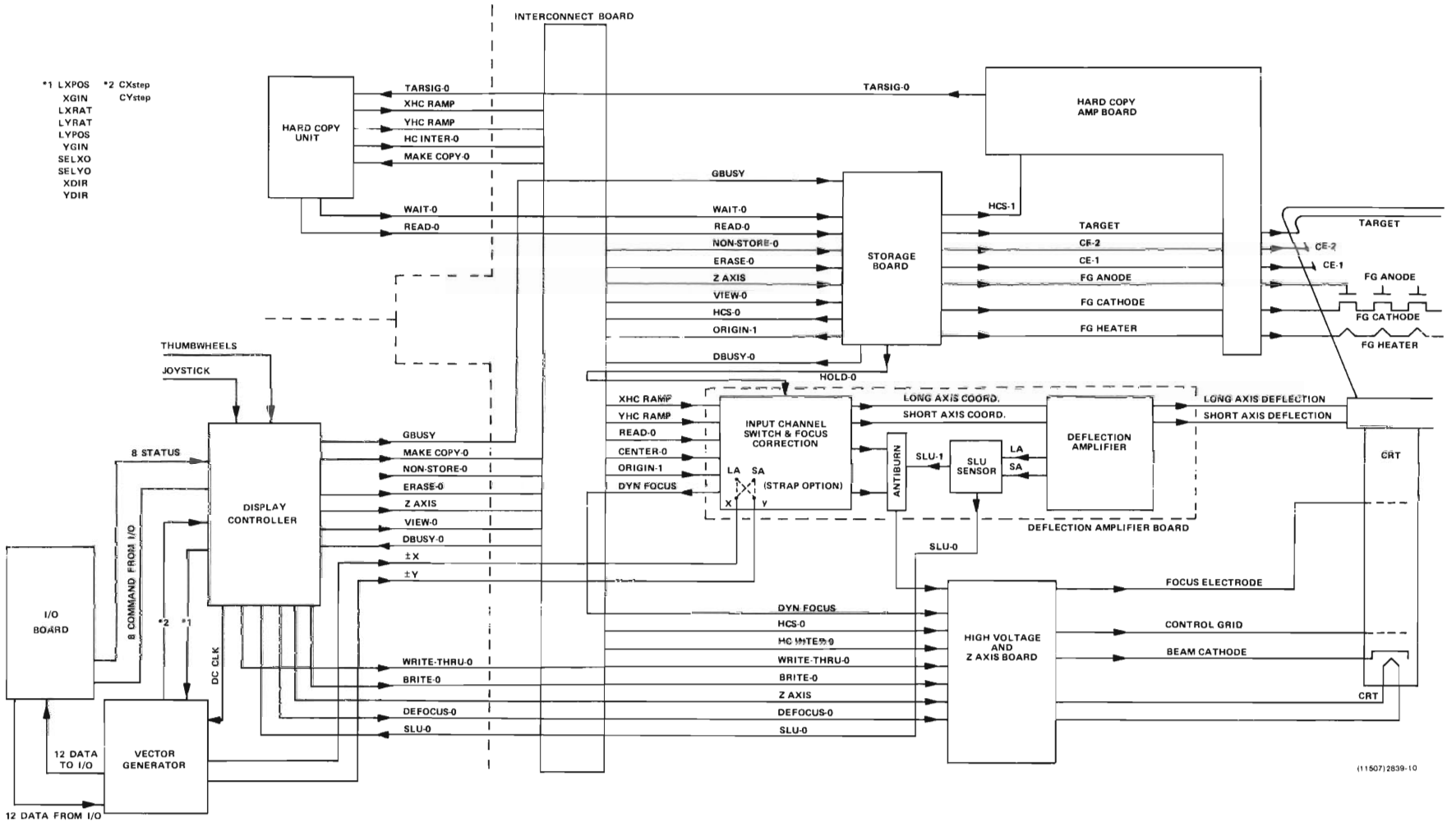


Figure 12-1. 4054 Display Block Diagram.

CIRCUIT DESCRIPTION

Interconnect Board

The Interconnect Board provides the connections between the display boards, cables from the I/O Board, and other inputs to the display. It has no circuitry other than connectors and connecting bus leads between boards and cables.

High Voltage and Z Axis Board

Refer to Figure 12-2. It may also be helpful to refer to the schematics from the Parts and Schematics Manual while reading this section.

The High Voltage and Z Axis Board controls and regulates the writing beam focus, intensity, and high voltage. The main circuit sections are:

- High Voltage Oscillator
- High Voltage Supply (Rectifier)
- Intensity Control Logic
- Z Axis Amplifier
- Control Grid DC Restorer
- Dynamic Focus Amplifier
- Focus DC Restorer

High Voltage Supply

The High Voltage Supply is a voltage-doubling rectifier circuit which delivers -6000 Vdc to the crt cathode and provides a control reference for the High Voltage Oscillator. The High Voltage Supply also provides a -6000 V reference to the crt Heater supply, Control Grid DC restorer, and the Focus DC restorer. It is described in the 4054 power supply section (14).

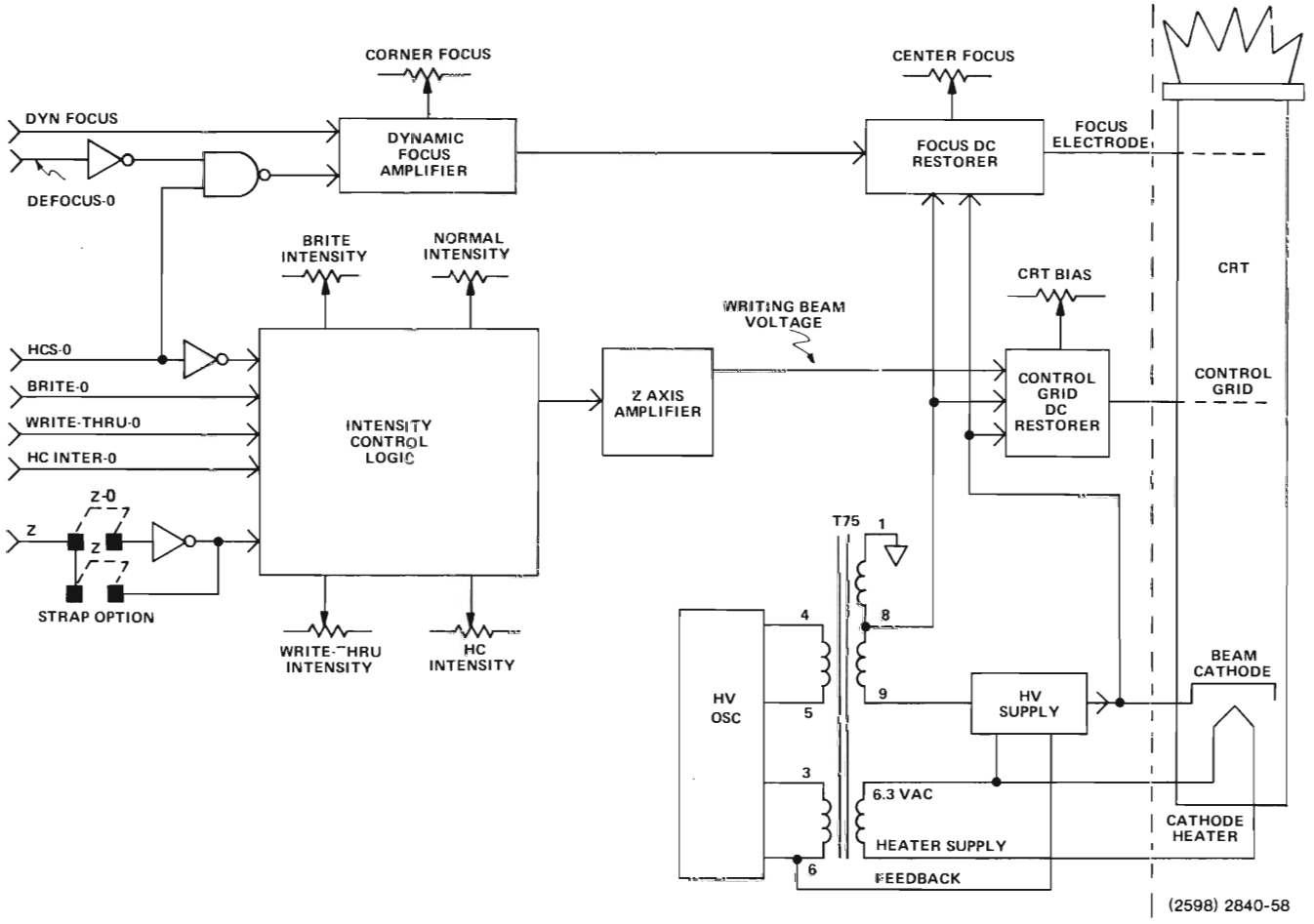


Figure 12-12. High Voltage and Z-Axis Board Block Diagram.

Intensity Control Logic

The Intensity Control Logic controls the crt writing beam intensity as selected by the logic values of HCS-0 (Hard Copy Switch), BRITE-0, and WRITE-THRU-0.

Whenever HCS-0 is low, all other control signals are disabled. At that time, HC INTER-0 from the hard copy unit controls the Z Axis Amplifier. The crt writing beam can then be adjusted by the HARD COPY INTENSITY control. This adjustment is located on the front of the instrument near the power switch.

Unless the display is in Hard Copy mode, the Z Axis signal controls the Z Axis Amplifier and the crt writing beam.

There are several intensities and related adjustments selected by the Intensity Control Logic. The logic combination of WRITE-THRU-0 and BRITE-0 selects the intensity of the crt writing beam while HCS-0 is false. If WRITE-THRU-0 is low, the effects of Brite and Normal intensities are inhibited and the crt writing beam intensity is controlled by the WRITE-THRU INTENSITY adjustment. This control is located on the front of the instrument near the power switch. If WRITE-THRU-0 is high, BRITE-0 determines whether the crt writing beam is Brite or Normal. If the BRITE-0 signal is not true (high), the NORMAL INTENSITY adjustment determines the crt writing beam intensity. When the BRITE-0 signal is true (low), the crt writing beam will be made slightly brighter than than Normal Intensity. This is accomplished by adding the current from the BRITE INTENSITY adjustment to that from the NORMAL INTENSITY adjustment. This causes the Z Axis Amplifier to increase writing beam intensity.

Z Axis Amplifier

The Z Axis Amplifier is a logic-controlled amplifier that provides a crt writing beam voltage to the Control Grid DC Restorer. The crt control grid voltage is switched between a non-writing and a writing level. This level is set by the adjustments in the Intensity Control Logic section. The Z Axis Amplifier turns the crt writing beam on and off under the control of the Z Axis signal and the logical state of HCS-0, BRITE-0, and WRITE-THRU-0.

Dynamic Focus Amplifier

The Dynamic Focus Amplifier maintains a constant crt writing beam focus. It also provides an alternate crt writing beam width. This function is provided by modification of the reference voltage sent to the Focus DC Restorer. The DYN FOCUS (Dynamic Focus) signal makes the necessary changes needed to maintain proper focus over the entire screen by providing a voltage that increases with increased deflection to the Dynamic Focus Amplifier. The CORNER FOCUS adjustment sets the DYNAMIC FOCUS signal magnitude necessary to maintain a focused crt writing beam.

When DEFOCUS-0 is low (except in Hard Copy mode), the crt writing beam will be defocused. The use of the DEFOCUS-0 signal allows a focused or defocused crt writing beam in combination with WRITE-THRU, BRITE, and NORMAL intensities.

Control Grid DC Restorer

The Control Grid DC Restorer furnishes the grid voltage that controls the crt writing beam. The CRT BIAS adjustment provides a reference voltage to set the crt writing beam cutoff bias. The Z Axis Amplifier shifts this voltage to make the beam write on the crt face.

Focus DC Restorer

The Focus DC Restorer provides a controllable negative voltage to the focus electrode of the crt. The focus electrode voltage is set by the CENTER FOCUS adjustment and is shifted by the Dynamic Focus Amplifier as the writing beam is deflected.

Deflection Amplifier Board

The Deflection Amplifier Board does the following:

- Provides the crt with writing beam deflection and the dynamic focus necessary for information display and hard copy production.
- Produces a signal, SLU-0, to indicate to the Display Controller that a temporary wait is needed while the Deflection Amplifier catches up with the input information.
- Provides Antiburn protection to prevent crt phosphor damage due to a slow moving, high intensity beam.

Refer to the block diagram of the Deflection Amplifier Board, Figure 12-3. You may also want to refer to the instrument schematics which are blocked out according to circuit function. The Deflection Amplifier Board has five functions. These are:

- Channel Switch and Origin Shift
- Geometry and Focus Correction
- Deflection Amplifiers
- SLU Sensor

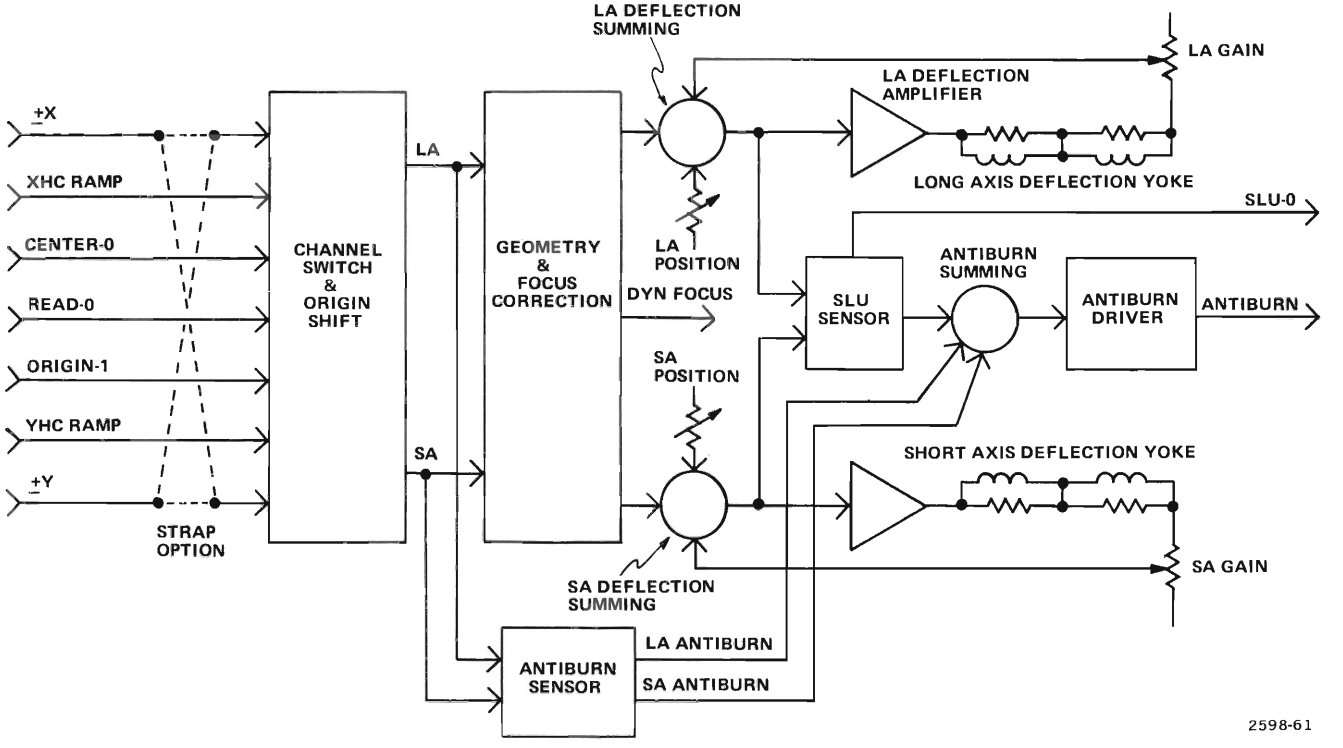


Figure 12-3. Deflection Amplifier Board Block Diagram.

Channel Switch and Origin Shift

The Channel Switch and Origin Shift block provides two analog signals (LA - Long Axis and SA - Short Axis) to the

Geometry and Focus Correction circuitry. The signal source is determined by READ-0 and HOLD-0. READ-0 is normally high and the Channel Switch and Origin Shifter then uses -X and +Y signal lines as the LA and SA signals. LA and SA are used in reference to the major axes of the crt face.

During hard copy operation, READ-0 goes low, and the Channel Switch and Origin Shifter then use XHC RAMP and YHC RAMP signals from the hard copy unit to provide the LA and SA signals.

Hold mode begins (crt operation is shifted to low intensity operation) when there is no crt input for 100 seconds. HOLD-0 goes low and connects the Channel Switch to a separate set of inputs that are at ground potential. The grounded inputs prevent beam deflection and make certain that there is minimum deflection amplifier power dissipation during Hold mode. Any keyboard operation or other input will bring the circuit out of Hold mode.

The Origin Shifter circuitry slightly moves the writing area on the crt to prolong the life of the crt phosphor. The Origin Shifter is an eight position binary counter clocked by ORIGIN-1, which comes from the Erase pulse. The output of the binary counter is fed through current dividers and then added to the LA and SA signals to modify the reference position for each new screen display of information. The eight positions of information ensure that no point on the crt is repetitively written. See Figure 12-4.

The Origin Shifter Circuitry is disabled by placing a low on the CENTER-0 signal line. With zero volts on the +X and +Y signal lines, the crt writing beam is centered on the crt.

Geometry and Focus Correction

The LA ands SA deflection signals are input to the Geometry and Focus Correction circuitry. Geometry correction is necessary to compensate for the "pin cushion" effect common with magnetic type deflection systems. See Figure 12-5. This circuit adds a voltage that varies according to the writing beam position to the LA and SA deflection signals, providing a compensated deflection voltage to the Deflection Amplifiers.

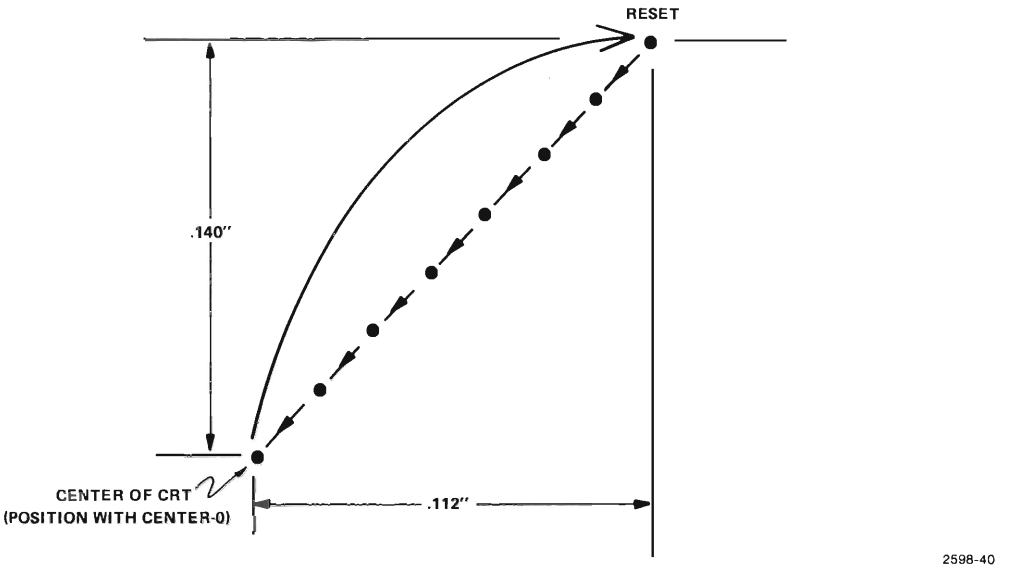


Figure 12-4. Origin Shift.

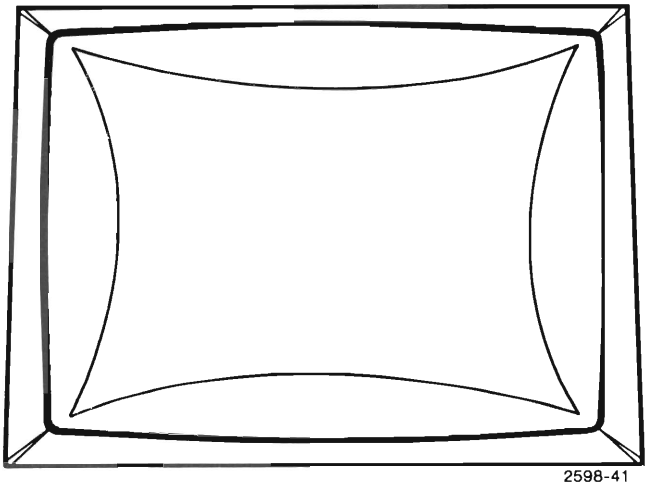


Figure 12-5. Pincushion Effects.

The Geometry and Focus correction circuit also produces a focus correction voltage. The length of the writing beam varies as it is deflected. This voltage (DYN FOCUS) compensates for focus changes caused by variations in the length of the writing beam.

Deflection Amplifiers

The Deflection Amplifier circuitry provides the deflection currents for the crt deflection yoke. The Deflection Amplifier circuitry consists of:

- LA (Long Axis) Deflection Amplifier
- SA (Short Axis) Deflection Amplifier

The four major adjustments on the Deflection Amplifier Board control the display size and position. LA POS and SA POS control the position of the displayed data. LA GAIN and SA GAIN control the width and height of displayed data.

The LA and SA Deflection Amplifiers are high gain current amplifiers that supply the drive currents to the deflection yoke. These yoke currents establish a magnetic field in the deflection yoke for crt writing beam deflection. Deflection coil currents are supplied by the +9 V and the -9 V supplies.

Input to the Deflection Amplifier is a summation of the following:

- The deflection signal from the Geometry and Focus Correction circuitry.
- The Position Current.

A change in the inputs to the summing point causes the output of the Deflection Amplifier to change, altering the crt beam deflection. The gain of the Deflection Amplifier is controlled by the GAIN adjustment which regulates the feedback.

SLU Sensor

The SLU sensor circuitry generates the output signal SLU-0 to the Display Controller. When low, SLU-0 indicates that the Deflection Amplifiers are lagging behind the input deflection signal and that they cannot accept additional data until SLU-0 goes inactive.

The SLU Sensor compares the outputs of the Deflection Summing Amplifiers against a threshold of about zero volts. The Sensor is active when either Deflection Summing Amplifier has an output other than zero. The voltage out of the Deflection Summing Amplifiers is zero when the proper deflection current is maintained in the deflection yoke. If the velocity of the input slew signal is higher than the Deflection Amplifiers can follow (about 60kcm/sec or 17kV/sec), the Deflection Amplifiers will lag behind and operate in an open loop manner until they catch up. SLU-0 prevents the Display Controller from beginning another move before the Deflection Amplifiers have caught up with the input signal.

STORAGE BOARD

Refer to the block diagram of the Storage Board, Figure 12-6. The Storage Board controls electrodes in the crt to store, view, and erase displayed information. The basic circuits of the Storage Board are shown in the block diagram.

The display is a bi-stable, direct view, storage crt. The crt display area has a glass front plate coated with a transparent conductive layer called the target backplate. The target backplate is covered with a layer of insulating phosphor called the target.

The information display target has two stable states, The flood gun electron beams establish the bistable operation of the phosphor. When the writing beam strikes the target phosphor, the target in the written area goes to a light emitting state. The flood guns keep the written areas in the light emitting state. The unwritten areas are close to the light emitting state, but need the extra input from the writing beam to change them to the light emitting state.

Operation of the storage circuitry is centered around the View-Erase Timer. This circuit consists of two divide-by-16 counters in series. These provide the timing for the Hold and Auto Erase functions. The View-Erase Multivibrator provides a 0.143 Hz square wave to the View-Erase Counter. This counter also has a Reset input from the View Mode Control circuit. One of the counter outputs is activated if 100 seconds elapse before a Reset occurs. The other output is activated if a Reset does not occur in about 30 minutes; when this happens, the screen is erased.

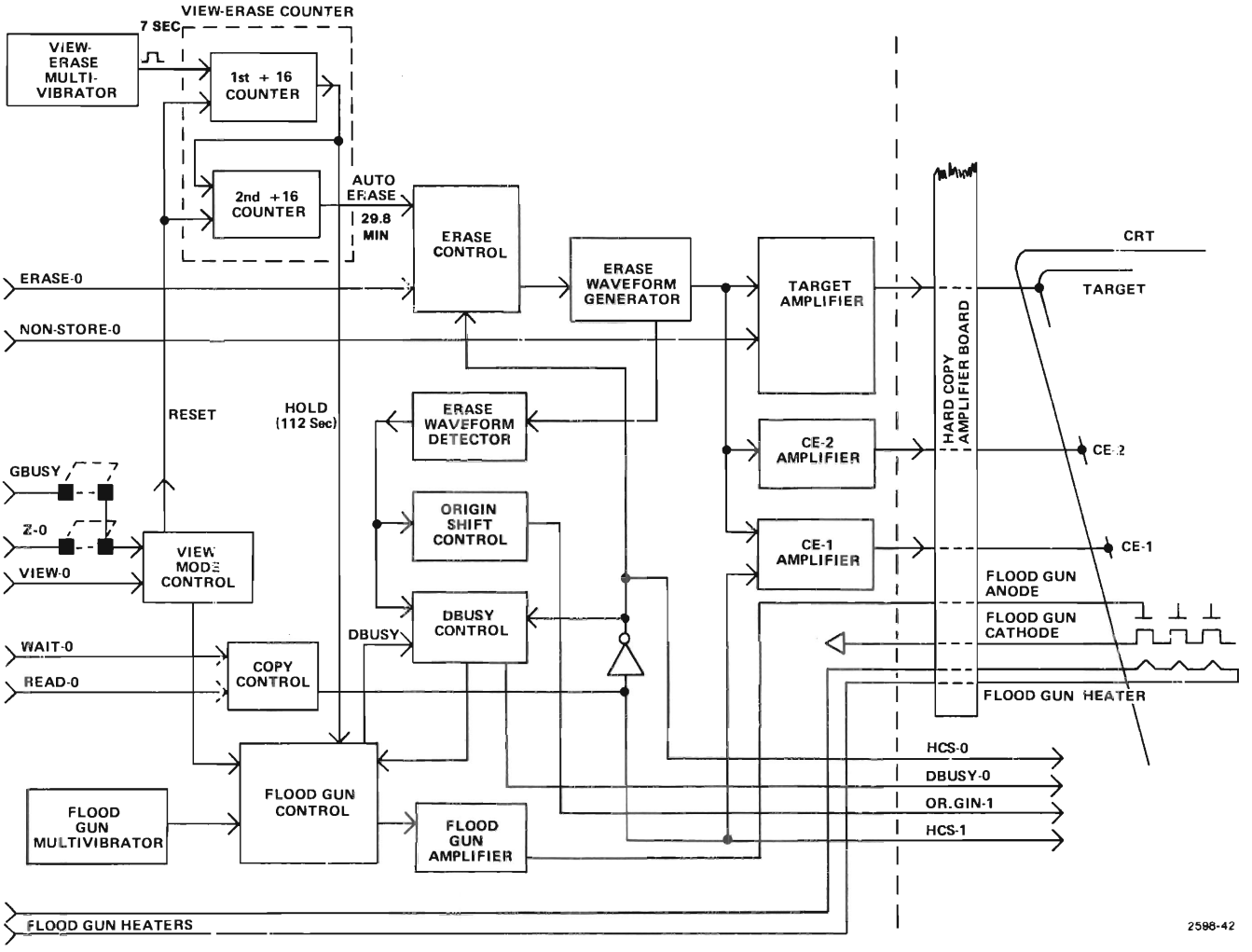


Figure 12-6. Storage Board Block Diagram.

View Mode and Hold Mode

As long as the View-Erase Counter receives an active Reset at least once every 100 seconds, the Storage Board circuitry maintains View mode. A Reset occurs from the View Mode Control when a GBUSY signal is received. The Flood Gun Control circuit then provides an output to the Flood Gun Amplifier, supplying voltage to the flood gun anode to maintain View mode.

The Flood Gun Control operates like a set-reset flip-flop. It is in a reset condition when the 4054 is in View mode. When the view/erase counter clocks through its count, indicating 100 seconds of inactivity, the HOLD-0 line goes active. The Flood Gun Control is then set and sends a 100 Hz signal to the Flood Gun Amplifier. This amplifier then pulses the flood gun anode at this rate, reducing the intensity of stored information.

During Hold mode, the Flood Gun Control circuit places a TTL low signal on the DBUSY-0 line. This tells the Display Controller that the system is busy and cannot accept further information until it is brought out of Hold mode and into View mode.

The Flood Gun Control circuit stays in Hold mode until reset into the View mode by a GBUSY signal or a low on the VIEW-0 signal line that goes to the View Mode Control. This is the same signal that resets the View-Erase counters.

A one-shot multivibrator in the DBUSY Control circuit extends the length of the DBUSY-0 signal for approximately 0.8 seconds longer than the Hold or Hard Copy Cycle. This allows time for the system to stabilize in View mode.

Auto Erase

An erase command can occur either automatically or by direct command from the keyboard.

The 100 second square wave signal that initiates the Hold Mode also starts a second divide-by-16 counter. When the Auto Erase output from this counter goes active after about 30 minutes, the screen is erased. The erase cycle is two complete erasures of the screen that are 100 milliseconds apart. The Target erase and the CE-2 erase signals go to the crt through amplifiers.

The erase signals going to the target or the CE-2 electrodes, first goes positive and floods the target. Then it drops to near zero volts to erase the target. After the erasure, it gradually returns to its operating level.

The Erase Waveform generator generates an ORIGIN-1 pulse and a 1.0 second low DBUSY-0 pulse each time the screen is erased. The ORIGIN-1 pulse goes to the Deflection Amplifier Board where it clocks the Origin Shifter circuit. The DBUSY-0 signal is used by the Display Controller as a flag against further input to the system. This allows time for the circuitry to recover after an erasure.

The circuitry has a guard against erasure when the second divide-by-16 View Erase Counter is reset by a low on VIEW-0. Without this protection, the counter could cause an undesired erasure of the screen before 30 minutes has passed.

Erase Command

An erase command can also come from the PAGE key via the Display Controller and the ERASE-0 line. A READ-0 or WAIT-0 signal from the hard copy unit prevents an erasure during Hard Copy operation.

Target Amplifier

The Target Amplifier provides the operating voltage for the target backplate. The target backplate voltage is about +170 V during the Storage Mode. See Figure 12-7. During the erase cycle, it increases by 150 V for 2 milliseconds. This writes the entire screen by providing additional electron potential between the target phosphor and the flood guns. At the end of this period, the voltage drops to zero, erasing the target phosphor. Then the target voltage returns to the operating voltage level at a slow rate so that the phosphor remains unwritten. There are two of these erase cycles during each screen erasure. The target backplate voltage can be set by the OP LEVEL for best storage.

Collimation Amplifier

The collimation electrodes CE-1 and CE-2 are electronic lenses that cause a uniform flood gun beam pattern over all areas of the target. The CE-1 voltage is set by the CE-1 potentiometer.

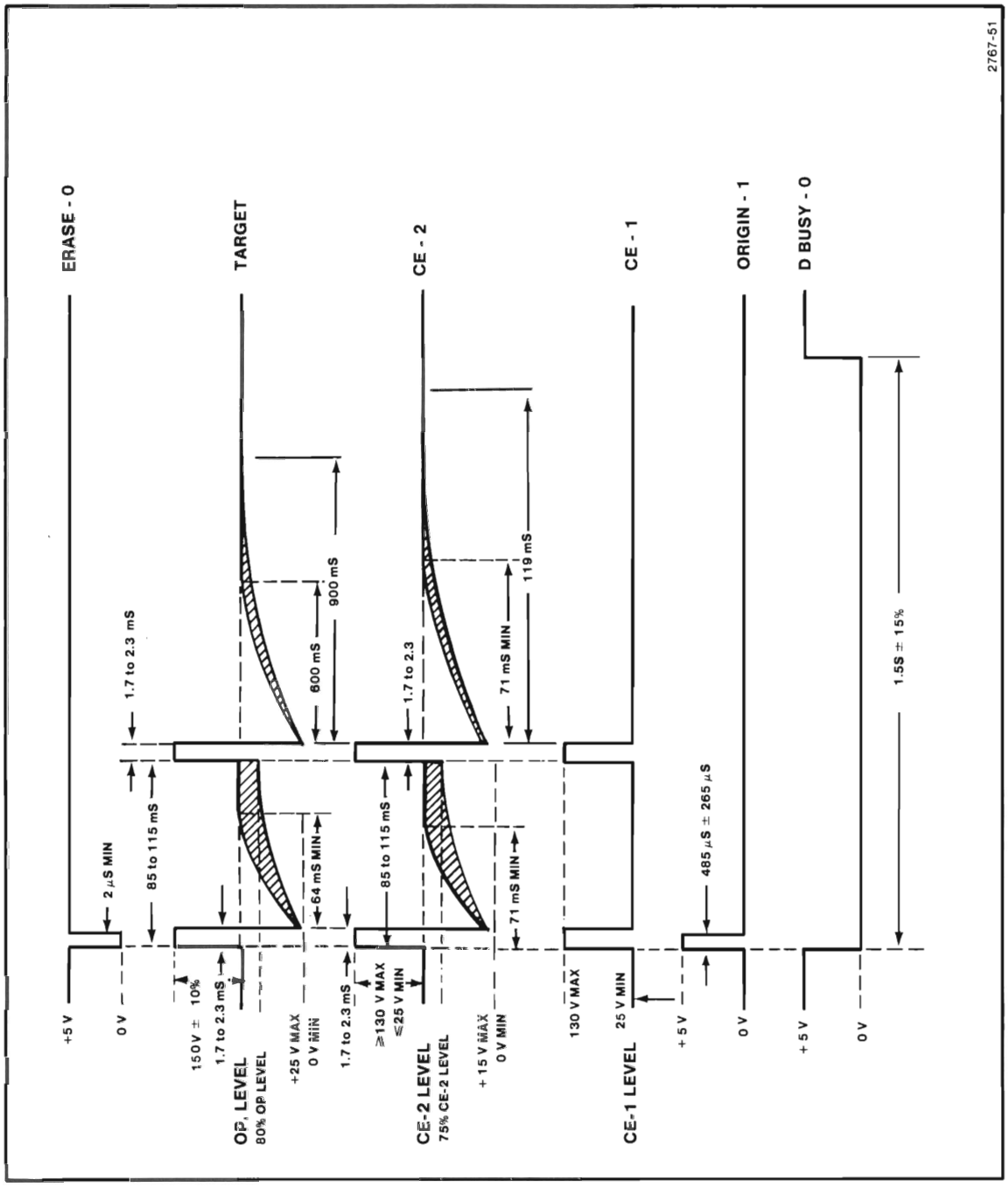


Figure 12-7. Storage Board Waveforms.

During an erase cycle, the CE-2 electrode has a voltage pattern similar to that on the target backplate. See Figure 12-7. First it increases by 25 V to 130 V for two milliseconds. Then it drops to zero and slowly returns to the operating level. The operating level is set by the CE-2 potentiometer.

During Hard Copy operation, +250 V is placed on CE-1 to prevent current oscillations within the crt that would degrade copy quality.

Hard Copy Operation

Stored information on the crt is recovered and amplified by the Hard Copy Amplifier. This display information is amplified and shaped to produce the TARSIG-0 output.

Whenever a hard copy is desired,the 4054 sends the MAKE COPY-0 signal to the hard copy unit. This generates several output signals. A READ-0 signal and, in the case of a hard copy unit with multiplex capabilities, a WAIT-0 signal go to the Storage Board, indicating that a hard copy is either being made or is about to be made. The HSC-0 (Hard Copy Switch) signal is produced by the Storage Board to enable the hard copy operation in the system. The Storage Board makes DBUSY-0 true to disable the Display Controller during hard copy operation.

The hard copy unit provides a negative going slow ramp, XHC RAMP, to the horizontal deflection circuit, causing one horizontal sweep for each copy made. As the slow ramp sweeps, a succession of fast ramps are applied to the vertical deflection circuits. When HCS-1 is high, the Channel Switch and Origin Shift select the XHC RAMP and YHC RAMP analog signals for the deflection circuit inputs. During each fast ramp, YHC RAMP, the hard copy unit supplies a repetitive interrogate signal HC INTER-0 to the Hard Copy Amplifier and to the High Voltage and Z Axis Board to turn on the writing beam. If stored data exists on the crt target at the position crossed by the writing beam, the resultant current in the target surface causes a TARSIG-0 signal from the Hard Copy Amplifier. This signal is used by the hard copy unit to reproduce on paper the image that is stored on the target backplate.

Vector Generator

The 4054 vector generator has an X and a Y channel. Since the circuitry in each channel is identical, only the Y channel will be discussed. The Y channel has six major sections (see Figure 12-8):

- An input buffer
- A rate multiplier
- An address counter
- A vector clipper
- A D/A converter and filter
- A speed compensator

Display Data Bus Receiver/Buffer

This buffer is a storage circuit for data from the I/O Board. This circuit stores data and isolates the twelve lines of data to the vector generator.

Rate Multiplier

A binary rate multiplier is like a programmable divider. The output frequency and pulse width are like that of the input signal, but with pulses missing to get the proper division. The number of pulses for a period of time is constant, but the rate of output pulses is not constant and pulse jitter from this circuit is normal. The input program lines (DD0 to DD11) make it possible to program the multiplier so that for every 64 input pulses a selected number from 0 to 63 output pulses are produced. Cascading two binary rate multipliers makes a range of 0 to 4096 pulses available.

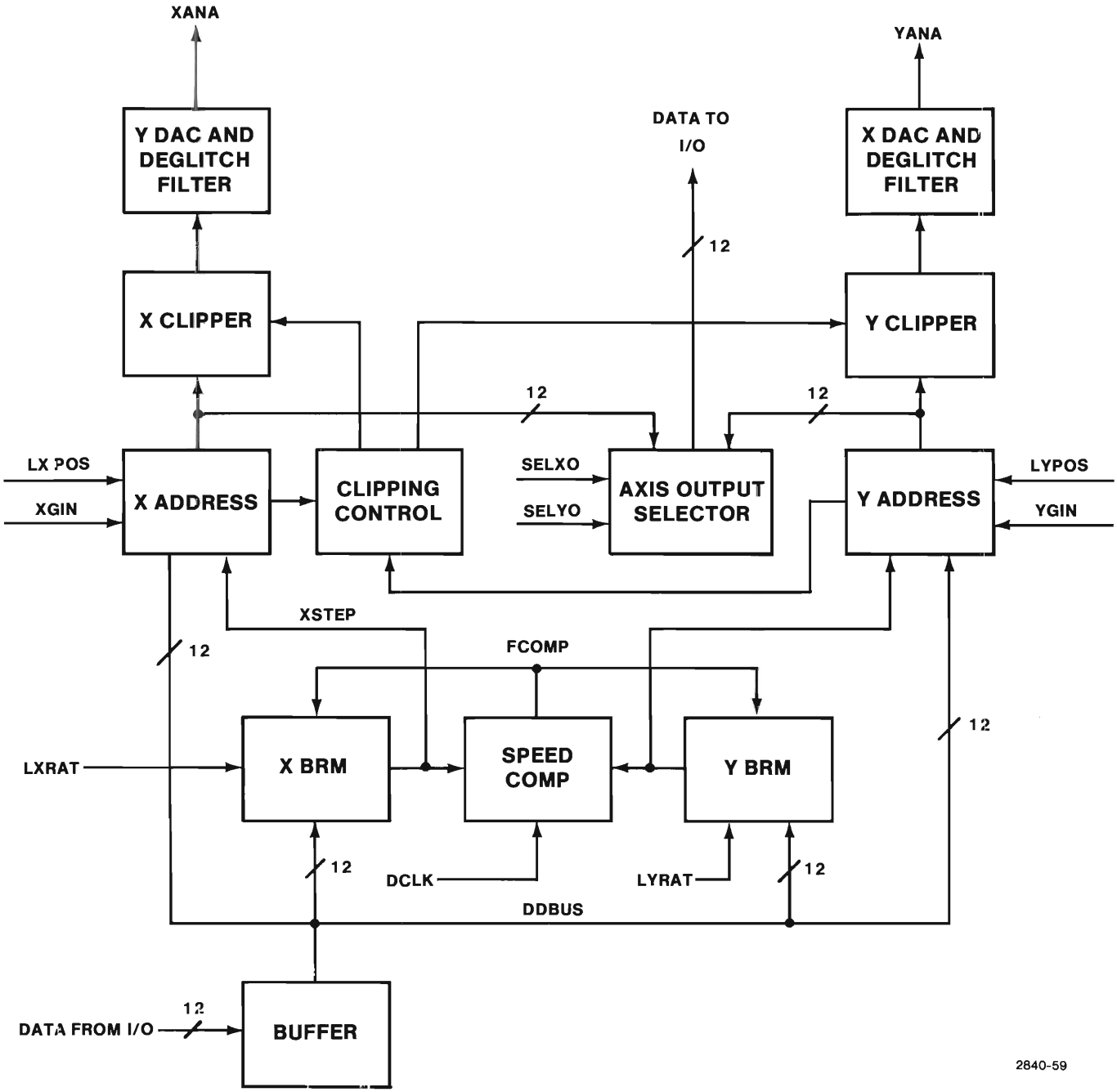


Figure 12-8. Vector Generator Block Diagram.

The Y STEP counter is clocked by the output of a 12-bit rate multiplier.

There are two inputs to the rate multiplier. One input comes from speed compensator circuit. The second input is the DD1 to DD11 data input from the buffer circuit. The Y multiplier output is CYSTEP. CYSTEP is a recurring signal that clocks the Y Step Counter. The frequency of this signal is determined by multiplying the frequency of the signal from the speed compensator by the DD11-DD0 data input and dividing the result by 4096. These two inputs determine how fast the beam is deflected to the new position.

Speed Compensator

The inputs to the speed compensator are CXSTEP and CYSTEP. This circuit is a shift register that remembers what has happened for the two preceding steps. It remembers whether X has stepped, Y has stepped, or whether both have stepped, and divides the input by a number from 1 to 4. Because both the XSTEP and the YSTEP signals are used as inputs to the speed compensator, a closed loop feedback path is established and ensures that the drawing speed for vectors is fairly constant. This results in stored vector lines that have a constant width.

Address Counter

The address counters are composed of three up/down counters with a total count capacity of 4096. The X-DIR and Y-DIR input lines determine whether the counters count up or down. Whenever the counters reach 000 or FFF, the carry/borrow output from the last counter sends a signal to the vector clipper which inverts the signal output from the clipper and

turns off the crt writing beam. The twelve lines of data into the counters determine the starting position of the vector. The lower left hand corner of the crt display corresponds to a count of 000. The upper right hand corner of the crt display corresponds to an X-AXIS count of 4096 and a Y-Axis count of 3150. Any Y-AXIS travel above the upper edge of the crt is clipped by the firmware. The CYSTEP-1 and the CXSTEP-1 signals determine the vector length from the starting point.

Vector Clipper

The Vector clipper circuit is composed of twelve exclusive "or" gates. Data from the counters is passed through them to the D/A converters. Normally the writing beam is enabled and the counter outputs are not inverted. When the address counters decrement past 000 or increment past FFF in their count, a borrow or carry output toggles the state of the clipper. This turns off the writing beam and inverts the outputs to the D/A converters. The deflection amplifiers are then kept from being driven beyond the edges of the crt target and drawing excessive current.

X and Y Address counters

The data contained in the X and Y Address Counters sets the position of the display's writing beam on each axis. Each move or draw operation changes the contents of the Address Counters to move the writing beam.

An absolute move loads a new 12-bit absolute address word directly into the X or Y Address Counters. The data word for the Address Counters comes on the DD11-1 to DD0-1 lines from the I/O board. The new position is immediately sent to the D to A converter and the outputs from the Vector Generator quickly move the writing beam to the new position.

A relative move or a draw changes the writing beam position one address unit at a time. Each unit of movement equals a single positive or negative change of the Address Counters state. Either the X or Y Address Counter is clocked once each timing cycle while a vector is being drawn. This clocking is controlled by firmware.

Vector address data is either positive or negative. Positive data for a particular axis causes the counter for that axis to count up. Negative data causes that counter to count down. The XDIR-1 or the YDIR-1 signals control the direction of count. The clocks to the counters are the CYSTEP-1 and the CXSTEP-1 signals from the Binary Rate Multipliers.

X and Y D to A Converters

The X and Y D to A Converters (Digital to Analog) translate the 12 bits of data from each Clipper Circuit into analog signals. Each D to A Converter is an integrated circuit module that contains no replaceable parts. The module's performance allows it to convert the input data to a settled output signal within the clock period of the Vector Generator. The outputs of the converters control the display's deflection circuitry. The output from the Converters ranges from -1.0 mA with all bits false to 1.0 mA with all input bits true.

X and Y Deglitch Filters

The X and Y filters amplify and smooth the output signals from the D to A Converters. The Filters use integrated and discrete devices to remove unwanted noise from the analog signal. The filters also allow high speed deflection during absolute moves. The outputs of the X and Y filters are X- and Y+. Normal signal outputs from the filters is +/- 5 V an the X output and +/- 3.75 V on the Y output.

Figure 12-9 contains some of the circuitry that is common to the X and Y Filters. The output from the D to A Converter is amplified by UA, a differential output wide bandwidth amplifier. The outputs of UA drive QC and QD. QE and QF form

a current mirror and a current sink for the differential pair. They are arranged so that a change in QC's collector current reflects into QF to stabilize gain. Capacitor CA charges or discharges to a level set by the signal amplified by QD. The charging and discharging of CA develops a voltage across the capacitor. The maximum rate at which CA charges or discharges is controlled by the current flowing through RB and QF. This limit on the maximum charging current for CA sets the maximum rate of change for the voltage across CA.

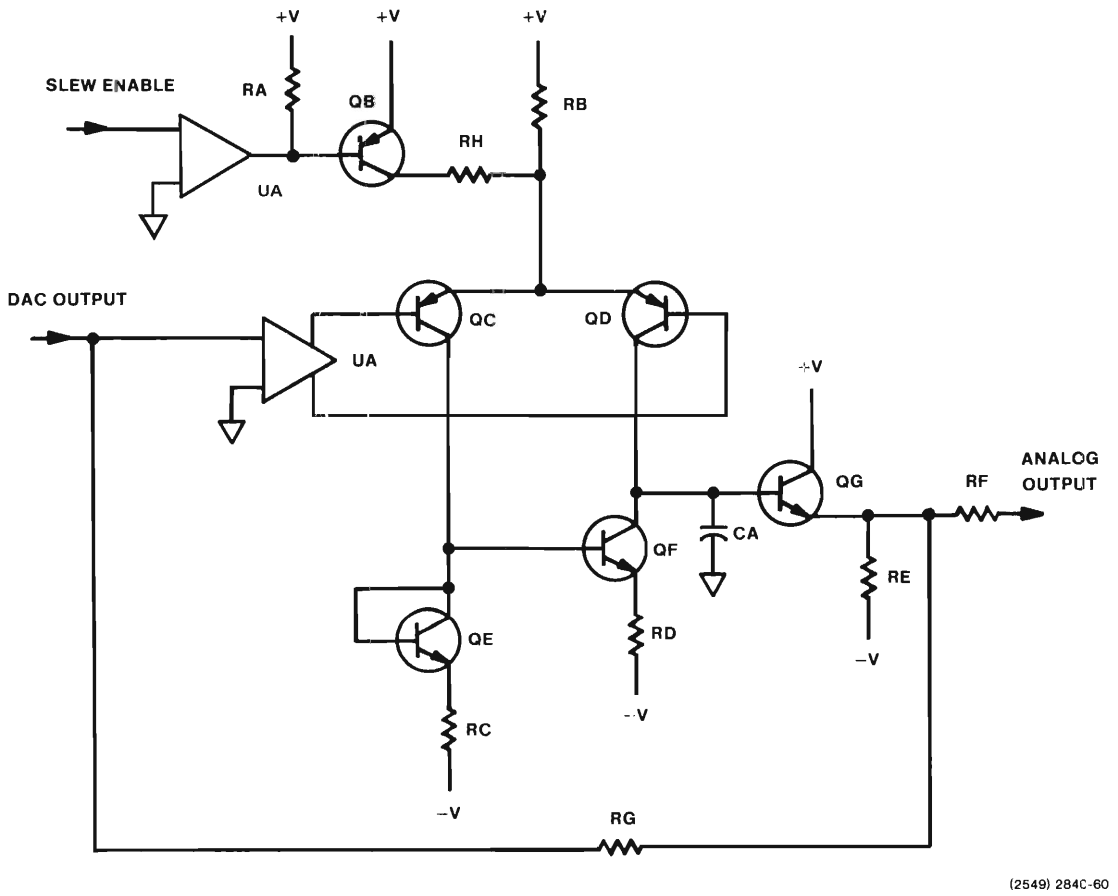


Figure 12-9. Details of X and Y Filters.

During absolute moves, NOLI-1 is true and QB supplies additional current through RH. With the increased current

available, CA can charge or discharge at a faster rate. This allows the filter to respond to large changes rapidly when noise suppression of the D to A converter output is not needed.

DISPLAY CONTROLLER

The Display Controller is made up of six main blocks (see Figure 12-10):

- Refresh Timer
- Clock Generator
- Control
- Vector Length and Direction
- Graphics Input (GIN) Control
- Z Axis Control

Refresh Timer

The Refresh Timer block is a divide by 256 circuit to divide the DSPRCK signal from the I/O Board down to the 37.5 Hz signal needed to clock the refresh timer. This circuit operates continuously with no reset. Its output goes to the display status buffer.

Clock Generator

The clock generator operates at 14.7456 MHz. It is followed by a divide by three circuit that has an output at 4.9152 MHz. DCLK and DSCLK have clock outputs of 14.7 MHz or 4.9 MHz, depending on the WRITETHRU line signal. The 14.7 MHz output is used during WRITETHRU. The DO2-1 and DO1-1 signals control the timing of the Control section of the Display Controller.

Three input signals to this section are BRESTART, VLCC, and CTLSTB. BRESTART is a signal from the Restart circuitry that sets initial conditions on power up of the instrument. VLCC (Vector Length Counter Carry) stops the clock outputs at the end of a vector. The other signal, CTLSTB-1 (Control Strobe) originates on the I/O Board while writing a display command to the I/O Board. The Display Controller starts to process a command on the first rising edge of CTLSTB-1.

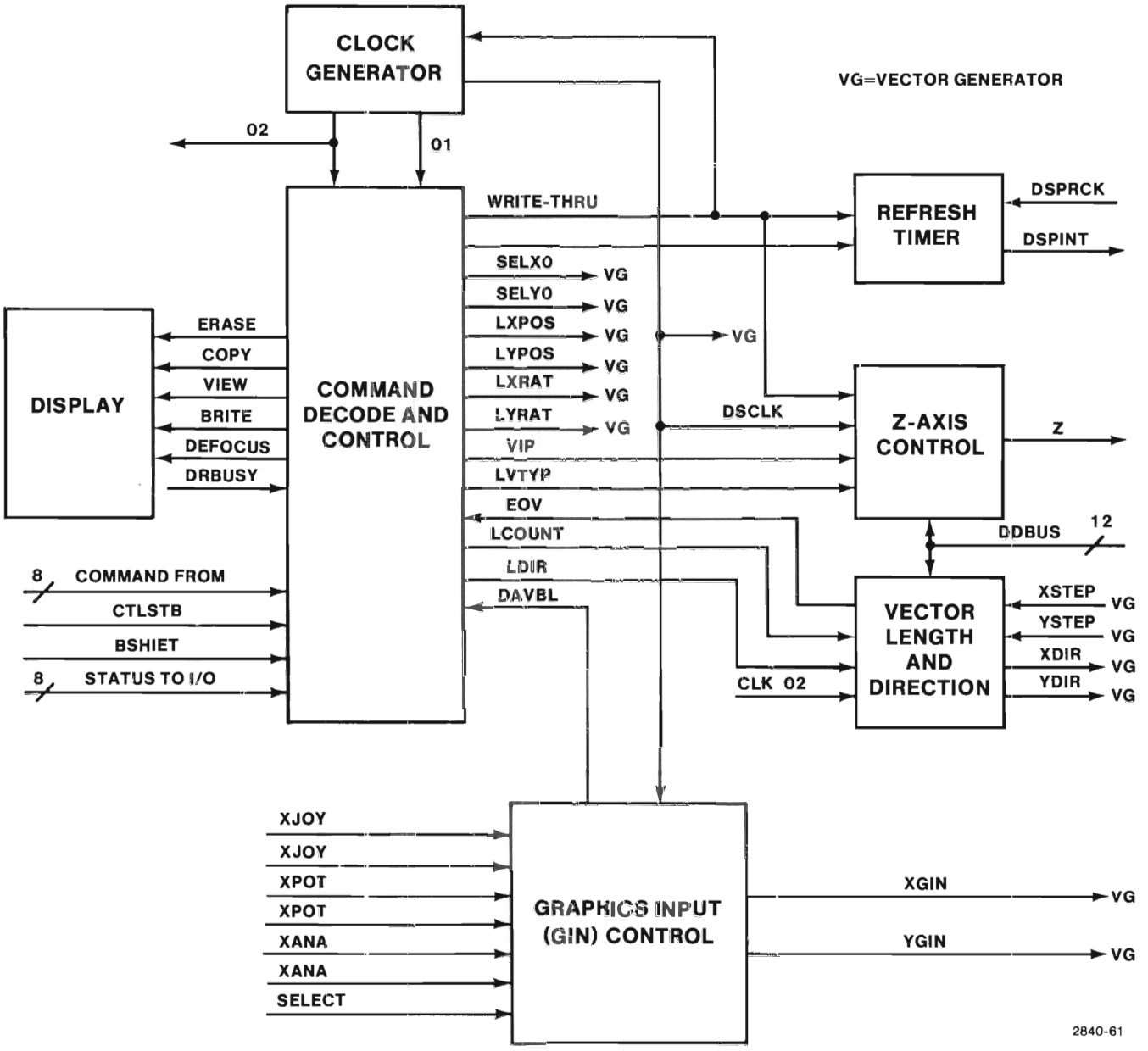


Figure 12-10. Display Controller Block Diagram.

Control

The primary function of this section is to decode the control commands from the I/O Board and direct them to the proper section of the instrument display.

There are eight display control lines (DCTL0-DCTL-7) and CTLSTB-1 (Control Strobe) coming from the I/O Board. The processing of I/O commands begins on the rising edge of the Control Strobe. The eight control lines come into a tri-state buffer and then go to three decoders. BRITE-1, DEFOCUS-1, WRITETHRU-1, DRL-1, DRM-1, and VIP-1 are all stored in quad latches because they are continuous commands. VIEW-0, MAKECOPY-0, and ERASE-0 all go through pulse stretching multivibrators. LCOUNT-0 and LDIR-0 go to the Vector Length and Direction section. The rest of the lines go to the Z Axis and High Voltage Board to control the writing beam focus and intensity.

A tri-state latch monitors the status of the decoder outputs and passes this information back to the I/O Board for display status information as DSTAT0 - DSTAT7.

Vector Length and Direction

The Vector Length and Direction circuit determines when a vector has reached its end and stops the vector at that point.

There are five main inputs to this part of the circuit, CXSTEP, CYSTEP, LCOUNT (Load Count), LDIR (Load Direction), and 12 lines of Display Data from the I/O Board, DD1-11. In addition, the four least significant bits of data contain extra information. The zero bit indicates whether the X Axis or the Y axis is the longest part of the drawn vector. A 1 indicates that the X axis is the longest vector. Number one bit indicates whether the X direction is positive or negative. A one on this bit indicates that the X direction is to the right or positive. A one on the number two bit indicates that the Y direction is negative. A one on the number three bit indicates that the instrument is making an absolute move, a zero indicates that a vector is being drawn.

The DD0-DD11 lines from the I/O Board load the count of the vector length into the three vector length counters when the LCOUNT (Load Count) line goes high. The zero bit of data tells whether the longest vector is the X axis or the Y axis, and selects the CXSTEP (Counter X Axis Step) or CYSTEP (Counter Y Axis Step) to clock the programmable counter. When the counter reaches a full count, output signals EOVT (End Of Vector) and VLCC (Vector Length Counter Carry) turn off the Display Controller clock output and reset the vector length control counter.

If the crt beam is turned on and off too fast with a very short vector, nothing will be seen. To remedy this, a turn-off delay circuit is used to extend any writing time so that the screen will have time to store the information.

Graphics Input (GIN) Control

The GIN control section of the Display Controller Board takes the input voltages from the thumbwheels on the keyboard or the external Joystick and uses these voltages to move the position of the GIN crosshairs on the screen of the 4054. The SELECT-C line is true when the Joystick input is selected.

The voltages from the thumbwheel or Joystick potentiometers are divided and sent to the input of operational amplifiers. The +Y and the -X outputs from the Vector Generator board go to the other inputs of the operational amplifiers. When the inputs of the operational amplifier cross the same voltage level, the output of the operational amplifier switches polarity quickly.

In GIN mode, the clocks to the X and Y Address counters run, causing the Vector Generator outputs to change. The crt beam is deflected, but the beam is not turned on. The changing levels at the Vector Generator outputs are sent back to the operational amplifier inputs. When the operational amplifier input voltage coincidence occurs, a pulse is sent from the GIN circuit to the X and Y Address counters that stops the clock and the deflecting voltage at that point.

The circuitry following the operational amplifiers alternately selects the X and Y position outputs and insures that the output pulse that stops the Address counter occurs at the proper time. The XGIN and YGIN outputs go to the vector clippers to stop the vectors and turn off the writing beam of the crt. The DAVBL output goes to the status register to be sent to the I/O Board.

Z Axis Control

The Z Axis control circuitry turns the writing beam of the crt off and on at the proper time. A turn on delay circuit makes certain that the beam stays on long enough to write the crt phosphor and doesn't turn on until the beam starts moving. WRITETHRU-1 causes the crt beam to turn on hard enough to be seen on the phosphor, but not quite hard enough to store on the phosphor.

Two divide-by-256 circuits provide clock inputs to the shift registers. The data line inputs to the shift registers determine whether the written vector on the crt is a solid line or one of several combinations of dot-dash vectors.

Input/Output Board Circuitry

The I/O Board controls the input and output data timing and direction for the 4054 Graphic Computing System. It controls the tape drive, the GPIB connected peripherals, the backpack

peripherals, and information from the keyboard. There are several sections to the I/O Board (see Figure 12-11):

- Power Supply
- Restart Circuitry
- Default Parameters
- Address Decoders
- Clocking Circuitry
- I/O Board GPIB Interface
- Display Interface
- Keyboard Interface
- Magnetic Tape Control Circuitry

Power Supply

There are two power supplies on the I/O Board. The operation of these supplies is described in the 4054 power supply section.

Restart Circuitry

This circuitry is described in the 4052 power supply section.

Default Parameters

The Default Parameters section of the I/O Board has several straps that are preset to initialize the circuitry to print character size 4 and font 0 when the system is turned on.

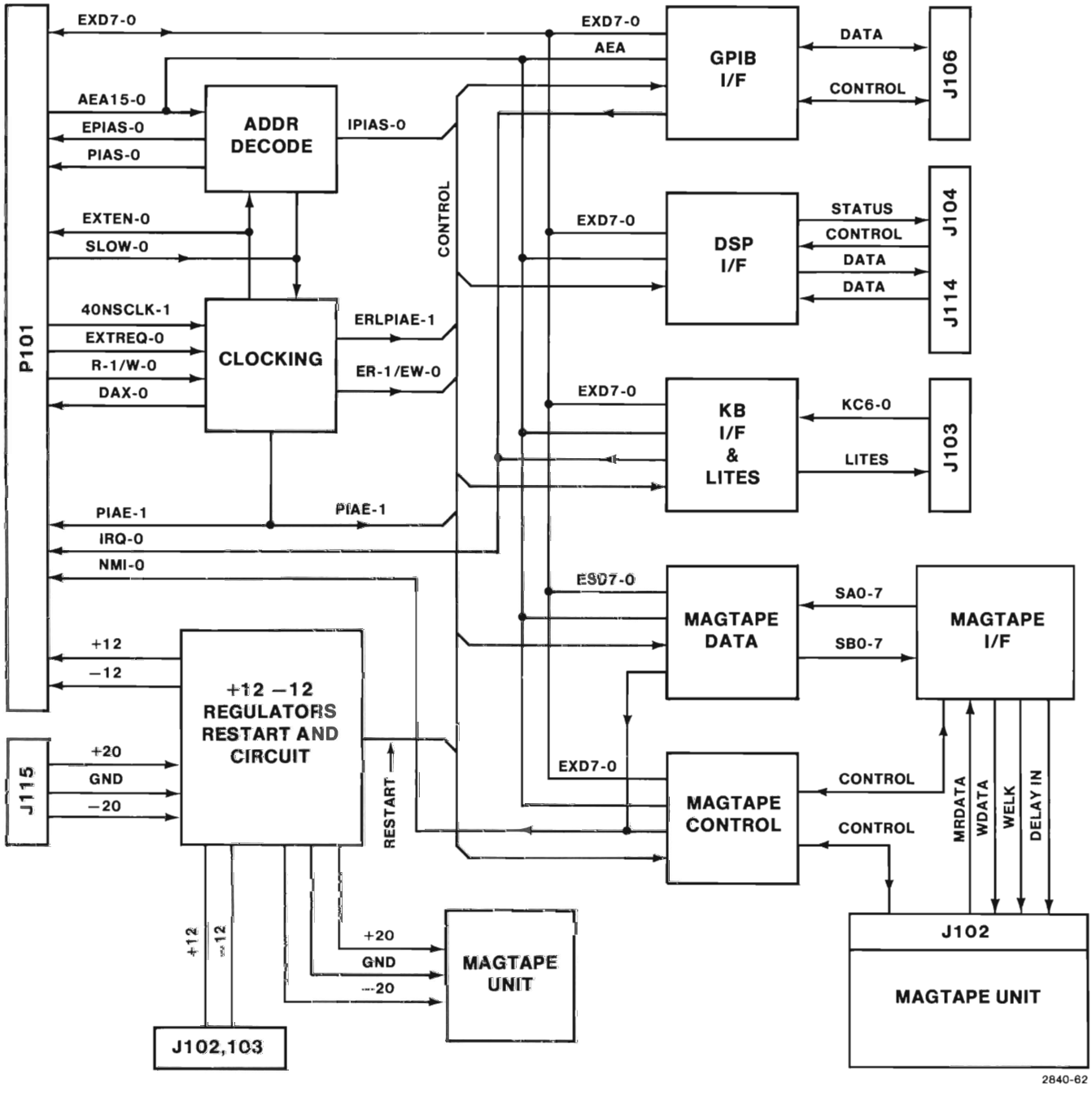


Figure 12-11. I/O Board Block Diagram.

Straps A and B determine the print size. They are set to binary 11 which is size 4 (00 is size 1). A is the least significant bit and B is the most significant bit.

Strap C is "WHO". The low or "0" strap is for the 4054. A "1" or high would indicate a 4052.

Strap D is reserved for future use.

The straps E,F,H, and J are strapped to font 0 (0000). They may be changed for any font from 0 through 8. E is the least significant bit and J is the most significant bit. To change these straps, the printed circuit runs must be cut with a sharp instrument. Wire straps can then be inserted in the holes provided to preset the desired default parameters.

Address Decoder

The Address Decoder in the I/O Board circuitry is used to decode the I/O address lines from the MAS Board (Memory Access Sequencer). From these lines the decoder logic generates two main signals, PIAS-0 (Peripheral Interface Adapter) and EPIAS-0 (External Peripheral Interface Adapter). PIAS-0 is the signal that determines whether the PIAE (Peripheral Interface Adapter Enable) high state is extended for slow peripheral devices or not. The EPIAS-0 signal is used to select external ROMPACKS and other peripherals.

Clocking Circuitry

The Clocking Circuitry provides the proper timing for peripheral devices such as peripheral interface adapters and asynchronous communication interface adapters.

The circuitry is primarily made up of three shift registers. Under normal conditions, the time that it takes the input 40 ns clock to pass through the six sections of the first shift register determines the low time of the PIAE (Peripheral Interface Adapter Enable) signal. When the signal comes out of the first shift register, the signal shifts the PIAE line flip-flop to its high state. It remains in its high state until the signal also passes through the second shift register. At that time, all of the registers will be reset to their original state.

If either PIAS-0 or SLOW-0 signals are turned on, the high state of the PIAE signal is extended by about 240 ns. The extra time is introduced by the addition of a third shift register in series with the second shift register. This approximately doubles the PIAE signal "on" time. It is used to extend the on time for external devices that operate slowly.

I/O Board GPIB Interface

The GPIB interface section of the I/O Board is the interface between the GPIB connector and the MAS Board external data bus lines. The MAS Board external data bus lines are EXD0-1 to EXD7-1. The GPIB connector lines are DIO1-0 to DIO8-0.

The circuitry is composed of buffers, bidirectional latches and command decoding circuitry to control the direction of data flow. The bidirectional buffers are specially designed for GPIB requirements. The control signals to the decoder are six address lines from the MAS Board (AEA0-5), two read/write lines (ER/EW), and two peripheral interface adapter select lines (ERLPIAE and IPIAS). For additional GPIB operation see Section 10.

Display Interface

The Display Interface section of the I/O Board combines the read/write lines (ER/EW), the peripheral interface address lines (RD0-RD11), and the MAS data lines (DSTAT0 to DSTAT7) to control the data flow between the Display Controller Board and the Vector Generator. The decoding logic multiplexer controls the storage registers and buffers that pass the data between these two boards.

Keyboard Interface

The Keyboard Interface section of the I/O Board is made up of a peripheral interface adapter chip and current drivers to the status indicator lights. The interface adapter chip performs the TTY conversion of all letters to upper case and the combination of the CTRL (CONTROL) key with other keys for other ASCII characters and functions. The paralleled drivers are for the Busy, Break, and I/O lights on the Status Indicator Board. The inputs from the keyboard are KC0-KC6, KEY-1, TTY-0, and CTRL-0.

Mag Tape Control

The Mag Tape Control section of the I/O Board controls the operation of the tape drive unit. It decodes the control data, determines whether the tape drive unit is ready to receive or send data, and directs the data to or from the tape drive unit in read or write operations. It also converts the parallel data from the I/O Board to serial data for the tape drive unit and converts the serial data from the tape drive to parallel data for the I/O Board data input. In addition, the circuitry detects the beginning or ending of files and, together with the system's firmware, determines which file is being read from or written to.

Refer to Figure 12-12 for the circuit block diagram.

During a tape read cycle, two signals come from the tape unit read circuitry. They are RCLK (Read Clock) and MRDATA (Magnetic Tape Read Data). The Read Clock signal shifts the serial data from the tape into a shift register to provide it in eight-bit parallel form for the PIA.

The read clock timing circuits check the RCLK timing sequences to decode RMARK (End of Record), FMARK (End of File), and the beginning of data information. The 40 microsecond monostable multivibrator times out if a data gap equal to or larger than an intercharacter gap is found. The bit counter following the 40 microsecond multivibrator makes the RDBYTE (Read Byte) signal low during data read operations. After the last data bit is loaded into the read data register, RDBYTE again goes high. The ICG (Intercharacter Gap) counter interprets four consecutive intercharacter gaps as a record mark and eight intercharacter gaps as a file mark.

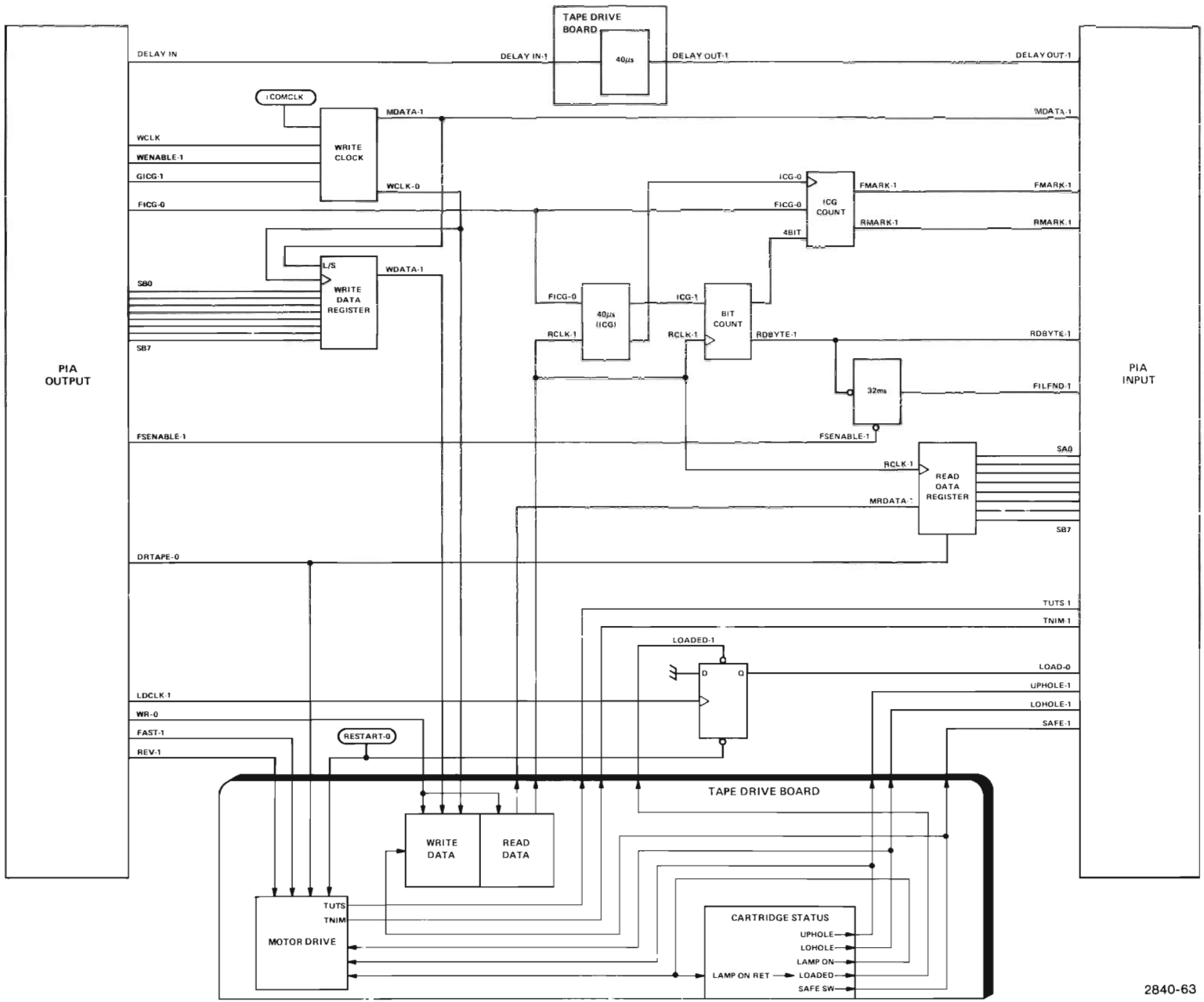


Figure 12-12. Mag Tape Block Diagram.

Interfile gaps are found by a 32 millisecond monostable multivibrator. The multivibrator is reset by a fast search enable signal from the command decoding PIA, and it is triggered by RDBYTE (Read Byte). The output, FILEFOUND, goes high after 32 milliseconds.

During a write cycle, there are two inputs to the tape. One input is WCLK (Write Clock). The frequency of COMCLOCK is divided down to become WCLK. WCLK strobes the write data onto the tape. The other input is WDATA (Write Data). This serial information is to be written on the internal magnetic tape. Eight lines of parallel data are loaded from the PIA into a shift register and clocked out in series for WDATA information to the tape drive unit. Refer to Figure 12-12 for the block diagram of the circuit.

Additional information is contained in section nine, the Tape Unit Theory of Operation.

Section 13

4052 POWER SUPPLY THEORY OF OPERATION

The 4052 power supplies provide the necessary regulated voltages for the operation of the instrument. There are five major regulated supplies in the instrument. They are:

+15 V Supply.
+12 V Supply.
-12 V Supply.
+5 V Supply (Switching Power Supply).
This supply is the same as the 4054 +5 V power supply and is described in that section.

High Voltage Supply.
This supply is described in the 4052 Display Theory of Operation, Section 11.

The Power Supply section also contains the restart circuitry for the instrument.

The basic circuitry is the same for three supplies, +15 V, +12 V, and -12 V.

The circuit has two operational amplifiers and two transistors. The overcurrent detector is an operational amplifier, OC. Normally this amplifier operates with the plus input more positive than the minus input. The output rests at a voltage near the +19 V supply potential. If the voltage across the low resistance ,RS, in series with the output becomes high enough to raise the minus input to a more positive potential than the plus input on the operational amplifier, the output will switch to a negative potential and reverse bias D1. This reverse bias will disconnect the voltage regulator from the circuit and hold the output at a safe level until the excessive current drain is reduced.

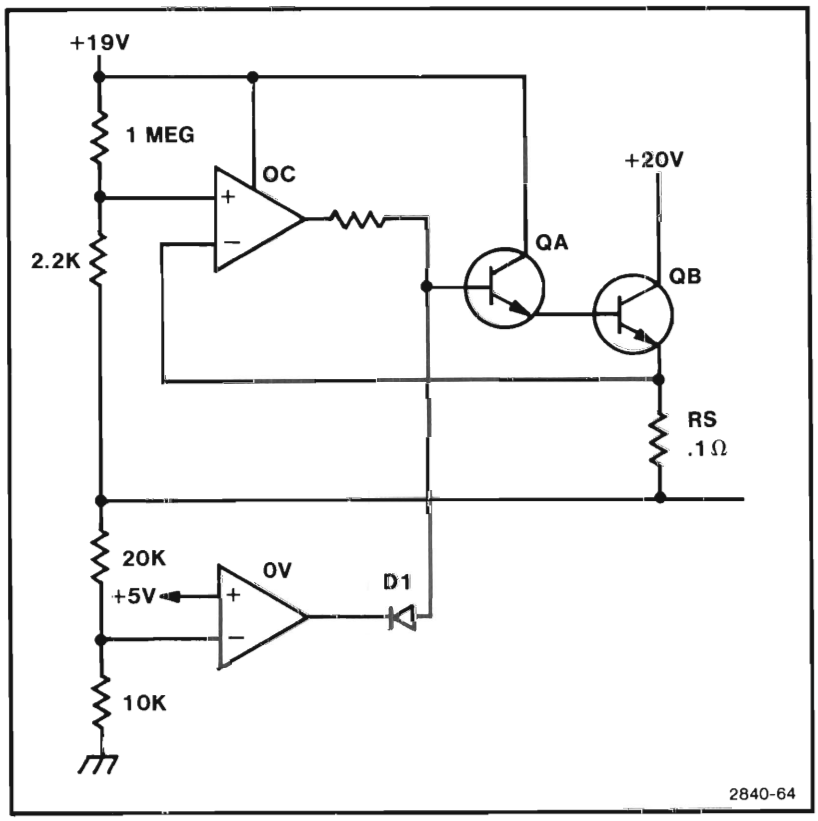


Figure 13-1. Twelve Volt Regulator.

When the output voltage drops with the pull down action of the over-current detector, this lower voltage is also fed back to the positive input of the over-current detecting operational amplifier to switch even more toward a negative output. This results in a "foldback" action which protects the regulator circuit from excessive current.

In normal action, the output of the over-current detector is near 19 V. D1 is forward biased. The output voltage level is monitored at the negative input of 0V, the voltage-sensing operational amplifier. It compares the voltage divided down to this input with a 5 V level at the positive input. Any difference with this comparison voltage is amplified, inverted, and fed back to the series voltage regulator to cancel out the difference. This makes the power supply output remain at a constant voltage.

RESTART CIRCUITRY

The purpose of the restart circuitry is to generate a RESTART-0 signal that will initialize the Graphic Computing System to its start-up conditions. This circuit holds RESTART-0 low until the power supplies are stable. When the power is turned off, it also turns the RESTART-0 signal on while the power supplies are still stable.

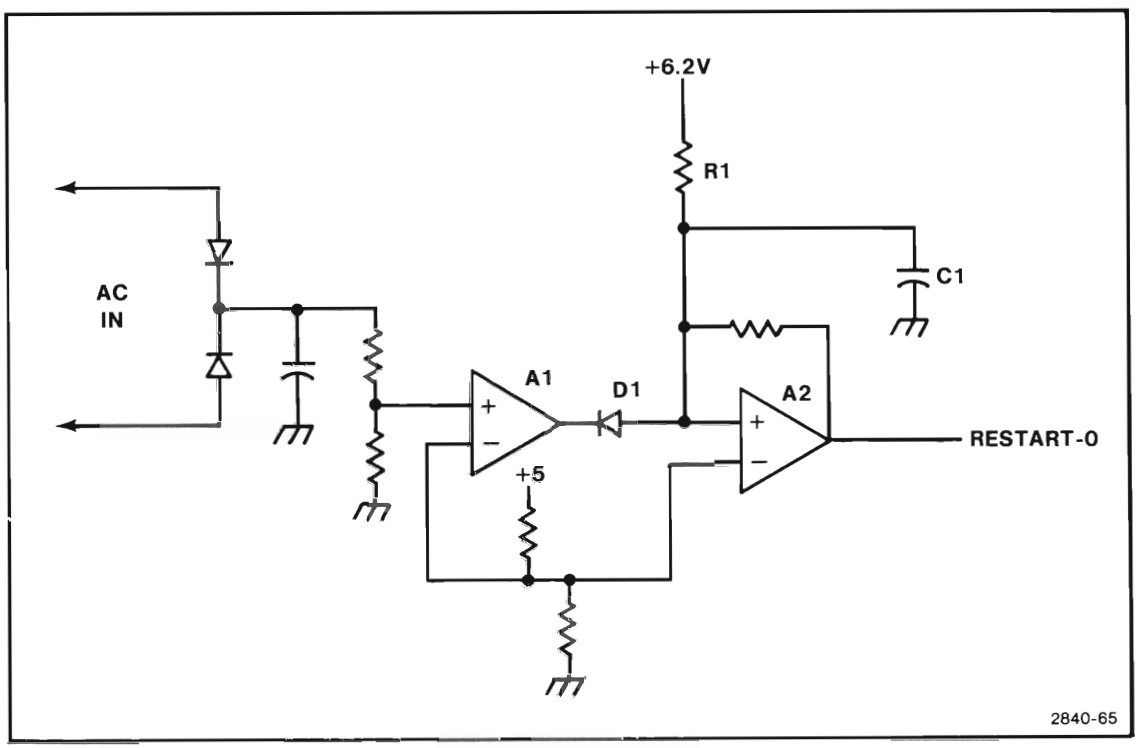


Figure 13-2. Restart Circuitry.

When the power is turned on, the rectified AC at the input of the operational amplifier, A1, switches its output to a maximum positive state. This reverse biases the coupling diode, D1, at the positive input of A2. The positive input of A2 gradually becomes positive at a rate determined by R1 and C1. When this positive voltage passes about 2.5 volts, the output switches in a positive direction terminating the RESTART-0 signal.

When the instrument is turned off, the positive input of A1 drops quickly and switches its output in a negative direction. This turns on D1 and discharges C1. A2 then switches its output to a negative voltage and generates the RESTART-0 before the power supply capacitors have discharged.

Section 14

4054 POWER SUPPLY THEORY OF OPERATION

The power supplies of the 4054 provide regulated voltages for the circuitry. The major regulated supplies are described here. Unregulated supplies and single-zener-regulated supplies are not described.

+15 V SUPPLY

The +15 V (Figure 14-1) supply obtains its power from the +20 V unregulated supply. This regulated supply provides the reference voltage for some of the other regulated supplies in the instrument. Whenever the +15 V supply is adjusted, some of the other regulated supplies will also change their voltages.

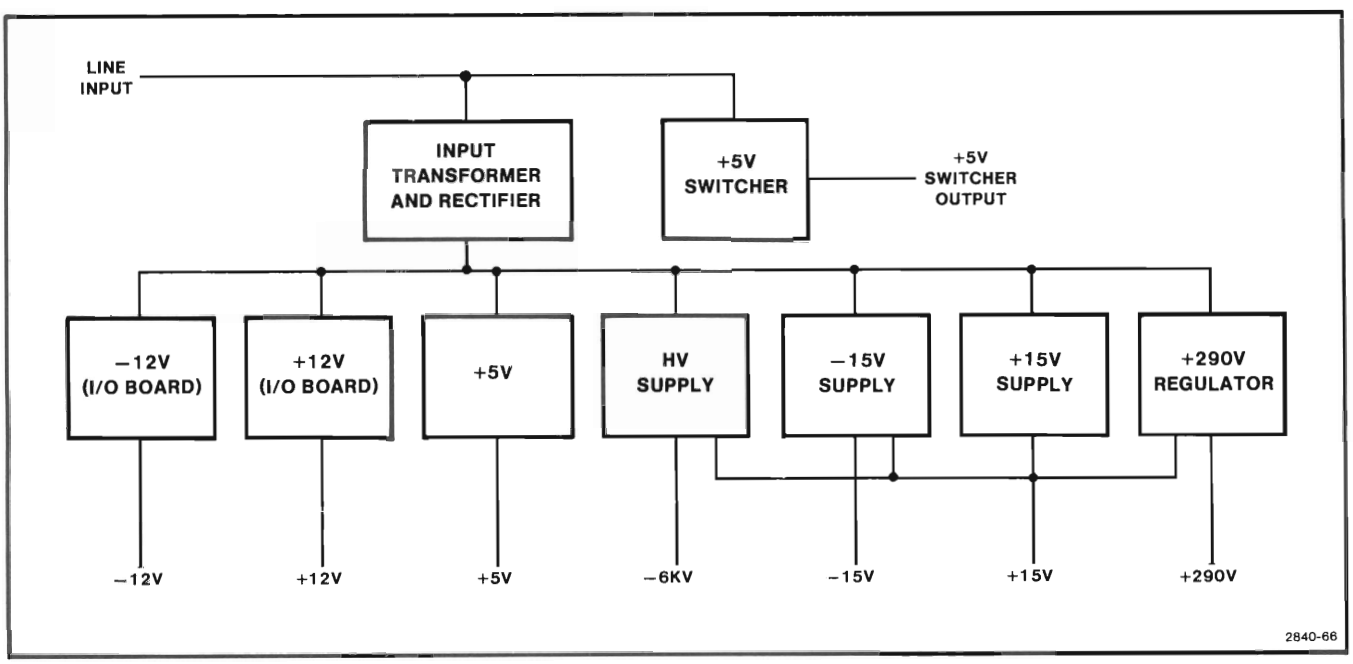


Figure 14-1. Power Supply Block Diagram.

This supply (Figure 14-2) has a precision voltage regulator containing its own reference voltage and current limiting circuitry. The output from this circuit goes to a driver transistor, QA, which controls a series pass transistor, QB. A current-sensing resistor, RS, in series with the collector of the pass transistor, develops a control signal that is sent back to the regulator. This feedback limits the available current if excessive current is drawn from the supply. The regulator is adjustable so that it can be set to +15 V.

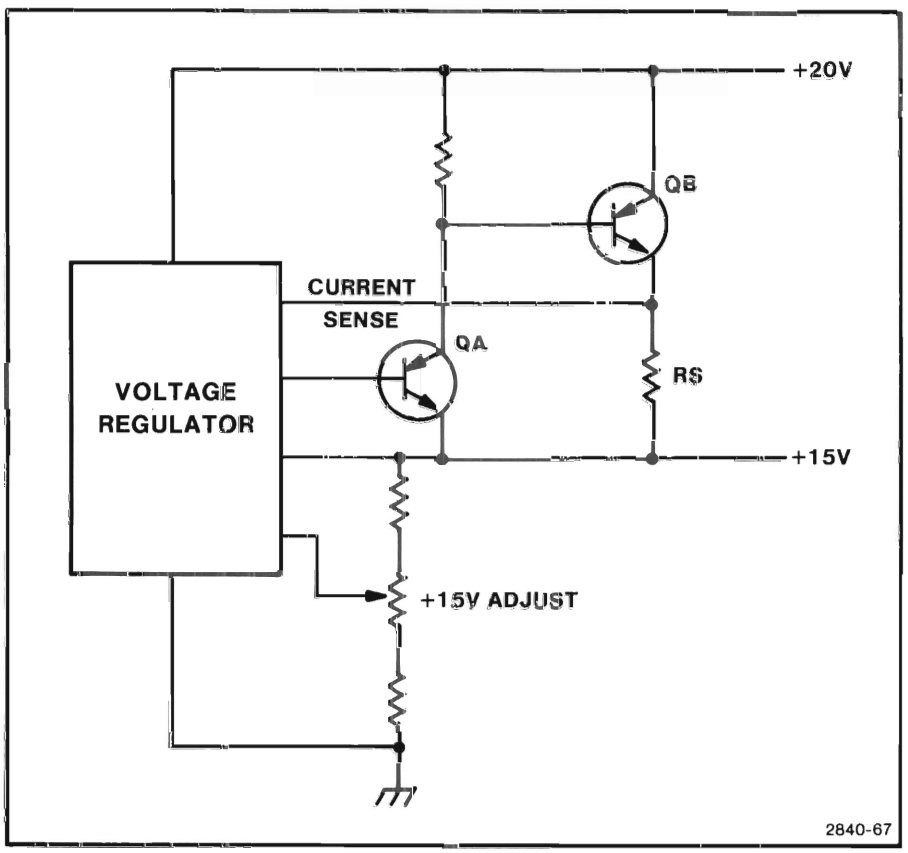


Figure 14-2. +15 V Regulator.

-15 V SUPPLY

The -15 V supply (Figure 14-3) gets its power from the -20 V unregulated supply. It uses a reference voltage from the +15 V supply for voltage comparison. Sample voltages from the +15 V and -15 V supplies are compared at the inputs of an operational amplifier (UA). The amplified difference voltage is coupled through a voltage offset Zener (Z1) to a Darlington series regulator transistor,Q1. Any change in supply output voltage is inverted and amplified by the operational amplifier to change the signal at the base of the series regulator and cancel the change. A second transistor, Q2, senses the voltage across RS. When the current through RS is enough to turn Q2 on, its collector current reduces the input voltage to the series regulator, Q1, reducing the input to a safe level until the cause for excessive current is removed.

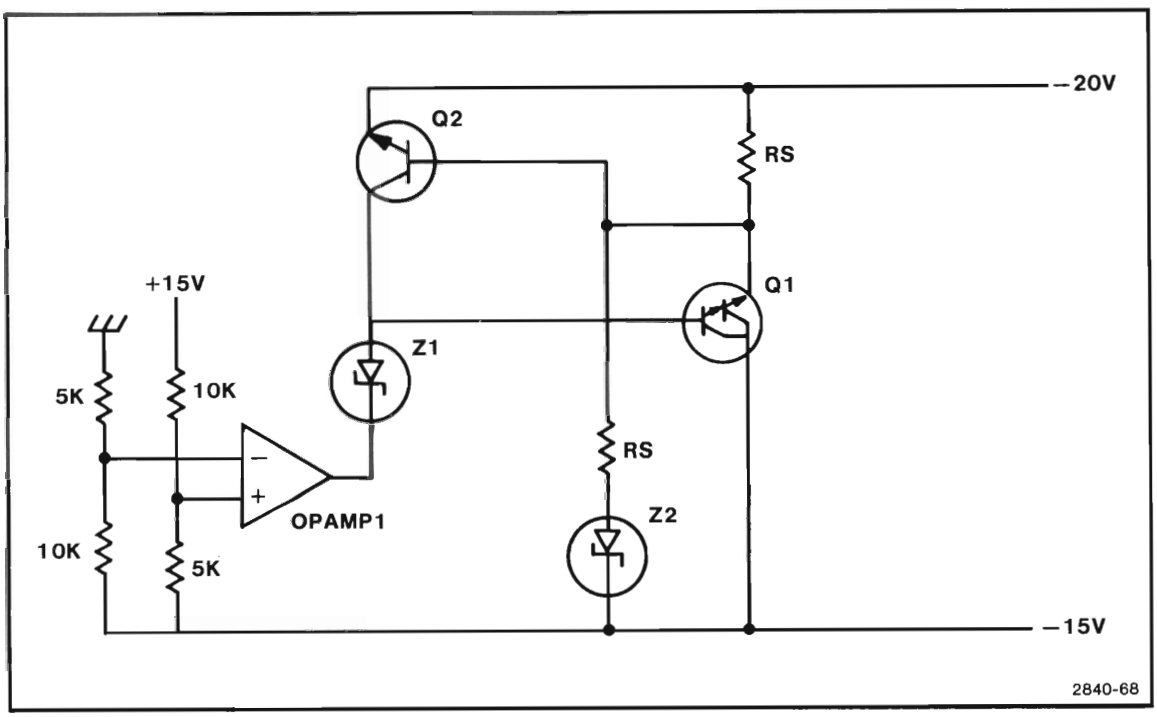


Figure 14-3. -15 V Power Supply.

If the voltage difference between the unregulated -20 V and the regulated -15 V exceeds approximately eight volts, Z2, a 7.5 V zener diode, conducts and provides current limiting also.

+5 V HIGH EFFICIENCY POWER SUPPLY

The +5 V high efficiency power supply supplies most of the +5 V power for the 4054. The supply (Figure 14-4) has a rectifier that runs directly from the power input lines and supplies power to switching transistors. These transistors drive an output transformer at about 20 kHz. The transformer output is rectified, filtered and regulated for use in the 4054. The supply is protected against low input line voltage, high output voltage and excessive output current.

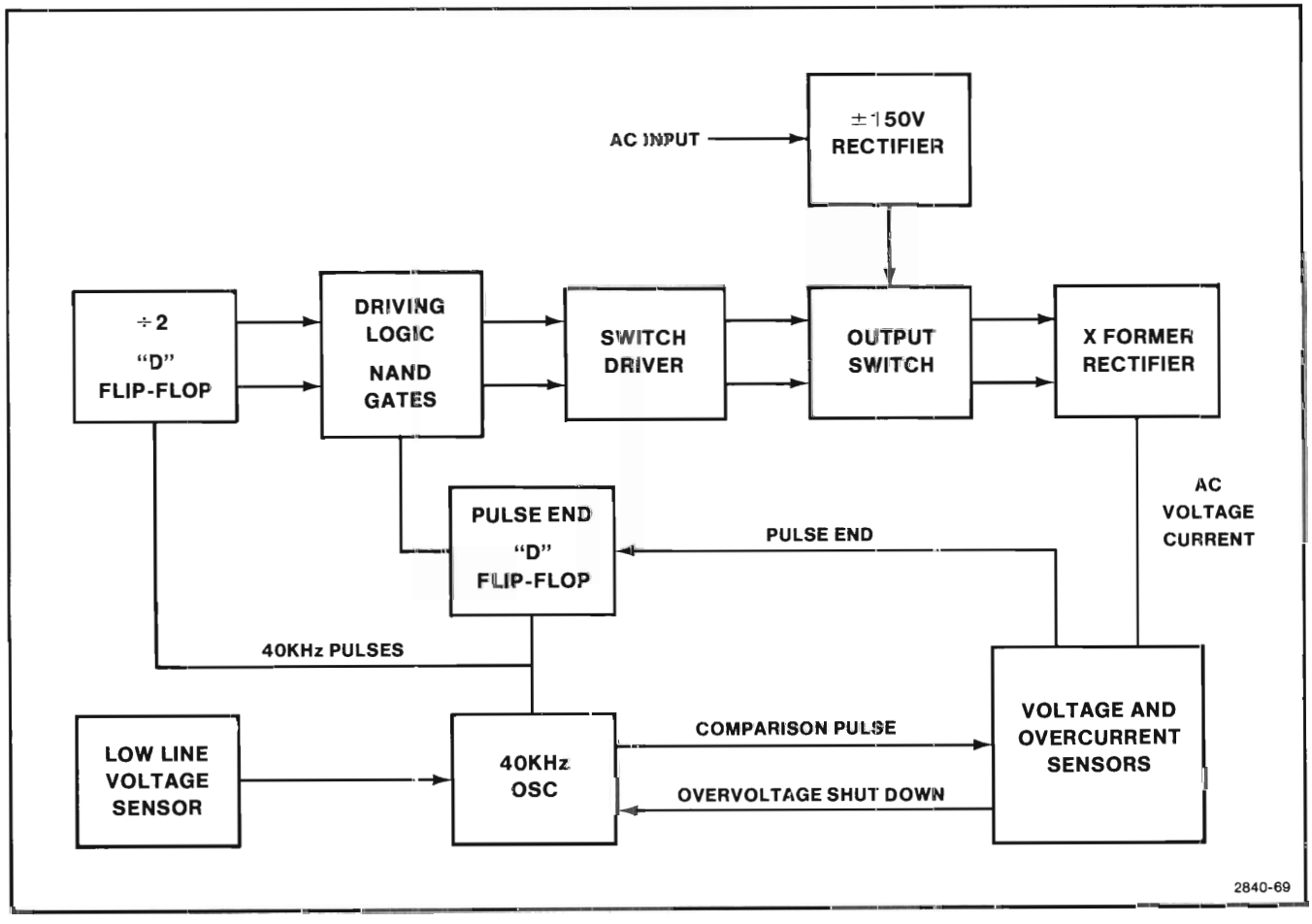


Figure 14-4. 5 V Switching Power Supply Block Diagram.

The signal that drives the output switching transistors comes from a 40 kHz oscillator. The output from the oscillator is a series of 5 microsecond pulses that are about 20

microseconds apart. This signal goes to the clock input of a D-type flip-flop (U2). The Q and not Q outputs from this flip-flop furnish a 20 kHz driving signal through nand gates to the drivers for the output stage. The output of the oscillator also goes to the reset input of another D-type flip-flop (U3) which enables the logic circuitry every time there is an output pulse from the oscillator.

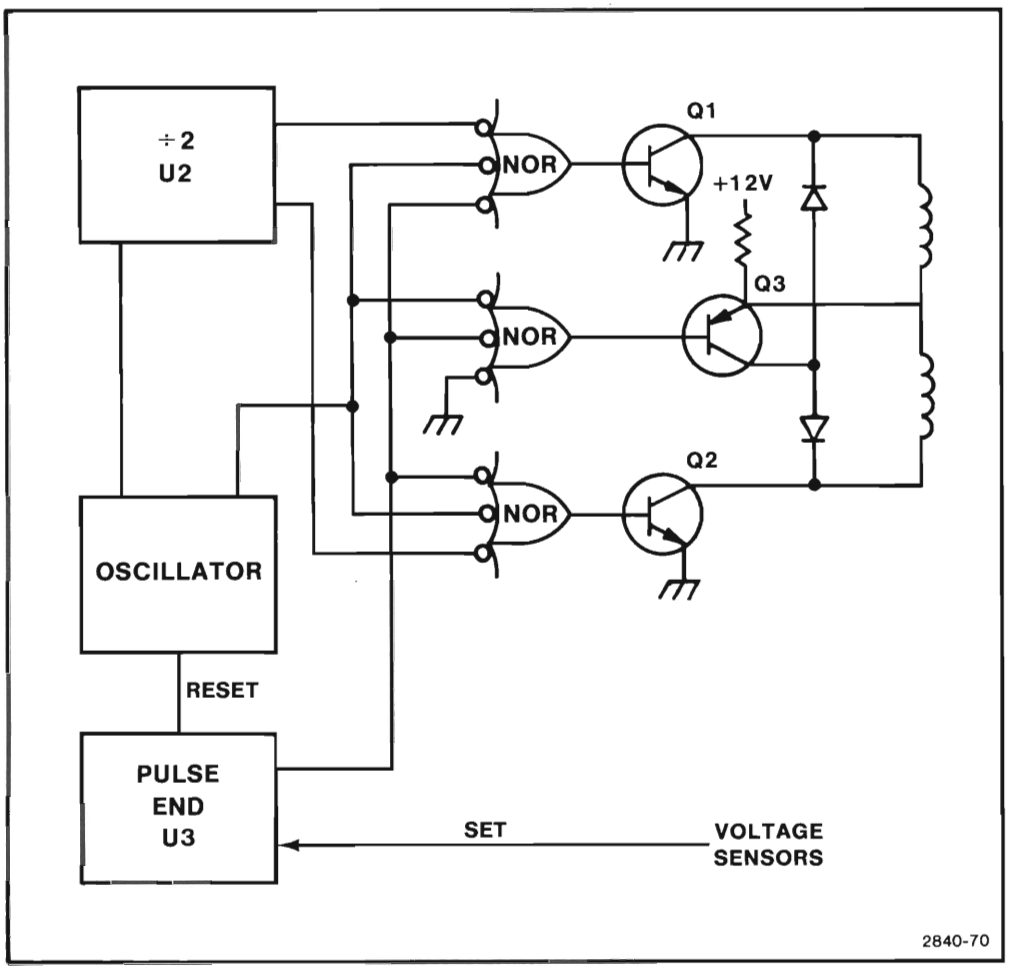


Figure 14-5. Switcher Driver Diagram.

The logic stage directs the signals to the three transistors connected to the driver transformer. The logic stage is three nor gates. The logic turns on either Q1 or Q2 for a short period of time. They are then turned off after a period of time that is determined by the load on the power supply. Whenever Q1 or Q2 is not turned on, Q3 is turned on, shorting the primary of the driving transformer, dissipating

any stored energy and eliminating undesired glitches or voltage spikes. The sequence of the "on" operation of the transistors is Q1, Q3, Q2, Q3, Q1, . . . (see Figure 14-6).

Low line voltage protection is provided by an operational amplifier, UB, that senses the voltage of the unregulated +20 V supply (see Figure 4-7). If the line voltage drops 25%, the operational amplifier shuts off the oscillator and eliminates the possibility of overheating the switching transistors.

Overvoltage protection is provided by another operational amplifier, UD (see Figure 14-8). It monitors the output voltage of the switching supply. If the output rises above 5.8 volts, this operational amplifier compares this voltage with the 5 V supply reference and through inverter, UC, shuts the oscillator off. This keeps excessive voltage from damaging circuitry.

Overcurrent protection is furnished by U1B, an operational amplifier that monitors the voltage across a .005 Ohm resistor in series with the negative side of the supply output. When the current becomes excessive, the operational amplifier senses the voltage across the resistor and narrows the driving pulses to the switching transistors to reduce the current to a safe value. (See Figure 14-7.)

Voltage regulation of the supply is provided by another part of the circuitry shown in Figure 14-8. Another output from the oscillator goes through an operational amplifier, UD, that is used as an inverter. The output from this inverter controls a two-transistor circuit. The top transistor, QA, is a switch that is turned on to charge capacitor CA to twelve volts quickly. It is then turned off and the capacitor discharges slowly at a rate determined primarily by QB and the resistor in its emitter. This voltage ramp goes to the positive input of an operational amplifier, U1C. This amplifier also has a sample of the 40 kHz ripple and the voltage from the output of the power supply applied to the negative input. When the negative going ramp crosses the power supply output voltage level, an output pulse is coupled through an inverter, U1D, to the "SET" input of the pulse-ending flip-flop U3. This terminates the pulse driving the switching transistors. If the power supply output voltage is low, crossover comes later and results in a wider pulse driving the switching transistors and an increased output voltage. If the power supply output voltage is high, the crossover comes sooner resulting in a narrower output pulse and a lower output voltage.

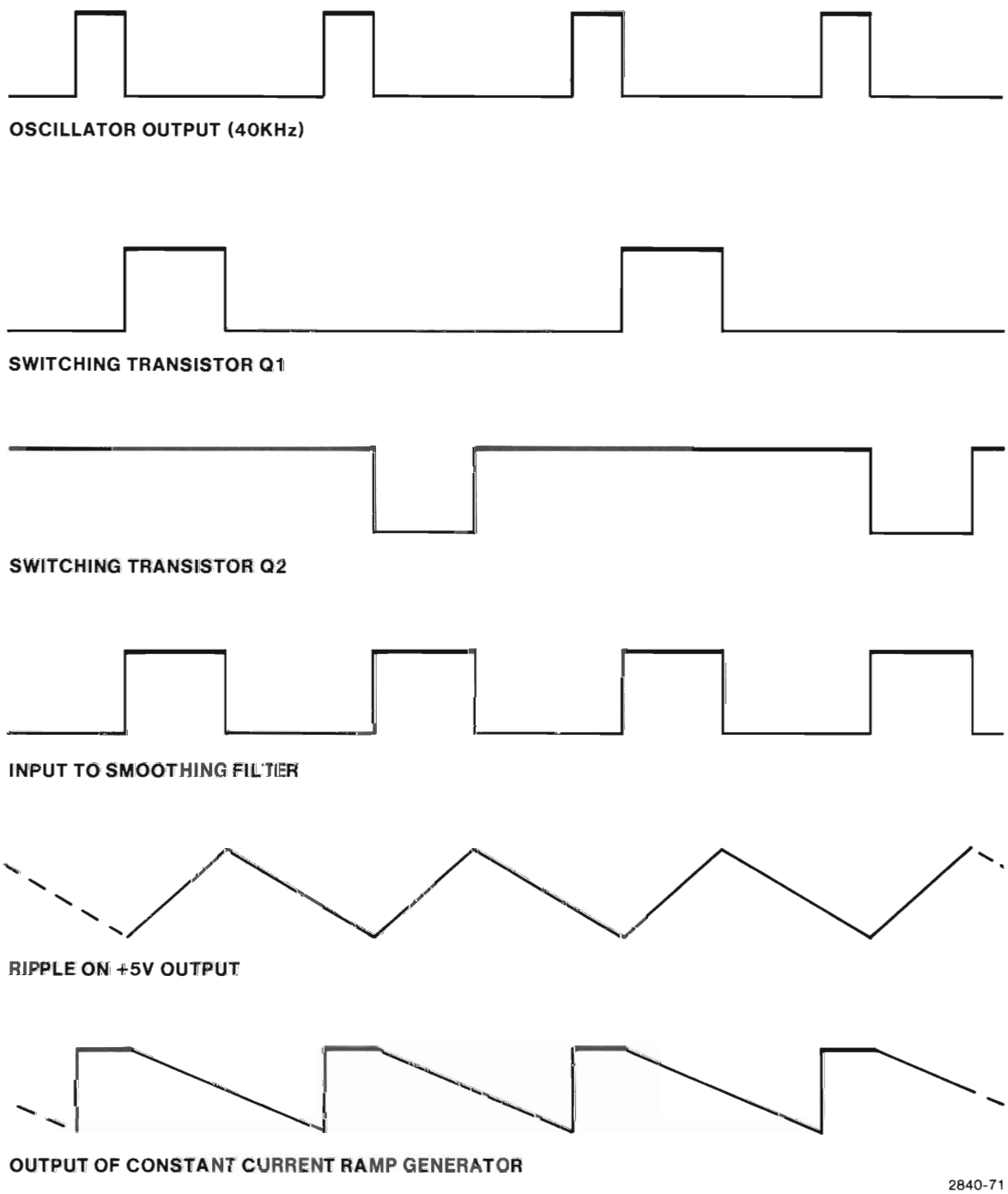


Figure 14-6. Switching Power Supply Waveforms.

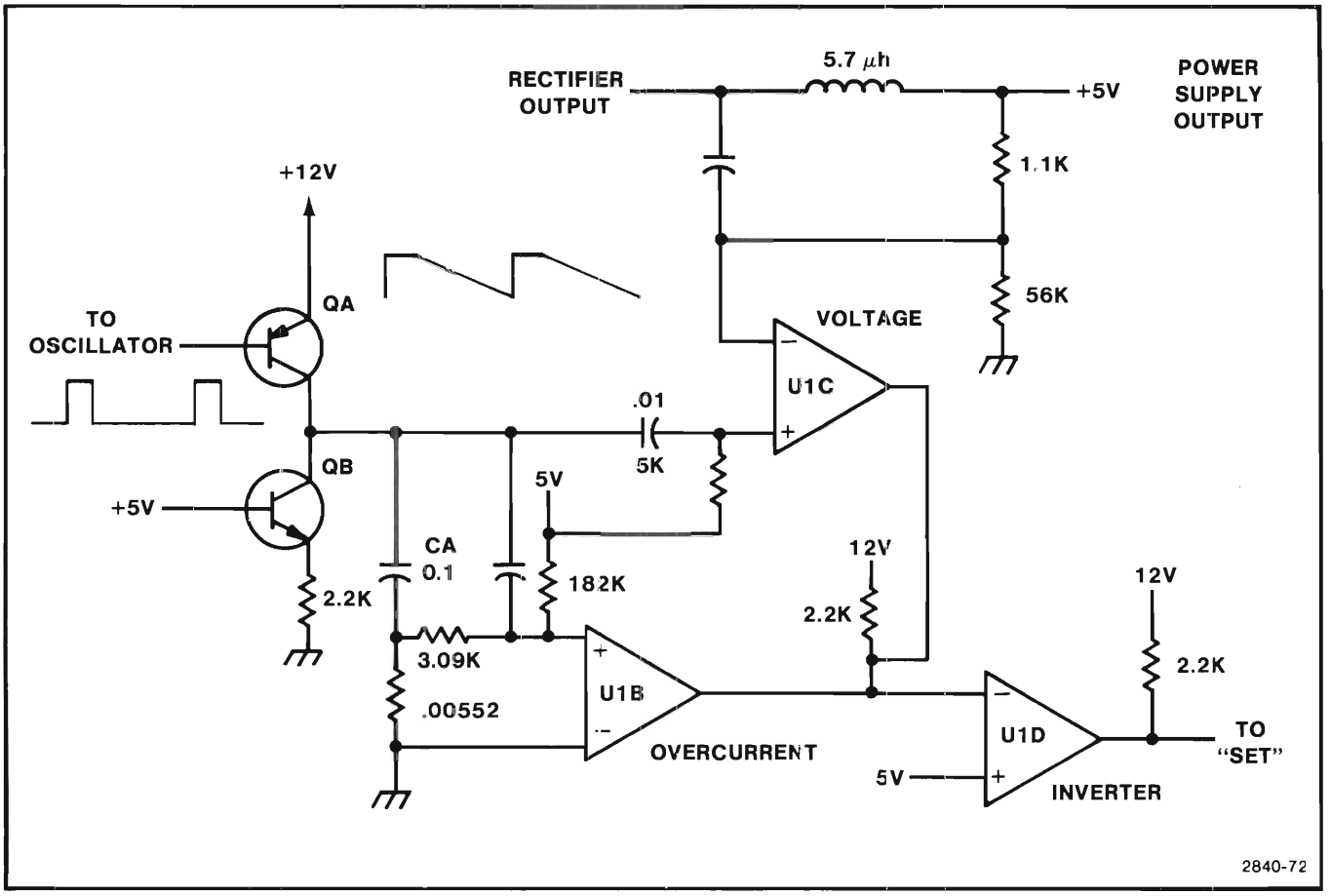


Figure 14-7. Switching Supply Voltage and Current Regulators.

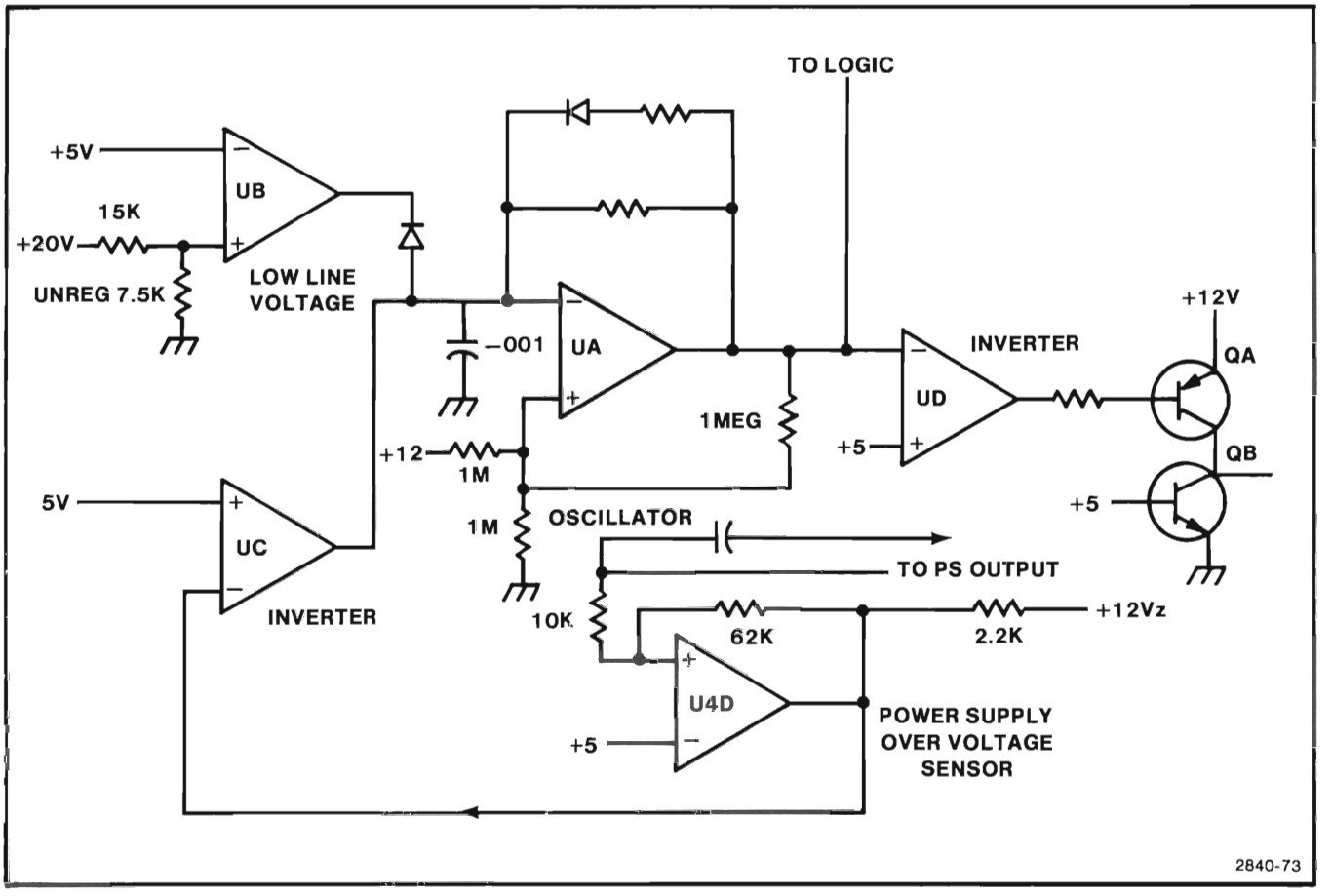


Figure 14-8. Switching Power Supply Oscillator.

+5 V REGULATOR

This +5 V regulator is a monolithic one chip regulator. It is not the same regulator as the 5 volt switching power supply. This regulator has all current limiting and voltage references as internal parts of the chip. It has a nominal current capacity of one ampere and gets its power from the +9 V unregulated supply.

+290 V REGULATOR

The basic circuit of the +290 V regulator is shown in Figure 14-9. It is composed of an operational amplifier and two transistors. The operational amplifier senses the divided down difference in voltage between the +290 V supply and the +15 V supply. Any difference is amplified and passed to Q3, inverted, and sent to the series pass transistor, Q3. The voltage drop across Q3 is controlled to maintain the +290 V supply at the proper voltage. The regulation of the +290 V supply also contributes some stabilization of output to the +175 V and +480 V supplies.

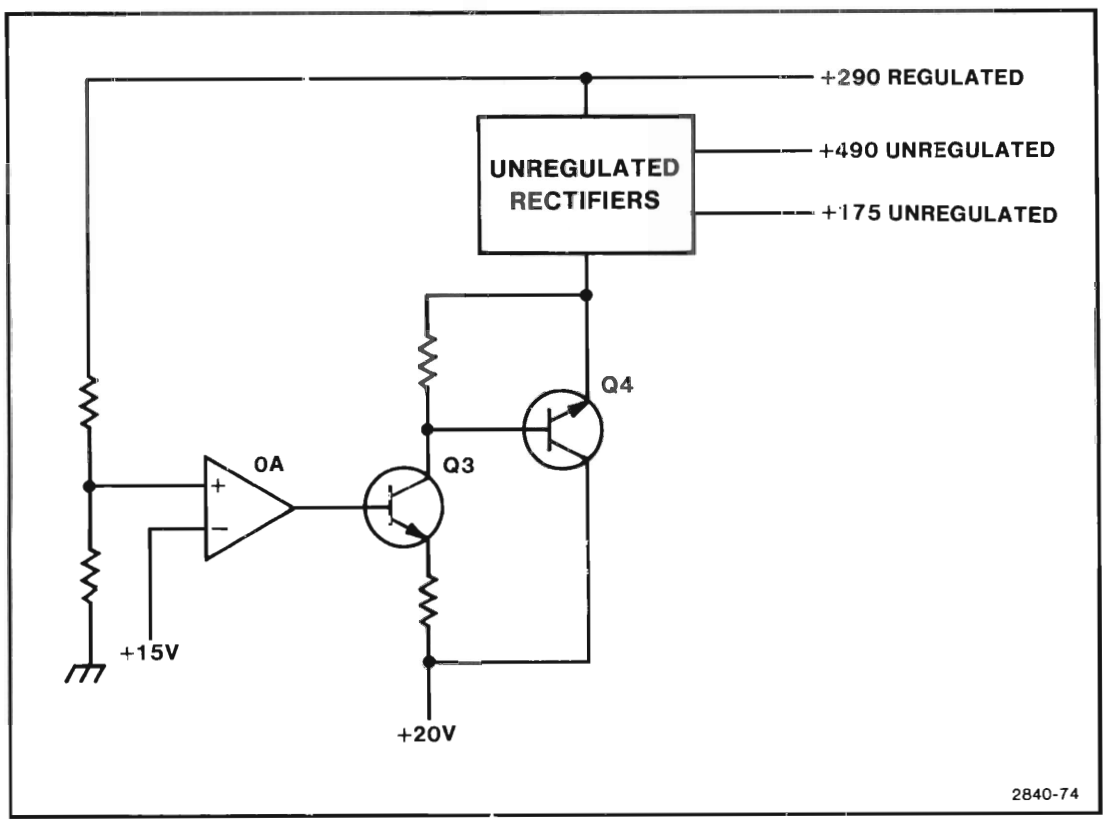


Figure 14-9. 290 V Regulator.

+12 V SUPPLY AND -12 V SUPPLY

There are two power supplies (Figure 14-10) on the I/O Board. These supply + and -12 V power for the system. Each supply has two zener referenced voltages. The regulation circuit is composed of one operational amplifier, A1, and two transistors, QA and QB. The operational amplifier A1, senses any change of output voltage through a divider R1 and R2, and compares this voltage to the reference voltage at the other input. It then sends the amplified and inverted change to the series regulator transistors, QA and QB, to cancel any change in voltage.

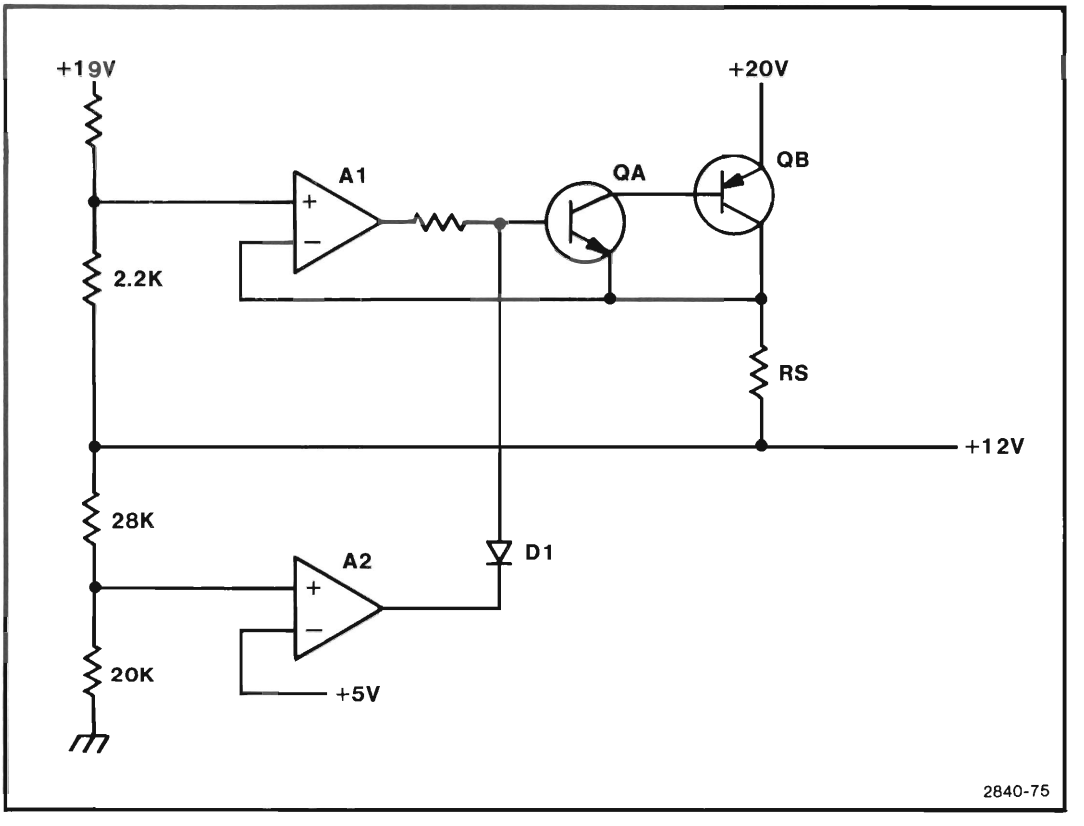


Figure 14-10. +12 V Power Supply.

If the current drawn by the supply exceeds its 1 ampere design limit, the second operational amplifier, A2, senses a reversed voltage at its input due to the increased drop across current-sensing resistor, RS, and its output voltage switches. When this output voltage changes, the voltage-regulating operational amplifier, A1, is disconnected by reversed polarity across D1. The series pass transistor, QB, is switched to a reduced output voltage, and the current is reduced to a safe value.

Both regulators have the same basic circuitry, although the polarities of the power supplies are different.

Restart Circuitry

The restart circuitry in the 4054 is the same as the 4052. The theory of operation is contained in the 4052 power supply section.

Section 15

4052 and 4054 BACKPACKS THEORY OF OPERATION

The backpacks on the Graphic Computing Systems are interfaces to other computer systems, printers, special backpack circuitry, and other peripheral equipment. There are two types of backpacks: a Firmware Backpack, and a Communications backpack. The Firmware Backpack provides interface to the backpack slots. The Communications Backpack also provides an additional RS232 interface port. Each of these backpacks comes in a two-slot or a four-slot version.

FIRMWARE BACKPACK

A block diagram of the Firmware Backpack circuitry is shown in Figure 15-1. The circuit diagram is in the Parts and Schematics manual. The Firmware Backpack circuitry extends the Graphic Computing System's data and address busses to external circuitry. It also provides a bank switch register to select specific hardware circuitry that is placed on the external lines. The external circuitry can be ROM packs or special interfaces.

Refer to the Firmware Block Diagram of Figure 15-1. Circuit operation is basically the connection of address and data lines from the Graphic Computing System to an external bus structure. There are also some control lines that are passed, such as CMCLK (Communications Clock), for timing, IRQ for interrupt requests, R-1/W-0 to initiate read and write output commands, EPIAS to strobe external PIAs, and PIAE to enable a PIA address. Several control lines are generated in the backpack to reduce the circuitry needed in external circuit modules. These lines are decoded external peripheral control lines, XPC2 and XPC3. BS(L) and BS(R) connect ROM devices in either of two backpack slots to the address and data busses.

4051 options cannot be used in these backpacks, and the 4052 options will not work in a 4051.

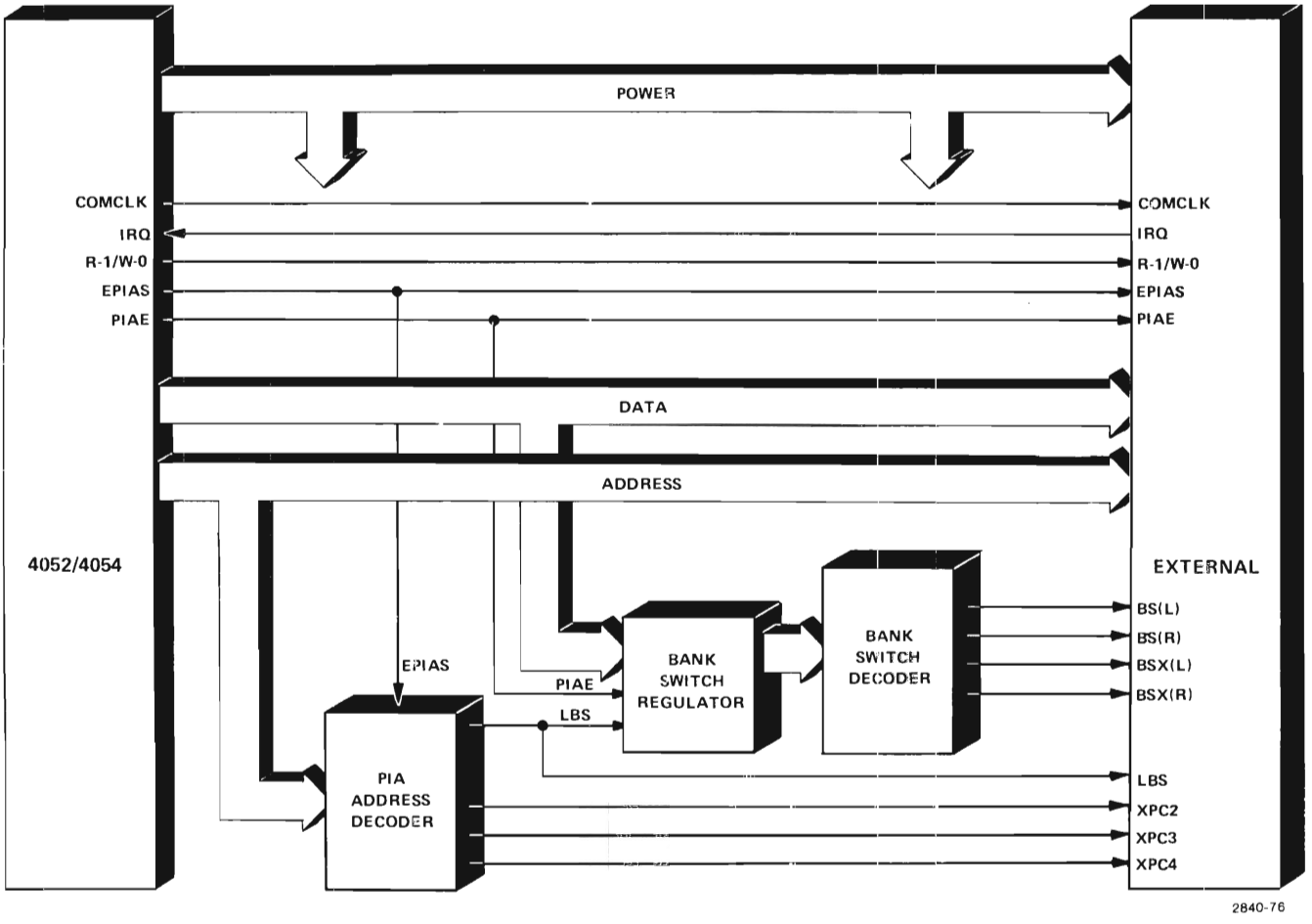


Figure 15-1. Firmware Interface Block Diagram.

BACKPACK ADDRESSING

Table 15-1

BANK SWITCH AND PERIPHERAL CONTROL ADDRESSES

Memory Address	Function
FF40	Load Bank Switch (LBS)
FF40 — FF43*	Communications PIA
FF44 — FF45*	Communications ACIA
FF48 — FF4B	External PIA 2 (XPC2)
FF4C — FF4F	External PIA 3 (XPC3)

* These addresses are used by the Communications Backpack.

Table 15-1 shows the memory addresses that activate the bank switch and peripheral control lines. Table 15-2 shows the interpetation of data loaded into a bank switch register. Some elements in these tables refer to circuitry available only in the optional Communications Backpack.

Bank switch operations simply write a data byte to the bank switch register(s) located at memory location FF40. Data in the bank switch register is decoded to enable external interfaces that occupy the specified backpack slot or location. The device remains enabled until the bank switch data is changed by another write operation to the bank switch register.

On power-up, the firmware in the Graphic Computing System sequentially loads all possible bank switch data locations to scan the available slots for ROM packs and optional interfaces. During a search for valid ROM packs, the microprocessor tries to read data from the ROM locations in the switch register and match the data to a standard data string. A data match means that a valid ROM pack is installed in that location. This ROM may also contain the firmware necessary to operate a special interface.

Table 15-2

BANK SWITCH SELECT DATA

Bank Switch Data								Address		(2 Slot) Function	(4 Slot) Function
7	6	5	4	3	2	1	0				
X	X	0	0	0	X	X	X	61	BS00	X	BS(RC)
X	X	0	0	1	X	X	X	71	BS08	X	BS(R)
X	X	0	1	0	D	D	D	61-68	BS10	X	BSX(RC)
X	X	0	1	1	D	D	D	71-78	BS18	X	BSX(R)
X	X	1	0	0	X	X	X	41	BS20	BS(L)	BS(L)
X	X	1	0	1	X	X	X	51	BS28	BS(R)	BS(LC)
X	X	1	1	0	D	D	D	41-48	BS30	BSX(L)	BSX(L)
X	X	1	1	1	D	D	D	51-58	BS38	BSX(R)	BSX(LC)

X = Don't Care Bit

DDD = Expansior Addresses

(L) = Left Backpack Slo:

(R) = Right Backpack Slot

(LC) = Left Center Backpack Slot (4 Slot Only)

(RC) = Right Center Backpack Slot (4 Slot Only)

COMMUNICATIONS BACKPACK

The Communications Backpack provides the same functions as the Firmware Backpack and includes an RS232 asynchronous communications interface. The RS232 interface allows the 4052 to emulate a TEKTRONIX 4012 Display Terminal. The 4054 emulates a TEKTRONIX 4014 Display Terminal. Both also provide formatted line communications with a host terminal like an intelligent computer terminal. Much of the Communications Backpack circuitry is the same as the Firmware Backpack. Primary circuit differences are an ACIA (asynchronous communications interface adapter) and a PIA (communications peripheral interface adapter). The bank switch register is the "A" data register of the output PIA, instead of a separate register like the one in the Firmware Backpack.

For detailed operation information of the RS232 interface in the Communications Backpack, refer to the 4050 Series Option 1 Data Communications Interface Instruction manual. The various modes of operation of the interface and the BASIC language statements that implement those modes are described in that manual. The following text describes the interface circuitry.

Communications Circuitry

Refer to the Communications Backpack schematic in the Parts and Schematics Manual and to the communication interface block diagram of Figure 15-2. RS-232 signal name definitions are given in Table 15-3. The operational status of each of the RS-232 communications lines is sensed by the PIA (peripheral interface adapter). This PIA also controls the data on the CTS and STX-A or STX-C lines to initiate transmission line turn-around operations, particularly in half duplex supervisor operation. The output connector looks like the lines from a data communications modem. The communications cable that is used transposes RDATA - TDATA, STX - SRX, RTS - CTS, DSR - DTR when the Graphics Computing System is connected to modem data communications equipment.

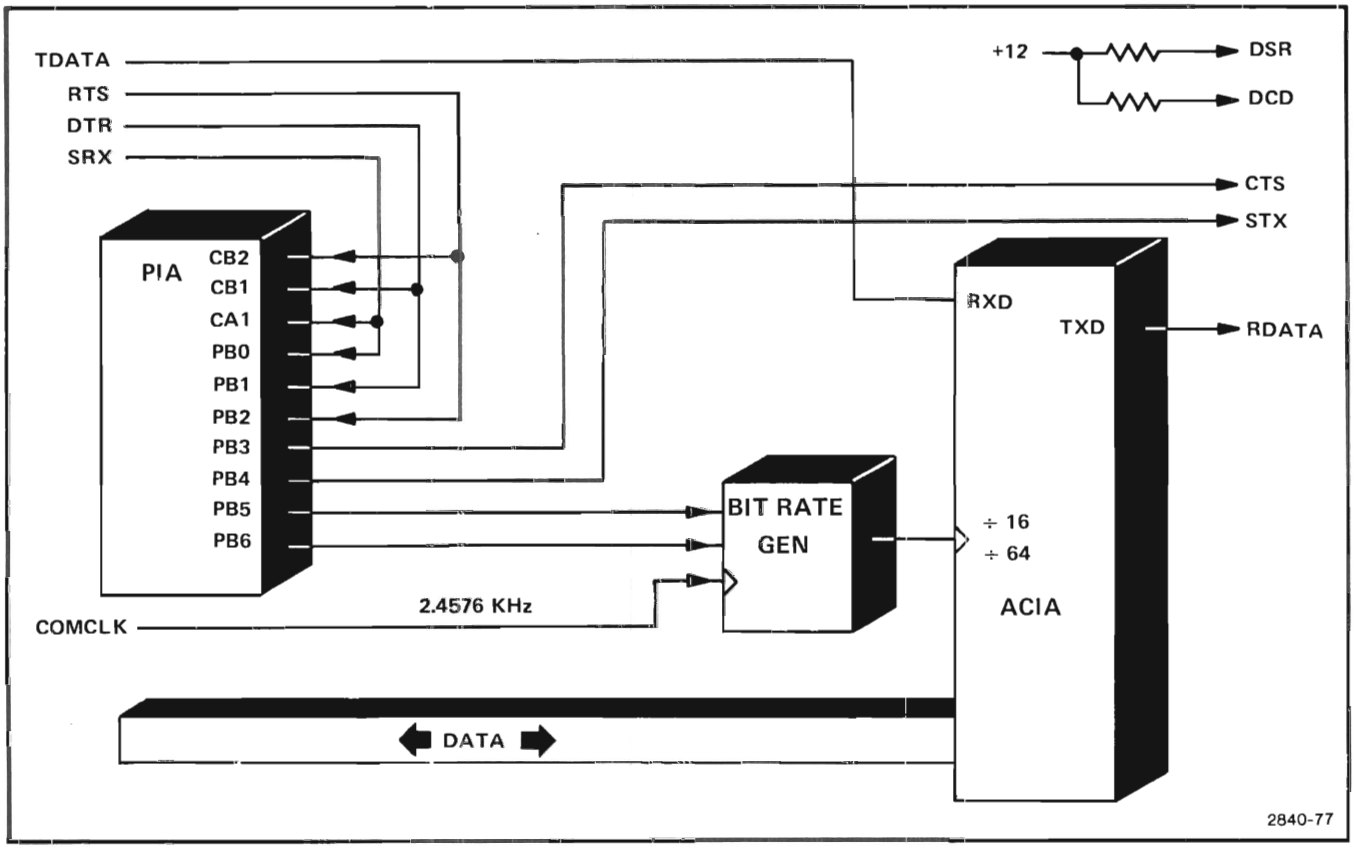


Figure 15-2. Communications Interface Block Diagram.

Table 15-3

RS-232 DEFINITIONS

TDATA	Transmitted Data
RDATA	Receive Data
STX	Secondary Transmit Data
SRX	Secondary Receive Data
DCD	Data Carrier Detect
DSR	Data Set Ready
RTS	Request To Send
CTS	Clear To Send

The Baud rate selection is determined by the data bytes sent from the I/O Board to both the ACIA and the PIA. Data sent to the ACIA determines whether the clock signals are divided by 16 or by 64. The COMCLK signal comes into the backpack at 2.4576 MHz and is divided by a programmable rate generator before it is sent to the ACIA to be divided again. Table 15-4 lists the division rates and logic input for the rate generator. Provisions are also included for using external transmit and receive clocks.

Table 15-4

BIT RATE GENERATOR DATA

Baud Rate	68B21			68B50	Error
	PB7	PB6	PB5	÷	
9600	0	0	0	16	0%
4800	0	0	1	16	0%
2400	1	0	0	16	0%
1200	0	1	1	16	0%
600	1	0	0	64	0%
300	1	0	1	16	0%
150	1	1	0	16	0%
110	1	1	1	16	−0.83%

Data addressed to the ACIA control register has the format as specified in Table 15-5:

Table 15-5

DATA BIT FUNCTIONS

BIT 7 CONTROLS THE READ BUFFER FULL INTERRUPT

Bit 7	
0	Receive Interrupt Disabled
1	Receive Interrupt Enabled

BITS 1-0 SPECIFY BAUD RATE CLOCK DIVISION

Bit 1	Bit 0	
0	0	÷1 (not used)
0	1	÷16
1	0	÷64
1	1	Master Reset

BITS 4-2 SPECIFY PARITY ENCODING/DECODING

Bit 4	Bit 3	Bit 2	
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bits
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

BITS 6-5 ENABLE OR DISABLE TRANSMIT BUFFER EMPTY INTERRUPT AND BREAK — SPACING OF DATA TRANSMISSION.

Bit 6	Bit 5	
0	0	Transmit Interrupt Disabled
0	1	Transmit Interrupt Enabled
1	0	Transmit Interrupt Disabled
1	1	Transmit Interrupt Disabled — Send BREAK

PIA data register addressing relies upon setting a specific bit (bit 2) in the associated PIA control register. To address a peripheral register or peripheral data bus, the control register bit 2 must be set to a one. A zero in bit 2 causes the data direction register to be addressed by the same memory address.

Communication Cable

The backpack output has a female connector that corresponds to EIA RS-232 standards for data communication equipment modems. To use the Graphic Computing System as a data terminal, a special cable is provided that interchanges the line pairs 2-3, 4-5, and 8-20. All other control lines go directly through the cable. See Figure 15-3.

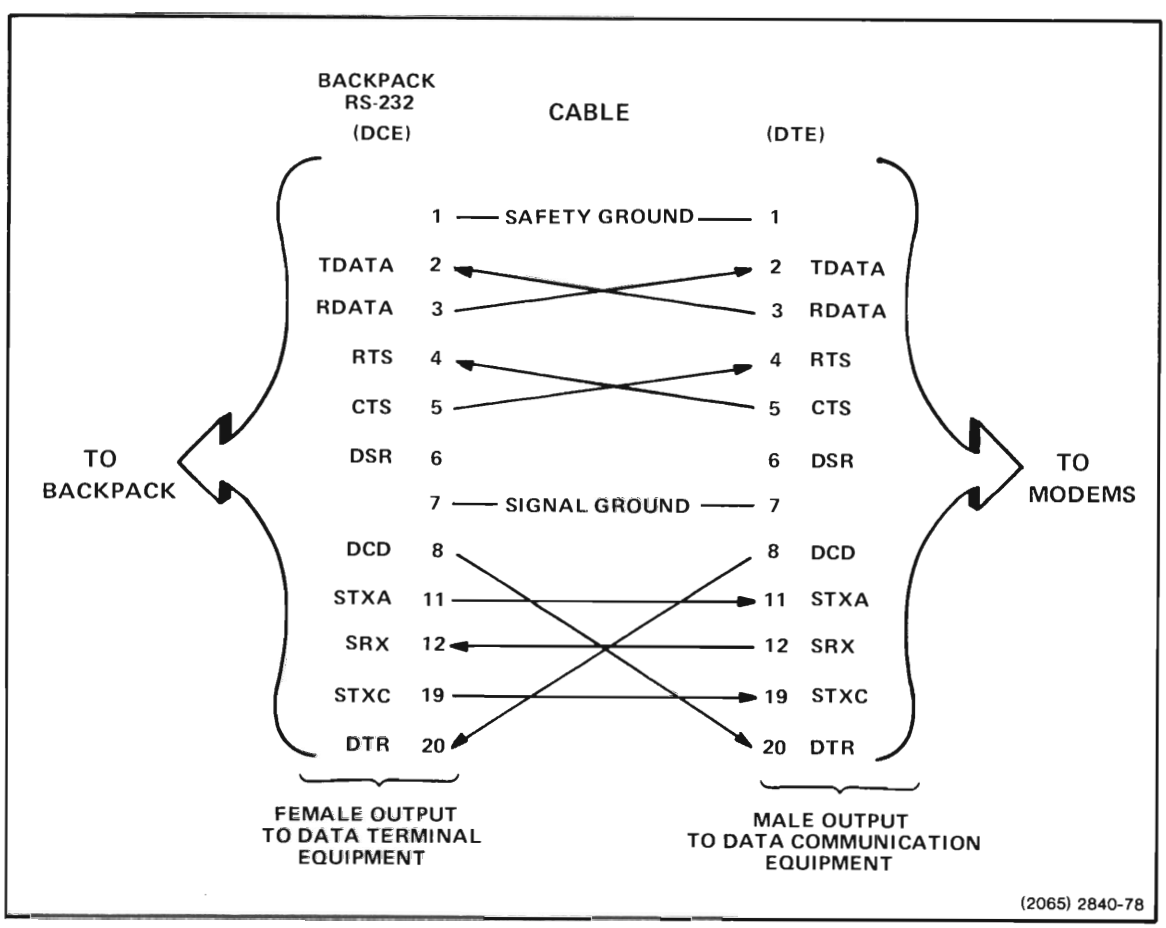


Figure 15-3. Communication Backpack Cable.

COMMUNICATION INTERFACE TEST PROGRAM

The communication interface test is initiated by typing the CALL "CMTEST" command on the keyboard. The test is performed in the following two parts.

If the self-test adapter is not installed, the display will appear as shown in Figure 15-4.

```
Control Line
1  000111
2  000001
3  010111
4  000110
5  110111
7  100111
8  000111  ERROR --
        Type RETURN to continue
```

2840-91

Figure 15-4. "CMTEST" Screen Display Without Self-Test Adapter.

If the system is operating properly with the self-test adapter connected to the end of the communications cable, the message displayed will be the same as that displayed in Figure 15-5. The "type RETURN to continue" message has no function in this test.

If the Communication Interface is not operating properly, an ERROR message will be displayed.

```
Control Line
Data Line
@ABCDEFGHIJKL
NOPQRSTUVWXYZ[\]↑_ !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTU
VWXYZ[\]↑_`abcdefghijklmnopqrstuvwxyz{|}~↓
pin#3 for  (BAUD RATE)/2
        Type RETURN to continue
```

2840-80

Figure 15-5. "CMTEST" Screen Display With Self-Test Adapter Installed.

Appendix A

4052/4054 FIRMWARE INSTRUCTIONS

The following table gives the hex code, opcode abbrevation, and address mode for the 4052/4054 system firmware instructions.

Hex Code	Opcode	Address Mode
00	TRAP	NONE
01	NOP	INHERENT
02	NOP2	INHERENT
03	SFA	INHERENT
04	TRAP	NONE
05	TAP	INHERENT
06	TAP	INHERENT
07	TPA	INHERENT
08	INX	INHERENT
09	DEX	INHERENT
0A	CLV	INHERENT
0B	SEV	INHERENT
0C	CLC	INHERENT
0D	SEC	INHERENT
0E	CLI	INHERENT
0F	SEI	INHERENT
10	SAB	INHERENT
11	CBA	INHERENT
12	TAPX	INHERENT
13	TPAX	INHERENT
14	ADXI	IMMEDIATE
15	ASPI	IMMEDIATE
16	TAB	INHERENT
17	TBA	INHERENT
18	SDA	INHERENT
19	TRAP	NONE
1A	NLDXX	INHERENT
1B	ABA	INHERENT
1C	NLDAX	INHERENT
1D	NLDBX	INHERENT
1E	NSTAX	INHERENT
1F	JMPAX	INHERENT
20	BRA	RELATIVE
21	SDB	INHERENT
22	BHI	RELATIVE

Hex Code	Opcode	Address Mode
23	BLS	RELATIVE
24	BCC	RELATIVE
25	BCS	RELATIVE
26	BNE	RELATIVE
27	BEQ	RELATIVE
28	BVC	RELATIVE
29	BVS	RELATIVE
2A	BPL	RELATIVE
2B	BMI	RELATIVE
2C	BGE	RELATIVE
2D	BLT	RELATIVE
2E	BGT	RELATIVE
2F	BLE	RELATIVE
30	TSX	INHERENT
31	INS	INHERENT
32	PULA	INHERENT
33	PULB	INHERENT
34	DES	INHERENT
35	TXS	INHERENT
36	PSHA	INHERENT
37	PSHB	INHERENT
38	JMPIN	EXTENDED
39	RTS	INHERENT
3A	FPSHD	DIRECT
3B	RTI	INHERENT
3C	FPSHX	INDEXED
3D	FPSH	EXTENDED
3E	WAI	INHERENT
3F	SWI	INHERENT
40	NEGA	INHERENT
41	FPSHI	IMMEDIATE
42	FPULD	DIRECT
43	COMA	INHERENT
44	LSRA	INHERENT
45	FPULX	INDEXED
46	RORA	INHERENT
47	ASRA	INHERENT
48	ASLA	INHERENT
49	ROLA	INHERENT
4A	DECA	INHERENT
4B	FPUL	EXTENDED
4C	INCA	INHERENT
4D	TSTA	INHERENT
4E	FDUP	INHERENT
4F	CLRA	INHERENT

Hex Code	Opcode	Address Mode
50	NEGB	INHERENT
51	FSWP	INHERENT
52	FADD	INHERENT
53	COMB	INHERENT
54	LSRB	INHERENT
55	FSUB	INHERENT
56	RORB	INHERENT
57	ASRB	INHERENT
58	ASLB	INHERENT
59	ROLB	INHERENT
5A	DECB	INHERENT
5B	FMUL	INHERENT
5C	INCB	INHERENT
5D	TSTB	INHERENT
5E	FDIV	INHERENT
5F	CLRB	INHERENT
60	NEGX	INDEXED
61	FNORM	INHERENT
62	PSHRET	DIRECT
63	COMX	INDEXED
64	LSRX	INDEXED
65	RTRN	DIRECT
66	RORX	INDEXED
67	ASRX	INDEXED
68	ASLX	INDEXED
69	ROLX	INDEXED
6A	DECX	INDEXED
6B	PSHX	INHERENT
6C	INCX	INDEXED
6D	TSTX	INDEXED
6E	JMPX	INDEXED
6F	CLRX	INDEXED
70	NEG	EXTENDED
71	STROKE	INHERENT
72	EC	INHERENT
73	COM	EXTENDED
74	LSR	EXTENDED
75	PULX	INHERENT
76	ROR	EXTENDED
77	ASR	EXTENDED
78	ASL	EXTENDED
79	ROL	EXTENDED
7A	DEC	EXTENDED
7B	TRAP	NONE

Hex Code	Opcode	Address Mode
7C	INC	EXTENDED
7D	TST	EXTENDED
7E	JMP	EXTENDED
7F	CLR	EXTENDED
80	SUBAI	IMMEDIATE
81	CMPAI	IMMEDIATE
82	SBCAI	IMMEDIATE
83	TRAP	NONE
84	ANDAI	IMMEDIATE
85	BITAI	IMMEDIATE
86	LDAAI	IMMEDIATE
87	TRAP	NONE
88	EORAI	IMMEDIATE
89	ADCAI	IMMEDIATE
8A	ORAAI	IMMEDIATE
8B	ADDAI	IMMEDIATE
8C	CPXI	IMMEDIATE
8D	BSR	RELATIVE
8E	LDSI	IMMEDIATE
8F	TRAP	NONE
90	SUBAD	DIRECT
91	CMPAD	DIRECT
92	SBCAD	DIRECT
93	TRAP	NONE
94	ANDAD	DIRECT
95	BITAD	DIRECT
96	LDAAD	DIRECT
97	STAAD	DIRECT
98	EORAD	DIRECT
99	ADCAD	DIRECT
9A	ORAAD	DIRECT
9B	ADDAD	DIRECT
9C	CPXD	DIRECT
9D	TRAP	NONE
9E	LDSD	DIRECT
9F	STSD	DIRECT
A0	SUBAX	INDEXED
A1	CMPAX	INDEXED
A2	SBCAX	INDEXED
A3	TRAP	NONE
A4	ANDAX	INDEXED
A5	BITAX	INDEXED
A6	LDAAX	INDEXED
A7	STAAX	INDEXED

Hex Code	Opcode	Address Mode
A8	EORAX	INDEXED
A9	ADCAX	INDEXED
AA	ORAAX	INDEXED
AB	ADDAX	INDEXED
AC	CPXX	INDEXED
AD	JSRX	INDEXED
AE	LDSX	INDEXED
AF	STSX	INDEXED
B0	SUBA	EXTENDED
B1	CMPA	EXTENDED
B2	SBCA	EXTENDED
B3	TRAP	NONE
B4	ANDA	EXTENDED
B5	BITA	EXTENDED
B6	LDAA	EXTENDED
B7	STAA	EXTENDED
B8	EORA	EXTENDED
B9	ADCA	EXTENDED
BA	ORAA	EXTENDED
BB	ADDA	EXTENDED
BC	CPX	EXTENDED
BD	JSR	EXTENDED
BE	LDS	EXTENDED
BF	STS	EXTENDED
C0	SUBBI	IMMDIATE
C1	CMPBI	IMMEDIATE
C2	SBCBI	IMMEDIATE
C3	TRAP	NONE
C4	ANDBI	IMMEDIATE
C5	BITBI	IMMEDIATE
C6	LDABI	IMMEDIATE
C7	TRAP	NONE
C8	EORBI	IMMEDIATE
C9	ADCBI	IMMEDIATE
CA	ORABI	IMMEDIATE
CB	ADDBI	IMMEDIATE
CC	ADAX	INHERENT
CD	WADAX	INHERENT
CE	LDXI	IMMEDIATE
CF	TRAP	NONE
D0	SUBBD	DIRECT
D1	CMPBD	DIRECT
D2	SBCBD	DIRECT
D3	TRAP	NONE

Hex Code	Opcode	Address Mode
D4	ANDBD	DIRECT
D5	BITBD	DIRECT
D6	LDABD	DIRECT
D7	STABD	DIRECT
D8	EORBD	DIRECT
D9	ADCBD	DIRECT
DA	ORABD	DIRECT
DB	ADDBD	DIRECT
DC	SBUG	INHERENT
DD	CBUG	INHERENT
DE	LDXD	DIRECT
DF	STXD	DIRECT
E0	SUBBX	INDEXED
E1	CMPBX	INDEXED
E2	SBCBX	INDEXED
E3	MVLR	INHERENT
E4	ANDBX	INDEXED
E5	BITBX	INDEXED
E6	LDABX	INDEXED
E7	STABX	INDEXED
E8	EORBX	INDEXED
E9	ADCBX	INDEXED
EA	ORABX	INDEXED
EB	ADDBX	INDEXED
EC	MVRL	INHERENT
ED	WADX	EXTENDED
EE	LDXX	INDEXED
EF	STXX	INDEXED
F0	SUBB	EXTENDE
F1	CMPB	EXTENDED
F2	SBCB	EXTENDED
F3	CPCH	IMMEDIATE
F4	ANDB	EXTENDED
F5	BITB	EXTENDED
F6	LDAB	EXTENDED
F7	STAB	EXTENDED
F8	EORB	EXTENDED
F9	ADCB	EXTENDED
FA	ORAB	EXTENDED
FB	ADDB	EXTENDED
FC	TRAP	NONE
FD	PCH	IMMEDIATE
FE	LDX	EXTENDED
FF	STX	EXTENDED

Table B-1

ASCII CODE CHART

BITS B4 B3 B2 B1	B7 B6 B5 Ø Ø Ø	Ø Ø 1	Ø 1 Ø	Ø 1 1	1 Ø Ø	1 Ø 1	1 1 Ø	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y	
Ø Ø Ø Ø	NUL 0	DLE 16	SP 32	0 48	@ 64	P 80	\ 96	p 112
Ø Ø Ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
Ø Ø 1 Ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
Ø Ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
Ø 1 Ø Ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
Ø 1 Ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
Ø 1 1 Ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
Ø 1 1 1	BEL BELL 7	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 Ø Ø Ø	BS BACK-SPACE 8	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 Ø Ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 Ø 1 Ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 Ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 Ø Ø	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	| 124
1 1 Ø 1	CR RETURN 13	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 Ø	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

Appendix B

ASCII CODE CHART

When the 4054 stores text in its memory, or sends and receives text from a computer, it represents that text as a collection of telegraph characters, using the ASCII telegraph code. ("ASCII" stands for "American Standard Code for Information Interchange". This code is known internationally as the ISO-7 code.)

Bits. Each character of the ASCII code is a collection of seven "bits" ("binary digits"). (Often an eighth bit, the "parity bit" is added for error-detection purposes.) Each bit is either "1" or "0". With 7 bits, there are 128 possible combinations; these are the 128 ASCII characters.

ASCII Decimal Equivalents. Each character may be regarded as a binary numeral, representing a number in the range from 0 to 127. For instance, the ASCII character for "Z" is "1011010", which is the binary numeral for the number 90. We say that 90 is the "ASCII decimal equivalent" for the letter Z.

Printing and Non-Printing Characters. The 128 characters in the ASCII alphabet include many characters which can be printed on paper; upper and lower case letters of the alphabet, numerals, the "space" character, punctuation marks and special symbols. In addition, there are some "non-printing" characters, or "control characters". These have special meanings such as "carriage return" or "device control #1", and are used to control machines.

Using the ASCII Code Chart. Table B-1 is an "ASCII Code Chart"; it lists the 128 ASCII characters, and shows the binary bits and ASCII decimal equivalent for each character. The chart is a rectangular array of 8 columns, each containing 16 characters; this makes it more compact than a table with a single column of 128 characters.

The "high order bits" (B7,B6,B5) for the characters in each column are the same; they appear at the top of the column. Similarly, the "low order bits" (B4,B3,B2,B1) for the characters in each row are the same, and are shown at the left of the row.

For instance, the letter "Z" is in the sixth column and twelfth row. At the top of the column, we see its high order bits: "1C1"; its low order bits, "1010", appear at the left of the row. Hence, its seven binary bits are:

B7	B6	B5	B4	B3	B2	B1
1	0	1	1	0	1	0

The binary numeral "1011010" represents the number "90". This is the ASCII decimal equivalent for "Z", and appears next to it in the chart.

The "control characters" occupy the first two columns in table B-1. There are keys on the keyboard for only a few of these characters: "escape" ("ESC"), "tab" ("HT"), "back-space" ("BS"), "carriage return" ("CR"), and "line feed" ("LF"). However, you can send any control character to the computer by using the CTRL key.

To send one of the control characters, you hold down the CTRL key and type one of the other ASCII characters. For instance, to type an "ENQ" character, you press CTRL-E; to type a "DC3", you press CTRL-S. Table B-2 lists the control characters and the keys you press to type these characters.

Table B-2

CONTROL CHARACTERS

Mnemonic	Usual ASCII Abbrev.	Name of Character	Keys to Press
NU	NUL	Null	CRTL- @
SH	SOH	Start of Heading	CTRL-A
SX	STX	Start of Text	CTRL-B
EX	ETX	End of Text	CRTL-C
ET	EOT	End of Transmission	CTRL-D
EQ	ENQ	Enquiry	CTRL-E
AK	ACK	Acknowledgement	CTRL-F
BL	BEL	Bell	CTRL-G
BS	BS	Backspace	CTRL-H
HT	HT	Horizontal Tab	CTRL-I
LF	LF	Line Feed	CTRL-J
VT	VT	Vertical Tab	CTRL-K
FF	FF	Form Feed	CTRL-L
CR	CR	Carriage Return	CTRL-M
SO	SO	Shift Out	CTRL-N
SI	SI	Shift In	CTRL-O
DL	DLE	Data Link Escape	CTRL-P
D1	DC1	Device Control 1	CTRL-Q
D2	DC2	Device Control 2	CTRL-R
D3	DC3	Device Control 3	CTRL-S
D4	DC4	Device Control 4	CTRL-T
NK	NAK	Negative Acknowledgement	CTRL-U
SY	SYN	Synchronization Character	CTRL-V
EB	ETB	End of Transmission Block	CTRL-W
CN	CAN	Cancel	CTRL-X
EM	EM	End of Medium	CTRL-Y
SB	SUB	Substitute	CTRL-Z
EC	ESC	Escape	CTRL-[
FS	FS	Field Separator	CTRL-\
GS	GS	Group Separator	CTRL-]
RS	RS	Record Separator	CTRL-↑
			CTRL- ∧ -(circumflex accent)
US	US	Unit Separator	CTRL-_ (underscore)