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4663

INTERACTIVE DIGITAL PLOTTER

(VOLUME 1)

SERVICE MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

MANUAL PART NO. 070-2669-00
PRODUCT GROUP 12

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

MANUAL REVISION STATUS

PRODUCT: 4663 and 4663S Interactive Digital Plotters

This manual supports the following versions of this product: Serial Numbers B010100 and up.

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MAR 1981	Revised: page 2-1.
JUL 1981	Revised: pages ii, iii, vi, vii, 3-27 and 3-35.
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JUN 1983	Deleted: pages 3-64 through 3-67, 4-6, and 4-7.

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Figure 1-1. 4663 Interactive Digital Plotter.

Section 1

SPECIFICATIONS

INTRODUCTION

The TEKTRONIX 4663 (and 4663S—see 4663 Operator's Manual) Interactive Digital Plotter, (Figure 1-1) is capable of dual-pen graphic recording from digital source devices. The standard 4663 Plotter is equipped with a RS-232-C Communications Interface, enabling it to be used with Tektronix terminal-based systems. In addition, an optional interface is available to connect the Plotter to devices having a GPIB (IEC)[1] interface (such as the TEKTRONIX 4050 Series Graphic System).

The X- and Y-axes of the Plotter are controlled by split-phase synchronous ac motors (two motors in the X-axis and one motor in the Y-axis). These motors control the movement of a pen carriage containing two pens through a system of cables and pulleys. The internal circuitry converts external commands into appropriate vector movements. The two-pen carriage permits multi-color graphics or graphics with multiple pen types. (Note that only one pen can draw at any instant.) The pen carriage also contains a crosshair cursor, which can be used to optically check or align plotted points and for digitizing.

The 4663 will draw on a variety of media in sheets up to 17 x 22 in (431.8 x 558.8 mm). In addition, a media advance option is available (Option 36) to automatically advance a roll of paper. This option uses a 200 ft roll of paper up to 18 in wide with 1/2 in tear-off strips (containing sprocket holes) on each side. Sheet paper is held in position by electrostatic attraction generated by the platen and roll paper is held in position mechanically by the paper advance mechanism.

The 4663 offers high quality resolution and plotting capabilities using a variety of pen types, media, and page/viewport sizes. The most basic Plotter operation is graphics — the moving of the pen carriage across the plotting surface, the lifting and lowering of either pen to produce written vectors. The Plotter can also print alphanumeric characters in any resident fonts. In addition, the Plotter can act as a digitizer, transmitting the coordinate position of the active pen along with pen status (up or down). Several user-definable variations of each recording operation can be used to increase the versatility of the Plotter. The variations include the following:

- modification of the size of the plotting area,
- scaling the plots,
- manual pen positioning using the joystick,
- rotation of the plot,
- alteration of the axes and character dimensions,
- point digitizing,
- choice of plotting speeds and pen pressures,
- use of programmable macros and,
- the initiation of a self-test.

Actual implementation of these variations differs according to the interface being used. Several user-defined variations can be conveniently introduced via a front panel Parameter Entry card. Parameters selected in this manner remain stored in the Plotter for up to 90 days, even when the Plotter is turned off.

[1] The GPIB Interface is defined in IEEE Standard 488-1975: IEEE Standard Digital Interface for Programmable Instrumentation.

ABOUT THIS MANUAL

The service documentation for the 4663 Interactive Digital Plotter consists of two volumes. Volume 1 (this volume) contains the Plotter's specifications, preventive maintenance procedures (including detailed calibration instructions), circuit descriptions, signal descriptions, error codes, and a Plotter interface command summary. Volume 2 contains a short form calibration procedure, assembly/dissembly procedures for replacing parts, interconnecting cable diagrams, electrical and mechanical parts lists, schematics, strapping tables, instrument and option installation procedures, and diagrams of circuit board component locations.

For detailed troubleshooting procedures, consult the 4663 Diagnostic Test Fixture Instruction Manual (see Section 8 of Volume 2).

GENERAL DESCRIPTION

The 4663's internal circuitry includes a 6800 and an 8X300 microprocessor. The 6800 microprocessor oversees all general aspects of the Plotter's operation. These include storing commands, communicating with the host computer, accepting front panel commands (including Parameter Entry), etc. The 8X300 microprocessor, on the other hand, controls the generation of motor pen drive signals (including the pen lifters) using information supplied by the 6800 microprocessor.

SPECIFICATIONS

The remainder of this section contains a series of tables summarizing the physical properties, the electronic specifications, and the performance characteristics of the 4663 Interactive Digital Plotter. The following tables are included:

Table 1-1	4663 Option Summary
Table 1-2	Accessories
Table 1-3	Physical Characteristics
Table 1-4	Power Requirements
Table 1-5	Environmental Specifications
Table 1-6	Performance Specifications
Table 1-7	Page Sizes (Full Page Aspect Ratio)

Option Summary

The standard instrument contains an RS-232-C interface with Full Duplex capability. Table 1-1 lists the options which can be added to the instrument. Notice that the Plotter can be equipped with only one serial interface at a time.

Table 1-1

4663 OPTION SUMMARY

Option	Name	Description
1	GPIB Interface	Provides communications with GPIB instruments, such as the TEKTRONIX 4050 Series Controller.
4	GPIB Interface Only	Same as Option 1, except that the standard RS-232 interface is removed.
30	RS-232 Interface to Tektronix 4081	Permits the Plotter to be connected to the TEKTRONIX 4081 Graphic System.
31	Circular Interpolation and Programmable Macros	Permits the Plotter to draw arcs and circles and to use programmed moves and draws (macros).
32	Downloadable Characters and Math Character Set	Permits the host computer to program the Plotter to draw user-defined, math, and Greek characters.
36	Media Advance	Permits the Plotter to be equipped with roll paper (instead of sheets), which can be advanced under host computer control.
37	Additional Parameter Entry Setup Memory	Allows more than one operating configuration to be stored in the Plotter.
48	220 V, 50 Hz	Permits the Plotter to be operated with a 220 V line source.

Table 1-2

ACCESSORIES

Standard Accessories

Power Cord
Pens, Fiber Tip (for paper)
- Red (3 each)
- Black (3 each)
- Blue (3 each)
- Green (3 each)

RS-232-C Interface Cable
Sheet Paper (17 x 22 in, 100 sheets/box)
4663 Interactive Digital Plotter Operator's Manual
4663 Interactive Digital Plotter Reference Guide

Optional Accessories

Wet Ink Pen Assembly
- With PL3 point (dia= .01 in, 0.3 mm)
- PL5 point (dia= .02 in, 0.5 mm)
- PL8 point (dia= .03 in, 0.8 mm)

Pen Replacement Parts Kit
- 1 cap
- 1 body section
- 1 barrel
- 1 locking nut
- 6 ink reservoirs

Ink Reservoir (6 per pkg)
- Ink
  - For Film (3/4 oz Squeeze bottle)
    - Black (each)
    - Red (each)
    - Green (each)
    - Blue (each)
    - Brown (each)
  - For Paper (3/4 oz Squeeze bottle)
    - Black (each)

Ball Point Pens
- Black (3 each)
- Red (3 each)
- Green (3 each)
- Blue (3 each)

Fiber Tip Pens (water soluble for acetate)
- Black (3 each)
- Brown (3 each)
- Red (3 each)
- Orange (3 each)
- Yellow (3 each)
- Green (3 each)
- Blue (3 each)
- Magneta (3 each)
- Purple (3 each)

Dust Cover (soft vinyl)
GPIB Cable
Roll Paper (18 in x 200 ft for Option 36)
Sheet Paper (17 in x 22 in 100 sheets per box)
Mylar (17 in x 22 in 100 sheets per box)
4663 Service Manual (two volumes)
4663 Diagnostic Test Fixture Manual

Table 1-3

PHYSICAL CHARACTERISTICS

Weight	Outside Dimensions		
	Length	Width	Height
80 lbs (36.4 kg)	38.0 in (965 mm)	30.1 in (765 mm)	6.8 in (173 mm)

Table 1-4

POWER REQUIREMENTS

Line Voltage, Switch Selection	Voltage Range	Line Fuse Size
110 V	90 — 130 V	5 A Fast-Blo
220 V	180 — 250 V	2.5 A Fast-Blo
Line Frequency.....	48 — 440 Hz	
Input Power 115 Vac.	3.5 A maximum; 2.4 A typical	

Table 1-5

ENVIRONMENTAL SPECIFICATIONS

Characteristic	Non-operating	Operating
Temperature	−67 to 167° F (−55 to + 75° C)	32 to 104° F (0 to 40° C)
Altitude	To 50,000 ft (15240 m)	To 15,000 ft (4572 m)
Vibration	Up to 40 Hz @.01 in (.03 cm) total displacement	— — — —
Shock	To 30 Gs, ½ sine, 11 ms duration	— — — —
Transportation	Meets National Safe Transit Committee type of test when packaged as shipped by factory. Test procedure 1A, Category II with a 12 in drop.	
Humidity	Mil-T-28800B per test conditions 810B at 50.71 procedure IV (5 day operating and non-operating, 90 to 95% Relative Humidity).	

Table 1-6

PERFORMANCE SPECIFICATIONS

Characteristic	Specifications
Default Paper Size	A Size — 8 ½ x 11 in (216 x 279 mm)
	B Size — 11 x 17 in (279 x 432 mm)
	C Size — 17 x 22 in (432 x 559 mm)
	A4 Size — 8.3 x 11.7 in (210 x 297 mm)
	A3 Size — 11.7 x 16.5 in (297 x 420 mm)
	A2 Size — 16.5 x 23.4 in (420 x 594 mm)
Paper Control (Sheets)	Electrostatic Hold-Down
(Roll)	Mechanical Hold-Down with Option 36
Paper Drive Speed (Option 36)	≥4.5 in/s (114 mm/s)
Paper Drive Resolution (Option 36)	0.016 in (0.4 mm)
Plotting Area	Y-Axis≤17.25 in (438 mm) X-Axis≤23.5 in (597 mm)
Plotting Speed	16.47 in/s along either axis, 23.3 in/s at a 45° angle
Acceleration	600 in/s^2 (15240 mm/s^2) in PREVIEW
	400 in/s^2 (10160 mm/s^2) in NORMAL
	300 in/s^2 (7620 mm/s^2) in ENHANCED 1
	240 in/s^2 (6096 mm/s^2) in ENHANCED 2

Characteristic	Specifications
Point Plotting Rate	30 Points/s (max)
Plotting Accuracy	0.15% of Vector Length ± 0.0025 in (0.0635 mm)
Repeatability	Returns any previously plotted point to within ± 0.0025 in (0.0635 mm)
	Resolution (Addressable) 0.001 in (0.0254 mm)
	Pen Pressure Coarse Pressure, ± 25%
	Pen Height (Up) 0.058 in ± 0.013 (1.47 ± 0.33 mm)
Linearity Geometry	Mean vector shall not deviate more than ± 0.015 in from a straight line between two points.
Line Aberrations	Short term non-linearity shall not deviate more than ± 0.003 in from mean vector.
Orthogonality	± 0.015 in (0.38 mm) across the plotting surface.

Table 1-7

PAGE SIZES (FULL PAGE ASPECT RATIO)

Page Format	Orientation	Page Size & Media Dimensions	Measurements (width x height)		Figure [b] No.
			English-inch	Metric-mm	
Drafting	Horizontal	C 22 x 17 in	21.00 x 15.5	533.4 x 393.7	1-2
Drafting	Horizontal	B 17 x 11 in	15.76 x 10.24	400.3 x 260.1	1-2
Drafting	Horizontal	A 11 x 8.5 in	10.50 x 7.74	266.7 x 196.6	1-2
Drafting	Horizontal	A2 594 x 420 mm	22.72 x 15.75	574.0 x 400.0	1-3
Drafting	Horizontal	A3 420 x 297 mm	15.75 x 10.91	400.0 x 277.0	1-3
Drafting	Horizontal	A4 297 x 210 mm	10.91 x 7.48	277.0 x 190.0	1-3
Drafting	Vertical	C 17 x 22 in	15.50 x [a]	393.7 x [a]	1-2
Drafting	Vertical	B 11 x 17 in	10.24 x 15.76	260.1 x 400.3	1-2
Drafting	Vertical	A 8.5 x 11 in	7.74 x 10.50	196.6 x 266.7	1-2
Drafting	Vertical	A2 420 x 594 mm	15.75 x [a]	400.0 x [a]	1-3
Drafting	Vertical	A3 297 x 420 mm	10.91 x 15.75	277.0 x 400.0	1-3
Drafting	Vertical	A4 210 x 297 mm	7.48 x 10.91	190.0 x 277.0	1-3
Graphing	Horizontal	C 22 x 17 in	20.50 x 16.00	520.7 x 406.4	1-4
Graphing	Horizontal	B 16.5 x 11 in	15.00 x 10.00	381.0 x 254.0	1-4
Graphing	Horizontal	A 11 x 8.5 in	10.00 x 7.00	254.0 x 177.8	1-4
Graphing	Horizontal	A2 594 x 420 mm	22.20 x 15.75	564.0 x 400.0	1-5
Graphing	Horizontal	A3 420 x 297 mm	15.35 x 10.91	390.0 x 277.0	1-5
Graphing	Horizontal	A4 297 x 210 mm	10.91 x 7.28	277.0 x 185.0	1-5
Graphing	Vertical	C 17 x 22 in	16.00 x [a]	406.4 x [a]	1-4
Graphing	Vertical	B 11 x 16.5 in	10.00 x 15.00	254.0 x 381.0	1-4
Graphing	Vertical	A 8.5 x 11 in	7.00 x 10.00	177.8 x 254.0	1-4
Graphing	Vertical	A2 420 x 594 mm	15.75 x [a]	400.0 x [a]	1-5
Graphing	Vertical	A3 297 x 420 mm	10.91 x 15.35	277.0 x 390.0	1-5
Graphing	Vertical	A4 210 x 297 mm	7.28 x 10.91	185.0 x 277.0	1-5

[a] The page dimension is clipped since it would extend beyond the platen boundary.

[b] All figures are shown with FULL PAGE initial aspect ratio.

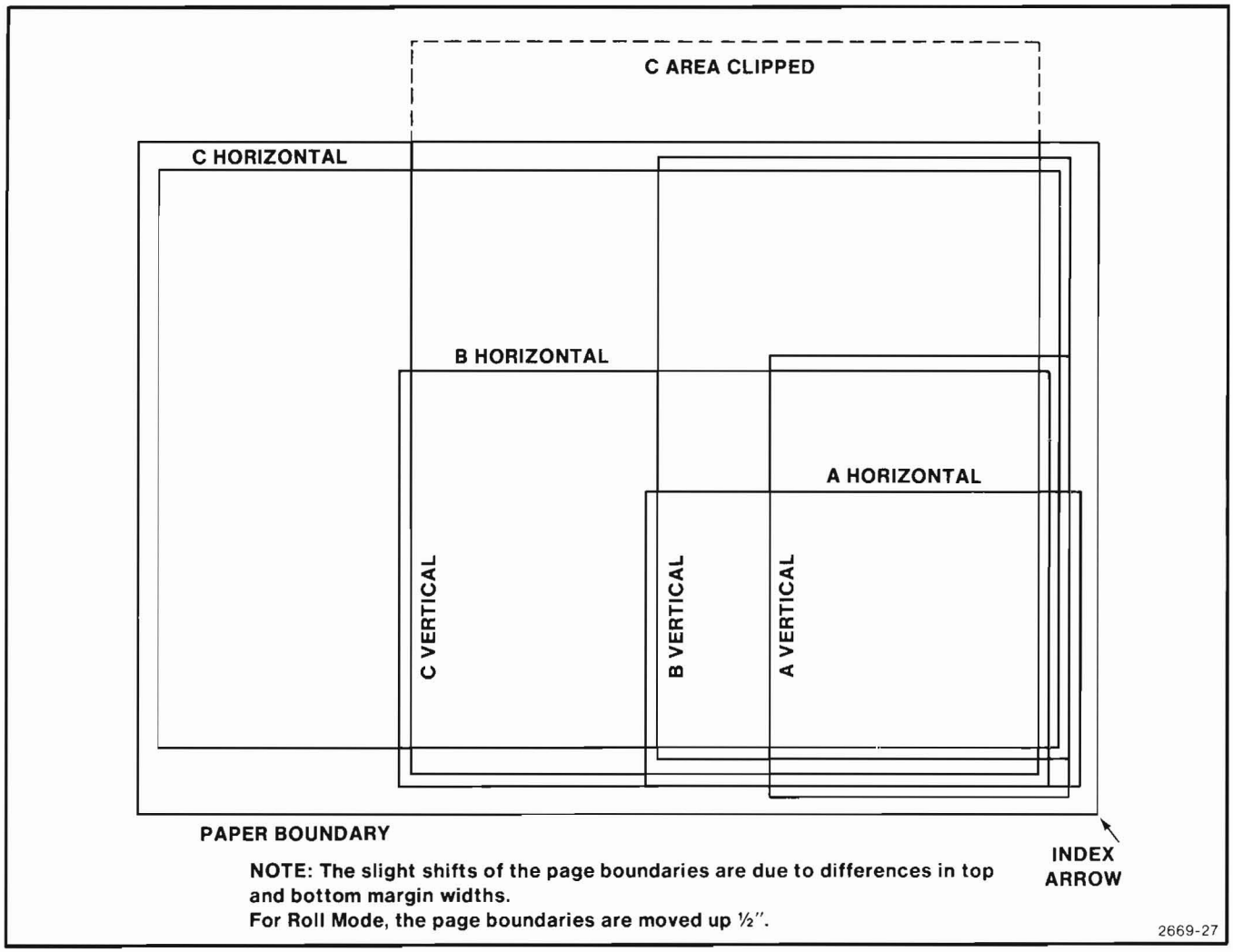

Figure 1-2. Horizontal and Vertical Page Orientations for English Page Sizes (Drafting).

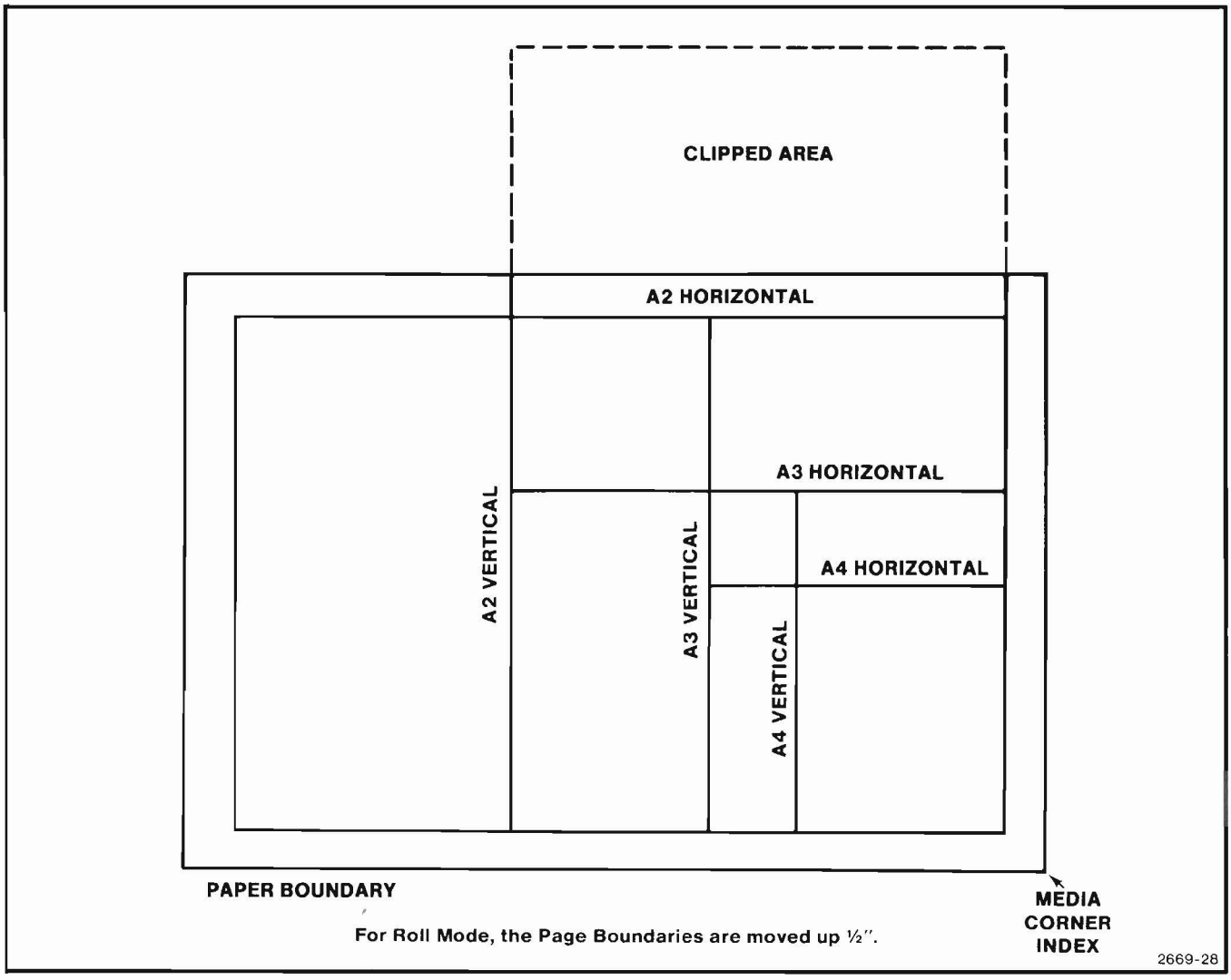

Figure 1-3. Horizontal and Vertical Page Orientations for Metric Page Sizes (Drafting).

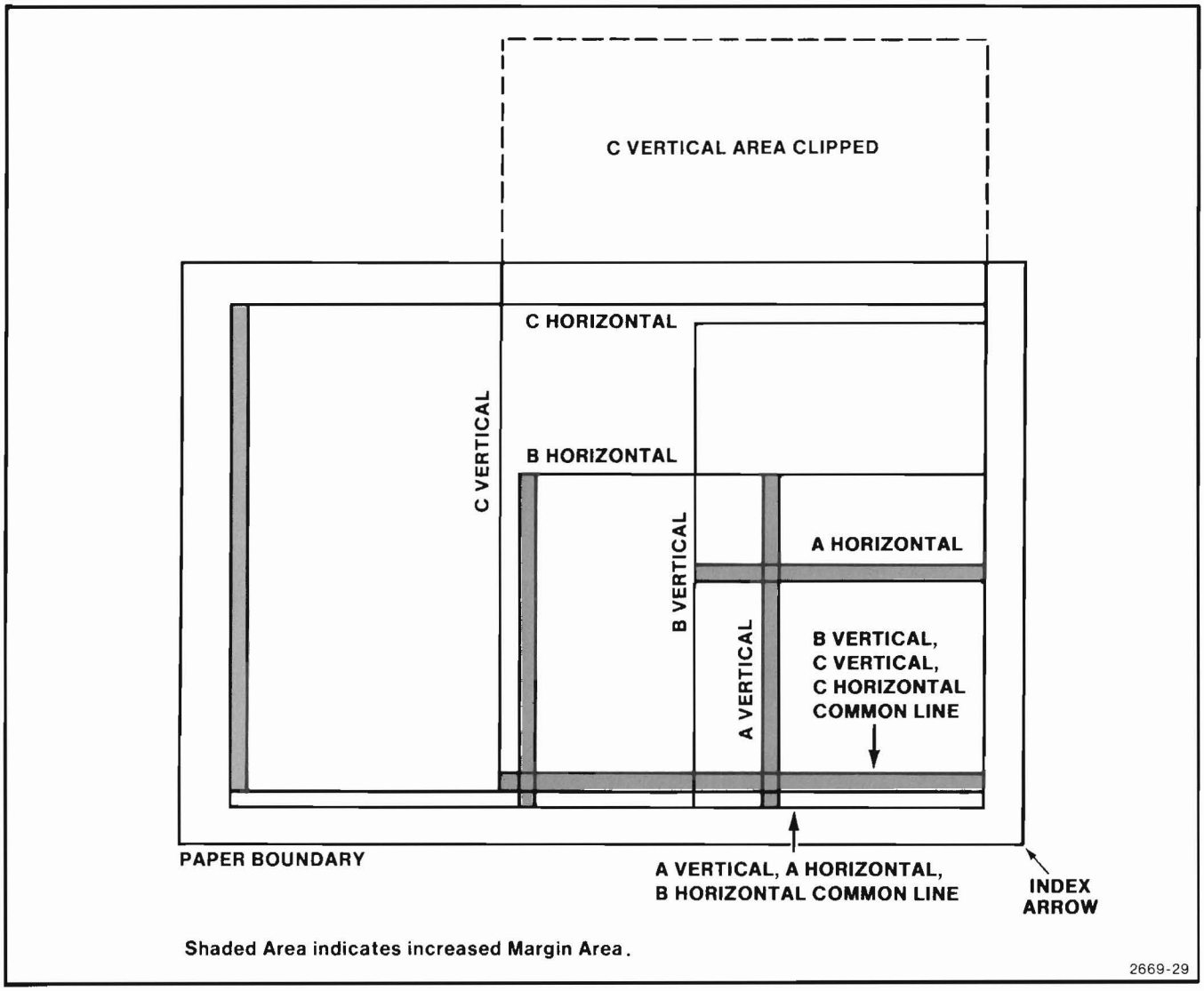

Figure 1-4. Horizontal and Vertical Page Orientations for English Page Sizes (Graphing).

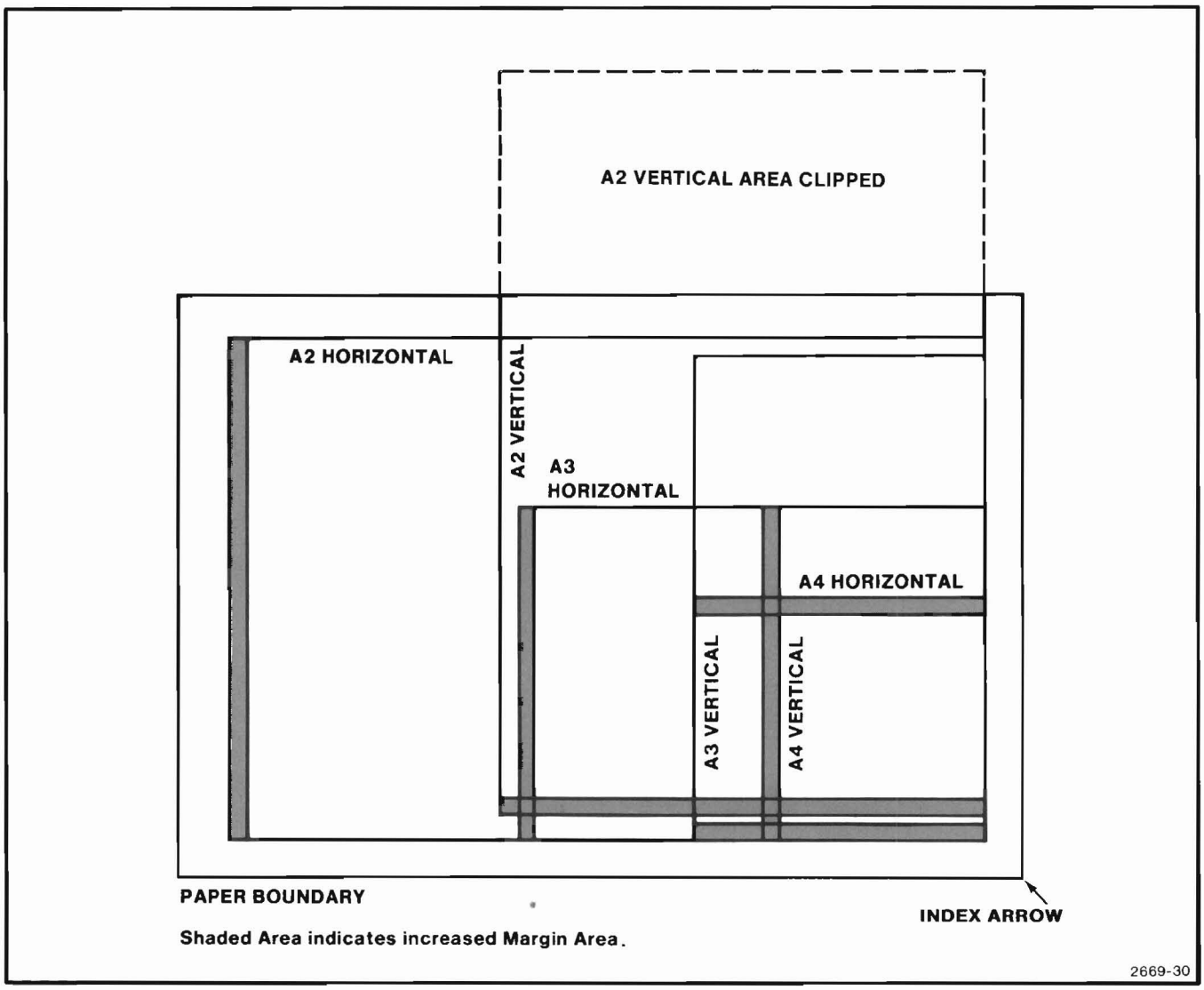

Figure 1-5. Horizontal and Vertical Page Orientations for Metric Page Sizes (Graphing).

Section 2

PREVENTIVE MAINTENANCE AND CALIBRATION

PREVENTIVE MAINTENANCE

General

Preventive maintenance consists of cleaning, visual inspection, adjustment, etc. Performed on a regular basis, preventive maintenance may improve the reliability of this instrument. The frequency and severity of the instrument's use will determine the required maintenance interval. It is, however, recommended that the Plotter's three pen drive cables be checked and adjusted at least every 500 hours of Plotter operation. Perhaps this might become the basis for performing preventive maintenance checks and calibration on the instrument. A convenient time to perform preventive maintenance is preceding calibration.

Cleaning the Platen and the Case

Occasional cleaning helps retain the electrostatic paper hold-down ability of the platen and preserves the appearance of the 4663. The frequency of cleaning varies with the instrument's environment. use the following procedure to clean the plotter:

1. Pull the Parameter Entry card out to the Media Form line and press the switch over SHEET.
2. Press the front panel MEDIA CHANGE switch. (If the Plotter was not in SHEET mode previously, it will be necessary to press MEDIA CHANGE twice more to move the pen carriage to the upper right corner.) Then, turn the POWER switch off and disconnect the power cord. Remove any paper present on the platen.

CAUTION

Do not use abrasive and strong chemical cleaners on the platen, as these can scratch or remove layers of the thin insulating film on the platen's electrostatic surface. Conductive cleaners must also be avoided. These include products containing ammonia, oils, liniments, or scents which leave an electrically conductive film if not entirely removed. This film causes the electrostatic paper hold-down to fail due to the conductivity of the film residue.

3. The most acceptable way to clean a platen is to use water, because it will not leave a residue on the platen's surface.
4. If more extensive cleaning is necessary, use a plain detergent or alcohol pad (Tektronix P/N 006-2398-00). A plain detergent is one that contains no bleach, scents, fabric softeners, or colored crystals. Either detergent or alcohol pad method will leave a residue which must be removed.

NOTE

Part number 006-2398-000 is for one pad only. A box of 50 can be ordered by using a quantity of 50.

5. If alcohol was used, remove the thin alcohol residue on the platen surface by wiping the platen with a soft, moist (with water) cloth. Turn the cloth frequently to avoid smearing the residue.
6. To remove any detergent residue, use step five, and repeat at least three times to remove all the residue.
7. Dry the platen with a clean, dry cloth.
8. Clean the Plotter case with a cloth lightly dampened with a mild detergent solution.
9. Connect the power cord to the power source, and if necessary, change the Parameter Entry card's Media Form line back to ROLL mode. The Plotter may again be operated.

Viscous Oil Dampers

On the end of each pen drive motor capstan, there is a viscous oil damper. It is normal for this damper to contain an air bubble in the oil resevoir and to have a thin residue of oil on its outer surface. The damper is not defective when these items appear. The air bubble helps compensate for tolerances and heat expansion. The thin oil residue is inherently present on the surfaces of the damper, though it serves no purpose.

Isopropyl alcohol is a partial solvent for silicone oil such as that used in these dampers. It is the only cleaning agent used to clean up oil residues. Most other solvents effective for removing silicone oil will also attack the polycarbonates used in 4663 parts such as the damper covers.

CAUTION

Silicone oils have insulating properties. Do not touch circuit boards or plug connectors without first washing your hands if the dampers have been handled. Oil may prevent electrical contact or result in excess capacitance on circuit boards and plugs.

Lubrication Information

The Plotter requires no periodic lubrication since all cable pulley bearings, motor bearings, fan bearings, and the bearings for the Y-axis arm rollers are all permanently lubricated. In addition, the rubber treads for all Y-axis arm rollers have lubrication impregnated in them.

Pen Drive Cable Checks

The Plotter uses a system of three cables, each driven by a separate motor, to move the pen carriage. Although the cables are coated with plastic and made of multiple strands of steel wire, they may eventually become worn and break, especially when used after extensive periods of time without adjustment. Periodically (at least every 500 hours), the entire length of the three cables should be checked for broken wire strands, kinks, worn spots, or other failures. If any of these conditions are found in a cable or its coating, replace the cable. Check and adjust the cable tension, if necessary. This procedure is covered in the instrument calibration procedures later in this section.

ADJUSTMENT AND CALIBRATION PROCEDURES

Introduction

A thorough cleaning and inspection for loose, damaged, or worn parts should precede any adjustments. It is especially important to check the three pen drive cables for broken strands, worn spots, etc., at this time. After a 30-minute warm-up period, perform the adjustment procedures in a + 68 to + 86° F (+ 20 to + 30° C) environment.

Equipment Required

Large screwdriver.

7/16 in nutdriver (or screwdriver listed above).

Fish-weighing scales (0-6 lbs capacity).

Pozidrive screwdriver.

PBUS Extender Circuit Card 067-0813-00 (670-5235-00).

Voltmeter (DVM). Range, 0 to + 20 Vdc minimum; accurate within ± 0.05%. Also a range to + 1000 Vdc.

Short screwdriver with a narrow flat blade.

5/64 in Allen wrench bent at a 90° angle.

Pen Carriage Height Gauge 003-0957-00.

Two X-Axis Limit Switch Calibration Fixtures (003-0840-00).

Pozidrive screwdriver, very short.

Y-Axis Limit Switch Calibration Fixture (003-0849-00).

Oscilloscope. (A Tektronix 465 or equivalent.) Single trace with a vertical deflection factor of at least 5 mV per division and a sweep rate of at least 10 ns per division. Bandwidth should be from dc to at least 100 MHz.

C size plotting paper.

Square.

Preliminary Steps

1. Turn off the power to the Plotter and disconnect the power cord.
2. Lower the two end panels by turning the large quarter-turn end panel latches ¼ turn CCW. There are two latches on each end panel (see Figure 2-1).
3. When both end panels have been lowered, lower the front and back panels. To do this, unscrew each of four knurled thumbscrews that hold the front and back panels in place (see Figure 2-2).

X-Axis Cable Adjustments

For replacement of these cables, refer to Volume 2.

1. Attach a scale (like a fish-weighing scale) to a loop (you may have to tie one, preferably a Bowline) on the end of the front X-axis cable (see Figure 2-3). While loosening the cable tie-down screw next to the loop, maintain six pounds (2.7 kg) of tension in the cable.
2. Continue to maintain six pounds of cable tension while moving the Y-axis arm back and forth across the platen several times.
3. Tighten the cable tie-down screw (loosened in Step 1) while the scale continues to indicate six pounds of cable tension.
4. Repeat steps 1-3 for the rear X-axis cable (refer to Figure 2-4).

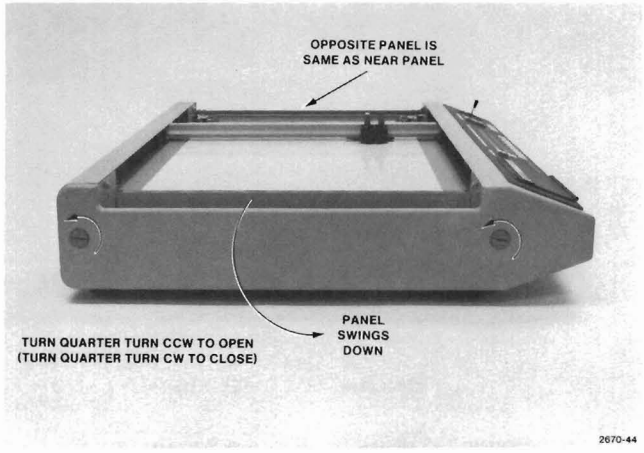

Figure 2-1. Side Panel Quarter-Turn Latches.

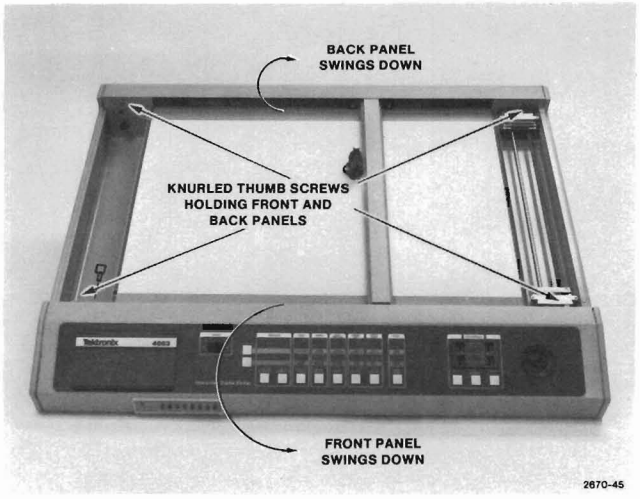

Figure 2-2. Front and Back Panel Thumbscrew Locations.

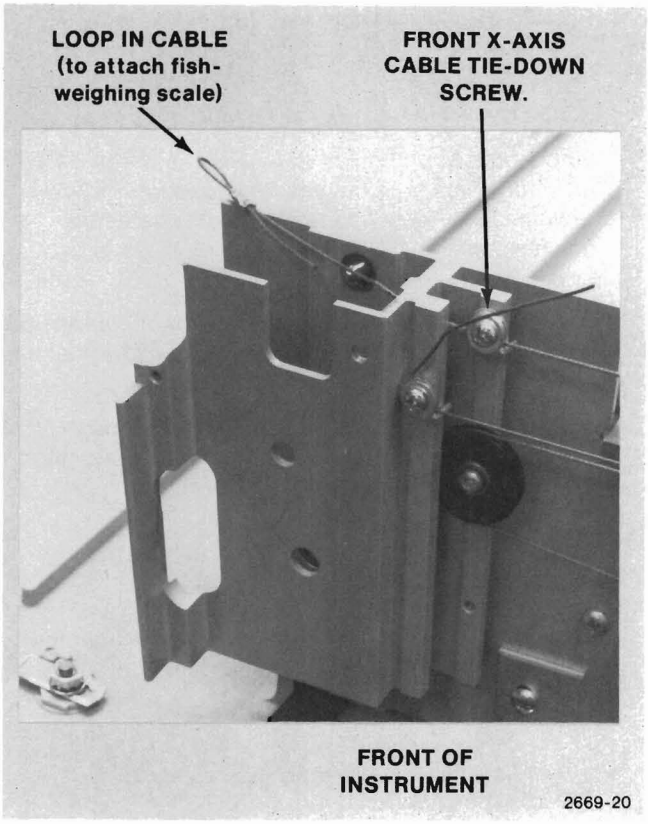

Figure 2-3. Front X-Axis Cable Tie-Down Screw and Loop Detail.

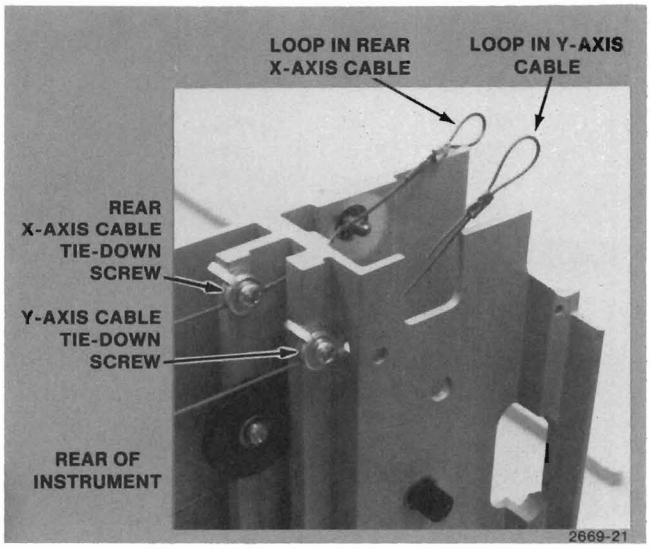

Figure 2-4. Y-Axis and Rear X-Axis Cable Tie-Down Screw and Loop Detail.

Y-Axis Cable Adjustment

For replacement of this cable, refer to Volume 2.

1. Attach the scale, used in the previous steps, to a loop on the end of the Y-axis cable (see Figure 2-4). (Again, you may have to tie a loop, preferably a Bowline.) While loosening the Y-axis cable tie-down screw, maintain three pounds (1.4 kg) of tension in the cable.
2. Continue to maintain three pounds of cable tension while moving the pen carriage back and forth along the Y-axis arm several times.
3. Tighten the cable tie-down screw (loosened in Step 1) while the scale continues to indicate three pounds of cable tension.

Power Supply Adjustment

1. Unscrew the eight nuts (on studs) which hold the pen drive mechanism assembly to the Plotter base (Figure 2-5).

CAUTION

Before tilting up the pen drive mechanism assembly in the next step, make sure the rear panel has been opened and swung down out of the way. Also, exercise care to avoid damaging or stretching the pen drive cables.

2. Grasp the front of the pen drive mechanism assembly under the corner brackets and lift the front of the assembly only, back to about a 45° angle. A support rod is stored along the right side of the circuit card cage to hold this assembly up. Insert the free end of the support rod into the hole located about three inches (75 mm) to the right of the front cable capstan (see Figure 2-6).
3. Remove the circuit card holding bracket (retainer). Then, insert the PBUS Extender circuit card into any of the unoccupied circuit card cage connectors on the right side of the circuit card cage.

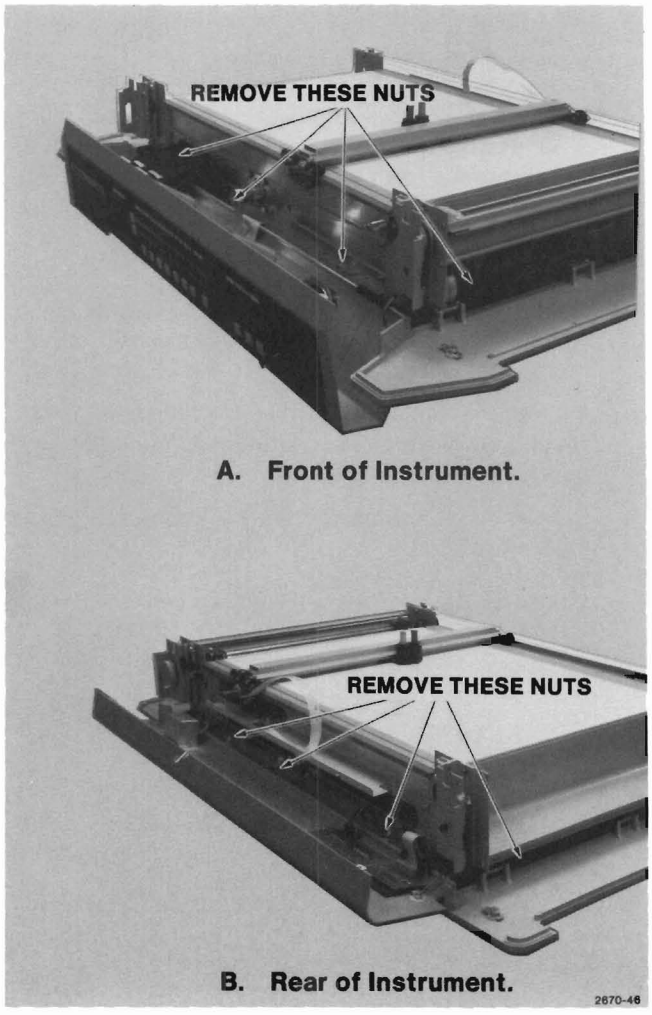

Figure 2-5. Nuts Holding the Pen Drive Mechanism Assembly.

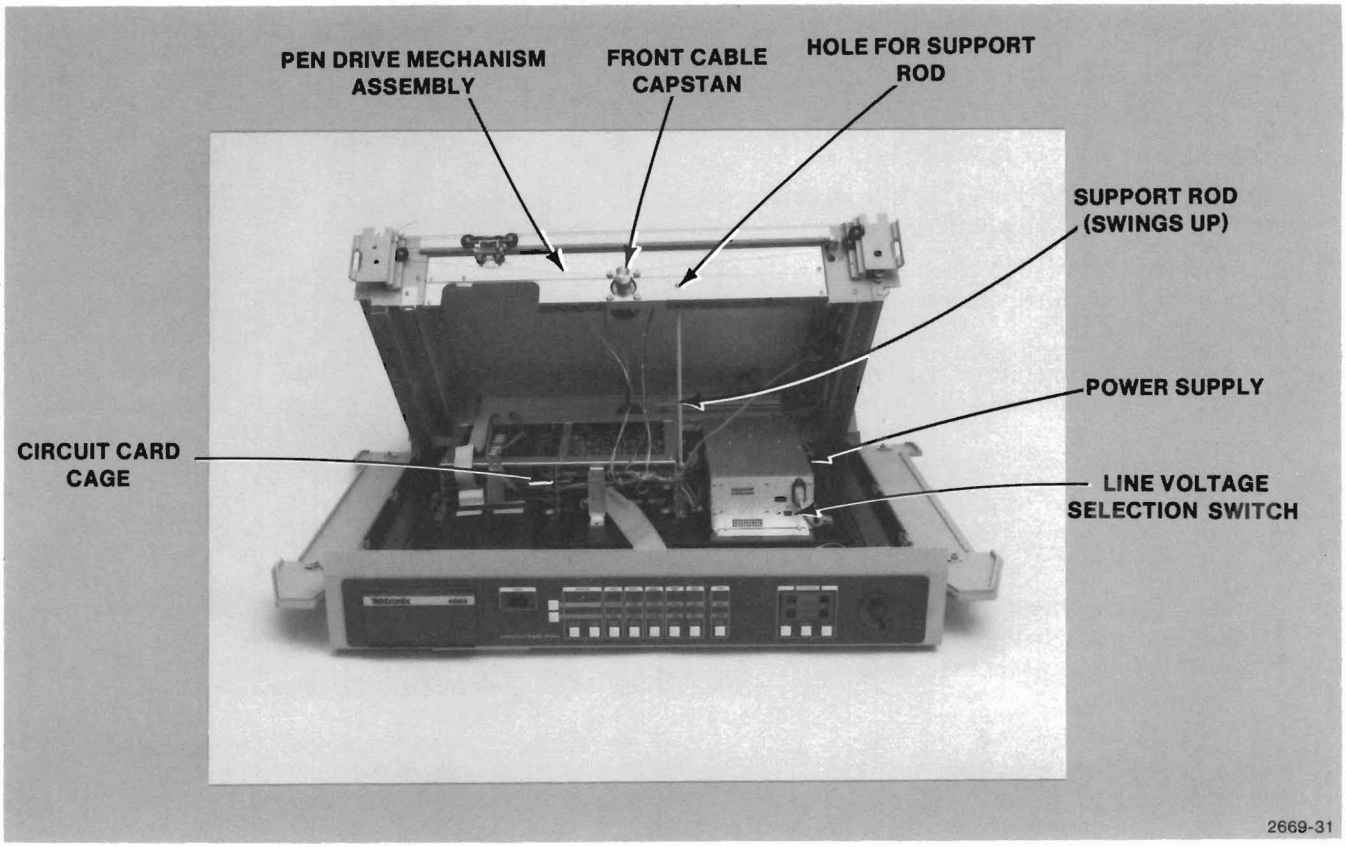

Figure 2-6. Access to the Plotter's Electrical Circuitry.

4. Plug the Plotter's power cable in and turn the POWER switch to ON. After about a five-second wait, the pen carriage moves to the upper-right corner of the platen. If the INIT light is still on, move the Parameter Entry card slightly (fully in) until the light goes out.

5. Connect the positive lead of the digital voltmeter to Pin 71 (+ 12 Vdc) of the Extender card. The other lead should be connected to GND (Pin 1, 2, 79, or 80). Adjust R1 on the back of the power supply (use a short screwdriver with a narrow, flat blade) to obtain a + 12 V ±60 mVdc reading.

6. Observe that the cooling fan is working. It is located between the circuit card cage and the power supply.

Joystick Sensitivity Adjustments

Y-Axis Adjustment

1. Insert the 5/64 in Allen wrench into the Y-axis adjustment hole shown in Figure 2-7.
2. Turn the wrench slowly until the Y-axis motor starts to turn. Note this wrench position.
3. Turn the wrench back the other direction until the motor begins to turn the other direction. Note this wrench position also.
4. Set the final adjustment near the center of these two extreme wrench positions.

X-Axis Adjustment

1. Repeat the Y-Axis Adjustment procedure for the X-axis adjustment.
2. See Figure 2-7 for the X-axis adjustment location. This will affect both of the X-axis motors together in the same manner as for the Y-axis motor.

X-Axis Limit Switch Adjustment

When you power up the Plotter, the pen carriage and the Y-axis arm move into the light beam of three carefully positioned photo-detectors (referred to as limit switches). These limit switches establish the initial pen position, and all subsequent plotting is done with reference to this position. Therefore, if any problems are noticed in the positioning of plots, calibrate these limit switches as follows:

1. Unplug J7, J8, and J9 from the Motor Pen Drive circuit card.
2. Connect the positive lead of the DVM to Pin 6 of the extender card (X LIM-1) and the negative lead to ground (Pin 1, 2, 79, or 80).
3. Attach the two X-axis limit switch calibration fixtures in place (see Figure 2-8). Both fixtures go on the right end (front and rear) of the instrument.
4. Move the Y-axis arm up against these two fixtures as shown in Figure 2-8.

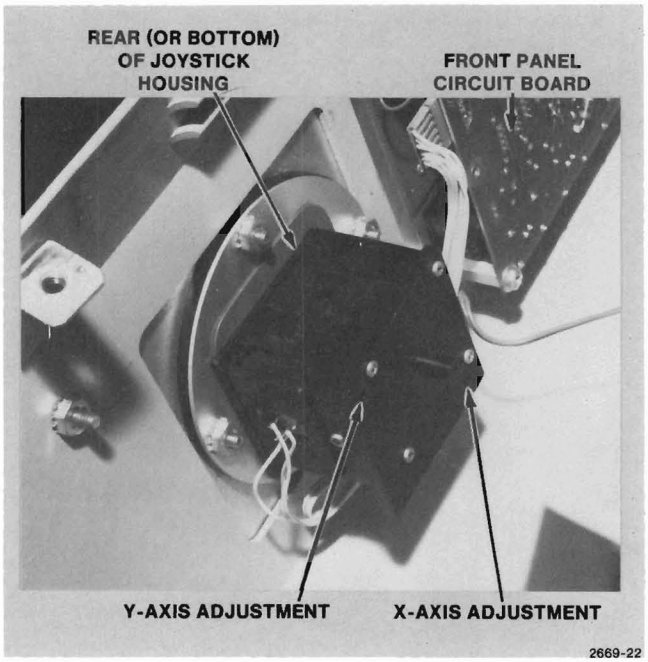

Figure 2-7. Joystick Adjustment.

5. Loosen (but do not remove) the locking screw on the underside of the front limit switch (see Figure 2-9).
6. Adjust the knurled thumbscrew to change the voltage observed on Pin 6 back and forth from a TTL high to a TTL low.
7. Tighten the locking screw on the underside of the front limit switch.
8. Repeat Steps 5-7 for the rear limit switch. This time, observe the voltage on Pin 8 of the Extender card. It may be necessary to use a short Phillips screwdriver to reach the locking screw on this limit switch.
9. Remove the X-axis limit switch calibration fixtures.

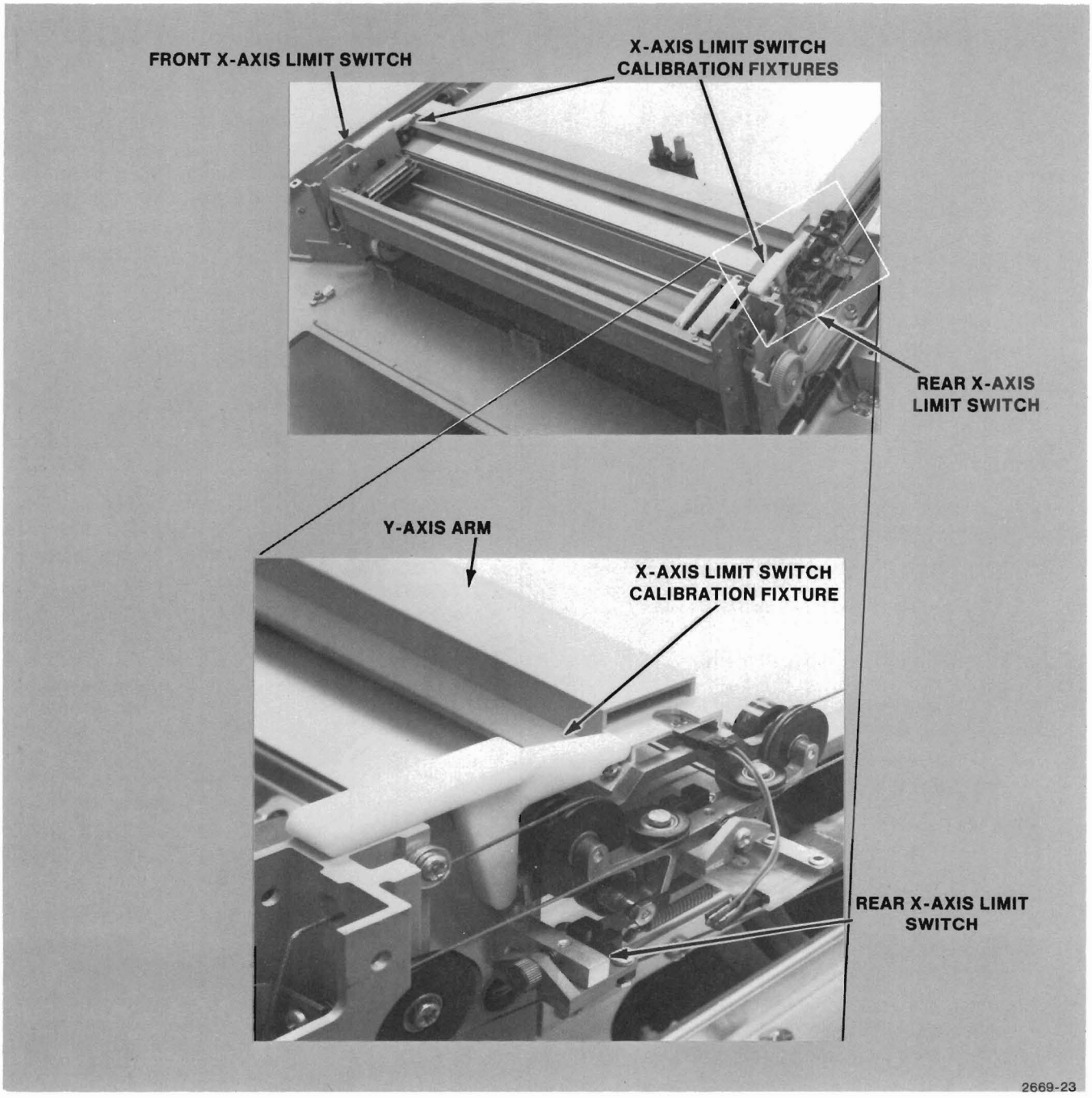

Figure 2-8. X-Axis Limit Switch Calibration Fixture Placement.

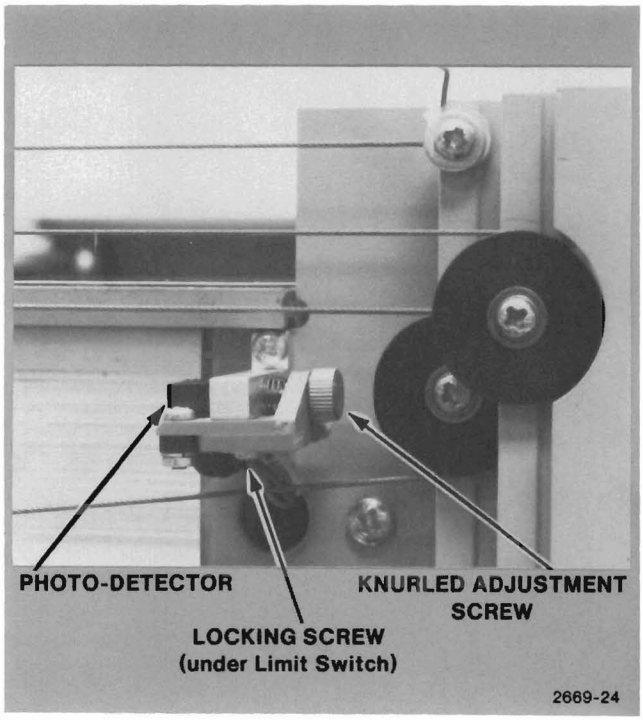

Figure 2-9. X-Axis Limit Switch Detail.

Y-Axis Limit Switch Adjustment

1. Attach the positive lead of the DVM to Pin 10 of the PBUS Extender circuit card.
2. Attach the Y-axis limit switch calibration fixture to the back edge of the platen (see Figure 2-10).
3. Move the pen carriage so that it presses firmly against the fixture as shown in Figure 2-10. Also ensure that the fixture is seated tightly against the back edge of the platen.
4. Loosen the locking screw under the Y-axis limit switch (see the insert in Figure 2-10). It may be necessary to use a short Phillips screwdriver.
5. Turn the adjusting screw (see Figure 2-10) until the observed voltage on Pin 10 of the Extender card changes back and forth from a TTL high to a TTL low.
6. Tighten the locking screw under the limit switch (loosened in Step 4).
7. Remove the Y-axis limit switch calibration fixture.
8. Reconnect J7, J8, and J9 to the Motor Pen Drive circuit card. (These were removed in Step 1 of the X-Axis Limit Switch Adjustments.)

Carriage Height Adjustment (Plotters with serial numbers B062075 and up)

Check the pen carriage height by using the Pen Carriage Height Gauge. Lay the gauge flat on the platen surface. Attempt to slide either end of the gauge under the pen carriage as shown in Figure 2-9A. The shaved end of the gauge should slide under the carriage easily. The thick end should not.

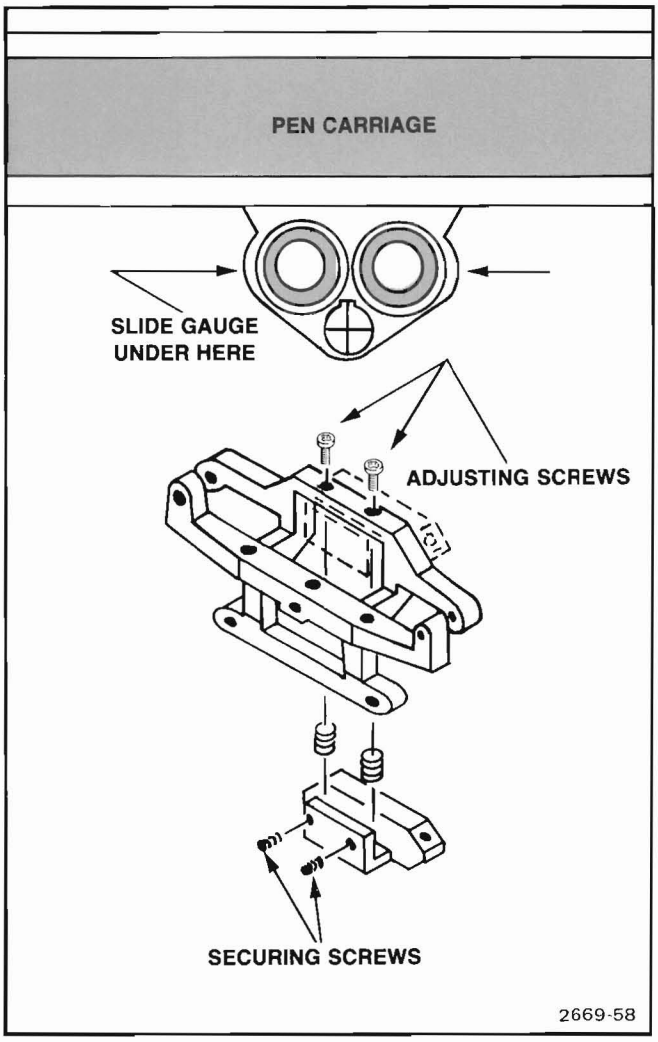

Figure 2-9A. Pen Carriage Height Adjustment.

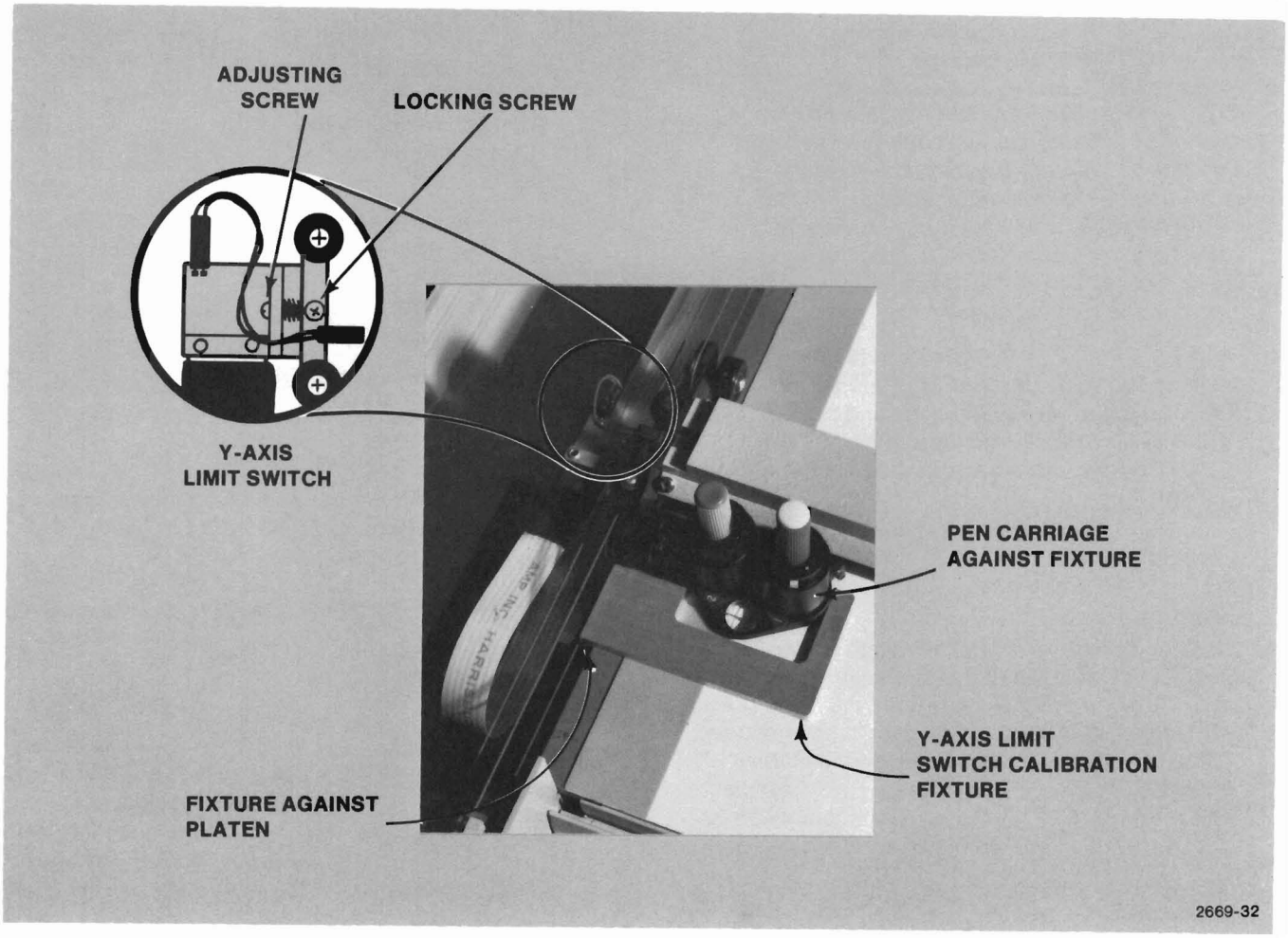

Figure 2-10. Y-Axis Limit Switch Calibration Fixture Placement.

Raise or lower the carriage height as follows:

1. Loosen the two setscrews at each end of the carriage (Figure 2-9A).
2. Adjust the adjustment screws in the rail adjusters until the pen carriage height is between 0.085 and 0.105 inches from the platen surface as measured with the Pen Carriage Height Gauge. The height should be checked at several locations on the platen surface.
3. When the pen carriage is set at the proper height, tighten the two setscrews in each rail adjuster to secure the adjustment screws at the proper setting.

Measuring Platen Electrostatic Voltage

WARNING

Dangerous voltages are measured in this procedure. While making these measurements, make sure that you are not touching the voltmeter probe tip and that the probe tip does not touch other components or the Plotter chassis. In addition, use only one hand to hold the voltmeter probe and make sure that no part of your body is touching the Plotter chassis.

1. Place the Plotter in SHEET mode (if not already in this mode). To do this, pull the Parameter Entry card out to the Media Form line and press the switch over SHEET. Then press the MEDIA CHANGE front panel switch twice.
2. Set the voltmeter to read the + 1000 Vdc scale.
3. Attach the negative voltmeter lead to Pin 6 of J11 on the Motor Pen Drive circuit card (see Figure 2-11).
4. Carefully attach or touch the positive voltmeter lead (probe) to each of the four load resistors directly behind J11 as shown in Figure 2-11. A reading of + 880 Vdc ±10% should be measured at each resistor. The input impedance of the voltmeter will affect this reading. The technician should interpret this reading with the input impedance of the voltmeter in mind.

NOTE

If an attempt is made to measure this voltage on Pins 1-4 of J11, the input impedance of even a 10 MΩ voltmeter will place a sizable load on the High Voltage Platen Power Supply. This will lower the voltmeter reading and provide an inaccurate check.

Processor Timing Checks

1. Attach an oscilloscope lead to Pin 77 (MASTER CLOCK) of the Extender card. Set the oscilloscope to 10 ns/DIV and 2 V/DIV. Check that the MASTER CLOCK has a period of 67.8 ns (or 6.8 DIV on the scope).
2. Attach the oscilloscope lead to Pin 27 (INTERRUPT TIMER) of the Extender card. Set the oscilloscope to 1 ms/DIV and 2 V/DIV. Check that the period of the INTERRUPT TIMER is 8 ms (or 8 DIV on the scope). Tolerance is ±10% or ±0.8 ms.
3. Turn the Plotter's power OFF.
4. Remove the Extender circuit card.
5. Replace the circuit card retainer.
6. To return the Plotter back to its normal mechanical configuration, perform Steps 1-5 of Appendix C (Volume 2) in reverse order.

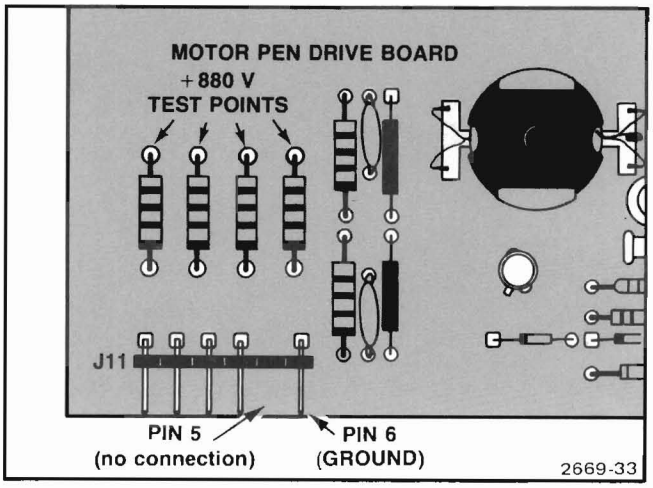

Figure 2-11. Platen Electrostatic Voltage Test Points.

Pen-To-Pen Registration Check

1. Turn the Plotter's power back ON.
2. With a pen in each pen holder (preferably each pen should have a different color) and a sheet of C size paper on the platen, press PEN SELECT 1, unless that light is already on.
3. Move the pen carriage near the middle of the platen.
4. Press the UP/DOWN switch, turning that light on. The pen carriage should move toward the rear of the instrument slightly and to the left (nearly a 45° angle). Then the pen should lower to the paper.
5. Press the UP/DOWN switch again, turning that light off. The pen should move back to its original position, leaving a dot on the paper.
6. Press PEN SELECT 2, turning that light on and the PEN SELECT 1 light off.
7. Press the UP/DOWN switch again, turning that light on. The pen carriage should move toward the front of the instrument slightly and to the left (nearly a 45° angle) before lowering to the paper.
8. Press the UP/DOWN switch again, turning that light off. The pen should move back to its original position, leaving a dot on the paper.
9. Verify that these two dots are on top of each other.

Orthogonality Check

1. Pull the Parameter Entry card out and make the following entries:

   INITIAL PAGE SIZE: C
   PAGE ORIENTATION: HORIZONTAL
   INITIAL ASPECT RATIO: FULL PAGE
   AXIS ORIENTATION: Column 1

2. Press OUTLINE VIEWPORT. Remember to press the lower of the two left SHIFT switches prior to pressing the PLOT CONTROL switch. The Plotter should draw a rectangular box which has the dimensions shown in Table 1-7. Measure these to verify size accuracy and use a square to verify orthogonality.

Lamp Test

1. Pull the Parameter Entry card out to the EXECUTE SELF TEST line and press the switch over column 2. All of the front panel lights (except the Parameter Entry light) should come on.
2. Replace any lights that are not on (see Volume 2).
3. Press the switch again to extinquish the lights.

Line Quality and Accuracy Check

1. Press the switch over column 1 (on the EXECUTE SELF TEST line). The Plotter should draw a plot similar to that shown in Figure 2-12.
2. Examine this plot for line quality and accuracy. Early in the plot, the Plotter draws the right side of the center "X" in the box; finally, after permitting the technician to briefly exercise the joystick, the Plotter completes this center "X." Verify that the Plotter has not lost any positional accuracy by examining the center of the "X."
3. If the line quality checks indicate non-straight lines, the three dampers might be suspect. There is one damper on the end of each pen drive motor capstan, except on early model Plotters which do not use dampers. The damper is an oil-filled, inertia-absorbing device. Check to see if oil has leaked out. Notice that the damper is not entirely filled with clear-colored oil; there should be a bubble of about 1/4 to 1/3 of the damper's volume.

Joystick Operational Check

1. Move the joystick control.
2. Verify that the pen carriage moves in the direction that the joystick handle is pressed and that its speed is dependent upon the deflection angle of the joystick handle.

Media Advance Clutch Tension Check

1. If the Plotter is equipped with Option 36, check the paper roll clutch assembly tension. To do this, first disengage the paper from the paper drive tractors. Then, pull the paper from the roll at least six inches (150 mm) and release. The paper roll should rewind at least ½ to ¾ revolution. If it does not, refer to Appendix A of Volume 2 for the clutch adjustment (under Option 36 Installation).
2. Thread the paper back into the paper drive tractors.

Media Advance Adjustments

1. Refer to Section 2 of the Operator's Manual for adjustments of the paper drive mechanism. There are two adjustments: one to accommodate different paper widths, and the other to adjust the paper laterally. Adjust both as necessary.
2. Turn the Plotter's power off.

This completes the adjustment and calibration procedures for the 4663 Plotter.

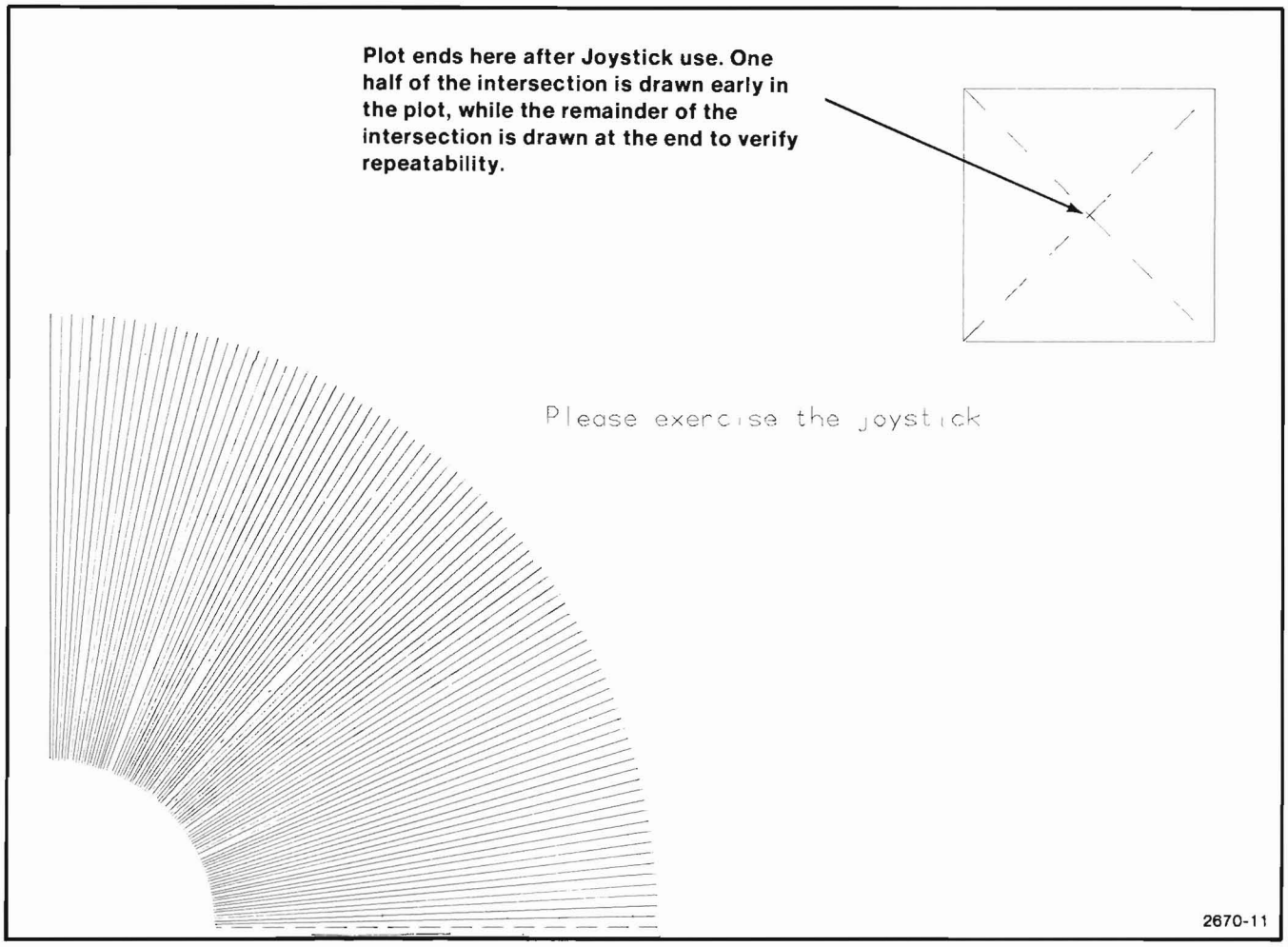

Figure 2-12. Test Pattern Produced by Self-Test Feature.

Section 3

THEORY OF OPERATION

SYSTEM DESCRIPTION

The basic electronics structure of the 4663 Plotter is composed of functional blocks residing on a central bus. A diagram of this structure is shown in Figure 3-1. The central bus is an 80-pin backplane circuit card cage and most functional blocks, representing circuit cards, connect directly into this backplane. There are a few exceptions, however, where a functional block does not connect directly to the bus. First, the Parameter Entry, Front Panel Switches and Lights, and the ROM Patch blocks "piggy-back" onto other modules, which in turn, are connected to the central bus. Second, the Motor Pen Drive block is functionally piggy-backed, or indirectly connected, to the Vector Generator module, simply because this block communicates primarily with the Vector Generator. Physically, however, the Motor Pen Drive circuit card connects into the backplane to obtain its power. Figure 3-1 shows the functional piggy-back relationships.

The 4663 Plotter contains two microprocessors. The 6800 residing on the Processor circuit card controls the overall operation of the Plotter. The second microprocessor (an 8X300) resides on and controls the operation of the Vector Generator functional block. The Plotter is electrically organized such that the 6800 microprocessor views all other functional blocks as peripheral devices, including the Vector Generator and its microprocessor.

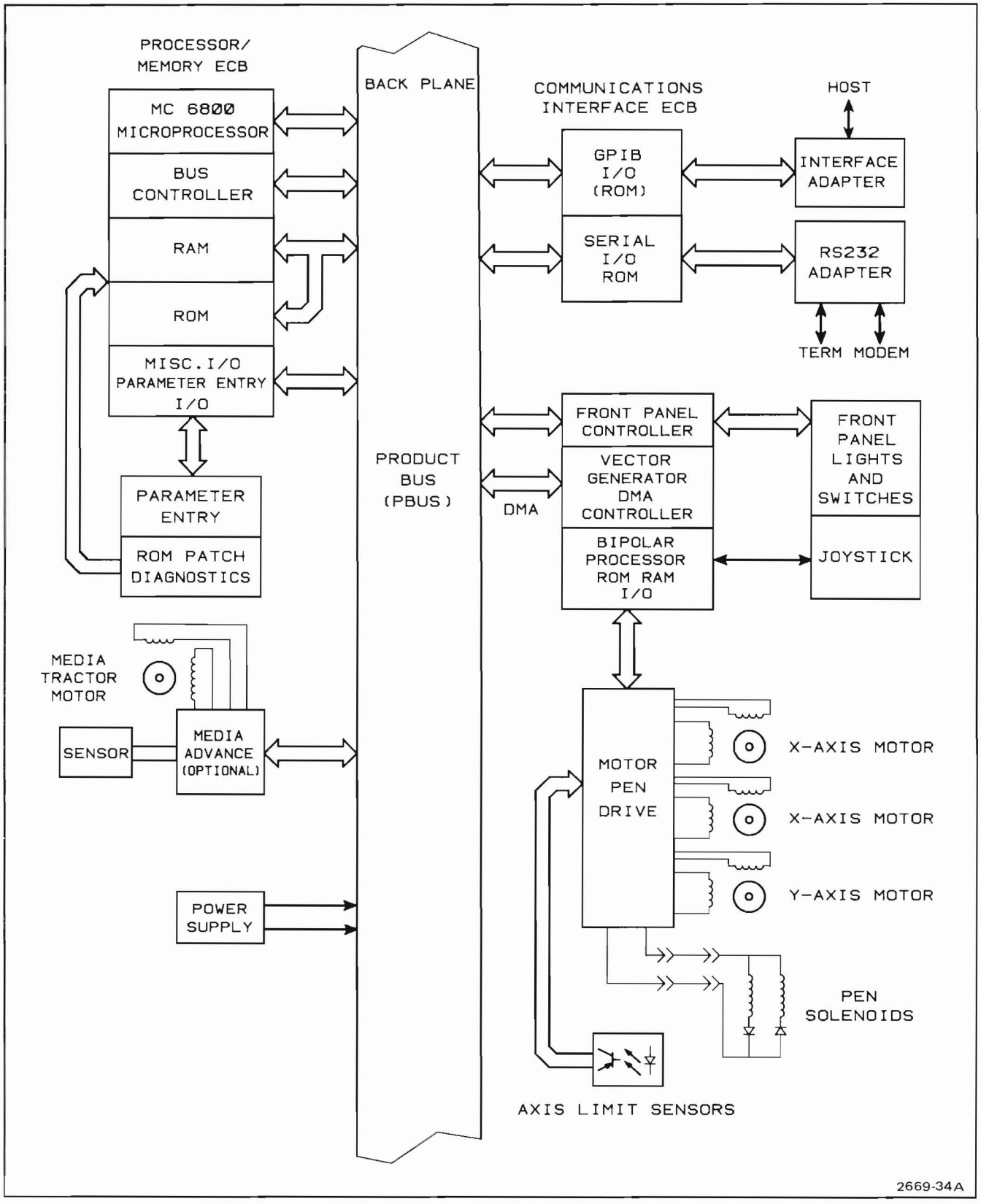

Figure 3-1. Functional Block Diagram of the 4663 Plotter.

BACKPLANE (CENTRAL BUS)

The 4663 Backplane is a circuit board with eight 80-pin connectors, each of which is designed to connect to a circuit card. This arrangement forms a bus structure between the other functional blocks. (In most cases, each functional block represents one circuit card.) A diagram of the 4663 Backplane and the functional blocks that connect directly to the Backplane are shown in Figure 3-2.

NOTE

The right and left sides of the Backplane are **NOT** *symmetrical. Therefore, it is not possible to interchange circuit cards from the left side to the right side and vice-versa. However, it is possible to interchange any of the cards within a side.*

A detailed description of the electrical signals on the Backplane is located in Appendix A of this volume. A pin/signal list is included in Volume 2.

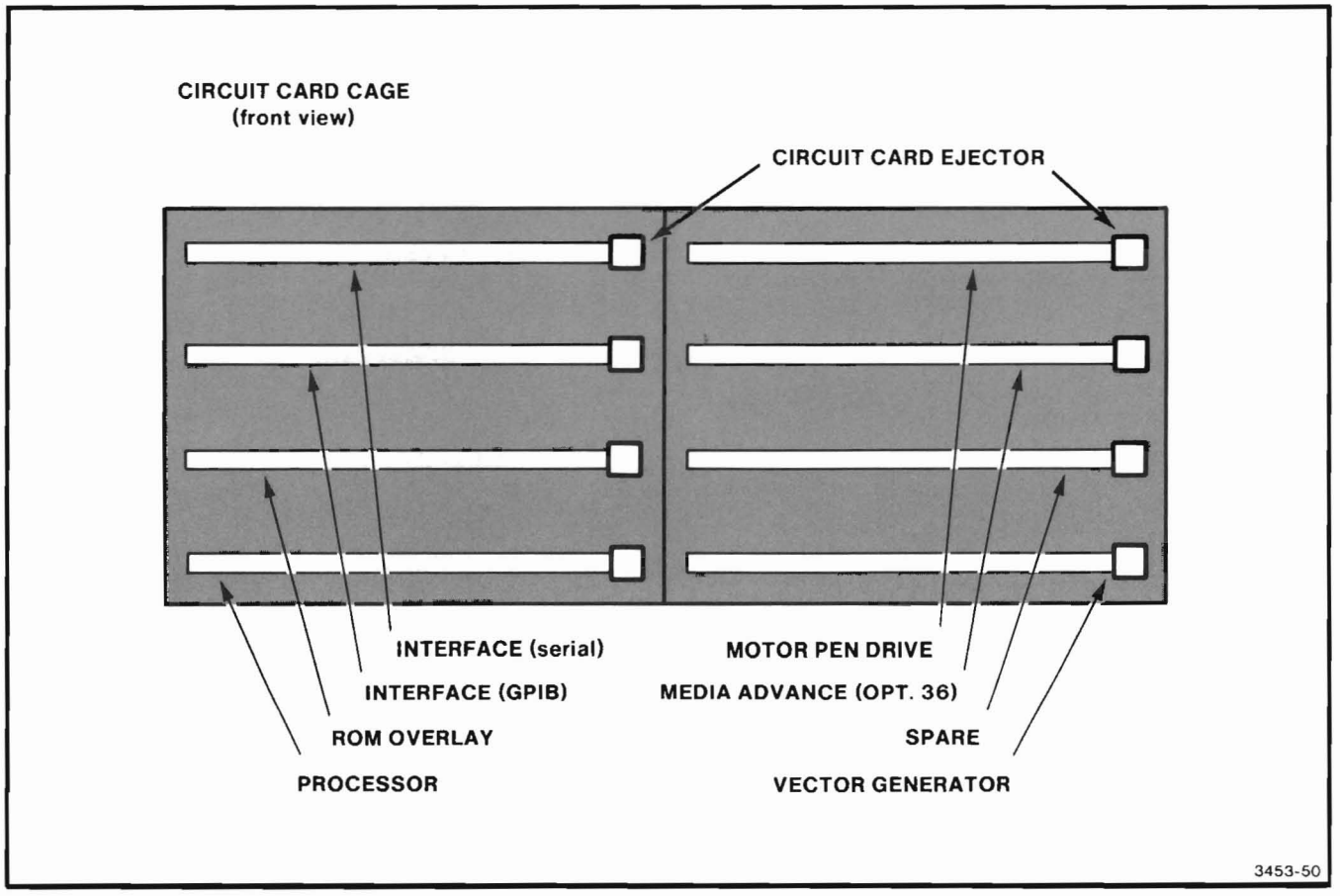

Figure 3-2. 4663 Backplane.

INTER-FUNCTIONAL BLOCK COMMUNICATIONS PROTOCOL

Following is a description of the communications protocol between the functional blocks in the 4663. The basic transactions are the following:

Read
Write
Interrupts
DMA (Direct Memory Access)
I/O Addressing (In/Out)

The rest of this section gives detailed circuit descriptions.

NOTE

For the purposes of this manual, "Processor" refers to the main Plotter microprocessor (i.e., the 6800).

Read Cycle Description

The Read transaction begins when the Processor places the BUS ADDRESS on lines BA0-1 to BA15-1. (This is labeled as **1** in Figure 3-3.) The address is simultaneously qualified as valid by ADDRESS STROBE (ASTB-0), also sent from the Processor. One bus clock cycle later, at **2**, the address value has settled and can be considered valid. Notice that the WRITE-0 control line is not asserted with the address in this example; this indicates a Read transaction is occurring. Several bus clock cycles (at a frequency of 14.7456 MHz) later, at **3**, the device being read (a RAM, ROM, or I/O register) places BUS DATA on the lines BD0-1 to BD15-1. BUS DATA is simultaneously qualified as valid by DATA STROBE (DSTB-0), which is also sent from the device being read. One bus cycle later, at **4**, the data value has settled and can be considered valid.

The delay between address assertion by the Processor and data response by the device being read is the device access time; it may range from one bus clock cycle (67.8 ns) up to when the total read transaction is completed (within 3.8 μs, which is the bus timeout period). The assertion of ASTB-0 must precede DSTB-0 by at least one bus clock cycle. If DSTB-0 is not asserted before the bus timeout period, the Processor assumes the device being read is non-existent and automatically terminates the transaction by releasing

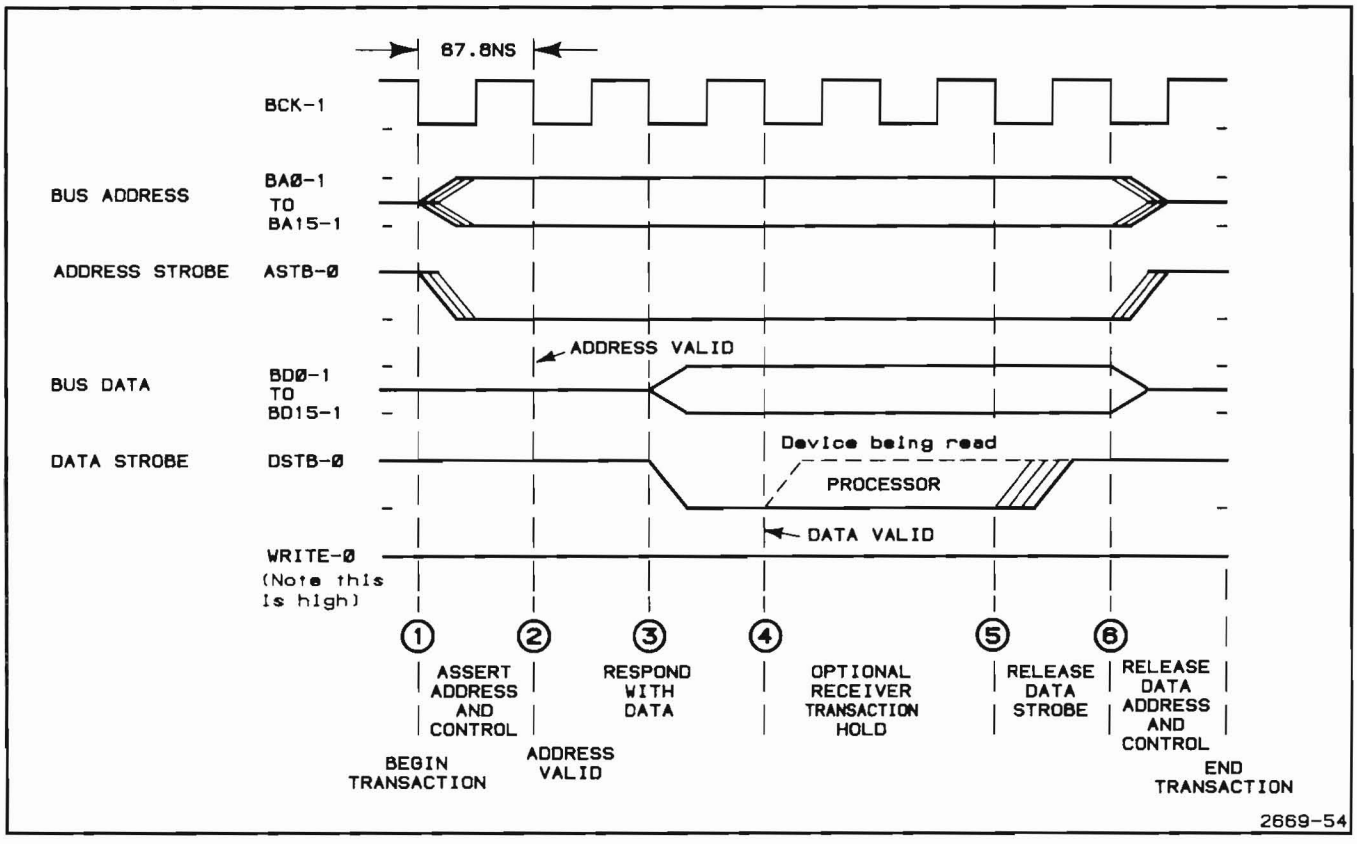

Figure 3-3. Bus Read Transaction Timing.

both BUS ADDRESS and ASTB-0. The Bus Control causes the BUS TIMEOUT INTERRUPT to be generated to the Processor whenever the bus timeout period has been exceeded.

One clock cycle after the device being read has asserted DSTB-0 (at **3**), the device releases it (at **4**, when data is defined as valid). If the Processor requires a longer hold time for the data, it must now assert DSTB-0. This ensures that the Processor has control of the transaction and can delay the termination if necessary. At **5**, the Processor releases DSTB-0, indicating that it has read the BUS DATA. Finally, one bus clock cycle later, at **6**, the Processor releases BUS ADDRESS and ASTB-0, which also causes the device being read to release BUS DATA. This completes the entire Read transaction. On the next falling edge of the bus clock, a new transaction can begin with the assertion of a new BUS ADDRESS by the Processor.

Write Cycle Description

The Write transaction begins when the Processor places the BUS ADDRESS on the lines BA0-1 to BA15-1. (This is labeled **1** in Figure 3-4.) The address is simultaneously qualified as valid by ADDRESS STROBE (ASTB-0), which is also sent from the Processor. One bus clock cycle later, at **2**, the address value has settled and can be considered valid. Notice that the WRITE-0 control line is also asserted with the address in this example. This indicates that a Write transaction is occurring. Several bus clock cycles later, at **3**, the Processor places BUS DATA on the lines BD0-1 to BD15-1. The BUS DATA can be considered valid one bus clock cycle later, at **4**, when the data value has settled. The delay between address assertion by the Processor and data assertion may range from one bus clock cycle up to when the total write transaction is completed (within 3.8 μs, which is the bus timeout period). The assertion of ASTB-0 must precede DSTB-0 by at least one bus clock cycle.

All information is now valid, and at **4** the Processor releases DSTB-0, since it was held for one bus clock cycle. The device being written to must now assert DSTB-0 for a minimum of one bus clock cycle until at least **5**. If the device being written to requires a longer hold time for the data, it must continue to hold DSTB-0. This ensures that the device has control of the transaction and can delay the termination, if necessary (in case the device has a slower memory, for example). If the device does not hold DSTB-0, the Processor assumes that the device being written to is non-

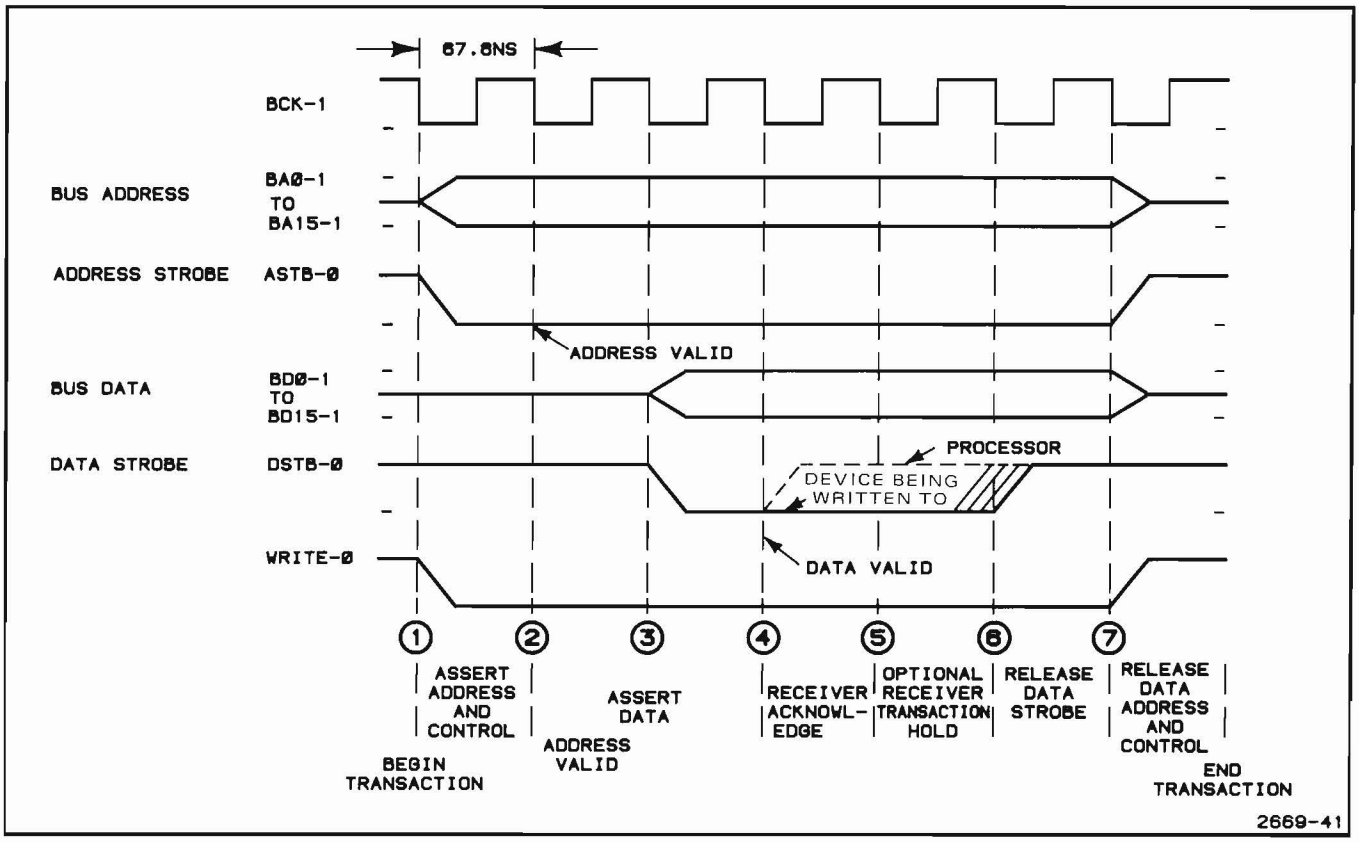

Figure 3-4. Bus Write Transaction Timing.

existent and automatically terminates the transaction by releasing both BUS ADDRESS and ASTB-0. The Bus Control causes the BUS TIMEOUT INTERRUPT to be generated to the Processor if the bus timeout period has been exceeded. This might occur, for example, if a memory location has failed.

When the device being written to has stored the BUS DATA, it releases DSTB-0, at **6**. This signals the Processor to end the write cycle. On the next bus clock cycle, at **7**, the Processor releases BUS ADDRESS, ASTB-0, WRITE-0, and BUS DATA. Then, on the next falling edge of the bus clock, a new transaction can begin when the Processor asserts a new BUS ADDRESS.

Interrupt Operation

The Plotter is an interrupt-driven device. This means that each module has a predetermined interrupt level visible to the 6800 Processor. Before a functional block receives or generates some activity, it must first interrupt the Processor. The Processor completes its present activity and then services the interrupt, unless a higher priority interrupt comes along. The interrupt is serviced according to a set of instructions stored in ROM (the system firmware). This means that if a functional block generates (or transmits) a request for action to another block(s), it must first convert the request (or data) into an 8-bit data byte(s) before interrupting the Processor. Some typical requests that generate interrupts include pressing a front panel switch, host-generated commands, joystick commands, generating output responses to the communications interface, turning the front panel lights on or off, etc.

The Plotter uses eight levels of priority-vectored interrupts to identify the functional block requesting the interrupt. The Processor can then access the system firmware for instructions on servicing that interrupt, since each interrupt level has its own interupt vector in the system firmware (ROM).

The eight levels of priority interrupt are used with a serial poll scheme, which is controlled with a three-bit counter (Interrupt Poll Counter, located on the Processor circuit card). This counter runs continuously on the bus at one-half the bus clock frequency (or 7.3728 MHz). The three counter lines are INTERRUPT POLL 0-1 to INTERRUPT POLL 2-1 (IRP0-1 to IRP2-1). When a functional block with a pending interrupt sees its preassigned (strapped) interrupt level appear, it asserts INTERRUPT REQUEST (IRQ-0). This signals the Processor to begin its interrupt sequence. If, however, the Processor is busy at that time and can not immediately service the interrupt, the Interrupt Poll Counter continues to count. However, the limits of the count are modified to eliminate counts of a lower priority. This means that the counter counts only between 0 (the highest priority) and the level of the pending interrupt, but no lower. Each time the counter counts to a lower priority level, the functional block with a pending interrupt drops the IRQ-0 signal. The poll count therefore continues, scanning only for higher priority interrupt levels. When the Processor finishes its present activity and reaches the vectoring stage of the interrupt cycle, the current pending interrupt having the highest count is used to locate the next interrupt vector.

A higher level (priority) interrupt, if one occurs before the Processor's vectoring in the interrupt sequence has started, may subsequently update a lower priority limit. This means that a functional block with a higher interrupt level can come along and also assert IRQ-0 when it sees its strapped interrupt poll count. Then, all subsequent poll counts will be between the highest priority and the new interrupting device's level. Therefore, the device with the first interrupt will not be included in the poll count. After the Processor has serviced the highest priority interrupt, the poll will expand again to include the lower priority levels (or down to the next highest priority level with a pending interrupt). This expansion occurs when the interrupt service firmware handler writes a new interrupt control byte to the interrupt poll hardware.

A table of the plotter's assigned interrupt levels is shown in Appendix E of Volume 2.

A timing diagram of the interrupting process is shown in Figure 3-5; the following discussion explains the key points in this diagram.

The INTERRUPT REQUEST POLL (IRP0-1 to IRP2-1) occurs synchronously with bus clock (but at one-half the frequency) but asynchronously with any bus transactions, (shown by **1**). A level 2 module with a pending interrupt sees the level 2 poll count at **2** and asserts INTERRUPT REQUEST (IRQ-0). This action now establishes the lower priority limit at 2, resets the poll counter, and initiates the Processor's interrupt service cycle.

The interrupt request poll continues over the range 0-2. Notice that whenever the poll count is anything but 2, the level 2 interrupting device releases IRQ-0. Then, before the Processor can clear the level 2 interrupt, a level 1 module with a pending interrupt appears, at **3**. This level 1 interrupting device sees the level 1 poll count appear and asserts an INTERRUPT REQUEST (IRQ-0), which establishes 1 as the new lower priority level at **4**.

With two interrupts now pending, the Processor finishes the current transaction while the poll continues to count within the new limits 0-1. After the Processor has completed the prior transaction and the poll counter has counted to the level number of the interrupting module (in this case 1), the Processor locates the interrupting vector and transfers to the appropriate service routine in system firmware to clear the interrupt at **5**. Since the poll counter is now limited to level 0 and 1 interrupts, the pending level 2 interrupt must wait until the Processor is finished with higher priority transactions. After the level 1 interrupt is cleared, the poll counter is allowed to count again until it reaches the next highest priority interrupt level (which is now level 2) at **6**.

The level 2 interrupt establishes the upper scan register at 2 and initiates another interrupt cycle by asserting IRQ-0, and the process is repeated until this interrupt is also cleared. Then, with no other interrupts pending, the interrupt poll counter proceeds to count between 0 and 7, waiting for another interrupt from one of the 4663 functional blocks.

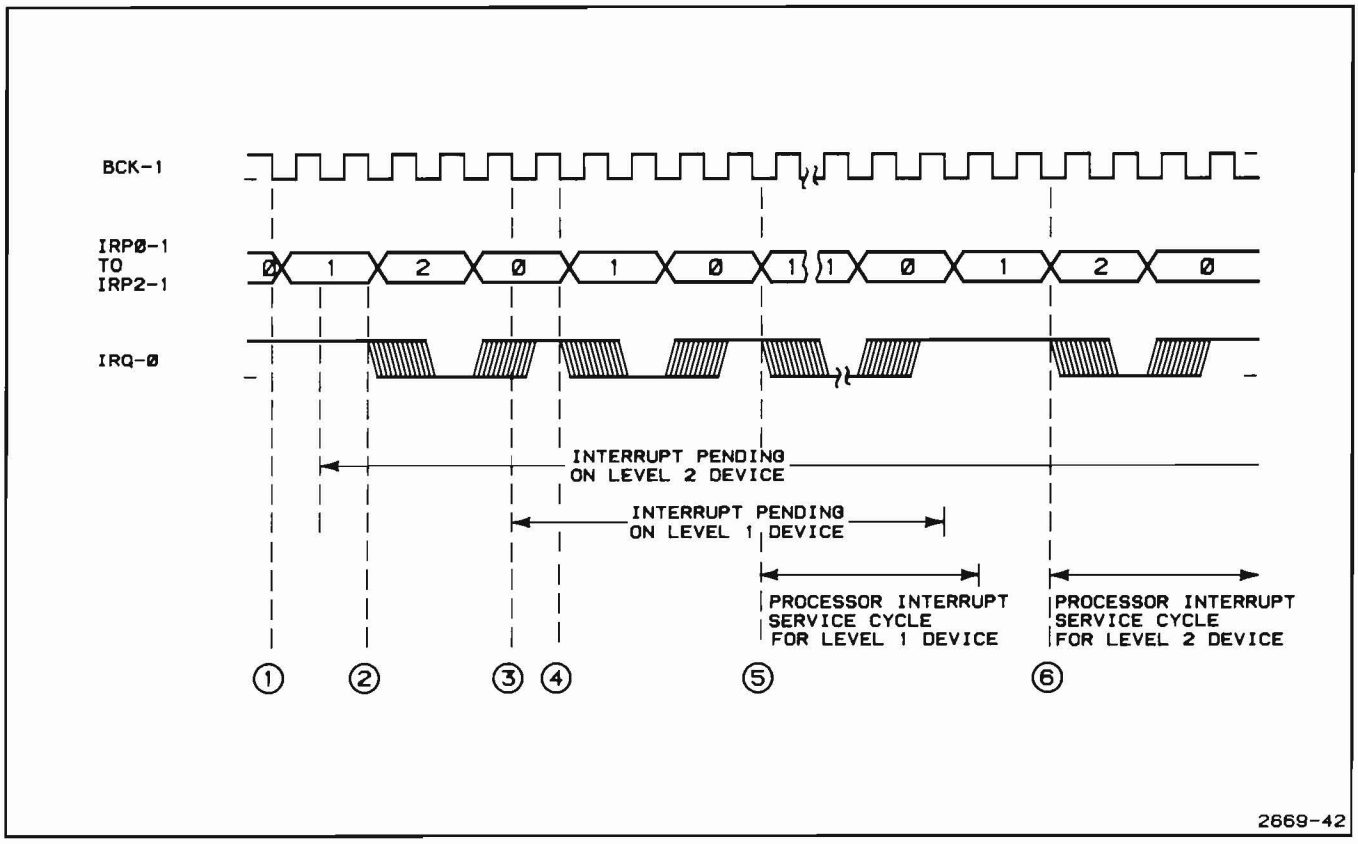

Figure 3-5. Bus Interrupt Timing Diagram.

Bus DMA Operation

In the interest of speed, the Vector Generator through its DMA (Direct Memory Access) Control receives all of its data from the "circular queue," a 64-byte portion of the main system RAM. The DMA Bus Control in the Processor module transfers data to the Vector Generator's DMA Control during the Processor's Phase 1 clock time (when the Processor is inactive). (Phase 1 and Phase 2 descriptions are given later in the Processor circuit descriptions.) The DMA Bus Control transfers the data one character at a time. Once the Vector Generator DMA has received the data, the 8X300 Processor can read it to compute a subsequent Move or Draw. During Phase 2, the 6800 resumes its normal activity. On the following Phase 1, the two DMA ports can transfer another character from the circular queue. So, the main Processor operates during Phase 2, and the Vector Generator gets its data during Phase 1. Once a move or draw vector is computed, the Vector Generator generates pen drive motor signals. The Motor Pen Drive circuit card uses these signals to produce currents and voltages for the three pen drive motors and the two pen solenoids.

The structure of the bus is such that there is a single master Processor (the 6800) and up to eight DMA (Direct Memory Access) devices. However, in reality, only one DMA device is actually present. This is the 8X300 microprocessor in the Vector Generator module. The DMA scheme uses a 3-bit counter, the Bus Request Poll Counter, which is similar to the Interrupt Poll Counter described previously. The Bus Request Counter runs continuously on the bus at one-half the bus clock frequency (7.3728 MHz). The three lines used by this counter are BUS REQUEST POLL (BRP0-1, BRP1-1, and BRP2-1).

A DMA operation can take place anytime that the bus is free (for example, during the Processor's Phase 1 clock cycles). First, the Vector Generator DMA Control asserts BUS REQUEST (BRQ-0) when it sees its address (001) on the BUS REQUEST POLL lines. However, unlike the Interrupt Poll Counter, BRQ-0 halts the Bus Request Poll count at 1. After the Processor has completed its present transaction, and Phase 1 has started, the Processor's DMA control asserts BUS GRANT (BGRNT-0) on the first falling edge of bus clock. This indicates that the bus is free and the Vector Generator's DMA Control may use the bus for one character transfer.

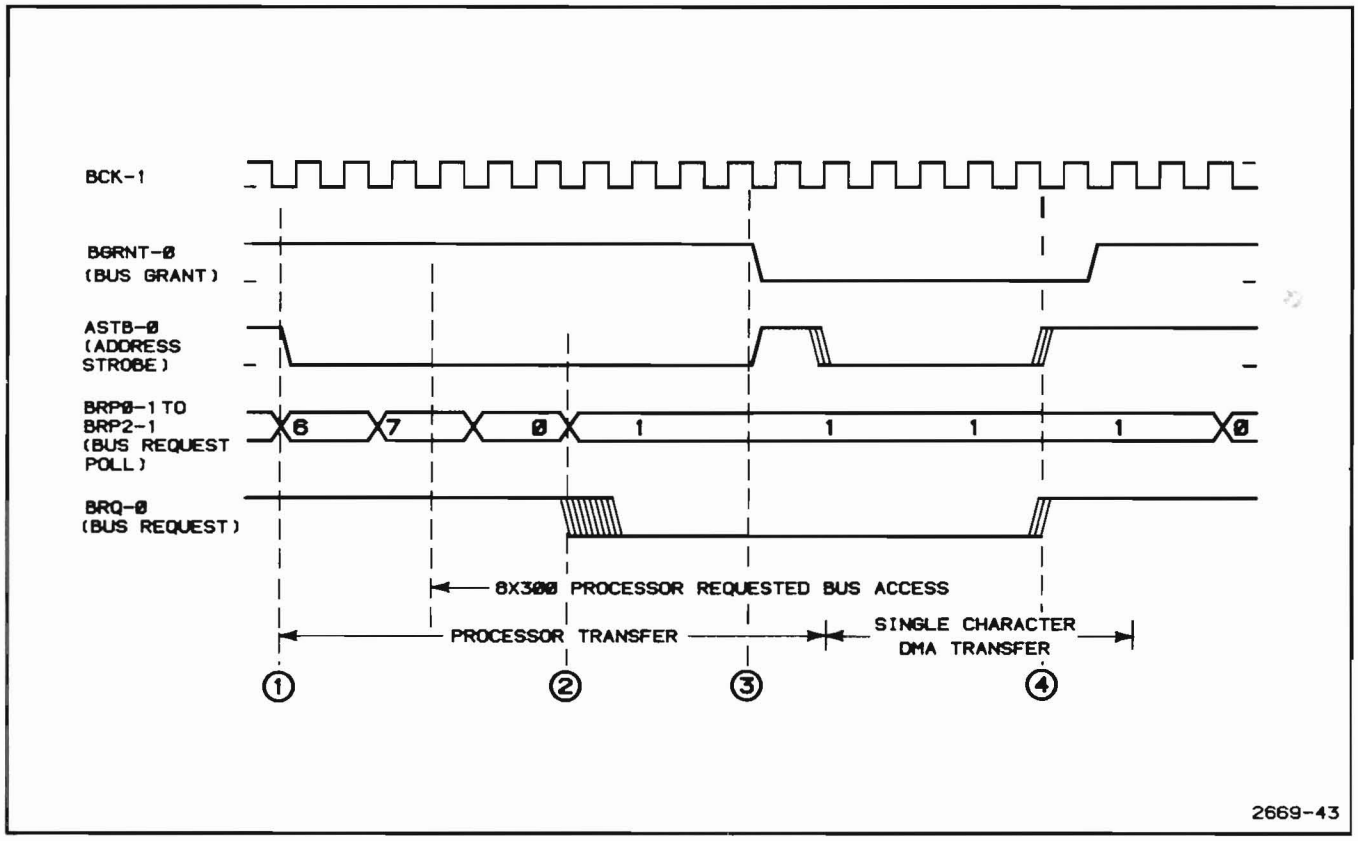

Figure 3-6. Bus Character DMA Timing Diagram.

When the DMA transfer is completed, the Bus Request Poll Counter is allowed to count over all of the eight DMA levels. The DMA transfer must begin immediately after the last Processor transaction to avoid tying up the bus and exceeding the bus timeout period. (The Processor must be able to access the bus during the next Phase 2.) If the DMA transaction exceeds the bus timeout period (3.8 μs), the Processor's DMA Bus Control releases BGRNT-0. This causes the Vector Generator DMA Control to release all lines asserted on the bus and terminates its transaction. The DMA Bus Control will then generate a BUS TIMEOUT INTERRUPT to the Processor, informing the Processor that the DMA operation failed.

A typical timing diagram in Figure 3-6 illustrates the DMA transfer procedure. The following paragraphs discuss this diagram in detail.

The BUS REQUEST POLL (BRP0-1 to BRP2-1) occurs synchronously with the bus clock (but at one-half the frequency) but asynchronously with any bus transactions. A Processor transaction is shown beginning at an arbitrary point, indicated by **1**, in the bus request poll. Since the 8X300 does not require the bus at this time, the Bus Request Poll Counter counts from 0 to 7 and repeats this count continuously.

At **2**, the 8X300 processor, which wishes to access the bus, has recognized its strapped count (1) on the poll line (BRP0-1 to BRP2-1) and has asserted BRQ-0. This halts the poll counter at a count of 1. The poll counter remains halted as long as BRQ-0 is asserted. The 8X300 is now prioritized and must wait for BGRNT-0 from the Processor before beginning a DMA transfer.

At **3**, the Processor asserts BUS GRANT (BGRNT-0) in response to the 8X300's BRQ-0. This indicates that the Processor has completed its transaction and that the bus is available for the DMA transfer (which must begin immediately). The 8X300 device then carries out the DMA transfer using BUS ADDRESS and ASTB-0, etc. An example of a typical DMA Read operation is a transfer of motion commands from the 64-byte circular queue (RAM) to the Vector Generator. The only time a DMA Write occurs is when the Vector Generator informs the 6800 system of the new pen position after an operator-controlled joystick movement. In this case, the Vector Generator writes into the 6800's system RAM.

At **4**, the DMA transfer is complete and BRQ-0 is released along with ASTB-0. Releasing BRQ-0 clears the Bus Request Poll Counter to 0 and allows the counter to start again. The main Processor then takes control of the bus again for at least one transaction during Phase 2.

I/O Addressing

The I/O area addressed by IOADD-1 is a 2K-byte block of addresses assigned to I/O devices (functional block modules, etc.). Table 3-1 gives the addresses for these I/O block assignments.

Table 3-1

I/O BLOCK ASSIGNMENTS (F7FF TO FFFF)

I/O Block	Address	Function
0	FFE0-FFFF	Processor Hardware Vector
1	FFC0-FFDF	Processor Enhancements
2	FFA3	Parameter Entry Switch/LED Data
	FFA2	Parameter Entry Interrupt Flags
	FFA1	Self Interrupt, Bus Error Flag
	FFA0	Interrupt Mask, DMA Enable
3	NOT USED	
4	FF63	GPIB Mode/Command Register
	FF62	GPIB Input/Output Data
	FF61	GPIB Status Register
	FF60	GPIB Handshake Register
5	FF43	Serial I/O Status/Control Register
	FF42	Serial I/O Baud Rate
	FF41	Serial I/O Tx/Rx Data
	FF40	Serial I/0 Comm Link/ACIA Status
6	NOT USED	
7	NOT USED	
8	FDF2	Vector Generator Dispatch Table Pointer
	FDF1	Vector Generator Interrupt Flags
	FDF0	Vector Generator Control Register
	FDE3	Front Panel Bell Register
	FDE2	Front Panel Light Data
	FDE1	Front Panel Switch Data
	FDE0	Front Panel Interrupt Flags & Control

THE PROCESSING OF COMMANDS

The processing sequence for host-generated or switch-activated commands corresponds to the processing sequence for one of the following general groupings. Understand that the system firmware controls the exact process for each separate command or activated switch, but these groupings give a general idea of how the 4663 Plotter processes the command.

Commands and their arguments are first converted into data bytes which are routed throughout the Plotter following one of the internal communications protocol methods just described. Refer to Figure 3-1 for a diagram of the Plotter's functional block structure while reading the following command routing descriptions.

Host commands, when received by the active interface, are decoded by the Command Decoder in the Communications Interface and an interrupt is sent to the Processor. The Processor then routes the decoded command to the appropriate Plotter functional block.

The general command processing groups are as follows:

- Host-Generated Commands
  - Pen Movement Commands
  - Interface Commands
  - Transform-Modifying Commands
  - Response-Invoking Commands
- Front Panel Switch Commands

Host-Generated Commands

There are four basic types of commands issued from the Plotter's host system: Pen Movement Commands, Interface Commands, Transform-Modifying Commands, and Response-Invoking Commands. These commands are discussed on the following pages.

Pen Movement Commands

The Plotter's host system issues commands to direct pen movement and drawing. These commands are called Pen Movement Commands. These commands are modified by any existing transforms stored in RAM. Once again, the system firmware controls this modification. The 64-byte circular queue in RAM then stores the modified commands. The 8X300 processor, which can also access the circular queue (by DMA), reads the information and uses it to generate signals to the Motor Pen Drive. The Motor Pen Drive circuit card amplifies these signals to the three pen carriage motors (two X-axis and one Y-axis) and the active pen solenoid (which raises or lowers the active pen). Examples of host-generated pen movement commands are listed here:

Move to Load Point
Move
Draw
Outline Viewport
Mark Viewport
Axis
Print Character
Character Move
Move to Home
Draw Arc
Draw Circle
Expand Macro
Print-Centered Character

Interface Commands

Once decoded by the Command Decoder, these commands modify the logic of the active communications interface module. Typical host-generated interface commands are the following:

Device On
Device Off
Block Start
Set Turnaround Delay
Block End
Set Block Size
Set Bypass Cancel Character
Set Signature Character
Set Prompt String
Interface Parameter Reset
Data Reset
Select Command/Response Format

Transform-Modifying Commands

These commands set the parameters for drawing alpha or graphic plots. Like the commands described earlier, these commands are first decoded and then are used to modify applicable existing RAM-stored transforms (i.e., alpha parameter modifications alter the RAM-stored alpha transform, while graphic parameter modifications alter the RAM-stored graphic transform). The Plotter executes all subsequent Move, Draw, or Print commands after they are modified by the applicable transform. Examples of host-generated transform-modifying commands are as follows:

Graphic Transform-Modifying Commands	Alpha Transform-Modifying Commands
Select Graphic Units	Set Alpha Size
Select Device Units	Set Alpha Ratio
Select Line Type	Set Alpha Dimension
Set Dash Patterns	Set Alpha Rotation
Set Dash Pattern Length	Set Alpha Slant
Select Coordinate Type	Set Alpha Scale
Set Origin to Current Position	Set Tab Separation
Set Rotation to Last Angle	Set Alpha Margin Separation
Set Scale	Set Alpha Spacing Control
Set Translation	Select Standard Alpha Font
Set Skew	Select Alternate Alpha Font
Set Rotation	Reset Alpha Parameters
Set Window	Set Downloaded Character Size
Set Viewport	Begin Character Definition
Select Clipping Control	Set Character X-Extent
Set Arc Smoothness	Specify Non-Advancing Character
Begin Macro Definition	End Character Definition
End Macro Definition	Delete Character Definition
Delete Macro	Delete Font Definition
Set Auto Macro	

Response-Invoking Commands

These commands, once decoded by the Command Decoder, cause the Plotter to perform some action (other than a pen movement) or to output a response through the active communications interface. The Read, Identify, or Digitizing commands cause the Processor to read a selected system RAM location and transfer this information back to the active communications interface for proper output formatting to the host. Action commands cause the Processor (under system firmware control) to transfer the decoded command to the applicable module(s), where the command is used to generate an action. Typical response-invoking commands are the following:

Device Reset	Restore Previous Transform
Read Status	Read Formlength
Read Error	Advance Media
Identify	Read Macro Status
Read Viewport	Page Change
Select Pen	Digitize
Save Current Transform	Operator Digitize

Front Panel Switch Commands

In addition to commands generated by the host system, the Plotter receives commands that are activated by the front panel switches. All front panel commands (other than Parameter Entry commands) are routed through the Vector Generator module. These commands then act in the same manner as the decoded host-generated commands described previously. For example, front panel pen movement functions, such as LOCATE PAGE/VIEWPORT, OUTLINE/MARK VIEWPORT, or joystick movements, use the same process as decoded host-generated pen movement commands. Also, action or response functions, such as MANUAL MOTION, MEDIA CHANGE, INIT, ERROR RESET, LAST POINT, DRAW POINT or MOVE POINT, use the same process as decoded host-generated response-invoking commands; front panel transform-modifying commands, such as SET PAGE/VIEWPORT, use the same process as decoded host-generated transform-modifying commands. The POWER, INTERFACE, and PEN CONTROL switches/adjustments simply reconfigure the Plotter's hardwiring of the applicable module (i.e., POWER reconfigures the hardwiring of the Power Supply; INTERFACE switches alter the logic of the active interface module; and the PEN CONTROL switches/adjustment alter the logic in the Vector Generator module).

CIRCUIT DESCRIPTIONS

Introduction

This section and Section 4 contain detailed descriptions of the Plotter's electrical operation. As mentioned earlier, the Plotter is composed of the functional blocks shown in Figure 3-1. Each functional block is described in detail. In some cases, a functional block is further broken down in a block diagram showing all of the important electronic components. Keep in mind that most internal communications use one of these three methods: a Processor Read or Write (where the Processor is interrupted), or a DMA character transfer.

The following circuit descriptions are based on the schematics in Volume 2. The more complex schematics are further divided in the same manner as the block diagrams.

For additional information, the reader may wish to refer to the component location photographs (also in the Volume 2 schematics) and the signal descriptions in Appendix A of this volume.

Processor and Memory

Figure 3-7 is a block diagram of the Processor and Memory circuit card. It shows the major circuit blocks and the connecting signal lines to the bus, Parameter Entry, and ROM Patch "B" functional blocks.

This circuit card description is divided into two basic functional blocks: Processor and Memory. Each is described separately.

Processor Functional Block

The Processor is composed of the following functional sections:

- Bus Buffers and Transceivers
- Timing and Processor/Bus Handshake
- IRQ Vectoring
- DMA Bus Control
- Miscellaneous Interface/Parameter Entry I/O

NOTE

The following description, except for the Timing and Processor/Bus Handshake information, covers all versions of the Processor used in the Plotter. Early Processors operated with a seven-clock cycle Phase 1 (0.4747 μs) and an eight-clock cycle Phase 2 (0.5425 μs). The timing for both Processors is covered separately in the Timing and Processor/Bus Handshake circuits.

6800 Processor. The 6800 microprocessor (hereafter called the Processor) controls the transfer of data and commands between the other Plotter functional modules. The Plotter can be described as an interrupt-driven device. This means that whenever a functional block receives, generates, or passes a command, the block first sends an interrupt to the Processor. The Processor uses this interrupt request to identify the interrupting module and to access instructions from the system firmware stored in ROM. These instructions then guide the Processor in transferring or modifying the command. The functional blocks receiving this command data then take the required action.

The Processor requires two non-overlapping clock signals (Phase 1 and Phase 2) from the Timing and Processor/Bus Handshake circuit (described later) and a RST-0 signal from the Power Supply. RST-0 causes the Processor to begin operation by jumping to the restart instruction address in the system firmware. Although the Processor has two interrupt lines (IRQ and NMI), only IRQ is used. All interrupts from the Plotter's functional modules are routed through the IRQ Vectoring section.

VMA (Valid Memory Address) indicates that there is a valid address on the address lines, and is used to generate ADDRESS STROBE (ASTB-0).

The Processor's R/W (Read/Write) signal line is referred to as the WRITE-0 line (or W-0/1). This line indicates whether the Processor is in a read or receiving state (when high) or a write or transmitting state (when low). Since this line is buffered with a tri-state buffer, the Vector Generator DMA Control can also use this line during Phase 1 DMA operations. WRITE-0 is also buffered and becomes MEMORY WRITE-0 (MW-0) to the Memory functional block.

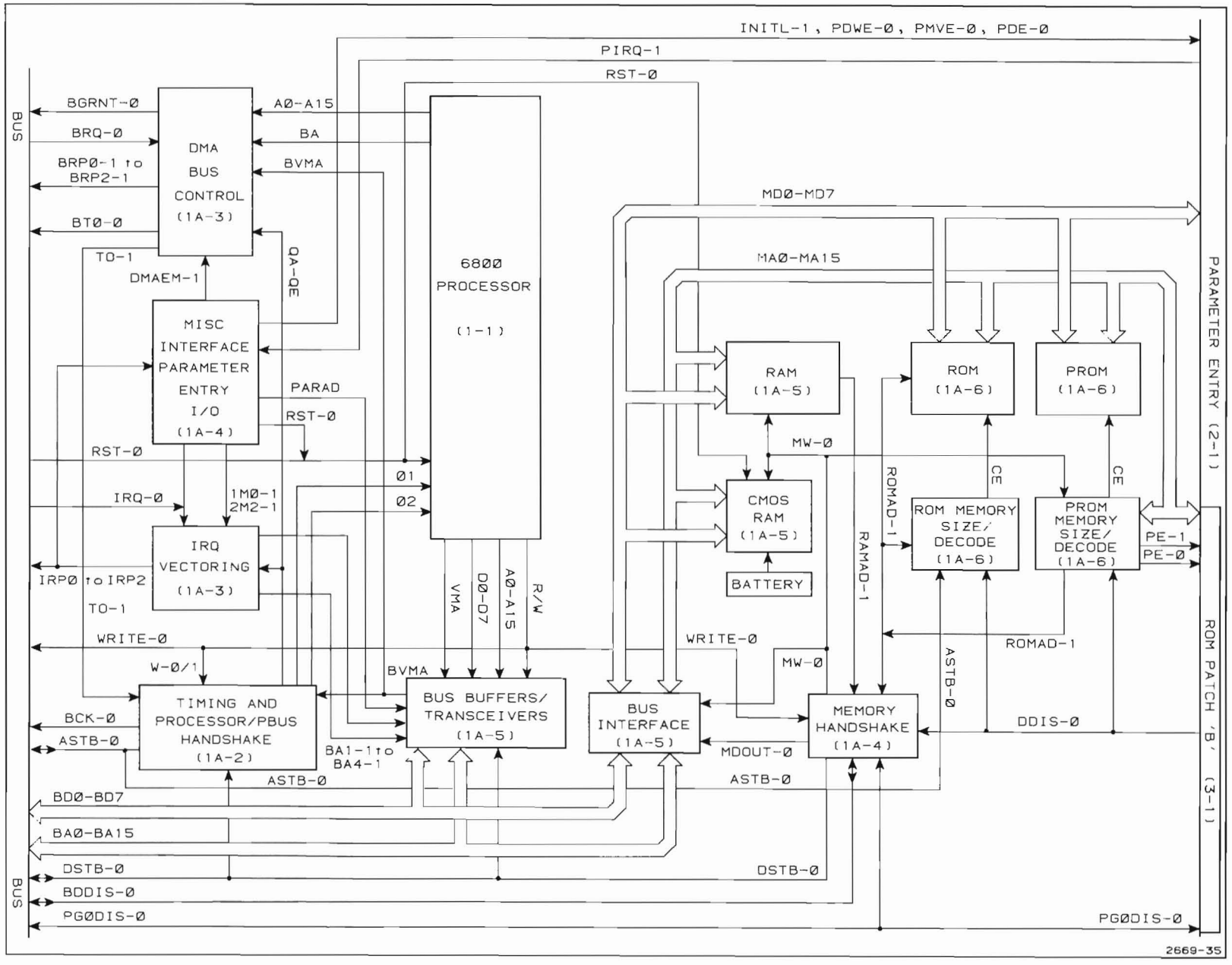

Figure 3-7. Processor/Memory Functional Block Diagram.

Bus Buffers And Transceivers. Tri-state transceivers buffer the address lines (BA0 through BA15) and data lines (BD0 through BD7).

The address lines are used by the Processor (or the Vector Generator DMA Control) to select specific memory locations within the Plotter for read, write, or DMA operations.

The data lines carry bytes of data between the various functional modules addressed by the address lines.

Timing and Processor/Bus Handshake. The Processor Clock, which is an LC crystal, operates at 14.7456 MHz and provides both CK-0 and CK-1 to the Processor circuit card for basic synchronization. CK-0 is also used to produce the Phase 1 and 2 timing signals to the 6800 microprocessor. The Processor Clock also provides the overall system timing signal (BCK-0) for all functional module timing (including the Interface baud rate generator and bus signal synchronization). All bus signals, except BUS REQUEST (BRQ-0), INTERRUPT REQUEST (IRQ-0), and BUS DATA DISABLE (BDDIS-0) begin on the falling edge of BCK-1.

Refer to the Processor Schematic 1A-2 when reading the following description. System timing is generated using a series of four shift registers connected as a Johnson Counter. When power is first applied, the individual register outputs of the Johnson Counter are random. However, the COUNTER CLEAR from Pin 8 of the Read/Wait Gate provides a means to automatically clear the counter.

The first register (QA) is the key element in the register clearing process. If QA's Q-NOT (Pin 3 or QA-0) is initially a TTL high, a COUNTER CLEAR TTL low will be fed back into the first register (Pin 4). This will set the outputs QA-1 through QD-1 to TTL lows or the outputs QA-0 through QD-0 to TTL highs in four clock cycles. On the other hand, if QA-0 initially started as a TTL low, the COUNTER CLEAR sets a TTL high back into the first register (Pin 4). Normally, this reset action also takes four clock cycles to set QA-1 through QD-1 to TTL highs. But the circuit permits only QA-1 through QC-1 to be reset in three clock cycles. Therefore, in either case, the registers are reset to either all lows in four clock cycles or all highs in three clock cycles.

After the initial resetting process, the Processor Clock proceeds to change the outputs of the registers sequentially; that is, one register for each bus clock cycle. If QA-1 through QD-1 had been reset low, each successive counter stage is changed to a TTL high with each clock cycle. When the third clock cycle changes the output of the forth register (QD-1) from a low to a high, COUNTER CLEAR starts changing each successive register output to a high (for QA-0 through QD-0) or to a low (for QA-1 through QD-1). Once again, each successive register is changed with each clock cycle. After four clock cycles (clock period eight), all outputs (QA-0 through QD-0) are TTL highs, and the COUNTER CLEAR input to the first register changes to a TTL high, which starts the whole process over. On the other hand, if the registers had been initially reset to TTL highs, the first register would change to a TTL low and the entire cycle would be reversed; that is, QA-1 through QD-1 would be set low for four cycles, then high for four cycles.

The period during which a TTL high COUNTER CLEAR is input to the Johnson Counter, is defined as Phase 1. During Phase 1, the 6800 Processor is inactive, allowing the 8X300 microprocessor to conduct DMA activity. The period during which a TTL low COUNTER CLEAR is input to the Johnson Counter, is defined as the Phase 2 time. This is the period in which the main Processor is active on the bus. See Figure 3-8A.

Phase 1 and Phase 2 Stretch. The four-clock cycle Phase 1 and the four-clock cycle Phase 2, which together total 0.47472 μs, are the default Processor synchronization times. However, some functional modules may require a longer time in order to complete a transaction. The Timing and Processor/Bus Handshake section can lengthen (stretch) either of the two Processor phase times to accommodate any slower modules on the bus. DMA activity can stretch Phase 1 up to 3.8 μs, and the Processor bus handshaking can also stretch Phase 2 up to 3.8 μs.

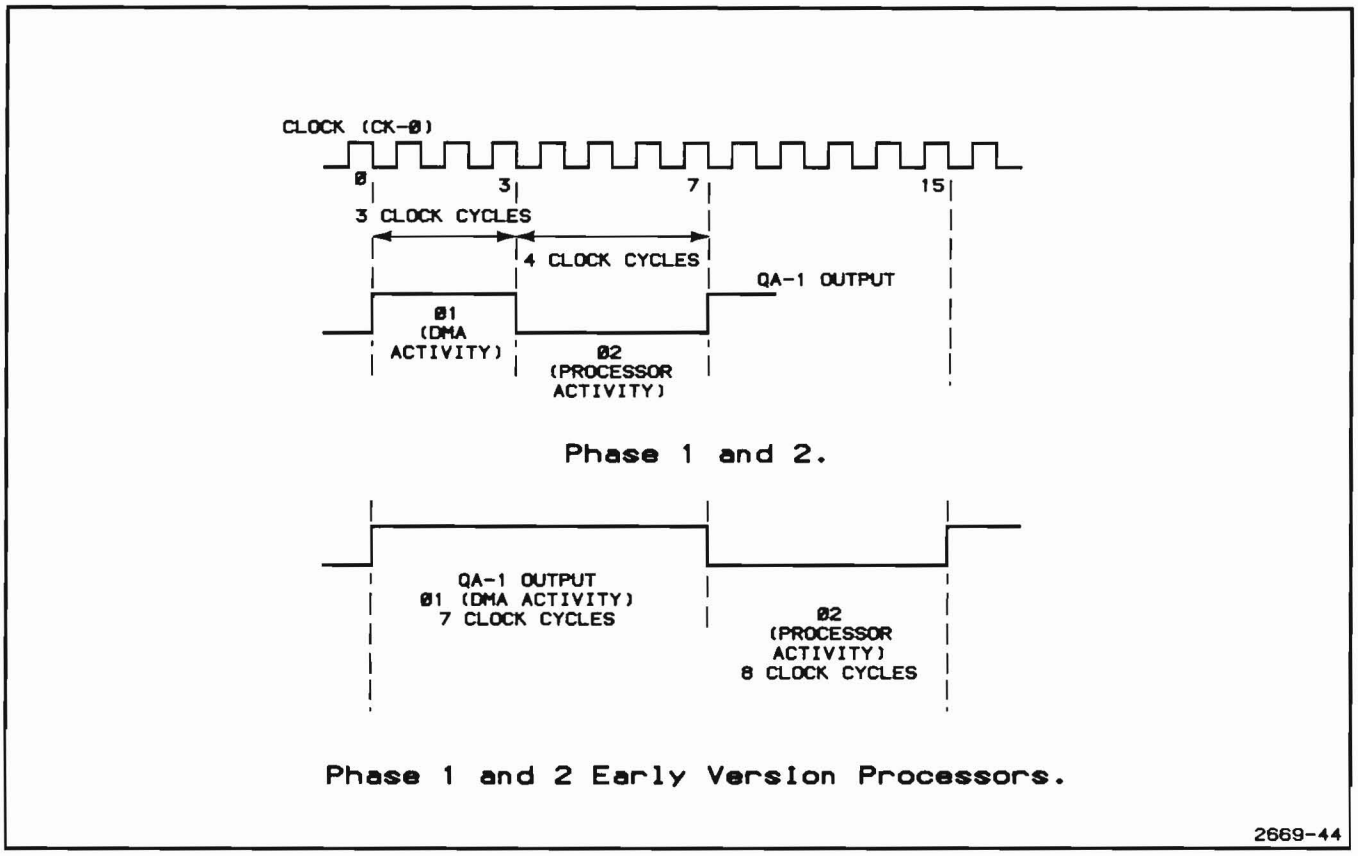

Figure 3-8. Phase 1 and Phase 2 Clock.

The Phase 1 stretch process is described under the DMA Bus Control section (described later).

DSTB-0 is the key handshake signal affecting the length of the Phase 2 time. Normally, when the Processor is writing, it initiates DSTB-0 for one BUS CLOCK cycle after placing valid data on the Bus Data lines. The memory device being written to then asserts and holds DSTB-0 for as long as it needs to process the data (up to 3.8 μs). While the device being written to is asserting DSTB-0, the Processor cannot release VMA (valid memory address, via BVMA-1, which generates ASTB-0) and WRITE-0. While a signal is being asserted on these two lines (and DSTB-0), the Johnson Counter is prevented from switching to the Phase 1 cycle (at least until the 3.8 μs timer, described later, forces the next Processor cycle).

On the other hand, if the Processor is reading, the WRITE-0 signal at the Read/Wait gate controls the length of Phase 2. One of its inputs is WRITE-0 (if high indicates a Read) from the Processor. As long as the Processor is reading, Phase 2 is stretched. This means that whenever the device being read does not provide data before at least two bus clock cycles prior to the end of Phase 2, the length of Phase 2 is stretched.

Timing and Processor/Bus Handshake (Early Versions — 670-5121-00, 01, and 02 circuit boards). The Processor Clock, which is an LC crystal, operates at 14.7456 MHz and provides both CK-0 and CK-1 to the Timing and Processor/Bus Handshake section (this section). These signals are then used to produce the Phase 1 and 2 timing signals to the 6800 microprocessor. The Processor Clock also provides the overall Plotter system timing signal, which is used for all functional module timing (including the Interface baud rate generator) and bus signal synchronization (BCK-1). All bus signals, except BUS REQUEST (BRQ-0), INTERRUPT REQUEST (IRQ-0), and BUS DATA DISABLE (BDDIS-0) begin on the falling edge of BCK-1.

Refer to Schematic 1-2 when reading the following description. System timing is generated using a series of eight shift registers (rather than four, as in new versions) connected as a Johnson Counter. The output of the Johnson Counter is sent to U921, an 8-input NAND gate. When power is first applied, the individual register outputs of the Johnson Counter are random. However, the COUNTER CLEAR from Pin 8 of the Read/Wait Gate provides a means to clear the counter automatically.

As in late model Plotters, the first register of the Johnson Counter is the key element in the register clearing process. If QA's Q-NOT (Pin 3 or QA-0) is initially a TTL high, a TTL low COUNTER CLEAR is fed back into the first register (Pin 4). This sets the QA-1 through QH-1 outputs to TTL lows (or the QA-0 through QH-0 outputs to TTL highs) in eight clock cycles. On the other hand, if QA-0 initially started as a TTL low, the COUNTER CLEAR sets a TTL high back into the first register (Pin 4). Normally, this reset action also takes eight clock cycles to set QA-1 through QH-1 to all TTL highs. But, the circuit permits only QA-1 through QG-1 to be reset in seven clock cycles. In either case, the registers are reset either all lows in eight clock cycles or all highs in seven clock cycles.

After the initial resetting process, the Processor Clock changes each register's output sequentially on each bus clock cycle. If QA-1 through QH-1 had been reset low, each successive counter stage is changed to a TTL high with each clock cycle. When the seventh clock cycle changes the output of the seventh register (QG-1) from a low to a high, COUNTER CLEAR starts changing each successive register's output to high (for QA-0 through QH-0) or to a low (for QA-1 through QH-1). Once again, each successive register changes with each clock cycle. After eight clock cycles (clock period 15), all outputs (QA-0 through QH-0) will be TTL highs, and the input (COUNTER CLEAR) to the first register will be changed to a TTL high, which starts the whole process over. However, if the registers had been initially reset to TTL highs, the first register would be a TTL low and the entire cycle would be reversed; that is, the eight-clock cycle period would occur first and then the seven-clock cycle period.

The seven-clock cycle period, during which a TTL high COUNTER CLEAR is input to the Johnson Counter, is defined as Phase 1. During Phase 1, the 6800 Processor is inactive, allowing the 8X300 microprocessor to conduct DMA activity. The eight-clock cycle period, during which a TTL low feedback is input to the Johnson Counter, is defined as the Phase 2 time. This is the period in which the 6800 Processor is active on the bus. See Figure 3-8B.

Phase 1 And Phase 2 Stretch. The seven-clock cycle Phase 1 and the eight-clock cycle Phase 2, which together total 1.017 μs, are the default Processor synchronization times. However, some functional blocks may require a longer time in order to complete a transaction. The Timing and Processor Bus Handshake section can lengthen (stretch) either of the two Processor phase times to accommodate any slower modules on the bus. DMA activity can stretch Phase 1 up to 3.8 μs, and the Processor bus handshaking can also stretch Phase 2 up to 3.8 μs.

The Phase 1 stretch process is described under the DMA Bus Control section (described later).

DSTB-0 is the key handshake signal affecting the length of the Phase 2 time. Normally, when the Processor is writing, it initiates DSTB-0 for one bus clock cycle after placing valid data on the Bus Data lines. The memory device being written to then asserts and holds DSTB-0 for as long as it needs to process the data (up to 3.8 μs). While the device being written to is asserting DSTB-0, the Processor can not release BVMA (valid memory address, which generates ASTB-0) and WRITE-0. While a signal is being asserted on these two lines (and DSTB-0), the Johnson Counter is prevented from switching to the Phase 1 cycle (at least until the 3.8 μs timer, described later, forces the next Processor cycle).

On the other hand, if the Processor is reading, the WRITE-0 signal at the Read/Wait Gate will control the length of Phase 2. One of its inputs is WRITE-0 (if high indicates a Read) from the Processor. As long as the Processor is reading, Phase 2 is stretched. Whenever the device being read does not provide data before at least two bus clock cycles prior to the end of Phase 2, the length of Phase 2 is stretched.

IRQ Vectoring. The IRQ (Interrupt Request) Vectoring circuit prioritizes interrupts from the Plotter's functional modules to the Processor. Examples of these interrupts include requests for the Processor to transfer data between the various internal Plotter functional modules. The prioritizing of interrupts ensures that important tasks get done first. To accomplish this end, each functional block is factory-assigned a priority level (see Appendix E of Volume 2). Normally, all interrupts are serviced as soon as the Processor can finish its present task, unless two or more requests are pending simultaneously. In this case, the one with the highest priority is serviced first.

Refer to Schematic 1A-1 when reading the following description. The Plotter uses eight levels of interrupts. The Interrupt Poll Counter, a 4-bit binary poll counter operating at one-half the bus clock frequency, provides the priority count ranging from 0 to 7. Zero is assigned the highest priority. The counter's three high-order bits become signal lines IRPO-0 through IRP2-1 and go to each interrupt source on the bus. Each interrupting block examines this count through its hardware decoder. If a functional block wishes to issue an interrupt (for example, requesting the Processor to transfer some data to another block), the module asserts IRQ-0 to the Processor at the time it decodes its assigned priority count.

Unlike the DMA Poll Counter (described later), the Interrupt Poll Counter does not stop and wait for the Processor to act. Instead, IRQ-0 is output to the Processor (starting its interrupt routine after completing its present task), and the counter continues to poll for a higher priority level interrupt. This means that the poll continues, ranging from 0 to the level of the pending interrupt. All lower priority counts are eliminated. This new lower level limit count is stored in the Low Level Limit Storage Register. When the Processor reaches the vectoring stage of its interrupt cycle, the current lower limit is used to locate the highest priority interrupt vector. This vector identifies the interrupting module and points to the location of the interrupt service routine (instructions stored in ROM). The new lower limit may be subsequently increased if a higher priority level interrupt request comes along before the Processor vectoring occurs.

Interrupt levels may be masked or unmasked by the Processor by writing and reading the Interrupt Mask Register. This register establishes a secondary lower limit on the poll using the IMO-1 through IM2-1 signal lines.

Interrupt Service Routine Locations. When the Processor starts its interrupt service routine, it loads two address bytes, FFF8 and FFF9 from the internal M6800 hardware assignments for IRQ vectors, on the Address Bus. The low order three bits are dropped and the contents of the Lower Limit Poll Counter are used instead. To do this, the I/O Address Space Decoder (on Schematic 1A-1) first decodes FFF8 and FFF9 and then disables (using LADEN-1) the BA1 through BA4 output tri-state buffer (U791 on Schematic 1A-1). This drops these four low order bits. At the same time, the Lower Limit Poll Counter is enabled and transfers the contents of the Low Limit Storage Register onto the Address Bus. This address is then used by ROM to specifically instruct the Processor in the applicable interrupt service routines. The resulting addresses of the interrupt routines are shown in Table 3-2.

Table 3-2

ROM 0 INTERRUPT SERVICE ROUTINE LOCATIONS

Address	Interrupt Routines
F7FF F7FE	Restart Vector
F7FD F7FC	Non-Maskable Interrupt Vector (not used)
F7FB F7FA	Software Interrupt Vector (not used)
F7F9 F7F8	Self Interrupt Vector (used by system firmware)
F7F7 F7F6	Hardware Interrupt Vector Level 7 (lowest priority)
F7F5 F7F4	Hardware Interrupt Vector Level 6
F7F3 F7F2	Hardware Interrupt Vector Level 5
F7F1 F7F0	Hardware Interrupt Vector Level 4
F7EF F7EE	Hardware Interrupt Vector Level 3
F7ED F7EC	Hardware Interrupt Vector Level 2
F7EB F7EA	Hardware Interrupt Vector Level 1
F7E9 F7E8	Hardware Interrupt Vector Level 0 (highest priority)

DMA Bus Control. The DMA Bus Control circuit controls the Plotter's DMA activity when transferring data from the system RAM's circular queue to the Vector Generator. Although the Plotter's circuitry is designed for up to eight levels of DMA, only Vector Generator DMA is used. The DMA Poll Counter is a 4-bit binary poll counter and operates at one-half the bus clock frequency. Its outputs are BRP0-1 through BRP2-1. The binary count on these lines ranges from zero to seven (0-7). Zero is the highest priority.

However, priority one is the level assigned to the Vector Generator. To either read the circular queue or update the Processor with a new pen position after a joystick movement, the Vector Generator asserts BUS REQUEST (BRQ-0) at the time it decodes a one (priority level) from the DMA Poll Counter. BRQ-0 also stops the DMA Poll Counter at the count of one. The DMA Poll Counter remains stopped as long as BRQ-0 is asserted. Then, during the next Processor's Phase 1 clock cycle (the Processor's dormant period), the Processor's DMA Bus Control issues BUS GRANT (BGRNT-0) on the first falling edge of the bus clock. BGRNT-0 informs the Vector Generator's DMA Control that the bus is available for a one-character DMA transfer. The Vector Generator issues a Read or Write signal (WRITE-0), an address, and ASTB-0 to the Processor's DMA Bus Control and normal bus handshaking takes place between the two DMA Controls (as shown in Figure 3-7). The Vector Generator's DMA Control can then either read the circular queue or write into another area in RAM. At the end of the DMA transaction, BRQ-0 and ASTB-0 are released, clearing the DMA Poll Counter to zero. The DMA Poll Counter then begins to count from zero to seven again until the Vector Generator issues its next request.

Bus Transaction Timer. The DMA Bus Control circuitry also contains a 3.8 μs bus transaction timer. This timer limits all bus transactions (whether DMA or Processor Read or Write) to a maximum time of 3.8 μs. All transactions taking longer than this must terminate on the next falling edge of BCK-1. The timer is triggered by the start of each Phase 1 or Phase 2. If a DMA transaction takes place one clock cycle after the start of Phase 1 and takes longer than approximately 0.20 μs (the normal length of Phase 1) but less than 3.8 μs, the presence of BGRNT-0 (using GRNT-1) prevents the QC-1 (Johnson Counter) from producing a Read/Wait Gate output, which starts Phase 2. Normally, when a DMA transaction is complete, GRNT-1 ends and the Read/Wait Gate starts the Phase 2 cycle. However, if a DMA transaction takes longer than 3.8 μs, the timer times out, producing TIMEOUT-1 (TO-1), and ends GRNT-1 one clock cycle later. Either of these two signal conditions enables the start of Phase 2. When the timer times out, BUS TIMEOUT (BTO-0) is asserted to signal the Vector Generator that the DMA transaction must be completed in the next bus clock cycle or it will be forced off the bus and Phase 2 will begin.

In a similar manner, the Processor's Read/Write signal line (W-0 and W-1) prevents the Johnson Counter from starting a new Phase 1 while the Processor is conducting a Phase 2 transaction which requires more than 0.27 μs (the length of phase 2). But, if the Processor requires more than 3.8 μs, the timer will timeout, producing TO-1. TO-1 essentially forces the Processor off the bus and ends Phase 2 one bus clock cycle later.

Miscellaneous Interface/Parameter Entry I/O. The Miscellaneous Interface/Parameter Entry I/O circuitry on Schematic 1A-4 contains an 8 millisecond timer, Processor Interrupt Poll Select circuitry, and the Processor's General Purpose (GP) I/O registers. These circuits are discussed in the following paragraphs.

Eight Millisecond Timer. The eight millisecond timer provides timing for system firmware task management.

Processor Interrupt Poll Select. The Processor Interrupt Poll Select circuitry selects the particular interrupt level for the three possible interrupt requests to the IRQ Vectoring. The three strapable interrupt requests indicate a change in: a parameter entry status, the eight millisecond timer, or a bus error. The Processor Interrupt Poll Select selects the input corresponding to the binary value of the interrupt poll lines (IRP0-1 through IRP2-1) and presents that interrupt request as IRQ-0.

Processor General Purpose (GP) I/O Circuitry. The Processor's GP I/O circuitry consists of two registers in the Miscellaneous Interface/Parameter Entry I/O circuitry and two registers physically located on the Parameter Entry circuit card. The Processor GP I/O circuitry interfaces the Parameter Entry functional block through J4 to the Processor. This provides an I/O port for either the Firmware Patch circuit card or the Diagnostics Test Fixture circuit card (used in troubleshooting). The four registers are addressed from FFA0 to FFBF.

FFA0 The FFA0 Register stores the interrupt masks, DMA ENABLE, Parameter INIT LED, the Parameter Entry enables, and the eight millisecond timer interrupt flag and enables. The individual bit assignments for this register are as follows:

Bit 7 (MD7) — A logical 1 indicates that the eight millisecond timer requested an interrupt. This interrupt is strapped at level 5 (J101/J102).

Bit 6 (MD6) — A logical 1 enables the timer interrupt.

Bit 5 (MD5) — A logical 1 enables the Parameter Entry functional block to generate interrupts for any switch depressions or Parameter Entry card movement (strapped at level 4 on J101/J102).

Bit 4 (MD4) — A logical 1 lights the Parameter Entry INIT LED.

Bit 3 (MD3) — A logical 1 enables DMA activity for levels 1-7.

Bits 0-2 (MD0-MD2) — These three bits reflect the binary count of the lower limit of the interrupt polling. Active levels are true (1). Bit 0 is represented by IM0. If Bits 0-2 are all low, interrupt polling extends to level seven (the lowest priority). A 101 output limits the interrupt polling to levels 0-3. This means that functional blocks strapped for levels 4 through 7 are not polled.

FFA1 The FFA1 Register contains the flag bits for Bus Error, Self-Interrupt, and System RST-0. The bit assignments for this register are as follows:

Bit 7 (MD7) — A logical 1 indicates that a bus error condition requested an interrupt. Strapped for level 0, the interrupt is cleared when the Processor reads this register. This bit is a read-only bit.

Bit 6 (MD6) — Bit 6 is not used.

Bit 5 (MD5) — Bit 5 is not used.

Bit 4 (MD4) — Bit 4 is not assigned, but is tied to a logic 0 (GND). This bit is a read-only bit.

Bits 0-3 (MD0 through MD3) are not used.

The two remaining registers, FFA2 and FFA3, are physically located on the Parameter Entry circuit card. Refer to Schematic 2-1 for this portion of the Miscellaneous Interface/Parameter Entry I/O.

FFA2 The FFA2 Register is a read-only register which stores Parameter Entry interrupts and status bits. The bit assignments of this register are as follows:

Bit 7 (MD7) — A logical 1 indicates that either a Parameter Entry switch was pressed or the card requesting an interrupt was moved. The interrupt level is strapped to level 4.

Bit 6 (MD6) — A logical 1 indicates that the Parameter Entry card caused an interrupt request. The bit, if set, is cleared after the Processor has read this register.

Bit 5 (MD5) — A logical 1 indicates that the Parameter Entry card was moved while a Parameter device interrupt (generated by previous card movement) was still pending. This bit is intended to flag an overrun which indicates a positional loss of the card-line-pointer. The bit is cleared when the Parameter Entry card is returned to its "home" (fully inserted) position. An overrun state inhibits any further interrupts caused by Parameter Entry card movement.

Bit 4 (MD4) — Bit 4 indicates the direction of the Parameter Entry card movement which generated an interrupt request. A logical 0 indicates that the card has been withdrawn, while a logical 1 indicates that the card has been moved in.

Bits 0-3 (MD0 through MD3) are not used.

FFA3 The FFA3 Register allows the Processor to light the Parameter Entry switch status LEDs and to interrogate the input Parameter Entry switches. This register add uses two other registers, the Parameter Entry LED Register and the Parameter Entry Switch Register. The Processor writes data to the LED Register and reads data from the Switch Register in complementary form. When either a switch is depressed or a LED is illuminated a logical 0 is used. After a Parameter Entry switch is pressed, a 25-millisecond "debounce" circuit delays the issue of an interrupt request (IRQ-0) to the Processor.

The left most switch/LED combination (viewing the Parameter Entry device from the front) is Bit 7 (MD7), while the right most switch/LED combination is Bit 0 (MD0).

Memory Functional Block

The Processor's memory consists of RAM and EPROM (PROM)/ROM. Different parts of this memory are used for different purposes. Figure 3-9 shows the memory allocations for 65,536 address spaces which are located mostly on the Processor circuit card. However, some Plotters use a ROM Overlay circuit card which contains some or all of the Processor's firmware memory in the form of PROMs. Other portions of the memory consist of Interface ROMs, located on the interface circuit cards, and the Firmware Patch, which is an electrical extension of the Processor circuit card that contains the "fix-it ROM." Refer to Figure 3-7 for a diagram of the Memory functional block. The Memory functional block consists of the following functional circuits:

Bus Interface
RAM
CMOS RAM
ROM
Memory Handshake
PROM
ROM Memory Size Decode
PROM Memory Size Decode

The Firmware Patch is also described here even though it is physically part of the Parameter Entry.

Bus Interface. The Bus Interface circuit (shown in Schematic 1A-5) consists of two tri-state transceivers for the data lines D0 through D7 and two buffers for the address lines A0 through A15. When WRITE-0 (via MW-0) is asserted, data is allowed to transfer from the bus to the memory. On the other hand, when WRITE-0 is not asserted, the transaction is from the memory to the bus (a Read transaction). Address and Data lines between the memory and the Bus Interface are referred to as MA0 through MA15 (Memory Address) and MD0 through MD7 (Memory Data). If DDIS-0 is asserted by the Firmware Patch, MDOUT-1 prevents data from being transferred from the memory to the bus. This is how the Firmware Patch disables the Memory block and transfers data from the patch FPLA to the Processor.

RAM. The system RAM (shown in Schematic 1A-5) stores incoming interface commands, downloaded characters, transforms, macros, and motion commands to the Vector Generator, and provides a workspace for the Processor. The 64-byte space reserved to store motion commands to the Vector Generator is referred to as the circular queue. The standard RAM configuration is 8K-bytes. The address of the RAM storage starts at location 0000 (see Figure 3-9) and proceeds to 1FFF. The RAM Address Decoder decodes the address lines MA10 through MA15 and signal lines from the Memory Handshake section. The RAM consists of 16 (1K x 4-bit) devices.

CMOS RAM. When the Plotter is turned OFF, 128 bytes of CMOS RAM (refer to Schematic 1A-5) are kept electrically energized by a Ni-Cad battery. (Option 36 adds up to an additional 384 bytes of CMOS RAM.) This RAM is used to store all of the current Parameter Entry selection information. When the Plotter is operating, the battery is kept charged and the CMOS RAM memory is powered through diodes CR1 and CR2. However, when the power is turned off, the battery not only keeps the CMOS RAM memory energized but also inhibits the CHIP ENABLE (CE) inputs. Since this 1/2K block of RAM is mapped just below the I/O Address space (refer to Figure 3-9), I/OADD-1 (decoded from bus addresses of F800 or greater) is used along with signals from the Memory Handshake section and the A8 through A10 address lines to form the CMOS RAM CE.

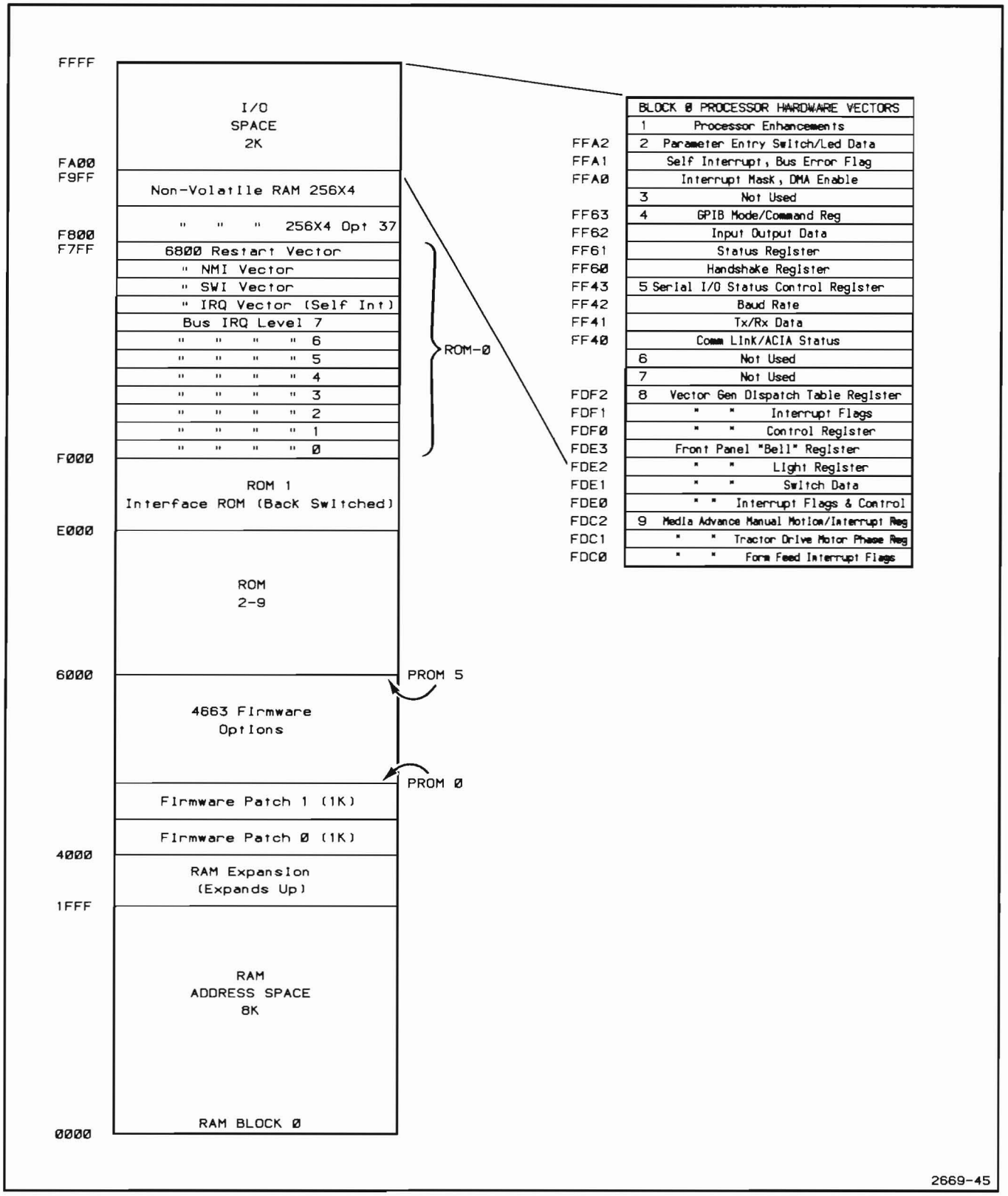

Figure 3-9. Memory Map for the 4663 Plotter.

ROM. The ROM Memory (shown in Schematic 1A-6) is permanent storage for the Processor's operating instructions. The ROM memory for the Plotter consists of approximately 34K bytes; the ROM addresses range from 6000 to F7FF. Most ROM resides on the Processor circuit card. However, approximately 4K of the instructions apply to the Communications Interface and, therefore, are located physically on that circuit card. Another small portion of the ROM is located on the ROM Patch "B" circuit board.

To prevent the firmware for both interfaces from being mapped onto the bus, bank switching is used. This means that only the firmware for the active interface is available to the Processor.

A list of ROMs and their general content is shown in Table 3-3.

Table 3-3

ROM CONTENT

ROM No.	Content
0	Power-up, Monitor, Error Handler, Hardware Interrupt Dispatcher, Self Interrupt Dispatcher
1G	GPIB Interface Functions (Note that this ROM is actually located on the Communications Interface circuit card.)
1R	Serial Interface Function (Note that this ROM is actually located on the Communications Interface circuit card or the Serial Interface Module.)
2	Math Interpreter and Math Functions
3	Buffer Handlers, Device Command Handlers, Utilities, Battery Backup RAM Handlers, Interrupt Select, Parameter Entry Interrupt Handler, Timer Interrupt Handler
4	Transform Command Handlers, Clipping, Page Set-up, Parameter Entry Line Handlers, Units Selection Command Handlers
5	Motion Task Set-up, Motion Command Set-up, Motion Profile Tables, Pen and Line Quality Parameter Entry Line Handlers, Pause, Front Panel Interrupt, Command and Timer Handlers
6	Alpha Command Handlers, Resident Alpha Table
7	Dashed Line Command Handlers, Arc/Circle Command Handlers, Transform Command Handlers, Move to Load Point, Move/Draw Command Handlers, Digitizing, Prompt, Read Viewport/Formlength Command Handlers
8	Common Interface Functions, Common Interface Utilities, Serial Output Functions
9	Self-Test, Carriage Control, Media Advance, Fixed Macro Command Handlers

ROM Overlay Circuit Card EPROMs. Early instruments stored Processor instructions in EPROM instead of ROM. This EPROM was located on a ROM Overlay circuit card, which plugged into the backplane. Later, when ROMs became available, these instructions were stored in ROMs, which were moved to the Processor card (see Tables 3-3 and 3-4). Some instruments may have both EPROMs and ROMs.

Table 3-4

EPROM/ROM COMPARISON

Firmware Partition Number	EPROM (On ROM Overlay Card) Socket Location	Replaced by ROM (on Processor Card)
0	U575 (160-0305-00,01,02...)	U491 (160-0243-00,01,02...)
2(L)	U570 (160-0303-00,01,02...)	U271 (160-0236-00,01,02...)
(H)	U565 (160-0304-00,01,02...)	
3(L)	U560 (160-0301-00,01,02...)	U275 (160-0237-00,01,02...)
(H)	U555 (160-0302-00,01,02...)	
4(L)	U550 (160-0299-00,01,02...)	U281 (160-0238-00,01,02...)
(H)	U545 (160-0300-00,01,02...)	
5(L)	U540 (160-0297-00,01,02...)	U291 (160-0239-00,01,02...)
(H)	U535 (160-0298-00,01,02...)	
6(L)	U470 (160-0295-00,01,02...)	U171 (160-0240-00,01,02...)
(H)	U465 (160-0296-00,01,02...)	
7(L)	U460 (160-0293-00,01,02...)	U175 (160-0241-00,01,02...)
(H)	U455 (160-0294-00,01,02...)	
8(L)	U450 (160-0291-00,01,02...)	U181 (160-0242-00,01,02...)
(H)	U445 (160-0292-00,01,02...)	
9(L)	U440 (160-0289-00,01,02...)	U191 (160-0280-00,01,02...)
(H)	U435 (160-0290-00,01,02...)	

Interface ROMs. Table 3-5 shows the Interface EPROM/ROM on the Communications Interface circuit cards. See Appendix H of Volume 2 for EPROM/ROM locations on the Serial Interface Module circuit card.

Table 3-5

COMMUNICATIONS INTERFACE BOARD EPROM/ROM PLACEMENT

Firmware Partition Number	Socket Location (EPROM)	Socket Location (ROM Replacement)
GPIB	670-5503-00,01,02... card	
1GL	U171 (160-0309-00,01,02...)	U171 (160-0235-00,01,02...)
1GH	U181 (160-0308-00,01,02...)	
RS-232	670-5579-00,01,02... card	
1RL	U171 (160-0306-00,01,02...)	U171 (160-0234-00,01,02...)
1RH	U181 (160-0307-00,01,02...)	

Memory Handshake. The Memory Handshake circuitry (shown in Schematic 1A-4) consists of decode circuits which enable the Processor to access the memory. This circuitry also enables the Processor's DMA Control to access the circular queue in the system RAM for pen drive motor information.

For normal bus transactions (Processor Read and Write), ASTB-0 precedes DSTB-0 by at least one bus clock cycle. The transmitting device then asserts DSTB-0 for one clock cycle, after which the receiving device must assert and hold DSTB-0 to extend the transaction time (see Processor Read/Write description, located earlier in this section). DSTB-0, from the bus, is buffered in the Timing and Processor/Bus Handshake circuit and becomes BDSTB-0 into the Memory Handshake circuit. If the Processor writes to the system RAM, BDSTB-0 is clocked through U611 and back out onto the bus. This fulfills the requirement of the receiving device (the memory in this case) to assert and hold DSTB-0 after receiving that signal from the Processor.

If the memory is transmitting data (during a Processor read, for example), DSTB-0 is asserted for one clock bus cycle in the Timing and Processor Bus Handshake section.

DATA DISABLE (DDIS-0) disables any data output from the ROM memory. If an error in the ROM has been substituted by a "fix-it ROM," DDIS-0 is generated by the ROM Patch "B" circuit. When this circuit decodes the erroneous address, DDIS-0 generates MDOUT-0. MDOUT-0 disables the Bus Interface between that erroneous memory device and the bus. Then, the Firmware Patch asserts on the bus corrected data stored in the Firmware Patch board's PROM. The result is that correct data appears on the bus and the Processor (or any other module on the bus) never knows, that in reality, it came from the Firmware Patch rather than the ROM (PROM) memory.

PROM. The PROM memory (shown in Schematic 1A-6) is used when Plotter options (such as Options 31 and 32) are added. This circuitry accommodates up to 6K of PROM and resides at the memory locations indicated in Figure 3-9). See Appendix H of Volume 2 for a diagram of these PROM locations.

ROM Memory Size Decode. This circuitry (shown in Schematic 1A-6) decodes addresses for the ROM memory block regardless of the individual size of the ROMs used. The size of the individual ROMs used, rather than the total amount of ROM used, determines the strap settings. In other words, the straps (J445 and J455) are set in one position if 2K ROMs are used and in other positions if 4K or 8K ROMs are used. The Plotter normally uses 4K ROMs (except for ROM 0, which is 2K). Refer to Appendix B of Volume 2 for details concerning these straps. Notice that between ROM 0 and ROM 2 (see Figure 3-9), there is a 4K block of ROM labeled "Interface ROM." This is the serial and GPIB Interface module ROM that resides on the Communications Interface circuit card. Since this ROM is not physically located on the Processor circuit card, the ROM Chip Size section ignores the addresses for that I/O Communications ROM as well as all addresses above and below the remainder of the ROM memory space. This means that the ROM Chip Size section responds to addresses F000 through F7FF (for ROM 0) and 6000 through DFFF (for ROM 2 through ROM 9). U451 is a 4-bit full-adder which prevents the memory from handshaking addresses E000 through EFFF. The jumpering for memory size affects the decoding for ROM 2 through ROM 9. It does not affect ROM 0, since ROM 0 is always 2K bytes between F000 and F7FF.

PROM Memory Size Decode. The PROM Memory Size Decode circuitry (shown in Schematic 1A-6) decodes addresses for the PROM memory. The memory is arranged such that the PROM memory addresses are just below that of the ROM (see Figure 3-9). A group of six straps (J13) are weighted in a binary fashion to permit the PROM Memory Size Decoder (a 6-bit full-adder) to identify the PROM's bottom location; therefore, the straps indicate the size of the entire memory less the RAM. The PROM Memory Size Decode responds to addresses 4800 through 5FFF. Refer to Appendix B of Volume 2 for details concerning these straps.

U545 also generates the enables (PE0-0 and PE1-0) to the Firmware Patch (refer to the Firmware Patch description later).

Parameter Entry Functional Block

The Parameter Entry functional block enables the operator to select (or verify) operating configurations of the Plotter. This module, residing on the lower left corner of the front panel, consists of:

- a FFA3 Parameter Entry Switch Register, which is read by the Processor whenever a switch is pressed,
- a write-only FFA3 Parameter Entry LED Register, which drives an LED display (inside each switch) to indicate the current operational parameter status,
- a motion detector for the Parameter Entry card which relates any movement and directional information (this detector is also read by the Procesor using the FFA2 Register), and
- an "overrun" error detector (the INIT LED) which monitors the Parameter Entry card for proper synchronization.

Refer to Schematic 2-1 and Figure 3-9 when reading this description. The eight Parameter Entry switches are debounced by a 25-millisecond one-shot debounce timer. At the end of the debounce period, PARAMETER INTERRUPT REQUEST (PIRQ-1) is asserted to the Processor's IRQ Vectoring circuits. The Miscellaneous Interface/Parameter Entry I/O issues PARAMETER DATA ENABLE (PDE-0) to the FFA3 Parameter Entry Switch Register. PDE-0 enables the Processor to read the content of that switch register.

The Processor writes the current operating configuration into the write-only FFA3 Parameter Entry LED Register after the Miscellaneous Interface/Parameter Entry I/O asserts PARAMETER DATA WRITE ENABLE (PDWE-0). The writing of each true bit into the LED register causes the corresponding LED to turn on. Each possible operating configuration for a given line of the Parameter Entry card is associated with one or two switches. A current operating configuration is indicated by a lighted LED.

To access the operating configurations, simply move the plastic Parameter Entry card in or out past the outside bezel. Serrations and holes along one edge of the card allow a small light bulb to shine on three carefully placed phototransistors which detect the movement and positioning of the card. A quadrature Motion Detector, composed of Q307, Q309, U111, U121, U131, U141, U211, U221, and U231, detects the direction of card movement by comparing the order in which holes cover or uncover the photodetectors. If the card is moved in, U121 is triggered through Pin 11, which is sensitive to the rising edge of track A. On the other hand, if the card is moved out, U141 is triggered through Pin 3, which is sensitive to the falling edge of track B. In either case, PIRQ-1 is asserted. This signal interrupts the Processor; to read the output buffer, the Processor then asserts PARAMETER ENTRY CARD MOVE (PMVE-0), which is addressed at FFA2.

The FFA3 Register's bit assignment is as follows:

- Bit 7, when true, indicates that the Parameter Entry functional block generated the interrupt.
- Bit 6, when true, indicates a card movement generated the interrupt (as opposed to an activated switch).
- Bit 5, indicates an overrun condition (described later).
- Bit 4, indicates the direction of card movement (true indicates the card moved out).

When the system is initialized, the INITL-0 line lights the INIT LED. This LED indicates that the initialization sequence is not completed. All Parameter Entry switch and display interrupt activity is disabled while the INIT LED is on. To extinquish the INIT LED, the operator moves the Parameter Entry card to the "home" position (card fully inserted). At this point, a hole in the card allows light to strike the track C photodetector (Q311). This turns off the INIT LED and enables the quadrature detector and the Parameter Entry interrupts, thus completing the initialization sequence.

An overrun condition is caused when the Processor is not able to clear the card movement interrupt because of higher priority operations before the operator moves the card again.

ROM Patch "B" Functional Block

It is sometimes necessary to modify or correct some of the Plotter's programmed ROMs. Minor changes to the firmware coding in the ROMs are accomplished using a 2K-byte ROM Patch "B" circuit board (referred to as the Firmware Patch functional block). The ROM Patch "B" circuit board shown in Schematic 3-1 is electrically an extension of the Processor circuit card. The board plugs into a slot just above the Parameter Switches and can accommodate up to two FPLAs (Field Programmable Logic Arrays) with up to 48 locations each, two PROMs (either EPROM or the fusable-link form), and four other fusable-link PROMs. Figure 3-9 shows that these PROMs are located functionally between addresses 4000 and 47FF.

If the data at an address is to be changed, that address and its "new" data are programmed into one of the two FPLAs. Then, when that memory location is addressed, the FPLA first prevents the system ROM memory from placing the incorrect data on the data bus and then places the corrected data on the data bus. To disable the system ROM memory, the ROM Patch "B" circuit board issues FLAG-0. FLAG-0 becomes DDIS-0, which the Processor's Memory Handshake section uses to produce BDDIS-0 (bus data disable). BDDIS-0, in turn, disables the CHIP SELECTS to the system firmware ROMs (or PROMs). The result is that when FLAG-0 is issued by the ROM Patch "B" circuit board, the Processor ROMs do not place any data on the data bus but they still perform all other necessary handshaking with the Processor.

The ROM Patch "B" circuitry permits either single byte replacements or jump instructions to be overlayed. Jump instructions can be made to address locations programmed into other patch PROMs (U315 and U325). Capacity for these two PROMs is 1K-bytes for either EPROMs or 82S2708 field-programmable fusable-link PROMs. In addition, four fusable-link 74S471 PROMs can be used at locations U105, U115, U125, or U135. These provide an additional 512 byte capacity.

PE1-0 from the Processor's PROM/PROM Memory Size section enables U325 (Firmware Patch 1 in Figure 3-9).

PE0-0 and MA8-MA9 enable either U315 or the four 74S471 PROMs through the decoder U305. The address of these locations is shown as Firmware Patch 0 in Figure 3-9.

PG0DIS-0 provides memory bank switching when operating the Diagnostics System (described in Volume 2). On some diagnostic tests, the patches are disabled.

Communications Interface

The plotter uses a Communications Interface circuit card to control host/terminal/plotter communications. Even though the Communications Interface circuit card is designed to control both the GPIB and RS-232 interfaces, the card's electronic circuitry supports only one interface at a time. This means that this circuit card has two separate versions: a GPIB and a RS-232. In either case, the portion of the circuit card controlling the opposite interface is left blank. Therefore, if the Plotter is equipped with both RS-232 and GPIB interfaces, two separate circuit cards, representing each version, are present.

The operation of each interface is controlled by a portion of the Plotter's system memory known as ROM 1. Unlike the remainder of the Plotter's system memory, this ROM is located on the corresponding Communications Interface Module circuit card. This means that the ROM for controlling the RS-232-C Interface is located on the RS-232 version (670-5579-00, 01, 02 . . .) circuit card and is identified as ROM 1R; the ROM for controlling the GPIB (General Purpose Interface Bus) Interface (if installed) is located on the GPIB version (670-5503-00, 01, 02 . . .) circuit card and is identified as ROM 1G. In addition, some early model Plotters used two EPROMs instead of a single ROM. These EPROMs were located in sockets U171 and U181 of either version circuit card. Later, when ROMs became available, the ROMs were installed in socket U171 or U181 of the corresponding circuit cards.

The Communications Interface can be divided into the following circuits, which are described in subsequent paragraphs:

RS-232-C Interface
- Bus Data and Address Transceivers
- Decode
- GPIB/RS-232 ROM
- Bus Handshake
- GPIB/RS-232 Interrupt
- RS-232 Interface
- Terminal-ACIA-Modem Connection
- Baud Rate Generator

GPIB Interface
- Data Bus
- Management Bus
- Transfer Bus
- GPIB Handshake Sequence

RS-232-C Interface

Table 3-6 summarizes all the RS-232 Interface Read/Write Registers in the RS-232 version Communications Interface. The complete description of each register is included in the circuit description.

Table 3-6

RS-232 REGISTERS

Register	Location	Address Strap Setting		Function
		Pri	Sec	
RSCTRL	ACIA	FF40	FF60	Gives the status of ACIA
RSSTUS	ACIA	FF40	FF60	Controls ACIA
RSDATA	ACIA	FF41	FF61	Data from ACIA
RSDATA	ACIA	FF41	FF61	Data to ACIA
READ STATUS	U861	FF43	FF63	Status of control bits (Read)
WRITE STATUS	U761	FF43	FF63	Status of control bits (Write)
BAUDWR	U751	FF42	FF62	Sets receive and transmit baud rate (Write Only)

A complete description of all the RS-232 registers follows in Tables 3-7, 8, 9, 10, 11, and 12.

Bus Data and Address Transceivers. The Data Transceiver (shown in Schematic 4-1), buffers data to and from the Plotter bus (BD0 through BD7). This transceiver is enabled by the Bus Handshake circuit (described later). The direction of data flow through the Data Transceiver is controlled by the WRITE-0 line.

The Address Transceivers separate the Communications ROM and registers from the Plotter bus. These transceivers are always enabled.

Decode. The Decode circuitry (shown in Schematic 4-1) decodes addresses intended for either the ROM or the various registers on the Communications Interface. The Plotter can accommodate up to two separate interfaces — a primary and a secondary. The Communications Interface circuit card has strap provisions (the RS-GP-P-S strap) to assign either interface (GPIB or RS-232) as the PRIMARY or SECONDARY interface. Each interface is assigned a 32-byte address space within the 2K I/O space (see Figure 3-9). The 32-byte address space for the primary Communications Interface (usually the RS-232) is located between FF40 and FF5F; the address space for the secondary Communications Interface (usually the GPIB, if installed) is located between FF60 and FF7F.

GPIB/RS-232 ROM. Since the RS-232 ROM and the GPIB ROM (shown in Schematic 4-1) use the same addresses (E000 to EFFF), it is necessary that the inactive interface is turned off. This happens when the active interface is selected by pressing the desired switch over the INTERFACE SELECT line on the Parameter Entry card. If both interfaces (RS-232-C and GPIB) are installed in the Plotter, the RS-232 Interface is strapped as PRIMARY and, therefore, made active whenever INTERFACE #1 is pressed. On the other hand, if the GPIB interface is the only interface in the Plotter, it is strapped as PRIMARY and, likewise, made active whenever INTERFACE #1 is pressed. The active interface ROM then controls the Processor in the transfer of data to and from the internal bus and between the host and/or terminal.

Bus Handshake. The Bus Handshake circuitry (shown in Schematic 4-1) performs all of the necessary handshaking between the bus and the Communications Interface circuit card as well as enabling the respective GPIB or RS-232 Interface circuitry (described later). When the active interface ROM address is decoded, ASTB-0 and BCK-0 combine with address decode signals (such as RSADR-1 and COMSP-1) to generate ACIEN-1 (ACIA ENABLE) and RSEN-1 (RS-232 ENABLE), when communicating through the RS-232 port. In a similar manner, GPEN-1 (GPIB ENABLE) is generated when communicating through the GPIB port. RSEN-1 and GPEN-1 are used to enable their respective circuits.

GPIB/RS-232 Interrupt. Three interrupts from the Communications Interface (shown in Schematic 4-2) initiate an interrupt to the Processor. Two interrupts, HAND INTERRUPT (HDI) and STATUS CHANGE (SCI), originate from the GPIB circuitry. The other interrupt is the RS-232 INTERRUPT (RSI). (The origin of these interrupts is described in their respective sections described later.) Although the GPIB/RS-232 Interrupt section enables these interrupts to be strapped (RSI-HDI-SCI-0 through 7 strap) at any level zero through seven, the factory sets HDI to level seven and both SCI and RSI to level one. The Interrupt Multiplexer encodes the eight interrupt levels based upon the IRP0-1 to IRP2-1 signal lines. The IRQ-0 output goes to the Processor's IRQ Vectoring circuitry.

RS-232 Interface. The RS-232 Interface circuitry (shown in Schematic 4-2) interfaces the Plotter bus to a RS-232-C line, which is normally connected between a terminal and a modem (host). The Communications Interface is then in series with this line. When the Communications Interface is not using the RS-232-C interface section (or when the Plotter is turned off), all RS-232-C lines are looped through the Plotter without interruption. The relay, K811, controls this looping process (refer to the following Terminal-ACIA-Modem Connection description). The Plotter receives serially transmitted data over the RDATA (received data) line and transmits serial data over the TDATA (transmitted data) line. Three Read/Write Registers and one Write-Only Register transfer and control data through the RS-232 section. Two Read/Write Registers are located inside the ACIA. The other Read/Write and Write-Only Registers are separate in this circuit. All addresses to the various registers depend upon the setting of the primary-secondary strap.

The bit assignments of the Read/Write Status Registers are shown in Table 3-7.

Table 3-7

BIT ASSIGNMENTS FOR RS-232 REGISTERS

Bit	Function
D7	Write — Not used. Read — Always low.
D6	Setting mute to a high disables the data line from the modem to the terminal.
D5	Setting ROMEN to a high enables the RS-232-C PROM/ROM.
D4	LOCAL-1 connects the terminal to the interface only and sends a constant "MARK" to the modem.
D0-D3	Not used.

Terminal-ACIA-Modem Connection. The terminal, the Plotter's interface (primarily the ACIA), and the modem (host) are connected in a "Tee" fashion as shown in Figure 3-10. A relay, K811, determines whether the terminal-modem signals pass through the Communications Interface when the Plotter's power is on. (The signals bypass the interface completely whenever the Plotter is turned off. See Figure 3-10C.) Two possible modes exist when the Communications Interface is active; that is, when Plotter is on and the relay is energized. These modes are LINE and LOCAL.

In LINE mode, the ACIA can receive terminal RDATA from the modem. LINE mode also prevents the terminal from receiving terminal RDATA if MUTE is chosen (Parameter Entry card). In this variation of LINE mode, the terminal's RDATA is heard only by the Communications Interface. Also in LINE mode, the Terminal TDATA is OR'd with the transmit line from the ACIA to the modem. This means that the modem receives data from either the terminal or the Plotter (see Figure 3-10A).

In LOCAL mode, the modem is cut off and all communications occur between the terminal and the Communications Interface (see Figure 3-10B).

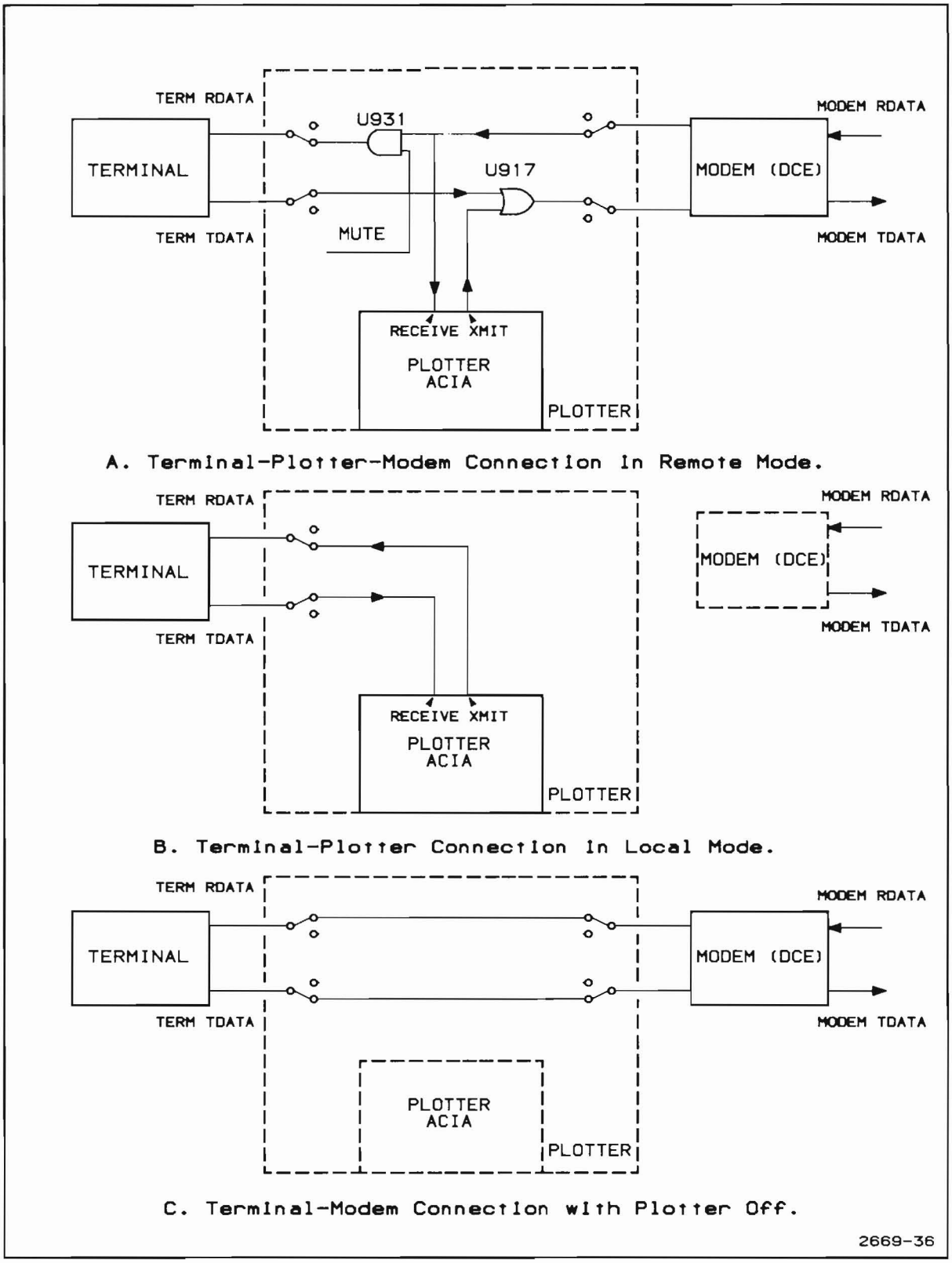

Figure 3-10. Terminal-Plotter-Modem RS-232 Connection.

The Processor uses the three chip select lines, CS0, CS1, and CS2, plus REGISTER SELECT (RS) to read or write into the internal ACIA registers (see the register descriptions which follow). ACIEN-1 from the Bus Handshake section is used to provide a timing signal to the ACIA (all data transfers take place during the Phase 2 portion of the Processor cycle). The control signals CLEAR-TO-SEND (CTS), DATA CARRIER DETECT (DCD), REQUEST-TO-SEND (RTS), and DATA TERMINAL READY (DTR) are provided for handshaking with the terminal-modem line.

The bit assignments of the internal registers in the ACIA are shown in Tables 3-8, 9, 10, 11, and 12.

Table 3-8

RSCTRL REGISTER (ACIA)

Bit	Function
D7	Enables interrupts from the receive section of the ACIA (i.e., Receive Data Register Full, RDRF, and Data Carrier Detect, DCD-0, cause an interrupt when this bit is set high).
D6	Provide for interrupt control from the Transmit Data Terminal Ready output and for the transmission of a break level (space). See Table 3-18.
D2-D4	Select word length, parity and stop bits (see Table 3-19).
D0-D1	Select the divide ratio utilized in both transmitter and receiver (see Table 3-20).

Table 3-9

D5 AND D6 BITS OF RSCTRL REGISTER (ACIA)

D6	D5	Function
0	0	If DTR-0 is low, Transmitting Interrupt is disabled.
0	1	If DTR-0 is low, Transmitting Interrupt is enabled.
1	0	If DTR-0 is high, Transmitting Interrupt is disabled.
1	1	If DTR-0 is low, a Break level is transmitted on the Transmit Data Output, and Transmitting Interrupt is disabled.

Table 3-10

D2, D3, AND D4 BITS OF RSCTRL REGISTER (ACIA)

D4	D3	D2	Function
0	0	0	Seven Bits + Even Parity + Two Bits
0	0	1	Seven Bits + Odd Parity + Two Stop Bits
0	1	0	Seven Bits + Even Parity + One Stop Bit
0	1	1	Seven Bits + Odd Parity + One Stop Bit
1	0	0	Eight Bits + Two Stop Bits
1	0	1	Eight Bits + One Stop Bit
1	1	0	Eight Bits + Even Parity + One Stop Bit
1	1	1	Eight Bits + Odd Parity + One Stop Bit

Table 3-11

D0 AND D1 BITS OF RSCTRL REGISTER (ACIA)

D1	D0	Function
0	0	Divide by one
0	1	Divide by 16
1	0	Divide by 64
1	1	Master Reset

Table 3-12

RSSTUS REGISTER (ACIA)

Bit	Function
D7	This bit indicates the status of the interrupt request line (IRQ). A high means a pending interrupt.
D6	A high indicates a parity error has occurred.
D5	A high indicates an overrun error has occurred.
D4	A high indicates a framing error has occurred.
D3	When low, a CTS-0 has been sent by the modem.
D2	DCD-0 indicates the carrier from the modem is not present. DCD-0 is cleared when RSSTUS is read.
D1	Transmit Data Register Empty indicates when new data may be entered.
D0	Receive Data Register Full indicates receive data has been transferred to the Receive Data Register. RDRF is cleared when the Receive Data Register is read or reset.

Bits D7 through D0 of the RSDATA Register form the data byte to and from the ACIA. Bytes to and from the ACIA pass through this register. Writing data into RSDATA causes TDRE to go low, indicating that the register is full. When a byte is to be read, RDRF will be true. After a RSDATA read, RDRF will be cleared, although the data is still available and valid.

Baud Rate Generator. Refer to Schematic 4-2 while reading the following description. The Communications Interface uses one byte to represent both the receive and transmit baud rates (see Table 3-13). When the Baud Rate Register (a Write-Only Register) is addressed, it loads the baud rate byte from the Plotter bus. The incoming Bus Clock frequency (14.7456 MHz) is divided by six and is fed into a Programmable Bit Rate Generator. The bit rate generator has the following internal components:

- a prescaler used as a scan counter for multichannel operation,
- a network of counter chains to generate the required standardized frequencies, and
- an output multiplexer to allow the selection of the desired bit rate.

The Q0 output of the prescaler (Pin 1) is used to select alternately the B inputs to the Transmit Clock Latch and the A inputs to the Receive Clock Latch. The outputs of these latches are used as input multiplexer select bits in the Programmable Bit Rate Generator to generate the respective baud rates at the Z output (Pin 10). The Programmable Bit Rate Generator also multiplexes external RCLK and TCLK inputs, if used. Table 3-23 gives the baud rates available and the corresponding hex character notation received by the Baud Rate Generator.

Table 3-13

BAUDWR (WRITE-ONLY)

Bit	Function
D0-D3	Sets transmit baud rate (see Table 3-23).
D4-D7	Sets receive baud rate (see Table 3-23).

Table 3-14

U951 HEX CODES FOR BAUD RATE GENERATION

Hex Code	Baud Rate Selected
0	Multiplexed Input
1	Multiplexed Input
2	50
3	75
4	134.5
5	200
6	600
7	2400
8	9600
9	4800
A	1800
B	1200
C	2400
D	300
E	150
F	110

To set transmit and receive baud rates, send both rates to BAUDWR at the same time. In other words, to transmit at 1200 and receive at 4800, write 9B to the Baud Rate Generator. When using external clocks from a modem, select either Multiplexed Input.

GPIB

General Information. The GPIB circuitry (shown in Schematics 13-1, 13-2, and 13-3) transfers data between the GPIB bus connector and the Plotter's bus. The Plotter's GPIB interface uses the second version of the Interface circuit card (with the RS-232 circuitry removed). The GPIB is a group of 24 signal lines between the Plotter and the GPIB Controller. Eight of these lines are grounds and the other 16 are functionally grouped into three buses: Data, Management, and Transfer. These three buses are described in more detail in subsequent paragraphs.

The Plotter's back panel GPIB connector (mounted on the GPIB Adapter circuit board) is shown in Figure 3-11. All devices on the GPIB are connected in parallel and all lines on the GPIB bus are active low and passive high.

Table 3-15 outlines the GPIB Interface Read/Write Registers while Table 3-16 gives the bit assignments for each register.

Table 3-15

GPIB INTERFACE READ/WRITE REGISTERS

Register	Location	Address Strap Setting		Function
		Pri	Sec	
COMMAND READ	U321, U517	FF40	FF60	Command Byte Read
COMMAND WRITE	U121	FF40	FF60	Command Byte Write
STATUS READ	U131	FF41	FF61	Status Byte Read
STATUS WRITE	U337	FF41	FF61	Status Byte Write
SHAKE	U317	FF42	FF62	Shake Read
SHAKE	U551	FF42	FF62	Shake Write
DATA READ	U317, U517	FF43	FF63	Data Read From GPIB
DATA WRITE	U117	FF43	FF63	Data Write to GPIB

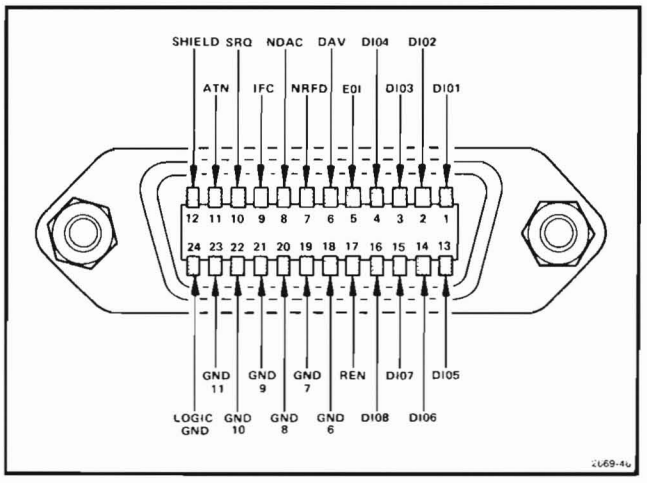

Figure 3-11. GPIB Connector.

Table 3-16

BIT ASSIGNMENTS FOR GPIB REGISTERS

Register	Bit	Function
COMMAND READ (MANAGEMENT BUS)	D7	Attention (ATN) from GPIB.
	D6	End or Identify (EOI) from GPIB.
	D5	Error (ERR-1) when NDAC and NRFD both not true (an invalid condition on the GPIB).
	D4	D4 of CMDWR.
	D3	D3 of CMDWR.
	D2	Remote Enable (REN) from GPIB.
	D1	Service Request (SRQ) from GPIB.
	D0	Interface Clear (IFC) from GPIB.
COMMAND WRITE (MANAGEMENT BUS)	D7	Sets Attention (ATN) on GPIB.
	D6	Sets End or Identify (EOI) on GPIB.
	D5	Enables the EPROM/ROM containing the GPIB driver.
	D4	Sets the interface as a Talker to the GPIB; for a Read, becomes a Listener.
	D3	Enables GPIB bus drivers for handshake lines.
	D2	Sets Remote Enable (REN) on GPIB.
	D1	Sets Service Request (SRQ) on GPIB.
	D0	Disables U311 from driving GPIB (used for OFFLINE).
STATUS READ	D7	When high, denotes an interrupt is pending in the GPIB section.
	D6	When low, denotes a HAND interrupt has occurred. This indicates that data is valid from the GPIB to the bus or that data has been received by the GPIB listeners.
	D5	When low, denotes a state change interrupt of ATN, SRQ, IFC, REN, or EOI has occurred.
	D4	Additional representation of HAND.
	D3	High always.
	D2	High always.
	D1	Reads D1 of STSWR.
	D0	Reads D0 of STSWR.

Table 3-16 (cont)

BIT ASSIGNMENTS FOR GPIB REGISTERS

Register	Bit	Function
STATUS WRITE	D7	Not used.
	D6	Writing a 1 clears HAND Interrupt.
	D5	Writing a 1 clears SCI Interrupt.
	D2-D4	Not used.
	D1	Hand Interrupt Enable (HIE), which when true, allows the HAND signal to generate an interrupt. (HAND either initiates or terminates a data transfer from the GPIB.)
	D0	State Change Interrupt Enable (SCIE), which when true, allows a state change of ATN, SRQ, IFC, EOI, and REN to cause an interrupt.
SHAKE	D2-D7	High always.
	D1	When high, GPIB PROM/ROM has been enabled.
	D0	Low always.
SHAKE	D1-D7	Not presently used.
	D0	Writing a high into this bit position pulses the SHAKE line to either transmit a byte to the GPIB or to acknowledge the receipt of a data byte.
DATA READ	D0-D7	This is the data byte read from the GPIB.
DATA WRITE	D0-D7	This is the data byte written to the GPIB.

For information on the following GPIB circuits, refer to Schematic 13-1 and the corresponding topics in the RS-232 Interface discussion:

- Bus Data and Address Transceivers
- Decode
- GPIB/RS-232 ROM
- Bus Handshake
- GPIB/RS-232 Interrupt (refer to Schematic 13-2)

Data Bus (and Read/Write Registers). The Data Bus (refer to Schematic 13-3) consists of eight bi-directional signal lines (DIO1 through DIO8) and is separated from the Plotter's data bus by two quad Data Bus Transceivers. Data Read or Data Write Registers control the data flow throughout the GPIB interface. The addresses of these registers depend upon the PRIMARY-SECONDARY strap setting (see the RS-232 Decode section earlier).

Incoming data, DIO1 through DIO8, from the GPIB Interface passes through the Data Bus Transceivers to the Data Read Registers and onto the Plotter's data bus as D0 through D7. On the other hand, outgoing data passes from the Plotter bus (D0 through D7) through the Data Write Register to the Data Bus Transceiver and onto the GPIB Data Bus as DIO1 through DIO8. One eight-bit byte is transferred over the bus at a time in parallel. DIO1 (DATA IN-OUT, BIT 1) represents the least significant bit in the byte whereas DIO8 represents the most significant bit. Each byte can represent a primary or secondary address, a universal command, or a data byte. Primary or secondary addresses and universal commands are distinquished from data bytes by having ATTENTION (ATN — see the Management Bus described later) asserted while they are sent.

Management Bus. The Management Bus is a group of five signal lines which are used to control the data transfer over the GPIB Data Bus. The five signal lines are shown in Table 3-17.

Table 3-17

MANAGEMENT BUS SIGNAL LINES

Signal	Signal Name	Function
ATN	Attention	When ATN is asserted on the GPIB, the Communications Interface is forced to listen. Only device addresses (primary or secondary) and control messages can be transferred over the GPIB when ATN is active low.
SRQ	Service Request	Any device on the GPIB can request the attention of the GPIB Controller by asserting SRQ active low.
IFC	Interface Clear	The IFC signal may be sent by the GPIB controller to put all devices on the GPIB into an inactive state. If the Communications Interface is performing a task when the GPIB controller asserts IFC (active low), the interface interrupts that task and goes into an inactive state, awaiting possible commands from the GPIB Controller.
REN	Remote Enable	The REN signal is used by the GPIB systems to transfer devices from manual operation to remote control operation.
EOI	End or Identify	The EOI signal is used by the Talker to indicate the end of a data transfer sequence. The Talker activates EOI as the last byte of data is transmitted.

Management Bus signals, which originate as data bytes from the Processor, are transferred from the Plotter's bus to the GPIB bus. To do this, they go through the Command Write Register and the Management Bus Transceiver to the GPIB Management Bus (except EOI, which goes through U311, another quad-bus transceiver). The incoming management signals are routed through the Management Debounce circuit (for SRQ, ATN, and IFC). Separate combinations of U351, a 220 Ω resistor, and a .1 μF capacitor are used to debounce REN and EOI. Following the Debounce Management circuit, the bus signals pass through the Command Read Register to the Plotter's data bus (except U517 handles EOI and ATN). After the management signals are debounced, their status is monitored by a combination of two hex-latches, U541 and U547, and a six-bit comparator, U537. If the status of any management line should change, a STATUS CHANGE INTERRUPT (SCI) is sent to the GPIB/RS-232 Interrupt section to produce IRQ-0. This causes the Processor to read the Status Register to see whether the interrupt was a HAND INTERRUPT (described later) or a STATUS CHANGE INTERRUPT.

Transfer Bus. The Transfer bus is composed of three signal lines which execute a handshake sequence each time a byte is transferred over the data bus. The Transfer Bus signals are as shown in Table 3-18:

Table 3-18

TRANSFER BUS SIGNAL LINES

Signal	Signal Name	Function
NRFD	Not Ready For Data	An active low NRFD signal indicates that one or more assigned Listeners are not ready to receive the next byte. When all of the Listeners for a particular data transfer have released NRFD, the NRFD line goes inactive high. This tells the Talker that it may place the next byte on the data bus.
DAV	Data Valid	The DAV line is activated by the Talker shortly after placing a valid byte on the data bus. An active low DAV signal tells each Listener to capture the data presented on the data bus. The Talker is inhibited from activating DAV when NRFD is active low.
NDAC	No Data Accepted	The NDAC signal is held active low by each Listener until it has captured the byte currently presented on the data bus. When all Listeners have captured the byte, NDAC goes inactive high. This notifies the Talker that it may remove the byte from the data bus.

Handshake Sequence. The GPIB interface uses two signal lines — SHAKE and HAND — to cause the Communications Interface to handshake with the receiving device on the GPIB bus (Figure 3-12 shows this handshaking sequence).

If the GPIB Interface is transmitting bytes to the GPIB bus from the Plotter bus, the initial conditions would have NRFD (Not Ready For Data) as false and NDAC (No Data Accepted) asserted true. The Processor would then load data into the Data Write Register and write a 01 in hex to the Shake Write Register. This asserts SHAKE-0, which in turn asserts DAV (Data Valid) to the receiving device on the GPIB bus. The receiving of this data (and DAV) causes the receiving device to change the status of NRFD to true and NDAC to not true. The GPIB Interface then uses the false condition of NDAC to change DAC to false. Later, after the receiving device has processed the data and sees DAC false, it changes the states of NDAC to true and NRFD to false. This indicates that the receiving device can receive more data. Now, the false indication of NRFD in the receiving device causes the Plotter's GPIB Interface to generate HAND-1. This signal, in turn, causes an interrupt (HDI) to be processed by the GPIB/RS-232 Interrupt section. This interrupt goes to the Processor as IRQ-0. The Processor responds by loading more data into the Data Write Register and writing a 01 in hex to the Shake Write Register, thereby repeating the process.

The sequence is reversed when the GPIB Interface is receiving bytes from the GPIB bus and transferring them to the Plotter bus. The receiving Plotter GPIB Interface has NRFD false and NDAC true as initial conditions. The transmitting device starts by loading data on the GPIB bus and asserting DAV. This means that this data is received by the Data Read Registers. The Communications Interface receives the DAV signal as a HAND-1 signal. Receiving a HAND signal causes two things to happen. First, it causes an HDI interrupt to the GPIB/RS-232 Interrupt section. This signal is converted to an IRQ-0 to the Processor, which causes the Processor to stop and process the incoming GPIB data. Secondly, the Plotter's GPIB Interface asserts NRFD-0 back to the transmitting device. This tells the transmitting device that the Communications Interface is not yet ready to receive more data. The HDI Interrupt is cleared when the Processor writes a 40 in hex into Status Write. After the data has been read, the Processor writes 01 in hex to the Shake Write Register, which causes NDAC to be changed to false. This, in turn, tells the transmitting device that the data has been accepted and another byte can be sent. The transmitting device must then change DAC to false, which will, in turn, cause the Plotter's GPIB Interface to change NDAC to true and NRFD to false. This establishes the initial receive condition; the transmitting device can now load more data on the GPIB bus and assert DAV to repeat the process.

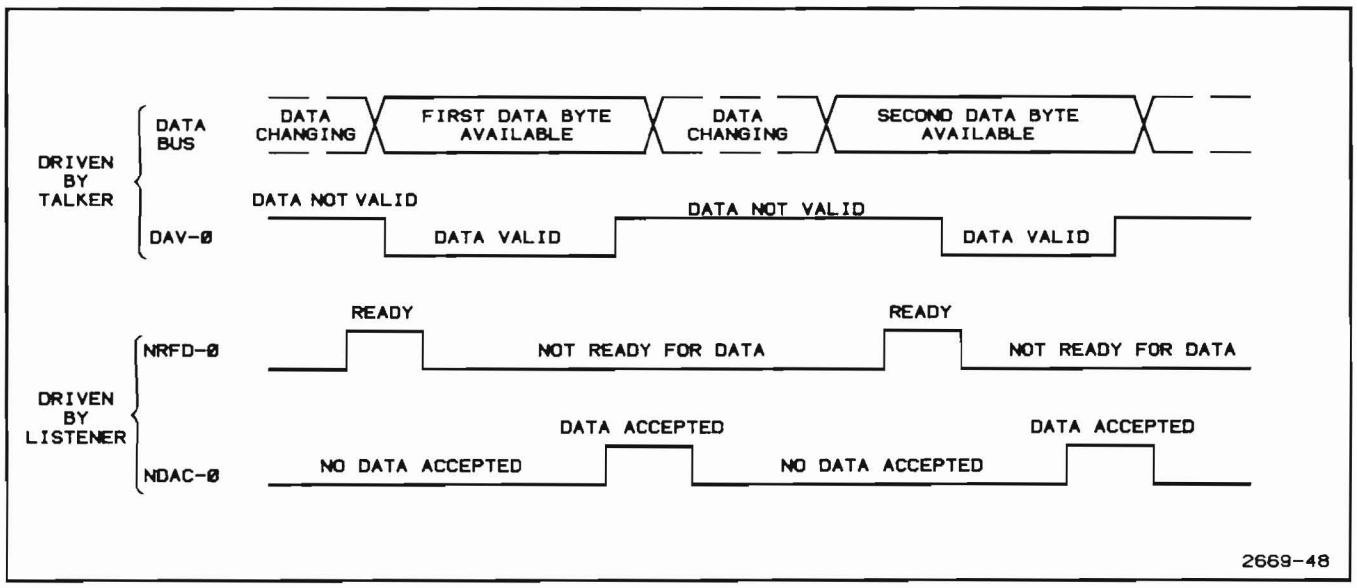

Figure 3-12. GPIB Handshake Sequence.

RS-232-C Adapter

The RS-232-C Adapter board schematic 5-1 has two connectors — "Terminal" and "Host." This Adapter board was designed to operate with the Communications Interface circuit card.

Vector Generator

The Vector Generator performs two functions in the 4663 Plotter. First, it converts the operator switch commands into data bytes to be processed by the Processor. (Conversely, this also means that the Vector Generator converts data from the Processor into front panel light displays which show the Plotter's current operational status.) The second major function of the Vector Generator is retrieving commands for pen motion and pen force from system memory and converting these into motor phase and pen solenoid information for the Motor Pen Drive functional block (described later).

The Vector Generator resides on the Plotter's backplane and communicates with three other functional blocks which are not directly connected to the main backplane. These three other modules are the Front Panel Switches and Lights, the Joystick Rate Generator, and the Motor Pen Drive.(Figure 3-1 shows a diagram of this relationship.)

The Vector Generator can be divided into two major circuits: the Front Panel Switches and Lights Interface, and the Motion Generation Interface. While following the descriptions of these two Vector Generator circuits, it may be helpful to refer to the circuit descriptions of the Front Panel Switches and Lights, the Joystick Rate Generator, and the Motor Pen Drive later in this section.

Front Panel Switches and Lights Interface

The Front Panel Switches and Lights Interface converts operator activated switch commands into data bytes suitable for processing. This also means that the circuitry converts data bytes from the Processor into the front panel light display to show the Plotter's current operational status. The data from the Front Panel Switches and Lights may be used to control other circuits or generate desired functions, such as advancing paper, outlining the viewport, establishing the viewport, etc.

A diagram of the Vector Generator's Front Panel Interface is shown in Figure 3-13. Each functional block shown on this diagram is discussed in subsequent paragraphs. Refer to Schematics 6-1 and 6-2 when reading these descriptions.

Address Decode. The Address Decode section performs the address decode function for both the Front Panel Switches and Lights Interface and the Motion Generation Interface. The Address Decode section responds to all addresses between FDE0 and FDFF. This is a portion of the I/O Address Space (the upper 2K) shown in Figure 3-9 and Table 3-1.

The Front Panel Switches and Lights Interface, however, uses only the addresses between FDE0 and FDE3. These are decoded with the Front Panel Register Enable. Whenever a Vector Generator address is decoded, the Data Bus Transceiver must be enabled. To this, each time a Vector Generator address is decoded, the Address Decode sends the following two signals:

1. A signal, labeled FDE0 to FDFF Decode, is sent to the Bus Handshake, which enables the Vector Generator to observe normal bus protocol.
2. A signal is sent to Pin 10 of U55 (a NAND gate).

After the Bus Handshake section has completed its handshake (described under Processor Read/Write protocol earlier) with the Processor, a signal from the Bus Handshake goes to Pin 9 of this same NAND gate to signal the end of ASTB-0. The combination of the signals on this gate generates the signal XCVR-0. XCVR-0, in turn, enables the Bus Transceiver to transfer data back and forth between the Vector Generator and the Plotter bus. The direction of data flow through the Bus Transceiver depends upon the condition of the Processor's WRITE-0 line.

In the remaining descriptions, if the Processor is communicating with any functional block in the Vector Generator, it is assumed that the Address Decode and the Bus Handshake sections have enabled the Bus Transceiver in the manner described here.

If an address above FDE3 is decoded, the Motion Generation Register Enable provides the enable for the appropriate registers and the Data Bus Transceiver.

Bus Handshake. See description of Address Decode earlier.

Bus Transceiver. See description of Address Decode earlier.

Switch Change Logic. Although the Front Panel Switches and Lights are described in detail later, a brief overview of that circuit is provided here. Each time a front panel switch is either pressed or released, the Front Panel Switches and Lights circuit board produces SWCHG-0. SWCHG-0 causes the Vector Generator Switch Change Logic to generate SWWR1-0 (or SWWR2-0 which will be described later). This signal causes Switch Latch 1 to store the data from the switch matrix lines SWPOS0-1 through SWPOS4-1. At the same time, SWWR1-0 (or SWWR2-0) also causes the Front Panel Interrupt section to generate FPIRQ-0 to the Interrupt circuit. FPIRQ-0 then becomes IRQ-0 and tells the Processor that a switch has been pressed (or released) and to stop and read its status. The Processor, after completing its present task, first reads address FDE1; reading this address enables the Interrupt circuitry and is a part of the Processor's interrupt routine. Reading FDE1 also causes the Switch Change Logic to generate SWRD1-0, which is sent to Switch Latch 1. This transfers the switch matrix data stored in Switch Latch 1 to the Vector Generator's D0-D7 data bus. Then, after all necessary bus handshaking between the Processor and the Vector Generator has been accomplished, the switch matrix data is further transferred through the Bus Transceiver to the Processor's data bus.

The Switch Change Logic also provides 2-key rollover, by using a second switch latch (Switch Latch 2). This second latch is used when the operator presses (or releases) a second front panel switch before the Processor can read and clear the status of an earlier activated switch. If the second switch latch is used, the generation of SWWR2-0 causes the Switch Change Logic to generate CTRDIS-1, which is used by the Front Panel Switches and Lights section to disable the keyboard matrix scan counter until the Processor can read the status of Switch Latch 2.

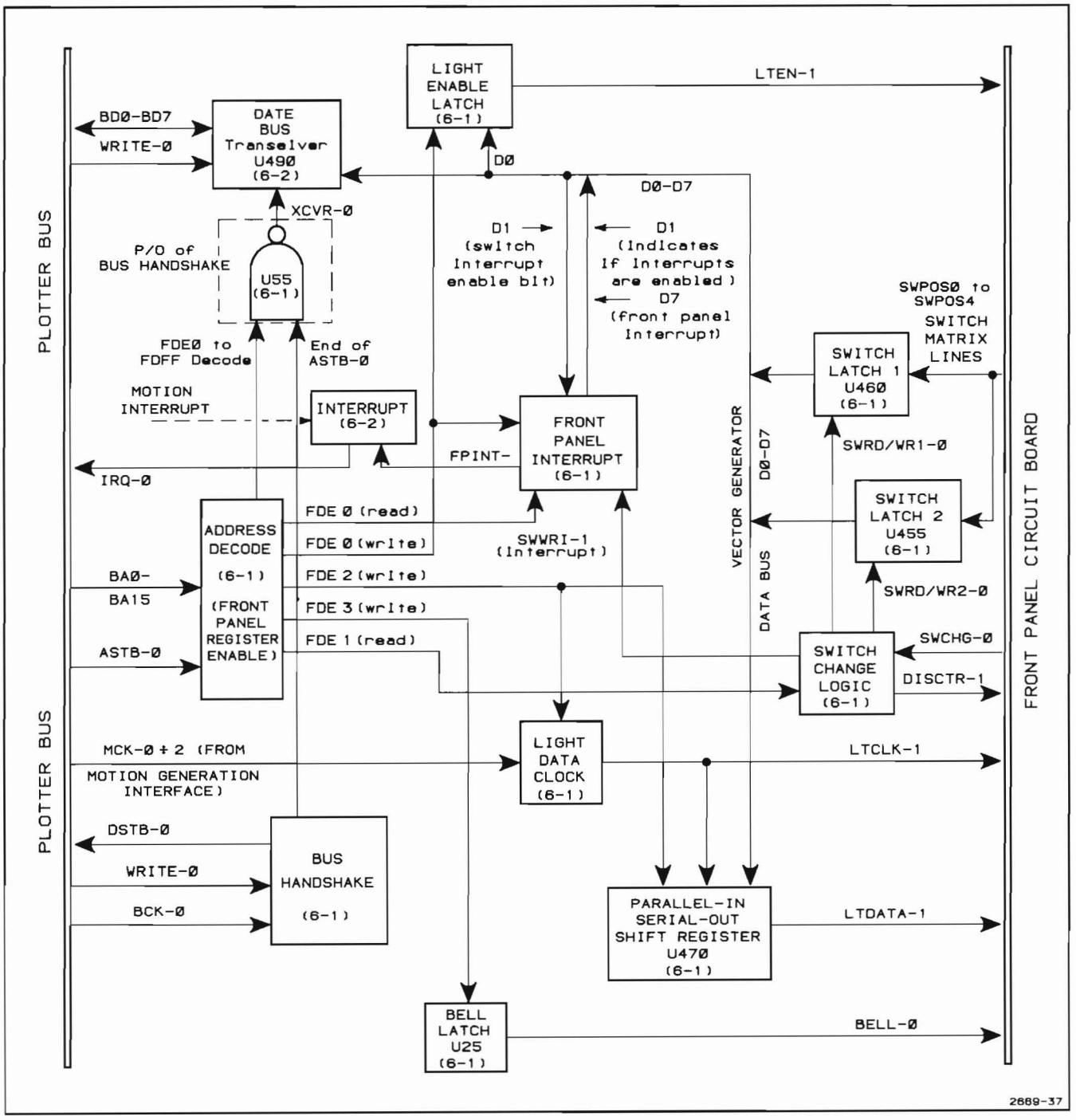

Figure 3-13. Front Panel Interface Portion of the Vector Generator.

Front Panel Interrupt. The Front Panel Interrupt generates an FPINT-0 signal to the Interrupt circuit each time the Switch Change Logic receives a SWCHG-0 signal from the Front Panel circuit board. This interrupt is converted to an IRQ-0 to the Processor (refer to the description of the Interrupt circuitry later in the Motion Generation Interface description). Each time that CTRDIS-1 is generated (see Switch Change Logic earlier), FPINT-0 is also asserted. This interrupt is enabled when the Processor writes a "1" into Bit 1 of address FDE0 (this is part of the interrupt service routine). The reading of a "1" at address FDE0 indicates that the Front Panel Interrupt section is enabled.

Light Enable Latch. The Light Enable Latch generates LTEN-1 whenever the Processor writes a "1" into FDE0. LTEN-1, in turn, enables the front panel status lights to be turned on. Remember that this signal does **NOT** in itself turn the lamps on. The lamps are powered by lamp-drivers, which are addressed when the Processor sends LTDATA-1. LTEN-1 simply functions as an enable for the lamp-drivers and is instrumental in the lamp status update sequence. When the Processor wishes to change the status of any of the lights, it first turns off LTEN-1 by writing a "0" into address FDE0. This turns all of the lamps off. LTDATA-1 is then serially fed into the lamp-drivers on the Front Panel circuit board. Following LTDATA, LTEN-1 is again asserted, enabling those lamp-drivers with LTDATA-1 asserted to be turned on.

Parallel-In/Serial-Out Shift Register. The Parallel-In/Serial-Out Shift Register is used to store the serial transfer of LTDATA-1 to the Front Panel circuit board. The Processor first places one half of the LTDATA-1 information on the Vector Generator data bus D0-D7 in a parallel form (through the Data Bus Transceiver). Since each bit corresponds to one light, eight lights are represented. Then, the Processor writes into address FDE2. This causes the Parallel-In/Serial-Out Shift Register to serialize this byte as LTDATA-1. The Light Data Clock generates a eight-count clock to regulate the serial transfer of LTDATA-1 to one half of the front panel lamp-drivers. After the first byte of LTDATA-1 has been transferred, the process is repeated for the second byte of LTDATA-1 (representing the remaining eight lights on the front panel).

Light Data Clock. The Light Data Clock generates a string of eight pulses (LTCLK-1) to clock LTDATA-1 through the parallel-to-serial conversion in the Parallel-In/Serial-Out Shift Register. LTCLK-1 is also used by the Front Panel Switches and Lights functional block to shift LTDATA-1 into the proper lamp-drivers. The clock is started at the same time that the Processor writes into address FDE2, which loads the Parallel-In/Serial-Out Shift Register with LTDATA-1. The clock counts every other MCK-0 pulse (MCK-0, as will be described later, is a 1/8 division of the bus clock, BCK-0). The clock outputs these pulses as LTCLK-1 at Pin 14 of the Parallel-In/ Serial-Out Shift Register. This means that LTCLK-1 is a 1/16 division of BCK-0. When the Light Data Clock has counted 16 and output eight of these MCK-0 pulses, the carry pulse at Pin 15 of U130 shuts off the counter until the next time the Processor writes to address FDE2.

Bell Latch. The Bell Latch provides an enable (BELL-0) to a 1000 Hz oscillator located on the Front Panel circuit board whenever the Processor writes a "01" into address FDE3. The output of this oscillator is fed into a small speaker in the chassis of the Plotter. This bell tone can function as an alert or prompt to the operator. The bell will remain on until a "00" is written in address FDE3.

Motion Generation Interface

The Motion Generation Interface, which is the second major portion of the Vector Generator, retrieves and converts commands for pen motion and pen force/selection into motor phase and pen solenoid information. The Motion Generation Interface is shown in Schematics 6-2, 6-3, and 6-4. Figure 3-14 is the functional block diagram for this portion of the Vector Generator.

The heart of the Vector Generator is the 8X300 microprocessor. The 8X300 has its own RAM, FPROM, and I/O registers just like any other processing system. It connects with the remainder of the Plotter through a DMA port. This means that the Motion Generation Interface portion of the Vector Generator appears as a DMA (direct memory access) device to the 6800 Processor.

It may be helpful to refer to the description of the Bus DMA Operation earlier in this section for details concerning DMA transactions.

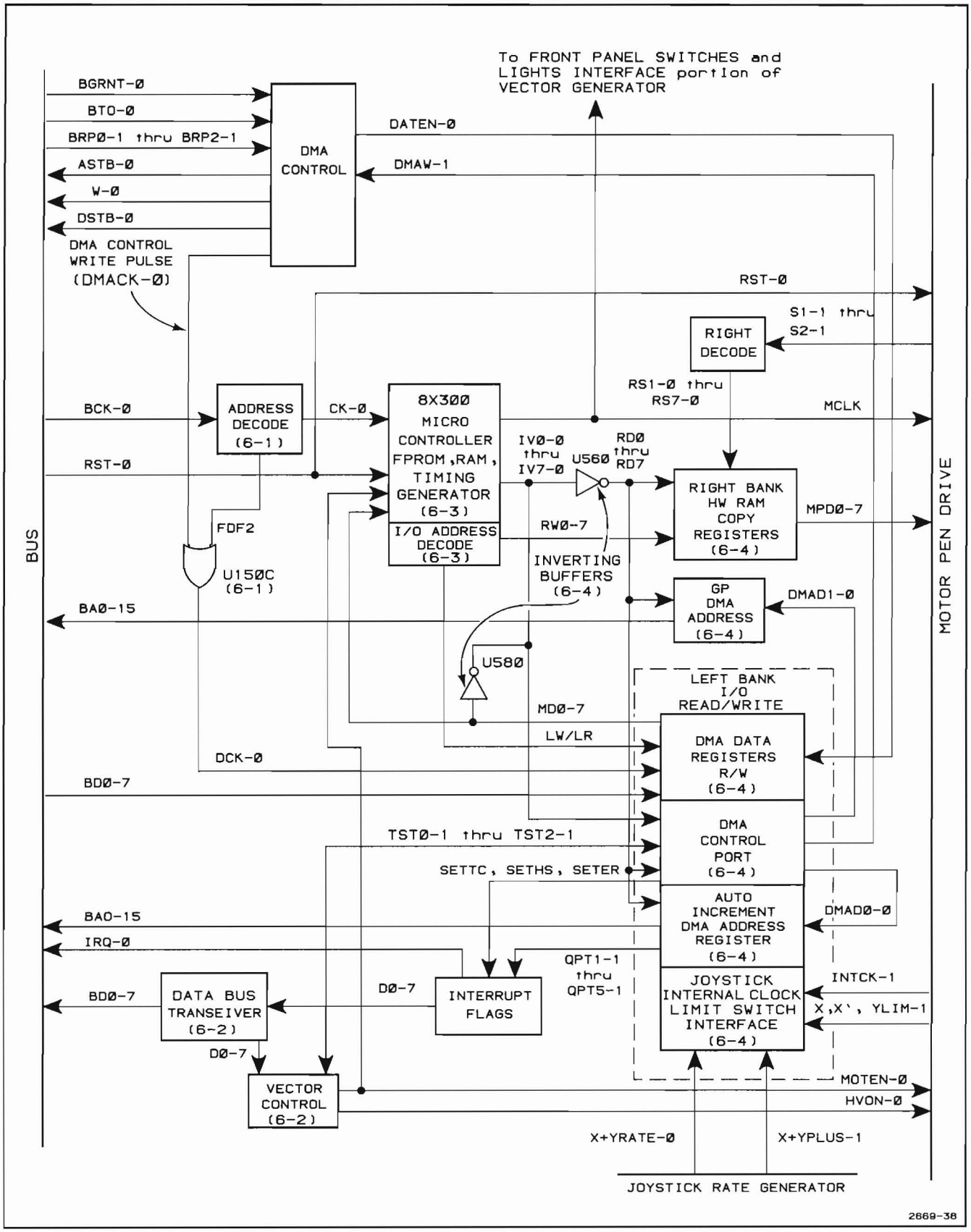

Figure 3-14. Motion Generation Interface Portion of the Vector Generator.

General Operating Scheme. When the Plotter is first turned on, the 6800 Processor provides the 8X300 microprocessor with the information necessary for the Vector Generator's DMA Control to communicate with the Processor's DMA Bus Control. Specifically, the Processor provides the 8X300 with the locations to vector-generating data stored in the 6800's RAM and ROM. Other data includes the location of a 64-byte segment of RAM referred to as the "circular queue," X- and Y-axis position registers, pen parameter tables, and pen velocity profile tables. This information is transmitted via a DMA operation into several I/O registers in the Vector Generator.

In particular, the Vector Generator uses two versions of DMA. Instructions in the 8X300's own ROM tell the 8X300 which version of DMA is to be carried out during Plotter operation.

The first type of DMA is referred to as an Auto Increment DMA. The Vector Generator uses this type of DMA to access only the 64-byte circular queue in system RAM. Information stored in this circular queue includes pen status (up or down), pen commands, and joystick axis enable commands. To guide the Vector Generator in addressing this portion of the system RAM, a 64-step counter automatically increments the address on the address bus lines with each DMA transaction. This means that once the first address is established, the 8X300 reads each address of the circular queue in sequence. Data read from this portion of RAM is the motion and pen data written there by the 6800 Processor earlier.

The second version of DMA is referred to as a General Purpose DMA. In this version, the 8X300 uses memory locations supplied by the 6800 Processor during power-up to access data from ROM or RAM. This means that only one byte of data can be retrieved with each DMA transaction. General Purpose DMA is also used to obtain the first address of the circular queue. Generally, the type of data obtained using this version of DMA includes X- and Y-axis position, and pen pressure or speed tables.

The 8X300 converts the data obtained from the 6800 Processor by DMA transactions into a series of four bytes for the Motor Pen Drive functional block. Three bytes provide motor phase information for the three pen drive motors, while the fourth byte provides the pen pressure for the active pen.

8X300 Microprocessor. The 8X300 (shown in Schematic 6-3) is a bi-polar microprocessor. For the purpose of this description, the 8X300 microprocessor also consists of RAM, FPROM, and timing. The 8X300 microprocessor has been configured for direct workspace addressing by adding the address lines ID16 through ID23. This permits the 8X300 to both output an address and read (or write) data during a single 8X300 clock cycle.

Most of the 8X300's memory consists of a right and left bank. These two banks contain several registers and together form the workspace for the 8X300 microprocessor. This means that the 8X300 can mix or interchange data between the two banks. The 8X300's LB-0 and RB-0 outputs are used by the I/O Address Decode to determine which memory bank is addressed for a given transaction. The I/O Address Decode uses SC-1 as the address write, while WC-1 becomes the data write.

Because the 8X300 uses signal states that are complementary to the remainder of the Plotter's circuitry, the Inverting buffers are used to connect the 8X300. Therefore, the 8X300 signal lines are shown as IV (data); the complement (normal Plotter convention) is RD.

Normally, the 8X300 stores DMA-obtained data in the left bank memory (the Read DMA Data Register). The Write DMA Data Register, on the other hand, stores data which is pending a DMA write from the Vector Generator to the 6800 Processor.

The Timing Generator converts BCK-1 into two 50% duty-cycle, square-wave signals, X1 and X2, which are 180° out of phase. These signals form the basic timing for the 8X300. Vector Generator and Motor Pen Drive synchronization is controlled by MCK-1, which is produced by the 8X300. MCK-1 is a 1/4 division of X1 (or a 1/8 division of BCK-1).

Table 3-19 shows the memory map for the 8X300 processing system.

Table 3-19

8X300 MEMORY MAP

LEFT BANK

Transaction	Locations	Bit	Contents
Read	00-77 (Octal)	7	Integration clock (15.191 μs)
		6	Joystick X-axis move flag
		5	Joystick Y-axis move flag
		4	Joystick X-axis direction
		3	Joystick Y-axis direction
		2	X-axis limit detector
		1	X'-axis limit detector
		0	Y-axis limit detector
	100-177	0-7	Data byte returned from DMA read
	200-277	0-7	Not used
	300-377	7	DMA completed flag
		3-6	Not used
		0-2	Indicates diagnostic test desired
Write	00-77 (Octal)	7	Not used
		6	Resets Joystick X-axis moved flag
		5	Resets Joystick Y-axis moved flag
		3-4	Not used
		2	Sets Task Complete interrupt
		1	Sets Motion Sync interrupt
		0	Sets Error interrupt
	100-177	0-7	Data byte for DMA write
	200-277	0-7	Loads Queue DMA base pointer (U285)
	300-377	7	Triggers General Purpose/Queue DMA cycle
		6	Allows pre-increment of Queue DMA address
		5	Selects DMA read/write cycle
		0-4	Not used

RIGHT BANK

Transaction	Locations	Bit	Contents
Write Only	77	0-7	Pen Pressure Register (U380)
	76	0-7	X-phase register (U375)
	75	0-7	X'-phase register (U370)
	74	0-7	Y-phase register (U365)
	73	0-7	Not used
	72	2-7	Not used
		1	X-axis low current
		0	Y-axis low current
	71	0-7	MSB of General Purpose DMA address
	70	0-7	LSB of General Purpose DMA address
	00-67	0-7	RAM

Right Bank Hardware RAM Copy/Right Decoder. After DMA data is received, the 8X300 uses this information to write motor rotation and/or pen pressure data into the right bank memory, known as the Hardware RAM Copy (shown in Schematic 6-4). This information is transferred to the Motor Pen Drive functional block to cause the Plotter's pen to go up or down or to move the pen carriage. To do this, the Motor Pen Drive module interrogates the four registers sequentially. The sequence is controlled by the binary count on the S0-1, S1-1, and S2-1 signal lines. These lines cause the Right Decode section to output motor phase information for the X motor, the X' motor, and the Y motor, and pen pressure information. This process is described in more detail under the Motor Pen Drive functional block.

Left Memory Bank. The left memory bank (shown in Schematics 6-2 and 6-3) consists of four groups of registers which operate under DMA control. These four groups of registers are discussed in the following paragraphs:

Read/Write DMA Data Registers
DMA Control Port Registers
Auto Increment DMA Address Registers
Joystick, Integration Clock, Limit Switch Interface

Read/Write DMA Data Registers. The DMA Data Register section consists of two registers: the Read DMA Data Register transfers incoming DMA data, and the Write DMA Data Register transfers outgoing DMA data. DATA CLOCK (DCK-0), which is the OR of the I/O address FDF2 from the Address Decode and the DMA Control WRITE pulse, enables the Read DMA Data Register to accept DMA data. When the Plotter is initially turned on, the 6800 Processor writes DMA address instructions into the Read DMA Data Register and the 8X300 reads these locations to organize the Plotter's operating parameters. Some of these instructions include pen pressure and velocity table locations stored in the 6800 system ROM or the first address of the circular queue in the 6800 system RAM.

Whenever the joystick is used to move the pen carriage, the Vector Generator sends pen location updates as DMA data to the 6800 system. To do this, a DMAW-1 signal from the DMA Control Port causes the DMA Control section to generate a DMA request (following normal protocol) to the 6800 DMA Controller. After the Vector Generator's DMA Control section gains access to the bus, a buffer inverts the DMA data, which consists of pen position bytes. DATEN-0 then enables the Write DMA Data Register to output the data onto the bus.

DMA Control Port Registers. The second group of registers in the left memory bank is the DMA Control Port. The DMA Control Port determines which type of DMA is to be used in setting up addresses on the 6800 system address bus. For example, if the 8X300 wants data for pen velocities or pressures from various locations in the Plotter memory system, the General Purpose (GP) DMA Address Registers are enabled. The addresses that the GP DMA Address Register uses to access this data were sent to the Vector Generator from the 6800 Processor during the initial Plotter power-up sequence. If, on the other hand, the Vector Generator needs motor rotational information or pen selection data, an Auto Increment DMA is used (described next). To determine which DMA method is used, the DMA Control Port causes either the GP Address Register or the Auto Increment DMA Address Register to output the address onto the bus address lines. The DMA Control Port sends either DMAD1-0 to enable the GP DMA Address Register or DMAD0-0 to enable the Auto Increment DMA Address Register. The 8X300 firmware generates these signals.

When the DMA Address is placed in either the GP DMA Address Register or the Auto Increment DMA Register, the DMA Control Port sends DMAW-1. DMAW-1 notifies the DMA Control to observe normal DMA protocol (this handshaking procedure is described earlier under Bus DMA Operation).

The DMA Control Port generates three other signals which inform the 6800 Processor of the Vector Generator's current operational state. These are SETTC, SETMS, and SETER. Each signal generates an interrupt through U20 and J5 to the Processor.

- SETTC (task complete) is issued when the 8X300 has finished its last task.
- SETMS (motion synchronization) is used to inform the 6800 of its progress through a series of commands. From time to time, the 6800 injects synchronization markers throughout the circular queue; each time the 8X300 encounters one of these, it interrupts the 6800 Processor. For example, these markers are used to tell the Processor to turn on the other pen select light when the 8X300 has completed all of the tasks with the first pen.
- SETER (error) is generated if an error is encountered, to tell the 6800 Processor of the error condition.

Auto Increment DMA Address Register. The Auto Increment DMA Address Register (shown in Schematic 6-4) consists of an address register and a 64-step counter. This circuit is used to sequentially access each address of the 64-byte circular queue in the 6800 system RAM. The Auto Increment DMA Address Register is enabled by DMAD0-0 from the DMA Control Port. The counter is counting LEFT WRITE 2 (LW2-0) pulses — the write commands from the 8X300 microprocessor — via the I/O Address Decode circuit. Later, as each received DMA character is written into a memory location, the 64-step counter is automatically incremented by one. At the same time, the DMA Control Port asserts DMAW-1, which causes the DMA Control to follow normal DMA handshaking protocol to gain access to the 6800 bus for one DMA character transfer. After the 8X300 has read and filed the DMA byte away, the 64-step counter is again incremented by one and the whole process is repeated during the next Phase 1 clock period.

The signal lines QPT1-1 through QPT5-1 are used to inform the 6800 Processor at which address in the circular queue the 8X300 is currently obtaining DMA data. This prevents the Processor from placing data in the circular queue beyond the location where the Vector Generator is currently obtaining data.

Joystick, Integration Clock, and Limit Switch Registers. The Joystick, Integration Clock, and Limit Switch registers form the interface between the Joystick Rate Generator and the Motor Pen Drive module, both described later. The joystick's XRATE and YRATE signals are read by the 8X300 and are used for joystick-controlled movements of the pen carriage. These signals, along with INTEGRATION CLOCK (INTCK-1, which is BCLK-1 from the Motor Pen Drive module divided by 56), generate the motor speed and pen pressure commands for manual pen carriage movements.

During initial power-up, the pen carriage is moved to the upper right corner of the platen until the X, X', and Y limit photodetectors output X, X', and YLIM-1 signals. These signals are used to inform the Vector Generator where the pen carriage is during this referencing period. After that, the Vector Generator maintains pen carriage status by writing into the left bank memory. Anytime a LIM-1 signal is asserted, which occurs when the pen carriage has reached the edge or a corner of the platen, the respective axis motor is stopped.

Interrupt Flags. The Interrupt Flags circuitry (shown in Schematic 6-2) multiplexes the interrupt from either the front panel interface (FPINT-0) or the Motion Generation Interface (SETTC, SETMC, or SETER). This circuitry then outputs IRQ-0 to the Processor at the proper count of the IRP0-1 through IRP2-1 lines.

DMA Control. The DMA Control circuit interfaces to the Processor's DMA Bus Control when transferring data from the circular queue to the Vector Generator. Refer to DMA Bus Control (in the Processor Functional Block discussion) for a description of the handshaking between the two DMA Controls during DMA character transfers.

Vector Control. The Vector Control circuit (shown in Schematic 6-2) determines whether the Vector Generator will function as a "normal" Vector Generator or whether it will perform a diagnostics test for troubleshooting. TST0-1 through TST2-1 (originating from the Parameter Entry) determine this.

When operating as a "normal" Vector Generator, MOTEN-0, BUSEN-0, and HVON-0 are generated to enable other Plotter circuits. MOTEN-0 starts the 8X300, enables the DMA Control Port, and enables the Motor Pen Drive to accept data from the Vector Generator. BUSEN-0 enables the DMA Control Port to decide which DMA access process (GP or Auto Increment) will be performed. HVON-0 is used by the Motor Pen Drive functional block to turn on the high voltage, electrostatic paper hold-down circuit.

Motor Pen Drive

The Motor Pen Drive functional block converts digital data from the Vector Generator to dc currents for the pen solenoids and ac analog signals for the Plotter's three split-phase synchronous ac motors (X,X', and Y-axes). Two of the motors, the X and X', work in tandem to move the pen carriage in the X-axis direction. (However, these motors are electrically and mechanically separated from each other.) The third motor, the Y, is used to move the pen carriage in the Y-axis direction. Figure 3-15 is a block diagram of the overall electronic circuitry of the Motor Pen Drive.

The Motor Pen Drive circuit functionally and electrically attaches to the Vector Generator. This means that the Motor Pen Drive circuit receives all pen movement commands from the Vector Generator. Figure 3-1 shows the relationship of the Motor Pen Drive to the rest of the Plotter.

Motor Pen Drive Operation Sequence

The Vector Generator sends a series of four digital eight-bit bytes containing motor speed and direction information. Three bytes provide motor rotational data — one for each motor. The fourth byte contains information for the active pen's pressure against the paper. The three motor bytes are addresses for the Motor Pen Drive Sine/Cosine ROM. This ROM contains 128 haversine and 128 havercosine values in digital form. If each haversine in the ROM is addressed in sequence, the output consists of the digital values for a 360° haversine with 128 points (a point for every 2.8125°). In a similar manner, if each havercosine is addressed in sequence, the output consists of the digital values for a 128 point, 360° havercosine waveform. The digital haversine/havercosine values from the Sine/Cosine ROM are converted to analog signals by the Digital-to-Analog Converter. This results in a 128-step analog haversine or havercosine waveform.

To convert the four digital bytes from the Vector Generator to haversine or havercosine analog waveforms, a sequence of seven conversion cycles is required. The three eight-bit bytes carrying motor rotational information undergo two conversion cycles each, while the fourth pen pressure byte is converted in a single cycle. One of the two conversion cycles for each motor byte yields a haversine analog voltage for one motor winding; the other conversion cycle yields the havercosine analog voltage for the other motor winding. This means that one winding of a motor is driven by a sine wave signal (the eventual signal from the Motor Drive Amplifiers), while the other motor winding is driven by a cosine wave signal. The seven conversion cycles are listed in order:

Y Motor Phase B (Y Cosine)
Pen Pressure
X Motor Phase A (X Sine)
X Motor Phase B (X Cosine)
X' Motor Phase A (X' Sine)
X' Motor Phase B (X' Cosine)
Y Motor Phase A (Y Sine)

The Vector Generator sends one data byte every 4.32 μs. This means that each of the seven conversion cycles requires 2.16 μs. Notice that the pen pressure byte, which undergoes only one conversion, is also present for 4.32 μs.

The Sequence Control Circuit (see Figure 3-15) controls the transmission of the four bytes from the Vector Generator through the digital-to-analog conversion process to the respective motor winding (or the Pen Activation Drive). Sequence Control generates the control lines S0-1, S1-1, and S2-1. These lines perform the following functions:

1. Interrogate the Vector Generator's registers for each digital data byte.
2. Cause the Sign Latch to separate and store Bit 7 from each byte. Later, Sign Latch sends Bit 7 to its respective Motor Drive Amplifier or the Pen Activation Drive.
3. Direct the Analog Demultiplexer to produce haversine/havercosine signals for the Sample Buffers.

In processing the four data bytes from the Vector Generator, the three motor bytes are routed through the Sine/Cosine ROM, while the pen byte is routed around the ROM and through the Buffer. T2 from the Sequence Control controls this routing process.

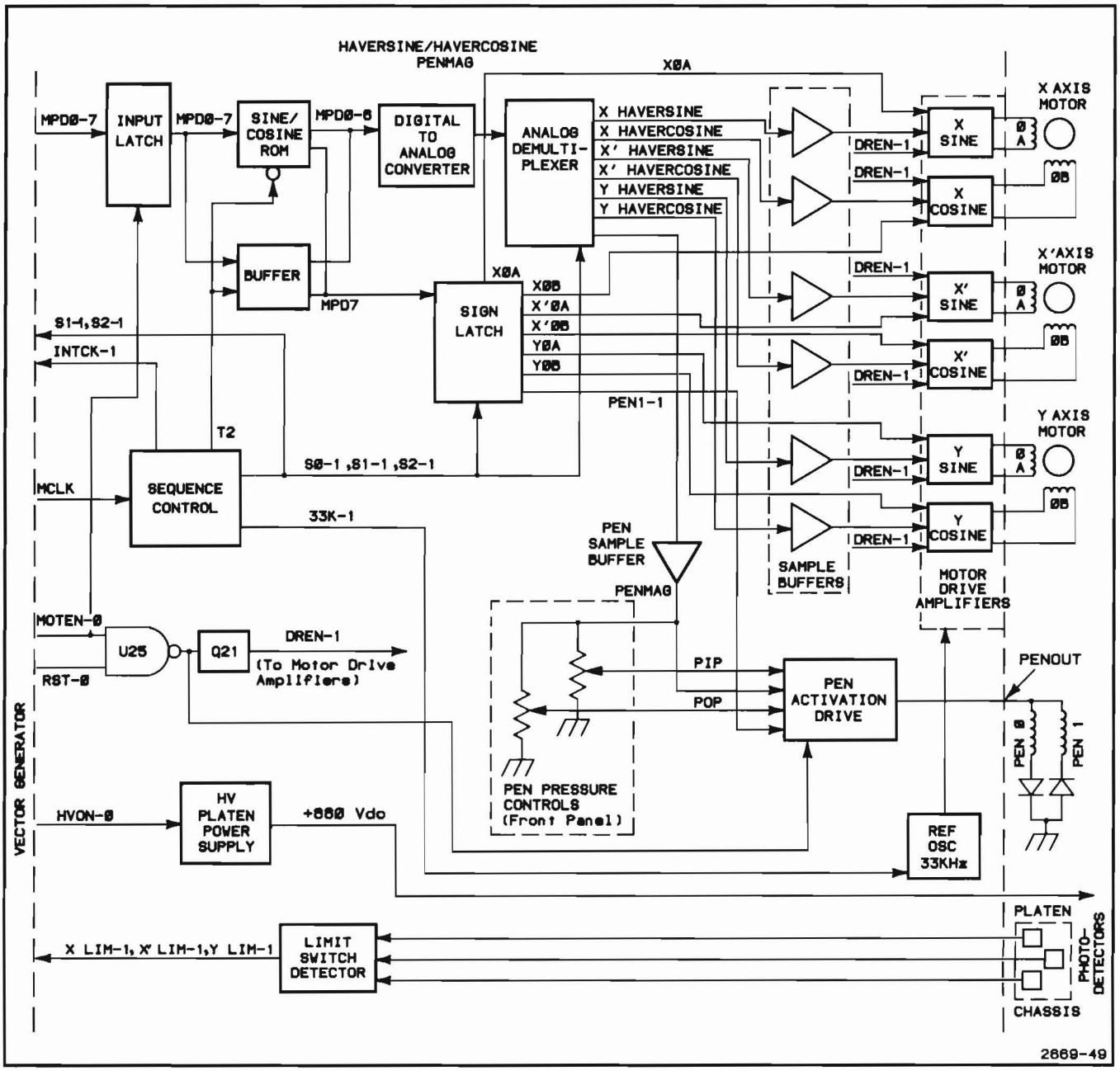

Figure 3-15. Motor Pen Drive Block Diagram.

The Sample Buffers use a capacitor to sample and hold the input signal until the winding or pen solenoid is addressed again with a new data byte 17.28 μs later. From the Sample Buffers, the haversine/havercosine signal goes to the Motor Drive Amplifier, which consists of a bridge amplifier for each motor winding. This bridge amplifier is composed of two identical amplifiers "back-to-back." One side of the bridge amplifier conducts while the other half is shut off and bypassed. Bit 7 (the steering bit stored in the Sign Latch) is used to alternately turn on or off the respective sides of the bridge amplifier each time the haversine/havercosine goes to zero. This effectively creates a bi-polar sine/cosine signal by causing the current flow to the motor winding to reverse every 180° (see Figure 3-16).

Each complete 128-step sine or cosine waveform applied to the motor winding moves the motor armature shaft 7.2°. Fifty complete sine or cosine cycles (a total of 6400 addresses) are necessary for one complete motor armature revolution.

Each digital data byte (with Bit 7 removed for current direction control) assigns one sine value to one motor winding and one cosine value to the other motor winding. After processing by the Digital-to-Analog Converter, this sequential series of 128 analog voltage levels forms a 360° haversine or havercosine waveform signal to the respective Motor Drive Amplifier. Notice that from Figure 3-15, the haversine signal is applied to one motor's drive amplifier, while the havercosine signal is applied to the other motor's drive amplifier. Also notice that the Pen Activation Drive does not receive a 128-step sine or cosine waveform because the data bytes containing pen pressure information bypass the Sine/Cosine ROM and are converted to a constant dc voltage. This dc voltage level is then applied to a coil in the pen solenoid to pull the pen down against the paper with a force proportional to the amount of current directed.

Bit 7 affects the Pen Activation Drive in a similar manner as the Motor Drive Amplifiers. While each pen solenoid has a diode in series with it, the two diodes are reversed from each other. This causes current to flow from the Pen Activation Drive through Pen 1 (activating that solenoid) but not through Pen 2. If the current flows in the other direction, Pen 2 will be activated. As with the Motor Pen Drive Amplifiers, Bit 7 controls the Pen Activation Drive to select the polarity of its amplifier.

The three pen drive motors are turned on and off with a comparative switch. The output of a Sample Buffer is compared to a feedback voltage developed by the motor current through a series resistor. When the Sample Buffer output voltage is greater than that of the feedback voltage, the amplifier is turned on, starting the motor. Later, when the feedback voltage across this resistor equals (or exceeds) the Sample Buffer output, the amplifier shuts off and the motor stops.

Following is a detailed description of each of the functional blocks shown in Figure 3-15.

Input Latch. The Input Latch (shown in Schematic 7-1) holds each byte of incoming MOTOR PEN DATA (MPD0-7) from the Vector Generator for 4.32 μs during the digital-to-analog conversion process. This ensures that static data can be accessed repeatedly throughout the multi-step conversion process.

Sine/Cosine ROM. The Sine/Cosine ROM (shown in Schematic 7-1) assigns both a haversine value and a havercosine value to the Input Latch byte from the Vector Generator. These haversine and havercosine values correspond to the phase angle or position of one of the three pen drive motors. Bit 7 is not used by this ROM. Instead, this bit is separated and sent to the Sign Latch to be used in the current steering circuitry of the Sample Buffers and the Motor Drive Amplifiers.

Each motor byte is assigned a corresponding sine and cosine value with the Sine/Cosine ROM. However, the pen pressure byte, which is the second conversion in the sequence of seven conversion cycles, is routed through the Buffer. T2 from the Sequence Control enables the pen data to be transferred to the Digital-to-Analog Converter.

Buffer. The Buffer (shown in Schematic 7-1) transfers MPD0-7 data from the Input Latch to the Digital-to-Analog Converter whenever the MPD0-7 contains pen data (rather than Motor Pen Drive data). T2 from the Sequence Control section enables this buffer.

Digital-to-Analog Converter. The Digital-to-Analog Converter (Schematic 7-2) converts the haversine/havercosine data from the Sine/Cosine ROM or the pen information from the Buffer into an analog magnitude signal. This analog output signal is a positive-going haversine or havercosine signal (unipolar) ranging from 0 V to about + 8 V. For pen information, the output is simply a positive magnitude that is proportional to the pressure and ranges from 0 V to + 8 V.

Analog Demultiplexer. The Analog Demultiplexer (Schematic 7-2) routes the analog signal to the respective Sample Buffer. The Analog Demultiplexer outputs consist of X motor haversine (TP 430) and havercosine (TP 440), X' motor haversine (TP 335) and havercosine (TP 345), Y motor haversine (TP 330) and havercosine (TP 340), and PENMAG (TP 230). The signals S0-1 through S2-1 control the routing and conversion of the four motor and pen data bytes.

Sequence Control. Sequence Control (shown in Schematic 7-1) acts as the master synchronization control for the conversion of the digital data bytes to analog ac signals for the motor pen and pen activation drive amplifiers. Sequence Control generates three signals that permit the Vector Generator to multiplex four bytes in the proper sequence and transmit them to the Motor Pen Drive where they are demultiplexed and routed to their respective destinations. Specifically, Sequence Control counts in binary on the signal lines S0-1 through S2-1. A new count occurs every 2.16 μs. MCK-1 (MOTION CLOCK) from the Vector Generator provides the clock for this binary counter.

Sign Latch. The Sign Latch (shown in Schematic 7-1) is an eight-bit latch that is used to store Bit 7 from each data byte in the four-byte sequence. Later, as each motor phase or pen pressure byte is converted to an analog signal, Bit 7 enables one side of the respective Motor Drive Amplifier or the Pen Activation Drive. This means that this bit then (1) controls the direction of the current flow in the two motor coil windings or (2) determines which pen is active by controlling the direction of current flow through the pen coils (via PEN1-1).

Sample Buffers. The Sample Buffers (shown in Schematic 7-2) provide a unit gain isolation between the Analog Demultiplexer and the Motor Drive Amplifiers. A .001 μF capacitor on the input acts as a sampling capacitor and holds the input signal constant until the Analog Demultiplexer can output another signal level 17.28 μs later.

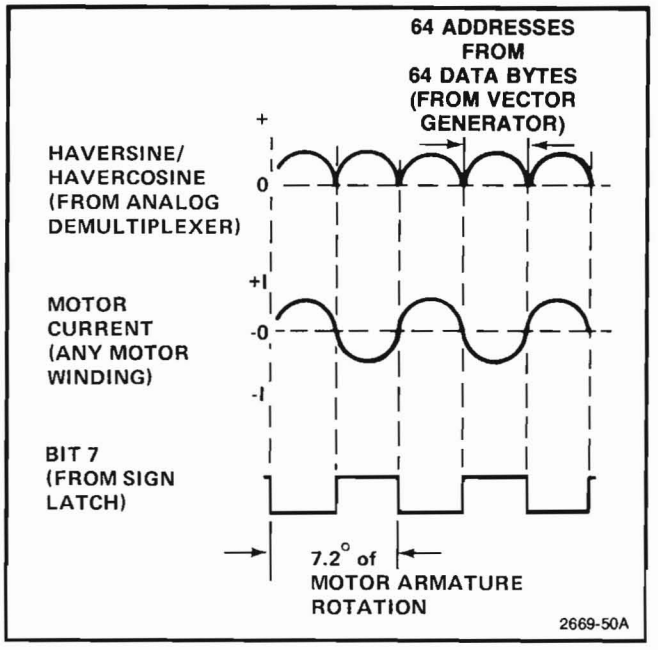

Figure 3-16. Motor Drive Amplifier Signals.

Motor Pen Drive Amplifiers. The six Motor Pen Drive Amplifiers (Schematic 7-3) used in the Plotter are switching bi-polar bridge amplifiers. These amplifiers generate a pulse-width modulated ac signal to the motor coil windings. Each amplifier drives one of the two windings in a motor and is composed of two identical halves. Only one half can be turned on and active while the other is turned off and bypassed for alternate haversines/havercosines. Later, when the haversine/havercosine signal switches to the second half of its 360° cycle, the two amplifier halves reverse their roles. Bit 7 from the Sign Latch is used to turn on or off the proper amplifier halves.

To examine the operation of the Motor Pen Drive Amplifiers, look at the Phase B windings of the Y motor amplifier as an example. If Bit 7 from the Sign Latch is high (Q1 at Pin 5 of U125), the TTL high at Pin 1 of U61 and the complementary TTL low at Pin 1 of U165 causes the amplifier half composed of Q71, 72, 170, and 171 to become active. The other half, composed of Q75, 76, 174, and 175, becomes inactive. This means that there is an electron current flow from the Y phase BL signal line through the phase B winding of the Y-axis motor and back into the Y phase BL signal line. On the other hand, if Bit 7 from the Sign Latch is low (which it is on the second half of the sine wave), the two amplifier halves exchange roles and the current flow through the phase B windings of the Y-axis motor is reversed.

The motors are turned on and off using a comparative switch. The Sample Buffers' output (current reference input to the Motor Drive Amplifiers) is compared to the feedback voltage developed in the amplifier. This feedback voltage is developed across R164 in the case of the phase B winding amplifier of the Y-axis motor. Whenever there is a difference in the input voltage to the Motor Drive Amplifier and the feedback voltage, the comparator (U161) and Bit 7 from the Sign Latch turn on the respective Motor Pen Drive Amplifier. Later, when the feedback voltage from the energized amplifier equals (or exceeds) the input voltage, the amplifier shuts off. When the feedback voltage from the now de-energized amplifier falls below the input voltage, the amplifier is again turned on.

Reference Oscillator. To control the frequency of motor turn-on and turn-off, a 33 kHz Reference Oscillator (Q234 and Q242 in Schematic 7-2) is used. This oscillator prevents the motor turn-on and turn-off frequency from exceeding 33 kHz. The saw-tooth signal from the 33 kHz Reference Oscillator is coupled to the Sample Buffer output and fed into the comparator, which compares the output to the feedback voltage. The waveforms of the comparator inputs are shown in Figure 3-17.

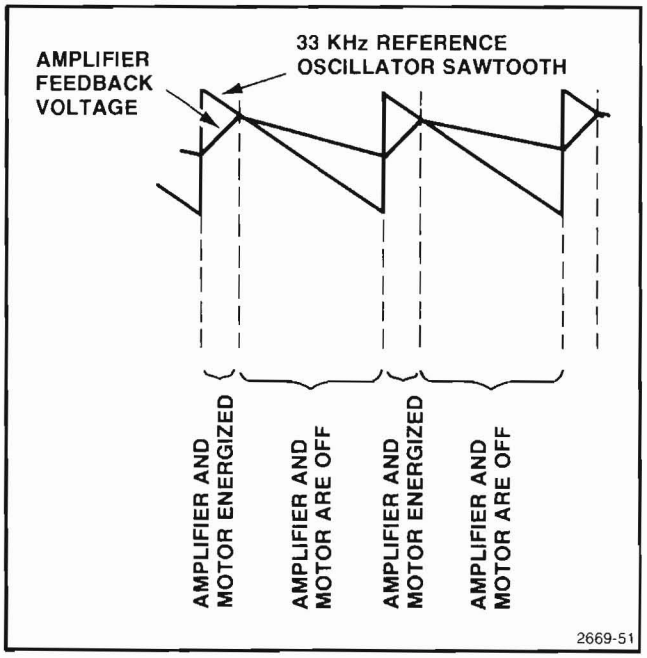

Figure 3-17. Motor Drive Amplifier Comparator Inputs.

Pen Activation Drive. The Pen Activation Drive (shown in Schematic 7-4) provides the proper amount and direction of current to the active pen coil when the pen is down. One of the seven digital-to-analog conversion cycles discussed earlier consists of converting digital pen pressure data from the Vector Generator to an analog signal. This analog output from Pin 6 of the Op-Amp U235 is PENMAG and is applied to both inputs of an Op-Amp U191.

The operator can modify PENMAG for either pen slightly with two front panel adjustments: R1000 and R1003 of the PEN PRESSURE OVERRIDE. (See the description of the Front Panel Switches And Lights circuit later in this section.) The PEN PRESSURE OVERRIDE adjustments can vary the Plotter's range of pen pressures by about ± 25%. The wiper arms of these two potentiometer adjustments (R1000 and R1003) are PIP-A and POP-A and add to or subtract from the PENMAG op-amp input.

Earlier, Bit 7 was separated from the pen byte and now becomes PEN1-1 from the Sign Latch. PEN1-1 is used to determine which pen becomes the active pen by shorting the complementary PENMAG signal to ground. This is done by turning on either Q184 or Q185. Pen 1 is active whenever this signal is high. The op-amp then uses the resulting differences between the two PENMAG signals and outputs current through R183. Depending upon the relative amplitudes of these two PENMAG signals, the current source is from either the + 12 volt supply through R182 or the −12 volt supply through R194. If the current for the op-amp comes from the + 12 volt source, Q85 is turned on and electron current goes out through Pin 5 of J1 to activate Pen 1. The current returns via Pin 6 of J1. On the other hand, if the source current for the op-amp is the −12 volt scurce, Q95 is then turned on. The electron current is reversed, causing Pen 2 to be activated.

Limit Switch Detector. Three Limit Switch Detectors (shown in Schematic 7-4) are used in the initial power-up sequence. These detectors position the Plotter's pen in the upper right corner, ready for plotting, and initialize the Vector Generator. The Limit Switch Detectors consist of three phototransistors, three LEDs, and three U35 comparators. An LED-phototransistor combination is positioned at each right end of the X- and X'-axes and the upper end of the Y-axis.

When the Plotter's power is turned on, the pen carriage moves to the upper right corner of the platen. When the Y-axis arm and the pen carriage reach the end of their axes, where the photodetectors are located, a "knife-blade" interrupts the light path from the LED to the corresponding phototransistor. The comparator detects the cessation of conduction in the phototransistor and outputs a high on the corresponding X, X', or Y LIMIT-1 line to the Vector Generator. This output stops the corresponding axis motor drive amplifier and the motor. After all three motors have stopped and the three LIMIT-1 lines have gone high, the remainder of the power-up sequence is continued. The Vector Generator now knows the exact location of the pen carriage.

High Voltage Platen Power Source. The High Voltage Platen Power Source (shown in Schematic 7-1) places an electrostatic charge of approximately 880 V inside the platen. The electrostatic charge is used to attract and hold the paper against the platen when the Plotter is being used in SHEET mode. This circuit does not operate during ROLL mode in Option 36, if available.

After the paper has been changed and the MEDIA CHANGE button is pressed, the Vector Generator outputs HVON-0 to signal that the Motion Generation Interface is enabled. HVON-0 forward biases a blocking oscillator (Q490) and starts the oscillations at a rate of approximately 20-30 kHz. A feedback winding on the transformer, T480, maintains the oscillations by retriggering Q490 into conduction on each oscillation. The secondary windings of this transformer are rectified and filtered to form the dc electrostatic charge inside the platen. The platen looks electrically like four large capacitors in parallel with a bleeder resistor (R484 and R494). The reason for dividing the platen into four electrical areas is to minimize the shock hazard if the platen coating becomes severely damaged.

Front Panel Switches and Lights

The Front Panel Switches and Lights module (shown in Schematic 8-1) contains the front panel switch input circuitry (not including the Parameter Entry switch), as well as the display indicator lamps located in each switch. When a front panel switch is pressed, the Front Panel Switches and Lights module decodes the location of the switch and interrupts the Processor. The Processor, in its interrupt service routine, reads the switch location in a register on the Vector Generator to determine the switch's function. The Processor then refers to the system ROM memory for directions in carrying out the switch's function.

All of the front panel switches are wired in a scanned switch matrix. Each switch, which is a normally open, momentary SPST pushbutton, is located between a COLUMN signal line and a ROW signal line. Each COLUMN signal line is connected to the input of the Column Multiplexer (an eight-to-one multiplexer) and each ROW line is connected to the output of the Row Demultiplexer (a two-to-four demultiplexer). FPCLK-1 is divided until it is 1/2048 of BCK-0 and becomes the Row Demultiplexer input. This causes each ROW line to change to a TTL low in a sequential order such that three complete ROW scans take 13 ms. Any key closure, while its ROW line is being scanned and is low, couples a ROW-0 through the key switch and causes its corresponding COLUMN line to go low. The COLUMN lines form an input to the Column Multiplexer. If any of the column lines go low, a low is asserted on the output (Pin 5). This output is stored in the first stage of the Switch Register (a four-position shift register). The scanning then continues, and if that same switch is still closed for two more scan cycles, the output (now debounced) is gated out as SWITCH CHANGE (SWCHG-0). At the same time, the logical state of SWITCH POLARITY (SWPOL-1) is changed to indicate that the switch was pressed down or closed. The action of the circuit works in the same manner when a switch which had been closed is opened.

As each ROW line is scanned, its status is reflected in Switch Latch 2 (located on the Vector Generator, Schematic 6-1) through the lines SWPOS0-1 through SWPOS4-1. When a switch is pressed or released, the SWCHG-0 signal is used by the Vector Generator module to generate an interrupt which causes the Processor to stop and read the Switch Latch. The bit combination of the SWPOS0-1 through SWPOS4-1 and SWPOL-1 lines furnishes enough information for the Processor to determine which switch was pressed and whether it was opened or closed. Table 3-20 shows the addresses on the SWPOS signal lines for each switch. When the switch's status changes, the whole process is repeated for three scans. SWCHG-0 is output again and SWPOL-1 is changed to not true; another interrupt is sent to the Processor. The Processor then reads the interrupt in the same manner and sees that the switch's function is accomplished.

Table 3-20

FRONT PANEL SWITCH ADDRESSES

Switch Name	Switch Number	Address
SHIFT #2 (upper of two SHIFT switches)	S15	02
SHIFT #1 (lower of two SHIFT switches)	S105	01
INTERFACE (off-on line)	S211	04
INTERFACE (local/remote)	S215	05
RESET	S225	06
MEDIA	S231	07
PLOT CONTROL	S235	08
LOWER LEFT	S241	09
UPPER RIGHT	S245	0A
POINT	S255	0B
SELECT #1	S281	0E
PEN UP/DOWN	S291	0F
SELECT #2	S295	10

The keyboard switch circuit provides for two-key rollover. This permits a second front panel switch to be pressed or released before the Processor reads the first one. When this happens, the Vector Generator's Switch Change Logic asserts COUNTER DISABLE (CTRDIS-1). CTRDIS-1 stops the scanning process until the Processor can catch up.

Each pushbutton has an incandescent lamp inside. The pushing of a key does not, in itself, turn the lamp ON or OFF. Instead, the Processor causes the lamp to be lit or extinquished as a task in its interrupt routine. The Processor loads the lamp information as LTDATA-1 into the Parallel-In/Serial-Out Shift Register in the Vector Generator. LTDATA-1 is then clocked by LTCLK-1 into Lamp Register 1 (a serial-in, parallel-out shift register). While the lamp information is being shifted in, LTEN-1 goes false, turning off all of the lamps. After the data for all 8 lights has been loaded in Lamp Register 1, the process is repeated to load Lamp Register 2. After that, LTEN-1 goes true to enable the lamp-drivers and turn the lights back on.

The speaker, driven by a 1 kHz oscillator, is enabled by BELL-0. BELL-0 is asserted with such Plotter functions as Error and Point (digitizing the pen coordinates). The duration of the bell is controlled by the length of time BELL-0 is asserted by the Processor writing to address FDE3 in the Vector Generator.

Additionally, an analog voltage, PENMAG, comes from the Motor Pen Drive module through the Vector Generator to the Front Panel Switches and Lights section. This voltage is applied to the tops of two potentiometer controls (PEN PRESSURE OVERRIDE, R1000 and R1003) located on the front panel. The output voltage from the respective wiper arms is labeled PIP-A and POP-A. These two voltages add to or subtract from the PENMAG voltage on the pen lifter solenoids and are used as the operator's fine adjustment of the pen pressure.

Joystick Rate Generator

The Joystick Rate Generator (shown in Schematic 8-2) interfaces the joystick and the Plotter pen carriage or the Media Advance module (if Option 36 is installed). This means that the joystick can be used to manually move the pen carriage to a desired location on the platen surface or to manually move the paper (in either direction) across the platen.

The joystick consists of two potentiometers arranged perpendicular to each other with a common control. This control is oriented such that the pen moves in the same direction as the joystick's handle. (The paper moves in the same left-right manner as the joystick.) One potentiometer is used for Y-axis pen movement and the other potentiometer is used for X-axis pen movement. The Media Advance option uses only the X-axis potentiometer. Figure 3-18 shows the relationship of these two potentiometers.

The Joystick Rate Generator converts the two wiper arm dc analog voltages (XJOY and YJOY) into digital signals (XRATE, YRATE). The frequency of these signals is directly related to the magnitude of XJOY and YJOY. The Vector Generator then uses these digital signals to develop the necessary deflection signals for the Motor Pen Drive module to move the pens or for the Media Advance option to move the paper.

Since both axes are identical in operation, only the X-axis is described in detail here. The Y-axis is the same, except that its wiper-arm voltage is YJOY.

The analog wiper-arm (XJOY) is integrated by a resistor-capacitor combination, R91 and C91, to produce either a positive or negative ramp voltage which is applied to both a Positive and a Negative Ramp Detector. The ramp voltage produced corresponds to the joystick position. A positive-going ramp indicates a right movement of the pen (X-axis) or an up movement of the pen (Y-axis). When the ramp voltage becomes 100 mV greater than (or less than, in the case of negative-going ramps) Vref, which is approximately .320 V set by a resistor voltage divider, the corresponding Detector's output goes high. This signal is sent to two locations, both of which are inputs to flip-flops. One of these flip-flops is a D type and the other is a J-K type. Both flip-flops are clocked by RATE CLOCK (RATCLK-1), which is a 1/32 division of the bus clock (BCK-0). The clocked output from the D type flip-flop (U71) is a series of pulses, X or YRATE-0. The output X or YRATE-0 signal is used by the Vector Generator's Joystick, Integration Clock, and Limit Switch Interface to determine the speed and the distance that the pen must be moved. X or YRATE is also used to turn on the analog switches used to discharge the integrating capacitor back to Vref. This causes the Ramp Detector to switch to a low output, and with the next clock pulse, the D type flip-flop is reset. If the joystick is still deflected, the process is repeated. Therefore, the output (X or YRATE-0) is a series of pulses which have a frequency dependent upon the rate of the voltage increase (ramp), which in turn is directly proportional to the analog voltage (X or YJOY) and the RATCLK-1 frequency.

The second flip-flop to which the Ramp Detector's output is connected is a J-K flip-flop (U171). The output (XPLUS-1) of this flip-flop is used by the Vector Generator's Joystick, Integration Clock, and Limit Switch Interface to determine the direction of the pen movement. When the joystick is moved either up (Y-axis) or to the right (X-axis), the Positive Ramp Detector outputs a positive signal. This signal is input to the J input, while the K input is kept low. With the next RATCLK-1 clock pulse's positive-going edge, the Q output (X or YPLUS-1) asserts a TTL high. XPLUS-1 causes the pen drive motors to move the pen to the right, if the joystick is exercised in the X-axis direction, or up, if the joystick is moved in the positive Y-axis direction.

Conversely, if the joystick is moved either down (Y-axis) or to the left (X-axis), the Negative Ramp Detector outputs a positive signal. This signal becomes the input to the K side of the flip-flop (U171), while the J input is kept low. On the next positive going edge of a RATCLK-1 pulse, the Q output (X or YPLUS-1) asserts a TTL low. This low on XPLUS-1 causes the pen drive motors to move the pen to the left (for X-axis joystick control) or down (if the joystick is moved in the negative Y-axis direction).

XPLUS-1 and XRATE-0 are also sent through the Vector Generator and onto the Plotter bus. These signals are used by the Media Advance option, if installed. In this case, the joystick is used to control the advance of paper across the Plotter's platen.

Also located in the analog comparator input circuit is a waveshaping circuit which attenuates in a non-linear fashion the ramp voltage to the integrator. This permits fine resolution with reasonable joystick control deflections but still allows rapid pen movement with a substantial joystick control deflection.

BRST-0 (RESET) is used to close the analog switches (U191) which discharge the integrators to Vref. This prevents any pen movement which would be generated by a joystick control deflection during Plotter power-up.

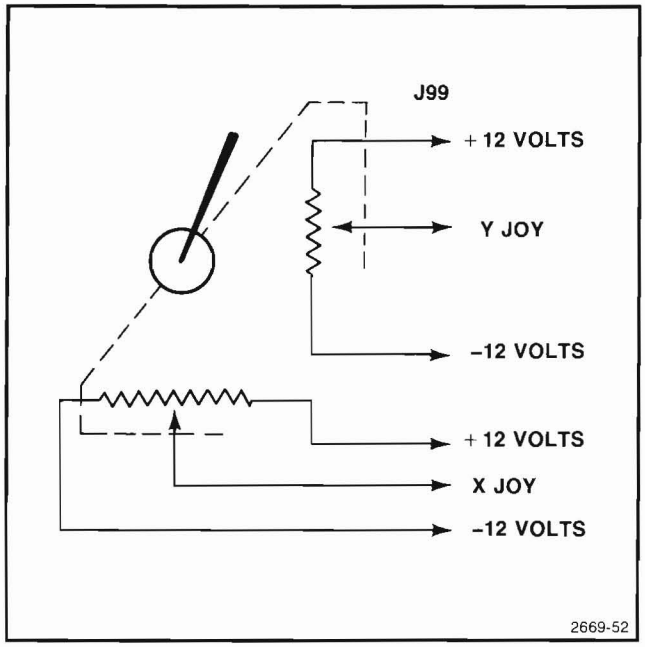

Figure 3-18. Joystick Connection.

Power Supply

The Power Supply (shown in Schematic 9-1) provides all of the electrical power for the 4663 Plotter. Except for the cooling fan and the three pen drive motors, all power is distributed to the Plotter's major functional blocks (circuit boards) via the backplane. A 20-pin connector/cable assembly transfers power from the power supply to the backplane through J101. The corresponding backplane connector is J9.

General Power Supply Operation

The 4663 Power Supply uses a switching, or "chopping" method of regulating its output voltage. Refer to Figure 3-19, which is a simplified block diagram of the entire power supply, and to Figure 3-20. The chopper (the switching transistor section) functions like a switch, sending current through the primary windings of a transformer (T251) first in one direction and then in the other direction. This causes the secondary windings to produce a pulse-width modulated square-wave signal which is rectified and filtered with a choke-input smoothing filter.

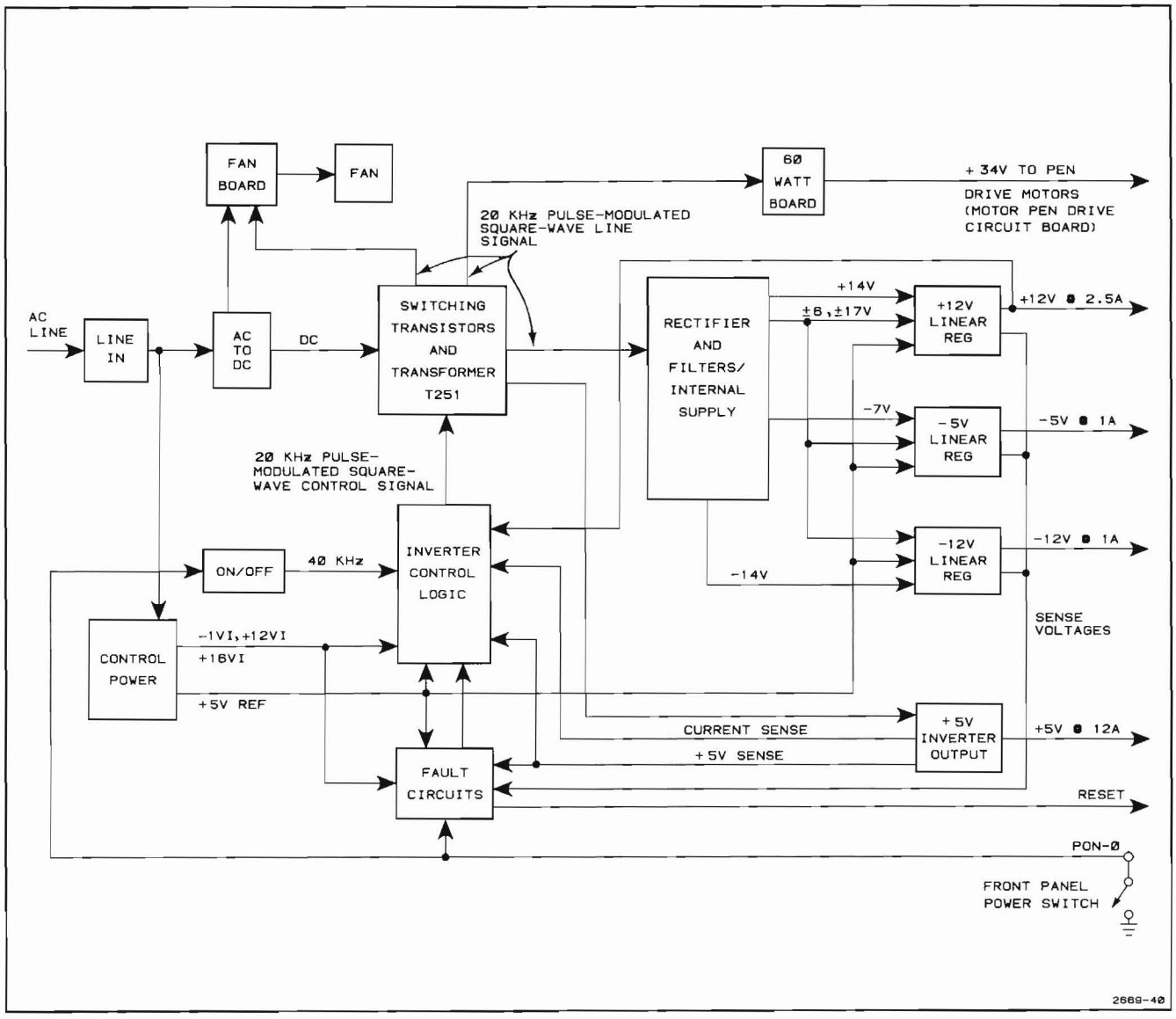

Figure 3-19. Power Supply Block Diagram.

The + 5 Vdc output of the filter is kept constant by varying the duration of the pulses from the switching transistor section. This means that if the output voltage starts to rise, the switching transistors are simply turned on for shorter periods of time; if the output voltage starts to fall (if the load increases, for example), the switching transistors are turned on for longer periods of time. The control of the switching transistors' "on-time" is the responsibility of the Inverter Control Logic circuit. This circuit controls the switching transistors by using three signals. The first is from a 40 kHz oscillator within the On-Off circuit. The second is a sample of the + 5 V output (+ 5 V sense), and the third is a + 5 V reference voltage from the Control Power section which is compared to the + 5 V output supply. Since all three signals are interrelated, they are discussed together in the following paragraphs.

On every other negative pulse from the oscillator, the Inverter Control Logic permits current to flow through one half of the primary windings of a switching transistor base drive transformer (T161). With the first pulse, either transformer primary may conduct; thereafter, the Inverter Control Logic only permits each half of the primary transformer winding to conduct on alternate oscillator cycles. Pin 2 is the common connection. The current conduction in one half of the primary windings turns on the corresponding switching transistor (Q261 or Q271). This switching transistor, in turn, supplies current to the primary winding of the large power transformer (T251). Then, on the next oscillator cycle, the other half of the T161 primary conducts, causing the other switching transistor to turn on, completing the cycle. This results in a 20 kHz positive- and negative-going square-wave signal on the secondary of T251.

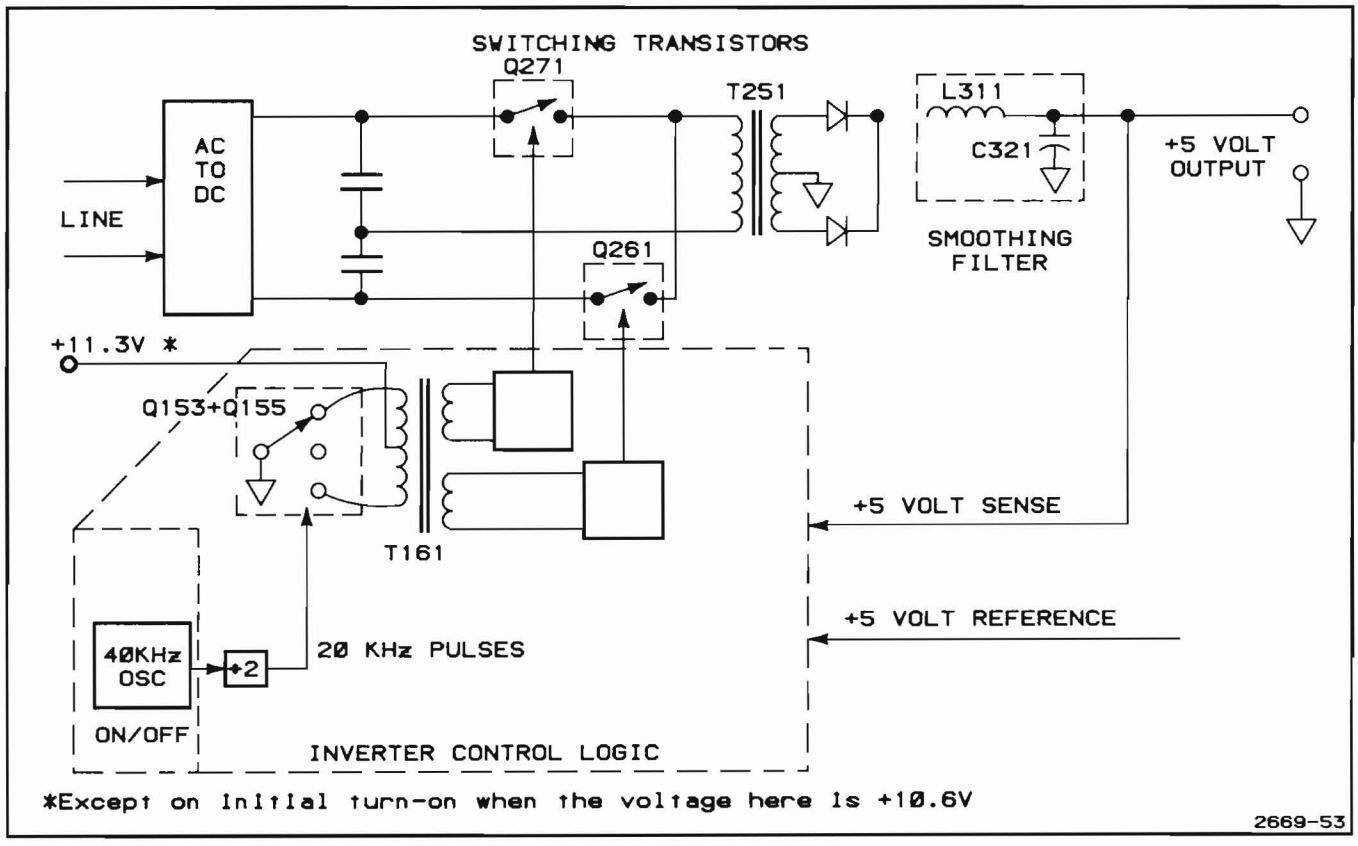

Figure 3-20. +5 V Power Supply Regulation.

As long as either switching transistor is turned on, a rectified dc pulse is introduced to the input smoothing filter in the + 5 V supply section, the Rectifiers/Filters and Internal Supply section, and the 60 Watt Aux board. This pulse causes a filter capacitor (C321) to charge, producing an increasing voltage on the + 5 V supply's output. The Inverter Control Logic monitors this increasing voltage (with the 5 V sense line) and compares it to the reference voltage. When the output reaches the reference voltage, the Inverter Control Logic circuitry turns off the conducting switching transistor. This naturally shuts off the dc pulse at the smoothing filter's input, and the + 5 V supply output starts to decay (the rate depends upon the load). The decay continues until the next pulse from the divide-by-two circuit causes the Inverter Control Logic to turn the opposite switching transistor on. Now the current flow in the primary winding of T251 is in the opposite direction. However, the full-wave rectifier in the + 5 V Inverter output rectifies this as a positive pulse, and starts charging C321 again, and the process is repeated.

The −5, −12, and + 12 V power supply outputs are produced from separate windings on the main transformer (T251). The current from each winding is rectified, filtered, and regulated (described later).

The following paragraphs describe each functional block of the 4663 Power Supply shown in Figure 3-19.

Line In

When the ac line cord is connected to both a source and J1001, the entire primary circuit (up to the two switching transistors Q261 and Q271) remains energized at all times regardless of the status of the Plotter's POWER switch. The POWER switch is a logic function, PON-0, and enables the U41B oscillator when grounded. T61 provides continuous power to the control power section as long as the line cord is plugged in. SW1001, the line voltage selector switch, rearranges the circuitry to permit 220 V to be applied to T61 and the ac-to-dc section when operating with Option 48. RT71 and RT181 act as surge current limiting resistors.

Two spark gaps (E81 and E82) provide overvoltage protection in case the instrument is accidently plugged into a 230 V source when the input power selection switch is set for 115 V.

Some early Plotters used a triac (Q81) as a line switch. Turning on the front panel switch (grounding PON-0) turns on the triac switch.

Ac-to-Dc

The ac-to-dc section uses a full-wave bridge rectifier to convert the ac line voltage to dc. If SW1001 (the 115-230 V selection switch) is set for 115 V operation, the rectifiers and capacitors C362 and C371 form a voltage doubling circuit. This results in approximately 300 Vdc across these two capacitors. On the other hand, if the incoming line voltage is 230 Vac and the switch is properly set, the voltage doubling circuit is eliminated. In this case, the 230 Vac line voltage is full-wave bridge rectified and 300 V appears across C362 and C371. T381 and associated circuitry perform EMI filtering.

Control Power Supply

The Control Power Section is used to provide −1, + 12, and + 16 V to power the logic circuits in the Inverter Control Logic and Fault Circuit sections, as well as to provide base drive for the switching transistors. This section also provides the + 5 V reference which is used by each of the output regulators as a comparison for correction.

Inverter Control Logic/On-Off

The Inverter Control Logic controls the switching transistors Q261 and Q271. The key to the operation of the Inverter Control Logic is an oscillator (U41B, in the On-Off section). The frequency of this oscillator is controlled by C42. C42 is allowed to charge and discharge at separate rates, giving a 40 kHz square-wave signal shown in Figure 3-21. This output is used to control the switching transistors. When the oscillator's output goes high, the NOR logic (U151A, B, and C) turns off Q51, Q152, and the two switching transistors. At the same time, Q151 is turned on, shorting the transformer T161 primary. Later, when the oscillator's output goes low, one of the two transistors (Q51 or Q152) turns on, energizing one half of the T161 primary. These two transistors are forward-biased on alternate oscillator cycles by U142B, a divide-by-two circuit. Energizing one half of the T161 primary turns on the corresponding switching transistor. Later, when the oscillator's output goes high again, that switching transistor and its corresponding transformer primary-driving transistor shut off. The cycle is completed when the oscillator's output goes low again. This time the opposite transistor driving the transformer primary winding turns on, energizing the other half of the primary winding of T161. This, in turn, forward biases the opposite switching transistor (which was turned off during the previous oscillator cycle).

The on-time of the base drive transistors (either Q51 or Q152) and their associated switching transistors is also dependent upon the condition of two + 5 V output signals (the + 5 V sense and the output current), the fault circuitry, and the + 5 V reference. Two comparators, U211A and B, monitor the voltage on the regulated + 5 V Inverter output and the current drawn from the + 5 V regulated supply. If either is excessive, the comparator's output turns off the switching transistors through their respective base drive transistors. This is accomplished with the Inverter gate, U141D. An intentional characteristic of the + 5 V Inverter's output is that it has a 40 kHz ripple, and the input to these comparators rises and falls in step with this ripple frequency. Q211 and Q212 form a constant current ramp generator and use the inverted output from the 40 kHz oscillator (U41B) to generate a saw-tooth ramp voltage. This ramp voltage (see Figure 3-21) is added to and subtracted from the + 5 V reference voltage at the inputs to the over-current and voltage sensing comparators (U211A and B). This ensures that the + 5 V output voltage and its ripple rises and falls in step with the oscillator. If the output ripple frequency should change and get out of step with the oscillator frequency, the comparator (U211A) detects a voltage difference and turns off the switching transistors until the next oscillator pulse.

If any of the output regulators (+ 12, −12, + 5, and −5 V) fail and the voltage changes appreciably, the fault circuitry (described later) through U141C turns off the switching transistors until the next fault oscillator pulse. However, a circuit not used in early model Plotters (consisting of U143C and D mounted on the Soft-Start circuit board and wired as a type of AND gate) remembers which switching transistor was last on. Later, when the fault circuit permits the normal switching process to continue, U143C and D automatically reverse the states of the switching transistors. This means that the switching transistor that was last on when the fault circuit detected a problem and stopped the switching process is switched off; the opposite switching transistor (which was previously off) is turned on when the fault circuit permits the power supply to operate normally. This prevents possible transformer saturation.

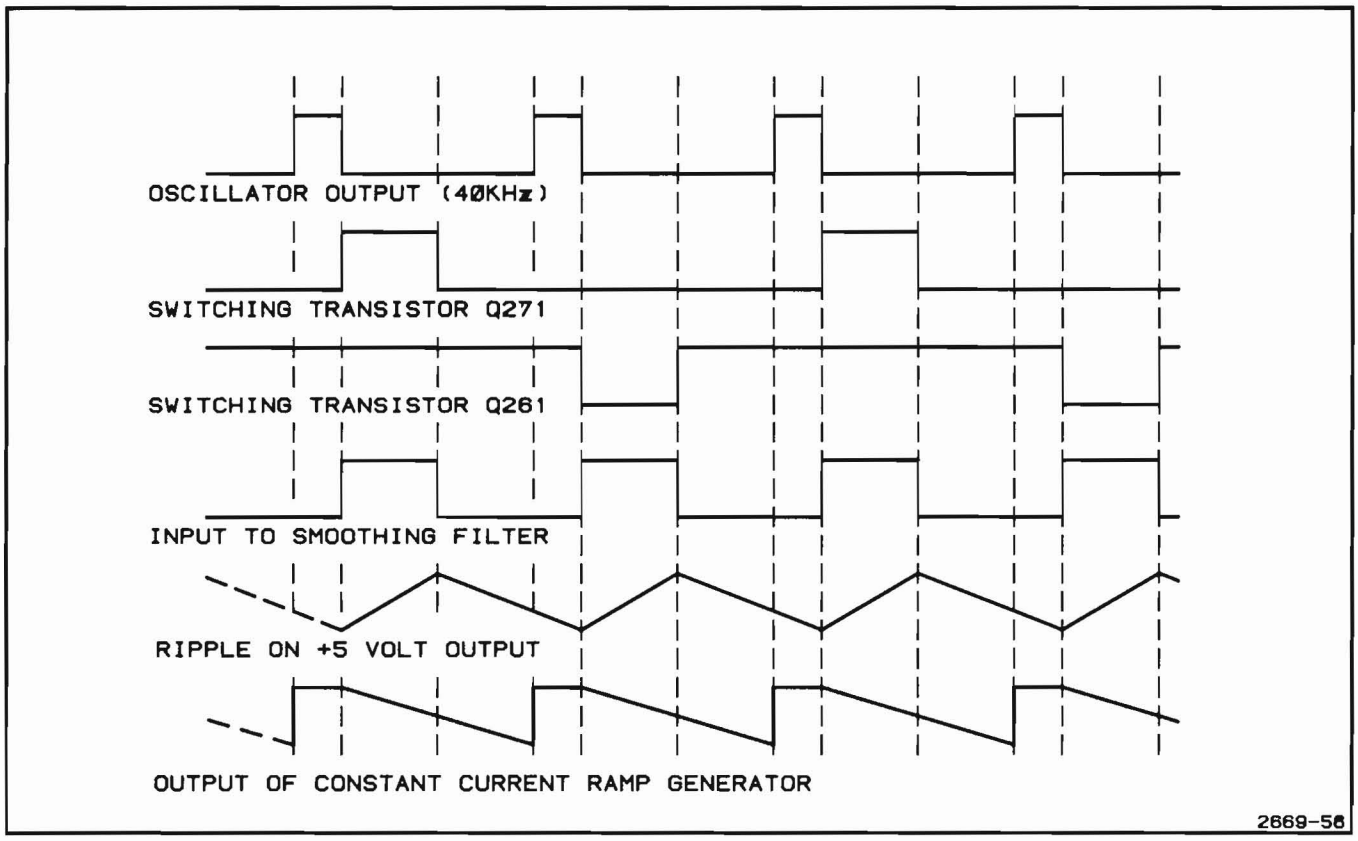

Figure 3-21. Power Supply Waveform Summary.

U143A, B, Q142, and Q143 (all mounted on the Soft-Start circuit board and not present in early model Plotters) form a "soft-start" circuit that allows the switching transistors to build up the output slowly. Q142, R47, and C45 produce a fast ramp sawtooth signal to U143A, while Q143, R49, and C44 produce a slow ramp sawtooth to the same comparator. The comparator output becomes the turn-on times for the switching transistors as shown in Figure 3-22. Notice that as the slow ramp increases, the switching transistor's on-time, represented by the width of the shaded areas, increases. Finally, when the slow ramp's level exceeds the peaks of the fast ramp, the on-time of the switching transistor is controlled normally by the sense and reference voltages, as described earlier.

Switching Transistors and Transformer

The switching transistors (Q261 and Q271) function as current switches, directing the 300 Vdc current through the transformer's (T251) primary first in one direction and then in the other. The switching transistors, which operate alternately from each other, are controlled by the Inverter Control logic section described earlier. Three transformer secondary windings supply power to the + 5 V Inverter output, the Rectifiers/Filters and Internal Supplies, and the 60 Watt Aux Board. The switching transistors also provide a small amount of current (at a 20 kHz rate) to the Fan circuit board to operate its internal + 28 V supply.

+5 V Inverter Output

The + 5 V Inverter output consists of one of the three secondary windings (Taps 21, 22, and 23) of transformer T251, a full-wave center-tapped rectifier, followed by a smoothing filter. The smoothing filter is composed of a series of inductors and a shunt capacitor. A zener diode (CR301) and an SCR (Q1001) provide "crowbar" protection for the 4663's logic circuitry by shorting the + 5 V supply to ground if the output voltage becomes excessive. A sample of this output voltage is sent to the Inverter Control Logic as the + 5 V sense to be compared to the + 5 V reference for regulation purposes. A comparator (U211B in the Inverter Control Logic) is connected across a 0.01Ω resistor (R311) on the ground line to the center tap of T251's secondary winding to detect excessive current from the + 5 V supply.

Rectifiers/Filters/Internal Supply

The Rectifiers, Filters, and Internal Supply section consists of the second of three T251 secondary windings (Taps 13 through 17) and the + 6, + 14, + 17, −6, −7, −14, and −17 V supplies for the + 12, −5, and −12 V linear regulators and the power supply's own internal circuitry. The various taps of this secondary winding feed full-wave rectifiers and LC smoothing filters in the case of the + 14, −7, and −14 V supplies. The + 17 and −17 V supplies obtain their power in a similar manner from taps on T251's secondary winding but use full-wave, center-tapped rectifiers followed by series regulators and filter capacitors to complete the + 17 and −17 V supplies. The + 6 and −6 V supplies obtain their power through 10 V zener diodes from the + 17 and −17 V supplies.

+12, −5, and −12 V Linear Regulators

The + 12, −5, and −12 V Linear Regulators supply three of the five voltages to the rest of the 4663 Plotter. (The + 5 V Inverter output and the + 32 V from the 60 W Aux circuit board are the fourth and fifth voltages.) Basically, each of these three series-pass regulators are the same and receive their power from the Rectifiers, Filters, and Internal Supply section; only the component values differ between these regulators. The B portions of U101, U121, and U111 perform as voltage regulators by comparing the sense voltage (a sample of the output) with a multiple of the + 5 V reference. The A portions of U101, U121, and U111 act as fold-back current limiters. They sense overcurrent situations across 0.1Ω current sensing resistors (R11, R25, and R16). If the current drawn exceeds the capacity of the individual supply, the A portion of the regulator takes over and folds the current back. This means that, as the voltage across the current sensing resistor increases or the voltage output decreases, the available current through the series-pass transistor is reduced.

Fault Circuit

The Fault Circuit detects failures in any of the four power supply outputs (+ 5, + 12, −5, and −12 V). If a failure is detected, the switching transistors are shut off for approximately 0.5 seconds and are allowed to restart. The fault circuitry also issues RST-0 (reset) to the Processor on initial power turn-on and on power-downs.

A sample of all power supply sense voltages are summed together and compared to the reference voltage. If any output is not within tolerance, either of two comparators (U211C and D, one detecting excessive voltages and the other detecting insufficient voltages) enables a fault oscillator (U241B). The fault oscillator through U141C turns the switching transistors off for approximately 0.5 seconds by disabling the 40 kHz Inverter Control Oscillator. Then, the switching transistors are allowed to turn back on and operate normally. Whenever the switching transistors are either initially turned on or off by a fault, RST-0 is sent to the Processor. If the fault continues, the fault circuit permits the power supply to try and operate. However, the fault circuit is shut down for one-half second each time the faulty output is detected. U41A forms an oscillator which defeats the fault circuit for approximately 100 ms each time the switching transistors are turned on. This allows the power supply to stabilize before attempting to detect a fault.

Upon initial power turn-on, RST-0 is low. Later when the power supply's voltage approaches normal, RST-0 goes high. This tells the Processor that all voltages are normal. In the event of an input line power failure or an output supply failure, RST-0 goes low.

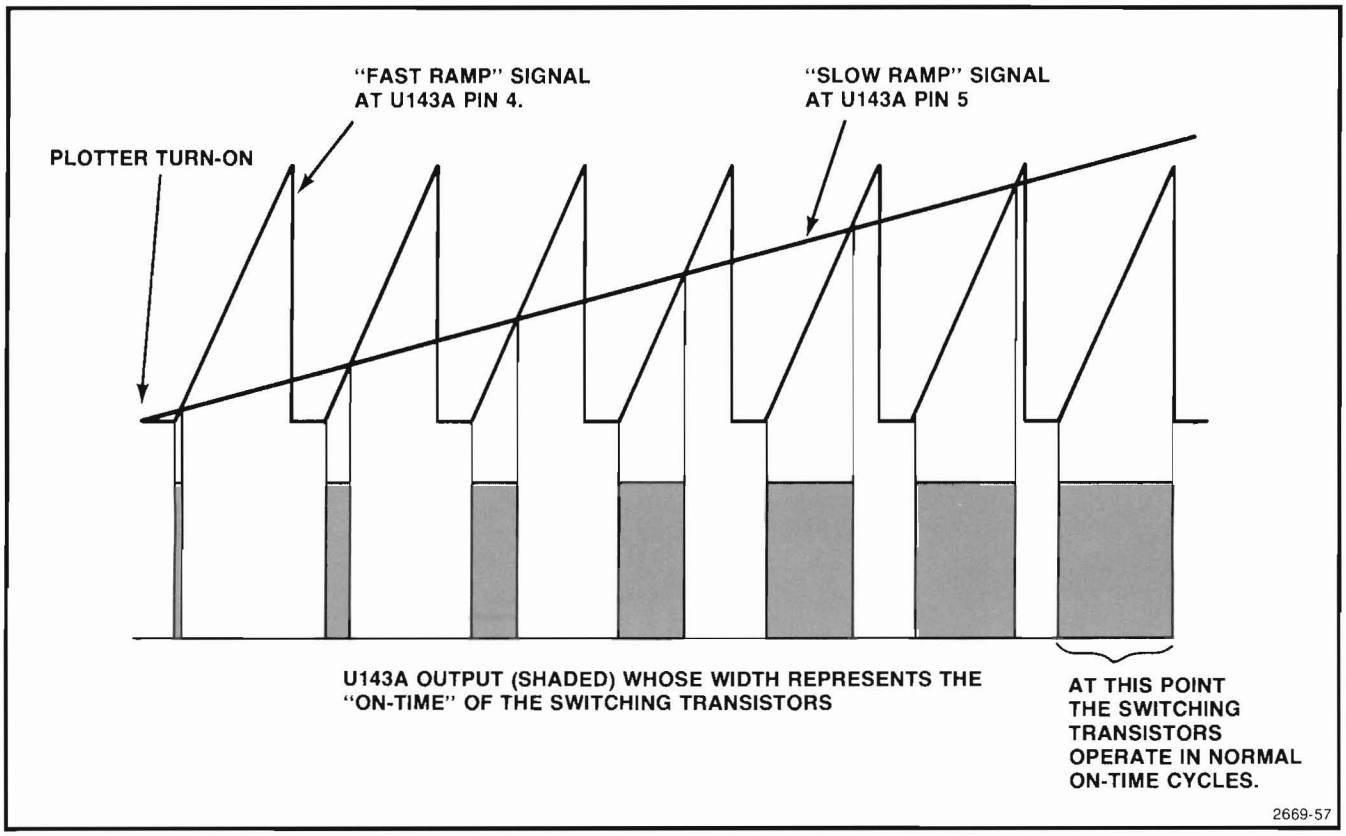

Figure 3-22. Soft-Start Waveforms.

60 Watt Auxiliary Board

The 60 Watt Auxiliary circuit board (shown in Schematic 10-1) provides + 32 Vdc power to operate the three pen drive stepping motors. This board obtains its power from one of the three secondary windings (Taps 7 through 12) of the transformer (T251) in the Plotter's main power supply. This ac signal is rectified by a full-wave rectifier and filtered with an LC filter.

Overcurrent situations (more than three amps) are detected across a 0.1Ω resistor (R34) located in the ground leg of the three pen drive motors. U131, a comparator, uses the voltage across this resistor to control the output transistor Q221. When the pen drive motors' current exceeds three amps, an RC network of R35 and C31 delays the comparator's input sense by about 1/2 ms. The comparator, then, outputs a low on Pin 1, which is passed on to Pin 5 of a second comparator. This second comparator acts as a duty cycle limiter (permits less than 1/2 of 1% duty cycle during overcurrent situations). The low at Pin 5 of this second comparator causes it to output a low, which turns on Q131. Turning on Q131 turns off Q232 and Q221, and shuts down the + 32 V source to the pen drive motors. With the pen drive voltage shut off, the overcurrent comparator returns to normal (with a high output). After approximately 110 ms (governed by R142 and C141), the duty cycle limiter also outputs a high, as in normal operation. This turns off Q131 and turns on Q231 and Q221, restoring the supply to normal operation. If however, the + 32 V supply is still operating in an overcurrent situation, the voltage detected across R34 again causes U131's overcurrent detection portion to output a low. The supply shutdown process is repeated after a 1/2 ms delay.

Two diodes in series (CR133 and CR134) remove rapid positive-going voltage spikes.

CR241 is for reverse-polarity connections.

Fan Regulator Circuit Board

The Fan Regulator circuit board (shown in Schematic 11-1) supplies a pulse-width modulated square-wave ac voltage to operate the instrument's cooling fan. The Fan board obtains its power from the ac-to-dc section of the main power supply and from the switching transistors Q261 and Q271. A pair of switching transistors (Q311 and Q411) alternately switch + 150 and −150 Vdc power to the cooling fan motor at a 60 Hz rate. The resulting fan motor signal, which is a square-wave, has an effective average (RMS) of around 110 V.

The Cooling Fan Power Supply board components obtain their power (+ 28 Vdc) by half-wave rectifying (using CR321) the 20 kHz ac line voltage from the switching transistors. This dc voltage is then filtered. Two zener diodes regulate the + 28 and + 10 V power. The + 28 voltage is used as the overall circuit component power, whereas the + 10 V source is used as a reference to preset R-S Flip-Flop (U211B) whenever the voltage on Pin 5 is less than 10 V.

On initial power-up, a 60 Hz oscillator (U211A) starts to output a square-wave to one end of the primary transformer T221. At the same time, the Exclusive-Or (U211D) turns on so that its initial output is a low. This means that each time the 60 Hz Oscillator outputs a high, the primary of T221 conducts. This causes one of the two switching transistors (Q311 or Q411) on the secondary winding to turn on. The conduction of either transistor switches either + 150 V or −150 Vdc to the fan motor. With this power applied to the fan motor, C212 starts charging toward + 150 or −150 V. However, when its voltage raises to approximately either + 10 V or −10 V, the Precision Rectifier (U211C) outputs a positive pulse. This positive pulse causes the R-S Flip-Flop to reverse and output a high. The high at the inputs of the Exclusive-Or causes it to also output a high. This high on the outputs of both the Oscillator and the Exclusive-Or causes the primary transformer winding to stop conducting and turns off the conducting switching transistor. This shuts off the current to the fan motor. Later, when the Oscillator reverses to a low output, current again flows in the primary of the transformer T221. However, this time the current flows in the opposite direction to the previous cycle. This turns on the opposite switching transistor, which in turn, causes the opposite power source (+ 150 V or −150 V) to be applied to the fan motor and C212. The Oscillator's changing state also resets the R-S Flip-Flop. Then, recharging the capacitor (C212) to either approximately + 10 or −10 V causes the Precision Rectifier to output another positive pulse. The whole process is repeated, and on each half cycle the oscillator resets the R-S Flip-Flop.

Rom Overlay Circuit Board

Early model Plotters contained all of their system firmware in PROMs. Because of the different pin configurations from ROMs and PROMs, these PROMs were installed on a ROM Overlay circuit card (shown in Schematic 12-1). Then later, as portions of the system firmware were coded into ROMs, these ROMs were transferred to the Processor circuit card and the corresponding PROMs on the ROM Overlay circuit card were removed. When the last of the system firmware was coded into ROMs, the ROM Overlay circuit card was removed. This means that it is possible to find Plotters with many combinations of ROM/PROM. The ROMs are located on the Processor circuit card and the PROMs are located on the ROM Overlay circuit card.

The ROM Overlay circuit card may contain all of the system firmware except for ROM 1, which is always found on the Serial Interface Module or Communications Interface, and the 8X300 microprocessor firmware, which is always on the Vector Generator circuit card.

The circuitry on the ROM Overlay circuit card behaves like an extension of the Processor's ROM memory and operates similar to the ROM Patch "B" circuit board described earlier. This means that when the ROM Overlay circuit card recognizes an address contained in a resident PROM, BDDIS-0 is asserted to prevent any ROM on the Processor card from placing erroneous data on the data bus. However, the Processor and its Memory Handshake section still carry out all necessary handshaking as normal. Then, data from the PROM on the ROM Overlay board is placed on the Plotter's data bus.

Bus addresses are buffered through U280 and U380 and are decoded by U155, U255, and U260. U155 and U255 provide the proper CHIP SELECTS to the PROMs at these locations:

U435	U440	U445	U450
U455	U460	U465	U470
U535	U540	U550	U555
U560	U565	U570	U575

Notice that the ROM Overlay circuit board uses two 2K x 8-byte EPROMs for each corresponding 4K x 8-byte ROM on the Processor circuit card except for ROM 0. ROM 0 contains only 2K x 8 bytes.

Also notice that U155 and U255 always supply CHIP SELECTS to the corresponding PROM sockets regardless of whether a PROM is actually located there or not. When selected, the EPROM then puts its data on the bus to U480 (a bus transceiver). However, the bus transceiver does not always transfer this data to the Plotter's system data bus. The following two factors control this.

First, U480 is controlled by the OR of all straps J1 through J9. If the corresponding EPROM is not strapped as present, ASTB-0 and its address are not decoded by U160, and consequently, U480 is not enabled.

Secondly, BDDIS-0 is monitored. If BDDIS-0 is asserted by the Processor circuit card in response to an address, it indicates that that address location is being patched (see the ROM Patch "B" functional block description earlier). Therefore, no response from this circuit card is necessary. On the other hand, if BDDIS-0 is not asserted by the Processor, the high on the BDDIS-0 line is clocked through the J-K flip-flop (U175A) to U275D. Then, four clock cycles later (via U170), ASTB-0 and the output from the J-K flip-flop enable U480 to transfer the data from the addressed PROM to the Plotter's data bus. During this process, any ROMs on the Processor card are prevented from placing unwanted data on the data bus. This is because just after the high on BDDIS-0 was clocked through the J-K flip-flop, U165 and U180 asserted BDDIS-0 to disable any Processor circuit card ROMs.

ASTB-0 is also used to enable the decoder (U260) and release the clear function to the J-K flip-flop U175. This means that the J-K flip-flop is cleared whenever ASTB-0 is high.

J260, J263, and J265 are strapped for the proper addressing of the PROMs, while J1 through J9 are strapped according to the presence of individual PROMs.

U150A and B and U275B clear U170C one bus clock cycle after DSTB-0 goes high at the end of a bus transaction. Then, after one more bus clock cycle, the J-K flip-flop U175A removes the enable to U480. This eliminates the PROM's data from the Plotter's data bus and the process can be repeated with the next Processor read request.

Section 4

CIRCUIT DESCRIPTIONS OF OPTIONS

ABOUT THIS SECTION

The 4663 Plotter is available with several electrical options; circuit descriptions for these options are included in this section.

Option 1—Standard Plotter (Including RS-232) Plus GPIB

The circuit descriptions of both RS-232 and GPIB are in Section 3. Notice that the GPIB uses an additional version of the Communications Interface circuit card.

Option 4—GPIB Only

The circuit description of GPIB is described in Section 3. GPIB uses another version of the Communications Interface circuit card.

Option 30—4081 Interface

The TEKTRONIX 4081 System uses the standard RS-232 Communications Interface when connected to the Plotter. Section 3 of this manual contains the description of the RS-232 Interface.

Option 31—Circular Interpolation and Macros

Option 31 does not use any unique electronic circuitry. This option consists of two ROMs which are installed on the Processor circuit card.

Option 32—Downloadable Characters and Math

Option 32 does not use any unique electronic circuitry. This option consists of four ROMs which are installed on the Processor circuit card.

Option 36—Media Advance

Early versions of this option were known as Paper Advance. This circuit description is common to both Media or Paper Advance options.

The Media Advance option consists of a roll of writing media, a drive motor, and control circuitry to permit the host or operator to advance paper (or other writing media) across the Plotter platen. The paper can be advanced with a form feed (determined by current Parameter Entry settings or host commands) or in small (1/64 in) increments.

The Media Advance functional block circuitry (shown in Schematic 15-1) is divided into the following functional blocks: Address Decode, Joystick Interface, IRQ, Motor Drive, and Out-of-Paper Detector. Each of these blocks is described in subsequent paragraphs.

Address Decode

The Address Decode is a group of AND gates which monitor the Plotter's address bus and look for addresses FDC0, FDC2, and FDC3. These are the addresses of the three registers controlling the Media Advance operation. The Media Advance functional block, like others residing on the Plotter backplane, communicates with the Processor using normal handshaking protocol. This handshaking protocol is described in Section 3, under Processor Read, Write, and Interrupt cycle descriptions. The Address Decode processes DATA STROBE (DSTB-0) according to this protocol. The Processor asserts WRITE (W-0) either high or low (false or true) to determine whether it is going to write into/read from a register in the Media Advance. The W-0 signal not only enables the proper processing of DSTB-0 but also is used to route the incoming addresses FDC0, FDC1, and FDC2. If the Processor is reading a Media Advance register, the Read half of the Read/Write Demultiplexer is enabled. If a write into a Media Advance register is performed, the Write half of the Demultiplexer is enabled. The outputs of Read FDC0 and FDC2 (Read FDC1 is not used), and Write FDC0, FDC1, and FDC2 are used to enable other functions of the Media Advance.

Joystick Interface

The Joystick can be used for manually controlled media advances. To move the writing media in either direction, the operator pushes the front panel switch for MANUAL MOTION. This interrupts the Processor, which then writes a "1" into Bit 7 of FDC2. The writing of a "1" into Bit 7 of FDC2 enables the interrupt request flag. Then, when the operator pushes the joystick control in either X-axis direction, two signals from the Joystick Rate Generator via the Vector Generator are used by this circuit. One of these signals is XPLUS-1, which becomes Bit 6 of FDC2. The Processor reads this bit position at the next interrupt and indicates the direction of the joystick control deflection (the desired direction of paper travel). A "1" in Bit 6 indicates a request for CW motor rotation which causes the paper to move from left to right (viewing from the front of the instrument). The second signal from the Joystick Rate Generator is XRATE-0, which is sent through a divide-by-32 counter (U420, U520, and U720). The frequency of the XRATE-0 signal is directly proportional to the angle of joystick deflection, which corresponds to the desired speed of media advance. The XRATE-0 signal, now divided by 32, is used by the IRQ circuit to generate an interrupt (IRQ-0) to the Processor via Bit 7 of FDC2. This means that the Processor is interrupted with every 32'd XRATE-0 pulse. Each time the Processor is interrupted by a 32'd XRATE-0 pulse, the Processor updates the Motor Drive Register (described later).

IRQ

The IRQ circuit is composed of a Media Advance Clock and an Interrupt Decoder strapped to an interrupt level of 6. Both host command-generated and joystick-controlled incremental media advances generate interrupts to the Processor. If the host is sending commands requesting a media advance (which can be either an incremental or a form feed advance), Bit 7 of register FDC2 is addressed. This enables the Media Advance Clock to generate clock pulses at a one ms rate. The clock output becomes a level 6 IRQ-0 to the Processor. The Processor, then, updates the Motor Drive Register. The Motor Drive Register, in turn,

controls the speed of the media advance motor. As long as the host continues to request an incremental media advance, the Processor is interrupted every millisecond and responds by updating the Motor Drive Register at each interrupt. For a form feed advance, the Processor calculates the number of 1/64-inch increments necessary to advance the paper the amount determined by current Parameter Entry settings. Then, the Processor is interrupted that number of times at a one-millisecond rate.

At the beginning and end of a form feed media advance, the Media Advance Clock is enabled at a rate somewhat less than the full one-millisecond rate. This means that for the first few milliseconds, only one pulse out of every three or four is used to generate an IRQ-0. Later, the clock rate is increased until every one-millisecond pulse is used to generate a paper advance step. In the opposite way, the paper is slowed down near the end of an advance. This gradual build-up at the start and decline at the end of a paper advance permits the large paper supply spool to start and stop gradually, preventing torn paper or supply spool overruns.

If the joystick is used to advance the media, another interrupt comes from the Joystick Interface (described earlier). The XRATE-0 from the Joystick Interface on the Vector Generator is also divided by 32 and becomes IRQ-0 (also strapped to the interrupt level of 6). This IRQ-0 causes the Processor to interrupt and update the Motor Drive Register in the same manner as for a host-requested media advance. As long as the joystick is deflected, paper advances across the Plotter's platen.

Motor Drive

The Motor Drive circuitry supplies power to the media advance motor. The media advance motor contains four windings, each driven by a + 12 V source. The speed of the motor and its direction depend upon which combination and how often the windings are energized. Each time the Processor is interrupted by XRATE-0 or the Media Advance Clock pulse, the Processor, with instructions from the firmware, updates the Motor Drive Register with the information shown in Table 4-1 in a four-step sequence.

Table 4-1

MOTOR DRIVE REGISTER UPDATE INFORMATION

Step	CW (Paper Advance)	CCW (Paper Rewind)
1	0011	0011
2	1001	0110
3	1100	1100
4	0110	1001

Notice that the table shows the Motor Drive Register information for the motor turning in either direction. The interrupt rate and the register update occur simultaneously. This means that the interrupt rate is a direct function of the motor speed.

Each time the register is updated, two other simultaneous events occur. First, + 12 V is applied for a minimum of 50 ms by the 50 Millisecond Timer (a retriggerable one-shot multivibrator) to the collectors of the four switching transistors. Each of these transistors is in series (emitter-collector) with one of the four motor windings. The second event is that the Motor Drive Register output is applied to the bases of these same motor winding switching transistors according to Table 4-1. A "1" in one of the bit positions of the Motor Drive Register turns on the corresponding motor winding switching transistor and applies + 12 V to that motor winding. If no paper advance interrupts are generated within 50 ms (for example, when no further paper advance is desired, when the motor is first beginning to turn, or when the motor is slowing down to stop), the 50 Millisecond Timer turns off Q285. This, in turn, turns off the + 12 V source (Q180) to the motor winding switching transistors. While the + 12 V source is turned off, a + 5 V source is applied through VR280 to each of the four windings and serves as a motor "hold" voltage. This motor hold, plus the tension generated by the paper roll slip clutch, acts as a constant tension to hold the paper tight across the platen while the Plotter is drawing.

Out-of-Paper Detector

The Out-of-Paper Detector consists of a photodetector and a 0.5-second timer (U380). The detector, located between the paper supply spool and the platen, looks for movement of the paper's sprocket holes as the paper is advancing. As long as paper is still moving past the detector when the media advance cycle is finished, the Plotter assumes it has enough paper to make the next plot. On the other hand, if the paper stopped moving or ran out *during* the media advance cycle, the Processor reads an Out-of-Paper flag at address FDC0 (Bit 6) and does not permit the Plotter to draw the next plot.

The photodetector is a cyclops detector using an IR LED to reflect off the paper and shine on a phototransistor. The LED turns off the phototransistor each time a paper sprocket hole goes by. The ac output of the phototransistor is amplified by an op-amp (U110) which has a low range and limited bandpass of less than 50 or 60 Hz. The amplified ac is applied to the retriggerable 0.5-second timer. Each time a sprocket hole moves by the phototransistor, the timer is reset.

If the Plotter should run out of paper during the media advance cycle, no sprocket holes are detected, and the timer would not be reset. Approximately 0.5 seconds later, the timer times out and outputs a signal to U430 (a D flip-flop), signifying an out-of-paper condition. The FDC1 addresses which are usec to apply the + 12 volt power to the motor winding switching transistors and to update the Motor Drive Register are also used to clock the Out-of-Paper signal through the D flip-flop. The Out-of-Paper signal eventually becomes a "1" in Bit 6 of FDC0. The Processor reads this bit at the completion of each media advance cycle. If the Processor reads a "1" in Bit 6 of FDC0, it assumes that the Plotter is out of paper or the amount of paper on the platen is insufficient to accomplish the next plot.

If the paper and the media advance motor both stop moving together (indicating a normal media advance with sufficient paper), the 0.5-second timer generates the same Out-of-Paper condition approximately 0.5 seconds later. However, since the motor has stopped, no more FDC1 addresses are needed to apply + 12 volts to the motor windings and update the Motor Drive register. This Out-of-Paper condition signal is *not* clocked through U430 (the D flip-flop) to Bit 6 of register FDC0. Bit 6 of FDC0 then continues to read as a "0", and the Processor reads this "0" at Bit 6 of this register and permits the next plot to be drawn.

Table 4-2 describes the various registers in the Media Advance.

Table 4-2

MEDIA ADVANCE REGISTERS

Register	Bit	Function
FDC0 (U830)	7 (READ)	Form feed clock interrupt flag, nominal rate of 1 ms where the active level is "1." Interrupt flag is strapped to level 6; flag is self-clearing after the Processor has read this register by System Reset or when the Processor has written a "0" in its interrupt mask bit.
	7 (WRITE)	Form feed clock interrupt mask, active level is "0." A "1" in this bit position enables the clock and interrupt request flag. System Reset clears this bit.
	6 (READ)	This bit position indicates paper status, where a "1" implies Out-of-Paper. This is read upon completion of incremental advance or a form feed.
	0-5	Not used.
FDC1 (U530) (WRITE ONLY REGISTER)	4-7	Not used.
	0-3	Corresponds to motor windings 1-4. A "1" energizes the associated motor winding.

Table 4-2 (cont.)

MEDIA ADVANCE REGISTERS

Register	Bit	Function
FDC2 (U830)	7 (READ)	Incremental rate interrupt flag whose nominal rate is equal to or less than 4 ms. Active level is "1." The interrupt flag is strapped to IRQ level 6. This flag is cleared following a register read, by System Reset, or by writing an "0" into its interrupt mask bit.
	7 (WRITE)	Incremental rate interrupt mask bit whose active level is "0." Writing a "1" into this bit position enables the joystick XRATE-0 signal to generate interrupts. System Reset clears this bit and the rate scaling counter.
	6 (READ)	The bit position indicates the direction of joystick deflection which caused the paper increment interrupt request. A "1" indicates a request for CW motor rotation (paper moves left to right).
	0-5	Not Used.

Option 37—Additional Parameter Entry Set-Up Memory

Option 37 does not consist of any unique electronic circuitry. This option consists of up to three CMOS RAMs which are installed on the Processor circuit card.

Option 48—220 Volt @ 50 Hertz Operation

Option 48 reconfigures the Plotter's power supply such that it can operate with a 220 volt (and 50 Hertz) line voltage. See the description of the Power Supply in Section 3 of this manual for details.

Appendix A

SIGNAL DEFINITIONS

Signal	Name	Source	Destination	Bus #	Description
ACIEN-1	ACIA Enable	Bus Handshake (4-1)	RS-232 Interface (4-4)	————	Enables the ACIA.
AGND	Analog Gnd	————	————	70	Return for Motors, etc.
ASTB-0	Address Strobe	Timing & Processor Bus Handshake (1-2), Vector Generator DMA Control (6-2)	Memory/Register (many), Memory Handshake (1-4), ROM Memory Size Decode (1-6)	66	Asserted by the Processor (or the Vector Generator DMA Control) to indicate that the address on the address bus is valid.
BA0-BA15	Bus Address	Bus Buffers and Transceiver (1-1), or Vector Generator DMA Control (6-2)	Memory/Register (many)	49-64	The Processor (or Vector Generator DMA Control) uses these lines to address ROM, RAM, or registers throughout the Plotter.
BA-1	Bus Available	6800 Microprocessor (1-1)	DMA Bus Control (1-3)	————	Indicates that Phase 1 is present and that the Processor is inactive. The bus is available for DMA activity.
BAUDSH-1	————	Read Status Register (4A-2)	Terminal	————	————
BAUDWR-0	Baud Rate Write	Address Decode (4A-1)	Baud Rate Generator (4A-2)	————	Enables the Baud Rate Register to load the baud rate byte from the data bus lines.
BCK-0	Bus Clock	Timing & Processor Bus Handshake (1-2)	Many places	77	This 14.7456 MHz signal provides basic timing for Plotter.

Signal	Name	Source	Destination	Bus #	Description
BD0-BD7	Bus Data	Memory/Registers (many), Buffers/Transceivers (1-1)	Memory/Registers (many), Buffers/Transceivers (1-1), Bus Interface (1-5)	33, 35, 37, 39, 41, 43, 45, 47	These lines transfer data which is being read/written between memory and the Processor or between memory and the Vector Generator DMA Control.
BDDIS-0	See DDIS-0				
BDSTB-0	See DSTR-0				
BELL-0	Bell Enable	Bell Latch (6-1)	Front Panel Switch Board (8-1)	----	This signal enables the 1 kHz oscillator driving the front panel speaker.
BERR-1	Bus Error	DMA Bus Control (1-3)	Misc Interface/Parameter Entry I/O (1-4)	----	This signal indicates a bus transaction failure, such as a defective component, or a missing address, etc.
BGRNT-0 (also GRNT-1)	Bus Grant	DMA Bus Control (1-3)	Vector Generator DMA Control (6-2)	30	This signal indicates that the bus is available for a DMA character transfer operation.
BRP0-1 BRP1-1 BRP2-1	Bus Request Poll	DMA Bus Control (1-3)	Vector Generator DMA Control (6-2)	22, 24, 26	Bus Request counts binarily at a 7.3728 MHz rate to provide an address to prioritize the DMA requests. This count is the DMA priority level.
BRQ-0	Bus Request	Vector Generator DMA Control (6-2)	DMA Bus Control (1-3)	28	The Vector Generator asserts this signal when it wishes to perform a DMA character transfer operation.

Signal	Name	Source	Destination	Bus #	Description
BRST-0	Buffered Reset	RST-0 (Bus #67)	Joystick Rate Generator (8-2)	----	Activates the analog switches to discharge the integration circuits in the Joystick Ramp Detection circuits upon power-up.
BTO-0 (or TO-1)	Bus Time Out	DMA Bus Control (1-3)	Vector Generator (6-2), Timing and Processor Bus Handshake (1-2)	29	This signal indicates that a bus transaction took longer than 3.8 μs to perform and that a memory device has probably failed. When asserted, the Johnson Counter is forced to switch phases on the next bus clock cycle.
BUSEN-0	Bus Enable	Vector Control (6-2)	DMA Control Port (6-4)	----	Enables the DMA Control Port to decide which DMA access process will be used (GP or Auto Increment).
BVMA	See VMA				
CK-0 (or CK-1)	Processor Clock	Timing & Processor Bus Handshake (1-2)	DMA Bus Control (1-3), Misc Interface/Parameter Entry I/O (1-4)	----	Produced by the Processor Clock to provide basic synchronization for the Processor functional block. CK-0 produces the Phase 1 and Phase 2 timing signals to the 6800 Processor.

Signal	Name	Source	Destination	Bus #	Description
CK-1	See CK-0				
CLMVI-0	Clear Parameter Entry Card Movement Interrupt	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	----	Clears the Parameter Entry Movement Interrupt.
CLSWI-0	Clear Parameter Entry Switch Interrupt	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	----	Clears the Parameter Entry Switch Interrupt.
COMPS-1	----	Bus Handshake (4-1)	RS-232 ACIA Interface (4-2)	----	----
Counter Clear	Counter Clear	Read/Wait Gate (1-2)	Johnson Counter (1-2)	----	This is the feedback used to reset the Johnson Counter and to initiate Phase 1 and Phase 2 periods.
CSI-1	----	IRQ Vectoring (1-3)	Misc Interface/Parameter Entry I/O (1-4)	----	----
CTRDIS	Counter Disable	Switch Change Logic (6-1)	Front Panel Switchboard (8-1)	----	This signal stops the front panel switch matrix scanning process when a second front panel switch has been pressed before the Processor has had a chance to read and act on the first one.
DASTB-1	Delayed Address Strobe	Memory Handshake (1-4)	DMA Bus Control (1-3)	----	----
DATEN-0	Data Enable	DMA Control (6-2)	Write DMA Data Register (6-4)	----	Enables the Write DMA Data Register to output data on the 6800 Processor Bus during a DMA operation.

Signal	Name	Source	Destination	Bus #	Description
DCK-0	Data Clock	Address Decode (6-1)	Read DMA Data Register (6-4)	----	This signal enables the Read DMA Data Register to accept and store DMA data from the 6800 Processor system.
DDIS-0 (or BDDIS-0)	Data Disable	ROM Patch "B" (3-1)	Memory Handshake (1-4)	4	This signal is generated by the ROM Patch "B" circuit when it decodes any ROM address that has been "corrected" by coding in the Firmware Patch. This signal generates MDOUT-0, which in turn disables the Bus Interface from transmitting the erroneous data out of the ROM.
DIO1-DIO7	(GPIB Data Bus)	----	----	----	----
DMAD0-0	DMA Address Register Enable	DMA Control Port (6-4)	Auto Increment DMA Address (6-4)	----	Enables the Auto Increment DMA Address Register to load a DMA address on the address bus.
DMAD1-0	DMA Address Register Enable	DMA Control Port (6-4)	GP DMA Address Registers (6-4)	----	Enables the GP DMA Address Registers to load a DMA address on the address bus.
DMAEN-1	DMA Enable	FFA0 Register (1-4)	DMA Bus Control (1-3)	----	----
DMAW-1	DMA Write	DMA Control Port (6-4)	DMA Control (6-2)	----	Indicates that the pen is moved by the operator (via the Joystick) and the Vector Generator wishes to initiate a DMA transaction with the 6800 Processor to update the pen position registers.

Signal	Name	Source	Destination	Bus #	Description
DSTB-0 (or BDSTB-0)	Data Strobe	Memory/Registers (many), Memory Handshake (1-4)	Memory/Registers (many), DMA Bus Control (1-3), Timing & Processor Bus Handshake (1-2)	32	Asserted by memory during a read transaction to indicate that the data is valid on the data bus, or by the Processor (or Vector Generator DMA Control) during a write cycle to indicate that the write data is valid.
ENAB-1	Enable	Bus Interface Logic (4A-1)	ACIA (4A-2)	----	Enables the ACIA to convert incoming serial RDATA to parallel data on the data bus (or vice versa).
FFF8 & 9	Addresses FFF8 & 9 Detected	I/O Address Space Decode (1-1)	IRQ Vectoring (1-3)	----	Each time the Processor is interrupted, it loads FFF8 and FFF9 on the bus, to be detected by the I/O Address Space Decode. When these addresses have been detected, FFF8 & 9 is generated, which in turn generates LADEN-1 to disable the BA1 through BA4 output buffers and allow the contents of the Lower Limit Poll Counter to be used instead.

Signal	Name	Source	Destination	Bus #	Description
FPCLK-1	Front Panel Clock	Light Data Clock (6-1)	Front Panel Switch Board (8-1)	----	This signal, a 1/32 division of BCK-0, is further divided until it is a 1/2048 division of BCK-0 and is used as an input to the ROW Demultiplexer. This causes each ROW line to be sequentially changed to a TTL low such that 3 scans take 13 ms.
FPINT-0	Front Panel Interrupt	Front Panel Interrupt (6-1)	Interrupt (6-2)	----	Generates an IRQ-0 signal to the Processor each time the Switch Change Logic receives SWCHG-0 from the Front Panel.
GPEN-1	GPIB Enable	Bus Handshake (13-1)	GPIB Interface (13-3)	----	Indicates that one of the GPIB Communications Interface addresses has been decoded and enables the remainder of the GPIB interface circuitry.
GRNT-1	See BGRNT-0				
HALT-0	Halt	Not Used	----	69	----
HLTRQ-0	Halt Request	Not Used	----	----	----

Signal	Name	Source	Destination	Bus #	Description
HVON-0	High Voltage On	Vector Control (6-2)	High Voltage Platen Power Supply (7-1)	17	This signal forward biases a 20 to 30 kHz blocking oscillator which creates the 800 voltage electrostatic paper hold-down voltage.
IM0-1 IM1-1 IM2-1	Interrupt Mask	Misc Interface/Parameter Entry I/O (1-4)	IRQ Vectoring (1-3)	----	These lines are set by the firmware through U201 to indicate the interrupt mask level below which all interrupts are suppressed.
IN0-IN2	(Not Used)	----	----	13, 15, 17	----
INITL-1	Initial Light	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	----	This signal indicates that the Plotter's initialization sequence is not completed. The signal turns on the INIT LED (immediately to the left of the Parameter Entry switches).
INTCK-1	Integration Clock	Sequence Control (7-1)	Joystick, Integration Clock, and Limit Switch Interface (6-4)	16	Integration Clock is used by the 8X300 in the Vector Generator to synchronize the construction of the four data bytes to the Motor Pen Drive. This signal goes high every 17.28 μs (the start of a new series of 4 Motor Pen data bytes).
I/O ADD-1	In-Out Address	Bus Buffers/Transceivers (1-1)	Many registers, Misc Interface/Parameter Entry I/O (1-4), CMOS RAM (1-5)	65	Indicates that an access to the top 2K of memory is being performed.

Signal	Name	Source	Destination	Bus #	Description
IRP0-1 IRP1-1 IRP2-1	Interrupt Poll Counter	IRQ Vectoring (1-3)	Miscellaneous Interface/Parameter Entry I/O (1-4), GPIB Interface Logic (13-2), Vector Generator (6-2), Media Advance (14-1)	21, 23, 25	Interrupt Poll counts binarily at a 7.3728 MHz rate to provide an address to prioritize the interrupt requests. This count is the interrupt priority level.
IRQ-0	Interrupt Request	GPIB Interface Logic (13-2), Misc Interface/Parameter Entry (1-4), Vector Generator (6-2), Media Advance (14-1)	IRQ Vectoring (1-3)	27	Asserted by any functional block that wishes to interrupt the Processor.
IV0-0 through IV7-0	Inverted Data	————	————	————	8X300 data complementary to the remainder of the Plotter.
LADEN-1	Low Order Address Enable	IRQ Vectoring (1-3)	Bus Buffer Transceivers (1-1)	————	This signal is used by the IRQ Vectoring section to disable the BA1-1 to BA4-1 address bits from the Processor when identifying the interrupting functional block. After these address bits have been disabled, the IRQ Vectoring section substitutes the current lowest level count for the address BA1-1 to BA4-1 to identify the applicable interrupt service routine.

Signal	Name	Source	Destination	Bus #	Description
LOAD-0	Load	Bus Interface Logic (4A-1)	Bus Interface Logic (4A-1)	----	A 67.8 ns pulse resulting from the Processor's ASTB-0, which causes the SIM's Handshaking and Strobe Generator to load an initial count of 5.
LTCLK-1	Light Clock	Light Data Clock (6-1)	Front Panel (8-1)	----	A 1/16 division of BCK-0 used to clock LTDATA-1 into the lamp-drivers of the Front Panel Switches and Lights circuit board.
LTDATA-1	Light Data	Parallel-In/Serial-Out Shift Register (6-1)	Front Panel Switch Board (8-1)	----	This signal becomes the enable for the lamp-drivers in the Front Panel Switches and Lights circuit board. A "1" indicates that the lamp is to be on.
LTEN-1	Light Enable	Light Enable Latch (6-1)	Front Panel Switch Board (8-1)	----	Enables the Lamp Drivers in the Front Panel Switches and Lights circuit board.
MA0-15	Memory Address	Bus Interface (1-5)	Memory Devices (1-5, 1-6)	----	Bus Address lines between the Bus Interface and the actual memory devices.

Signal	Name	Source	Destination	Bus #	Description
MCK-0	Motion Clock	8X300 (6-3)	Light Data Clock(6-1), Sequence Control (7-1)	15	Provides the master synchronization between the Vector Generator and the Motor Pen Drive (MCK-0 is a 1/8 division of BCK-0).
MD0-7	Memory Data	Bus Interface (1-5)	Memory Devices (1-5, 1-6)	————	Bus data lines between the Bus Interface and the actual memory devices.
MDOUT-0	Memory Device Out	Memory Handshake (1-4)	Bus Interface (1-5)	————	Disables the Bus Interface from passing data from the memory when the ROM Patch "B" circuit board desires to substitute "corrected" data.
MOTEN-0	Motion Enable	Vector Control (6-2)	8X300 Microprocessor (6-3), DMA Control Port (6-4), Motor Pen Drive Sequence Control (7-1)	13	This signal starts the 8X300, enables the DMA Control Port, and enables the Motor Pen Drive to accept data from the Vector Generator.
MPD0-7	Motor Pen Data	Hardware RAM Copy Digitizer (6-4)	Digital-to-Analog Converter (7-2)	34, 36, 38, 40, 42, 44, 46, 48	Pen Drive Motor Phase angle information (or pen pressure) in digital form. Data is transferred from the Vector Generator to the Motor Pen Drive functional block.
MW-0	See WRITE-0				

Signal	Name	Source	Destination	Bus #	Description
OUT0-OUT2	(Not used)	----	----	14, 16, 18	----
PAREN-1	Parameter Entry Enable	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	----	Enables the Parameter Entry Card Movement Interrupt.
PDE-0	Parameter Data Enable	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	----	This signal enables the Processor to read the contents of the FFA3 Parameter Entry Switch Register (reads which switch was pressed).
PDWE-0	Parameter Data Write Enable	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	----	This signal enables the Processor to write into the FFA3 Parameter Entry LED Register (which turns on the LEDs).
PE0-0 PE1-0	ROM Patch Enable	PROM Memory Size Decode (1-6)	ROM Patch "B" (3-1)	----	PE0-0 is generated to enable Firmware Patch 0 (address is between 1K and 2K bytes below the last PROM). PE1-0 is generated to enable Firmware Patch 1 (address is less than 1K below the last PROM).
PENMAG	Pen Magnitude	Sample Buffer (7-2)	Pen Activation Drive (7-4)	9	Source current for the pen holder coils; this is modified by the PEN PRESSURE OVERRIDE adjustments.
PFAIL-0	Power Fail	Not Used	----	68	----

Signal	Name	Source	Destination	Bus #	Description
PG0DIS-0	Page 0 Disable	Diagnostic Test Fixture (service fixture)	ROM Patch B (3-1)	————	Used in troubleshooting to disable Memory.
PGND	Plotter gnd (signal or chassis)	————	————	1, 2, 79, 80	————
Phase 1 (and Phase 2)	Phase 1, Phase 2	ϕ1 and ϕ2 Clock (1-1)	6800 Processor (1-1)	————	Clock signals used for timing the 6800 Processor. Phase 1 has a 3 clock cycle period of .20345 μs (.47472 μs or 7 clock cycles in early Plotters). Phase 2 has a 4 clock cycle period of .27127 μs (.54245 μs or 8 clock cycles in early Plotters).
PIP (or POP)	Pen 1 Pressure or Pen 2 Pressure	Front Panel Switch Board (8-1)	Pen Activation Drive (7-4)	11, 12	These voltages, taken from the wiper arms of the front panel PEN PRESSURE OVERRIDE adjustments, add to or subtract from PENMAG, the voltage on the pen lifter solenoids. These voltages can be considered the "fine adjust" of the pen pressure.
PIRQ-0	Parameter Entry Interrupt Request	Parameter Entry (2-1)	Misc Interface/Parameter Entry I/O (1-4)	————	An interrupt request to the Processor indicating a Parameter Entry card movement or Parameter Entry Switch activation.
PLINE-1	See LINE-1				
PMVE-0	Parameter Entry Card Move	Misc Interface/Parameter Entry I/O (1-4)	Parameter Entry (2-1)	————	This signal enables the Processor to read the contents of the Parameter Entry FFA2 Register.

Signal	Name	Source	Destination	Bus #	Description
PON-0	Power On	Front Panel Power Switch (8-1)	Power Supply (9-1)	3	This signal (when grounded) enables the 40 kHz oscillator in the power supply's ON-OFF circuit to turn the Plotter on.
POP	See PIP				
QA to QH-0 (or QA to QH-1)	————	Johnson Counter (1-2)	ϕ1 and ϕ2 Clock (1-1), DMA Bus Control (1-3), IRQ Vectoring (1-3)	————	Timing signals from the Johnson Counter to generate the Phase 1 and 2 signals to the 6800 Processor as well as other Processor synchronization timing.
QPT1-1 through QPT5-1	Queue Pointer	Auto Increment DMA Address Register (6-4)	Interrupt Flags (6-2)	————	These address lines inform the Processor from which address in the system RAM's circular queue that the 8X300 is currently obtaining DMA data.
RAMAD-1	RAM Address Transaction	RAM (1-5)	Memory Handshake (1-4)	————	Indicates a Processor/RAM transaction of addresses 0000-1FFF.
RAMEN-0	RAM Enable	Memory Handshake (1-4)	RAM (1-5)	————	Enables the RAM Address Decoder to decode specific RAM addresses.
RATCLK-1	Rate Clock	Front Panel Switch Board (8-1)	Joystick Rate Generator (8-2)	————	A 1/32 division of BCK-1, used to establish the frequency of XRATE-0 and YRATE-0.
RCLK	External Receive Clock	Host	Baud Rate Generator (4A-2)	————	Can provide interface synchronization if the Plotter clock is not desired.

Signal	Name	Source	Destination	Bus #	Description
RD0-0 through RD7-0	Write Data	Inverting Buffer (U560)	Right or Left RAM Bank (6-4)	————	Write Data from the inverting buffer to either the right or left memory bank.
RDATA	Receive Data (to the terminal)	Host	RS-232 Interface ACIA (4-2, 4A-2)	————	Serial data from host.
RE-1	————	Memory Hand-shake (1-4)	CMOS RAM (1-5)	————	————
ROMAD-1	ROM Address Transaction	PROM Memory Size Decode (1-6)	ROM (1-2), Memory Hand-shake (1-4)	————	Indicates a Proces-sor/ROM transaction of addresses 4000-F7FF.
ROMCS-0	ROM Chip Select	ROM Decode (4A-1)	Serial Interface ROM (4A-2)	————	Indicates that the ROM Decode decod-ed an address of FF40 to FF43 or FF60 to FF63.
RSADR-1	RS-232 Address	Bus Handshake (4-1)	ACIA (4-2, 4A-2)	————	Indicates that one of the RS-232 Commu-nications Interface addresses has been decoded.
RSEN-1	RS-232 Enable	Bus Handshake (4-1)	RS-232 Interface (4-2, 4A-2)	————	Indicates that one of the RS-232 Commu-nications Interface addresses has been decoded and enables the remainder of the RS-232 interface cir-cuitry.
RST-0 (also RSTB-0 or RSTB-1)	Reset	Fault Circuit (9-1)	Throughout the Plotter	67	Indicates to the Pro-cessor that the Power Supply's voltages have reached normal condition. Is used to clear or reset many registers throughout the Plotter.

Signal	Name	Source	Destination	Bus #	Description
RSTB-0	See RST-0				
RSTB-1	See RST-0				
R/W	See WRITE-0				
S0-1 S1-1 S2-1	————	Sequence Control (7-1)	Analog Demultiplex (7-2), Right Decode (6-4)	18, 19 20	These signals control the routing and division of the four Vector Generator motor and pen bytes through the Motor Pen Drive functional block.
SC-1	————	8X300	I/O Address Decode	————	Determines a Processor Address Write.
SINT-0	————	Misc Interface/Parameter Entry I/O (1-4)	IRQ Vectoring (1-3)	————	————

Signal	Name	Source	Destination	Bus #	Description
SWCHG-0	Switch Change	Front Panel Switch Board (8-1)	Switch Change Logic (6-1)	----	Each time a front panel switch is pressed or released, this signal is generated to the Vector Generator causing an interrupt to the Processor.
SWPOL-1	Switch Polarity	Front Panel Switch Board (8-1)	Switch Latches (6-1)	----	Each time a front panel switch is pressed or released, this signal is generated to the Switch Latches, so that the Processor, after being interrupted, can read whether the switch was pressed or released.
SWPOS0-1 through SWPOS4-1	Switch Position	Front Panel Switch Board (8-1)	Switch Latches (6-1)	----	The bit combination of these lines (stored in the Switch Latch) furnishes enough information for the Processor to determine which front panel switch was pressed and which way it changed (either opened or closed).
SWRD1-0 (or SWRD2-0)	Switch Read	Switch Change Logic (6-1)	Switch Latches (6-1)	----	Transfers switch matrix data stored in the Switch Latches to the Vector Generator Data Bus.
SWWR1-0 (or SWWR2-0)	Switch Write	Switch Change Logic (6-1)	Switch Latches (6-1), Front Panel Interrupt (6-1)	----	This signal causes Switch Latch 1 to accept data from the front panel switch matrix lines (SWPOS0-0 through SWPOS4-0).

Signal	Name	Source	Destination	Bus #	Description
T2	————	Sequence Control (7-1)	Buffer (7-1), Sine/Cosine ROM (7-1)	————	Enables either the Sine/Cosine ROM to accept the motor pen bytes from the Vector Generator or the Buffer to accept the pen pressure byte.
TCLK	External Transmit Clock	Host	Baud Rate Generator (4A-2)	————	Can provide interface synchronization if the Plotter clock is not desired.
TDATA	Transmit Data (from the terminal)	Terminal	RS-232 Interface ACIA (4-2, 4A-2)	————	Serial data from the terminal.
Terminal Count	Terminal Count	Handshaking and Strobe Generator (4A-1)	Handshaking and Strobe Generator (4A-1)	————	Resets the SIM's Handshaking and Strobe Generator to 0
TO-1	See BTO-0				
VMA (also BVMA)	Valid Memory Address	6800 Processor (1-1)	Timing & Processor/Bus Handshake (1-2), DMA Bus Control (Processor) (1-3), Bus Buffers/ Transceivers(1-1)	————	Indicates that there is a valid address on the address lines and is used to generate ADDRESS STROBE (ASTB-0).
W-0	See WRITE-0				
W-1	See WRITE-0				
WC-1	————	8X300 (6-3)	I/O Address Decode (6-3)	————	Determines a Processor Data Write.
WEREN-1	Wait Error Enable	Timing & Processor Bus Handshake (1-2)	DMA Bus Control (1-3)	————	Timing signal used to synchronize a potential Bus Error.

Signal	Name	Source	Destination	Bus #	Description
WRITE-0 (also W-0, W-1, MW-0, R/W)	Read/Write	6800 Processor (1-1), Vector Generator DMA Control (6-2)	Memory/Registers (many)	31	Indicates a read or receiving state (when low) or a write or transmitting state (when high). Write-0 can be buffered and become high. Write-0 can also be buffered and become Memory Write-0 (MW-0) to the Memory functional block.
XCVR-0	Transceiver Enable	Bus Handshake (6-1)	Data Bus Transceiver (6-2)	————	Enables the Vector Generator Data Bus Transceiver whenever addresses from FDE0 to FDFF are received.
XJOY (or YJOY)	X-Axis Joystick (Y-Axis Joystick)	Joystick	Joystick Rate Generator (8-2)	————	These voltages are the wiper arm voltages from the two joystick potentiometers and are used to create the signals to either the pen drive motors or the Option 36 motor, if present.
X, X', Y LIMIT-1	————	X, X', or Y Limit Switches (7-4)	Limit Switch Detector (7-4), Joystick , Integration Clock, Limit Switch Interface (6-4)	6, 8 10	Indicates that the "knifeblade" has interrupted the light beam in the phototransistor. Used in the Plotter initialization process.
XPLUS-1 (or YPLUS-1)	X-Axis Plus (or Y-Axis Plus)	Joystick Rate Generator (8-2)	Joystick, Integration Clock, Limit Switch Interface (6-4)	7 (XPLUS)	This signal determines the direction of the pen (or paper) movement.

Signal	Name	Source	Destination	Bus #	Description
XRATE (YRATE)	X-Axis Rate (or Y-Axis Rate)	Joystick Rate Generator (8-2)	Joystick, Integration Clock, Limit Switch Interface (6-4)	5 (XRATE)	A pulse-width modulated signal used to determine the speed and distance that the pen (or paper) has to be moved. Also turns on the switch to discharge the integrating capacitors.
YJOY	See XJOY				
YLIMIT-1	See XLIMIT-1				
YPLUS-1	See XPLUS-1				
YRATE	See XRATE				

Appendix B

COMMAND SUMMARY

SERIAL INTERFACE

Interface Commands

Device On	ATN ADD E
Device Off	ATN ADD F
Block Start	ATN ADD (
Set Turnaround Delay	ATN ADD G DELAY TIME (milliseconds)
Block End	ATN ADD) CHECKSUM VALUE
Set Block Size	ATN ADD H BLOCKSIZE (bytes)
Set Bypass Cancel Character	ATN ADD U ASCII CHARACTER
Set Signature Character	ATN ADD S ASCII CHARACTER
Set Prompt String	ATN ADD R ASCII CHARACTER STRING
Interface Parameter Reset	ATN ADD CR
Data Reset	ATN ADD CD
Select Command/Response Format	ATN ADD CC CHOICE

Device Commands

Device Reset	ATN ADD N RESET NUMBER (0-2)
Read Status	ATN ADD O STATUS REGISTER (0-3)
Read Error	ATN ADD CE
Identify	ATN ADD Q

Graphic Commands

Select Graphic Units	ATN ADD BW INCHOICE,OUTCHOICE (0,1)
Select Device Units	ATN ADD BV CHOICE (0-2)
Select Line Type	ATN ADD BL CHOICE (0-3)
Set Dash Pattern	ATN ADD BD NUMBER STRING
Set Dash Pattern Length	ATN ADD BS LENGTH (world units)
Select Pen	ATN ADD BP CHOICE (0-2)
Select Coordinate Type	ATN ADD BO CHOICE (0-1)
Page Change	ATN ADD BC
Move To Load Point	ATN ADD AI
Move	ATN ADD X X,Y(,X,Y)
DRAW	ATN ADD Y X,Y(,X,Y)
OUTLINE VIEWPORT	ATN ADD CB
MARK VIEWPORT	ATN ADD CM
AXIS	ATN ADD CA XSPACING,YSPACING,XORG,YORG

Transformation Commands

Save Current Transform	ATN ADD AX
Restore Previous Transform	ATN ADD AY
Set Origin To Current Position	ATN ADD AO
Set Rotation To Last Angle	ATN ADD AL
Set Scale	ATN ADD AS XSCALE,YSCALE (multiplier)
Set Translation	ATN ADD AT XORG,YORG
Set Skew	ATN ADD AQ XSKEW,YSKEW (degrees)
Set Rotation	ATN ADD AR ANGLE (degrees)
Set Window	ATN ADD AW LLX,URX,LLY,URY (world units)
Set Viewport	ATN ADD AV LLX,URX,LLY,URY (device units)
Select Clipping Control	ATN ADD AK CHOICE (0-1)
Read Viewport	ATN ADD CV

Alpha Commands

Set Alpha Size	ATN ADD BZ WIDTH, HEIGHT (world units based upon default window)
Set Alpha Ratio	ATN ADD BI XRATIO,YRATIO
Set Alpha Dimension	ATN ADD I CHARSPACE,LINESPACE
Set Alpha Rotation	ATN ADD J ANGLE (degrees)
Set Alpha Slant	ATN ADD BG ANGLE (degrees)
Set Alpha Scale	ATN ADD BH XSCALE,YSCALE (multiplier)
Set Tab Separation	ATN ADD BT NUMBER (multiple spaces)
Set Alpha Margin Separation	ATN ADD BR SPACES
Select Alpha Spacing Control	ATN ADD AJ CHOICE (0-1)
Select Standard Alpha Font	ATN ADD T FONT # (0-15)
Select Alternate Alpha Font	ATN ADD BQ FONT # (0-15)
Reset Alpha Parameters	ATN ADD V
Print Character	ATN ADD P STRING
Print Centered Character	ATN ADD AP ASCII CHARACTER
Move To Home	ATN ADD AH
Character Move	ATN ADD AM HSPACES,YSPACES
Set Arc Smoothness	ATN ADD BA VALUE (0.0-1.0)

Digitizing Commands

Digitize	ATN ADD M
Operator Digitize	ATN ADD AG MAXIMUM POINTS
Prompt Light On	ATN ADD K
Prompt Light Off	ATN ADD L
Joystick Axis Disable	ATN ADD BJ JOYSTICK AXIS (0-3)

Commands Associated with Plotter Options

Option 31

Draw Arc	ATN ADD AA X1,Y1,X2,Y2
Draw Circle	ATN ADD AC RADIUS
Set Arc Smoothness	ATN ADD BA VALUE (0.0-1.0)
Begin Macro Definition	ATN ADD BB MACRO NUMBER
End Macro Definition	ATN ADD BE
Expand Macro	ATN ADD AE MACRO NUMBER, MACRO NUMBER,...
Delete Macro	ATN ADD BK MARCO NUMBER, MACRO NUMBER,...
Read Macro Status	ATN ADD CN
Set Auto Macro	ATN ADD BN MACRO NUMBER

Option 32

Set Downloaded Character Size	ATN ADD CZ FONT #,XMIN,XMAX,YMIN,YMAX
Begin Character Definition	ATN ADD CN FONT #,ASCII CHARACTER
Set Character X-Extent	ATN ADD CT LEFT,RIGHT
Select Non-Advancing Character	ATN ADD CU
End Character Definition	ATN ADD CO
Delete Character Definition	ATN ADD CP FONT #,ASCII CHARACTER(S)
Delete Font Definition	ATN ADD CQ FONT #

Option 36

Advance Media	ATN ADD AU NUMBER OF INCREMENTS (1/64")
Read Formlength	ATN ADD CF
Set Formlength	ATN ADD BF NUMBER OF INCREMENTS (1/64")
Page Change	ATN ADD BC

GPIB INTERFACE COMMAND SUMMARY IN 4051 BASIC FORMAT

The normal operating format when using the Tektronix 4051 is Format #1. The following notation is: D is the GPIB device number to which the Plotter is set. R1, R2, R3,... are command dependent numeric responses.

Interface Commands

Data Reset	PRINT@D,32:"CD"
Select Command/Response Format	PRINT@ D,32:"CC",CHOICE

Device Commands

Device Reset	PRINT@ D,32:"N"
Read Status	PRINT@D,32:"V",STATUS REGISTER (0-3)
Read Error	PRINT@D,32:"CE"
	INPUT@D,32:R1,R2,R3
	INPUT@D,32:R4, R5, R6
Identify	PRINT@D,32:"I"
	INPUT@D,32:R1,R2,R3

Graphic Commands

Select Graphic Units		PRINT@D,32:"BW",INCHOICE,OUTCHOICE (0-1)
Select Device Units		PRINT@D,32:"BV",CHOICE (0-2)
Select Line Type		PRINT@D,32:"BL",CHOICE (0-3)
Set Dash Pattern		PRINT@D32:"BD",NUMBER STRING
Set Dash Pattern Length		PRINT@D,32:"BS",LENGTH (world units)
Select Pen		PRINT@D,32:"BP",CHOICE (0-2)
Select Coordinate Type		PRINT@D,32:"BO",CHOICE (0-1)
Page Change		PRINT@D,32:"BC"
Move To Load Point		PRINT@D,32:"AI"
Move		PRINT@D,32:"M",X,Y(,X,Y)
	OR	MOVE@D:X,Y
	OR	PRINT@D,21:X,Y
Draw		PRINT@D,32:"D",X,Y
	OR	DRAW@D:X,Y
	OR	PRINT@D,20:X,Y
Outline Viewport		PRINT@D,32:"CB"
Mark Viewport		PRINT@D:32:"CM"
Axis		PRINT@D,32:"CA",XSPACING,YSPACING,XORG,YORG

Transformation Commands

Save Current Transform	PRINT@D,32:"AX"
Restore Previous Transform	PRINT@D,32:"AY"
Set Origin To Current Position	PRINT@D,32:"AO"
Set Rotation To Last Angle	PRINT@D,32:"AL"
Set Scale	PRINT@D,32:"AS",XSCALE,YSCALE (multiplier)
Set Translation	PRINT@D,32:"AT",XORG,YORG
Set Skew	PRINT@D,32:"AQ",XSKEW,YSKEW (degrees)
Set Rotation	PRINT@D,32:"AR",ANGLE (degrees)
Set Window	PRINT@D,32:"AW",LLX,UR,LLY,URY (world units)
Set Viewport	PRINT@D,32:"AV",LLX,UR,LLY,URY (device units)
Clipping Control	PRINT@D,32:"AK",CHOICE (0-1)
Read Viewport	PRINT@D,32:"CV"
	INPUT@D,32:R1,R2,R3
	INPUT@D,32:R4,R5,R6

Alpha Commands

Set Alpha Size	PRINT@D,32:"BZ",WIDTH,HEIGHT (world units based upon default window)
Set Alpha Ratio	PRINT@D,32:"BI",XRATIO,YRATIO
Set Alpha Dimension	PRINT@D,32:"S",CHARSPACE,LINESPACE
Set Alpha Rotation	PRINT@D,32:"R",ANGLE (degrees)
Set Alpha Slant	PRINT@D,32:"BG",ANGLE (degrees)
Set Alpha Scale	PRINT@D,32:"BH",XSCALE,YSCALE (multiplier)
Set Tab Separation	PRINT@D,32:"BT",NUMBER (multiple spaces)
Set Alpha Margin Separation	PRINT@D,32:"BR",SPACES
Select Alpha Spacing Control	PRINT@D,32:"AJ",CHOICE (0-1)
Select Standard Alpha Font	PRINT@D,32:"F",FONT # (0-15)
Select Alternate Alpha Font	PRINT@D,32:"BQ",FONT # (0-15)
Reset Alpha Parameters	PRINT@D,32:"A"
Print Character	PRINT@D:"TEXT STRING"
	or PRINT@D,32:"PTEXT STRING"
Print Centered Character	PRINT@D,32:"AP CHARACTER"
Move To Home	PRINT@D,32:"H"
Character Move	PRINT@D,32:"AM",HSPACES,YSPACES
Set Arc Smoothness	PRINT@D,32:"BA",VALUE (0.0-1.0)

Digitizing Commands

Digitize		PRINT@D,32:"G"
		INPUT@D,32:R1,R2,R3
	OR	GIN @ D:X,Y
Operator Digitize		PRINT@D,32:"AG",MAXIMUM POINTS
Prompt Light On		PRINT@D,32: "T",1
Prompt Light Off		PRINT@D,32:"T",0
Joystick Axis Disable		PRINT@D,32:"BJ",JOYSTICK AXIS (0-3)

Commands Associated With Plotter Options

Option 31

Draw Arc	PRINT@D,32:"AA",X1,Y1,X2,Y2
Draw Circle	PRINT@D,32:"AC",RADIUS
Set Arc Smoothness	PRINT@D,32:"BA",VALUE (0.0-1.0)
Begin Macro Definition	PRINT@D,32:"BB",MACRO NUMBER
End Macro Definition	PRINT@D,32:"BE"
Expand Macro	PRINT@D,32:"AE",MACRO NUMBER
Delete Macro	PRINT@D,32:"BK",MACRO NUMBER
Read Macro Status	PRINT@D,32:"CS"
	INPUT@D,32:R1,R2,R3
	INPUT@D,32:R4,R5,R6 (if necessary)
Set Auto Macro	PRINT@D,32:"BN",MACRO NUMBER

Option 32

Set Downloaded Character Size	PRINT@D,32:"CZ",FONT #,XMIN,XMAX,YMIN,YMAX
Begin Character Definition	PRINT@D,32:"CN",FONT #,ASCII CHARACTER
Set Character X-Extent	PRINT@D,32:"CT",LEFT,RIGHT
Select Non-Advancing Character	PRINT@D,32:"CU"
End Character Definition	PRINT@D,32:"CO"
Delete Character Definition	PRINT@D,32:"CP",FONT #,ASCII CHARACTER(S)
Delete Font Definitior	PRINT@D,32:"CQ",FONT #

Option 36

Advance Media	PRINT@D,32:"AU",NUMBER OF INCREMENTS (1/64")
Read Formlength	PRINT@D,32:"CF"
	INPUT@D,32:R1,R2,R3
Set Formlength	PRINT@D,32:"BF",NUMBER OF INCREMENTS (1/64")
Page Change	PRINT@D,32:"BC"

Appendix C

ERROR TYPES

The following Table shows the Parameter Entry switch display for each error type. For further information on identifying errors refer to Section 2 of the 4663 Operator's Manual.

● = Light is ON

Fatal Errors Parameter Entry Display	Hex Eq	Dec Eq	Cause of Error
O O O O O O O ●	01	1	Insufficient RAM
O O O O O O ● O	02	2	RAM check error
O O O O O O ● ●	03	3	ROM check error
O O O O O ● O O	04	4	Undefined common subroutine
O O O O O ● O ●	05	5	Command dispatch error
O O O O O ● ● O	06	6	Software interrupt
O O O O O ● ● ●	07	7	Non-maskable interrupt
O O O O ● O O O	08	8	Non-existent memory reference
O O O O ● O O ●	09	9	Unable to create a buffer (insuf RAM)
O O O O ● O ● O	OA	10	Unexpected system error
O O O O ● O ● ●	OB	11	No service routine for level
O O O O ● ● O O	0C	12	No self interrupt routine for level
O O O O ● ● O ●	OD	13	MSync address not in first 256 bytes of ROM

Fatal Errors Parameter Entry Display	Hex Eq	Dec Eq	Cause of Error
○○○○●●●○	OE	14	No routine for specified system command
○○○○●●●●	OF	15	ROM in wrong socket
○○○●○○○○	10	16	Motion buffer overrun

Non-Fatal Errors Parameter Entry Display	Hex Eq	Dec Eq	Cause of Error
○○○○○○○●	01	1	Data overrun
○○○○○○●○	02	2	Framing error
○○○○○○●●	03	3	Parity error
○○○○○●○○	04	4	Input buffer full error
○○○○○●○●	05	5	Output attempt when message is in progress
○○○○○●●○	06	6	ODBuffer full
○○○○○●●●	07	7	OBuffer full
○○○○●○○○	08	8	Block size exceeds input buffer size
○○○○●○○●	09	9	Block checksum error
○○○○●○●○	OA	10	GPIB — Illegal secondary address
○○○○●○●●	OB	11	GPIB — Talked with no listener on line
○○○○●●○○	OC	12	GPIB — Unable to complete message transmission
○●○○○○○○	40	64	Integer argument exceeds 16-bit value

Fatal Errors Parameter Entry Display	Hex Eq	Dec Eq	Cause of Error
O●OOOOO●	41	65	Illegal paper advance command
O●OOOO●O	42	66	Illegal macro command usage
O●OOOO●●	43	67	Macro called itself
O●OOO●OO	44	68	Integer outside legal range
O●OOO●O●	45	69	Too many entries or string too long (dash pattern)
O●OOO●●O	46	70	Unidentified interface attention sequence error
O●OOO●●●	47	71	Unidentified interface command error
O●OO●OOO	48	72	Invalid command for selected output format
O●OO●OO●	49	73	Scale = 0
O●OO●O●O	4A	74	Viewport of 0 length or outside page boundary
O●OO●O●●	4B	75	Window less than or equal to 0
O●OO●●OO	4C	76	Page upper right on top of lower left position
O●OO●●O●	4D	77	Argument type error (interface)
O●OO●●●O	4E	78	Command decoding error (interface)
O●OO●●●●	4F	79	Output value range error

Fatal Errors Parameter Entry Display	Hex Eq	Dec Eq	Cause of Error
●OOOOOOO	80	128	Invalid switch entry (Parameter Entry)
●OOOOOO●	81	129	Battery backup RAM checksum error
●OOOOO●O	82	130	Transform stack underflow or overflow
●OOOOO●●	83	131	Transform cannot produce virtual Digitizing data because of transform values
●OOOO●OO	84	132	RAM verify error — block not used
●OOOO●O●	85	133	Insufficient memory for buffer allocation
●OOOO●●O	86	134	Cannot find specified macro
●OOOO●●●	87	135	Illegal alpha table command byte
●OOO●OOO	88	136	Not assigned
●OOO●OO●	89	137	Illegal Monitor usage (RESTAT)
●OOO●O●O	8A	138	Output processing routine missing
●OOO●O●●	8B	139	Number greater than 99999.999 in fixed ASCII conversion
●OOO●●OO	8C	140	Too many PROM alpha tables in system
●OOO●●O●	8D	141	Selected interface hardware or ROM not present