TYPE RB

GENERAL PURPOSE MEMORIES

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TELEMETER MAGNETICS, INC.

TYPE RB

GENERAL PURPOSE MEMORIES

NOW
AMPEX
COMPUTER PRODUCTS COMPANY

TELEMETER MAGNETICS, INC.
P. O. Box 329
Culver City, California

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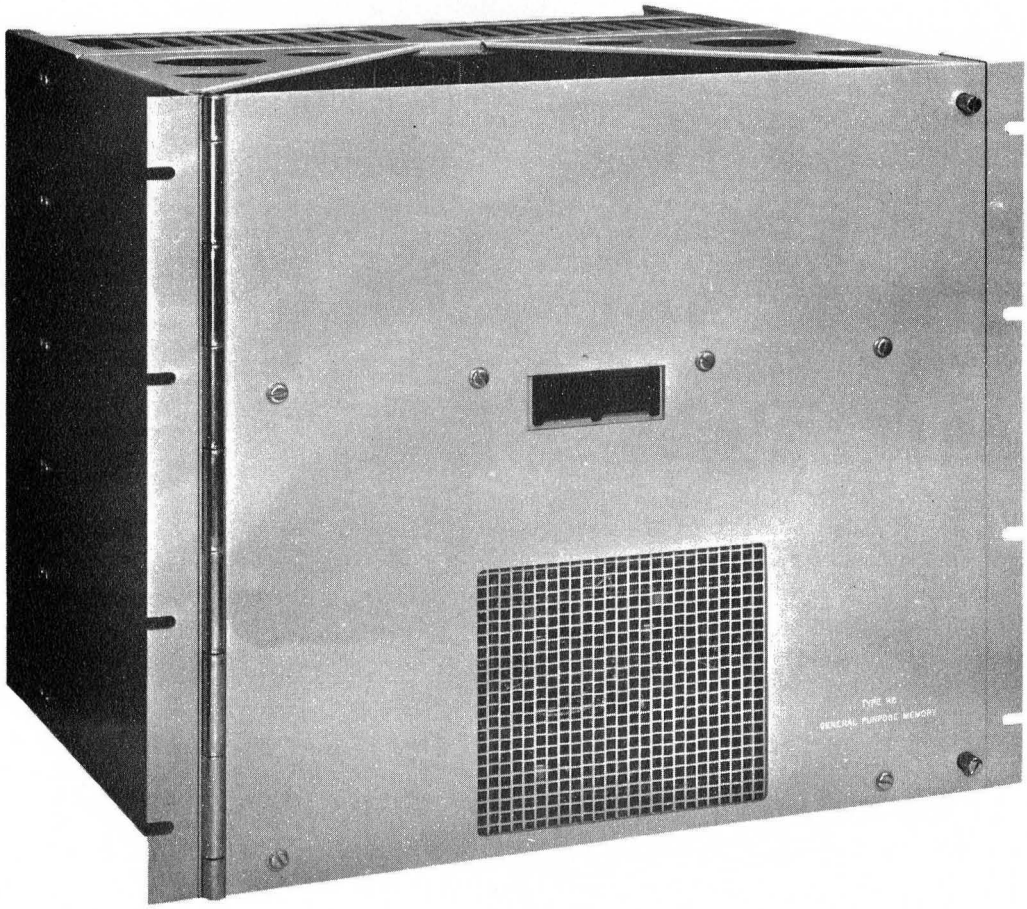


Figure 1-1. Type RB General Purpose Memory, Front View

SECTION I
GENERAL DESCRIPTION

1-1. INTRODUCTION.

1-2. SCOPE. This manual provides information on the installation, operation, theory of operation and maintenance of the Type RB General Purpose Memory. These memories are digital storage units designed and manufactured by Telemeter Magnetics, Inc., 9937 West Jefferson Blvd., Culver City, California.

1-3. MODEL DESIGNATIONS. The model designations indicate the storage properties of the system. The first number indicates the word storage capacity, and the second number designates the number of bits per word. For example, Model 1024-RB-24 means that the system can store 1024 24-bit words.

1-4. PURPOSE AND BASIC PRINCIPLES.

1-5. PURPOSE. The purpose of the system is to accommodate differences in rates of information flow in data handling systems. Digital information is loaded into the system at a time and rate convenient to one data system component and unloaded at a time and rate convenient to another. The RB memory can also be used as a general purpose memory with random access or sequential address selection.

1-6. The system provides utmost flexibility in its digital storage potentialities, modes of operation, and types of input-output signals. Its versatility is enhanced by high-speed operation and compact packaging. Complete transistorization coupled with control design insures reliability.

1-7. Typical applications include data editing and format revision, multiplexing data from several sources, analog-to-digital conversion and data recording, small digital computers, complex data processing, automatic checkout programming, process, machine tool or weapons fire control, digital data communication, meteor burst data transmission, nuclear energy analysis and instrumentation, and pulse height analysis.

1-8. BASIC PRINCIPLES. The RB memory employs a coincident current ferrite core storage system, driven by transistor switches through logical control circuits in response to externally applied synchro-

nization pulses. Load and unload sync pulses generate the coincident currents which determine the state of the bi-stable ferrite cores, and regulate the flow of information through the system. A load sync causes information in the Memory Register to be stored in the memory at a selected address. An unload sync causes information to be read out of the memory at a selected address and presents it to the information output lines. Strobe MR is used to transfer information from the output lines into the Memory Register (MR). Strobe AR is used to transfer information into the Address Register (AR).

1-9. The system is available in storage capacities of 128, 256, 512, or 1024 words, as determined by the customer. The bits per word can be varied from 4 to 24, in increments of two.

1-10. In addition to the synchronization pulses, an externally generated d-c control level is applied to the Timing and Control circuits. This level determines whether the system will perform a typical buffer load or unload cycle, or will function as a regenerative memory to provide clear and write, or read and restore operation. Amplitude and polarity required of this input varies with the chosen output levels. Buffer operation speed is 200 kc (5 microseconds per cycle), and regenerative memory operation speed is 125 kc (8 microseconds per cycle).

1-11. The basic system provides for random access operation as a buffer or memory. The addition of an optional Count Network affords forward or reverse sequential (count) operation. With the addition of the Count Network and optional Transpose Register, load and unload operations can be interlaced in any desired pattern, without loss of speed.

1-12. A wide range of reference levels and signal amplitudes is available, assuring system compatibility with tube or transistor circuits. Input signals may be of either polarity, and may be levels or pulses of varying amplitude. Memory unit output signals are delivered as levels of a selected amplitude. The input voltage level range is established by the output levels chosen.

1-13. A buffer load operation is initiated when a load sync pulse is presented to the Timing and Control circuits. Decoding of the Address Register inputs enables the X and Y switches to select a chosen core in each digit plane of the Memory Module. An inhibit timing pulse from the Timing and Control circuits turns on only those inhibit drivers which are enabled by outputs of the Memory Register flip-flops. An X-Y timing pulse is applied to the X and

Y drivers, and cores not inhibited by the inhibit drivers are set to the ONE state.

1-14. The application of an unload sync plus a disable MO level initiates a buffer unload operation. A pulse from the Timing and Control circuits clears the Memory Register, and an X-Y timing pulse then triggers the X and Y drivers to reset all cores at the selected address that were in the ONE state. Sense winding voltages are applied to Read Amplifiers which are strobed by the Timing and Control circuits. Read amplifier outputs set the Memory Register flip-flops, providing output information.

1-15. A clear/write (clear and write) memory operation is similar to a buffer load, except that the Timing and Control circuits gate the X and Y drivers to reset all cores to ZERO before the normal load operation begins. Read amplifiers are not strobed when the cores are reset.

1-16. Read/Restore (read and restore) memory operation consists of a cycle that restores the information to the memory after it has been read out (cores have been reset). This is a regenerative action in which the information which was read into the Memory Register is re-loaded in the cores.

1-17. Addition of the Count Network affords forward or reverse sequential capabilities in addition to random access. Two externally generated d-c control levels determine whether the count will progress forward or reverse. Upon application of a count pulse, the address is applied to the Count Network, which increases or decreases it by one digit, and returns it to the Address Register for application to the X and Y drivers. The address can be counted forward or backward as desired.

1-18. Interlaced load and unload operations are available with the addition of the Count Network and Transpose Register.

1-19. COMPONENTS.

1-20. GENERAL. There are many possible configurations of the RB Memory System. Figures 1-1 and 5-1 show equipment typical of those systems in which the number of bits per word exceeds 12. Lower bit requirements (4-12 bits) eliminate the bottom card cage (C) with all its printed circuit cards, and decrease the number of digit planes in the Memory Module.

1-21. The RB Memory system is a compact unit consisting of control and logic circuits which are mounted on printed-circuit cards (top

right), a Memory Module made up of matrix planes (lower right), and the power supply (left). The system as illustrated is 15-3/4 inches high, 16 inches deep, and fits into a standard 19-inch rack. The power supplies are hinge-mounted, and can be swung out to provide easy access to the printed cards. If the third card cage is not required, the height is decreased to 10½ inches.

1-22. Basic circuits are mounted on nine types of printed-circuit cards. Six of the cards are common to all system configurations. These are input, timing, register, switch, inhibit, and read amplifier. Three types of cards, count logic, transpose register, and BQ logic are optional additions to the system.

1-23. The number of cards required per system is chiefly determined by the bits-per-word requirements, and to a lesser extent by the number of words. Table 1-1 shows the number of cards of each type required. Register T & C (timing and control) is not electrically different from the other register cards, but is functionally a part of the Timing and Control circuit, whereas the remaining register cards comprise the Address and Memory Registers. An additional register card is required when increasing the word capacity from 128 or 256 to 512 or 1024. For example, eight register cards plus the Register (T & C) are required for Model 256-RB-8; nine plus the Register (T & C) for the 512-RB-8.

1-24. Table 1-2 shows the number of additional cards required when adding the Count Network, or the Transpose Register and Count Network, or BQ Logic. Except the BQ logic card, one additional card of each is required for the 512 or 1024 word system.

1-25. The number of matrix planes is determined by the bits-per-word requirements of the system. One matrix plane is required for each bit, with the number of cores per plane equal to the word capacity of the system. The maximum number of cores is required in Model 1024-RB-24, which uses 24,576 ferrite cores.

1-26. The number of card slots in the card cages is constant for all models, with 24 slots in Card Cage A, and 14 slots in Card Cage B, as well as Card Cage C if required. Since the number of cards used varies with the number of bits, all of the slots are not filled in most models.

1-27. Through the use of Figure 1-2, it is possible to determine the placement of cards in any model. Cards with no symbol (○) included are common to all models. In Card Cage A, card requirements are determined by word rather than bit requirements. The

TABLE 1-1. CARDS REQUIRED FOR VARIOUS CONFIGURATIONS

128 OR 256 WORD SYSTEM	BITS - PER - WORD					
CARD TYPE	4	8	12	16	20	24
INPUT	2	2	2	2	2	2
TIMING	1	1	1	1	1	1
REGISTER (T & C)	1	1	1	1	1	1
SWITCH	2	2	2	2	2	2
INHIBIT	1	2	2	3	4	4
READ AMPLIFIER	2	4	6	8	10	12
*REGISTER	6	8	10	12	14	16
TOTAL CARDS	15	20	24	29	34	38

* - USE ADDITIONAL REGISTER CARD FOR 512 OR 1024 WORD SYSTEM

TABLE 1-2. CARDS REQUIRED TO ADD COUNT NETWORK, TRANSPOSE REGISTER AND COUNT NETWORK, OR BQ LOGIC

128 OR 256 WORD SYSTEM / CARD TYPE	Add Count Network	Add Trans. Reg. and Count Network	Add BQ Logic
INPUT	1	1	1
*COUNT LOGIC	2	2	2
**TRANSPOSE REGISTER	0	4	4
BQ LOGIC	0	0	1
TOTAL CARDS	3	7	8

* - USE ADDITIONAL COUNT LOGIC CARD FOR 512 OR 1024 WORD SYSTEM

** - USE ADDITIONAL TRANSPOSE REGISTER CARD FOR 512 OR 1024 WORD SYSTEM

symbol (x) indicates that the card is used in a 128 or 256 word system. The symbol (xx) indicates additional cards required for 512 or 1024 word systems. Appropriate symbols indicate the addition of optional cards.

1-28. In card cages B and C, the encircled numerals show the various card configurations necessitated by increasing word bits. The symbol (4) indicates those cards necessary to a 4-bit system, and (8) indicates cards added to accommodate an 8-bit system. All of the requirements through 24 bits are shown.

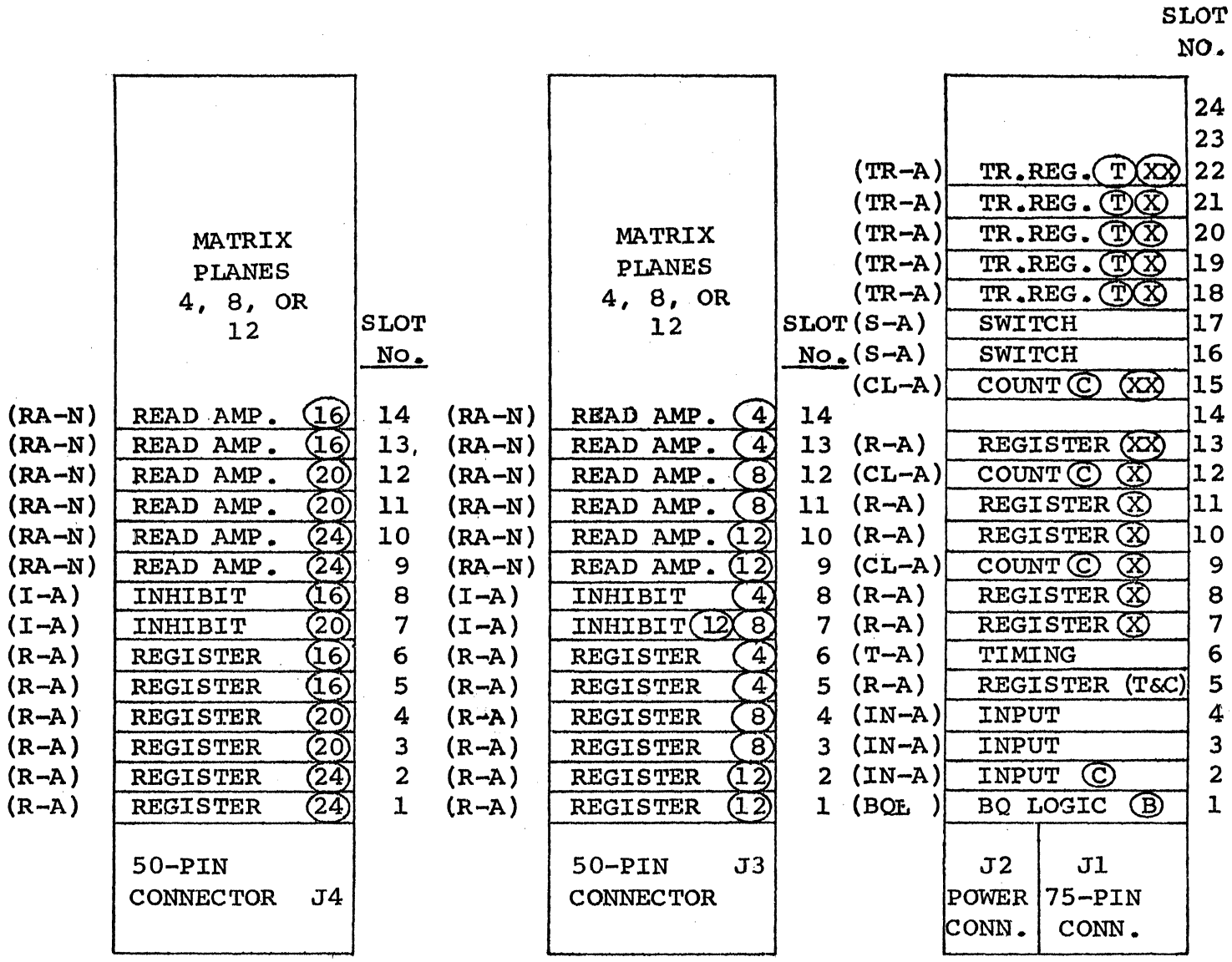
1-29. Although they are identical, the register cards in Card Cage A are used in the Address Register circuitry, while those in Card Cages B and C are incorporated in the Memory Register circuitry. Cards may be identified by the following letters stamped thereon: S-A, switch; R-A, register; RA-N, read amplifier; I-A, inhibit; IN-A, input; T-A, Timing; TR-A, transpose register; BQ-L, BQ Logic; and CL-A, count logic. They are also stamped with the assembly drawing number and issue letter.

1-30. MAGNETICS MODULE. The Magnetics Module (memory module) contains the ferrite storage cores which store the digital information bits. The cores are arranged on rectangular matrix planes with all the cores on a frame representing one digit plane. Each plane mounts the specific number of cores necessary to meet the address requirements of a particular model, and may contain a maximum of 1024 and a minimum of 128 cores. The number of planes will match the number of bits specified for the system model. On each matrix plane, coordinate X and Y windings support the cores and carry set and reset currents into the Magnetics Module.

1-31. READ AMPLIFIER CARD. A read amplifier delivers a binary ONE signal to the Memory Register when a selected storage core changes state (turns over) during a buffer unload or memory read operation. Two read amplifiers are mounted on a printed card. The number of printed cards is half the number of bits specified for the system.

1-32. TIMING CARD. A single timing circuit card contains the circuitry that generates timing and control pulses for the memory. Timing voltages sequence the several logical operations that constitute a complete buffer or memory cycle. Externally generated signals enter the timing card via an input card to initiate a buffer or memory cycle.

1-33. COUNT LOGIC CARDS. Either two or three count logic cards are used in the RB memory. If the memory has a capacity equal to or less



4 - 4-bit words
8 - 8-bit words
12 - 12-bit words
16 - 16-bit words
20 - 20-bit words
24 - 24-bit words

C - Count Network added
T - Transfer Register added
B - BQ Logic Added

X - 128 & 256 words
XX - 512 & 1024 words

Figure 1-2. Card Cage Configuration, Rear View

than 256 words, two count logic cards are used. If the memory has a capacity greater than 256 words, three count logic cards are used.

1-34. The count logic cards are used to enable the Address Register to be stepped up one address or stepped down one address. These cards also enable the Transpose Register to be set to the same address as the Address Register or to be set to the same address as the Address Register, plus or minus one digit.

1-35. REGISTER CARD. The register card is used as a temporary storage device in the Memory Register and Address Register, and as a logic element in the Timing and Control circuits. A register card contains two register circuits. Each register contains a flip-flop, four output inverters and two input gating circuits. Two inverters furnish an output to the external equipment; the other two provide gate levels to the RB system. Those inverters furnishing an output to the external equipment are clamped to deliver either a six or twelve volt swing. A mode selector at the input of each flip-flop permits a choice among a wide range of input modes.

1-36. SWITCH CARD. Thirty-two drive line switches are used to select one of 64 X and one of 64 Y matrix windings when information is transferred into or out of the Memory Module. The switches are gated by the Address Register and a timing register flip-flop. One group of 16 switches steers set (load) and reset (unload) currents through the X windings, the second group of 16 switches steers set and reset currents through the Y windings. Two printed cards contain the two sets of switches.

1-37. INHIBIT CARD. An inhibit card contains six inhibit drivers and six clear drivers; the system model determines the number of cards used. The inhibit drivers transfer information from the Memory Register to the Memory Module by preventing or permitting turn-over of address-selected storage cores during buffer or memory operations. Each inhibit driver is gated by a specific Memory Register flip-flop and controls information transfer into one specific matrix (digit) plane. The drivers prevent core turn-over by conducting through inhibit windings to cancel the effect of the Y current. Each clear driver passes current through an associated inhibit winding to force all of the cores in that plane to their reset (clear) state.

1-38. INPUT CARD. An input card receives externally generated synchronization and control signals, and inverts, amplifies, and shapes these voltages before delivery to the timing and register circuits. The output of this card consists of trigger pulses and

gating levels. The system model determines whether two or three input cards are employed.

1-39. TRANSPOSE REGISTER CARD. Transpose Register cards are used as temporary storage devices in the Transpose Register to accept and hold address information. The number of cards used in a register varies with the system model, but is always equal to the number of Address Registers. The Transpose Register is optional equipment.

1-40. BQ LOGIC CARD. A single BQ Logic card is used to furnish the RB Memory with a method of interlace operation that does not require an externally generated count pulse and transpose pulse for each address count or each address transposition. When selected, the BQ Logic circuits sense each load or unload command and deliver an attendant count or transpose pulse that controls the address in the Address Register during interlace operation. This card is optional equipment.

1-41. POWER SUPPLY. A single power supply that furnishes all of the d-c voltages is contained in a separate hinged chassis at the front of the assembly. The power supply output consists of seven regulated voltages and two temperature-compensated negative current supplies for the Memory Module. A voltage sensing circuit disables the power supply if any output voltage is not at its proper level. Swinging the hinged chassis outward provides access to a panel that mounts three control potentiometers, seven overload fuses, and two margin switches. A thermal switch inside the blower wind tunnel removes the primary 115 volt single phase a-c voltage for approximately one hour if the temperature reaches 85 degrees centigrade. A constant operating temperature is maintained by a 115 volt a-c blower.

1-42. INPUT-OUTPUT CHARACTERISTICS.

1-43. INPUT AND OUTPUT SIGNALS. Selection of word length, number of addresses, and incorporation of the Count Network, Transpose Register, or BQ Logic Card, must be performed by the manufacturer, but the user may select from a variety of polarities and amplitudes of output and input voltages. The input voltage range is established by the output levels chosen, as shown in Table 1-3.

1-44. Maximum current available in either polarity from any level is 6 ma. Rise or fall time depends on loading, and can vary from 0.05 to 0.3 usec under normal load variations.

TABLE 1-3. OUTPUT VOLTAGES AND INPUT EXCURSION LIMITS (INFORMATION, ADDRESS, AND CONTROL SIGNALS)

Outputs	Input Excursion Limits	Memory Reference Voltage
0 v (ONE) -6 v (ZERO)	-2 to +2 v -4 to -8 v	-3 v
+6 v (ONE) 0 v (ZERO)	+4 to +8 v -2 to +2 v	+3 v
0 v (ONE) -12 v (ZERO)	-4 to +2 v -8 to -14 v	-6 v
+6 v (ONE) -6 v (ZERO)	+2 to +8 v -2 to -8 v	0 v
+12 v (ONE) 0 v (ZERO)	+8 to +14 v -2 to +4 v	+6 v

Input excursion limits are absolute values, and must not be exceeded. All input and output voltages are referenced to the external equipment ground.

Output voltages are nominal. The following deviations may be encountered:

Output Voltage	Deviation
0 v	-0.2 to -0.4 v
±6 v	+0.1 to -0.7 v
+12 v	+0.4 to -1.0 v
-12 v	+1.0 to -1.0 v

1-45. SIGNAL LINES. The input-output connectors provide lines for each address bit into the Address Register, and for each bit out of the Address Register. Similarly, two lines are provided for each information bit into the Memory Register, and for each bit out of the Memory Register. However, input/output lines to the RB memory

can be either single or double-ended. Two lines, L and $\overline{L}$,furnish the Operating State signal from the Timing and Control circuits.

1-46. One wire each is provided for the following signals into the Timing and Control circuit: load sync, unload sync, master clear, clear AR (Address Register), clear MR (Memory Register) and Memory Operation. If d-c level information is applied to the Address and Memory Registers, one input is needed for strobe AR, and one for strobe MR. All control signals should possess amplitudes similar to the information and address inputs.

1-47. When the Count Network and Transpose Register are installed, one line each is required for count, forward, reverse, and transpose signals. When the BQ Logic card is installed, one line is required for BQ operation.

1-48. INPUT POLARITY. Positive or negative going pulses may be used for load and unload sync, master clear, strobe and clear AR, strobe and clear MR, and count and transpose signals. The count signal and the transpose signal each consist of a pulse used in conjunction with one of two levels. One level gates the count network forward, the other gates it in reverse. A positive or negative level, in association with a positive or negative sync pulse, is employed to select one of the two memory or two buffer operating modes. Positive or negative pulses, or double or single-ended levels are used for the Address and Memory Register inputs. A positive or negative level selects BQ operation.

1-49. The d-c currents on each input line are 4 ma for positive pulses or double-ended levels; 1 ma for negative pulses or double-ended levels; and 5 ma for positive or negative going single-ended levels. When the input voltage is positive with respect to the memory reference potential, the input d-c current is zero. The input capacitance of the unit is 200 mmfd.

1-50. TIMING. To operate the system at its maximum speed, all input pulses must rise within 0.2 usec, posess a duration of from 0.5 to 1.0 usec, and fall within 0.4 usec. A rise time as slow as 1.0 usec may be used, but the additional time in excess of 0.2 usec must be added to the cycle time. A rise time in excess of 1.0 usec will not trigger the input circuits, and hence, is unacceptable.

1-51. Zero time is defined as the instant when the load or unload sync pulse crosses the input reference voltage. The end of cycle for a buffer operation is 5 usec after zero time; for a memory operation it is 8 usec.

1-52. Inputs to either the Memory Register or the Address Register may be presented in one of the four following ways:

1. Double ended levels in conjunction with a strobe pulse.

2. Single ended levels in conjunction with a strobe pulse.

3. Double ended pulses.

4. Single ended pulses.

The strobe pulse (item 1 and 2) and the single or double-ended pulse must occur no sooner than 0.5 usec before the end of the previous command cycle and no later than zero time of the next cycle. Level inputs must be settled 0.25 usec before the application of the strobe pulse. Single-ended pulses require the register to be cleared at least 1.0 usec before application of the pulses. The clear pulse for this function must occur no sooner than 0.5 usec before the end of the previous cycle.

1-53. Timing for the count and transpose signals is the same as for AR and MR strobe signals. Forward and reverse signals must be settled at least 3.5 usec before a count or transpose pulse has crossed the reference voltage (zero time), and must not be changed until this occurs.

1-54. For a Memory Operation the MO line must be enabled at least 0.5 usec before zero time, and must maintain that state until 4 usec after zero time.

1-55. The master clear pulse may not be applied until after the end of cycle, and no other pulses may be transmitted to the system for an additional 25 usec. This pulse must not be applied again for 100 usec, and there shall be no more than 40 clear system pulses in any 10 millisecond period. An excessively high repetition rate may result in circuit failure.

1-56. The address output lines settle within 1.5 usec after being changed by the application of one of the following: AR strobe, address input pulses, count pulse, transpose pulse, AR clear, or master clear pulse. This address output remains available until it is changed by another input. During an Unload or a Read/Restore cycle the information output lines settle within 4.0 usec after zero time and maintain that state until changed by the application of one of the following: information input pulses, unload sync., MR clear, or master clear pulse. If the input causing the Memory register to

change is an unload sync, there is a 1.0 usec delay before any change occurs.

1-57. REFERENCE DATA.

(1)	Capacity	128 to 1024 words, 4 to 24 bits per word in two-bit increments
(2)	Operating Modes	Buffer load and unload, memory clear and write, and read and restore. Random or sequential access or interlaced load and unload
(3)	Speed	5 usec for buffer operation, 8 usec for memory operation
(4)	Load Rate	Asynchronous to 200 kc for buffer, 125 kc for memory operation
(5)	Clearing Time	25 usec
(6)	Input and Output levels	Inputs may be levels or pulses of either polarity, outputs are levels
(7)	Output Level Rise & Fall Time...	0.175 ± 0.125 usec
(8)	Input Pulses or Levels	
	a. Rise Time	0.2 usec
	b. Duration	0.75 ± 0.25 usec
	c. Fall Time	0.4 usec
(9)	Power Requirements	Less than 250 watts from 115 ± 15 volts, single phase 60^{+3}_{-12} cps.

(10) Environment

a.	Operating Ambient Temperature ...	+32°F to +122°F, occasional excursions to + 158°F
b.	Storage Conditions	-4°F to + 158°F
c.	Relative Hunidity	0% to 90%

(11) Dimensions

a.	4 to 12 Word Bit Models	19 x 10-1/2 x 16 inches
b.	14 to 24 Word Bit Models	19 x 15-3/4 x 16 inches

(12) Weight ..... 95 lbs. maximum net weight
193 lbs. maximum shipping weight

(13) Mounting ..... Standard 19-inch rack. Western Electric notching

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. GENERAL. This section contains instructions for installing the Type RB General Purpose Memory. Preliminary checks are included to determine that the system is operational.

2-3. UNPACKING.

2-4. SHIPPING CONTAINERS. The power supply and the memory assembly are packed and shipped in separate packing cases. Each unit is packed in a corrugated container; fiberboard end plates (G-packs) provide rigid internal support. The container is placed inside a plywood packing case, and is supported by eight rubber corner blocks. The packing case cover is nailed in place.

2-5. When unpacking, a crowbar may be used to pry the top off the packing cases. Open the corrugated containers and lift the units out, then remove the G-packs. Packing materials should be retained for possible future reshipment.

CAUTION

Exercise extreme care to avoid damaging the units while opening the crates and removing the contents. Do not disturb the setting of any adjustment control.

2-6. Examine the equipment as soon as it has been unpacked. Report any damage at once to the shipper.

2-7. EQUIPMENT SUPPLIED. In addition to the RB General Purpose Memory the shipping cases contain two or three input-output connectors, a Winchester MRA-75S-JTC6 and one or two Winchester MRA-50S-JTC6, and a power connector, Cannon MS 3106E 14S-2S (2).

2-8. CABLING INSTRUCTIONS.

2-9. ASSEMBLING UNITS. The power supply is hinge-mounted at the front of the system (Figure 5-1). Before shipment, the power supply was detached from the hinge by removing four mounting screws, and

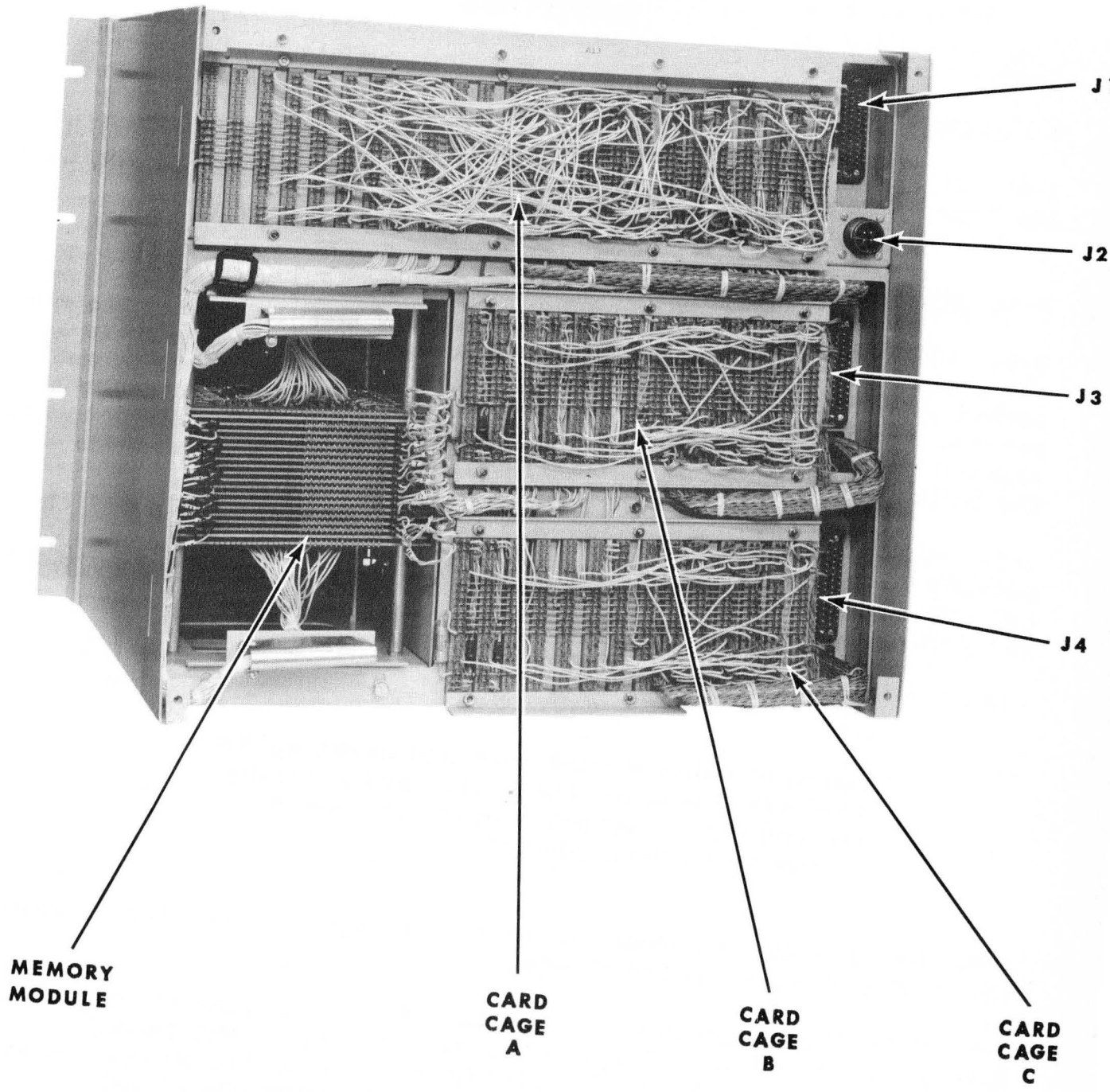


Figure 2-1. Type RB General Purpose Memory, Rear View

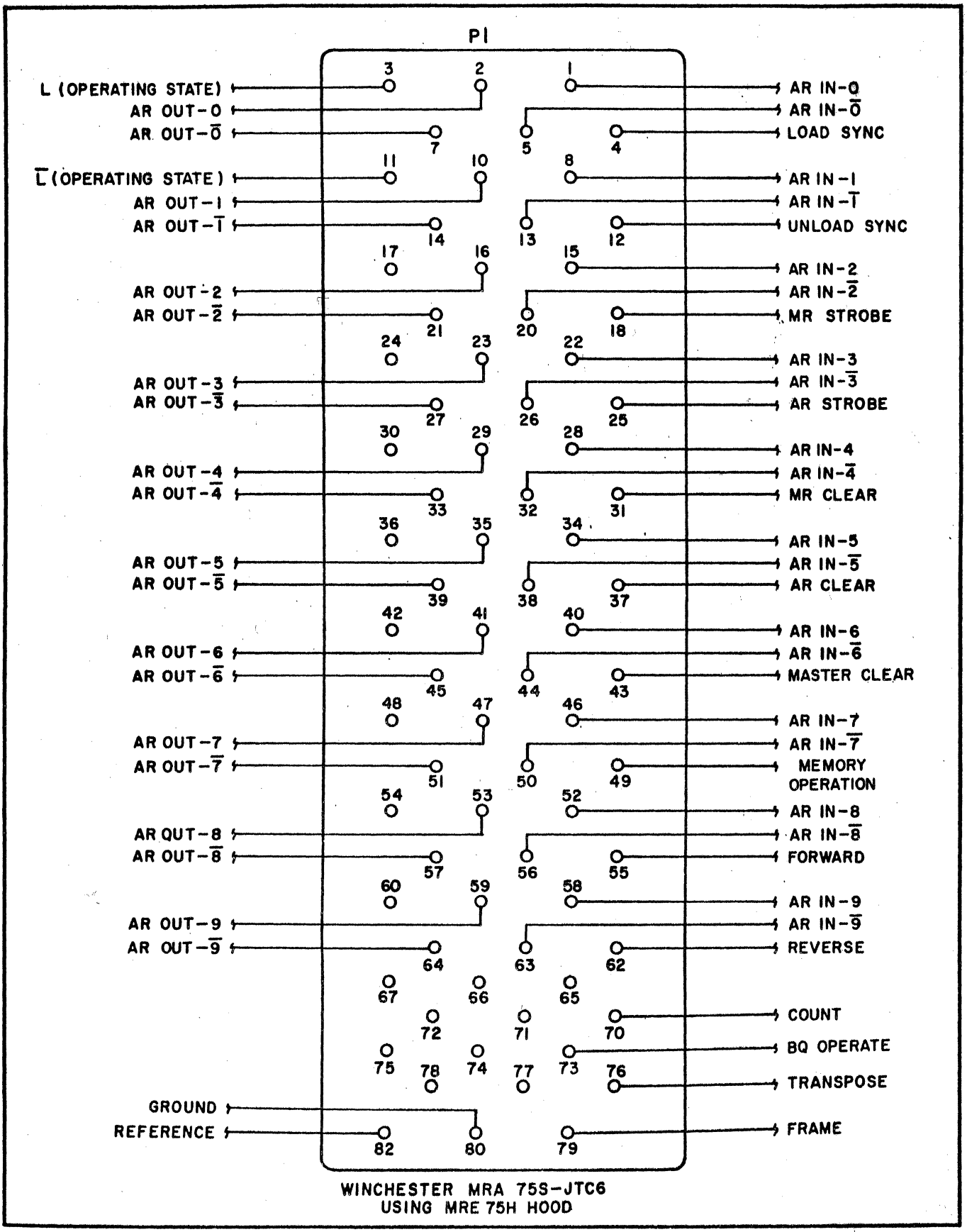


Figure 2-2. Input-Output Connector, Address In-Out and RB Control Inputs

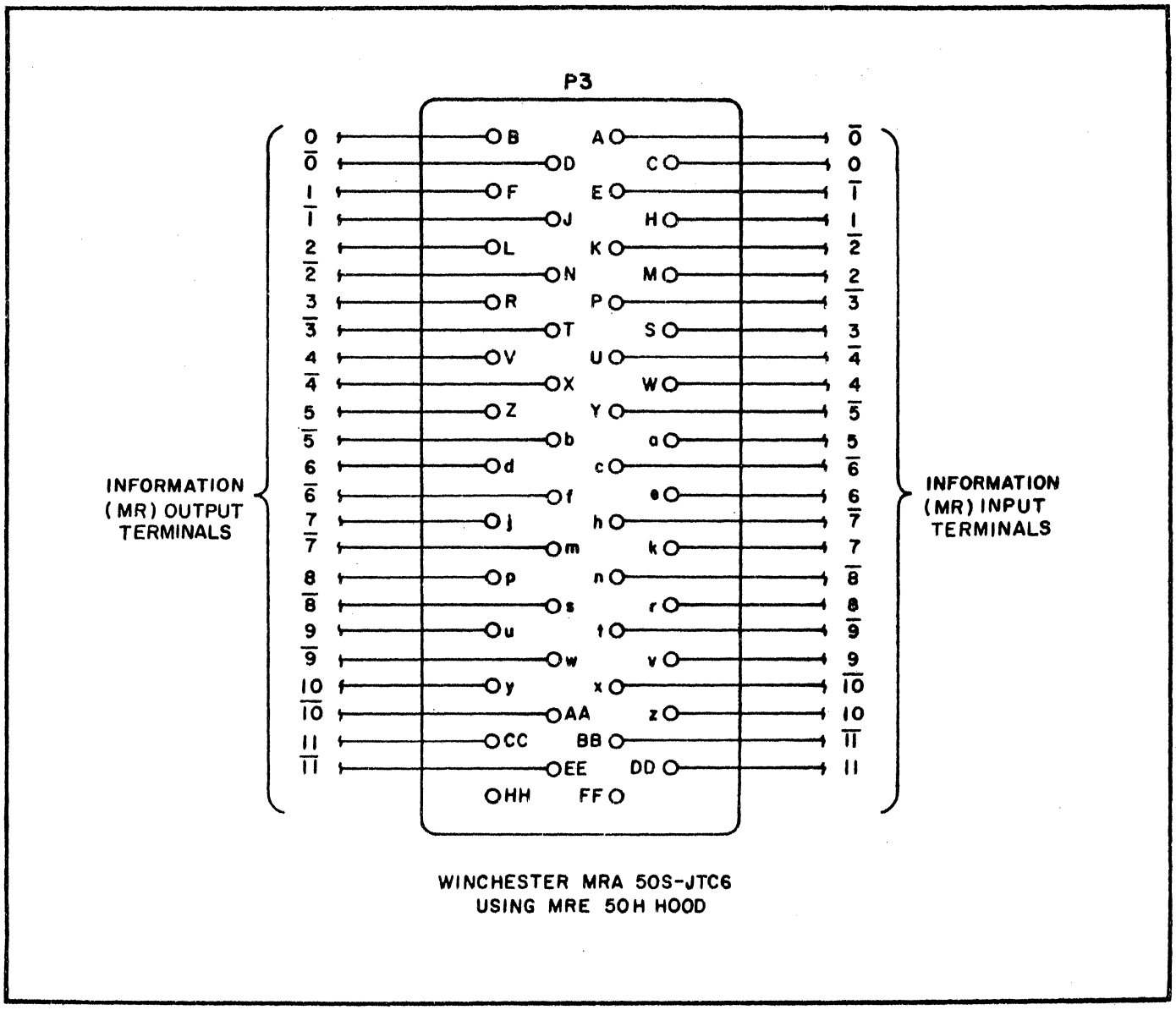


Figure 2-3. Input-Output Connector, Information In-Out

the screws were then re-inserted in the frame. Prior to attaching the cable connectors, mount the power supply, using the four screws to attach it to the hinge.

2-10. INPUT-OUTPUT CABLES. The Winchester connectors, used to connect the memory system with external equipment, are to be wired as shown in Figures 2-2 and 2-3. Figure 2-2 shows address input and output connections for a 1024-word system. When installing a smaller system, connect only the lines required. If any of the P1 connector pins listed below are not used, they should be connected to the voltage level that represents a logical "0" (at the external equipment).

Any Address Register input
MR Strobe (Pin 18)
AR Strobe (Pin 25)
Master Clear (Pin 43)
MR Clear (Pin 31)
AR Clear (Pin 37)
Forward (Pin 55)
Reverse (Pin 62)
Count (Pin 70)
Transpose (Pin 76)
Memory Operation (Pin 49)
BQ operate (Pin 73)

Figure 2-3 shows information input and output connections for a 12-word-bit system. For fewer word-bits, connect only the lines required.

2-11. External equipment connections to the input-output connectors shown in Figures 2-2 and 2-3 are determined by the customer's choice of input signals. All address and information signals are applied to the register circuits via input selector switches mounted on each printed card. These selectors are positioned to provide circuit compatibility with any one of the inputs listed in (1) through (7). The register card circuit description in Section IV describes the input selectors and input-output circuits in detail.

(1) A double-ended level

(2) A single-ended level with a negative voltage representing a logical ONE

(3) A single-ended level with a positive voltage representing a logical ONE

(4) A double-ended positive going pulse

(5) A double-ended negative going pulse

(6) A single-ended positive going pulse

(7) A single-ended negative going pulse

2-12. Table 2-1, Input Connections, indicates input connections to the RB memory for each of the seven possible inputs. Only pins A and C, the 0 and $\overline{0}$ lines to the Memory Register flip-flop, are

described. Connections to all other Memory or Address Register inputs lines can be similarly treated. Signal inputs (1) through (7) in Table 2-1 are defined in paragraph 2-11.

TABLE 2-1. INPUT CONNECTIONS

Signal Input		Input Selector Position
(1)	To load a logical ONE from the external equipment, connect the input line which is more positive than its complement to terminal C. Connect the more negative line to terminal A.	C
(2)	Connect the input line to terminal A.	D
(3)	Connect the input line to terminal C.	B
(4)	To load a logical ONE from the external equipment, connect the pulse line to terminal C; to load a logical ZERO, connect the pulse line to terminal A. Both lines must be connected.	A
(5)	To load a logical ONE from the external equipment, connect the pulse line to terminal A; to load a logical ZERO, connect the pulse line to terminal C. Both lines must be connected.	C
(6)	Connect the input line to terminal C.	A
(7)	Connect the input line to terminal A.	C

NOTE

Paragraph 2-11 describes signal inputs (1) through (7).

2-13. RB memory output connections to the external equipment are not described in Table 2-1. Each of the seven possible inputs enables a register flip-flop to produce a high (positive with respect to its complementary output) output when a logical ONE is applied to the memory. The two complementary outputs from each register flip-flop are brought to their associated input-output

connector terminals. A non-negated terminal is always high when a logical ONE is applied to its associated input lines.

2-14. When a logical ONE is loaded at input terminals C (0) and A ($\overline{0}$), output terminal B (0) is always high, terminal D ($\overline{0}$) is low. All other input-output terminals can be similarly described. When single-ended inputs are applied, all unused address and information lines are connected to the voltage that represents a logical ZERO at the external equipment. Connections to the RB memory output terminals are determined by external equipment requirements.

2-15. For an RB memory employing 14 or more word-bits, a second Winchester MRA 50S-JTC6 connector is provided. It is to be wired the same as Figure 2-3, starting with input 12 and continuing. For example, INFO OUT-12 goes to Pin B, INFO OUT-$\overline{12}$ to pin D, INFO IN-12 to Pin C, and INFO IN-$\overline{12}$ to Pin A. Continue down the connector as far as word bits require, up to 24.

2-16. Use No. 22 wire to connect all input and output lines. Keep all lines short, and route them as far from noise sources as possible.

2-17. The RB memory system uses a circuit ground that is always referred to as zero volts. The circuit ground may or may not be connected to chassis ground, depending upon the output voltages selected by the customer. The frame should be grounded to the external equipment using the frame connection (Pin 79 in Figure 2-2) and 16 gauge wire.

2-18. POWER CABLE. Connect the a-c power cable to pins A and B of the Cannon connector as shown in Figure 2-4. Two connections, pins C and D, are provided for wiring an optional remotely-mounted push button switch. This switch or the front panel START switch may be used to start the power supply. As a further alternative, a jumper may be installed across pins C and D to immediately initiate operation of the power supply whenever 115 volts a-c power is applied. A remote stop can be initiated by opening the 115 volt input circuit to terminals 17 and 18 on terminal strip TS-1.

2-19. PRELIMINARY CHECKS.

2-20. TEST EQUIPMENT. The following checks require a Tektronix Type 531 oscilloscope and a Simpson Model 260 multimeter or their equivalents.

2-21. EXTERNAL SOURCES. Check that the input signals conform to the requirements outlined in Paragraph 1-42, and that the power source meets the specifications of Paragraph 1-56 (9).

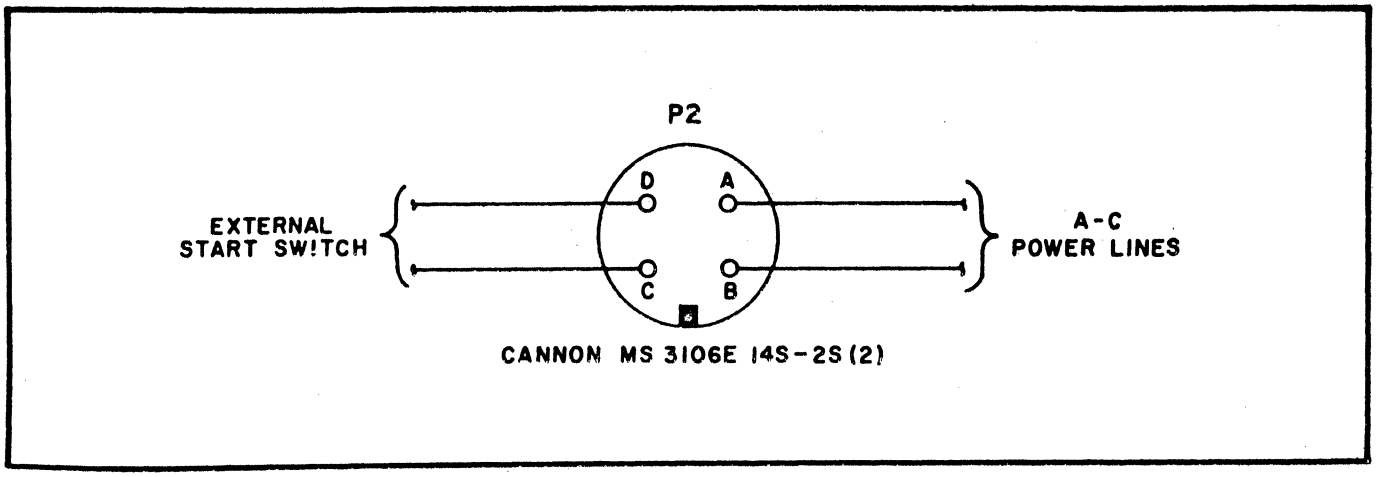


Figure 2-4. Power Connector Wiring

NOTE

Attach the input-output connectors before starting the following checks.

2-22. APPLICATION OF POWER. Attach the a-c power connector. Note that the green START light on the front panel is illuminated, indicating 115 volts a-c is available to the power supply. Depress the green START push button, and note that the amber STOP lamp lights, indicating power supply operation. If this sequence is interrupted, consult the power supply trouble-shooting procedures in Section V, Maintenance.

2-23. Check all power supply output voltages.

2-24. INSTALLATION. The RB memory system may be installed in a standard 19-inch relay rack, and has Western Electric notching. Equipment may be mounted immediately below the system, but a space of at least 3/8 inch is required between the unit and equipment above it. The system will operate continuously in temperatures from 32° to 122°F, with occasional excursions to 158°F. It will tolerate any humidity between the limits of 0% to 90%.

SECTION III
OPERATION

3-1. INTRODUCTION.

3-2. This section lists RB General Purpose Memory indicators and controls, explains the modes of operation, and contains operating instructions.

3-3. INDICATORS AND CONTROLS.

3-4. Two indicator lights are housed in push button switches on the front panel. When the green lamp on the left, labelled START, is illuminated, power is available to the power supply. When the amber light on the right, labelled STOP, is illuminated, the power supply is functioning and all d-c voltages are at their prescribed levels.

3-5. The two push button switches are used to control power supply operation. The START button places the supply in operation, and the STOP button halts its operation.

NOTE

If a jumper was installed across pins C and D of the Cannon power connector during installation, the START switch is inoperative, and the power supply should operate whenever 115 volts a-c is applied. These instructions assume that the jumper was not installed.

3-6. Seven fuses are mounted on the rear panel of the power supply. Their ratings are indicated below.

F1 - 4 amperes	F4 - 5 amperes
F2 - 8 amperes	F5 - 3 amperes (slow blow)
F3 - 3 amperes	F6 - 3 amperes (slow blow)
F7 - 2 amperes	

If the amber lamp does not light when the START button is depressed, or if it stops burning during operation, the operator should check for blown fuses or a burned out lamp. Also mounted on the panel are three screwdriver-adjustable controls; two are voltage controls, the third controls the sensitivity of a voltage sensing circuit. Two margin switches are used to vary the power supply outputs.

Voltage levels should be checked monthly as a part of the regular preventive maintenance routine.

3-7. OPERATING MODES.

3-8. GENERAL. The four basic operating modes of the RB General Purpose Memory consist of: buffer load, buffer unload, memory clear and write, and memory read and restore. The buffer mode commands require 5 usec for each execution, the memory mode commands are executed in 8 usec.

3-9. BUFFER LOAD. In this mode, one information word is transferred from the Memory Register into the storage cores at a selected address when a buffer load command is applied. The number of words stored is only limited by the capacity of the Magnetics Module, but each word requires a separate load command. Unless an optional count logic card is used, an externally generated address is necessary for each buffer load command.

3-10. BUFFER UNLOAD. This mode transfers one information word out of the storage cores at a selected address and into the Memory Register when an unload command is applied. Separate unload commands are required for each word read out of the Magnetics Module. Unless an optional count logic card is used, an externally generated address is necessary for each buffer unload command.

3-11. The addition of optional count logic cards furnish the RB system with a count network that permits sequential address operation without the application of an externally generated address for each command. This permits loading or unloading words at consecutive addresses in forward or reverse sequence. For each command, an externally generated control voltage instructs the count network to increase or decrease the Address Register (or Transpose Register, if used) by one digit, or to leave the address unchanged.

3-12. The addition of both an optional count logic card and the optional Transpose Register furnishes the system with interlace capability. Interlace consists of the following operations:

(a) Load at an address or a series of consecutive addresses.

(b) Unload an address or a series of consecutive addresses beginning at the first address loaded.

(c) Alternate load and unload commands and maintain address continuity for all load commands and all unload commands.

Paragraphs 4-66 through 4-68 furnish a detailed description of interlace operation.

3-13. Inclusion of an optional BQ Logic card in the RB system furnishes a method of interlace operation without the normally added requirement of an externally generated count pulse and transpose pulse. Paragraphs 4-71 through 4-73 furnish a detailed description of interlace using a BQ Logic card.

3-14. MEMORY CLEAR AND WRITE. Memory clear and write clears (sets to ZERO) all of the storage cores at a selected address in the Magnetics Module and then loads these cores with an information word. A clear and write command is required for each word loaded. Information is not read out when the cores are cleared.

3-15. MEMORY READ AND RESTORE. Memory read and restore transfers an information word from the storage cores at a selected address to the Memory Register when a read and restore command is applied. The read process consists of resetting all cores at a selected address to ZERO if they are in the ONE state. This is termed destructive readout. During the read portion of the cycle, all of the ONE state cores are set to ZERO and the information is transferred to the Memory Register. During the restore portion of the cycle, the Memory Register information is rewritten back into the same address from which it was taken, but is still retained by the Memory Register. A read and restore command is required for each word unloaded.

3-16. OPERATING PROCEDURE.

3-17. The following steps outline the procedure for starting, operating and stopping the system.

(1) Check that the input-output and a-c power connectors are firmly attached and locked by their retainers.

(2) Determine that the system is receiving a-c power by noting that the green START lamp is lighted. If the START lamp is not lighted, check fuses F5 and F6 at the rear of the power supply, and determine that the lamp is not burned out.

(3) With the system receiving a-c power, depress the green START push button. Determine that the power supply is operating properly by noting that the amber STOP lamp is lighted.

(4) If the amber STOP lamp does not light when the green START push button is depressed, check for burned out power supply fuses F1 through F4, fuse F7, or a defective STOP lamp.

(5) Apply an external master clear pulse, to clear the Address and Memory Registers and the Magnetics Module. The RB Memory system is now ready for buffer or memory operation.

(6) Should the indicator lamps stop illuminating during operation, loss of power and malfunction of the power supply is indicated. This may result from overheating, which opens the 185°F temperature switch in the a-c power input line. The switch will not close for at least one hour after opening, during which time the system is not operable.

NOTE

Information stored in the buffer storage system is usually destroyed if power is removed.

(7) To stop system operation, depress the amber STOP push button. The STOP lamp will be extinguished, indicating that the power supply is no longer operating. The green START lamp will remain lighted, showing that a-c power is available for resumption of operations.

3-18. INPUT AND OUTPUT INFORMATION. Address and information is presented to the system in the form of d-c levels or pulses on the parallel input lines. If information is in the form of levels, AR and MR strobe pulses must be provided for the Address and Memory Registers.

3-19. System operation is always initiated by a load or unload sync pulse. Zero time in a cycle is defined as the instant at which this pulse crosses the input reference voltage. AR and MR strobe pulses are applied at or before zero time. The voltage level (MO) which determines whether the system will operate as a buffer or memory must be applied 0.5 usec prior to zero time, and must be maintained until 4 usec after zero time.

3-20. In a buffer load operation, address and information out are available 1.5 usec after zero time. This information may be used for checking or timing purposes. In a buffer unload operation,

address out is available at zero time plus 1.5 usec, with information available at zero time plus 4 usec.

3-21. In a memory operation, address out is available at zero time plus 1.5 usec. In memory read and restore, information out is available at zero time plus 4 usec.

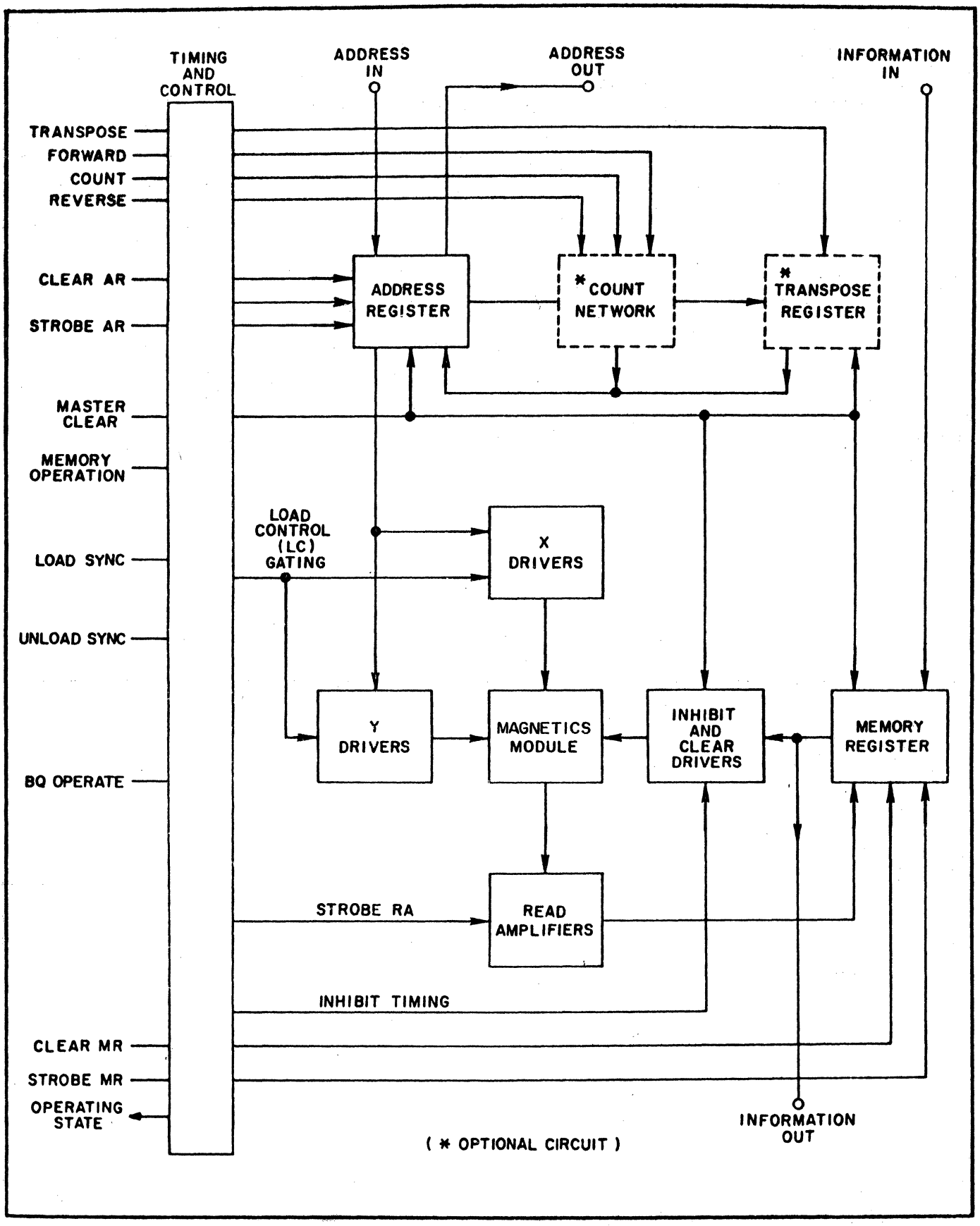


Figure 4-1. Type RB General Purpose Memory Block Diagram

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION. This section explains the operation of the Type RB General Purpose Memory. The system operates as a buffer or memory. The basic unit provides random access to the ferrite core Magnetics Module; addition of optional equipment makes sequential (count) access or interlaced load and unload possible.

4-2. GENERAL THEORY.

4-3. BASIC CIRCUITS. A functional block diagram of the system is shown in Figure 4-1. The basic system is indicated by solid lines, with dashed lines signifying optional equipment. The memory system uses modular construction, and, with the exception of the Magnetics Module, is mounted on nine types of cards. Cards of differing types may be incorporated in one of the functional blocks shown. Each card type is discussed under Detailed Theory, and the following paragraphs describe the functional circuits.

4-4. TIMING AND CONTROL. The Timing and Control circuits generate voltages which sequence system functions during an operation cycle. They include input cards, a timing card and a register card. An additional input card is included when the optional Count Network or Transpose Register is used. A BQ logic card is used for interlaced load and unload operations.

4-5. Each input card contains two d-c amplifiers, two pulse generators, an inverter and a current switch. All externally generated signals, except address and memory information, are amplified and shaped by the input cards before being applied to their respective circuits.

4-6. The register card contains two flip-flops and is identical to the register circuits employed in the Address and Memory Registers. One of the flip-flops is termed LC (load control), the second is termed L/U (load-unload). LC furnishes levels that determine whether the X and Y drive switches energize set or reset drive lines, and also enables the inhibit timing pulse during a memory or a buffer load operation (set drive lines energized). L/U provides levels that gate the read strobe and determine whether the Memory Register should be cleared during a memory or buffer cycle.

4-7. The Timing and Control circuits control the four basic operating modes listed in (a) through (d):

(a) Buffer load

(b) Buffer unload

(c) Memory clear and write

(d) Memory read and restore

4-8. BUFFER LOAD. A buffer load is initiated by a load sync pulse in conjunction with a disabled MO (memory operation) control level. The load sync sets flip-flops L/U and LC and is applied to a 1 usec delay circuit whose output triggers a drive timing generator. A 2.5 usec drive timing voltage operates the drive line switches selected by the Address Register (AR). The trailing edge of the timing pulse resets LC. During the 3.5 usec that it is in the set state, LC enables those X and Y switches used for loading, disables those used for unloading, and furnishes a gate that times the inhibit currents to the desired part of the operating cycle.

4-9. BUFFER UNLOAD. A buffer unload is initiated by an unload sync pulse in conjunction with a disabled MO control level. The unload sync resets flip-flop L/U and is applied to a 1 usec delay circuit whose output drives the X-Y timing and clear MR (Memory Register) gate circuits. A 2.5 usec drive timing voltage operates the drive line switches selected by the AR. Read strobe RA is produced when the timing pulse leading edge triggers the strobe generator. Strobe RA enables the read amplifiers to apply amplified core turn-over signals to the Memory Register. The clear MR gate produces a positive MR clear pulse that operates the clear MR generator.

4-10. MEMORY CLEAR AND WRITE. A memory clear and write is initiated by a load sync pulse in conjunction with an enabled MO control level. The load sync sets flip-flop L/U and is applied to a 1 usec delay circuit whose output operates the MR gate and the X-Y timing generators. A 2.5 usec drive timing voltage operates the address selected drive line switches to reset (clear) all cores at the desired address only. A second timing voltage is produced when the trailing edge of the initial X-Y pulse is applied to the 1 usec delay circuit and X-Y generator. Flip-flop LC is set by this trailing edge, and reset when the second timing pulse falls.

4-11. While in the reset state during the first 3.5 usec of the operating cycle, LC enables those address selected X and Y switches used to reset the storage cores to ZERO (clear state), disables those switches used to set the cores to ONE. During the 3.5 usec period that it remains in the set state, LC enables those address selected X and Y switches used for writing (loading), disables those

used for reading (unloading), and furnishes a gate that times the inhibit currents to the write portion of the cycle. Because the trailing edge of the second timing voltage finds LC in the set state, it is unable to initiate a third X-Y pulse.

4-12. MEMORY READ AND RESTORE. A memory read and restore is initiated by an unload sync pulse in conjunction with an enabled MO control level. The unload sync resets flip-flop L/U and is applied to a 1 usec delay circuit whose output operates the drive timing generator and clear MR gate. A 2.5 usec drive timing voltage operates those drive line switches selected by the Address Register. Read strobe RA is produced when the timing pulse leading edge triggers the strobe generator. Strobe RA enables the read amplifiers to apply amplified core turn-over signals to the Memory Register. The MR clear generator produces MR clear to set the Memory Register to zero.

4-13. A second drive timing voltage is produced when the trailing edge of the initial X-Y pulse is applied to the 1 usec delay circuit. Flip-flop LC is set by this trailing edge, and reset when the second X-Y pulse falls. While in the reset state during the first 3.5 usec of the operating cycle, LC enables those selected X and Y switches used to reset the storage cores to ZERO (clear state), disables those switches used to set the cores to ONE. During the 3.5 usec period that it remains in the set state LC enables those address selected switches used for writing (restore), disables those used for reading, and furnishes a gate that times the inhibit currents to the restore portion of the cycle.

4-14. MASTER CLEAR. A master clear pulse applied to the clear generator resets all of the Address and Memory Register flip-flops, and drives the clear amplifiers in the Inhibit and Clear Drivers circuit. Clear currents are applied to each core in the Magnetics Module, resetting all memory cores to the ZERO state.

4-15. MAGNETICS MODULE. The Magnetics Module contains the ferrite cores that store the information presented to the RB system. Its operation results from the ability of ferrite cores to be magnetized in one of two possible states, and to maintain that state indefinitely until it is electrically changed.

4-16. The Magnetics Module is made up of a number of horizontal matrix planes containing the X and Y drive lines on which the ferrite cores are strung. The planes are identical in size and are stacked in a vertical array. The number of cores per plane varies with the address requirements of the system. The 1024-word system uses 1024 cores per plane, arranged in a 32 X 32 array. The cores are strung in 32 horizontal rows and 32 vertical columns, with a core at the

intersection of each row and column. A 512-word system has 32 rows and 16 columns, a 256-word system 16 rows and 16 columns, and a 128-word system 16 rows and 8 columns.

4-17. The number of planes is determined by the bits-per-word requirements of the system. Since the number of bits per word can vary from 4 to 24 in steps of two, the minimum number of planes in a Magnetics Module is 4, and the maximum number 24.

4-18. Through the arrangement of cores in coordinate rows and columns, it is possible to locate the core associated with a particular word by determining the intersection of a row and column. The same core location is maintained on each plane. By addressing that location on every plane, all bits of the word can be loaded (written) or unloaded (read).

4-19. The two states of magnetization of a core are shown by the hysteresis loop of Figure 4-2. When the full switching (full-select) current passes through a core in one direction, it is magnetized in the ONE state. Reversing the current returns the core to the ZERO state. If two wires pass through a core, a half-select (half-switching) current through each in the same direction is sufficient to set the core. It is convenient to use the wires to support the cores with the horizontal wires providing the X drive, and the vertical wires furnishing the Y drive, as shown in Figure 4-2.

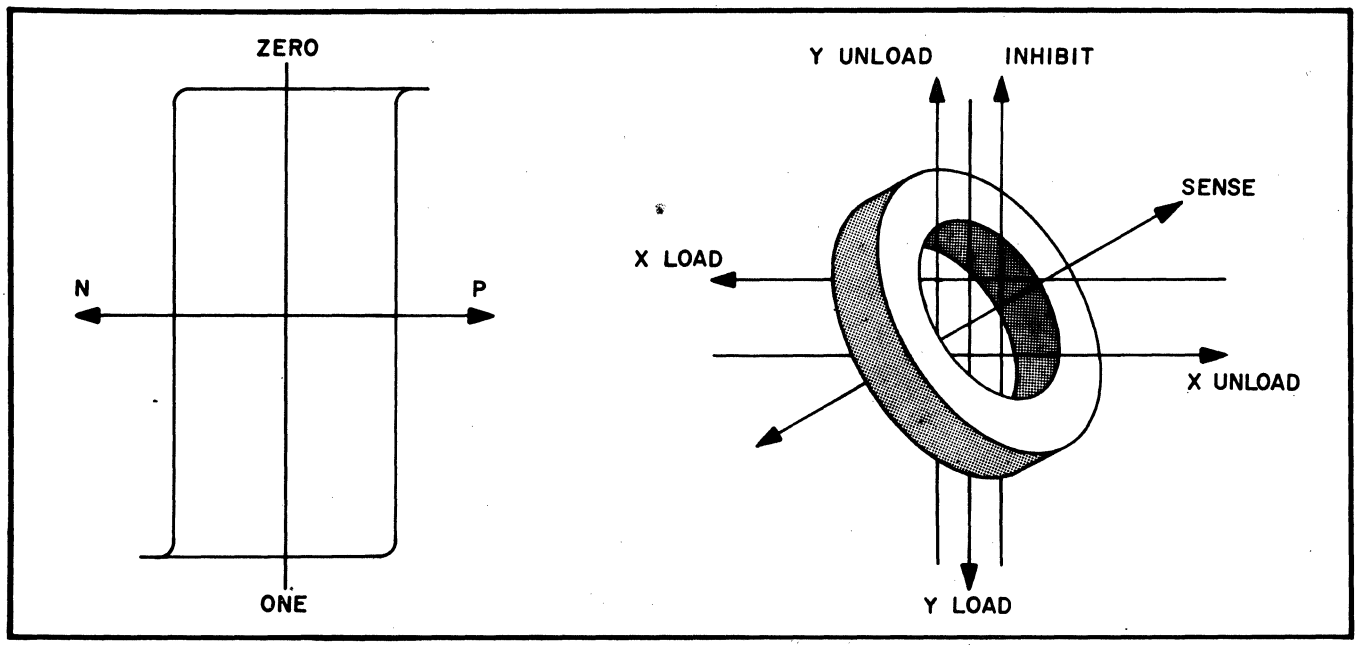


Figure 4-2. Storage Core Hysteresis Loop and Core Windings

4-20. Rather than reverse the current in a single wire to change the magnetic state of a core, two separate wires, termed set drive line and reset drive line respectively, are used. The ONE state is induced by half-select currents through X and Y set lines, and the ZERO state by half-select currents through X and Y reset lines. If current passes through the Row 3 X set line, a half-select current will pass through all the cores in that row, and if current passes through Column 3 Y set line, a half-select current passes through all the cores in that column, but it is only the core at the coincidence of Row 3 and Column 3 which receives the full current and hence is set to the ONE state.

4-21. All X and Y drive lines are wired continuously from one digit plane to the next. Continuing the above description, this would tend to set all of the cores at the intersection of Row 3 and Column 3 to the ONE state. Since a word normally contains some ZEROs, it may be necessary to inhibit the load (write) process on one or more planes, and this is the purpose of the inhibit line shown in the figure. With the inhibit half-select current opposing the Y set half-select current, the two cancel out as far as their effect on the core is concerned, and the X load half-select current does not set the core to ONE. Unlike the X and Y lines which continue through the entire matrix stack, there is an individual inhibit winding for each plane that links all cores in that plane. If it is energized, the load operation is inhibited in that plane, otherwise it is not.

4-22. Applying a half-current to specific X and Y reset drive lines will reset the selected magnetic core in each plane to the ZERO state. If it is already in the ZERO state, the core will not be affected. With the sense line shown in Figure 4-2 passing through the core, the changing flux in the core when it goes from ONE to ZERO, induces a voltage in the sense line. Since a sense line is provided for each digit plane, it is possible during an unload operation to determine which planes had been loaded with a ONE at a selected address, and which had not. This is the read operation, with the sense winding outputs of all planes applied to the Read Amplifiers, one Read Amplifier for each digit plane. The readout process is destructive; all cores at the address being read are set to the ZERO state during an unload operation. This effect can be negated by a regenerative readout, in which unload is followed by a load operation that writes the information back into the Magnetics Module. Passing a full core switching current through the inhibit winding in each plane will clear the memory, resetting all cores to ZERO. This is accomplished during a system clear operation by turning on a set of clear drivers. There is one clear driver and one inhibit driver for each inhibit winding.

4-23. Figure 4-3 illustrates the placement of cores in a digit plane. They require no further support than that provided by the windings. The X set and Y set currents reverse directions alternately, making it possible to thread the inhibit line as shown. X and Y reset windings are not shown. They run parallel to the set lines, but their currents flow in a reverse direction to those shown for the set windings. The sense winding is shown passing through half of the cores.

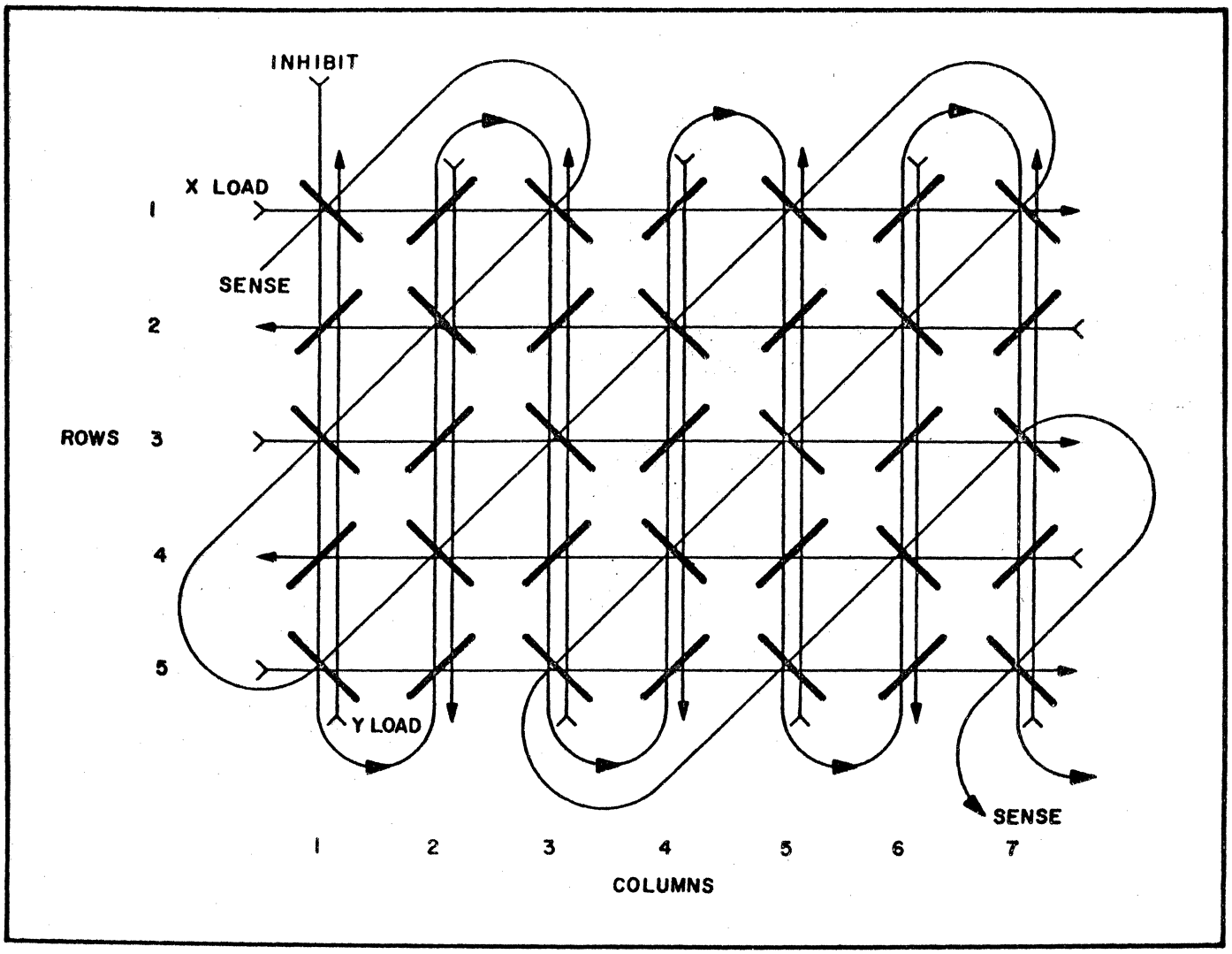


Figure 4-3. Placement of Cores on Matrix Assembly

4-24. ADDRESS REGISTER. The Address Register (AR) consists of register flip-flops. The number of flip-flops is established by the number of addresses in the Magnetics Module; a maximum of ten are required for 1024 words, a minimum of seven for 128 words. The Address Register receives and temporarily stores the address that

is used to select a specific group of Magnetics Module storage cores. An address is applied to the AR in the form of d-c levels in conjunction with an externally generated AR strobe; or the address may be applied as pulses without an attendant strobe. At the start of each cycle, the AR contains a group of digits that represents the address (Magnetics Module storage location) at which the subsequent command will load or unload binary information.

4-25. When operated with a count logic card the AR can be counted forward one digit, or in reverse one digit, with each operation. This enables the RB system to load or unload consecutive memory addresses without requiring an externally generated address for each command.

4-26. Information in the AR is used to simultaneously select two of sixteen X drive line switches and two of sixteen Y drive line switches for each operation. The Address Register can be set to zero address (all zeros) by an externally generated master clear pulse only when the system is not operating with BQ logic.

4-27. X AND Y DRIVE SWITCHES. (See Figure 4-4.) The 16 X and 16 Y drive line switches receive address levels from the Address Register which enable them to energize Magnetics Module drive lines associated with each address. X and Y switch operation is identical, so only the X will be described. A full complement of 32 switches is provided in every RB system, although fewer are required for those systems using less than 1024 addresses.

4-28. The maximum memory configuration mounts 1024 cores in each digit plane and requires 64 X set (read) and 64 X reset (write) lines. Smaller Magnetics Modules use a reduced number of switches, drive lines and AR inputs. The 16 drive line switches are arranged in two groups of eight. Every address selects two switches, one in group A, one in group B. A selected pair of switches will energize either a set or reset drive line by permitting current from the X-Y drive current supply to flow through the one line that is in series with their outputs.

4-29. The specific pair of switches selected for each address depends on whether a set (write) or reset (read) current is desired. This is accomplished by including the LC flip-flop as a gate term on the A bank of switches. Two switches are enabled when level $\overline{LC}$ is high during read; two different switches are enabled when level LC is high during write.

4-30. X AND Y CURRENT SWITCHES. (See Figure 4-4.) An X current switch and a Y current switch respectively control the X and Y

drive line current amplitudes. When quiescent, the switches are closed and function as very low impedance shunts across the drive lines. The drive line current is held close to zero amperes. A timing pulse opens the current switches and permits NCS current to flow through the selected drive line circuits. Each current switch is contained on an input card.

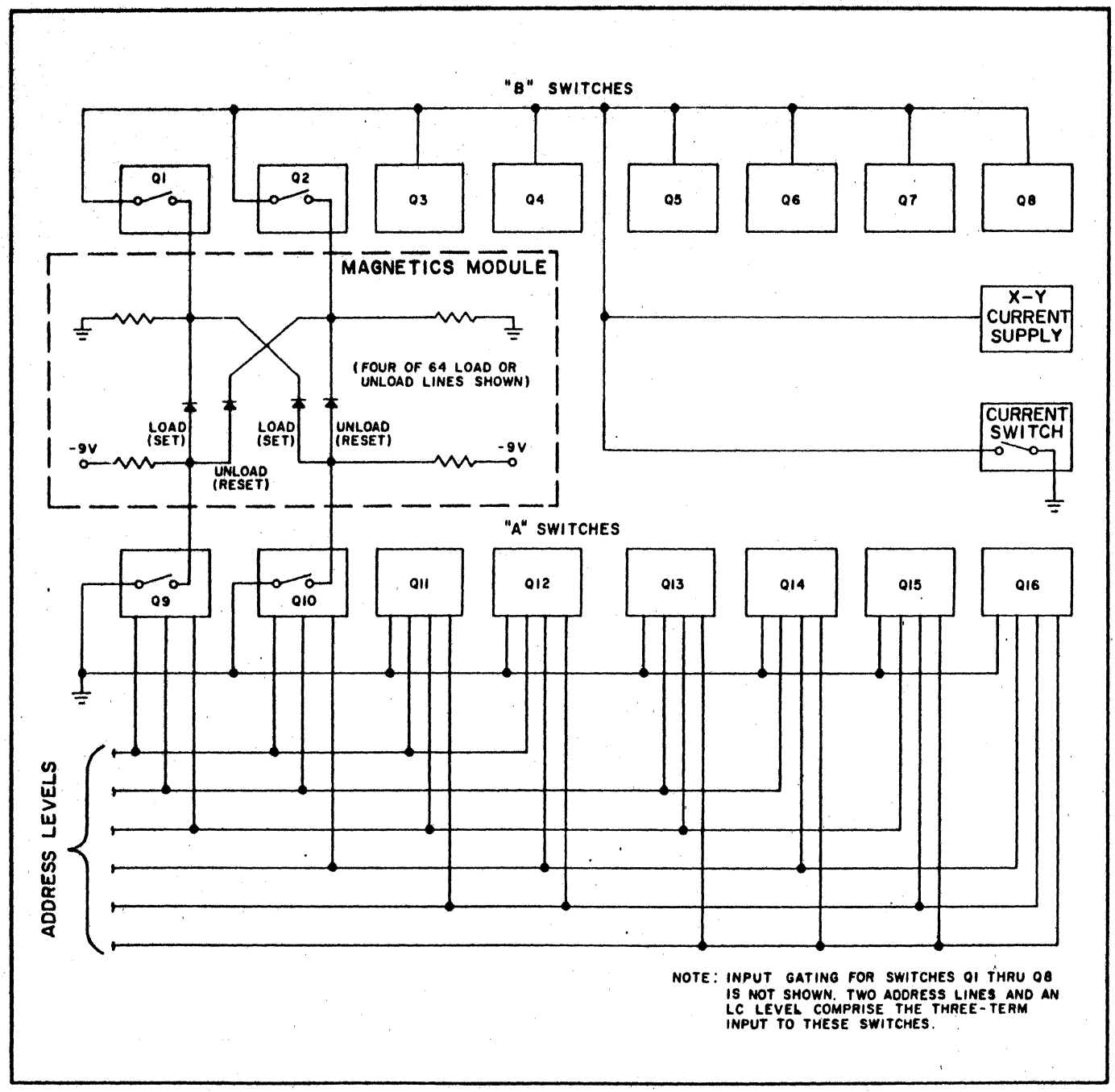


Figure 4-4. Simplified Schematic, X or Y Switch and Drive Lines

4-31. MEMORY REGISTER. The Memory Register (MR) consists of register flip-flops. The number of flip-flops used is established by the number of bits in a memory word; a maximum of 24 are required for a 24-bit word, a minimum of 4 for a 4-bit word. The Memory Register receives and temporarily holds information that is being stored in, or read out of the Magnetics Module. Information to be stored in the Magnetics Module enters the MR as d-c levels in conjunction with an externally generated strobe, or as pulses without a strobe. Information read out of the Magnetics Module always enters the MR as pulses. The read amplifiers apply only set pulses to the Memory Register. These flip-flops are therefore placed in the reset state by a clear MR pulse before strobe RA time. During buffer unload and memory read and restore, information is cleared from the MR by an unload sync delayed one usec.

4-32. Each Memory Register flip-flop gates a single inhibit driver to control inhibit current flow through one specific digit plane during buffer load, memory read and restore, and memory clear and write modes. When the system is operating in the buffer unload or memory read and restore modes each MR flip-flop is controlled by a read amplifier output.

4-33. INHIBIT AND CLEAR DRIVERS. Each inhibit driver controls the flow of inhibit current through one specific plane of the Magnetics Module matrix stack. The inhibit driver output consists of an inhibit winding that links every storage core in a given plane. Each flip-flop in the MR furnishes a gating level to a single inhibit driver to control information transfer into the Magnetics Module. The LC flip-flop also gates the inhibit circuits and thereby times the flow of inhibit current to the desired part of the operating cycle.

4-34. Inhibit driver conduction produces a half-select current that opposes and cancels the effect of the half-select Y drive line set current when a ZERO is to be stored during buffer load, memory clear and write, or memory read and restore. An MR flip-flop disables its associated inhibit driver when a ONE is to be stored.

4-35. One clear driver is associated with each inhibit driver and inhibit winding. The clear driver is gated only by the clear pulse and passes a full-select current into its inhibit winding to reset all of the cores within a specific plane to ZERO during a master clear operation.

4-36. READ AMPLIFIERS. Each read amplifier is associated with one specific plane of the Magnetics Module matrix stack. One of the read amplifier inputs consists of a read winding that links every

storage core within its plane. Another input, strobe RA, consists of a gating pulse that enables every read amplifier to set a specific Memory Register flip-flop with an amplified core turn-over signal from its read winding. A single wire carries the read amplifier output pulse to the set input of its MR flip-flop.

4-37. A read winding and read amplifier operate in conjunction with each digit plane and are common to all of the cores within that plane. However, only the single core selected by coincident X and Y drive line currents can turn over to produce a signal voltage on the read winding. Each read amplifier will produce a +9 volt one usec output pulse during buffer unload or memory read and restore in coincidence with RA strobe when an address-selected core within its plane turns from ONE to ZERO. This is termed destructive readout, since all selected cores storing ONEs change their state from ONE to ZERO while being read.

4-38. COUNT NETWORK. The count network (CN) consists of optional count logic cards that function with the Address Register, or with the Address Register and Transpose Register (TR). When operating with the AR and count logic cards only, the count network can add or subtract one digit from the AR when driven by an externally generated count pulse and Forward or Reverse control level. When operating with the AR, TR and count logic cards, the count network can add or subtract one digit from the AR; it cannot add or subtract from the TR number entering the AR during a transposition of the AR and TR digits. If a master clear pulse is used to start a BQ interlace, the AR is set to all ONEs, and the TR to ZERO. The CN permits the RB memory system to load or unload consecutive memory addresses without requiring an externally generated address for each command.

4-39. TRANSPOSE REGISTER. The Transpose Register (TR) is an optional register consisting of transpose register flip-flops. The number of flip-flops in a TR is always equal to the number of register flip-flops in the Address Register. Their number varies from seven flip-flops for a 128 word system, to ten for 1024 words. The Transpose Register functions with the Address Register and the count logic cards to provide interlace capability for the RB system.

4-40. Address information in the AR and TR is transposed upon command. The contents of the AR may be increased by one digit, decreased by one digit, or remain unchanged while being transferred into the TR. The contents of the Transpose Register are transferred into the Address Register unchanged. This function forms the basis of every interlace operation.

4-41. Address information is normally transposed between registers when an externally generated transpose pulse is applied to the RB system. However, inclusion of an optional BQ logic card provides for an automatic transposition under prescribed conditions.

4-42. LOAD CONTROL (LC) AND LOAD/UNLOAD (L/U) FLIP-FLOPS. These flip-flops consist of standard register circuits that provide gate levels to control system functions. Load sync, unload sync, and drive timing pulses are used to set or reset the LC and L/U circuits.

4-43. Those circuits gated by the state of LC or L/U include inhibit timing, BQ operation, Memory Register clear, X and Y switches, drive timing, and read strobe RA. The function of each flip-flop as related to a specific circuit or operating mode is explained in the applicable circuit or operating mode description. The LC outputs are termed LC and $\overline{LC}$; L/U outputs are termed L and $\overline{L}$.

4-44. FUNCTIONAL OPERATION.

4-45. TIMING AND CONTROL. Figure 4-5 is a simplified timing diagram which shows the timing relationship of inputs and the outputs during the various modes of operation. As indicated in the diagram, 5 usec is required for one buffer cycle, and 8 usec for a memory cycle.

4-46. Although a buffer cycle requires 5 usec, address out information is available at the end of 1.5 usec. In buffer load, the loaded information is available in 1.5 usec, and in buffer unload, the unloaded information is available at the end of 4 usec. In the memory read and restore operation, the unloaded information is also available at the end of 4 usec.

4-47. MODES OF OPERATION. The equipment has two primary modes of operation, as a buffer or as a memory. With the system functioning as a buffer, it is capable of loading or unloading the Magnetics Module. Performing as a memory, the system can either clear and write, or read and restore.

4-48. LOAD OPERATION. In the load operation, it is customary to apply the address to the Address Register, and the information to the Memory Register, slightly prior to zero time. Zero time occurs when the unload or load sync crosses the input reference voltage. At zero time, strobe AR is applied to the Address Register, strobe MR is applied to the Memory Register, and the load sync is directed to the Timing and Control circuits. The MR and AR strobes are not required when pulse inputs are applied to the registers.

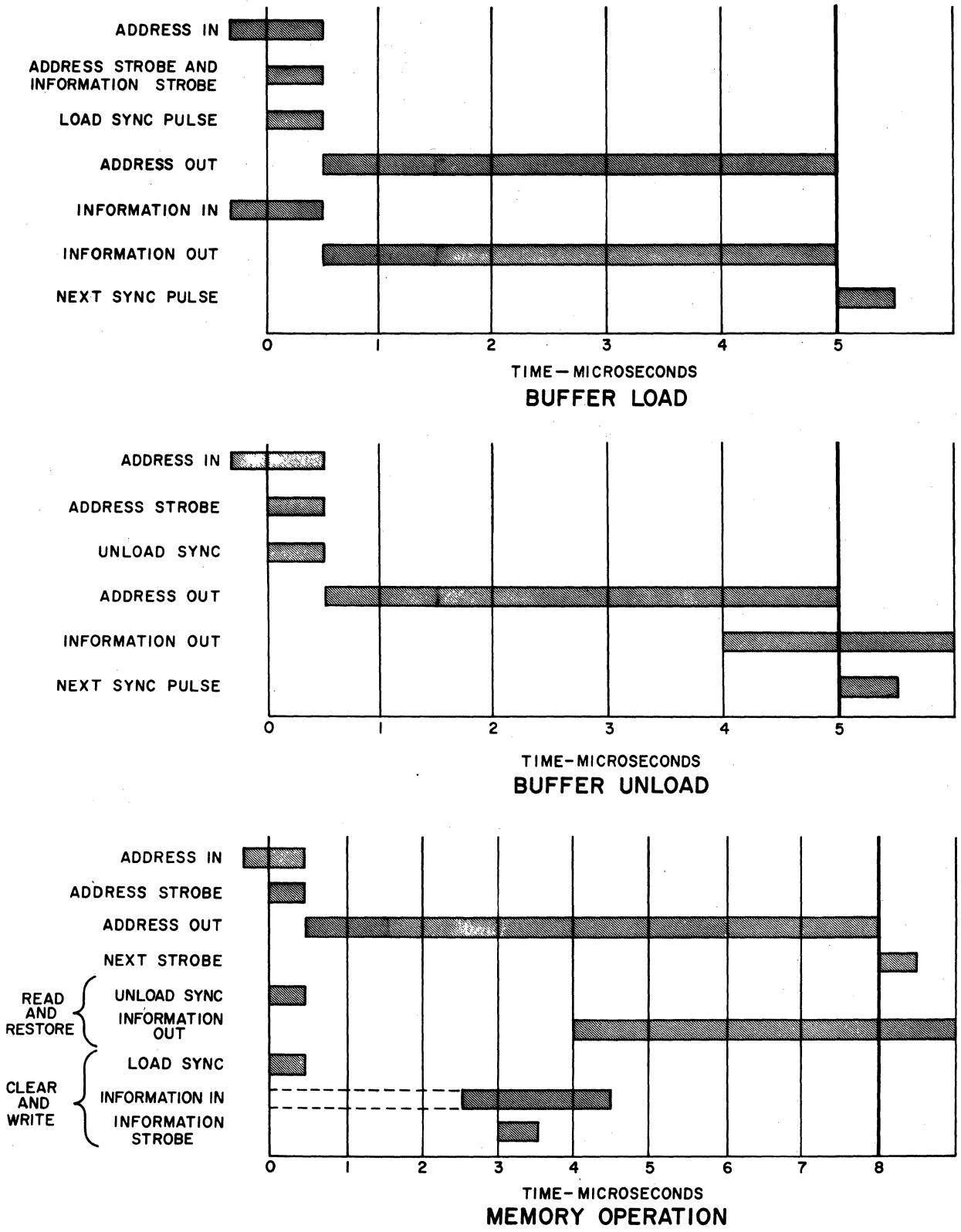


Figure 4-5. Simplified Timing Diagram

4-49. Address levels from the AR operate the X and Y switches to select one core in each digit plane. Because the drive timing pulse is developed one usec after zero time, the load sync is allotted time to generate an inhibit timing signal that turns on those inhibit drivers which are enabled by the MR flip-flops. Each inhibit driver prevents the single address selected core in its respective plane from turning to the ONE state (if at ZERO) when the drive timing signal is applied. The selected core in each plane that does not receive inhibit current is switched to the ONE state when the drive pulse permits NCS current to flow through the switches and set drive lines.

4-50. At 1.5 usec after zero time, address out and information out signals are available.

4-51. If the load operation has not been preceded by an unload operation at that address, the new information may be loaded into the memory together with information already present. This would change those cores in the ZERO state to ONE, but would not change any core already in the ONE state. This procedure is sometimes considered desirable, and two or more load operations to the same address may occur in succession. However, normal procedure is to unload or clear a core prior to loading it.

4-52. UNLOAD OPERATION. In the unload operation, the address is normally applied to the Address Register slightly before zero time, with the strobe AR (if used) and unload sync pulses applied to the system at zero time. The unload sync generates an MR clear and a drive timing pulse one usec after zero time. The MR flip-flops are reset to zero, and then set by their associated read amplifier outputs (if a selected core turns from ONE to ZERO) at strobe RA time.

4-53. A drive timing pulse enables the address selected switches to conduct current through their reset drive lines and select one core in each plane. If at ONE, the selected core turns to ZERO and induces a voltage in the sense windings. Each sense winding voltage, in conjunction with strobe RA develops a one usec, +9 volt read amplifier output that sets its associated MR flip-flop.

4-54. Address information is available 1.5 usec after zero time. Information out is available 4 usec after zero time, and the system is ready for another cycle 5 usec after zero time.

4-55. CLEAR AND WRITE. Since this operation involves clearing the address selected cores in the Magnetics Module before loading them, additional time is involved, and the operation requires 8 usec, as compared with 5 usec for a loading operation.

4-56. The enabled MO (Memory Operation) control level applied to the Timing and Control circuits causes those circuits to develop a sequence of pulses which will result in operation of the system as a memory. With an address input applied to the Address Register slightly prior to zero time, the strobe AR (if used) and load sync pulses are applied to the system at zero time.

4-57. The Timing and Control circuits apply a drive timing pulse to the X and Y current switches, resetting all of the address selected cores to ZERO, thus clearing the applicable portion of the memory. Since no strobe RA pulse is generated, there is no read-out of the core information, as contrasted with a buffer unload operation.

4-58. Upon application of input information to the Memory Register, the remainder of the cycle is identical with buffer load.

4-59. READ AND RESTORE. Since the read-out of a core is destructive, for memory operation the information must be restored after read-out. This involves reloading the cores, hence, read and restore operation requires 8 usec, compared with 5 usec for an unload operation.

4-60. Development of pulse sequences in the Timing and Control circuits for operating the system as a memory is effected through application of positive MO control level to those circuits. With address input applied to the Address Register slightly before zero time, the strobe AR and unload sync pulses are furnished at zero time. A clear MR pulse from the Timing and Control circuits resets all the flip-flops in the Memory Register, preparing them to receive information from the read amplifiers.

4-61. The Timing and Control circuits next apply a drive timing pulse to the X and Y current switches and a strobe pulse to the read amplifiers. Those address selected cores in a ONE state are reset to ZERO and supply core turn-over signals to the read amplifiers. The final operation consists of restoring information in the Memory Register to those cores unloaded by the preceding drive timing pulse. This is accomplished by a normal load operation, in which inhibit timing pulses are applied to the inhibit drivers, and a drive timing pulse is applied to the X and Y current switches.

4-62. Address and MR Register outputs are available at the same time as during buffer operations.

4-63. CLEAR OPERATIONS. All circuits in the system which require clearing may be cleared by a single pulse applied to the

Timing and Control circuits, or each register may be cleared by an externally generated signal.

4-64. When it is desired to clear the system, a master clear pulse is applied to the Timing and Control circuits, which apply clear pulses to the Memory Register, Address Register, Transpose Register, and clear drivers. The clear drivers reset all of the cores in the Magnetics Module to ZERO. This operation places a heavy current demand on the power supply, and limitations must be placed on the frequency of its use.

4-65. A master clear pulse must only be applied after the end of a cycle, and no other pulses may be transmitted to the system for 25 usec. The master clear pulse may not be applied again for 100 usec, nor more frequently than once every 250 usec averaged over any 10 millisecond period. A clear MR or clear AR pulse can be applied at any time conditions indicate their necessity.

4-66. INTERLACE. Interlace operation consists of a load command or a series of load commands alternated with an unload command or a series of unload commands, subject to the following provisions:

(a) The number of consecutive load commands is limited to the capacity of the Magnetics Module.

(b) The total number of words unloaded never exceeds the total number of words loaded during interlace.

(c) Words are unloaded in the same sequence in which they were loaded.

(d) When a load command is applied after an unload command, the system resumes loading at the address immediately following the last address loaded.

(e) When an unload command is applied after a load command, the system resumes unloading at the address immediately following the last address unloaded.

While the number of consecutive load commands is limited by the Magnetics Module capacity, the obvious procedure of reloading addresses which had previously been loaded and unloaded, can extend the interlace operation for an indefinite period.

4-67. To load or unload at a series of consecutive addresses, the RB system must be able to count the AR forward one digit with each command (sync pulse). This function is performed by the count network.

4-68. Interlace operation requires the RB system to load an address or a series of consecutive addresses, and then unload an address, or a series of consecutive addresses beginning at the first address loaded, alternate load and unload commands and maintain address continuity for all load commands and all unload commands. The functions listed in (a) through (d) are performed by the count network and Transpose Register.

(a) Set the TR to address X and the AR to address X.

(b) Load at address X or a consecutive address series beginning at X. Increase by one digit the last address loaded and transfer it into the TR. Simultaneously transfer the TR address into the AR.

(c) Unload at address X or at a series of consecutive addresses beginning at X. Increase by one digit the last address unloaded and transfer it into the TR. Simultaneously transfer the TR address into the AR.

(d) Load at the address transferred into the AR or at a series of consecutive addresses beginning at the address transferred into the AR. The count pulse and Forward level required for each address change while loading or unloading consecutive addresses, and the transpose pulse and Forward level required for each AR to TR transposition are externally generated.

4-69. BQ LOGIC CARD. Inclusion of an optional BQ logic card in the RB memory furnishes a method of interlace operation without the normally added requirement of an externally generated count pulse and transpose pulse for each address count or each address transposition. During interlace, each address transposition occurs with a change in operating mode from load to unload or from unload to load. A different operating mode indicates a change from an unload sync to a load sync, or a change from a load to an unload sync. The BQ logic circuits sense these changes by comparing each load or unload sync pulse with the state of flip-flop L/U (L/U is the operating state flip-flop that is set by each load sync, reset by each unload sync).

4-70. Each sync pulse is checked by the BQ logic card. If the command being checked is not identical to the preceding command, the BQ circuits generate a transpose pulse. If the command being checked is identical to the preceding command, the BQ circuits generate a count pulse. A master clear signal with the BQ level

enabled sets the Address Register to all ONEs, the Transpose Register to ZERO, and resets flip-flop L/U to its ZERO (unload) state.

4-71. BQ interlace operation is usually, but not necessarily, started by a master clear pulse. The clear pulse may be omitted and any alternate starting address placed in the TR; the TR address minus one digit is placed in the AR. Interlace using a BQ card requires only the following externally generated voltages: a master clear pulse, a positive Forward level, an enabled BQ level, and alternate load and unload sync pulses with MO disabled. When operating interlace with a BQ logic card, the RB system performs the following consecutive operations:

(a) Sets the AR to all ONEs and the TR to ZERO with a master clear pulse.

(b) Loads at address ZERO or at a series of consecutive addresses beginning at ZERO.

(c) Increases the last address operated on by one digit and transfers it into the TR. Simultaneously transfers the TR address into the AR.

(d) Unloads at address ZERO or at series of consecutive addresses beginning at ZERO.

(e) Increases the last address operated on by one digit and transfers it into the TR. Simultaneously transfers the TR address into the AR.

(f) Loads at the new address transferred into the AR or at a series of consecutive addresses beginning at the new address.

4-72. Because the master clear pulse that sets the AR to one digit less than the TR has also reset L/U to its ZERO state, the first load command will generate a transpose pulse. The count network then provides gating that enables the transpose pulse to transfer the address plus one digit from the AR to the TR. Address ZERO in the TR enters the AR without change and the first load information enters address ZERO about 1.0 usec after zero time.

4-73. Each subsequent load command, unless interrupted by an unload command, will generate a count pulse to permit consecutive address operation. The first unload command to interrupt the series of load commands will cause the BQ logic circuits to develop a transpose pulse. Table 4-1, Interlace Using a BQ Logic Card,

plots the load and unload sync pulses against the state of flip-flop L/U and indicates whether a count or transpose pulse is generated.

TABLE 4-1. INTERLACE USING A BQ LOGIC CARD

State of L/U Flip-Flop	Load Sync	Unload Sync	Transpose Pulse	Count Pulse
$\underline{L}$	X			X
L	X		X	
$\underline{L}$		X	X	
L		X		X

4-74. DETAILED THEORY.

4-75. The following paragraphs contain the detailed theory of operation of RB General Purpose Memory circuits. The first two drawings in Section VI are the system logic diagrams. They should be consulted while this portion of the manual is being read. The simplified schematics in this section are taken from the complete schematics included in Section VI.

4-76. INPUT - A CARD.

4-77. GENERAL. (See Figure 4-6 and 4-7 and Drawing 11930.) All externally generated timing and control signals, except the memory and address register information, enter the buffer via an input card. The card accepts positive or negative input voltages and delivers positive pulses and levels with specified amplitudes and timing. An input card consists of d-c amplifier Q1 and Q2, d-c amplifier Q3 and Q4, 0.5 usec pulse generator Q7, Q6 and Q5, 0.5 usec pulse generator Q8, Q9, Q10 and Q11, inverter Q13, and current switch Q12.

4-78. Two plug-in adapters serve as input selectors and enable the two d-c amplifiers and two pulse generators to function with either positive or negative going input signals. Input selector 1 is inserted in either of two positions at the Q1, Q2 inputs. Input selector 2 is inserted in either of two positions at the Q7, Q8 inputs. The timing and control signals applied to an input card depend upon its card-cage location. These input signals can be identified on Drawing 12310, Logic Diagram.

4-79. Input signals may start at zero or at either positive or negative levels. The reference voltage applied to the Q1, Q3 or Q7, Q8 transistors is determined by the midpoint of the input voltage swing. Since the reference voltage is established as one-half the input signal swing, the no-signal voltages will always hold Q1 and Q3 at cut-off, Q7 and Q8 conducting.

4-80. D-C AMPLIFIERS. Operation of the two d-c amplifiers is identical so only Q1, Q2 will be discussed. With input selector 1 set for positive going signals, the reference voltage is applied to the emitter of Q1. When the input signal voltage is negative with respect to the reference level, diode CR3 conducts, and the base of transistor Q1 is reverse biased, so that this transistor does not conduct. Transistor Q2 is also cut off, since current through R2 is routed through CR1. Excessive reverse base bias of Q2 is prevented by clamp diode CR4. With Q2 off, its collector load resistance is clamped at zero volts by CR2. The junction of CR2 and the Q2 collector is connected to the circuit output terminal.

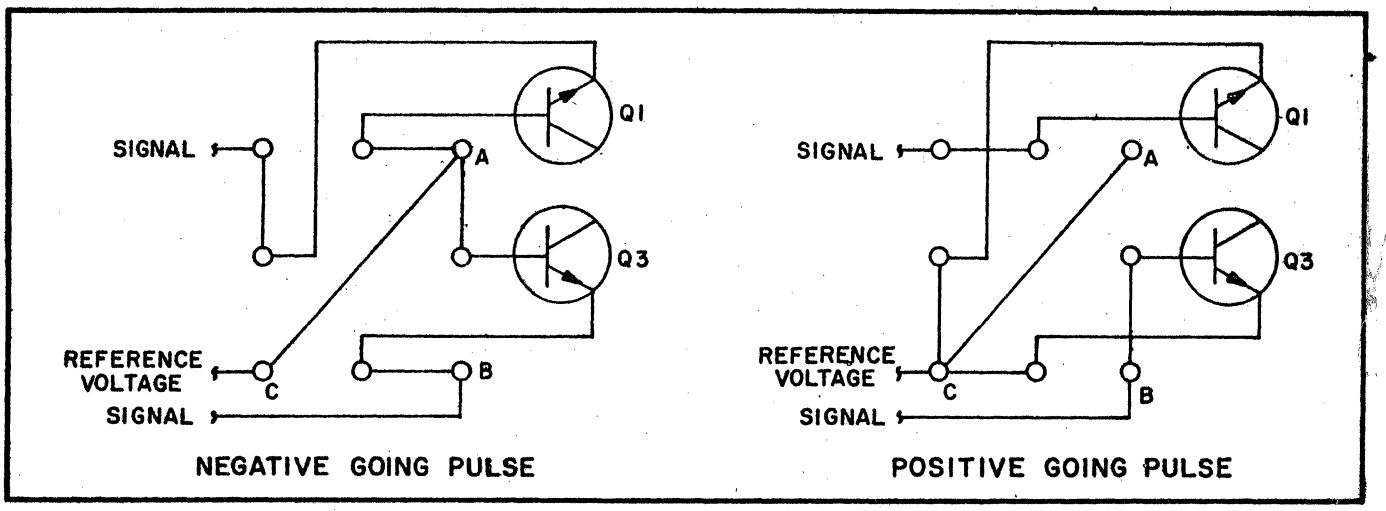


Figure 4-6. Input Selector 1, Input Wiring

4-81. A positive input voltage (with respect to the reference level) reverse biases CR3 and allows current from R1 to drive Q1 into conduction. The collector voltage of Q1 drops to a value which reverse biases diode CR1. This diverts the current from R3 into the base of transistor Q2, turning it on. As a result, the collector voltage of Q2 approaches its emitter level of +6 volts.

4-82. With the input selector connected for negative signals, the reference voltage is applied through CR3 to the base of Q1. The signal is applied directly to the emitter of Q1 which is non-conducting when the signal voltage is positive with respect to the reference

level. A negative input signal voltage causes Q1 to conduct and enables the output of Q2 to rise to +6 volts.

4-83. PULSE GENERATOR Q7, Q6 and Q5. When input selector 2 is set for positive going signals, the reference voltage at the base of Q7 holds this transistor in conduction when the input voltage is negative. With Q7 conducting, diode CR11 is reverse biased, and current from R11 flows through the base of Q6, causing it to conduct. In the collector circuit, a constant current flows through an inductor L1 and a current limiting resistor R12. Transistor Q5 is normally cut off, being reverse biased by R14 and clamped by CR14.

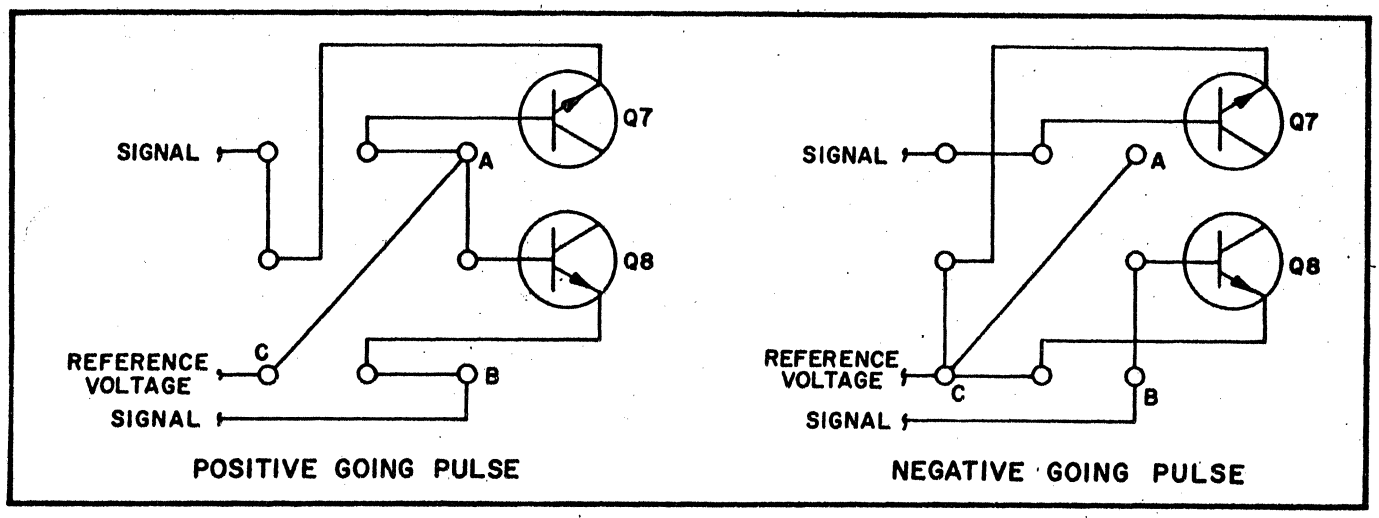


Figure 4-7. Input Selector 2, Input Wiring

4-84. An input signal which rises positive with respect to the reference level cuts off Q7, causing CR11 to conduct and bias Q6 out of conduction. The abrupt current change through L1 results in a negative spike which turns on Q5, generating an output pulse through transformer T1. At the end of this pulse the negative overshoot across T1 is limited by clamp diode CR10.

4-85. PULSE GENERATOR Q8-Q11. With the input selector set for positive-going signals, the reference voltage at the base of Q8 holds this transistor in conduction when the input voltage is negative. With Q8 conducting, the reference voltage on its emitter appears on the collector and is coupled to the base of Q9 through diode CR17. This potential enables Q9 to remain close to cut-off if the potentials on the anodes of diodes CR19 and CR21 are also at

negative or low positive voltages. If Q9 is not conducting heavily, Q10 is biased into conduction by the -6 volt supply. In the Q10 collector circuit a constant current flows through an inductor L2 and a current limiting resistor R22. Transistor Q11 is normally cut off, being reversed biased by resistor R23 and clamped by diode CR23.

4-86. An input signal which rises positive with respect to the reference level cuts off Q8, causing CR17 to couple a positive potential from the +24 volts to the base of Q9. Q9 conduction places a +6 volt potential on the anode of diode CR22 and cuts off Q10. The abrupt current change through L1 results in a negative spike which turns on Q11, generating an output pulse through transformer T2. At the end of this pulse, the negative overshoot across T1 is limited by clamp diode CR20. Q9 may also be driven into conduction by a positive pulse on the anodes of diode CR19 or CR21.

4-87. INVERTER Q13. When driven into conduction by a negative input to its base, Q13 delivers a +6 volt output to terminal C. Current through resistor R33 and diode CR27 clamps a +6 volt cut-off bias on the Q13 base when input signals are not present. With Q13 biased out of conduction, its collector output circuit is clamped to zero volts by current through diode CR26.

4-88. CURRENT SWITCH. The two inputs to current switch Q12 consist of the X-Y current supply which is applied directly to the collector, and a drive timing pulse that is applied to diode CR24. During the interval when an input signal is not present, the -24 volt current through resistor R29 holds the transistor in saturation. The Q12 collector is now kept very close to zero volts by the low emitter-collector impedance.

4-89. A positive drive timing pulse causes CR24 to conduct and place a positive cut-off bias on the Q12 base. The zero volts is removed from the transistor collector for the duration of the input pulse and the X-Y current is directed through the selected drive switches.

4-90. TIMING - A CARD.

4-91. GENERAL. (See Figure 4-8 and Drawing 11926.) This card contains timing circuits that generate timing and control pulses to sequence the several logical operations that constitute a complete buffer cycle. The timing circuits consist of delay blocking oscillator Q1, clear MR gate Q2 and Q3, drive timing

generator Q4 and Q5, strobe generator Q6 and Q8, matrix clear generator Q9 and Q10, LC set and reset (inhibit timing) Q7 and Q11.

4-92. DELAY BLOCKING OSCILLATOR. The function of this circuit is to generate a pulse delayed by one microsecond when triggered by either a Load Sync or Unload Sync pulse, or by a "Set LC" pulse from Q7. Quiescently, transistor Q1 is non-conducting. When a positive trigger pulse is applied to its emitter through either CR12 or CR16 which act as an OR gate for Load and Unload Sync pulses, or through CR29 in the case of a "Set LC" pulse, emitter current is initiated, causing the collector of Q1 to rise in potential. Since the collector is connected to the blocking oscillator transformer, regenerative action occurs through the transformer windings via CR8, and the desired pulse is obtained. The time duration of the pulse is determined by the L/R time constant of T1 and R1. Output is obtained from a third winding of the transformer. This winding is connected so that the one microsecond pulse is of negative polarity. Diode CR6 blocks this, and allows only the positive overshoot at the trailing edge of the pulse to be used.

4-93. CLEAR MR GATE. This circuit (Q2 and Q3) operates the clear MR generator when a +6 volt pulse is received from the Q1 blocking oscillator and a negative level from flip-flops LC and L/U is applied by CR31 and CR34. When the voltage applied across R14 is positive, Q2 conducts, clamping the Q3 emitter to zero. Q3 is then prevented from responding to the delay pulse from Q1. If the base of Q2 goes negative (LC and L/U are low), the Q3 emitter is still zero, but only because Q3 is conducting in the absence of a blocking oscillator pulse. When this pulse is received, Q3 conduction is reduced, the emitter rises with the increased collector-emitter impedance, and the clear MR signal is generated. When the LC or L/U outputs are high, Q2 again conducts to clamp the Q3 emitter to zero and a clear MR pulse cannot be developed. The load level from L/U is always low during buffer unload and memory read and restore. When the system is in these modes, LC establishes the voltage at the base of Q2. The clear MR signal is sent to the clear MR generator, mounted on input card A3.

4-94. DRIVE TIMING GENERATOR. This circuit provides a drive timing pulse which defines the duration of the drive currents to the selected address of the magnetic storage unit. A blocking oscillator Q4 similar to that described above is triggered by the trailing edge overshoot of the one microsecond delay blocking oscillator, and provides a pulse of 2.5 microseconds duration. During this period, Q5 is driven into conduction to furnish the +3.5 volt timing output.

4-95. STROBE GENERATOR. The strobe generator develops a positive 9 volt 0.5 microsecond output pulse that enables the read amplifiers

to produce a binary ONE signal when driven by a core turn-over voltage. The leading edge of each X-Y timing pulse triggers blocking oscillator Q6 which produces a 1.5 microsecond pulse, whose duration can be adjusted by R33. The trailing edge of this pulse from transformer T3 has an overshoot which is used to turn on transistor Q8, providing the strobe pulse.

4-96. Quiescently, Q8 is non-conducting. During the operation of Q6, terminal 6 of transformer T3 is driven positive, but this signal is blocked by diode CR17. At the trailing edge of the pulse, the voltage from the transformer overshoots, causing CR17 to conduct the negative excursion to the base of Q8. The other end of the transformer's output winding, terminal 3, does not go positive until approximately 1.6 ma of base current is delivered to Q8; excessive base drive to Q8 is prevented by unclamping of CR21 at that point.

4-97. If either the LC or L/U input to diodes CR31 and 34 is positive, Q8 is cut off. A read amplifier output is only desired during unload or read operations.

4-98. MAGNETICS MODULE CLEAR GENERATOR. This clear generator gives a +6 volt 15 usec pulse that resets all matrix module cores to their ZERO state. A positive clear sync input signal cuts off Q9 and swings the base of Q10 negative. The Q10 collector rises from zero to +6 volts to provide a 12 microsecond clear timing voltage.

4-99. LC SET AND RESET. Set and reset LC pulses control the state of the LC flip-flop to establish inhibit circuit timing. The state of LC also determines whether the drive switches will conduct into the load or unload drive lines. The LC flip-flop is set for each load or write operation and is reset at the end of the drive timing pulse. There are two paths by which LC may be set.

4-100. When the Memory Operation control level is negative (buffer mode) gated inverter Q11 produces a positive set LC pulse if driven by a load sync pulse to its emitter. When the MO (Memory Operation) control level is positive (memory mode) LC is set by inverter Q7 which furnishes a positive output pulse when driven into conduction at the trailing edge of a drive timing pulse. When the MO and $\overline{LC}$ levels are positive, the output pulse from Q7 passes through CR26 to set LC. Simultaneously, it is also coupled through CR29 to initiate another timing cycle by triggering Q1. Thus, a Memory Clear and Write or Memory Read and Restore full cycle is carried through with LC being set for the second half of the operation (Write or Restore). Since $\overline{LC}$ is negative during the restore (Write)

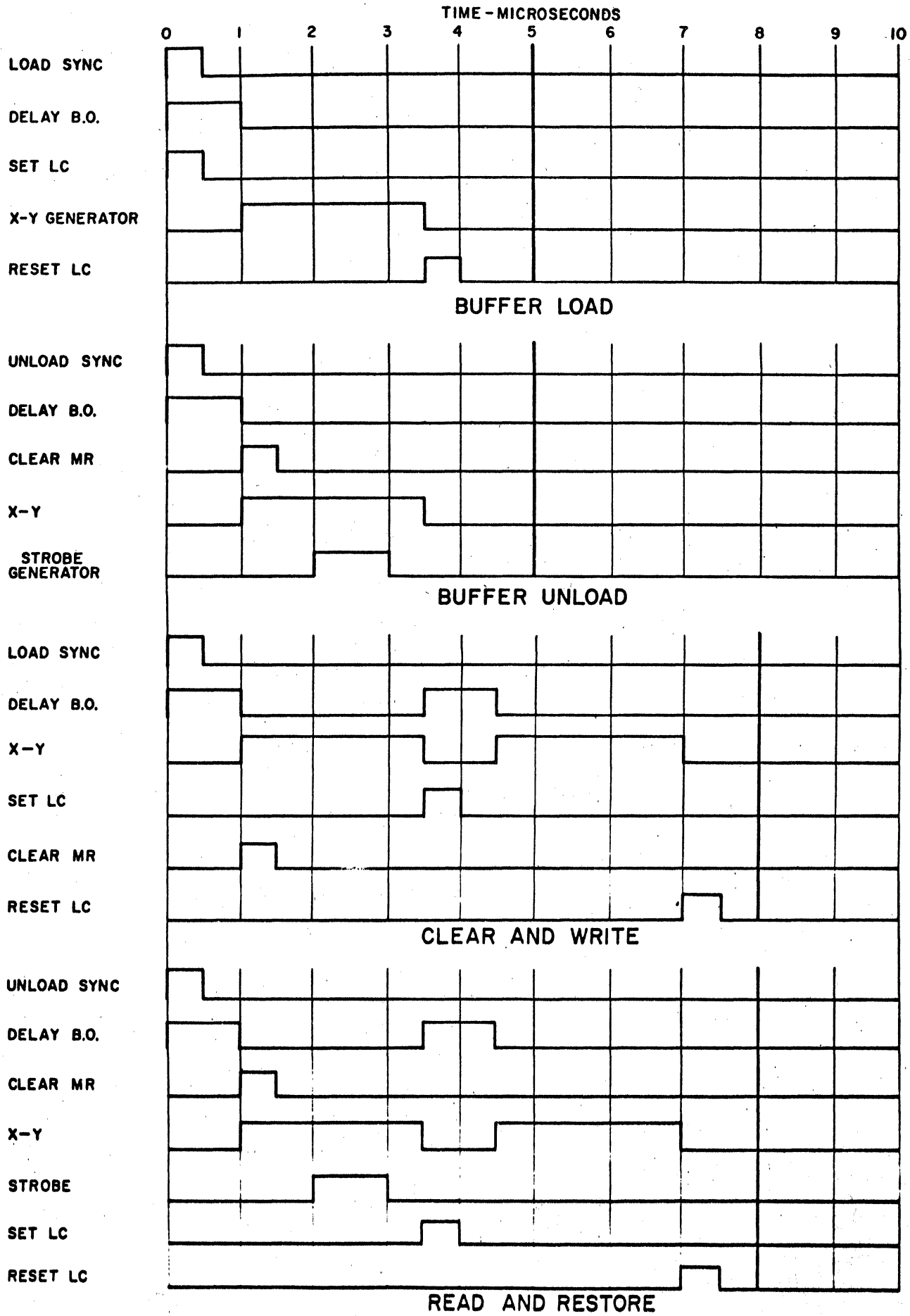


Figure 4-8. Timing Waveforms

portion of a memory cycle, further cycle initiate pulses via CR29 are not obtained. When quiescent, Q7 is held cut off by the small positive base-emitter voltage developed across diode CR30. The collector is clamped to zero volts by diode CR33.

4-101. Application of the positive going X-Y pulse charges inductor L2 through resistor R31 but does not alter the cut-off state of Q7. When the input pulse falls to zero, the L2 field collapses and provides a negative overshoot that is coupled through capacitor C5 to turn on Q7.

4-102. The output pulse of Q7 is also used to reset the LC flip-flop at the end of each cycle during which it had been set. This is accomplished by a pulse gate consisting of C4,R24 and CR22.

4-103. REGISTER - A CARD.

4-104. GENERAL. (See Figure 4-9 and Drawing 11920.) The register flip-flop is a bi-stable circuit used as a temporary storage device in the address, memory and timing registers. The flip-flop circuit consists of an Eccles-Jordan circuit, Q3, Q4; four output inverters, Q1, Q2, Q5, Q6; and two input circuits, Q7 and Q8, with their associated gates. There are two register flip-flops on each printed circuit card.

4-105. The two stable states of the flip-flop are designated ZERO and ONE. Input pulses set and reset the circuit from ZERO to ONE and from ONE to ZERO. In the ONE state, Q3 is conducting at saturation and Q4 is cut off. Q3 conduction places a positive voltage at the base of inverters Q11 and Q5 and enables the inverter collector circuits to swing negative. The Q5 output is -6 volts. With Q4 cut off the Q2 and Q6 inverter bases are negative and drive their respective emitter-collector circuits into conduction. The Q6 output is +3.5 volts. The output voltages are reversed when the flip-flop is switched to the ZERO state.

NOTE

All terminals referred to, unless identified otherwise, are those of the Circuit 100 or 200 schematic. They are not the printed card terminals identified by operating voltages or signal designators.

4-106. The negative output level from the Q1 and Q2 inverters is established by the output clamp circuit at terminal 2. Any pair of the following five pair of voltages may be derived from the Q1, Q2 inverters. Refer to Table 1-3 for the input voltage swing associated with each of these outputs.

(a) 0 and -6 volts

(b) +6 and 0 volts

(c) 0 and -12 volts

(d) +12 and 0 volts

(e) +6 and -6 volts

4-107. A positive input pulse of more than +6 volts at terminals 17 or 18 will reset the flip-flop to ZERO by driving the Q3 base positive. As Q3 cuts off, its collector becomes more negative and, through a voltage divider, moves the Q4 base in a negative direction. With Q3 at cut-off, the Q4 base receives -12 volt current through resistors R4 and R9, and its collector saturates. Conduction through the Q4 emitter-collector circuit places the R5-R10 junction close to +6 volts and holds Q3 reverse biased in the ZERO state. The switching time depends on circuit loading and can vary from 0.05 to 0.3 microseconds under normal operation.

4-108. An input selector is inserted in one of four possible positions to permit RB memory operation with any of the seven inputs described in paragraph 2-11. The four selector positions are identified as A, B, C or D. Table 2-1 indicates which position is used with each input.

4-109. All register input lines that are not used (not applicable to a specific input) are connected to the voltage that represents a ZERO at the external equipment. A reference voltage that is one-half the amplitude of the input signal excursion is applied to input transistors Q7 and Q8. This voltage is the same reference potential that is applied to the input card and indicates that all control, synchronization, address and information signal swings should be of the same amplitude. These voltages are not required to possess similar polarities.

4-110. SELECTOR POSITION A. (See Figure 4-9.) This selector position is used with single or double-ended positive going pulses.

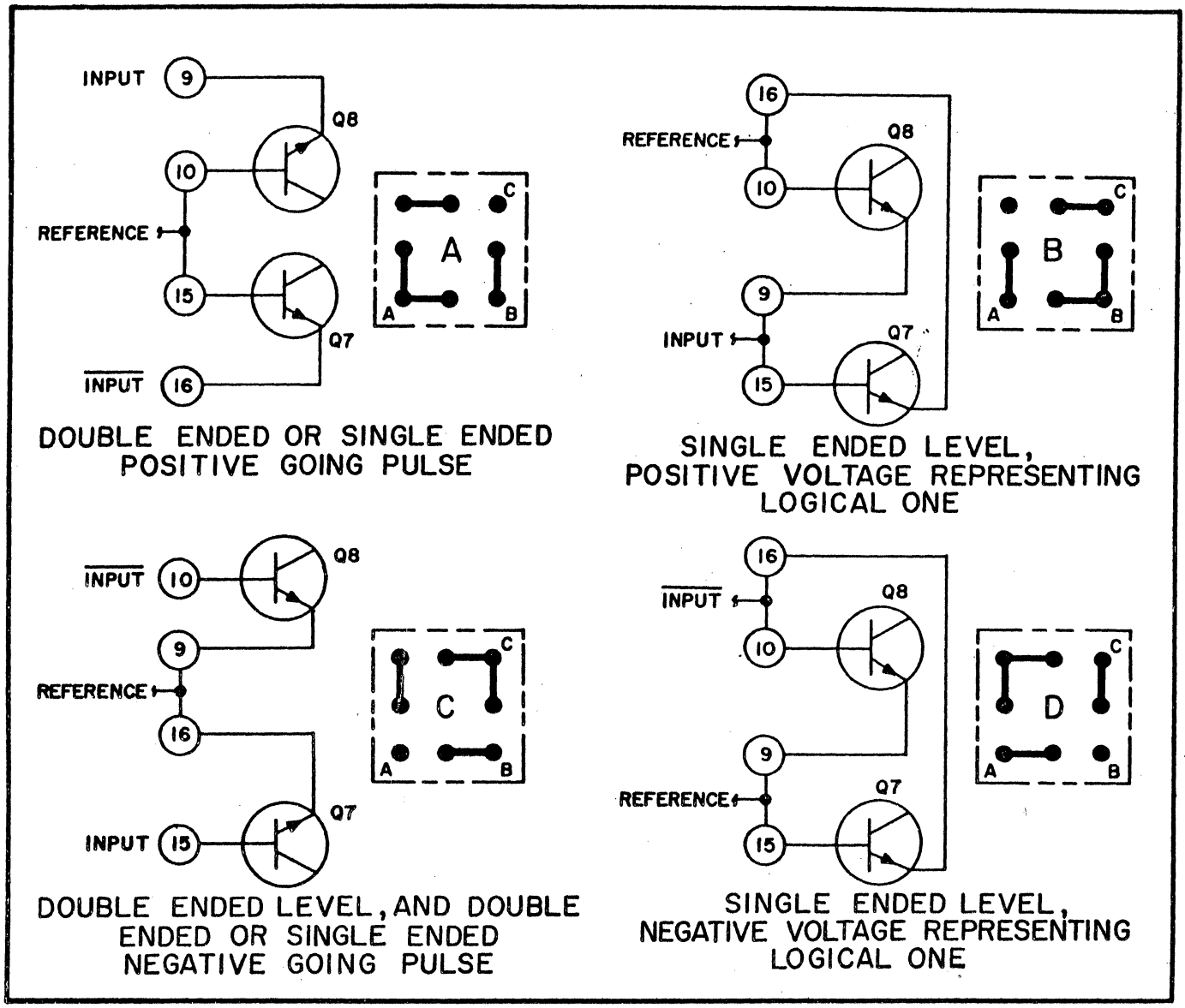


Figure 4-9. Input Selector Wiring

The reference voltage is connected to the Q7 and Q8 bases. These transistors are controlled by the signals applied to their respective emitter circuits. A circuit modification for positive going pulse operation places a +7.5 volt potential at terminal 12 by disconnecting the strobe line and connecting 2 series diodes between terminals 12 and 13. Because a single-ended positive input pulse can only force the flip-flop into its set (ONE) state, this operation requires a clear pulse to reset all register flip-flops before the start of each cycle.

4-111. Q7 is held permanently conducting by the logical ZERO voltage connected to its emitter. Input pulses are applied to the Q8 emitter.

When its emitter moves positive, Q8 cuts off and permits CR15 and CR12 to couple +7 volts to the Q4 base. The flip-flop is forced to its ONE state and generates a high (positive with respect to its complementary output) output at terminal 4. This output is connected to a non-negated terminal at an input-output connector (Figure 2-3).

4-112. Positive going double-ended pulses set or reset the register immediately upon application and do not require a strobe or clear signal. A pulse on the Q8 input switches the circuit to ONE, a pulse on the Q7 input switches the circuit to ZERO.

4-113. SELECTOR POSITION B. (See Figure 4-9.) This selector position permits the register to operate with a single-ended input whose most positive level represents a logical ONE. The reference voltage is placed on the base of Q8 and the emitter of Q7. The input level is applied to the emitter of Q8 and the base of Q7. A positive level at Q8 cuts off this transistor and enables the +9 volt strobe input at terminal 12 to set the flip-flop to its ONE state. Paragraph 4-115 describes the strobe input gating. The terminal 4 output to a non-negated terminal at the input-output connector is high when the circuit is at ONE.

4-114. SELECTOR POSITION C. (See Figure 4-9.) This selector position allows the RB memory to be used with double-ended levels, double-ended negative going pulses, and single-ended negative going pulses. The reference voltage is connected to the Q7 and Q8 emitters. These transistors are controlled by the signals applied to their respective base circuits.

4-115. A double-ended level that moves Q8 negative, cuts off this transistor. The +3.5 volt quiescent level from terminal 12 places the anode of diode CR12 at approximately +3 volts. When the strobe rises to +9 volts, diodes CR15 and CR12 couple a reverse bias to the Q4 base. Q7 is held conducting by the complementary positive input level, and conducts through resistors R13 and R16 to hold the anodes of CR11 and CR14 at a low positive potential. The strobe is therefore blocked from the Q3 base. The strobe input to the flip-flop is always enabled by the non-conducting input transistor.

4-116. A double-ended input should force the flip-flop into its ONE state and provide a high output at terminal 4 when a logical ONE is presented at the memory input. This is accomplished by the inputs described in paragraph 4-115. Double-ended operation does not require a clear pulse to reset the register flip-flop at the start of each cycle.

4-117. Double-ended negative going pulses set or reset the flip-flop immediately upon application and do not require a strobe or

clear signal. The modification described in paragraph 4-110 places a +7.5 volt level at terminal 12. A pulse at either Q7 or Q8 base cuts off the transistor, and permits the terminal 12 voltages to switch the register.

4-118. Single ended negative going pulses set the flip-flop immediately upon application. This operation requires the modification described in paragraph 4-117. The single pulse line is connected to the Q8 base only. A negative pulse cuts off Q8 and permits the terminal 12 voltage to switch the flip-flop to its ONE state. A clear pulse is required to reset the circuit to its ZERO state.

4-119. SELECTOR POSITION D. (See Figure 4-9.) This selector position permits the flip-flop to be set or reset with a single-ended input whose most negative level represents a logical ONE. The reference voltage is applied to the base of Q7 and the emitter of Q8. The input level is applied to the emitter of Q7 and the base of Q8. A negative level at Q8 cuts off this transistor and enables the +9 volt strobe input at terminal 12 to set the flip-flop to its ONE state. Paragraph 4-115 describes the strobe input gating. The terminal 4 output to a non-negated terminal at the input-output connector is high when a logical ONE is loaded.

4-120. TRANSPOSE REGISTER - A CARD.

4-121. GENERAL. (See Figure 4-10 and Drawing 11924.) This card contains two Transpose Register (TR) flip-flops. Each flip-flop is a bi-stable circuit used in conjunction with a transpose pulse to control the state of a corresponding Address Register (AR) flip-flop during the transpose operation. Transpose is initiated by a transpose pulse that exchanges the contents of the Address and Transpose Registers. During transposition the Address Register digits entering the Transpose Register may be counted forward or back one digit, or may be transposed without a count. The Transpose Register digits entering the Address Register are not altered.

4-122. The number of TR flip-flops used varies with the buffer configuration but is always equal to the number of AR flip-flops. Each flip-flop consists of an Eccles-Jordan circuit, Q1, Q2, and an input circuit, Q3, and Q4. The two stable states of the Eccles-Jordan circuit are designated ZERO and ONE. In the ONE state, Q2 is conducting at saturation and Q1 is cut off to provide approximately +6 volts on the anode of diode CR4 and a negative bias on the anode of diode CR1. The outputs are reversed when the circuit is in the ZERO state with Q1 conducting and Q2 cut off.

4-123. INPUT. Input terminal 11 furnishes an AR level that indicates the state of an AR flip-flop; input terminal 10 furnishes a carry level from the count logic card. These inputs determine whether the flip-flop generates outputs that will enable the transpose pulse to set or reset the corresponding AR circuit. Diodes CR6, CR7, resistors R9, R10 and transistor Q3 comprise an EXCLUSIVE OR gate. Only one of the inputs at terminal 10 and 11 may be of positive polarity in order for the gate to produce a positive output at the Q3 collector. Voltages of +3.5 and -6 volts or -6 and +3.5 volts at the respective AR and count logic terminals enable the transpose pulse to set the TR flip-flop to ONE. Two +3.5 or two -6 volt inputs cause the flip-flop to be reset to ZERO.

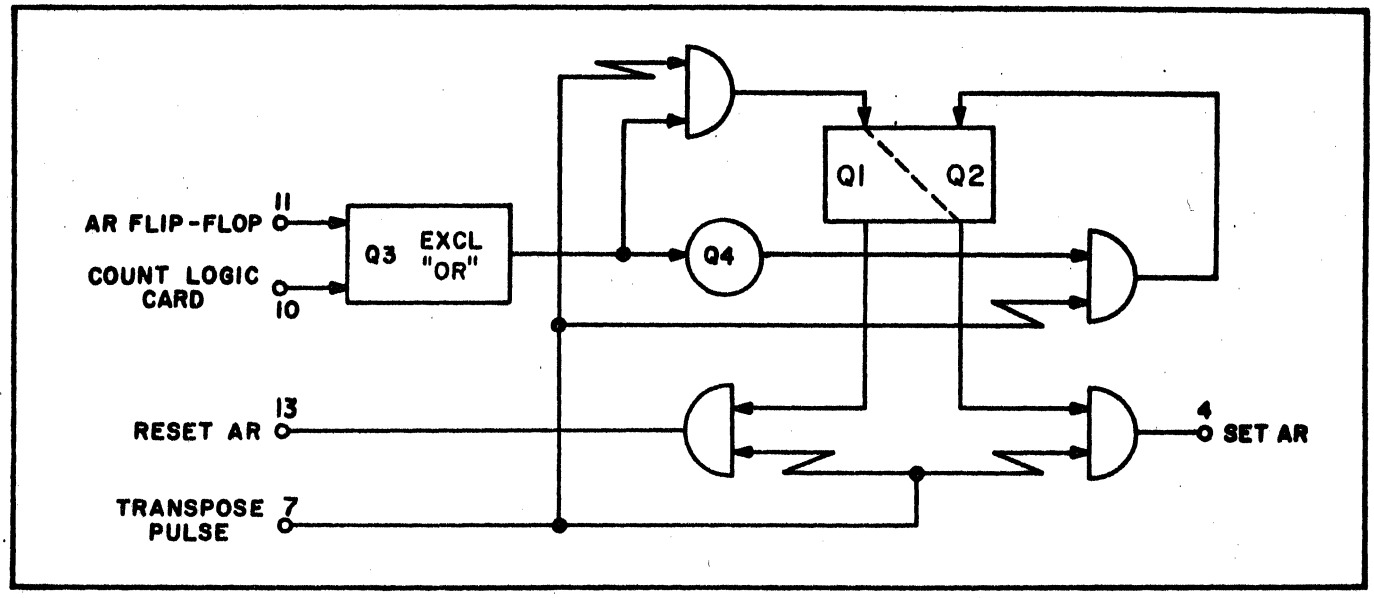


Figure 4-10. Logic Block, TR-A Flip-Flop

4-124. A positive input on the anode of either CR7 or CR6 is coupled to the Q3 emitter. A simultaneous negative input at either R9 or R10 moves the base of Q3 negative and drives Q3 into saturation. The positive Q3 output appears on the anode of diode CR8 and enables the positive transpose pulse from terminal 7 to reverse bias the Q1 base and set the circuit to its ONE state. Inverter Q4 is cut off by the positive Q3 voltage and permits the -12 volts appearing at its collector to place a negative bias on the anode of diode CR9. The transpose pulse is therefore blocked from the Q2 base.

4-125. With two +3.5 or -6 volt inputs the Q3 base is positive with respect to its emitter and the Q3 collector does not conduct, causing a negative potential on CR8 anode. Q4 is biased into

conduction and its positive collector voltage biases CR9 close to conduction. A +6 volt transpose pulse now swings the Q2 base positive and is blocked from Q1 by CR8. In this manner, the state of the address register flip-flop and the count logic card output establish whether a transpose pulse sets or resets the TR circuit. A positive clear pulse is applied at terminal 14 to cut off Q2 and switch the circuit to ZERO during a clear operation.

4-126. OUTPUT. With the circuit at ONE, CR4 is biased close to its conduction level to permit the transpose pulse through C4 to go out on terminal 4 and set the AR flip-flop to ONE. With the circuit at ZERO, CR1 is biased close to its conduction level to permit the transpose pulse through C1 to go out on terminal 13 and reset the AR flip-flop to ZERO.

4-127. The TR flip-flop gates the TR pulse to set or reset the associated AR circuit at the same instant that the inputs from terminal 10 and 11 gate the transpose pulse to set or reset the TR flip-flop. However, the AR circuit is gated by the previous state of the TR flip-flop, not the new state which may be imposed by the count logic carry and AR inputs.

4-128. SWITCH - A CARD.

4-129. GENERAL. (See Figures 4-4 and 4-11 and Drawing 11918.) There are two identical printed circuit cards, one containing 16 X and the other 16 Y switches. Each of the switches includes a 3-term gate whose output enables a transistor to close a specific X or Y drive line. One card is used to select X lines, while the other selects Y lines. The switches are selected in pairs to simultaneously ground one end of a matrix winding and connect the opposite end to the negative current supply.

4-130. Two of 16 switches are selected to energize an X row and two of 16 switches are selected to energize a Y column of matrix drive lines. X and Y circuit operation is identical so only the X will be described. The 16 X switches are segregated into two banks of eight; transistors Q9 through Q16 comprise bank A, transistors Q1 through Q8 comprise bank B. Each memory operation selects one A and one B switch to energize either a set or reset X line. The gate inputs to the B switch consist of two Address Register lines that establish the memory module address and a single load control (LC) level that determines whether the selected switches will close a set or a reset circuit. The gate inputs to the A switch consist of three Address Register lines. (Refer to paragraph 5-51).

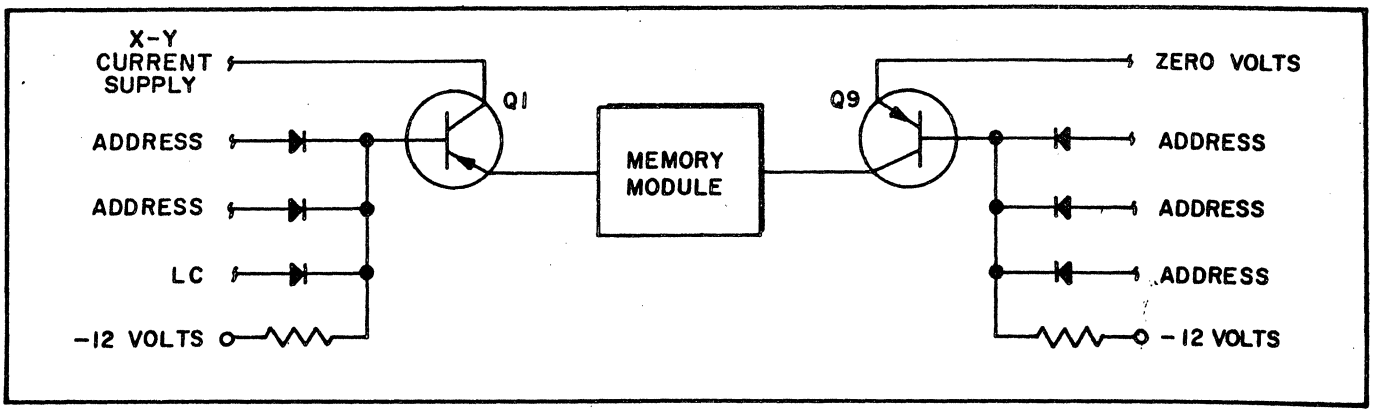


Figure 4-11. SWITCH-A Simplified Schematic

4-131. INPUT. A positive level on any leg of an input gate will reverse bias the transistor base and hold the emitter-collector circuit open. Three negative levels permit the transistor to conduct through the output circuit in series with its emitter if in the A bank, or collector if in the B bank. Address line coding simultaneously selects one A and one B switch to conduct.

4-132. In the B bank switches two of the 3-term inputs to every gate represent address information. The third term is a control level that enables the switches to deliver either set or reset currents in conformance with the input command. This is accomplished by permitting half of the 64 X windings to conduct only set current and the remainder only reset. The 64 lines are effectively reduced to 32 since two lines are required for each core. The specific pair of switches selected for each address depends on whether a set (write) or reset (read) current is desired.

4-133. OUTPUT. (See Figure 4-4.) The output circuit of each A and B switch consists of 8 matrix drive lines that are connected to its emitter or collector output line within the memory module. Each of the 8 lines from each A switch is connected to a separate B switch; each of the 8 lines from each B switch is connected to a separate A switch. A total of 64 lines interconnect the two banks of switches.

4-134. A back-biased diode is in series with every B switch output to steer the drive currents through the selected switches only. Since every A switch is connected to every B switch and every B switch is connected to every A switch, a selected pair of switches contain more than one current path between their respective outputs. For example: the direct path for switch Q1 to switch Q9 is

the desired mode; an alternate route from Q1 to Q10, from Q10 to Q2, and from Q2 to Q9 would also be available in the absence of the diodes. One desired and seven alternate paths exist for every pair of switches. The reverse bias on the diode in series with the direct path is removed when the A switch closes to place zero volts on the diode anode. The diodes in series with the alternate paths retain -9 volts on their anodes during energization of a selected line and block conduction through their circuits. These diodes and their associated resistors are mounted on the top and bottom end plates of the Magnetics Module. The schematics (11932 and 11934) and assembly illustrations (11933 and 11935) that show these components are located in Section VI.

4-135. X-Y CURRENT SUPPLIES. (See Drawing 12310.) Currents for the X and Y drive lines are respectively furnished by the X and the Y negative current supplies. The X and Y current sources are identical in operation, so only the X will be described. The X negative current supply consists of a 16.6 volt (at 25 degrees Centigrade) source in the RB power supply. A current limiting resistor that precisely establishes the drive line current amplitude is placed in series with the supply output voltage.

4-136. During the interval when the matrix windings are not energized, a transistor current switch closes to place a ground at junction of the drive line switches and the current limiting resistor. The negative current is thus diverted from the address selected switches until a drive timing pulse opens the current switch. As the timing pulse falls to zero, the current switch re-closes and again diverts the negative current supply output to ground. In this manner, conduction through the switches selected by address and control (LC) gating is accurately timed to the required portion of the operating cycle. The current switch also contributes to effective regulation by maintaining a constant load on the negative current supply.

4-137. Since the voltage drop across the magnetics module is reasonably constant, a current regulator is not required. The drive line current amplitude is established by use of a precision resistance in series with a controlled voltage source. Temperature compensation is obtained by a thermally sensitive resistance element which controls the voltage level to which the current-determining resistor is connected.

4-138. INHIBIT - A CARD.

4-139. GENERAL. (See Drawing 11916.) Each matrix in the Magnetics Module has an inhibit winding which links all cores in that matrix.

A separate inhibit driver is used for each matrix. When energized, the inhibit driver current opposes the X-Y drive currents to prevent selected cores from turning over when a ZERO is written. The inhibit driver is only used during write (load) operations.

4-140. The inhibit card also includes a clear driver with each inhibit driver circuit to provide a master clear for every core in the memory. While the inhibit current is only half-select amplitude, the clear current is of full-select amplitude and is applied to the inhibit winding to reset all cores in each matrix.

4-141. One printed circuit card contains six inhibit and clear circuits. The number of inhibit cards used depends on the word length of the unit (number of bits).

4-142. CLEAR. A clear action is initiated by operation of the clear timing generator (Q9 and Q10 of the timing and control logic). This signal is applied to circuits 300 and 400 of the inhibit cards. Quiescently, this signal line places zero volts at terminal 5 to keep the output of these circuits above +3 volts. This is applied to Q2 (the clear drivers) of the 500 through 1000 circuits, maintaining them in the non-conducting condition.

4-143. When a pulse is emitted by the clear timing generator, all 300 and 400 circuits are turned off, and Q2 of all 500 through 1000 circuits conducts to provide the clear current at terminal 3 to the magnetics inhibit winding. Each printed circuit card contains one 300 and one 400 circuit to obtain sufficient control current for the six clear drivers.

4-144. INHIBIT. The inhibit current is turned on by transistor Q1 of the 500 through 1000 circuits. A two-term gate constitutes the input to each inhibit driver. One of these terms is the output of the associated MR (memory register) flip-flop, and thus determines whether inhibit action is to occur on a given operation. The other term is a timing level derived from the LC flip-flop and amplified in the 100 and 200 circuits before application to the inhibit input.

4-145. Until an inhibit timing pulse occurs, the input to the 100 and 200 circuits is at zero potential; Q1 of these circuits conducts and its collector voltage is above +3 volts. Thus, the input gate at Q1 of the 500 through 1000 circuit is held positive and the transistor is cut off. When an inhibit timing pulse turns off Q1 of the 100 and 200 circuits, those inhibit driver circuits whose other gate input term from the memory register is negative, conduct at terminal 3 to energize the inhibit winding. Inhibit driver Q1 and clear driver Q2 circuits differ only in the size of their load

resistors, which limit the Q1 output to half-select current, but provide full-select current from Q2.

4-146. READ AMPLIFIER - N CARD.

4-147. GENERAL. (See Drawing 12173.) This card contains two read amplifiers. Each amplifier produces a positive binary ONE signal on receipt of a core turn-over voltage from a memory matrix plane in coincidence with a strobe pulse. A read amplifier consists of two differential amplifiers, Q1, Q5, and Q2, Q6, pulse rectifier Q2, Q7, and output stage Q4. One end of a matrix plane sense winding is connected to input capacitor C3 , and the other end is connected to input capacitor C9. Since the sense windings are laced through the cores in opposing directions (paragraph 4-211), a turn-over signal may be of either polarity.

4-148. READ ZERO. The Q1, Q5 push-pull input accepts positive or negative core turn-over signals at either base. Matched emitter and collector load resistors ensure that the quiescent base bias maintains equal currents through both transistors.

4-149. Differential amplifier Q2, Q6 is nearly identical to the input amplifier. Pulse rectifier Q3, Q7 is cut off by the +24 volts and operates as a full-wave rectifier. In the absence of an input signal its common emitter potential holds Q4 conducting, and terminal 7 is zero volts. A positive read strobe in the absence of a core signal reverse biases diode CR3, and the circuit delivers a zero volt output at read time.

4-150. READ ONE. When the turn-over voltage from a selected core moves Q1 negative and Q5 positive, the change in collector potentials is coupled to the succeeding amplifier. The negative going Q2 collector potential causes Q3 to saturate, while Q7 is cut off.

4-151. Q4 is cut off by Q3 conduction and the circuit output rises from zero to +3.5 volts, the quiescent strobe level coupled through CR3. A strobe raises the output to +9 volts at read time to indicate a ONE. Core turn-over voltages resulting from a memory clear and write or master clear operation cut off Q4 and develop a +3.5 volt pedestal, but the read strobe is not received.

4-152. Input signals of reversed polarity that move Q1 positive and Q5 negative also result in Q4 cut-off and a +3.5 to +9 volt output at read time.

4-153. A binary ONE is represented by the +9 volt pulse resulting from coincident core turn-over and read strobe voltages. A zero volt level at read time represents a binary ZERO.

4-154. COUNT LOGIC-A CARD.

4-155. GENERAL. (See Drawing 11922.) Unless the RB memory system is ordered with count options, the count logic cards are not included. The first option is inclusion of these cards to allow the address register (AR) to add or subtract one digit from the address register (count) when driven by an externally generated count pulse and a Forward or Reverse control level. An additional option is the inclusion of a separate transpose register (TR) which operates with the count logic cards to permit the use of widely separated memory areas in an interlaced mode. With this optional equipment, a variety of operations may be performed. As in the option which includes the count logic cards but omits the transpose register, the count in AR may be stepped in either direction. However, inclusion of a TR also permits transposition of the contents of AR and TR with the ability to enter TR either what was in AR, or that number plus one, or minus one.

4-156. Three count logic cards, one for each AR module, operate to add or subtract one digit from the address register upon receipt of externally generated input signals. The AR add or subtract (count) operation is initiated when either the forward or reverse control levels are positive and a count pulse is received. This count must occur between buffer cycles, or coincident with a load or unload sync pulse. Any number of consecutive counts may be used to count the address register to a desired address.

4-157. The address register is organized into three groups of flip-flops. The first group of 4 flip-flops is organized as a 4 bit module and counts from zero through 15. A second group is also organized as a 4 bit module and counts from zero through 15 at the rate of one count each time the first group develops a carry voltage. A third group is organized as a 2 bit module and counts from zero through 3 at the rate of one count each time the second group develops a carry voltage. Each module counts in pure binary and is controlled solely by its associated count logic.

4-158. REGISTER CODING. The first 4 flip-flops of the address register comprise the least significant module (LSM). The adjacent group of four is the next least significant module (NLSM) and the remaining 2 are designated as the most significant module (MSM). A maximum modulo of 16 in the LSM and NLSM and of 4 in the MSM provides the AR with a range of 1024 digits (16 x 16 x 4).

4-159. COUNT FORWARD. A positive forward level at terminal V permits a count pulse to pass through those set and reset gates on the count logic cards which have been energized by the gate control

inverters and count up the corresponding AR flip-flops. The forward level for the LSM count logic card is externally generated; the forward level for each subsequent card is generated by the preceding card. An externally generated count pulse, transformed to +6 volts in the input card is applied to each count logic card for each count. When the count pulse occurs, only AR is affected; even if the TR option is included, TR is unaffected.

4-160. A forward level of +6 volts to the count logic card cuts off transistor Q1 and its collector assumes a -6 volt potential, clamped by CR9. The output of Q1 feeds a chain of cascaded carry logic gate circuits which perform the "carry" logic for successive stages of the AR module by gating the gate control inverters. The least significant flip-flop (LSF) of the AR module is controlled through a circuit which includes transistor Q3. Q1 collector is connected to Q3 base through R6 to form one leg of a gate. This gate has two terms that are implemented by resistors R5 and R6.

4-161. If both Q1 and Q2 are conducting and apply +3.5 volts to R6 and R5 respectively, as is the case if neither the Forward nor Reverse control line to this card is positive, Q3 will be cut off. However, when Q1 is cut off by a positive Forward level, its negative collector voltage causes Q3 to saturate. This raises Q3 collector to nearly +3.5 volts. The collector of Q3 feeds set and reset gate circuits that gate each side of the LSF in the AR module. The set gate consists of C44, C4, R36, CR31 and R19; the reset gate is CR43, C3, R35, CR30 and R18. Diodes CR12 and CR13 couple the Q3 collector voltage to diodes CR30 and CR31 respectively. When the LSF is in the ZERO (reset) state the cathode of CR31 is positive, and current through resistor R19 makes the anode of set gate diode CR31 positive. This voltage rise is coupled through R36 to place a small forward bias on diode CR44.

4-162. When the count pulse occurs, it is coupled through C4 and CR44 to the set terminal of the LSF, triggering it to the ONE state. The reset gate connected to Q3 collector includes diodes CR43 and CR30. This gate is not enabled when the LSF is in the ZERO state, since the cathode of CR30 is connected to the LSF ONE side output, which is negative at that time. When the flip-flop has been set to the ONE state as described, the voltage on CR30 rises and enables the next count pulse to pass through diode CR43 to reset LSF to the ZERO state. The set gate is inhibited at this time.

4-163. The first carry gate consists of CR6 and CR15. The carry is propagated only when the anode of CR6 is negative (forward status) and when CR15 anode is negative (LSF flip-flop in the ONE state). When these conditions are met, current through R8 causes Q4 to conduct.

4-164. Gate control inverter Q4 energizes the set and reset gates for the next least significant flip-flop (NLSF), and have the same operating principles as described for the Q3 circuit. Q4 is enabled by a carry logic gate whose inputs consist of Q1 and the ZERO side of the LSF. A count pulse therefore complements the NLSF whenever the LSF is in the ONE state. A flip-flop false output is +3.5 and -6 volts when the circuit is at ZERO and ONE respectively. The true outputs are direct opposites of the false. Q5 controls the next most significant flip-flop (NMSF) and is enabled by a gate whose terms are the output of CR7 and the ZERO side of the NLSF. The count pulse therefore complements the NMSF whenever the LSF and NLSF are not ONE.

4-165. The most significant flip-flop (MSF) in the module is controlled by Q6. A carry logic gate with the output of CR8 and the ZERO side of the NMSF as inputs, produces conduction bias for the Q6 base. The count pulse is permitted to complement the MSF only when all of the less significant flip-flops are in the ONE state.

4-166. Until a count of 15 is reached, one or more of the gating diodes on the input of NPN Q8 are positive and Q8 is conducting. The cathode of CR58 is positive and current for the base of Q8 is supplied through R43. When the count of 15 is reached in the forward status, all terms of the input gate go negative and current through R48 pulls CR43 negative to cut off the transistor. The output line is taken from the Q8 collector and applied to the count logic card for the NLSM via terminal 5. It permits the NLSM to count forward on the next count pulse. A count pulse with a module at 15 brings every flip-flop in the module to the ZERO state.

4-167. Q8 cut off also furnishes a positive voltage to reverse bias the Q9 base, and a positive "INHIBIT" voltage. The Q9 negative collector output ("FORCE") and the "INHIBIT" output are not used on standard memory models (refer to paragraph 4-174, modulo selection).

4-168. COUNT REVERSE. A positive reverse level at terminal W in conjunction with a positive count pulse input enables each count logic card to produce set and reset pulses to count down its corresponding module of AR flip-flops. The reverse level for the LSM card is externally generated; the reverse level for each subsequent card is generated by the preceding card. An externally generated +6 volt count pulse is always applied to each count circuit if a count is desired.

4-169. During application of a reverse level to the counter, Q2 cuts off to bias Q3 into conduction. The carry logic gates and

operation of the Q4, Q5, and Q6 inverters and their respective set and reset circuits is identical to the count forward function, except that inputs to the carry logic gates are taken from the ONE side of the module flip-flops. They are all positive when the associated module is at ZERO.

4-170. The final reverse carry logic gate on each count logic card includes diodes CR29 and CR41. All four AR flip-flops associated with a given count logic card must be in the ZERO state for the output of this carry logic gate to go negative. This circuit controls Q7, allowing its collector to rise to +6 volts at the count of ZERO. This is the reverse carry output level. The reverse carry level leaves the card at terminal E and enters the count logic card for the next module on the reverse level input, terminal W. With the reverse input to the next module count logic card positive, the next count pulse subtracts one digit from the address in this module and counts the less significant down to 15.

4-171. All ZERO's in the address register implies a ZERO in each module and represents address zero. This condition permits the next reverse count to complement every flip-flop in every module and set all ONE's in the AR. The modules then contain 15, 15 and 3, in the coded figure for address 1023.

4-172. TRANSPOSE. The transpose register is organized into modules in the same manner as the address register. A forward or reverse level input to the count network in conjunction with a Transpose pulse input to the transpose register flip-flops adds or subtracts one digit from the address information entering TR. The count network input to each TR flip-flop consists of a carry level.

4-173. The gate control inverters furnish positive carry levels to their respective TR flip-flops when they are driven into conduction by their input carry logic gates. Paragraphs 4-159 through 4-170 describe the selection and operation of the gate control inverters with a forward or reverse input signal to the count network.

4-174. MODULO SELECTION. The foregoing descriptions define count network operation with standard memory modules. When the unit is employed with a system using a decimal (or other) address structure, the count networks are slightly modified to establish modulos compatible with memory address requirements. This is achieved by the force and inhibit circuitry. Table 4-2 shows the modulos for the four standard memory configurations.

4-175. Any of the count network modulos may be modified by changing the gating on the Q8 base to generate "FORCE" and "INHIBIT" levels

TABLE 4-2. STANDARD RB MEMORY MODULOS.

Memory Model	Least Significant Module	Next Least Significant Module	Most Significant Module
128	16	8	
256	16	16	
512	16	16	2
1024	16	16	4

at a number less than 15. The force and inhibit voltages over-ride or block the carry logic gates at the input of selected gate control inverters and thus enable the next count to set the module to zero. Force and inhibit circuitry is not included in standard memories or on Drawing 11922.

4-176. The three modules are normally set to count binary but may be counted as binary coded decimal in non-standard modules. When used as binary coded decimal the count network operates modulo 999. Logic for this system is not included in this manual.

4-177. The four left hand columns of Table 4-3 show the state of each flip-flop in a module for every count from zero through 15. The force or inhibit voltage that must be applied to each gate control inverter can be deduced from the four right hand columns. These columns indicate when a specific flip-flop should be forced to complement or inhibited from complementing in order to attain a zero count in the module. To operate at modulo seven, a module count of seven must complement the NMSF and NLSF and inhibit the MSF and LSF from complementing. When the module is at six the count logic card must generate voltages that enable or inhibit the appropriate gate control inverters per Table 4-3.

4-178. BQ LOGIC CARD.

4-179. GENERAL. An optional BQ logic card enables the RB memory to operate interlace without the normal requirement of an externally generated count or transpose pulse. The single BQ logic card contains seven individual circuits, identified as circuits 100 through 700 on Drawing 12195.

TABLE 4-3. MODULE COUNT AND FORCE/INHIBIT GATING.

Flip-Flop State				MODULO	Force & Inhibit Gating			
MSF 2^3	NMSF 2^2	NLSF 2^1	LSF 2^0		MSF 2^3	NMSF 2^2	NLSF 2^1	LSF 2^0
0	0	0	0	1	I	I	I	I
0	0	0	1	2	I	I	I	F
0	0	1	0	3	I	I	F	I
0	0	1	1	4	I	I	F	F
0	1	0	0	5	I	F	I	I
0	1	0	1	6	I	F	I	F
0	1	1	0	7	I	F	F	I
0	1	1	1	8	I	F	F	F
1	0	0	0	9	F	I	I	I
1	0	0	1	10	F	I	I	F
1	0	1	0	11	F	I	F	I
1	0	1	1	12	F	I	F	F
1	1	0	0	13	F	F	I	I
1	1	0	1	14	F	F	I	F
1	1	1	0	15	F	F	F	I

4-180. CIRCUIT 500. Circuit 500 receives either a positive or negative externally generated level at terminal 19, and delivers an output at terminal 3 that rises from zero to +6 volts. A reference potential that is one-half the amplitude of the BQ input is applied to terminal 20. A plug-in adapter serves as an input mode selector that enables either a positive or a negative voltage

to drive transistor Q1 into saturation. The BQ voltage must be of the same amplitude as the other externally generated control levels.

4-181. When used with a positive going input voltage, the input selector places a positive reference potential on the emitter of Q1 to hold this transistor cut off when the BQ level at terminal 19 is low. Voltage divider R2, CR1, R3 enables the +24 volts to cut off Q2, and the terminal 3 output is clamped near zero volts by diode CR4.

4-182. A positive BQ input results in Q1 saturation. Q2 is also saturated and its collector current holds terminal 3 at approximately +6 volts for the duration of the positive input.

4-183. CIRCUIT 400 AND 700. These circuits differ only in their terminal pin numbers and in the signals at their inputs and outputs.

4-184. The signal inputs to Circuit 400 consist of a load sync (terminal 24) and a $\overline{L}$ level from the L/U (Load/Unload) flip-flop (terminal 22). Signal outputs consists of a load sync (terminal 1) and an L level (terminal 2) that are applied to the input of Circuits 100 and 600. The signal inputs to Circuit 700 are an unload sync (terminal 23) and an L level from flip-flop L/U (terminal 21). Signal outputs are an unload sync (terminal 4) and an L level (terminal 5), also applied to the input of Circuits 100 and 600. Because the L and $\overline{L}$ inputs are inverted by Q1, they respectively appear as $\overline{L}$ and L at the circuit output.

4-185. The input to transistor Q1 will be either +3.5 or -6 volts, depending on the state of flip-flop L/U. A positive input cuts off Q1 and enables diode CR1 to clamp the output at zero volts. A negative input level saturates the transistor, developing +6 volts output.

4-186. When a positive load or unload pulse is applied to the Q2 base, the transistor conducts to produce a +6 volt output. The externally generated input sync voltages are applied only to a d-c amplifier before arriving at the Q2 input, so may possess an unsatisfactory pulse width. Inductor L1 differentiates the input signals to ensure a properly shaped pulse. Diode CR3 limits the negative overshoot when the L1 field collapses.

4-187. CIRCUIT 300. This circuit develops a clear AR pulse to set the Address Register to zero when the BQ level is zero and a master clear pulse is received.

4-188. A positive BQ input (terminal 3) saturates Q1 to clamp the Q2 emitter (terminal 17) to zero whether or not a master clear pulse is applied to the base of Q2. However, when the BQ input is zero, Q1 is cut off and Q2 conducts. The clear AR output at terminal 17 is still zero, but when a master clear pulse is applied to the Q2 base, Q2 current is decreased and the emitter voltage rises to produce a replica of the input clear signal.

4-189. CIRCUIT 200. A BQ control level and a master clear pulse are respectively applied to terminals 3 and 14 as inputs to this circuit. Its output consists of a positive 0.5 to 1 usec pulse that rises from +3.5 to +9 volts and sets the Address Register to all ONEs; the Transpose Register to zero.

4-190. The BQ level and master clear inputs each constitute one leg of an AND gate. A zero volt level on either leg places a zero volt level on the anode of coupling diode CR3 and enables the -6 volts to supply current to the Q1 base. Transistor Q1 is held in saturation until both legs of the AND gate input go positive. Capacitor C1 cannot couple static Q1 collector current into the Q2 base, so this transistor is held at cutoff. The set AR and TR output line remains at +3.5 volts.

4-191. A positive BQ level in conjunction with a master clear voltage permits CR3 to couple a cut-off voltage to the Q1 base. When Q1 cuts off, current through inductor L1 is abruptly stopped. The collapsing L1 field develops a negative voltage that is coupled through C1 and produces Q2 saturation. Collector current through transformer T1 develops an output pulse that rises from +3.5 to +9 volts. Diode CR1 limits T1 overshoot when the pulse falls. Resistor R9 and diode CR7 comprise a feedback loop that improves pulse rise time.

4-192. CIRCUIT 100. Interlace operation with the BQ logic card selected requires the BQ circuits to generate a count pulse for each load sync or unload sync that is preceded, respectively, by a load sync or unload sync. This is the function of circuit 100. Circuit operation is controlled by two sets of input signals, either of which enables the card to generate a count pulse for the count network.

4-193. Terminals 1, 2 and 3 respectively connect the load sync, L and a BQ level to one of two AND gate inputs. Terminals 4, 5, and 6 respectively connect the unload sync, $\overline{L}$ and a BQ level to the second AND gate inputs. Each AND gate output forms one leg of a two term OR gate, diodes CR4 and CR7, that controls transistor Q1. A count pulse that rises from +3.5 to +9 volts is produced at

terminal 11. Terminal 9 may receive an externally generated count pulse output that is placed on a +3.5 volt level and then applied to the count pulse output at terminal 11. A count pulse input to terminal 9 is not normally used during BQ operation.

4-194. A zero volt BQ input holds both AND gate outputs, and the OR gate output at zero. Q1 is forward biased and maintains Q2 in saturation. There is no voltage coupled through capacitor C2 and transistor Q3 is reverse biased by the +6 volts. The output at terminal 11 is a quiescent +3.5 volts.

4-195. A positive load sync pulse in conjunction with a positive BQ level (BQ operation selected) and a positive level from L produces a positive output from one of the two input AND gates. If the preceding command was a buffer load, L/U will have been set by a load sync at the start of that cycle. This logic enables the BQ circuits to generate a count pulse only when the existing command is the same as the preceding command.

4-196. A positive potential at the anode of CR4 forward biases emitter follower Q1 and is coupled through the low base-emitter resistance to forward bias the anode of diode CR8. The Q2 base is reverse biased and collector current through L1 is abruptly stopped. The collapsing field develops a negative voltage that is coupled through C2 and produces current in the Q3 base. Saturation collector current through transformer T1 produces a count pulse output that rises from +3.5 to +9 volts.

4-197. A second set of input signals, ULS, $\overline{L}$ and BQ operate the other input AND gate. If an existing buffer unload command was not preceded by a similar command, the $\overline{L}$ output will be zero and the gate output zero. A count pulse would not be generated. All circuit functions are identical to the operation described in paragraph 4-194. The input terms for both AND gates are received from the outputs of Circuits 400, 500, and 700.

4-198. CIRCUIT 600. Interlace operation with the BQ card selected requires the BQ circuits to generate a transpose pulse for each load sync or unload sync that is preceded, respectively, by an unload sync or load sync. This is the function of circuit 600. The circuit consists of two three-term AND gates and one OR gate. Each AND gate output is applied to the OR gate as an input term.

4-199. Terminals 1, 5, and 3 respectively receive LS, $\overline{L}$, and BQ as input terms to one of the two AND gates. Terminals 4, 2, and 3 respectively receive ULS, $\overline{L}$ and BQ as input terms to the second gate. The transpose pulse output is taken from terminal 18.

4-200. A load sync in conjunction with a BQ level and $\bar{L}$ from the L/U flip-flop will enable the first AND gate to place a positive transpose pulse on diode CR4 and the output line. Because the two associated inputs are levels, the LS signal will determine the timing of the output transpose pulse.

4-201. If the preceding command was a buffer unload, L/U will have been reset by an unload sync at the start of that cycle. The load sync associated with the existing load command will set L/U and simultaneously cause the AND gate to develop the transpose output. The AND circuit is enabled by the previous state of flip-flop L/U, not by the state attendant on the existing load command. This logic enables the BQ circuits to develop a transpose pulse only when the existing command differs from the immediately preceding command.

4-202. An unload sync in conjunction with a BQ level and an L level from the L/U flip-flop will enable the second AND gate to place a transpose pulse on diode CR6 and the output line. If the preceding command was a buffer load, L/U will have been set by load sync at the start of that cycle. The unload sync associated with the existing unload command will reset L/U and simultaneously cause the OR gate to develop the transpose output. The terms for both AND gates are received from the outputs of Circuits 400, 500, and 700.

4-203. MAGNETICS MODULE.

4-204. GENERAL. (See Figures 4-2 and 4-3.) The function of the Magnetics Module (Memory Module) is to store a maximum of 1024 24-bit words when operating with the 1024-RB-24 General Purpose Memory. Section One defines the storage capacities of Magnetics Modules associated with other RB system configurations. Circuit logic for these is identical to the 1024-RB-24 described below; only the number of digit planes and/or storage addresses will differ.

4-205. The Magnetics Module consists of arrays of ferrite storage cores assembled in matrix planes. There are 24 matrices in the module with 1024 storage cores in each matrix. Each matrix is capable of storing one bit of binary information in a storage core at each of the 1024 possible address positions.

4-206. Each core has six wires threaded through it; 2 X-Y lines for core set, 2 X-Y lines for core reset, a sense winding and an inhibit winding. There are 24 separate sense and 24 separate inhibit windings (RB-24 memory), one for each matrix.

4-207. CORE CHARACTERISTICS. The storage device used in the RB Memory system is a ferrite core (toroid) with a substantially

rectangular hysteresis loop, as illustrated in Figure 4-2. Every core can be magnetized to one of two discreet and stable (remanent magnetic) states commonly called ONE and ZERO. A drive pulse, P, will drive a core into the ONE state (SET) while a pulse in an opposite direction, N, will drive it into the ZERO state (RESET). The squareness of the loop makes it possible to drive a core up to a certain point (knee) without materially changing its remanent magnetic state, and then to switch it very quickly by driving just beyond this critical point. This permits a coincident current type of operation, requiring the coincidence of two half-select currents for switching a core. Conversely, switching of a core can be prevented through cancellation of one of the two coincident drive pulses by means of an inhibiting (opposing) drive pulse.

4-208. X AND Y DRIVE LINES. Every matrix plane contains 64 rows of X drive lines and 64 columns of Y drive lines controlled by the X and Y switches. The 64 X and 64 Y lines are paired to provide 32 X rows and 32 Y columns. This network of 32 X 32 coordinates furnishes a total of 1024 intersects, one intersect for each storage core. Each intersect consists of one pair of X and one pair of Y lines. One group of X-Y lines provides current pulses that set the cores to their ONE state; the second group of X-Y lines furnishes current to reset the cores to their ZERO state.

4-209. The X and Y lines each carry only half the current required to turn over a core. A full-select magnetomotive force to set or reset a core is produced by coincident X and Y currents at one of 1024 addresses in each matrix plane.

4-210. SENSE WINDING. The sense winding in a specific matrix plane passes through every core within the plane and drives the single sense amplifier associated only with that plane. Core turn-over from a ONE to a ZERO state, or vice-versa, induces a voltage in the sense winding which is connected to the input of a sense amplifier. A read strobe pulse, generated in the timing and control circuits, is required to gate the sense amplifiers before a core turn-over signal can be delivered as an information output signal.

4-211. Although coincident half-select currents from the X and Y lines are required to change the state of a core, the cores on the selected X and Y wires are affected to some extent by the half-excitation X and Y pulses. The sense winding is therefore interlaced through the cores in such a manner as to cancel these small spurious signals from half-selected cores. The sense winding is arranged so that cancellation occurs in pairs of cores.

4-212. INHIBIT WINDING. A separate inhibit winding threads through every core within a specific matrix plane and is driven by a single inhibit driver associated only with that plane. The inhibit winding supplies a half-select current that opposes the effect of the Y drive line current to prevent a selected core within a specific matrix from turning over when a ZERO is being written into the Magnetics Module. Since both X and Y lines must be simultaneously energized with half-select currents to switch a core, opposition to the Y drive line current by a half-select inhibit current will nullify the result of X and Y coincidence. During a CLEAR operation all inhibit windings are energized with full-select currents to reset every core to its ZERO state.

4-213. POWER SUPPLY.

4-214. GENERAL. (See Drawing N12149.) The transistorized power supply develops seven regulated d-c voltages and the temperature compensated X-Y drive current source. Each of the regulated voltages is maintained within 2 per cent of the rated output. Four bridge rectifiers provide outputs that are separately fused and filtered before application to their respective circuits.

4-215. Start switch S3 energizes relay K2 to apply 115 volts single phase power across the primary of transformer T1. When S3 closes, a pulsating d-c voltage from diode rectifier CR7 is applied across capacitor C7 and relay K2. K2 immediately closes and then re-opens when the pulsating d-c has charged C7 to an appreciable percentage of the applied voltage. The capacitor's charging time determines the interval that the relay remains closed. If the required d-c voltages rise to their correct levels, relay K1 is energized to provide a latch (lock-up) circuit for T1 power before K2 re-opens.

4-216. Failure of a regulated output at any time immediately opens K1 and removes the prinary line voltage. If the regulated supplies do not rise to their correct levels, depressing the start switch will not energize K1 until five seconds after the first attempt. This delay is introduced by the C7, R48 discharge time constant and protects the power supply from continuous attempts by the operator to apply power to the system when it is malfunctioning. K1 and K2 are shown in their de-energized states on Drawing N12149.

4-217. Thermal switch S5 is located in the blower wind tunnel and opens when the temperature reaches 85 degrees centigrade. If actuated, S5 will remain open for a period of at least one hour and cannot be manually reset. All connections to the power supply are made through a terminal board mounted on the rear of the hinged chassis.

4-218. The regulated supplies are arranged in series in order to minimize dissipation in the series regulating transistors, and to reduce voltage stress across rectifiers and capacitors. In addition, this permits a desirable inter-relationship between voltages during the initial rise when power is first applied.

4-219. The +24 volt power supply level will be described first, since it is used as a reference for all other supply voltages. The +24 volts is connected in series with the +6 volt supply as described above, and therefore is only required to develop 18 volts.

4-220. +24 VOLTS. A transformer secondary winding which connects to bridge rectifier CR12 supplies power to this circuit. The unregulated, pulsating d-c is filtered in C9. The partially filtered voltage across C9 is designed to slightly exceed the +18 volts required from this supply, under minimum a-c input voltage conditions. Transistor Q22 is the series regulating transistor; it is controlled by a feedback amplifier and a voltage reference Zener diode. The base current to Q22 is developed by a smaller transistor Q23, also used as an emitter follower. Current from the emitter of Q23 provides the base of Q22 with the appropriate base current, as determined by the voltage comparator portion of feedback amplifier, Q24 and Q25. Zener reference diode CR13 provides a reference voltage at the base of Q24.

4-221. When the power supply is initially energized, the emitters of Q24 and Q25 move in a positive direction since they are returned via R59 to the positive side of the rectifier circuit. The base of Q25 initially rises faster than the base of Q24 since no current flows through Zener diode CR13 until its operating (break down) voltage is reached. Saturation Q24 current through common emitter resistor R59 furnishes the initial reverse bias that momentarily holds Q25 cut off. With Q25 non-conducting, all of the current through resistor R49 flows into the base of emitter follower Q23. The resulting amplified current is applied to the base of Q22, causing this transistor to conduct.

4-222. Increasing Q22 conduction lowers the voltage drop across its emitter-collector impedance and forces the positive terminal of the supply to a higher voltage. As the output voltage approaches its prescribed value, the relative voltages on the bases of Q24 and Q25 converge and Q25 begins to conduct, decreasing the turn-on base current previously supplied to Q23 until a point of equilibrium is reached and the circuit is regulating. Potentiometer R57 is used to initially set the output at +24 volts.

4-223. Switch S2 permits the output voltage to be shifted 5% higher or lower than normal for marginal checking purposes. This is accomplished by switching additional resistances R58 or R61 into the divider network or Q25 base.

4-224. The +24 volt supply is used as the reference for other regulating circuits. One of these, the +6 volt supply, uses resistance divider network R46 and R44 to establish the base potential of Q21. The emitter of Q21 is connected to the +6 volt output line. If +6 volts is low, Q21 is reverse biased and current through R42 flows into cascaded emitter followers Q20 and Q19, causing heavier conduction in Q19 and a correspondingly lower voltage drop across it. This raises the output voltage of the +6 volt line toward its proper value. In operation, the emitter of Q21 diverts the proper amount of current from R42 so that a stabilized operating point of +6 volts is obtained from the supply.

4-225. For marginal voltage checking, the output of the +6 volt supply varies in proportion to the +24 volt supply, since no separate margin switch is provided. The +6 volt supply is required to provide not only the current for +6 volt loads, but also the current taken by +24 volt loads, since that supply is arranged in series with the +6 volt unit. An additional 3.5 volt output is obtained from +6 volts by the use of three silicon diodes in series to provide the proper voltage drop.

4-226. -12 VOLTS. The -12 volt supply is regulated by a circuit similar to those previously described. The +24 volt supply is used as a reference level and applied through a resistance divider network R63 and R28 to the base of Q12. Since a larger current is required of the -12 volt supply, three power transistors, Q8, Q10 and Q11 are paralleled to carry the current. Equalizing resistors R19, R21, and R27 are placed in the emitter lead of each of these transistors.

4-227. A marginal checking facility for the -12 volts is provided by switch S1. This switch increases or decreases the resistance in series with the voltage divider network to the base of Q12. However, since the reference voltages are obtained from the +24 volt supply, it is desirable to eliminate the effect of margining that supply. For this reason, when the +24 volts is margined a separate section of switch 2 places a compensating series resistance in the divider chain to the -12 volt potential so that the prescribed variations of +24 volts do not affect the -12 volt supply.

4-228. -6 AND -3 VOLTS. Two other regulating circuits are connected to the regulated -12 volt output. One of these includes transistors

Q15 and Q17. The circuit operation is again similar to that previously described. The emitter of Q15 is connected to the -6 volt output terminal. A regulator consisting of transistors Q16 and Q18 is connected to this regulated -6 volt terminal and provides a stabilized -3 volt output. Since the load on this -3 volt supply may be of either polarity, load resistor R41 is connected across the output of this supply voltage to ground so that this level may be used as a sink for up to 100 ma if required by the external connections and choice of signal levels supplied by the customer. Both the -6 and -3 volt supplies are margined in conjunction with the -12 volt supply by means of switch S1.

4-229. -24 VOLTS. The -24 volt regulating circuit consisting of transistors Q1, Q2 and Q5 receives power from a transformer secondary via bridge rectifier CR1 and filter capacitor C1. This supply is connected in series with the -12 volts. Therefore, all current required by -24 volt loads must also be generated by the -12 volt supply. Margining of the -24 volt supply is performed concurrently with other negative levels by means of switch S1.

4-230. X-Y DRIVE CURRENT SUPPLY. The temperature compensated current supply Q3, Q4, Q6 and Q7 provides X and Y drive line currents that decrease linearly with increasing operating temperatures. Resistor R18 is a sensistor (temperature sensitive resistor) with a calibrated positive temperature coefficient. It is mounted on the power supply directly beneath the Magnetics Module, and furnishes a Q7 base bias that varies with changes in the magnetics operating temperature.

4-231. An increase in environmental temperature moves the Q7 base in a negative direction and the Q4 base in a positive direction. The base voltage of emitter-follower Q4 appears at its emitter and on the base of Q3. This positive going change on the Q3 base is similarly coupled to its emitter to decrease the voltage applied to the load. Series resistors R3 and R8 determine the drive current amplitudes.

4-232. Potentiometer R16 is adjusted to provide a -16.6 volt output at a temperature of 25 degrees Centigrade.

4-233. VOLTAGE SENSING. Transistors Q13, Q14, and Q26 constitute a voltage sensing circuit that removes the 115 volt a-c primary supply if the regulated voltages are more than 15 percent from their prescribed values. The three transistors are conducting when the supply outputs are at their correct levels and relay K1 is closed. If any one of the three transistors fails to conduct due

to a failure in the power supply or voltage sensing circuit, relay K1 is de-energized.

4-234. K1 is held energized by current flow through Q14. Zener diode CR3 and diodes CR4 and CR5 maintain a fixed reference potential of -6.4 volts on the Q26 emitter. If the -24 and -6 volt outputs are correct, Q26 conducts to forward bias the Q14 base with the -6.4 volt reference potential.

4-235. The +24 volts normally places a forward bias on Q26. The Q26 base then assumes the 6.4 volt reference potential on its emitter and places a back bias on the anodes of diodes CR16, CR17 and CR18. Q26 may be reverse biased by: a negative going change in the -6 volt output which is coupled through CR18, a negative going change in the -24 volt output which is coupled through CR16, or a positive going change in either output which is coupled through CR17.

4-236. Positive going changes are coupled through diodes CR14 and CR15 to cut off Q13. Current from the -24 volts then flows through CR17 and resistor R25 to reverse bias Q26. With Q26 cut off, the +24 volts places a reverse bias on Q14 to de-energize K1. The positive power supplies are all interdependent due to their series output.

4-237. Monitoring of the -24 volts also serves to indicate failures in the -12 volts since these two supplies are connected in series. Because the +24 volts is used as a reference by the other supplies, any failure in this output will be recognized by a shift in the -24 volts. Potentiometer R30 is factory adjusted and should not be reset in the field.

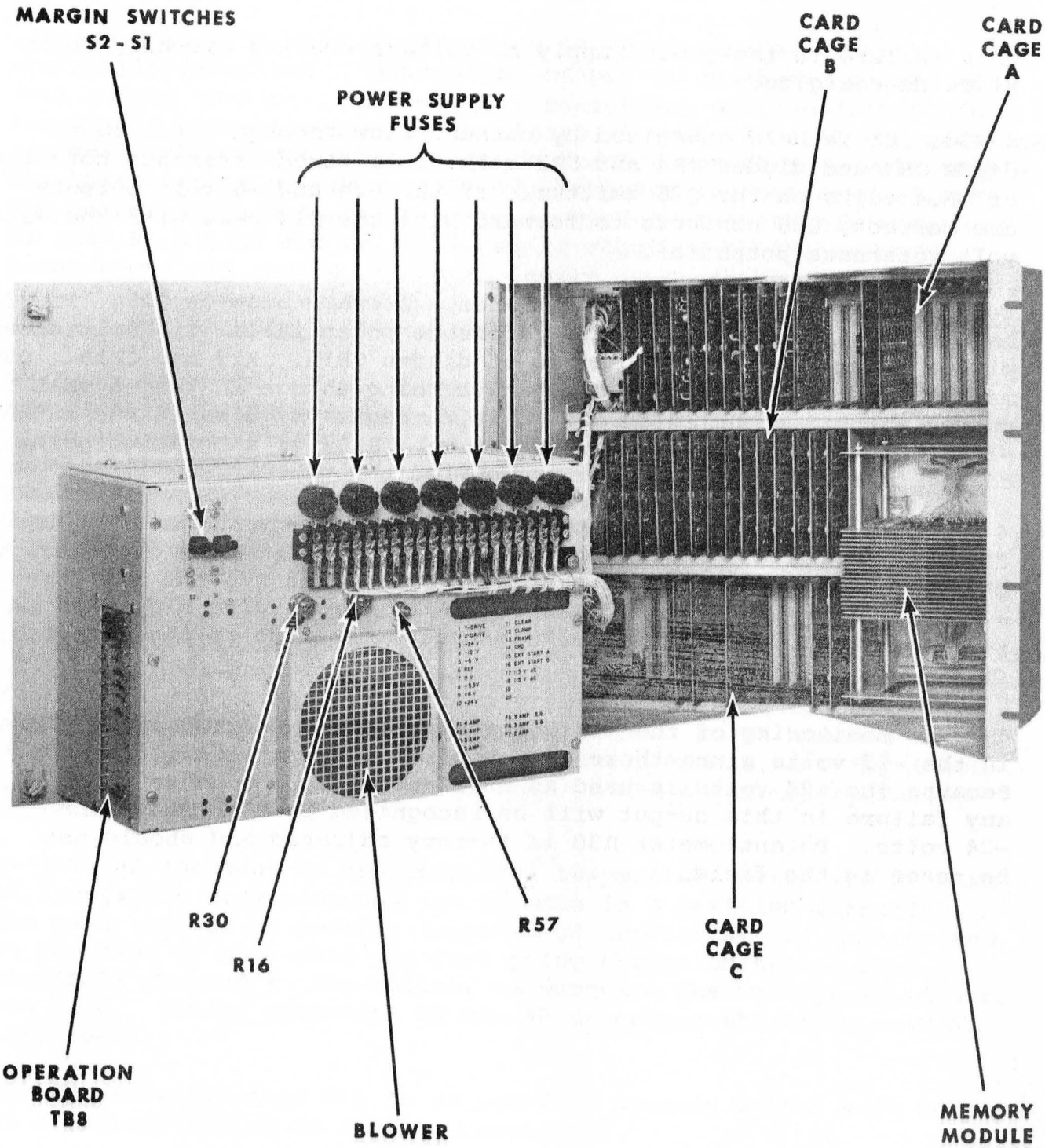


Figure 5-1. Type RB General Purpose Memory, Front Panel Open

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section of the manual contains information on the maintenance of the RB General Purpose Memory. Data is included on the required test equipment, repair procedures, and trouble-shooting techniques.

5-3. TEST EQUIPMENT.

5-4. Table 5-1 lists the test equipment required to properly service the RB memory.

TABLE 5-1. TEST EQUIPMENT REQUIRED

ITEM	CHARACTERISTICS
1. Oscilloscope	1. Tektronix, Inc., Type 531, 541 or equivalent.
2. Multimeter	2. Simpson 260, or equivalent, with milliammeter, voltmeter, and ohmmeter functions.
3. Alligator Clips	3. Mueller Electric Co. Mini-Gator #30 with #32 sleeve, or equivalent, to be used at terminals.
4. Differential Pre-amplifier	4. Tektronix Inc., Type G or equivalent.
5. Extender Card-Long N12449	

5-5. MECHANICAL INTEGRITY.

5-6. Determine that mechanical connections are secure before employing more advanced trouble-shooting procedures. Check that nuts and bolts holding connectors are not loose, that the unit is not

physically damaged, and that no wires have been torn loose accidentally. Make certain electrical connectors fit firmly in their sockets.

CAUTION

The printed circuit card sockets are not keyed, so it is possible to insert a printed card in the wrong socket. Use constant care to avoid this (see Figure 1-2). Although the card will not be damaged electrically, the system will not operate. Ascertain that all cards are firmly seated in their receptacles.

5-7. PRINTED CIRCUIT CARDS.

5-8. SPARE CARDS. Table 5-2 lists the printed circuit cards suggested as spares for maintenance and as aids in trouble-shooting. Also listed are the assembly and schematic drawing numbers.

TABLE 5-2. SPARE CARD LIST

Type	No. Recommended	Card Ref.	Assembly Dwg. No.	Schematic Dwg. No.
Input-A	1	IN-A	11931	11930
Timing-A	1	T-A	11927	11926
Register-A	1	R-A	11921	11920
Switch-A	1	S-A	11919	11918
Inhibit-A	1	I-A	11917	11916
Read Amplifier-N	1	RA-N	12174	12173
*Count Logic-A	1	CL-A	11923	11922
*Transpose Register-A	1	TR-A	11925	11924
*BQ Logic	1	BQL	12196	12195

*Indicates optional equipment

5-9. HANDLING PROCEDURES. The printed circuit cards are designed to operate at very low power levels. As a result, their contacts are sensitive to dirt, dust. moisture and corrosion. They should never be inserted into the memory without cleaning. This is accomplished as follows:

(1) Wipe each contact with a cloth moistened with trichloroethylene, or equivalent.

(2) Erase the thin film left by the cleaning fluid from each contact with a rubber eraser.

(3) Wipe the rubber particles left by the eraser from the contact with a dry, lint-free cloth.

(4) Remove any loose surface metal between the plug-in contacts.

5-10. REPAIR PROCEDURES. The printed circuit cards can be serviced with the aid of the assembly drawings and schematics in Section VI.

5-11. TRANSISTORS. There is usually more than one transistor of a given type on each printed circuit card. If this is not the case, similar types may be found on adjacent cards. Suspected transistors therefore may be checked by substitution or resistance comparison. This latter method must be accomplished with an ohmmeter, exercising care to avoid damaging the transistors. Proceed as follows:

(1) Turn off the power and remove the questionable card.

CAUTION

Always turn off the power before removing or replacing a printed circuit card.

(2) Check the emitter-collector resistance of the transistor in both directions (alternate ohmmeter polarity) using the meter scale which applies the least amount of current to the transistor.

(3) Replace the transistor (refer to paragraph 5-14) when the readings differ by more than 10% of the values obtained for other transistors of the same type. Table 5-3 gives approved commercial equivalents of TM transistors. TM 12051 (RCA 2N643) must be selected for a collector-to-emitter breakdown voltage of not less than 50 volts.

TABLE 5-3. TM SEMICONDUCTORS AND APPROVED EQUIVALENTS

Transistors	Manufacturer	Type
TM 12010	Delco	2N277
TM 12025	Sylvania	2N385
TM 12030	Delco	2N553
TM 12036	Philco	2N598
TM 12041	Philco	2N597
TM 12050	RCA	2N1301
TM 12051	RCA	2N643
TM 12053	RCA	2N404
Diodes		
TM 63006	Gen. Inst.	DR211
TM 63014	Transitron	SG22
TM 63015	Gen. Inst.	Spec.
TM 63023	Hughes	1N482
TM 64022	Hoffman	1N468

5-12. DIODES. Check diodes in the same manner as transistors, by comparison of the forward and backward resistance of one with others of the same type. If the resistance differs by more than 10%, replace the diode. Table 5-3 gives approved commercial equivalents of TM diodes. TM 63015 is purchased to TMI specifications, and does not possess a commercial equivalent.

5-13. RESISTORS AND CAPACITORS. Check these components by first ascertaining that one end is free, then using the ohmmeter in a conventional manner. A small capacitor may be quickly checked for an open circuit by applying a sensitive ohmmeter across its terminals and observing a needle "kick".

CAUTION

Never apply meter probes where there is any possibility that the meter current could damage a transistor.

5-14. COMPONENT REPLACEMENT. Replacing components on printed circuit cards presents problems not normally encountered in conventional electronic repair work. The following basic rules must always be observed:

(1) Use only top quality rosin core 60/40 solder, equivalent to that required by Federal Specification QQ-S-571, Sn-60.

(2) Use a small, hot iron and a heat sink to conduct heat away from other components while soldering. A large pair of pliers clamped to the wire being soldered will satisfy this requirement.

(3) Replace spaghetti taken from any wire during removal.

(4) Clean the solder grommets thoroughly by shaking the printed card over a cloth immediately after the hot iron is removed.

(5) Insert wires from new components into and through the grommets, then solder from the bottom of the board--never from the component side.

(6) Clip off surplus wire and examine the card very carefully for excess solder or possible strings of spilled solder. Check for rosin deposits, determining that joints are clean and bright, similar to factory quality.

(7) Refer to paragraph 5-9.

5-15. TROUBLE-SHOOTING.

5-16. GENERAL. In the absence of a firm clue to the problem area, memory system failures should be approached in two stages, preliminary and advanced.

5-17. PRELIMINARY TECHNIQUES. The preliminary trouble-shooting techniques should establish:

(a) The mechanical integrity (refer to paragraph 5-5) of the unit

(b) blower operation

(c) the presence of requisite d-c voltages at power supply terminal strip TS1 (mounted on the rear of the power supply cabinet Figure 5-1).

NOTE

Ascertain that all cards are firmly seated in their receptacles.

5-18. ADVANCED TECHNIQUES. If preliminary techniques have not corrected or located a failure, the advanced trouble-shooting

techniques should be employed. The logic drawings in Section VI should be consulted while analyzing system trouble. Paragraph 5-43 and succeeding paragraphs describe the use of these drawings for Magnetics Module continuity measurements and can contribute to an understanding of circuit layout. All oscilloscope and ohmmeter checks are referenced to the logic or schematic diagrams.

5-19. Power supply troubles can usually be recognized by failure of the START and STOP button lamps which indicate when primary power is removed from the supply. A 15 percent deviation of any output voltage will disconnect primary power from the RB system. Paragraphs 5-21 through 5-34 describe power supply trouble-shooting procedures.

5-20. POWER SUPPLY TROUBLE-SHOOTING. (See Figure 5-1.)

5-21. A-C INPUT. The green DS3-DS4 and amber DS1-DS2 lamps built into the respective START and STOP control buttons monitor the status of the 115 volts a-c power supply input. Power input to the K2 start relay is removed by an open fuse F5 or F6, or an overheated thermal switch S5. This is indicated when DS3-DS4 is extinguished. DS3-DS4 ON signifies that 115 volts is available for the start control circuits at the START button, but does not establish that a-c is applied to the power transformer primary. DS1-DS2 ON determines that 115 volts is applied across the primary of power transformer T1. This lamp is extinguished when a 15 percent deviation in any supply voltage enables the voltage sense circuit to remove 115 volts from the T1 primary, but DS3-DS4 remains illuminated.

5-22. Thermal switch S5 is mounted on the blower wind tunnel wall. When activated, the switch requires 60 minutes to reset itself and cannot be closed manually. Failure of the wind tunnel blower or an ambient operating temperature in excess of 185 degrees Fahrenheit (85 degrees Centigrade) will open the thermal switch and remove primary power from the supply.

5-23. START-STOP CONTROL. Primary power to the power supply can be controlled from a remote location, or by the START and STOP push-button switches, S3, S4. S3 starts the power supply; S4 stops it.

5-24. Remote start control is achieved by closing the external start circuit between terminals 15 and 16 of TS1. A push-button switch placed across these terminals will duplicate S3 operation. If terminals 15 and 16 are permanently jumpered, STOP switch S4 can remove primary power only while it is held manually depressed; 115 volt a-c is restored when pressure on the switch is released. Remote stop can be accomplished by opening the 115 volt a-c input circuit to terminals 17 and 18 on TS1.

5-25. BLOWER. The blower is wired across the a-c power line on the power supply side of fuses F5 and F6. If thermal switch S5 is open, the blower will operate but green lamp DC3-DC4 will be extinguished. When the green lamp lights, the temperature is at a level that permits S5 to close, and 115 volts is applied to the power supply start circuits. The blower operates whenever 115 volts is applied to the power supply and is not controlled by the START and STOP switches.

5-26. MARGIN SWITCHES. Margin switches S1 and S2 are provided to test the operation of the memory system under marginal d-c voltages. S1 increases or decreases the -24, -12, -6, and -3 volt potentials by 5%. S2 increases or decreases the +24, +6 and +3.5 volts by 5%. The switches are so oriented that the voltage is increased 5% when they are raised above the neutral position, and decreased 5% when they are depressed below the neutral position. Use of margin switches may produce transients which de-energize K1 and disable the power supply. Operation may be resumed by depressing S3. If the trouble persists, adjust the voltage sense circuits (see paragraph 5-33).

CAUTION

The margin switches should be in a neutral position during normal operation.

5-27. D-C VOLTAGES. A failure resulting from a 15 percent deviation in any output except the +3.5 volts and -16 volts (X-Y drive current supply), de-energizes K1 and extinguishes DS1-DS2 only. Efforts to close start control switch S3 are limited to one effective attempt per five-second interval by an automatic RC timing circuit. Failures that cannot be corrected by replacing open fuses may be approached by disconnecting the supply voltages from their respective loads at terminal strip TS1 to eliminate the memory circuits as the possible source of malfunction.

NOTE

When the power supply is disconnected from the RB Memory, the +3.5 volts will deviate from its nominal potential. All other voltages should remain constant.

5-28. When the power supply is inoperative because the voltage sense circuits have removed 115 volts from the power transformer primary, the failing voltage can frequently be identified by voltmeter checks at the TS1 terminal strip. Pushing the START

button will enable the power supply for about one second, long enough for the output potentials to rise and reach their prescribed values before the sense circuits again remove primary power.

5-29. Any deviation in the +6 or +24 volt outputs will directly affect all of the negative outputs. A deviation in any of the negative outputs will not directly affect the positive outputs. An approximately 15 percent change in any supply except the -16 volts (X-Y drive current supply) and +3.5 volts will remove 115 a-c from the power transformer primary. Voltage checks should narrow the failure area to either the positive or negative supplies. If all voltages rise to their correct levels, the voltage sense circuits become suspect. D-C resistance measurements with the 115 volts disconnected should be employed after the voltmeter checks have indicated a discrepant rectifier or regulating circuit.

5-30. If the process described in paragraph 5-28 does not locate the problem area, the assembly panels should be removed. A very thorough visual inspection should check for charred resistors, loose wires, and leaking capacitors. D-C resistance measurements made on suspect filter capacitors, rectifier diodes, or transistors can be compared against measurements made on similar components to establish out-of-tolerance readings.

5-31. When all alternate techniques fail to establish the area of failure, pins 4 and 5 on start control relay K2 can be jumpered to hold 115 volts on the power transformer primary. The voltage sense circuits are now bypassed and voltmeter checks can be made on the rectifying and regulating circuits.

CAUTION

Always disconnect the power supply from the RB system before bypassing the voltage sense circuits. Bypassing the sense circuits can result in serious damage to the supply. Be alert for any indication of overheated components.

5-32. VOLTAGE CONTROLS. (Figure 5-1.) R57 and R16 are factory-adjusted, and should not be disturbed unless a calibrated voltmeter measurement indicates a new setting is required. R57 is adjusted for a +24 volt output at terminal strip TS1-10. R16 is set for an X or Y drive voltage at 16.6 volts at TS1-2 with an operating temperature of 77° F (25° C)

5-33. R30 controls the sensitivity of the voltage sense circuits and should be adjusted only when component replacement or conclusive operating checks indicate this requirement. To adjust R30, perform steps a through d.

(a) Use R57 to raise the -24 volt output to between -26 and -27 volts. Adjust R30 so that the power supply disconnects. The disconnect voltage should be as high as possible within the specified limits.

(b) Check the disconnect range by noting that the power supply also disconnects at -21 $\pm$0.5 volts.

(c) Tighten the lock nut on R30. Use R57 to check that the disconnect range has not shifted due to the locking of R30.

(d) Adjust R57 to provide +24 volts at terminal strip TS1-10.

5-34. A sensistor mounted inside the power supply and located directly beneath the Magnetics Module provides temperature compensation for the X and Y drive voltages. Figure 5-2, Operating Temperatures vs. X and Y Drive Voltages, shows the variations in drive voltage that attend changes in operating temperature. The blower normally maintains the system very close to ambient room temperature.

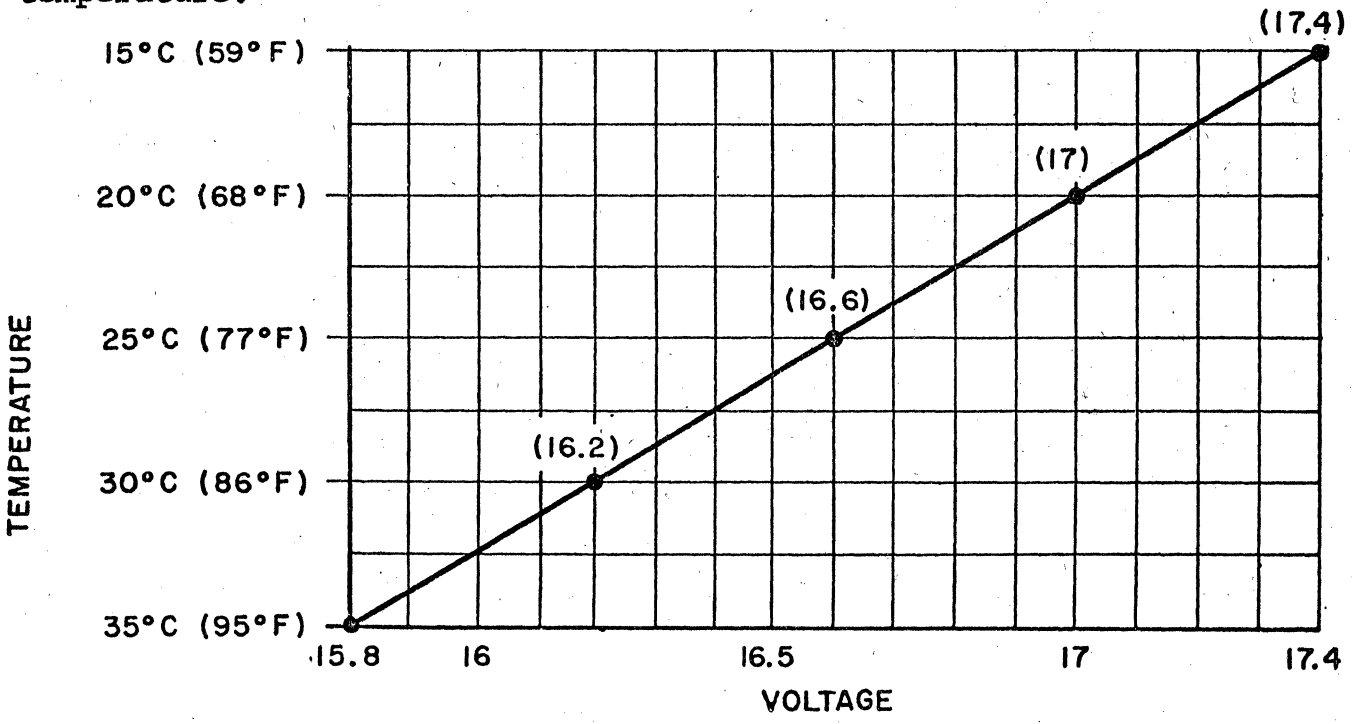


Figure 5-2. Operating Temperature vs X and Y Drive Voltages

5-35. MEMORY TROUBLE-SHOOTING.

5-36. GENERAL. The memory trouble-shooting information in this portion of the manual includes Address Gating in paragraph 5-37, the Waveform Checks in Table 5-4, and Magnetics Module checks in paragraph 5-43. Trouble-shooting information in the subsequent paragraphs does not include further reminders to check power supply voltages and establish the system's mechanical integrity. Preliminary Techniques, paragraph 5-17, should always be performed prior to a more detailed approach to the system failure.

5-37. ADDRESS GATING AT SWITCH INPUTS. The two X and two Y drive line switches selected for each address can be identified from Drawing 12310, sheet 2. An examination of the AR contents at a failing address will indicate which register outputs carry high levels. Tracing the register outputs to their switch inputs will indicate which circuits will be selected for a specific address. Every address level at the gate input to a selected switch only is low. The gate inputs to all non-selected switches include at least one high level.

5-38. For address 1, only Address Register flip-flop AR-0 is in its set (ONE) state. The reset (ZERO) side output at A7-E is low. The Y switch associated with line BY3 receives this level, plus a low input from $\overline{LC}$ and a low input from the ONE side of flip-flop AR-1 at A7-S (AR-1 is at ZERO). A drive timing pulse will pass set current through this switch and its output circuit by removing a ground from the drive current supply output line. The set and reset drive lines, and steering diodes associated with each switch can be identified by tracing the switch output to a matrix module schematic. This is described in the text following paragraph 5-49, X AND Y DRIVE LINES.

5-39. Before starting the waveform checks in Table 5-4, all RB control, address and information input signals should be checked. Paragraphs 1-42 through 1-57 describe these inputs.

5-40. WAVEFORMS. Table 5-4, Waveforms, shows the waveforms present at selected check points, describes the circuit under test, and indicates the probable remedy for a non-conforming pattern. Each check (step) includes a printed card and pin number reference that enables the circuit under test to be located on the logic diagrams in Section VI.

5-41. All of the waveforms are grouped and identified with the specific operating mode to which they apply. Each step is shown with a load or unload sync pulse that establishes an accurate timing reference.

5-42. When using Table 5-1, both the GENERAL NOTE and the specific NOTE that applies to the operating mode under test should be read. An analysis of the failure symptoms will usually indicate which of the four operating modes should be checked first. The sequence in which the waveforms (STEPS) for each mode are presented is not significant.

CAUTION

Use extreme care when applying test probes to the card connector terminals. Momentarily shorted terminals can result in damage to the equipment.

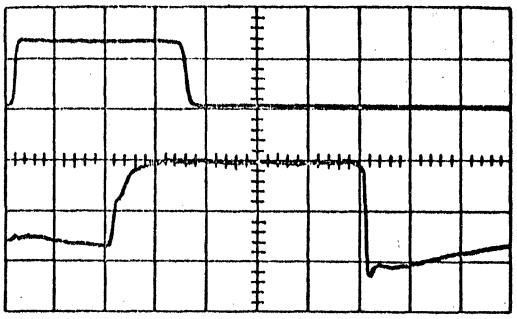
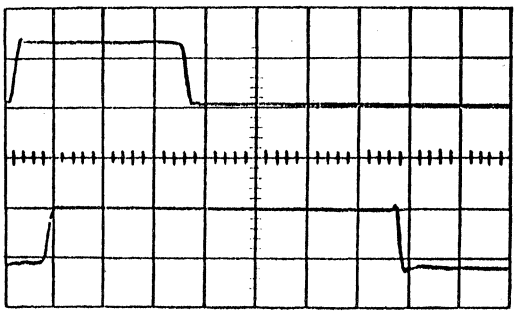
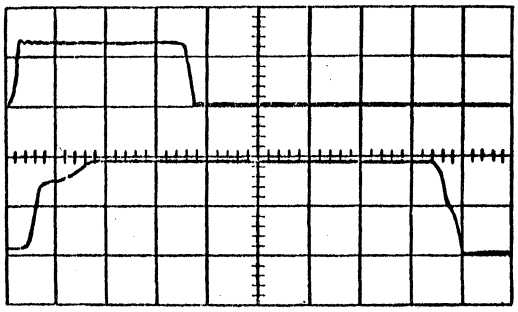
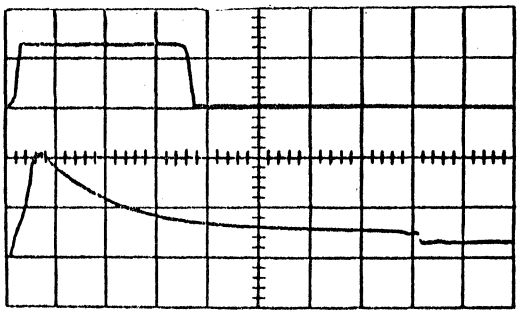
TABLE 5-4. WAVEFORMS

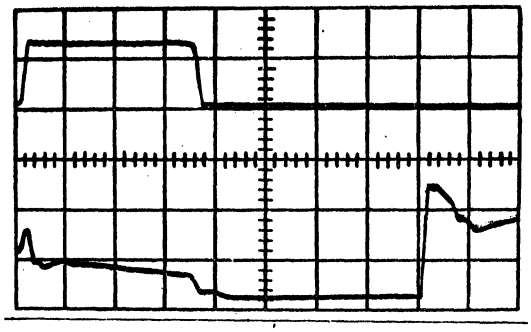
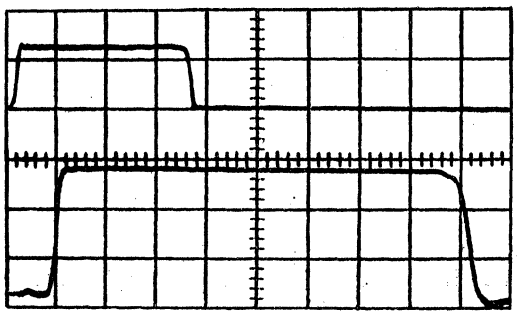
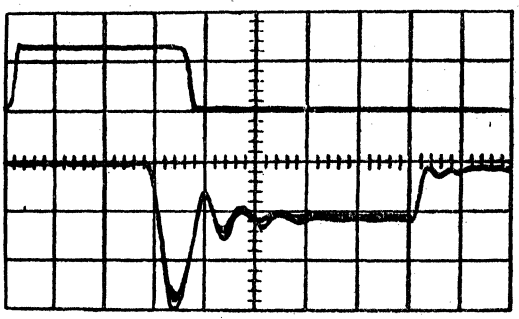
NOTE 1

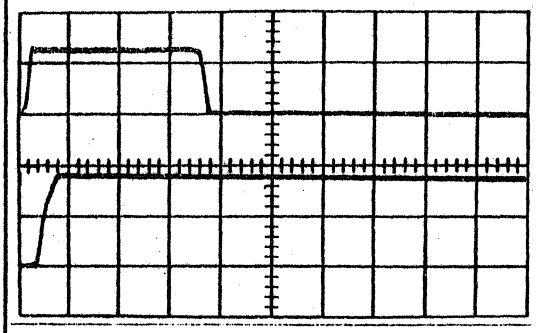
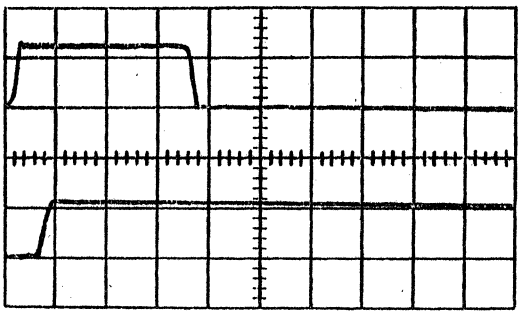
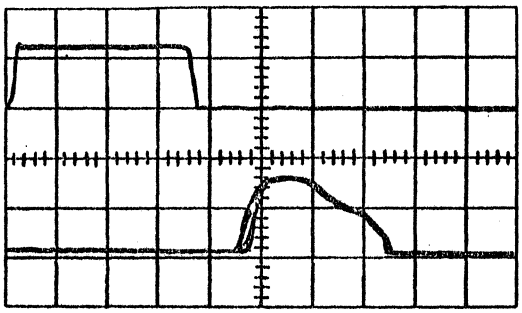
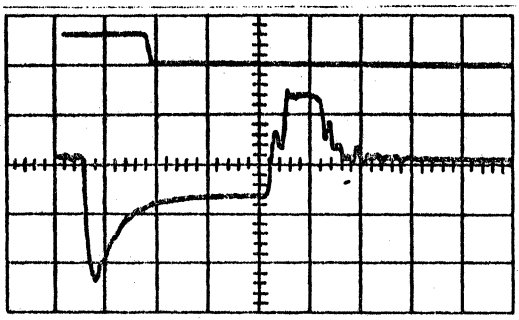
NOTE 1 is applicable to every Step in this table. The voltage levels from which the waveforms rise or fall is, in some cases, established by the input signal swings. These waveforms are arbitrarily shown with the levels introduced by zero to -6 volt input swings. They are identified by an asterisk. Every address, beginning with address zero, is loaded and unloaded in consecutive sequence.

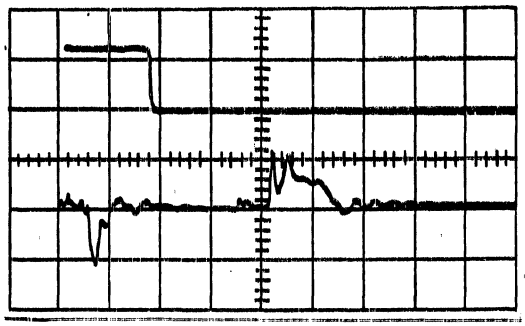
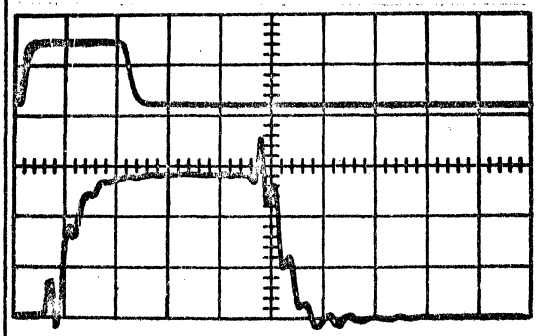
NOTE 2

NOTE 2 is applicable to Steps 1 through 15. The memory input consists of a disabled M0 level (buffer operation) with alternate load and unload sync pulses. The top waveform in each Step is a load sync at A4-21 (card-cage A, position 4, pin 21) which is used as the oscilloscope sync. All waveforms except 13, 14 and 15 are shown on a 0.5 us/CM time base. All sync waveforms except 12 are measured at 5 v/cm. Use care to avoid shorting card connector terminals when applying test probes.

STEP	DESCRIPTION	WAVEFORM	REMEDY
1.	Drive timing at A6-Y, 2 v/cm. The voltage rises to a +3.5 volt level.		Check timing card, M0 level at A6-18. M0 should be disabled.
2.	LC at A5-1, 5 v/cm. The voltage is shown rising from a -6 volt level.		Check Set LC and Reset LC (steps 4 and 5). Check register card A5.
3.	LC at A5-6, 5 v/cm. The voltage rises from a -6 volt level.		Same as step 2.
4.	Set LC at A6-20, 5 v/cm. The voltage rises from a +3 volt level.		Check inputs to timing card (M0 at A6-18 should be disabled). Check Step 3. Check timing card.

STEP	DESCRIPTION	WAVEFORM	REMEDY
5.	Reset LC at A6-16, 1 V/cm. The voltage is shown rising from a +5 volt level.		Check: Step 4, LC at A6-15, and timing card. LC should be high.
6.	Inhibit timing at A3-C (also A4-C for models with more than 12 bits per word), 2 v/cm. The voltage rises from a zero volt level.		Check $\overline{LC}$ at A3-5 (Should be the inverse of waveform shown in Step 3). Check input Cards A3 and A4.
7.	X drive voltage at A3-W, 2 v/cm.		Check: Step 1, input card A3.
8.	Y drive voltage at A4-W, 2 v/cm	Same as Step 7.	Check: Step 1, input card A4.

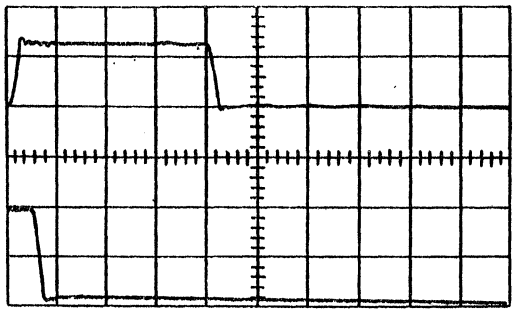
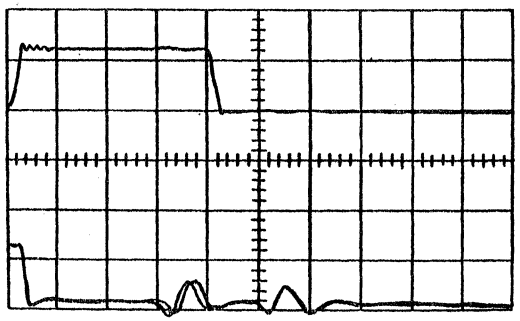
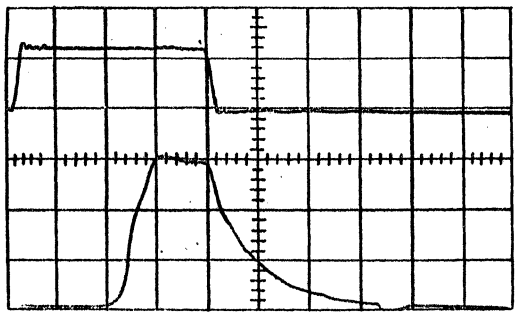
STEP	DESCRIPTION	WAVEFORM	REMEDY
9.	L (L/U level) at A5-S, 5 v/cm. The voltage rises from a -6 volt level.		Check register card A5.
10.	L at A5-22, 5 v/cm. The voltage is shown rising from a -6 volt level.*		Check register card A5.
11.	Read Amplifier output at B14-E while writing ONEs, 2 v/cm. The voltage rises from zero volts. The pulse results from core turnover while writing ONEs. Strobe RA is not present and the amplifier output does not set its MR flip-flop.		Check steps 7, 8 and 12. Check input to read amplifier during load cycle-should be same as waveform 24 except top trace will be LS at A4-21. Check read amplifier card.
12.	The load sync is measured at 10 v/cm, 1.0 us/cm. Inhibit drive line voltage at B8-1 while writing ZEROs, 2 v/cm, 1/0 us/cm.		Check step 6. Check input to inhibit driver from corresponding bit of the address register (Should be at +3.5V level during load cycle. Check inhibit card.

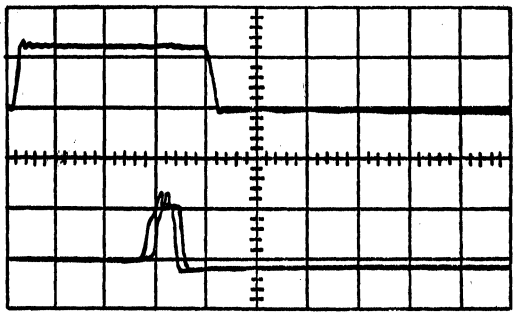
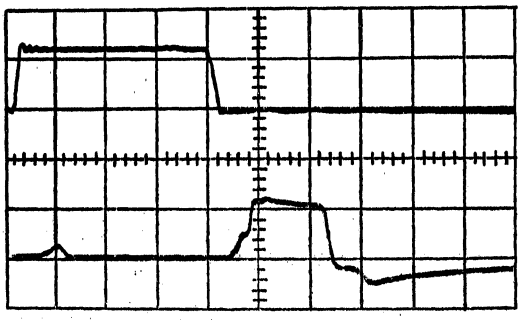
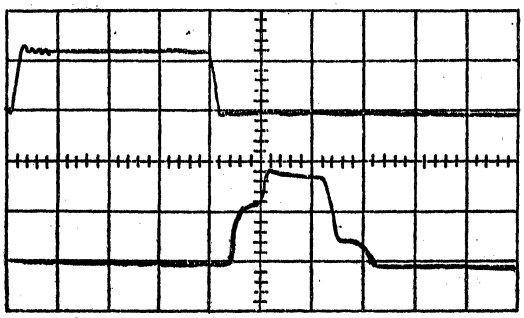
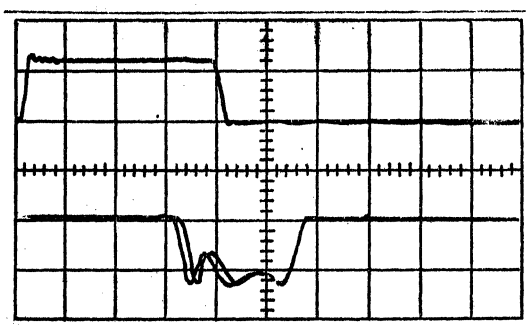
STEP	DESCRIPTION	WAVEFORM	REMEDY
13.	The load sync is shown on a 1.0 us/cm time base. Selected X switch output at A17-S during buffer load cycle, .05 v/cm.		Check Steps 1, 7, switch card A17, gate inputs to A17.
14.	The load sync is shown on a 1.0 us/cm time base. Selected Y switch output at A16-S during buffer load cycle, .05 v/cm.	Same as Step 13.	Check Steps 1, 7, switch card A16, gate inputs to A16.
15.	The load sync is shown on a 1.0 us/cm time base. A differential amplifier is required for this check. Inhibit current in inhibit line zero when loading a zero, 50 ma/cm. (This waveform was taken by observing the voltage across a 1 ohm resistor in series with the inhibit line connected to B8-1).		Check Step 12. Check other planes.

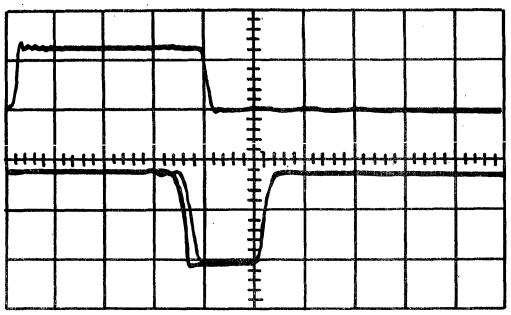
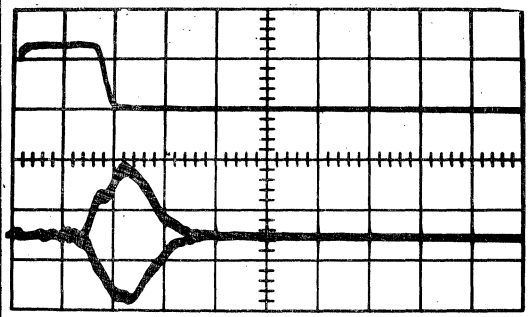
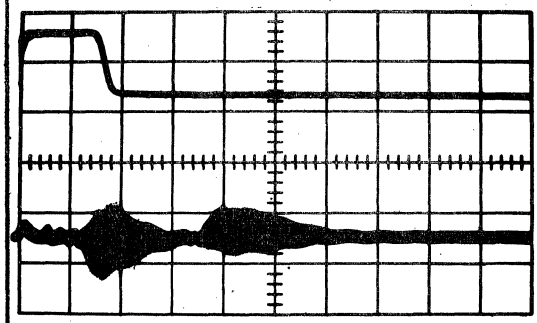
NOTE 3

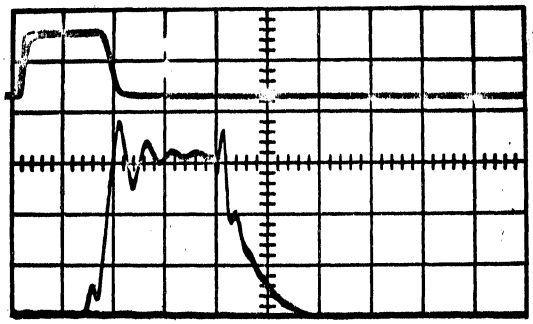
NOTE 3 is applicable to Steps 16 through 26. The top waveform is an unload sync pulse at A4-X which is used as the oscilloscope sync. All waveforms except 24, 25, 26 are shown on a 0.5 us/cm time

base. Alternate load and unload sync pulses are applied with the M0 line disabled. Refer to NOTE 1. Use care to avoid shorting card connector terminals when applying test probes.

STEP	DESCRIPTION	WAVEFORM	REMEDY
16.	L (L/U level) at A5-S, 5 v/cm. The voltage falls from a +3.5 volt level.		Check Step 17, set and reset inputs to card A5, LU register card A5.
17.	L at A5-22, 5 v/cm. The voltage is shown falling from a 0 volt level. *		Check Step 16, set and reset inputs to card A5, LU register card A5.
18.	MR clear at A6-1, 2 v/cm. The voltage rises from approximately +1 volt level.		Check Load gating (L) at A6-Z, LC gating at A6-15, timing card. L and LC levels should be at -6 volts.

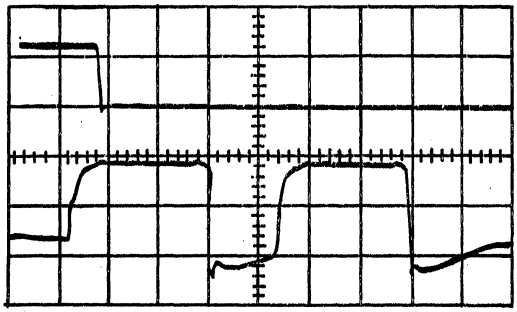
STEP	DESCRIPTION	WAVEFORM	REMEDY
19.	MR clear at A3-20, 5 v/cm. The voltage is shown rising from a +3.5 volt level.		Check Step 18, input card A3.
20.	Strobe RA at A6-U, 5 v/cm. The strobe rises from a +3.5 volt level.		Check timing card, Step 16, LC gating at A6-15.
21.	Read amplifier output at B14-E while unloading a ONE, 5 v/cm. The signal rises from a zero volt level.		Check Step 11 to determine that a ONE is loaded, check Steps 2, 7, and 8.
22.	Memory Register output at B6-1 while unloading a ONE, 5 v/cm. The voltage is shown dropping from a zero volt level.*		Check Step 21, MR card B6.

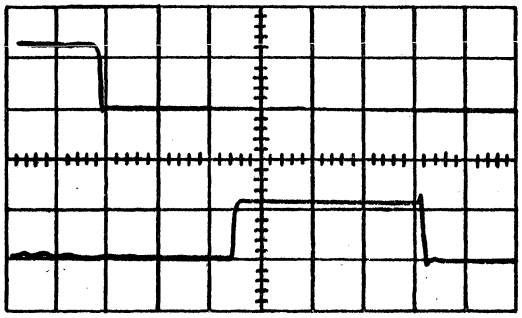
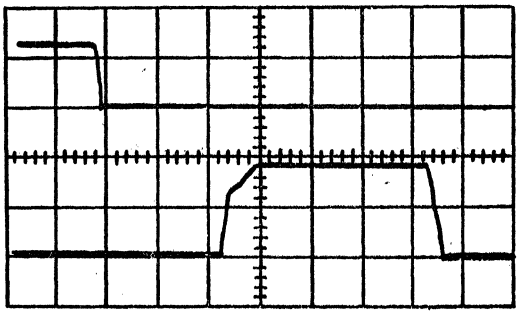
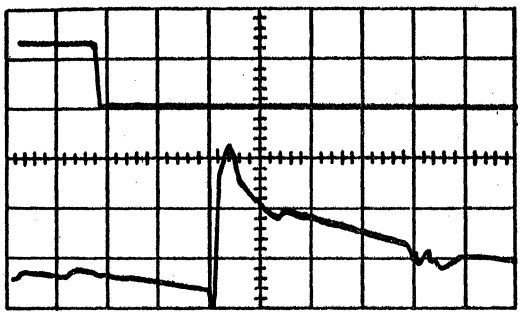
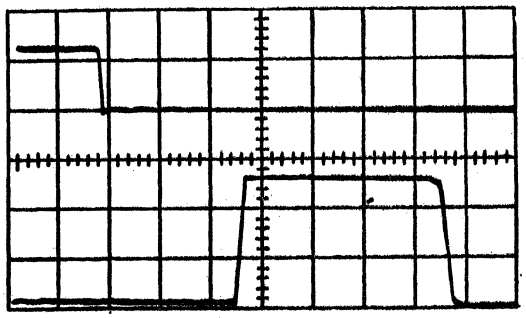
STEP	DESCRIPTION	WAVEFORM	REMEDY
23.	Memory Register output at B6-6 while unloading a ONE, 5 v/cm.		Check Step 17 MR card B6.
24.	Read amplifier input at B14-1 and 2 while reading ONEs, 20 mv/cm. Note both positive and negative turn-over signals. The unload sync is shown on a 1.0 us/cm time base.		If failure occurs in more than one plane; check switch drivers, inhibit timing, X-Y drive voltages (-16.6).
25.	Read amplifier input at B14-1 and 2 while reading ZEROs, 1.0 mv/cm. The unload sync is shown on a 1/0 us/cm time base.		If failure occurs on one plane only; check applicable MR and inhibit driver outputs, check matrix plane. If a ONE signal appears, establish that a ZERO is loaded. If excessive noise, check external sources, note if noise is confined to specific planes or addresses, check matrix.

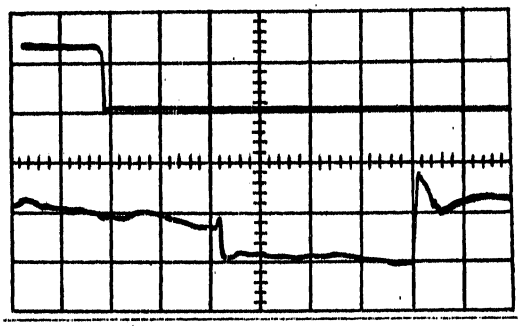
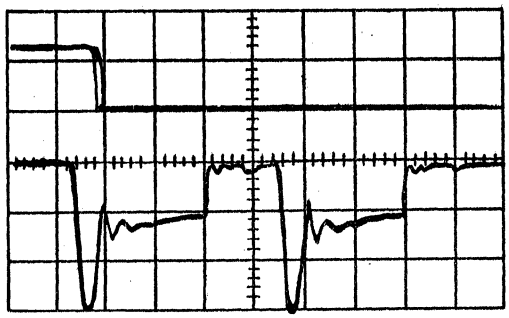
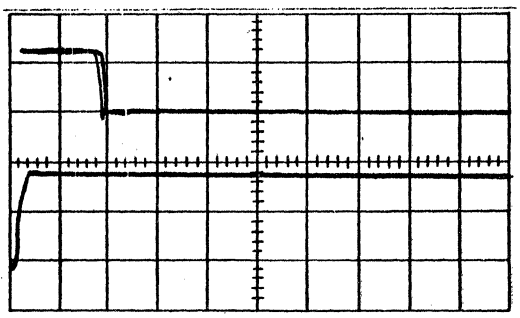
STEP	DESCRIPTION	WAVEFORM	REMEDY
26.	The unload sync is shown on a 1.0 us/cm time base. X drive current, 50 ma/cm. (This waveform was taken by observing the voltage across a 1 ohm resistor in series with the drive line connected to A17-S.) A differential amplifier is required for this check.		Check card A17, Step 7.

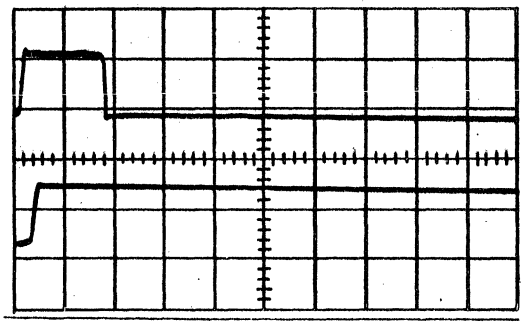
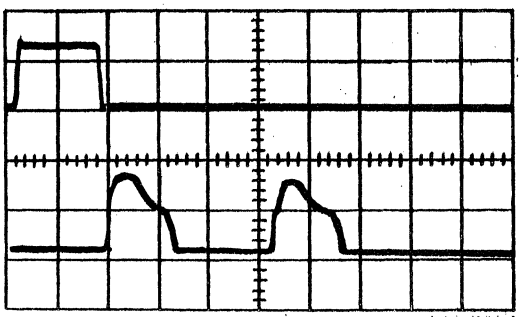
NOTE 4

NOTE 4 is applicable to Steps 27 through 37. The top waveform is a load sync pulse at A4-21 which is used as the oscilloscope sync. All waveforms are shown on a 1.0 us/cm time base. Alternate load and unload sync pulses are applied with the M0 line enabled. Refer to NOTE 1. Use care to avoid shorting card connector terminals when applying test probes.

27.	Drive timing at A6-Y, 2 v/cm. The voltage rises to a +3.5 volt level.		Check timing card, M0 level at A6-18. M0 should be enabled.

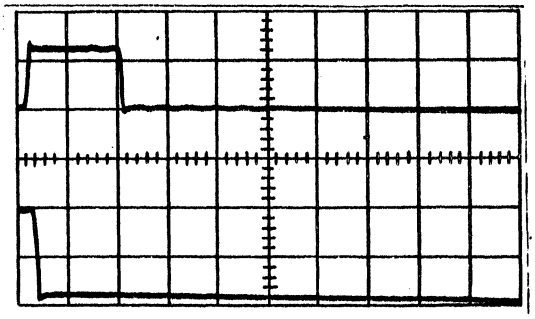
STEP	DESCRIPTION	WAVEFORM	REMEDY
28.	LC at A5-1, 5 v/cm. The voltage is shown rising from a -6 volt level.*		Check Step 29, LC register card, M0 level at A6-18, timing card. M0 should be enabled.
29.	LC at A5-6, 5 v/cm. The voltage rises from a -6 volt level.		Check Step 28, LC register card, M0 level at A6-18, timing card. M0 should be enabled.
30.	Set LC at A6-20, 1 v/cm. The voltage rises from a +5 volt level.		Check $\overline{LC}$ level at A6-19, M0 at A6-18, timing card. M0 and $\overline{LC}$ should be high.
31.	Inhibit timing at A3-C (also A4-C for models with more than 12 bits per word), 2 v/cm. The voltage rises from a zero volt level.		Check input card A3 (A4). Check $\overline{LC}$ at A5-E, timing card.

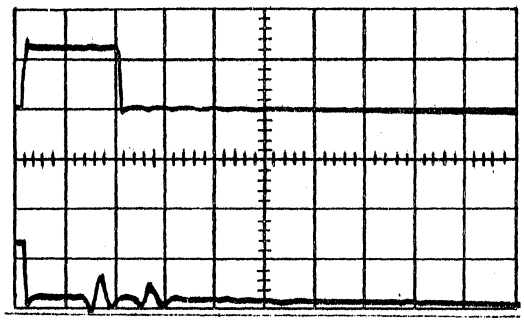
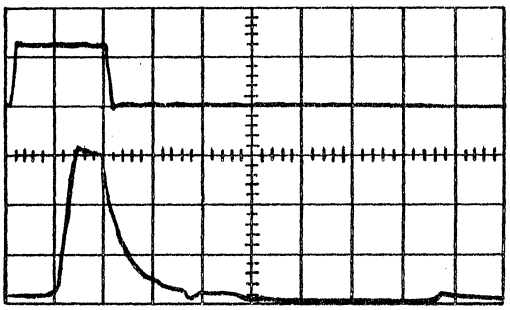
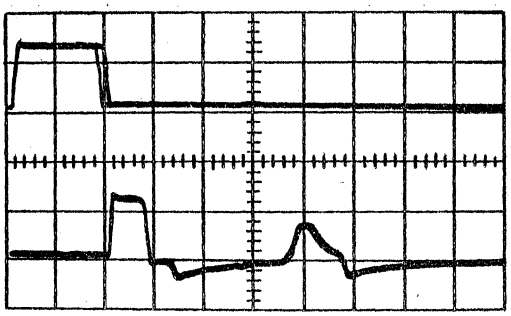
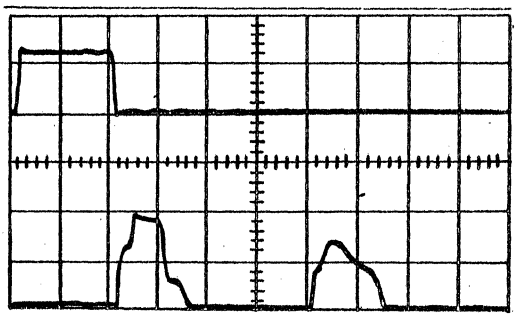
STEP	DESCRIPTION	WAVEFORM	REMEDY
32.	Reset LC at A6-16, 1 v/cm. The voltage is shown rising from a +5 volt level. *		Check Step 30, LC at A6-15, timing card. LC should be high.
33.	X drive voltage at A3-W, 2 v/cm.		Check Step 27, input card A3.
34.	Y drive voltage at A4-W, 2 v/cm.	Same as Step 33.	Check Step 27, input card A4.
35.	L (L/U level) at A5-S, 5 v/cm. The voltage rises from a -6 volt level.		Check Step 34, set and reset inputs to card A5, L/U register card A5.

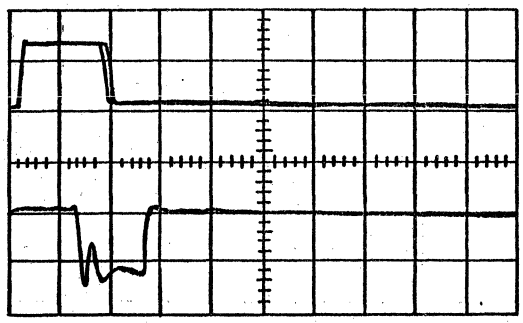
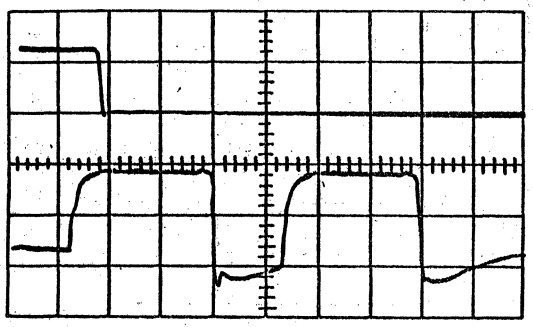
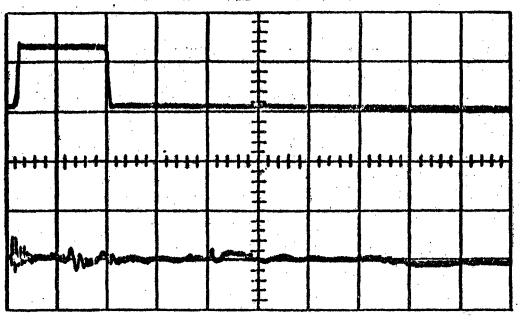
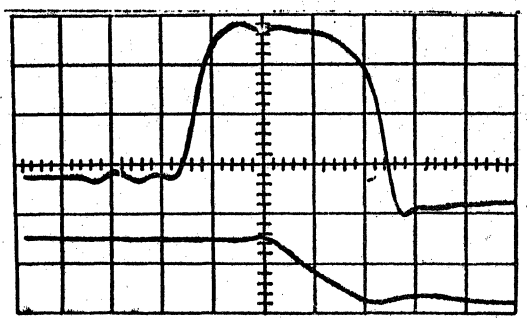
STEP	DESCRIPTION	WAVEFORM	REMEDY
36.	L at A5-22, 5 v/cm. The voltage is shown rising from a -6 volt level.*		Check Step 35, set and reset inputs to card A5, L/U register card A5.
37.	Read amplifier output at B14-E while writing ONEs, 5 v/cm. The voltage rises from zero volts.		Check Steps 27 through 36, Check card B14. Note if failure occurs in other planes.

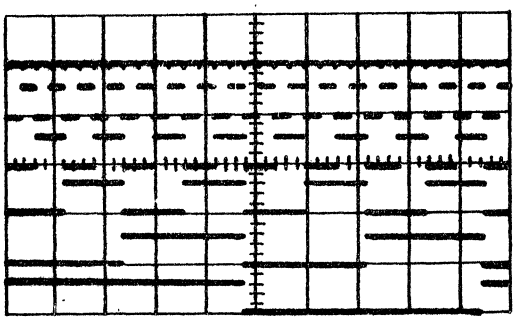
NOTE 5

NOTE 5 is applicable to Steps 38 through 45. The top waveform is an unload sync pulse at A4-X which is used as the oscilloscope sync. All waveforms are shown on a 1.0 us/cm time base. Alternate load and unload sync pulses are applied with the MO line enabled. Refer to NOTE 1. Use care to avoid shorting card connector terminals when applying test probes.

38.	L at A5-S, 5 v/cm. The voltage falls from a +3.5 volt level.		Check Step 39, set and reset inputs to card A5, L/U register card A5.

STEP	DESCRIPTION	WAVEFORM	REMEDY
39.	L at A5-22, 5 v/cm. The voltage is shown falling from a zero volt level.*		Check Step 38, set and reset inputs to card A5, L/U register card A5.
40.	MR clear at A6-1, 2 v/cm. The voltage rises from a +1 volt level.		Check Load (L) gating at A6-Z LC gating at A6-15, timing card, L and LC levels should be -6 volts.
41.	Strobe RA at A6-U, 5 v/cm. The strobe rises from a +3.5 volt level.		Check Step 38, LC gating at A6-15, timing card. L gating at A6-Z. L and LC should be -6 volts.
42.	Read amplifier output while reading and restoring ONEs at B14-E, 5 v/cm. The voltage rises from a zero volt level.		Check Step 11 to determine that a ONE is loaded, check Step 41, read amplifier card B14, Check if other planes are failing.

STEP	DESCRIPTION	WAVEFORM	REMEDY
43.	MR-0 at B6-1 while reading ONEs, 5 v/cm. The voltage falls from a zero volt level.		Check Steps 42, 40, MR card B6.
44.	Strobe RA at A6-U, 5 v/cm. The strobe rises from a +3.5 volt level. Drive timing at A6-Y, 2 v/cm. The voltage rises to a +3.5 volt level.		Check Step 39, LC gating at A6-15, timing card. LC should be +3.5 volts. Check timing card, M0 level at A6-18. M0 should be enabled.
45.	Read amplifier output at B14-E while reading and restoring ZEROs, .05 v/cm. The level is at zero volts. Note low transient noise.		Check Step 25, read amplifier card B14. Note if failure occurs in other planes.
46a.	The top waveform is a count pulse at A2-A, 2 v/cm, 0.1 us/cm.		Check input pulse at A2-1, input card A2.

STEP	DESCRIPTION	WAVEFORM	REMEDY
46b.	The bottom waveform is the AR-0 at A7-1 5 v/cm, 0.1 us/cm. AR-0 is shown falling from a zero volt level.*	(See 46a)	Check for count pulse at A7-1 input. Check A7-1, count logic cards.
47.	The 1st (top) waveform shows count pulses at A2-A, the 2nd shows AR-0 at A7-1, the 3rd AR-1 at A7-22, the 4th AR-2 at A8-1, the 5th AR-3 at A8-22, the 6th AR-4 at A10-1. Vertical scale is 10 v/cm, horizontal scale is 100 us/cm.		Check count logic cards. If count pulses are not present, check Step 46a.

5-43. MAGNETICS MODULE CHECKS. Continuity through the Magnetics Module, in addition to signal path wiring through the entire RB system, can be checked by using the referenced schematic and logic diagrams. The X and Y drive lines with their associated steering diodes are shown on the Magnetics Module schematics. Inhibit and sense windings are indicated, but not shown, on sheet 1 of the logic diagram. Magnetics Module failures are very unusual. The Magnetics Module should be investigated only when all other possible failure areas have been checked. A study of the following paragraphs and the referenced illustrations can contribute to an understanding of circuit layout.

5-44. INHIBIT WINDINGS. (See Drawing 12310 and Figure 5-3.) Sheet 1 of drawing 12310, Logic Diagram, shows the common output from each pair of current switches on an inhibit driver card entering a matrix plane. Each output is connected to the single inhibit winding within that plane. Continuity can be measured between an inhibit card output terminal and the zero volt bus, or between the split-leaf connectors at the digit plane inputs. When facing the matrix from the assembly rear (end plate connector side), the inhibit winding inputs are located at the left hand column of split-leaf connectors.

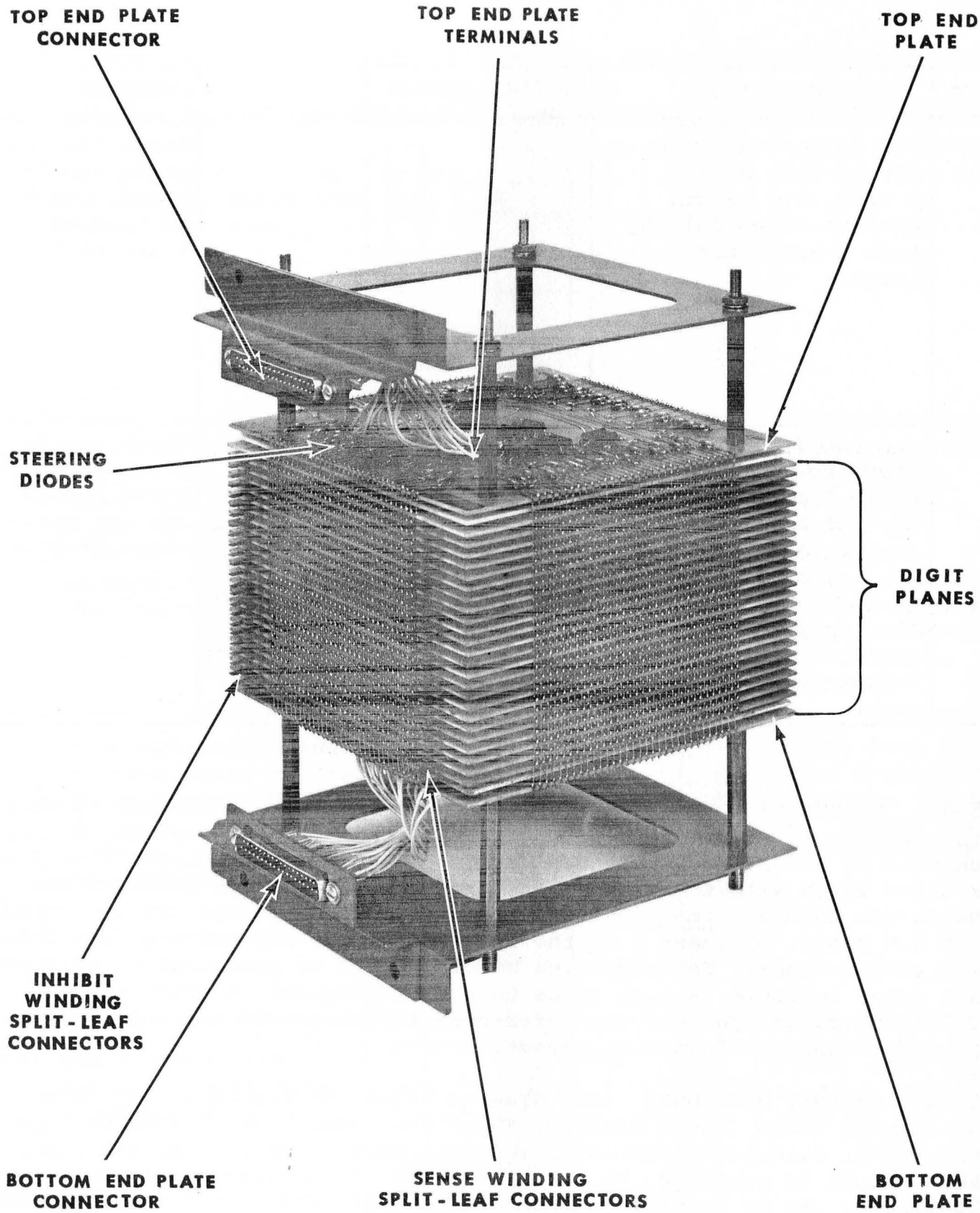


Figure 5-3. Magnetics Module

5-45. The d-c resistance per winding should be about ten ohms. Inhibit winding resistance may vary with different matrix (digit) planes. Each inhibit winding is an open circuit to all other windings.

5-46. A suspect digit or sense (paragraph 5-47) winding may be checked by substituting another digit plane for the suspect unit. Digit plane 0 can be substituted for plane 1 by:

a. removing the four split-leaf connectors at both the sense and digit winding inputs to plane 1.

b. removing the four split-leaf connectors at the sense and digit winding inputs to plane 0 and connecting them to plane 1 inputs.

c. connecting the four split-leaf connectors formerly attached to plane 1 to plane 0.

This test will conclusively establish a defective matrix plane.

CAUTION

Each inhibit winding input consists of a white lead that carries -12 volts, and a black lead for the common bus return. When substituting windings, observe the wire color coding to maintain the same input polarities at each connector pin.

5-47. SENSE WINDINGS. (See Figure 5-3 and Drawing 12310.) Sheet 1 of drawing 12310 shows a pair of leads connecting each matrix plane to a read amplifier. Each of the leads is connected to one end of the single sense winding within that matrix plane. Continuity can be measured between the printed card connector pins shown at the read amplifier input, or between the split-leaf connectors at the digit plane input. When facing the matrix from the assembly rear (end plate connector side), the sense winding inputs are located at the right hand column of split-leaf connectors.

5-48. Each sense winding is an open circuit to all other sense windings. The d-c resistance per winding should be about 12 ohms. Sense winding resistance may vary with different digit planes. Paragraph 5-46 describes the procedures necessary to check a suspect sense or inhibit winding by substituting another digit plane.

5-49. X AND Y DRIVE LINES. (See Drawings 12310, 11932, 11934 and Figures 5-4 and 5-5.) The X and Y drive line switches on sheet 2 of drawing 12310 are shown on two identical cards. Card A16 contains the sixteen switches that function with the Y set and reset drive lines, card A17 operates with the X lines. The circuit logic and trouble-shooting checks described for the Y lines and their associated steering diodes will also apply to the X circuits.

CAUTION

Handle the Magnetics Module with care. The matrices can be damaged by careless probing or sharp jolts.

5-50. Resistance checks on the steering diodes and X and Y drive lines require removing the Magnetics Module from its mounting in the memory assembly. Make a careful visual inspection for loose wires, charred components and solder bits. When conclusive tests indicate a defective module, return the unit to the manufacturer if a repair cannot be effected without disassembling the matrix stack.

5-51. The Y switches are segregated into two complementary banks (groups), AY0 through AY7, and BY0 through BY7. Four of the B switches are gated by LC and address lines, the remaining four are gated by $\overline{LC}$ and address lines. All A switches are gated by address lines only. Those switches enabled by LC control current flow into reset drive lines, those enabled by $\overline{LC}$ control current flow into the set drive lines. A single LC or $\overline{LC}$ switch in the B bank is selected (enabled) in conjunction with one of the eight A bank switches. The selected switches provide a current path from the X-Y drive current supply, through the set or reset lines, to the zero volt bus.

5-52. Address 1 selects the B switch associated with output BY3 at A16-D and the A switch associated with output AY0 at A16-16 when the $\overline{LC}$ line is low (load operation). Terminal A16-D is connected to P5-21 and enters the matrix module top end plate connector on pin 21. Output BY3 is connected to eight diodes, whose anode leads are each connected to drive lines Y1UE, 5UE, 9UE, 13UE, 17UE, 21UE, 25UE; and Y29UE. All lines discontinued on the top end plate schematic enter the first matrix plane to function as the co-ordinate X and Y drive lines. The X and Y drive lines pass through each of the series connected digit planes (not shown), and then enter the bottom end plate schematic. Reference designators provide cross-referencing between top and bottom end plate circuits.

5-53. At the bottom end plate schematic, the eight Y drive lines from BY3 leave the bottom end plate connector and are each connected to one of eight switches via connector P6. Since address 1 also selects the A switch associated with output AY0, a circuit through set (load) drive line Y1UE is completed. The remaining seven YUE drive lines from the BY3 output are each connected to one of the remaining seven A bank switches.

5-54. The end plate schematics depict the steering diodes that are inserted between the switches and matrix drive lines; they do not show the drive line circuits through the digit planes. Continuity between the top end plate connector pins and the top end plate terminals (see Figure 5-3) is illustrated on the top end plate schematic. Continuity between the bottom end plate connector pins and the bottom end plate terminals is indicated, but not shown on the bottom end plate schematic.

5-55. The inhibit winding and sense winding associated with each matrix plane do not appear on the end plate schematics.

5-56. Drive line continuity through the digit (matrix) planes can be measured from the printed terminals mounted on the periphery of the bottom end plate to the printed terminals mounted on the periphery of the top end plate. Figures 5-4 and 5-5 identify those drive lines connected directly to a printed terminal at the end plate periphery. Those drive lines containing a diode in series with their separate connections to this printed terminal can be identified by using the associated diodes as a cross reference to the applicable end plate schematic (diode CR1 on Figure 5-5 is shown connected to drive line Y1UE on the top end plate schematic). Magnetics Modules containing less than 1024 word address structure will contain fewer drive line connections and steering diodes than indicated on the end plate schematics and assembly instructions. They will otherwise be identical to the 1024 word structure shown on the illustration.

5-57. Drive line resistance through a single digit plane is approximately 0.3 ohm. Total resistance through the matrix will be determined by the total number of planes. Discrepant resistance measurements should always be evaluated against system performance.

5-58. Because many of the drive lines are connected together at either of the end plates, resistance measurements will generally not be effective in locating shorted lines. A shorted drive line circuit can usually be located within a comparatively narrow area

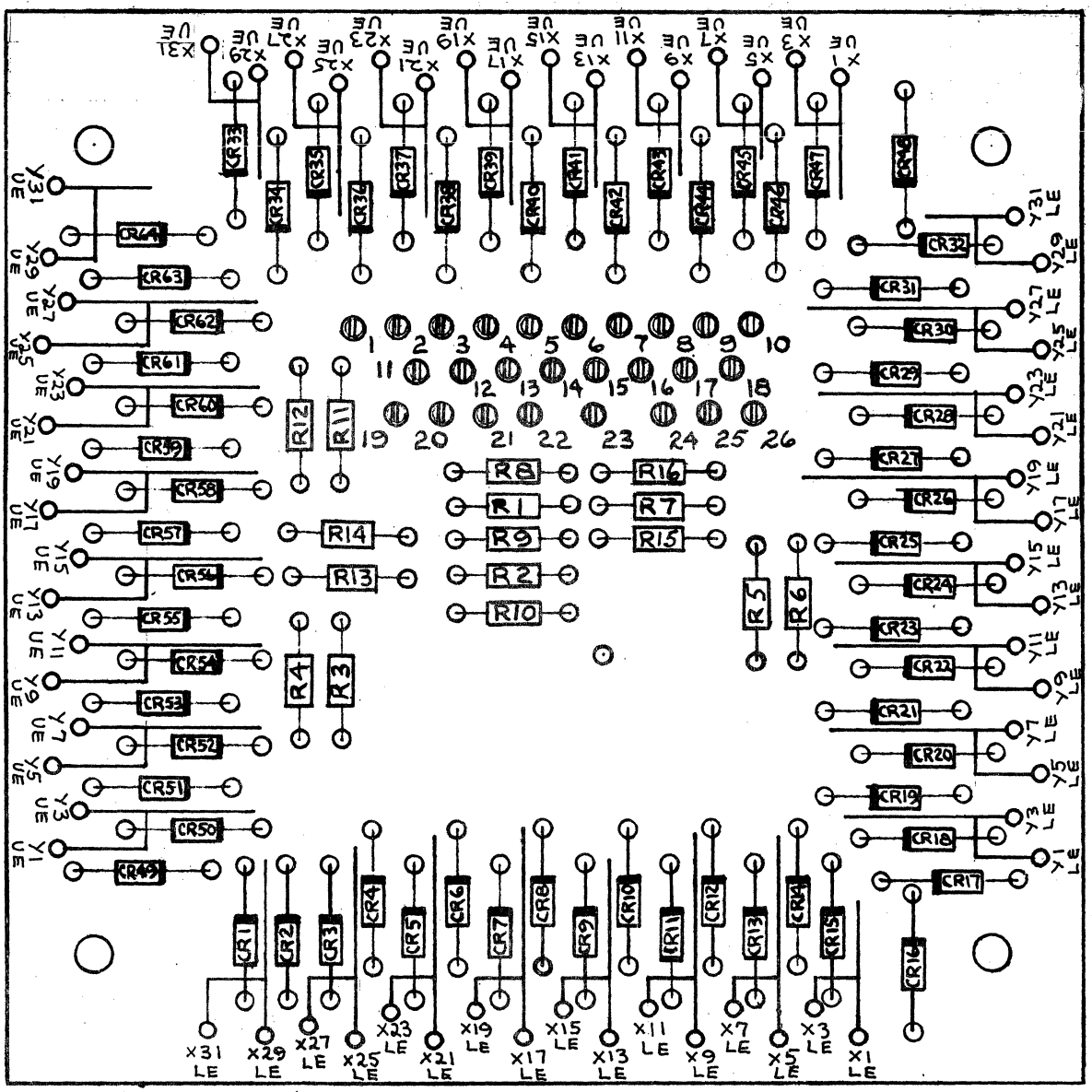


Figure 5-4. Bottom End Plate, Matrix Module, Assembly 11935

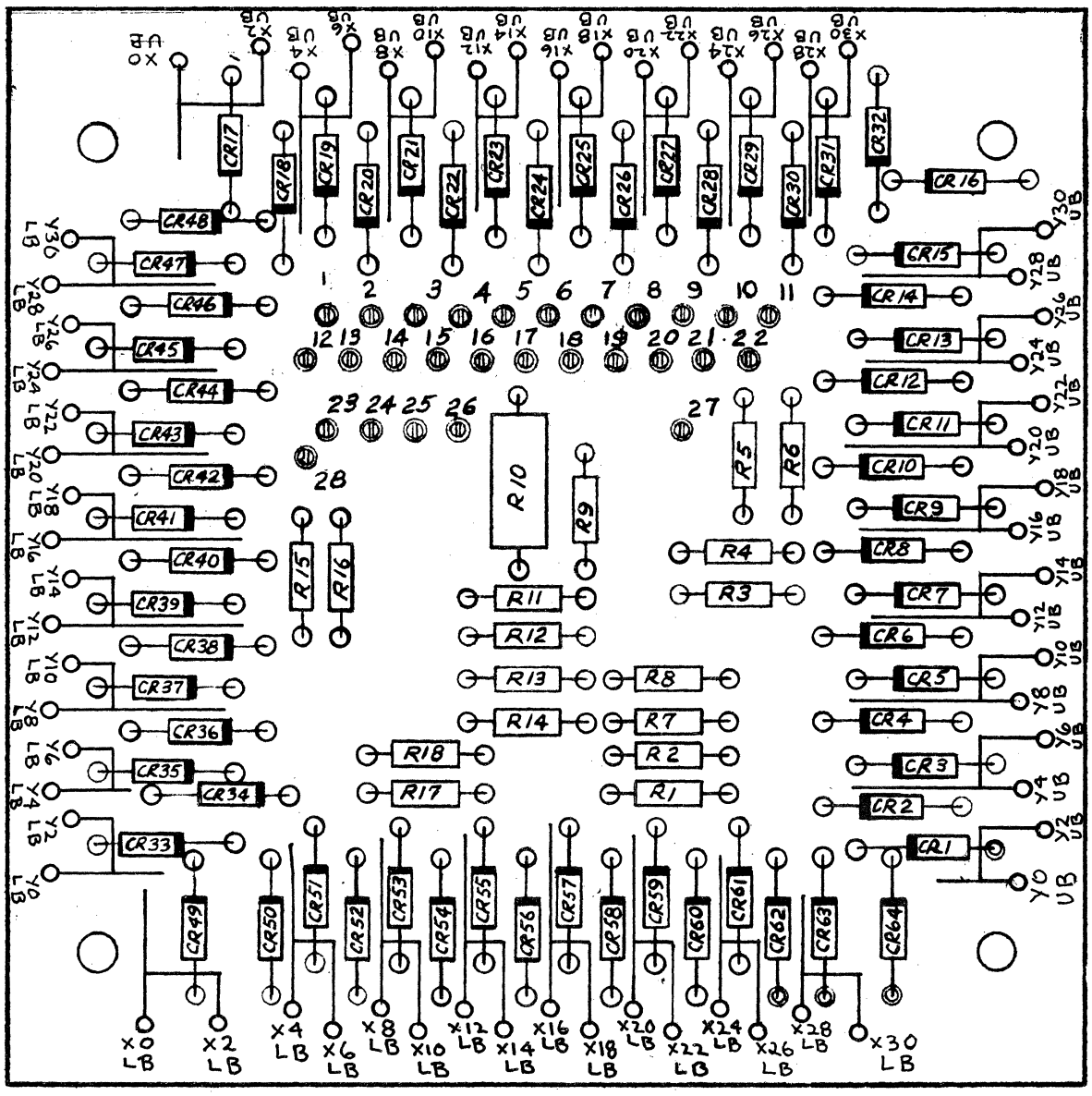


Figure 5-5. Top End Plate, Matrix Module, Assembly 11933

by determining which drive line switches are selected by the failing address (addresses). Resistance measurements between those lines connected together at their top end plate can be taken from their bottom end plate. Measurements between those lines connected together at their bottom end plate can be taken from their top end plate. The d-c resistance between any two lines joined at their opposite end plates should be about 0.6 ohms per matrix plane. D-C resistance between those lines not connected together should be at least 2200 ohms.

5-59. Suspect steering diodes can be checked without being disconnected from their circuits. Unless the diode is open, an ohmmeter check is usually not conclusive: a diode tester should be used. Step 8 in Table 5-4 illustrates a waveform check that can indicate a defective steering diode in the Y circuits. If the diode is open or presents a high forward resistance, the waveform in Step 8 will show a marked increase in amplitude. A defective drive line switch, or an open drive line can also present this symptom. Step 7 illustrates a similar waveform check for the X circuits.

SECTION VI
DRAWINGS

6-1. INTRODUCTION.

6-2. This section contains logic and schematic drawings, and assembly illustrations pertinent to the RB General Purpose Memory and its components. A complete listing of all drawings in Section VI is given in the List of Illustrations at the front of this manual.

6-3. PRINTED CIRCUIT CARD DRAWINGS. Each printed circuit card is depicted by a schematic drawing and an assembly illustration. The assembly illustration provides component location information for its associated schematic. Every schematic contains a NOTES column that includes component information and a cross-reference to its assembly illustration. Signal leads entering or leaving a printed circuit schematic can be traced by referring to the logic diagrams. The card is shown as a dotted line enclosure and is identified by its card cage position.

6-4. LOGIC DIAGRAMS.

6-5. GENERAL. Drawings 12310, sheets 1 and 2, and N12491, sheets 1 and 2 are logic diagrams of the RB memory system that depict printed circuit cards as dotted line enclosures. Circuitry mounted on the card is illustrated by logic symbols. A dotted line enclosure that does not contain logic symbols is an identical replica of a card shown elsewhere on the drawings. Each enclosure includes a reference to the printed card cage position. Figure 1-2, Card Cage Configuration, identifies the card at each cage position. Drawing N12491 should be used for serial numbers 1337 and 1339 through 1345, Drawing 12310 for all other serial numbers.

6-6. CIRCUIT CONFIGURATION. Both logic diagrams show the circuit configuration for a 12-bit word. System configurations compatible with words of greater bit length (16, 20 and 24 bits), require an additional connector, J4, and a larger number of cards and matrix planes. The cards and matrix planes illustrated for bits 1 through also apply to bits 13 through 24. Those circuits required to increase the system bit-per-word capacity above 12 bits are indicated by an alternate card-cage position reference within the dotted enclosure. Figure 1-2 defines the specific card associated with each matrix plane.

6-7. The logic diagrams illustrate continuity through the matrix planes (sense and inhibit windings only) and signal paths through the entire RB system. D-C operating voltages appearing on the printed card connectors are not shown. They are identified on the circuit schematics. The logic symbols used in this diagram indicate logic functions only; they do not indicate circuitry.

6-8. REFERENCING. Signal leads discontinued on sheet 1 and continued on sheet 2 are cross-referenced by a card and pin number designator. Discontinued leads are always continued on the adjacent sheet of the logic diagram.

6-9. Leads entering or leaving on the J1, J3, and J4 input-output connectors can be traced to the external equipment via the mating connector and pin number. Leads entering or leaving on the P5 and P6 connectors are respectively connected to the top and bottom end plates of the Magnetics Module. The pin numbers can be found on the applicable matrix schematic where the mating connector is identified.

6-10. SYMBOLS. Figure 6-1, Logic Symbols, identifies the symbols used in the logic diagrams. Their functions are briefly defined in the following descriptions. The RB memory uses positive true logic exclusively and all symbols are appropriately referenced to high inputs and outputs. In the following descriptions, the terms "high" and "low" are used when defining circuit inputs and outputs. A "high" is construed as the more positive of two possible voltages. A "low" is construed as the less positive of two possible voltages. Each symbol indicates a specific function; it is not intended to convey specific circuitry.

6-11. AND GATE. This circuit produces a high output only when all inputs are high. Any low input results in a low output.

6-12. OR GATE. A high applied to any input of this gate produces a high output. Its output is low only when all inputs are low.

6-13. INVERTING AMPLIFIER. A high input to this circuit develops a low output;a low input develops a high output. The asterisk, when present, indicates the circuit may be used as either an inverting amplifier or a non-inverting amplifier. The printed circuit card containing the amplifier provides an input selector whose position determines whether the circuit will invert.

6-14. UNIVIBRATOR. This circuit (UNI) generates a sharp rising pulse of approximately one microsecond duration when triggered by

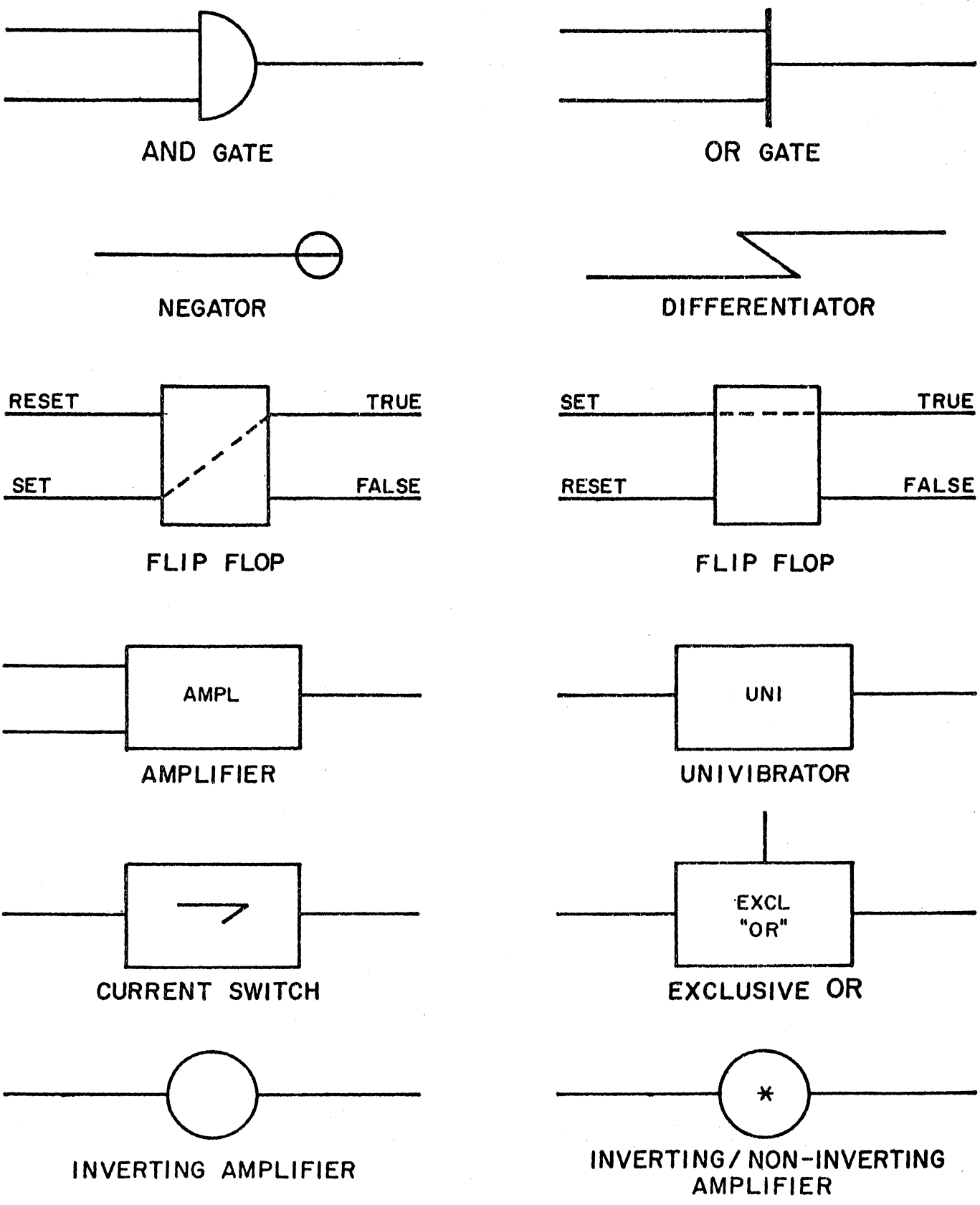
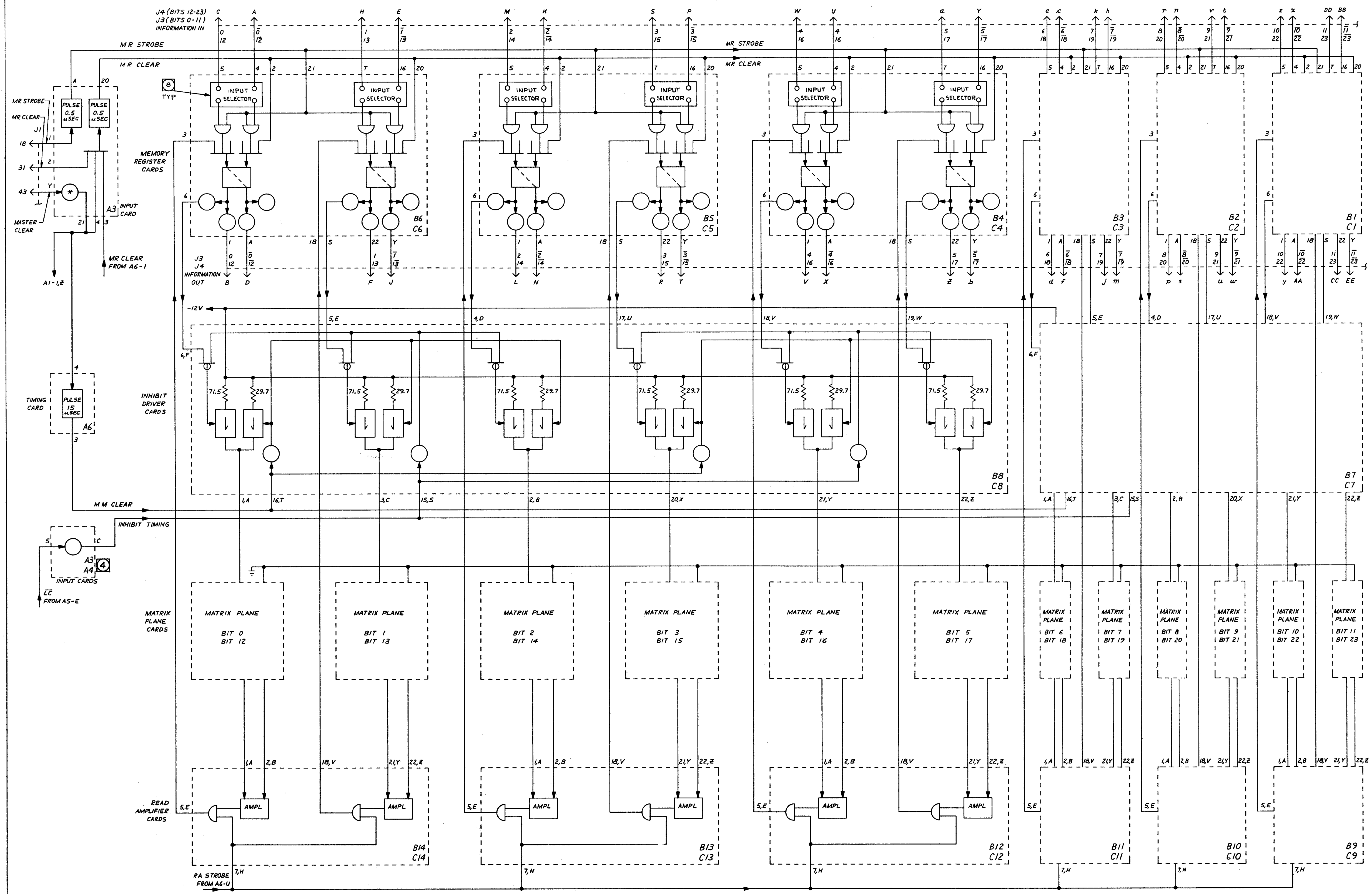


Figure 6-1. RB Logic Symbols

SERIAL EFFECTIVITY	LTR	REVISIONS DESCRIPTION	DRAFTSMAN	DATE	CHECK
1240 THRU 1336, 1389 & UP	A			5-6-60	
1240 THRU 1336, 1389 & UP	B	CHANGED PER E.O. NO. 2953	STOVALL	5-13-60	



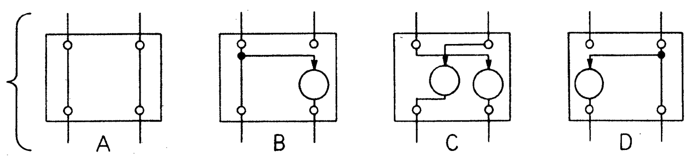
USE THIS DRAWING FOR ALL SERIAL NOS. EXCEPT 1337 AND 1339 THROUGH 1345

12310 B

5. IF BQ CARD (A1) IS NOT USED, THESE JUMPERS ARE INSTALLED
4. A3-C IS CONNECTED TO B8-15,S & B7-15,S
A4-C IS CONNECTED TO C8-15,S & C7-15,S
3. BITS 0 THRU 11 ARE ASSOCIATED WITH "B" CARD LOCATIONS
BITS 12 THRU 23 ARE ASSOCIATED WITH "C" CARD LOCATIONS
2. (*) : INVERTING OR NON-INVERTING AMPLIFIER DEPENDING UPON INTERNAL CONNECTIONS
1. ALL RESISTANCE VALUES IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

8. LOGIC FOR REGISTER INPUT SELECTOR



7. THE FUNCTION OF THESE GATES IS PERFORMED WITH NO PHYSICAL GATE PRESENT

6. GATES WIRED ON BACK OF CARD CAGE

SERIAL	NEXT ASSY	USED ON	FINAL ASSY
1240 THRU 1336, 1389 & UP		RB SERIES	

LIST OF MATERIAL

TELEMETER MAGNETICS, INC.
2937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM - RB SERIES

PROJ SUPER: B.T. 5/6/60
PROJ ENGR: 5/6/60
ENGINEER: R. 5/6/60
CHECKER: 29 APR 1960
DRAFTSMAN: 20 APR 60

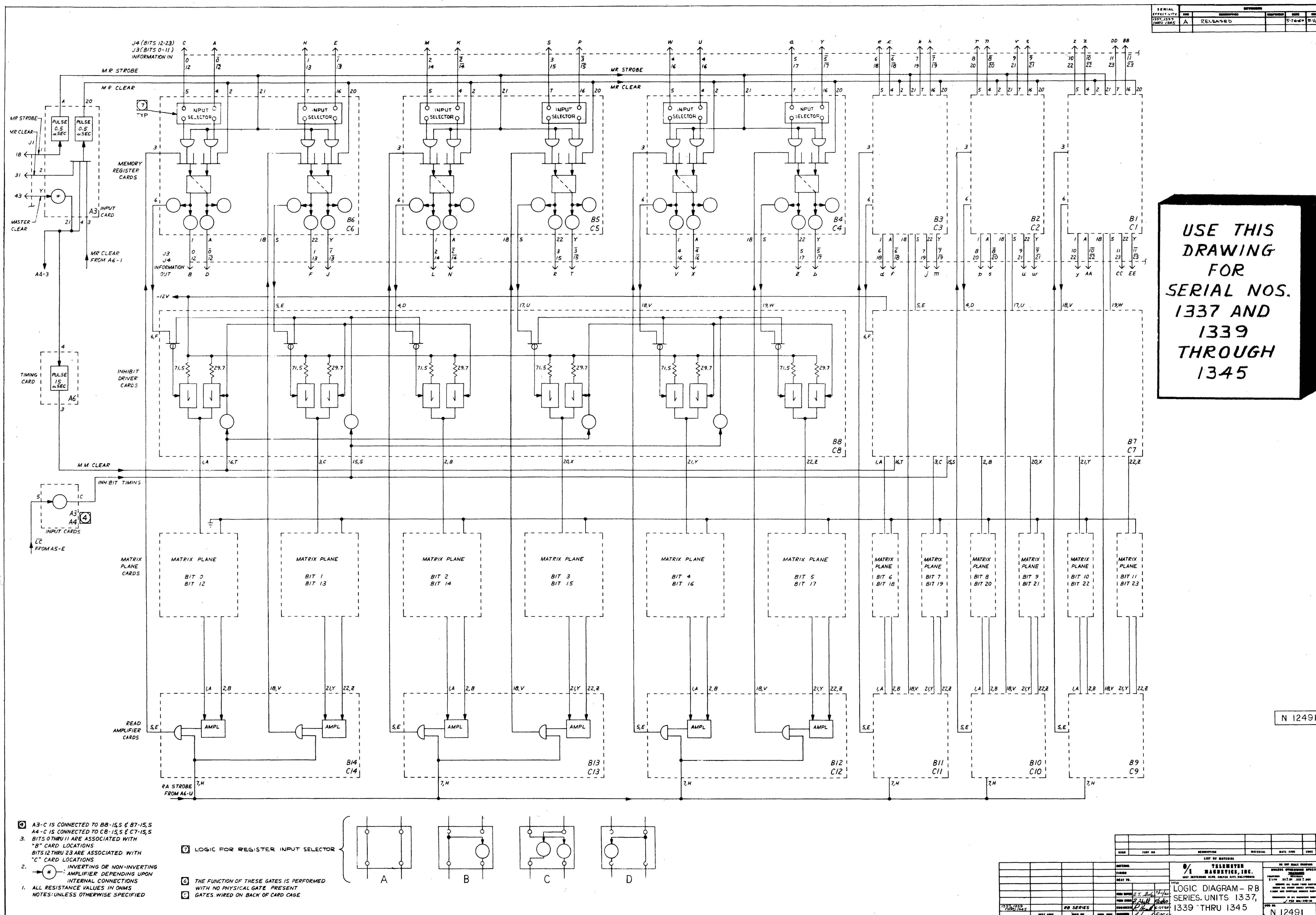
SCALE NONE

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED

DWG NO 12310 B

SHEET 1 OF 2


USE THIS DRAWING FOR SERIAL NOS. 1337 AND 1339 THROUGH 1345
J4 (BITS 12-23)
J3 (BITS 0-11)
INFORMATION IN
M.R. STROBE
M.R. CLEAR
INPUT SELECTOR
MEMORY REGISTER CARDS
INPUT CARD
MASTER CLEAR
MR CLEAR FROM A6-1
J3 J4 INFORMATION OUT
TIMING CARD
PULSE 15 μSEC
INHIBIT DRIVER CARDS
M.M. CLEAR
INHIBIT TIMING
INPUT CARDS
LC FROM A5-E
MATRIX PLANE CARDS
MATRIX PLANE
READ AMPLIFIER CARDS
AMPL
RA STROBE FROM A6-U
4 A3-C IS CONNECTED TO B8-15,S & B7-15,S
A4-C IS CONNECTED TO C8-15,S & C7-15,S
3. BITS 0 THRU 11 ARE ASSOCIATED WITH "B" CARD LOCATIONS
BITS 12 THRU 23 ARE ASSOCIATED WITH "C" CARD LOCATIONS
2. INVERTING OR NON-INVERTING AMPLIFIER DEPENDING UPON INTERNAL CONNECTIONS
1. ALL RESISTANCE VALUES IN OHMS
NOTES: UNLESS OTHERWISE SPECIFIED
7 LOGIC FOR REGISTER INPUT SELECTOR
6 THE FUNCTION OF THESE GATES IS PERFORMED WITH NO PHYSICAL GATE PRESENT
5 GATES WIRED ON BACK OF CARD CAGE
A B C D
RELEASED
TELEMETER MAGNETICS, INC.
LOGIC DIAGRAM - RB SERIES. UNITS 1337, 1339 THRU 1345
N 12491 A
RB SERIES

USE THIS DRAWING FOR ALL SERIAL NOS. EXCEPT 1337 AND 1339 THROUGH 1345

TO MAGNETIC MODULE
P6 TO SCHEMATIC 11934
P5 TO SCHEMATIC 11932

SWITCH CARDS
A16- Y SWITCH
A17- X SWITCH

COUNT LOGIC CARDS

TRANSPOSE REGISTER CARDS

ADDRESS REGISTER CARDS

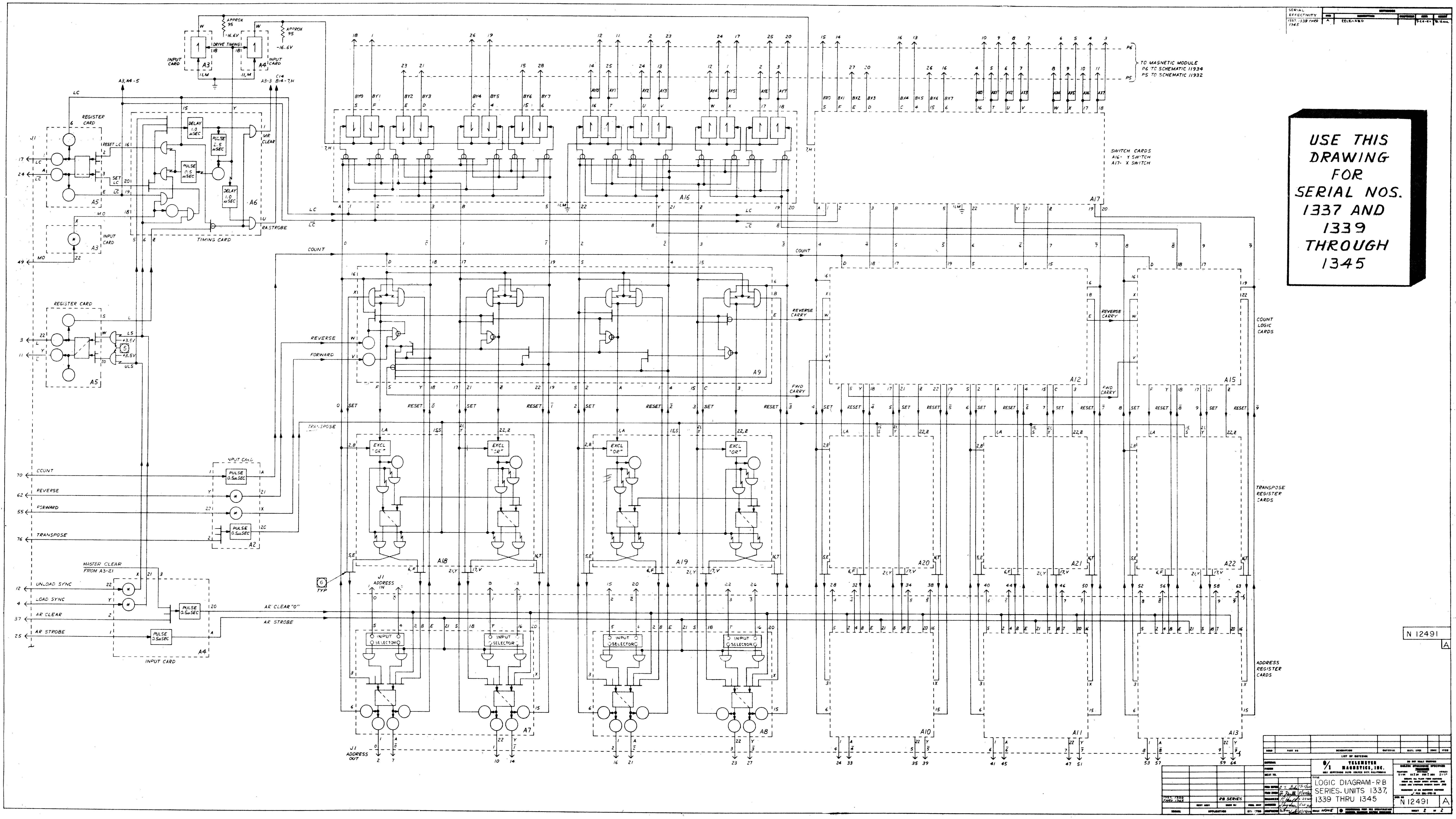
12310 B

LOGIC DIAGRAM - RB SERIES

TELEMETER MAGNETICS, INC.

SIZE B | 12310 | B

SHEET 2 OF 2


USE THIS DRAWING FOR SERIAL NOS. 1337 AND 1339 THROUGH 1345
TO MAGNETIC MODULE
P6 TO SCHEMATIC 11934
P5 TO SCHEMATIC 11932
SWITCH CARDS
A16 - Y SWITCH
A17 - X SWITCH
REGISTER CARD
INPUT CARD
TIMING CARD
DRIVE TIMING
DELAY 1.0 μSEC
PULSE 2.5 μSEC
PULSE 0.5 μSEC
MR CLEAR
RASTROBE
COUNT
REVERSE
FORWARD
TRANSPOSE
REVERSE CARRY
FWD CARRY
COUNT LOGIC CARDS
TRANSPOSE REGISTER CARDS
ADDRESS REGISTER CARDS
EXCL "OR"
INPUT SELECTOR
J1 ADDRESS IN
J1 ADDRESS OUT
MASTER CLEAR FROM A3-21
UNLOAD SYNC
LOAD SYNC
AR CLEAR
AR STROBE
AR CLEAR "0"
SET
RESET
N 12491
LOGIC DIAGRAM - RB SERIES. UNITS 1337, 1339 THRU 1345
RB SERIES

either a positive or negative-going input voltage. Any time delay between input and output pulses is indicated in microseconds.

6-15. FLIP-FLOP. This circuit furnishes two pairs of complementary levels. One level in each pair is high, the other is low. Input voltages control the flip-flop to establish which level in each complementary pair of outputs is high. In the symbol, the extremes of the dashed line indicate the set input and the true output.

6-16. CURRENT SWITCH. A current switch controls the flow of comparatively high amplitude, short duration currents into a low impedance load. The state of the switch is controlled by input gating levels. A high input is required to turn a switch ON.

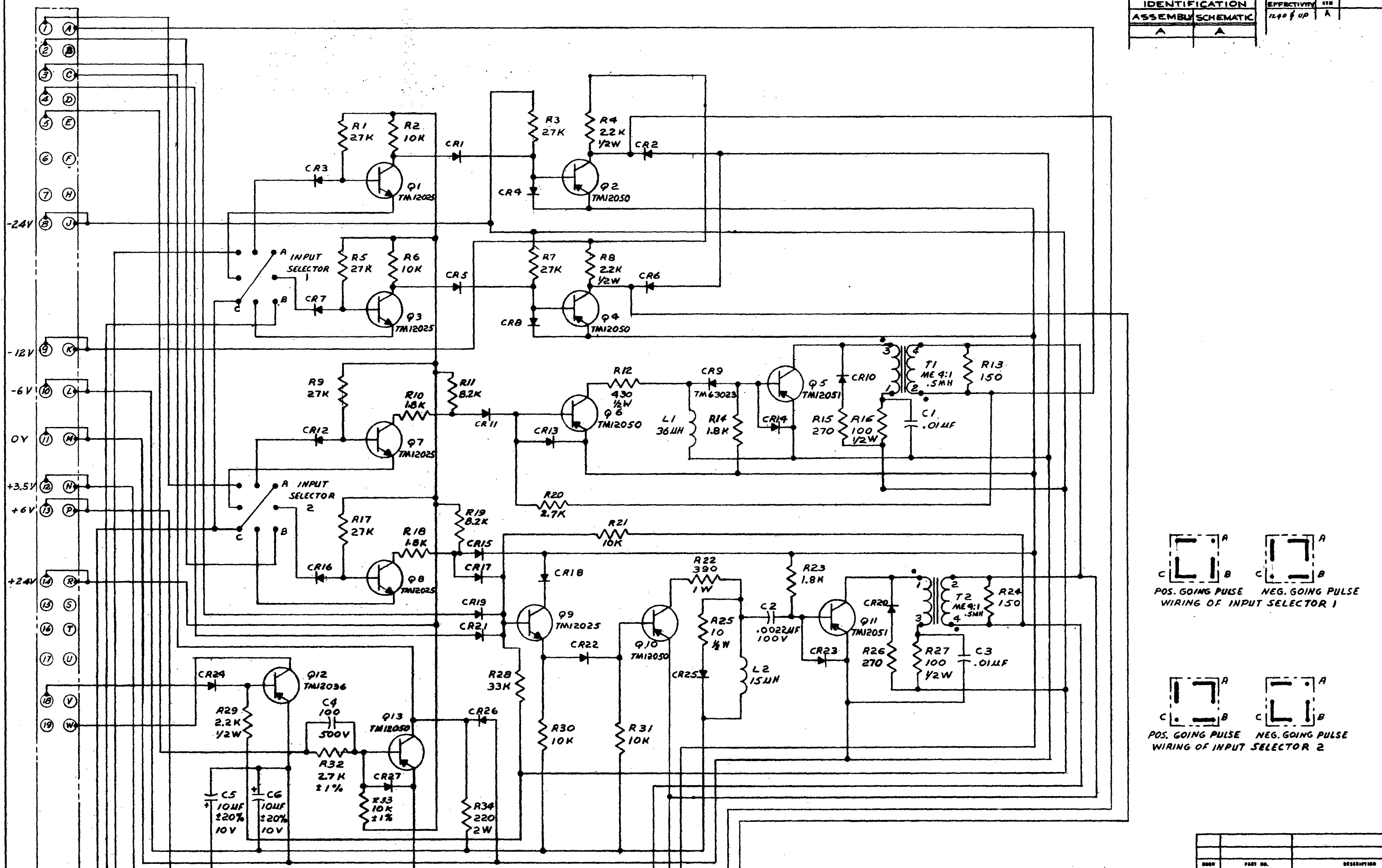
6-17. EXCLUSIVE OR. The required high output from this gate is developed only when one of its two inputs is low, and the other is high. Two high inputs develop a low output.

6-18. DIFFERENTIATOR. A differentiator produces a pulse whose duration is proportional to the rise or fall time of the input signal level. Either a pulse, or a changing d-c level can produce a comparatively short duration output voltage from the differentiator.

6-19. NEGATOR. This term expresses a negation of the signal with which it is associated. An OR gate, followed by a Negator, develops a required high (signal) output only when all of its input legs are low. An AND gate, followed by a Negator, develops a required high (signal) output when any of its input terms are low.

6-20. AMPLIFIER. This circuit amplifies positive or negative input signals. Outputs are the same polarity as inputs.

LEGEND OF ISSUE IDENTIFICATION		SERIAL EFFECTIVITY	LTR	DESCRIPTION	DATE
ASSEMBLY	SCHEMATIC				
A	A	1240 & UP	A		2-19-60



7. ASSY. DWG 11931
6. TRANSFORMERS ARE TECHNITROL MQ4UA
5. CAPACITORS RATED ±10%
4. CAPACITANCE VALUES IN MICROMICROFARADS
3. RESISTANCE VALUES IN OHMS
2. RESISTORS RATED ±5%, 1/4W
1. DIODES ARE TM63015
NOTES: UNLESS OTHERWISE SPECIFIED

11930 A

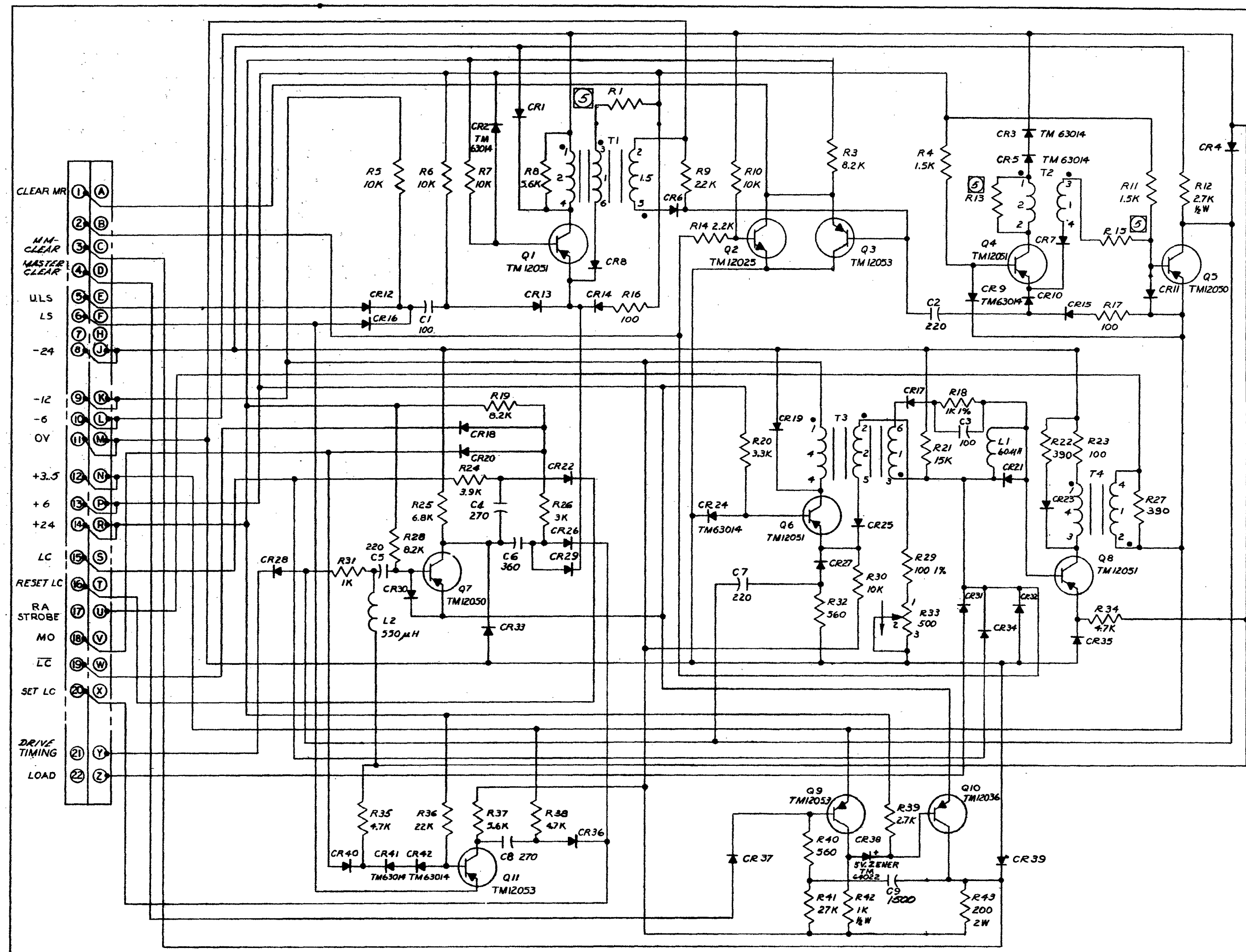
1240 & UP — R.B. SERIES

TELEMETER MAGNETICS, INC.

SCHEMATIC DIAGRAM
INPUT-A

11930 A

3.0



7. ALL CAPACITORS RATED ±5%, 500VDC
6. ALL DIODES TM63015
5. R1, R13 & R15 VALUE TO BE DETERMINED IN TEST
4. ALL CAPACITANCE VALUES IN MICROMICROFARADS
3. FOR ASSY SEE DWG Nº 11927
2. ALL RESISTORS RATED ±5%, ¼W
1. ALL RESISTANCE VALUES IN OHMS
NOTES: UNLESS OTHERWISE SPECIFIED

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE

SERIAL EFFECTIVITY	SYM	DESCRIPTION	DRAFTSMAN	DATE	CHECK
1240 & UP	A	R. [illegible]		2-29-60	B.H.m

ITEM	PART NO.	DESCRIPTION	MATERIAL	MATL SPEC	ZONE	ITEM

LIST OF MATERIAL

TELEMETER MAGNETICS, INC.
2051 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

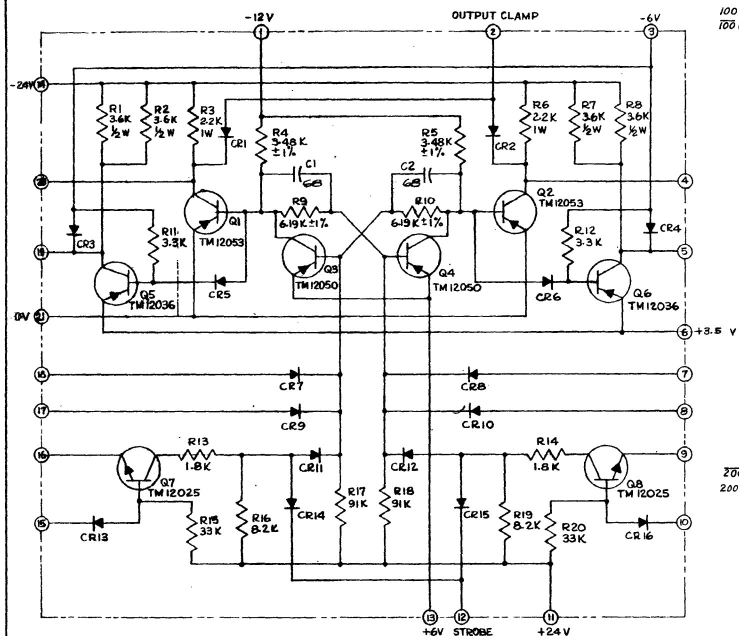
TITLE: SCHEMATIC - TIMING - A

SERIAL	1240 & UP
APPLICATION	RB SERIES
SCALE	NONE
DWG NO.	11926 A
SHEET	1 OF 1

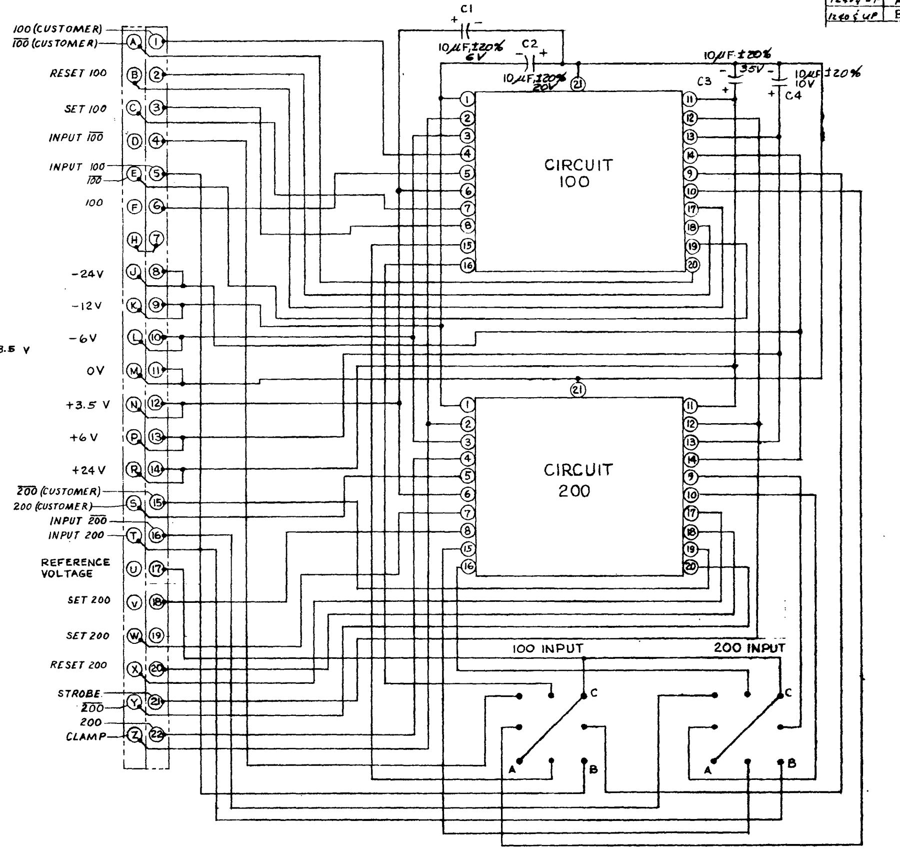
11926 A

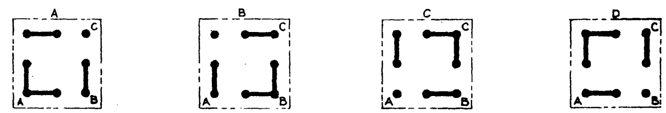
2.0

SERIAL EFFECTIVITY	SYM	DESCRIPTION	DRAFTSMAN	DATE	CHECK
1240 & UP	A	RELEASED		2-24-60	
1240 & UP	B	CHGD PER E.O. 3017		5-11-60	



CIRCUIT SERIES 100 & 200





POSITIVE GOING PULSES (SINGLE OR DOUBLE ENDED)

SINGLE ENDED LEVEL (WHERE THE MORE POSITIVE LEVEL LOADS A "1".

NEGATIVE GOING PULSES (SINGLE OR DOUBLE ENDED) OR DOUBLE ENDED LEVELS

SINGLE ENDED LEVEL (WHERE THE MORE NEGATIVE LEVEL LOADS A "1"

WIRING OF INPUT SELECTOR

LEGEND OF ISSUE IDENTIFICATIONS	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A
A	B

11920 B

7. ALL CAPACITORS RATED ± 5%, 300V
6. SAMPLE PART NO. CALLOUT: R1 WOULD BE R101 AND R201.
5. ASSEMBLY DWG: 11921
4. ALL CAPACITANCE VALUES ARE IN MICROMICROFARADS.
3. ALL RESISTORS RATED ±5%, 1/4 W.
2. ALL RESISTANCE VALUES ARE IN OHMS
1. ALL DIODES ARE TM 63015.

NOTES; UNLESS OTHERWISE SPECIFIED.

SERIAL	NEXT ASSY	USED ON	FINAL ASSY	QTY REQD
1240 & UP		RB SERIES		

LIST OF MATERIAL

TELEMETER MAGNETICS, INC.
Jefferson Blvd. Culver City, California

TITLE: SCHEMATIC– REGISTER - A

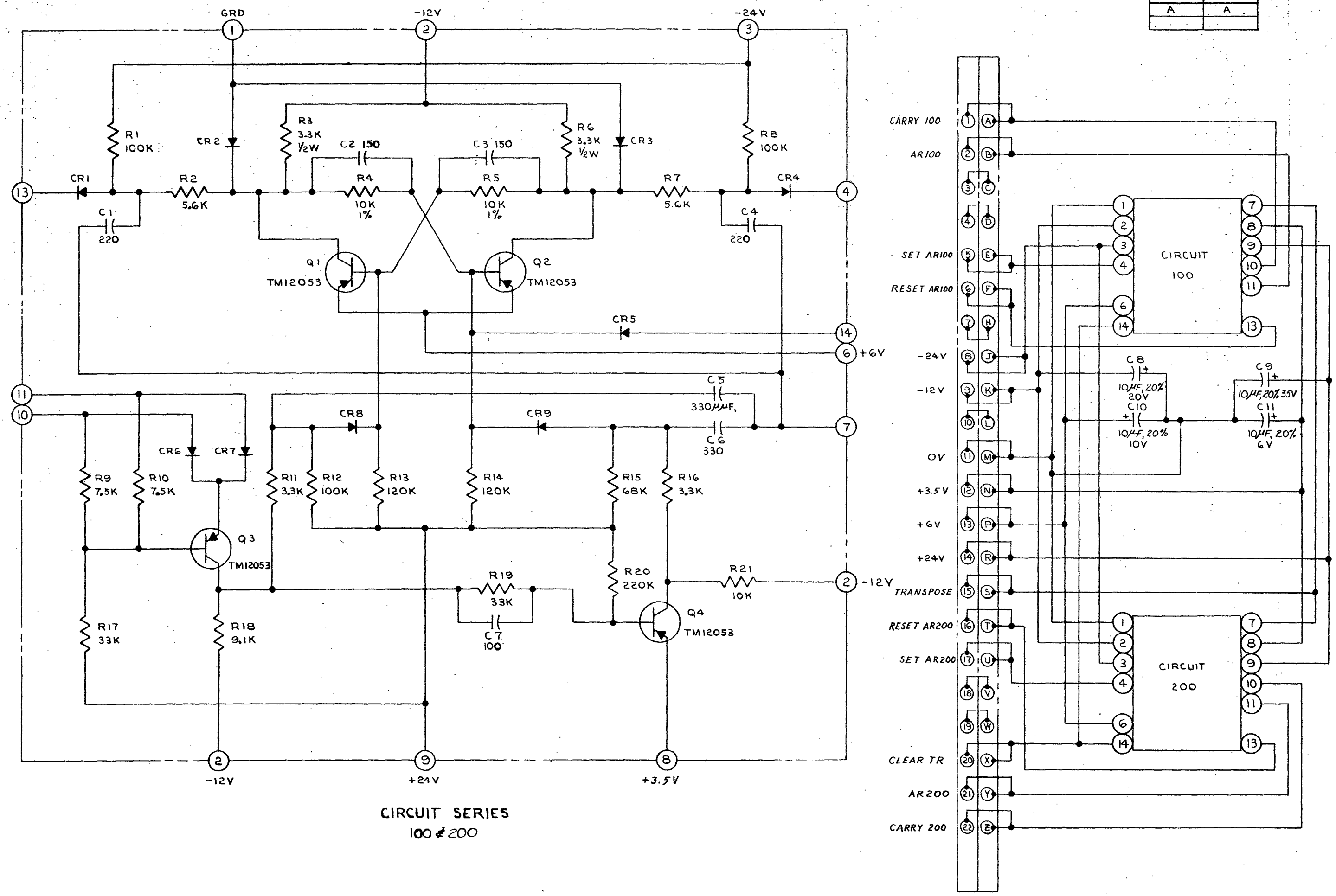
DO NOT SCALE DRAWING

DWG NO. 11920 B

SCALE NONE

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A

SERIAL EFFECTIVITY	SYM	DESCRIPTION	DRAFTSMAN	DATE	CHECK
1240 & UP	A	Released		2-24-60	B. Hue



11924
A

7. ALL CAPACITORS RATED ±5%, 500V
6. ALL CAPACITANCE VALUES IN MICROMICROFARADS
5. ALL RESISTORS RATED ±5%, 1/4W
4. SAMPLE PART Nº CALLOUT:
R1 WOULD BE R101 & R201
3. FOR ASSEMBLY DWG. SEE 11925
2. ALL RESISTANCE VALUES ARE IN OHMS
1. ALL DIODES TM 63015

NOTES: UNLESS OTHERWISE SPECIFIED.

REQD	PART NO.	DESCRIPTION	MATERIAL	MATL SPEC	ZONE	ITEM

LIST OF MATERIAL

SERIAL	NEXT ASSY	APPLICATION / USED ON	FINAL ASSY / QTY REQD
1240 & UP		RB SERIES / 1ST	

MATERIAL
FINISH
HEAT TR.
PROD. ENG. R. Heald 2/19/60
PROJ SUPER. B. T. Gooke 2/19/60
PROJ ENGR. J. Hall 2/19/60
ENGINEER H. Bassuo 2/19/60
CHECKER [illegible] 12/3/59
DRAFTSMAN C. Stovall 11/21/59

TELEMETER MAGNETICS, INC.
2527 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC—TRANSPOSE REGISTER-A

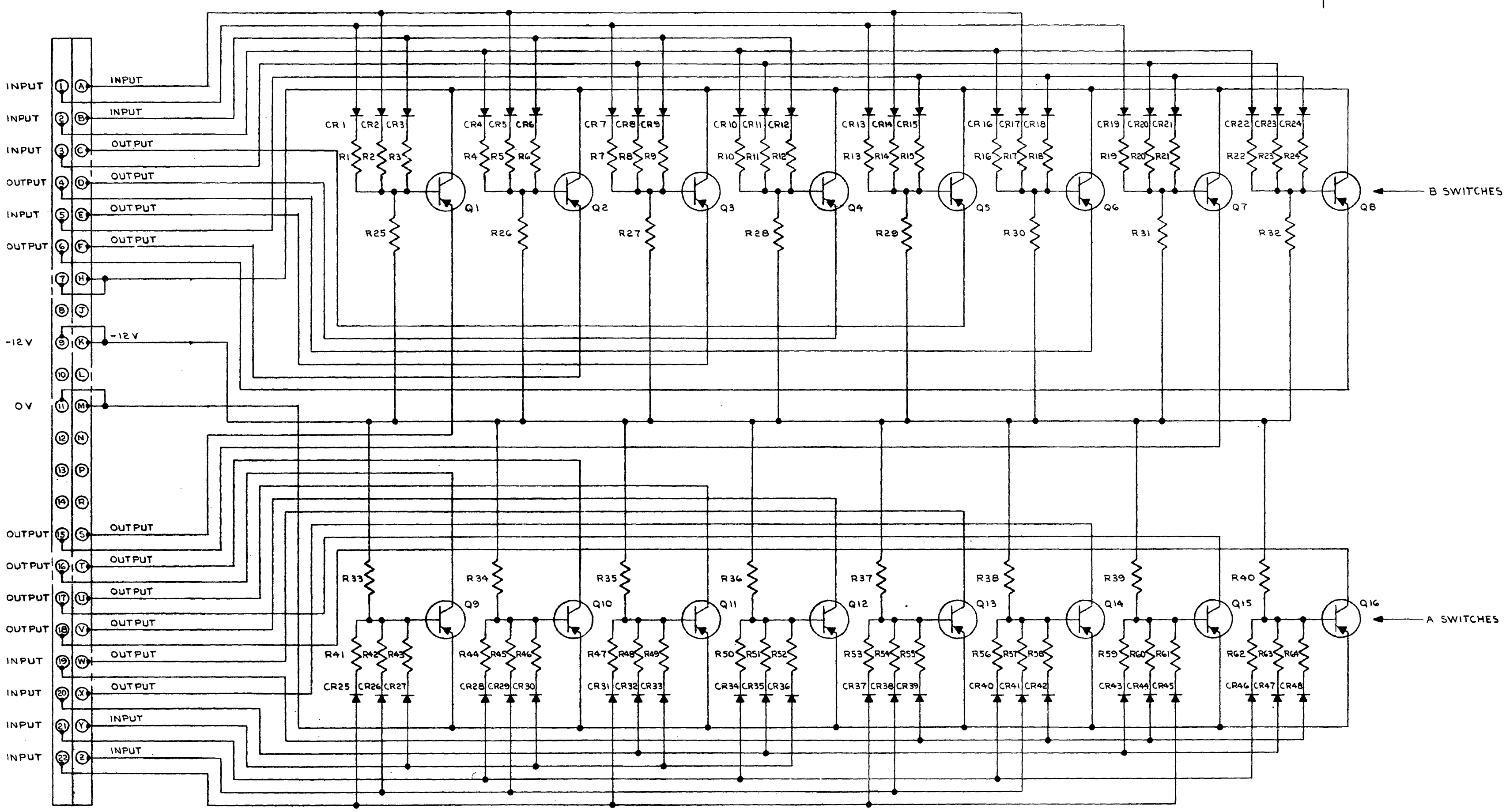
SCALE NONE
COMMERCIAL PART. SEE SPECIFICATION CONTROL DRAWING BEFORE ORDERING

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES
FRACTIONS ±1/64 DECIMALS .XX ±.01 .XXX ±.005 ANGLES ±1/2°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .005
CORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

DWG NO. 11924 A
SHEET OF

1.0

SERIAL EFFECTIVITY	REVISIONS				
	SYM	DESCRIPTION	DRAFTSMAN	DATE	CHECK
	A	Released		2-19-60	B.Hun



LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A

11918 A

5. FOR ASSEMBLY SEE DWG. NO. 11919
4. R25 TO R40; 1000 OHMS, ±5%, 1/2W
3. R1 TO R24, R41 TO R64; 47 OHMS, ±5%, 1/4W.
2. ALL TRANSISTORS TM 12036
1. ALL DIODES TM-63015

NOTES: UNLESS OTHERWISE SPECIFIED.

REQD	PART NO.	DESCRIPTION	MATERIAL	MATL SPEC	ZONE	ITEM

LIST OF MATERIAL

		RB SERIES	
	NEXT ASSY	1ST USED ON	FINAL ASSY
SERIAL	APPLICATION		QTY REQD

MATERIAL		
FINISH		
HEAT TR.		
PROD ENG	R Heath	2/19/60
PROJ SUPER	E. T. Lide	2/19/60
PROJ ENGR	[illegible]	2/18/60
ENGINEER	H. Graf	2/18/60
CHECKER	[illegible]	[illegible]
DRAFTSMAN	C. Sternall	11/20/59

0/1 TELEMETER MAGNETICS, INC.
5937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE SCHEMATIC— SWITCH - A

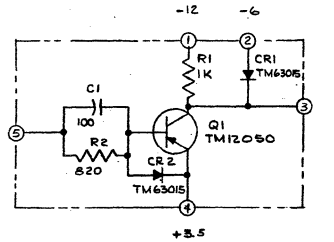
SCALE NONE

✱ COMMERCIAL PART. SEE SPECIFICATION CONTROL DRAWING BEFORE ORDERING

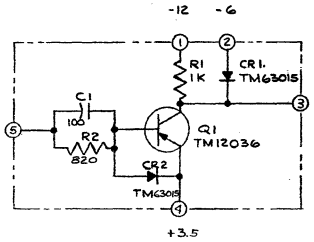
DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
TOLERANCES
FRACTIONS ±1/64 DECIMALS .XX ±.01 .XXX ±.005 ANGLES ±1/2°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010
CBORE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

DWG NO. 11918 A

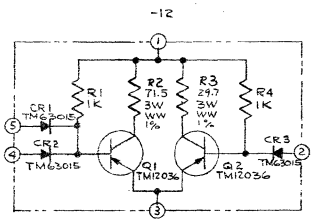
SHEET OF



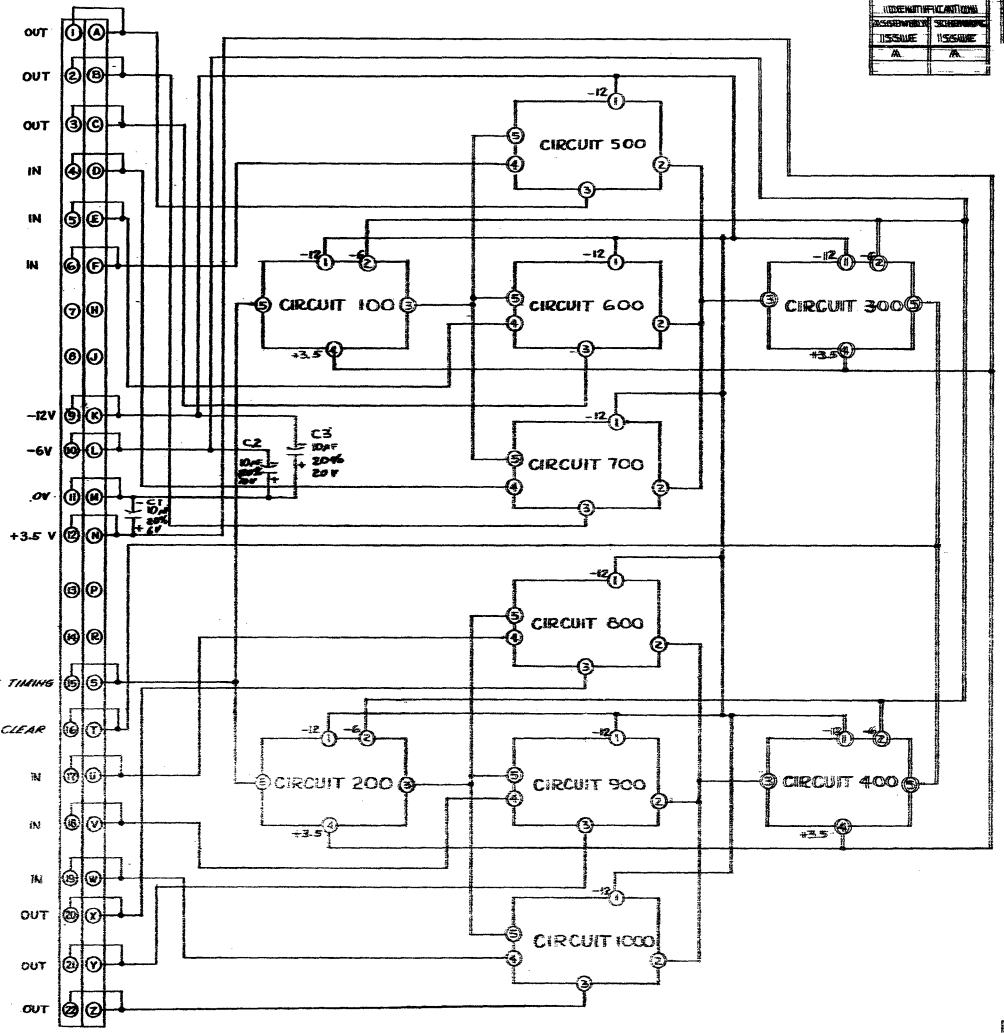
CIRCUIT SERIES 100 & 200



CIRCUIT SERIES 300 & 400



CIRCUIT SERIES 500 THRU 1000



11916 A

6. SAMPLE PART Nº CALLOUT:
   R1 IN SERIES 100 & 200 IS R101 & R201.
5. ALL CAPACITORS RATED ±10% ; 600V
4. ALL RESISTORS RATED ± 5%, ½ W
3. ALL RESISTANCE VALUES ARE IN OHMS
2. ALL CAPACITANCE VALUES ARE IN MICROMICRO FARADS
1. ASSY DWG NO. 11917

NOTES: UNLESS OTHERWISE SPECIFIED.

RB SERIES

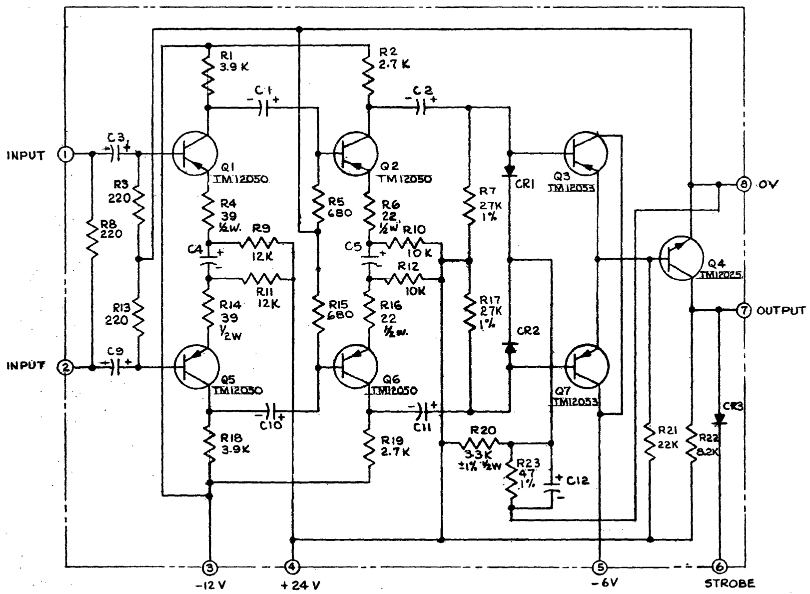
SCHEMATIC-
INHIBIT-A

TELEMETER MAGNETICS Incorporated

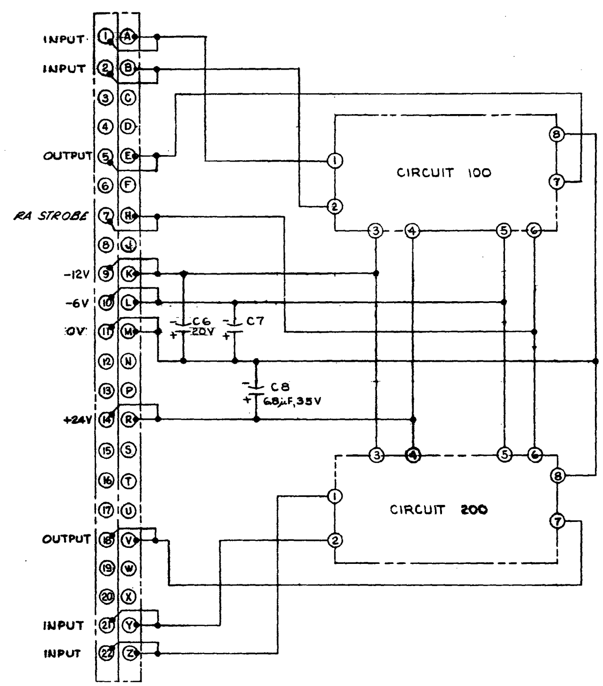
11916

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A

SERIAL EFFECTIVITY	REVISIONS LTR	DESCRIPTION	DRAFTSMAN	DATE	CHECK
12408 UP	A	Release		2-24-60	G.Hall



CIRCUIT SERIES 100 & 200



12173
A

6. DIODES ARE TM 63015.
5. SAMPLE CIRCUIT REF. DESIGNATION; R1 WOULD BE R101 & R201.
4. ASSY DWG NO. 12174
3. CAPACITORS 10µF, ±20%, 10V
2. RESISTORS RATED ±5%, ¼W
1. RESISTANCE VALUES IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

SERIAL	APPLICATION		QTY REQD
12408 UP		RB SERIES	
	NEXT ASSY	USED ON	FINAL ASSY

LIST OF MATERIAL

CODE	PART NO.	DESCRIPTION	MATERIAL	MATL SPEC	ZONE	ITEM

MATERIAL
FINISH
HEAT TR.
PROD. ENG. R. Heath 2/10/60
PROJ SUPER. D. T. [illegible] 2/11/60
PROJ ENGR. B. Hall 2/19/60
ENGINEER [illegible] 2/19/60
CHECKED [illegible]
DRAFTSMAN [illegible] 5 JAN 60

TELEMETER MAGNETICS, INC.
2027 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC-READ AMPLIFIER 'N'

DWG NO. 12173 A

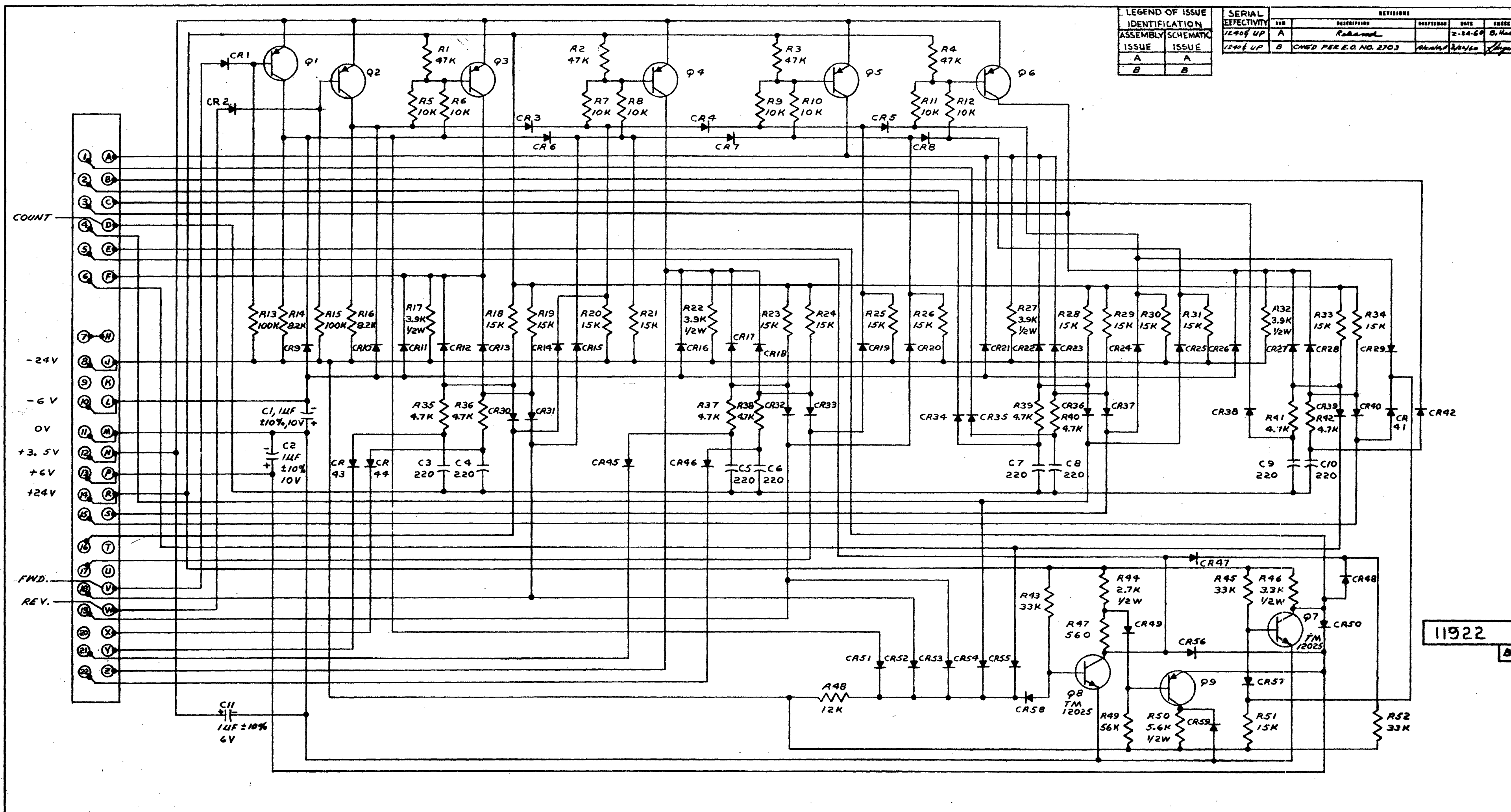
SCALE NONE
COMMERCIAL PART-SEE SPECIFICATION CONTROL DRAWING BEFORE ORDERING

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED TOLERANCES

SHEET OF

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A
B	B

SERIAL EFFECTIVITY	SYM	DESCRIPTION	DRAFTSMAN	DATE	CHECK
12406 UP	A	Released		2-24-60	B. Hau
12406 UP	B	CHG'D PER E.O. NO. 2703			



7. ASSEMBLY DRAWING 11622
6. ALL TRANSISTORS TM 12050
5. ALL DIODES TM 63015
4. ALL CAPACITORS RATED ±5%, 500V
3. ALL CAPACITANCE VALUES IN MICROMICROFARADS
2. ALL RESISTORS RATED ±5% 1/4W
1. ALL RESISTANCE VALUES IN OHMS

NOTES: UNLESS OTHERWISE SPECIFIED

SERIAL	APPLICATION		
12406 UP	RB SERIES	1ST	

TELEMETER MAGNETICS, INC.

SCHEMATIC-COUNT LOGIC-A

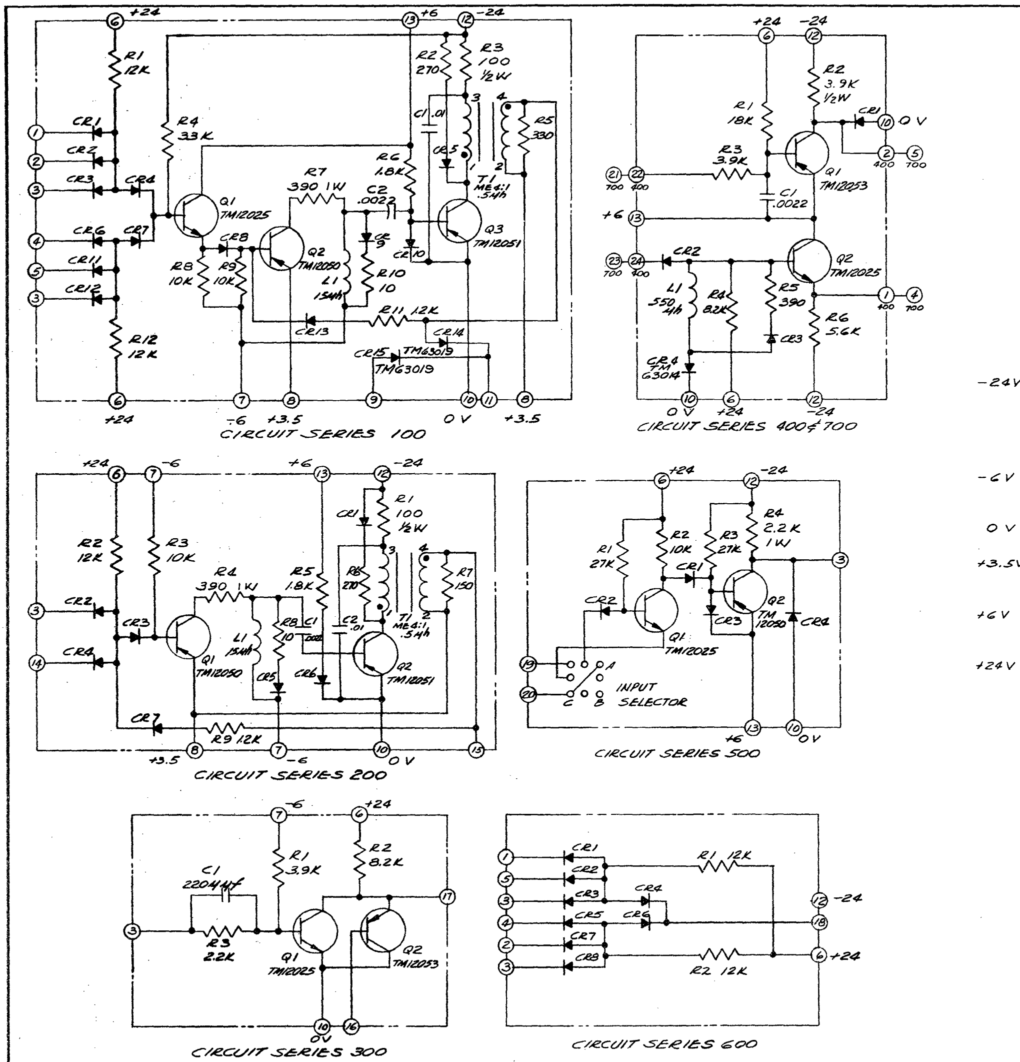
SCALE NONE

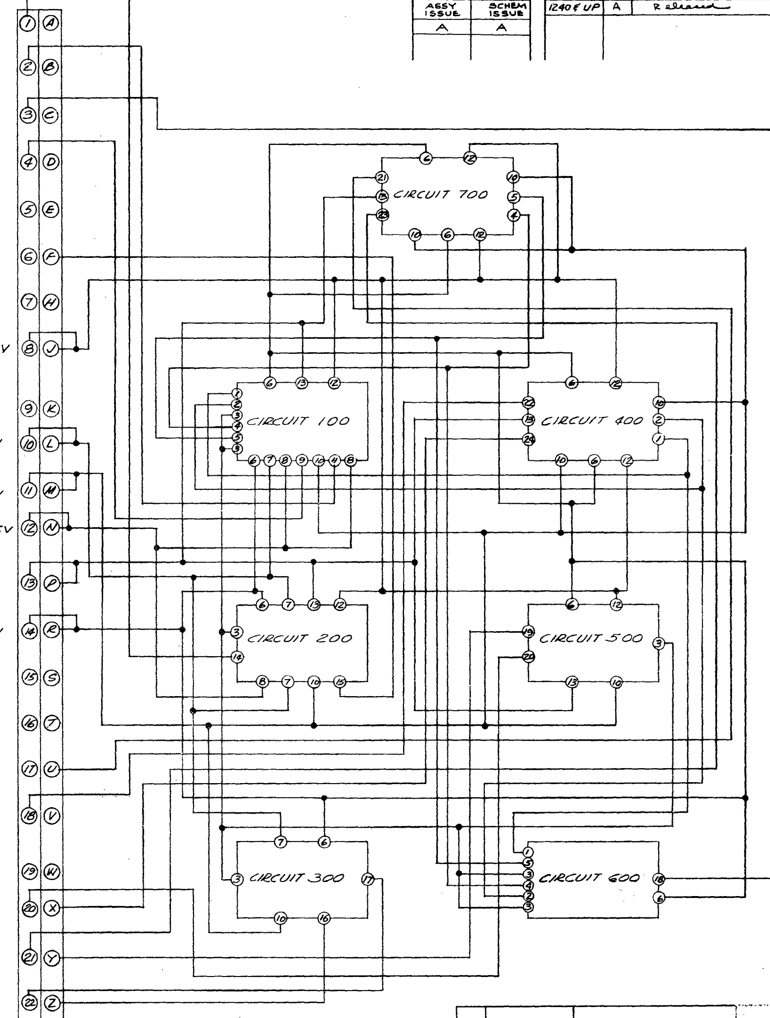
DWG NO. 11922 B

SHEET 1 OF 1

LEGEND OF ISSUE INDENTIFICATION	
ASSY ISSUE	SCHEM ISSUE
A	A

SERIAL EFFECTIVITY	REVISIONS				
	SYM	DESCRIPTION	DRAFTSMAN	DATE	CHECK
1240 & UP	A	Released		5-16-60	[illegible]





12195 A

6. SAMPLE PART Nº CALLOUT: FOR CIRCUIT 100 R1 WOULD BE R101 ETC.
5. ALL TRANSFORMERS ARE TECHNITROL MQ4UA
4. ASSY DWG NR. 12196
3. ALL DIODES ARE TM63015
2. ALL CAPACITANCE VALUES IN MICROFARADS
1. ALL RESISTANCE VALUES IN OHMS, ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

REQD	PART NO.	DESCRIPTION	MATERIAL	MATL SPEC	ZONE	ITEM

LIST OF MATERIAL

SERIAL	NEXT ASSY	USED ON	FINAL ASSY
1240 & UP		RB SERIES	
	APPLICATION		QTY REQD

MATERIAL		
FINISH		
HEAT TR.		
PROD. ENG.	R. Hegel	5/16/60
PROJ SUPER	D. McKee	5/16/60
PROJ ENGR	J. Hull	5/16/60
ENGINEER	D. McKee	5/16/60
CHECKER	[illegible]	3/2/60
DRAFTSMAN	[illegible]	FEB 1, 1960

0/1 TELEMETER MAGNETICS, INC.
9937 JEFFERSON BLVD. CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC DIAGRAM- BQ LOGIC

SCALE NONE

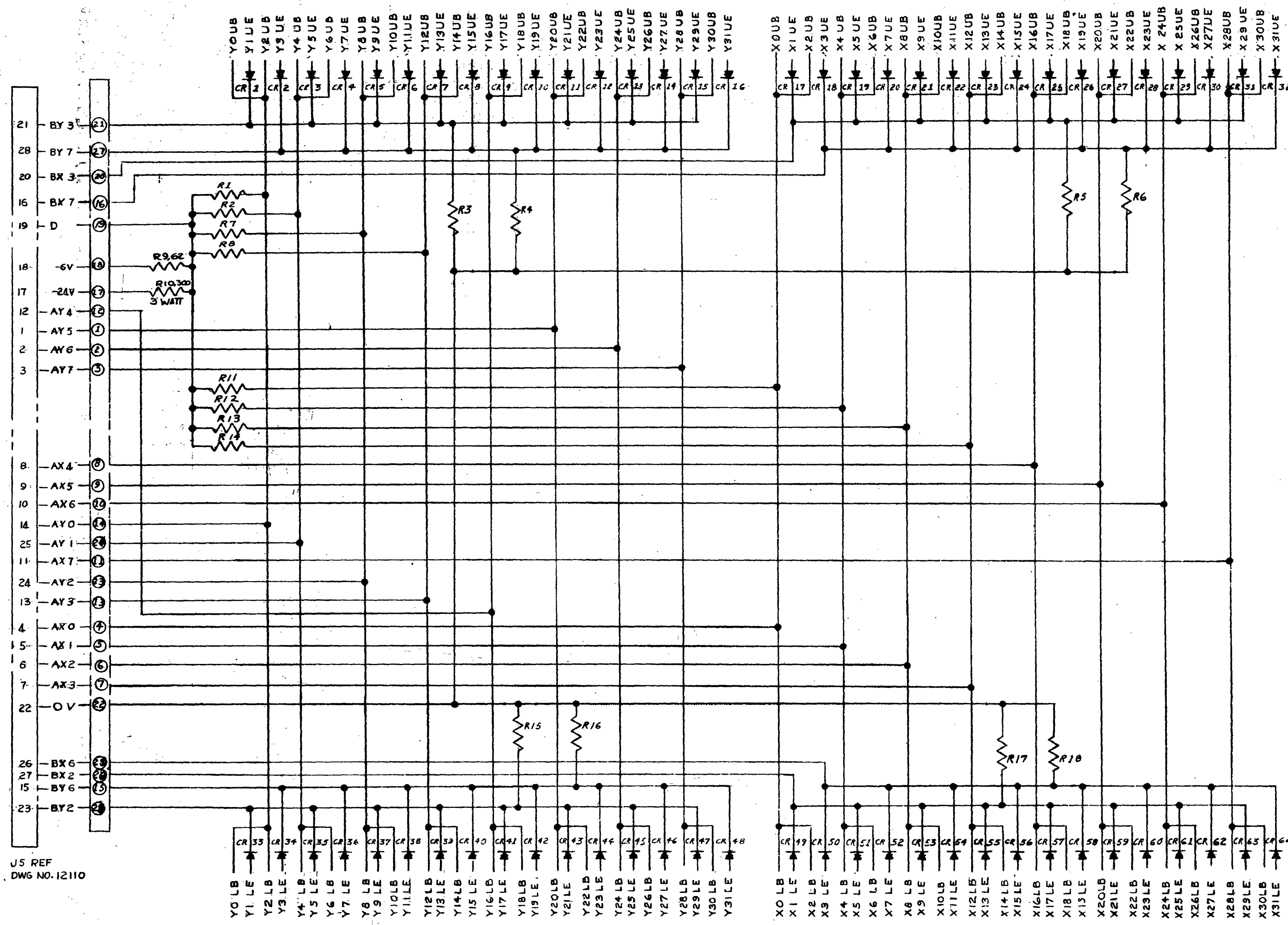
COMMERCIAL PART-SEE SPECIFICATION CONTROL DRAWING BEFORE ORDERING

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED TOLERANCES
FRACTIONS ±1/64 DECIMALS .XX ±.01 .XXX ±.005 ANGLES ±1/2°
REMOVE ALL FLASH FROM CASTINGS
BREAK ALL SHARP EDGES APPROX. .010
FORGE AND SPOTFACE CORNER RADII .010
ROUGHNESS OF ALL MACHINED SURFACES ✓ PER MIL-STD-10

DWG NO. 12195 A

SHEET 1 OF 1



SERIAL EFFECTIVITY	LTR	DESCRIPTION	DATE	APPROVAL
	A	Released	2-17-60	B. Harr
1328, 1331 THRU 1336, 1340 & UP	B	CHG'D PER E.O. NO. 2702	3/22/60	
	C	CHG'D PER E.O. 3019	3/24/60	

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A
B	B
B	C

11932 C

5. ALL RESISTANCE VALUES IN OHMS.
4. RESISTORS R1–R8 & R11–R18, 2.2 K.
3. ASSEMBLY DRAWING 11933
2. ALL RESISTORS RATED ±5%, ½W
1. ALL DIODES ARE TM-63006

NOTES: UNLESS OTHERWISE SPECIFIED.

DO NOT SCALE DRAWING

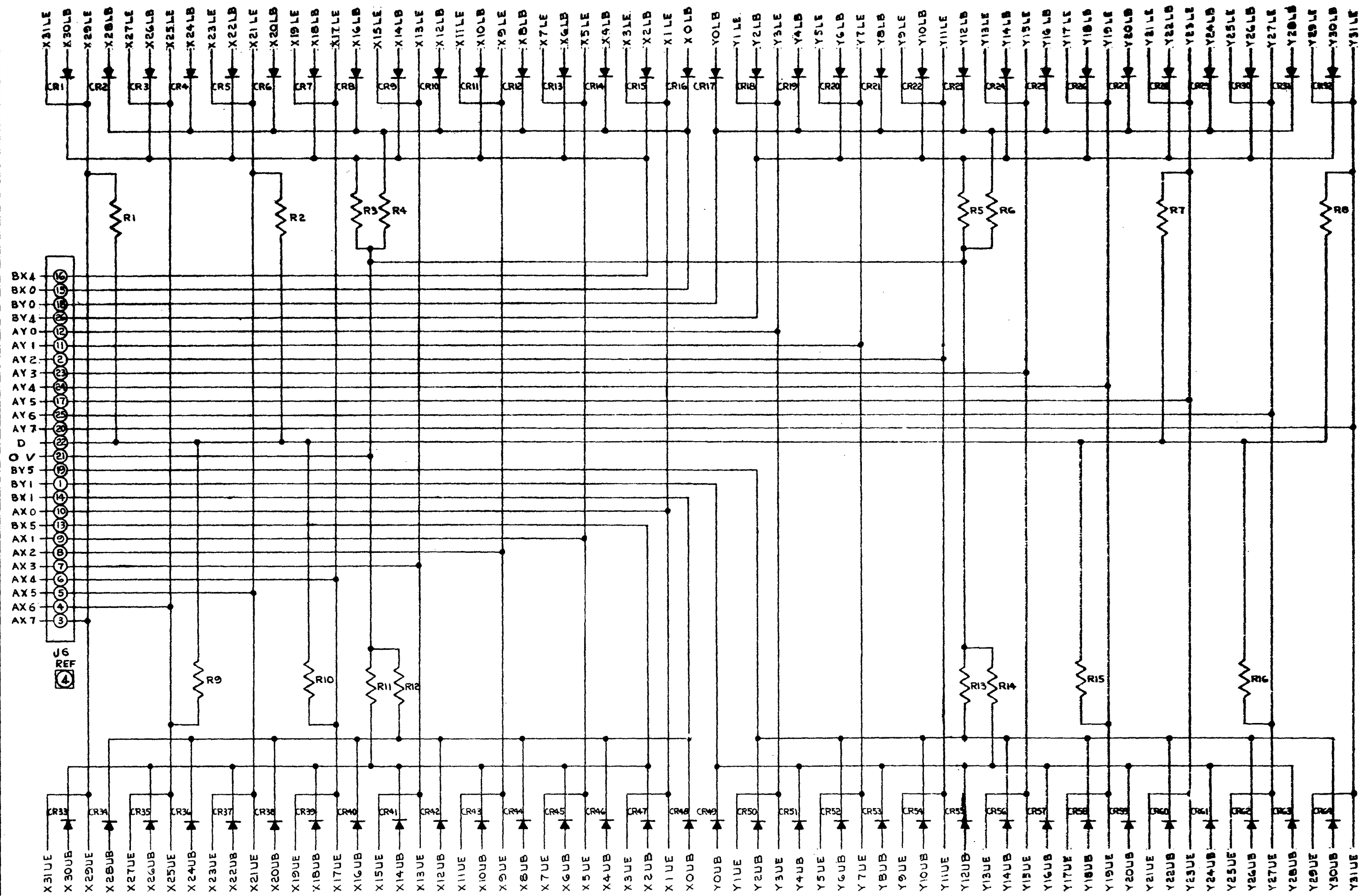
APPLICATION | QTY REQD

SCHEMATIC– TOP END PLATE, MATRIX MODULE

TELEMETER MAGNETICS Incorporated

SCALE NONE

11932



SERIAL EFFECTIVITY	SYM	REVISIONS			
	A	[illegible]			
	B	CHGD PER E.O. NO 2701			
	C	CHGD PER E.O. NO. 3020			

LEGEND OF ISSUE IDENTIFICATION	
ASSEMBLY ISSUE	SCHEMATIC ISSUE
A	A
B	B
B	C

11934 C

4 TERMINAL NO'S ON J6 (DWG NO. 12110) ALSO REPRESENT THE TERMINAL NO'S ON 11935 (BOTTOM END PLATE)

3. FOR ASSEMBLY SEE DWG. NO. 11935
2. ALL RESISTORS 2.2 K, ±5%, ½ W.
1. ALL DIODES ARE TM 63006

NOTES: UNLESS OTHERWISE SPECIFIED.

RB SERIES

LIST OF MATERIAL

TELEMETER MAGNETICS, INC.

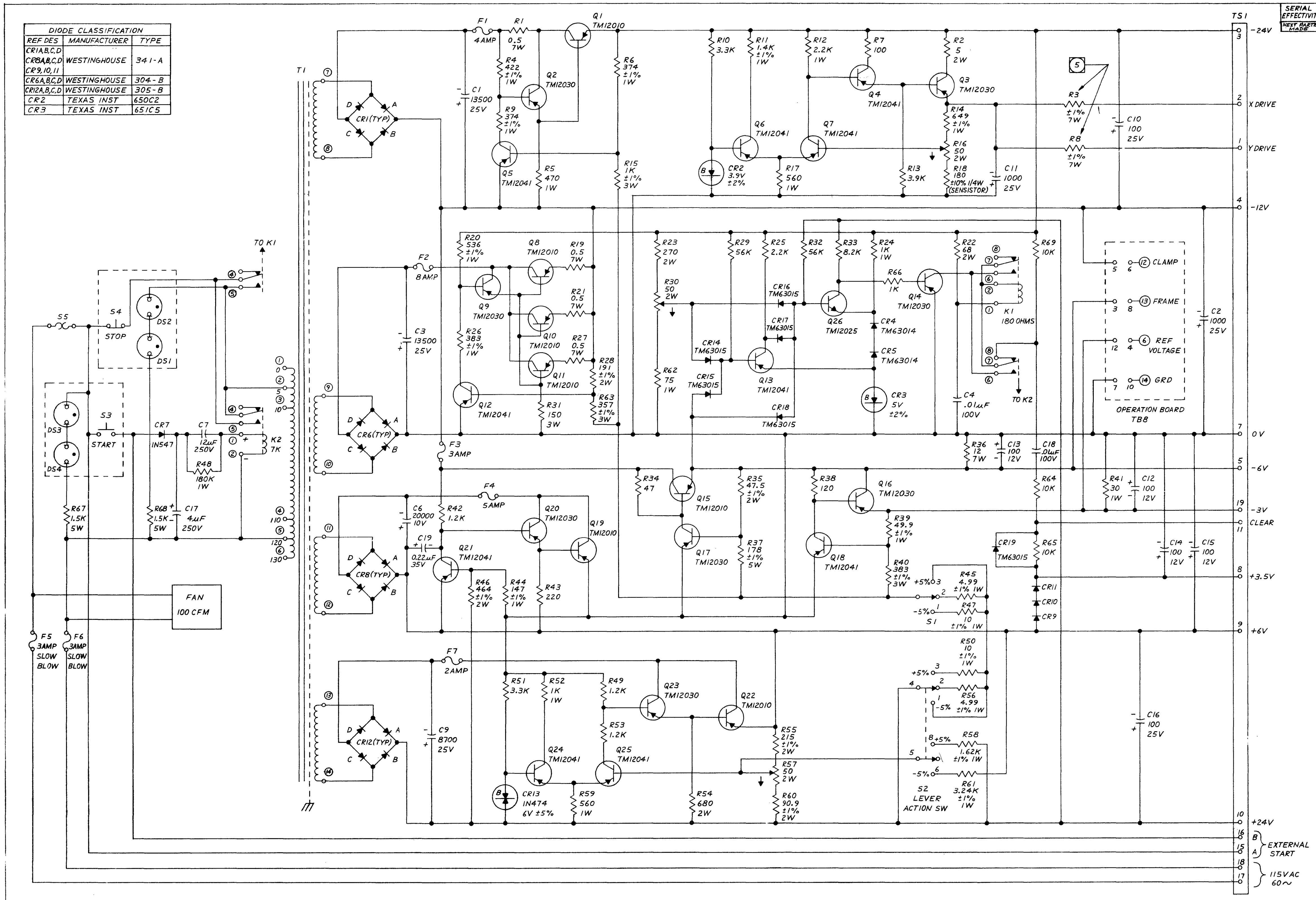
CULVER CITY, CALIFORNIA

SCHEMATIC - BOTTOM END PLATE MATRIX MODULE

SCALE NONE

DWG NO. 11934 C

DIODE CLASSIFICATION		
REF DES	MANUFACTURER	TYPE
CR1A,B,C,D CR3A,B,C,D CR9,10,11	WESTINGHOUSE	341-A
CR6A,B,C,D	WESTINGHOUSE	304-B
CR12A,B,C,D	WESTINGHOUSE	305-B
CR2	TEXAS INST	650C2
CR3	TEXAS INST	651C5



COMPONENTS LAST USED:
C19 R69
CR19 S5
F7 T1
Q26

7. DS3, DS4 & S3 (START SWITCH - GREEN) ARE ONE UNIT
6. DS1, DS2 & S4 (STOP SWITCH - YELLOW) ARE ONE UNIT
5. VALUES OF R3 & R8 TO BE DETERMINED IN TEST
4. NOS. IN CIRCLES ON T1, K1 & K2 INDICATES TERMINAL NOS.
3. ASSY DWG NO. 12128
2. ALL CAPACITANCE VALUES IN MICROMICROFARADS
1. ALL RESISTANCE VALUES IN OHMS ±5% 1/2W

NOTES: UNLESS OTHERWISE SPECIFIED

SERIAL EFFECTIVITY	REV	DESCRIPTION	DRAFTSMAN	DATE
	B	REVISED & REDRAWN PER E.O. 2765	NK	31 MAR 60

N12149 B

PROJ ENGR	R. HEATH 2-22-60
	B.T. GODA 2-22-60
	F. HULL 2-22-60
ENGINEER	N. YOST 2-22-60
CHECKER	SVETINA 2-10-60
DRAFTSMAN	B. BLEUER 11-17-59

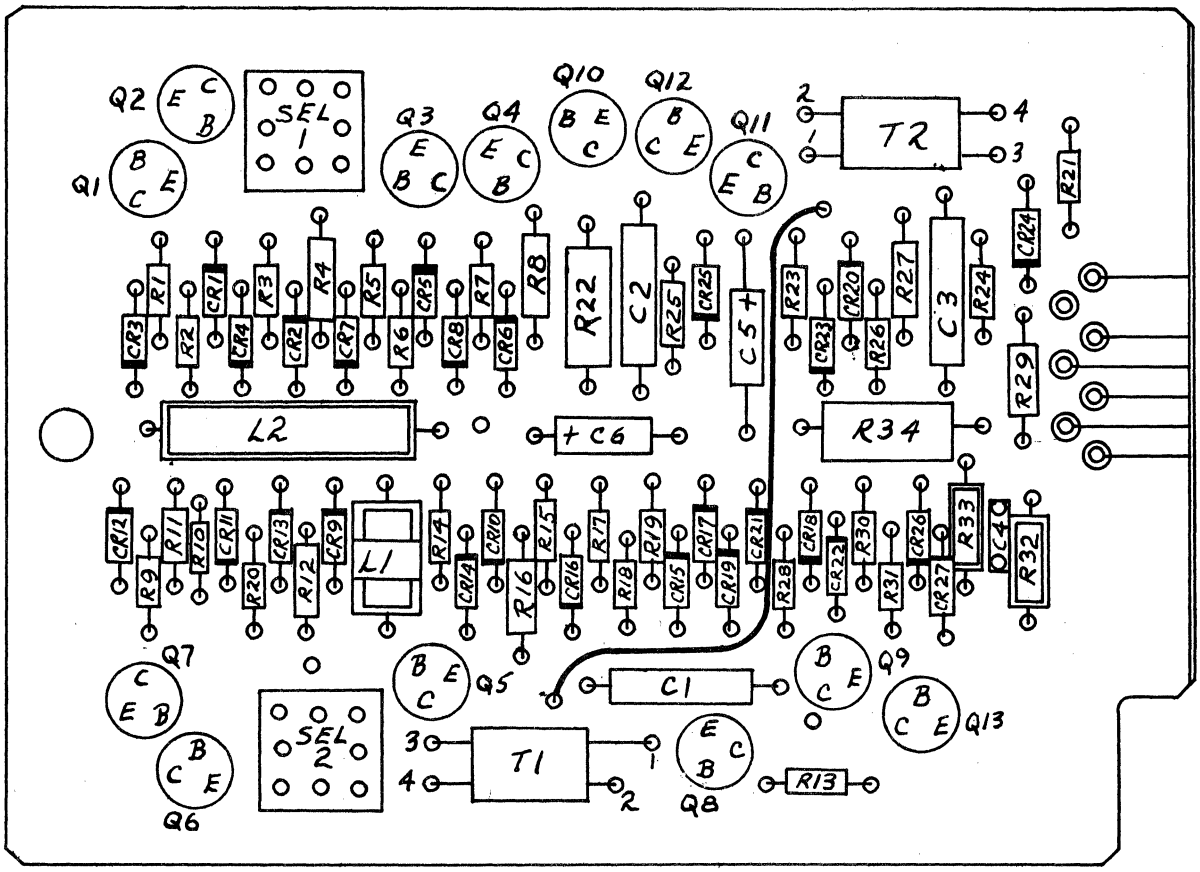
1240 & UP — RB SERIES

TELEMETER MAGNETICS, INC.

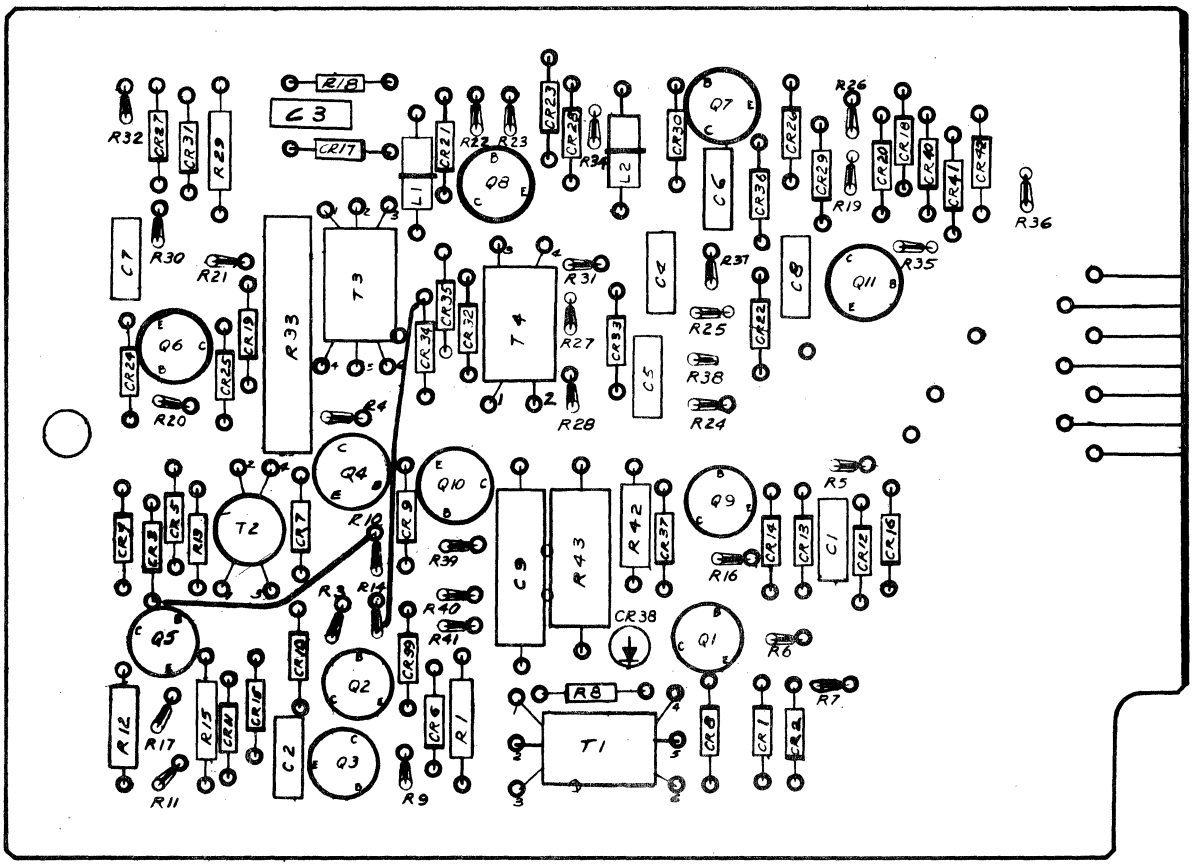
SCHEMATIC DIAGRAM - POWER SUPPLY

SCALE NONE

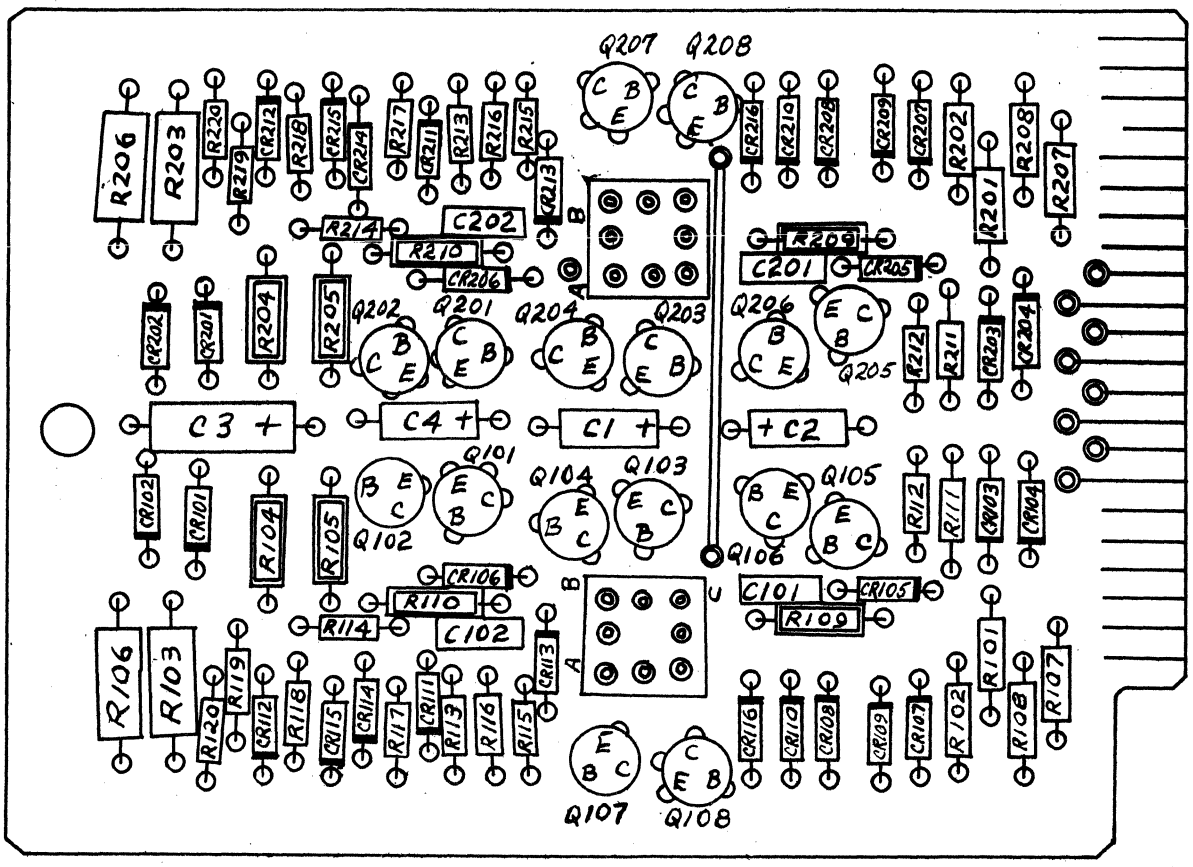
DWG NO. N12149 B



Input-A Card, Assembly 11931

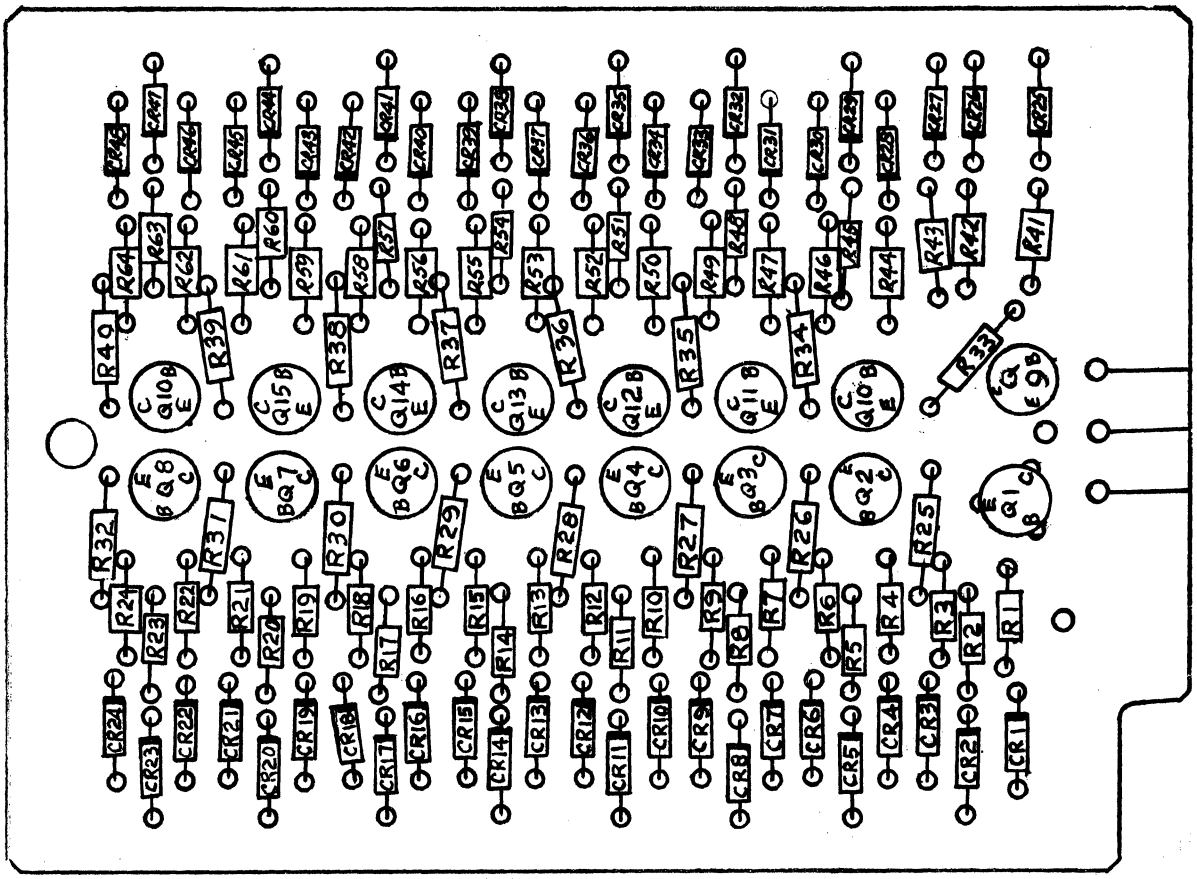


Timing-A Card, Assembly 11927

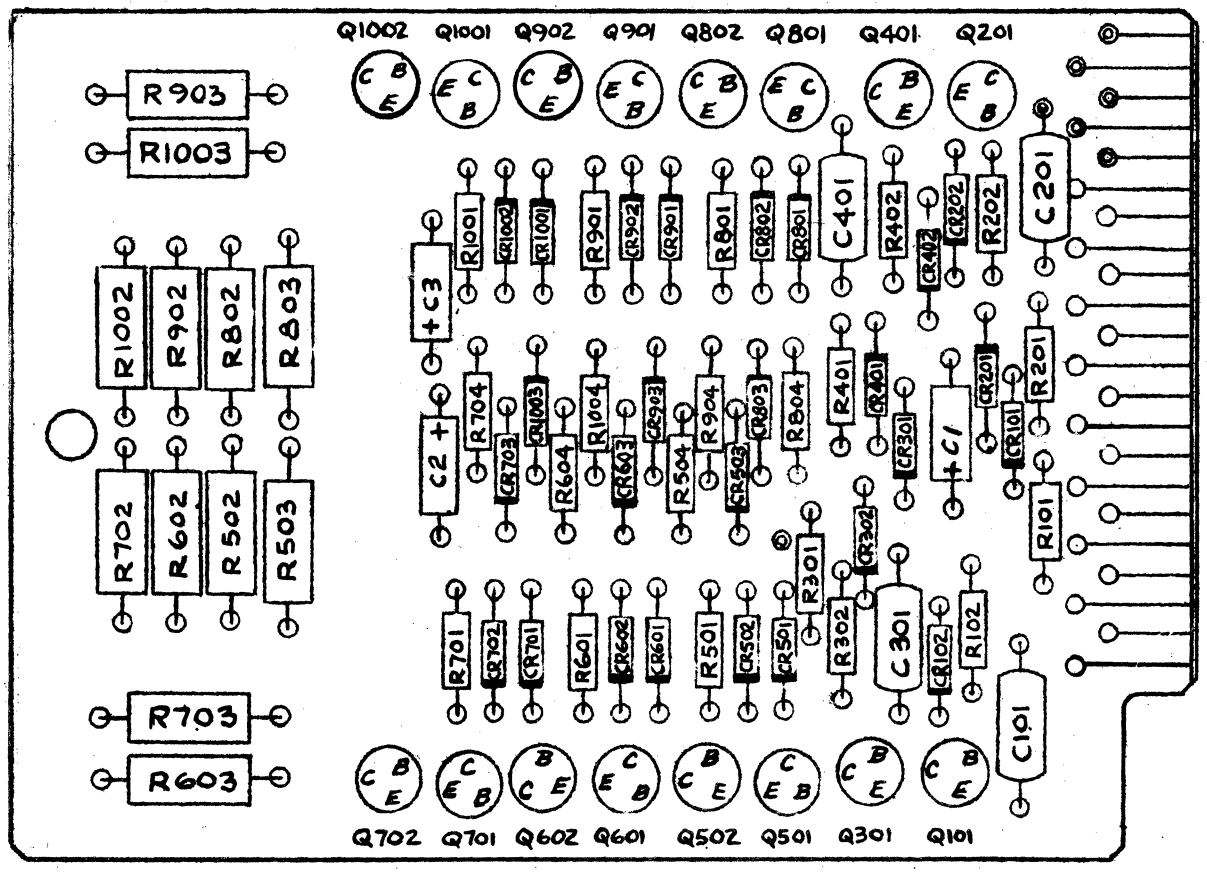


Register-A Card, Assembly 11921

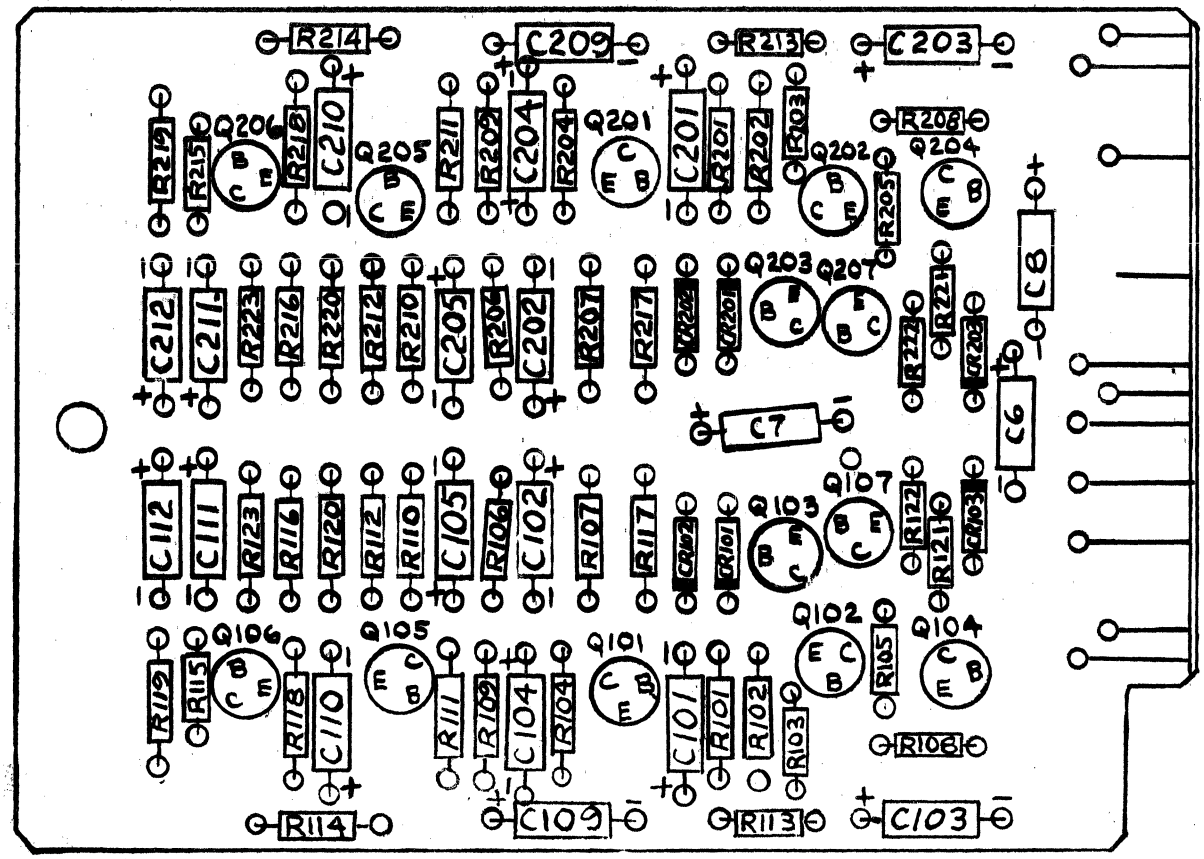
Transpose Register-A Card, Assembly 11925



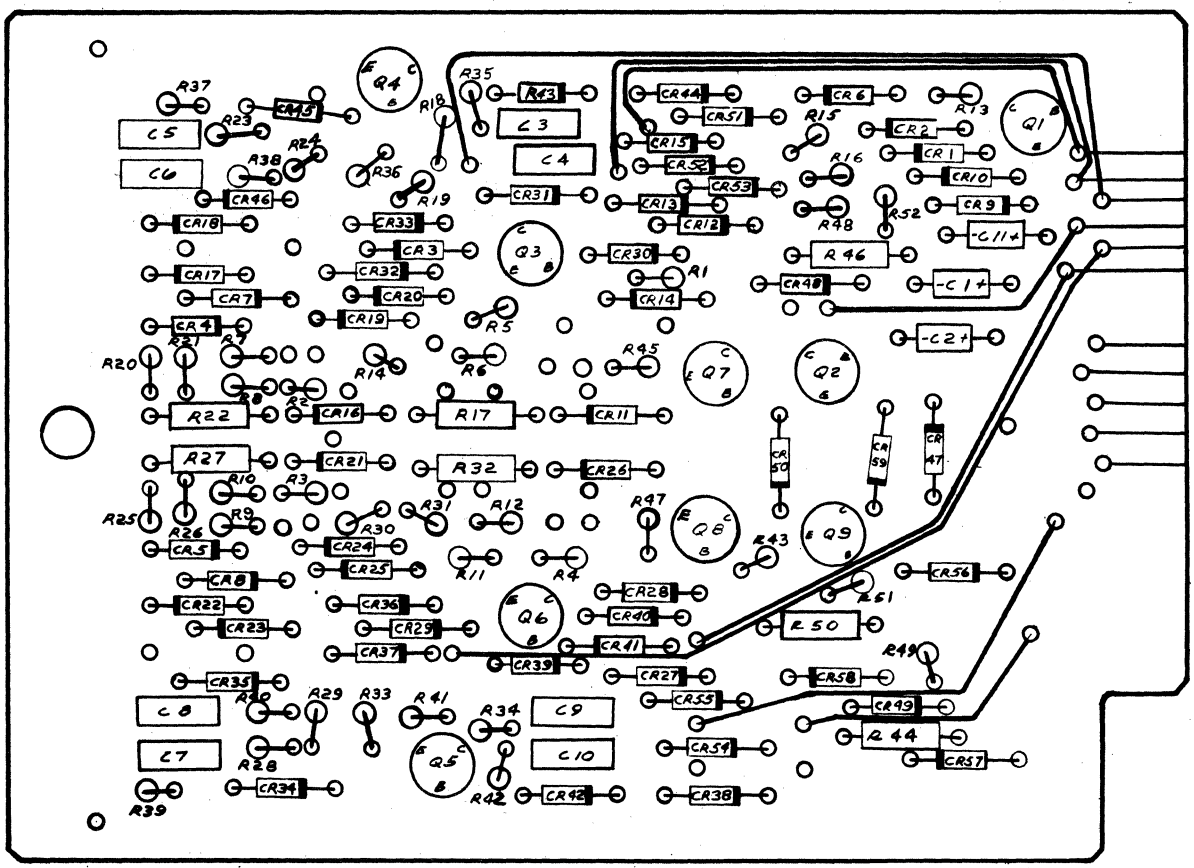
Switch-A Card, Assembly 11919



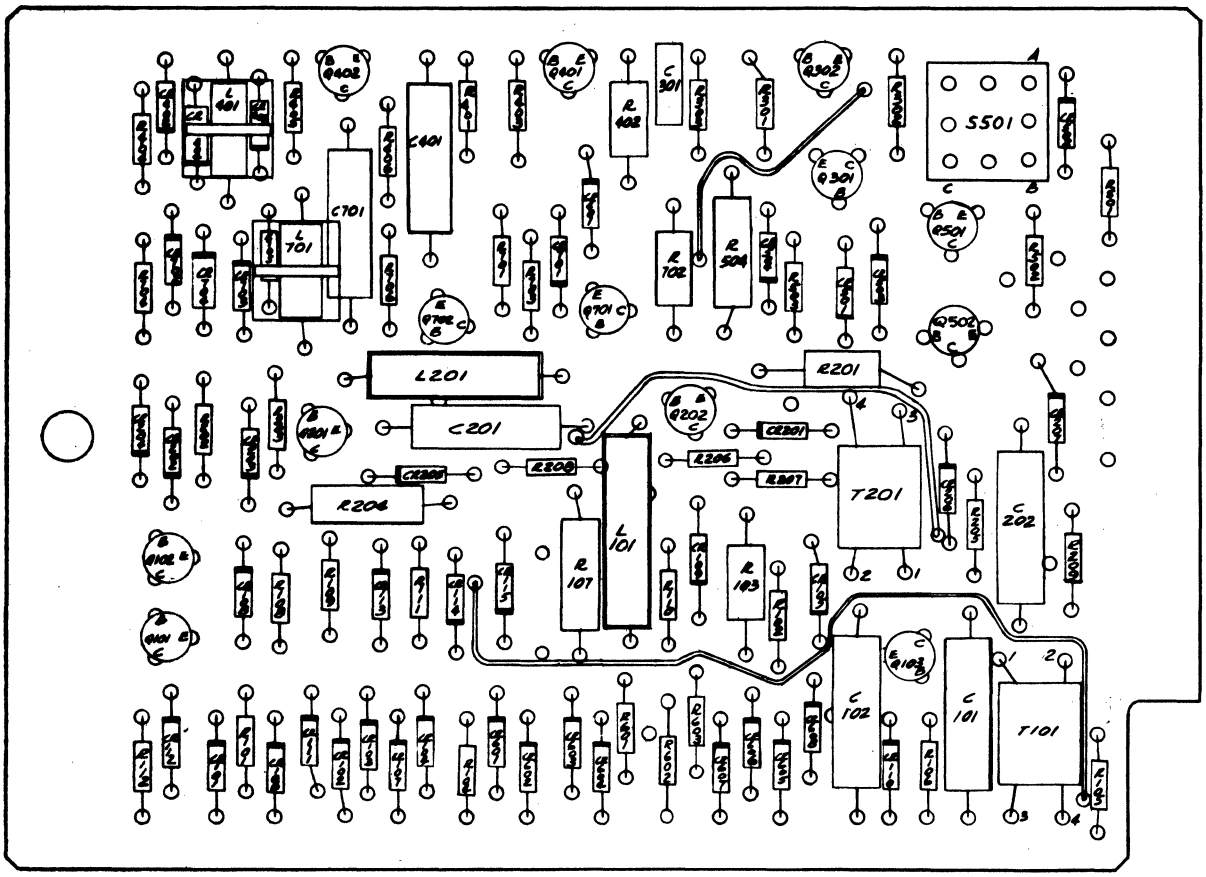
Inhibit-A Card, Assembly 11917



Read Amplifier-N Card, Assembly 12174



Count Logic-A Card, Assembly 11923



BQ Logic Card, Assembly 12196