TEXAS INSTRUMENTS

Improving Man's Effectiveness Through Electronics

Model 990/4 Computer

System Hardware Reference Manual

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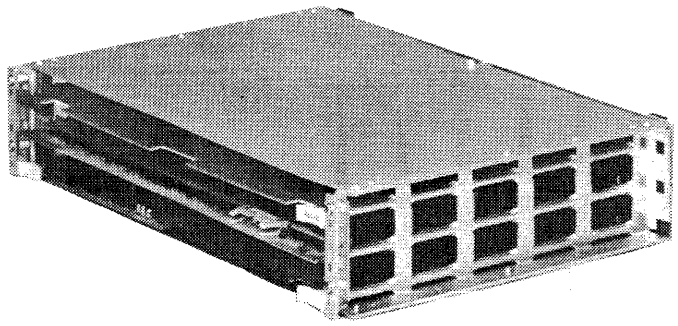

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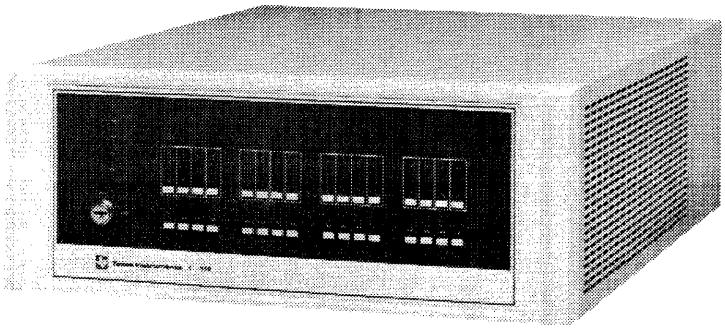

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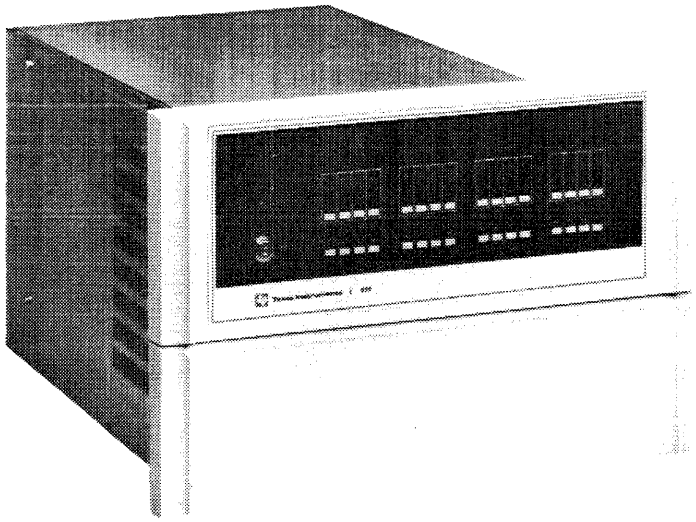

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Figure 1-1. Model 990/4 Microcomputer in Three Packaging Options

SECTION I

GENERAL DESCRIPTION

1.1 GENERAL

This manual provides operation and installation instructions for the Model 990/4 Microcomputer System manufactured by Texas Instruments Incorporated. The manual also provides sufficient hardware description to permit the user to modify existing logic boards or custom design new logic boards for special system applications.

This section provides a brief physical and functional description of the Model 990/4 Microcomputer System (figure 1-1) and describes the options available. For ease of reference, the Model 990/4 Microcomputer System is referred to as the 990/4 Microcomputer System or simply the 990/4.

1.2 PURPOSE OF EQUIPMENT

The 990/4 Microcomputer System is a low-cost, high-performance computer system constructed around the TMS 9900 16-bit microprocessor chip. The microcomputer system may be configured as a general-purpose computer with a wide range of supporting peripherals or it may be implemented as a special-purpose controller with a minimum configuration OEM chassis and limited set of peripherals.

1.3 HARDWARE DESCRIPTION

The 990/4 Microcomputer System consists of a main chassis (one of three optional types) and up to seven optional I/O expansion chassis for adding peripherals to the system when configuring large systems.

The main chassis in the 990/4 System consists of the following hardware units:

- 990/4 Microcomputer Board
- Chassis Assembly

} minimum configuration

- 990/4 Memory Expansion Board (optional)
- EPROM Memory Module (optional)
- CRU Expansion Board (optional)
- CRU Interface Board(s) (optional)

A simplified block diagram of the 990/4 System is shown in figure 1-2. The features and configurations of each unit in this figure are described in the following paragraphs.

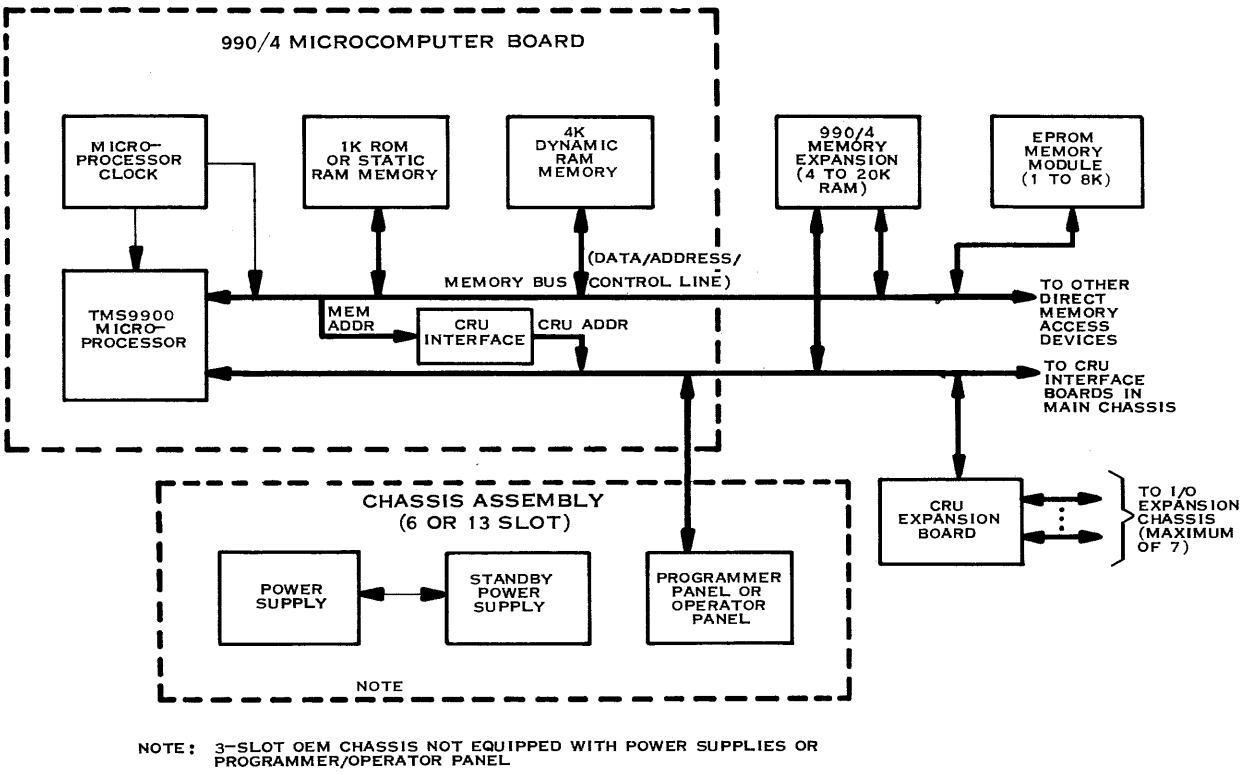


Figure 1-2. Model 990/4 Microcomputer System Block Diagram

1.3.1 **990/4 MICROCOMPUTER.** The 990/4 Microcomputer (figure 1-3) is a complete microcomputer on a single full-sized printed circuit board. The 990/4 Microcomputer includes the TMS 9900 microprocessor chip, supporting clock and interface logic plus two on-board memories. Some of the major features of the 990/4 Microcomputer board include:

- Up to 4K by 16-bit words of local on-board dynamic random access memory (RAM).
- Up to 1K by 16-bit words of local on-board read only memory (ROM) or static RAM.
- Microprocessor capability for direct accessibility of up to 32K by 16-bit words of memory.
- Communications register unit (CRU) serial I/O channel.
- Sixteen-Bit-Parallel I/O channel for communications with external memory or direct memory access controllers.
- Eight vectored interrupts plus provisions for real-time clock and power-up interrupts from power supply and memory interrupts from on-board and external RAM memories using optional error detect circuits.
- One CRU interface for the programmer panel (or operator panel).

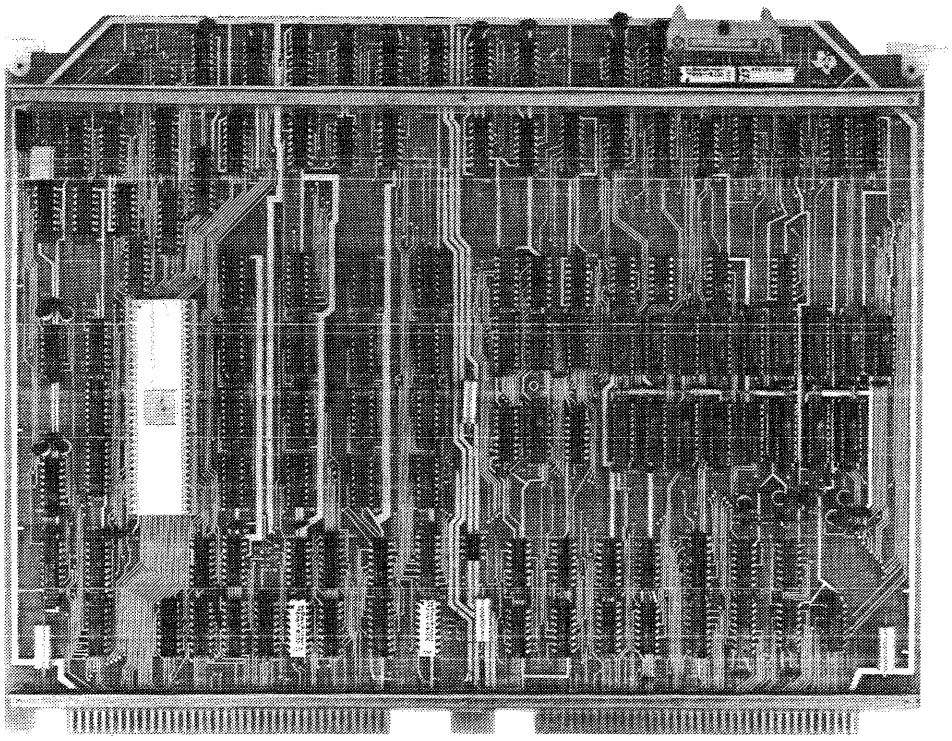


Figure 1-3. 990/4 Microcomputer Board

The special-purpose controller configuration of the 990/4 Microcomputer comes equipped with one bank of 256 by 16-bit words of static RAM. Four TMS 4043 (256 X 4) static RAM devices are mounted in four 16-pin sockets to form the 256-word bank of memory. Twelve additional 16-bit sockets are available to allow implementation of up to 768 words of either static RAM or PROM (programmable ROM) in 256-word increments. Each 256-word bank must be either all static RAM or all PROM. The PROM devices are SN74S287 256 by 4-bit programmable read only memory ICs.

The general-purpose computer configuration of the 990/4 Microcomputer is equipped with 4K by 16-bit words of MOS dynamic RAM. Sixteen TMS 4051 devices (4096 X 1) are required to provide the 4K words of memory. A seventeenth TMS 4051 is used in a factory-installed parity option for the dynamic RAM. This second configuration of the 990/4 Microcomputer board has sixteen 16-pin sockets for the addition of up to 1024 words of static RAM or ROM in 256-word increments. A third configuration of the microcomputer board is the same as the second configuration except that a set of eight ROMs are installed in eight of the memory sockets. These ROMs contain the on-board CPU basic diagnostics, bootstrap loader program and programmer panel software.

1.3.2 **CHASSIS ASSEMBLY.** The Model 990/4 Microcomputer System may be implemented in a 3-slot, 6-slot or 13-slot chassis assembly. The 6-slot and 13-slot chassis contain built-in power supplies, cooling fans, and either an operator panel or a programmer panel. The features and options available in each of the chassis assemblies are discussed in more detail in the following paragraphs.

1.3.2.1 **3-Slot OEM Chassis.** The low-cost 3-slot OEM chassis option consists of a 3-slot chassis assembly with a 3-slot chassis backpanel. In the 3-slot configuration, slot 1 of the backpanel is wired to accept the full-sized 990/4 Microcomputer printed circuit board and the other two slots are wired to accept two full-sized logic boards or four half-sized boards. However, the 3-slot OEM chassis is not equipped with built-in power supplies or cooling fans; the user must supply the computer with a source of regulated dc power and cooling air.

1.3.2.2 **6-Slot Chassis.** The 7-inch, 6-slot chassis consists of a chassis and backpanel which accommodates the 990/4 Microcomputer board in slot 1 (or CRU buffer board when used as an I/O expansion chassis), up to six full-sized logic boards, a built-in 20-ampere power supply, and either a programmer panel or an operator panel. The user may also select an optional standby power supply consisting of a standby power supply board (mounts on and connects to the 20-ampere power supply), a 12-volt battery and a chassis-mounted switch and fuse.

During normal operation, the standby power supply board maintains a trickle charge on the battery and develops the regulated dc voltages used in the semiconductor memory circuits. During a power-failure condition, the board automatically switches to battery operation to preserve data in the semiconductor memory.

The backpanel of the 6-slot chassis is wired to accept the 990/4 Microcomputer in slot 1; the other five slots are wired to accept five full-sized logic boards or as many as 10 half-sized logic boards. An air filter and fans provide filtered air cooling for the power supplies and circuit cards mounted in the chassis.

1.3.2.3 **13-Slot Chassis.** The 12-inch, 13-slot chassis is an enlarged version of the 6-slot chassis that accommodates a greater number of logic boards. The 13-slot chassis is used both as a main chassis for the microcomputer and as an I/O expansion chassis for CRU-type devices only (all DMA devices must be implemented in main chassis). The 13-slot chassis assembly consists of a chassis backpanel with slots for 13 full-sized logic boards, a 40-ampere power supply, and either a programmer panel or an operator panel. The standby power supply is also available with the 13-slot chassis. The backpanel is wired to accept the 990/4 Microcomputer board (or CRU buffer card when used as an expansion chassis) in slot 1 and the remaining 12 slots are wired to accept 12 full-sized logic boards or as many as 24 half-sized logic boards.

1.3.3 **990/4 MEMORY EXPANSION BOARD.** The optional memory expansion board (module) is a full-sized, double-sided, 160-pin printed circuit board that installs in one of the chassis slots of the main chassis other than slot 1. The interconnections between the expansion board and the memory and CRU buses on the 990/4 Microcomputer board are accomplished through etch wiring on the chassis backplane. When fully implemented, the memory expansion board provides 20K words of dynamic random access memory (RAM) storage. The board is also available in memory sizes ranging from 4K to 20K in 4K increments. However, the memory size is set up at the time of manufacture and is not alterable in the field. Each 4096-word increment uses 16 Texas Instruments TMS 4050 integrated circuit devices. Each of the 16 TMS 4050s is a high-speed dynamic 4096-bit MOS circuit organized as 4096 one-bit words. As another option, odd parity may be factory-implemented by installing a seventeenth TMS 4050 for each 4K words of memory storage and installing two parity generator/checker ICs on the board. Data is preserved in the dynamic MOS memory storage cells on the board by performing a memory refresh cycle at each of 64 row addresses every two milliseconds.

The expansion memory module is addressed in a block of consecutive addresses with the start address set for zero or any 4K work boundary in the memory address space. The start address is selected via switches on the board, and the upper limit address is indicated by module-sized jumper wires. The expansion memory is electrically connected to the memory bus in the main chassis and may be accessed for read and write operations by either the TMS 9900 Microprocessor or by a direct memory access controller (installed in the main chassis only). A memory protect option adds the capability to define a write protect zone in memory. The boundaries of the protected zone are programmable in 256-word increments. The protected zone is defined by two 7-bit registers that are addressed through a CRU interface with the 990/4 Microcomputer board. The protect function may be disabled under program control without altering contents of the boundary registers. An attempt to write to protected memory results in a setting of a software-readable Protect Violation flag that may be wired (optionally) to any unused interrupt level.

1.3.4 **EPROM MEMORY MODULE.** The EPROM (Erasable, Programmable Read Only Memory) module is an optional memory board equipped with IC sockets and associated addressing and control logic to accommodate from 1K to 8K of field expandable memory. The EPROM memory is currently implemented with INTEL 2708 1024 by 4-bit EPROM ICs. The EPROM board may be used in either a 990/4 or 990/10 System simply by connecting the correct set of jumper wires corresponding to the computer type.

The EPROM memory is also addressed in a block of consecutive addresses with the start address set to zero or any 1K boundary in the 990/4's 32K address space.

1.3.5 **CRU INTERFACE BOARDS.** The main chassis may optionally contain a number of CRU interface boards to provide an interface between the computer's serially oriented CRU bus and each of the parallel-data oriented peripherals in the system. CRU boards are available for all standard peripherals such as card readers, video display terminals, teleprinters and other similar devices. In addition, 16 I/O data modules are available which provide a general-purpose 16-bit input and output interface between the CRU and any device requiring EIA or TTL levels at its interface. Section III of this manual provides sufficient CRU interface card design data to permit a user to custom-build a new CRU interface card or modify any existing card to accommodate any specific requirements not met by the line of CRU interface cards presently being manufactured by Texas Instruments.

1.3.6 **CRU EXPANSION BOARD.** The CRU expansion board is an optional plug-in module used in the main chassis to expand the CRU interface signals present at the chassis backpanel to drive up to seven expansion chassis. Each of seven connectors on the CRU expansion board may be cabled to an associated connector on the CRU buffer board located in slot 1 of each expansion chassis.

The CRU expansion board also contains provisions for monitoring the interrupt lines from chassis 1 through 4 (designated Section A) and chassis 5 through 7 (Section B). The board then issues either an A or B interrupt to the computer indicating the chassis group in which the interrupt occurred. The CRU expansion board also develops and provides temporary storage for a 16-bit interrupt vector which may be read under software control to determine the source of the interrupt. In addition to the above described interrupt scheme, the CRU expansion board also fans in direct interrupt lines from all seven chassis and issues an interrupt to the microcomputer if a direct interrupt is detected from any board in any of the seven expansion chassis. The direct interrupt feature is used to permit more rapid interrupt recognition for those peripherals in the expansion chassis that require a faster interrupt response than is available through the scanner method.

SECTION II

INSTALLATION AND OPERATION

2.1 GENERAL

This section provides information and procedures for unpacking the computer from its shipping container, installing it in either a tabletop or a rackmounted configuration, and checking the operation of the newly installed computer system. The section also includes a procedure for modifying the interrupt structure of the computer and verifying that the proper jumper wire options have been installed. The procedures assume that the user has a fundamental knowledge of basic handtools and cabling techniques, but they do not require a detailed understanding of computer hardware or software. This section does not cover installation of any of the peripheral devices that may accompany the computer shipment. Installation instructions for those devices are included in the Installation and Operation manual that is shipped with each peripheral device. To aid in planning to meet the installation requirements for the computer, table 2-1 summarizes the specifications and requirements of the available chassis for the computer.

2.2 UNPACKING/PACKING (6- AND 13-SLOT CHASSIS)

The computer is shipped in a corrugated cardboard container together with the circuit boards and interconnecting cables required to install the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. After completion of the preliminary inspection, perform the following steps to remove the computer from its container and ready it for operation. Figure 2-1 illustrates the required steps.

NOTE

Save shipping carton, shipping brackets and all packing materials for use in reshipment of the unit.

1. Position container so that the address label is right-side up.

2. Open top of container, and remove cushioning material from corners.

NOTE

If the computer has the tabletop enclosure (6-slot chassis only), no foam block is required to secure circuit boards in chassis.

3. Remove cardboard inner sleeve and foam block (rackmount configurations) from shipping container.

WARNING

Use proper lifting techniques to avoid backstrain when lifting computer chassis.

4. Remove computer and attached shipping pallet from container. When lifting assembly, lift from under the assembly to avoid undue strain on the chassis assembly.

Table 2-1. Computer Chassis Specifications

Characteristic	6-Slot Chassis	13-Slot Chassis	3-Slot (OEM) Chassis
Height	7 inches (17.8 cm)	12-¼ inches (31.1 cm)	4-13/16 inches (12.2 cm)
Width	16-½ inches (41.9 cm)	16-½ inches (41.9 cm)	11-7/8 inches (30.2 cm)
Depth	23 inches (58.4 cm)	23 inches (58.4 cm)	15-¾ inches (40.1 cm)
Ambient Temperature			
Operating[1]	32° to 122° F (0° to 50° C)	32° to 122° F (0° to 50° C)	32° to 122° F (0° to 50° C)
with Low Speed Fan	32° to 95° F (0° to 35° C)	32° to 95° F (0° to 35° C)	Does not apply
Storage	-40° to +158° F (-40° to +70° C)	-40° to 158° F (-40° to +70° C)	-40° to +158°F (-40° to +70° C)
Humidity[2]	0% to 95%	0% to 95%	0% to 95%
Altitude	0 to 10,000 feet (0 to 3.05 km)	0 to 10,000 feet (0 to 3.05 km)	0 to 10,000 feet (0 to 3.05 km)
Heat Load			
Full Card Slot	50 watts	50 watts	50 watts[3]
Power Supply	170 watts	170 watts	170 watts[3]
Exhaust Temperature	149° F (maximum) (65° C)	149° F (maximum) (65° C)	149° F (maximum) (65° C)
External Power Requirements			
Standard	115 Vac ± 10% 3-wire service (hot, neutral, gnd)	115 Vac ± 10% 3-wire service (hot, neutral, gnd)	-5 Vdc ±6% +5 Vdc ±3% ±12 Vdc ±3% Ground
Optional	100, 200 or 230 Vac ± 10% 3-wire service (hot, neutral, gnd)	100, 200 or 230 Vac ± 10% 3-wire service (hot, neutral, gnd)	Does not apply

Notes:

1. Lower the upper operating limit by 3.6° F (2° C) for every 2500 feet (762 meters) increase in altitude.
2. No condensation should be allowed.
3. Cooling capacity attainable only when externally supplied with a 600 feet/minute ambient air flow.

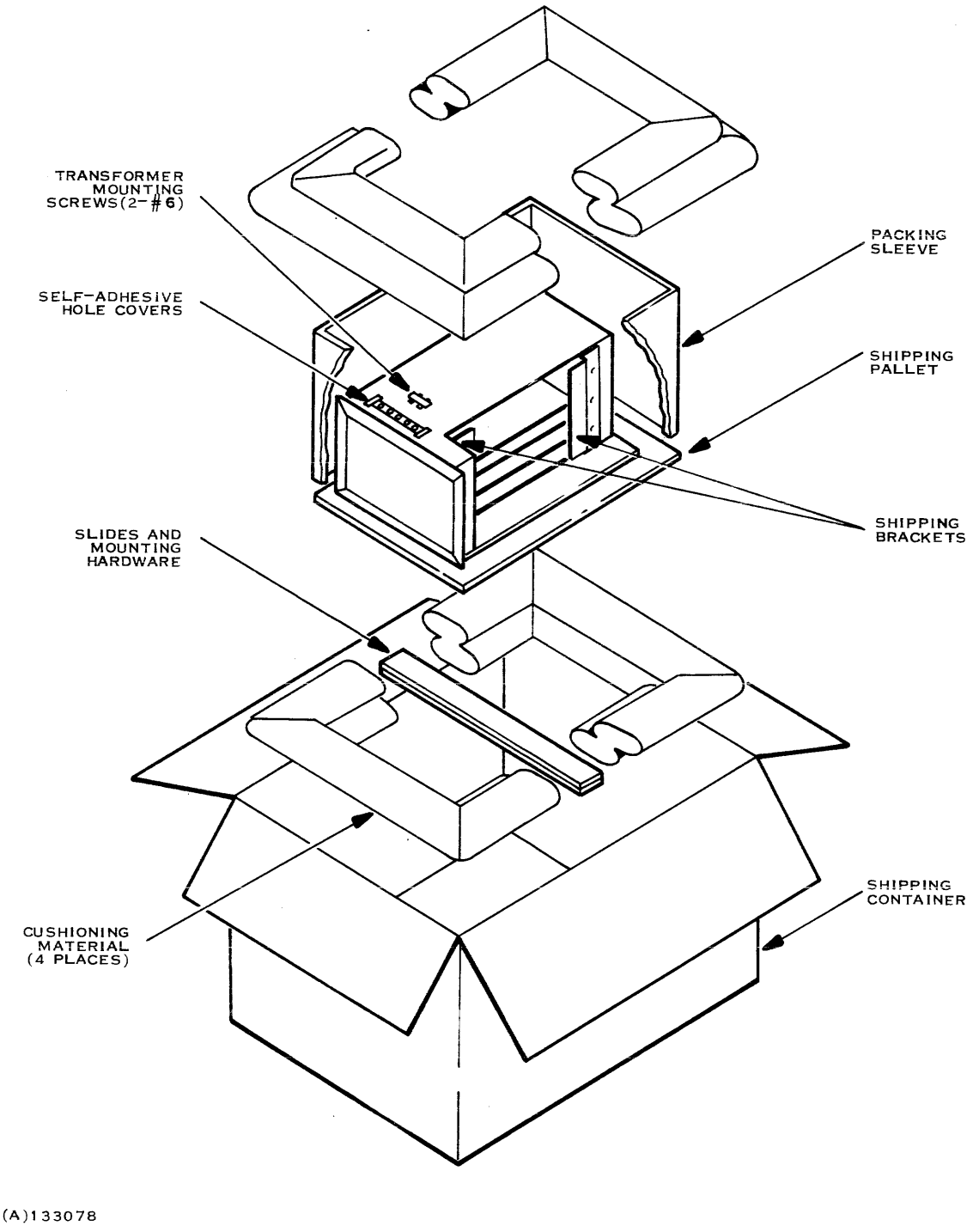


Figure 2-1. Computer Shipping Packaging

CAUTION

To prevent the mounting screws on the underside of the shipping pallet from scratching table surface, place a shielding material (the packing sleeve removed in step 3 makes an excellent shield) on the table before setting the assembly on the table.

5. Place the removed assembly on a convenient, protected work surface.

NOTE

For rackmount configurations, the slides are packed in the bottom of the shipping container.

6. Remove rackmount slides (if present) and interface cables from bottom of shipping container.

CAUTION

In following steps, do not allow the unit to overhang the work surface so far that it will fall off the surface.

7. Position computer and shipping pallet assembly so that front edge of assembly overhangs edge of work surface to reveal two (2) #10 mounting screws that secure computer to shipping pallet. See figure 2-2 for location of all mounting screws.

8. Use a straight blade screwdriver to remove two screws and their associated washers and lock washers. Save screws and washers for reshipment.

9. Reposition computer and shipping pallet assembly so that rear edge of assembly overhangs the edge of work surface to reveal three (3) #10 mounting screws that secure computer to shipping pallet.

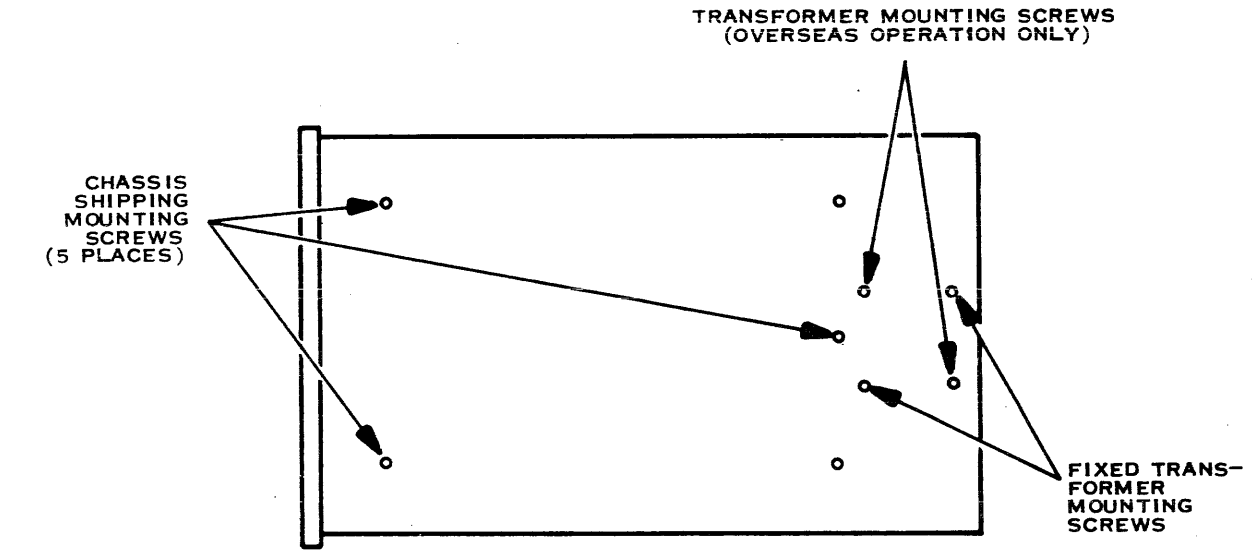
10. Remove the three screws, washers and lock washers and save for reshipment.

NOTE

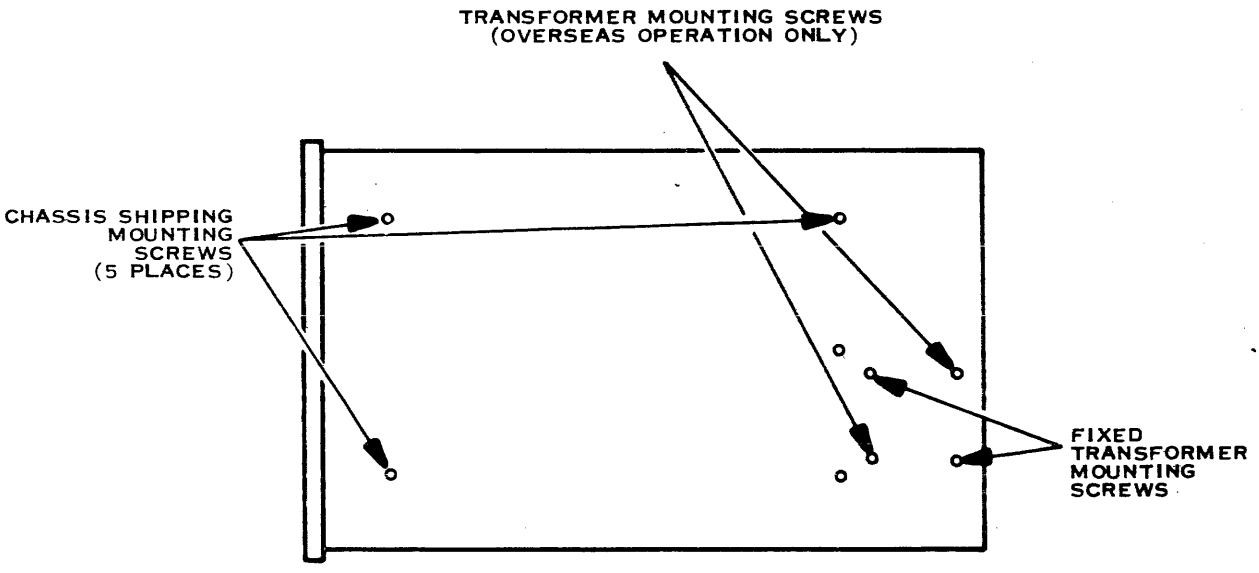
If the computer was ordered for overseas operation, two (2) additional mounting screws are visible on the underside of shipping pallet. If these screws are not included on the unit being installed, skip step 11.

11. Remove two (2) #6 transformer mounting screws and their associated washers and lock washers, and save for reshipment.

12. Lift computer chassis from shipping pallet and place it on work surface such that the rear of unit overhangs work surface to reveal holes for previously removed mounting screws.



(A) 6-SLOT AND TABLE TOP CHASSIS BOTTOM VIEW



(B) 13-SLOT CHASSIS BOTTOM VIEW

(A)133079

Figure 2-2. Location of Chassis Shipping Pallet Mounting Screws

NOTE

If unit being installed did not have the two #6 mounting screws (see step 11), skip step 13 and proceed to step 14.

13. Remove two (2) #6 screws taped to top of computer chassis and insert them in holes vacated by two #6 mounting screws removed in step 11. Tighten two new screws to secure transformer to chassis.

14. Remove strip of self-adhesive hole covers that are taped to top of computer chassis. Use three of the hole covers to cover three mounting screw holes along the rear of chassis.

15. Reposition computer chassis such that front edge overhangs work surface to reveal the mounting holes for front mounting screws.

16. Use remaining two (2) self-adhesive hole covers to cover front mounting screw holes.

17. Set computer chassis in a safe position on work surface to continue with remaining portions of installation procedure.

18. Pack all shipping materials into original shipping container and store container for use in reshipment of unit.

19. Inspect computer chassis (and included components) for signs of damage that may have occurred during shipment. If damage has occurred, notify the carrier immediately.

To repack the unit, reverse above procedure using original packing material.

2.3 UNPACKING/PACKING (OEM CHASSIS)

The OEM chassis is shipped in a corrugated cardboard container together with the circuit boards and mounting hardware for the system. Upon receipt of the container, inspect to ensure that no signs of physical damage are present. After completion of the preliminary inspection, perform the following steps to remove the chassis from its container. Figure 2-3 illustrates the material included in the packing container.

NOTE

Save shipping carton and all packing materials for use in reshipment of the unit.

1. Position container so that address label is right-side up.

2. Open top of container and remove chassis assembly enclosed in cushion wrap.

3. Remove cushion wrap from chassis assembly.

4. Remove bag containing mounting hardware from chassis assembly.

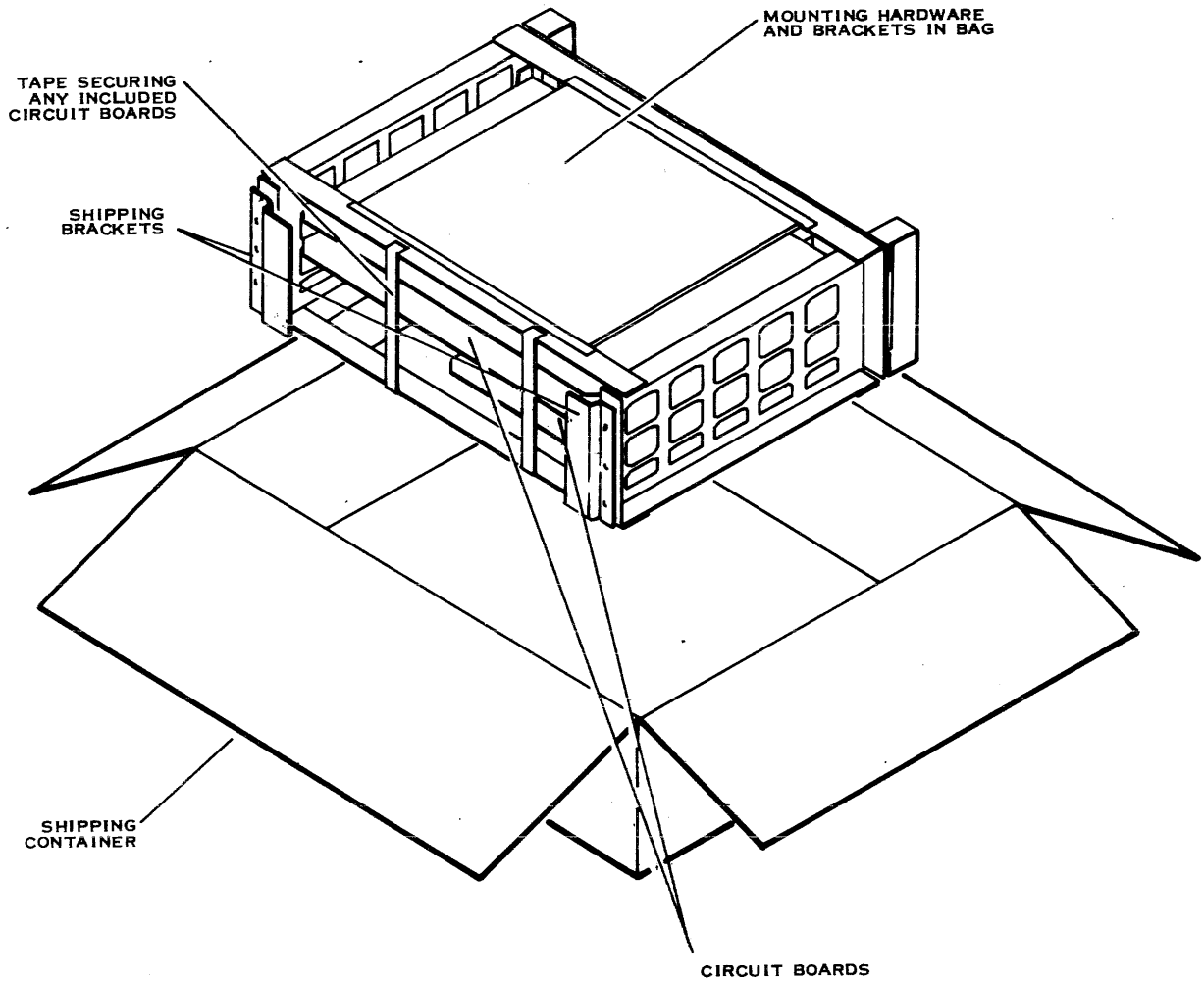


Figure 2-3. OEM Chassis Shipping Packaging

NOTE

If circuit boards are included in shipment, they are secured in place by shipping brackets. If no circuit boards are included, skip step 5.

5. Remove shipping brackets that secure circuit boards in chassis and save for use in reshipment of the unit.

6. Inspect the chassis and all included components for signs of damage that may have occurred during shipment. If damage has occurred, notify carrier immediately.

2.4 INSTALLATION (TABLETOP CHASSIS)

The tabletop chassis is a 6-slot chassis configuration contained in an attractive enclosure. The unit is shipped fully assembled to ensure that all components arrive safely. However, before operating the computer the enclosure must be removed to connect the computer to the system peripheral devices. The following procedure describes the steps required to completely integrate the new computer into its operating environment.

1. Set unpacked chassis assembly in the approximate installation position.

NOTE

The chassis enclosure is secured to the chassis by three (3) oval-head screws on each side of the chassis and one (1) oval-head screw at the rear of the assembly as illustrated in figure 2-4.

2. Remove seven (7) oval-head screws and their associated finishing washers that secure the chassis enclosure to the chassis. Save screws and washers for reinstallation of enclosure.

3. Carefully lift enclosure up from the chassis and set enclosure in a safe place. Remove the shipping brackets that hold the logic boards in place and save for reuse at a later date.

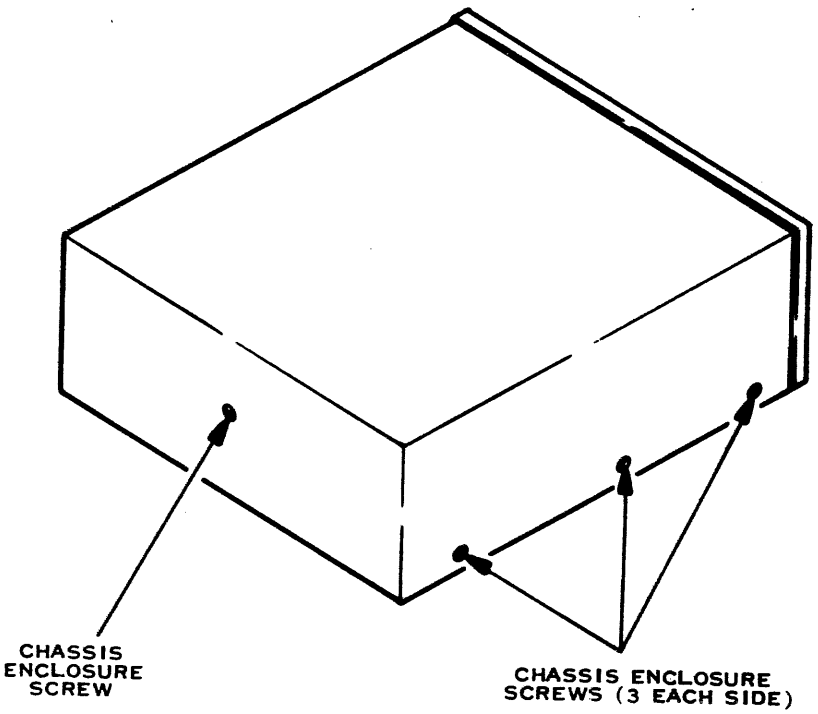


Figure 2-4. Location of Chassis Enclosure Screws

NOTE

The chassis is shipped from the factory with interrupts installed in predetermined locations as illustrated in figure 2-5. CRU addresses are fixed and cannot be changed.

4. Determine chassis location and interrupt assignments for each peripheral interface in system. If interrupt assignments do not match the factory-installed interrupts, or if additional interrupt assignments are required, perform Interrupt Installation procedure in this section of manual.

5. Remove the interface modules, memory boards and processor boards from the chassis one at a time, and refer to the Circuit Board Jumper Modifications paragraph near the end of this section to verify that all jumper wires are properly installed. Return boards to original slots.

6. Install peripheral device interface cables on proper interface module in computer chassis as described in Installation and Operation manual included with peripheral device. All interface cables should be routed through cable clamps at rear of chassis and should exit at rear of chassis.

7. Connect ac power cord to a source of ac power with specifications applicable to equipment being installed.

8. Turn key switch on front panel to ON (or UNLOCK) position. Observe that POWER indicator (and the RUN indicator) on front panel light and that fans operate.

9. Perform System Checkout procedure specified later in this section of manual.

SLOT NO.	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 AU	N/A	N/A	990/4 AU	N/A
2	0120	MEMORY EXPANSION OR SPARE	N/A	0100	MEMORY EXPANSION OR SPARE	N/A
3	00E0	913A VDT NO. 1	3	00C0	913A VDT NO. 1	3
4	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
5	0060	SPARE	N/A	0040	CARD READER	4
6	0020	PROM PROGRAMMER	NOT USED	0000	733 ASR/KSR	6

(A) 6-SLOT PREWIRED CHASSIS

(A)133082

Figure 2-5. 6-Slot Chassis Prewired Configuration

10. Slip chassis enclosure over chassis and align it so that it mates properly with front panel and mounting-screw holes.

11. Secure chassis enclosure to chassis using seven oval-head screws and finishing washers removed in step 2.

12. Position computer in final installation site.

13. Perform system software installation procedures for operating system to be used with computer. For Texas Instruments supplied software, this information is provided in System Operation Guide for specific software package.

2.5 INSTALLATION (RACKMOUNT CHASSIS)

Either the 6-slot or the 13-slot chassis can be ordered for mounting in a 19-inch equipment rack. The chassis is shipped with all circuit boards installed in chassis; the rackmounting hardware is packed in same carton as chassis. After performing the unpacking procedure, perform following steps to install the computer in rack:

NOTE

The following procedure requires access to the rear of installation rack after computer chassis is mounted in rack.

1. Set unpacked chassis assembly on a convenient work surface near equipment rack in which computer will be installed.

WARNING

Ensure that the power cord is not connected to a source of ac power before continuing with procedure. Failure to observe this precaution could result in severe electrical shock.

2. Remove six (6) screws that secure air filter and rear access plate to rear of chassis. It is not necessary to remove air filter from access plate.

3. Install two clip nuts in predrilled holes in chassis as illustrated in figure 2-6.

4. Reinstall rear access cover/air filter assembly using the six mounting screws removed in step 2.

5. Inspect the front and rear mounting supports in the rack (or desk) to ensure that distance between front and rear supports is 24-1/4 inches ± 1/4 inch (61.6 cm ± 0.6 cm) as illustrated in figure 2-7.

6. Determine desired vertical position of bottom edge of computer front panel. When using an EIA standard vertical support, the bottom edge of front panel must be centered between two holes that are 0.5 inch (1.27 cm) apart as illustrated in figure 2-8. Using that figure, locate position of two slide mounting holes on each of four mounting supports. These holes are 0.65 inch (1.65 cm) and 1.275 inches (3.24 cm) above the bottom edge of front panel.

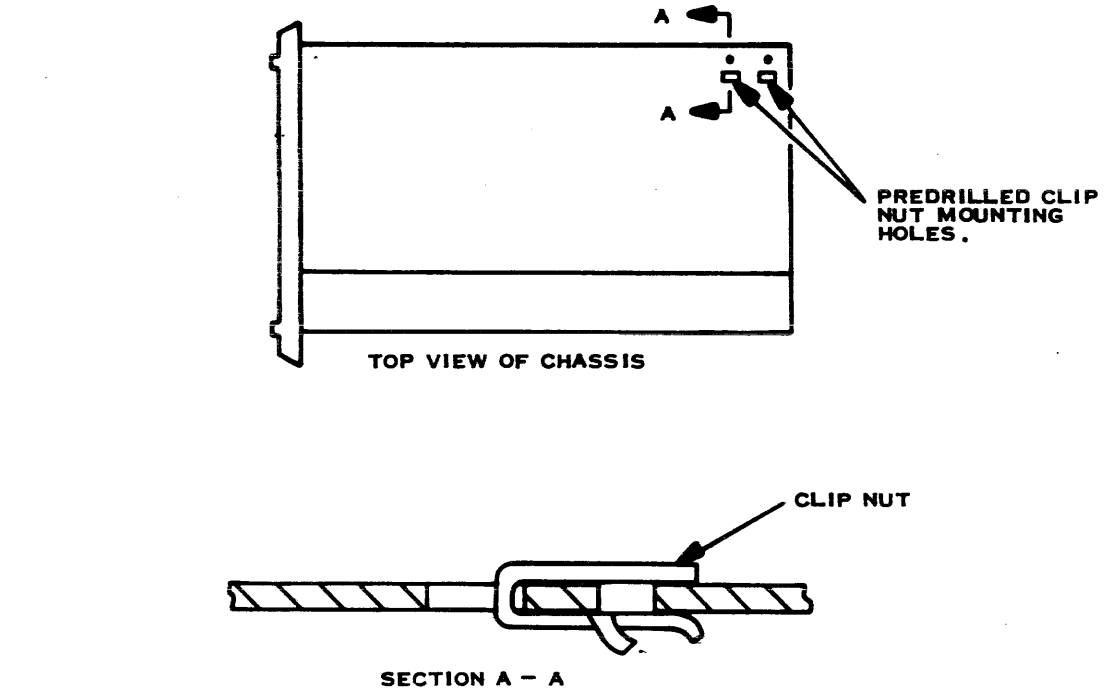


Figure 2-6. Clip Nut Installation

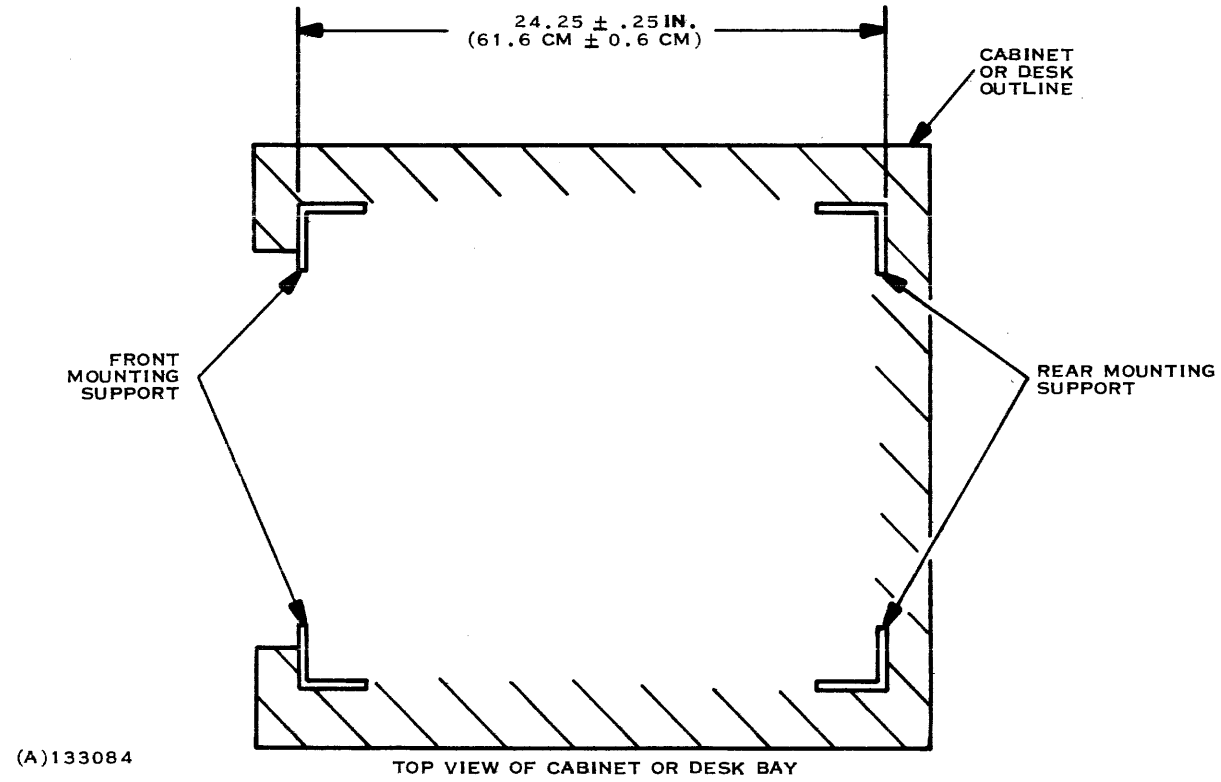


Figure 2-7. Mounting Cabinet Depth Specification

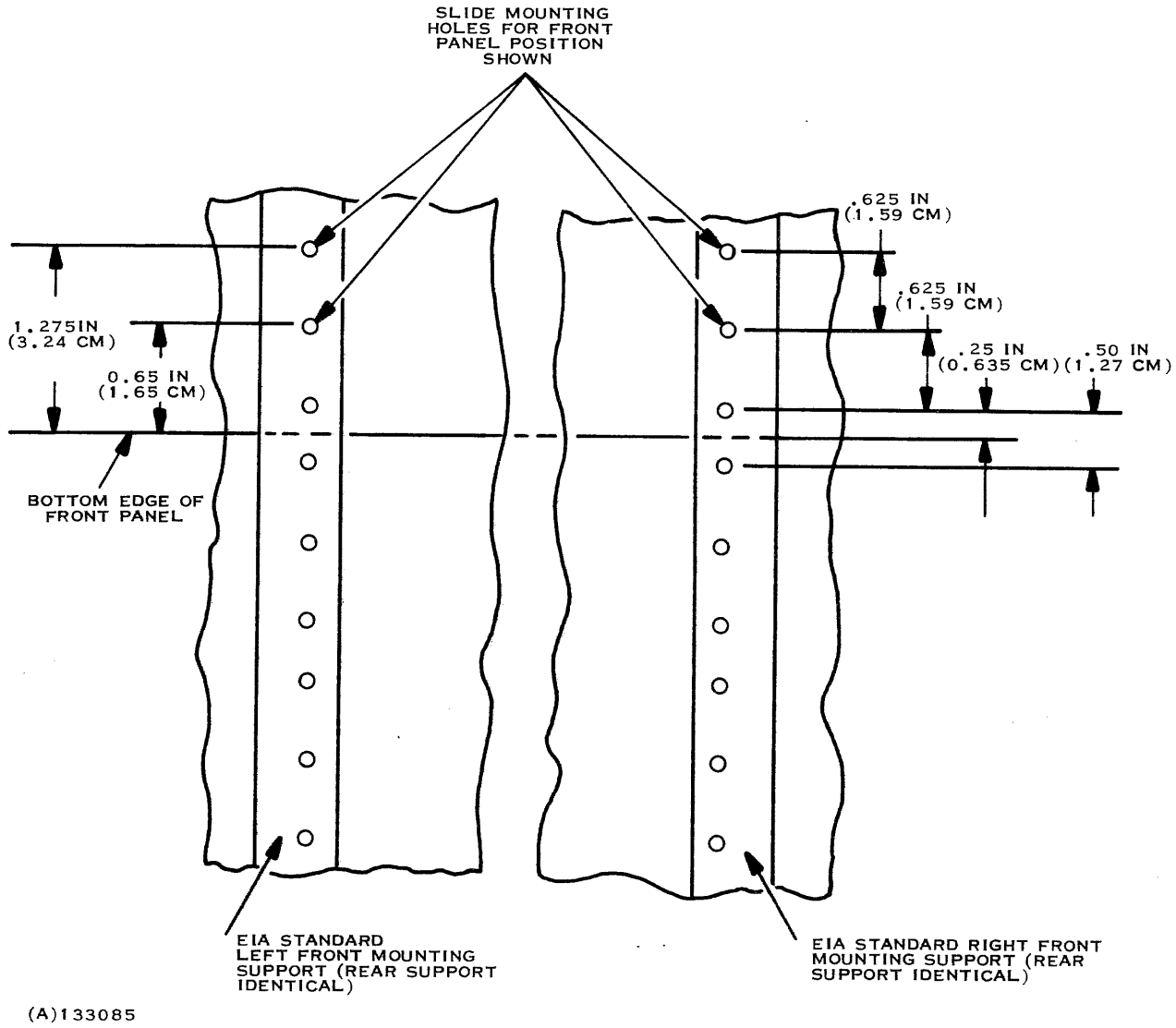


Figure 2-8. Mounting Hole Positioning

7. Loosely install eight (8) 10-32 X 1/4 mounting screws and their associated flat washers and lock washers in eight selected holes in mounting supports (front and rear). Screws are installed from inside of enclosure as illustrated in figure 2-9.

8. Loosely assemble rear mounting brackets to slides using hardware provided with slides. Finger tighten rear mounting bracket screws.

9. Position left side against front and rear mounting supports such that slide mounting brackets fit between washers of mounting screws and mounting supports. Finger tighten four mounting screws to hold slide in place.

10. Adjust slide so that distance from center of cabinet mounting screws to innermost point of slide assembly is 1-1/2 inches (3.91 cm) as illustrated in figure 2-10.

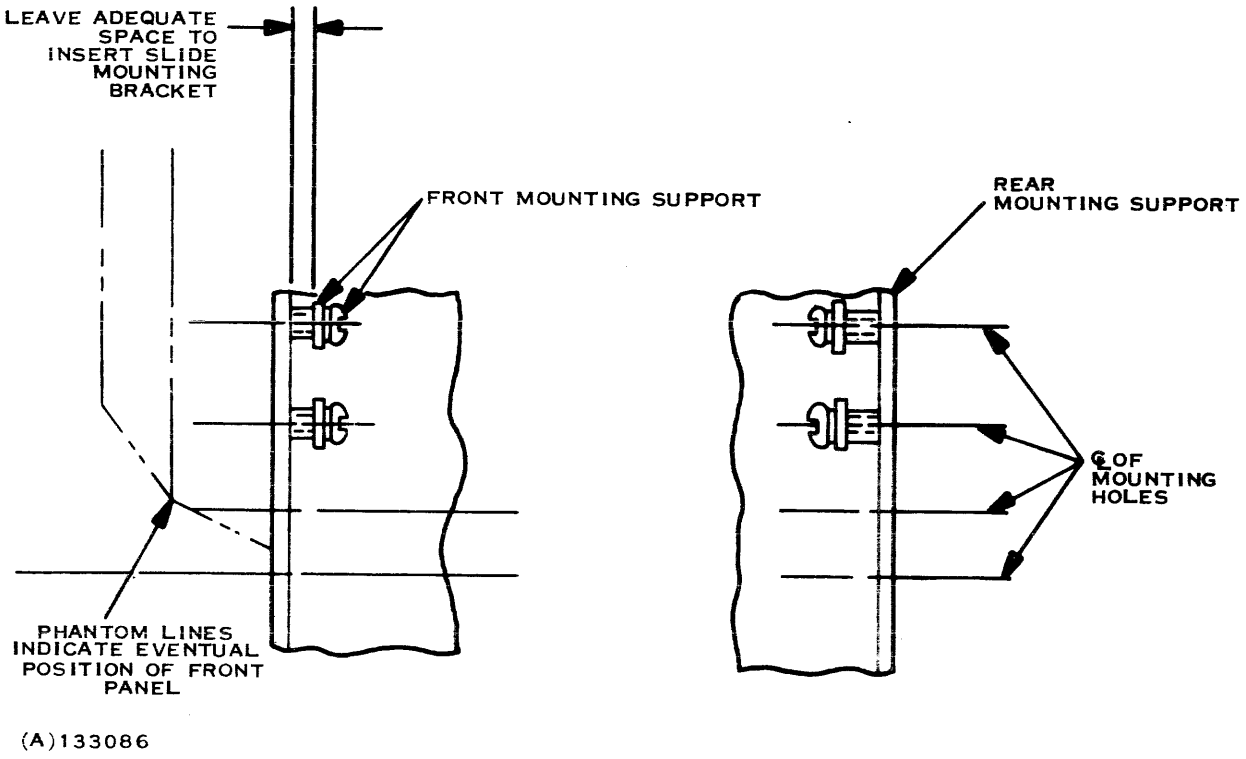


Figure 2-9. Mounting Screw Installation

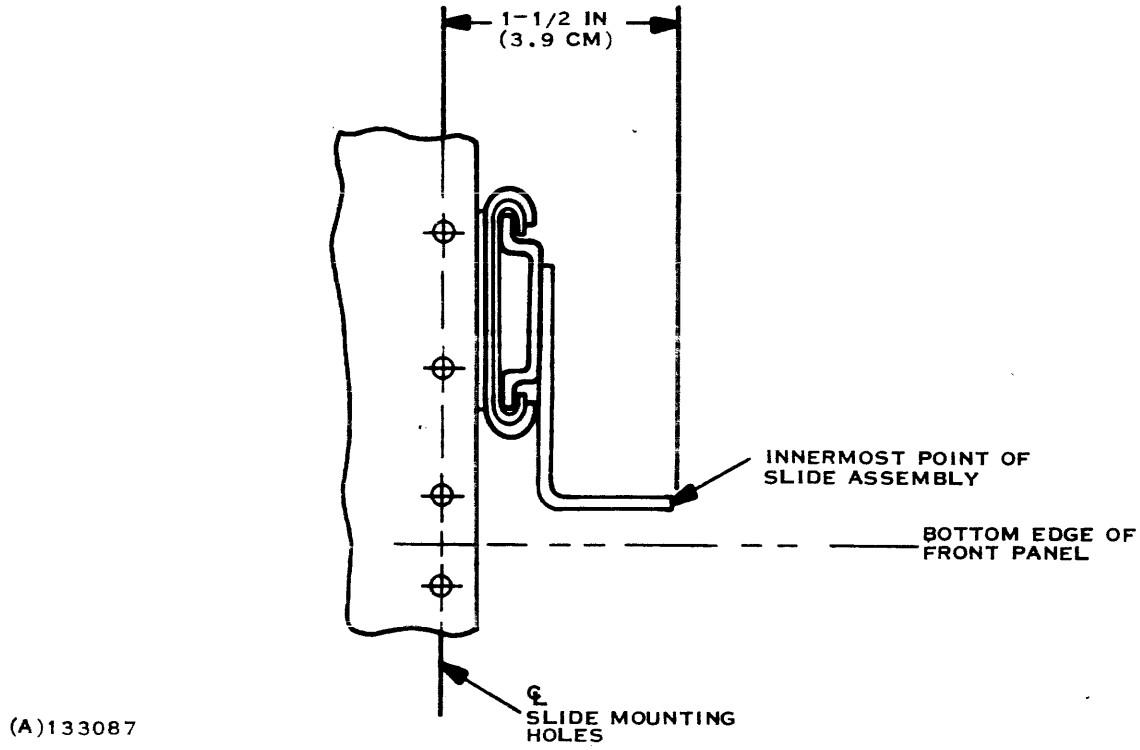


Figure 2-10. Chassis Slide Positioning

11. Ensure that slide assembly is square with cabinet mounting supports and tighten four (4) slide mounting screws and rear bracket mounting screws.

12. Repeat steps 9 through 11 with right slide.

13. Extend both slides and release disconnect mechanism to remove inner slide member from slide assemblies.

14. Attach inner slide members to left and right underside of computer chassis using 6-32 X 1/4 self-tapping screws. Do not overtighten screws.

15. Mount ball stud to ball stud carrier bar using a 6-32 nut and lock washer as illustrated in figure 2-11.

16. Loosely install ball stud carrier bar to top of computer chassis using 6-20 screws and flat washers inserted into clip nuts installed in chassis in step 3.

17. Insert chassis into mounted slides and reseat the disconnect mechanism. Push chassis into rack. During last inch of travel, lift front of chassis to ensure correct slide mating.

18. Assemble ball stud receptacle to stop plate using mounting hardware provided.

19. Install stop plate assembly to back edge of left rear mounting support of cabinet at a height such that ball stud receptacle mates with ball stud of the computer chassis.

20. Adjust forward-backward position of ball stud carrier bar on computer chassis such that chassis stops and ball stud latches into receptacle when back of front panel is between 1/32 inch to 1/16 inch (0.8 cm to 0.16 cm) from front mounting support of cabinet.

21. Slide computer chassis in and out of cabinet several times to ensure smooth operation and good alignment of all parts. Readjust as required.

22. Connect power cord from back of computer chassis to ac power distribution system of cabinet. Do not apply power at this time.

23. Slide chassis out from the cabinet to expose circuit boards mounted within the computer chassis. Remove shipping brackets that hold logic boards in place.

NOTE

The chassis is shipped from factory with interrupts installed in predetermined locations. Figure 2-12 illustrates these assignments for the 13-slot chassis; 6-slot chassis assignments are identical to those previously described for tabletop chassis. CRU addresses shown in figure cannot be changed.

24. Determine chassis location and interrupt assignments for each peripheral interface in system. If interrupt assignments do not match the factory-installed interrupts, or if additional interrupt assignments are required, perform Interrupt Installation procedure in this section of manual. If board slot assignments are unknown or an expansion chassis is being used, refer to Preparation Planning procedure in this section.

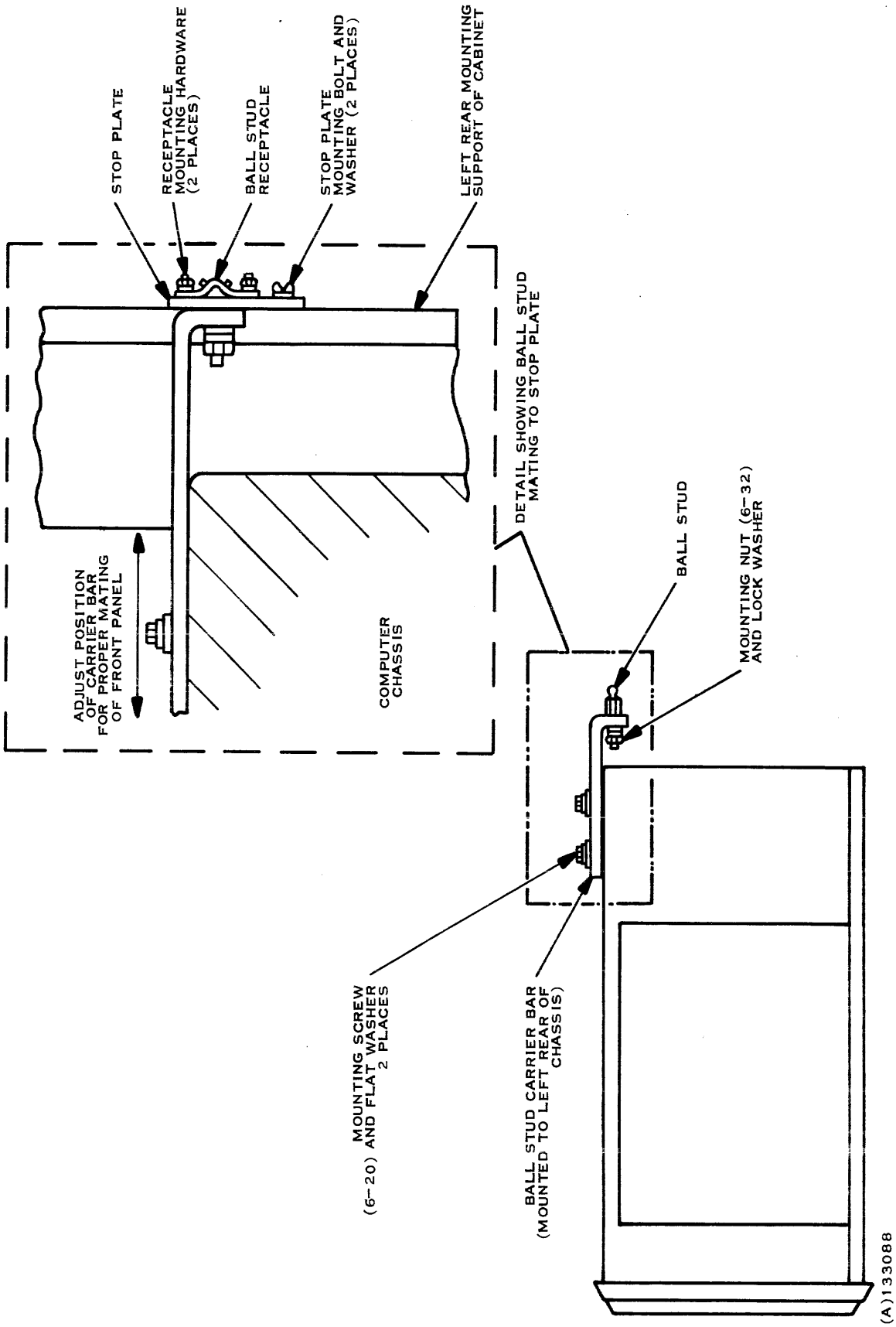


Figure 2-11. Installation of Ball Stud and Stop Plate

SLOT NUMBER	P1 (CHASSIS FRONT)			P2 (CHASSIS REAR)		
	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 AU	N/A	N/A	990/4 AU	N/A
2	02E0	MEMORY EXPANSION OR SPARE		02C0	MEMORY EXPANSION OR SPARE	
3	02A0	MEMORY EXPANSION OR SPARE		0280	MEMORY EXPANSION OR SPARE	
4	0260	SPARE		0240	SPARE	
5	0220	SPARE		0200	SPARE	
6	01E0	SPARE		01C0	SPARE	
7	01A0	SPARE	(13)*	0180	SPARE	(13)*
8	0160	CRT 3	(9)*	0140	CRT 3	(9)*
9	0120	CRT 2 OR CRU EXPANDER	(10)*	0100	CRT 2 OR CRU EXPANDER	(10)*
10	00E0	CRT 1	(11)*	00C0	CRT 1	(11)*
11	00A0	FLOPPY DISC CONTROLLER	7	0080	FLOPPY DISC CONTROLLER	7
12	0060	LINE PRINTER	(14)*	0040	CARD READER	4
13	0020	PROM PROGRAMMER	(15)* NOT USED	0000	733 ASR/KSR	6

*INTERRUPTS PREWIRED BUT NOT RECOGNIZED BY 990/4. MUST BE RECONFIGURED FOR USE WITH 990/4.

(A)133090

(B) 13-SLOT PREWIRED CHASSIS

Figure 2-12. 13-Slot Chassis Prewired Configuration

25. Verify that all boards are in their proper slots and are firmly seated in chassis.

26. Install peripheral device interface cables on proper interface module in computer chassis as described in Installation and Operation manual included with peripheral device. All interface cables should be routed through cable clamps at the rear of chassis and should exit at rear of chassis.

27. Turn key switch on front panel to ON (on programmer panel to the UNLOCK) position. Observe that the POWER and RUN indicators on front panel light and that fans operate.

28. Perform the System Checkout procedure specified later in this section of the manual.

29. Slide computer into cabinet to complete final installation of computer.

30. Install blank panels (if supplied) to fill open spaces in cabinet or rack.

31. Perform system software installation procedures for the operating system to be used with computer. For Texas Instruments supplied software, this information is provided in the System Operation Guide for the specific software package.

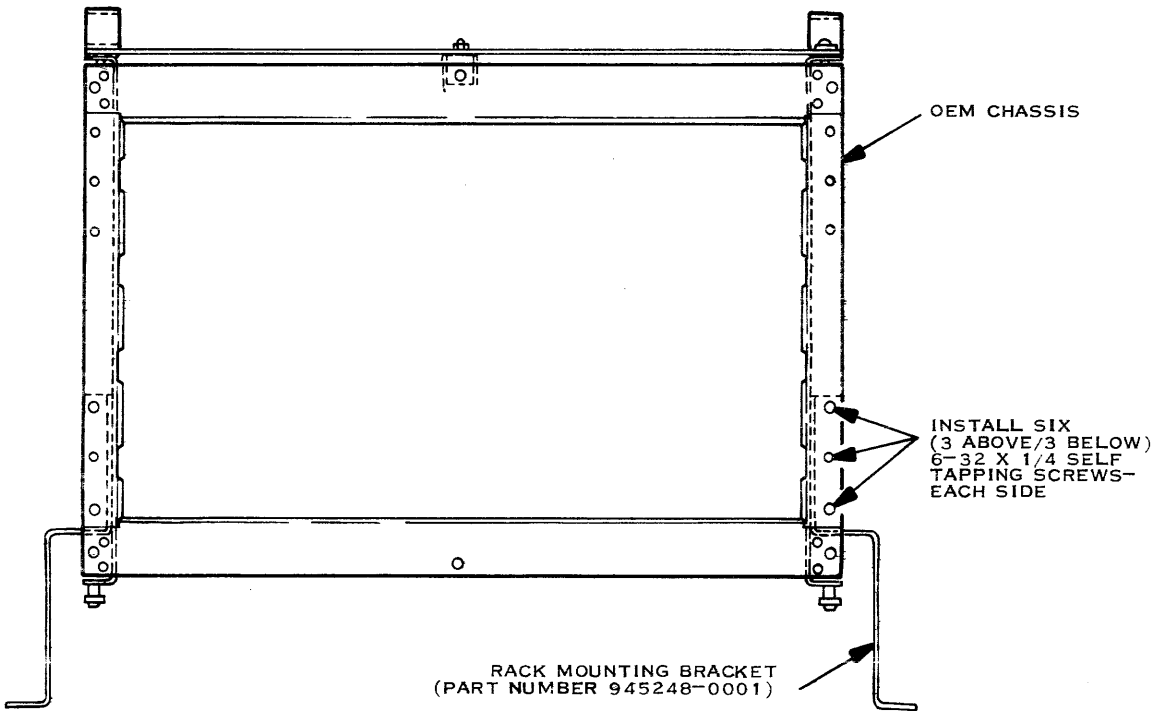
2.6 INSTALLATION (OEM CHASSIS)

The OEM (3-slot) chassis can be mounted in a customer-designed configuration, or it can be ordered for installation in a 19-inch equipment rack. The chassis is shipped with all circuit boards installed in the chassis; the rackmounting hardware (if ordered) is packed in the same carton as the chassis. The following procedure describes the steps required to mount the OEM chassis in a 19-inch rack. Other types of installation will require similar steps, but modified to suit the customer's site requirements.

1. Set unpacked chassis assembly on a convenient work surface near equipment rack in which chassis will be installed.

2. Attach one rackmounting bracket (Part Number 945248-0001) to each side of chassis using six (6) 6-32 X 1/4-inch, self-tapping screws for each bracket as illustrated in figure 2-13.

3. Determine desired vertical position of chassis in rack. The mounting bracket requires two holes, 2-1/4 inches apart, on each of front mounting supports of rack as illustrated in figure 2-14.



(A)133091

Figure 2-13. Mounting Bracket Installation

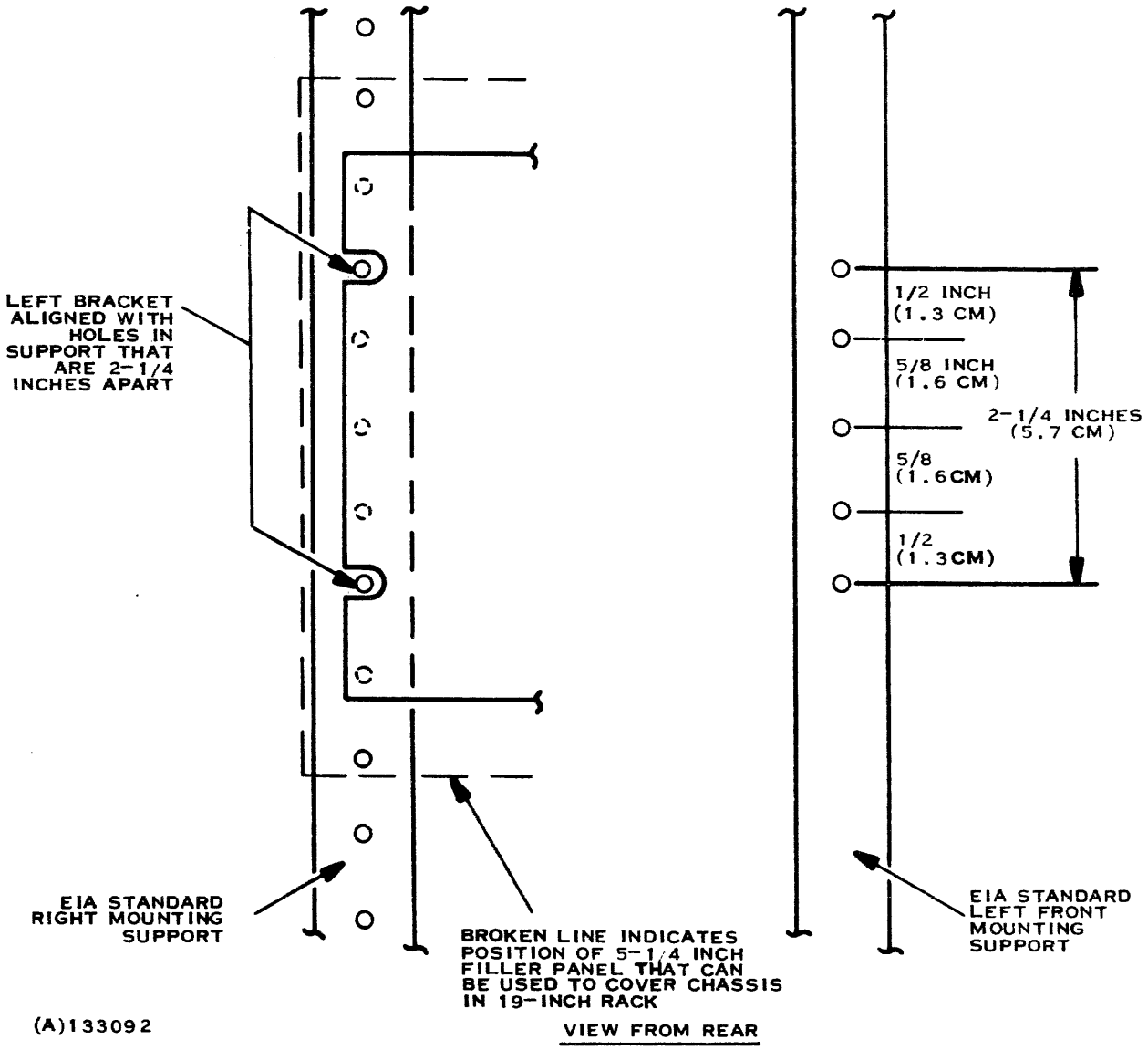


Figure 2-14. Positioning of OEM Chassis in 19-Inch Rack

4. Loosely install four (4) 10-32 X 1/4 mounting screws, and their associated flat washers and lock washers in the four selected holes in front mounting supports. Screws are installed from inside of enclosure.

5. Position slots in chassis mounting bracket on installed mounting screws such that bracket fits between cabinet mounting support and flat washer of mounting screws.

6. Ensure that chassis is square with cabinet mounting supports, and tighten all four mounting screws.

7. Connect external power and control lines to terminal strip at the rear of chassis as illustrated in figure 2-15.

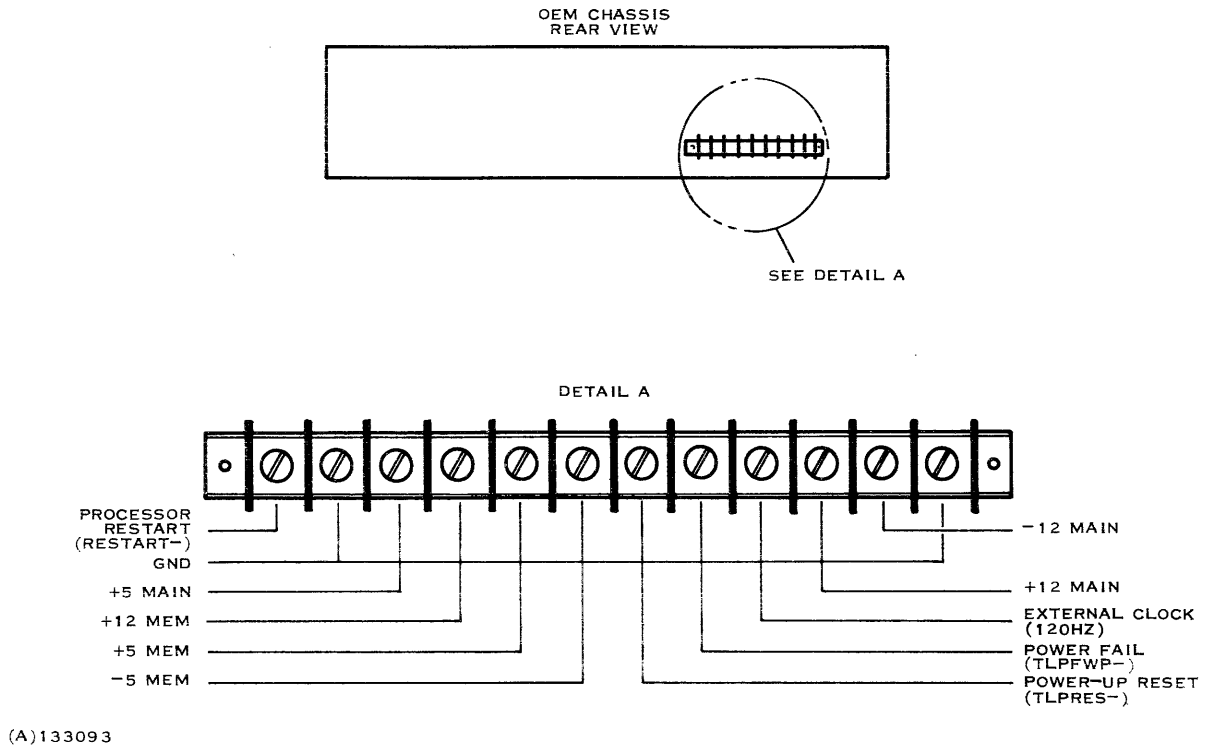


Figure 2-15. OEM Chassis External Connections

NOTE

The chassis is shipped from the factory without any interrupt lines installed. These must be installed to enable operation of interface circuits.

8. Remove shipping brackets that hold logic boards in place, and save brackets for reuse. Perform Interrupt Installation procedure described later in this section of the manual.

9. Verify that interface modules, memory board (if installed) and the processor board are firmly seated in their correct positions in chassis.

10. Install peripheral device interface cables and any other external interface cables that lead to chassis. Peripheral device cabling for Texas Instruments supplied devices is described in the Installation and Operation manual included with each peripheral device.

11. Apply power and use the Model 990 Computer Maintenance Unit to perform the System Checkout procedure as described later in this section.

12. Install 5-1/4-inch blank panel to cover chassis in rack or cabinet.

2.7 INTERRUPT INSTALLATION

The computer chassis (except the OEM chassis) is shipped from the factory with predetermined interrupts installed. These interrupt assignments are listed in the installation procedure for the particular chassis elsewhere in this section. If the interrupts do not meet the requirements of the system being installed, they may be easily modified. Wiring in the backplane of the chassis brings the interrupts from each connector to a pair of jumper plugs located on the backplane above the AU circuit board. Similarly, backplane connections bus the interrupt inputs to the processor to the jumper plug connections. Installing jumper wires in the jumper plugs connects the interrupts from the modules in the chassis to the appropriate interrupt level input to the processor. Modification of the predetermined interrupt configuration is a three-part procedure consisting of:

- Preparation and planning
- Modification of jumper plug
- Reinstallation of system

2.7.1 PREPARATION AND PLANNING. To ensure that the interrupt configuration is correctly installed and does not upset the operation of the software system that will control the system, proper planning of the chassis configuration is required. To aid in this planning, figure 2-16 provides a Chassis Configuration chart for each type of chassis that should be completed with the information for the system being installed. The following steps outline the procedure to prepare for modifying interrupts in either chassis:

1. Fill-in locations in Chassis Configuration chart with modules that comprise system to be installed. Observe following restrictions:

    a. In the main chassis, the 990/4 Microcomputer circuit board must occupy the topmost slot (slot 1). In an expansion chassis, the CRU buffer board must occupy slot 1.

    b. The memory circuit boards (if used) must occupy the slots immediately below the processor in the main chassis only. Memory boards or DMA devices cannot be installed in an expansion chassis.

    c. CRU addresses for interface modules that are assigned by the system software must correspond to the CRU address of the chassis slot in which the module is installed. Texas Instruments supplied software requires that the modules be located in the slots designated in the chassis installation procedures in this section. Before deciding on a chassis location for a new board, determine the address that system software has assigned to the board. If the CRU word address is less than or equal to $01E0_{16}$ (byte address $03C0_{16}$), the circuit board must be installed in the main chassis. If the CRU word address is greater than or equal to 0200_{16} (byte address 0400_{16}), the board must be installed in one of the expansion chassis. The CRU address that must be added to a CRU

SLOT NUMBER	P1 (CHASSIS FRONT) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	P2 (CHASSIS REAR) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 CIRCUIT BOARD*	N/A	N/A	990/4 CIRCUIT BOARD	N/A
2	02E0			02C0		
3	02A0			02B0		
4	0260			0240		
5	0220			0200		
6	01E0			01C0		
7	01A0			0180		
8	0160			0140		
9	0120			0100		
10	00E0			00C0		
11	00A0			0080		
12	0060			0040		
13	0020			0000		

	P1 (CHASSIS FRONT) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	P2 (CHASSIS REAR) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 CIRCUIT BOARD*	N/A	N/A	990/4 CIRCUIT BOARD	N/A
2	0120			0100		
3	00E0			00C0		
4	00A0			0080		
5	0060			0040		
6	0020			0000		

6-SLOT CHASSIS

*990/4 BOARD IS USED IN MAIN CHASSIS ONLY. IN EXPANSION CHASSIS, CRU BUFFER BOARD OCCUPIES SLOT 1.

	P1 (CHASSIS FRONT) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL	P2 (CHASSIS REAR) FIXED CRU BASE ADDRESS	CIRCUIT BOARD	INTER-RUPT LEVEL
1	N/A	990/4 CIRCUIT BOARD	N/A	N/A	990/4 CIRCUIT BOARD	N/A
2	0060			0040		
3	0020			0000		

3-SLOT CHASSIS

(A)133094

Figure 2-16. Chassis Configuration Charts

slot address (as shown in figure 2-16) to develop the address for the same slot in an expansion chassis is as follows:

Chassis No.	Value to be Added to CRU Base Address
1	0400
2	0800
3	0C00
4	1000
5	1400
6	1800
7	1C00

For example, if a board is to be located in half-slot 9P2 of expansion chassis 6, the fixed CRU base address value for 9P2 (0100 as shown in figure 2-16) must be added to the expansion chassis value for chassis 6 (1800 as shown above). The resulting value of 1900_{16} is the CRU address value that must be loaded into workspace register 12 by the system software during a transfer to or from the CRU interface board located in slot 9P2 of expansion chassis 6.

2. Determine interrupt level that each interface module or controller will be assigned, and enter those assignments in Interrupt Level column of Chassis Configuration chart. More than one module may be assigned to a particular interrupt level if interrupt service routine for that level interrupt can determine source of active interrupt.

NOTE

The 990/4 main chassis uses interrupts 1 through 7 only. The expansion chassis uses interrupts 1 through 15.

CAUTION

Ensure that the key switch on front panel of chassis is turned off before removing circuit boards from chassis. Failure to observe this caution could result in damage to circuit board components.

3. Remove enough circuit boards from chassis to enable free access to interrupt jumper plug as illustrated in figure 2-17. Typically, this operation requires removal of the boards in at least locations A1 through A5. While boards are out of chassis, check boards for proper jumper wire options as described later in this section.

4. Remove two jumper plugs from backplane by pulling firmly out on plugs. Do not twist or bend plug during removal.

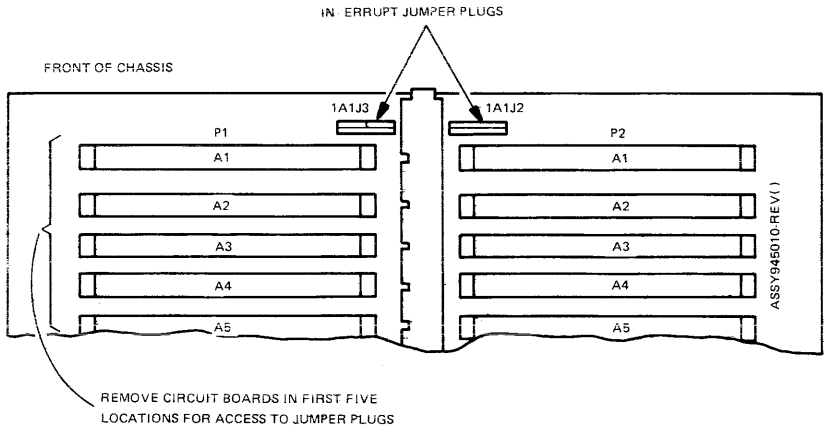


Figure 2-17. Location of Interrupt Jumper Plugs (6- and 13-Slot Chassis)

2.7.2 **MODIFICATION OF JUMPER PLUG.** The jumper plugs are molded plastic connectors with two rows of square holes for inserting jumper wires. The jumper plug for the 6-slot chassis has 10 holes in each row; the jumper plug for the 13-slot chassis has 24 holes in each row; the jumper plug for the 3-slot chassis has 8 holes in each row. Each hole has a plastic detent that holds the jumper wire in place when it is completely inserted into the hole. Figure 2-18 illustrates the mating of the jumper wire with the plastic jumper plug. Notice that the brass connector on the jumper wire must be oriented properly when inserted into the jumper plug so the plastic detent can engage the slot in the top of the jumper wire brass connector. The jumper wire can be removed from the jumper plug by lifting up on the plastic detent to free the jumper wire brass connector to slide out the rear of the jumper plug. The spring force of the detent is slight enough that only a fingernail is required to lift it up to release the jumper wire.

Figure 2-19 illustrates the position assignments on the interrupt plugs for both the 6- and the 13-slot chassis. Notice that each interrupt generated by a module has two positions on the plug assigned to it. This configuration allows interrupts that will be recognized on the same level to be daisy-chain linked to each other. For example, if the interrupts generated by the modules in locations 6P1, 5P2 and 4P2 are to be level 7 interrupts, the chain would be connected as follows:

1. Insert one end of a jumper wire in hole assigned to Level 7 and the other end of that jumper wire into one of two holes assigned to 4P2.

2. Insert one end of a second jumper wire into second hole assigned to 4P2 and the other end of that jumper wire into one of two holes assigned to 5P2.

3. Insert one end of a third jumper wire into second hole assigned to 5P2 and the other end of that jumper wire into one of two holes assigned to 6P1.

The resulting jumper configuration would appear as illustrated in figure 2-20.

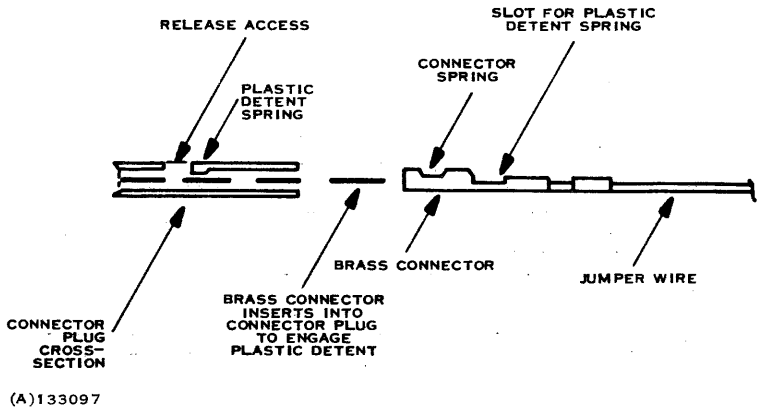


Figure 2-18. Interrupt Jumper Wire Installation

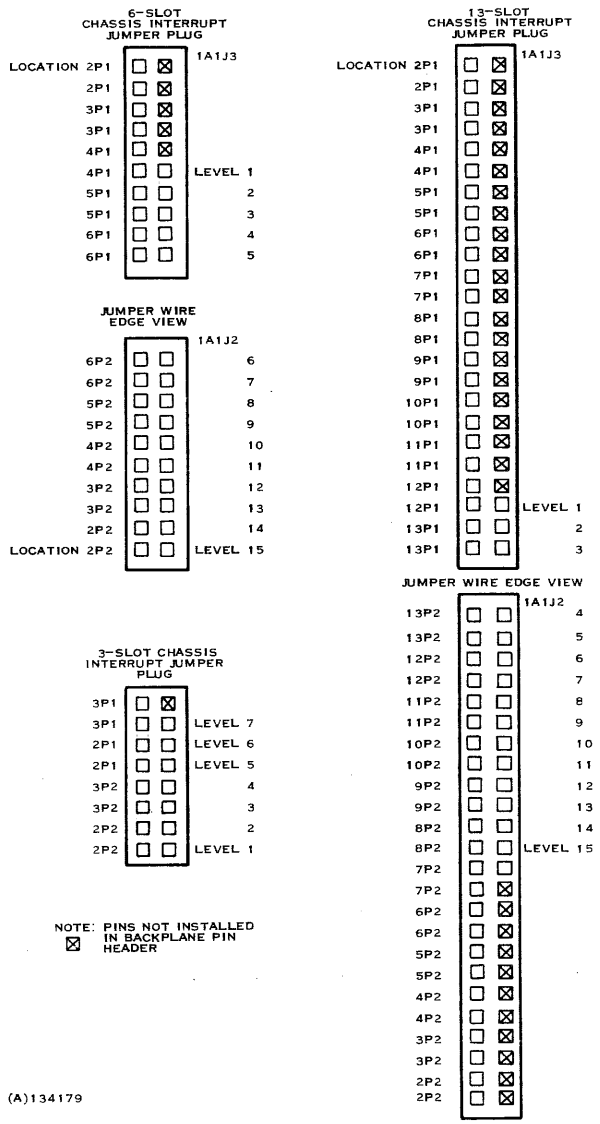


Figure 2-19. 3-, 6- and 13-Slot Chassis Interrupt Jumper Plugs (Main and Expansion Chassis)

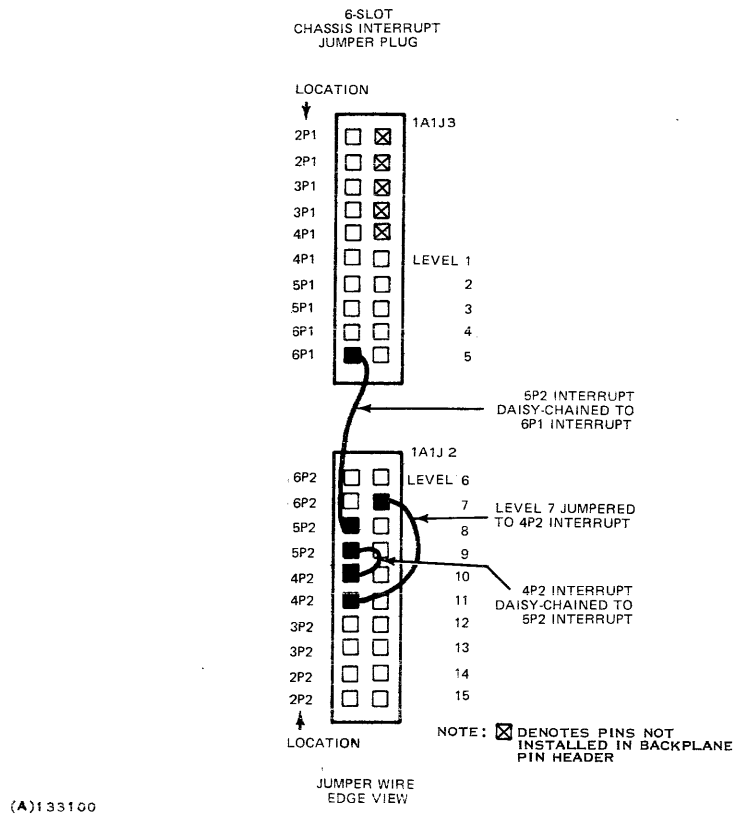


Figure 2-20. Jumper Plug Daisy-Chain Sample Connection

To install the jumper configuration for the system being modified, refer to the Chassis Configuration chart, and perform the following steps:

1. Determine if any of factory-installed jumper wires are still valid interrupt assignments for the modified system, and remove factory-installed jumper wires that are not valid.

2. Determine all locations that generate an interrupt for one of active priority levels, and connect them together similar to method used in the example.

3. Repeat step 2 for all active interrupt levels.

2.7.3 **REINSTALLATION OF SYSTEM.** When the jumper plugs have been modified to suit the interrupt configuration required for the system, perform the following steps to reconstruct the system:

1. Insert the reconfigured jumper plugs into their proper positions on backplane of computer chassis. Ensure that they are oriented correctly with the interrupt connections along top edge and the generated interrupts along bottom edge.

NOTE

Prior to performing step 2, refer to the Circuit Board Jumper Modifications paragraph at the end of this section and verify that all options are properly installed.

2. Consult the Chassis Configuration chart that was filled out for modified system, and install circuit boards into chassis according to those assignments. Ensure that component side of circuit boards faces up.

3. Return to Chassis Installation procedure for the specified chassis in this section, and ensure that all steps in that procedure have been properly performed.

2.8 CIRCUIT BOARD JUMPER MODIFICATIONS

All circuit boards used in the 990/4 Microcomputer System are equipped with various jumper wire options which must be correctly installed prior to normal use of the system. The jumper options associated with the 990/4 Microcomputer board, the 990/4 memory expansion board, the EPROM memory module, and the CRU expansion and CRU buffer boards are summarized in table 2-2 and briefly described in the following paragraphs. Additional detail is provided in Section III of this manual.

2.8.1 990/4 MICROCOMPUTER BOARD JUMPER OPTIONS. At present, there are two standard configurations of 990/4 Systems including:

- Machine Controller Configuration, Part Number 944910-1. This config uration is not equipped with a 4K RAM memory. Bank 3 of the 1K RAM/ROM memory contains static RAM ICs. The ROM/RAM memory is jumpered to a starting memory address at 0; the power-up trap is set for 0; the jumper is removed between E1 and E2, and static RAM implemented in bank 3; memory-error interrupt is connected to level 2, power-fail interrupt is connected to level 1 and the real-time clock interrupt is connected to level 5; 4K dynamic RAM memory is not implemented.

- General-Purpose Computer Configuration, Part Number 944910-2. This configuration contains 4K RAM, loader ROM and self-test ROMs installed in banks 2 and 3 of 1K ROM/RAM memory; power-up trap set for 0; 4K RAM start address set for 0; start address for 1K ROM/RAM memory set for F800; interrupt levels are assigned identically to the machine controller configuration.

The two standard configurations of the 990/4 Microcomputer board are shown in figure 2-21. All possible combinations of the jumper options are summarized in table 2-2.

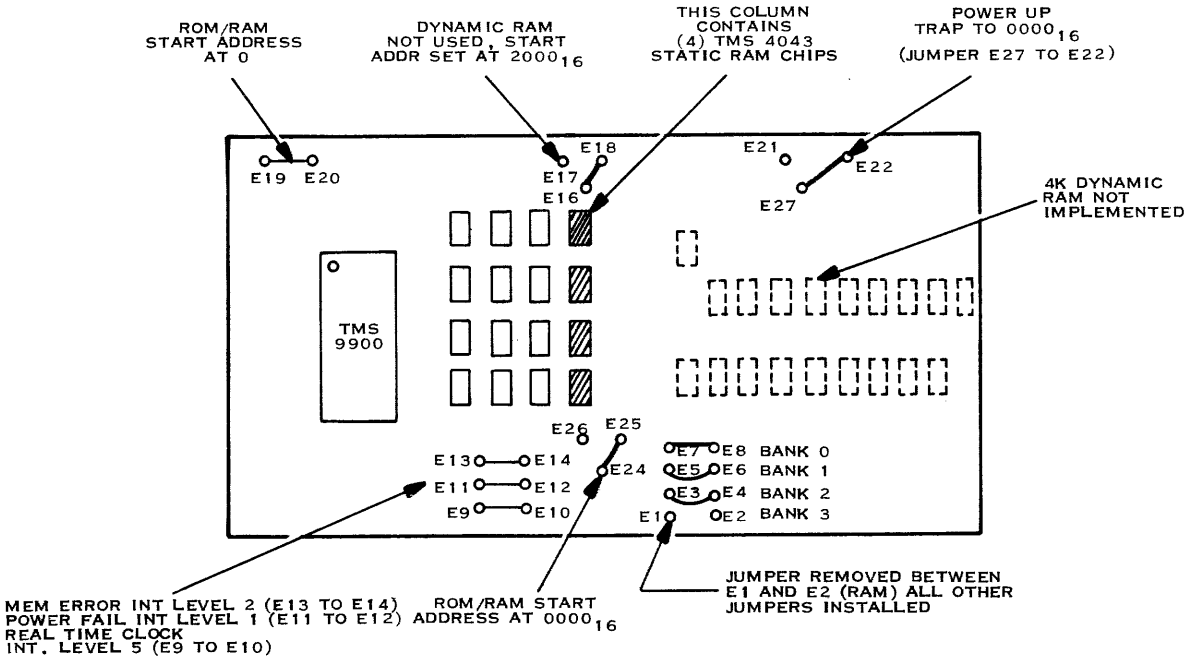
2.8.2 990/4 MEMORY EXPANSION BOARD OPTIONS. The 990/4 memory expansion board must be set up with the proper starting memory address using bias switches S2 through S4, and the memory size jumpers (E1 through E6) must reflect the amount of memory implemented on the board. In addition, a jumper is required between terminals E7 and E8 if the write-protect option is *not* installed (see figure 2-22). In the standard configuration, the starting address is set to 2000_{16} (S2 and S3 set to OFF positions, S4 set to ON position as shown in table 2-3). The amount of memory implemented on the board may be determined by counting the number of rows of memory chips (4K per row).

Table 2-2. 990/4 Circuit Board Jumper Options

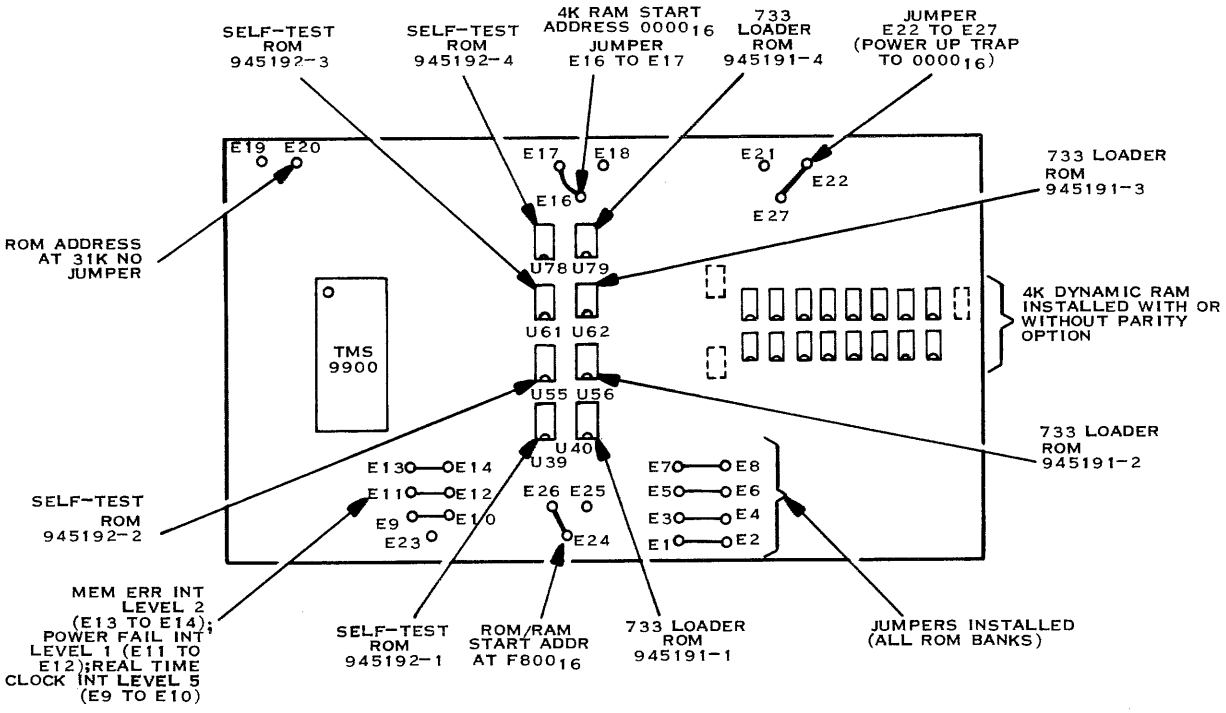
Function	Jumper Option
1K ROM/RAM Starting Address	
Start address = 0000_{16} (0K)	E19→E20; E24→E25
Start address = 0800_{16} (1K)	E19→E20; E24→E26
Start address = $F000_{16}$ (30K)	E19, E20 Open; E24→E25
Start address = $F800_{16}$ (31K)	E19, E20 Open; E24→E26
1K ROM/Static RAM Option	
Bank 0 = PROM	E7→E8
Bank 0 = RAM	E7, E8 Open
Bank 1 = PROM	E5→E6
Bank 1 = RAM	E5, E6 Open
Bank 2 = PROM	E3→E4
Bank 2 = RAM	E3, E4 Open
Bank 3 = PROM	E1→E2
Bank 3 = RAM	E1, E2 Open
4K Dynamic RAM Starting Address	
Start address = 0000_{16} (0K)	E16→E17
Start address = 2000_{16} (4K)	E17→E18
Power-Up Trap Vector	
Vector at address = 0000_{16}	E22→E27
Vector at address = $FFFC_{16}$	E21→E22
Clock Interrupt Level	
Level = Interrupt 5	E9→E10
Level = Interrupt 7	E10→E23
Not Connected	E9, E10, E23 Open
Memory Error Interrupt	
Connected to Interrupt 2	E13→E14
Not Connected	E13, E14 Open
Power-Fail Interrupt	
Connected to Interrupt 1	E11→E12
Not Connected	E11, E12 Open

2.8.3 **EPROM MEMORY MODULE JUMPER OPTIONS.** Prior to installing the EPROM memory module in the main chassis, the following jumper- and switch-selectable options must be incorporated:

- Starting address must be set-up using microswitch S2 (figure 2-22). Typically, the EPROM memory is set up just above the expansion memory. The specifics for setting the starting address are provided in table 2-4.
- Memory size must be designated by wiring jumpers between terminals E1 to E8 as shown in figure 2-23 and table 2-4.
- "Computer type" jumper must be installed between E11 and E12 for use in 990/4 System.



(A) MACHINE CONTROLLER CONFIGURATION (944910-1)



(B) GENERAL PURPOSE COMPUTER CONFIGURATION (944910-2)

(B)133342

Figure 2-21. 990/4 Microcomputer Board Options

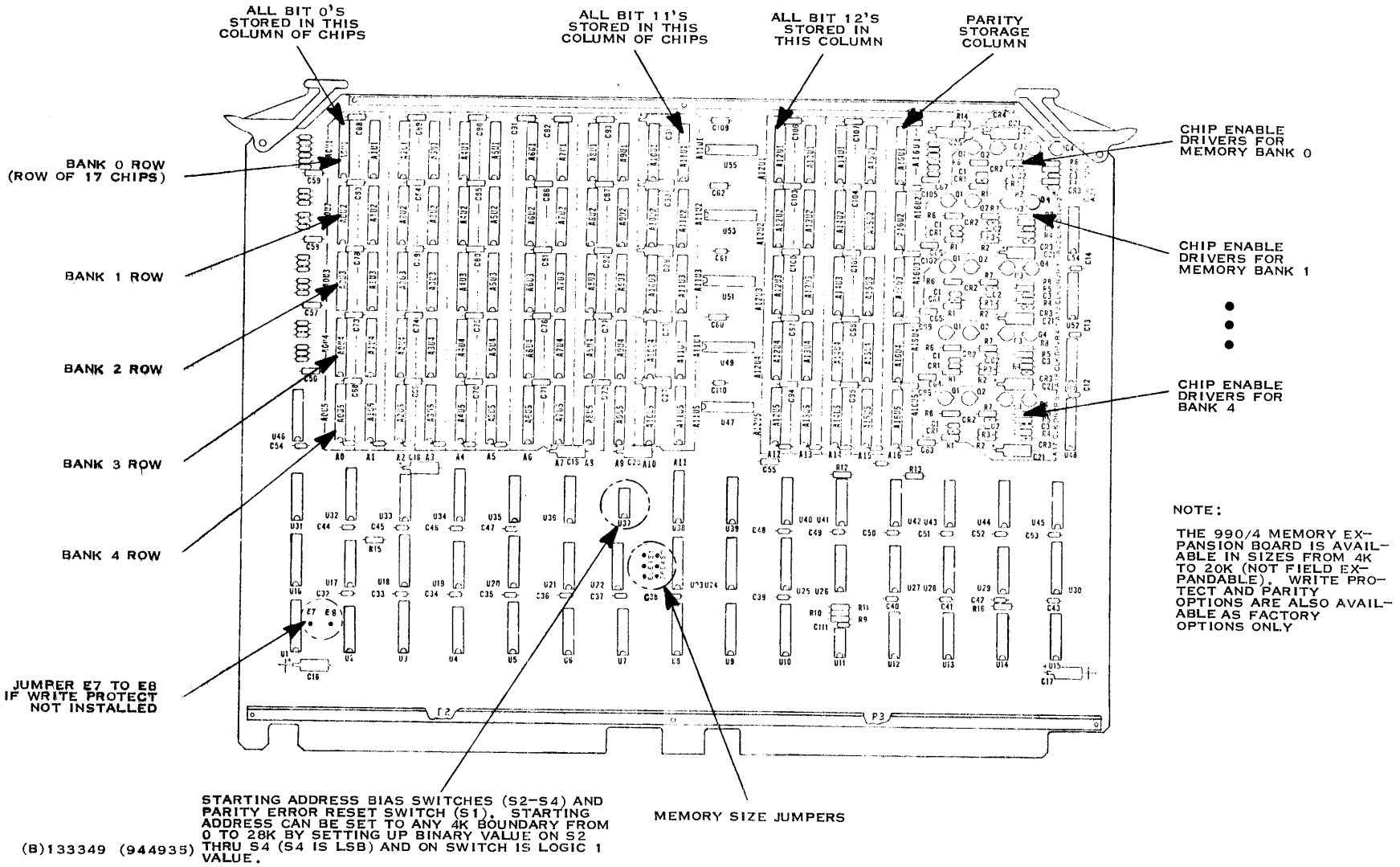


Figure 2-22. 990/4 Memory Expansion Board Options

Table 2-3. 990/4 Memory Expansion Board Jumper Options

990/4 MEMORY EXPANSION BOARD

Starting Address	Switch Settings
0000_{16} (0)	S2, S3 and S4 off
2000_{16} (4K)	S2, S3 off; S4 on
4000_{16} (8K)	S2 off; S3 on; S4 off
6000_{16} (12K)	S2 off; S3, S4 on
8000_{16} (16K)	S2 on, S3, S4 off
$A000_{16}$ (20K)	S2 on, S3 off; S4 on
$C000_{16}$ (24K)	S2, S3 on; S4 off
$E000_{16}$ (28K)	S2, S3, S4 on

Note: S1 is manual reset for parity error light (S1 on = Reset)

Memory Size	Jumpers Required
4K	None
8K	Jumper E1 to E2 (E3 thru E6 OPEN)
12K	Jumper E3 to E4 (E1, E2, E5 and E6 OPEN)
16K	Jumper E1 to E2, E3 to E4 (E5 and E6 OPEN)
20K	Jumper E5 to E6 (E1 thru E4 OPEN)

Write Protect Option	Jumpers Required
Option installed	E7 and E8 OPEN
Option not installed	Jumper between E7 and E8

2.9 CRU EXPANSION INSTALLATION REQUIREMENTS

Up to seven I/O expansion chassis may be connected to the main chassis when configuring larger 990/4 Systems. The electrical interconnection between the main chassis backpanel and the expansion chassis is accomplished via the CRU expansion board which is installed in an unused card slot in the main chassis. The CRU expansion board contains seven top-edge connectors designated P3 through P9 (see figure 2-24), each of which contains all necessary data, address, interrupt and interrupt identification lines required to link an external chassis to the main chassis.

Typically, the plugs are assigned to expansion chassis as follows:

- P3 – expansion chassis 1 (buffer board in slot 1 of the expansion chassis must also be programmed for the chassis 1 ID).
- P4 – expansion chassis 2

  :
- P9 – expansion chassis 9

Table 2-4. EPROM Memory Module Jumper Options

Starting Address (Hex Byte Addresses)		Bias Switch Setting S1	S2	S3	S4	S5	Starting Address (Hex Byte Addresses)		Bias Switch Setting S1	S2	S3	S4	S5
0000	(0)	off	off	off	off	off	9000	(18K)	on	off	off	on	off
0800	(1K)	off	off	off	off	on	9800	(19K)	on	off	off	on	on
1000	(2K)	off	off	off	on	off	A000	(20K)	on	off	on	off	off
1800	(3K)	off	off	off	on	on	A800	(21K)	on	off	on	off	on
2000	(4K)	off	off	on	off	off	B000	(22K)	on	off	on	on	off
2800	(5K)	off	off	on	off	on	B800	(23K)	on	off	on	on	on
3000	(6K)	off	off	on	on	off	C000	(24K)	on	on	off	off	off
3800	(7K)	off	off	on	on	on	C800	(25K)	on	on	off	off	on
4000	(8K)	off	on	off	off	off	D000	(26K)	on	on	off	on	off
4800	(9K)	off	on	off	off	on	D800	(27K)	on	on	off	on	on
5000	(10K)	off	on	off	on	off	E000	(28K)	on	on	on	off	off
5800	(11K)	off	on	off	on	on	E800	(29K)	on	on	on	off	on
6000	(12K)	off	on	on	off	off	F000	(30K)	on	on	on	on	off
6800	(12K)	off	on	on	off	on	F800	(31K)	on	on	on	on	on
7000	(14K)	off	on	on	on	off							
7800	(15K)	off	on	on	on	on							
8000	(16K)	on	off	off	off	off							
8800	(17K)	on	off	off	off	on							

Memory Size	Jumpers Required
1K	E1 to E2; E4 to E5; E7 to E8
2K	E1 to E2; E4 to E5; E8 to E9
3K	E1 to E2; E5 to E6; E7 to E8
4K	E1 to E2; E5 to E6; E8 to E9
5K	E2 to E3; E4 to E5; E7 to E8
6K	E2 to E3; E4 to E5; E8 to E9
7K	E2 to E3; E5 to E6; E7 to E8
8K	E2 to E3; E5 to E6; E8 to E9

Computer Type	Jumper Required
990/4	E11 to E12; E10 OPEN

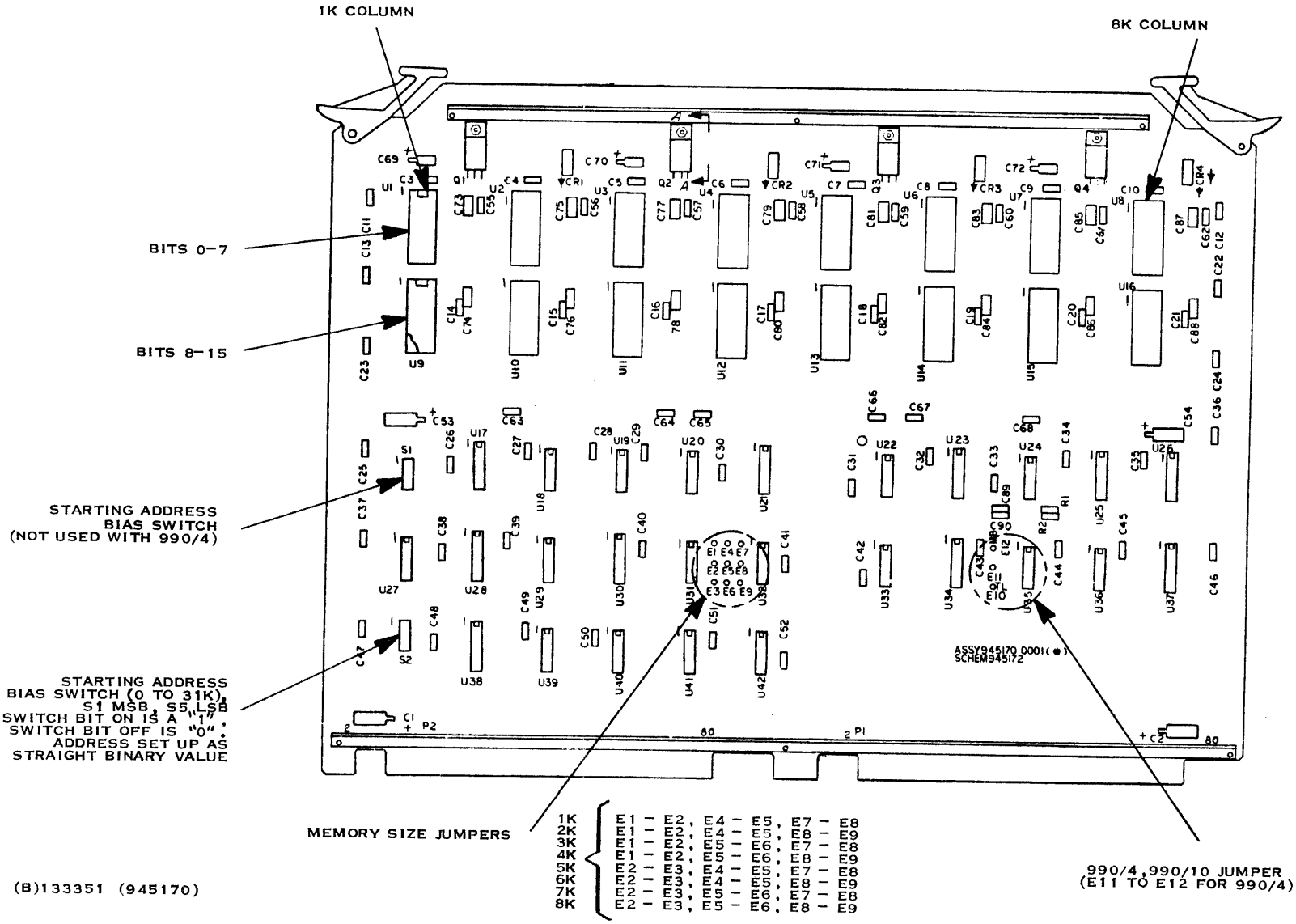


Figure 2-23. EPROM Memory Module Options

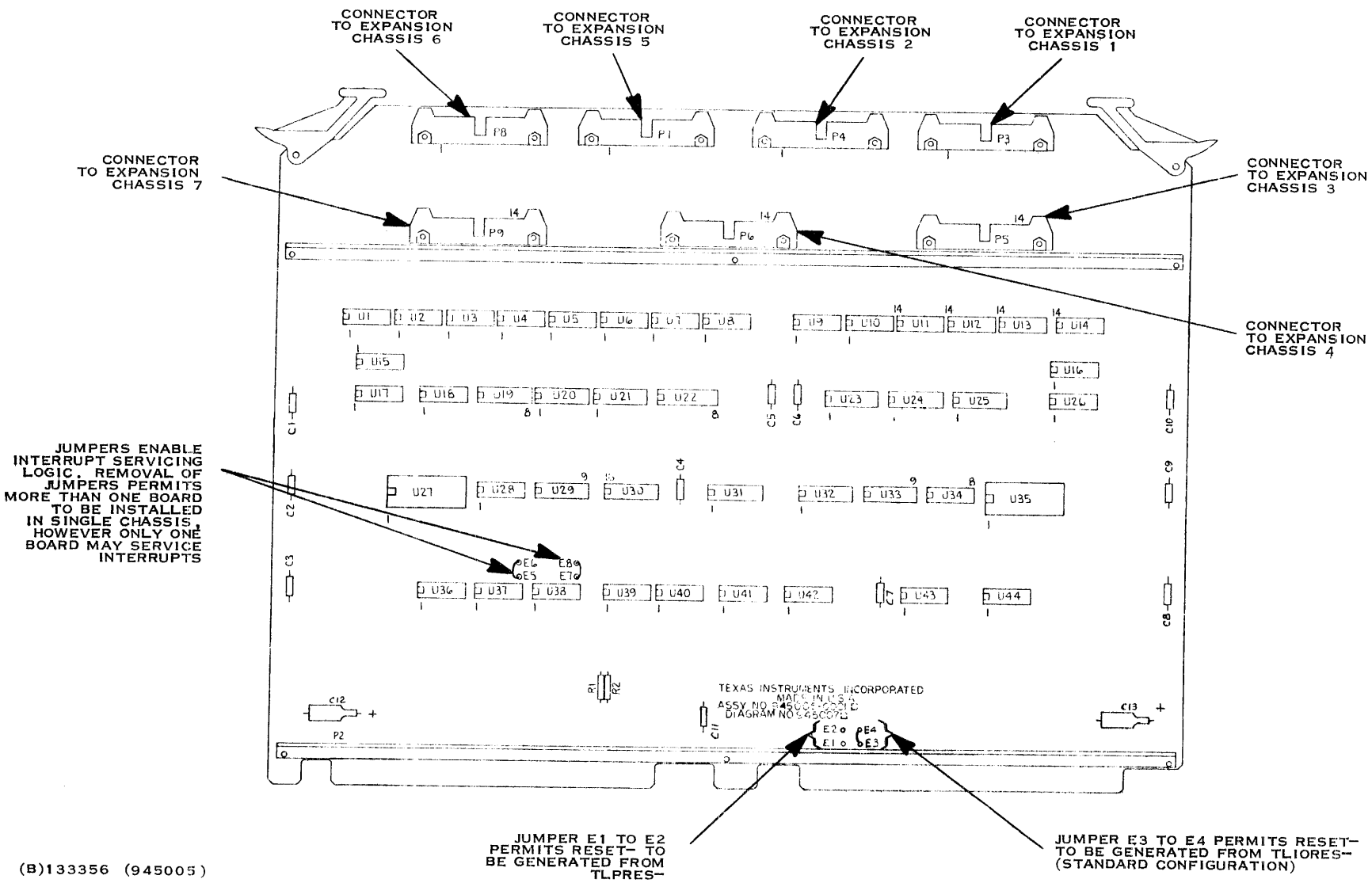


Figure 2-24. CRU Expansion Board Options

2.9.1 CRU EXPANSION BOARD JUMPER OPTIONS. The jumper options on the CRU expansion board include:

- Jumper-wire selection of either power-up reset signal (TLPRES–) from the power supply or IORES– from the 990/4 Microcomputer in the main chassis. Typically, the IORES– signal is used which includes an OR of the main chassis power supply power-on reset and the software CLR instruction (jumper connected between terminals E3 and E4, and terminals E1 and E2 are both open).

- Interrupt section enable option. If four or less expansion chassis are being used, interrupt Section A is enabled (jumper wire between E5 and E6) and interrupt Section B is disabled (jumper wire removed between terminals E7 and E8). If five or more chassis are being installed, both sections must be enabled.

These jumper options are shown in figure 2-24 and summarized in table 2-5.

2.9.2 CRU BUFFER BOARD JUMPER OPTIONS. The CRU buffer board in each expansion chassis must be programmed with the proper chassis ID. In the standard configuration, the chassis which is cabled to P3 on the CRU expansion board in the main chassis is designated chassis 1, and the expansion chassis connected to J9 is designated chassis 7 (in numerical order). The chassis ID must then be programmed on the CRU buffer board which is installed in slot 1 of each expansion chassis. The chassis ID is set up by installing plug P4 in the selected position 1 through 7 (see figure 2-25).

The CRU buffer board also contains provisions for bypassing the interrupt scanner for interrupt level 1 when a peripheral requiring fast interrupt response time is implemented in an expansion chassis. In this case, J1 is installed in DI1 and DI2. For normal interrupt scanner processing of interrupt level 1, J1 is installed in DI3 and DI4.

For normal operation, the internal clock enable jumper must be installed between terminals E1 and E2. For maintenance purposes, the internal clock may be disabled by removing this jumper. An external clock source may be connected to the board via terminal E3, and the scan counter may be cleared by temporarily applying a ground to terminal E4. The CRU buffer board jumper options are summarized in table 2-6.

2.9.3 EXPANSION CHASSIS INTERRUPT WIRING. The interrupt wiring for each expansion chassis is performed in a similar fashion to that used in the main chassis. However, interrupt levels 1 through 15 are available in the expansion chassis while only levels 1 through 7 are available in the main chassis (level 0 assigned to power-up trap). Actual interrupt wiring in both cases is identical (see figures 2-19 and 2-20).

Table 2-5. CRU Expansion Board Jumper Options

Reset Source	Jumper Required
TLPRES–	Jumper E1 to E2, E3 and E4 OPEN
IORES–	Jumper E3 to E4; E1 and E2 OPEN

Interrupt Section Enable Option	Jumper Required
Interrupt Section A enabled	Jumper E5 to E6
Interrupt Section B enabled	Jumper E7 to E8

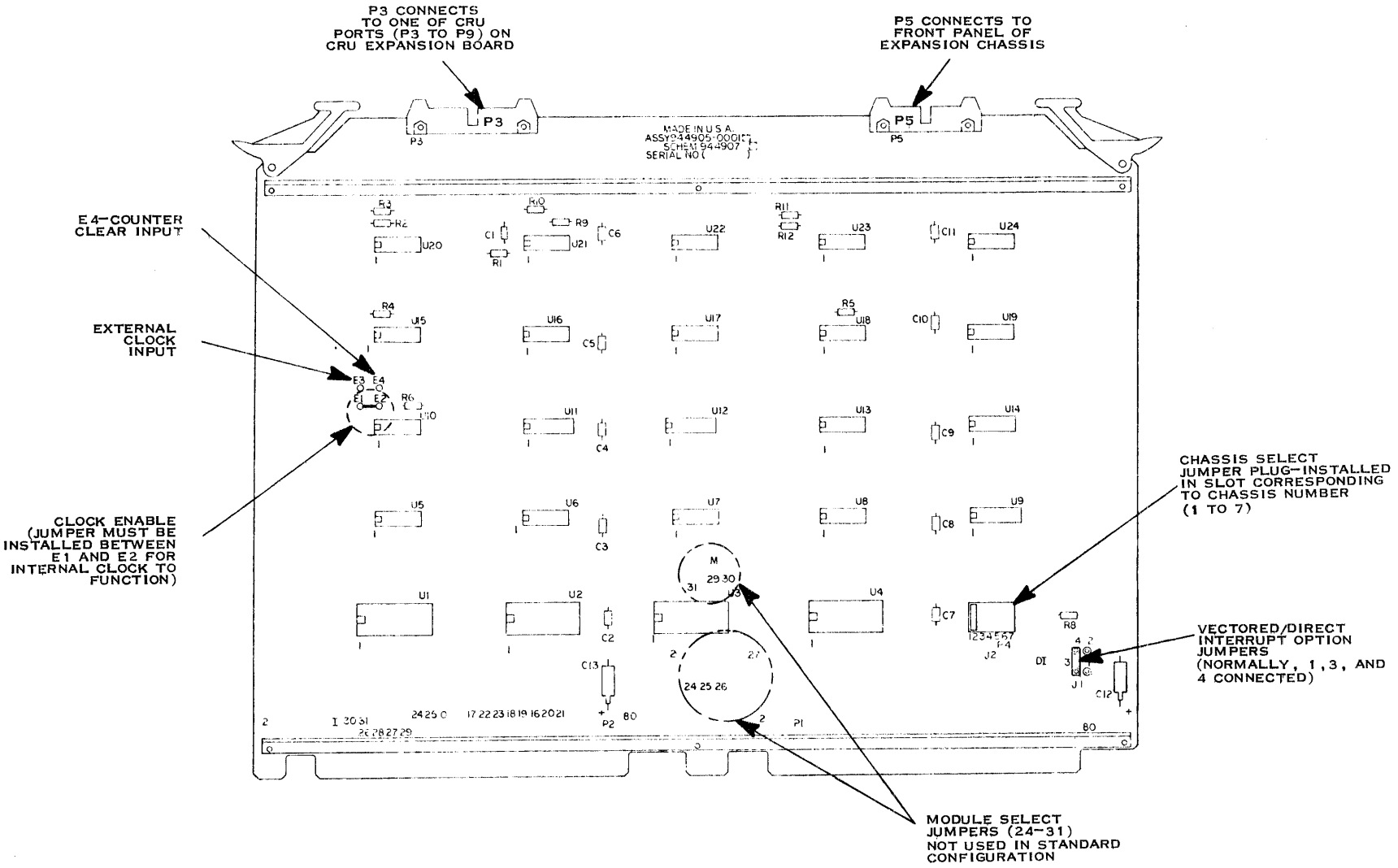


Figure 2-25. CRU Buffer Board Options

Table 2-6. CRU Buffer Board Jumper Options

Chassis ID Select	Jumper Required
1	P4 in position 1 of J2
2	P4 in position 2 of J2
:	:
7	P4 in position 7 of J2

Internal Clock Option	Jumper Required
Normal operating system	E1 to E2
clock disabled	E1 and E2 open

Vectored/Direct Interrupt Option	Jumper Required
Level 1 vectored	J1 in DI3, DI4
Level 1 direct	J1 in DI1, DI2

2.10 LOGIC BOARD INSTALLATION PROCEDURES

Before installing a logic board in the main chassis or one of the expansion chassis, the chassis map located on top of the chassis should be consulted. If adding a new board to the system, the Preparation and Planning paragraph in this section should be consulted to ensure that the interrupt and CRU addressing requirements of the system are being met. In general, logic boards are either half-sized or full-sized boards. The half-sized boards require the addition of a center card guide into the selected card slot prior to the installation of the logic board.

Procedures for installing both types of logic boards are provided in the following paragraphs.

2.10.1 FULL-SIZED LOGIC BOARD INSTALLATION. The following procedure should be used to install a full-sized logic board into a 990 chassis:

1. Set the key switch on the chassis front panel to the OFF position.

CAUTION

Failure to shut off power to the chassis when installing or removing a logic board may result in damage to the board due to temporary misalignment of board and connector pins.

2. Insert the board into the selected slot of the chassis with the component side of the board facing upward.

3. Ensure that the slots in the circuit board mate properly with the alignment comb on the backpanel connector.

4. Press the board firmly into place, and ensure that the board is properly seated.

5. For a CRU interface board, refer to the associated Installation and Operation manual for cabling information.

6. The board may be removed from the chassis by removing the interface cable and lifting the plastic, pivoted tabs (card ejectors) to free the board from the chassis backpanel.

2.10.2 **HALF-SIZED LOGIC BOARDS.** Half-sized logic boards may be installed in a 990 chassis using the following procedure:

1. If a center card guide is installed in the desired slot, proceed to step 7. If the center card guide is *not* installed, proceed to step 2.

2. Disconnect the chassis ac power cord from its ac power source.

WARNING

The Center Card Guide Installation procedure requires exposure to dangerous ac voltages unless the chassis is disconnected from the ac power source.

3. If the card guide is being installed on a 6-slot or 13-slot chassis, the left-side access panel and the power supply board(s) must be removed. The standby power supply (when used) is mounted piggyback over the main power supply board. To remove the standby supply board, disconnect cable connector plugs 1A6P1 and 1A6P2, and remove five holding screws. To remove the main power supply board, disconnect cable connectors 1A3P1 and 1A3P2, and remove four holding screws and three standoffs from the center of the board.

4. Examine the card comb located between the two rows of connectors on the front side of the motherboard. If a screw is located between the two connectors in the position where the card guide is to be installed, remove the screw and associated hardware from the motherboard, and install in an adjacent hole either above or below the original location.

5. Install the center card guide, TI Part Number 945226-0001, using a flat washer and screw as shown in figure 2-26. Inspect the card guide to ensure that it is not rotated with respect to the card comb. Correct if misaligned.

NOTE

If two half-sized logic cards are being installed in the same full-sized chassis slot, center the card guide. If only one card is being installed, mount the card guide toward the side of the chassis where the logic card is being installed.

6. Replace the main power supply board and the standby power supply board (if used). Ensure that all screws and standoffs are snug and that all connectors are properly installed. Replace the side access panel.

7. Insert the logic board into the selected half-slot chassis location with the component side of the board facing upward.

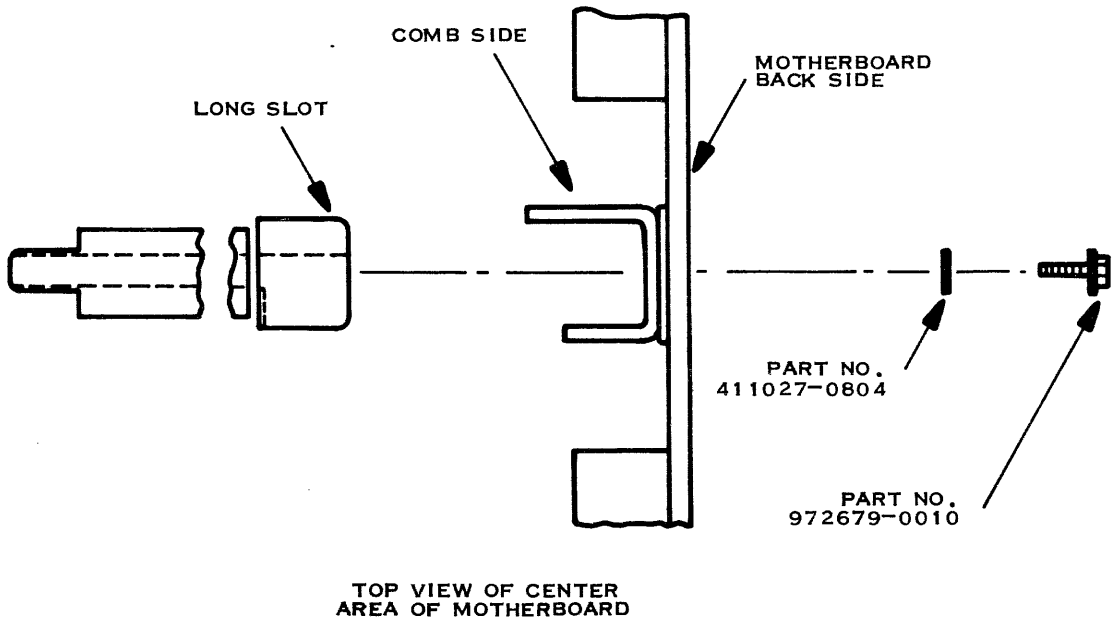


Figure 2-26. Center Card Guide Installation Diagram

8. Ensure that the slots in the circuit board mate properly with the alignment comb on the backpanel connector. Press the board firmly into position.

9. Refer to the associated Installation and Operation manual for the CRU logic card type for additional cabling information.

2.11 SYSTEM CHECKOUT PROCEDURE

System checkout for the computer consists of loading and executing processor diagnostic tests to ensure that the computer is operating within specifications, and then loading and executing a set of hardware demonstration tests to verify that all system peripheral devices are connected properly to the computer. Refer to the Model 990 Computer Diagnostics handbook for a listing of the diagnostic tests for the 990/4 Microcomputer. This handbook also contains:

- A list of all the 990 diagnostics
- A description of the loaders and loading devices that are available and how to use them
- A description of what a standalone test is and how to run one
- A description of the available Verb packages and how to use them with the 990/4 with a CRT or 733, and the 990/4 with a programmer front panel as an I/O device
- A brief description of each test.

SECTION III

PRINCIPLES OF OPERATION

3.1 GENERAL

This section provides a block diagram level discussion of each of the hardware units of the Model 990/4 Microcomputer System including units that are optional.

3.2 990/4 CIRCUIT BOARD

The TMS 9900 Microprocessor along with associated logic mounted on the 990/4 circuit board performs as a complete computer. As shown on the block diagram for the 990/4 circuit board, figure 3-1, the TMS 9900 Microprocessor serves as the central processor for the computer. In addition to the microprocessor, the circuit board contains 9900 Memory Bus logic that permits the microprocessor to address local memory mounted on the board for high-speed read and/or write operations. Local memory may consist of up to 4096 16-bit words of dynamic random access memory (RAM), and up to 1024 16-bit words of programmable read only memory (PROM), or 1024 16-bit static RAM, or a combination of PROM and static RAM in 256-word increments for the total of 1024 16-bit words. The 9900 Memory Bus also connects to connectors P1 and P2 of the circuit board so when the circuit board is installed in a chassis backpanel slot, the microprocessor may address external expansion memory for read and write operation. In addition, an external device can take control of the 9900 Memory Bus to address either local or external memory by setting the HOLD– signal line low.

Serial data transfer between the microprocessor and interfaces for external CRU devices is effected through CRU interface logic with control and signal lines brought to connectors P1 and P2 on the circuit board.

The programmer panel is a CRU device, and separate CRU interface logic provides control and signal lines at connector P3 of the circuit board through which the interface to the programmer panel is made.

The microprocessor clock provides timing signals for the microprocessor and board-mounted logic and is connected to connector P1 to exert timing control of externally connected devices.

A 120-Hz signal input from the power supply drives the programmable real-time clock interrupt circuit on the circuit board which may optionally be connected to interrupt level 5 or 7. Up to seven priority vectored interrupt levels (levels 1 through 7) may be applied to the circuit board at connector P1. A detailed description of each of these functions is provided in the following subparagraphs.

3.2.1 TMS 9900 MICROPROCESSOR. The TMS 9900 is a 16-bit microprocessor on a chip which, when combined with an external memory and clock source, functions as a full-scale, general-purpose computer. In addition to its compact size, the microprocessor chip offers such advanced features as vectored interrupts and memory located register files for efficient context switching, two I/O channels including a command-driven (CRU) channel and a 16-bit direct memory access channel, a full 64K bytes of memory addressing space, and a flexible set of 69 instructions (five of which are implemented external to the chip). A summary of TMS 9900 Microprocessor characteristics is provided in table 3-1. A simplified block diagram of the TMS 9900 internal structure is shown in figure 3-2.

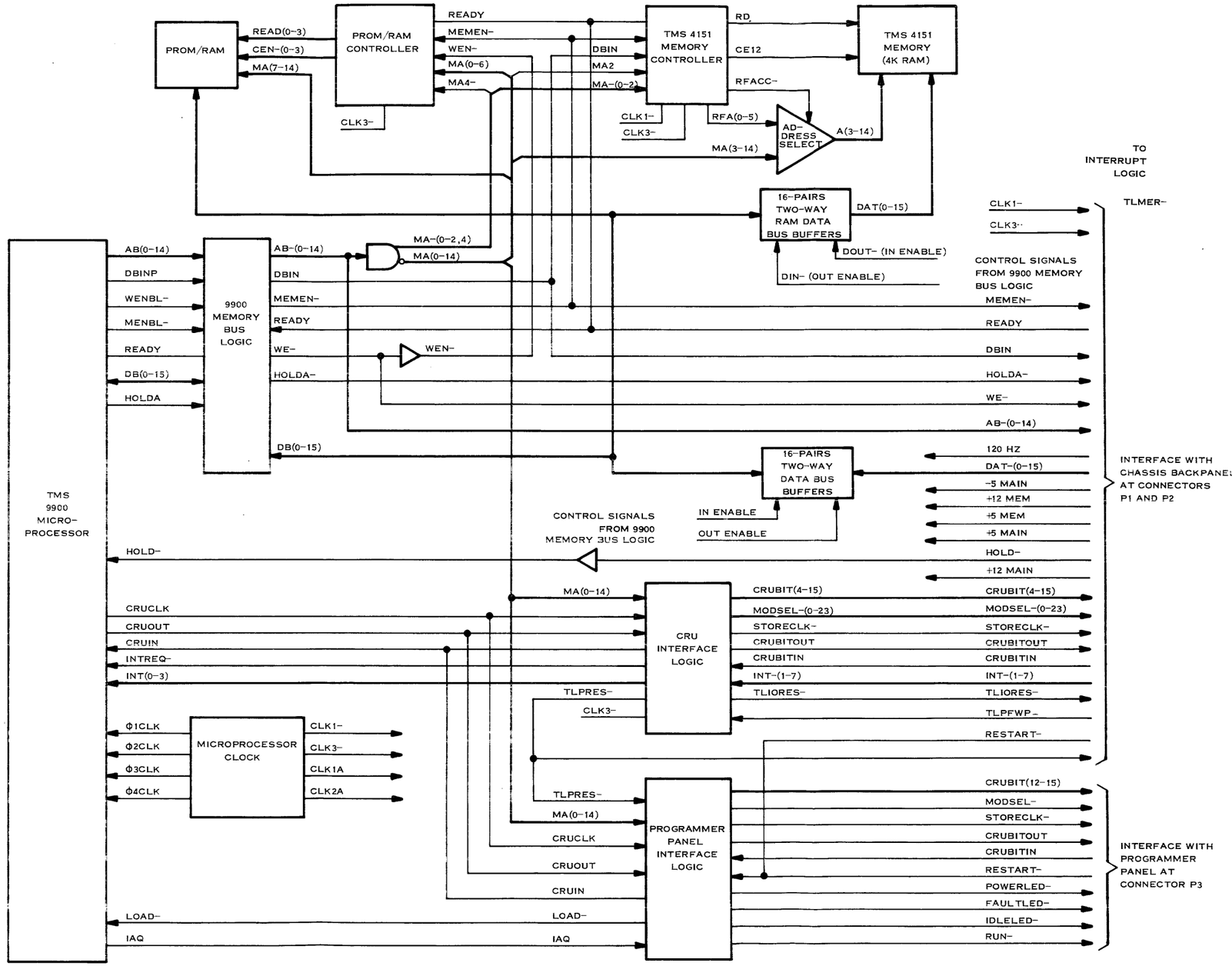
3.2.1.1 **Architecture.** The memory word of the TMS 9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits each. The instruction set of the TMS 9900 allows both word and byte operands. Thus, all memory word locations are on even byte address boundaries. Byte instructions can address either the even or odd byte. The memory space is 65536 bytes or 32768 words. Word and byte formats are as shown in figure 3-3.

Registers and Memory. The TMS 9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal hardware registers as program data registers. The TMS 9900 memory map is shown in figure 3-4. The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory. Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the interrupt mask level and status information pertaining to the instruction operation. Each bit in the register signifies a particular function or condition that exists in the microprocessor. Figure 3-5 illustrates the bit position assignments. Some instructions use the status register to check for a prerequisite condition, others affect the values of the bits in the register, and others load the entire status register with a new set of parameters. A description of the instruction set contained in the Model 990 Computer Assembly Language Programmer's Guide details the effect of each instruction on the status register. The workspace pointer register (WP) contains the address of the first word in the currently active set of workspace registers. A workspace register file occupies 16 contiguous memory words in the general memory area (see figure 3-4). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. Some workspace registers take on special significance during execution of certain instructions. Table 3-2 lists each of these dedicated workspace registers and the instructions that use them. During instruction execution, the processor addresses any registers in the workspace by adding the register number to the contents of the workspace pointer as shown in figure 3-6.

The workspace concept is particularly valuable during operations that require a context switch (a change from one program to another or to a subroutine, as in the case of an interrupt). Such an operation using a conventional multiregister arrangement requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the contents of the program counter, status register, and workspace pointer, the microprocessor accomplishes a complete context switch with only three store cycles and two fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine, and the contents of the WP, PC, and ST registers from the previous routine have been saved in new workspace registers 13, 14, and 15, respectively. A corresponding saving in time occurs when the original context is restored. Instructions in the microprocessor that result in a context switch include:

- Branch and Load Workspace Pointer (BLWP)
- Return from Subroutine (RTWP)
- Extended Operation (XOP)

Device interrupts, RESET-, and LOAD- also cause a context switch by forcing the microprocessor to trap a service subroutine.



(C)133175

Figure 3-1. 990/4 Circuit Board Block Diagram

Table 3-1. TMS 9900 Microprocessor Characteristics

Item	Characteristic
Word size	16 bits
Maximum memory	32K words
Clock rate	3 MHz
Instruction cycle time	Average- 5 microseconds
	Minimum- 2 microseconds
	Maximum- 31.5 microseconds
Addressing modes	Immediate
	Workspace register
	Workspace register indirect
	Symbolic memory (direct)
	Indexed memory
	Workspace register indirect auto-increment
	Program Counter Relative
	CRU Relative
Interrupts	16 capability, only 8 implemented on 990/4 circuit board
Registers	16
Input/Output	Direct (CRU) and Direct Memory Access (DMA)
Address bus	15 bits
Data bus	16 bits
Power	+12 vdc, ±5 vdc
Package	64 pins, dual-in-line package
Technology	N-channel silicon gate
Instruction set	5 general address modes, set includes multiply and divide

Interrupts. The TMS 9900 Microprocessor can accommodate 16 interrupt levels with the highest priority level 0 and the lowest level 15. Level 0 is reserved for the RESET– function, and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements. Only levels 0 through 7 are implemented in the 990/4 configuration.

The microprocessor continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the microprocessor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15 of the new workspace. The microprocessor then forces the interrupt

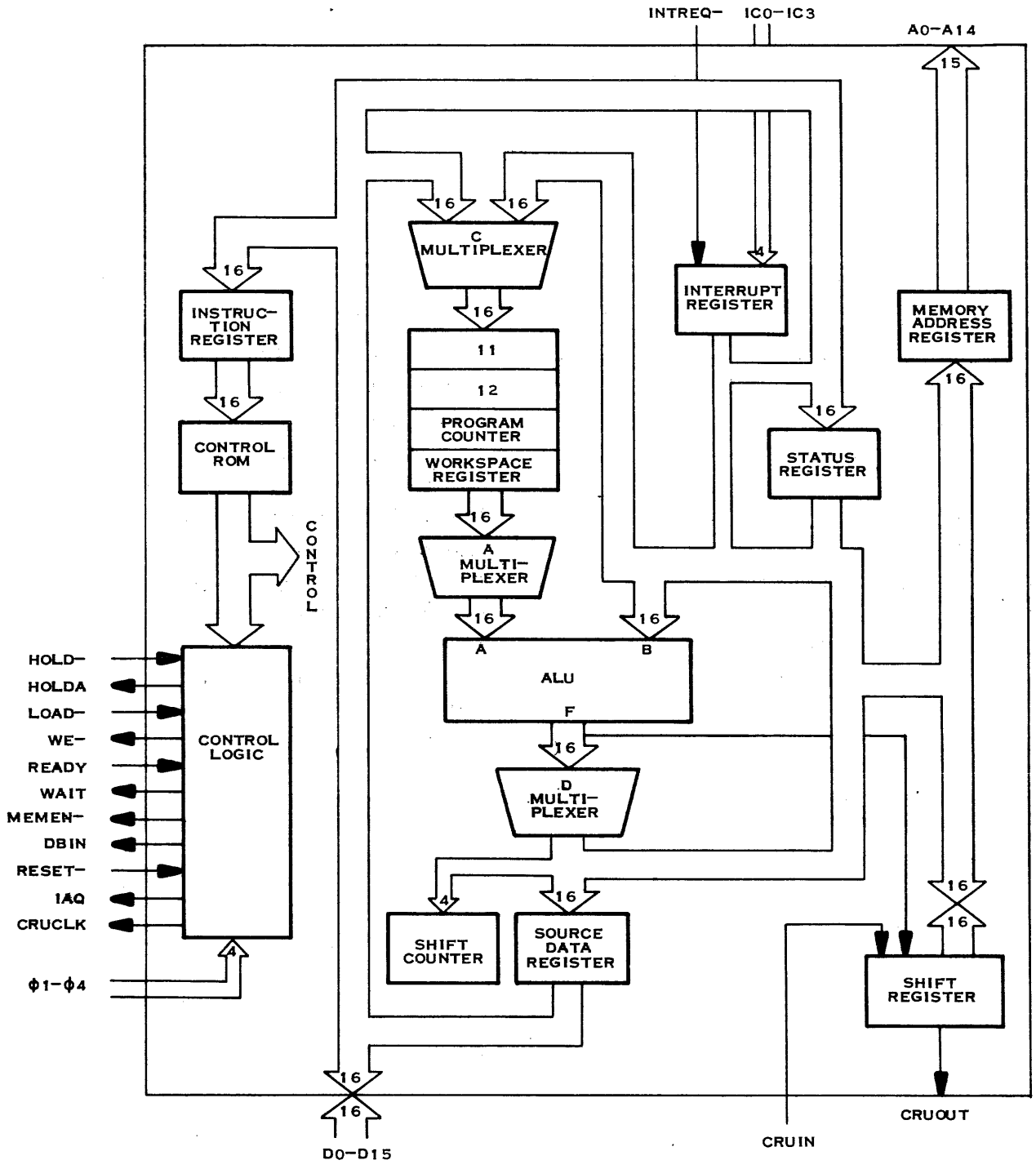


Figure 3-2. TMS 9900 Microprocessor Architecture

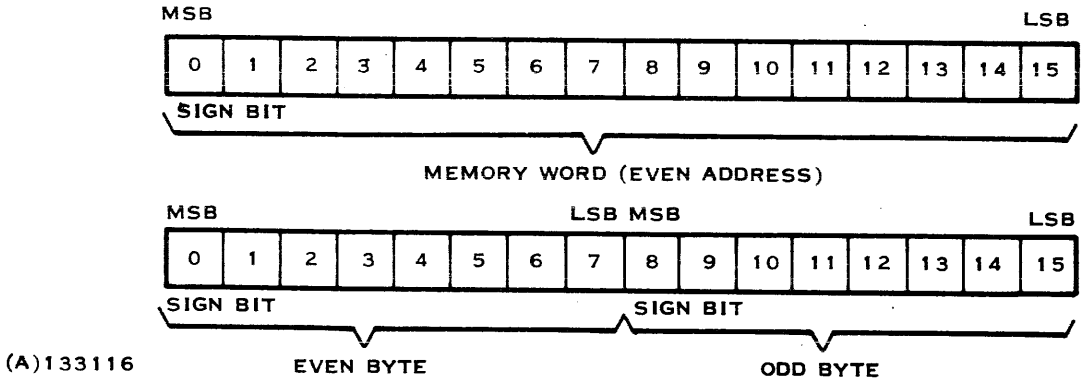


Figure 3-3. Microprocessor Word and Byte Format

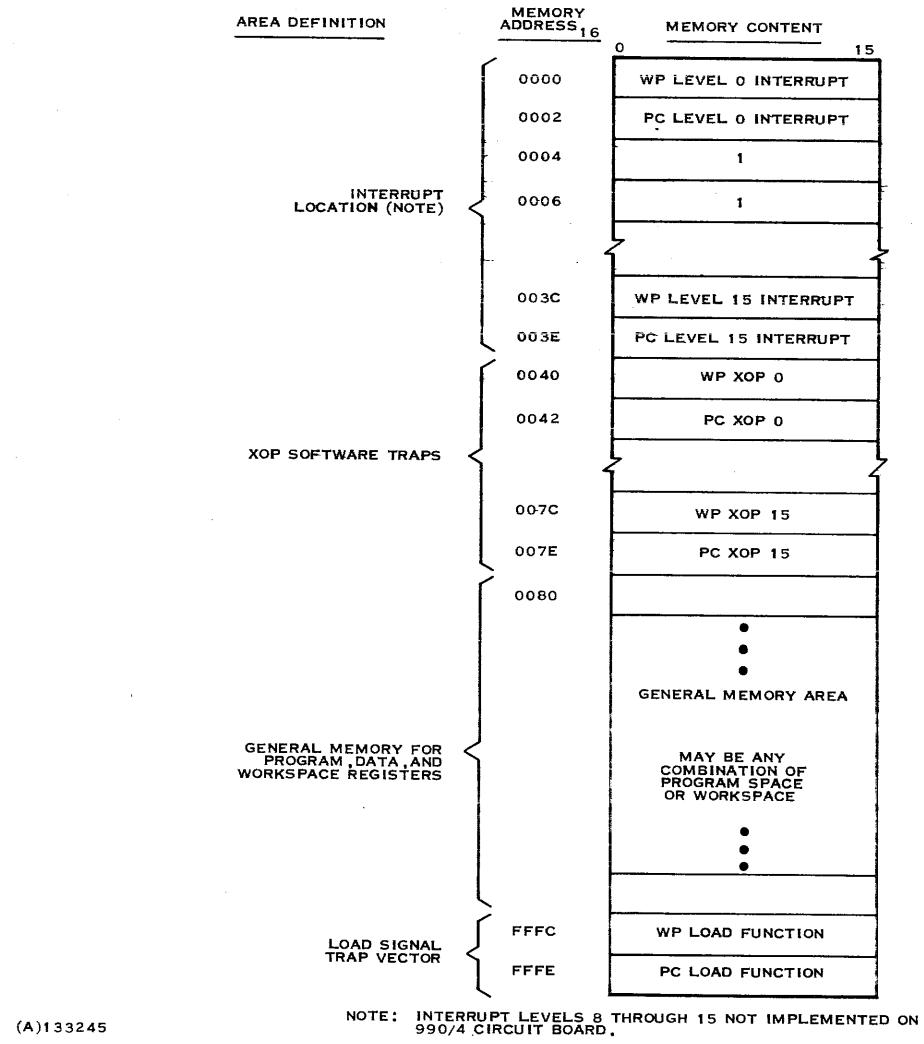


Figure 3-4. TMS 9900 Memory Map

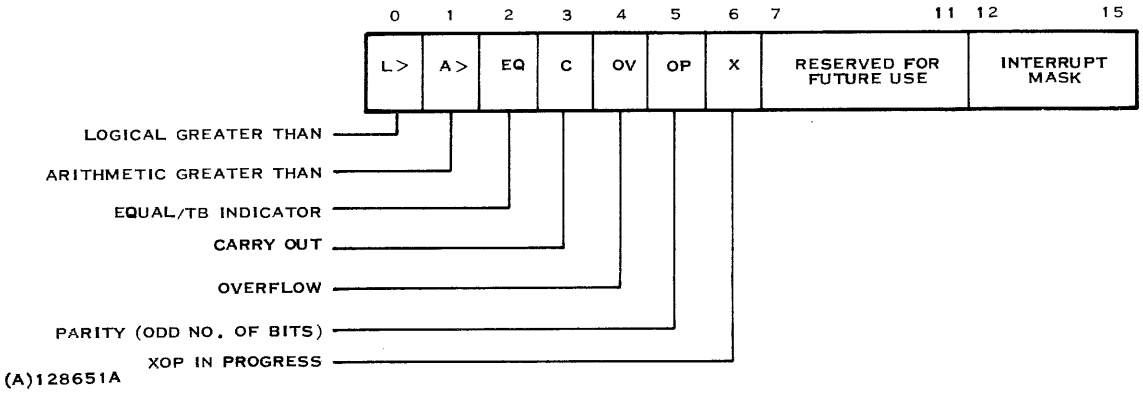


Figure 3-5. Status Register Bit Assignments

Table 3-2. Dedicated Workspace Registers

Register No.	Contents	Used During
0	Shift count (optional)	Shift instructions (SLA, SRA, SRC and SRL)
11	Return address	Branch and Link Instruction (BL)
	Effective address	Software implemented Extended Operation (XOP)
12	CRU base address	CRU instructions (SBO, SBZ, TB, LDCR and STCR)
13	Saved WP register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
14	Saved PC register	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD, and RESET)
15	Saved ST registers	Context switching (BLWP, RTWP, software XOP, recognized interrupt, LOAD and RESET)

mask to a value that is one less than the level of the interrupt being serviced, except for level 0 interrupt that loads zero into the mask. This allows only interrupts of higher priority to interrupt a service routine. The microprocessor also inhibits interrupts until the first instruction of the service routine has been executed so that program linkage is preserved should a higher priority interrupt occur. All interrupt requests should remain active until recognized by the microprocessor in the device service routine. The individual service routines must reset the interrupt requests before the routine is complete. If a higher priority interrupt occurs, a second context switch is made to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters.

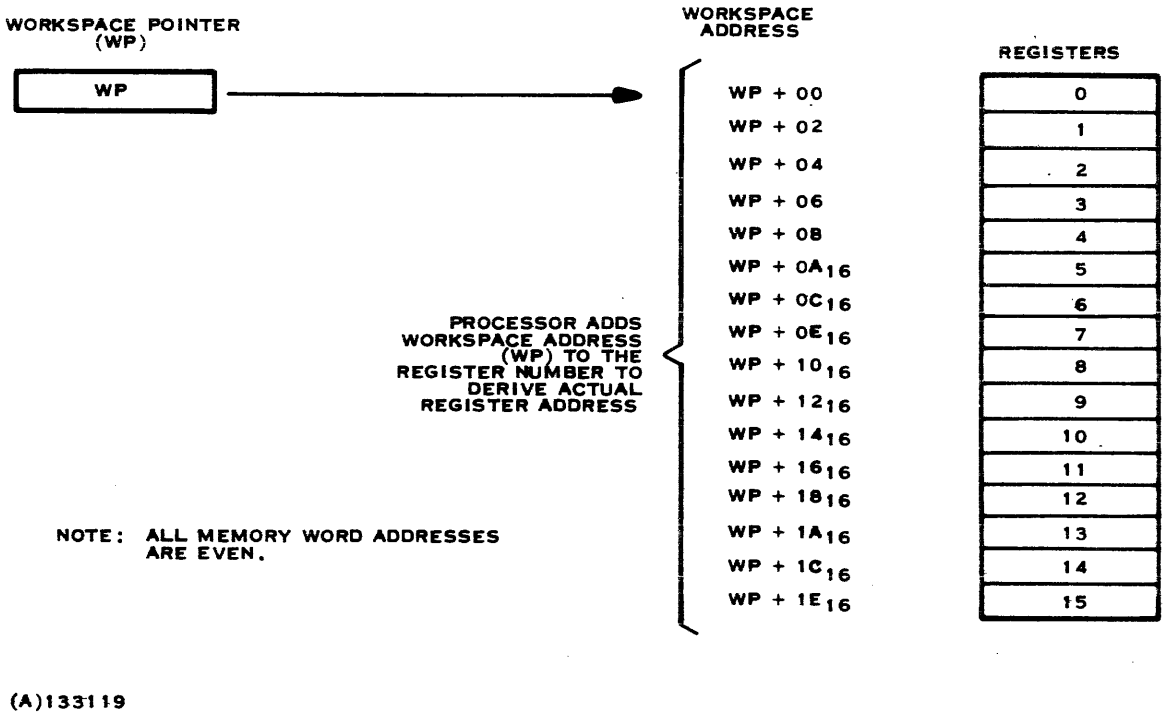


Figure 3-6. Workspace Pointer and Registers

Input/Output. The TMS 9900 Microprocessor uses a versatile direct command-driven I/O interface designated as the Communications Register Unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The microprocessor employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus at the interface to the CRU system. The microprocessor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move data between memory and CRU data fields.

Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data transaction operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of several data or status bits.

The microprocessor performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the microprocessor develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the microprocessor generates a CRUCLK pulse that indicates to the CRU device that the operation is one of output and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a ONE for SBO and a ZERO for SBZ). The test bit instruction is an input operation that transfers the addressed CRU bit from the CRUIN input line to bit 2 (equal bit, see figure 3-5) of the status register.

The microprocessor develops a CRU-bit address for the single-bit operations from the CRU base address contained in workspace register 12 (W12) and the signed displacement contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from bits 3-14 in W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 3-7 illustrates the development of a single-bit CRU address.

The microprocessor performs two multiple-bit CRU operations: store communications registers (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in figure 3-8. Although the figure shows a full 16-bit transfer operation, any number of bits from 1 to 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves 8 or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves 9 or more bits, those bits come from the right-justified field within the whole memory word. As the bits are transferred to the CRU interface, the CRU address is incremented for each successive bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves 9 to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero. When the input from the CRU device is complete, the first bit from the CRU is in the least significant bit position in the memory word or byte.

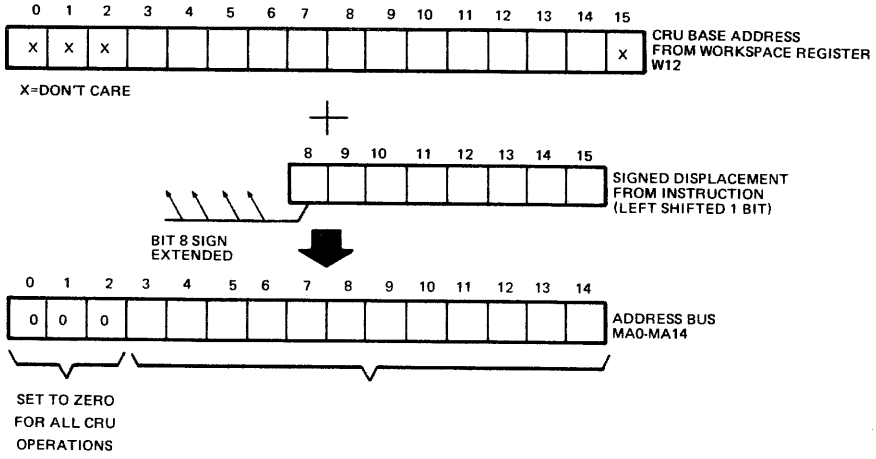


Figure 3-7. TMS 9900 Single-Bit CRU Address Development

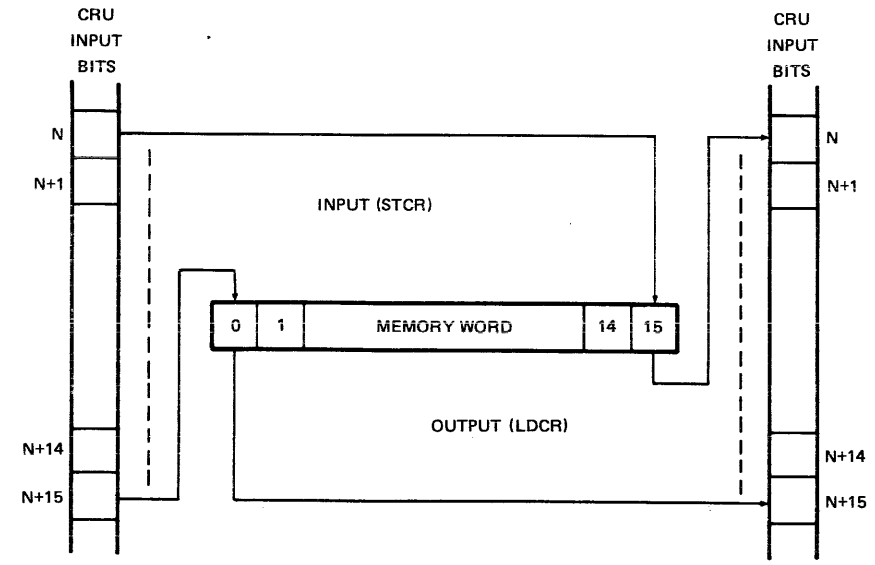


Figure 3-8. TMS 9900 LDCR/STCR Data Transfer

External Instructions. The TMS 9900 Microprocessor has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are CKON, CKOF, RSET, IDLE, and LREX. These mnemonics, except for IDLE, relate to functions that have been implemented on the 990/4 circuit board and do not restrict use of the instructions to initiate various user-defined functions in external devices. IDLE also causes the microprocessor to enter the idle state and remain until an interrupt, RESET-, or LOAD- occurs. When any of these five instructions are executed by the microprocessor, a unique 3-bit code appears on the three most significant bits of the address bus (A0 through A2) along with the CRUCLK pulse. When the microprocessor is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The external instructions codes are as shown in table 3-3.

Load Function. The LOAD- signal permits cold-start ROM loaders and front panels to be implemented for the TMS 9900 Microprocessor. When active, LOAD- causes the microprocessor to initiate a trap immediately following the instruction being executed.

Memory location FFFC is used to obtain the trap vector (WP and PC). The old PC, WP, and ST are loaded into the new workspace and the interrupt mask is set to 0000. Then, program execution resumes using the new PC and WP.

3.2.1.2 **Interface Signals.** TMS 9900 Microprocessor pin assignments and interface signal functions are as described in table 3-4.

3.2.1.3 **Timing.** A basic memory read and write cycle, a hold operation, and a CRU operation are discussed in the following paragraphs with emphasis placed on the timing of the interface signals involved in each operation.

Table 3-3. TMS 9900 Microprocessor External Instruction Codes

EXTERNAL INSTRUCTION	A0	A1	A2
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L

Memory. Timing for a memory read and memory write cycle is as shown in figure 3-9. The read cycle is shown with no wait states and the write cycle is shown with one wait state.

MEMEN- goes active (low) during each memory cycle. At the same time that MEMEN- is active, the memory address appears on address bus bits A0 through A14. If the cycle is a memory read cycle, DBIN will go active (high) at the same time MEMEN- and A0 through A14 become valid. The memory write signal WE- will remain inactive (high) during a read cycle. If the read cycle is also an instruction acquisition cycle, IAQ will go active (high) during the cycle.

The READY signal, that allows extended memory cycles, is shown high during $\phi 1$ of the second clock cycle of the read operation. This indicates to the TMS 9900 that memory read data will be valid during $\phi 1$ of the next clock cycle. If READY is low during $\phi 1$, then the TMS 9900 enters a wait state suspending internal operation until a READY is sensed during a subsequent $\phi 1$. The memory read data is then sampled by the TMS 9900 during the next $\phi 1$ to complete the memory read cycle.

At the end of the read cycle, MEMEN- and DBIN go inactive (high and low, respectively). The address bus may also change at this time, however, the data bus remains in the input mode for one clock cycle after the read cycle.

A write cycle is similar to the read cycle with the exception that WE- goes active (low) as shown in figure 3-9 and valid write data appears on the data bus at the same time the address appears. The write cycle is shown as an example of a one-wait-state memory cycle. READY is low during $\phi 1$ resulting in the WAIT signal shown.

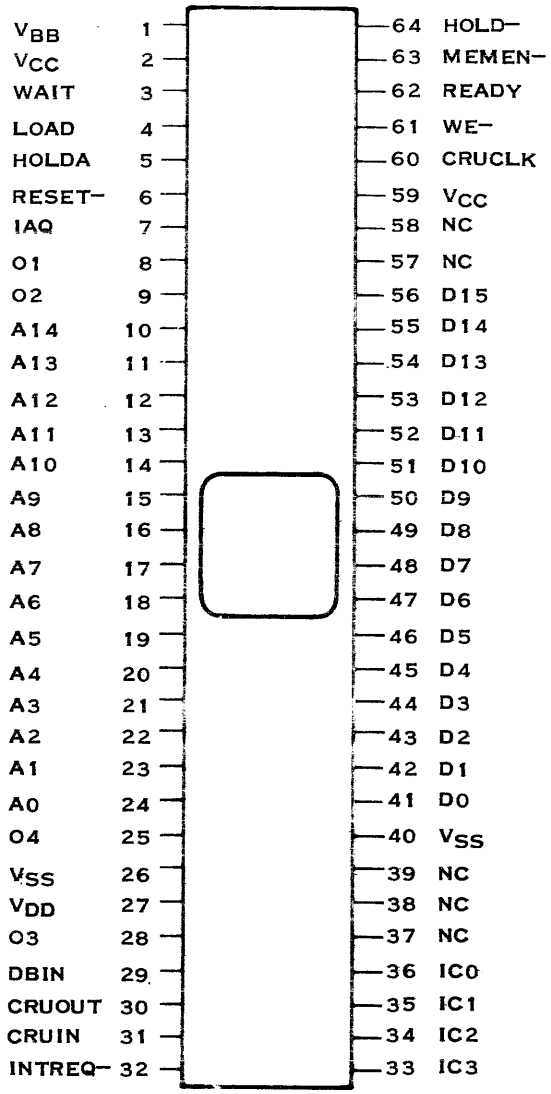
Hold. Other interfaces may use the TMS 9900 Memory Bus by causing the microprocessor to go into a hold operation. The timing for interface signals involved in a hold operation is as shown in figure 3-10. When HOLD– is active (low), the TMS 9900 enters the hold state at the next available nonmemory cycle clock period. The TMS 9900 will not enter a hold state during CRU bit-transfer sequences. When the TMS 9900 has entered the hold state, HOLDA goes active (high), and A0 through A14, DO through D15, DBIN and WE– go into a high impedance state to allow external devices to use the memory bus. When HOLD– goes inactive (high), the TMS 9900 resumes processing as shown.

CRU Operation. CRU interface timing for the 990/4 CRU bus is as shown in figure 3-9. The timing for transferring two bits out and one bit in is shown. These transfers would occur during the execution of two CRU instructions. The other cycles of the instruction execution are not shown. During a CRU-bit output operation, the CRU-bit address is placed on the address bus A0 through A14 and the actual bit data on the CRUOUT line. During the second clock cycle, a CRU pulse is supplied by CRUCLK. This process is repeated until the number of bits specified by the instruction have been transferred.

Table 3-4. TMS 9900 Pin Assignments and Functions

SIGNATURE	PIN	I/O	DESCRIPTION
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise
A1	23	OUT	the address bus. This 3-state
A2	22	OUT	bus provides the memory-
A3	21	OUT	address vector to the exter-
A4	20	OUT	nal-memory system when
A5	19	OUT	MEMEN- is active and I/O-
A6	18	OUT	bit addresses and external-
A7	17	OUT	instruction addresses to the
A8	16	OUT	I/O system when MEMEN-
A9	15	OUT	is inactive. The address bus
A10	14	OUT	assumes the high-impedance
A11	13	OUT	state when HOLDA is active.
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise
D1	42	I/O	the bidirectional 3-state data
D2	43	I/O	bus. This bus transfers mem-
D3	44	I/O	ory data to (when writing)
D4	45	I/O	and from (when reading) the
D5	46	I/O	external-memory system
D6	47	I/O	when MEMEN-is active. The
D7	48	I/O	data bus assumes the high-
D8	49	I/O	impendance state when
D9	50	I/O	HOLDA is active.
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{SS}	26, 40		Ground reference
V_{BB}	1		Supply voltage (-5 V NOM)
V_{CC}	2, 59		Supply voltage (5 V NOM)
V_{DD}	27		Supply voltage (12 V NOM)
			CLOCKS
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

TMS 9900 PIN ASSIGNMENTS



NC-NO CONNECTION

Table 3-4. TMS 9900 Pin Assignments and Functions (Continued)

SIGNATURE	PIN	I/O	DESCRIPTION
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the TMS 9900 has disabled its output buffers to allow the memory to place memory-read data on the data during MEMEN-. DBIN remains low in all other cases except when HOLDA is active.
MEMEN-	63	OUT	Memory enable. When active (low), MEMEN- indicates that the address bus contains a memory address.
WE-	61	OUT	Write enable. When active (low), WE- indicates that memory-write data is available from the TMS 9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
INTREQ-	32	IN	Interrupt request. When active (Low), INTREQ- indicates that an external interrupt is requested. If INTREQ- is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the TMS 9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. INTREQ- should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the requested interrupt.
IC0 (MSB) IC1 IC2 IC3 (LSB)	36 35 34 33	IN IN IN IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when INTREQ- is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.

Table 3-4. TMS 9900 Pin Assignments and Functions (Continued)

SIGNATURE	PIN	I/O	DESCRIPTION
			MEMORY CONTROL
HOLD-	64	IN	Hold. When active (low), HOLD- indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The TMS 9900 enters the hold state following a hold signal when it has completed its present memory cycle or CRU output. The hold operation is inhibited for any bit-transfer sequence during a CRU-instruction execution. The processor then places the address and data buses in the high-impedance state (along with WE-, MEMEN-, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When HOLD- is removed, the processor returns to normal operation.
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs (WE-, MEMEN-, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the TMS 9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the TMS 9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the TMS 9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
LOAD-	4	IN	Load. When active (low), LOAD- causes the TMS 9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. LOAD- will also terminate an idle state. If LOAD- is active during the time RESET- is released, then the LOAD-trap will occur after the RESET- function is completed. LOAD- should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
RESET-	6	IN	Reset. When active (low), RESET- causes the processor to be reset and inhibits WE- and CRUCLK. When RESET- is released, the TMS 9990 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. RESET- will also terminate an idle state. RESET- must be held active for a minimum of three clock cycles.

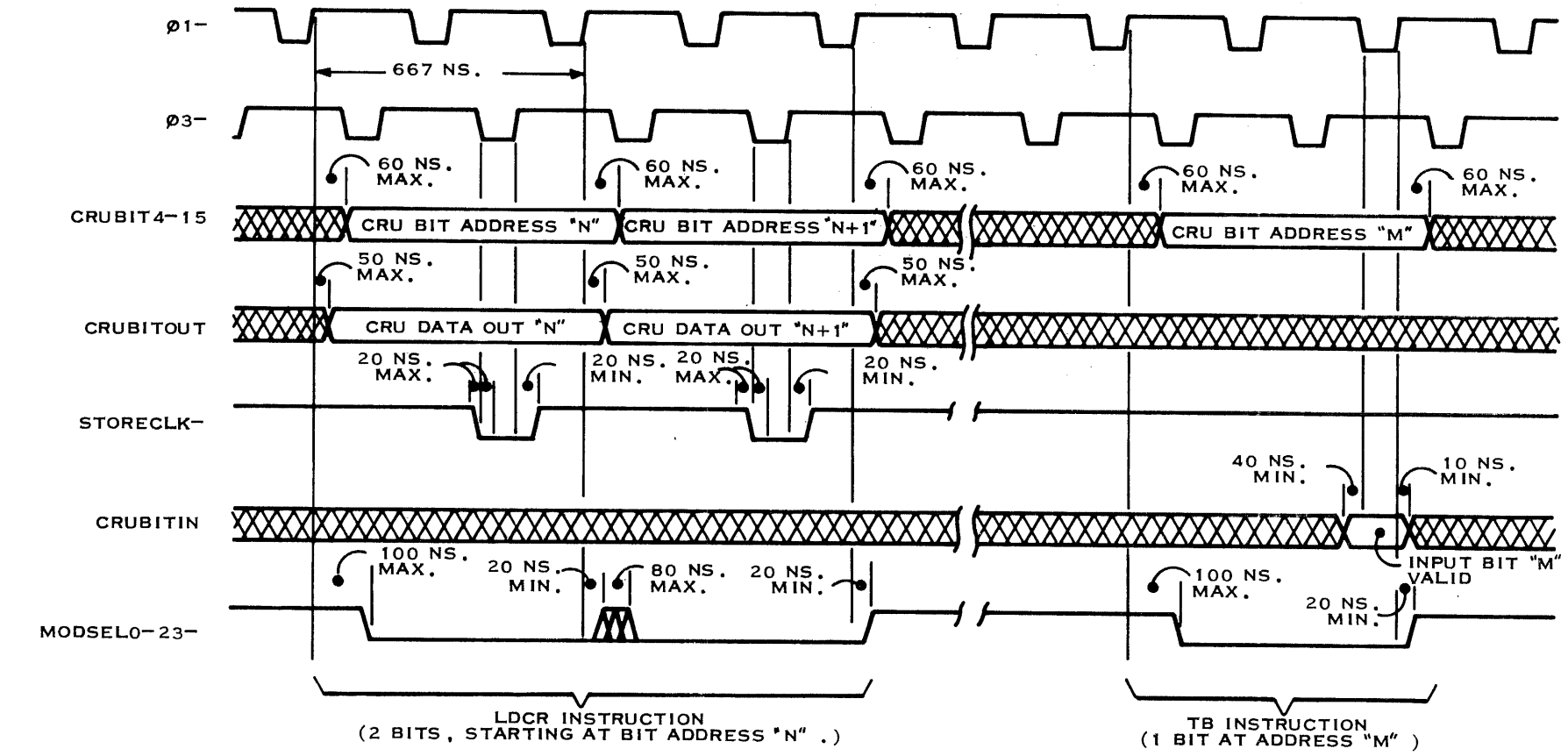


Figure 3-9. 990/4 CRU Interface Timing

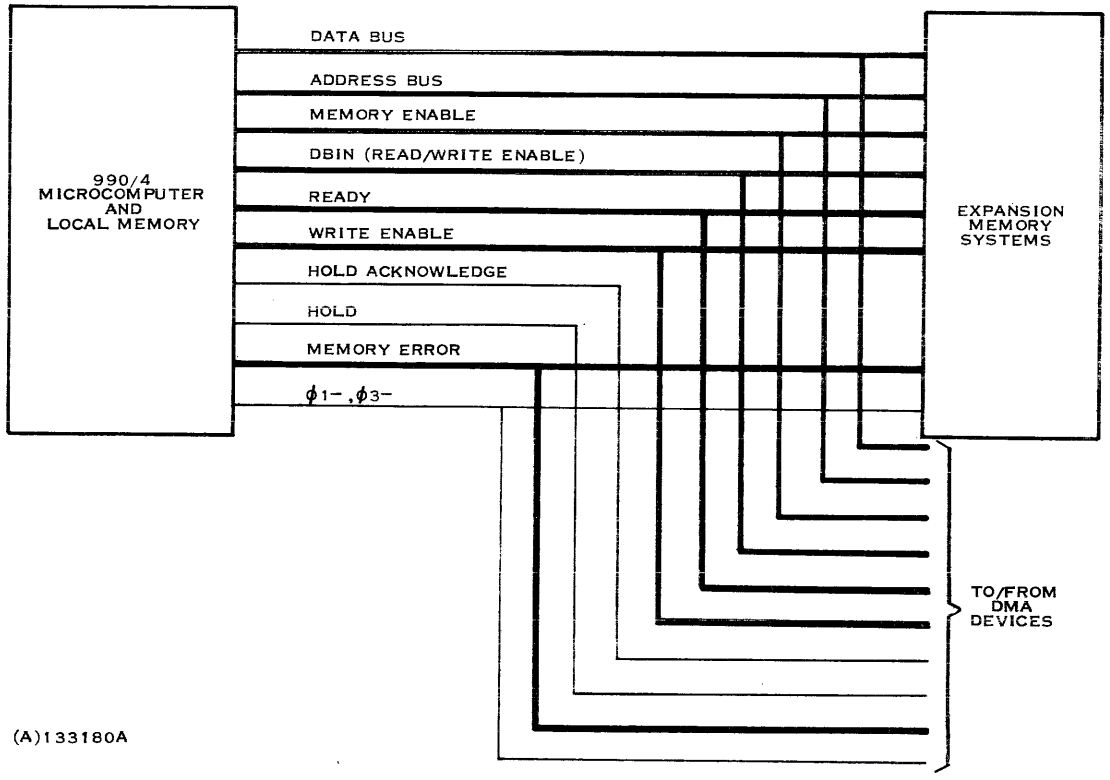


Figure 3-10. 990/4-9900 Bus Functional Diagram

The CRU input operation is similar in that the bit address appears on A0 through A14. During the subsequent cycle, the TMS 9900 accepts the bit input data as shown. No CRUCLK pulses occur during a CRU input operation.

3.2.2 **990/4 – 9900 MEMORY/DMA BUS.** The 990/4 9900 Bus is the high-speed communication resource used for transfers of data between the 990/4 and memory expansion boards, and between direct memory access (DMA) devices and memory. The 9900 Bus is routed to all chassis slots in a 990/4 Computer chassis. Memory or DMA devices may be used in any chassis slot other than the CPU slot (slot 1). 9900 Bus signals are distributed over both the P1 and the P2 connectors in each slot so that a full-sized card is required to interface the bus. Figure 3-10 is the functional diagram of the 990/4 9900 Bus, and figure 3-11 lists the signal/pin assignments for the 990 chassis.

3.2.2.1 **9900 Memory Bus Interface Signals.** A functional description of the data bus, the address bus and the control signals is provided in the following paragraphs.

Data Bus. The data bus is a 16-bit bidirectional bus used by the 990/4 to transmit data to and from the memory systems under microprocessor or DMA device control. During a 990/4 read operation, the 990/4 output data buffer is disabled while the control signal Data Bus In (DBIN) is a ONE to allow memory to place read data on the data bus. During a 990/4 write operation, the 990/4 enables write data onto the bus while DBIN = 0.

PIN	SIGNAL	
P1–	SLOT 1 WITH 990/4	ALL OTHER SLOTS
1,2	GND	GND
3,4	+5 MAIN	+5 MAIN
5,6	+12 MEM	+12MEM
7,8	+5 MEM	+5 MEM
9,10	–5 MEM	–5 MEM
11	DBIN	TLREAD
12	GND	GND
13	TLPRES–	TLPRES–
14	TLIORES–	TLIORES–
15	GND	GND
16	TLPFWP–	TLPFWP–
17	GND	GND
18	CRUBITOUT	CRUBITOUT
19	GND	GND
20	READY	TLTM–
21	GND	GND
22	STORECLK–	STORECLK–
23	MODSEL0–	SPARE
24	GND	GND
25	MEMEN–	TLGO–
26	GND	GND
27	DAT12–	DAT12–
28	DAT13–	DAT13–

PIN	SIGNAL	
P1–	SLOT 1 WITH 990/4	ALL OTHER SLOTS
29	120 HZ	120 HZ
30	DAT14–	DAT14–
31	DAT15–	DAT15–
32	CRUBIT13	CRUBIT13
33	IAQ–	SPARE
34	CRUBIT15	CRUBIT15
35	MODSEL1–	SPARE
36	CRUBIT12	CRUBIT12
37	MODSEL2–	SPARE
38	CRUBIT14	CRUBIT14
39,40	+12 MAIN	+12 MAIN
41,42	–12 MAIN	–12 MAIN
43	MODSEL3–	SPARE
44	MODSEL4–	SPARE
45	MODSEL5–	SPARE
46	MODSEL6–	SPARE
47	MODSEL7–	SPARE
48	MODSEL8–	MODSELB–
49	MODSEL9–	SPARE
50	CRUBIT7	CRUBIT7
51	MODSEL10–	SPARE
52	CRUBIT6	CRUBIT6
53	MODSEL11–	SPARE
54	CRUBIT5	CRUBIT5
55	TLMER–	TLMER–

PIN	SIGNAL	
P1–	SLOT 1 WITH SLOTS	ALL OTHER SLOTS
56	CRUBIT4	CRUBIT4
57	GND	GND
58	WE–	TLAV
59	GND	GND
60	CRUBITIN	CRUBITIN
61	MODSEL12–	SPARE
62	CRUBIT8	CRUBIT8
63	WAIT–	TLWAIT–
64	CRUBIT9	CRUBIT9
65	INT1–	SPARE
66	INT2–	INTERRUPTA–
67	MODSEL13–	SPARE
68	CRUBIT10	CRUBIT10
69	MODSEL14–	SPARE
70	CRUBIT11	CRUBIT11
71	OPEN	TLAK–
72	GND	GND
73	CLK1–	CLK1–
74	GND	GND
75	CLK3–	CLK3–
76	MODSEL15–	SPARE
77,78	+5 MAIN	+5 MAIN
79,80	GND	GND

(A)134182

Figure 3-11. 990/4 Chassis Signal Assignments – P1 Connector Pins (Sheet 1 of 2)

PIN	SIGNAL	
P2–	SLOT 1 WITH 990/4	ALL OTHER SLOTS
1,2	GND	GND
3,4	+5 MAIN	+5 MAIN
5	SPARE	HOLDA–(IN)
6	HOLDA–(OUT)	HOLDA–(OUT)
7	GND	GND
8	ADR09–	TLADR14–
9	ADR10–	TLADR15–
10	ADR05–	TLADR10–
11	ADR07–	TLADR12–
12	ADR06–	TLADR11–
13	MODSEL23–	TLPRES–
14	GND	TLIORES–
15	ADR08–	TLADR13–
16	MODSEL22–	TLPFWP–
17	ADR03–	TLADR08–
18	MODSEL21–	CRUBITOUT
19	ADR04–	TLADR09–
20	DAT11–	DAT11–
21	DAT08–	DAT08–
22	MODSEL20–	STORECLK–
23	DAT10–	DAT10–
24	INT3–	GND
25	ADR13–	TLADR18–
26	HOLD–	HOLD–

PIN	SIGNAL	
P2–	SLOT 1 WITH 990/4	ALL OTHER SLOTS
27	ADR12–	TLADR17–
28	RESTART–	SPARE
29	ADR11–	TLADR16–
30	GND	GND
31	ADR14–	TLADR19–
32	MODSEL19–	CRUBIT13
33	DAT09–	DAT09–
34	MODSEL18–	CRUBIT15
35	DAT02–	DAT02–
36	MODSEL17–	CRUBIT12
37	DAT03–	DAT03–
38	MODSEL16–	CRUBIT14
39,40	+12 MAIN	+12 MAIN
41,42	–12 MAIN	–12 MAIN
43	DAT06–	DAT06–
44	OPEN	TLADR01–
45	DAT07–	DAT07–
46	INT4–	MODSELB–
47	ADR01–	TLADR06–
48	INT5–	MODSELA–
49	ADR02–	TLADR07–
50	INT6–	SPARE
51	OPEN	TLADR02–
52	INT7–	SPARE

PIN	SIGNAL	
P2–	SLOT 1 WITH 990/4	ALL OTHER SLOTS
53	OPEN	TLADR03–
54	INT8–	SPARE
55	OPEN	TLADR00–
56	INT9–	SPARE
57	OPEN	TLADR04–
58	INT10–	GND
59	ADR00–	TLADR05–
60	GND	CRUBITIN
61	DAT04–	DAT04–
62	INT11–	SPARE
63	DAT05–	DAT05–
64	INT12–	SPARE
65	INT13–	SPARE
66	INT14–	INTERRUPTA–
67	DAT00–	DAT00–
68	INT15–	SPARE
69	DAT01–	DAT01–
70	SPARE	SPARE
71,72	–5 MEM	–5 MEM
73,74	+5 MEM	+5 MEM
75,76	+12 MEM	+12 MEM
77,78	+5 MAIN	+5 MAIN
79,80	GND	GND

(A)134183

Figure 3-11. 990/4 Chassis Signal Assignments – P1 Connector Pins (Sheet 2 of 2)

The data bus is a 3-state bus that permits configurations wherein DMA devices may have shared use of the bus. A DMA device can request the use of the 9900 Memory Bus by setting control signal HOLD– = 0. When the 990/4 recognizes the HOLD– = 0 signal, the memory cycle or CRU-bit transfer then in progress is completed, the 990/4 output buffers are forced into high-impedance state, and the HOLD ACKNOWLEDGE (HOLDA–) = 0 control signal is generated by the microprocessor to indicate that the 990/4 has relinquished use of the 9900 Memory Bus to the requesting DMA device. Each signal line of the data bus will support a load of one standard TTL device per card slot.

Address Bus. The address bus is a 15-bit wide, 3-state bus with signals labeled ADR00– through ADR14–. Signals ADR00– and ADR15– are the most significant bit (MSB) and least significant bit (LSB), respectively, of the memory address. The address bus is used by the 990/4 to transmit addresses to the memory systems. During the time when the 990/4 has relinquished use of the 9900 Memory Bus to a DMA device (HOLDA– = 0), the address buffers of the 990/4 are set to a high impedance state to permit use of the address bus by the DMA device. Each address line of the address bus will support a load of one standard TTL device per card slot.

Data Bus In (DBIN). The DBIN signal is a read/write control signal generated by the 990/4 Microprocessor chip (or DMA device controller) before initiating a memory cycle. When DBIN = 1, the memory system enables its data output buffers for a memory read operation. A memory write cycle is performed when DBIN = 0. The DBIN signal line is a 3-state line and assumes a high impedance at the 990/4 when Hold Acknowledge (HOLDA–) = 0. In this state, a DMA device may exert control. The DBIN signal should be buffered on each memory user's circuit board by an interface circuit equivalent to the Texas Instruments SN75138 IC.

Write Enable (WE–). The Write Enable (WE–) is an active low signal provided by the 990/4 or a DMA device to indicate that memory write data is available to be written into memory. This signal is buffered via receiving circuits in the memory system using an interface circuit device type such as the Texas Instruments SN75138. Write Enable is not used by standard 990/4 memory and need not be generated by DMA devices.

Memory Enable (MEMEN–). The Memory Enable (MEMEN–) control signal is an active low signal provided by the 990/4 or a DMA device to generate enables for the memory system. This control signal line also has three states, and during HOLDA– = 0 the 990/4 presents a high impedance to the line. This line should be received by the memory with a system interface circuit device such as the Texas Instruments SN75138.

READY. READY is an input control signal to the 990/4 or DMA device provided by the memory system to indicate the readiness of the memory system to read or write during the next clock cycle. The 990/4 samples the READY signal during the memory cycle on phase one of the clock, and if READY = 0 is recognized, the 990/4 sets control signal WAIT– = 0 and enters a wait state wherein internal operations are suspended until READY = 1. When READY = 1, the WAIT control signal is reset, and the microprocessor resumes operation. Though the microprocessor generates the WAIT signal, the signal is not used in the 990/4 configuration. When an external DMA device is using the memory bus, the READY signal is available to the external device to indicate the ready state of the memory. This line should be received by the user at each card slot with a system interface circuit device such as the Texas Instruments SN75138.

HOLD (HOLD–). The HOLD signal is supplied by a DMA device as an input to the 990/4. A DMA device sets HOLD– = 0 to request use of the 9900 Memory Bus. When the request is presented, the microprocessor relinquishes the memory bus to the DMA device after the first nonmemory clock cycle. The 990/4 places the address bus, the data bus, and control signals DBIN and MEMEN– in a high impedance state (i.e., floating the memory bus). Additionally, the 990/4 sets control signal HOLDA– = 0. The 990/4 keeps the memory bus floating as long as HOLD– is asserted (low), and internal microprocessor operation is suspended until HOLD– is released. The HOLD– signal should be driven by the user with an open-collector device.

Hold Acknowledge (HOLDA–). The Hold Acknowledge signal is a control signal supplied by the 990/4 that is set to 0 in response to the HOLD– = 0 signal to indicate that the 990/4 buffers driving the memory bus have been placed in a high impedance state and that the bus is available to a DMA device. HOLDA is reset to 0 when the external device relinquishes the hold on the memory bus. HOLDA– is wired serially through an AND-gate in each DMA device in a 990/4 system to determine device priority. The user load on the HOLDA control line should not exceed one standard TTL device per card slot.

Memory Error (TLMER–). The Memory Error (TLMER–) is an active-when-low control signal supplied by memory devices to indicate parity errors. Logic on the 990/4 circuit board generates a level 2 interrupt to the microprocessor in the presence of TLMER–. The user load on the TLMER– line should not exceed one device per card slot.

Wait (WAIT–). The Wait signal indicates that the 990/4 has entered a wait state because of a not-ready condition from memory. The user load should not exceed one standard TTL device per card slot.

Clock (CLK1–, CLK3–). CLK1– and CLK3– are phase one and phase three of the 990/4 System clock. The user load should not exceed one standard TTL device per card slot.

Restart (RESTART–). The Restart signal causes an unmaskable interrupt through the trap vector at location $FFFC_{16}$. This is normally a ROM address, and in standard 990/4 Systems, it contains the code which operates the programmer panel. The Restart signal is normally generated by the HALT button on the panel. Dedicated 990/4 applications with user-supplied ROM at $FFFC_{16}$ may use the restart line to initialize special functions programmed in the ROM. The Restart signal is filtered in the 990/4 to eliminate switch bounce so that either TTL or a mechanical switch can generate it. Restart may be interfaced in the backpanel or at the 20-pin top-edge ribbon connector of the 990/4 board.

Instruction Acquisition (IAQ–). The Instruction Acquisition signal indicates that the current memory cycle is an instruction acquisition cycle. The user load should not exceed one standard TTL device per card slot.

Power Reset (TLPRES–). Power Reset is a normally high signal generated by the power supply that goes low at least 10 microseconds before any dc power voltage begins to fail due to normal shutdown or ac power failure. This signal remains low on power turn-on until after all dc power voltages are stable. The user load should not exceed 10 standard TTL devices per card slot.

I/O Reset (TLIORES–). I/O Reset is a 333-nanosecond active low pulse generated by the 990/4 during execution of the I/O Reset instruction or whenever Power Reset is asserted. The user load should not exceed one standard TTL device per card slot.

Power Failure Warning (TLPFWP–). Power Failure Warning is generated by the 990/4 power supply to indicate that a power shutdown sequence is about to occur. This signal goes low at least 7 milliseconds before Power Reset is asserted. The leading edge of this pulse causes the 990/4 to trap via the power failure trap vector. User load should not exceed one standard TTL device per card slot.

120-Hertz Clock (120HZ). The 120-Hertz Clock signal is generated by the power supply to furnish the 990/4 with timing for the Real-Time Clock interrupt (level 5).

Interrupts (INT1– through INT7–). Seven interrupt signal lines are available for interrupt stimuli to the 990/4. A logic low on one of these lines will cause the 990/4 to trap through the appropriate trap vector unless the interrupt level is masked by the status register.

3.2.2.2 Memory Bus Operation. The 9900 Memory Bus operates in one of three modes: the memory read, the memory write or the microprocessor hold mode of operation. The description that follows discusses each mode of operation separately and is based on the timing diagram, figure 3-12, and the simplified logic diagram, figure 3-13.

Memory Read Mode. To perform a memory read cycle, the microprocessor sets up the memory address and the required control signals. The memory read operation may be performed from the local programmable ROM/RAM, the 4K words of TMS 4051 dynamic RAM that is mounted on the 990/4 circuit board, or from the memory expansion system via lines external to the circuit board (if memory expansion has been included for the 990/4 configuration in use).

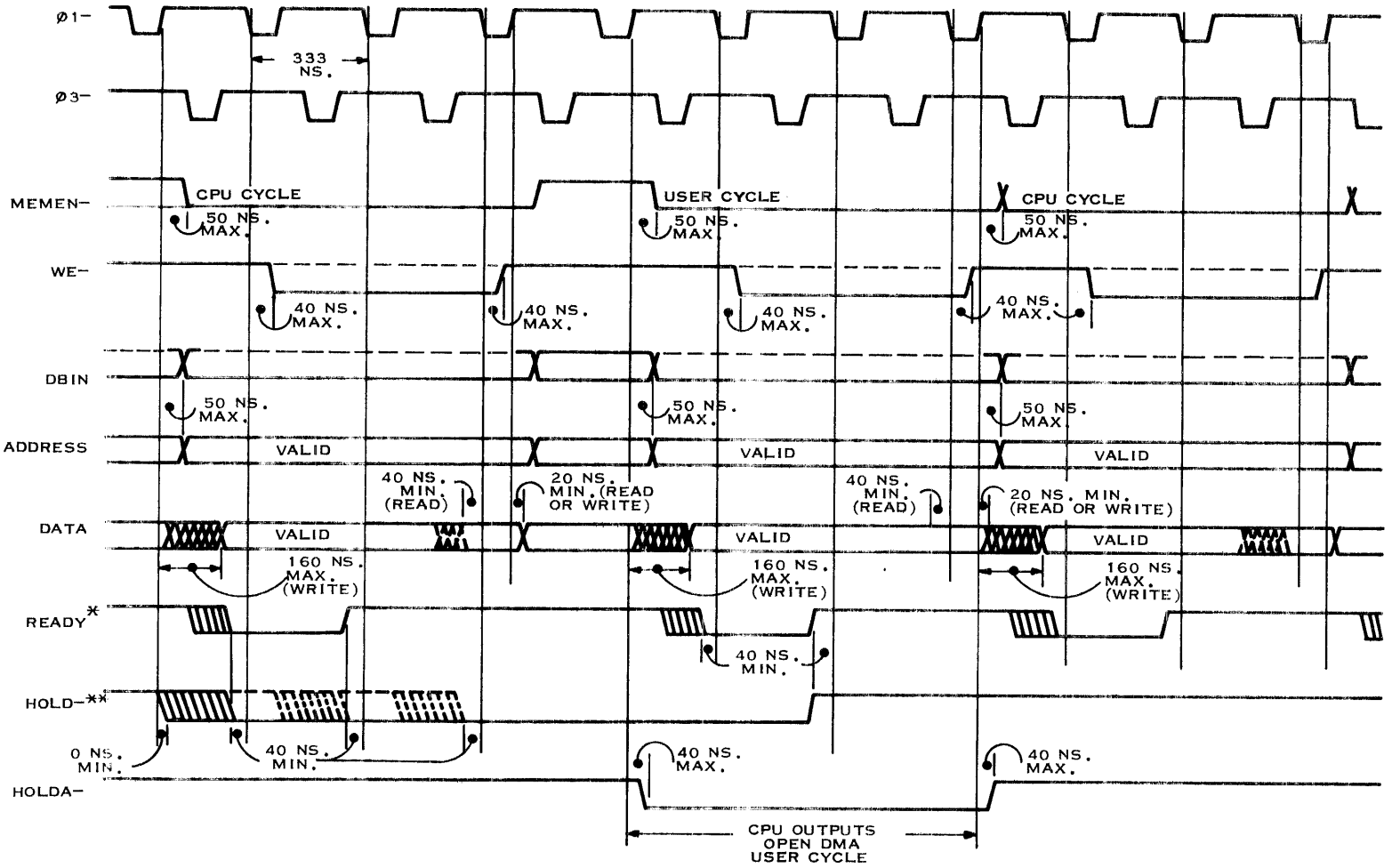
At the beginning of the memory read cycle, the microprocessor places a valid memory address on the address bus, sets DBIN control signal high, and sets control signal MEMEN- low. The low MEMEN- signal is applied to controller logic of the addressed memory to generate a chip enable signal. The high DBIN control signal indicates to the enabled memory that the cycle to be performed is a memory read operation.

The addressed memory responds to the memory request by generating a high READY input to the microprocessor and memory data is accepted.

Memory Write Mode. The memory write cycle is very similar to the memory read cycle as the microprocessor sets up the memory address and required control signals. The memory write operation may be to the 4K words of TMS 4050 dynamic RAM mounted on the 990/4 circuit board or to the memory expansion system via external lines.

At the beginning of the memory write cycle the microprocessor places a valid memory address on the address bus, sets DBIN control signal low, and sets control signal MEMEN- low. As during the memory read cycle, the low MEMEN- signal is applied to controller logic of the addressed memory to generate a chip enable signal. The low DBIN control signal indicates to the enabled memory that the memory cycle to be performed is a memory write operation. The addressed memory responds by generating a high READY input to the microprocessor and write data is made available on the data bus.

Microprocessor Hold Mode. An external device may request use of the 9900 memory bus by setting control line HOLD- low. When the microprocessor recognizes the logic 0 at the HOLD- input, the microprocessor completes the current memory cycle or CRU bit transfer and enters the microprocessor hold mode. In the hold mode of operation, the microprocessor temporarily suspends processing activity and forces the address bus, the data bus, and control signals DBIN and MEMEN- to a high impedance state (floats the outputs). The microprocessor sets the the hold



**THE CPU WILL ACKNOWLEDGE HOLD AFTER THE FIRST NON-MEMORY CLOCK CYCLE. AT THIS TIME THE CPU OUTPUTS WILL FLOAT AND THE USER MAY ASSERT MEMEN–, DBIN, ADDRESS (AND DATA AND WE FOR A WRITE CYCLE).

*MEMORY CYCLES SHOWN HERE HAVE ONE WAIT CYCLE EACH. ACTUAL MEMORY MAY TAKE MORE OR LESS TIME.

(A)134181

Figure 3-12. 990/4-9900 Bus Timing

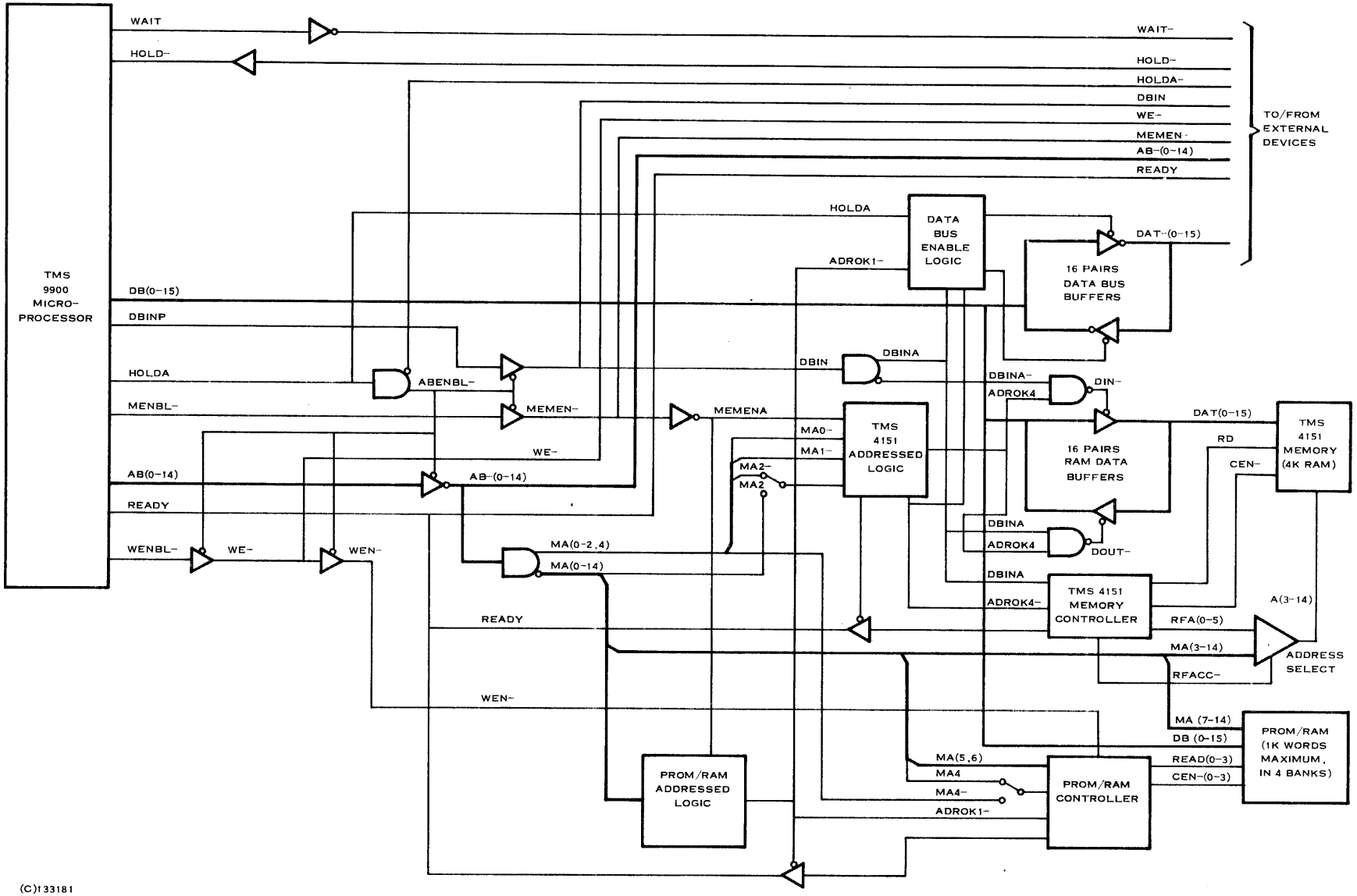


Figure 3-13. Simplified Logic Diagram of 9900 Memory Bus

acknowledge control signal HOLDA to 1 to indicate to the external device that it has relinquished the memory bus. The microprocessor buffers driving the memory bus remain in a state of high impedance as long as HOLDA = 1. The external device sets control line HOLD- high to release the memory bus and the microprocessor resumes its processing activity.

3.2.3 PROGRAMMABLE ROM/RAM. A 1024-word memory is implemented as part of local memory on the 990/4 circuit board using sixteen 256-word by 4-bit devices. These devices may be either Texas Instruments type SN74S287 TTL Programmable Read-Only Memory (PROM) devices or Texas Instruments type TMS 4043 static Random-Access Memory (RAM) devices or a combination of the two. When fully implemented, the memory is organized into four banks of 256 16-bit words, each bank consisting of 4 devices. Each bank must be either all PROM or all RAM. Not all 990/4 circuit boards have the 1024-word memory fully implemented. One configuration has just one bank of 256 words of static RAM with 12 wired sockets for either PROM or RAM device implementation as required by the user. An address jumper wire determines whether the memory may be addressed at address zero or at address 31K (word address). With address jumper wire in place, the address extends from 0000_{16} to $07FE_{16}$; with jumper wire removed, the address extends from $F800_{16}$ to $FFFE_{16}$. A RAM-enable jumper wire is provided for each 256-word bank. With RAM-enable jumper wire in place, that bank of devices is enabled for PROM device operation; with jumper wire removed, the bank is enabled for RAM device operation. Parity is not used in this memory.

3.2.3.1 Memory Controller. The PROM/RAM controller, as implemented on the 990/4 circuit board, monitors the 990 Memory Bus, directs the PROM to perform read operations, and, when so equipped, directs the RAM to perform read or write operations under the direction of the microprocessor. The following description of the memory controller operation is keyed to figure 3-14.

Address Examination. An active (low) MENBL- signal from the microprocessor is inverted and applied to the memory address decoder as a high MEMENA signal. When the memory address decoder senses the high memory enable (MEMENA), it examines the four most significant bits of the address bus (MA0 through MA3) that are applied to the memory address decoder. The memory address decoder is a 4-bit magnitude comparator and memory address bits MA0 through MA3 are compared to either four high level or four low level inputs as determined by jumper wire strapping. When the input levels are high (jumper wire disconnected and memory beginning address set for $F800_{16}$) and the memory address bits MA0 through MA3 are also high, the ADROK1- output signal of the memory address decoder goes active to trigger the timing and control logic and thus generate an internal memory request. When the memory address decoder is strapped for beginning address of zero, the four input levels are low and memory address bits MA0 through MA3 must also be low to generate the ADROK1- signal. The low ADROK1- signal is also used as a control signal for the three-state external data bus drivers during a microprocessor to PROM/RAM or external DMA device to PROM/RAM read or write operation.

Memory Bank Chip Enable Decoder. The low ADROK1- signal is applied as an enabling signal to the memory bank chip enable decoder. The memory bank chip enable decoder is strapped to input memory address bit MA4- to make memory address $F800_{16}$ valid; to MA4 to make memory address 0000_{16} valid. Memory address bits MA5 and MA6 are memory bank select bits and are BCD inputs that are decoded as chip enable signals CEN0- through CEN3-. If the selected memory bank is PROM device equipped, the low chip enable signal is applied as one of two chip-select signals at the CS1 pin of the SN74S287 device. If the selected memory bank is static RAM equipped, the low chip enable signal is applied at the chip enable CE- pin of the TMS4043 device.

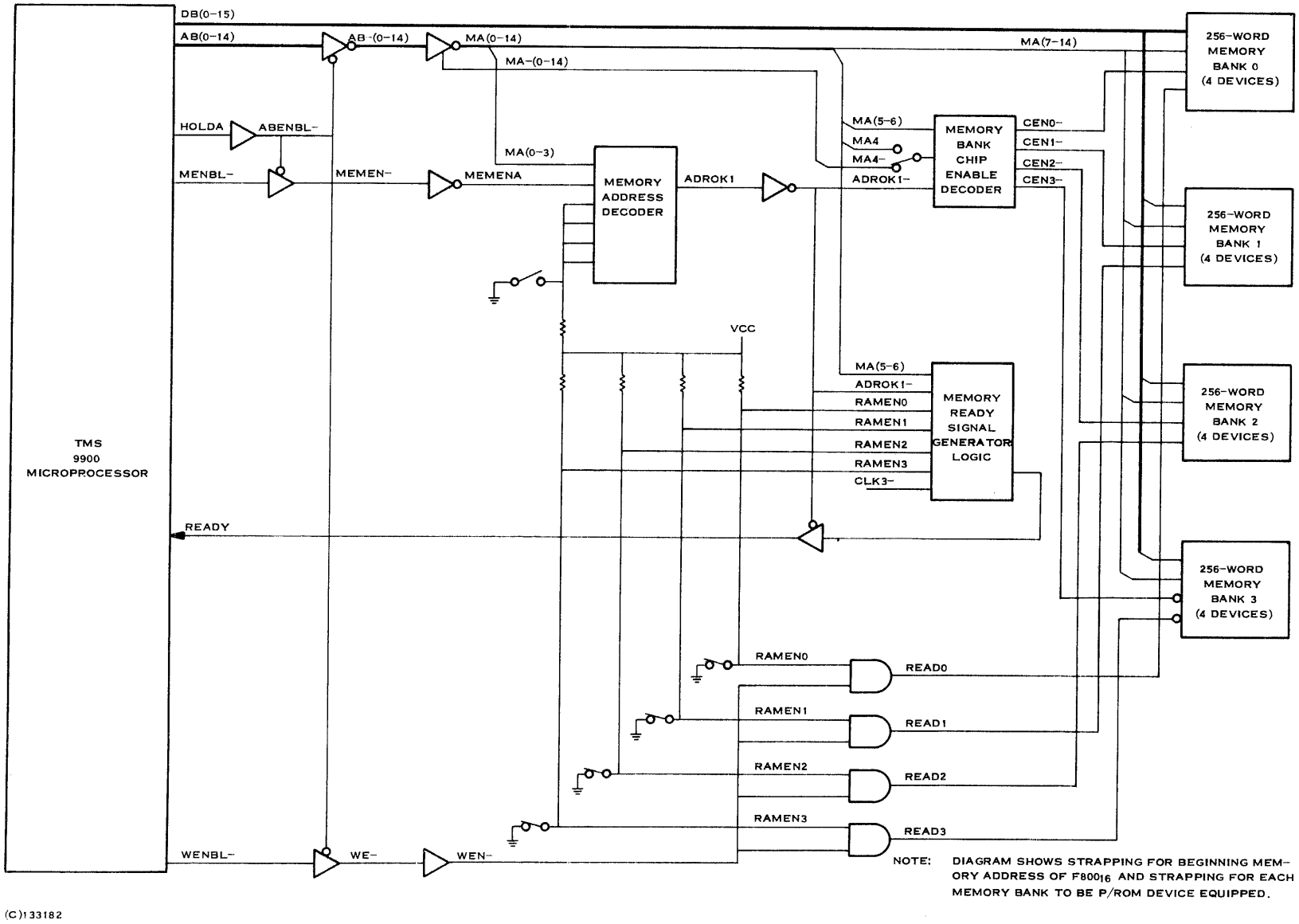


Figure 3-14. Simplified Functional Block Diagram of PROM/RAM and Controller

Memory READY Signal Generation. The low ADROK1- applies an enabling strobe to a data selector/multiplexer in the memory ready signal generator logic and the memory bank select bits, memory address bits MA5 and MA6, select one of four inputs, RAMEN0 through RAMEN3, as the output of the data selector/multiplexer. These signals are strapped low for each PROM equipped memory bank; high for each static RAM equipped memory bank. Assuming PROM operation, the low RAMEN signal for the selected memory bank is strobed out of the data selector/multiplexer to the initial D-type flip-flop in a three-stage flip-flop delay circuit. Clock signal CLK3- clocks the Q- output of the initial flip-flop without delay through a three-state driver as the memory READY signal to indicate to the microprocessor that memory will be ready to read or write during the next clock cycle. For static RAM operation, the READY signal is delayed for two clock cycles to meet the one microsecond cycle time requirements of the static MOS RAM.

The RAMEN signal, high for static RAM operation, for the selected memory bank is strobed out of the data selector/multiplexer to the input of the initial D-type flip-flop of the delay circuit. In this instance the Q- output of the flip-flop is clocked low by CLK3- and it is not until after two additional clock cycles have clocked the signal through the delay circuit that the initial flip-flop is cleared to set the READY signal high.

3.2.3.2 PROM Memory Read Operation. For PROM memory read operations, a low RAMEN signal is applied as one of two inputs to an AND gate to develop a low READ enable signal at the output of the gate. The WEN- signal at the other input to the AND gate has no function in a PROM memory read operation. The READ signal is applied to chip-select pin CS2 of the SN74S287 devices as the second of two enable signals. With the memory bank enabled, the memory word as addressed by memory address bits MA7 through MA14 is placed on the data bus for input to the microprocessor. The memory read cycle is terminated as MEMEN- from the microprocessor returns high.

3.2.3.3 Static RAM Memory Read/Write Operation. For static RAM operation the RAMEN signal for the selected memory bank applied as one of two inputs to an AND gate is high. The high WENBL- signal generated by the microprocessor during a memory read operation develops the high WEN- signal that is applied as the other input to the AND gate. The high READ signal at the output of the AND gate is applied to the read/write pin of the TMS 4043 devices and a read operation is enabled for the memory word addressed by memory address bits MA7 through MA14. For a memory write operation, WENBL- is low and a low READ signal is developed at the output of the AND gate of the selected memory bank. A low applied to the read/write pin of the memory chip enables the chip for a write operation.

3.2.4 DYNAMIC RANDOM ACCESS MEMORY (RAM). A 4096-word dynamic RAM is implemented on the 990/4 circuit board using sixteen Texas Instruments TMS 4051 integrated circuit devices. The TMS 4051 is a high-speed dynamic 4096-bit MOS circuit organized as 4096 one-bit words. As an option, odd parity is implemented by installing a seventeenth TMS 4051. Twelve address input lines allow selection of any of the 4096 bits in the storage matrix for either a read or write operation. A refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every two milliseconds to preserve data that is stored in the dynamic MOS memory storage cells. Data selectors select the refresh address lines to replace the six least significant bits of the memory address, MA9 through MA14, to refresh 1/64th of the memory during a refresh cycle. An address jumper wire determines whether the memory may be addressed at address zero or at address 4K (word address). Grounding the jumper wire at a third position disables the memory. The dynamic RAM is on the 9900 Memory Bus and so may be accessed for read and write operations by the TMS 9900 Microprocessor or by an external device also located on the memory bus.

3.2.4.1 **Dynamic RAM Memory Controller.** The dynamic RAM memory controller, as implemented on the 990/4 circuit board, monitors the 9900 Memory Bus, decodes addresses on the memory bus, and directs the dynamic RAM to perform read and write operations under the control of the 9900 Microprocessor or under the control of an external device that is on the 9900 Memory Bus. The memory controller also initiates refresh cycles to the memory. The following description of the dynamic RAM memory controller is keyed to figure 3-15.

Address Examination. The active (low) MENBL- signal from the microprocessor or from an external DMA device is inverted and applied to the memory address decoder as a high MEMENA signal. When the memory address decoder senses the high memory enable (MEMENA), it examines the three most significant bits of the address bus (MA0 through MA2) that are applied to the memory address decoder. A low 4KOK- signal is generated at the output of the memory address decoder to signify that the dynamic RAM has been addressed. The low 4KOK- signal is applied as an enabling signal to a 3-state driver. If a memory refresh cycle is not in progress, the refresh access signal RFACC input to the driver is low and when inverted provides the high READY signal to indicate to the microprocessor that the dynamic RAM will be ready to read or write during the next clock cycle.

Memory Read, Memory Write Data Bus Enable. The low 4KOK- signal generated when the memory has been addressed is inverted and applied as a high 4KOK signal to a NAND gate. With a memory refresh cycle not in progress, RFACC- at the other input to the NAND gate is high and a low ADROK4- signal is generated. The low ADROK4- is ORed with the RFACC- signal at the input to the memory cycle timer to start a memory cycle. ADROK4- is also applied to an inverter to produce a high data bus enable signal. ADROK4, that is applied as one input to two separate NAND gates. If the memory cycle initiated is to be a read from memory cycle, a high DBINP signal is generated by the microprocessor (or DMA device) to produce a high DBINA signal and a low DBINA- signal. The high DBINA is ANDed with the high ADROK4 signal to generate a low DIN- signal that is applied to sixteen 3-state drivers to enable the data bus for a memory read operation. The low DBINA- signal ANDed with the high ADROK4 signal at the input to the other NAND gate sends DOUT- high and the sixteen 3-state drivers in the memory write path of the data bus are set to high impedance. For a memory write cycle, the microprocessor generates a low DBINP signal to produce a low DOUT- signal and a high DIN- signal to enable the memory write data path of the data bus.

Memory Timer. The memory timer produces a timed enabling signal, CE, to memory for both read and write memory cycles. This includes timing for the memory refresh cycle that is in itself a memory read operation. Either a low ADROK4- signal, in the instance of a read or write operation when the memory is addressed on the address bus, or a low RFACC- signal, when a memory refresh cycle is to occur, at the input to the memory timer provides a high input to a D-type flip-flop. The next clock CLK3- pulse applied to the clock of the flip-flop clocks out a high CE signal at the Q output of the flip-flop. The high CE signal is inverted and applied as a low CE12 signal to the chip-enable pin of each of the TMS 4051 memory devices. The high CE signal is also applied as a write-enable signal at the input to a NAND gate when all other conditions for a memory write operation are met at the input to the NAND gate, and the high CE signal is applied at the D-input of a second flip-flop in the memory timer. The low CE-signal at the Q- output of the first flip-flop in the memory timer is applied to a NAND gate at the clock input to a flip-flop in the refresh cycle controller to inhibit generation of a RFACC- signal during the memory cycle in progress. The high CE input to the second flip-flop of the memory timer is clocked out as a CED signal by the second CLK3- pulse of the memory cycle. The CED signal is applied as one of two inputs to two AND gates. If the memory cycle in progress is a write operation, the RD signal input to the memory chip is low. This low is inverted and ANDed with the CED signal to generate a low cycle-end CYEND- signal. For a memory read or memory refresh cycle the RD signal is high and the CYEND- signal is not generated until CK1A that is

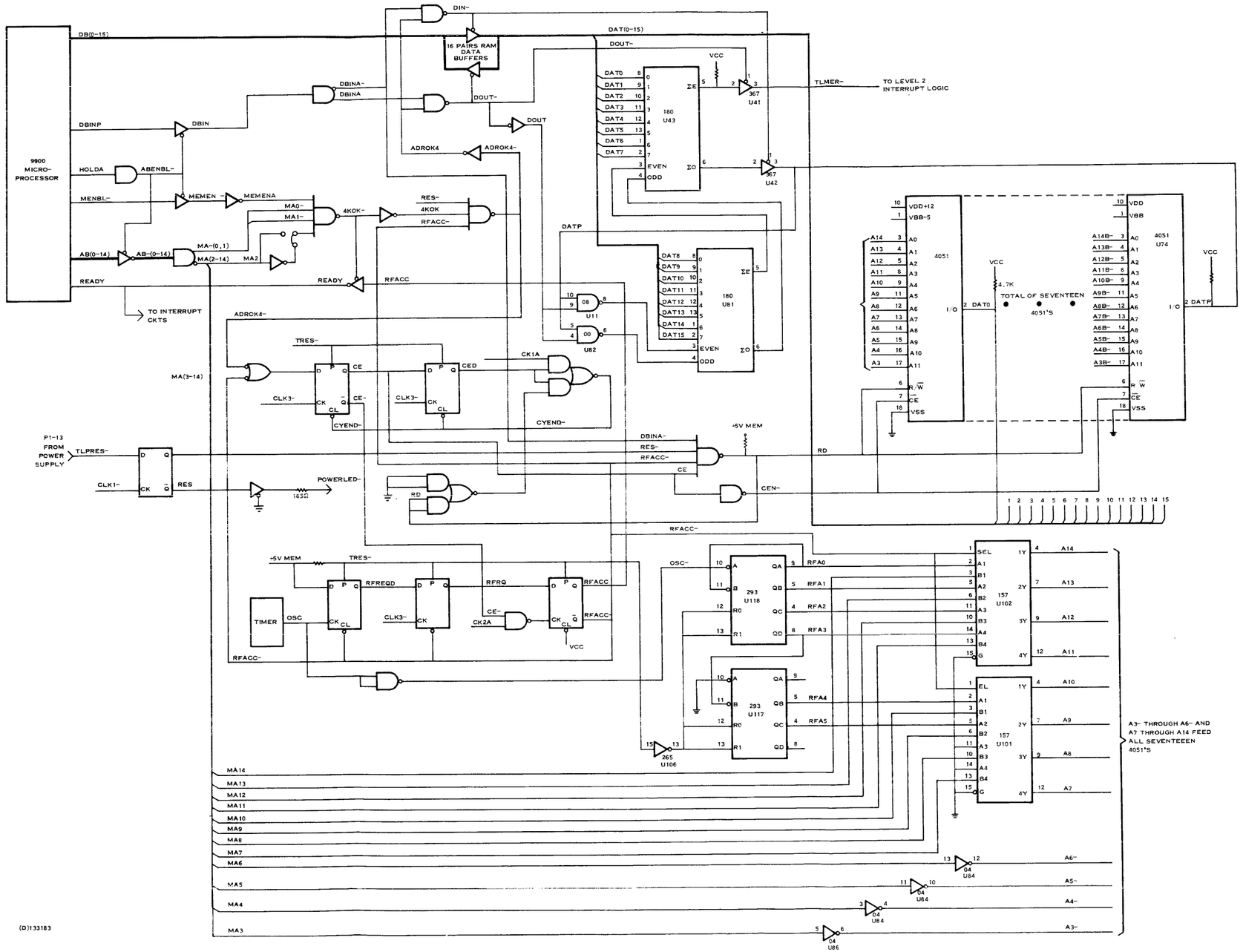


Figure 3-15. Simplified Functional Diagram of Dynamic RAM and Controller

ANDed with CED goes high 83 nanoseconds after CED is generated. In either event, CYEND- clears both flip-flops in the memory timer to remove the enabling signal from the memory chips and ready the memory timer for a new memory cycle. The timed enabling signal, CE, has a duration of 333 nanoseconds for a memory write operation and of 417 nanoseconds for a memory read operation. Memory refresh cycles are either 333 or 417 nanoseconds depending on the state of DBIN.

Refresh Cycle Controller. The refresh cycle controller consists of an RC timer, three flip-flops, a binary counter, and a data selector. The values of two external resistors and a capacitor cause the timer to run in the astable mode of operation at a frequency of 64 cycles every 2 milliseconds. The time period for each cycle is 31 microseconds; a 20 microsecond positive pulse and an 11 microsecond negative pulse. The OSC signal output of the timer is applied to a 64-count binary counter to increment the counter by one for each refresh memory cycle. The output of the binary counter is selected by the data selector during a memory refresh cycle to address each of the 64 rows of the memory devices in turn, one row for each refresh cycle. The OSC signal output of the timer is also applied to the clock of the first of three flip-flops to clock a high RFREQD that is clocked through a second flip-flop on the positive transition of clock CLK3-. If CE- is high, indicating that a memory cycle is not now in progress, the high RFRQ output of the second flip-flop is clocked through the third flip-flop by CK1A to generate the refresh access signals. The high RFACC signal applied to a 3-state driver-inverter provides a low READY signal output to indicate the not-ready state of memory if it is addressed during a refresh cycle. The low RFACC- signal is applied to the input of the memory timer as previously described and the RFACC- signal is applied to the select pin of the data selector and the data selector selects the output of the binary counter, RFA0 through RFA5, to address the memory chips at row address pins A0 through A5.

The low RFACC- signal applied to a NAND gate develops the high RD signal that sets the memory devices to the read mode of operation. Additionally, the low RFACC- signal clears the first two of the three flip-flops and on the next CK1A clock the low RFRQ signal resets the third flip-flop and the refresh cycle is ended as RFACC goes low and RFACC- goes high. The data selector returns to normal selection of memory address bits MA9 through MA14 to address row address pins A0 through A5 of the memory devices.

3.2.4.2 **Dynamic RAM Memory Read/Write Operation.** For a memory read operation, the microprocessor or external device addresses the memory and generates a high DBIN signal to enable the memory read path of the data bus. The memory devices have been enabled for a memory read or write operation by the low CEN- signal applied to chip-enable pins. The low DBINA- generated by the high DBIN is applied to a NAND gate to develop the high RD signal to set the memory devices to the memory read mode of operation and the memory word as addressed by memory address bits MA3 through MA14 is placed on the data bus for input to the microprocessor or external device, as applicable. A memory write operation occurs in the same manner except that a low DBIN signal is generated by the microprocessor or external device. The resultant high DBINA- that is ANDed with the high RES-, RFACC-, and CE signals sends RD low to set the memory devices to the memory write mode of operation and the data on the data bus is written into memory in the location addressed by memory address bits MA3 through MA14.

3.2.4.3 **Parity Generation/Parity Check Option.** Parity is implemented on the 990/4 circuit board by installing a seventeenth TMS 4051 memory device for storage of the parity bit, DATP, and by installing two Texas Instruments Type SN74180 9-bit Odd/Even Parity Generators/ Checkers that are wired for odd parity. For a memory write cycle, the data word on the data bus (DAT0 through DAT15) is applied to the two SN74180 parity generators/checkers. A parity bit (DATP) is generated that makes the total number of ONE's in the data word and the parity bit, inclusive, odd. In a memory write operation, DIN- is low to enable a 3-state driver at the

parity bit output of the parity generators/checkers. With the driver enabled and with the memory devices enabled and in the write mode, the parity bit is stored in memory as the seventeenth bit of the data word. For a memory read cycle, the data word along with its parity bit is read from memory and applied to the parity generators/checkers. The DOUT- signal that is low during a memory read operation is inverted as DOUT and used to enable an AND gate and a NAND gate at the even and odd inputs of one of the parity generators/checkers. The parity bit applied as the other input to the two gates controls the sense of the inputs to cause a low memory error signal, TLMER-, to be generated if the word read from memory is not one of odd parity. The low TLMER- causes a level two interrupt to occur.

3.2.5 MICROPROCESSOR CLOCK. Timing and control for the 9900 microprocessor, memory controllers, and interrupt logic on the 990/4 circuit board are derived from the microprocessor clock that is mounted on the 990/4 circuit board. The microprocessor clock consists of a 12-MHz oscillator, a 3-MHz clock generator, and a 4-phase clock driver as shown in the block diagram for the microprocessor clock (figure 3-16).

The oscillator is a free-running 12-MHz crystal-controlled oscillator that generates a 12-MHz output signal to drive the 3-MHz clock generator. Provision is made at the input of the oscillator to disable the oscillator and insert an external oscillator signal to drive the 3-MHz clock generator under maintenance conditions.

The 3-MHz clock generator consists of a dual D-type flip-flop and two quadruple 2-input buffers that are connected so that a frequency divide-by-four is effected and four 3-MHz clock signals and the complements to two of the clock signals are generated. As shown in the block diagram, CLK1A, CLK2A, CLK1-, and CLK3- are used directly as control signals for the 4050 memory controller, the PROM controller, external devices and the interrupt logic on the 990/4 circuit board. Additionally, the four outputs of the 3-MHz clock generator, CLK1A through CLK4A, are inputs to the 4-phase clock driver. From the four inputs, the 4-phase clock driver provides the four separate phases of the clock to the microprocessor. Each of the clock phases (ϕ1, ϕ2, ϕ3, and ϕ4) has a nominal period of 333.3 nanoseconds with a one-fifth duty cycle consisting of a high signal of approximately 67 nanoseconds duration and a low of 266 nanoseconds duration. Figure 3-17 shows the timing relationships between the four clock signals.

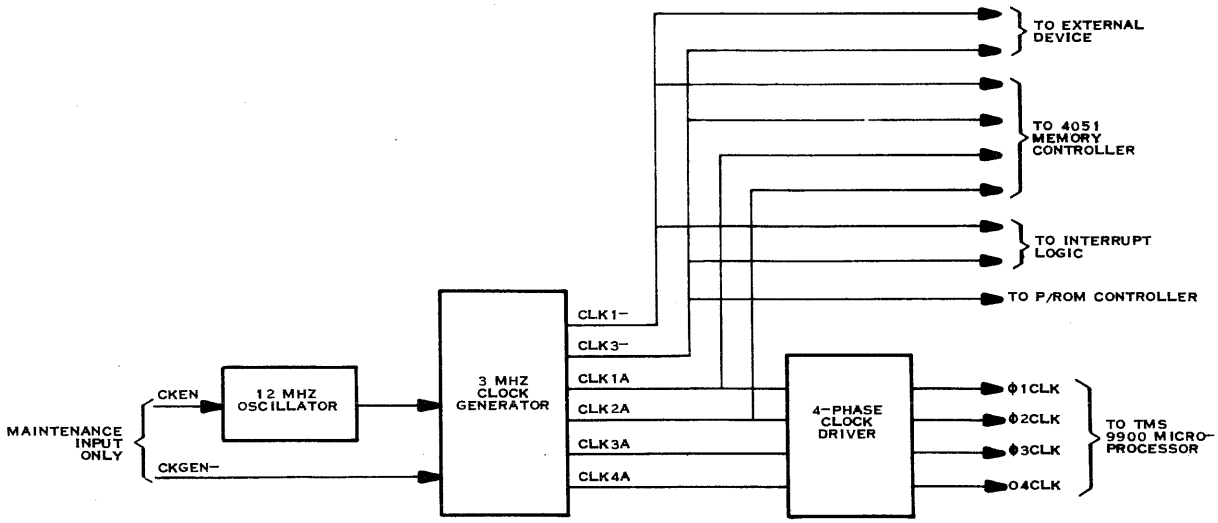


Figure 3-16. Simplified Block Diagram of Microprocessor Clock

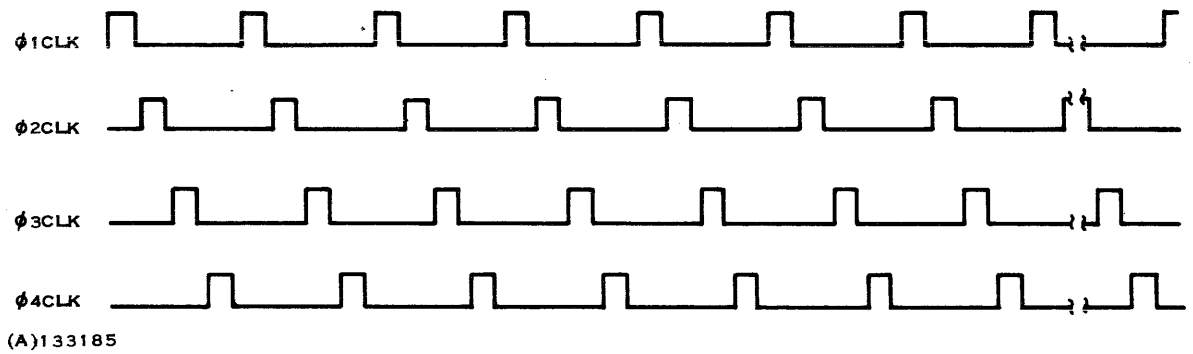


Figure 3-17. Timing Diagram, 4-Phase Clock Input to Microprocessor

3.2.6 **INTERRUPTS.** The 990/4 uses eight interrupt levels. A priority ranking system assigns numbers from 0 (highest priority) to 7 (lowest priority) to the levels so that interrupt conflicts can be resolved. The highest priority level is used for the power-up trap and seven inputs (INT1- through INT7-) for external interrupts are provided for on the 990/4 circuit board. Interrupt inputs are synchronized with the microprocessor clock on the 990/4 circuit board, are encoded, and presented to the TMS 9900 Microprocessor along with an interrupt request, INTREQ-. The interrupt levels are vectored for rapid reaction to recognized interrupts. That is, corresponding to each interrupt level is a 2-word vector located in low-order memory (addresses 00 through 1F, hexadecimal). When the TMS 9900 Microprocessor recognizes an interrupt, it loads the vector for that level into WP (first vector word) and PC (second vector word) to define the new workspace and program starting point for the interrupt servicing routine. The old values of the WP, PC, and ST are saved at the bottom of the new workspace. When the interrupt routine is complete, the microprocessor returns to the program that was executing when the interrupt occurred by restoring the original values to the PC, WP, and ST registers. Should a higher priority interrupt occur while an interrupt service subroutine is executing, the microprocessor will honor the interrupt. The microprocessor enters the higher priority interrupt subroutine and preserves the linkage to the earlier interrupt in the same manner described for the first interrupt. Thus, many interrupts can occur simultaneously with the microprocessor maintaining an orderly linkage between the interrupt programs. Table 3-5 lists the interrupt levels, assignments, vector location, and mask information. Three interrupt conditions are generated on the 990/4 circuit board and are wired directly to external interrupt INT1-, INT2-, and INT5- (or INT7-). Any of these three interrupts may be disconnected by cutting a jumper wire.

3.2.6.1 **Masking.** The microprocessor uses a 4-bit field in the status register to determine the lowest priority interrupt that will be recognized during a program operation and also to ensure that an interrupt service routine will not be halted due to another interrupt of equal or lower priority. At the start of a program the mask field in the status register is loaded with the mask value. The microprocessor compares this value continuously with any interrupts that occur. If the level of the interrupt is equal to or less than the mask value (equal or greater priority), then the microprocessor recognizes the interrupt and calls the service routine for that interrupt level. When the microprocessor sets up the service routine, it loads a value into the mask field that is one less than the interrupt level being serviced, thereby disabling interrupts from devices of equal or less priority. The enabling mask values for different interrupt levels are as shown in table 3-5.

Table 3-5. Interrupt Level Data

Interrupt Level	Vector Location (Trap Address)	Device Assignment	Enabling Mask Values
0	00	Reset	0 through F
1	04	Power failure	1 through F
2	08	Memory error	2 through F
3	0C	External device	3 through F
4	10	External device	4 through F
5	14	Real time clock*	5 through F
6	18	External device	6 through F
7	1C	External device*	7 through F

* Real time clock interrupt may be implemented at interrupt level 5 or 7 or may be disconnected. The normal configuration is for implementation at level 5.

3.2.6.2 **Interrupt Logic.** The TTL logic for implementing the seven external interrupts is located on the 990/4 circuit board and consists, in main, of two SN74174s and an SN74148 along with flip-flop circuits for setting and resetting those interrupts generated on the circuit board itself. Figure 3-18 is an extraction from the logic diagram of the 990/4 circuit board that shows circuit board interrupt logic and has been reproduced here for convenience. The SN74174s each contain six D-type flip-flops with single-rail outputs with only one of the flip-flops of the second SN74174 in use for a total of seven flip-flop circuits. The seven interrupts are applied as D-inputs to the SN74174s and are transferred to the Q-outputs on the positive transition of the CLK3- clock signal. Here they are applied as inputs to the SN74148 8-line-to-3-line priority encoder. The encoder provides a binary coded interrupt level at signals INT1 through INT3 that corresponds to the highest priority interrupt level input. With only seven interrupt levels in use at the input to the encoder, the enable output (EO) at pin 15 is not used for octal expansion but is simply inverted and applied to the microprocessor as INT0 as are signals INT1 through INT3. An interrupt, at any level, causes a low INTREQ- signal to be generated by the encoder and applied to the microprocessor.

Power Failure Interrupt. When ac power begins to fail, a sensor in the power supply generates a low TLPFWP- pulse that is applied to the 990/4 circuit board as a level 1 interrupt through a jumper wire to the I1- input of an SN74174 and the level 1 interrupt is generated. At this point, the computer has 7.0 milliseconds of program time before a power supply reset halts operation. This interrupt sets the interrupt mask in the status register to 0. The jumper wire on the circuit board may be cut to disable this interrupt. TLPRES- generated by the power supply clears the interrupts generated on the 990/4 circuit board during the power-up sequence.

Memory Error Interrupt. Logic to generate a level 2 interrupt in the event a parity error occurs in the local 4K RAM on the 990/4 circuit board or in externally implemented expansion memory is included in the interrupt logic on the 990/4 circuit board. Memory error interrupts are cleared by a CRU output to bit 12 of the programmer panel base address by a RSET instruction or by a power reset signal. The interrupt mask is set to 1 in the status register as a result of this interrupt. The jumper wire on the circuit board may be cut to disable the on-board generation of this interrupt.

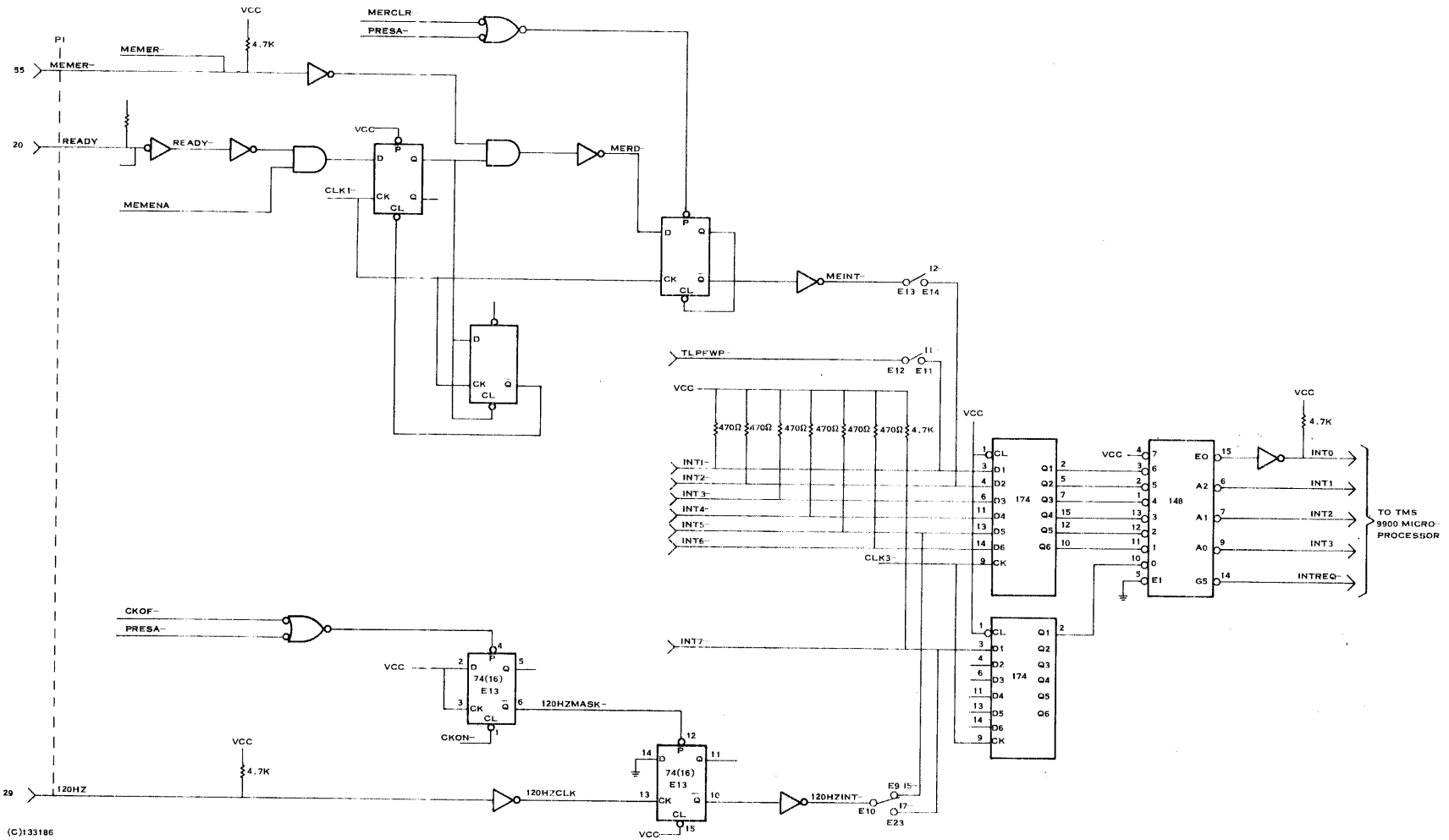


Figure 3-18. 990/4 Circuit Board Interrupt Logic

Real-Time Clock Interrupt. The power supply contains a line frequency synchronized clock that generates the 120 Hz signal. The 120 Hz real-time clock interrupt logic is implemented on the 990/4 circuit board. A signal is generated every 8.33 milliseconds to provide a level 5 interrupt request. The interrupt is enabled by a CKON- signal generated by the control instruction CKON. The interrupt is cleared by either PRESA- or CKOF- signals that are also generated by RSET or CKOF control instructions. PRESA- is also generated by the TLPRES- power-up sequence from the power supply. Though the real-time clock is normally wired for level 5 interrupt it may be wired for level 7 interrupt or may be disconnected altogether. When the level 5 interrupt is taken, the microprocessor sets the interrupt mask to 4.

External Interrupts. Interrupt levels 3, 4, 6, and 5 or 7 are available for assignment to CRU external devices. The external levels may be shared by several devices depending upon system requirements. All interrupt requests must remain active until recognized by the interrupt service routine. The individual service routines must reset the interrupt before the routine is complete.

3.2.7 EXTERNAL INSTRUCTIONS AND PROGRAMMER PANEL FUNCTIONS. The implementation of external instructions and of certain programmer panel functions on the 990/4 circuit board is as shown in figure 3-19.

3.2.7.1 External Instruction Implementation. There are five external instructions executed by the microprocessor that are implemented with TTL logic on the 990/4 circuit board. When any of the five instructions are executed, a unique 3-bit code appears on the three most significant bits of the address bus (see table 3-3) along with a CRUCLK pulse. The 3-bit code and CRUCLK pulse are applied to an SN7442A that operates as an instruction decoder as shown in figure 3-19.

IDLE Instruction. An IDLE instruction generated by the microprocessor provides a low IDLECLK- signal at the output of the SN7442A instruction decoder. The low IDLECLK- presents a flip-flop that in turn provides a low IDLE- signal at its Q- output. The low IDLE- signal is applied to the programmer panel interface as a low IDLELED- signal to illuminate the IDLE LED on the panel as an indication of microprocessor inactivity. The low IDLE- signal is ANDed with RUNQ so that when the microprocessor is in the IDLE mode a low RESTART- signal from the programmer panel (or other external device) can develop the LOAD- signal without delay causing the microprocessor to trap to the nonmaskable interrupt at memory location $FFFC_{16}$.

RSET Instruction. The RSET instruction generated by the microprocessor provides a low RSET- signal at the output of the SN7442A instruction decoder. The low RSET- applied directly to a fault flip-flop sets the FAULTED- signal high to extinguish the FAULT LED on the programmer panel. RSET- is also ORed with TLPRES- and when RSET- is low, low TLIORES- and PRESA- signals are generated. The low TLIORES- is applied to external devices via the backpanel and is used as a master reset. The low PRESA- clears the memory error interrupt and real-time clock interrupt logic on the 990/4 circuit board.

CKON and CKOF Instructions. The CKON and CKOF instructions generated by the microprocessor provide the low CKON- and CKOF- signals, respectively, at the output of the instruction decoder. CKON enables the 120 Hz real-time clock logic and CKOF clears the interrupt and inhibits the interrupt until CKON is generated by the microprocessor. After the real-time clock interrupt has been generated, a CKOF, CKON instruction sequence is required to enable a second interrupt.

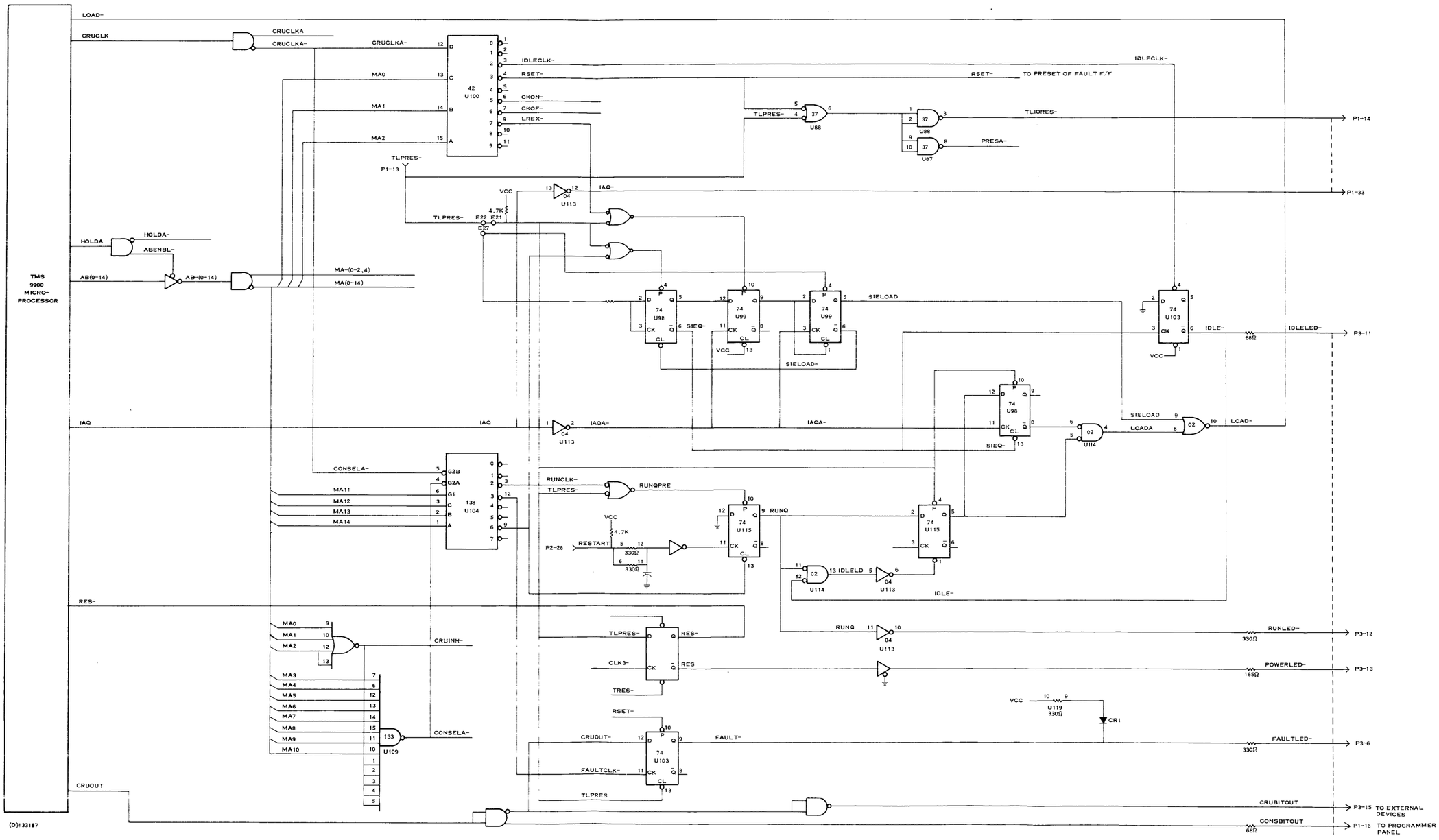


Figure 3-19. Simplified Logic Diagram of External Instructions and Programmer Panel Functions Implementation

LREX Instruction. The LREX instruction generated by the microprocessor provides a low LREX- signal at the output of the instruction decoder. The low LREX- applied to an AND gate develops a low signal that presets a flip-flop. The high at the Q-output of the flip-flop is applied to the D-input of another flip-flop. The high is clocked through the flip-flop by the instruction acquisition signal, IAQ, from the microprocessor as a high SIELOAD signal that causes a low LOAD- signal to be applied to the microprocessor causing the microprocessor to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector. The low SIELOAD- signal at the Q- output of the flip-flop clears the LOAD- signal as the microprocessor generates another instruction acquisition signal, IAQ. When strapped E22 to E21, TLPRES- generated by the power supply during a power-up sequence is applied to the other input of the AND gate to generate the LOAD- signal in the same manner as did the LREX- signal to cause the trap to $FFFC_{16}$. When TLPRES- is strapped E22 to E27 an immediate LOAD- is generated that is cleared by the first IAQ cycle. Since the microprocessor does not look for the LOAD- signal until the second IAQ cycle, the LOAD- signal is not recognized and the microprocessor takes the trap to 0000_{16} as a result of the RESET- input (see table 3-4).

3.2.7.2 **Programmer Panel Functions.** A number of programmer panel control functions along with a memory clear control function are implemented directly on the 990/4 circuit board as shown on figure 3-19.

Power Light. As power to the microcomputer stabilizes, a high TLPRES- is clocked through a flip-flop by clock CLK3- to provide a low RES signal at the Q- output of the flip-flop. The RES signal is applied through a driver and resistor as the low POWERLED- signal at the programmer panel interface to cause illumination of the POWER LED on the programmer panel.

Idle Light. The low IDLE- signal developed in response to an IDLE instruction from the microprocessor as discussed in paragraph 3.2.7.1 is applied to the programmer panel interface to illuminate the IDLE LED on the programmer panel.

Strobe Decoder. By addressing CRU bits at the programmer panel base address, $1FE0_{16}$, four control signals are generated at the output of an SN74138 that is used as a strobe decoder. The signals are used to exert control over functions on the 990/4 circuit board and on the programmer panel.

An SBO or SBZ instruction addressed to the programmer panel CRU output bit 10 generates a low RUNCLK- signal at the output of the strobe decoder that is ORed with the TLPRES- signal. The low output of the OR gate presets the run flip-flop to provide a high RUNQ signal at the Q output of the flip-flop. RUNQ is inverted and applied to the programmer panel interface as the low RUN- signal to illuminate the RUN LED on the panel and to set the scan counter on the programmer panel to a 10_2 scan count. The high RUNQ is automatically cleared by the RESTART- signal or by addressing programmer panel CRU output bit 14 to generate a low SIECLK- signal at the output of the strobe decoder. Note that addressing CRU output bit 10 at the programmer panel base address also generates a low RUNCLK signal at the output of a strobe decoder in the programmer panel.

An SBO instruction from the microprocessor addressed to CRU output bit 11 of the programmer panel base address generates a low FAULTCLK- signal at the output of the strobe decoder that is applied to a fault indicator flip-flop to clock a low signal through flip-flop. The low FAULT- signal at the output of the flip-flop illuminates a fault lamp on the 990/4 circuit board and is applied through a resistor to the programmer panel interface to illuminate the FAULT LED on the programmer panel. A low TLPRES- signal generated during a power-down or power-up cycle also clears the fault indicator flip-flop to illuminate the fault lamps. A RSET instruction or an SBZ instruction from the microprocessor is required to extinguish the fault lamps.

An SBO or SBZ instruction addressed to programmer panel CRU output bit 12 generates a low MERCLR- signal at the output of the strobe decoder that is applied to the memory interrupt flip-flop to clear the memory error interrupt. A RSET instruction or a low TLPRES- during the power-down or power-up cycle generates a low PRESA- that also clears the memory interrupt.

An SBO or SBZ instruction addressed to programmer panel CRU bit 14 generates a low SIECLK- at the output of the strobe decoder that is applied to the clear pin of the run flip-flop. As RUNQ goes low, the RUN LED on the programmer panel is extinguished and a low LOAD- signal is generated after two instruction acquisition cycles to cause a trap to memory location $FFFC_{16}$.

3.2.8 **PROGRAMMER PANEL INTERFACE.** The programmer panel interface is comprised of TTL devices mounted on the 990/4 circuit board that serve as the interface between the TMS 9900 Microprocessor and the programmer panel. Thirteen signal lines plus 5 volts main power and ground are brought to a 20-pin male connector at the top edge of the 990/4 circuit board at plug P3 where the interface to the programmer panel is completed through a 20-conductor ribbon cable. The interface signals are as shown in figure 3-20. The following description of each of the signals and how they are implemented is keyed to the simplified logic diagram of figure 3-21.

3.2.8.1 **CRU Bit Select Bits.** The CRU bit select bits, CRU bits 12 through 15, are developed from bits of the microprocessor address bus as follows. The Hold Acknowledge (HOLDA) output from the microprocessor is low when the microprocessor is not in the HOLD state and a low ABENBL- signal enables the address bus to external CRU devices and/or the programmer panel. Address bus signals AB0- through AB14- are applied to four quadruple complementary output devices to generate memory address signals MA0 through MA14, MA0-, and MA1-.

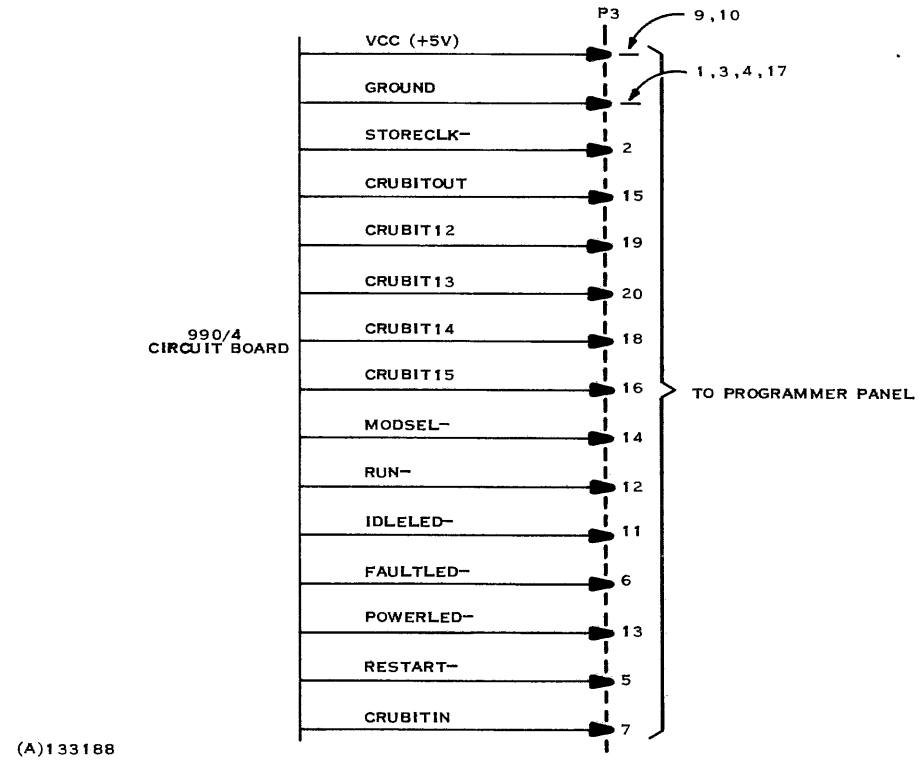


Figure 3-20. Programmer Panel Interface Signals

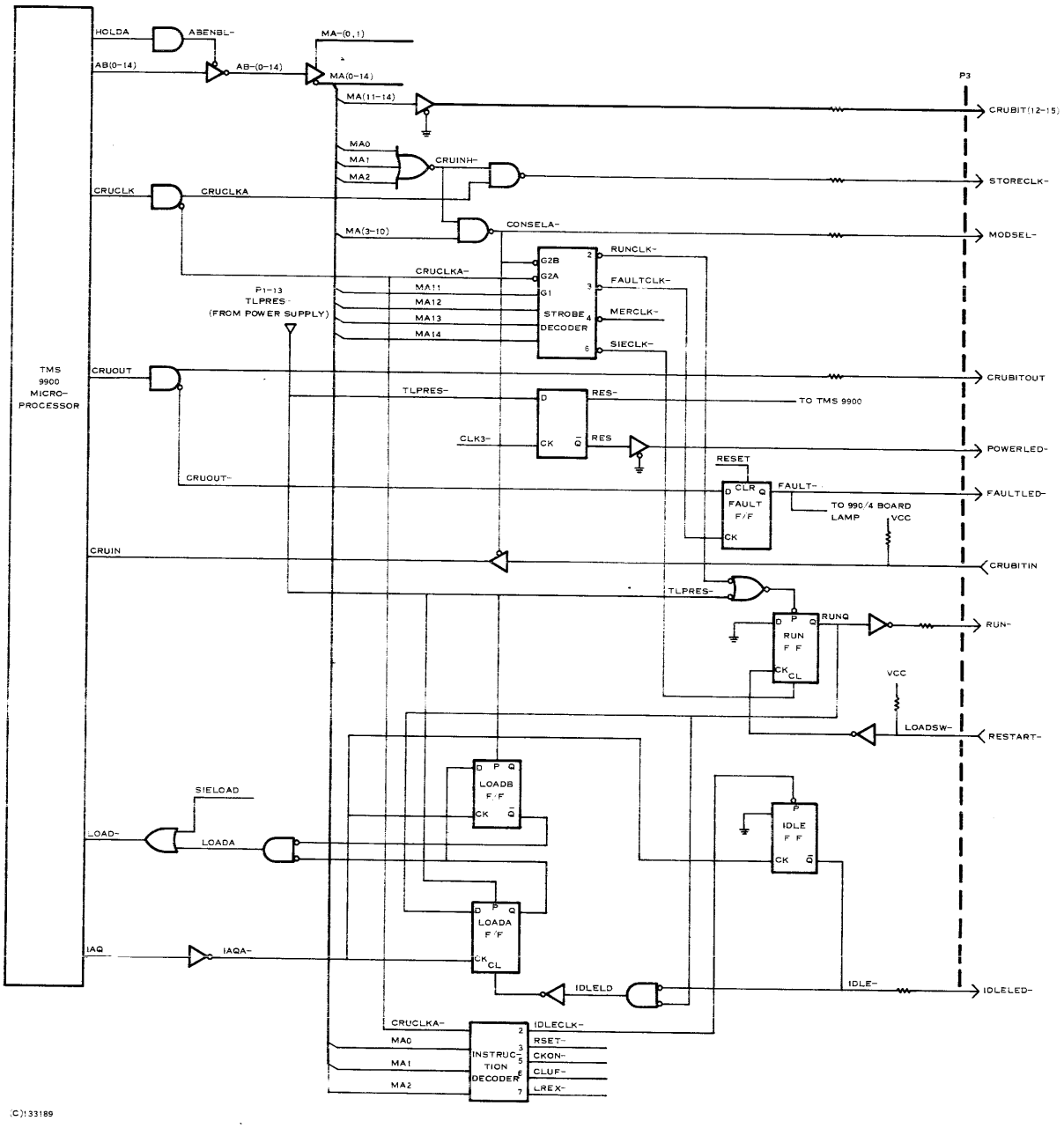


Figure 3-21. Simplified Logic Diagram of Programmer Panel Interface

CRU bits 12 through 15 are the CRU bit select field of the CRU 12-bit address word and as shown in figure 3-21 are developed from memory address bits MA11 through MA14. During a read operation, the bit select field bits applied to the programmer panel select a particular bit for input to the microprocessor whereas during a write operation the bits are used to generate control strobes in the programmer panel.

3.2.8.2 **STORECLK- Signal.** The STORECLK- signal is active when low to generate control strobe enable or write enable logic in the programmer panel. When a CRU device such as the programmer panel is being addressed by the microprocessor, bits MA0 through MA2 applied to a NOR gate are all low so the CRU inhibit signal, CRUINH-, remains high. The high CRUINH- is

applied as one input to a NAND gate. When CRUCLKA, applied to the other input to the NAND gate, is driven high by the high CRUCLK signal from the microprocessor, a low STORECLK- signal is provided at the programmer panel interface.

3.2.8.3 **MODSEL- Signal.** A low MODSEL- signal at the programmer panel interface signifies to the programmer panel that it has been selected by the computer as the addressed module. Memory address bits MA3 through MA10 that are generated by address bits AB3 through AB10 are all high when the programmer panel is the addressed module and are applied as inputs to a NAND gate. Also applied as an input to the NAND gate is the high CRUINH- signal generated as described in paragraph 3.2.8.2. The low CONSELA- signal at the output of the NAND gate is applied through a resistor as the low MODSEL- signal at the programmer panel interface. Note that CONSELA- is also applied as an enabling input to a strobe decoder and a three-state driver in the CRUBITIN serial data line.

3.2.8.4 **Serial Data Lines CRUBITOUT and CRUBITIN.** CRUOUT serial data from the microprocessor is applied through a driver and resistor to the programmer panel interface as the CRUBITOUT signal and is sampled by the programmer panel when the STORECLK- input to the panel goes low. CRUBITIN serial input data is applied as the CRUIN signal to the microprocessor through a three-state driver that is enabled by the low CONSELA- signal when the programmer panel is the addressed module.

3.2.8.5 **POWERLED- Signal.** A normally high TLPRES- supplied by the computer power supply is applied to a flip-flop that is clocked by CLK3-. The low Q- output of the flip-flop, RES, is applied through a buffer to provide a normally low POWERLED- signal at the interface. The low POWERLED- signal illuminates the POWER LED on the programmer panel to indicate that the system power supply is on.

3.2.8.6 **FAULTLED- Signal.** The FAULTLED- signal is a programmable low output signal generated by the microprocessor to illuminate the FAULT LED on the programmer panel to indicate the result of a microprocessor test. A logic ONE on the microprocessor CRUOUT serial data line addressed to the programmer panel CRU output bit 11 lights the panel LED. As shown in figure 3-21, a logic ONE at CRUOUT develops a low CRUOUT- at the input to a flip-flop. This low is clocked out of the flip-flop as a low FAULT- signal by the FAULTCLK- strobe. The FAULTCLK- strobe is generated at the output of a strobe decoder when enabling signals CONSELA- and CRUCLKA- along with memory address bits MA11 through MA14 that have been set to hexadecimal 11 by the microprocessor are all applied to the input of the strobe decoder. The low FAULT- signal that generates the low FAULTLED- signal at the programmer panel interface is also connected to a FAULT lamp on the 990/4 circuit board. Both FAULT lamps are illuminated following a power-up and must be turned off by the user's software. A set-bit-to-zero instruction addressed to programmer panel CRU output bit 11 or a RSET instruction extinguishes both lamps.

3.2.8.7 **RUN- Signal.** The RUN- signal is an active-when-low signal at the programmer panel interface that is generated by the computer while in the RUN mode. The low illuminates the RUN LED on the programmer panel and holds one side of the programmer panel HALT/SIE switch low so that by pressing the switch a low RESTART- signal is applied to the interface. As shown in figure 3-21, either a low TLPRES- or a low RUNCLK- signal sets a flip-flop to provide a high RUNQ signal that is inverted and applied at the programmer panel interface as the RUN- signal. Since TLPRES- is initially low during a power-up the RUN- signal is always generated when power is applied. The low RUNCLK- signal is programmable and is generated with an SBO or SBZ instruction addressed to CRU output bit 10 of the programmer panel. As long as RUNQ is held high, the LOAD- signal to the microprocessor is inhibited.

3.2.8.8 **RESTART- Signal.** RESTART- is a low signal generated at the programmer panel interface by pressing the HALT/SIE switch on the programmer panel when the microcomputer is in the RUN mode. On the 990/4 circuit board, RESTART- is inverted and debounced by an SN7414 Scmitt-trigger inverter and then applied to a flip-flop where it is used to clock the RUNQ output of the flip-flop low. The RUN- signal at the programmer panel interface goes high and the programmer panel moves into its active (HALT) mode of operation. The low RUNQ signal is also applied to one input of a positive NOR gate. If the computer is in the idle state, the low IDLE- signal at the other input to the NOR gate causes its IDLELED output to go high. The high IDLELED signal is inverted and applied to the clear pin of a flip-flop. The low at the Q output of the flip-flop is ANDed with low at the Q- output of a second flip-flop to develop a high LOADA signal. The LOADA signal is applied to a NOR gate that generates the low LOAD- signal that in turn is applied to the microprocessor to cause the trap to memory address $FFFC_{16}$. If the computer is not in the idle state at the time the low RUNQ signal is developed when RESTART- is generated at the programmer panel interface, the LOAD- signal is not generated until the memory cycle in progress is completed as described in the following. The low RUNQ signal is applied to a flip-flop and the low that is clocked through the flip-flop by the next instruction acquisition signal (IAQ) generated by the microprocessor is ANDed with an existing low from the Q- output of a second flip-flop. A high LOADA signal is generated that causes the LOAD- signal to be generated. A second instruction acquisition signal applied to this second flip-flop removes the existing low and the LOAD- signal returns high.

3.2.8.9 **IDLELED- Signal.** A low IDLELED- signal at the programmer panel interface illuminates the IDLE LED on the panel as an indication of microprocessor inactivity. When the microprocessor executes an IDLE instruction it causes MA(0-2) = 010 and CRUCLKA- to go low. These signals at the input to an instruction decoder provide a low IDLECLK- signal out of the decoder. IDLECLK- is applied to the present pin of the IDLE flip-flop causing the IDLE- output of the flip-flop to go low. IDLE- generates the low IDLELED- signal at the interface and is also applied as one input to a NOR gate as described in paragraph 3.2.8.8. The IDLE flip-flop changes state on the first instruction acquisition when program execution resumes due to an interrupt, load, or reset.

3.2.9 **COMMUNICATIONS REGISTER UNIT (CRU) INTERFACE.** The direct command driven input/output interface for the microprocessor is called the CRU. The CRU provides for up to 4096 directly addressable input bits and up to 4096 directly addressable output bits. Input and output operations can address each of the bits individually or in fields of from one to sixteen bits. The microprocessor instructions that drive the CRU can set, reset, or test any bit in the CRU array, or the microprocessor instructions can move data between memory and the CRU data fields.

Logic for the CRU is mounted on the 990/4 circuit board and this logic exerts control over the interface data and control lines. These lines are available to all chassis locations except for that location used by the 990/4 circuit board itself. Twenty-four module select signals are decoded by CRU interface logic and are made available to 12 chassis locations when the 12-inch chassis is used. Only ten of the module select signals are used for the five chassis locations used in the 7-inch chassis. Each chassis location (full-sized slot) accommodates one double-connector circuit board or two single-connector circuit boards.

3.2.9.1 **Main Chassis Implementation.** A minimum CRU implementation can be effected by installing a 990/4 circuit board into a 990 family chassis/power supply assembly. This combination is defined as a main chassis and can be implemented with either a 7-inch chassis that has a maximum of five available full-sized slots or with a 12-inch chassis that has a maximum of 12 available full-sized slots. Each full-sized slot has the capability to implement a maximum of 32

input/output bits. Main chassis CRU addresses begin at 000_{16} and extend to a maximum of $09F_{16}$ for the 7-inch chassis and to a maximum of $17F_{16}$ for the 12-inch chassis. If the main chassis contains a memory circuit board, the number of available full-sized CRU chassis slots is reduced accordingly.

3.2.9.2 **Standard CRU Expansion Implementation.** If a computer system requires more CRU slots than are available in the main chassis, then from one to seven 12-slot CRU expansion chassis can be added. A CRU address map for the standard expansion implementation is shown in figure 3-22. The hardware required for the standard CRU expansion implementation is as shown in figure 3-23. One 26-conductor ribbon cable is required to connect each expansion chassis. The chassis and backpanels used in the expander chassis are identical to those used for the 12-inch main chassis. The expander board installed in the main chassis contains line drivers and receivers for the expansion cables. The buffer board installed in each expansion chassis decodes module select signals, contains buffers and receivers for the CRU address and data, and additionally generates clock signals for the expander chassis cards. The buffer board also implements an interrupt scanner for up to 32 interrupts per expansion chassis. Software can use the interrupt scanner to construct vectored interrupts for each slot of the expander chassis and eliminate the need to poll devices to determine the source of the interrupt.

3.2.9.3 **CRU Applications.** Because of its extremely flexible data format, the CRU interface can be used effectively for a wide range of control and data transactions operations. These applications can be divided into two broad categories: those involving a single control bit transfer, and those requiring input or output of a word of several data or status bits.

Single-Bit Operations. Single-bit operations typically involve the computer sampling a status bit. When the status bit sets, the computer responds by setting a control bit or by transferring to a different set of instructions. This operation is exemplified by a communications interface unit that generates a single interrupt for one of several reasons such as output complete, input complete, or line status change. An output or input complete requires a transfer to instructions that perform another output or input operation. A line status change might require the setting of a control output or the transfer to instructions that handle the change in other ways.

Multiple-Bit Operations. Multiple-bit operations typically involve a data input device such as a keyboard or card reader, or an output device such as a display or card punch. An interrupt from the device causes the microprocessor to perform a store communications register (STCR) instruction to read data from the CRU device and store it into memory. Similarly, to output data to the device the microprocessor executes a load communications register (LDCR) instruction to fetch data from memory and transfer it to the CRU device.

3.2.9.4 **CRU Interface Signals.** Logic on the 990/4 circuit board implements a dedicated CRU interface for the programmer panel as was described in paragraph 3.2.8 and also the standard CRU interface for the main chassis. The interface signals to the main chassis are effected at the bottom edge connectors, P1 and P2, of the 990/4 circuit board. A simplified logic diagram of the CRU interface that shows the interface signals to the main chassis is provided in figure 3-24. Table 3-6 provides the function of each of the CRU interface signals, the pin numbers of the signals on the 990/4 circuit board that installs in main chassis slot designated slot 1, and the pin numbers of the signals as they appear on the backpanel chassis slots of either the main chassis or an expansion chassis. These chassis slots are designated slots 2 through 6 for a 6-slot chassis and 2 through 13 for a 13-slot chassis. Both connectors in each chassis slot are furnished with the CRU bit select bits (CRUBIT 12-15) and other CRU interface signals that permit each connector to address 16 bits of the CRU. Connector P1 in a chassis slot receives one module select signal corresponding to one 16-bit register whereas connector P2 receives two module select signals and thus may address up to 32 bits of the CRU. Connector P1 also receives the eight most significant bits of the CRU address thus permitting the chassis slot to be used for a CRU expansion driver or for modules that ignore module select signals to directly decode their own CRU address.

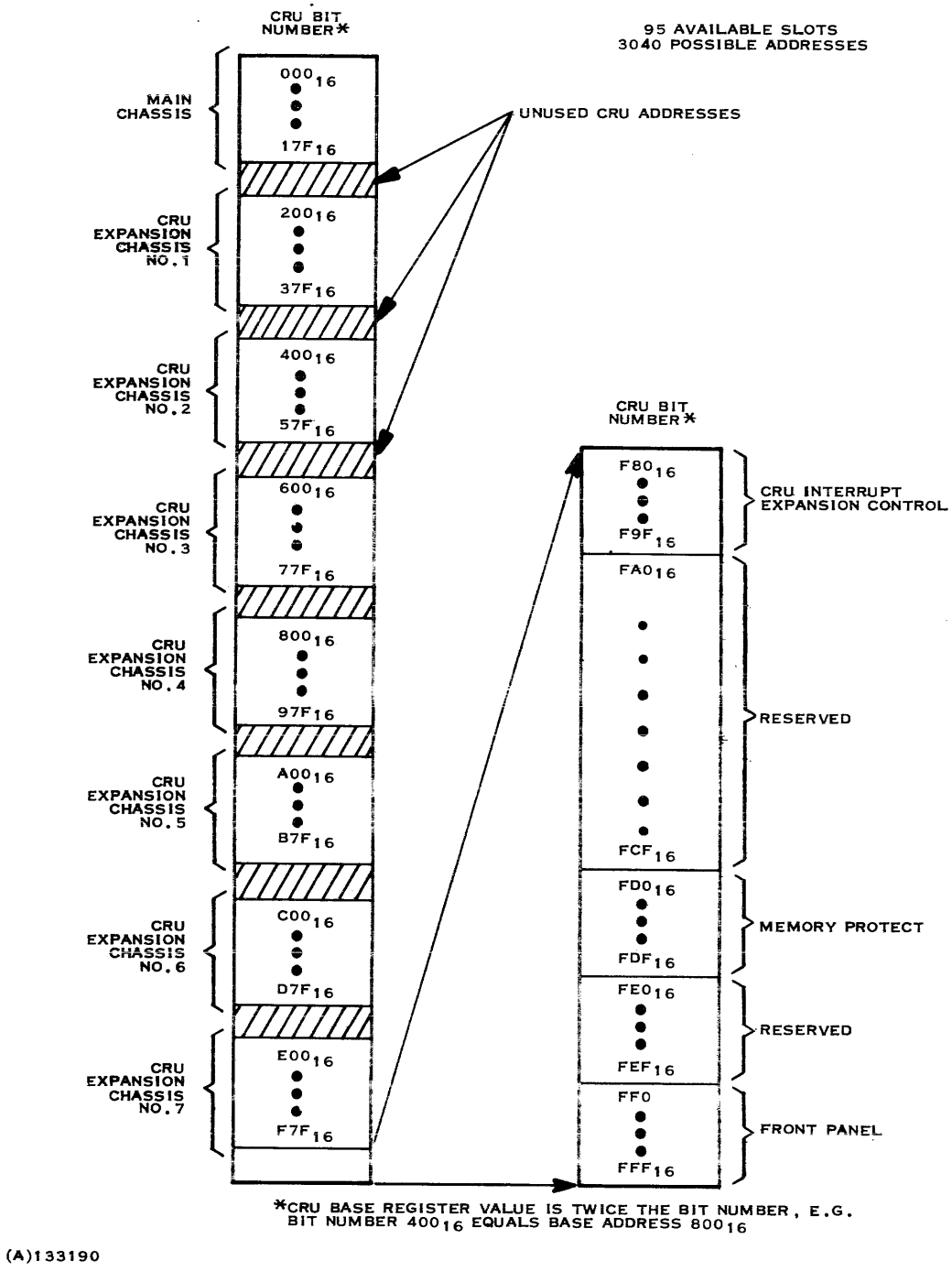


Figure 3-22. CPU Address Map for Standard Expansion Implementation Using 12-Inch Chassis

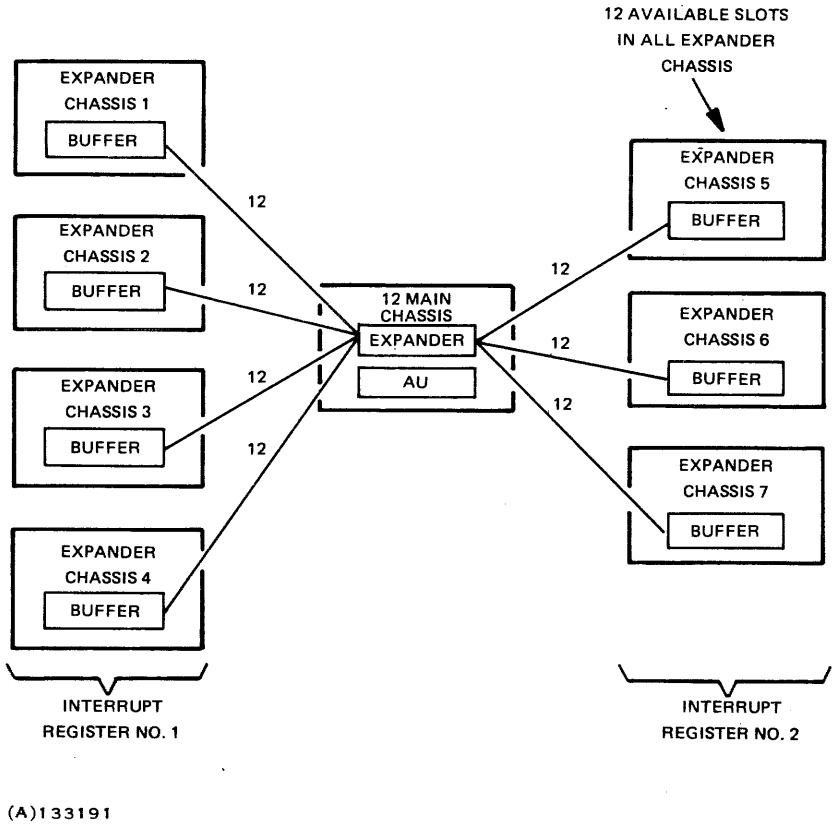


Figure 3-23. Standard CRU Expansion Implementation Hardware

3.2.9.5 CRU Power Supply Requirements. The chassis power supply provides three regulated voltages for use of the CRU, provides power status signals to the CRU, provides signal isolation from the power line or earth ground, and provides ground fault protection for logic signals.

Chassis Power Supply CRU Interface Signals. The chassis power supply interface signals that are implemented in the chassis/power supply assembly are described in table 3-6 along with the pin numbers of the signals at the 990/4 circuit board and also at the chassis backpanel. The description that follows is a description of the signals in greater depth than that provided in the table.

The chassis power supply generates a low Power Fail Warning Pulse (TLPFWP-) to warn of imminent power supply failure. The TLPFWP- pulse connects to the 990/4 circuit board and to all CRU connectors. TLPFWP- has a duration of at least 7.0 milliseconds. Figure 3-25 shows the timing relationship between signals furnished by the power supply and main voltages of the power supply.

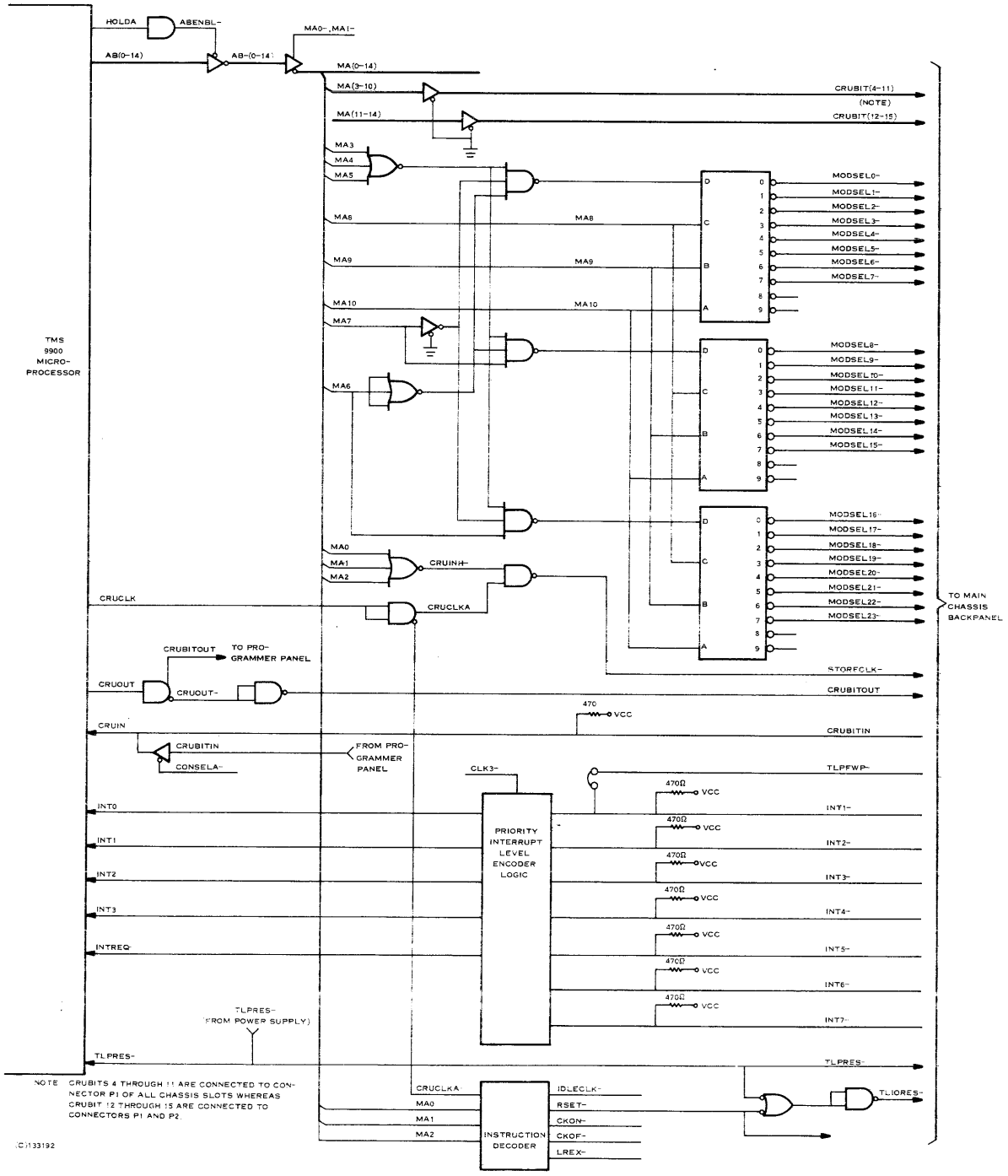


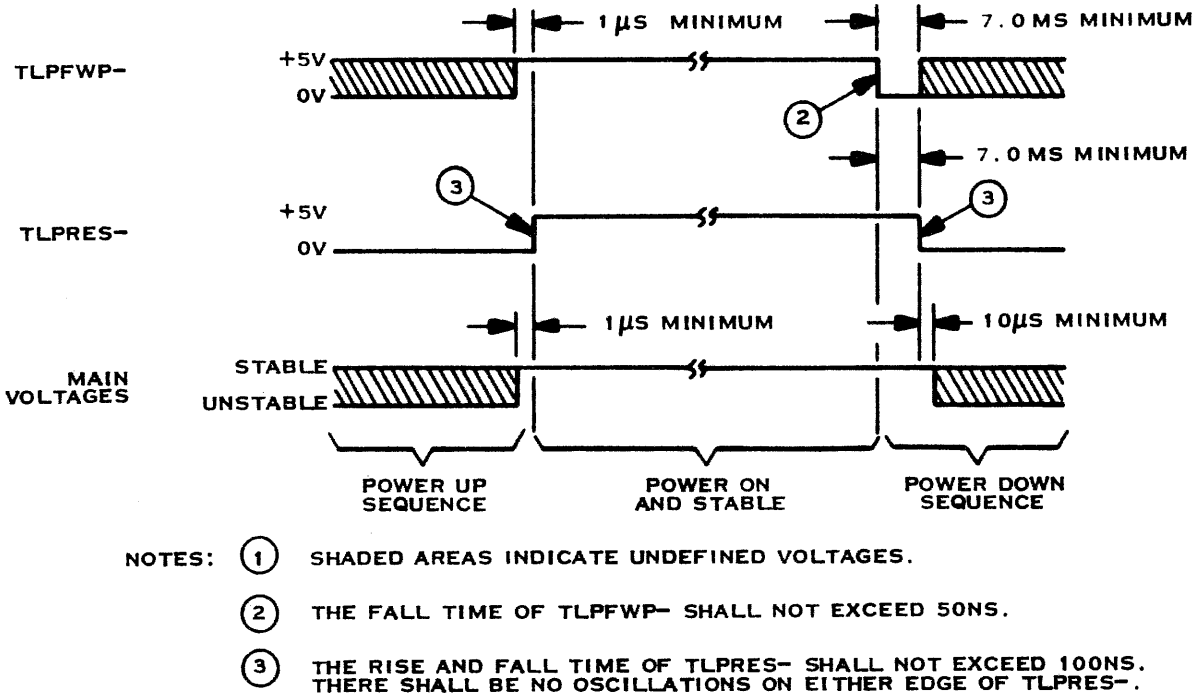
Figure 3-24. Simplified Logic Diagram of 990/4 CRU Interface Implementation

Table 3-6. CRU Interface Signals

Signature	990/4 Circuit Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
MODSEL0-	P1-23	Slot 13, P2-48	Module select signals generated by the microprocessor from address bits 7-11 (CRUBITS 8-11) for use within the main or an expansion chassis. Note that P1 in each slot of the backpanel receives one module select signal whereas P2 receives two module select signals. This configuration permits P2 to use 32 bits of the CRU. Note that pin 48 of successive P2 connectors in the chassis slots are connected to even-numbered module select signals and at the CRU circuit board level carries a MODSELA– signature. Pin 46 of successive P2 connectors in the chassis slots are connected to pin 48 of P1 of that slot and then to an odd-numbered module select signal and carries a signature of MODSELB–. Pin P1-48 is not used when a full-sized CRU circuit board is implemented in a chassis slot. MODSEL signal lines will drive 10 TTL loads.
MODSEL1-	P1-35	Slot 13, P1-48 and P2-46	
MODSEL2-	P1-37	Slot 12, P2-48	
MODSEL3-	P1-43	Slot 12, P1-48 and P2-46	
MODSEL4-	P1-44	Slot 11, P2-48	
MODSEL5-	P1-45	Slot 11, P1-48 and P2-46	
MODSEL6-	P1-46	Slot 10, P2-48	
MODSEL7-	P1-47	Slot 10, P1-48 and P2-46	
MODSEL8-	P1-48	Slot 9, P2-48	
MODSEL9-	P1-49	Slot 9, P1-48 and P2-46	
MODSEL10-	P1-51	Slot 8, P2-48	
MODSEL11-	P1-53	Slot 8, P1-48 and P2-46	
MODSEL12-	P1-61	Slot 7, P2-48	
MODSEL13-	P1-67	Slot 7, P1-48 and P2-46	
MODSEL14-	P1-69	Slot 6, P2-48	
MODSEL15-	P1-76	Slot 6, P1-48 and P2-46	
MODSEL16-	P2-38	Slot 5, P2-48	
MODSEL17-	P2-36	Slot 5, P1-48 and P2-46	
MODSEL18-	P2-34	Slot 4, P2-48	
MODSEL19-	P2-32	Slot 4, P1-48 and P2-46	
MODSEL20-	P2-22	Slot 3, P2-48	
MODSEL21-	P2-18	Slot 3, P1-48 and P2-46	
MODSEL22-	P2-16	Slot 2, P2-48	
MODSEL23-	P2-13	Slot 2, P1-48 and P2-46	
CRUBIT4	P1-56	P1-56	Address bit generated by the microprocessor to select a particular chassis (bits 4-6), a 16-bit module within that chassis (bits 7-11), and a particular bit from that module (bits 12-15). CRUBITS 4-11 are capable of driving at least 12 normalized TTL loads, CRUBITS 12-15 are capable of driving 30 normalized TTL loads.
CRUBIT5	P1-54	P1-54	
CRUBIT6	P1-52	P1-52	
CRUBIT7	P1-50	P1-50	
CRUBIT8	P1-62	P1-62	
CRUBIT9	P1-64	P1-64	
CRUBIT10	P1-68	P1-68	
CRUBIT11	P1-70	P1-70	
CRUBIT12	P1-36	P1-36, P2-36	
CURBIT13	P1-32	P1-32, P2-32	

Table 3-6. CRU Interface Signals (Continued)

Signature	990/4 Circuit Board Pin Number	Main or Expansion Chassis Backpanel Pin Number	Function
CRUBIT14	P1-38	P1-38, P2-38	
CRUBIT15	P1-34	P1-34, P2-34	
CRUBITOUT	P1-18	P1-18, P2-18	Serial data line for transfer of data from the microprocessor to the addressed CRU bit(s). This line is active only when STORECLK– goes low. (This line will drive 30 normalized TTL loads.)
CRUBITIN	P1-60	P1-60, P2-60	Serial data line for transfer of data from the addressed CRU bit(s) to the microprocessor. This line must be driven by an open collector gate and only when the module is selected. A 470-ohm pull-up resistor is mounted on the 990/4 circuit board for this line.
STORECLK-	P1-22	P1-22, P2-22	An active-when-low pulse that indicates to the selected CRU module that the operation is a write (Set Bit or LDCR) operation. This pulse transfers the data on the CRUBITOUT line into a holding flip-flop that is the CRU bit. (Will drive 30 TTL loads.)
TLIORES-	P1-14	P1-14, P2-14	I/O Reset: A normally high signal that, when low, resets all connected devices. This signal is a minimum 250 nanoseconds pulse that is generated by a RSET instruction in the microprocessor. This signal is also low until dc power is up and stable. (Will drive 30 TTL loads.)
TLPFWP-	P1-16	P1-16, P2-16	Power Failure Warning Pulse: A low signal of at least 7.0 milliseconds duration that indicates that a power failure is imminent. (Will drive 30 TTL loads.)
TLPRES-	P1-13	P1-13, P2-13	Power Reset: A normally high signal that goes low to reset connected devices at least 10 microseconds before dc voltages begin to fail during power down.



NOTES:
1. SHADED AREAS INDICATE UNDEFINED VOLTAGES.
2. THE FALL TIME OF TLPFWP- SHALL NOT EXCEED 50NS.
3. THE RISE AND FALL TIME OF TLPRES- SHALL NOT EXCEED 100NS. THERE SHALL BE NO OSCILLATIONS ON EITHER EDGE OF TLPRES-.

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Figure 3-25. Chassis Power Supply Timing

The chassis power supply generates a Power Reset (TLPRES-) to indicate that power supply voltages are unstable. The TLPRES- signal is connected to the 990/4 circuit board and to all the CRU connectors. TLPRES- is low true. The chassis power supply furnishes three separate supply voltages to all connectors on the chassis backpanel; +5 MAIN, +12 MAIN, and -12 MAIN. The +5 MAIN supply is +5±.15 volts referenced to logic ground and has the capacity for 20 amperes if mounted in a 6-slot chassis and 40 amperes if mounted in a 13-slot chassis. Note that to determine the power available to CRU devices the current drain of the 990/4 circuit board must be subtracted from the above currents. The +12 MAIN supply is +12±.36 volts referenced to logic ground and has the capacity for 2 amperes in the 6-slot chassis and for 4 amperes if mounted in the 13-slot chassis. The -12 MAIN supply is -12±.72 volts referenced to logic ground and has the capacity for 1 ampere in the 6-slot chassis and for 2 amperes when mounted in the 13-slot chassis. All power supply voltages and logic levels are referenced to logic ground. Additionally, the backpanel in the chassis contains a logic ground plane on the connector side of the backpanel to minimize crosstalk and noise problems for CRU signals. Logic ground is electrically isolated from chassis or earth ground to minimize ground loop problems when two chassis of slightly different earth ground potentials must interconnect. Fault protection capacitors between earth and logic ground are provided to perform two functions. First, the capacitors bleed off high frequency noise on logic ground that would interfere with the operation of high frequency analog devices such as CRT displays and second, the capacitors provide protection for the user when voltages greater than 30 volts dc or 15 volts ac exist between earth and logic ground as the fault protection capacitors will short to trip the users circuits breaker to prevent a potential shock hazard. Earth ground is supplied from the ground prong on the chassis power cord. Earth ground is connected to all exposed metal parts of the chassis but is not made available to any CRU circuit board.

3.2.9.6 CRU Circuit Board Mechanical Requirements. The chassis/power supply assembly is able to accept CRU (or other) circuit boards with the dimensions specified in figure 3-26 without clearance problems. Maximum power load for each full-sized slot is 50 watts.

3.2.9.7 CRU Addressing. The microprocessor issues a 12-bit address (CRUBIT4 through CRUBIT15) to address up to 4096 individual bits. The 12-bit address is used for both input and output operations. Figure 3-27 illustrates the field assignments for the 12-bit CRU address. The four least significant bits, CRUBIT12 through CRUBIT15, select one of sixteen possible bits from a particular module select. The next five bits, CRUBIT7 through CRUBIT11, have the capability of generating 32 module select signals but only 24 module select signals are implemented on the 990/4 circuit board since this is the maximum number of CRU modules that can be installed in the 13-slot chassis. The three most significant bits identify the chassis containing the addressed module. Chassis 0 is by definition the main chassis. All CRU address bus signals are high true.

3.2.9.8 Microprocessor CRU Output Timing. The microprocessor conforms to minimum CRU output timing restrictions as defined by figure 3-28. The figure shows the timing sequence for a LCDR R1, 2 instruction followed by a SBZ 15 instruction. Minimum timing restrictions are the same for both instructions. CRU addresses and module selects are defined only during the execution of CRU output or CRU input instructions. CRUBITOUT and STORECLK- are held high when the microprocessor is not executing a CRU output instruction. The CRU device clocks the CRUBITOUT line using the positive edge of the STORECLK- pulse. Figure 3-28 describes general design timing requirements for CRU interface cards. The 250-nanosecond timing is found in faster 990 computers. CRU bits are transferred at a 667 nanosecond per bit rate in the 990/4 computer but nevertheless cards should be designed to operate at the faster 250 nanoseconds per bit rate.

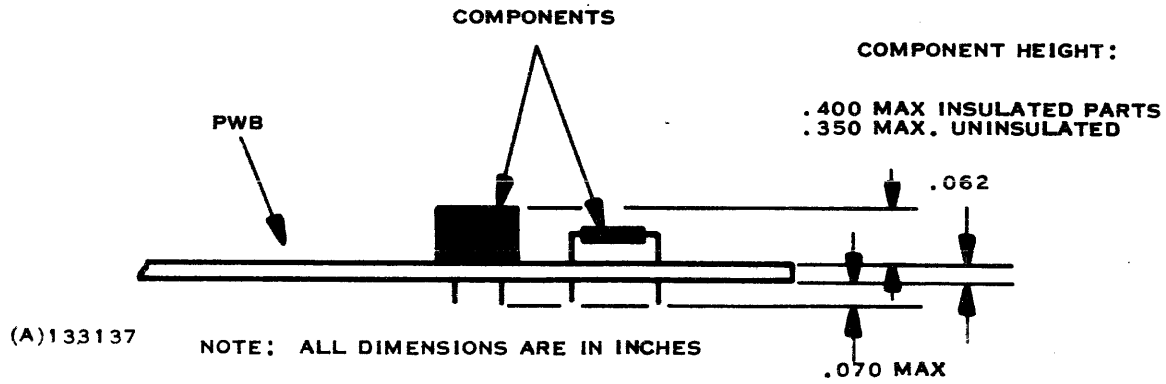

Figure 3-26. CRU Circuit Board Dimensions Required

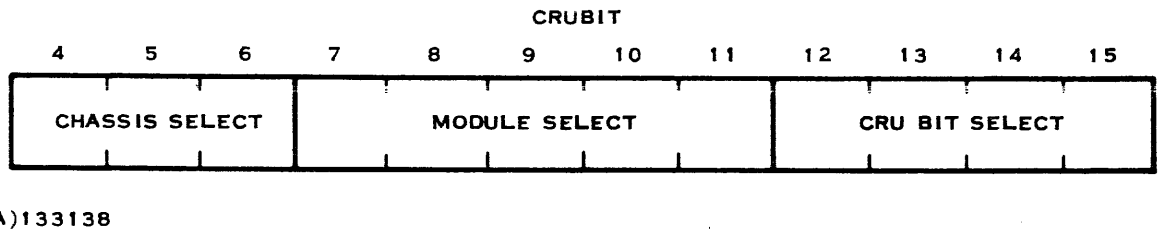

Figure 3-27. CRU Address Field Assignments

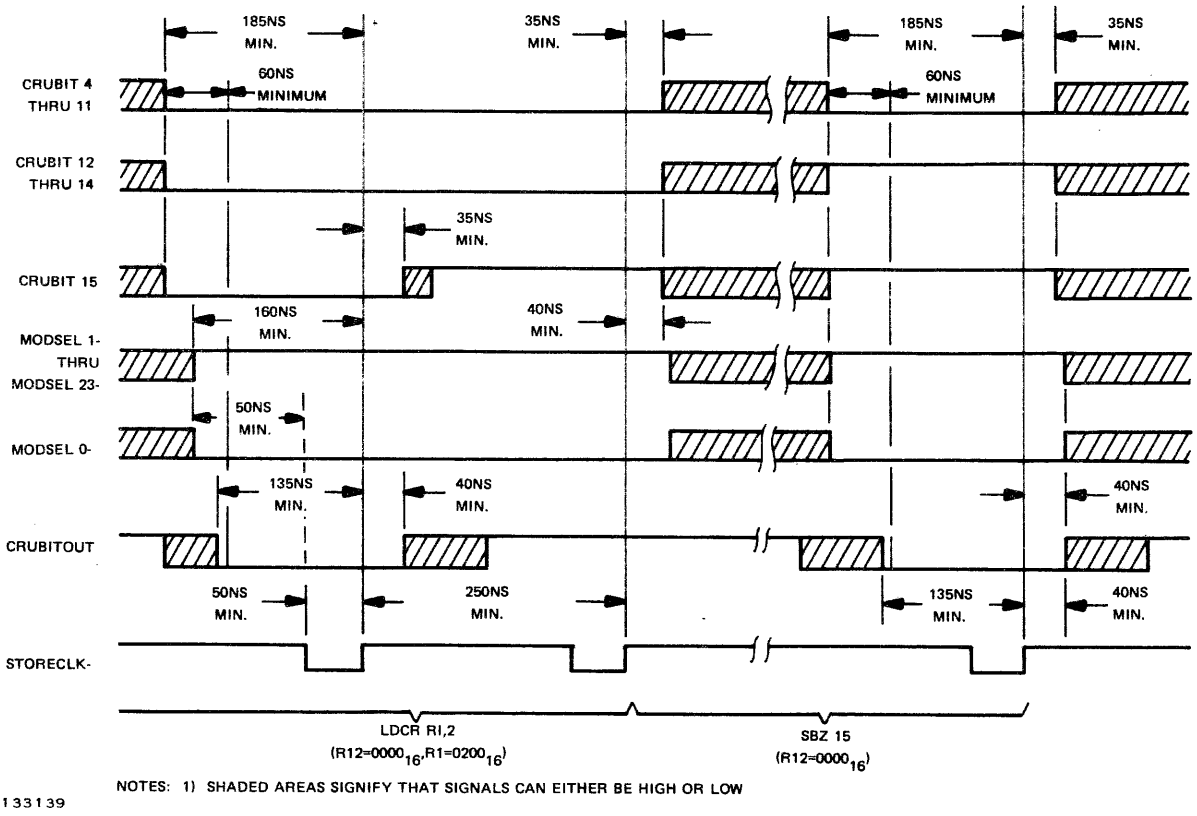

Figure 3-28. CRU Output Timing Minimum Restrictions

3.2.9.9 **Microprocessor CRU Input Timing.** The CRU interface modules are designed to conform to minimum CRU input timing restrictions as defined by figure 3-29 so as to accomodate the faster 990 computers. As it was for output bit transfer, the CRU input data transfer is at the 667 nanoseconds per bit rate in the 990/4 computer. The figures show the timing sequences for STCR R1, 2 instruction followed by an SBZ 15 instruction. Minimum timing restrictions are the same for both instructions. CRU addresses and module selects are defined only during the execution of CRU input or CRU output instructions. CRUBITIN is defined only during the execution of a CRU input instruction. The CRU device decodes the CRU address and places the appropriate data on the CRUBITIN line. The CRU module drives the CRUBITIN line with an open collector or three-state gate that is enabled only when that module is selected. Timing restrictions shown in figure 3-29 are based on a clock period of 250 nanoseconds.

3.2.9.10 **CRU Circuit Board Requirements.** Texas Instruments offers CRU interface modules that plug into CRU slots to act as the interface between the microcomputer and external devices. The 16 I/O EIA Data Module, TI Part Number 945140-0001, provides a general purpose 16-bit input and output interface between the microcomputer and any external device that requires EIA voltage levels at the interface. The 16 I/O TTL Data Module with Interrupt Option, TI Part Number 945145-0001, provides a two-way communication path between the microcomputer and devices which are operated by or generate discrete signals. Sixteen input and sixteen output lines are provided with each line capable of being manipulated as a single independent line or as a member of a group of lines. For the customer that has special requirements and wishes to implement a special CRU circuit board, the following information is provided.

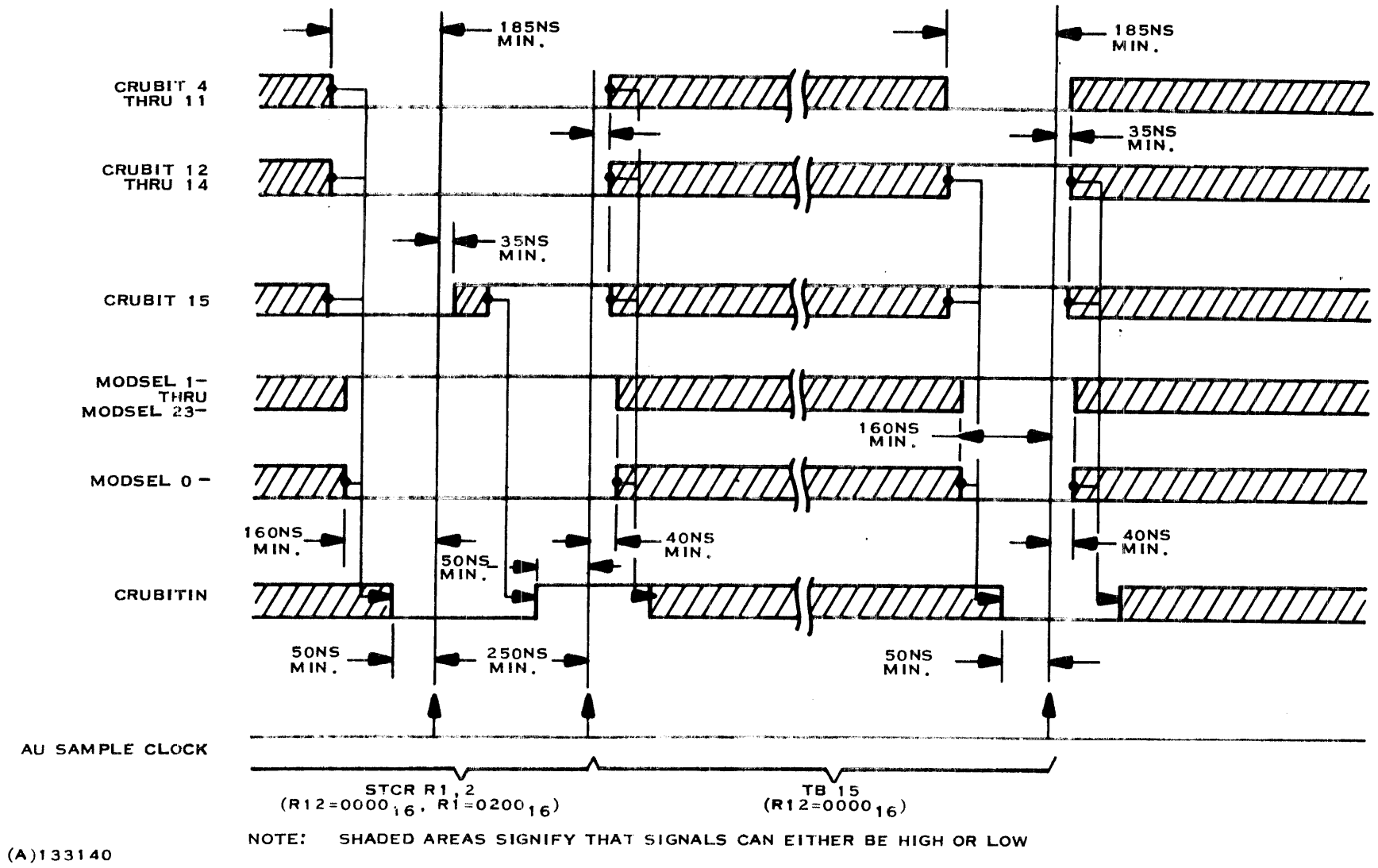

Figure 3-29. CRU Input Timing Minimum Restrictions

CRU circuit boards may be implemented as either full-sized or half-sized circuit boards. Full-sized boards may implement a maximum number of two interrupt vectors and 32 input/output bits along with two module select signals. Half-sized boards may implement one interrupt vector and as many as 32 input/output bits (16 for P1 connectors). A CRU circuit board may be implemented as a standalone peripheral such as an interval timer or may be part of a peripheral kit such as a CRT controller. As part of a peripheral kit, the CRU circuit board interconnects to the CRU peripheral device using a cable.

All CRU signals with the exception of interrupts and module select signals are implemented on the same pins of both connectors P1 and P2 of the chassis backpanel so that the half-sized CRU circuit boards may be installed in either side of a chassis slot. Table 3-7 shows the pin number of these interface signals and figure 3-30 is a logic diagram of a 16 I/O TTL data module that is provided as an example of a CRU interface module. The data module inputs and outputs are negative logic levels that switch zero and some positive voltage level. Each output is an open-collector transistor capable of sinking up to 50 milliamperes at up to 30 volts. Pads are available on the module for installing pull-up resistors or resistor divider networks at each input of the module. Pads for input filter capacitors are also available on the module.

Interrupts. Each side of a chassis slot is provided with a pin through which a CRU circuit board may interrupt the microprocessor. Full-sized board have two interrupts available. Jumper wires on the backpanel are used to assign interrupt priority levels.

Table 3-7. CRU Circuit Board Signals

SIGNATURE	CONNECTOR	PIN NUMBER
INTP2A- (INTA-**)	P2	66
INTP1A- (INTA-**)	P1	66
MODSELA-	P2(wired to an even-numbered MODSEL)	48
	P1(wired to an odd-numbered MODSEL)	48*
MODSELB-	P2(wired to the same MODSEL as P1-48	46
CRUBIT12	P2,P1	36
CRUBIT13	P2,P1	32
CRUBIT14	P2,P1	38
CRUBIT15	P2,P1	34
CRUBITOUT	P1,P2	18
STORECLOCK-	P2,P1	22
CRUBITIN	P2,P1	60
TLIORES-	P2,P1	14
TLPFWP-	P2,P1	16
TLPRES-	P2,P1	13

** Half sized circuit board signature

* This signal should not be used when implementing a full sized CRU circuit board.

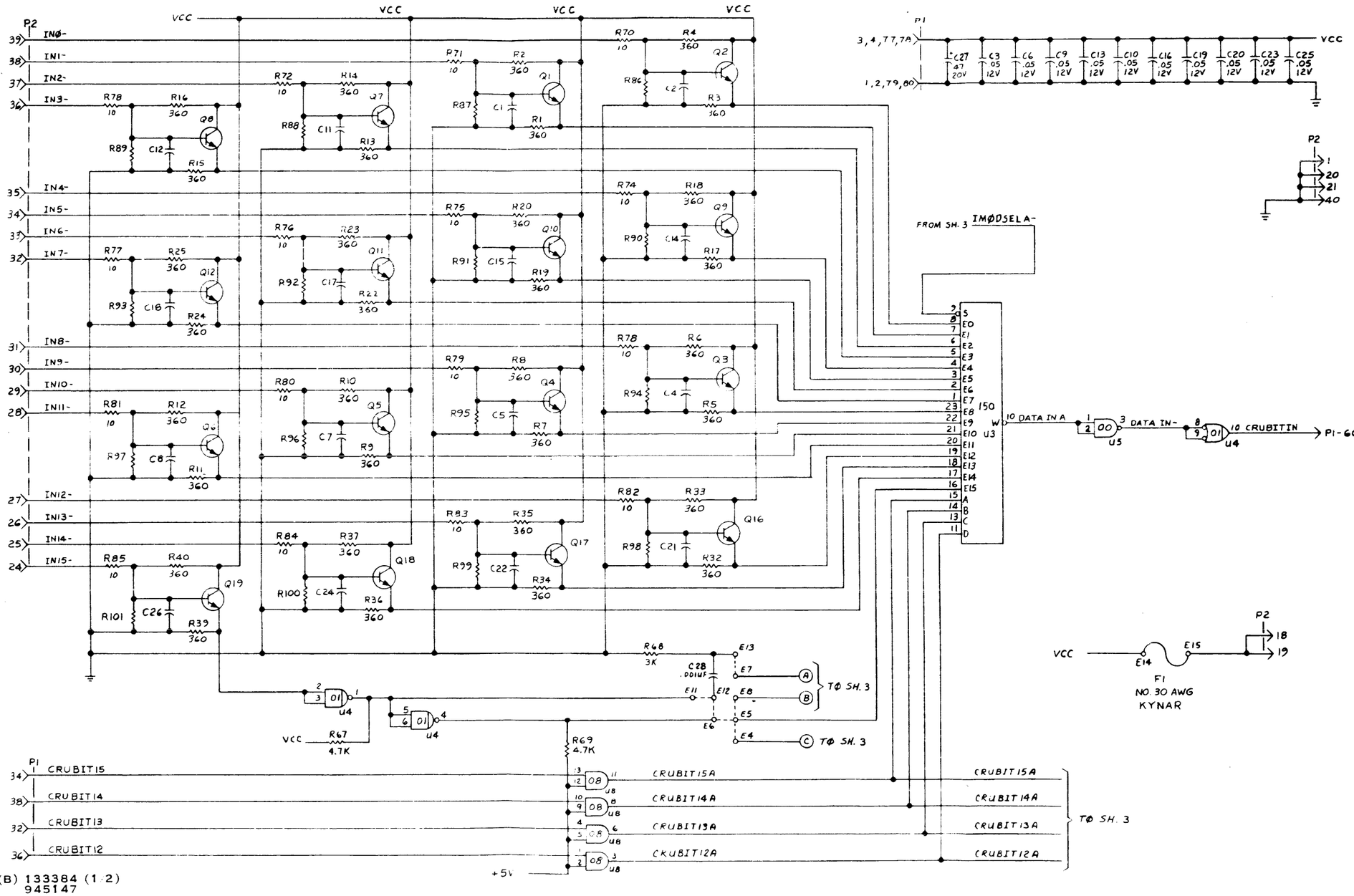

Figure 3-30. Example CRU Module – Logic Diagram of 16 I/O TTL Data Module (Sheet 1 of 2)

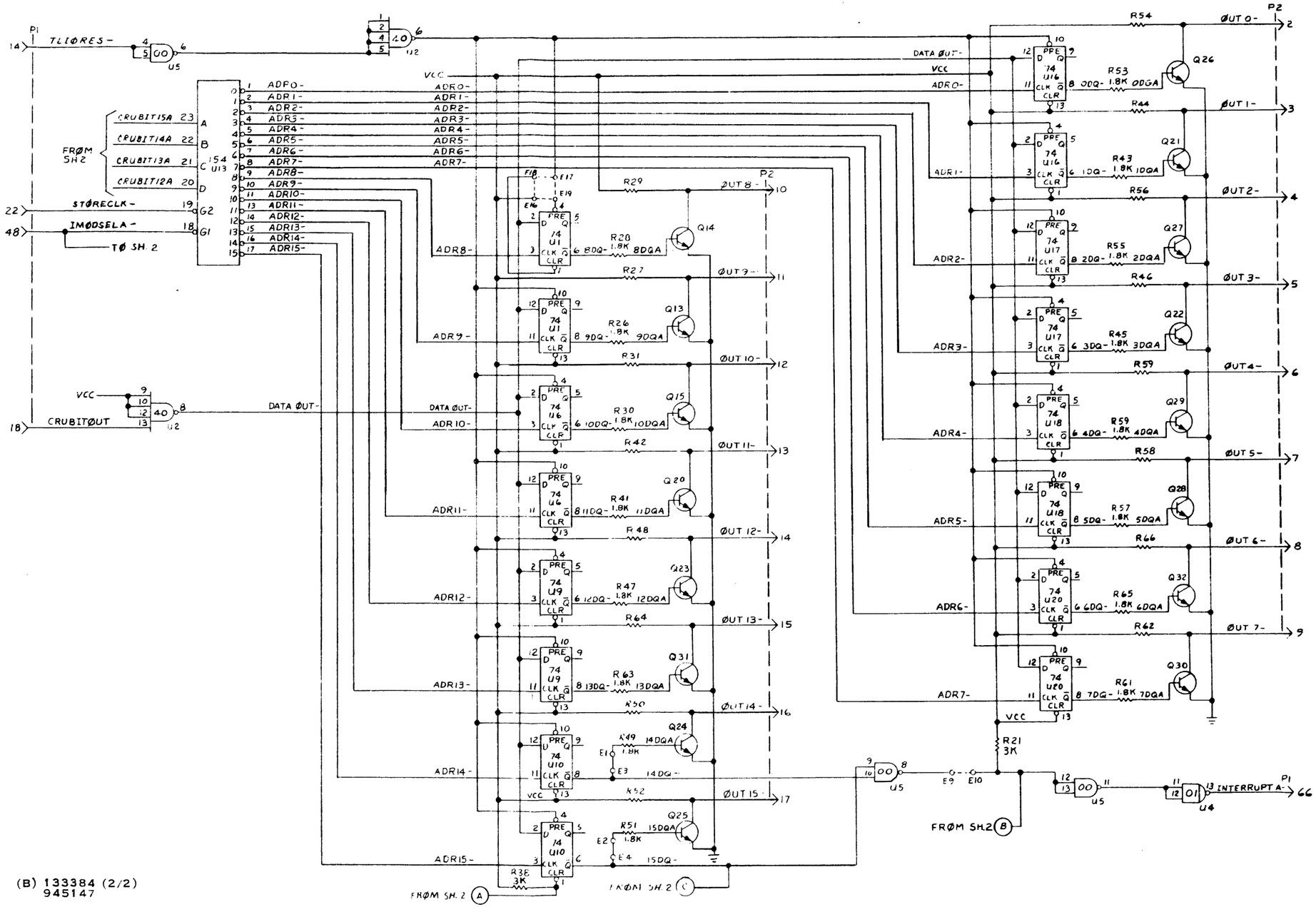

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Figure 3-30. Example CRU Module – Logic Diagram of 16 I/O TTL Data Module (Sheet 2 of 2)

When the CRU circuit board requests an interrupt, the interrupt pin should be driven low with an open-collector TTL gate on the CRU circuit board. This signal should be held low until the microprocessor, using a CRU output operation, clears the interrupt. This signal should be forced clear by TLIORES- and should always be high or floating after a power-up.

Module Select A- (MODSELA-). MODSELA- is the primary or lowest address module select of a full-sized chassis slot and is the only module select available on connector P1. MODSELA-, depending on the CRU circuit board's location in the chassis, is connected to one of the module selects generated by the 990/4 circuit board by way of the chassis backpanel. MODSELA- is low true and CRU circuit board loading should not exceed 5 normalized TTL loads.

Module Select B- (MODSELB-). MODSELB- is the secondary or highest address module select of a full-sized chassis slot. MODSELB- is not implemented on connector P1. MODSELB- on connector P2 is the same signal as MODSELA- on connector P1. This is done so that two half-sized CRU circuit boards can be installed into one full-sized slot. Other characteristics and requirement for the MODSELB- signal are the same as those for the MODSELA- signal.

CRU Address Bits 12 Through 15 (CRUBIT 12-15). The function of CRU bits 12 through 15 is the same as that described in table 3-6. Each signal should be high true and CRU circuit board loading should not exceed one normalized TTL load per connector.

CRUBITOUT. The function of CRUBITOUT is as described in table 3-6. CRUBITOUT should be high true and CRU circuit board loading should not exceed one normalized TTL load per connector.

Store Clock (STORECLK-). The function of STORECLK- is as described in table 3-6. CRU circuit boards should use the positive edge of STORECLK- to clock CRU data into edge-triggered or master-slave flip-flops. STORECLK- may be combined with a CRU address to set or reset a latch. CRU addresses and module selects are valid only during CRU operations and therefore they cannot be used reliably to perform output operations without STORECLK-. CRU circuit board loading on STORECLK- should not exceed one normalized TTL load per connector.

CRUBITIN. The function of CRUBITIN is as described in table 3-6. CRUBITIN is high true and should be driven by either an open collector or three-state gate on the CRU circuit board. CRUBITIN should be allowed to go low only when the CRU circuit board has been addressed by a module select signal.

I/O Reset (TLIORES-). The function of TLIORES- is as described in table 3-6. TLIORES- shall be used by the CRU circuit board to clear and mask all interrupts and shall also be used to reset any state controllers to the start or power-up state. TLIORES- should be low true and CRU circuit board loading should not exceed one normalized TTL load per CRU connector.

Power Fail Warning Pulse (TLPFWP-). The function of TLPFWP- is as described in paragraph 3.2.9.5. TLPFWP- should be low true and CRU circuit board loading should not exceed one normalized TTL load per CRU connector.

Power Reset (TLPRES-). The function of TLPRES- is as described in paragraph 3.2.9.5. TLPRES- should be used without buffering to inhibit critical control and data lines to peripheral devices so that erratic operation of the peripheral does not occur when the chassis power is cycled. TLPRES- is a low true signal and CRU circuit board loading should not exceed ten loads per connector. Total loading for the 6-slot chassis is 50 TTL loads maximum and for the 13-slot chassis is 100 TTL loads maximum.

CRU Circuit Board Output Timing. All CRU circuit boards shall operate in conformance with output timing specified in figure 3-28. Additionally, the CRU circuit board should not delay STORECLK- more than two gate delays or 30 nanoseconds with respect to CRU data out. High speed logic should be used when gating STORECLK- to ensure minimum delay.

CRU Circuit Board Input Timing. All CRU circuit boards should operate in conformance with input timing specified in figure 3-29. Additionally, CRUBITIN should be stable within 90 nanoseconds after address or module select signals become stable.

CRU Circuit Board Power-up, Power-down Sequence. All CRU circuit boards should use the signal described in the timing diagram of figure 3-25 to inhibit any glitches on control or data lines from the CRU circuit board to the CRU peripheral device so that the CRU peripheral device does not receive any false data or control commands during a power-up or power-down sequence. Also the signals should be used to reset all control and data storage elements to the desired state during the power-up sequence. This includes resetting the interrupt and the interrupt mask.

Loopback Test Feature. All CRU circuit boards that operate with CRU peripheral devices should contain a loopback function on the CRU device interface connector for all data and control lines so that when the device cable is removed and a test enable bit is set the CRU circuit board can be exercised to determine whether it is defective or not.

Production Testing. All CRU circuit boards should be checked in a main chassis of a 990 computer or equivalent to ensure that it conforms to high speed CRU operation.

CRU Circuit Board Peripheral Device Interface. CRU peripheral device interface connections to CRU circuit boards should be made with low cost ribbon cable whenever possible. The interface connector that connects to an RS232 CRU peripheral device, such as a modem, auto dialer, teleprinter, or 912 CRT, should be a right-angle subminiature 25-pin connector (AMP HDP-20 or equivalent).

All TTL drivers on the CRU peripheral device interface should be discrete TTL gates or transistors. The output of these drivers should not be loaded by any devices on the CRU circuit board. All TTL receivers on CRU circuit boards should place no more than one normalized TTL load on the CRU peripheral device interface.

In order to prevent ground loops, no signal on the CRU peripheral device interface should be connected directly to earth ground by the peripheral device. All CRU peripheral devices shall be tested to make sure that the resistance between chassis ground and logic ground does not exceed 5000 ohms.

CRU Circuit Board Software Requirements. All CRU circuit boards should implement interrupts as shown in figure 3-31. Interrupts are enabled only after the user program sets the interrupt mask flip-flop. When the CRU circuit board requests an interrupt it sets the interrupt request flip-flop and an interrupt is generated by the open-collector gate. Once the interrupt request is set it must remain set until it is cleared by either an interrupt acknowledge or an I/O reset. The interrupt ID CRU input bit is implemented so the user program can poll CRU circuit boards connected to the same interrupt to determine which board caused the interrupt. Once the user program has finished servicing the interrupt it clears the interrupt request flip-flop by addressing the interrupt acknowledge CRU output strobe. The interrupt request flip-flop and the interrupt mask flip-flop should be reset after a power-up or whenever a RSET instruction is executed.

Corresponding input and output bits that are used by the LDCR and the STCR instructions shall have the same CRU addresses so that driving software does not have to change the CRU base address between input and output operations.

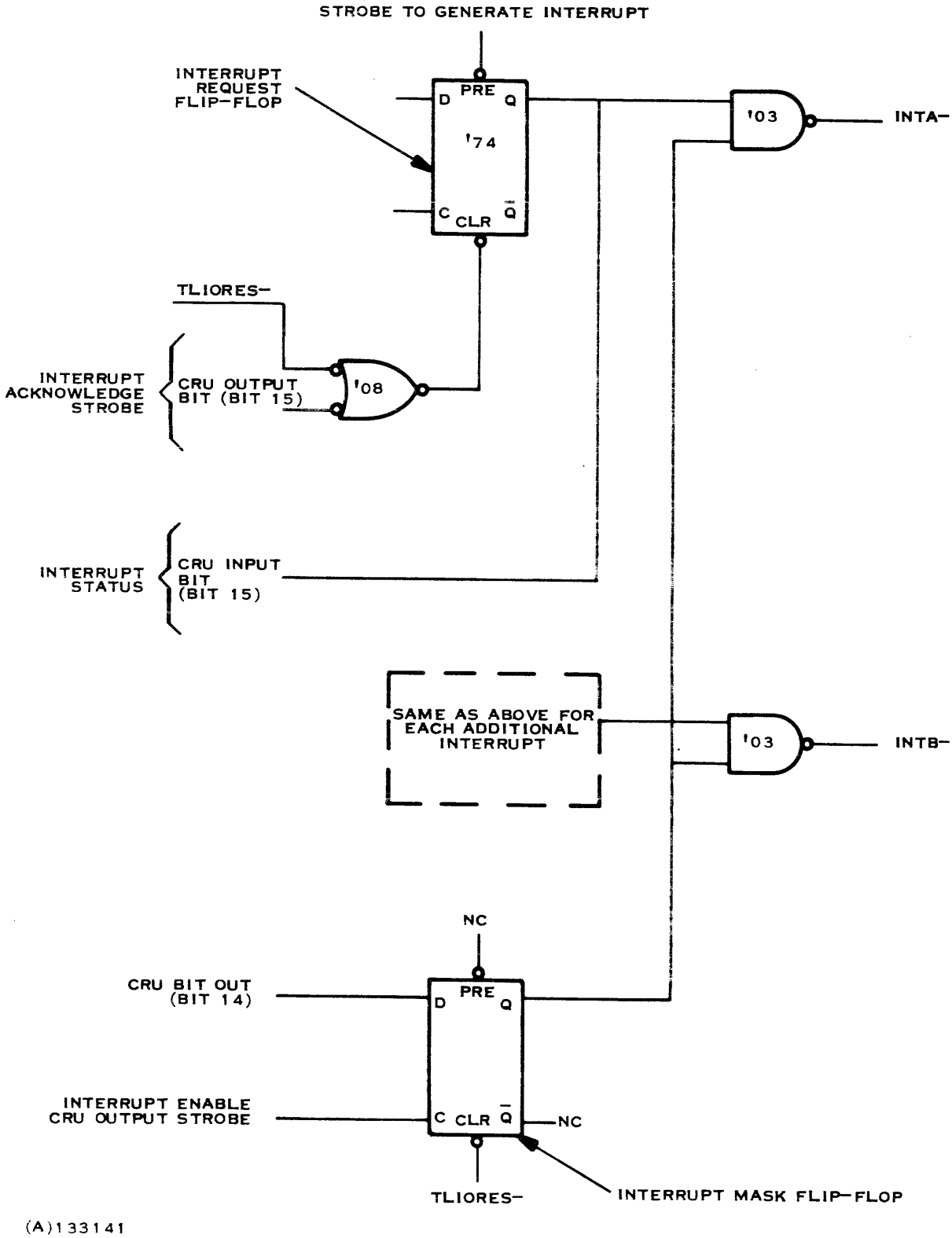


Figure 3-31. CRU Interrupt Implementation

Dedicated CRU Circuit Boards. Dedicated CRU circuit boards are full-sized circuit boards that decode the full 12-bit CRU address instead of using module selects. Dedicated CRU circuit boards should have dedicated CRU addresses at the high end of the CRU address space. Dedicated CRU boards will operate in any main chassis or I/O expansion chassis without software modifications. Dedicated CRU circuit boards should be implemented when more than 32 bits are required on a full-sized CRU circuit board. Dedicated CRU circuit boards have the same requirements as regular CRU circuit boards except that loading on CRU bits 3 through 11 should not exceed one normalized TTL load.

3.2.9.11 990/4 Circuit Board CRU Interface Implementation. The CRU interface as implemented on the 990/4 circuit board is comprised of TTL devices that serve as the interface between the TMS 9900 Microprocessor and external CRU devices. The CRU interface signals are brought to two 80-pin male connectors, P1 and P2, at the bottom edge of the 990/4 circuit board. When the circuit board is installed in full-sized chassis slot 1 of the main chassis, the interface signals are connected to each of the chassis slots through backpanel wiring. The following description of the interface signals and how they are implemented is keyed to the simplified logic diagram of figure 3-24.

CRU Bits 4 through 15. CRU bits 4 through 15 are developed from bits of the microprocessor address bus as follows. The Hold Acknowledge (HOLDA) output from the microprocessor is low when the microprocessor is not in the HOLD state and a low ABENBL- signal enables the address bus. Address bus signals AB0- through AB14- are applied to four quadruple complementary output devices to generate memory address signals MA0 through MA14. The 12-bit CRU address field consisting of CRU bits 4 through 15 is developed from memory address bits MA3 through MA14. The CRU bits are applied through drivers to connector P1 with pin numbers as shown in table 3-6.

Module Select Signals. Memory address bits MA3 through MA10 are applied to three SN7442A BCD-to-decimal decoders (used as 3-to-8 binary decoders) to develop module select signals MODSEL0- through MODSEL23-. Memory address bits MA3 through MA5, that correspond to chassis select address field bits CRUBIT4 through CRUBIT6, are applied as enabling bits to a NOR gate and when all are low the main chassis module select signals are enabled. Memory address bits MA6 through MA10, that correspond to module select address field bits CRUBIT7 through CRUBIT11, are decoded to develop the module select signals for the addressed module. The module select signals are applied to connectors P1 and P2 with pin numbers as shown in table 3-6

Store Clock (STORECLK-). The microprocessor sets CRUCLK high to indicate to external interface logic to sample the output data on CRUOUT or to decode external instructions at address bits AB0 through AB2. For a CRU output operation, AB0 through AB2 are low and memory address bits MA0 through MA2 applied to a positive NOR gate are low. The high CRUINH- signal at the output of the NOR gate is ANDed with CRUCLKA (derived from CRUCLK) to generate the low STORECLK- signal that is applied to pin 22 of connector P1.

Serial Data Lines. The serial CRU data out line from the microprocessor, CRUOUT, is applied to a complementary output element. The CRUOUT- output of the element is applied to a positive NAND buffer to develop the CRUBITOUT signal at pin 18 of connector P1. Serial data in to the microprocessor is brought in from external CRU devices to the 990/4 circuit board at pin 60 of connector P1 as CRUBITIN. The signal is developed across a 470-ohm pullup resistor and applied to the microprocessor as CRUIN.

Interrupts. Seven external interrupt levels are brought to the 990/4 circuit board from the external CRU devices at connectors P1 and P2 with pin numbers as shown in table 3-6. Paragraph 3.2.6 contains detailed information on interrupt logic implementation.

Power Failure Warning Pulse (TLPFWP-). The TLPFWP- signal is brought into the 990/4 circuit board at pin 16 of connector P1 to generate the power fail interrupt signal. TLPFWP- is applied through a removable jumper wire from terminals E12 to E11 to the input of the priority interrupt level encoder as a level 1 interrupt.

Power Reset (TLPRES-). The normally high TLPRES- signal generated by the power supply goes low at least 10 microseconds before dc voltages begin to fail during power-down and is used to reset connected devices. TLPRES- is brought to the 990/4 circuit board at pin 13 of connector P1.

I/O Reset (TLIORES-). TLIORES- is a normally high signal that, when low, resets all connected devices. TLIORES- is generated by a RSET instruction in the microprocessor and goes low for a minimum duration of 250 nanoseconds. TLIORES- is held low by TLPRES- until dc power is up and stable. TLIORES- is applied to external devices at pin 14 of connector P1.

3.2.10 990/4 BOARD ASSEMBLY CONFIGURATIONS. There are two standard configurations of the 990/4 circuit board assembly. One configuration has 256 words of static RAM and an additional 12 sockets into which may be installed either PROM or static RAM device kits to provide up to 1024 total words of on-board PROM or static RAM or a combination of the two in 256-word increments (4 devices per 256-word increment). A second configuration has 16 sockets for installation of 1024 words of PROM and/or static RAM and has 4096 words of on-board MOS dynamic RAM and three additional sockets for installation of the parity option.

Applications. The PROM/RAM configuration of the 990/4 circuit board assembly primarily has its application as a hard-wired machine controller. The installed 256 words of static RAM is addressable at starting address 768. User supplied ROM at starting address 0 is required for this configuration and can be supplemented with additional ROM and/or static RAM at starting addresses 256 and 512 as desired. This configuration provides for a power-up interrupt at level 0, a power-fail interrupt at level 1, and a real-time clock interrupt at level 5. This configuration does not support maintenance or the programmer panel.

The second configuration of the 990/4 circuit board assembly with its installed 4096 words of dynamic RAM functions primarily as a general purpose microcomputer. With customer-supplied down-loader ROM and video display terminals with keyboards the microcomputer operates as an intelligent terminal system. Starting address of the dynamic RAM is zero. This configuration is supported by T.I. with either 256 words of on-board ROM supplying a 733 ASR Loader and Card Reader Loader or 256 words of ROM supplying a Floppy Disc Loader. Both loaders feature a front panel utility program and both loaders optionally may be augmented with a self-test program by implementation of an additional 256 words of on-board ROM. The starting address for ROM is at 31K. Both loaders use dynamic RAM memory address 80_{16} through $9F_{16}$ for dedicated workspace.

This configuration provides for a power-up interrupt at level 0, a power-fail interrupt at level 1, a memory error interrupt at level 2, and a real-time clock interrupt at level 5. This board does support the maintenance panel and the programmer panel if T.I. supplied loaders are used.

Standard Option Jumper Schedules. Jumper wire strapping between terminals on the two standard 990/4 circuit board configurations select the power-trap location, memory starting addresses, PROM or static RAM operation, and internal interrupt levels as shown in figure 2-21 and summarized in table 2-2.

System Operation. For the PROM/RAM 990/4 configuration, operation is initiated by applying power to the board. When power is first applied, a reset signal generated by the power supply causes the microprocessor to trap to location 0000 in the user-supplied ROM program and processing of the user program follows.

Operation for the dynamic RAM configuration of the 990/4 Microcomputer equipped with a programmer panel, a 733 ASR data terminal, and various peripherals and display terminals is as follows. This discussion assumes that the 990/4 circuit board has the 733 ASR/Card Reader Loader with Self-Test ROM and panel software ROM installed on the board and that jumper options have been made that sets the following conditions.

Starting dynamic RAM address on 990/4 circuit board set to 0000.

Starting PROM/RAM address set to $F800_{16}$ (31K words).

Power-up trap vector is 0000.

RESTART signal traps to $FFFC_{16}$.

When the key switch on the programmer panel is moved from the OFF to the LOCK position, AC power is applied to the main chassis and the power supply generates the reset signal causing the microprocessor to trap to location 0000 and begin processing.

When the key switch on the programmer panel is set to the UNLOCK position, the HALT/SIE switch on the panel is enabled. When the HALT/SIE switch is pressed, the programmer panel generates a RESTART signal to the 990/4 circuit board that in turn develops the LOAD- signal that is applied to the microprocessor. This signal causes the microprocessor to trap through location $FFFC_{16}$ in ROM after saving the workspace pointer, current PC, and ST register values from the main program. Location $FFFC_{16}$ contains the workspace pointer value of 80_{16} that is the starting memory address for the programmer panel software workspace. The microprocessor transfers this value to its workspace register and fetches the program counter value that is the starting memory address for the programmer panel software from the next consecutive memory address, $FFFE_{16}$. This action transfers control to the front panel utility program that runs to interpret the programmer panel buttons. As the panel software begins executing, the controls and indicators on the programmer panel become active and the RUN light on the programmer panel is extinguished. At this point, a program load may be initiated at the programmer panel by pressing the LOAD button on the panel. Pressing of the LOAD button is interpreted as a "branch to the loader" routine. The branch to the loader may be made to a 733 ASR Loader at CRU base address 00 with interrupt level 6, the Card Reader Loader at CRU base address 040_{16} with interrupt level 4, or to the Floppy Disc Loader at CRU base $080/0A0_{16}$ with interrupt level 7 as applicable. Before initiating the load operation, the loader program checks to see if a self-test ROM program is present. If present, the branch is made to the program and a diagnostic test of the microprocessor and of the dynamic RAM are made. If the program fails to run to completion without errors, the FAULT LED on the programmer panel and the 990/4 circuit board light and the load operation is inhibited. If the self-test program runs to completion, the program branches to the appropriate loader and the user's program is loaded into memory under

software control. If the self-test program is not present a branch is made back to the loader. Upon completion of the load operation, the microprocessor is ready to begin program execution. Program execution is usually initiated by a transfer vector in the object code of the loaded program.

To prevent program intervention from the programmer panel, the key switch is generally set to the LOCK position and the key removed after loading. In this position, the switches on the panel are locked out, (the programmer panel is inactive) and manual intervention cannot occur until the key is reinserted and the switch rotated to the UNLOCK position.

3.3 990/4 MEMORY EXPANSION MODULE

The 990/4 memory expansion module is a full-sized, double-sided, 160-pin printed circuit board that installs in a chassis slot of the computer where the interface to the power, data, and control signals is effected at the chassis backplane. When fully implemented, the memory expansion module has 20K words of dynamic random access memory (RAM) capacity in 4096-word increments. Module memory capacity is set at time of manufacture and is not alterable in the field. Each 4096-word increment uses 16 Texas Instruments TMS 4050 integrated circuit devices. The TMS 4050 is a high-speed dynamic 4096-bit MOS circuit organized as 4096 one-bit words. As an option, odd parity may be implemented by installing a seventeenth TMS 4050 for each 4K words of memory storage and two each of the SN74180 parity generators/checkers in the sockets provided. Twelve address input lines allow selection of any of the 4096 bits in the TMS 4050 storage matrix for either a read or write operation. A refresh of the cell matrix is accomplished by performing a memory read cycle at each of the 64 row addresses every two milliseconds to preserve data that is stored in the dynamic MOS memory storage cells. Data selectors select the refresh address lines to replace the six processor address bits, ADRIN03 through ADRIN08, to refresh 1/64th of the memory during a refresh cycle.

The expansion memory module is addressed in a block of consecutive addresses with the starting address adjustable to any 4K word boundary in the address space. The start address is set by switches on the board with the upper limit address set by wire jumpers. For example, a 4K module responds to 4K addresses only whereas an 8K module responds to 8K addresses and so forth. The expansion memory is on the 9900 Memory Bus and may be accessed for read and write operations by the TMS 9900 Microprocessor or by an external device.

A memory protect option, when implemented, provides the capability to define a write protected zone in memory. The boundaries of the protected zone are programmable in 256-word increments. The protected zone is defined by two 7-bit registers, the upper bound and lower bound, that are addressed by the CRU. A 16-bit LDCR instruction must be used to load the registers because they are implemented as a serially loaded shift register. A dedicated CRU base address of $1FA0_{16}$ is used when addressing the write protect register of the memory expansion board. If more than one board is used in a system, the loading of the protect registers via the CRU occurs in parallel. It is not possible to load each board with unique protect bounds.

3.3.1 MEMORY CONTROLLER. The memory controller for the 990/4 memory expansion module monitors the 9900 Memory Bus to decode addresses on the bus and, when the memory expansion module is addressed, directs the dynamic RAM to perform read and write operations under the control of the 9900 Microprocessor or under the control of an external device that is also on the 9900 Memory Bus. The memory controller also initiates refresh cycles to the memory. The following description is keyed to figure 3-32.

3.3.1.1 Address Examination. An active low MEMEN- signal from the 9900 Memory Bus signifies that the address bus is addressing the memory system, either local memory on the 990/4 circuit board or memory external to the circuit board. The low MEMEN- signal is inverted to generate a high MEMEN signal that is applied as an input to both an AND gate and a NAND gate.

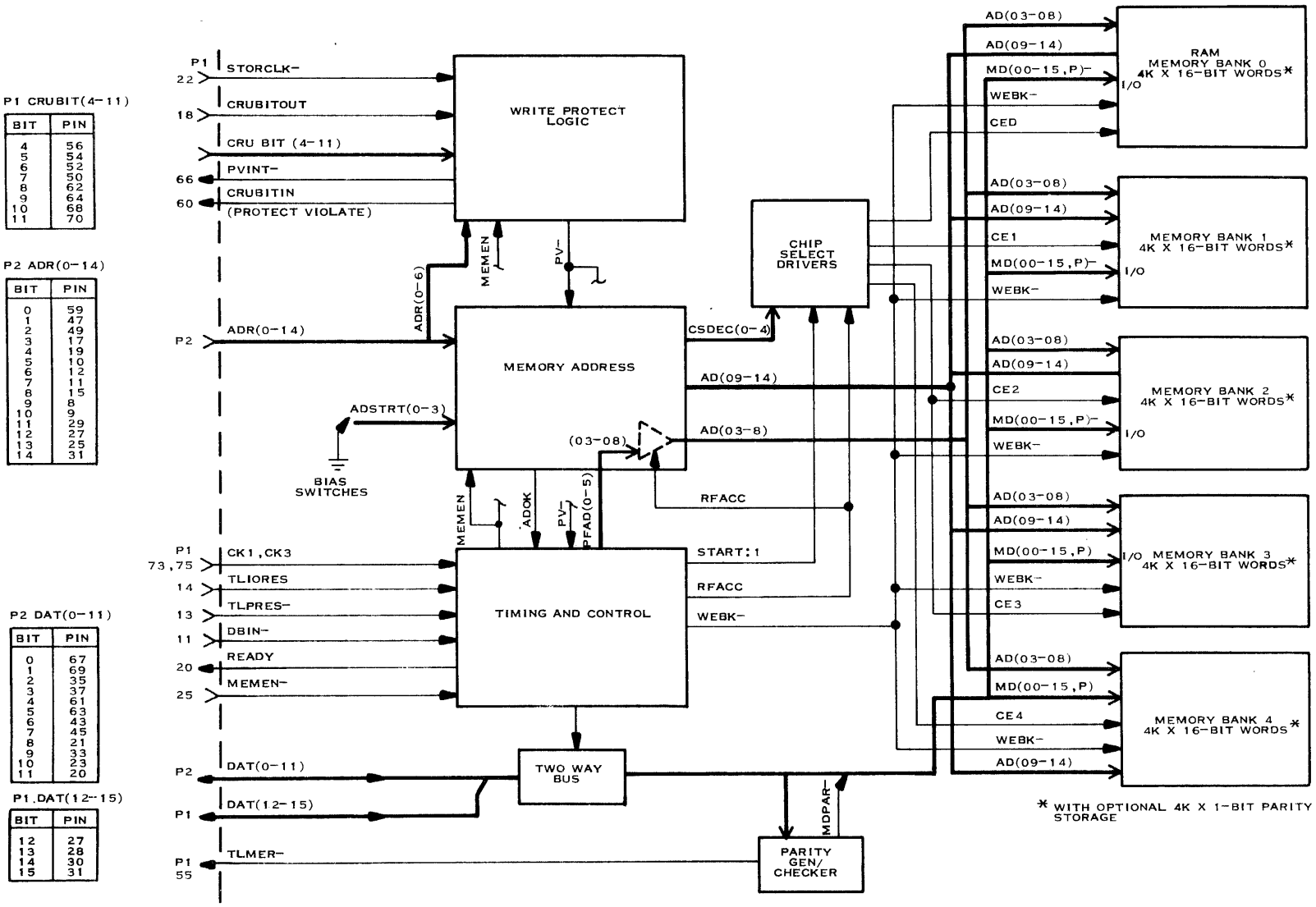


Figure 3-32. 990/4 Memory Expansion Board Block Diagram

The three most significant bits of the address bus, AD00- through ADR02-, are inverted and applied to an address start encoder as signals ADRIN00 through ADRIN02 where the bits are compared to the start address as determined by the state of switch-selected bits ADSTRT0- through ADSTRT2-. Starting addresses are established in 1's complement form. For example, to establish a start address at location 2000_{16} the address start bits (ADSTRT0- through ADSTRT2-) would be OPEN, OPEN, CLOSED. The address start encoder consists of an SN74LS283 4-bit binary full adder and when the address selected by the three most significant address bits is equal to or greater than the switch-selected start address a high GTEMIN signal is generated at the output of the start address encoder. Also, output signals CSSUM0 through CSSUM2 from the address start encoder represent the binary difference between the switch-selected start address and that address contained in the three most significant bits of the address bus and are used to determine which 4K memory bank to enable. Signals CSSUM0 through CSSUM2 along with GTEMIN are applied to upper limit address logic that consists of another SN74LS283 4-bit binary full adder. Here the signals are compared with option jumper signals JMP0 through JMP2. The option jumpers are strapped to correspond to that amount of memory implemented on the memory expansion module. Jumper options for the 990/4 memory expansion board are shown in figure 2-22 and listed in table 2-3.

When the memory address is not higher than the upper limit address, a high GTMAX- signal is generated at the output of the SN74LS283. The high GTEMIN signal output of the address start encoder signifies that the memory address is equal to or greater than the switch-selected start address and a high GTMAX- signal output from the upper limit address logic signifies that the address does not extend beyond the upper memory address limit. Both signals are applied to AND gate along with the high MEMEN signal that is generated indicating that the externally generated memory request pertains to this particular memory expansion module.

The memory protect option when implemented consists of a 16-bit write-protect data shift register that is addressed by the CRU, a 7-bit upper bound register, and a 7-bit lower bound register. To implement the memory protect feature, a 16-bit LDCR instruction must be executed to load the write-protect data shift register after each power-up since the low TLIORES- signal, generated when dc power is down, provides a low TLIORST- signal that clears the write-protect data shift register. When cleared, the low BIT00- output of the write-protect data shift register applied to an AND gate generates a low PROTWEN signal. The low PROTWEN signal applied to a NAND gate causes protect violation signal PV- to go high and the memory protect feature of the memory expansion module is disabled.

To use the memory protect feature, a LDCR instruction addressed to CRU base address $1FA0_{16}$ develops a high MODSEL signal that is ANDed with the STORECLK- signal and a 16-bit data word is clocked into the write-protect data shift register. The most significant bit of the data word, BIT00, is programmed low to enable the write protect circuitry. With BIT00 low, the inverted BIT00- output of the write-protect data shift register is high and it is this signal ANDed with DBIN- (high during a memory write operation) that develops the high write protect enabling signal, PROTWEN. At the output of the write-protect data shift register, BIT00- through BIT07- are applied to the lower bound protect register to set the lower bound of the protected zone (that is inclusive) and BIT09 through BIT15 are applied to the upper bound protect register to set the noninclusive upper bound. When address bits ADRIN00 through ADRIN06, applied to both the lower and upper bound protect register, address memory for a memory write operation within the protected zone a high GTELB signal and a low GTEUB signal are generated at the output of the two registers. The low GTEUB signal is inverted as the high GTEUB- signal that in turn is ANDed with GTELB to develop a high OUTBOUD signal.

The high OUTBOUD signal, along with enabling signals PROTWEN and MEMEN are applied to a NAND gate to send protect violation signal PV- low. The low PV- signal ANDed with ADOKL prevents the ADOK signal from being developed. The low PV- signal also generates the PVINT- signal that is applied to the 9900 memory bus to signify that a memory write protect violation has occurred.

In summary, when the three most significant bits of the address bus, ADRIN00 through ADRIN02, generate an address equal to or greater than the switch-selected start address of the memory expansion module but that does not exceed the jumper-strapped upper limit address then the resultant high GTEMIN and GTEMAX- signals ANDed with the high MEMEN signal generate the high ADOKL signal. Further assume that: a memory read operation is to be executed, memory protect logic is either not implemented or disabled, or during a memory write operation the addressed memory does not encroach into the protected zone. If any one of these conditions are met, a high PV- signal is generated and is ANDed with the high AKOKL signal and the resultant high ADOK signal signifies that the memory expansion module has been addressed with a valid address. The high ADOKL signal is also inverted and used to enable a three-state driver. If a memory refresh cycle is not in progress, the refresh access signal RFACC input to the driver is high to provide the high READY signal that indicates to the external processor that during the next $\phi 1$ clock data and error lines may be read.

When a protect violation occurs, the resultant low PV- enables a three-state driver to generate a low protect violation interrupt signal, PVINT-, at pin P1-66. Additionally, PV- at the input to a flip-flop develops the protect flag PVFF. By issuing an STCR instruction, the protect error flag is read into all 16 data bit positions of the input data word via CRUBITIN. The protect error flag is reset either by the low TLIORST- signal generated during dc power down or may be reset by programming BIT00 high and issuing an LDCR instruction to CRU base address $1FA0_{16}$.

If the write protect option is not installed on the 990/4 memory expansion board, a jumper wire must be installed between terminals E7 and E8 as shown in figure 2-22.

3.3.1.2 **Memory Read, Memory Write Data Bus Enable.** The high ADOK signal generated when the memory expansion module has been addressed is applied as one input to a NAND gate along with the normally high (when dc power conditions are stable) PRES- signal to generate a low ADOK- signal. The low ADOK- signal is ORed with the RFACC- signal at the input to the memory cycle timer to start a memory cycle. The high ADOK signal is also applied as one input to two separate NAND gates for use as a data bus enable signal. If the memory cycle initiated is to be a read from memory, the DBIN signal from the 9900 Memory Bus will be high. The high DBINA is ANDed with ADOK and RFACC- (when memory refresh cycle not in progress) to generate a low RDEN- signal that is applied to sixteen 3-state drivers to enable the data bus for a memory read operation. The low DBIN- signal ANDed with the ADOK and the RFACC- signals at the input to the other NAND gate sends WDEN- high and the sixteen 3-state drivers in the memory write data path of the data bus are set to their high impedance state. For a memory write cycle, a low DBIN signal produces a low WDEN- signal and a high RDEN- signal to enable the memory write data path of the data bus.

3.3.1.3 **Memory Timer.** The memory timer provides a timed enabling signal, START, to memory for both read and write memory cycles. This includes timing for the memory refresh cycle that is in itself a memory read operation. Either a low ADOK- signal, in the instance of a read or write operation when the memory is addressed on the address bus, or a low RFACC- signal, wnen a memory refresh cycle is to occur, at the input to the memory timer provide a high SETSTART input to a D-type flip-flop. The next CLK3- pulse applied to the clock of the flip-flop clocks out a high START signal at the Q output of the flip-flop. The START signal is applied as a write-enable at the input to a NAND gate when all other conditions for a memory

write operation are met at the input to the NAND gate, and the high START signal is also applied to the D-input of a second flip-flop in the memory timer. The low START- signal at the Q- output of the first flip-flop in the memory timer is applied to a NAND gate at the clock input to a flip-flop in the refresh cycle controller to inhibit generation of a RFACC- signal during the memory cycle in progress and is also applied to an inverter to generate a high START:1 signal that is applied to the clock of the five chip select flip-flops. The CSSUM0 through CSSUM2 signals (generated as described in paragraph 3.3.1.1) applied to a 4K memory bank chip select decoder are decoded to provide a low to the D-input of one of the five flip-flops. The positive transition of the START:1 signal at the clock of that flip-flop sets the Q-output of the flip-flop high to enable one of five 12-volt driver circuits. The enable driver circuit develops a 12-volt chip enable signal (one of signals CE0 through CE4) that is applied to the CE pins of sixteen TMS 4050's (seventeen if parity option implemented) to enable a 4K memory bank.

The high START input to the second flip-flop of the memory timer is clocked out as a buffered STRTDLBY signal by the second CLK3- pulse of the memory cycle. The STRTDLBY signal is applied as one of two inputs to two AND gates. If the memory cycle in progress is a write operation, the DBIN- signal is high. This high is ANDed with STRTDLBY to generate a low memory cycle and MCYEND- signal. For a memory read cycle the DBIN- signal is low and the MCYEND- signal is not generated until CLK1 that is ANDed with STRTDLBY goes high after STRTDLBY is generated. In either event, MCYEND- clears the two flip-flops in the memory timer to remove the enabling signals, START and START-, to ready the memory timer for a new memory cycle.

Refresh MCYEND-'s are entirely dependent on the DBIN line at the time STRTDLBY goes high and MCYEND- may be generated either in the memory write or memory read operation method.

3.3.1.4 Refresh Cycle Controller. The refresh cycle controller consists of a refresh timer, two flip-flops, a binary counter, and a data selector. At the heart of the refresh cycle controller is the refresh timer. The values of two external resistors and a capacitor have been chosen to cause the timer to run in the astable mode of operation at a frequency of 64 cycles every 2 milliseconds. The time period for each cycle is 31 microseconds; a 20 microsecond positive pulse and an 11 microsecond negative pulse. The buffered OSCA signal output of the timer is applied to a 64-count binary counter to increment the counter by one for each refresh memory cycle. The OSCA signal output of the timer is also applied to the clock of the first of the three refresh flip-flops to generate a refresh required RFREQD signal. RFREQD is synchronized with CLK3- at a second flip-flop and applied to a third refresh flip-flop. If START- is high, indicating that a memory cycle is not now in progress, the trailing edge of CLK1 clocks the flip-flop to generate the refresh access signals. The low RFACC- signal applied to a three-state driver provides a low READY signal output to indicate the not-ready state of memory if it is addressed during a memory refresh cycle. The low RFACC- signal is also applied to the input of the memory timer as previously described to initiate a timed memory cycle. Additionally, the low RFACC- signal is applied to the select pin of the data selector and the data selector selects the output of the binary counter, RFAD00 through RFAD05, to address the memory chips at row address pins A0 through A5. The low RFACC- signal applied to a NAND gate develops the high WEBK- signal that inhibits a write operation. The high RFACC signal output of the refresh cycle controller is ANDed with the high START:1 signal output from the memory timer to generate a low RFCS- signal that is applied to the clear pins of the five flip-flops in the 12-volt driver circuits to enable each circuit to develop a high chip enable signal for each of the 4K memory banks during the memory refresh cycle. The low RFACC- signal clears the first two flip-flops in the refresh cycle controller and on the next CLK1 clock trailing edge after START is reset the third flip-flop is reset and the refresh cycle is ended as RFACC goes low and RFACC- goes high. The data selector returns to normal selection of memory address bits ADRIN03 through ADRIN08 to address row address pins A0 through A5 of the memory devices.

3.3.2 MEMORY EXPANSION READ/WRITE OPERATION. For a memory read operation, the microprocessor or an external DMA device addresses the memory expansion module on the 9900 Memory Bus and a high DBIN signal on the 9900 Memory Bus to enable the memory read path of the memory expansion module data bus. One 4K memory bank has been enabled for a memory read and write operation by one of the chip enable signals CE0 through CE4 applied to chip enable pins of the memory devices. The low DBIN- signal generated by the high DBIN is applied to a NAND gate to develop the high WEBK- signal to set the enabled memory devices to the memory read mode of operation and the memory word as addressed by memory address bits AD03 through AD14 is placed on the data bus for input to the 9900 Memory Bus. A memory write operation occurs in the same manner except that a low DBIN is preset on the 9900 Memory Bus. The resultant high DBIN- that is ANDed with the High PRES-, RFACC-, and START signals sends WEBK- low to set the memory devices to the memory write mode of operation and the data on the data bus is written into memory in the location addressed by memory address bits AD03 through AD14.

3.3.3 PARITY GENERATION/PARITY CHECK OPTION. Parity is implemented on the memory expansion board by installing a seventeenth TMS 4040 memory device for each implemented memory bank for storage of the parity bit, MDPAR-, and by installing two Texas Instruments Type SN74180 parity generators/checkers. A parity bit (MDPAR-) is generated that makes the total number of ONE's in the data word and the parity bit, inclusive, odd. In a memory write operation, WDEN- is low to enable a 3-state driver at the parity bit output of the parity generators/checkers. With the driver enabled and with the memory devices enabled and in the write mode, the parity bit is stored in memory as the seventeenth bit of the data word. For a memory read cycle, the data word along with its parity bit is read from memory and applied to the parity generators/checkers. The WDEN- signal that is now high during the memory read operation enables an AND gate that has its output applied to the odd input and its inverted output applied to the even input of one of the parity generator/checkers. The parity bit applied as the other input to the AND gate controls the sense of the inputs to cause a low memory error signal, PARERR-, to be generated if the word read from memory is not one of odd parity. The low PARERR- signal applied to a 3-state driver that is enabled by RDEN, low during a memory read operation, generates the low TLMER- memory error signal for application to the memory bus. The low PARERR- signal also causes the parity LED on the memory expansion module to light and give visual evidence of a parity error. The LED remains active until reset by software (TLIORES-), power-up (PRES-), or manual reset (MANRST-).

3.4 EPROM MEMORY MODULE

The EPROM memory module is an optional memory board with IC sockets and associated control circuitry to accommodate from 1K to 8K of 16-bit words (field expandable) of erasable, programmable, read only memory (EPROM). This memory is implemented with INTEL 2708 1024 by 4-bit EPROM ICs. Two memory chips are required for each 1K memory bank. As shown in figure 2-23, a maximum of eight memory banks may be installed on the board with the leftmost column identified as bank 0 and the rightmost vertical column of two chips bank 7.

3.4.1 EPROM FUNCTIONAL THEORY. As shown in figure 3-33, the incoming address lines ADR(0-14) from the 990/4 Microcomputer board (or direct memory access device) map onto the EPROM address inputs TLADR(05-19), respectively. Address lines TLAD(00-04) are not used in the 990/4 System.

The incoming user memory address is biased with the starting address inputs from bias switch SW2 and processed in adder stages U28, 38 and 30, and gating stages U20 and U31. This process determines if the address is within the address space assigned to the EPROM memory and that the address does not exceed the amount of memory implemented on the board. If the address is

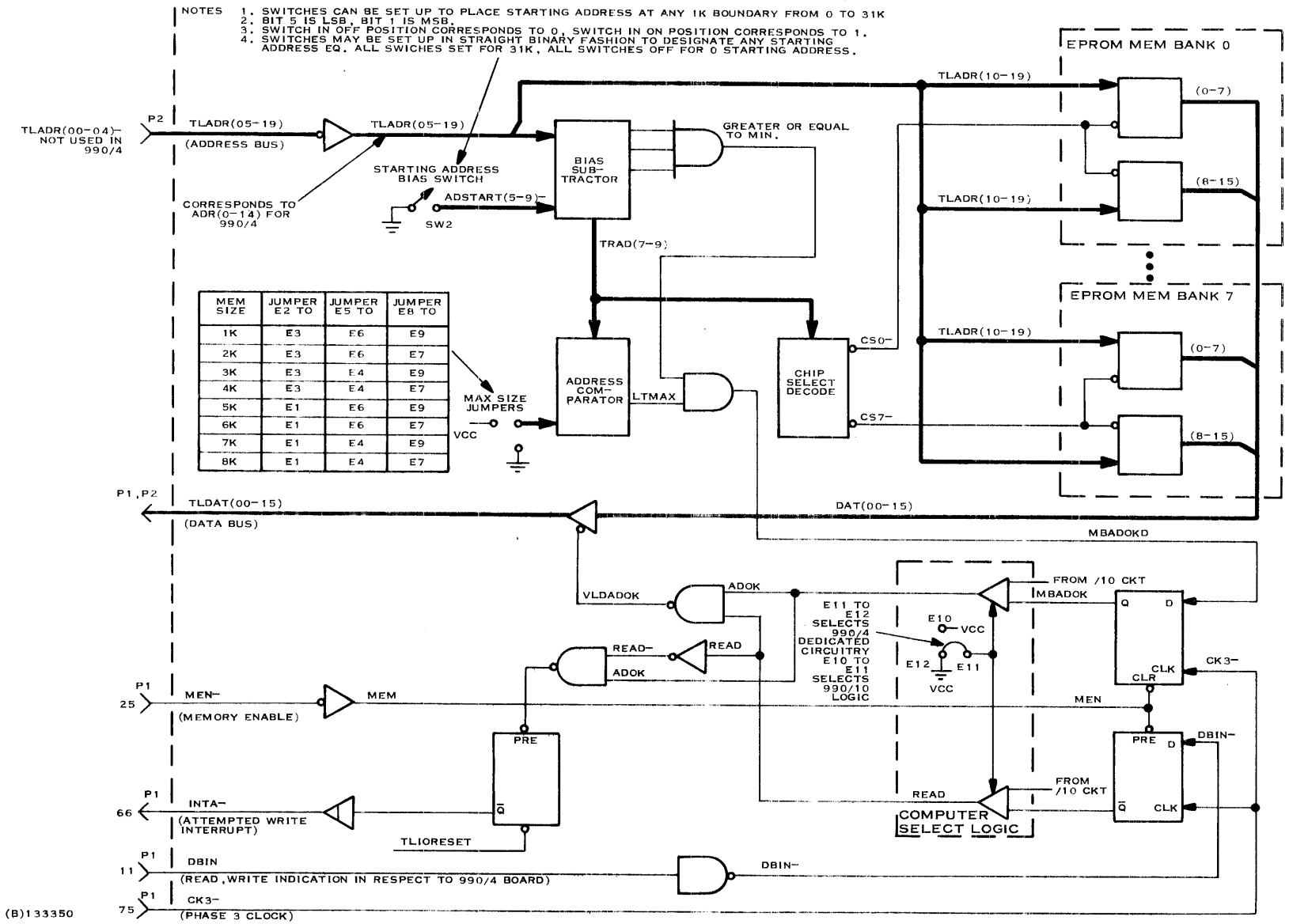


Figure 3-33. EPROM Memory Module Block Diagram

valid, a memory bus address OK (MBADOKD) is generated which is synchronized with the buffered 3-phase clock from the 990/4 Microcomputer board and gated with Memory Enable to generate MBADOK (address OK). This signal is routed through the Computer Type selector to generate address OK (ADOK) which initiates the memory cycle. ADOK, in turn, enables the chip select decoder which decodes the biased user address lines to enable 1 of 8 1K banks. At the same time, DBIN from the user is synchronized with the 3-phase clock and enabled through the Computer Type selector as READ. READ is gated with ADOK to enable the addressed data output onto the output data lines.

The READ signal is also inverted and gated with ADOK to generate an interrupt (INTA–) in the event that a write cycle is attempted in the memory address space assigned to EPROM memory.

3.4.2 **Memory Options.** The following paragraphs describe the jumper wire options that must be incorporated prior to installing the EPROM board in the system:

3.4.2.1 **Computer Type ID Jumper.** The 990 EPROM memory module may be used in either a 990/4 or 990/10 Computer. For use in a 990/4 chassis, a jumper wire must be installed between terminals E11 and E12 (E10 to E11 designates 990/10 chassis).

3.4.2.2 **Starting Memory Address Bias.** The starting address of the EPROM memory module may be placed at any 1K boundary in the 990/4's 32K address space between 0 and 31K as controlled by the five switch positions on DIP switch S2. Switch bit 1 is the MSB, and switch bit 5 is the LSB. To select a starting address, the switches are set up in straight binary fashion with a switch in the "on" position designating a logic 1 and a switch in the "off" position designating a logic 0. For example, a starting address at 0 would be set up with all five switches in the "off" position; a starting address at 1K would have only switch 5 set to the "on" position and all others set to the "off" position; and a starting address of 31K would have all five switch bits set to the "on" position. A listing of all possible starting addresses and the associated switch settings are provided in table 2-4.

3.4.2.3 **Memory Size Jumpers.** A group of nine terminals (E1 through E9) are used to encode the amount of memory implemented on the board (1K to 8K). These jumpers are set up as follows:

Memory Size	Jumper Connections
1K	E1-E2, E4-E5, E7-E8
2K	E1-E2, E4-E5, E8-E9
3K	E1-E2, E5-E6, E7-E8
4K	E1-E2, E5-E6, E8-E9
5K	E2-E3, E4-E5, E7-E8
6K	E2-E3, E4-E5, E8-E9
7K	E2-E3, E5-E6, E7-E8
8K	E2-E3, E5-E6, E8-E9

3.5 990/4 CHASSIS

The 990/4 circuit board may be installed in any one of three basic chassis configurations: the OEM chassis, the 6-slot chassis or the 13-slot chassis. The configurations are discussed in the paragraphs that follow.

3.5.1 **OEM CHASSIS.** The OEM chassis is a minimum configuration chassis consisting of a card support and a backpanel that provides connectors and mounting space for three full-sized logic boards. Each board position is subdivided physically and electrically so that it may accommodate two half-sized logic boards. One full-sized board position is required for installation of the 990/4 circuit board. Interconnect wiring is in the backpanel etch. The user must supply power and cooling for the OEM chassis. The OEM chassis is not equipped with fans, therefore, it must be supplied with an average input air flow of 600 feet per minute through the chassis. When so supplied, each full-sized board position will support a 50-watt heat load.

Maximum exhaust temperature should be 65°C (149°F). The physical configuration and dimensions of the OEM chassis are as shown in figure 3-34. The OEM chassis backpanel wiring is as shown in figure 3-35.

Connections from the user's power supply to the OEM chassis and the control lines are made at the terminal strip at the rear of the chassis, TB1. See paragraph 2.6 and figure 2-15. As shown in figure 3-35, a power reset circuit that develops the power reset signal, TLPRES, is included as an integral part of the backpanel. The power reset circuit consists of a two-transistor Schmitt trigger that controls transistor Q3 so that a high TLPRES– signal is developed approximately 250 milliseconds after power is applied to the chassis to indicate that dc power is up and stable. The low TLPRES– signal during the power-up sequence is used to reset connected devices. Available to the user at the terminal board are the RESET and RSTRT terminals. A low applied to the RESET terminal causes the microprocessor to initiate a level 0 interrupt and trap to memory location 0000. A low at the RSTRT terminal causes the microprocessor to execute a nonmaskable interrupt with memory location $FFFC_{16}$ containing the trap vector. The EXT CLOCK terminal allows the user to supply a real-time clock signal to implement real-time clock logic on the 990/4 circuit board. Instructions for installation of interrupts for the OEM chassis are in paragraph 2.7.

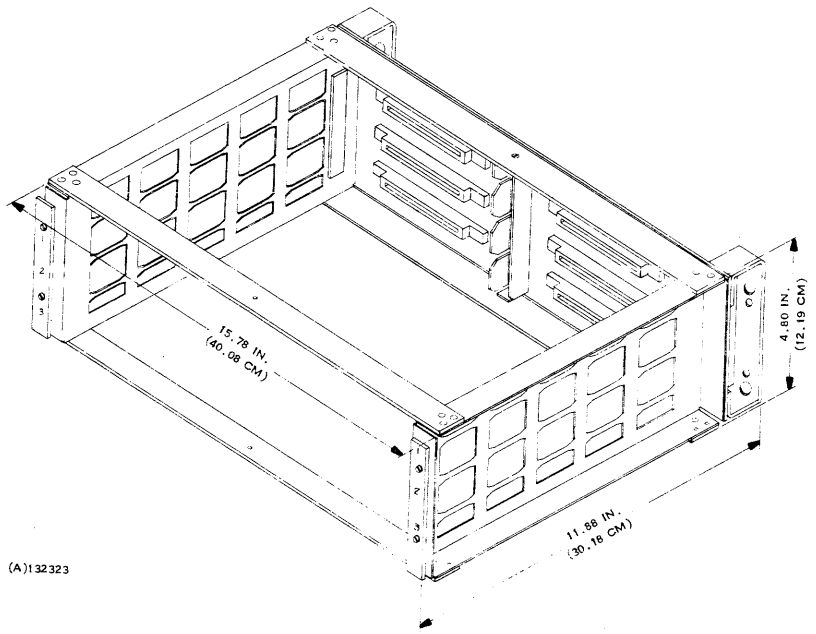


Figure 3-34. OEM Chassis Physical Configuration

3.5.2 **6-SLOT CHASSIS.** The 6-slot chassis provides full support that includes backplane wiring, power and cooling air for six full-sized logic boards. Two half-sized logic boards may be substituted for one full-sized board in any slot except the initial slot that is wired to accept the 990/4 circuit board (or CRU buffer board of chassis is used as an expansion chassis).

The 6-slot chassis is available in two different configurations: one configuration is supplied with an operator front panel assembly and the other with a programmer fromt panel assembly. The operator front panel assembly is basically a blank panel with indicators and switch as shown in figure 3-36. The programmer front panel is intended for use in applications requiring software troubleshooting. Panel controls may be locked out by a key-operated switch to prevent inadvertent use of the controls. A detailed description of the programmer panel is provided in paragraph 3.7.

The CRU, 9900 Memory Bus, and system reset signals are distributed to the individual chassis slots on backplane wiring.

The 6-slot chassis includes the card support and backpanel for the 6 slots, an ac power converter, a 20-ampere power supply and two fans for cooling. The chassis will support a 170-watt heat load in the power supply area and a 50-watt heat load for each full-sized board position. The maximum temperature of exhaust air is designed to be 65°C (149°F) for manufacturing and office installations.

Chassis slide kit or tabletop chassis options are available. The chassis slide kit consists of chassis slides and hardware for mounting the chassis in a standard 19-inch RETMA rack. The tabletop chassis option consists of a tabletop enclosure cover with mounting brackets to provide a dust-proof enclosure for desk or tabletop operation.

An international voltage option kit consisting of a transformer and necessary hardware permits the chassis to be operated from 100 V, 200 V or 230 V ac line voltages.

A standby power supply to provide standby power for volatile memory protection in the event of a primary power failure is available as an option. The standby power supply consists of batteries and a standby power supply/charger that installs in either the 6-slot or 13-slot chassis in the area behind the backpanel reserved for the power supply. The unit supplies +5 MEM, +12 MEM and -5 MEM power. A detailed description of the standby power supply is provided in paragraph 3.6.3. The 20-ampere power supply is an offline ringing choke (sometimes referred to as flyback) dc-to-dc converter.

The ac power converter full-wave rectifies the primary ac input to the chassis to provide the 160-volt dc input power to the 20-ampere power supply and to the standby power supply (if that option is implemented). A second full-wave rectifier develops a 120-Hz pulse that is optically coupled to the 20-ampere power supply where it is further refined and furnished as the line frequency synchronized real-time clock interrupt signal to the 990/4 circuit board. A detailed description of the ac power converter is provided in paragraph 3.6.1. The physical configuration and dimensions of the 6-slot chassis are as shown in figure 3-37. Chassis wiring for the 6-slot chassis is as shown in figure 3-38.

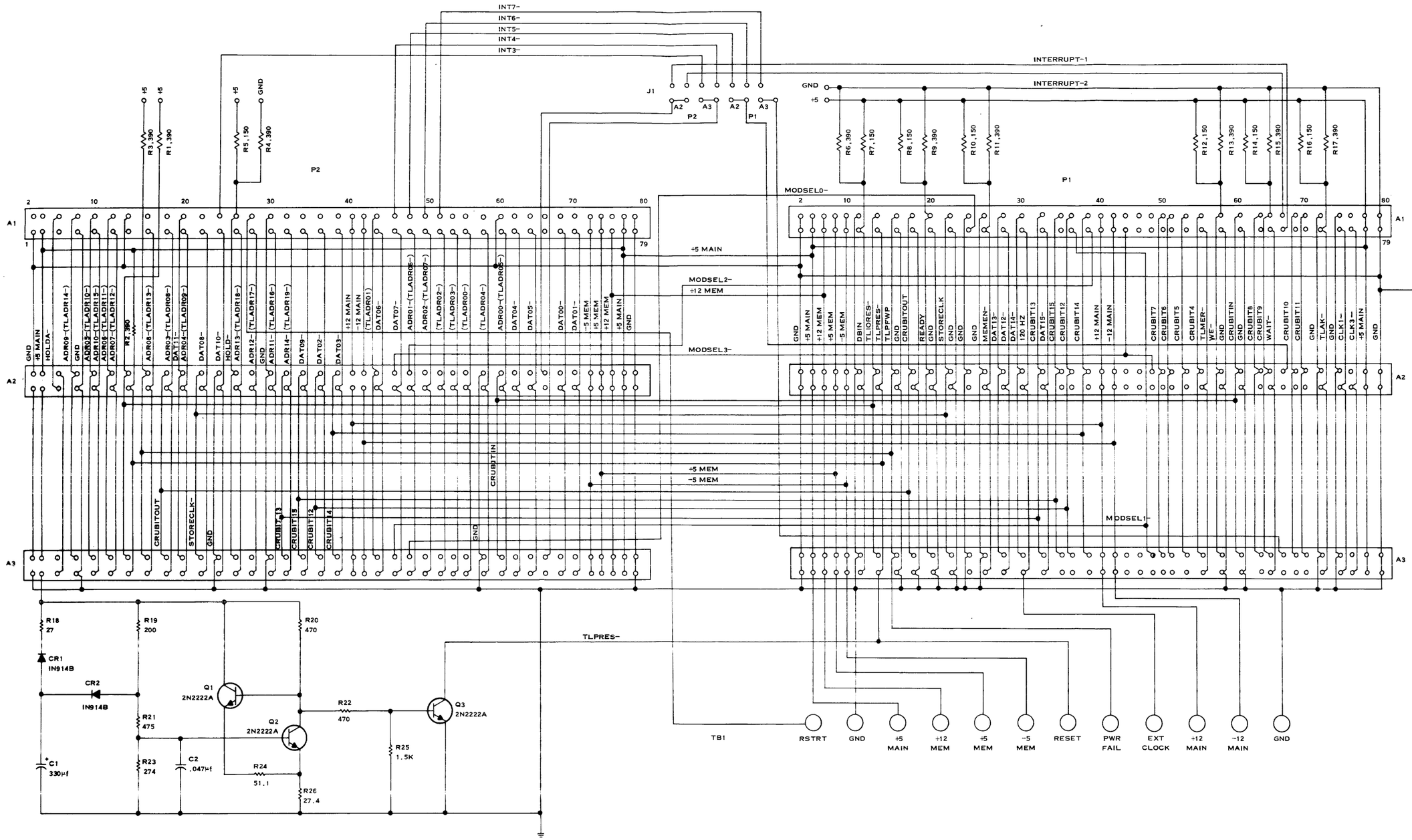


Figure 3-35. OEM Chassis Backpanel Schematic

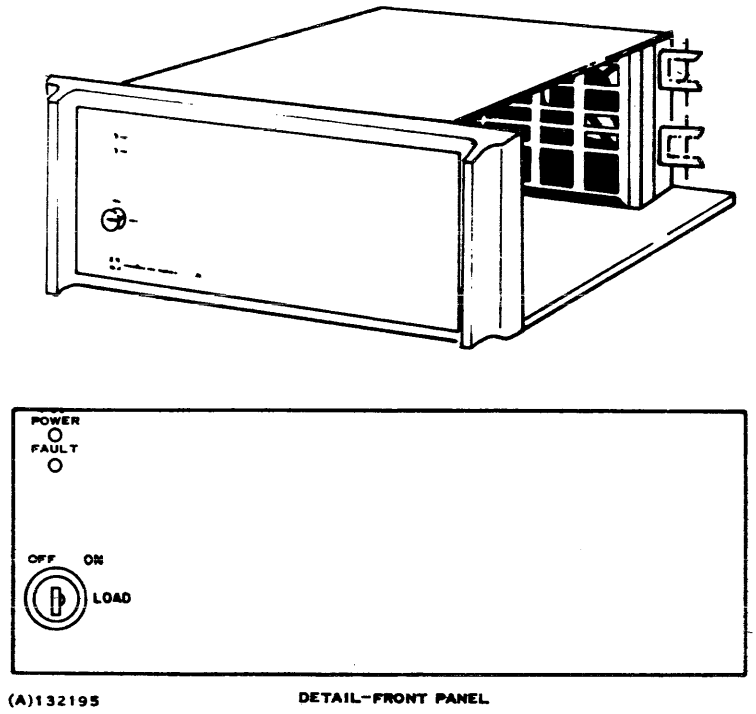


Figure 3-36. Operator Front Panel, 6-Slot Chassis

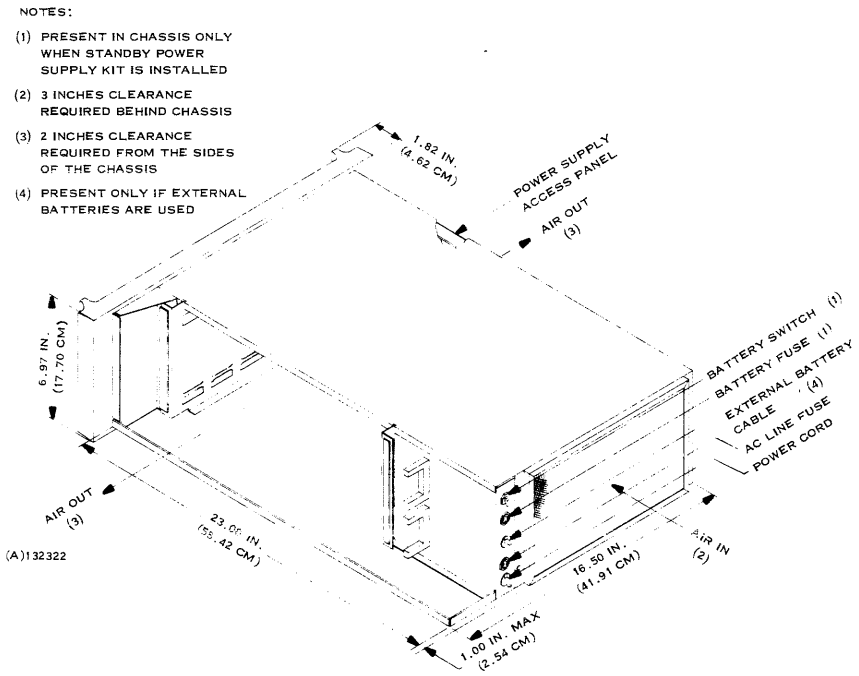


Figure 3-37. 6-Slot Chassis Physical Configuration

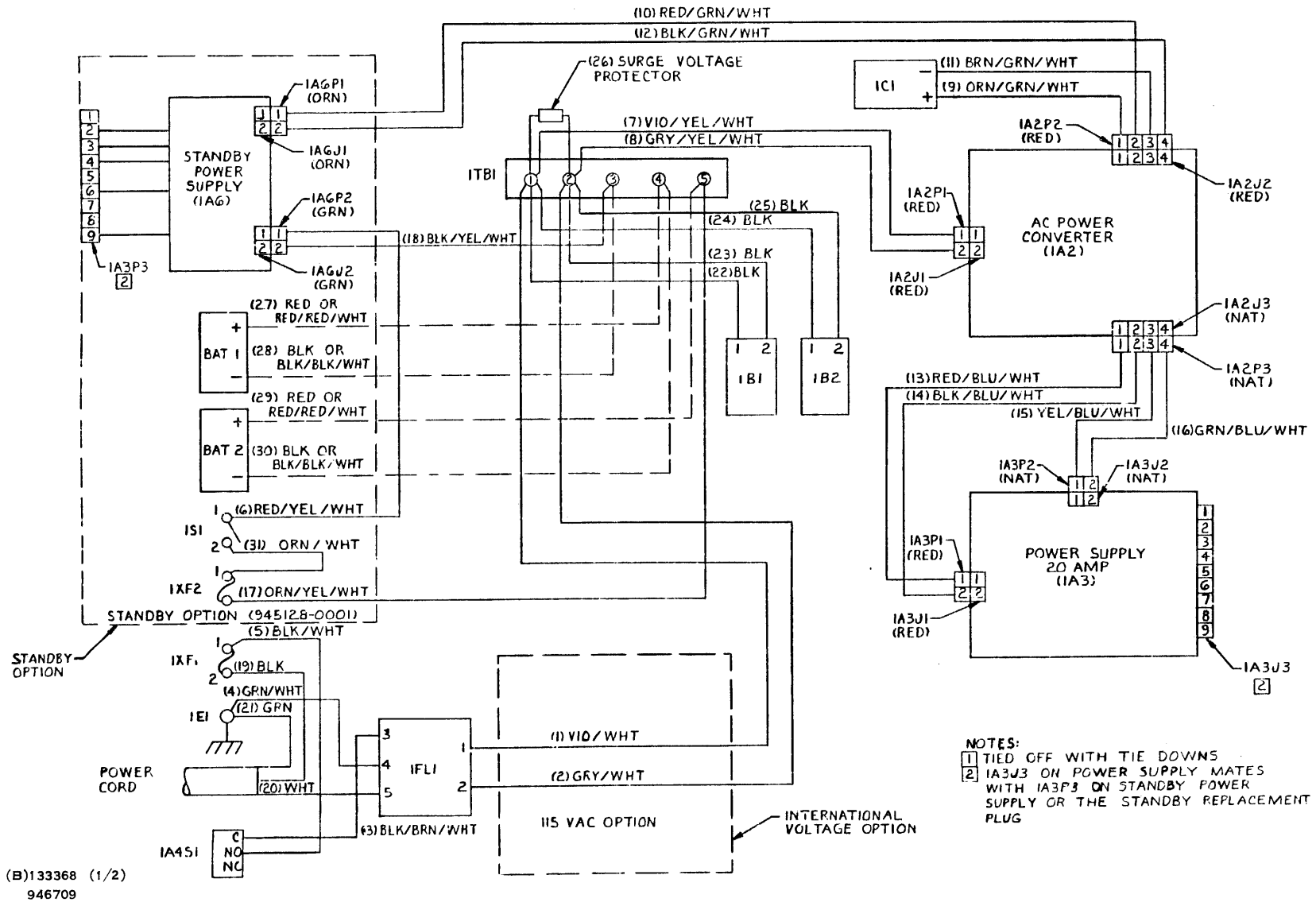


Figure 3-38. 6-Slot Chassis Wiring Diagram (Sheet 1 of 2)

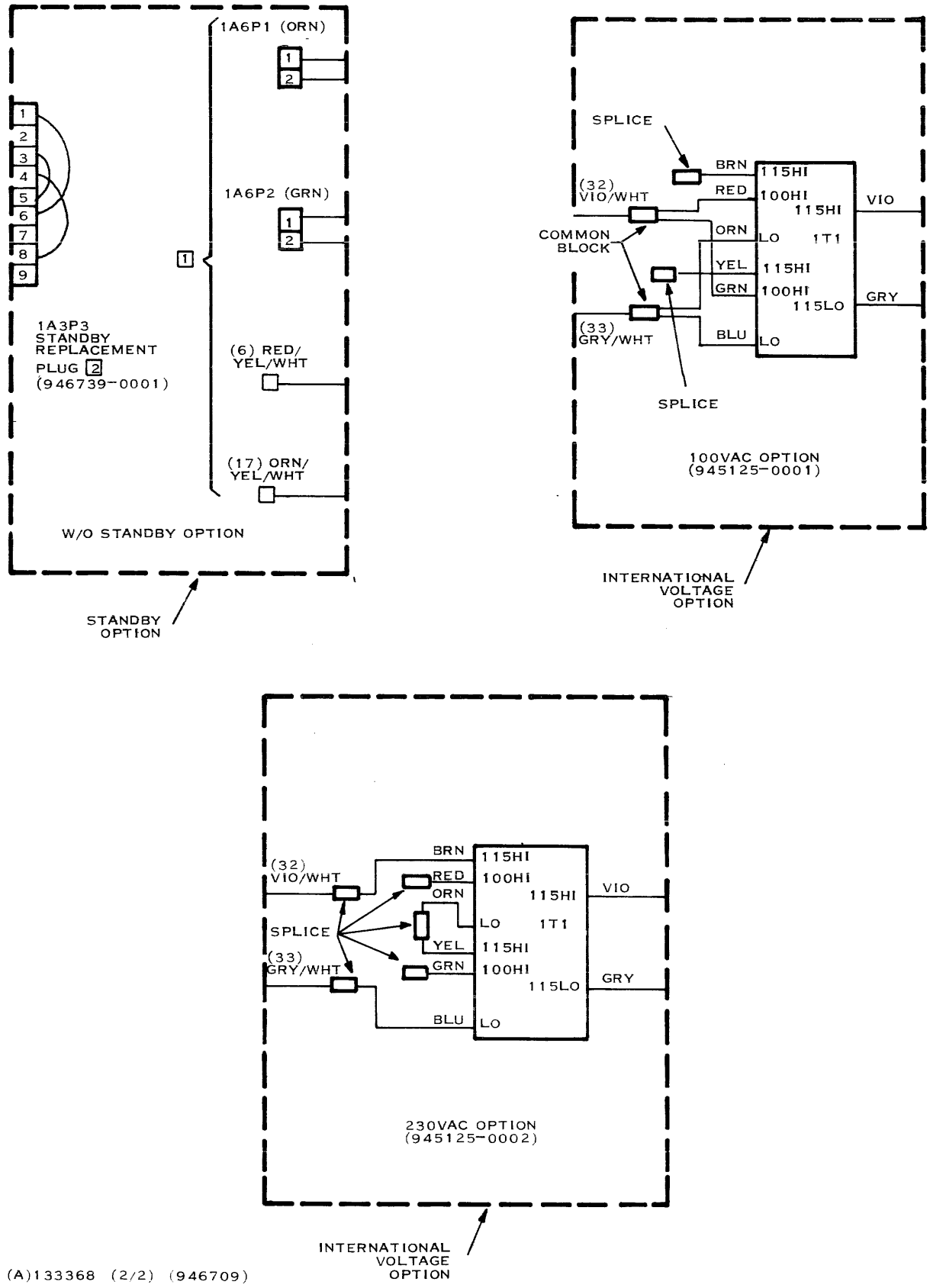


Figure 3-38. 6-Slot Chassis Wiring Diagram (Sheet 2 of 2)

3.5.3 **13-SLOT CHASSIS.** The 13-slot chassis is basically an enlarged version of the 6-slot chassis and will provide full support (backplane wiring, power and cooling) for 13 full-sized logic boards. Two half-sized boards may be substituted for one full-sized board in all but the initial slot reserved for the 990/4 circuit board (or CRU buffer board in an expansion chassis). The 13-slot chassis is also available in either the operator front panel or programmer front panel configuration but is not available in the tabletop chassis option. Other characteristics of the 13-slot chassis are as described for the 6-slot chassis in paragraph 3.5.2.

The physical configuration and dimensions of the 13-slot chassis are as shown in figure 3-39. Chassis wiring for the 13-slot chassis is as shown in figure 3-40.

3.6 CRU EXPANSION

From one to seven 990 I/O expansion chassis may be added to a 990/4 System when the main chassis does not contain enough board slots to house all of the required CRU interface boards. The chassis used as an I/O expansion chassis is identical to the main computer chassis except that it contains an operator panel instead of a programmer panel and slot 1 of the expansion chassis houses a CRU buffer board instead of a 990/4 Microcomputer board. Also, the interrupt wiring for the expansion chassis is accomplished through jumper plugs on the backpanel board similar to the main chassis except that all 15 levels are implemented in the expansion chassis. The dc power supplies in the expansion chassis are identical to the power supply used in the main chassis except that a standby supply is not used with an expansion chassis.

The operator panel on the expansion chassis contains a key switch which controls ac power to the chassis and a POWER LED which indicates when the power supplies are functioning properly. The interconnection between the operator panel and the CRU buffer board is accomplished through a 26-pin ribbon cable and connector which attaches to connector plug P5 on the top edge of the buffer board. The interface between the main chassis and the expansion chassis is accomplished through a 12-foot ribbon cable (Part Number 945001-1) which attaches to one of the seven ports on the CRU expansion board in the main chassis (P3 through P9 depending on chassis number) and attaches to plug P3 on the top edge of the CRU buffer board in the expansion chassis. A simplified block diagram of the CRU expansion system is shown in figure 3-41.

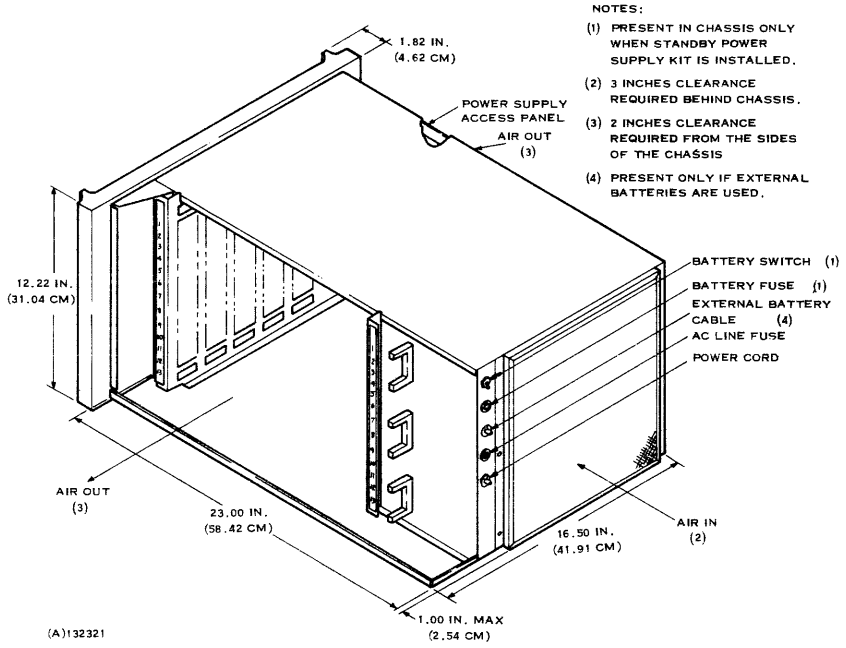


Figure 3-39. 13-Slot Chassis Physical Configuration

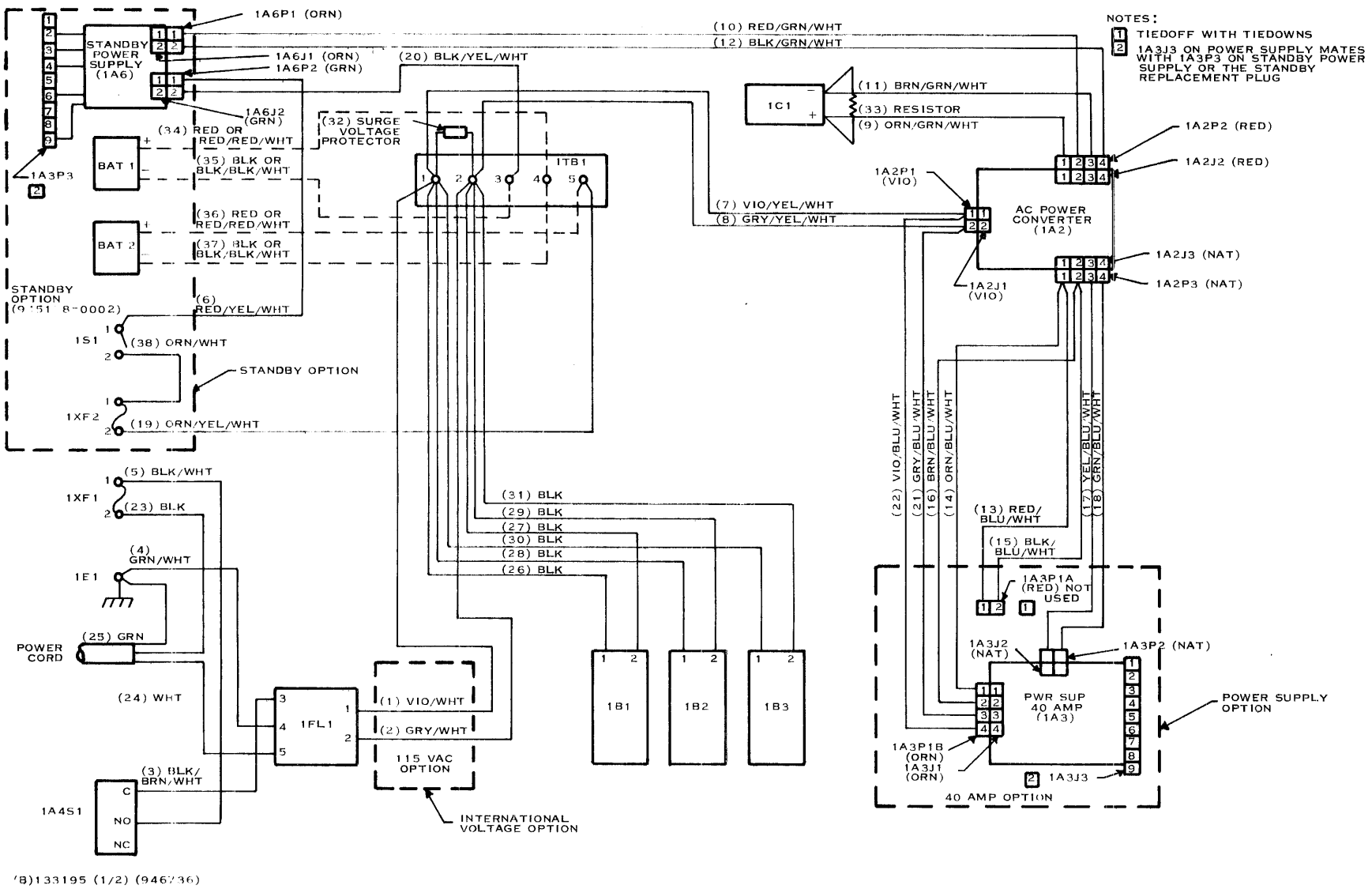
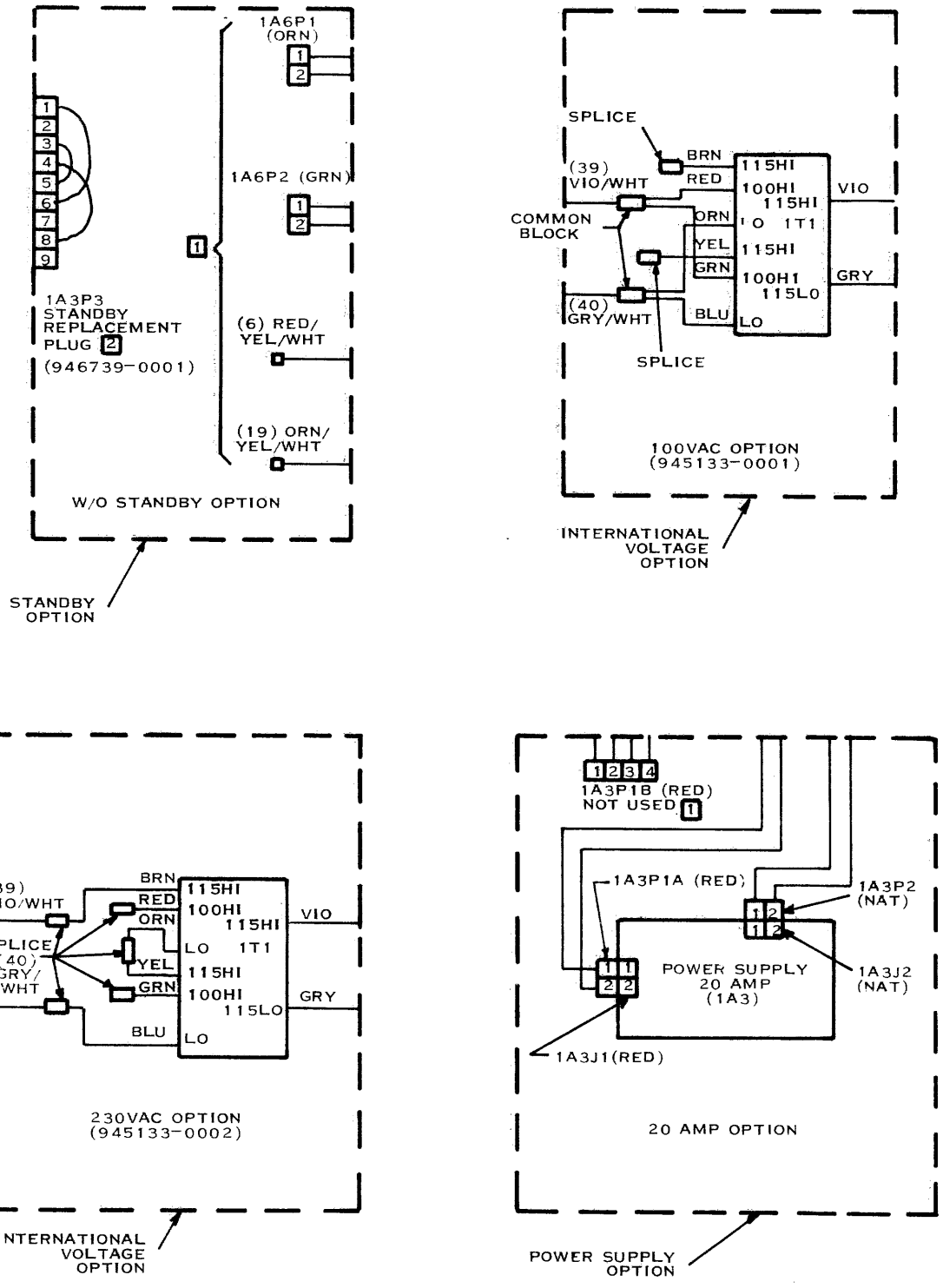


Figure 3-40. 13-Slot Chassis Wiring Diagram (Sheet 1 of 2)



(A)133195 (2/2) (946736)

Figure 3-40. 13-Slot Chassis Wiring Diagram (Sheet 2 of 2)

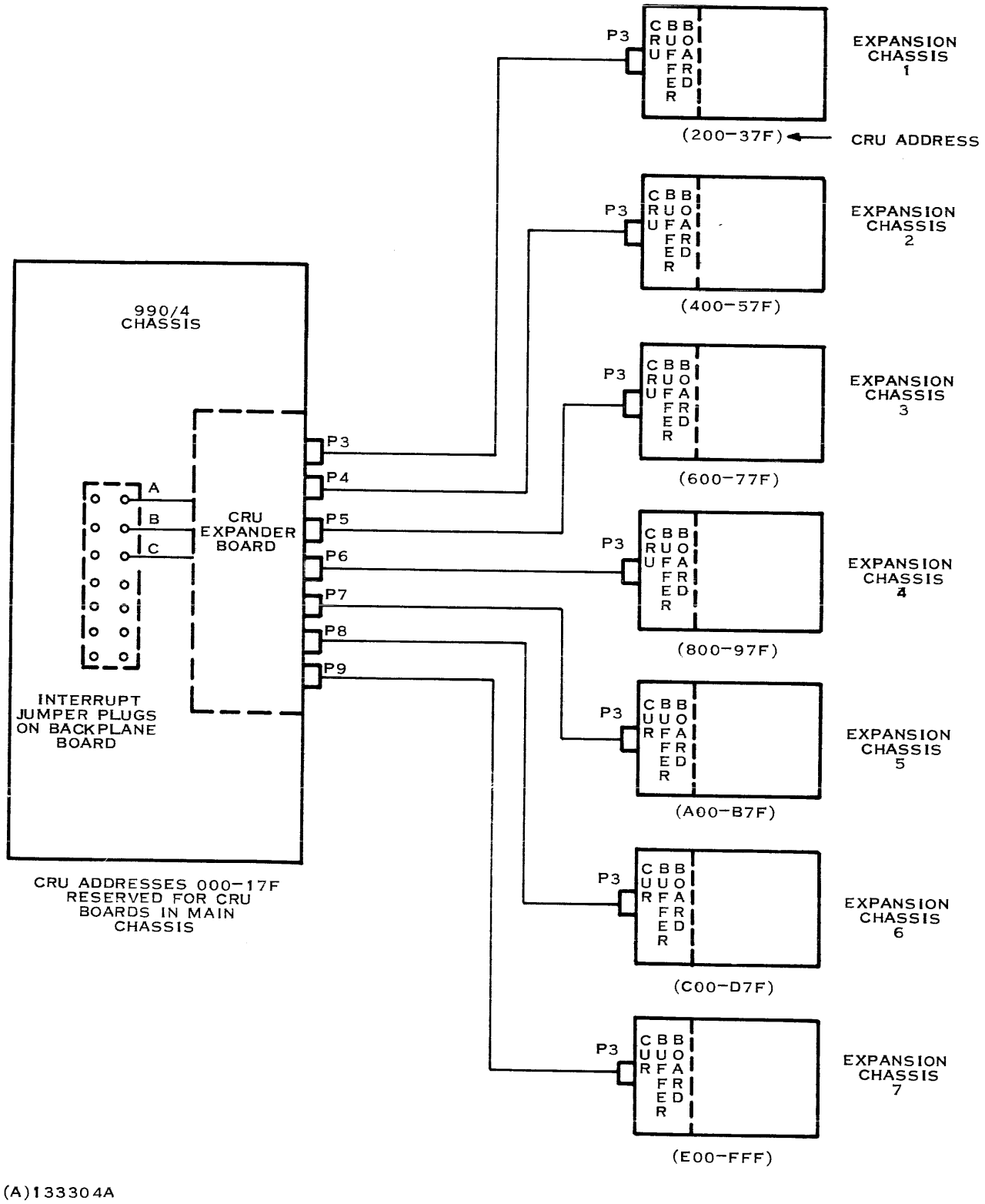


Figure 3-41. CRU Expansion, Simplified Block Diagram

3.6.1 **EXPANSION CHASSIS INTERRUPT SCHEME.** A simplified block diagram of the interrupt system associated with a fully expanded 990/4 Microcomputer System is shown in figure 3-42. As indicated in this figure, interrupts from each half-board slot in a given expansion chassis are wired to the interrupt jacks J2 and J3 on the backpanel board. These interrupt lines are then jumpered to selected interrupt levels 1 through 15 using wire jumpers on the backpanel board. The 15 interrupt levels are routed to an interrupt scanner on the CRU buffer board which is located in slot 1 of the expansion chassis. If an interrupt is received on any of the 15 interrupt levels, the CRU buffer board issues an interrupt present to the CRU expander board in the main chassis. The CRU expander board then responds to the interrupting chassis (having highest priority) with an ID enable signal. This enable is used to gate the four ID bits (which represent the binary value of the interrupt level) back to the CRU expander board. In response to an interrupt request from any of the seven chassis, the CRU expander board issues either an interrupt A (interrupt present in chassis 1-4), an interrupt B (interrupt present from chassis 5 through 7) or an interrupt C (direct interrupt present from interrupt chassis 1 through 7).

Interrupts A and B are used to activate the expander interrupt servicing routine in the microcomputer which, in turn, addresses the appropriate interrupt servicing section (A or B) with a store CRU instruction addressed to either $F80_{16}$ (interrupt A) or $F90_{16}$ (interrupt B). As a result of the store CRU instruction, a 16-bit interrupt vector is sent back to the microprocessor. As shown in figure 3-43, the interrupt vector contains the ID of the originating unit (developed by the CRU buffer board in the interrupting chassis), the ID of the expansion chassis (developed in the CRU expander board) and the status of the expansion chassis associated with the reporting interrupt section (chassis 1-4 associated with interrupt section,A and chassis 5-7 associated with section B). The interrupt vector is then used to select the proper device interrupt servicing routine associated with the interrupting board.

If a direct interrupt (INT C–) is generated, the interrupt is processed more speedily since the expansion interrupt servicing routine is bypassed and the microprocessor traps directly to the board-level interrupt servicing routine. This interrupt scheme is used when peripherals requiring rapid response to interrupts are located in the expansion system.

3.6.2 **CRU EXPANSION ADDRESS SCHEME.** A CRU address map for the standard fully expanded 990/4 System is shown in figure 3-22. As indicated in this figure, each chassis is assigned a band of location-dependent CRU addresses which are used to address the CRU interface boards implemented within a given chassis. The chassis number (1 to 7) which is assigned to each chassis is determined by an ID plug on the CRU buffer board.

3.6.3 **CRU EXPANSION BOARDS.** The CRU expansion system requires two board types including the CRU expander board and the CRU buffer board. These two boards are briefly described in the following paragraphs.

3.6.3.1 **CRU Expander Board.** The CRU expander board, Part Number 945005-1, basically expands the CRU interface present at the main chassis backpanel to drive up to seven expansion chassis. The board is equipped with buffer/drivers for fanout of data and control lines and contains interrupt processing logic to report interrupts to the microprocessor.

A functional block diagram of the CRU expander board, complete with interface pin numbers, is shown in figure 3-44. As indicated in this diagram, the CRU expander consists of two major sections including:

- CRU Fanout Logic
- Interrupt Recognition Logic

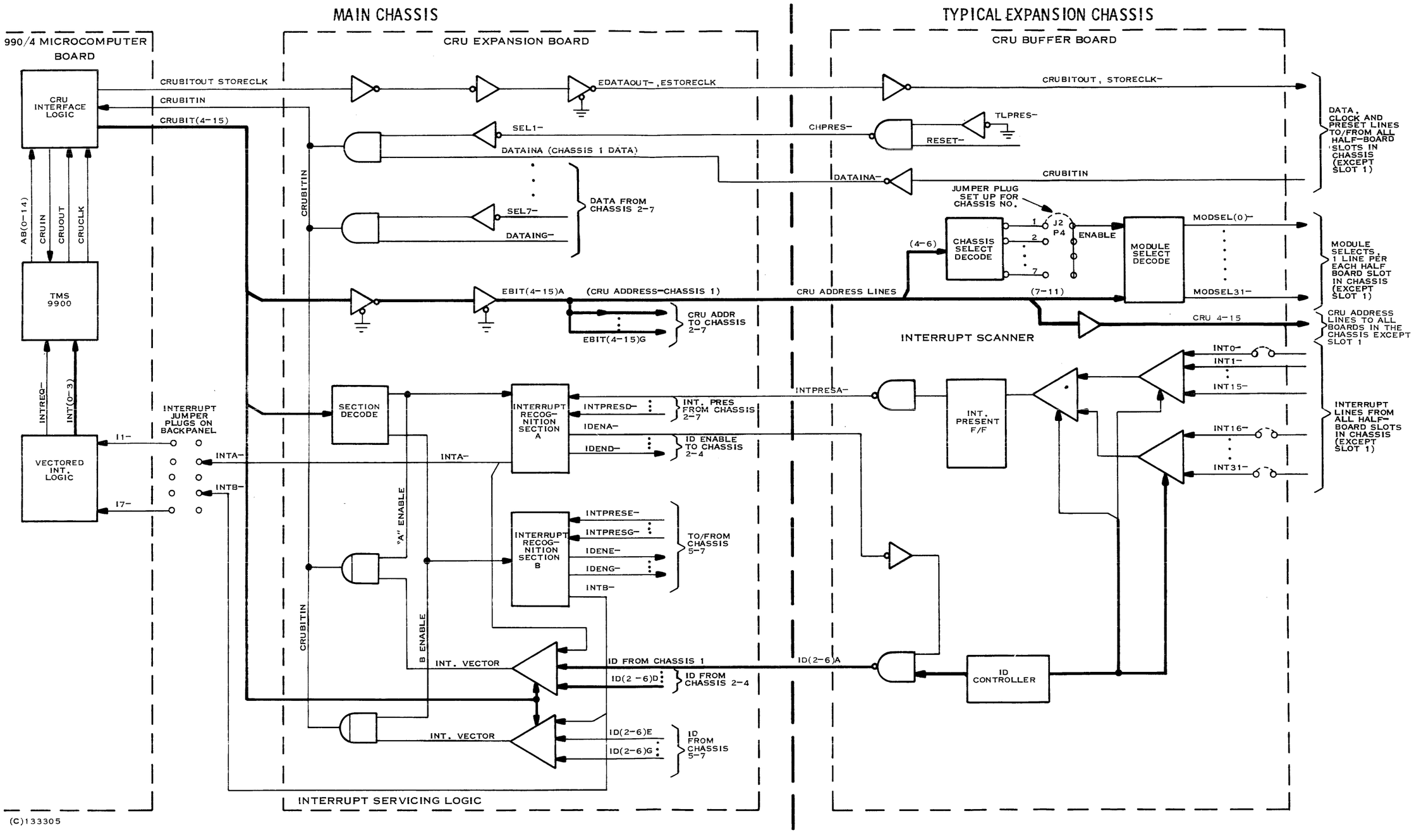


Figure 3-42. CRU Expansion System, Functional Diagram

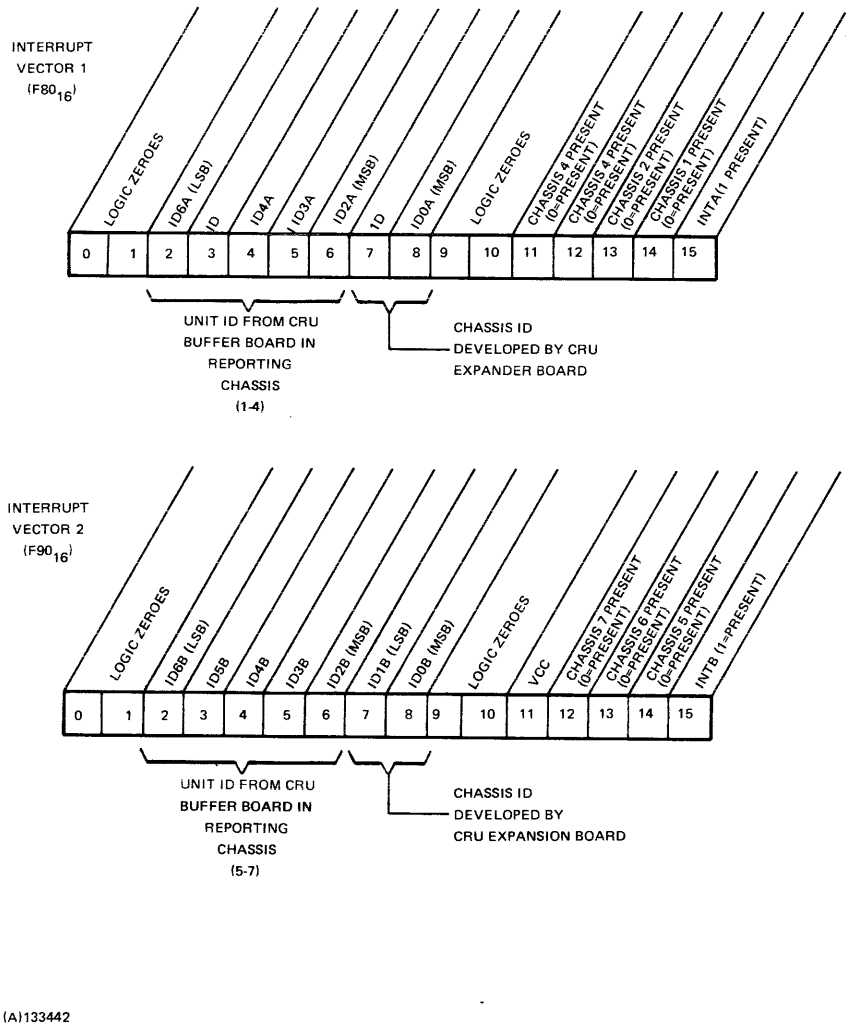


Figure 3-43. Expansion Interrupt Vector Format

CRU Fanout Logic. The CRU expansion board provides a 1 by 7 fanout of the following CRU interface signals:

- TLIORES– (or TLPRES– using jumper option)
- CRUBITOUT
- CRUBIT (4-15)
- STORECLK–

Each of these signals, with the exception of STORECLK–, is buffered and series terminated. STORECLK– is driven by a power gate which requires parallel termination in the CRU buffer board in the receiving chassis.

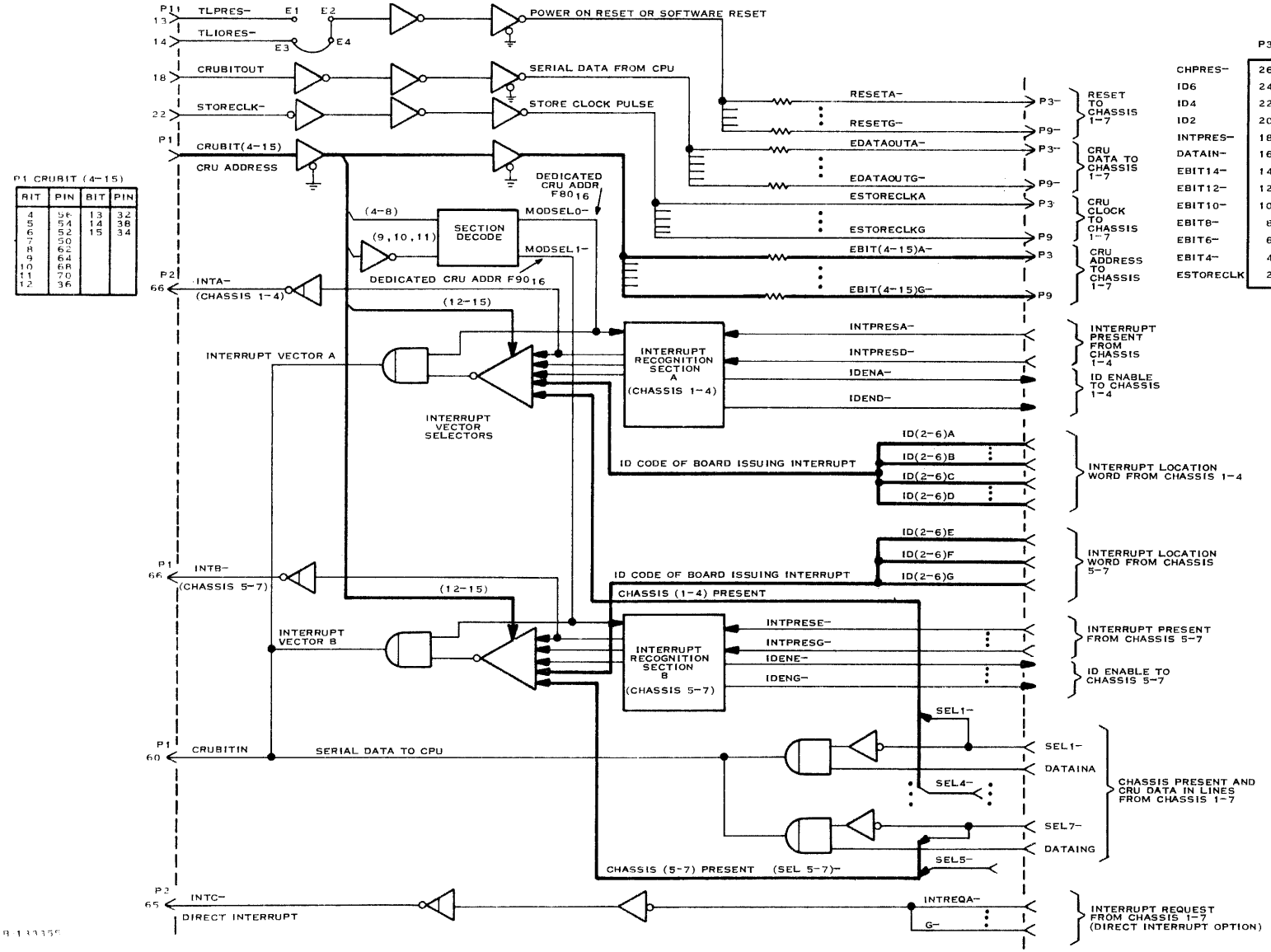


Figure 3-44. CRU Expander Board Block Diagram

Interrupt Recognition Logic. The interrupt recognition logic on the CRU expansion board is functionally divided into two sections, A and B. Section A monitors the interrupt lines from chassis 1-4 and reports interrupts to the computer over the INTA– line. Section B monitors the interrupts from expansion chassis 5-7 and reports interrupts over the INTB– line.

The interrupt request lines (INTREQ–) from all chassis are wire-ORed together, buffered and sent to the computer as INTC–. The direct interrupt feature is used when faster interrupt processing response time is required by a peripheral in an external chassis.

When an interrupt present (INTPRES–) is detected by one of the two interrupt recognition sections, it develops a 2-bit binary word (ID(0,1)) which corresponds to the highest priority interrupt present. This binary word is decoded to send a logic-low ID enable signal (IDEN–) to the selected requesting chassis. The ID enable is a request for the external chassis's CRU buffer board to send back the ID word (ID(2-6)) which identifies the board in the external chassis that initiated the interrupt.

In a similar fashion, Section B of the interrupt recognition logic monitors and processes the interrupts from chassis 5 through 7. Provisions are incorporated on the board to permit software to address either the A or B interrupt section via an STCR addressed to either $F80_{16}$ (section A) or $F90_{16}$ (section B). Then by manipulating the CRU address lines 12-15, software is able to serially transfer a full 16-bit interrupt vector from either interrupt section to computer memory via the CRUBITIN data line. The interrupt vector format is shown in figure 3-43.

Note that the vector includes the encoded binary word (ID(0,1)) developed by the interrupt sections, the ID word returned from the external chassis and the chassis present (SEL–) lines from each expansion chassis (if a chassis is connected, its associated SEL– line will be a logic 0 level).

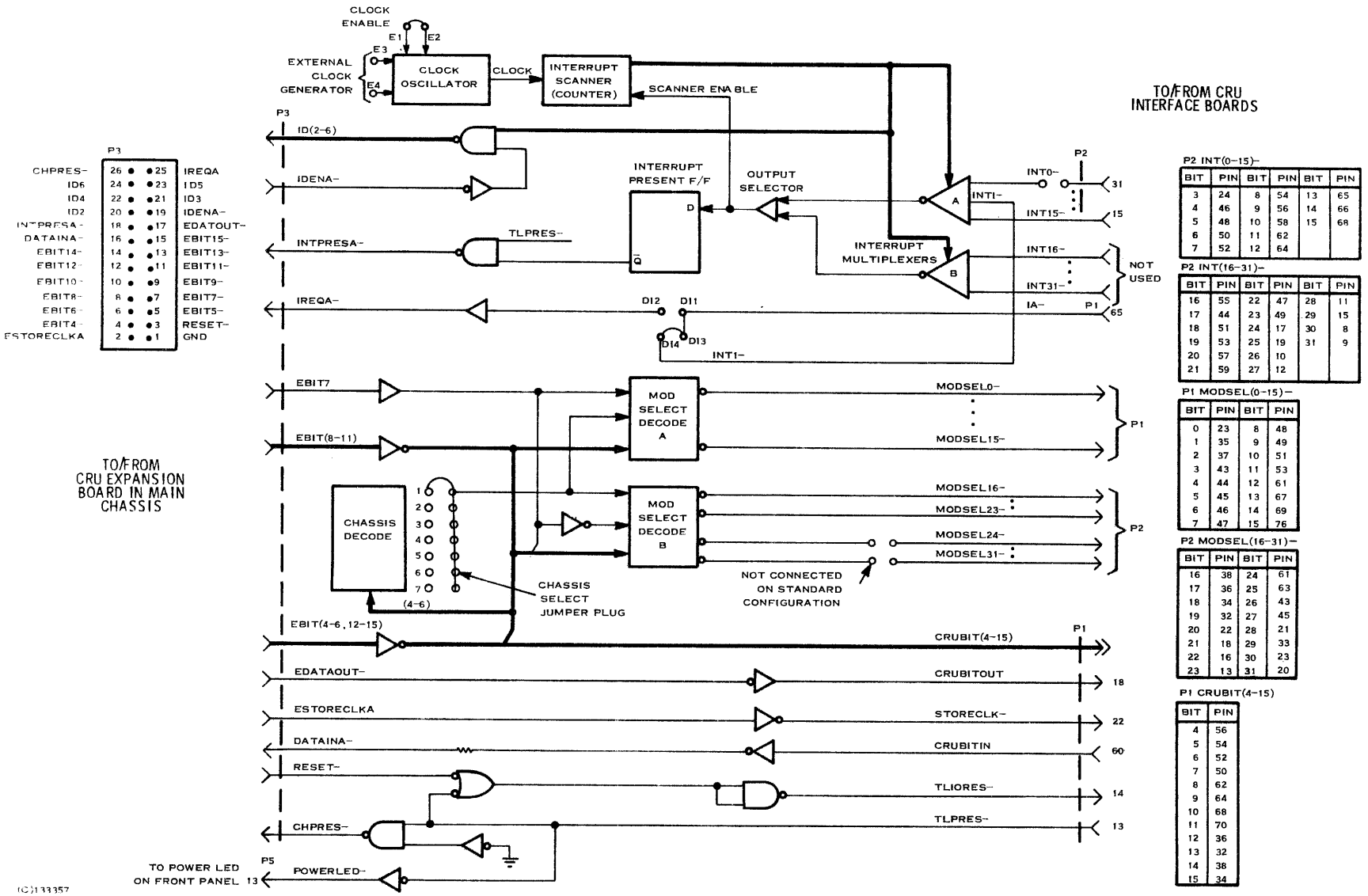
3.6.3.2 CRU Buffer Board. Each expansion chassis is equipped with a CRU buffer board in slot 1. Basically, the CRU buffer board performs a module select decode and CRU fanout/fanin function similar to that performed by the CRU interface logic on the 990/4 Microcomputer board. The buffer board decodes CRU address lines from the 990/4 chassis (via the 990 CRU expansion board) to generate the low-active Module Select signals for the CRU interface boards within the expansion chassis.

The board also buffers the CRUDATAOUT, CRUSTORECLK, TLIORES– and CRUBITOUT lines between the main chassis and all CRU slots in the expnasion chassis.

An interrupt scanner circuit on the buffer board (figure 3-45) continuously monitors for the presence of interrupts from any of the CRU buffer boards in the chassis and issues an Interrupt Present (INTPRES–) if an interrupt is detected on any line. The buffer board then enables the ID word (ID(2-6)) which identifies which board in the expansion chassis issued the interrupt when ID Enable signal (IDENA) is received from the CRU expansion board.

Interrupt Scanner Logic. The CRU buffer board contains provisions for encoding up to 32 interrupts onto a single interrupt line to the CRU expander board and supplying the expander board, on request, the ID of the board which originated the interrupt. However, in the present 13-slot chassis, only the first 15 interrupt lines (INT(1-15)–) are actually connected to the scanner circuitry.

The interrupt scanner consists of a clock oscillator stage (U21, U10 plus R1 and C1), a 5-bit counter (U11 and U12), two 16-bit multiplexer stages U1 and U2, a multiplexer selector U17, interrupt present flip-flop stage U22, and output driver stage U15.



P2 INT(0-15)-

BIT	PIN	BIT	PIN	BIT	PIN
3	24	8	54	13	65
4	46	9	56	14	66
5	48	10	58	15	68
6	50	11	62		
7	52	12	64		

P2 INT(16-31)-

BIT	PIN	BIT	PIN	BIT	PIN
16	55	22	47	28	11
17	44	23	49	29	15
18	51	24	17	30	8
19	53	25	19	31	9
20	57	26	10		
21	59	27	12		

P1 MODSEL(0-15)-

BIT	PIN	BIT	PIN
0	23	8	48
1	35	9	49
2	37	10	51
3	43	11	53
4	44	12	61
5	45	13	67
6	46	14	69
7	47	15	76

P2 MODSEL(16-31)-

BIT	PIN	BIT	PIN
16	38	24	61
17	36	25	63
18	34	26	43
19	32	27	45
20	22	28	21
21	18	29	33
22	16	30	23
23	13	31	20

P1 CRUBIT(4-15)

BIT	PIN
4	56
5	54
6	52
7	50
8	62
9	64
10	68
11	70
12	36
13	32
14	38
15	34

Figure 3-45. CRU Expander Board Block Diagram

The scanner oscillator, which is enabled when jumper E1 is connected to E2, develops a 250-nanosecond pulse train used to advance the 5-stage scan counter. The four least significant counter outputs (U11, pins 14, 13, 12 and 11) are used to address the two interrupt multiplexer stages U1 and U2. The most significant counter output bit (and its complement) is used to control the multiplexer selector stage U17. The output of the selector is also routed back to the counter inputs which permit the counter to be inhibited when an interrupt is detected by either of the multiplexers.

The output of the multiplexer selector stage U17 (INTPRES–) is clocked into the interrupt present flip-flop stage U22 and routed to the CRU expansion board in the main chassis.

When the ID enable is received from the expansion board, the outputs from all five stages of the scan counter are sent to the CRU expansion board for use by software in constructing the interrupt vector which identifies which chassis and which board slot issued the interrupt.

The interrupt logic on the CRU buffer board also includes an option to bypass the scanner for interrupt 1 (IA–). In this case, the interrupt is wired to the interrupt request gate U15 and used to generate a low-active IREQA– signal. This signal is wire-ORed on the CRU expansion board with the IREQ– signals from all seven CRU buffer boards. The direct interrupt option is used when a peripheral requiring more rapid interrupt processing time is implemented in an expansion chassis.

The interrupt scanner section also contains provisions for disabling the internal interrupt scanner clock and using an external pulse generator to advance the counter. Provisions are also included for clearing the counter manually. The jumper connections associated with the maintenance options are described in Section II of this manual.

Module Select Decoding. The module select decode function performed by the CRU buffer board is similar to the function provided in the main chassis by the 990/4 Microcomputer board. To set up the chassis address to correspond to the CRU expansion board connector (which may be connected to any connector from P3 to P9), a single jumper wire is installed on the 14-pin socket P4. Then if the incoming CRU address lines (EBIT4-11) indicate an address within the chassis address space, one of the 24 module select lines (MODSEL(0-23)–) goes low. This signal is routed to the appropriate CRU board slot via the chassis backpanel board.

The CRU buffer board has provisions for decoding up to 32 module selects but the option is not wired up on the conventional system.

CRU Buffer Options. The following jumper options are available on the CRU buffer board:

- Option to wire interrupt level 1 either directly to the CRU expansion board in the main chassis or through the interrupt scanner. If J1, pins 1 and 2 are connected, the interrupt is sent directly; if J1, pins 3 and 4 are connected, the interrupt uses the scanner circuitry (normal configuration).

- Module select decodes 24 through 31 – Jumpers are installed between appropriate P2 pins (see logic diagram 944907, sheet 2) and M 24-31 (see figure 2-25).

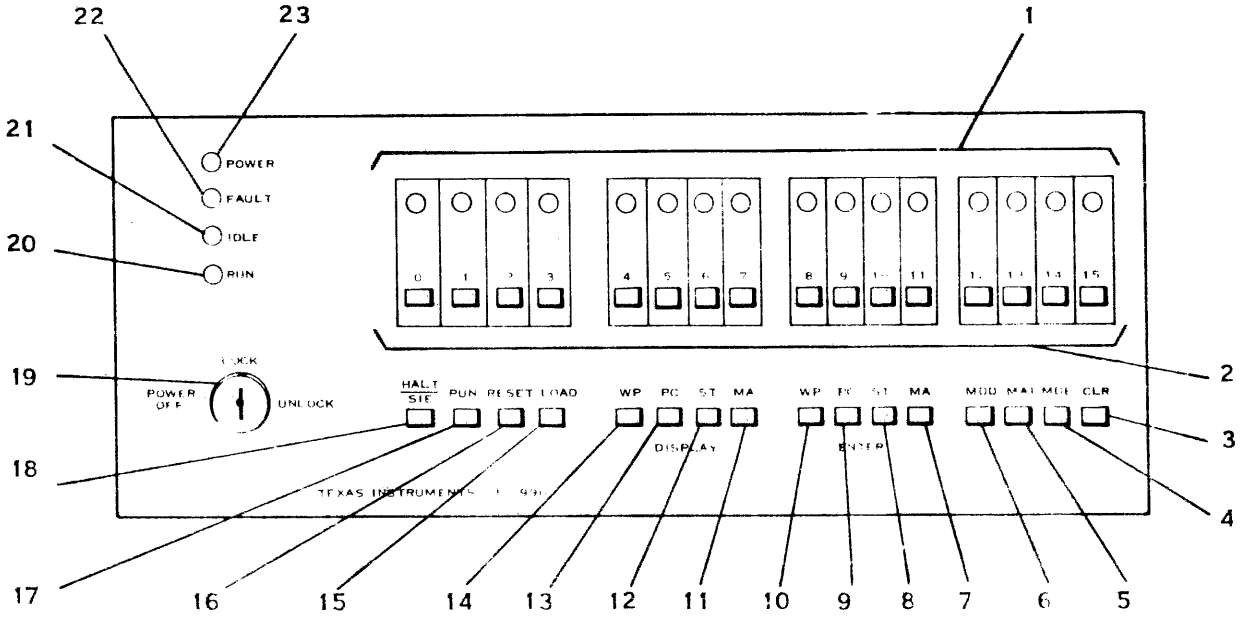
- Chassis select – A single jumper is installed on the 14 pin socket P4 as follows:

Expander Connector	Jumper Pins on P4	Chassis Number
P3	1, 14	1
P4	2, 13	2
P5	3, 12	3
P6	4, 11	4
P7	5, 10	5
P8	6, 9	6
P9	7, 8	7

3.7 PROGRAMMER PANEL

The 990 programmer panel operates as a CRU device with the Model 990/4 Computer. The programmer panel contains logic, switches and indicators that provide for manual control and operator observation of the operation of the computer. The switches are used for data entry and, along with light emitting diodes (LEDs), provide for display of data at the panel. Logic for the programmer panel is contained on a printed circuit board installed just to the rear of the panel. Interface signals between the programmer panel and the 990/4 Microcomputer circuit board are routed through a 20-conductor cable that leads from the programmer panel to a connector plug P3 at the top edge of the 990/4 Microcomputer circuit board. The panel can be installed on the front of either the 6-slot or 13-slot chassis. A 5-inch filler panel adapts the programmer panel for use with the 13-slot chassis.

3.7.1 PROGRAMMER PANEL CONTROLS AND INDICATORS. The programmer panel controls and indicators are shown in figure 3-46 which is keyed to table 3-8.



(A)133607

Figure 3-46. 990 Programmer Panel Controls and Indicators

Table 3-8. Programmer Panel Controls and Indicators

Reference Number	Control or Indicator	Function
1	DATA LEDs	In the RUN mode of operation, all DATA LEDs light except when the computer halts. At this point, the contents of the CPU's program counter is displayed. A lit LED denotes a logic 1, an extinguished indicator denotes logic 0. The LSB is displayed on the far right of the LEDs. In the HALT mode, the LEDs display a computer register contents, memory contents or a value entered into computer memory via the data entry switches depending on which switches are pressed (see reference 5, 7, 9, 11, 13, 15).
2	DATA entry switches	Used in conjunction with the ENTRY switches on the panel to enter data and addresses into selected computer registers and memory locations (active only when the panel is in the HALT mode of operation). In the HALT mode, the data LED located immediately above each data entry switch lights as each switch is pressed. The value indicated by the DATA LEDs is then stored in the register or memory address selected by the entry switches.
3	CLR switch	When pressed, this switch clears the DATA LED displays.
4	MDE switch	This switch is pressed to transfer a value displayed on the DATA LEDs to the memory location defined by the contents of the memory address (MA) register in the computer.
5	MAI switch	The memory address increment (MAI) switch is pressed to increment the value stored in the CPU's memory address register by a value of 2.
6	MDD switch	When pressed, this switch causes the contents of the memory location defined by the contents of the memory address register to be displayed on the DATA DISPLAY LEDs.
7	ENTER MA switch	When pressed, this switch causes the value displayed by the DATA LEDs to be entered into the computer's memory address register.
8	ENTER ST switch	When pressed, the value displayed on the DATA LEDs is entered into the computer's status register.
9	ENTER PC	When pressed, the value displayed on the DATA LEDs is loaded into the computer's program counter.
10	ENTER WP	When pressed, the value displayed on the DATA LEDs is loaded into the computer's workspace pointer register.
11	DISPLAY MA	When pressed, the value stored in the computer's memory address register is displayed on the DATA LEDs.
12	DISPLAY ST	When pressed, the contents of the computer's status register is displayed on the DATA LEDs.
13	DISPLAY PC	When pressed, the contents of the computer's program counter is displayed on the DATA LEDs.
14	DISPLAY WP	When pressed, the contents of the computer's workspace pointer register is displayed on the DATA LEDs.

Table 3-8. Programmer Panel Controls and Indicators (Continued)

Reference Number	Control or Indicator	Function
15	LOAD switch	When the panel is in the HALT mode, pressing this switch causes the computer to trap to the ROM loader starting address.
16	RESET switch	Pressing the RST switch results in an IORESET– pulse being generated which resets all units in the system.
17	RUN switch	When the computer is halted (programmer panel is active), pressing the RUN switch returns the computer to the RUN mode of operation and deactivates the panel.
18	HALT/SIE switch	When the computer is in the RUN mode (RUN LED is lit), pressing the HALT/SIE switch causes the computer to halt and begin processing the front panel software if the key switch is set to the UNLOCK position. Pressing the switch when the computer is not in the RUN mode causes the computer to execute a single instruction at the present PC (program counter) address. The contents of the program counter are incremented by two and displayed on the DATA LEDs.
19	Key switch	The key switch (OFF/LOCK/UNLOCK) switch prevents unauthorized computer turnon or program intervention. In order to apply ac power to the chassis, the key must be inserted into the switch and the switch set to the LOCK position. At this point, power is applied to the computer, but the programmer panel is locked out. In the UNLOCK position, the computer may be halted by pressing the HALT/SIE switch. The key may be removed from the switch in either the OFF or LOCK position.
20	RUN LED	The RUN LED lights when a low-active RUN– signal is generated by the computer indicating the computer is in the RUN mode. When this LED is lit, all switches on the panel except the HALT/SIE switch are disabled and the DATA LEDs are driven under program control. When the RUN LED is extinguished, the panel controls are active.
21	IDLE LED	Lights when the computer is executing an idle instruction (indication of computer inactivity for most interrupt driven software).
22	FAULT LED	The FAULT LED lights when the computer has detected a diagnostic test failure. The LED is extinguished by executing a RSET instruction or an SBO or SBZ addressed to panel bit 11.
23	POWER LED	Lights when power is applied to the unit (key switch on the panel set to the LOCK or UNLOCK position).

3.7.2 **PROGRAMMER PANEL MODES OF OPERATION.** The programmer panel may function in one of two modes including:

- Run Mode
- Halt Mode

Run Mode. In the Run mode of operation (RUN LED lit), all programmer controls are inoperative except for the HALT/SIE switch which may be enabled by setting the key switch to the UNLOCK position. If the key switch is in the LOCK position, all panel controls are disabled.

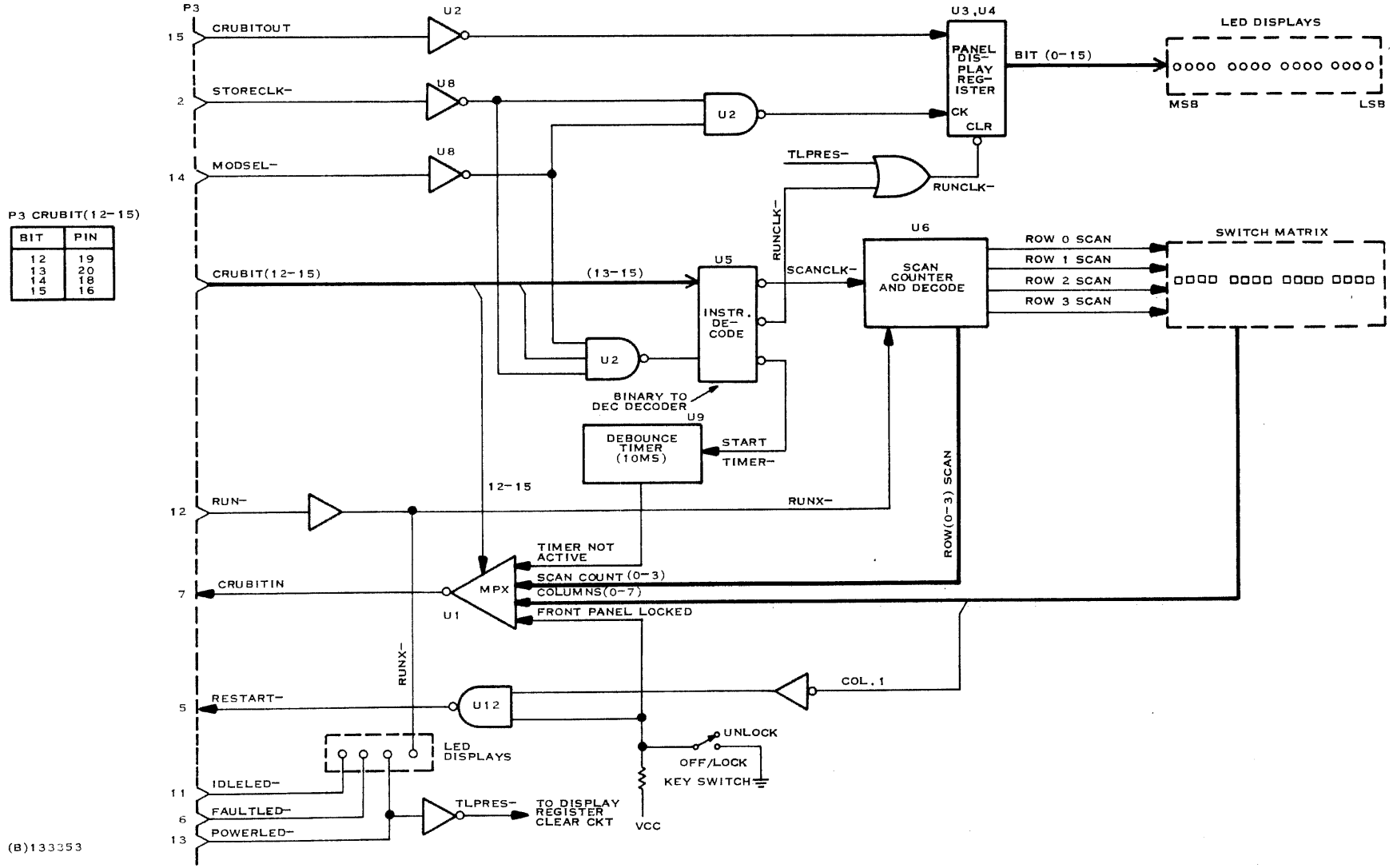
Halt Mode. If the key is inserted into the key switch and rotated to the UNLOCK position, the HALT/SIE switch is enabled. At this time, a Restart signal can be issued to the 990/4 Microcomputer board if the HALT/SIE switch is pressed. The Restart signal causes the microcomputer to trap to location FFFC in ROM and begin executing the panel software. As a result, the microprocessor is taken out of the Run mode and the RUN LED on the programmer panel is extinguished. At this time, the scan counter on the programmer panel logic board is advanced under software control and the programmer panel switch outputs are monitored by software (see figure 3-47).

If an indication is received that one of the panel switches has been pressed, the software utility activates a 10-millisecond debounce timer on the programmer panel board via an SBO or SBZ instruction addressed to bit 8 (CRUBIT12-15 encoded with 8_{16}). The resulting START TIMER– signal activates a debounce timer. Since the output of the timer is also routed to the CRUBITIN line via the multiplexer, software can determine when 10 milliseconds have elapsed. At this time, the software monitors the column containing the pressed key to ensure that the key is still pressed (see figure 3-48). If so, the software determines whether the key is a data key or function key. If it is a function key, panel software branches to the appropriate instruction in the program which executes the specified function. If it is a data key, the data bit is complemented (if previously a 1, changed to a zero and vise versa). The complemented bit is also stored in the data display register on the programmer panel board and applied to the corresponding DATA LED. A logic 1 is indicated by a lighted LED, and a logic 0 is indicated by an extinguished LED.

3.7.3 **INTERFACE SIGNALS.** Figure 3-49 shows the interface connections between the programmer panel and the programmer panel interface of the computer. The function of each interface line is described in table 3-9.

3.7.4 **PROGRAMMER PANEL ADDRESSING.** The programmer panel as a CRU interface device has 16 directly addressable input bits and 16 directly addressable output bits. Input and output operations can address each of the bits individually or in fields of from 1 to 16 bits. The computer instructions that drive the CRU interface can set, reset or test any bit and can move data between memory and the programmer panel.

3.7.4.1 **Address Format.** The 12-bit CRU address format with field assignments used by the computer is as shown in figure 3-27. The module select bits are decoded internally by the computer to generate a Module Select (MODSEL–) signal to address the programmer panel. The bit select field (CRUBIT 12-15) is the only portion of the CRU address that the programmer panel uses. When enabled by the hard-wired MODSEL– line, the programmer panel must decode the bit select field to determine which of its bits is affected by the operation.



P3 CRUBIT(12-15)

BIT	PIN
12	19
13	20
14	18
15	16

Figure 3-47. Programmer Panel Functional Block Diagram

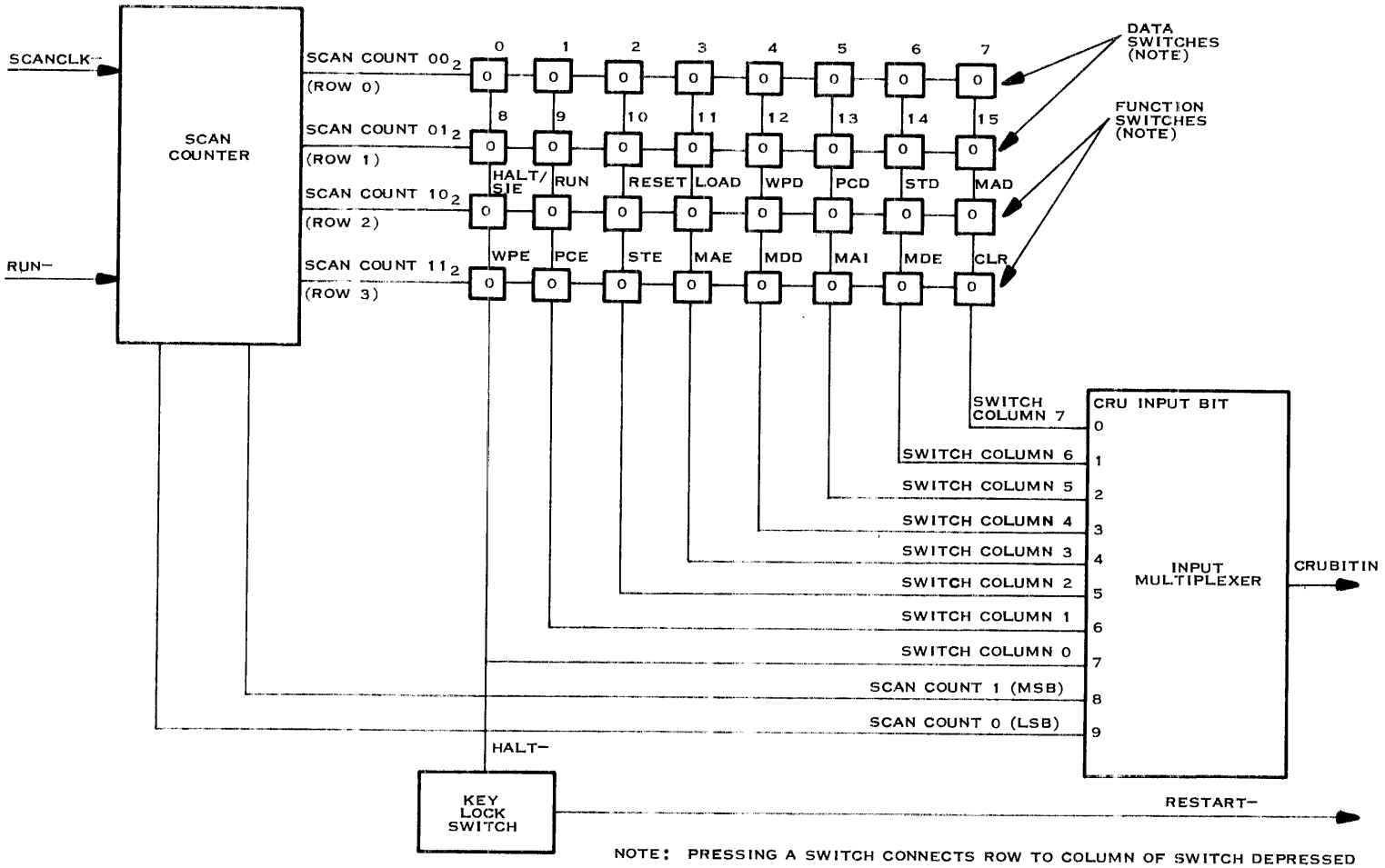


Figure 3-48. Switch Scanner Block Diagram

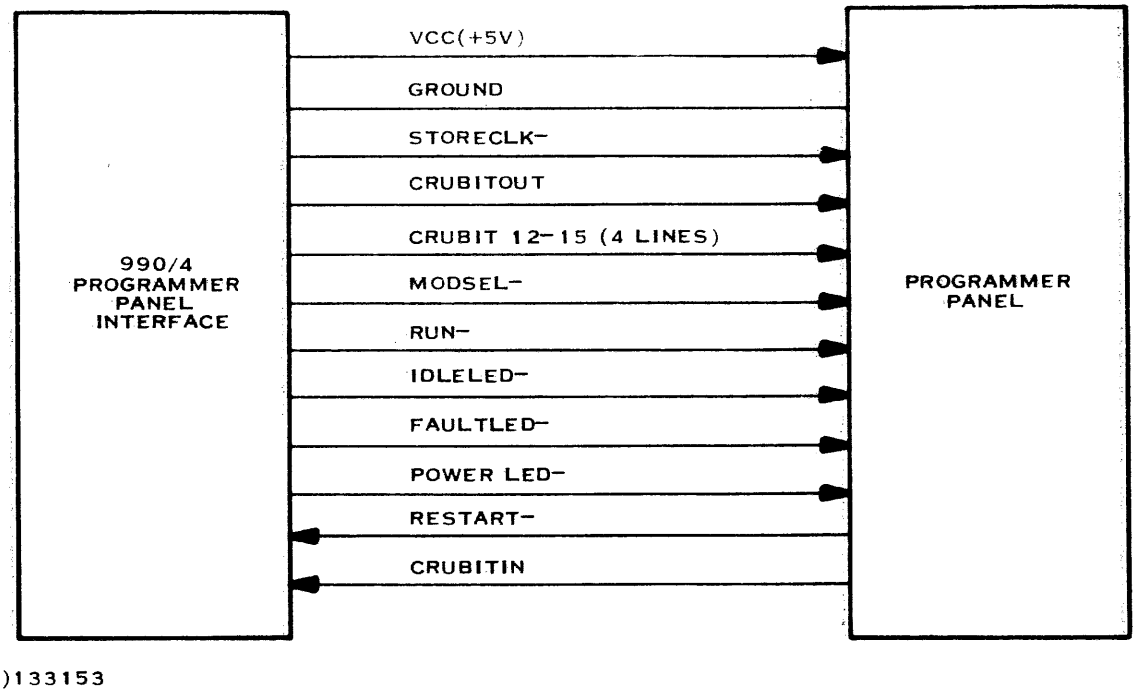


Figure 3-49. Programmer Panel Interface Diagram

3.7.4.2 **Bit Address Development.** The computer develops a CRU bit address from the CRU base address contained in workspace register 12 added to the signed displacement contained in bits 8 through 15 of the three single-bit CRU instructions: Test Bit (TB), Set Bit to One (SBO) and Set Bit to Zero (SBZ). The CRU base address loaded into workspace register 12 for the programmer panel is hexadecimal 1FE0. Individual CRU input bit address assignments for the programmer panel are as shown in table 3-10. The CRU output bit address assignments are provided in table 3-11.

3.7.5 **THEORY OF OPERATION.** The programmer panel operates in either the RUN mode or the HALT mode. The description that follows discusses each mode of operation separately and is based on the block diagram for the programmer panel as shown in figure 3-47.

3.7.5.1 **RUN Mode.** As the computer powers up in preparation to carry out its task of normal processing, the POWER LED– interface signal between the computer circuit board and the programmer panel goes low and is applied to a complementary output element on the panel. The low output from the element lights the POWER lamp on the panel, and the complementary output from the element, TLPRES–, goes high to remove the CLEAR signal from the data display register thus enabling the data display register for data entry. TLPRES has been low during computer power-down condition to hold the 16 data display lamps on the panel to logic ONE's (illuminated). The level 0 power-up interrupt is taken by the computer and the computer comes up in its RUN mode of operation. An SBO instruction addresses CRU output bit 10 of the panel causing the RUN– interface signal from the computer circuit to go low. Additionally, the strobe decoder is addressed and a low RUNCLK– is generated by the strobe decoder during one STORECLK period. The low RUNCLK clears the data display register and the 16 data display lamps light. The low RUN– interface signal lights the RUN lamp on the programmer panel and also is applied to the two flip-flops of the scan counter to hold the scan counter to a 10_2 scan count. This scan count holds one side of the row 2 switches (left-side function switches

Table 3-9. Programmer Panel Interface Connections

INTERFACE LINE	FUNCTION
Vcc (+5 volts)	Power for programmer panel furnished by computer power supply.
Ground	System ground.
STORECLK-	A low clock pulse that indicates to the programmer panel that the operation is a write operation. The pulse transfers the data on the CRUBITOUT line into the 16-bit parallel-out serial shift data display register of the programmer panel.
CRUBITOUT	Serial data line for transfer of data from the CPU to the addressed CRU bit(s) of the programmer panel. This line is active only when STORECLK- goes low.
CRUBIT 12 through 15	During a read operation, CRUBIT 12 through 15 applied to the input multiplexer of the programmer panel select a particular bit for input to the CPU. During a write operation, CRUBIT 12 through 15 applied to the strobe decoder of the programmer panel generate the SCANCLK-, RUNCLK-, and START TIMER strobes.
MODSEL-	Module select signal. When MODSEL- is low, the programmer panel has been selected by the computer as the addressed module.
RUN-	A low active signal generated by the computer when in the RUN mode. The low signal through a series resistor illuminates the RUN LED on the programmer panel. The low is also applied to the scan counter that in turn holds one side of the HALT/SIE switch low. Pressing the HALT/SIE switch transfers the low through the POWER OFF, UNLOCK, LOCK key switch (when in the UNLOCK position) to generate a low RESTART- signal to the computer.
IDLELED-	A low signal generated by the computer when in the IDLE mode. The low signal, through a series resistor, illuminates the IDLE LED on the panel.
FAULTLED-	A low signal generated by the computer that through a series resistor, illuminates the FAULT LED on the panel to indicate the result of a CPU test.
POWERLED-	A low signal generated by the computer that, through a series resistor, illuminates the POWER LED on the panel to indicate that the system power supply is on.
RESTART-	A low signal generated by pressing the panel HALT/SIE switch when the key switch is in the UNLOCK position. The low causes the CPU to stop processing and to start executing panel software.
CRUBITIN	Serial data line for transfer of data from the addressed CRU bit(s) at the input multiplexer of the programmer panel to the CPU.

as viewed from front panel and refer to figure 3-48) low. All switches on the panel with the exception of the HALT/SIE switch are inhibited and the panel is inactive while in the RUN mode. However, the data display register and data display lamps may be used by the computer to display program data by issuing LDCR instructions. Pressing the HALT/SIE switch while the computer is in the RUN mode causes the computer to stop processing and to execute programmer panel software. When activated, the HALT/SIE switch transfers the low at the row 2

Table 3-10. Programmer Panel CRU Input Bit Assignments

BIT	DESCRIPTION	FUNCTION
0	Switch column 7	CRU input bits 0 through 7 are assigned to switch columns 7 through 0 respectively. An 8-bit Store Communications Register (STCR) instruction from the computer stores the value of a row of eight switches as defined by the scan counter. A switch that has been depressed and has stopped bouncing is stored into memory as a logic ONE.
1	Switch column 6	
2	Switch column 5	
3	Switch column 4	
4	Switch column 3	
5	Switch column 2	
6	Switch column 1	
7	Switch column 0	
8	Scan Count 1	A logic ONE on CRU input bit 8 indicates that the scan counter is in the function (row 2 or row 3) group of switches.
9	Scan Count 0	A logic ONE on CRU input bit 9 indicates that the scan counter is in the least significant byte (row 1 or row 3) of either the data or the function group of switches.
10	Timer Active	A logic ONE on CRU input bit 10 indicates that the debounce timer has finished timing out.
11	Front Panel Not Present Or Locked	A logic ONE on CRU input bit 11 indicates that the panel is not connected to the computer or that the programmer panel key switch is in the LOCK position.
12 and 13	Not Used	
14	Maintenance Unit Not Present	A logic ZERO on CRU input bit 14 indicates that the 990 maintenance unit is connected to the computer rather than the standard programmer panel.
15	Not Used	

scan side of the switch through the key lock switch (in UNLOCK position) as a low RESTART– interface signal to the computer circuit board to cause the RUN– interface signal to the panel to go high. The RUN lamp is extinguished and the hold on the scan counter is relinquished so that it may respond to the SCANCLK– signal generated by the strobe decoder while the panel is in the HALT mode. The RESTART– interface signal also causes a trap through $FFFC_{16}$ and the computer begins to execute programmer panel software making the panel switches and lights active in the HALT mode of operation.

3.7.5.2 **HALT Mode.** As previously described, when the HALT/SIE switch is pressed while the panel is in the RUN mode the low RESTART- interface signal to the computer circuit board causes the RUN-interface signal to go high to extinguish the RUN lamp on the panel and release the hold on the scan counter. The computer performs the RESTART- trap and the two-word vector at memory address $FFFC_{16}$ is loaded into the workspace pointer register (first vector word) and program counter register (second vector word) to define the workspace and program starting point and the software for the programmer panel initializes and begins to execute. A test is made to see if the user has initiated an SIE instruction. If yes, the SIE register is cleared, the programmer panel is enabled and a branch is made to the user's program. If no SIE instruction has been initiated, a test is made of the Front Panel Present bit, CRU input bit 11. If the test shows the programmer panel is not present, the program jumps to a loader

Table 3-11. Programmer Panel CRU Output Bit Assignments

BIT	DESCRIPTION	FUNCTION
0 through 7	Data Display Lamps 0 through 15	A 16-bit word is transferred to the lamps for display by executing two 8-bit Load Communication Register (LDCR) instructions on the word to be displayed in a most significant byte, least significant byte order.
8	Increment scan	A Set Bit to ONE (SBO) or SBZ instruction addressed to CRU output bit 8 increments the scan counter. For example, if the scan counter is at count 11_2 then it will increment to count 00_2 after execution of the SBO. The scan counter is set to 10_2 when the RUN bit is set.
9	Not Used	CRU output bit 9 not used in the programmer panel.
10	Run	An SBO instruction addressed to CRU output bit 10 illuminates the RUN LED, sets the DATA LEDs to logic ONEs, sets the scan counter to 10_2, and enables the interrupt. The foregoing actions are effected by programmer panel ROM software when the RUN switch is pressed while in the HALT mode. Following a power-up, the RUN bit is set to a logic ONE.
11	Fault	The FAULT output bit is connected to an LED on both the programmer panel and the computer. A logic ONE to output bit 11 illuminates both LEDs. A zero clears both LEDs.
12	Clear internal interrupts	An SBO or SBZ instruction addressed to CRU output bit 12 clears the error interrupt flag in the computer. This action is performed by the CPU and is not a function of the programmer panel.
13	Start Timer	An SBO or SBZ instruction addressed to CRU output bit 13 starts the debounce timer. CRU input bit 10 monitors the timer output.
14	Single Instruction Execute (SIE)	An SBO or SBZ instruction addressed to CRU output bit 14 enables the computer to execute two more instructions before trapping to the programmer panel ROM. By addressing this bit and following with an RTWP, panel software can perform the SIE function. This action is performed by the CPU and is not a function of the panel.
15	Not Used	CRU output bit 15 not used in the programmer panel.

function. If the panel is present, the program displays the contents of the program counter at the panel data display lamps and the program moves to a main scan loop to determine if any panel switch is depressed.

As shown in the block diagram for the switch scanner, figure 3-48, the 32 data and function switches are part of a 4-row by 8-column matrix. As previously described, when the programmer panel is in the RUN mode the low RUN- signal input to the scan counter holds the scan count output of the scan counter at 10_2 and row 2 is held low. The HALT/SIE switch in row 2 is active and when pressed generates the low RESTART- signal through the unlocked key lock switch. In the HALT mode, the scan counter is incremented by the SCANCLK- signal through its binary count, 00_2 through 11_2, and rows 0 through 3 are brought low in turn. Pressing a switch transfers the low output of the scan counter to the input of the input multiplexer at the CRU input bit position that corresponds to the switch column of that switch. Though the switch column position can be determined simply by detecting CRU input bit position, the row position of the pressed switch also needs to be ascertained. To check the condition of the switches, the computer issues a byte-length STCR instruction to the programmer panel. Data switches in row 0 and function switches in row 2 are treated by software as the least significant byte of a two-byte word and the data switches in row 1 and the function switches in row 3 are handled as the most significant byte of the 16-bit word. By checking the scan count inputs to the input multiplexer at CRU input bit positions 8 and 9 a determination is made as to which row a pressed key is located. First, CRU input bit 9 (SCAN COUNT 0-) is tested to determine whether the least significant byte (rows 0 and 2) or the most significant byte (rows 1 and 3) is the location of the pressed key. If the location is determined to be in the most significant byte position the software executes SWPB instruction to reposition the CRU input bits as stored in computer memory so that they will be representative of either row 1 or row 3. A test is then made of CRU input bit 8 (SCAN COUNT 1-) to determine whether the pressed key is data switch (rows 0 and 1) or a function switch (rows 2 and 3).

In the main scan loop, the programmer panel is exercised as follows. CRU output bit 13 is addressed to start the debounce timer. After approximately 3 milliseconds delay and with the debounce timer no longer active, a read instruction is issued to see if a switch is depressed in that row of switches held low by the scan counter. If no switch is depressed this action is repeated two more times and then CRU output bit 8 is addressed to increment the scan counter to check the next row of switches three times. This scanning continues until a depressed key is detected. When a depressed key is detected, two more delayed passes are made using the debounce timer to ensure that the key is really depressed and is not noise. When the decision is made that the key is depressed, the test of CRU input bit 9 is made to see if the switch is represented by the least significant byte or the most significant byte of the word. If it is the most significant byte then the swap byte position instruction is issued. A test is then made of CRU input bit 8 to see if the switch is a data switch or a function switch. If it is a data switch, an exclusive OR instruction is issued which has the effect of changing the data in the data display register and the data display lamp that corresponds to the data switch depressed. If a function switch is depressed, an index table is set up in a workspace register to cause a jump to the instruction in the program that corresponds to the function required of the switch. The programmer panel stays in the HALT mode until the RUN function switch is depressed.

3.8 20-AMPERE POWER SYSTEM

The 20-ampere power system is used to furnish dc power for the 6-slot chassis and for a low-power consumption configuration of the 13-slot chassis. The 20-ampere power system is part of the chassis assembly, unit 1, and consists of input line filter 1FL1, ac power converter 1A2, filter capacitor 1C1, and 20-ampere power supply 1A3. An optional transformer 1T1 is required when the ac input voltage is not 115 volts ac. Also available as an optional addition to the 20-ampere power system is the standby power supply kit. The standby power supply, 1A6, provides power for protection of volatile memory during primary line failure and consists of

batteries and a power supply/battery charger. The standby power supply, when implemented, provides memory power during normal ac operation as well as during a primary line power failure and maintains a charge on the 12-volt battery supply. When the standby power supply option is not implemented as a part of the 20-ampere power system, a jumper plug is installed across pins of jack 1A3J3 of the 20-ampere power supply and memory power is then derived from the 20-ampere power supply.

The 20-ampere power supply provides dc power to the computer backpanel as shown in table 3-12. Additionally, +12MEM and +5MEM are either supplied by jumper wires from the +12MAIN and +5MAIN outputs respectively of the 20-ampere power supply or from the standby power supply when that option is implemented.

Three control signals are generated on the 20-ampere power supply and are provided to the computer system via the backpanel. The signals are TLPRES-, TLFWP-, 120HZ. TLPRES- remains at logic ZERO until all supply voltages are stable and then goes to logic ONE. The warning pulse, TLPFWP-, is generated when ac power failure is imminent. The 120HZ signal is the real-time clock signal provided to the processor and is a series of logic level pulses synchronized with the ac line frequency. Timing for control signals are as shown in figure 3-25.

A block diagram discussion of the elements of the 20-ampere power system is provided in the following paragraphs.

3.8.1 AC POWER CONVERTER AND FILTERS. The ac power converter and filters as shown in the block diagram of figure 3-50 transforms primary ac power into a 160-volt dc output and a 120-Hz output. The 160-volt dc output is applied to the 20-ampere power supply and also to the standby power supply when that option is in use. Refer to chassis wiring diagram figure 3-37 as well as to the block diagram for the ac power converter and filters as shown in figure 3-44 during the following description.

Primary power is applied through fuse 1F1 and the key lock switch on the programmer panel (or operator panel) to line filter 1FL1. The filtered ac is applied to terminals 1 and 2 of terminal board 1TB1. Note that transformer 1T1 is in the circuit only when its use is required to adapt the power system to 100-volt, 200-volt, or 230-volt ac input operation. Both chassis cooling fans are across the ac input at terminals 1 and 2 of the terminal board 1TB1 and the ac input is connected to the input of the ac power converter at pins 1 and 2 of jack 1A2J1.

The ac input to the power converter is applied to a bridge rectifier through two 5-ohm thermal resistors. The thermal resistors prevent excessive current through the rectifiers at power turn-on and are labeled soft start on the block diagram. The 160-volt dc output of the ac power converter is applied across filter capacitor 1C1 and to the input of both the 20-ampere power supply and, when implemented, the standby power supply.

Table 3-12. 20-Ampere Power Supply DC Power Output

SUPPLY	VOLTAGE	CURRENT MAX
+5 MAIN	5 ± 3%	20A
+12 Main	12 ± 3%	2A
-12 Main	-12 ± 6%	1A
-5 Mem	-5 ± 6%	0.05A

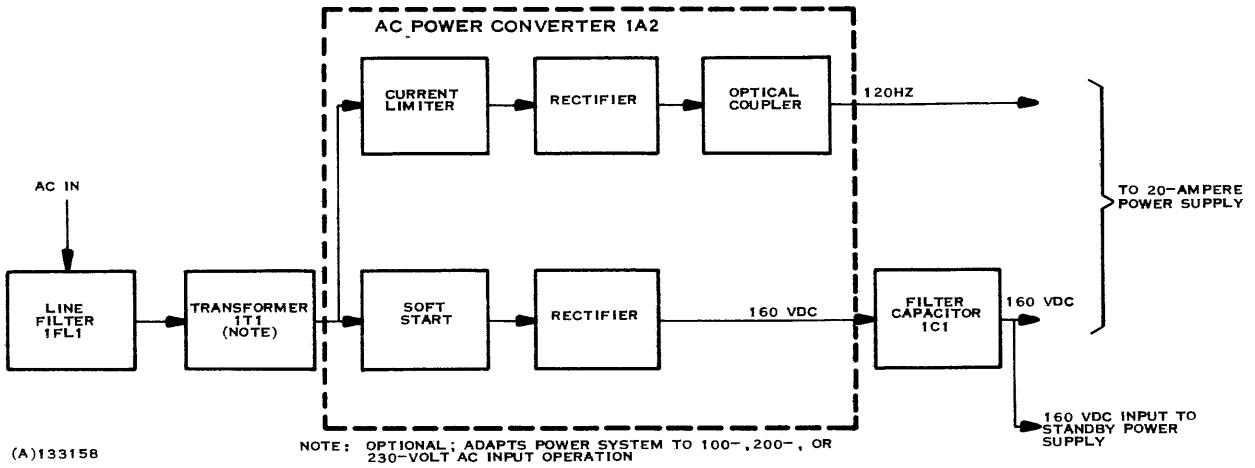


Figure 3-50. Block Diagram of Ac Power Converter and Filters

The ac input to the ac power converter is applied to another bridge rectifier circuit through four 2700-ohm current-limiting resistors. The 120-Hz full-wave output of the rectifier is optically coupled to pins 3 and 4 of jack 1A2J3 where it is wired to the input of the main power supply.

3.8.2 **20-AMPERE POWER SUPPLY.** The 20-ampere supply (see figure 3-51) is a ringing choke, sometimes referred to as flyback, dc-to-dc converter. The primary ac input is converted to approximately 160 volts dc by the ac power converter and applied to the input of the 20-ampere power supply. To this point no electrical isolation between input and output voltages has been achieved unless optional transformer 1T1 is in use. The primary voltage reference circuit is adjusted so that when the dc input voltage to the 20-ampere power supply rises to approximately 130 volts dc, the voltage threshold comparator switches in to drive an optical coupler that permits the reset to be removed from the TLPRES- and TLPFWP- circuits. The voltage threshold comparator switches off when the input dc voltage drops to about 120 volts dc.

The flyback control circuit causes the flyback switch to turn off and on at a frequency much higher than the 50 to 60 Hz input frequency. The flyback switch stores energy in the transformer through the primary winding. The flyback control circuit regulates the energy transfer from the input to the outputs by varying the frequency of operation of the flyback switch. This high frequency of application of the dc voltage to the isolation transformer reduces core size requirements of the transformer. Three secondary windings of the transformer develop multiple output voltages that are applied to their separate rectifier and filter circuits. The +5 MAIN output of the +5 volt rectifier is sensed and compared to a +5 volt reference level applied to the +5 volt regulator control circuit. A signal from the +5 volt regulator control circuit is optically coupled to the flyback control circuit and the flyback switch "on" time is varied to regulate to +5 volts. The other two output voltages applied to the rectifier and filter circuits for the +12 MAIN and -12 MAIN outputs are thus slaved to the +5 MAIN output. The outputs of the two rectifier and filter circuits are actually at approximately 16 volts in amplitude and each requires a 12-volt series regulator to provide +12 MAIN and -12 MAIN outputs. Another series regulator provides the -5 MEM output from either the -12 MAIN output or from the -12 MEM input from the standby power supply if implemented. The +12 MEM and +5 MEM outputs are patched from the +12 MAIN and +5 MAIN outputs respectively if a standby power supply is not used.

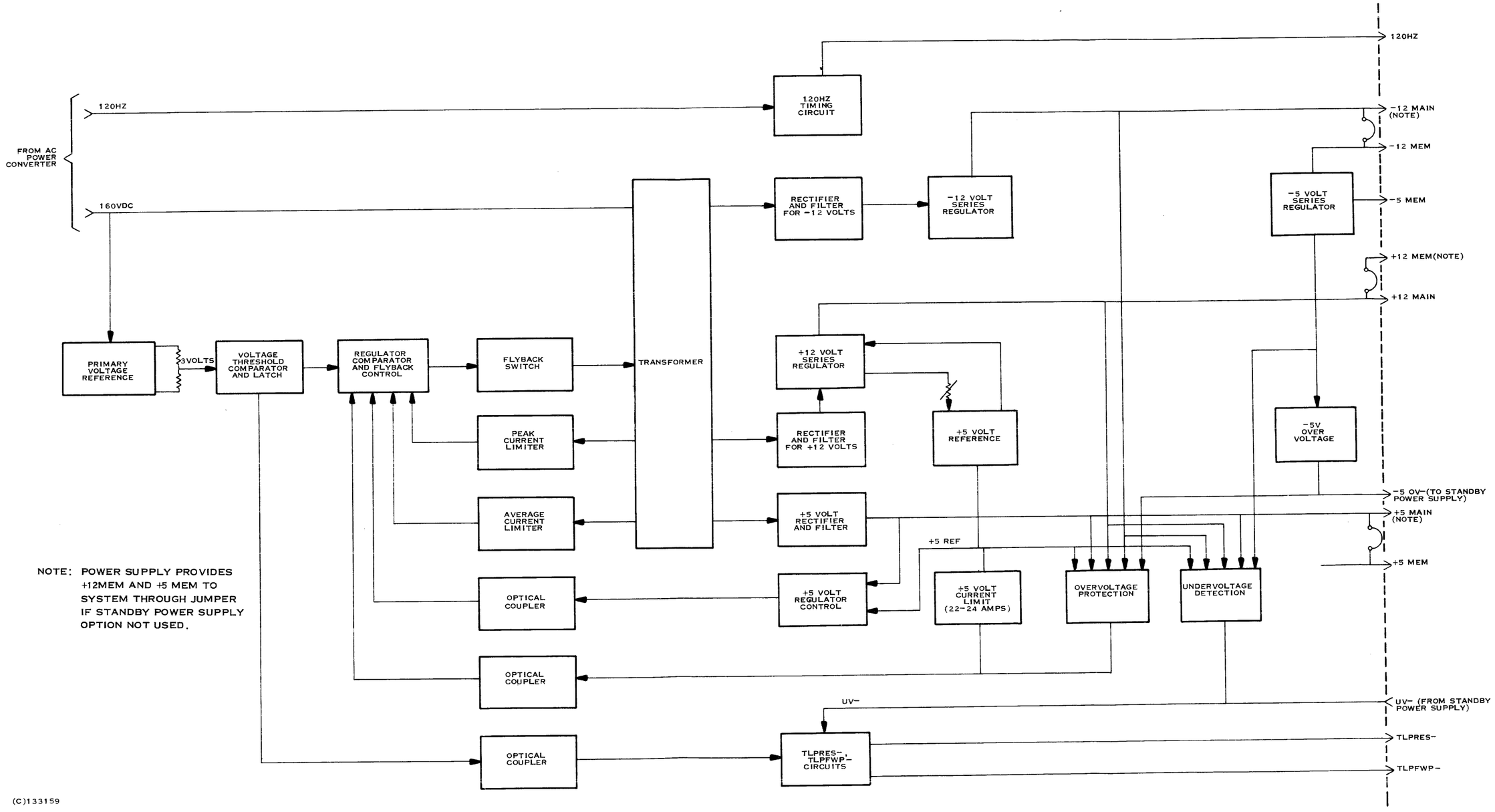


Figure 3-51. Block Diagram of 20-Ampere Power Supply

As shown in figure 3-51, an overvoltage condition at any of the power supply output voltages or an over current of the 5-volt output causes generation of a signal that is optically coupled to the flyback control circuit to shut down the power supply and power must be cycled to restart the power supply. This nondestructive shutdown also occurs when the average current in the primary winding is greater than approximately 2.5 amperes or when the temperature of the heatsink for the transistor in the flyback switch is approximately 105 degrees Celsius.

Optical couplers are used to maintain isolation between input and output voltages of the power supply. Additionally the power supply receives a 120-Hz signal input from the ac power converter, shapes the signal, and provides the signal as the real time clock input to the 990/4 circuit board. The TLPFWP- pulse output of the power supply is provided as a warning pulse prior to the loss of any output voltages and a TLPRES- reset signal is provided as an accurate status of all output power even during power-up, power-down, or total loss of power.

3.8.3 STANDBY POWER SUPPLY. The standby power supply is an optional power supply system consisting of a standby power supply assembly (mounted piggyback on the main supply) and a set of storage batteries which provide the regulated voltages used in the 990/4 memory (see table 3-13). In the event of an ac power failure, the supply automatically switches to battery power to prevent loss of data in the dynamic memory of the computer. Table 3-14 shows the normal standby time achieved by a fully charged battery under different temperature conditions.

During normal ac power conditions, the standby power supply derives its input power from the +160 volt dc output from the power converter assembly in the main power supply. The standby supply then converts the unregulated dc input into the regulated ±12 and +5 volts dc voltages required by the RAM memories used in the computer. The standby supply also contains a battery charger circuit used to provide charging current for the storage batteries.

The standby power supply automatically switches to battery operation any time the +160-volt output from the ac power converter fails to deliver adequate power. The standby power supply generates UV- to notify the main power supply of the status of the output voltages from the standby power supply. The low voltages signal (UV-) is used by the main power supply to generate the computer power reset (TLPRES-) signal sent to the computer circuit board. When the batteries discharge to the minimum functional voltage level, the standby power supply shuts down.

When normal ac power is restored, the standby supply develops an equalizing voltage until the charge current drops to the trickle charge level. The supply then switches to a float voltage to maintain the batteries at full charge. The standby power supply also has provisions for preventing battery operation unless ac power is first applied to the system (+160 volts dc output of the ac power converter is within tolerance).

Another feature of the standby power supply is an overvoltage protection circuit which disables the standby supply and blows the battery fuse in the event that any of the memory voltages exceed predetermined values.

Table 3-13. Standby Power Supply Specifications

Supply Voltage	Output Voltage	Output Current
+5 MEM	5 Vdc, ±3%	1.4A
+12 MEM	+12 Vdc, ±3%	1.2A
-12 MEM	-8 Vdc to -25 Vdc	0.1A
Battery	12 Vdc	0.5A

Table 3-14. Standby Operation Specifications

5 MEM Current (A)	12 MEM Current (A)	BATTERY TIME (Hours) Ambient Temperature		
		0°C	25°C	50°C
0.3	0.1	6.0	8.0	9.0
0.5	0.15	3.5	4.0	5.0
01.7	0.20	2.5	3.0	3.5

Notes: 1. As batteries age, standby lines will decrease.
2. Above chart assumes a fully charged battery.

Functionally, the standby power supply consists of the following major circuits:

160-volt to 20-volt converter

12-volt converter

Regulator control

5-volt regulator

12-volt overvoltage protection circuit

5-volt overvoltage protection circuit

Battery charger circuit

Battery circuit

A simplified block diagram of the standby power supply is shown in figure 3-52. The operation of the circuits is briefly described in the following paragraphs.

3.8.3.1 **160-Volt to 20-Volt Converter.** The 160-volt to 20-volt converter is a flyback type dc-dc converter similar to the converters used in the main power supply. The converter steps down the unregulated +160-volt (nominal) output of the power converter in the main supply to an unregulated +20-volt dc used by the battery charger, and by the 12-volt and 5-volt regulators during normal operation. The converter is automatically shut down if an overvoltage condition is detected on any of the memory supply voltage lines (±12 or 5 volts dc).

3.8.3.2 **12-Volt Converter.** The 12-volt converter is also of the flyback converter type that operates from the unregulated +20-volt dc output of either the 160-volt to 20-volt converter (normal operation) or from the standby batteries (power fail condition). The 12-volt converter also contains provisions for shutting down in the event of an overvoltage condition at the converter output.

3.8.3.3 **5-Volt Regulator.** The 5-volt regulator is a series regulator used to develop the reference voltage for the regulator control circuit and the 12-volt converter, and to develop the regulated +5-volt dc memory voltage. The overvoltage associated with the 5-volt regulator shuts down the 160-volt to 20-volt converter and causes the battery fuse to open in the event that the output of the +5-volt regulator rises above a predetermined value.

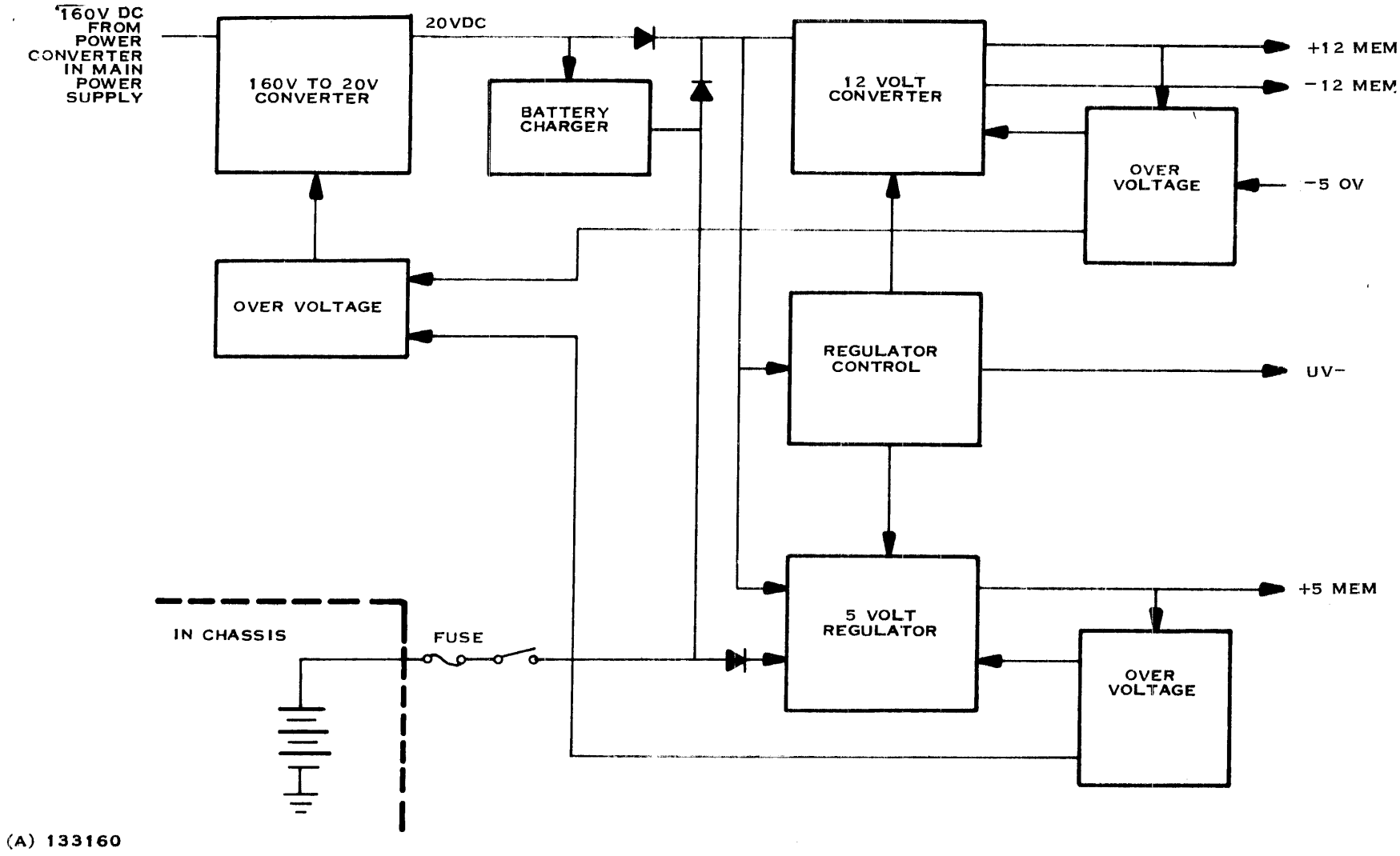


Figure 3-52. Standby Power Supply, Simplified Block Diagram

ALPHABETICAL INDEX

ALPHABETICAL INDEX

INTRODUCTION

The following index lists key words and concepts from the subject material of the manual together with the area(s) in the manual that supply major coverage of the listed concept. The numbers along the right side of the listing reference the following manual areas:

- Sections - References to Sections of the manual appear as "Section x" with the symbol x representing any numeric quantity.
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  Tx-yy

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  Fx-yy

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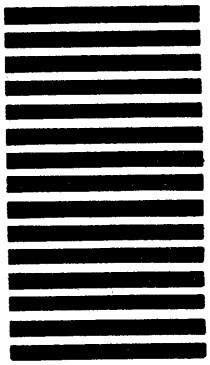

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