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PRINCIPLES OF OPERATION

FOR

ILLIAC IV MEMORY LOGIC UNIT

(June 6, 1972)

by

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ABSTRACT

This document describes the Operation of the Memory Logic Unit (MLU) of the ILLIAC IV Processing Unit. In particular this document describes the MLU major components from the functional point of view; it provides a summary of the main characteristics of the ECL integrated circuits used in the MLU and describes the WRITE, READ and TRANSFER cycles with regard to data movements between the PE, PEM and the ILLIAC IV I/O Subsystem.

The latter part of this document contains a signal glossary and a description of the power distribution in the MLU.

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PREFACE

This document is intended to serve as a source of detailed information regarding the principles of operation of the ILLIAC IV system memory logic unit. It is the first of a set of manuals that, together, will define the principles of operation of the major subunits of an ILLIAC IV system processing unit.

This manual will be most effective when used with the full set of memory logic unit logic diagrams. The Burroughs Corporation drawing numbers for these diagrams are:

1727-2188
1727-8755 (2 sheets)
1727-9084
1728-1486
1732-1076
1732-1019
1732-1092

For the reader's convenience, excerpts from these diagrams are included with the text. The excerpts are not controlled by an engineering change control procedure; in any discrepancy between the contents of the manual and the logic diagrams, the logic diagrams shall prevail.

SECTION 1.0

INTRODUCTION

The memory logic unit (MLU) is a subunit of the ILLIAC IV processing unit (PU). It serves as the main data switch for its PU, routing data between major subunits of the ILLIAC IV system during write memory cycles, read memory cycles and transfer cycles. Each PU in the system includes one MLU. Figure 1-1 illustrates the relationship of the MLU to other elements in the ILLIAC IV system in terms of their data paths through the MLU.

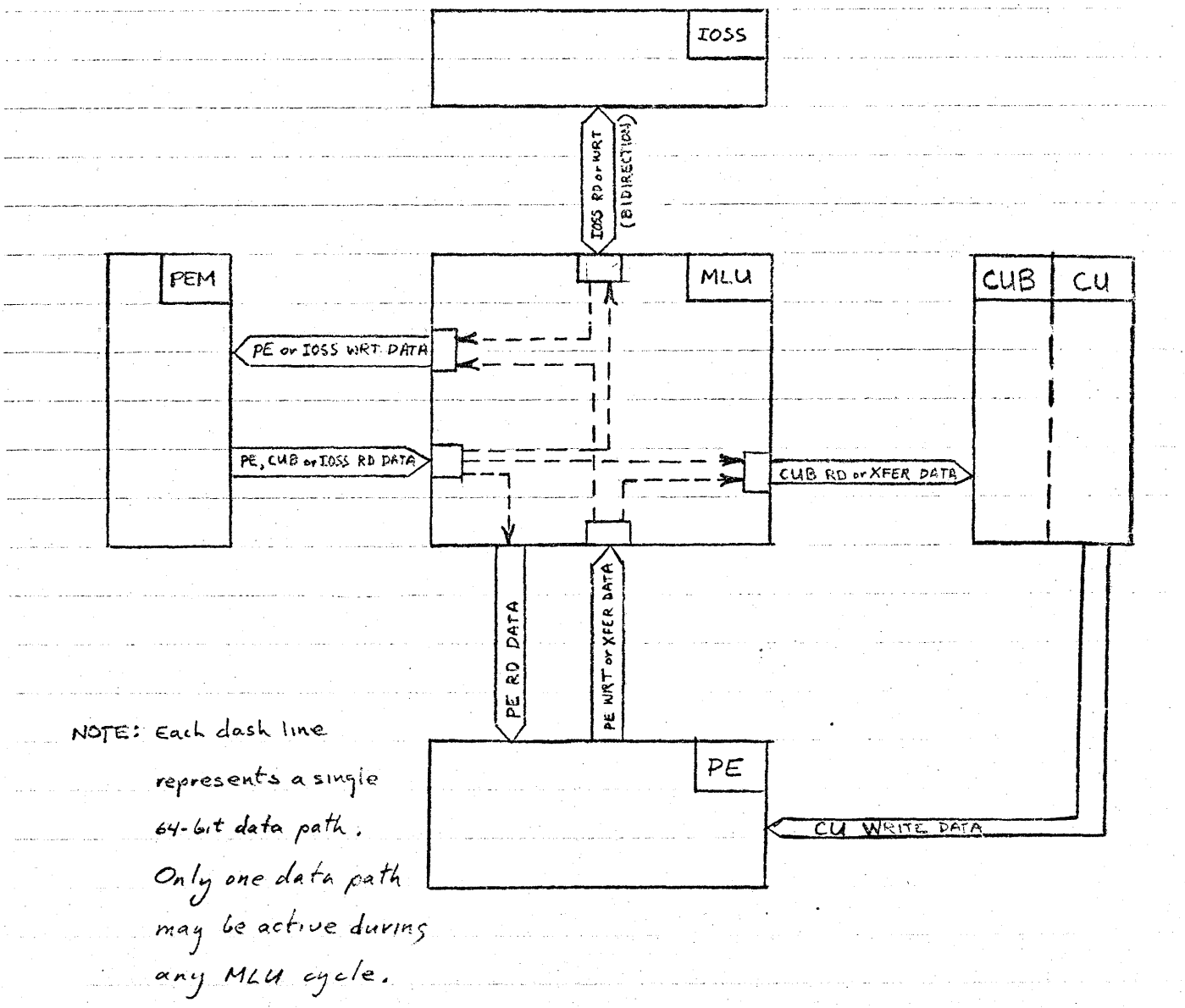


Figure 1-1. MLU Data Paths

As the emphasis in Figure 1-1 on data paths suggests, all MLU activity is based on the movement of data. These MLU activities constitute three types of data movement operations: write memory cycles, read memory cycles and transfer cycles.

A. Write Memory Cycle - Data is written into the processing element memory (PEM). The source of the data may be the processing element (PE), control unit (CU) or input/output subsystem (IOSS).

B. Read Memory Cycle - Data is fetched from the PEM. The destination of the data may be the PE, control unit buffer (CUB) or IOSS.

C. Transfer Cycle - Data is sent from the PE to the CUB.

In all cases, the data is routed through the MLU, which must multiplex the various data paths.

The data paths shown in Figure 1-1 are 64 bits wide. CU and IOSS write cycles and all read cycles always involve the movement of full 64-bit words. The PE, however, may choose to write or transfer either 32-bit or 64-bit words.

The PE writes or transfers the full 64-bit word by selecting both of a pair of control lines to the MLU. These control lines each enable a separate 32 bits of the appropriate data path (PE write or transfer). To write or transfer a 32-bit word, the PE selects only one of the control lines. The one it selects will depend on which half of the PE write or transfer data path it wishes to enable.

One 32-bit word is referred to as the inner word and the other as the outer word. This partitioning of the PE write and transfer data paths is done to satisfy PE requirements for an inner word/outer word data format. Details regarding the use of this format are contained in the PE theory of operations manual.

Address information for read and write memory cycles is provided by the CU through the PE. No address information is needed for transfer cycles. Those control signals not generated by the MLU (e.g., cycle initiate signals) are also issued to the MLU from the CU through the PE.

Internal MLU logic employs ECμL circuits. However, because two of the devices with which the MLU communicates use CTμL circuits, the MLU includes signal level conversion circuits to provide logic level compatibility among the devices. The units that use CTμL circuits are the PEM and IOSS. The PE and CUB are both ECμL devices.

The level converters are located at those points in the MLU signal paths where the MLU interfaces with the PEM, IOSS and CUB.

-NOTE-

Although internal CUB logic uses ECμL circuits, the MLU-to-CUB interface uses the same CTμL driver circuits employed by the MLU-to-IOSS interface. For this reason, signals sent from the MLU to the CUB are converted from ECμL levels to CTμL levels at the MLU and reconverted from CTμL levels to ECμL levels in the CUB.

Because ECμL levels are -0.4 V and +0.4 V and CTμL levels are -0.5 V and +2.5 V, ECμL-to-CTμL converters are designated up converters. CTμL-to-ECμL converters are designated down converters.

Power for the MLU logic circuits has two sources. Two power supplies in a power supply shunt regulator provide +1.32 V and -3.20 V. A power supply that is external to the PU provides +4.8 V and ground.

The MLU is housed as an integral part of its PU. Each PU contains, in addition to the MLU, a PE, PEM and power supply shunt regulator. Figure 1-2 illustrates the physical relationship of an MLU to these other major components of its PU.

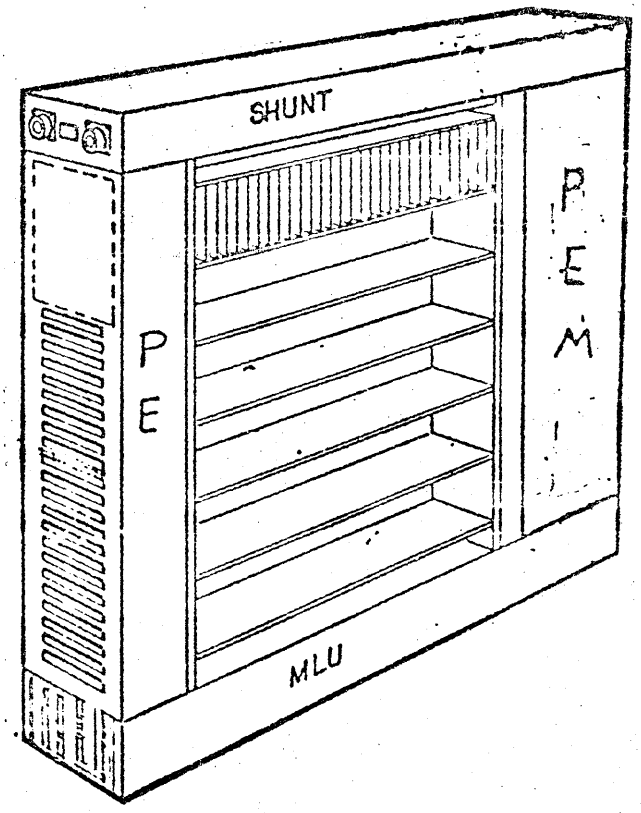


Figure 1-2. ILLIAC IV PU Subunits

SECTION 2.0
MLU COMPONENTS

The logic comprising an MLU can be classified into five functional categories: memory information register, (MIR), memory timing (MT), memory control (MC), input/output (IO) and up converter (UC). Figure 2-1 provides a block diagram of these functional components.

The logic responsible for performing these functions is distributed among five distinct printed circuit card types. For the most part, the logic is distributed along functional lines; for this reason the five card types are referred to by the five function labels listed above. This functional separation is not complete, however. Down conversion logic is located on the MIR cards and on the IO cards. Up conversion responsibility is also shared by the UC cards and some logic on the IO cards.

The parenthetical number next to each function label in Figure 2-1 indicates the quantity of printed circuit cards there are of that type in a single MLU.

2.1 MEMORY INFORMATION REGISTER

The MIR logic is the main switching station for data passing through the MLU. Read/transfer select gates multiplex read and transfer data paths, selecting one set of data or the other and routing it to the IO cards. PE/IO select gates multiplex PE write or transfer data with IOSS write data and drive the selected data into the MIR latches. The MIR logic also includes a set of latches for temporary storage of write data from the PE, CU and IOSS and transfer data from the PE. This temporary storage is required to allow time for MLU control logic to prepare for a write or transfer operation.

A set of down converters is also included on the MIR cards to convert the CTμL logic levels of the read data received from the PEM to the ECL logic levels required by MLU circuits. Details regarding the need for logic level conversions at various points in the data paths are provided in Section 3.0. The four functions performed by MIR logic are illustrated by the block diagram in Figure 2-2.

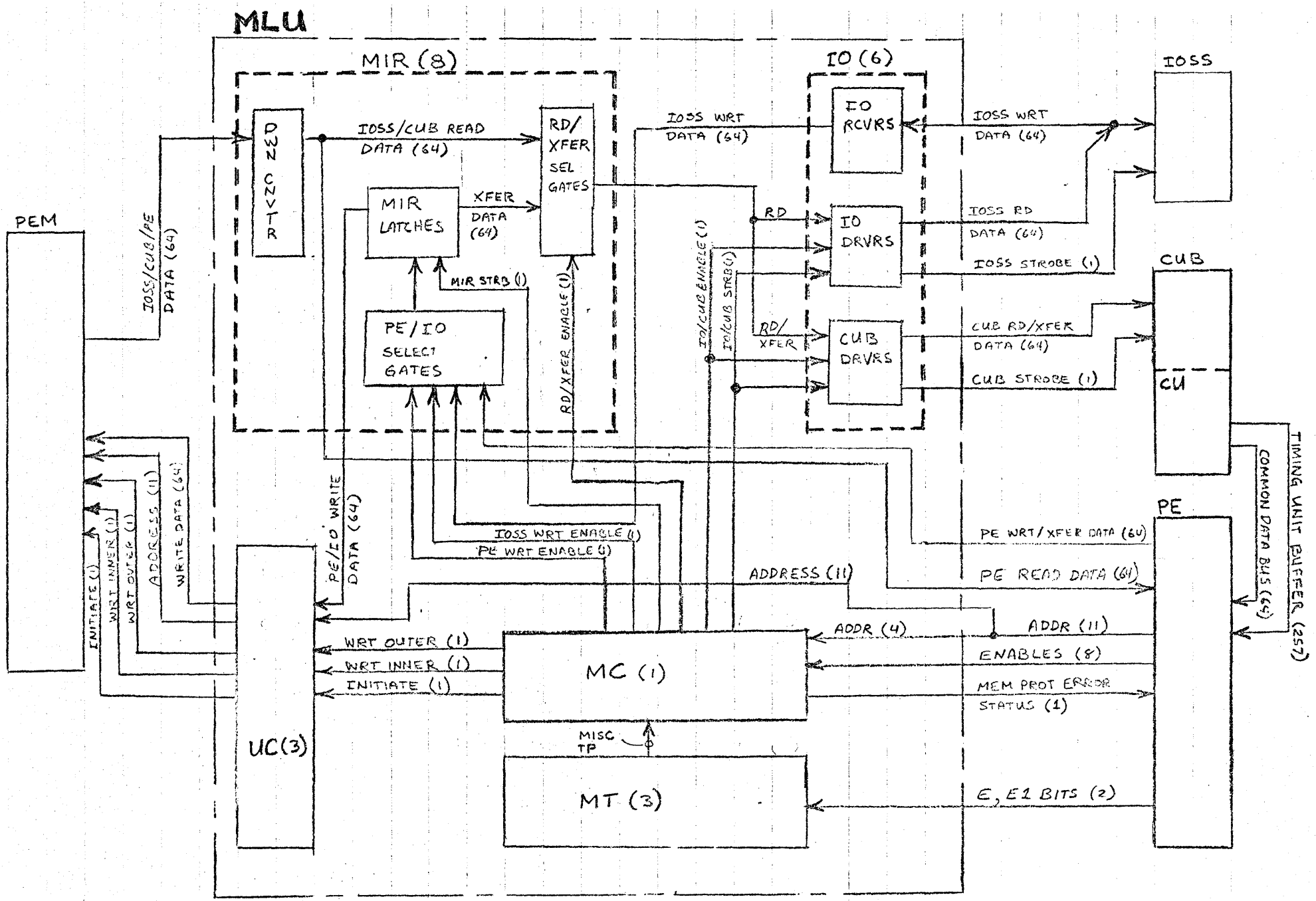


Figure 2-1. MLU Functional Organization

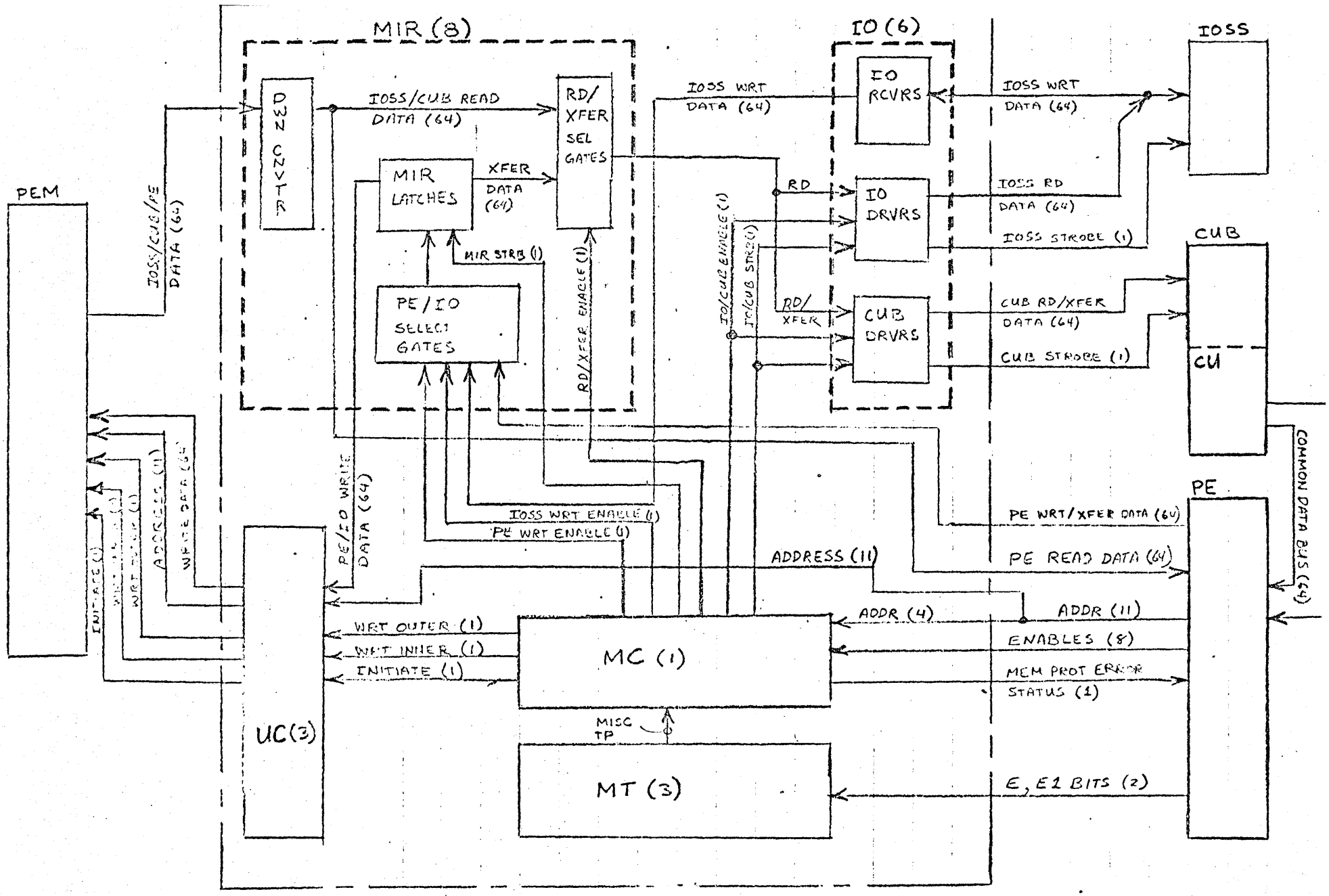


Figure 2-1 MLU Functional Organization

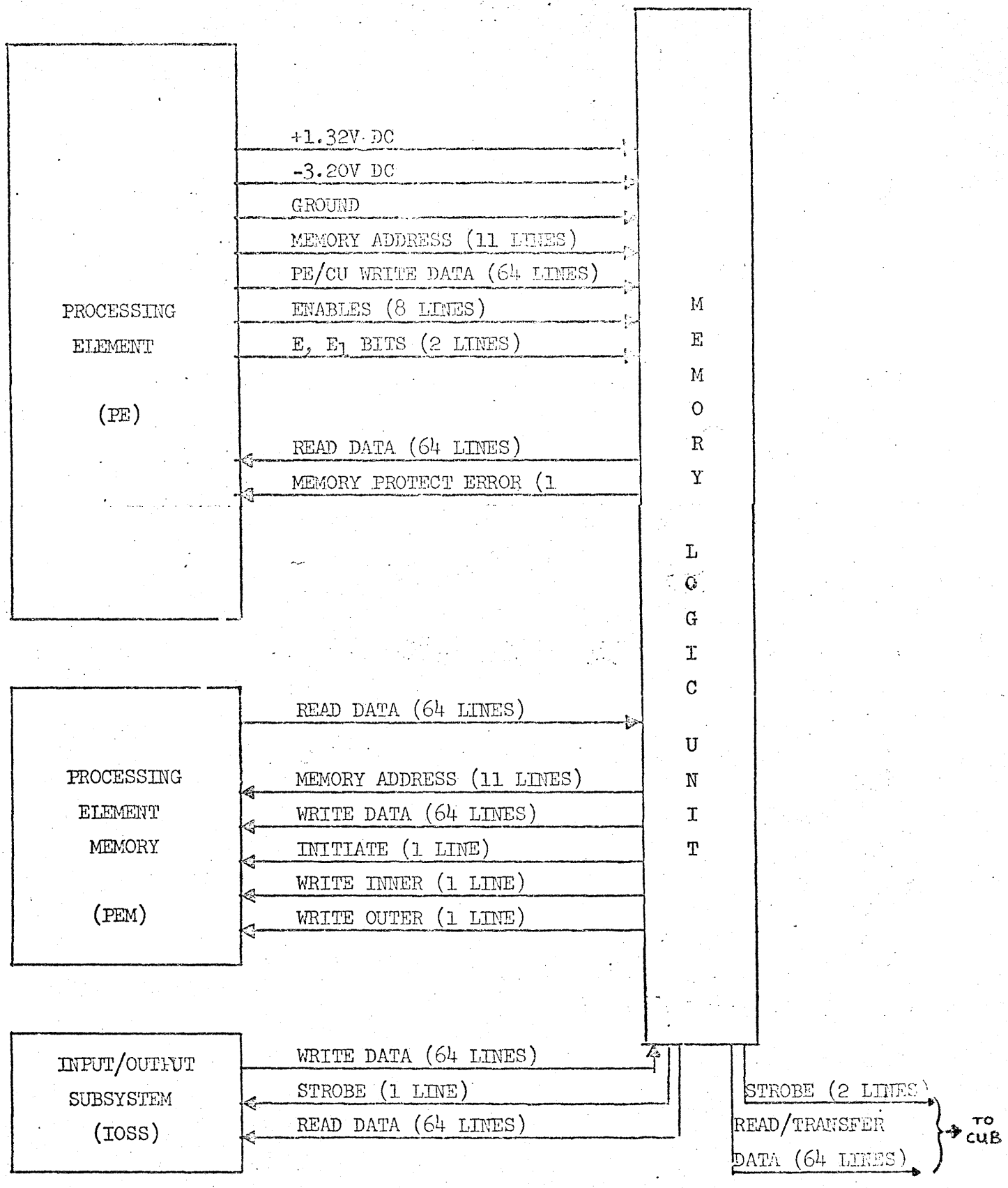


Figure 2-2. MIR Functional Block Diagram

There are eight MIR cards in an MLU, each of which accommodates eight data bits. These eight cards are not organized in a simple sequence (i.e., MIR1, MIR2, MIR3...MIR8) because of the inner word/outer word data format used for PE write and transfer data. Wiring of the data paths into and out of the MIR cards takes into account the byte organization of the inner and outer words. The inner word consists of bytes 2 through 5; the outer word, which is routed through the MIR as a continguous group, consists of bytes 1, 6, 7 and 8. Tables 2-1 and 2-2 match the eight data bytes with their respective MIR cards. Table 2-1 shows the order in which these cards are plugged into the MIR connector panel; Table 2-2 provides the signal names of the various data paths that pass through the MIR and identifies their respective sources and destinations.

Table 2-1. Data Routing Through MIR Cards

WORD	INNER WORD				OUTER WORD			
MIR CARD NO.	MIR 2	MIR 3	MIR 4	MIR 5	MIR 1	MIR 6	MIR 7	MIR 8
BITS ASSIGNED TO CARD	8-15	16-23	24-31	32-39	0-7	40-47	48-55	56-63
MLU CONNECTOR NO.	J04	J05	J06	J07	J08	J09	J10	J11

Table 2-3 lists all signals entering and leaving the MIR cards and identifies their respective sources and destinations. This table is followed by a glossary of those signals.

MIR		SOURCE OF DATA BIT			DESTINATION OF DATA BIT		
CARD NUMBER	BIT NUMBER	PE/CU PLW-W()--0	I/O MIWIW()--1	PEM MOWFW()--1	U-C MOWFW()--0	PE MOWPW()--1	I/O MOWIC()--1
1	0 thru 7	00 thru 07	00 thru 07	00 thru 07	00 thru 07	00 thru 07	00 thru 07
2	8 thru 15	08 thru 15	08 thru 15	08 thru 15	08 thru 15	08 thru 15	08 thru 15
3	16 thru 23	16 thru 23	16 thru 23	16 thru 23	16 thru 23	16 thru 23	16 thru 23
4	24 thru 31	24 thru 31	24 thru 31	24 thru 31	24 thru 31	24 thru 31	24 thru 31
5	32 thru 39	32 thru 39	32 thru 39	32 thru 39	32 thru 39	32 thru 39	32 thru 39
6	40 thru 47	40 thru 47	40 thru 47	40 thru 47	40 thru 47	40 thru 47	40 thru 47
7	48 thru 55	48 thru 55	48 thru 55	48 thru 55	48 thru 55	48 thru 55	48 thru 55
8	56 thru 63	56 thru 63	56 thru 63	56 thru 63	56 thru 63	56 thru 63	56 thru 63

Table 2-2. MIR Data List

Table 2-3. MIR Input/Output Signal List

INPUT SIGNALS		OUTPUT SIGNALS	
NAME	SOURCE	NAME	DESTINATION
PLW-W00--0	PE/J19, 20, 21	MOWPW00--1	PE/J19,20,21
↓	↓	↓	↓
PLW-W63--0	PE	MOWPW63--1	PE
MIWIW00--0	I/O/J1, 2, 3, 4, 5, 6	MOWIC00--1	I/O/J1, 2, 3, 4, 5, 6
↓	↓	↓	↓
MIWIW63--1	I/O	MOWIC63--1	I/O
MIWFW00--1	PEM/J22,24	MOWFW00--1	U.C/J16, 17, 18
↓	↓	↓	↓
MIWFW63--1	PEM	MOWFW63--1	U.C
MPTWSEL--1	MC, MIR8,7,6,5,1,4,3		
MIOWSEL--1	MC, MIR8,7,6,5,1,4.3		
MSMIRP--1	MT2, MT1		
MOUTPEN--1	MC, MIR8,7,6,5,1,4,3		
MTRANEN--1	MC, MIR8,7,6,5,1,4,3		
*MEOBIT--L1	MC, MIR6,7,8		
*MEIBIT--L1	MC, MIR3,4,5		

* MEOBIT--L1 is used by MIR#1, 6, 7, 8.

* MEIBIT--L1 is used by MIR#2, 3, 4, 5.

It must be noted also that PLW-W(00-63)--0/1 is in positive logic, which compared to the MLU negative logic corresponds to PLW-W(00-63)--1/0.

MNEMONIC	SOURCE DESTINATION	DEFINITION
MEIBIT-L1*	MT1 to MC	• Latched E_1 bit • Output of latch set by E_1 bit from PE • Allows 32-bit inner word to be written into PEM or transferred to CUB
MEOBIT-L1	MT1 to MC	• Latched E bit • Output of latch set by E bit from PE • Allows 32-bit outer word to be written into PEM or transferred to CUB
MIOWSEL-1	MC to MIR(1-8)	• Input/Output Buffer (IOB) write select • Output of MC decode logic when IOSS has been identified as source of write data • Gates IOSS write data into MIR latches for temporary storage
MIWFW00-1 through MIWFW63-1	PEM to MIR(1-8)	• PEM read data • CTL level data from the PEM, which is applied to down converters on the MIR cards • PEM output becomes valid at approximately 225 ns of the current read cycle; does not change until approximately 155 ns of next memory cycle

* All signal mnemonics are assigned 10 characters, including one or more dashes. However, in this glossary and elsewhere in the manual some of the dashes are omitted for simplification. The correct mnemonic for each signal mentioned in this manual may be found in the master signal glossary in Appendix A.

MNEMONIC	SOURCE DESTINATION	DEFINITION
MIWIW00-1 through MIWIW63-1	IO(1-6) to MIR (1-8)	• IOB input data • IOSS write data after level conversion to ECL by circuits on IO cards • Applied to PE/IO select gates on MIR cards • Data is valid from approximately 40 ns to 70 ns of a write cycle
MOUTPEN-1	MC to MIR(1-8)	• Output enable • Gates read data through read/transfer select gates on MIR cards • Occurs at beginning of output enable period of MLU cycle
MOWFW00-1 through MOWFW63-1	UC(1-3) to PEM	• PEM write data - CTpL • Write data that is sent to PEM from up converters • Data is valid for approximately 250 ns of write cycle
MOWIC00-1 through MOWIC63-1	MIR(1-8) to IO(1-6)	• CUB-IOB read/PE-CUB transfer data • Output of read/transfer select gates on MIR cards • Becomes valid as transfer data during transfer enable period of MLU cycle; becomes valid as read data during output enable period of MLU cycle

MNEMONIC	SOURCE DESTINATION	DEFINITION
MOWPW00-1 through MOWPW63-1	MIR(1-8) to PE	• PE output data • ECL level read data sent from down converters on MIR cards • Data is valid from approximately 235 ns of the read cycle to approximately 165 ns of the next memory cycle
MPTWSEL-1	MC to MIR(1-8)	• PE write/PE-CUB transfer select • Output from MC decode logic when PE has been identified as source of write or transfer data • Is ANDed with MEOBIT-1 and MEIBIT-1 to gate outer word and inner word of write or transfer data to inputs of MIR latches
MSMIRP1-1 through MSMIRP8-1	MT(1-2) to MIR(1-8)	• MIR strobes • Used by MIR logic to clock write or transfer data into MIR latches • Occurs at approximately 55 ns of the MLU cycle • 8 ns pulse width
MTRANEN-1	MC to MIR(1-8)	• Transfer enable • Gates transfer data through read/transfer select gates on MIR cards • Occurs at beginning of transfer enable period of MLU cycle

MNEMONIC	SOURCE DESTINATION	DEFINITION
PLW-W00-0 through PLW-W63-0	PE to MIR (1-8)	• PE input data • ECL level data bits sent from PE to PE/IO select gates on MIR cards • Data may have originated at CU but, at this point in data flow, is indistinguishable from PE write data • Data is valid from approximately 50 ns to 70 ns • One clock period wide

2.2 MEMORY TIMING

This logic is responsible for generating the timing signals used to control the data flow through the MLU during read, write and transfer operations. The memory timing logic is distributed among three printed circuit cards, which are referred to as MT1, MT2 and MT3.

The principal logic elements on each MT card are two variable delay lines DL1 and DL2, each having a maximum delay value of 50-ns, and four 50-ns tapped delay lines. These taps are at 5-ns increments; not all of the taps are used.

The output of DL1 on MT1 is used to strobe a pair of control pulses (P----E--30 and P----1--30), which are issued by the PE, into a pair of latches located on MT1. These are the pulses that are used by the PE to control the 32-bit inner word and 32-bit outer word in a PE write or transfer operation. The output of DL1 on MT2 strobes a pair of read select pulses (MCURSEL--1 and MIORSEL--1) into a pair of latches located on MT2. The output of DL1 on MT3 is not used.

The output of DL2 on MT1 is used to adjust the timing of the MIR strobes. The MIR strobes are the pulses that clock write and transfer data into the MIR latches. The second variable delay lines (DL2) on MT2 and MT3 are not used.

Among the three MT cards, there are a total of 12 tapped delay lines. These 12 delay lines are connected in series.

Figure 2-3 illustrates the relative positions of the components on the MT cards. This illustration is included because component numbering on the MT cards is not consistent with the numbering scheme used for other MLU card types.

Figures 2-4 and 2-5 provide a functional interface diagram and an interconnection diagram for the MT and MC cards. Table 2-4 lists the signals that enter and leave the MT cards and identifies their sources and destinations. The signals listed in that table are defined in the following glossary.

MNEMONIC	SOURCE DESTINATION	DEFINITION
MCURSEL-1	MC to MT2	• CUB read select • Indicates that CUB has been selected as destination of read data
MCURSEL-L1	MT2 to MC	• Latched CUB read select • Output of a latch set by MCURSEL-1 • Maintains CUB read select until data is gated out to CUB during output enable period of read cycle • Latch sets at approximately 130 ns of CUB read cycle

NOTE: Components at positions:

1) U1, U9, U17, U25 are Clock Terminations
2) U2, U6, U8, U10, U12, U16, U18, U22, U24, U27, are Pulldown resistors
3) U14 is Clock Buffer Reference Module
4) U4, U20 are Terminating Resistors

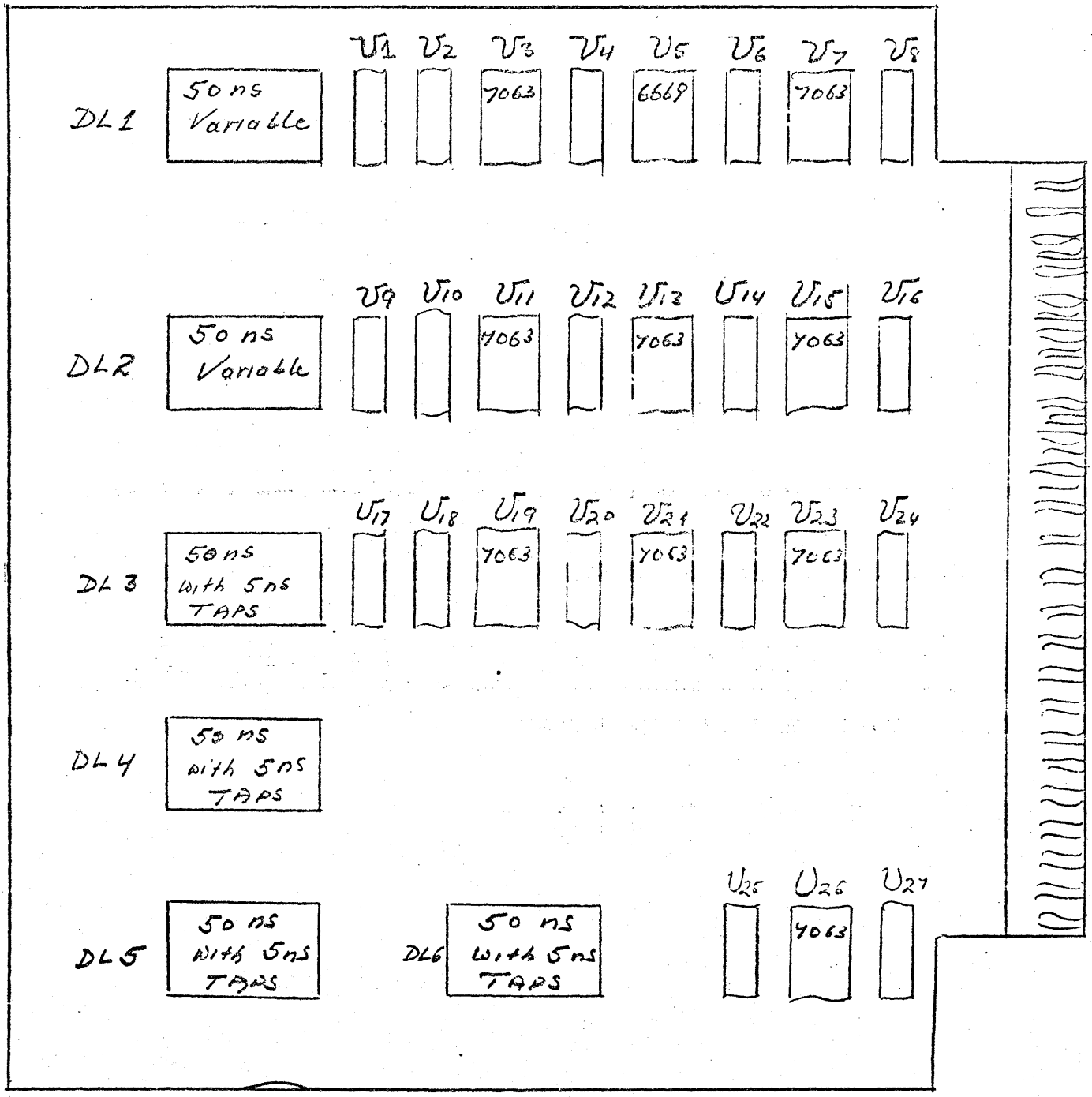


Figure 2-3. Component Numbering Scheme for MT Cards (Component Side)

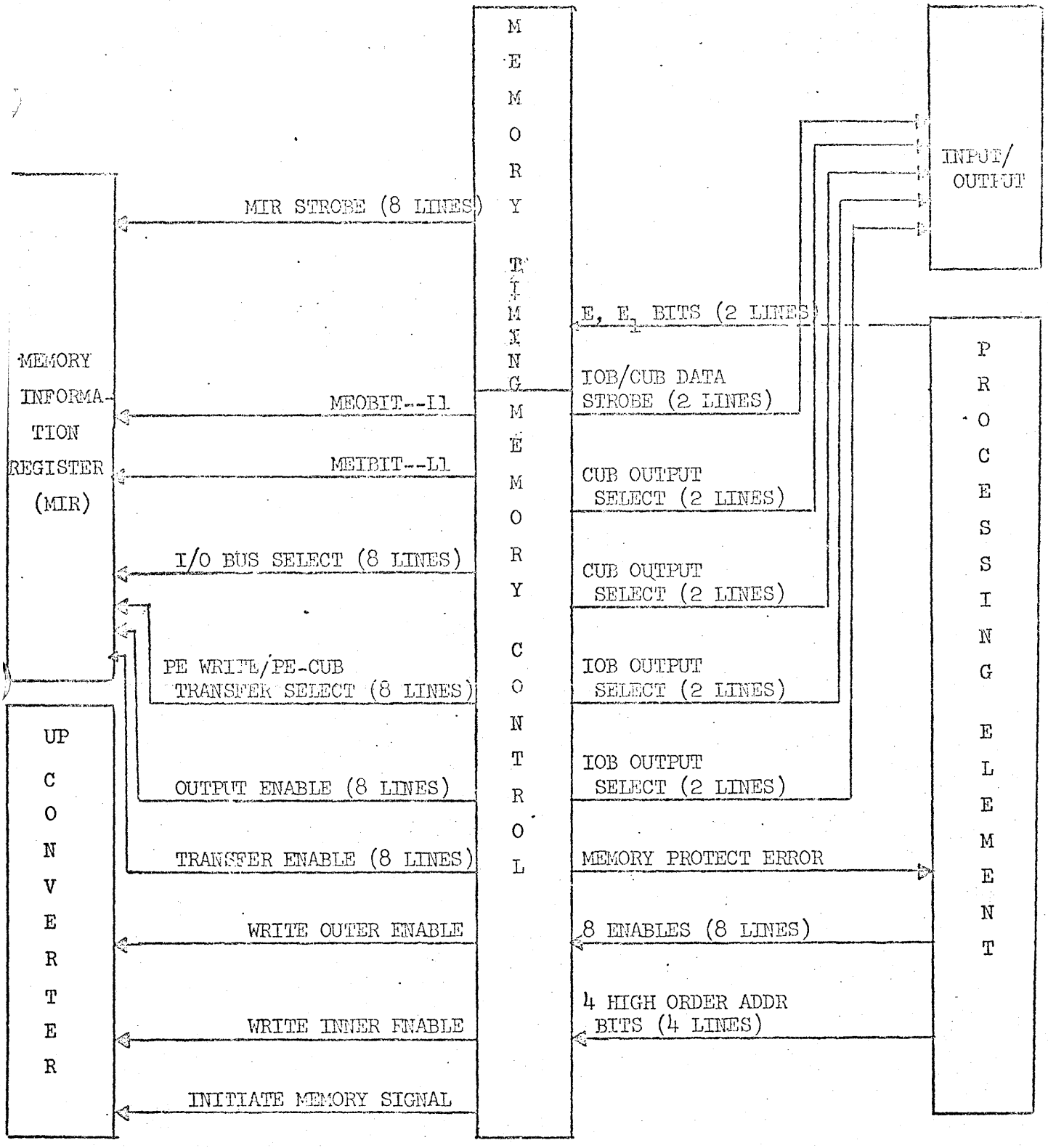


Figure 2-4. Memory Timing and Control
Functional Interface Diagram

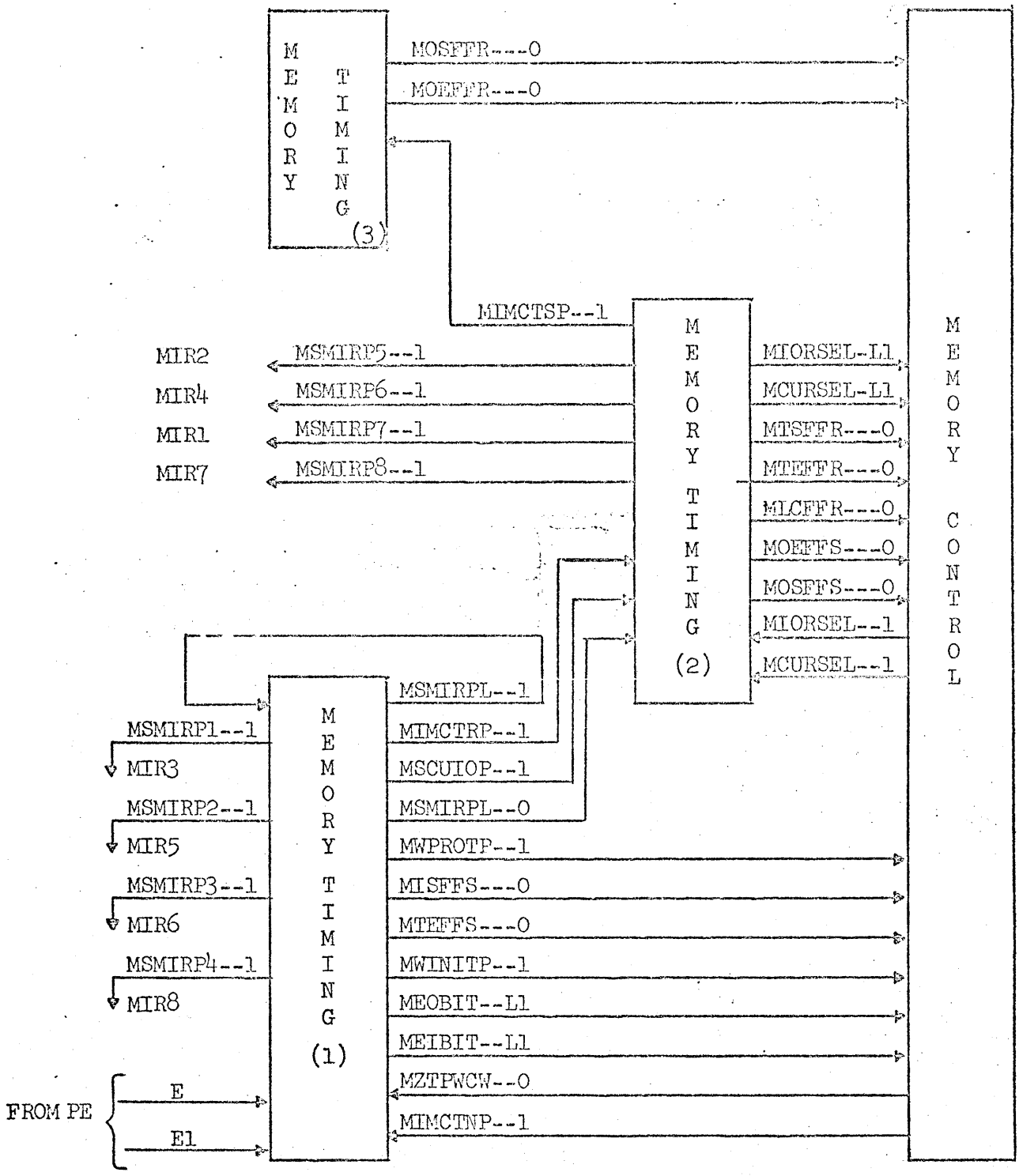


Figure 2-5. Memory Timing and Control Cards Interconnection

Table 2-4. Memory Timing Card Input/Output Signal List

M.T. CARD #	INPUT SIGNALS		OUTPUT SIGNALS	
	NAME	SOURCE	NAME	DESTINATION
1	MIMCTNP--1	MC/6C11	MEIBIT--L1	MC/B38
	MZTPWCW--0	MC/B20	MEOBIT--L1	MC/A39
	MSMIRPL--1	MT#1/C15	MWINITP--1	MC/B24
	P----E--30	PE/J19-C45	MSMIRPL--0	MT#2/D12
	P----1--30	PE/J19-A45	MSMIRPL--1	MT#1/D12
			MSMIRP1--1	MIR3/C45
			MSMIRP2--1	MIR5/C45
			MSMIRP3--1	MIR6/C45
			MSMIRP4--1	MIR8/C45
			MSCUIOP--1	MT#2/A23
			MTEFFS---0	MC/B26
			MIMCTRP--1	MT#2/A11
			MTSFFS---0	MC/B12
			MWPROTP--1	MC/A41
2	MIMCTRP--1	MT#1/B24	MIORSEL-L1	MC/B18
	MSCUIOP--1	MT#1/A33	MCURSEL-L1	MC/C11
	MSMIRPL--1	MT#1/C17	MTSFFR---0	MC/B6
	MCURSEL--1	MC/2C45	MTEFFR---0	MC/D14
	MIORSEL--1	MC/1C15	MSMIRP5--1	MIR2/C45
			MSMIRP6--1	MIR4/C45
			MSMIRP7--1	MIR1/C45
			MSMIRP8--1	MIR7/C45
			MLCFFR---0	MC/D26
			MOEFFS---0	MC/A11
			MIMCTSP--1	MT#3/A11
			MOSFFS---0	MC/A9
3	MIMCTSP--1	MT#2/B24	MOSFFR---0	MC/C5
			MOEFFR---0	MC/B8

MNEMONIC	SOURCE DESTINATION	DEFINITION
MEIBIT-L1	MT1 to MC	• Latched E_1 bit • Output of latch set by E_1 bit from PE • Allows 32-bit inner word to be written into PEM or transferred to CUB
MEOBIT-L1	MT1 to MC	• Latched E bit • Output of latch set by E bit from PE • Allows 32-bit outer word to be written into PEM or transferred to CUB
MIMCTNP-1	MC to MT1	• Initiate selected memory/ transfer cycle • Input to delay line; initiates sequence of timing pulses for read, write or transfer cycle • Results from FIMC-1 AND FMSEL-1 or FZTPWCW-0 • One clock period wide
MIMCTRP-1	MT1 to MT2	• MT1 delay line output • Output of series of delay lines on MT1 • Used as input to MT2 delay line series • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MIMCTSP-1	MT2 to MT3	• MT2 delay line output • Output of series of delay lines on MT2 • Used as input to series of delay lines on MT3 • 50 ns pulse width
MIORSEL-1	MC to MT2	• IOB read select • Output of MC decode logic when IOSS has been identified as destination of read data
MIORSEL-L1	MT2 to MC	• Latch IOB read select • Output of latch set by IOB read select signal • Preserves the IOB read select condition until the read data has been gated out to the IOSS • Becomes valid at approximately 130 ns of the read cycle
MLCFFR-0	MT2 to MC	• Control F-F reset • Resets memory write enable flip-flop and transfer flip-flop • Occurs at approximately 250 ns of MLU cycle • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MOEFFR-0	MT3 to MC	• Reset output enable F-F • Resets output enable flip-flop at approximately 370 ns of MLU cycle • 50 ns pulse width
MOEFFS-0	MT2 to MC	• Set output enable F-F • Sets output enable flip-flop at approximately 270 ns of MLU cycle • Begins output enable period of MLU cycle • 50 ns pulse width
MOSFFR-0	MT3 to MC	• Reset output strobe F-F • Resets output/transfer strobe generator at approximately 350 ns of MLU cycle • 50 ns pulse width
MOSFFS-0	MT2 to MC	• Set output strobe F-F • Sets output/transfer strobe generator at approximately 290 ns of MLU cycle • 50 ns pulse width
MSCUIOP-1	MT1 to MT2	• CU/IO read select latch • Strobes the CU and IO read select latches on MT_2 • Occurs at approximately 130 ns of MLU cycle • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MSMIRPL-1	MT1 to MT1	• MIR strobe pulse • Used to generate four of the eight MIR strobe signals, MSMIRP(1-4)-1. • Occurs at approximately 55 ns of MLU cycle • 8 ns pulse width
MSMIRPL-0	MT1 to MT2	• MIR strobe pulse • Complement of MSMIRPL--1 • Used to generate four of the eight MIR strobe signals, MSMIRP(5-8)-1 • Occurs at approximately 55 ns of MLU cycle • 8 ns pulse width
MSMIRP1-1 through MSMIRP8-1	MT(1-2) to MIR(1-8)	• MIR strobes • Used by MIR logic to clock write or transfer data into MIR latches • Occurs at approximately 55 ns of the MLU cycle • 8 ns pulse width
MTEFFR-0	MT2 to MC	• Reset transfer enable F-F • Resets transfer enable flip-flop at approximately 265 ns of MLU cycle • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MTEFFS-0	MT1 to MC	• Set transfer enable F-F • Sets transfer enable flip-flop at approximately 165 ns of MLU cycle • Begins transfer enable period of cycle • 50 ns pulse width
MTSFFR-0	MT2 to MC	• Reset transfer strobe F-F • Resets output/transfer strobe generator at approximately 245 ns of MLU cycle • 50 ns pulse width
MTSFFS-0	MT1 to MC	• Set transfer strobe F-F • Sets output/transfer generator at approximately 185 ns of MLU cycle • 50 ns pulse width
MWINITP-1	MT1 to MC	• Write initiate • Used with write control signal to generate initiate memory signal (MINITPL-0) • Occurs at approximately 55 ns of MLU cycle • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MWPROTP-1	MT1 to MC	• Write protect • Sets the memory protect error flip-flop if error has been detected or sets write enable flip-flop if no error is detected • Occurs at approximately 40 ns of read or write cycle; is suppressed by MZTPWCW-0 during transfer cycle to prevent setting of write enable flip-flop • 50 ns pulse width
MZTPWCW-0	MC to MT_1	• Transfer cycle • Output of transfer flip-flop when flip-flop is set by FZTPWCW-0 • Indicates that MLU is performing transfer operation • Conditions other MLU logic to allow transfer of data from PE to CUB • Prevents MWPROTP-1 from setting write enable flip-flop; this, in turn, prevents MLU from issuing write enable signals to PEM

MNEMONIC	SOURCE DESTINATION	DEFINITION
P-E-30	PE to MT1	• E bit signal • Sent by PE to allow passage of the outer word of PE write or transfer data (bits 00 through 07 and 40 through 63) through the MLU • Sets the E bit latch on MT1 to generate MEOBIT-L1 • At least one clock period wide
P-1-30	PE to MT1	• E1 bit signal • Sent by PE to allow passage of the inner word of PE write or transfer data (bits 08 through 39) through the MLU • Sets the E1 bit latch on MT1 to generate MEIBIT-L1 • At least one clock period wide

2.3 MEMORY CONTROL

The MC logic generates those signals needed by the other MLU logic to initiate, carry out and terminate read, write and transfer cycles. MC logic performs a memory protect function as well. The memory protect circuits examine the four least significant address bits and, during write operations, prevent access to a block of 128 PEM addresses if the PE indicates that they are to be protected.

Table 2-5 lists all signals entering and leaving the MC card and identifies their sources and destinations. These signals are defined in a glossary that follows the table. The functional relationship of the MC card to other elements of the MLU is shown in Figure 2-4. The signal interfaces shared by the MC card and MT cards is illustrated in Figure 2-5.

Table 2-5. Memory Control Card Input/Output Signals List

INPUT SIGNAL		OUTPUT SIGNAL	
NAME	SOURCE	NAME	DESTINATION
PYW-WO5--0	PE	MWOUTEN--0	UC#2/D26
PYW-WO6--0	PE	MWINNEN--0	UC#2/C11
PYW-WO7--0	PE	MPROER---1	PE
PYW-WO8--0	PE	MIMCTNP--1	MT#1/A11
FMEMPRO--1	PE	MINITPL--0	UC#2/C39
MEOBIT--L1	MT#1/A5	MZTPWCW--0	MT#1/A41
MEIBIT--L1	MT#1/C3	MTRANEN--1	MIR#1-8/D14
MWPROTP--1	MT#1/A35	MOUTPEN--1	MIR#1-8/C17
FRMPRO---0	PE	MSTROBE--1	IO#1, 4/04
MWINITP--1	MT#1/C23	MCURTSL--1	IO#1-3/72
FIMC-----1	PE	MCURTSL--3	IO#4-6/72
FMSEL----1	PE	MIOROSL--1	IO#1-3/70
FZTPWCW--0	PE	MIOROSL--3	IO#4-6/70
MLCFFR---0	MT#2/B36	MCURSEL--1	MT#2/A3
MCABCLR--0	MLU	MPTWSEL--1	MIR#1-8/B42
MCURSEL-L1	MT#2/A5	MIORSEL--1	MT#2/B2
MOEFFS---0	MT#2/B48	MIOWSEL--1	MIR#1-8/D44
MOEFFR---0	MT#3/A29	MEOBIT--L1	MIR#8/B44
MOSFFS---0	MT#2/B30	MEIBIT--L1	MIR#5/B44
MTSFFS---0	MT#1/B30		
MOSFFR---0	MT#3/A39		
MTSFFR---0	MT#2/A39		
MTEFFS---0	MT#1/B48		
MTEFFR---0	MT#2/A29		
MIORSEL-L1	MT#2/C3		
FREAD----1	PE		
FMDSEL1--1	PE		
FMDSEL0--1	PE		

MNEMONIC	SOURCE DESTINATION	DEFINITION
FIMC-1	CU via PE to MC	• Initiate memory cycle • Used by PE to begin any read or write cycle • All MLU timing during read or write is referenced to arrival of FIMC-1 at MC • One clock period wide
FMDSELO-1 and FMDSELI-1	CU via PE to MC	• Memory data select • Combination of logic levels identifies source of write data or destination of read data • Used by MC to develop appropriate data gating signals • Also used to override E-bit signals (P-E-30, P-1-30) during CU or IOSS write operations • Become valid at same time as FIMC-1 and remain valid until next FIMC-1
FMEMPRO-1	CU via PE to MC	• Memory protect • Enables memory protect circuits on MC card if PE wishes to protect PEM address locations 0000 through 0127 (decimal) from a write cycle • Becomes valid at same time as FIMC-1 and remains valid until next FIMC-1

MNEMONIC	SOURCE DESTINATION	DEFINITION
FMSEL-1	CU via PE to MC	• Memory select • Used by CU to select specific memory out of all memories in array • Becomes valid at same time as FIMC-1 and remains valid until next FIMC-1
FREAD-1	CU via PE to MC	• Read/Write control • Used by PE to specify read or write cycle to MLU • Low logic level specifies read; high logic level specifies write • Becomes valid at same time as FIMC-1 and remains valid until next FIMC-1
FRMPRO-0	CU via PE to MC	• Memory protect error reset • Used by CU to reset memory protect error latch on MC card • One clock period wide
FZTPWCW-0	CU via PE to MC	• Initiate transfer • Used by PE to begin transfer cycle • All MLU timing during transfer is referenced to arrival of FZTPWCW-0 • One clock period wide

MNEMONIC	SOURCE DESTINATION	DEFINITION
MCABCLR-0	PU pwr supply to MC	• Cabinet clear • Resets MC flip-flops when power is turned on • Signal goes low when power sequencing is complete
MCURSEL-1	MC to MT2	• CUB read select • Indicates that CUB has been selected as destination of read data
MCURSEL-L1	MT2 to MC	• Latched CUB read select • Output of a latch set by MCURSEL-1 • Maintains CUB read select until data is gated out to CUB during output enable period of read cycle • Latch sets at approximately 130 ns of CUB read cycle
MCURTSL-1 MCURTSL-3	MC to IO (1-3) MC to IO (4-6)	• CUB output select • These signals gate read or transfer data to the CUB • Both are true during transfer enable period of transfer cycle or output enable period of read cycle

MNEMONIC	SOURCE DESTINATION	DEFINITION
MEIBIT-L1	MT1 to MC	• Latched E_1 bit • Output of latch set by E_1 bit from PE • Allows 32-bit inner word to be written into PEM or transferred to CUB
MEOBIT-L1	MT1 to MC	• Latched E bit • Output of latch set by E bit from PE • Allows 32-bit outer word to be written into PEM or transferred to CUB
MIMCTNP-1	MC to MT1	• Initiate selected memory/ transfer cycle • Input to delay line; initiates sequence of timing pulses for read, write or transfer cycle • Results from FIMC-1 AND FMSEL-1 or FZTPWCW-0 • One clock period wide
MINITPL-0	MC to UC2	• Initiate memory-ECL • Will initiate read or write activity in PEM after level conversion by UC2 circuits • One clock period wide during read cycles; 50 ns wide during write cycles

MNEMONIC	SOURCE DESTINATION	DEFINITION
MIOROSL-1 and MIOROSL-3	MC to IO (1-3) MC to IO (4-6)	• IOB output select enable • Gates read data through the IO logic to the IOSS • Occurs during the output enable period of read cycle if the IOSS has been identified as the destination
MIORSEL-1	MC to MT2	• IOB read select • Output of MC decode logic when IOSS has been identified as destination of read data
MIORSEL-L1	MT2 to MC	• Latch IOB read select • Output of latch set by IOB read select signal • Preserves the IOB read select condition until the read data has been gated out to the IOSS • Becomes valid at approximately 130 ns of the read cycle
MIOWSEL-1	MC to MIR(1-8)	• Input/Output Buffer (IOB) write select • Output of MC decode logic when IOSS has been identified as source of write data • Gates IOSS write data into MIR latches for temporary storage

MNEMONIC	SOURCE DESTINATION	DEFINITION
MLCFFR-0	MT2 to MC	• Control F-F reset • Resets memory write enable flip-flop and transfer flip-flop • Occurs at approximately 250 ns of MLU cycle • 50 ns pulse width
MOEFFR-0	MT3 to MC	• Reset output enable F-F • Resets output enable flip-flop at approximately 370 ns of MLU cycle • 50 ns pulse width
MOEFFS-0	MT2 to MC	• Set output enable F-F • Sets output enable flip-flop at approximately 270 ns of MLU cycle • Begins output enable period of MLU cycle • 50 ns pulse width
MOSFFR-0	MT3 to MC	• Reset output strobe F-F • Resets output/transfer strobe generator at approximately 350 ns of MLU cycle • 50 ns pulse width
MOSFFS-0	MT2 to MC	• Set output strobe F-F • Sets output/transfer strobe generator at approximately 290 ns of MLU cycle • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MOUTPEN-1	MC to MIR(1-8)	• Output enable • Gates read data through read/transfer select gates on MIR cards • Occurs at beginning of output enable period of MLU cycle
MPROER-1	MC to PE	• Memory protect error • Output of memory protect error latch, which is set when write operation is attempted in protected area of PEM • Signal is sent to CU via PE • Does not prevent subsequent write operations • Latch is reset by FRMPRO-0 from CU
MPTWSEL-1	MC to MIR(1-8)	• PE write/PE-CUB transfer select • Output from MC decode logic when PE has been identified as source of write or transfer data • Is ANDed with MEOBIT-1 and MEIBIT-1 to gate outer word and inner word of write or transfer data to inputs of MIR latches

MNEMONIC	SOURCE DESTINATION	DEFINITION
MSTROBE-1	MC to IO1,4	• IOB/CUB data strobe • Output of strobe flip-flop • Sent to up converters on IO cards for conversion to CTuL levels
MTEFFR-0	MT2 to MC	• Reset transfer enable F-F • Resets transfer enable flip-flop at approximately 265 ns of MLU cycle • 50 ns pulse width
MTEFFS-0	MT1 to MC	• Set transfer enable F-F • Sets transfer enable flip-flop at approximately 165 ns of MLU cycle • Begins transfer enable period of cycle • 50 ns pulse width
MTRANEN-1	MC to MIR(1-8)	• Transfer enable • Gates transfer data through read/transfer select gates on MIR cards • Occurs at beginning of transfer enable period of MLU cycle
MTSFFR-0	MT2 to MC	• Reset transfer strobe F-F • Resets output/transfer strobe generator at approximately 245 ns of MLU cycle • 50 ns pulse width

MNEMONIC	SOURCE DESTINATION	DEFINITION
MTSFFS-0	MT1 to MC	• Set transfer strobe F-F • Sets output/transfer generator at approximately 185 ns of MLU cycle • 50 ns pulse width
MWINITP-1	MT1 to MC	• Write initiate • Used with write control signal to generate initiate memory signal (MINITPL-0) • Occurs at approximately 55 ns of MLU cycle • 50 ns pulse width
MWINNEN-0	MC to UC_2	• Write inner enable - ECL • Output of MC decode logic whenever inner word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTμL level
MWOUTEN-0	MC to UC_2	• Write outer enable - ECL • Output of MC decode logic whenever outer word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTμL level

MNEMONIC	SOURCE DESTINATION	DEFINITION
MWPROTP-1	MT1 to MC	• Write protect • Sets the memory protect error flip-flop if error has been detected or sets write enable flip-flop if no error is detected • Occurs at approximately 40 ns of read or write cycle; is suppressed by MZTPWCW-0 during transfer cycle to prevent setting of write enable flip-flop • 50 ns pulse width
MZTPWCW-0	MC to MT_1	• Transfer cycle • Output of transfer flip-flop when flip-flop is set by FZTPWCW-0 • Indicates that MLU is performing transfer operation • Conditions other MLU logic to allow transfer of data from PE to CUB • Prevents MWPROTP-1 from setting write enable flip-flop; this, in turn, prevents MLU from issuing write enable signals to PEM

MNEMONIC	SOURCE DESTINATION	DEFINITION
PYW-W05-0 through PYW-W15-0	PE to UC(1-3)	• PE memory address register bits • ECL level address bits sent from PE to up converters for conversion to CTμL levels • CTμL levels to be used by PEM to access desired memory location for read or write operation • Four high-order ECL level bits are also examined by memory protect logic as part of memory protect activity
PYW-W05-0 through PYW-W08-0	PE to MC	• Memory protect bits of memory address • Memory protect circuits on MC card examine these bits as part of memory protect activity

All MC logic is contained on a single printed circuit card.

2.4 INPUT/OUTPUT

This logic includes data drivers for sending read data to the IOSS or CUB or for sending transfer data to the CUB. It also includes receivers for accepting write data from the IOSS.

In addition, signal level conversion is provided by IO circuits for both incoming and outgoing signals. The CTμL logic levels of write data received from the IOSS is converted to the ECL levels required by the MLU. The ECL logic levels of read data and strobe signals being sent to the IOSS or CUB are converted to the corresponding CTμL levels. Transfer data and strobe signals being sent to the CUB are also converted from ECL to CTμL logic levels.

The IO logic is distributed among six cards, which are designated IO1 through IO6. Table 2-6 shows which data bits are routed to which IO cards.

Figure 2-6 provides a functional interface diagram of the six IO cards. Table 2-7 lists all signals that enter and leave the IO cards. These signals are defined in the glossary below.

MNEMONIC	SOURCE DESTINATION	DEFINITION
MCURTSL-1 MCURTSL-3	MC to IO (1-3) MC to IO (4-6)	• CUB output select These signals gate read or transfer data to the CUB • Both are true during transfer enable period of transfer cycle or output enable period of read cycle
MIOROSL-1 and MIOROSL-3	MC to IO (1-3) MC to IO (4-6)	• IOB output select enable • Gates read data through the IO logic to the IOSS • Occurs during the output enable period of read cycle if the IOSS has been identified as the destination
MIWIW00-1 through MIWIW63-1	IO(1-6) to MIR (1-8)	• IOB input data IOSS write data after level conversion to ECL by circuits on IO cards • Applied to PE/IO select gates on MIR cards • Data is valid from approximately 40 ns to 70 ns of a write cycle

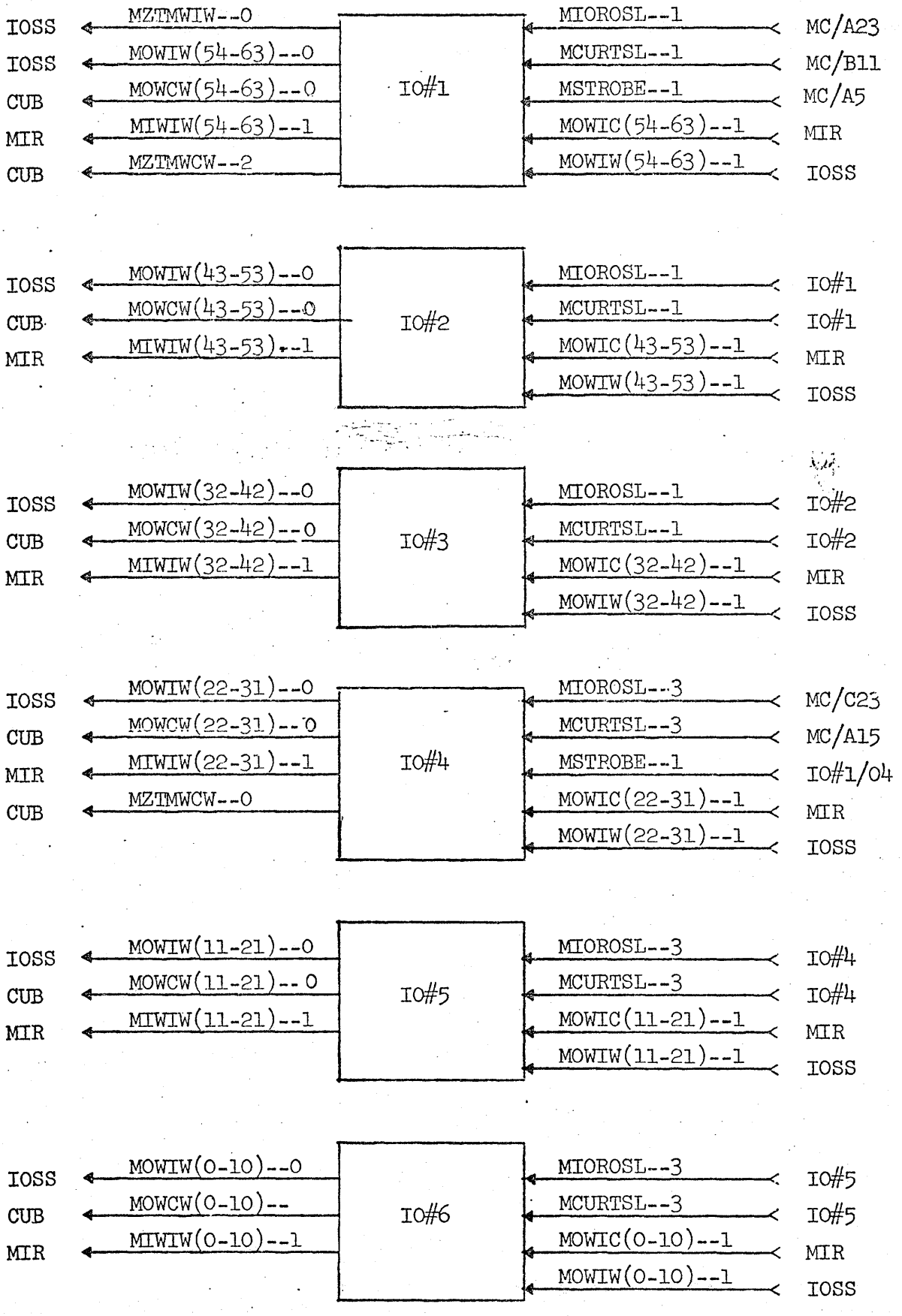


Figure 2-6 IO Card Functional Interface Diagram

Table 2-6. IO Card Organization

IO CARD NUMBER	IO#1	IO#2	IO#3	IO#4	IO#5	IO#6
BITS PER CARD	54-63	43-53	32-42	22-31	11-21	0-10
MLU CONNECTOR	J1	J2	J3	J4	J5	J6

MIOROSL--1
MCURTSL--1 are used by IO#1, 2, 3

MIOROSL--3
MCURTSL--3 are used by IO#4, 5, 6

MSTROBE--1 is used by IO#1, 4 only

Table 2-7. IO Card Input/Output Signal List

INPUT SIGNAL		OUTPUT SIGNAL	
NAME	SOURCE	NAME	DESTINATION
MIOROSL--1	MC/A23	MOWIW00--0	IOSS
MIOROSL--3	MC/C23	↓	↓
MCURTSL--1	MC/B11	MOWIW63--0	IOSS
MCURTSL--3	MC/A15	MOWCW00--0	CUB
MOWIC00--1	MIR#1-8	↓	↓
↓	↓	MOWCW63--0	CUB
MOWIC63--1	MIR#1-8	MIWIW00--1	MIR#1-8
		↓	↓
MOWIW00--1	IOSS	MIWIW63--1	MIR#1-8
↓	↓	MZTMWIW--0	IOSS
MOWIW63--1	IOSS	MZTMWCW--0	CUB
MSTROBE--1	MC/A5	MZTMWCW--2	CUB

MNEMONIC	SOURCE DESTINATION	DEFINITION
MOWCW00-0 through MOWCW63-0	IO(1-6) to CUB	• CUB output data • Read or transfer data sent to CUB from IO cards after conversion to CTuL levels by up converters on IO cards • Data becomes valid during output enable period of read cycle or during transfer enable period of transfer cycle
MOWIC00-1 through MOWIC63-1	MIR(1-8) to IO(1-6)	• CUB-IOB read/PE-CUB transfer data • Output of read/transfer select gates on MIR cards • Becomes valid as transfer data during transfer enable period of MLU cycle; becomes valid as read data during output enable period of MLU cycle
MOWIW00-0 through MOWIW63-0	IO(1-6) to IOSS	• IOB output data • CTL level read data sent to the IOSS • Data is gated out from IO cards during output enable period of read cycle • MOWIW-0 uses same bi-directional data lines as MOWIW-1 (IOSS write data)

MNEMONIC	SOURCE DESTINATION	DEFINITION
MSTROBE-1	MC to IO1,4	• IOB/CUB data strobe • Output of strobe flip-flop • Sent to up converters on IO cards for conversion to CTuL levels
MZTMWCW-0 and MZTMWCW-2	IO4 to CUB	• CUB output data strobe • Pair of strobes that allow CUB to accept read or transfer data • Gated out to CUB with read data during output enable period of MLU cycle or with transfer data during transfer enable period of MLU cycle
MZTMWIW-0	IO1 to IOSS	• IOB output data strobe • Strobe that allows IOSS to accept read data • Gated out to IOSS with read data during output enable period of MLU cycle

2.5 UP CONVERTER

All signals that leave the MLU for the PEM, CUB or IOSS (but not PE) are converted from ECL logic levels to CTuL levels. Since the ECL levels are relatively lower than the CTuL levels, the conversion is referred to as up conversion. There are three printed circuit cards in each MLU whose principal function is to perform up conversions. Table 2-8 matches those MLU output signals that are routed through the UC cards with their respective cards.

Table 2-8. Up Converter Organization

UC CARD NUMBER	UC1	UC2	UC3
ADDRESS BIT NUMBER	A5, A6 A9, AIO	A7, A8, A11 A12, A13	A14, A15
DATA BIT NUMBER	8 through 31	0 through 7 32 through 39	40 through 63
OTHER SIGNALS		Memory Initiate Write Outer Write Inner	

Some up conversion activity takes place on the IO Cards as well (refer to Section 2.4). Details regarding the need for signal level conversions in the MLU, both up and down, are provided in Section 3.0.

Figure 2-7 provides a functional interface diagram of the three UC cards. Table 2-9 lists all signals that enter and leave the UC cards. These signals are defined in the glossary that follows the table.

Table 2-9. UC Card Input/Output Signal List

UC CARD #	INPUT SIGNAL		OUTPUT SIGNAL	
	NAME	SOURCE	NAME	DESTINATION
1	PYW-W05--0	PE/J19	MYW-W05--0	PEM
	PYW-W06--0	PE/J19	MYW-W06--0	PEM
	PYW-W09--0	PE/J19	MYW-W09--0	PEM
	PYW-W10--0	PE/J19	MYW-W10--0	PEM
	MOWFW08--0	MIR2, 3,4/ J4, 5, 6	MOWFW08--1	PEM J22, 23
	MOWFW31--0	MIR2, 3,4/ J4, 5, 6	MOWFW31--1	PEM
2	PYW-W07--0	PE/J20	MYW-W07--0	PEM
	PYW-W08--0	PE/J20	MYW-W08--0	PEM
	PYW-W11--0	PE/J20	MYW-W11--0	PEM
	PYW-W12--0	PE/J20	MYW-W12--0	PEM
	PYW-W13--0	PE/J20	MYW-W13--0	PEM
	MOWFW00--0	MIR1/J8	MOWFW00-1	PEM J23
	MOWFW07--0	MIR1/J8	MOWFW07--1	PEM
	MOWFW32--0	MIR5/J7	MOWFW32--1	PEM J22
	MOWFW39--0	MIR5/J7	MOWFW39--1	PEM
	MINITPL--0	MC/A17	MINITPL--1	PEM
	MWOUTEN--0	MC/A29	MWOUTEN--1	PEM
	MWINNEN--0	MC/B32	MWINNEN--1	PEM
3	PYW-W14--0	PE/J21	MYW-W14--0	PEM
	PYW-W15--0	PE/21 J9, 10,11	MYW-W15--0 MOWFW40--1	PEM J23, 24
	MOWFW63--0	MIR6, 7,8/ J9, 10,11	MOWFW63--1	PEM

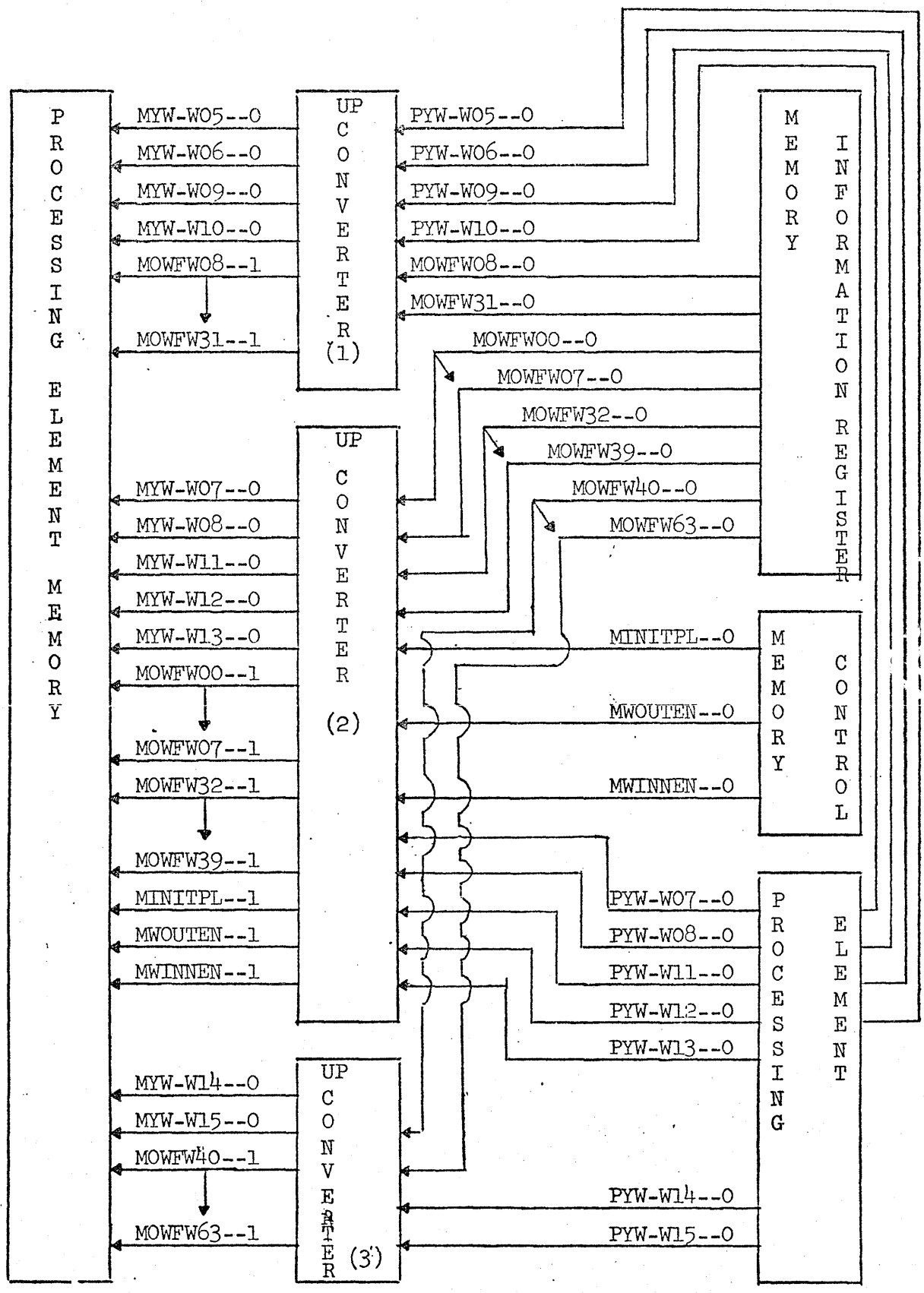


Figure 2-7 Up Converter Functional Interface Diagram

MNEMONIC	SOURCE DESTINATION	DEFINITION
MINITPL-0	MC to UC2	• Initiate memory-ECL • Will initiate read or write activity in PEM after level conversion by UC2 circuits • One clock period wide during read cycles; 50 ns wide during write cycles
MINITPL-1	UC2 to PEM	• Initiate memory - CTμL • CTuL level pulse used by PEM to initiate read or write cycle in PEM • One clock period wide during read cycles; 50 ns wide during write cycles • Width during read cycle (one clock period) is determined by frequency of CPU operation; example: for CPU frequency of 60.3 MHz, MINITPL-1 has approximately 62 ns duration • Occurs at approximately 30 ns of a read cycle; occurs at approximately 70 ns of a write cycle
MOWFW00-0 through MOWFW63-0	MIR(1-8) to UC(1-3)	• PEM write data - ECL Output of set (1) side of MIR latches • Data is sent to up converters for conversion from ECL to CTμL levels • Data becomes valid at approximately 70 ns of the write cycle

MNEMONIC	SOURCE DESTINATION	DEFINITION
MINITPL-1	UC2 to PEM	• Initiate memory - CTμL • CTμL level pulse used by PEM to initiate read or write cycle in PEM • One clock period wide during read cycles; 50 ns wide during write cycles • Width during read cycle (one clock period) is determined by frequency of CPU operation; example: for CPU frequency of 60.3 MHz, MINITPL-1 has approximately 62 ns duration • Occurs at approximately 30 ns of a read cycle; occurs at approximately 70 ns of a write cycle
MOWFW00-0 through MOWFW63-0	MIR(1-8) to UC(1-3)	• PEM write data - ECL Output of set (1) side of MIR latches • Data is sent to up converters for conversion from ECL to CTμL levels • Data becomes valid at approximately 70 ns of the write cycle
MWINNEN-0	MC to UC_2	• Write inner enable - ECL • Output of MC decode logic whenever inner word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTμL level

MNEMONIC	SOURCE DESTINATION	DEFINITION
MWINNEN-0	MC to UC_2	• Write inner enable - ECL • Output of MC decode logic whenever inner word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTμL level
MWINNEN-1	UC_2 to PEM	• Write inner enable - CTuL • CTμL level that enables the PEM to write inner word of PEM data (bits 8 through 39) • Signal is valid from approximately 60 ns to 210 ns of write cycle
MWOUTEN-0	MC to UC_2	• Write outer enable - ECL • Output of MC decode logic whenever outer word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTμL level
MWOUTEN-1	UC_2 to PEM	• Write outer enable - CTμL • CTuL level that enables the PEM to write inner word of PEM data (bits 0 through 7 and 40 through 63) • Signal is valid from approximately 60 ns to 210 ns of write cycle

MNEMONIC	SOURCE DESTINATION	DEFINITION
PYW-W05-0 through PYW-W15-0	PE to UC(1-3)	• PE memory address register bits • ECL level address bits sent from PE to up converters for conversion to CTuL levels • CTuL levels to be used by PEM to access desired memory location for read or write operation • Four low-order ECL level bits are also examined by memory protect logic as part of memory protect activity

SECTION 3.0

SUMMARY OF MLU LOGIC CHARACTERISTICS

All MLU logic circuits belong to the emitter-coupled logic (ECL) family. The basic ECL gate configuation is shown in Figure 3-1. Although several other ECL circuits are in use in the MLU, this circuit helps illustrate some of the general ECL characteristics discussed below.

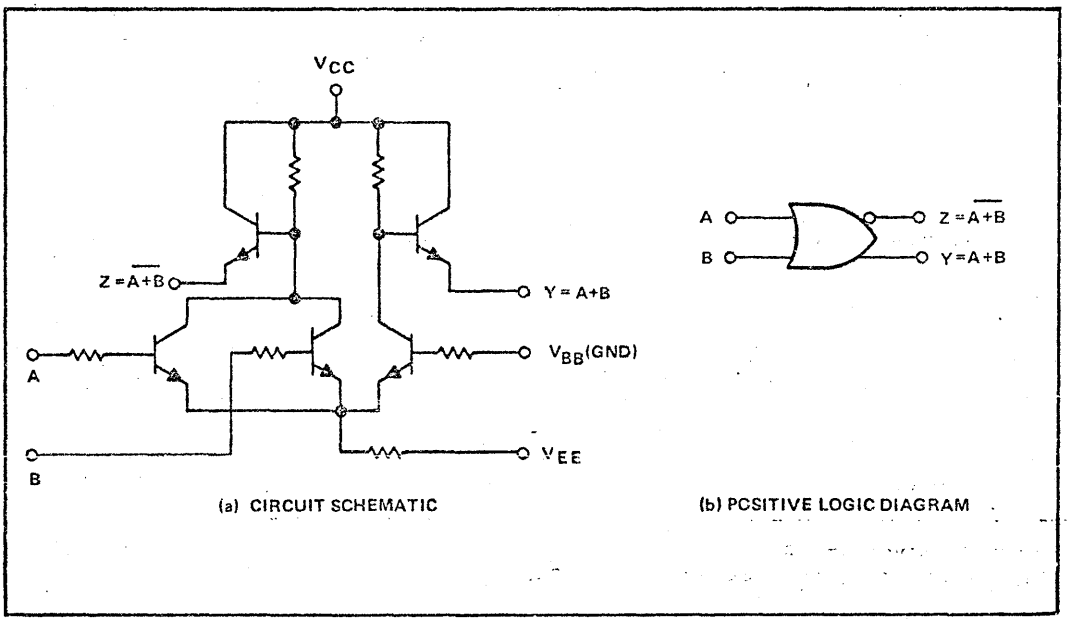


FIGURE 3-1. Basic ECL Gate

3.1 ECL CHARACTERISTICS

- LOGIC LEVELS*

Typical logic levels employed by the basic ECL gate are 400 mV and -400 mV, when V_{cc}=1.32V, V_{EE}=-3.2V and V_{REF}=0V. Minimum levels when operating at 25°C and loaded with 50 ohms to ground and 270 ohms (pulldown) to -3.2V are ±350mV. These logic levels are ensured with inputs at ±200mV, which provide 150mV of dc noise margin. Since the actual threshold is approximately 150mV and typical output levels are

*Information is taken from The Integrated Circuits Catalog, Texas Instruments Incorporated, Dallas, p. 4a-7.

400mV, typical noise margin in excess of 200 mV can be expected. Transfer characteristics for the basic gate are shown in Figure 3-2.

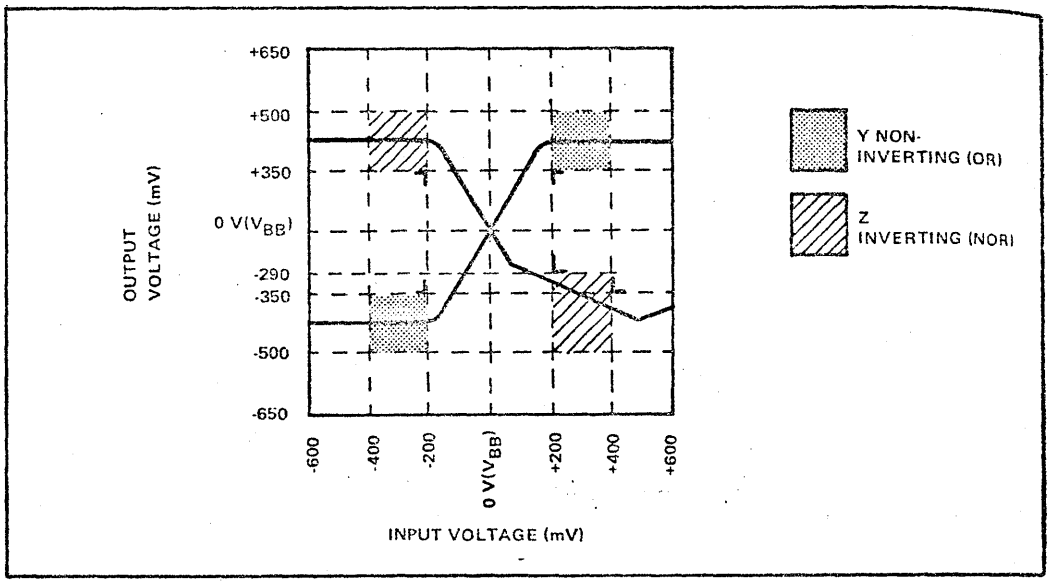


FIGURE 3-2. Transfer Characteristics of Basic ECL Gate

For gating functions which have emitter dots (wired OR), the relative-high level is increased to 450mV; the relative-low level is also increased by 50mV to -350mV.

Because the MLU must communicate with certain ILLIAC IV system elements that employ CTμL circuits, the MLU logic includes signal level converters. These converters use both ECL and CTμL logic levels for their operation. CTμL levels are 2.5V and -0.5V. Details regarding level conversion in the MLU are provided in Section 3.3, below.

- LOGIC CONVENTION

In general, MLU logic elements are seen as performing negative logic functions. For this reason, the more negative signal values (-400 mV

for ECL and -500mV for CTμL) are considered the logical ONE levels and the more positive signal values (400mV for ECL and +2.5V for CTμL) are considered the logical ZERO levels.

Some exceptions to this rule are the signals that reset the RS flip-flops in the MC logic and those signals sent to up converters before leaving the MLU. These signals are actually high-true. The signal mnemonics assigned to these exceptions take this into account. Suffixes to their mnemonics indicate that, while the circuits generating these signals are classified as negative logic gates because they are part of the MLU, the signals are active when high.

- GATE SPEED*

  Switching time performance at 25°C, with various capacitive loadings, is described in Figure 3-3. This capacitive loading is directly relatable to ac fan-out, assuming 4 to 5 pF per gate input. Delay time degradation with increasing fan-out approximates 75 ps per additional load. Switching-time waveform definitions and output terminations used for testing are shown in Figure 3-4. Typical propagation time through a single ECL gate is 4ns from leading edge to leading edge and 4ns from trailing edge to trailing edge. Corresponding values for propagation through single CTμL gate are 12ns and 12ns.

*Information is taken from The Integrated Circuits Catalog, Texas Instruments Incorporated, Dallas, Texas, pp. 4a-10, 4a-11.

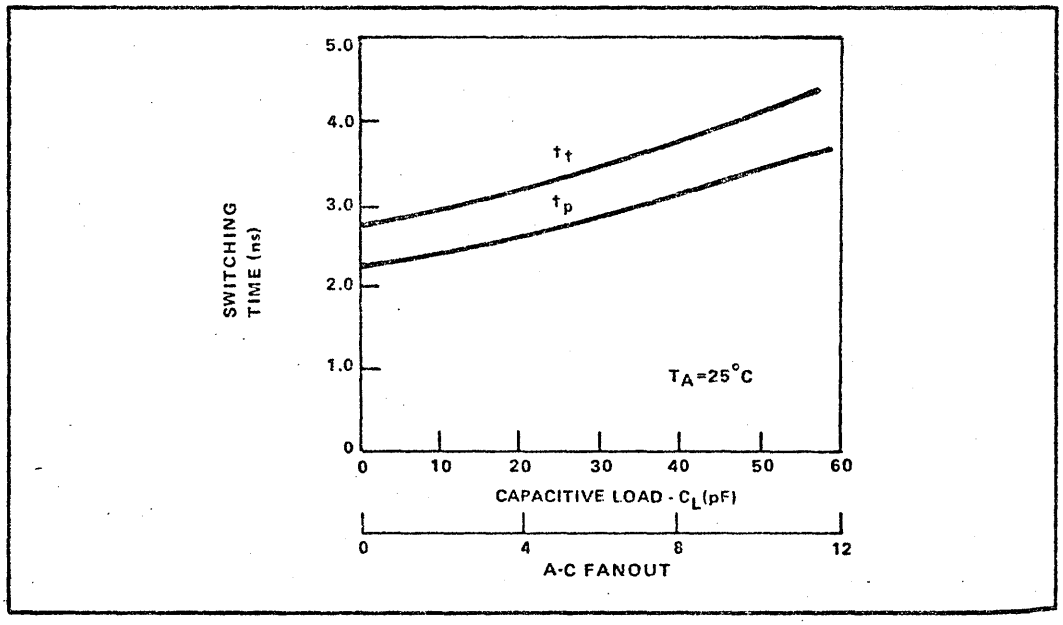


FIGURE 3-3. Switching Time vs. Loading

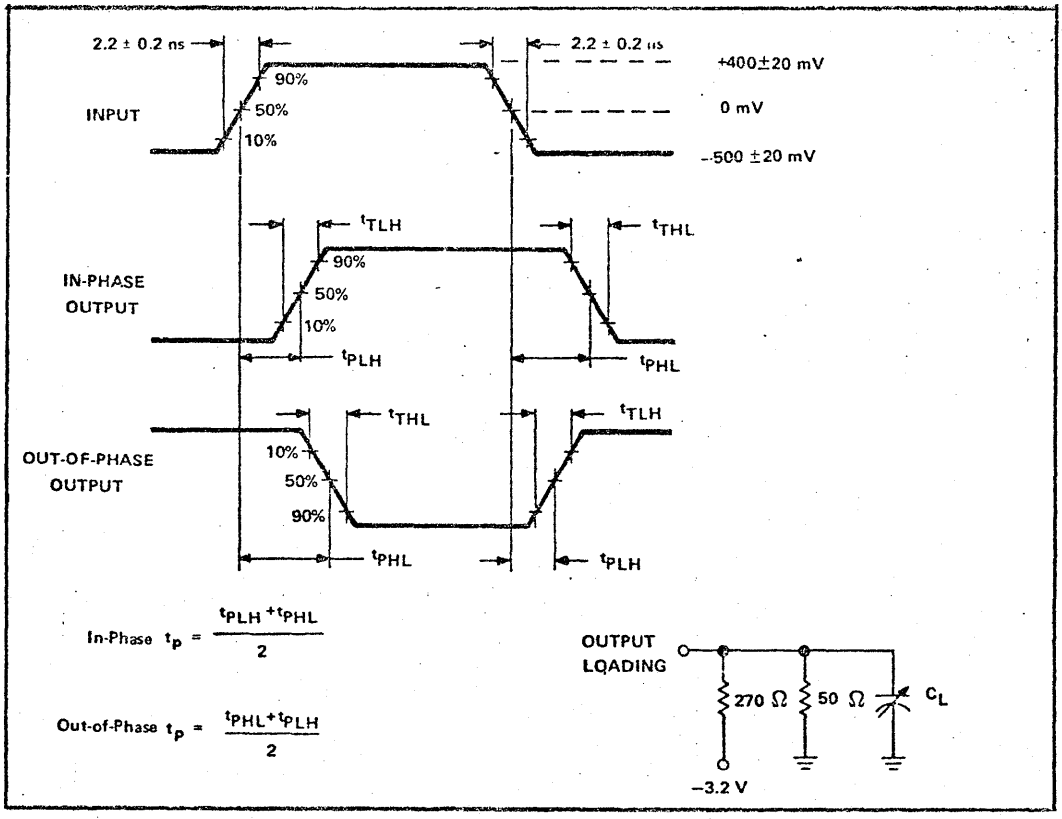


FIGURE 3-4. Switching-Time Waveforms

- NONSATURATION

ECL circuits operate in the nonsaturated mode. That is, the transistors in each gate are never fully cut off or in a saturated state. This is the chief reason for the high switching speed that is characteristic of these circuits. Because the transistors are always conducting, even when the inputs to the gate are false, the inputs do not have to pass a threshold before the logic decision is made. Since the output transistor does not have to be saturated for the output signal to be considered true, there is no switching delay caused by the need to overcome capacitance in the output transistor. For both of these reasons, the output of an ECL gate is able to follow the inputs almost immediately.

- COMPLEMENTARY OUTPUTS

Many integrated circuit packages included in the ECL family provide dual, complementary outputs. This results in the AND/NAND, OR/NOR and AND-OR/NOR functions illustrated in Figure 3-5. Propagation time through these circuits is the same for both outputs (both outputs become valid at the same time).

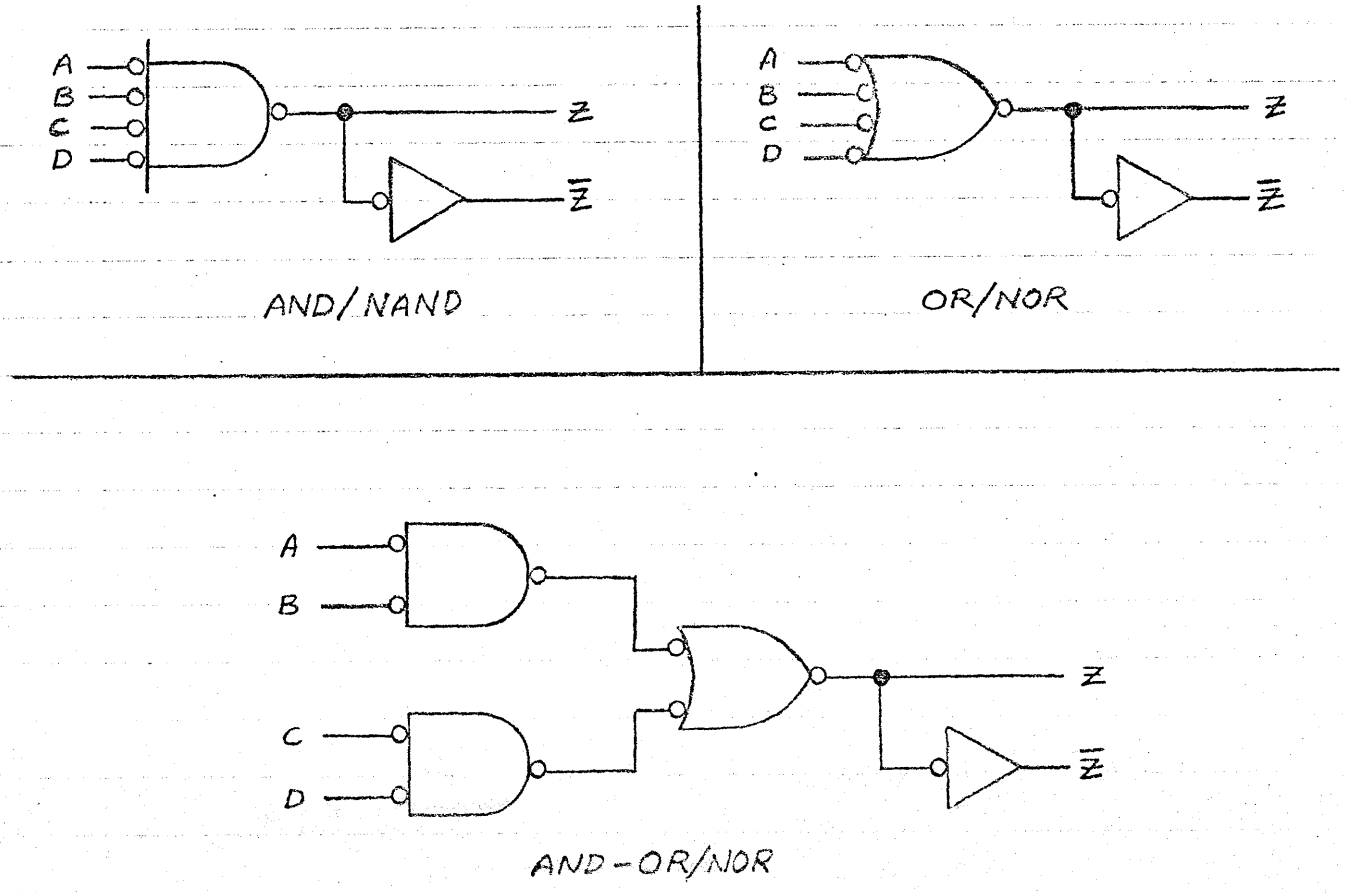


FIGURE 3-5. ECL Logic Functions with Dual Outputs

- POWER SUPPLY REQUIREMENTS

The MLU logic circuits require the following voltages and currents for proper operation:

A. 1.32V ± 2% } 20 amp, maximum
B. 4.8V ± 10% }

C. -3.20V ± 2%, 24 amp, maximum

D. 0.0V, ground current will vary between ± 10 amp

Details regarding the source of this power and the establishment of logic ground are provided in Section 5.0, POWER DISTRIBUTION.

3.3 LOGIC LEVEL CONVERSION

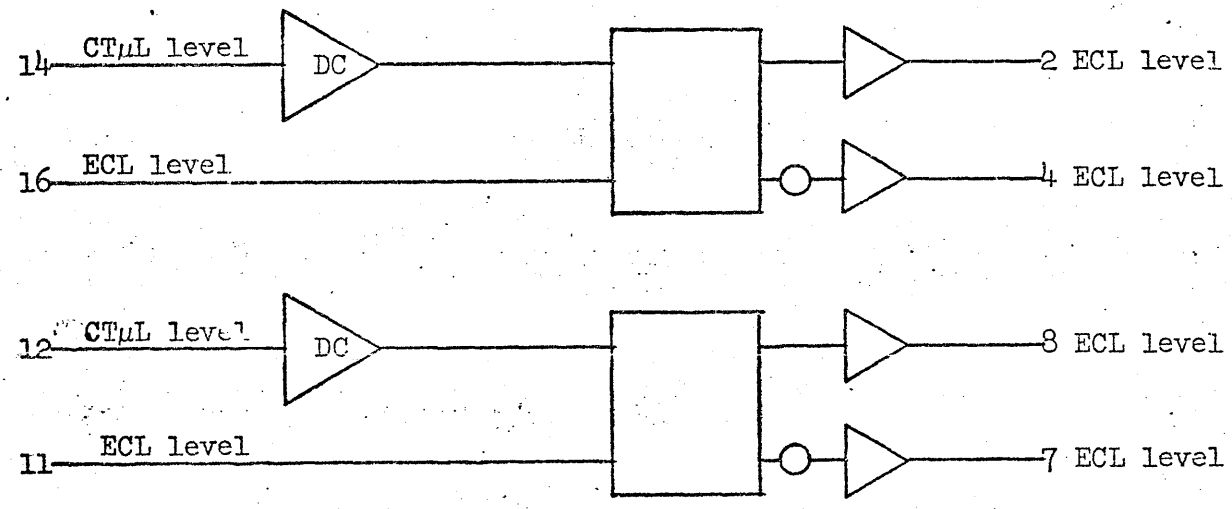
The PEM and IOSS both interface with the MLU through CTμL circuits. For this reason, the MLU is obliged to convert downward the CTμL levels it receives from these units to corresponding ECL levels and convert upward the ECL levels of those signals it must send these units. The necessary down converters and up converters are included at appropriate points in the data paths through the MLU. Table 3-1 identifies the level conversions that occur when information is sent between various subunits of the system.

SIGNAL SOURCE	SIGNAL DESTINATION	TYPE OF CONVERSION	UP/DOWN	LOCATION OF CONVERSION ELEMENT	REMARKS
PEM	PE	CT L to ECL	Down	MIR Cards	
PEM	IOSS	CT L to CT L	Down, then up	MIR Cards, then I/O Cards	
PEM	CUB	CT L to ECL	Down, then up	MIR Cards, then I/O Cards	CUB finally converts to ECL
PE	PEM	ECL to CT L	Up	UC Cards	
PE	CUB	ECL to ECL	Up	I/O Cards	CUB reconverts to ECL
IOSS	PEM	CT L to CT L	Down, then up	I/O Cards, then UC cards	

Table 3-1 LOGIC LEVEL CONVERSION

Read and transfer data destined for the CUB is converted to CTμL levels at the IO cards even though the CUB uses ECL levels. This is required because the CUB read and transfer data is routed through the same set of IO logic that provides conversion to CTμL levels for the IOSS read data. The CUB is therefore obliged to reconvert the CTμL levels it receives from the IO cards to ECL levels.

Figure 3-6 illustrates the gate configuration for the down converter circuit.



Pin 3,6 = V_{CC} = +1.32V

Pin 5 = V_{CL} = +4.8V

Pin 10 = V_{EE} = -3.2V

Pin 13 = HIGH LOGIC LEVEL GROUND (Reference Ground of the CTμL device)=0.0V

Pin 1,9 = ECL GROUND (V_{REF}) = 0.0V

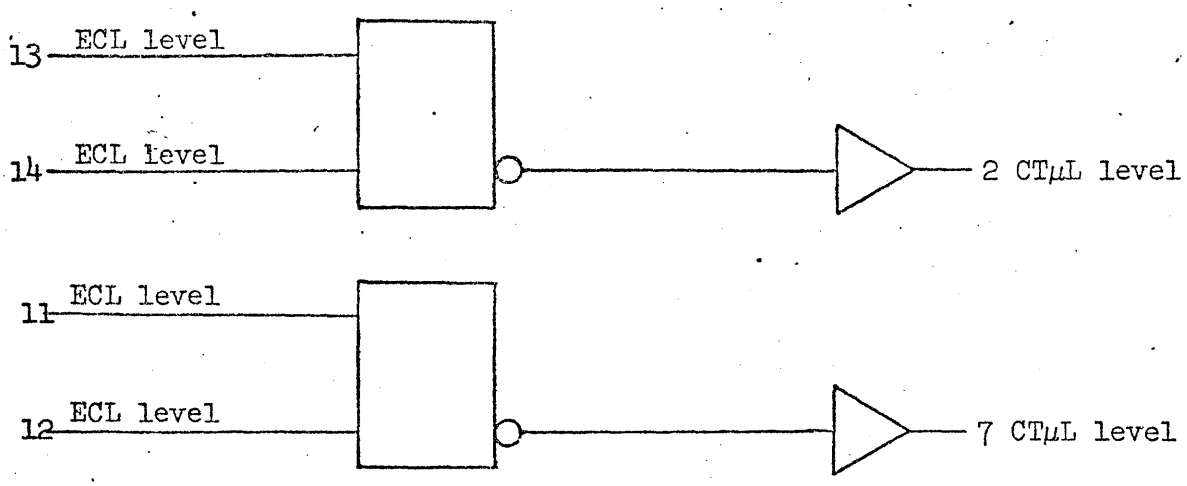
+2.5V is applied on Pin 14, 12 and +.4 on Pin 16, 11 and the output Pin 2, 8 can be +.4V

or -.5V is applied on Pin 14, 12 and -.4V on Pin 16, 11 and the output Pin 2, 8 can be -.4V

For more information see MIR drawing 1727 9084.

FIGURE 3-6. Down Converter Block Diagram

Figure 3-7 shows the gate configuration for the up converter circuit.



Pin 5 = V_{CC} = +4.8V

Pin 10 = V_{EE} = -3.2V

Pin 9, Pin 16 } = GROUND

+.4V is applied on Pin 13, 11 and/or Pin 14, 12 and the output Pin 2, 7 can be on -.5V

or -.4V is applied on Pin 13, 11 and/or Pin 14, 2 and the output Pin 2, 7 can be on +2.5V

FIGURE 3-7. Up Converter Block Diagram

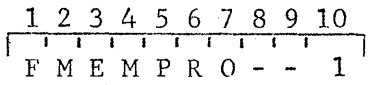
SECTION 4.0

THEORY OF OPERATION

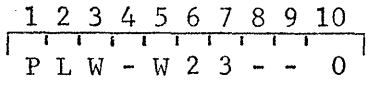
There are three types of ILLIAC IV operations that involve the MLU: write memory cycles, read memory cycles and transfer cycles. All three require the movement of data from some source external to the MLU, through the MLU, to some destination external to the MLU. The MLU multiplexes the various data paths and, for write and transfer cycles, temporarily stores the data being moved. The three MLU cycles are described in detail in the following subsections.

Before considering the detailed theory, however, it would be helpful to examine the rules followed for establishing signal mnemonics. These mnemonics are used extensively in the theory discussion and are not open to easy interpretation. The following examples illustrate the rules governing MLU mnemonics as they are discussed below.

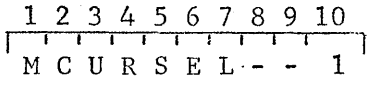
EXAMPLES:



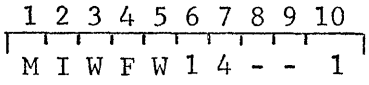
Source - CU via PE
Function - Memory Protect
Logic 1 - Relative Low



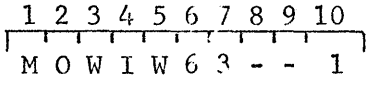
Source - PE
Function - Write Data - Bit 23
Logic 1 - Relative High



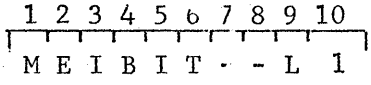
Source - MLU
Function - CUB Read Select
Logic 1 - Relative Low



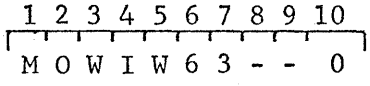
Source - PEM
Function - PEM Read Data - Bit 14
Logic 1 - Relative Low



Source - IOSS
Function - IOSS Write Data - Bit 63
Logic 1 - Relative High



Source - MLU
Function - Latched E1 Bit
Logic 1 - Relative Low



Source - MLU
Function - IOSS Read Data - Bit 63
Logic 0 - Relative High

The mnemonic format allows for 10 characters. The first character position contains one of three letters: F, M or P. Letter P indicates that the source of the signal is the PE. The letter M is used for all signals originating in the MLU. It is also used for read data received from the PEM and write data received from the IOSS. Letter F is used to indicate that the signal originates at the Final Station of the CU (FINST) and that it is sent to the MLU through the PE.

The signal function is designated by the next series of letters, usually character positions 2 through 7. For data and address bits this series ends with a pair of numbers that identifies the bit position in the data or address word.

The mnemonic is completed by one or two characters in the last position (s). If the mnemonic is terminated by two characters, the letter L in character position 9 indicates that the signal is the output of a latch.

The last character identifies which signal level, relative-high or relative-low, is considered the active or true level. However, the interpretation of this character depends on whether the source of the signal follows the positive logic or negative logic convention.

The write data, address and E-bit inputs to the MLU use positive logic notation. All other signals discussed in this section follow negative logic convention; these include read data sent to the MLU from the PEM, initiate and control information provided by the PE, MLU output signals and all internal MLU signals.

If the last character of a positive logic mnemonic is a 1, the signal is considered true when it is high; if the last character is 0, the signal is considered true when it is low. The opposite interpretation is made for negative logic mnemonics. If the last character is a 1, the signal is low-true; if the negative logic mnemonic ends with a 0, the signal is high-true. Table 4-1 provides a summary comparison of positive and negative logic mnemonics.

Table 4-1. Positive/Negative Logic Mnemonics

Input/Output Subsystem (IOSS)			Processing Element (PE)			Memory Logic Unit (MLU)		
Signal Name	Level	Logical	Signal Name	Level	Logical	Signal Name	Level	Logical
MOWIWXX--1	High	1	PLW-WXX--1	High	1	MOWFWXX--1	High	0
MOWIWXX--1	Low	0	PLW-WXX--1	Low	0	MOWFWXX--1	Low	1
			PLW-WXX--0	High	0	MOWFWXX--0	High	1
			PLW-WXX--0	Low	1	MOWFWXX--0	Low	0

There are a few signal pairs in which the signals are identical; the mnemonics in each pair are also identical, except for the last character. Where one signal in the pair ends with a 1, the other signal ends with a 3 to distinguish it from the first. A mnemonic ending with 0 will be paired with a mnemonic ending with a 2. The 3 and the 2 have the same meaning as the 1 and 0, respectively.

4.1 WRITE MEMORY CYCLE

During a write memory cycle, data is written into an addressed location in the PEM. The source of the data may be the CU, the PE or the IOSS.

As shown in Figure 1-1, the CU-to-PEM data path enters the MLU through the PE; consequently, CU-to-PEM data follows the same path through the MLU as PE-to-PEM data. For this reason, specific references to PE write activity apply equally to CU write activity, except where otherwise noted. These references include hardware and signal nomenclature.

A write cycle begins with the arrival at the MLU Memory Control (MC) logic of the memory select signal, FMSEL-1, and the initiate memory cycle signal, FIMC-1. Together, these signals provide the memory timing initiate pulse, MIMCTNP-1. This pulse is sent to the memory timing logic where it initiates the sequence of timing pulses used to control MLU activity during the memory cycle.

The read/write control signal, FREAD-1, will be false (relative-high) at this time; this signal level conditions various MC circuits for a write operation.

The 11 address bits, PYW-W05-0 through PYW-W15-0, are also received from the PE at this time. These bits are routed to the PEM via the UP Converter (UC) logic, where the ECL levels provided by the PE are converted to CTμL levels for use in the PEM. The address bits are decoded by the PEM to select one 64-bit storage location out of 2048 storage locations in the PEM.

- MEMORY PROTECT

  Address bits PYW-W05-0 through PYW-W08-0 are also sent to memory protect logic on the MC card where they are examined for logical ONE's

MEMORY PROTECT continued

whenever the PE decides to protect a certain portion of the PEM storage locations from unauthorized write operations.

The PE may protect the 128 lowest order PEM addresses by issuing the memory protect signal FMEMPRO-1. This low-level signal enables memory protect logic on the MC card to detect addresses 0000 through 0127 (decimal). If FMEMPRO-1 is true (relative-low) and address bits PYW-W05-0 through PYW-W08-0 are all false (relative-high), the memory protect circuits inhibit the write enable circuits and set the memory protect error latch. This is a status report latch only and does not inhibit subsequent write operations. The CU resets the memory protect error latch with the error reset signal, FRMPRO-0.

- MEMORY INITIATE PULSE (MINITPL--0)

If no memory protect error is detected, a memory initiate pulse is sent from the MC to the PEM to activate the PEM memory cycle logic (see Figure 4-1).

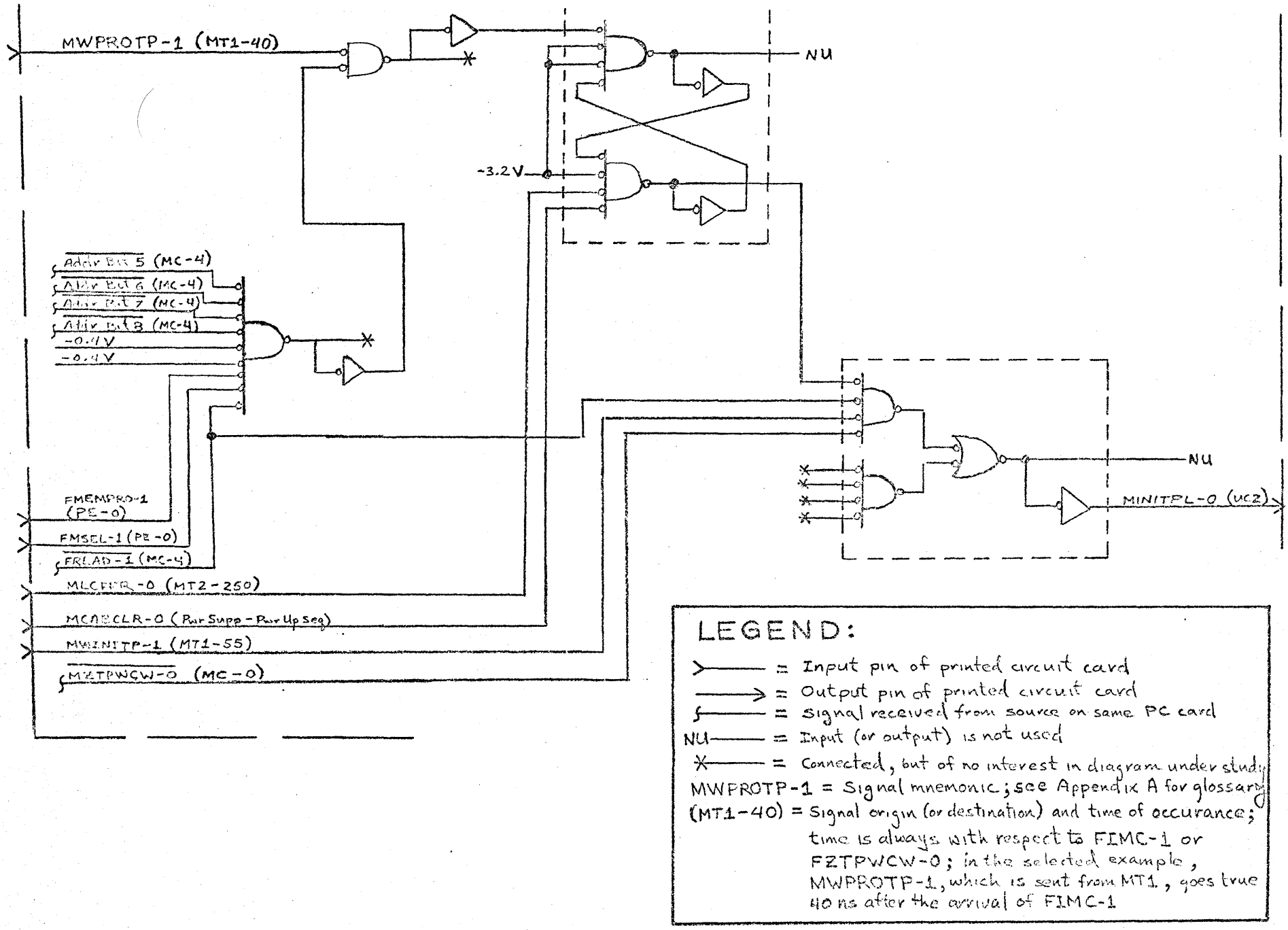


Figure 4-1. Memory Initiate Pulse Logic

MEMORY INITIATE PULSE continued

This pulse results from the ANDing of four conditions:

1. The read/write control signal, FREAD-1 is false
2. The write enable flip-flop is set; this flip-flop is normally set but will be reset by a memory protect error condition
3. The transfer flip-flop is not set
4. A write initiate pulse, MWINITP-1, is received from MT1; this pulse is generated as a result of the MT1 delay line receiving the memory initiate timing pulse, MIMCTNP-1. It occurs approximately 75 ns after FIMC-1 arrives at the MC card. The generation of MWINITP-1 is shown in Figure 4.2.

-NOTE-

This timing pulse is used to delay the generation of the memory initiate pulse to give the memory protect logic time to complete its analysis of the low order address bits. This delay is not used for read operations.

The memory initiate pulse is first sent to the UC as MINITPL-0. There, its relative-high ECL level is converted (and inverted) to a relative-low CTuL level. This low level pulse is then sent to the PEM as MINITPL-1.

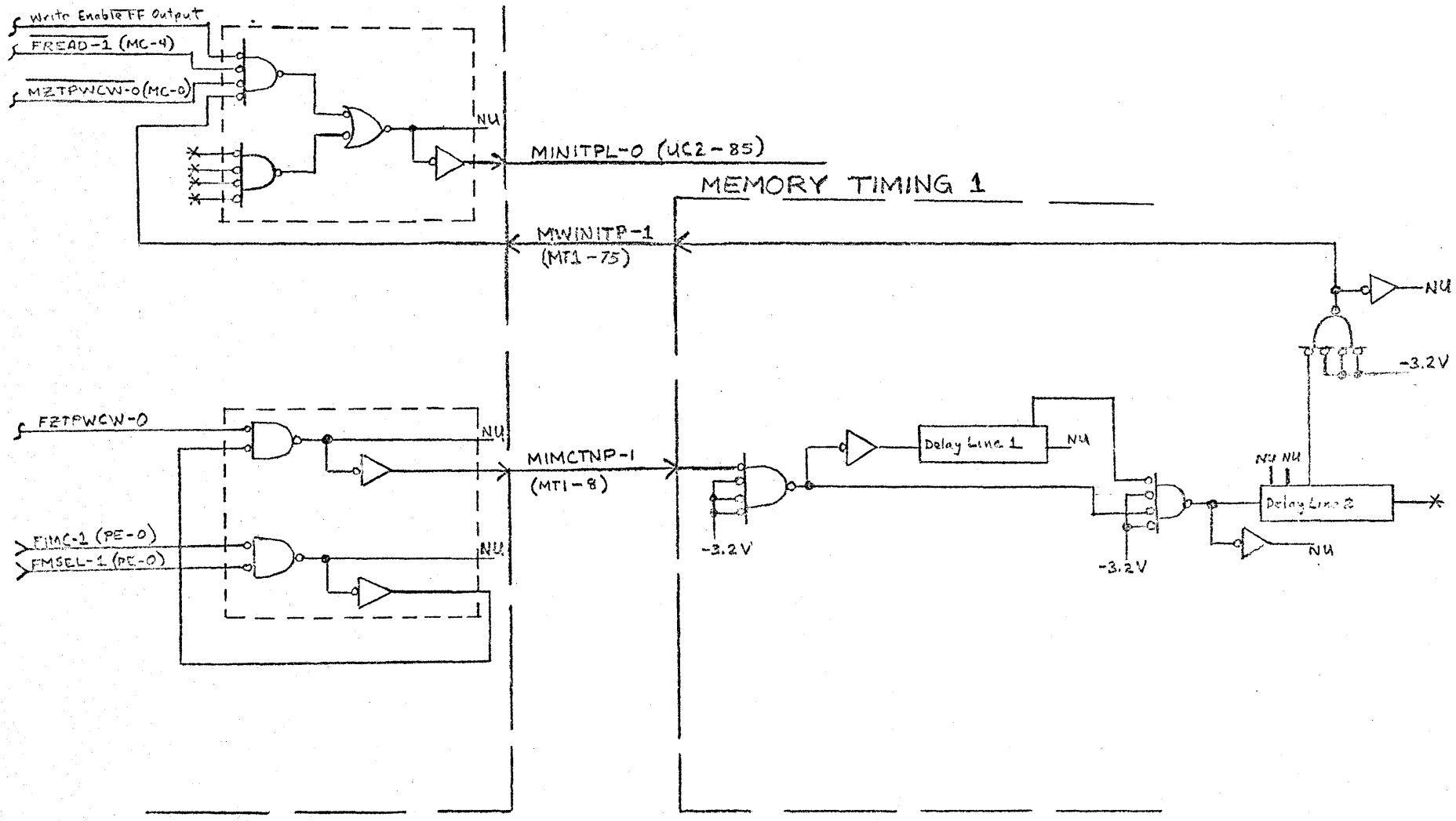


Figure 4-2. Write Initiate Pulse Logic

WRITE ENABLE

In addition to the memory initiate signal, the MC logic provides the PEM with one or both of a pair of write enable signals, MWOUTEN-0 and MWINNEN-0. One signal enables write logic in the PEM to store the outer 32 bits of data (bits 00 through 07 and 40 through 63) in the addressed storage location; the other signal enables the PEM to store the inner 32 bits of data (bits 08 through 39). If both signals are present all 64 bits will be written into the addressed storage location. During write operations, the selective generation of write enable signals depends on two considerations: the origin of the write operation and, if the PE is the origin, by a pair of bits issued by the CU through the PE. Generation of write enable signals is shown in Figure 4-3.

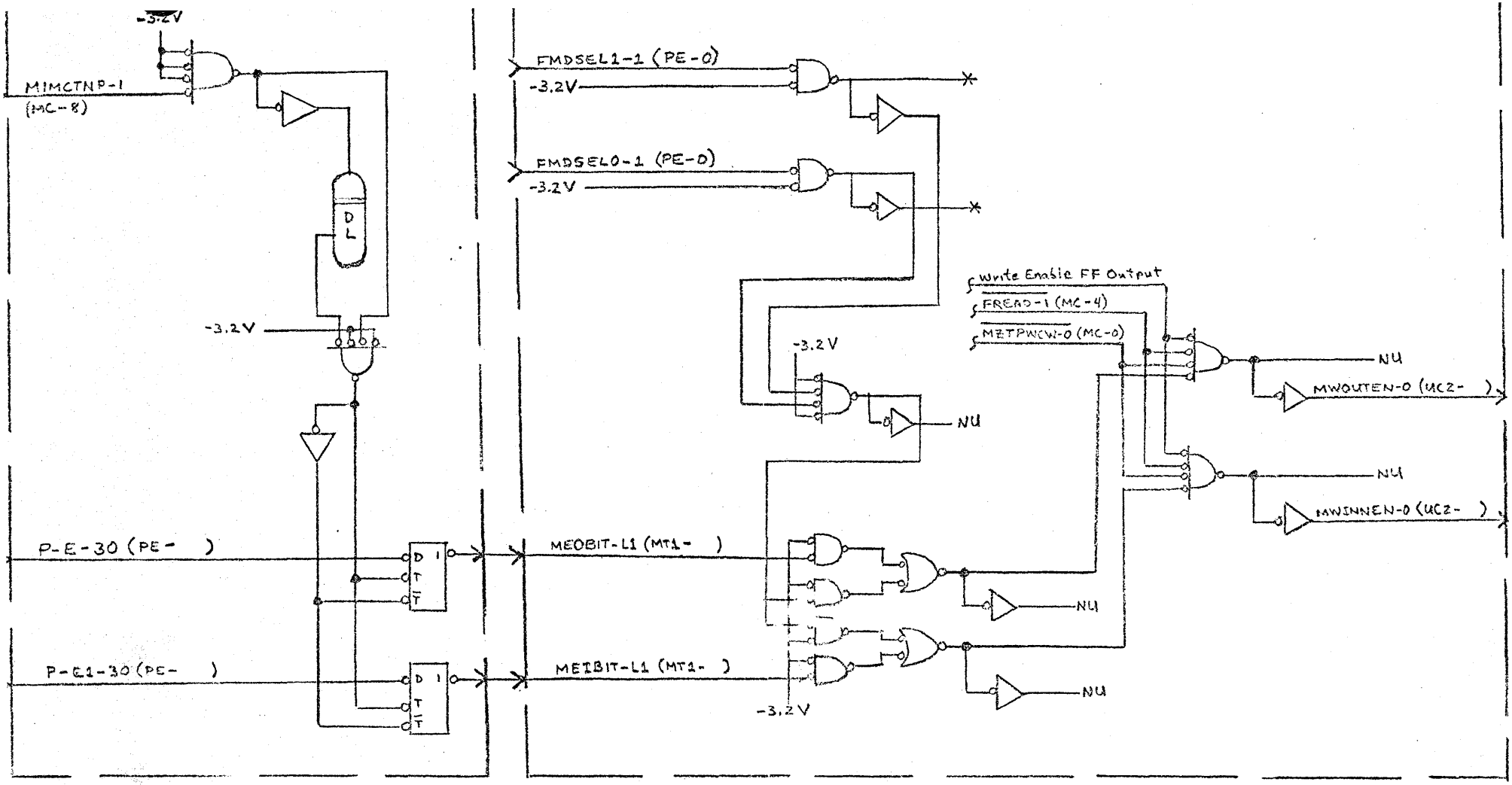


Figure 4-3. Write Enable Pulse Logic

WRITE ENABLE continued

During write operations initiated by the PE, the PE sends the MLU a pair of data control bits, P-E-30 and P-1-30, to a pair of latches on the Memory Timing 1 (MT1) card. A low level on one of these lines will set the corresponding E-bit latches. The outputs of the two E-bit latches, MEOBIT-L1 and MEIBIT-L1, are sent to the MC logic where they influence the generation of the write enable signals. P-E-30 controls the generation of MWOUTEN-0 through the MEOBIT latch and P-1-30 controls the generation of MWINNEN-0 through the MEIBIT latch.

If the CU or IOSS initiates the write operation, both write enable signals are generated regardless of the states of the E-bit latches. The outputs of these latches can be overridden by a pair of memory data select signals, FMDSEL0-1 and FMDSEL1-1, whose function is to identify the source of data during write memory cycles and the destination of data fetched from the PEM during read memory cycles.

When these signals identify the CU or the IOSS as the origin of a write operation, both write enable signals are forced to the true state (relative-high) regardless of the states of the E-bit latches. The binary codes for the memory data select signals are defined in Table 4-2 for read and write operations. These two signals originate in FINST and are fed into the MLU through the PE.

Table 4-2. Memory Data Select Signals Bit Combinations

BIT COMBINATION		WRITE MEMORY CYCLE (Source of Data)			READ MEMORY CYCLE (Destination of Data)		
FMDSEL0-1	FMDSEL1-1	PE	IOSS	CU	PE	IOSS	CUB
0 (H)	0 (H)	--	---	X	--	--	--
0 (H)	1 (L)	--	---	--	--	--	X
1 (L)	0 (H)	--	X	--	--	X	--
1 (L)	1 (L)	X	---	--	X	--	--

WRITE DATA PATHS

Write data received from the PE enters the MLU at the PE/IO select gates, which are located on the Memory Information Register (MIR) cards. Figure 4-4 illustrates the PE and IOSS write data paths. Remember that CU write data uses the PE write data path through the MLU.

Write data from the IOSS enters the MLU at the six IO interface cards. These cards contain line receivers for accepting write data from the IOSS and down converters for adapting the CTuL signal levels of the incoming data to the ECL levels used by the MLU. The IO logic also includes line drivers and up converters for forwarding read data to the IOSS and a separate set of line drivers and up converters for sending read or transfer data to the CUB.

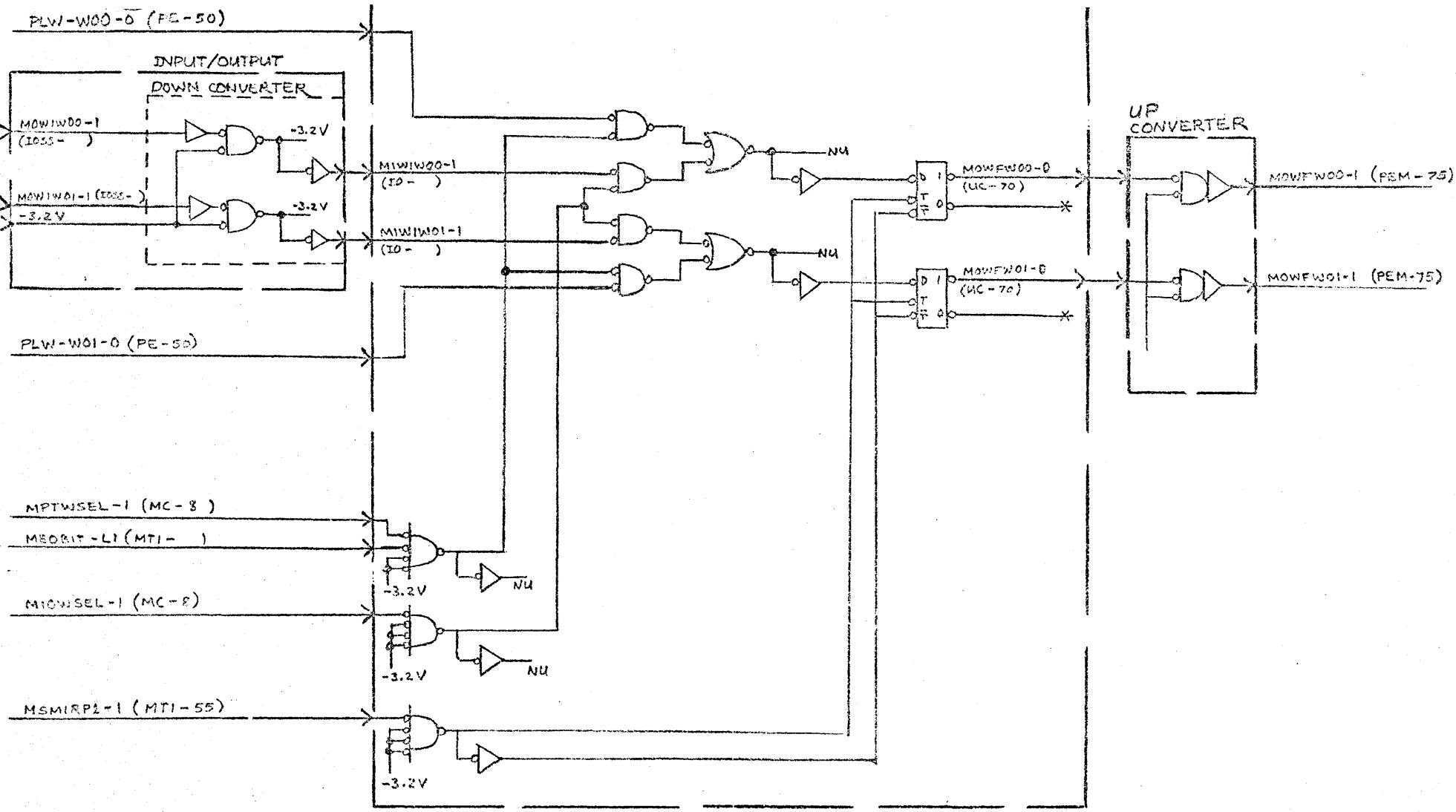


Figure 4-4. PE and IOSS Write Data Paths

WRITE DATA PATHS continued

The IO interface logic sends the IOSS write data on to the PE/IO select gates on the MIR cards as soon as it is received; no gating of IOSS write data takes place at the IO cards.

There are 64 sets of PE/IO select gates, eight sets on each of the eight MIR cards. In effect, the PE/IO select gates multiplex data received from two sources, the PE and the IOSS (via the IO cards). The output of each select gate is taken from its NOT side; consequently, the select gates also invert the selected data. Each select gate output is applied to the data input of an MIR latch located on the same MIR.

The eight PE/IO select gates on each MIR card multiplex one byte of data. Table 2-2 matches the eight data bytes with their respective MIR cards. This table also shows that wiring for the data path into and out of the MIR cards takes into account the inner word and outer word data formats used in the 32-bit mode; all bytes in the outer word are routed as a contiguous group.

Data originating at the PE or CU arrives at the select gates from the PE as PLW-W00-0 through PLW-W63-0. Data originating at the IOSS arrives at the select gates from the IO cards as MIWIW00-1 through MIWIW63-1. Data select signals developed on each MIR card determine which set of data will be gated through to the MIR latches.

WRITE DATA PATHS continued

IOSS data is selected by the input/output buffer (IOB) write select signal, MIOWSEL-1. This signal originates at the MC card and is true (relative-low) when:

A. The memory data select signals, FMDSEL0-1 and FMDSEL1-1, identify the IOSS as the source of the write operation.

B. The read/write control signal, FREAD-1, identifies the memory cycle as a write operation (relative-high).

C. The transfer cycle flip-flop is reset, indicating that a transfer cycle is not in progress.

The MC logic sends MIOWSEL-1 to all eight MIR cards. A noninverting driver on each MIR card forwards MIOWSEL-1 to the PE/IO select gates. If MIOWSEL-1 is true (relative-low), MIWIW00-1 through MIWIW63-1 will be inverted and applied to the data inputs of the MIR latches.

Data received from the PE is gated through the select gates as two separate half words: the outer word (bits 00-07 and 40-63) and the inner word (bits 08-39). The data select signal that gates the outer word results from ANDing the PE write/PE-CUB transfer select signal, MPTWSEL-1, with the latched E-bit signal, MEOBIT-L1. This ANDing occurs on MIR cards 1, 6, 7 and 8. The inner word gating signal results from ANDing MPTWSEL-1 and MEIBIT-L1 on MIR cards 2 through 5. In this way, the states of the E-bit latches also control the gating of the inner and outer words to the MIR latches during PE write operations.

Shortly after the data (PE/CU or IOSS) is made available to the MIR latches, a pair of complementary strobes are generated on each MIR card to clock the data into the latches. Each strobe pair is derived from one of eight MIR strobe pulses, MSMIRP1-1 through MSMIRP8-1, which are provided by delay lines on either MT1 or MT2.

From this point in the data flow (from the MIR latches on), the IOSS and PE/CU data paths coincide. The true outputs of the MIR latches are sent to the UC logic as MOWFW00-0 through MOWFW63-0 for conversion to CTTL levels and a second inversion.

WRITE DATA PATHS continued

The 64 data bits are distributed among the three UC cards in the following groups:

- UC1 - bits 08 through 31
- UC2 - bits 00 through 07 and 32 through 39
- UC3 - bits 40 through 63

The data is sent from the UC logic directly to the PEM for storage in the addressed location.

4.2 READ MEMORY CYCLE

During a read memory cycle, data is fetched from an addressed location in the PEM. The destination of the read data can be the CUB, the PE or the IOSS.

A read cycle begins, like a write cycle, with the arrival at the MLU of the memory select signal, FMSEL-1, and the initiate memory cycle signal, FIMC-1. The MC logic ANDs these signals to generate the memory timing initiate signal, MIMCTNP-1, which is then sent to the MT1 card. This signal initiates the sequence of timing pulses that are used to control read cycle activity.

- MEMORY INITIATE PULSE

The signals, FMSEL-1 and FIMC-1, are also ANDed with the read/write control signal, FREAD-1, which must be true (relative-low) at this time. The result of this ANDing is the memory initiate pulse, MINITPL-0. This pulse is used to activate memory cycle logic in the PEM. First, it is sent as a relative-high ECL level to the UC logic. There, it is converted and inverted to a relative-low CTμL level and sent to the PEM as MINITPL-1.

The 11 address bits, PYW-W05-0 through PYW-W15-0, must also be valid at this time. The PEM receives these bits from the PE via the UC cards in the MLU. During read operation, signal level conversion (from ECL to CTμL) is the only action taken by the MLU on the address bits. The memory protect logic on the MC card is not enabled during read cycles.

* READ DATA PATHS

The first segment of the read data path through the MLU is the same for all read cycles regardless of the destination of the read data. First, the CTμL-level data is sent from the PEM to the down converter logic on the MIR cards as bits MIWFW00-1 through MIWFW63-1. Read data paths through the MLU are shown in Figure 4-5.

There are eight down converters on each MIR card. Routing of read data into and out of the eight MIR cards conforms to the byte grouping used for routing of write data; that is, bytes 1, 6, 7 and 8 are routed through adjacent MIR cards (see Table 2-2). This routing is followed to maintain consistency between read and write paths only; inner and outer words are not selectively gated during read operations.

PEM-to-PE read data is sent direcly to the PE from the down converters. The ECL-level bits are labeled MOWPW00-1 through MOWPW63-1.

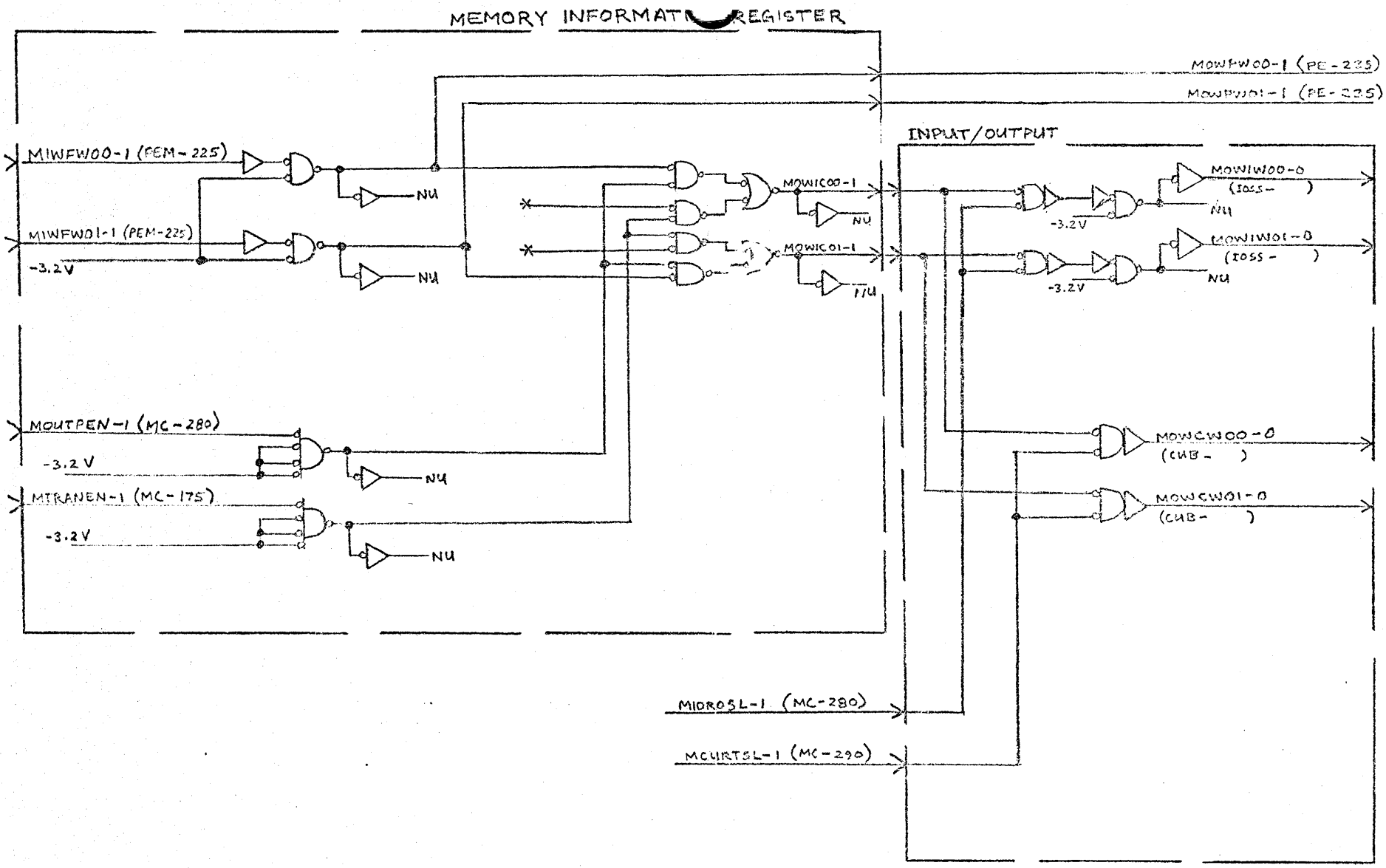


Figure 4-5. Read Data Paths

Read data being routed to the CUB or IOSS is sent from the down converters to read/transfer select gates, which are also on the MIR cards. PEM-to-CUB read data and PEM-to-IOSS read data use the same 64 lines between the down converters and the read/transfer select gates.

READ/TRANSFER SELECT GATES

These select gates multiplex CUB/IOSS read data with PE-to-CUB transfer data. Both sets of inputs to the select gates (read data and transfer data) are gated through the select gates to the IO cards during a read cycle, but at different times. The transfer data inputs are enabled first during a transfer enable period. Following this, the read data inputs are enabled; this second period is called the output enable period.

Two flip-flops in the MC logic define the transfer enable and output enable periods. A pair of timing pulses from the MT logic set and reset the transfer enable flip-flop at 165 and 265 ns, respectively, of the read cycle. A second pair of timing pulses set and reset the output enable flip-flop at 270 and 370 ns, respectively, of the read cycle. These flip-flops provide the pulses that enable the transfer data inputs and read data inputs to the select gates; they are, MTRANEN-1 and MOUTPEN-1. Each of these pulses remains true while its respective flip-flop is in the set state.

Although the transfer data inputs to the select gates are enabled for 100 ns of the read cycle, the invalid data present at those inputs is not made available to the CUB. During a read cycle, the CUB data drivers on the IO cards are held disabled throughout the transfer enable period; that is, the gating signals needed to activate the CUB data drivers are not generated until the output enable period. Details regarding operation of the logic during the transfer enable period of a transfer cycle are provided in Section 4.3, TRANSFER CYCLE.

- CUB/IOSS READ DATA SELECTION AND GATING

If the CUB is the destination for the read data, the MC logic generates the CUB read select signal, MCURSEL-1. If the IOSS is the destination, the IOSS read select signal, MIORSEL-1, is generated. In either case, the select signal is generated by select gates that decode the following conditions:

A. FREAD-1 is true, indicating that a read operation has been specified.

B. The transfer flip-flop is not set (MZTPWCW-0 is false), indicating that a transfer operation has not been specified.

C. Either FMDSEL0-1 is false and FMDSEL1-1 is true, indicating that the CUB is the destination for the data or FMDSEL0-1 is true and FMDSEL1-1 is false, indicating that the IOSS is the destination (see Table 4-2).

Figure 4-6 illustrates the logic involved in generating the CUB/IOSS read select signals.

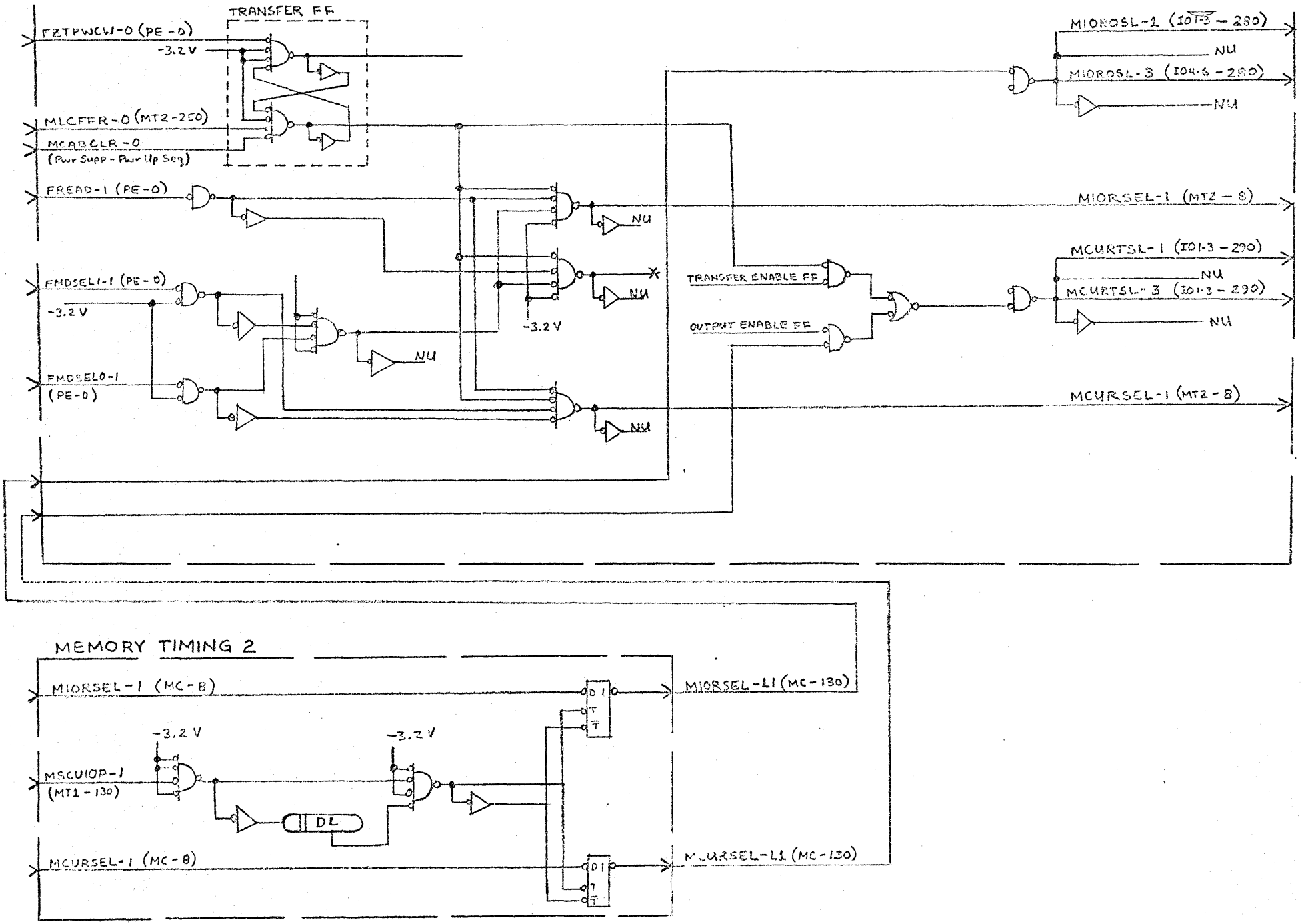


Figure 4-6. CUD/IOSS Read Select Logic

When these conditions are satisfied, one of the two read select signals (CUB or IOSS) is generated. This causes one of two latches on the MT2 card to be set at approximately 130 ns of the read cycle. The output of the set latch, MCURSEL-L1 or MIORSEL-L1, is sent to the MC logic, where it is used to generate either a pair of CUB data gating signals, MCURTSL-1 and MCURTSL-3, or a pair of IOSS data gating signals, MIORSL-1 and MIORSL-3.

The output of the output enable flip-flop is ANDed separately with the outputs of the two read select latches, MCURSEL-L1 and MIORSEL-L1. When the output enable flip-flop is set at the beginning of the output enable period, one of the two pairs of data gating signals will be generated, depending on which read select latch has been set. These signals are sent to the six IO cards (MCURTSL-1 or MIORSL-1 to IO1, 2 and 3 and MCURTSL-3 or MIORSL-3 to IO4, 5, and 6) where they gate the read data out to the CUB or IOSS.

The read data is provided to the IO cards by the read/transfer select gates as MOWIC00-1 through MOWIC63-1. This data becomes valid at the start of the output enable period when the output enable flip-flop sets. The MT2 signal, MOEFFS-1, sets the output enable flip-flop, resulting in MOUTPEN-1. This signal is sent to the MIR cards, where it gates the read data through the read/transfer select gates to the IO cards. The output enable flip-flop is reset 100 ns later by the MT2 signal, MOEFFR-0.

Logic on the IO cards converts the ECL levels of the incoming data bits to the CTuL levels required by the IOSS. Since the CUB uses ECL levels, it must reconvert the CTuL levels it receives from the IO cards. The IO logic also inverts the data before sending it to the CUB or IOSS. Consequently, the CUB data leaving the IO cards is labeled MOWCW00-0 through MOWCW63-0 and the IOSS data leaving the IO cards is labeled MOWIW00-0 through MOWIW63-0.

- CUB/IOSS DATA STROBES

The MLU also provides the CUB with a pair of strobes that enable the CUB to accept the read data. One strobe, MZTMWCW-0, is associated with data bits 0 through 31; the other strobe, MZTMWCW-2, allows the CUB to accept data bits 32 through 63. For IOSS read operations, the MLU sends the IOSS a single data strobe, MZTMWIW-0, for all 64 bits. Figure 4-7 illustrates the MLU logic related to these strobes.

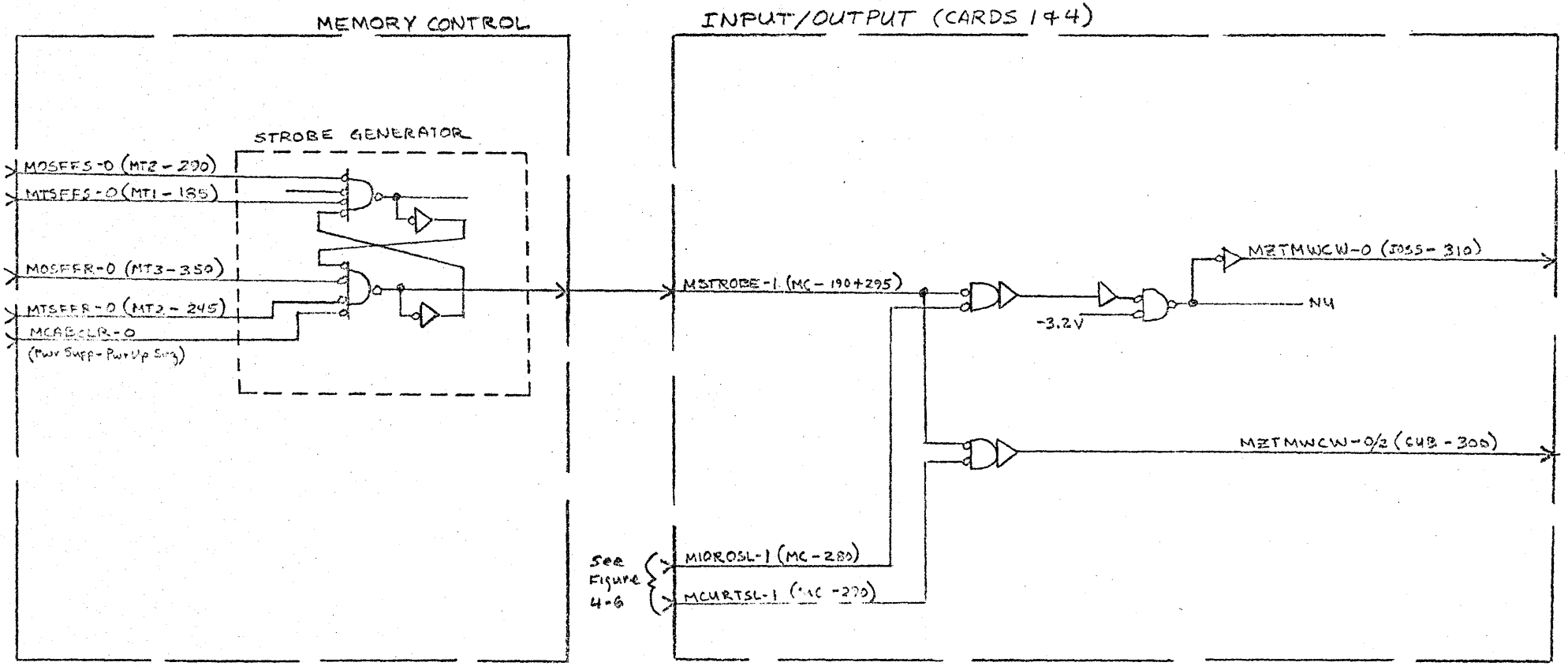


Figure 4-7. CUB/IOSS Read Data Strobes

Both CUB and IOSS strobes originate as the set output, MSTROBE-1, of a flip-flop on the MC card. This strobe flip-flop is set twice during a read cycle, once during the transfer enable period and once during the output enable period. The strobe flip-flop output is sent to IO cards 1 and 4 where it is gated out to the CUB or IOSS by the same signal that gates the read data through the IO logic.

Because gating of the CUB/IOSS read strobe is the same as gating of the CUB/IOSS read data, MSTROBE-1 is ignored during the transfer enable period of a read cycle. When the strobe flip-flop sets the second time (during the output enable period), MSTROBE-1 is gated out to the CUB from IO1 and IO4 as MZTMWCW-0 and MZTMWCW-2 or out to the IOSS as MZTMWIW-0. Remember that the IO logic inverts the incoming ECL level as well as converting it to the corresponding CTul level.

4.3 TRANSFER CYCLE

During a transfer cycle, data is moved from the PE to the CUB through the MLU. The PEM and IOSS play no part in a transfer operation.

The transfer cycle begins with the arrival at the MLU of the transfer signal, FZTPWCW-0. This signal is inverted by the MC logic to produce the memory timing initiate signal, MIMCTNP-1. This low-level signal is sent to the MT1 card where it initiates the sequence of timing pulses that are used to control transfer cycle circuitry.

FZTPWCW-0 also sets the transfer flip-flop on the MC card. The output of this flip-flop, MZTPWCW-0, is used to condition various MLU circuits for a transfer operation.

Because the PEM does not take part in a transfer operation, the memory initiate pulse, MINITPL-0 must be inhibited. The read/write control input, FREAD-1, is false (relative high); this disables one half of the read/write memory initiate select gate. The output of the transfer flip-flop, MZTPWCW-0, disables the other half of this select gate. With both halves of the read/write memory initiate select gate disabled, MINITPL-0 is sent to the UC card in its false state (relative low) and, consequently, MINITPL-1 is sent from the UC card to the PEM in its false state (relative high). This prevents the PEM logic from initiating a memory cycle.

TRANSFER DATA PATH

The transfer data path is the same, from the PE to the MIR data latches, as the PE write data path. That is, the transfer data is routed to the data latches over the same lines that carry PE write data and is multiplexed with the IO write data by the PE/IO select gates on the MIR cards. Figure 4-8 illustrates the data path for a transfer cycle.

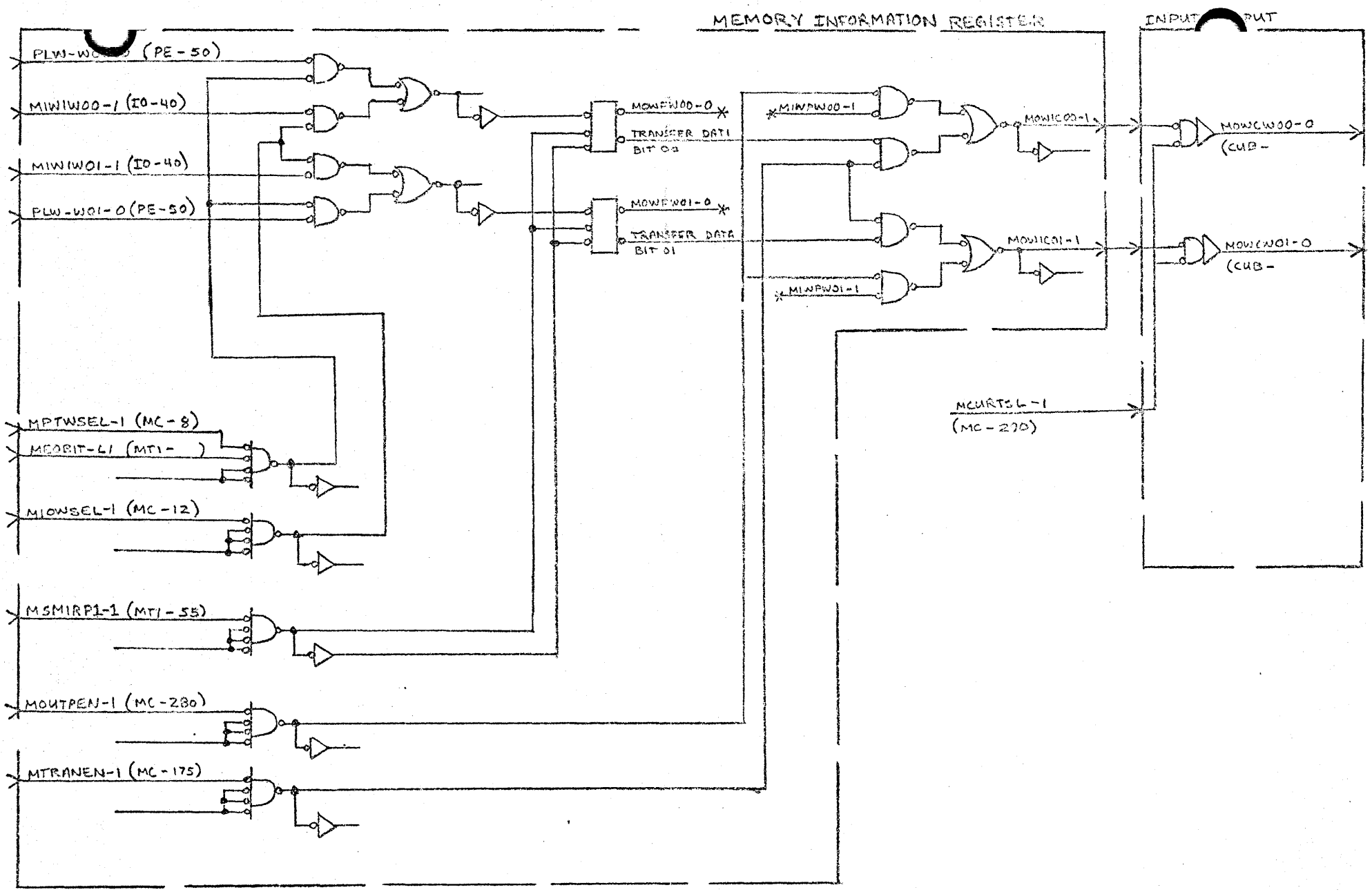


Figure 4-8. Transfer Data Path

As in a PE write operation, data is transferred from the PE to the CUB along two parallel, 32-bit data paths. The PE exercises separate control over data flow along these two paths through the use of two data control bits, P-E-30 and P-1-30. These are the same bits that control storage of the two halves of a PE write data word during a write memory cycle.

One data control bit, P-E-30, enables the transfer of bits 00 through 07 and 40 through 63 (referred to as the outer word); the other bit enables the transfer of bits 08 through 39 (referred to as the inner word). The PE sends one or the other or both of these control bits to a pair of latches (called the E-bit latches) on the MT1 card of the MLU. These control bits are strobed into the E-bit latches at the beginning of the transfer cycle. The output of each latch controls a different set of 32 bits of the transfer data.

The output of one latch, MEOBIT-L1, is sent to MIR cards 1, 6, 7 and 8 to develop the data select signal for the outer word. The output of the other latch, MEIBIT-L1, is sent to MIR cards 2,3, 4 and 5 to develop the data select signal for the inner word.

The E-bit latch outputs are ANDed on their respective MIR cards with the transfer select signal, MPTWSEL-1. If an E-bit latch is set, ANDing its output with MPTWSEL-1 will result in transfer data select signals for the four bytes of transfer data associated with that E-bit latch. If an E-bit latch is not set, the four transfer data select signals controlled by that latch will not be generated. Consequently, those four bytes of transfer data will not be gated through the select gates to the MIR latches.

The transfer select signal, MPTWSEL-1, is provided to each MIR card by logic on the MC card. For transfer operations, this signal goes true (relative-low) when the transfer flip-flop sets.

The selected transfer data bits are inverted by the select gates and applied to their respective MIR latches. Shortly after the transfer data is made available to the MIR latches, a pair of complementary strobes are generated on each MIR card to clock the data into the latches. Each strobe

pair is derived from one of eight MIR strobe pulses, MSMIRP1-1 through MSMIRP8-1, which are provided by delay lines on either MT1 or MT2. These are the same pulses that clock the MIR latches during write cycles.

- READ/TRANSFER SELECT GATES

The transfer data is sent from the complementary outputs of the MIR latches to the CUB via read/transfer select gates on the MIR cards and the IO logic.

The select gates multiplex the transfer data with CUB/IOSS read data. As in a read memory cycle, both sets of inputs to the select gates (transfer data and read data) are gated through the select gates to the IO cards during a transfer cycle, but at different times.

The transfer data inputs are enabled first during the transfer enable period. The transfer period begins when a timing pulse from MT1, MTEFFS-0, sets the transfer enable flip-flop at 165 ns of the transfer cycle. The output of the transfer enable flip-flop is ANDed with the output of the transfer flip-flop to generate a pair of CUB data gating signals, MCURTSL-1 and MCURTSL-3. These gating signals are sent to the six IO cards (MCURTSL-1 to IO1, 2 and 3 and MCURTSL-3 to IO4, 5 and 6) where they gate the transfer data out to the CUB.

The transfer data is provided to the IO cards by the read/transfer select gates as MOWIC00-1 through MOWIC63-1. This data becomes valid at the start of the transfer enable period when the transfer enable flip-flop sets. The transfer enable flip-flop output is sent to the MIR cards as MTRANEN-1, where it gates the transfer data through the read/transfer select gates to the IO cards. The transfer data remains valid for 100 ns until the transfer enable flip-flop is reset by the MT2 output, MTEFFR-0.

Logic on the IO cards converts the ECL levels of the transfer data to CTμL levels. This conversion takes place because IOSS read data is also routed through the IO cards and the IOSS requires the conversion. Consequently, the CUB is obliged to reconvert the CTμL levels of the transfer data to the corresponding ECL levels. The IO logic also inverts the transfer data before sending it to the CUB as MOWCW00-0 through MOWCW63-0.

- CUB DATA STROBE

As in a read memory cycle, the MLU provides the CUB with a pair of strobes that enable the CUB to accept the transfer data. Figure 4-7 illustrates the MLU logic related to these strobes.

Both strobes, MZTMWCW-0 and MZTMWCW-2, originate as the set output, MSTROBE-1, of a flip-flop on the MC card. This strobe flip-flop is set during the transfer enable period by the MT1 transfer timing pulse, MTSFFS, at 185 ns of the transfer cycle. The output of the strobe flip-flop is sent to IO cards 1 and 4 where it is gated out to the CUB by the same signal that gates the transfer data through the IO logic.

- WRITE ENABLE PREVENTION

During a transfer operation, it is necessary to prevent generation of the write enable signals, MWOUTEN-0 and MWINNEN-0. These are the signals ordinarily sent to the PEM during a write operation that enable its logic to write the outer and/or inner words. Generation of these signals is blocked during a transfer cycle in two ways.

1. The true output of the set transfer flip-flop, MZTPWCW-0, disables the two NAND gates that produce MWOUTEN-0 and MWINNEN-0.

2. MZTPWCW-0 also prevents the generation of the memory protect timing pulse, MWPROTP-0. This causes the write enable flip-flop to reset. The output of the reset write enable flip-flop also disables the MWOUTEN-0 and MWINNEN-0 NAND gates.

SECTION 5.0

POWER DISTRIBUTION

The MLU, as a subunit of the Processing Unit (PU), receives power from power supplies external to the PU in the following way.

In each PU cabinet (Figure 5-1), there are two power supplies that provide +4.8V and ground, two power supplies that provide -2.0V and ground, one power supply that provides +1.32V and -3.20V for the routing logic and eight power supplies (preregulators) that provide 4.52V. These power supplies provide power for the eight associated Processing Units.

The ground of all the power supplies in each PU cabinet is connected to the ground of the controller of the PU cabinet, which in turn connects to the ground of all the other controllers (eight), which, along with the ground of the B6700 control computer, are connected to Earth, thus establishing a ground (Earth) tie.

From the PU cabinet, the above voltages (+4.8V, -2.0V, ground and 4.52V) are brought into the Processing Unit in two groups. The first group brings +4.8V, -2.0V and ground; it is used exclusively for the PEM and the Up and Down converters of MLU. The second group, which brings 4.52V to the PU, is used for the PE and MLU circuits.

On the top of the PE there is a section called Dual Power Supply Shunt Regulator (see Figure 5.2). This regulator contains two main busses used to transfer the grouped voltages into the individual subunits of the Processing Unit (PE, MLU and PEM). Both busses consist primarily of large laminated planes that are properly isolated from one another. One bus is used for +4.8V, -2.0V and ground; the other bus is used for +1.32V, -3.20V and ground.

The +4.8V power is tapped from the bus plane for use by the MLU level conversion circuits. A two-plane strip routes the +4.8V power to the

MLU and provides a path from the MLU to the ground plane of the large bus. This ground path is used to shield the Cabinet Clear signal and as the ground level for the I/O circuits in the MLU.

A wire between the control card in the Dual Power Supply Shunt Regulator and the MLU provides the path for the Cabinet Clear signal (MCABCLR--O); this is the signal that resets flip-flops in the MLU when power is first applied to the PU.

The +1.32V and -3.20V are derived in the power supply shunt regulator from the incoming +4.52V. The ground plane of the bus for +1.32V and -3.20V is connected at one end with the chassis (PU) and with the ground plane of the second bus at the other end. This assures a common ground for all the subunits of the PU.

The +1.32V, -3.20V and ground levels are provided to the MLU and PE circuits via the large, three-plane bus shown in Figure 5-2. These laminated planes are, of course, fully isolated from one another.

Figure 5-3 depicts the basic current paths involved in the distribution of the +1.32V and -3.20V.

CURRENT AND VOLTAGE PROTECTION

Each power supply shunt regulator includes an overcurrent detector. This detector compares the current through a 50 amp, 50mV shunt resistor, with a fixed reference current. If the current through the shunt resistor exceeds the reference current significantly, the detector opens the circuit breaker in the preregulator.

Similarly, the over voltage/under voltage detector in the power supply shunt regulator senses an excessive or insufficient voltage level being applied to a load. If the detector determines that a voltage is outside some specified limit, it opens the appropriate circuit breaker.

Test points for the various MLU voltages are available on the MLU backplane.

a)

+4.8V 430AMP A2 TO B2,C2,D2,E2	+1.32, -3.2V 50AMP A3 TO ROUTE LOGIC	-2.0V 220AMP A4 TO B2,C2,D2,E2,F2,G2,H2, and J2	+4.8V 430AMP A5 TO F2,G2,H2,J2
PRE/REG 4.52V A6 TO C2	PRE/REG 4.52V A7 TO E2	PRE/REG 4.52V A8 TO G2	PRE/REG 4.52V A9 TO J2
PRE/REG 4.52V A10 TO B2	PRE/REG 4.52V A11 TO D2	PRE/REG 4.52V A12 TO F2	PRE/REG 4.52V A13 TO H2

b)

PU B2	PU C2	PU D2	PU E2	PU F2	PU G2	PU H2	PU J2

FIGURE 5-1. PU Cabinet. a) Power Supply Location
b) PU Power Distribution

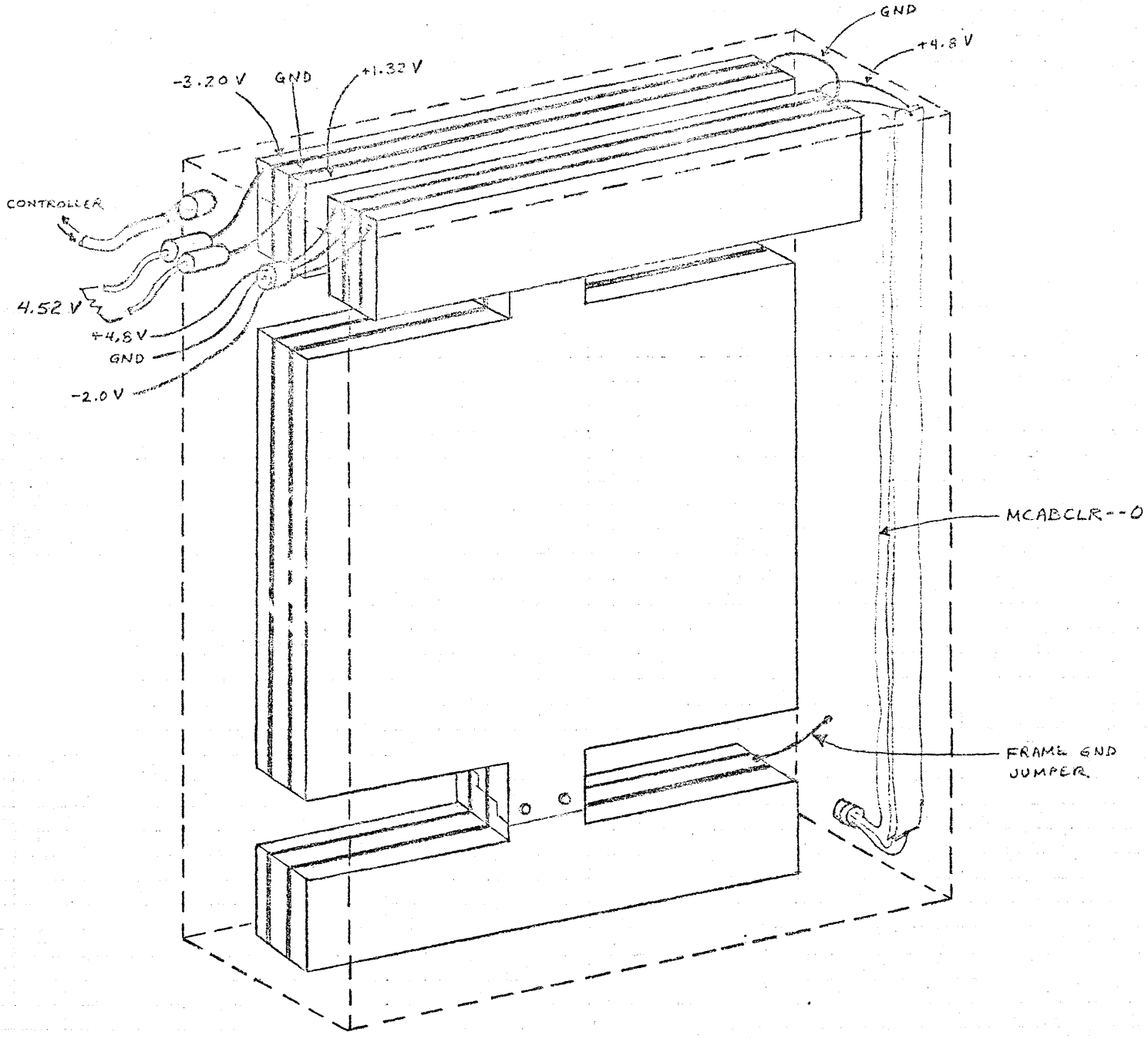


Figure 5-2. Power Distribution in the PU

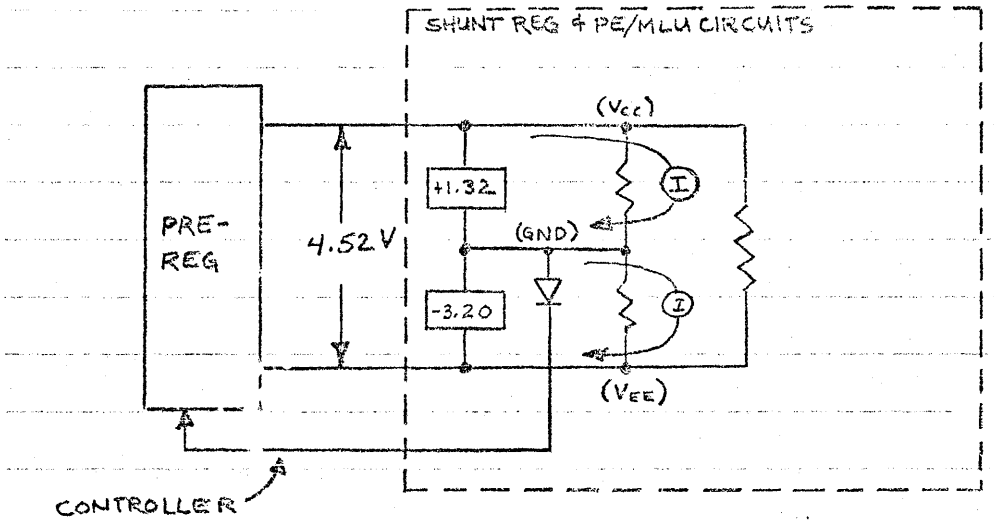


Figure 5-3. Current Paths for +1.32V and -3.20V Supplies

APPENDIX A

SIGNAL GLOSSARY

APPENDIX A

SIGNAL GLOSSARY

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
FIMC-----1	Neg	CU via PE to MC	• Initiate memory cycle • Used by PE to begin any read or write cycle • All MLU timing during read or write is referenced to arrival of FIMC-1 at MC • One clock period wide
FMDSELO--1 and FMDSEL1--1	Neg	CU via PE to MC	• Memory data select • Combination of logic levels identifies source of write data or destination of read data • Used by MC to develop appropriate data gating signals • Also used to override E-bit signals (P-E-30, P-1-30) during CU or IOSS write operations • Become valid at same time as FIMC-1 and remain valid until next FIMC-1
FMEMPRO--1	Neg	CU via PE to MC	• Memory protect • Enables memory protect circuits on MC card if PE wishes to protect PEM address locations 0000 through 0127 (decimal) from a write cycle • Becomes valid at same time as FIMC-1 and remains valid until next FIMC-1

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
FMSEL- - - -1	Neg	CU via PE to MC	• Memory select • Used by CU to select specific memory out of all memories in array • Becomes valid at same time as FIMC-1 and remains valid until next FIMC-1
FREAD- - - -1	Neg	CU via PE to MC	• Read/Write control • Used by PE to specify read or write cycle to MLU • Low logic level specifies read; high logic level specifies write • Becomes valid at same time as FIMC-1 and remains valid until next FIMC-1
FRMPRO- - -0	Neg	CU via PE to MC	• Memory protect error reset • Used by CU to reset memory protect error latch on MC card • One clock period wide
FZTPWCW- -0	Neg	CU via PE to MC	• Initiate transfer • Used by PE to begin transfer cycle • All MLU timing during transfer is referenced to arrival of FZTPWCW-0 • One clock period wide
MCABCLR- -0	Neg	PU pwr supply to MC	• Cabinet clear • Resets MC flip-flops when power is turned on • Signal goes low when power sequencing is complete

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MCURSEL--1	Neg	MC to MT2	• CUB read select • Indicates that CUB has been selected as destination of read data
MCURSEL-L1	Neg	MT2 to MC	• Latched CUB read select • Output of a latch set by MCURSEL-1 • Maintains CUB read select until data is gated out to CUB during output enable period of read cycle • Latch sets at approximately 130 ns of CUB read cycle
MCURTSL--1 MCURTSL--3	Neg Neg	MC to IO (1 3) MC to IO (4 6)	• CUB output select • These signals gate read or transfer data to the CUB • Both are true during transfer enable period of transfer cycle or output enable period of read cycle
MEIBIT--L1	Neg	MT1 to MC	• Latched E_1 bit • Output of latch set by E_1 bit from PE • Allows 32-bit inner word to be written into PEM or transferred to CUB

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MEOBIT--L1	Neg	MT1 to MC	• Latched E bit • Output of latch set by E bit from PE • Allows 32-bit outer word to be written into PEM or transferred to CUB
MIMCTNP--1	Neg	MC to MT1	• Initiate selected memory/ transfer cycle • Input to delay line; initiates sequence of timing pulses for read, write or transfer cycle • Results from FIMC-1 AND FMSEL-1 or FZTPWCW-0 • One clock period wide
MIMCTRP--1	Neg	MT1 to MT2	• MT1 delay line output • Output of series of delay lines on MT1 • Used as input to MT2 delay line series • 50 ns pulse width
MIMCTSP--1	Neg	MT2 to MT3	• MT2 delay line output • Output of series of delay lines on MT2 • Used as input to series of delay lines on MT3 • 50ns pulse width
MINITPL--0	Neg	MC to UC2	• Initiate memory-ECL • Will initiate read or write activity in PEM after level conversion by UC2 circuits • One clock period wide during read cycles; 50 ns wide during write cycles

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MINITPL--1	Neg	UC2 to PEM	• Initiate memory - CTμL • CTμL level pulse used by PEM to initiate read or write cycle in PEM • One clock period wide during read cycles; 50 ns wide during write cycles • Width during read cycle (one clock period) is determined by frequency of CPU operation; example: for CPU frequency of 60.3 MH_z, MINITPL-1 has approximately 62 ns duration • Occurs at approximately 30 ns of a read cycle; occurs at approximately 70 ns of a write cycle
MIOROSL--1 and MIOROSL--3	Neg Neg	MC to IO (1-3) MC to IO (4-6)	• IOB output select enable • Gates read data through the IO logic to the IOSS • Occurs during the output enable period of read cycle if the IOSS has been identified as the destination
MIORSEL--1	Neg	MC to MT2	• IOB read select • Output of MC decode logic when IOSS has been identified as destination of read data
MIORSEL-L1	Neg	MT2 to MC	• Latch IOB read select • Output of latch set by IOB read select signal • Preserves the IOB read select condition until the read data has been gated out to the IOSS • Becomes valid at approximately 130 ns of the read cycle

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MIOWSEL--1	Neg	MC to MIR(1-8)	• IOB write select • Output of MC decode logic when IOSS has been identified as source of write data • Gates IOSS write data into MIR latches for temporary storage
MIWFWOO--1 through MIWFW63--1	Neg	PEM to MIR(1-8)	• PEM read data • CTL level data from the PEM, which is applied to down converters on the MIR cards • PEM output becomes valid at approximately 225 ns of the current read cycle; does not change until approximately 155 ns of next memory cycle
MIWIWOO--1 through MIWIW63--1	Pos	IO(1-6) to MIR (1-8)	• IOB input data • IOSS write data after level conversion to ECL by circuits on IO cards • Applied to PE/IO select gates on MIR cards • Data is valid from approximately 40 ns to 70 ns of a write cycle
MLCFFR---0	Neg	MT2 to MC	• Control F-F reset • Resets memory write enable flip-flop and transfer flip-flop • Occurs at approximately 250 ns of MLU cycle • 50 ns pulse width

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MOEFFR---0	Neg	MT3 to MC	• Reset output enable F-F • Resets output enable flip-flop at approximately 370 ns of MLU cycle • 50 ns pulse width
MOEFFS---0	Neg	MT2 to MC	• Set output enable F-F • Sets output enable flip-flop at approximately 270 ns of MLU cycle • Begins output enable period of MLU cycle • 50 ns pulse width
MOSFFR---0	Neg	MT3 to MC	• Reset output strobe F-F • Resets output/transfer strobe generator at approximately 350 ns of MLU cycle • 50 ns pulse width
MOSFFS---0	Neg	MT2 to MC	• Set output strobe F-F • Sets output/transfer strobe generator at approximately 290 ns of MLU cycle • 50 ns pulse width
MOUTPEN--1	Neg	MC to MIR(1-8)	• Output enable • Gates read data through read/transfer select gates on MIR cards • Occurs at beginning of output enable period of MLU cycle

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MOWCW00--0 through MOWCW63--0	Neg	IO(1-6) to CUB	• CUB output data • Read or transfer data sent to CUB from IO cards after conversion to CTμL levels by up converters on IO cards • Data becomes valid during output enable period of read cycle or during transfer enable period of transfer cycle
MOWFW00--0 through MOWFW63--0	Neg	MIR(1-8) to UC(1-3)	• PEM write data - ECL • Output of set (1) side of MIR latches • Data is sent to up converters for conversion from ECL to CTμL levels • Data becomes valid at approximately 70 ns of the write cycle
MOWFW00--1 through MOWFW63--1	Neg	UC(1-3) to PEM	• PEM write data - CTμL • Write data that is sent to PEM from up converters • Data is valid for approximately 250 ns of write cycle
MOWIC00--1 through MOWIC63--1	Neg	MIR(1-8) to IO(1-6)	• CUB/IOB read/PE-CUB transfer data • Output of read/transfer select gates on MIR cards • Becomes valid as transfer data during transfer enable period of MLU cycle; becomes valid as read data during output enable period of MLU cycle

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MOWIWOO--0 through MOWIW63--0	Neg	IO(1-6) to IOSS	• IOB output data • CTL level read data sent to the IOSS • Data is gated out from IO cards during output enable period of read cycle • MOWIW-0 uses same bi-directional data lines as MOWIW-1 (IOSS write data)
MOWIWOO--1 through MOWIW63--1	Pos	IOSS to IO(1-6)	• IOSS write data • CTL level write data sent to IO cards from IOSS • MOWIW-1 uses same bi-directional data lines as MOWIW-0 (IOB output data)
MOWPWOO--1 through MOWPW63--1	Neg	MIR(1-8) to PE	• PE output data • ECL level read data sent from down converters on MIR cards • Data is valid from approximately 235 ns of the read cycle to approximately 165 ns of the next memory cycle
MPROER---1	Neg	MC to PE	• Memory protect error • Output of memory protect error latch, which is set when write operation is attempted in protected area of PEM • Signal is sent to CU via PE • Does not prevent subsequent write operations • Latch is reset by FRMPRO-0 from CU

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MPTWSEL--1	Neg	MC to MIR(1-8)	• PE write/PE-CUB transfer select • Output from MC decode logic when PE has been identified as source of write or transfer data • Is ANDed with MEOBIT-1 and MEIBIT-1 to gate outer word and inner word of write or transfer data to inputs of MIR latches
MSCUIOP--1	Neg	MT1 to MT2	• CU/IO read select latch • Strobes the CU and IO read select latches on MT_2 • Occurs at approximately 130 ns of MLU cycle • 50 ns pulse width
MSMIRPL--1	Neg	MT1 to MT1	• MIR strobe pulse • Used to generate the four MIR strobe signals, MSMIRP(1-4)-1. • Occurs at approximately 55 ns of MLU cycle • 8 ns pulse width
MSMIRPL--0	Neg	MT2 to MT2	• MIR strobe pulse • Complement of MSMIRPL--1 • Used to generate four of the eight MIR strobe signals, MSMIRP(5-8)-1 • Occurs at approximately 55 ns of MLU cycle • 8 ns pulse width

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MSMIRP1--1 through MSMIRP8--1	Neg	MT(1-2) to MIR(1-8)	• MIR strobes • Used by MIR logic to clock write or transfer data into MIR latches • Occurs at approximately 55 ns of the MLU cycle • 8 ns pulse width
MSTROBE--1	Neg	MC to IO1,4	• IOB/CUB data strobe • Output of strobe flip-flop • Sent to up converters on IO cards for conversion to CTμL levels
MTEFFR---0	Neg	MT2 to MC	• Reset transfer enable F-F • Resets transfer enable flip-flop at approximately 265 ns of MLU cycle • 50 ns pulse width
MTEFFS---0	Neg	MT1 to MC	• Set transfer enable F-F • Sets transfer enable flip-flop at approximately 165 ns of MLU cycle • Begins transfer enable period of cycle • 50 ns pulse width
MTRANEN--1	Neg	MC to MIR(1-8)	• Transfer enable • Gates transfer data through read/transfer select gates on MIR cards • Occurs at beginning of transfer enable period of MLU cycle

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MTSFFR---0	Neg	MT2 to MC	• Reset transfer strobe F-F • Resets output/transfer strobe generator at approximately 245 ns of MLU cycle • 50 ns pulse width
MTSFFS---0	Neg	MT1 to MC	• Set transfer strobe F-F • Sets output/transfer generator at approximately 185 ns of MLU cycle • 50 ns pulse width
MWINITP--1	Neg	MT1 to MC	• Write initiate • Used with write control signal to generate initiate memory signal (MWINITPL--0) • Occurs at approximately 55 ns of MLU cycle • 50 ns pulse width
MWINNEN--0	Neg	MC to UC_2	• Write inner enable - ECL • Output of MC decode logic whenever inner word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTuL level
MWINNEN--1	Neg	UC_2 to PEM	• Write inner enable - CTuL • CTuL level that enables the PEM to write inner word of PEM data (bits 8 through 39) • Signal is valid from approximately 60 ns to 210 ns of write cycle

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MWOUTEN--0	Neg	MC to UC_2	• Write outer enable -ECL • Output of MC decode logic whenever outer word of PE write data is to be written into PEM • Sent to up converter logic for conversion to CTμL level
MWOUTEN--1	Neg	UC_2 to PEM	• Write outer enable - CTμL • CTμL level that enables the PEM to write inner word of PEM data (bits 0 through 7 and 40 through 63) • Signal is valid from approximately 60 ns to 210 ns of write cycle
MWPROTP--1	Neg	MT1 to MC	• Write protect • Sets the memory protect error flip-flop if error has been detected or sets write enable flip-flop if no error is detected • Occurs at approximately 40 ns of read or write cycle; is suppressed by MZTPWCW-0 during transfer cycle to prevent setting of write enable flip-flop • 50 ns pulse width
MYW-W05--0 through MYW-W15--0	Neg	UC(1-3) to PEM	• PEM memory address bits • Eleven-bit address that is sent to PEM as CTμL levels • Used by PEM to access the desired location for read or write operation • Bits are valid from approximately 20 ns of MLU cycle to approximately 20 ns of next cycle

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
MZTMWCW--0 and MZTMWCW--2	Neg	IO4 to CUB	• CUB output data strobe • Pair of strobes that allow CUB to accept read or transfer data • Gated out to CUB with read data during output enable period of MLU cycle or with transfer data during transfer enable period of MLU cycle
MZTMWIW--0	Neg	IO1 to IOSS	• IOB output data strobe • Strobe that allows IOSS to accept read data • Gated out to IOSS with read data during output enable period of MLU cycle
MZTPWCW--0	Neg	MC to MT_1	• Transfer cycle • Output of transfer flip-flop when flip-flop is set by FZTPWCW-0 • Indicates that MLU is performing transfer operation • Conditions other MLU logic to allow transfer of data from PE to CUB • Prevents MWPROTP-1 from setting write enable flip-flop; this, in turn, prevents MLU from issuing write enable signals to PEM

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
PLW-W00--0 through PLW-W63--0	Pos	PE to MIR (1-8)	• PE input data • ECL level data bits sent form PE to PE/IO select gates on MIR cards • Data may have originated at CU but, at this point in data flow, is indistinguishable from PE write data • Data is valid from approximately 50 ns to 70 ns • One clock period wide
PYW-W05--0 through PYW-W15--0	Pos	PE to UC(1-3)	• PE memory address register bits • ECL level address bits sent from PE to up converters for conversion to CTμL levels • CTμL levels to be used by PEM to access desired memory location for read or write operation • Four low-order ECL level bits are also examined by memory protect logic as part of memory protect activity
PYW-W05--0 through PYW-W08--0	Pos	PE to MC	• Memory protect bits of memory address • Memory protect circuits on MC card examine these bits as part of memory protect activity

MNEMONIC	LOGIC CONVENTION	SOURCE DESTINATION	DEFINITION
P----E--30	Pos	PE to MT1	• E bit signal • Sent by PE to allow passage of the outer word of PE write or transfer data (bits 00 through 07 and 40 through 63) through the MLU • Sets the E bit latch on MT1 to generate MEOBIT-L1 • At least one clock period wide
P----1--30	Pos	PE to MT1	• E1 bit signal • Sent by PE to allow passage of the inner word of PE write or transfer data (bits 08 through 39) through the MLU • Sets the E1 bit latch on MT1 to generate MEIBIT-L1 • At least one clock period wide

APPENDIX B

WIRE LIST

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
PLW-W00--0	PE	J20-D08	MIR	J08-A29
01		-B08		-B14
02		-C09		-B08
03		-A09		-B12
04		-C11		-B38
05		-A11		-B26
06		-D12		-D48
07		J20-B12		J08-C39
40		J21-D02		J09-A29
41		-B02		-B14
42		-C03		-B08
43		-A03		-B12
44		-C05		-B38
45		-A05		-B26
46		-D06		-D48
47		-B06		J09-C39
48		-D08		J10-A29
49		-B08		-B14
50		-C09		-B08
51		-A09		-B12
52		-C11		-B38
53		-A11		-B26
54		-D12		-D48
55		-B12		J10-C39
56		-C17		J11-A29
57		-B14		-B14
58		-B08		-D18
59		-A15		-B12
60		-D20		-B38
61		-A17		-B26
62		-C21		-D48
PLW-W63--0	PE	J21-B18	MIR	J11-C39

Table 14A: WRITE/TRANSFER Data from PE to MIR Cards (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
PLW-W08--0	PE	J19-D02	MIR	J04-A29
09		-B02		-B14
10		-C03		-B08
11		-A03		-B12
12		-C05		-B38
13		-A05		-B26
14		-D06		-D48
15		-B06		J04-C39
16		-D08		J05-A29
17		-B08		-B14
18		-C09		-B08
19		-A09		-B12
20		-C11		-B38
21		-A11		-B26
22		-D12		-D48
23		-B12		J05-C39
24		-C17		J06-A29
25		-B14		-B14
26		-D18		-B08
27		-A15		-B12
28		-D20		-B38
29		-A17		-B26
30		-C21		-D48
31		J19-B18		J06-C39
32		J20-D02		J07-A29
33		-B02		-B14
34		-C03		-B08
35		-A03		-B12
36		-C05		-B38
37		-A05		-B26
38		-D06		-D48
PLW-W39--0	PE	J20-B06	MIR	J07-C39

Table 14B: WRITE/TRANSFER Data from PE to MIR Cards (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MIWIW00--1	IO	J06-65	MIR	J08-D12
01		-61		-A11
02		-53		-A09
03		-49		-C05
04		-43		-C33
05		-39		-A35
06		-35		-A41
07		J06-25		J08-B48
40		J03-21		J09-D12
41		-17		-A11
42		J03-07		-A09
43		J02-65		-C05
44		-61		-C33
45		-53		-A35
49		-49		-A41
47		-43		J09-B48
48		-39		J10-D12
49		-35		-A11
50		-25		-A09
51		-21		-C05
52		-17		-C33
53		J01-07		-A35
54		J01-55		-A41
55		-61		J10-B48
56		-53		J11-D12
57		-49		-A11
58		-43		-A09
59		-39		-C05
60		-35		-C33
61		-25		-A35
62		-21		-A41
MIWIW63--1	IO	J01-17	MIR	J11-B48

Table 15A: WRITE Data from IO to MIR Cards (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MIWIW08--1	IO	J06-21	MIR	J04-D12
09		-17		-A11
10		J06-07		-A09
11		J05-65		-C05
12		-61		-C33
13		-53		-A35
14		-49		-A41
15		-43		J04-B48
16		-39		J05-D12
17		-35		-A11
18		-25		-A09
19		-21		-C05
20		-17		-C33
21		J05-07		-A35
22		J04-65		-A41
23		-61		J05-B48
24		-53		J06-D12
25		-49		-A11
26		-43		-A09
27		-39		-C05
28		-35		-C33
29		-25		-A35
30		-21		-A41
31		J04-17		J06-B48
32		J03-65		J07-D12
33		-61		-A11
34		-53		-A09
35		-49		-C05
36		-43		-C33
37		-39		-A35
38		-35		-A41
MIWIW39--1	IO	J03-25	MIR	J07-B48

Table 15B: WRITE Data from IO to MIR Cards (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWFW00--0	MIR	J08-A23	UC	J17-B30
01		-A05		-C09
02		-A17		-D18
03		-C09		-B14
04		-A33		-A39
05		-B30		-B32
06		-B32		-A35
07		J08-C41		J17-C41
40		J09-A23		J18-C21
41		-A05		-D08
42		-A17		-B18
43		-C09		-D12
44		-A33		-B38
45		-B30		-D30
46		-B32		-C33
47		J09-C41		-A41
48		J10-A23		-B30
49		-A05		-C09
50		-A17		-D18
51		-C09		-B14
52		-A33		-A39
53		-B30		-B32
54		-B32		-A35
55		J10-C41		-C41
56		J11-A23		-D26
57		-A05		-C11
58		-A17		-B20
59		-C09		-A17
60		-A33		-C39
61		-B30		-A33
62		-B32		-C35
MOWFW63--0	MIR	J11-C41	UC	J18-B42

Table 16A: WRITE Data from MIR to Up Converter (UC) Cards (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWFW08--0	MIR	J04-A23	UC	J16-C21
09		-A05		-D08
10		-A17		-B18
11		-C09		-D12
12		-A33		-B38
13		-B30		-D30
14		-B32		-C33
15		J04-C41		-A41
16		J05-A23		-B30
17		-A05		-C09
18		-A17		-D18
19		-C09		-B14
20		-A33		-A39
21		-B30		-B32
22		-B32		-A35
23		J05-C41		-C41
24		J06-A23		-D26
25		-A05		-C11
26		-A17		-B20
27		-C09		-A17
28		-A33		-C39
29		-B30		-A33
30		-B32		-C35
31		J06-C41		J16-B42
32		J07-A23		J17-C21
33		-A05		-D08
34		-A17		-B18
35		-C09		-D12
36		-A33		-B38
37		-B30		-D30
38		-B32		-C33
MOWFW39--0	MIR	J07-C41	UC	J17-A41

Table 16B: WRITE Data From MIR to Up Converter (UC) Cards (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWFW00--1	UC	J17-B26	PEM	J23-C45
01		-C15		-D44
02		-B24		-C41
03		-A11		-C39
04		-A47		-D36
05		-A29		-C35
06		-D32		-C27
07		J17-B48		-D26
40		J18-A23		-D24
41		-D44		-C23
42		-C17		-C21
43		-B12		-D20
44		-D48		-C17
45		-C29		-C15
46		-B36		-D14
47		-A45		-D12
48		-B26		-C11
49		-C15		-C09
50		-B24		-D08
51		-A11		-D06
52		-A47		-C05
53		-A29		-C03
54		-D32		J23-D02
55		-B48		J24-B48
56		-A27		-A47
57		-B06		-A45
58		-A21		-B44
59		-A15		-B42
60		-B44		-A27
61		C45		-B26
62		-D36		-A35
MOWFW63--1	UC	J18-C47	PEM	J24-A33

Table 17A: WRITE Data From Up Converter Cards to PEM (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWFW08--1	UC	J16-A23	PEM	J23-A45
09		-D44		-B44
10		-C17		-A41
11		-B12		-A39
12		-D48		-B36
13		-C29		-A35
14		-B36		-A27
15		-A45		-B26
16		-B26		-B24
17		-C15		-A23
18		-B24		-A21
19		-A11		-B20
20		-A47		-A17
21		-A29		-A15
22		-D32		-B14
23		-B48		-B12
24		-A27		-A11
25		-B06		-A09
26		-A21		-B08
27		-A15		-B06
28		-B44		-A05
29		-C45		-A03
30		-D36		J23-B02
31		J16-C47		J22-D48
32		J17-A23		-C47
33		-D44		-C45
34		-C17		-D44
35		-B12		-D42
36		-D48		-C27
37		-C29		-D26
38		-B36		-C35
MOWFW39--1	UC	J17-A45	PEM	J22-C33

Table 17B: WRITE Data From Up Converter Cards to PEM (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MIWFW00--1	PEM	J24-A21	MIR	J08-C27
01		-B20		-C21
02		-A23		-C29
03		-B24		-D32
04		-A15		-D30
05		-A17		-C35
06		-B12		-B36
07		-A11		J08-A39
40		-B06		J09-C27
41		-B08		-C21
42		-D30		-C39
43		-D32		-D32
44		-A05		-D30
45		-A03		-C35
46		-D44		-B36
47		-C45		J09-A39
48		-C41		J10-C27
49		-C39		-C21
50		-C35		-C29
51		-D36		-D32
52		-C23		-D30
53		-C21		-C35
54		-C27		-B36
55		-D26		J10-A39
56		-D14		J11-C27
57		-D12		-C21
58		-C17		-C29
59		-D18		-D32
60		-C03		-D30
61		-C05		-C35
62		-C09		-B36
MIWFW63--1	PEM	J24-D08	MIR	J11-A39

Table 18A: READ Data from PEM to MIR Cards (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MIWFW08--1	PEM	J22-C21	MIR	J04-C27
09		-D20		-C21
10		-C23		-C29
11		-D24		-D32
12		-C15		-D30
13		-C17		-C35
14		-D12		-B36
15		-C11		J04-A39
16		-D06		J05-C27
17		-D08		-C21
18		-B30		-C29
19		-B32		-D32
20		-C05		-D30
21		-C03		-C35
22		-B44		-B36
23		-A45		J05-A39
24		-A41		J06-C27
25		-A39		-C21
26		-A35		-C29
27		-B36		-D32
28		-A23		-D30
29		-A21		-C35
30		-A27		-B36
31		-B26		J06-A39
32		-B14		J07-C27
33		-B12		-C21
34		-A17		-C29
35		-B18		-D32
36		-A03		-D30
37		-A05		-C35
38		-A09		-B36
MIWFW39--1	PEM	J22-B08	MIR	J07-A39

Table 18B: READ Data from PEM to MIR Cards (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWPW00--1	MIR	J08-A03	PE	J20-D32
01		-C11		-B32
02		-A27		-C33
03		-C15		-A33
04		-D18		-C35
05		-B24		-A35
06		-A15		-D36
07		J08-D26		J20-B36
40		J09-A03		J21-A23
41		-C11		-C23
42		-A27		-B24
43		-C15		-D24
44		-D18		-C29
45		-B24		-B30
46		-A15		-D30
47		J09-D26		-A29
48		J10-A03		-D32
49		-C11		-B32
50		-A27		-C33
51		-C15		-A33
52		-D18		-C35
53		-B24		-A35
54		-A15		-D36
55		J10-D26		-B36
56		J11-A03		-D38
57		-C11		-B38
58		-A27		-C39
59		-C15		-A39
60		-D18		-C41
61		-B24		-A41
62		-A15		-D42
MOWPW63--1	MIR	J11-D26	PE	J21-B42

Table 19A: READ Data from MIR Cards to PE (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWPW08--1	MIR	J04-A03	PE	J19-A23
09		-C11		-C23
10		-A27		-B24
11		-C15		-D24
12		-D18		-C29
13		-B24		-B30
14		-A15		-D30
15		J04-D26		-A29
16		J05-A03		-D32
17		-C11		-B32
18		-A27		-C33
19		-C15		-A33
20		-D18		-C35
21		-B24		-A35
22		-A15		-D36
23		J05-D26		-B36
24		J06-A03		-D38
25		-C11		-B38
26		-A27		-C39
27		-C15		-A39
28		-D18		-C41
29		-B24		-A41
30		-A15		-D42
31		J06-D26		J19-B42
32		J07-A03		J20-A23
33		-C11		-C23
34		-A27		-B24
35		-C15		-D24
36		-D18		-C29
37		-B24		-B30
38		-A15		-D30
MOWPW39--1	MIR	J07-D26	PE	J20-A29

Table 19B: READ Data from MIR Cards to PE (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWIC00--1	MIR	J08-B02	IO	J06-66
01		-B06		-62
02		-C03		-58
03		-D08		-50
04		-B20		-46
05		-C23		-36
06		-B18		-32
07		J08-A21		J06-24
40		J09-B02		J03-18
41		-B06		-12
42		-C03		J03-04
43		-D08		J02-66
44		-B20		-62
45		-C23		-58
46		-B18		-50
47		J09-A21		-46
48		J10-B02		-36
49		-B06		-32
50		-C03		-24
51		-D08		-18
52		-B20		-12
53		-C23		J02-04
54		-B18		J01-66
55		J10-A21		-62
56		J11-BC2		-58
57		-B06		-50
58		-C03		-46
59		-D08		-36
60		-B20		-32
61		-C23		-24
62		-B18		-18
MOWIC63--1	MIR	J11-A21	IO	J01-12

Table 20A: READ/TRANSFER data from MIR to IO Cards (OUTER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MOWIC08--1	MIR	J04-B02	IO	J06-18
09		-B06		-12
10		-C03		J06-04
11		-D08		J05-66
12		-B20		-62
13		-C23		-58
14		-B18		-50
15		J04-A21		-46
16		J05-B02		-36
17		-B06		-32
18		-C03		-24
19		-D08		-18
20		-B20		-12
21		-C23		J05-04
22		-B18		J04-66
23		J05-A21		-62
24		J06-B02		-58
25		-B06		-50
26		-C03		-46
27		-D08		-36
28		-B20		-32
29		-C23		-24
30		-B18		-18
31		J06-A21		J04-12
32		J07-B02		J03-66
33		-B06		-62
34		-C03		-58
35		-D08		-50
36		-B20		-46
37		-C23		-36
38		-B18		-32
MOWIC39--1	MIR	J07-A21	IO	J03-24

Table 20B: READ/TRANSFER data from MIR to IO Cards (INNER WORD)

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
PYW-W05--0	PE	J19-C47	UC	J16-B08
06		J19-A47		J16-A09
07		J20-C47		J17-B08
08		J20-A47		J17-A09
09		J19-D48		J16-A03
10		J19-B48		J16-A05
11		J20-D48		J17-A03
12		J20-B48		J17-A05
13		J20-A45		J17-C35
14		J21-D48		J18-A03
PYW-W15--0		J21-B48	UC	J18-A05
FIMC-----1		J20-C39	MC	J15-C17
FZTPWCW--0		-A39		-C33
FRMPRO---0		-C41		-B02
FMSEL----1		-A41		-B36
FMDSEL0--1		-D42		-D44
FMDSEL1--1		-B42		-C35
FREAD----1		-D44		-A35
FMEMPRO--1		J20-B44	MC	J15-D48
P----E--30		J19-C45	MT_1	J12-A03
P----1--30		J19-A45	MT_1	J12-B02
MPROER---1	MC	J15-A03	PE	J21-C45
MYW-W05--0	UC	J16-C03	PEM	J22-C39
06		J16-D14		J24-C33
07		J17-C03		J22-B38
08		J17-D14		J24-D42
09		J16-C27		J22-A47
10		J16-B02		J24-C29
11		J17-C27		J22-B24
12		J17-B02		J24-D06
13		J17-D36		J22-A11
14		J18-C27		J24-C15
MYW-W15--0		J18-B02		J22-B20
MWOUTEN--1		J17-A27		J24-B30
MWINNEN--1		-B06		J22-D38
MINITPL--1	UC	J17-B44	PEM	J24-B36
MWOUTEN--0	MC	J15-A29	UC	J17-D26
MWINNEN--0		-B32		-C11
MINITPL--0	MC	J15-A17	UC	J17-C39

Table 21A: Address and Control Signals List

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MTRANEN--1	MC	J15-B48	MIR_8	J11-D14
	IR_8	J11-D14	MIR_7	J10-D14
	MIR_7	J10-D14	MIR_6	J09-D14
	MIR_6	J09-D14	MIR_5	J08-D14
	MIR_5	J08-D14	MIR_1	J07-D14
	MIR_1	J07-D14	MIR_4	J06-D14
	MIR_4	J06-D14	MIR_3	J05-D14
MTRANEN--1	MIR_3	J05-D14	MIR_2	J04-D14
MOUTPEN--1	MC	J15-B30	MIR_8	J11-C17
	MIR_8	J11-C17	MIR_7	J10-C17
	MIR_7	J10-C17	MIR_6	J09-C17
	MIR_6	J09-C17	MIR_5	J08-C17
	MIR_5	J08-C17	MIR_1	J07-C17
	MIR_1	J07-C17	MIR_4	J06-C17
	MIR_4	J06-C17	MIR_3	J05-C17
MOUTPEN--1	MIR_3	J05-C17	MIR_2	J04-C17
MPTWSEL--1	MC	J15-A21	MIR_8	J11-B42
	MIR_8	J11-B42	MIR_7	J10-B42
	MIR_7	J10-B42	MIR_6	J09-B42
	MIR_6	J09-B42	MIR_5	J08-B42
	MIR_5	J08-B42	MIR_1	J07-B42
	MIR_1	J07-B42	MIR_4	J06-B42
	MIR_4	J06-B42	MIR_3	J05-B42
MPTWSEL--1	MIR_3	J05-B42	MIR_2	J04-B42
MIOWSEL--1	MC	J15-C21	MIR_5	J11-D44
	MIR_8	J11-D44	MIR_7	J10-D44
	MIR_7	J10-D44	MIR_6	J09-D44
	MIR_6	J09-D44	MIR_5	J08-D44
	MIR_5	J08-D44	MIR_1	J07-D44
	MIR_1	J07-D44	MIR_4	J06-D44
	MIR_4	J06-D44	MIR_3	J05-D44
MIOWSEL--1	MIR_3	J05-D44	MIR_2	J04-D44

Table 21B: Address and Control Signals List

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MEOBIT--L1	MC	J15-D32	MIR_8	J11-B44
	MIR_8	J11-B44	MIR_7	J10-B44
	MIR_7	J10-B44	MIR_6	J09-B44
MEOBIT--L1	MIR_6	J09-B44	MIR_1	J08-B44
MEIBIT--L1	MC	J15-D36	MIR_5	J07-B44
	MIR_5	J07-B44	MIR_4	J06-B44
	MIR_4	J06-B44	MIR_3	J05-B44
MEIBIT--L1	MIR_3	J05-B44	MIR_2	J04-B44
MSMIRP8--1	MT_2	J13-B20	MIR_7	J10-C47
7		-C05	MIR_1	J08-C47
6		-A21	MIR_4	J06-C47
5	MT_2	J13-B14	MIR_2	J04-C47
4	MT_1	J12-B06	MIR_8	J11-C47
3		-D08	MIR_6	J09-C47
2		-A15	MIR_5	J07-C47
MSIMRP1 --1	MT_1	J12-A09	MIR_3	J05-C47
MIOROSL--1	MC	J15-A23	IO_1	J01-70
	IO_1	J01-70	IO_2	J02-70
MIOROSL--1	IO_2	J02-70	IO_3	J03-70
MIOROSL--3	IMC	J15-C23	IO_4	J04-70
	IO_4	J04-70	IO_5	J05-70
MIOROSL--3	IO_5	J05-70	IO_6	J06-70
MCURTSL--1	MC	J15-B14	IO_1	J01-72
	IO_1	J01-72	IO_2	J02-72
MCURTSL--1	IO_2	J02-72	IO_3	J03-72
MCURTSL--3	MC	J15-A15	IO_4	J04-72
	IO_4	J04-72	IO_5	J05-72
MCURTSL--3	IO_5	J05-72	IO_6	J06-72
MSMIRPL--1	MT_1	J12-C15	MT_1	J12-D12
MSMIRPL--0	MT_1	J12-C17	MT_2	J13-D12

Table 21C: Address and Control Signals List

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
MEOBIT--L1	MT_1	J12-A05	MC	J15-D32
MEIBIT--L1		-C03		-D36
MWPROTP--1		-A35		-A41
MWINITP--1	MT_1	J12-C23		-B24
PYW-W05--0	UC	J16-B08		-B42
06		J16-A09		-B44
07		J17-B08		-A45
PYW-W08--0	UC	J17-A09		-C39
MCABCLR--0	POWR	J25-E		-C29
MCURSEL-L1	MT_2	J13-A05		-C11
MIORSEL-L1	MT_2	J13-C05		-B18
MTEFFS---0	MT_1	J12-B48		-B26
MTSFFS---0	1	J12-B30		-B12
MLCFFR---0	2	J13-B36		-D26
MTSFFR---0	2	-A39		-B06
MTEFFR---0	2	-A29		-D14
MOEFFS---0	2	-B48		-A11
MOSFFS---0	2	J13-B30		-A09
MOSFFR---0	3	J14-A39		-C05
MOEFFR---0	MT_3	J14-A29	MC	J15-B08
MZTPWCW--0	MC	J15-B20	MT_1	J12-A41
MSTROBE--1	MC	J15-A05	IO_1	J01-04
MSTROBE--1	IO_1	J01-04	IO_4	J04-04
MCURSEL--1	MC	J15-C45	MT_2	J13-A03
MIORSEL--1		-C15	MT_2	J13-B02
MIMCTNP--1	MC	J15-C41	MT_1	J12-A11
MIMCTNP--1	MT_1	J12-	MT_1	J12-
MIMCTRP--1	MT_1	J12-B24	MT_2	J13-A11
MIMCTSP--1	MT_2	J13-B24	MT_3	J14-A11
MSCUIOP--1	MT_1	J12- A33	MT_2	J13-A23

Table 21D: Address and Control Signals List

SIGNAL NAME	SOURCE OF SIGNAL		DESTINATION OF SIGNAL	
	Major Component	Connector & Pin	Major Component	Connector & Pin
-0.4v	MC	J15-A47	MC	J15-C47
-0.4v	MC	J15-C47	MT_3	J14-A41
-0.4v	MT_3	J14-A41	MT_2	J13-A41
-0.4v	MT_2	J13-A41	MT_1	J12-B08
-0.4v source	MT_1	J12-B08	MT_1	J12-C41

Table 21E: Address and Control Signals List

SIGNAL NAME	P E M X		P E M	
	Backplane Pin Number	Connector & Pin Number	Paddle Board	Pin Number
MOWFW00--1	1302-08	J5A-C45	P2	-109
01	1302-19	-D44		-110
02	1402-08	-C41		-112
03	1402-20	-C39		-113
04	1302-09	-D36		-115
05	1302-18	-C35		-116
06	1402-07	-C27		-121
07	1402-21	-D26		-122
40	1102-13	-D24		-123
41	1102-20	-C23		-124
42	1202-14	-C21		-125
43	1202-22	-D20		-126
44	1102-12	-C17		-128
45	1102-22	-C15		-129
46	1202-11	-D14		-130
47	1202-23	-D12		-131
48	1102-38	-C11		-132
49	1102-49	-C09		-133
50	1202-38	-D08		-134
51	1202-50	-D06		-135
52	1102-39	-C05		-136
53	1102-48	-C03		-137
54	1202-37	J5A-D02		-138
55	1202-51	J6A-B48		-139
56	1102-43	-A47		-140
57	1102-50	-A45		-141
58	1202-44	-B44		-142
59	1202-52	-B42		-143
60	1102-42	-A27		-153
61	1102-52	-B26		-154
62	1202-41	-A35		-148
MOWIW63--0	1202-53	J6A-A33	P2	-149

Table 22A: WRITE data from PEMX to PEM (OUTER WORD)

SIGNAL NAME	P E M X		P E M	
	Backplane Pin Number	Connector & Pin Number	Paddle Board	Pin Number
MOWFW08--1	1302-13	J5A-A45	P1	-109
09	1302-20	-B44		-110
10	1402-14	-A41		-112
11	1402-22	-A39		-113
12	1302-12	-B36		-115
13	1302-22	-A35		-116
14	1402-11	-A27		-121
15	1402-23	-B26		-122
16	1302-38	-B24		-123
17	1302-49	-A23		-124
18	1402-48	-A21		-125
19	1402-50	-B20		-126
20	1302-39	-A17		-128
21	1302-38	-A15		-129
22	1402-37	-B14		-130
23	1402-51	-B12		-131
24	1302-43	-A11		-132
25	1302-50	-A09		-133
26	1402-44	-B08		-134
27	1402-52	-B06		-135
28	1302-42	-A05		-136
29	1302-52	-A03		-137
30	1402-41	-B02		-138
31	1402-53	J4A-D48		-139
32	1102-08	-C47		-140
33	1102-19	-C45		-141
34	1202-08	-D44		-142
35	1202-20	-D42		-143
36	1102-09	-C27		-153
37	1102-18	-D26		-154
38	1202-07	-C35		-148
MOWIW39--0	1202-21	J4A-C33	P1	-149

Table 22B: WRITE data from PEMX to PEM (INNER WORD)

SIGNAL NAME	PEMX		PEM	
	Backplane Pin Number	Connector & Pin Number	Paddle Board	Pin Number
MIWFW00--1	1302-05	J6A-A21	P2	-157
01	1302-23	-B20		-158
02	1402-04	-A23		-156
03	1402-18	-B24		-155
04	1302-35	-A15		-161
05	1302-53	-A17		-160
06	1402-34	-B12		-163
07	1402-48	-A11		-164
40	1102-07	-B06		-167
41	1102-25	-B08		-166
42	1202-13	-D30		-183
43	1202-28	-D32		-182
44	1102-37	-A05		-168
45	1102-55	-A03		-169
46	1202-43	-D44		-174
47	1202-58	-C45		-173
48	1102-06	-C41		-176
49	1102-24	-C39		-177
50	1202-01	-C35		-180
51	1202-17	-D36		-179
52	1102-36	-C23		-188
53	1102-54	-C21		-189
54	1202-31	-C27		-185
55	1202-47	-D26		-186
56	1102-15	-D14		-194
57	1102-29	-D12		-195
58	1202-06	-C17		-192
59	1202-24	-D18		-191
60	1102-45	-C03		-201
61	1102-59	-C05		-200
62	1202-36	-C09		-197
MIWFW63--0	1202-54	J6A-D08	P2	-198

Table 23A: READ data from PEM to PEMX (OUTER WORD)

SIGNAL NAME	PEMX		PEM	
	Backplane Pin Number	Connector & Pin Number	Paddle Board	Pin Number
MIWFW08--1	1302-07	J4A-C21	P1	-157
09	1302-25	-D20		-158
10	1402-13	-C23		-156
11	1402-28	-D24		-155
12	1302-37	-C15		-161
13	1302-55	-C17		-160
14	1402-43	-D12		-163
15	1402-58	-C11		-164
16	1302-06	-D06		-167
17	1302-24	-D08		-166
18	1402-01	-B30		-183
19	1402-17	-B32		-182
20	1302-36	-C05		-168
21	1302-54	-C03		-169
22	1402-31	-B42		-174
23	1402-47	-A45		-173
24	1302-15	-A41		-176
25	1302-29	-A39		-177
26	1402-06	-A35		-180
27	1402-24	-E36		-179
28	1302-45	A23		-188
29	1302-59	-A21		-189
30	1402-36	-A27		-185
31	1402-54	-B26		-186
32	1102-05	-B14		-194
33	1102-23	-B12		-195
34	1202-04	-A17		-192
35	1202-18	-B18		-191
36	1102-35	-A03		-201
37	1102-53	-A05		-200
38	1202-34	-A09		-197
MIWFW39--0	1202-48	J4A-B08	P1	-198

Table 23B: READ data from PEM to PEMX (INNER WORD)

SIGNAL NAME	PEMX		MLU (IO)	
	Connector Number	Pin Number	Connector Number	Pin Number
MOWCW00--0	J4B	-A03	J06	-08
01		-B08		-14
02		-B12		-20
03		-A17		-26
04		-A21		-32
05		-B26		-38
06		-B30		-44
07	J4B	-A35	J06	-50
40	J5B	-C39	J03	-56
41		-D44		-62
42	J5B	-D48	J03	-68
43	J6B	-A03	J02	-08
44		-B08		-14
45		-B12		-20
46		-A17		-26
47		-A21		-32
48		-B26		-38
49		-B30		-44
50		-A35		-50
51		-A39		-56
52		-B44		-62
53		-B48	J02	-68
54		-C03	J01	-08
55		-D08		-14
56		-D12		-20
57		-C17		-26
58		-C21		-32
59		-D26		-38
63		-D30		-44
61		-C35		-50
62		-C39		-56
MOWCW63--0	J6B	-D44	J01	-62

Table 24A: CUB READ/TRANSFER data from MLU (IO) to PEMX (OUTER WORD)

SIGNAL NAME	P E M X		M L U (IO)	
	Connector Number	Pin Number	Connector Number	Pin Number
MOWCW08--0	J4B	-A39	J06	-56
09		-B44		-62
10		-B48		-68
11		-C03	J05	-08
12		-D08		-14
13		-D12		-20
14		-C17		-26
15		-C21		-32
16		-D26		-38
17		-D30		-44
18		-C35		-50
19		-C39		-56
20		-D44		-62
21	J4B	-D48	J05	-68
22	J5B	-A03	J04	-08
23		-B08		-14
24		-B12		-20
25		-A17		-26
26		-A21		-32
27		-B26		-38
28		-B30		-44
29		-A35		-50
30		-A39		-56
31		-B44	J04	-62
32		-C03	J03	-08
33		-D08		-14
34		-D12		-20
35		-C17		-26
36		-C21		-32
37		-D26		-38
38		-D30		-44
MOWCW39--0	J5B	-C35	J04	-50
MZTMWIW--0	J6B	-C47	J01	-65
MZTMWCW--0	J5B	-B48	J04	-68
MZTMWCW--2	J6B	-D48	J01	-68

Table 24B: CUB READ/TRANSFER data from MLU (IO) to PEMX (INNER WORD)

SIGNAL NAME	P E M X		M L U (IO)	
	Connector Number	Pin Number	Connector Number	Pin Number
MOWIW00--0	J4B	-B02	J06	-05
01		-B06		-11
02		-A11		-17
03		-A15		-23
04		-B20		-29
05		-B24		-35
06		-A29		-41
07	J4B	-A33	J06	-47
40	J5B	-D38	J03	-53
41		-D42		-59
42	J5B	-C47	J03	-65
43	J6B	-B02	J02	-05
44		-B06		-11
45		-A11		-17
46		-A15		-23
47		-B20		-29
48		-B24		-35
49		-A29		-41
50		-A33		-47
51		-B33		-53
52		-B42		-59
53		-A47	J02	-65
54		-D02	J01	-05
55		-D06		-11
56		-C11		-17
57		-C15		-23
58		-D20		-29
59		-D24		-35
60		-C29		-41
61		-C33		-47
62		-D38		-53
MOWIW63--0	J6B	-D42	J01	-59

Table 25A: IOSS READ/WRITE data from PEMX to MLU (IO) (OUTER WORD)

SIGNAL NAME	P E M X		M L U (IO)	
	Connector Number	Pin Number	Connector Number	Pin Number
MOWIW08--0	J4B	-B38	J06	-53
09		-B42		-59
10		-A47	J06	-65
11		-D02	J05	-05
12		-D06		-11
13		-C11		-17
14		-C15		-23
15		-D20		-29
16		-D24		-35
17		-C29		-41
18		-C33		-47
19		-D38		-53
20		-D42		-59
21	J4B	-C47	J05	-65
22	J5B	-B02	J04	-05
23		-B06		-11
24		-A11		-17
25		-A15		-23
26		-B20		-29
27		-B24		-35
28		-A28		-41
29		-A33		-47
30		-B38		-53
31		-B42	J04	-59
32		-D02	J03	-05
33		-D06		-11
34		-C11		-17
35		-C15		-23
36		-D20		-29
37		-D24		-35
38		-C29		-41
MOWIW39--0	J5B	-C33	J03	-47

Table 25B: IOSS READ/WRITE data from PEMX to MLU (IO) (INNER WORD)

SIGNAL NAME	PEMX		PEM	
	Backplane Pin Number	Connector & Pin Number	Paddle Board	Pin Number
MYW-W05--0	1304-55	J4A-C39	P1	-145
06	1304-49	J6A-C33	P2	-181
07	1304-43	J4A-B38	P1	-178
08	1404-38	J6A-D42	P2	-175
09	1404-44	J4A-A47	P1	-172
10	1404-37	J6A-C29	P2	-184
11	1304-54	J4A-B24	P1	-187
12	1304-48	J6A-D06	P2	-199
13	1404-43	J4A-A11	P1	-196
14	1404-48	J6A-C15	P2	-193
MYW-W15--0	1404-50	J4A-B20	P1	-190
MINITPL--1	1304-36	J6A-B36	P2	-147
MWOUTEN--1	1304-38	J6A-B30	P2	-151
MWINNEN--1	1304-42	J4A-D38	P1	-146

Table 26: Address and Control Signals from PEMX to PEM

MLU		PEM		PEMX	
CONNECTOR NUMBER	MAJOR COMPONENT	PADDLE BOARD	MAJOR COMPONENT	CONNECTOR NUMBER	REMARKS
J31 (J1)	IO1	P1	INNER WORD part of connector base	J1	1) MLU Connectors J26 thru J31 will be found as connectors J6 thru J1 respectively in tables 24 & 25
J30 (J2)	IO2			J2	
J29 (J3)	IO3			J3	
J28 (J4)	IO4			J4A	
J27 (J5)	IO5			J4B	
J26 (J6)	IO6	P2	OUTER WORD part of connector base	J5A	
				J5B	
J4	MIR2			J6A	2) In MLU there are connectors J19,J20, J21 to connect with PE connectors MLU1, MLU2, MLU3 respectively when PU (system) is not on PEMX
J5	MIR3			J6B	
J6	MIR4				
J7	MIR5				
J8	MIR1				
J9	MIR6				
J10	MIR7				
J11	MIR8				3) In MLU there are connectors J22,J23, J24 to connect with PEM Paddle Boards P1&P2 when PU (system) is not on PEMX
J12	MT1				
J13	MT2				
J14	MT3				
J15	MC				4) When testing PEM on PEMX, PEM Paddle Boards P1&P2 are connected to PEMX connectors J4A, J5A, and J6A
J16	UC1				
J17	UC2				
J18	UC3				
					5) When PU(system) is on PEMX, MLU connectors J26 thru J31 are connected to PEMX connectors J48,J58, J68 and MLU connectors J19 thru J21 are connected to PEMX connectors J1, J2, and J3

Table 27: List of MLU Connectors and Corresponding Major Components

APPENDIX C

CONNECTOR CONFIGURATION

PIN SIDE VIEW

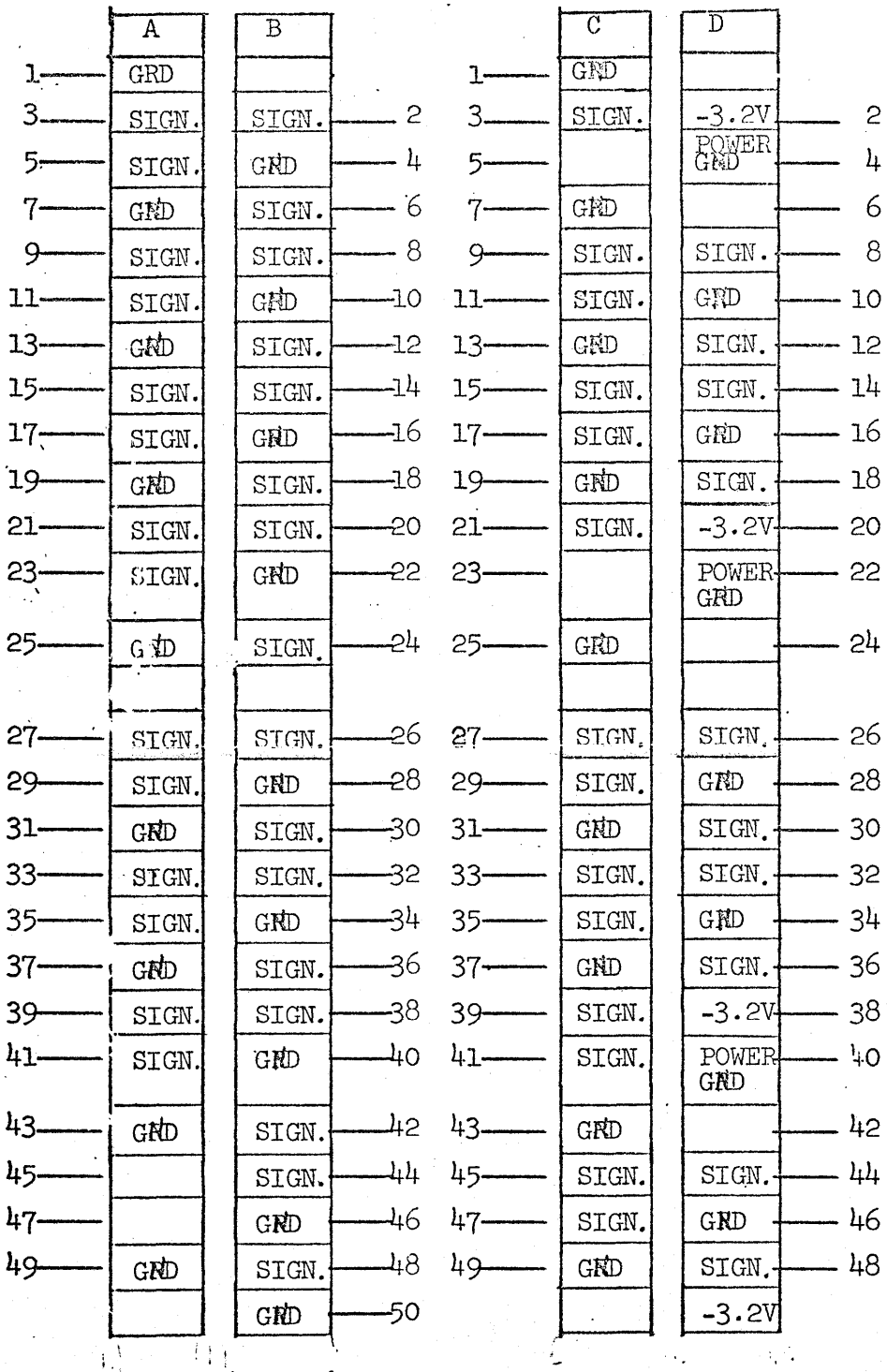


Figure 12: Pin Configuration of PE/MLU Connector

Remarks: 1. Pins A45 & 47 are used for signal in all PE/MLU cards, but in MIR cards they are used for +4.8V.

2. Pins C5 & 23 are used for signal in all PE/MLU cards, but in UC cards they are used for +4.8V.

3. Pins D6, D24, and D42 are used for +1.32V in all PE/MLU cards but in UC cards they are used for +4.8V.

4. SIGN. stands for Signal.

5. GND. stands for Ground.

CARD SIDE VIEW

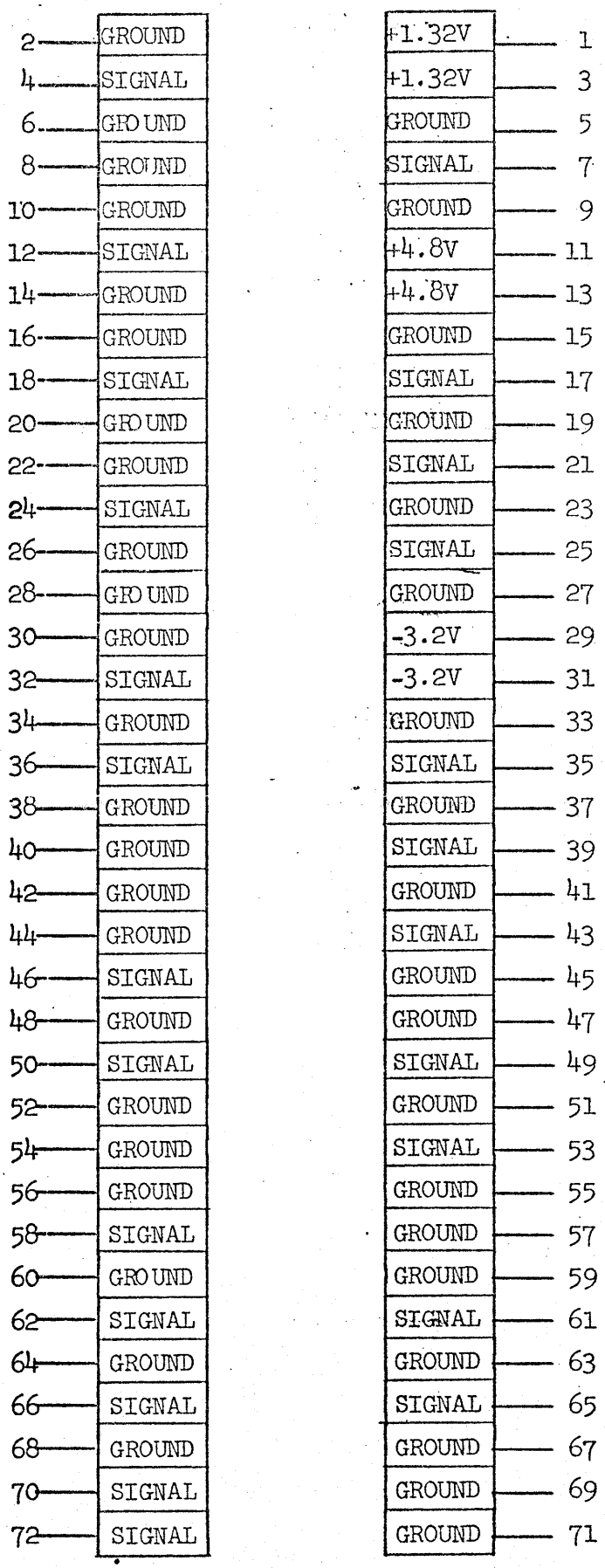


Figure 13: Pin Configuration of MLU (IO card) Connector