REVISIONS

SYM	DESCRIPTION	APPROVED	DATE
X	PROTOTYPE RELEASE		
X₁	REVISED FOR READ CLOCK CHANGE	D.E.P.	5/15/74
X2	REVISED TO INCLUDE E3004	RMK.	7/17/74
X3	ADDED ONE SHOT TIMING SHT. 34	RMK	9/3/74

PROTOTYPE

G.M. Watson, Director
Software Development and Support

T.H. Sweere, Director
Systems Engineering

DR C. Towner	10-19-72
CHK	
DSGN Sam Nooriala	10-20-72
ENGR Sam Nooriala	10-20-72
APPD	3/2/73
APPD	

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TITLE

ENGINEERING DESCRIPTION
9-TRACK PHASE ENCODED
MAG TAPE SYSTEM
E2053, E3004

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21101	A	98A0885	X3
SCALE			SHEET 1 OF 45

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ENGINEERING DATA FORM

OPTION	PE Mag Tape System
MODEL	620-E2053, E3004
NO. OF LOGIC CARDS REQ'D.	2
NO. OF CARD SLOTS REQ'D.	6
LOCATION OF SLOTS (NUMBERING)	-
CONNECTORS REQ'D. (EXCLUDING I/O)	-
KEYING	-
ST'D. DEVICE ADDRESS	10
WIRELIST NUMBER	95W0971 Controller, 95W0969 Formatter
MANUAL PUBLICATIONS NUMBER	98A0885
PERIPHERAL EQUIPT. REQ'D	PE Mag Tape Unit
MFG'R.	Pertec/Wangco
MODEL	
GEN'L. SPECS	See Section 2

NOTES:

Reference Drawings:	
95W0971	AWW List Controller Board
98A0885	Engineering Description
53A0712	Cable Assy. Cont. to Drive
53A0711	Cable Assembly Formatter to Drive
91C0425	Logic Diagram, Controller
92A0107-037	Standard Test Program
89A0247	Test Program SPS
91C0424	Logic Diagram, Formatter
95W0969	AWW List Formatter Board
01A1481	Top Assy. Formatter & Controller
44A0666	Assy. & Parts List Controller
44A0667	Assy. & Parts List Formatter
95W0973	Wire List Cable Assy. Controller
95W0972	Wire List Cable Assy. Formatter

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SECTION 1
INTRODUCTION

1.1 PURPOSE

This document provides the engineering description for the interface between the 620 series computers and the Phase Encoded 1600 BPI Magnetic Tape Transport.

1.2 DESCRIPTION

The interface is physically constructed on two Multipurpose socket boards.

1.2.1 Functional Description (Controller)

The controller accepts standard 620 I/O commands from the CPU and connects data and control signals to and from the formatter.

The controller performs the following basic functions:

1. Accepts EXC Commands from the CPU and converts them to motion control signals.

2. Monitors status signals from the formatter to enable sense responses to the CPU.

3. During write commands, generates IBM compatible ID bursts, preambles, postambles, file marks, and data records in 9 track, 1600 BPI, phase encoded format.

4. Accepts data from the CPU via the DMA channel and converts each 16 bit word to two-eight bit + odd parity bytes for transmission to the formatter.

5. Accepts byte oriented data from the formatter and organizes it into 16 bit words for transmission to the CPU via the DMA channel under BIC control.

1.2.2 Functional Description (Formatter)

The basic functions performed by the formatter are:

1. Accepting write data from the controller.

2. Converting this data to phase encoded format.

3. Accepting read P.E. information from tape drives.

4. Tracking the variations in read data rate.

5. Decoding the P.E. data into NRZ form.

6. Deskewing the data received from the 9 channels.

7. Checking parity on this data.

8. Checking for format errors and bad preamble or postamble.

9. Generating data strobes for read data to the controller.

10. General timing and control functions.

1.2.3 Interface Description

The interface between the formatter and the tape drive is all DTL/TTL compatible logic using DIP integrated circuits.

1.3 PREREQUISITES

A 620-20 (BIC) Buffered Interlace Controller is required at or above 75 IPS operation. Slower mag tape units may not require a BIC. Depending on system and software requirements, optimum operation is achieved with a BIC in all cases.

1.3.1 Model Numbers

E-2053A = Tape unit and controller, 9 track, RAW, 37-1/2 IPS, 1600 BPI,
Phase Encoded, (Pertec model no. 6640-9-37.5).

E-2053B = As above, but rate is 75 IPS (Pertec model no. 6640-9-75).

E-2053C = Slave tape unit and cables for E-2053-A

E-2053D = Slave tape unit and cables for E-2053-B

E-3004I = Magnetic tape unit and controller, 9 trk., phase encoded, 1600 BPI,
75 IPS, RAW, vacuum buffered.

E-3004K = Same as I except 45 IPS (model 1145)

E-3004J = Slave unit and cables for E-3004I

E-3004L = Slave unit and cables for E-3004K

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SECTION 2
SPECIFICATIONS

2.1   CONTROLLER SPECIFICATIONS

2.1.1   Physical Specification

Model   E-2053/E-3004

Size   Two 7-3/4 x 13-1/2 in. socket boards

Connectors   One 122 pin card edge connector on controller
                               board connects to CPU I/O bus. It also connects
                               to formatter board 122-pin connector as described
                               in installation section.

                               One 44 pin card edge connector per board connects
                               to tape drive.

2.1.2   Functional/Electrical Specifications

I/O Channel Loading   This controller presents one TTL load (1.6 ma)
                               to the 620 I/O channel signals. The formatter
                               board presents no loads to the I/O channel.

Logic Levels

   I/O Channel Interface   Logic zero   =   +3+ .5V DC
                               Logic one   =   0+ .5V DC

   Internal   Logic zero   =   0+ .5V DC
                               Logic one   =   2.4V DC

   Controller Drive Interface Logic zero   =   2.4V DC
                               Logic one   =   0+ .5V DC

Power Requirements   Controller +5V DC @ 1.8 a
                               Formatter +5V DC @ 2 a

Environment

   Operational   +10 to +45° C, 10 to 90% humidity with
                               no condensation

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Storage   0 to +55° C, 0 to 90% humidity with no
                                           condensation

2.2 TAPE TRANSPORT SPECIFICATION

Model Number	Reel Size	Packing Density (Character/Inch)	Character Transfer Rate	No. of Channels
6640 Pertec 11XX Wangco	10.5"	1600	20 – 120 KHz (Dependent on Tape Speed)	9

2.2.1 Functional Characteristics

The transport can record 9 track, 1600 CPI Phase Encoded USASCII and IBM format compatible magnetic tape recordings capable of being reliably read by any 9 track USASCII and IBM compatible tape transport.

The tape transport can reliably read any 9 track Phase Encoded magnetic tape that has been recorded in USASCII and IBM compatible format.

The transport provides Read After Write and Erase capability.

2.2.2 Mechanical and Electrical Specifications

2.2.2.1 Tape

The tape used is computer grade certified at 1600 CPI. IBM part number 457893 or equivalent.

The tape width is 0.498 +0.002 inches.

The tape thickness is nominally 1.5 mil.

The tape tension is nominally 8 ounce in the normal data transfer mode and in the rewind mode.

2.2.2.2 Reels

The transport can accept reels up to a diameter of 10.5 inches.

2.2.2.3 Motion Characteristics

Various versions of the transport can operate at each of the following standard speeds: 75 ips, 45 ips, 37.5 ips, 25 ips, 18.75 ips, and 12.5 ips.

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The long term speed variation in the forward direction is $\pm 1\%$ of the specified speed.

The speed in the reverse direction may differ from that in the forward direction by $\pm 3\%$.

The instantaneous speed variation is $\pm 1\%$ at speeds from 12.5 ips to 37.5 ips and $\pm 2\%$ at 45 ips.

The start and stop time of the transport is 8 ± 0.55 msecond at 45 ips and is inversely proportional to speed.

The start and stop displacement of the transport is 0.19 ± 0.02 inches.

The transport has a rewind speed of 150 ips. For further detailed specifications, refer to MTU manual supplied with each unit.

2.2.2.4   Interchannel Displacement Error

The maximum displacement between any two bits of a character when reading an IBM master tape in the forward direction and using the WRITE section of the Read After Write stack is 200μ inches.

The maximum displacement between any two bits of a character when reading an IBM master tape in the forward direction and using the READ section of the Read After Write stack is 400 μ inches.

2.2.2.5   Program Restrictions

There are no program restrictions for the capstan and reel servos. However, to preserve the normal Start/Stop times and distances, and to guarantee complete erasure of the gaps, the customer should ensure that the tape motion has ceased before changing the direction of the Read/Write status.   (See Section 4.2.8).

2.2.2.6   Magnetic Tape Head

The transport has a dual stack Read-After-Write head, with a separation of $0.150 \pm .005$ inch.

An erase head mounted to the Read-After-Write stack provides a full width erase capability. The separation between the Write and Erase gaps is nominally 0.34 inch.

2.2.2.7   EOT/BOT Detection

The transport has a photo electric EOT/BOT detector suitable for detecting IBM compatible EOT/BOT tabs.

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The detector is located approximately 1.2 inches from the center of the Read–After–Write head. This enables IBM compatible tapes to be recovered and read.

2.2.2.8   Tape Cleaner

The transport has a tape cleaner consisting of a curved perforated plate.

The tape cleaner is located between the supply reel and the supply tension arm.

2.2.2.9   Physical Description

	E-2053	E-3004
Height	24.0 inches	24.0 inches
Width	19.0 inches	19.0 inches
Depth from Mounting Surface	12.5 inches	19.0 inches
Mounting	19.0 inches consistent with EIA requirements	
Weight	85 pounds	160 pounds

A 1/2 inch filler panel is provided to make up a total height of 24.5 inches.

2.2.2.10   Power

The transport power transformer is provided with the following nominal input voltage combinations:

105, 115, 125, 210, 220, 230, 240, and 250

The system can accept variations of the mean voltage up to ± 10%.

The transport operates on AC power at any frequency between 48 to 62HZ.

The system requires 400 watts maximum power. (E2053) and 850 watts (E3004).

2.2.2.11   Electronics

All silicon.

The transport is designed to qualify for UL Approval.

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2.2.3	Environmental

2.2.3.1	Non-Operating

Temperature $\qquad$ −45°C (−50°F) to 71°C (160°F)

Altitude $\qquad$ 0 to 50,000 feet

Shock $\qquad$ The unit withstands shock and vibration encountered during normal installation, maintenance, and shipping. Shipping package conforms to the National Safe Transit Committee Pre-Shipment Test Procedure.

2.2.3.2	Operating

	E-2053	E-3004
Temperature	2°C (35°F) to 50°C (122°F)	
Altitute	0 to 20,000 feet	0 to 5,000 ft.
Humidity	15% to 95% (without condensation)	

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3.1 THEORY OF OPERATION (CONTROLLER)

In the following theory of operation, reference is made to the 91C0425 logic diagram sheet numbers and the more complex parts are described in detail.

The basic instructions used for communication between the controller and the computer are listed below.

WOR	(Write One Record)
WFM	(Write File Mark)
ROR	(Read One Record)
FOR	(Forward One Record)
BOR	(Backspace One Record)
RWND	(Rewind)

A set of 8 sense commands are provided.

The following sections discuss the sequence of events taking place within the logic for each of these commands.

3.1.1 WOR Command

The command is stored in a F/F shown on sheet 3 of the schematics. Immediately upon issuance of a command, a reset pulse, $\overline{TWRP}$, is generated. The $\overline{WOR}$ condition sets the Forward Drive F/F after the reset pulse is issued. WOR also enables the gate, which controls the firing of inter-record gap O/S.

If the tape was just loaded, and the BOT marker is being detected, an identification burst must be written to identify the phase encoded format.

The I.D. burst consists of a series of flux reversals at 1600 (FRPI) in the parity channel with all other channels erased.

When the above conditions exist, the $\overline{ENID+}$ F/F is set high. This enables the 1600 BPI clock to be sent to the transport and at the same time forces a true level on the parity line. The trailing edge of BOT will fire the 4" I.D. O/S. When the O/S times out, ID DONE will set high and causes ENID to reset. This will remove the clocks and data on the parity line.

FIRG signal is now enabled and the IRG O/S is fired. This will cause an inter-record gap. When F/F IRG DON is set, clocks are sent to the drive gate. It also

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enables the character counter. Zeros are written on tape until the counter reaches the count of 40 (decimal). This will cause F/F ENALLON to set and force all data lines true for one character time. Thus, the preamble (40 zeros and 1 all one's) is written. At count 41 of the counter, F/F ENDATA will set, thus enabling the data strobe lines.

Since every command will reset the buffer empty F/F's, upon connection of the BIC interface to the device, two consecutive requests are made for data transfer out of the memory. This is done via the trap request F/F.

Thus, the two word buffers are full by the time we are ready for data transfer. When the data strobes are enabled on count 41 of the counter, the bytes are strobed consecutively onto the transport's I/O lines. Starting with the most significant byte of the first word. Refer to timing diagram (Fig. 1).

Everytime two consecutive characters are transferred, the buffer empty flag is set and a request is generated via the trap request F/F.

DTOX and DRY will set the new data into the empty buffer. Parity is generated by presenting each byte to a parity generator chip and applying the output to the data buffer.

When no more data is received from the computer, and both buffers are empty, F/F ENALLON sets and forces all one's on the data lines. This is the first character of the postamble and is followed by 40 zeros. ENALLON resets with the next WDCLK, but clocks to the transport are still enabled, until the signal TEIL (End of Information) is received from the transport. This signal is delayed for 0.5 ms and is used to remove the forward drive status. This completes the cycle for a WOR command.

If BOT was not present when the command was issued, the I.D. burst would not be written and the cycle would start by firing the I.R.G., O/S.

3.1.2 WFM Command

A file mark is defined as approximately 3.75" of erased tape followed by 80-256 flux changes in tracks 1,2,4,5,7, and 8 while channels 3,6, and 9 are erased.

If a WFM command is issued when BOT is under the sensor, the I.D. burst shall be written as described for the case of a WOR command and followed by a file mark. If not, a normal file mark is written as described here.

The command is stored and the forward F/F is set after a reset pulse is generated. At the same time, the FM O/S is fired, no clocks are enabled, and during this time the tape is erased. When the O/S times out, F/F FMGAPD sets high, which

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in turn sets ENFM to enable the clocks, force the file mark character on the data lines, and enables the 40 character counter. Forty characters of file mark are written. When the counter reaches count 40 (EN F.M. F/F) resets. TEIL (delayed) will stop the motion by removing forward drive line. Any time the forward drive F/F is reset, a STPM signal is generated, which will fire O/S STOPED. At the end of this 14ms, MINT F/F sets. This signal (MINT) is used to disconnect the BIC if it was connected during a WOR command.

3.1.3 ROR Command

This command is used to read one record of information into the memory.

The command is stored. The ROR F/F output sets the forward drive F/F to start forward motion. Nothing else will happen until the first clock pulse is received from the transport. The clocks are then applied to the circuits where they are separated into 4 different strobe pulses to strobe the data in the 4 storage registers. Starting from the second strobe pulse, every other one will set the buffer full F/F's.

Any of the two buffer full F/F's being set will result in a trap request, which will be followed by DTIX F/F being set. A F/F separates every other DTIX pulse, thus strobing the first or the second buffer. This information is directly presented on the E-Bus to the computer. This process will continue until no more clocks are received and the postamble is detected by the transport. The signal TEIL will then reset forward drive status and result in a motion interrupt to the computer.

3.1.4 FOR Command

This command is the same as the ROR command except no data will be sent to the computer during the execution of this command.

3.1.5 BOR Command

This command will be stored and will set the backward drive F/F. Tape motion will continue in the backward direction until TEIL is detected, which removes the backward drive line and is delayed to remove the command.

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3.1.6 RWND Command

When this command is issued, F/F TRWL will set if not at load point, which will set TRWL (rewind) line at the transport. The tape will start rewinding until the signal TRGL makes a negative to positive transition which will reset the TRWL drive F/F.

Figures 2 thru 5 are timing diagrams for the command sequences described above.

3.1.7 Clock Generator

This circuit consists of a crystal oscillator with a frequency of 11.52 MHZ, two presetable synchronous counters, and control circuits to load the predetermined binary count at the proper time. The jumper board will be changed for different tape speeds.

The two counters can count up to 256 (0-255). That is, the input clock frequency can be divided by 256.

If predetermined counts are loaded into the counters at certain intervals, this frequency division can be adjusted (reduced). For example, for 112.5 ips tape speed, we will need a clock rate of 360KHZ. To determine the jumper configuration for any desired frequency, we use the following formula:

$$N = \frac{\text{Base Freq. (11.52 MHZ)}}{2 \text{ X desired frequency}} - 1$$

Where N is the number in binary to be loaded into the counter (using jumpers to ground for one bits).

For the 112.5 IPS example:

$$N = \frac{11.52 \text{ MHZ}}{2 \text{ X 360 KHZ}} - 1 = \frac{11.52}{720} - 1 = 16 - 1 = 15$$

Thus, 15 is the number that should be made up with jumpers to ground and loaded into the counter.

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WCLK φ D φ D φ D φ D φ D φ D φ D φ D φ

D9-3

WDCLK D D D D D D D

EN ALLØN

ENDATA+

CLKBYT+   1ST   3RD.

CLKBYT−   2ND.   4TH

BYTEA+

BYTE B+

BYTE1   BYTE1

BYTE2   BYTE2

BYTE3   BYTE3

BYTE4   BYTE4
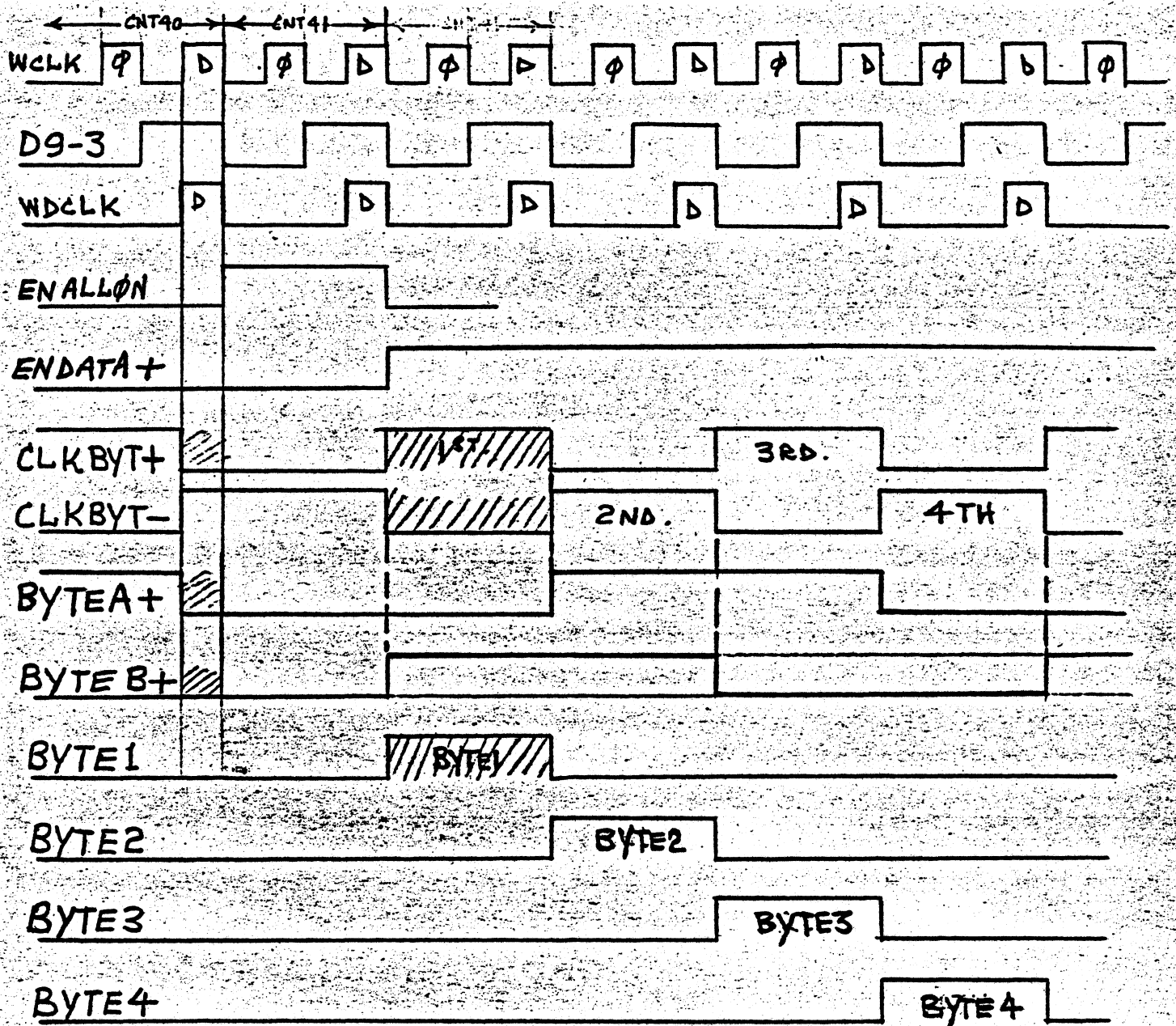
FIGURE 3.1
WRITE DATA XFER TIMING

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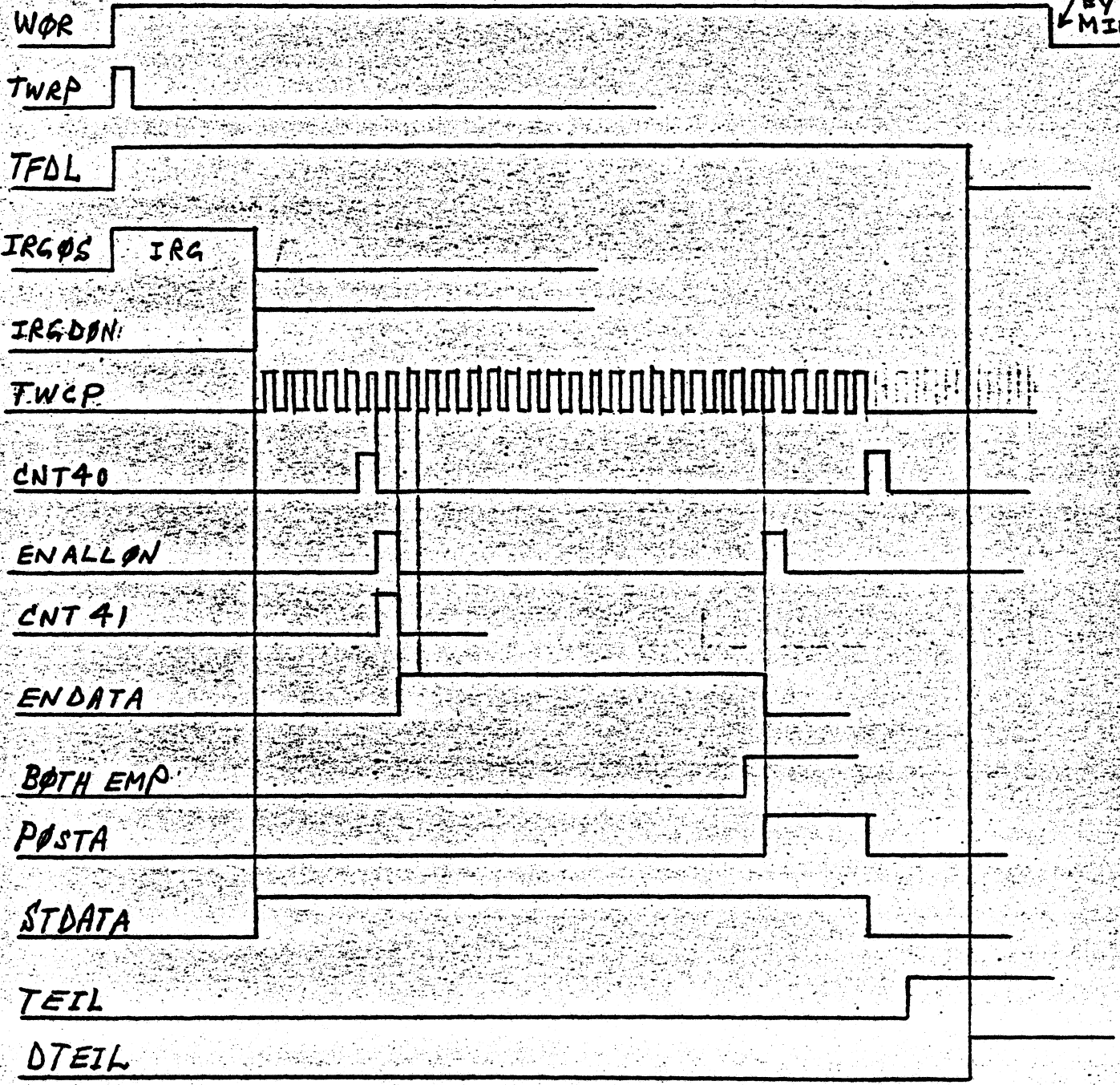
FIGURE 3.2
WOR COMMAND TIMING

WØR

BØT

TFDL

ENID

IDØS 4" O/S

IDDØNE

IRGØS IRG

←——— ID BURST ———→ ←——————— NORMAL WØR ———————→
REFER TO FIG. 3.2
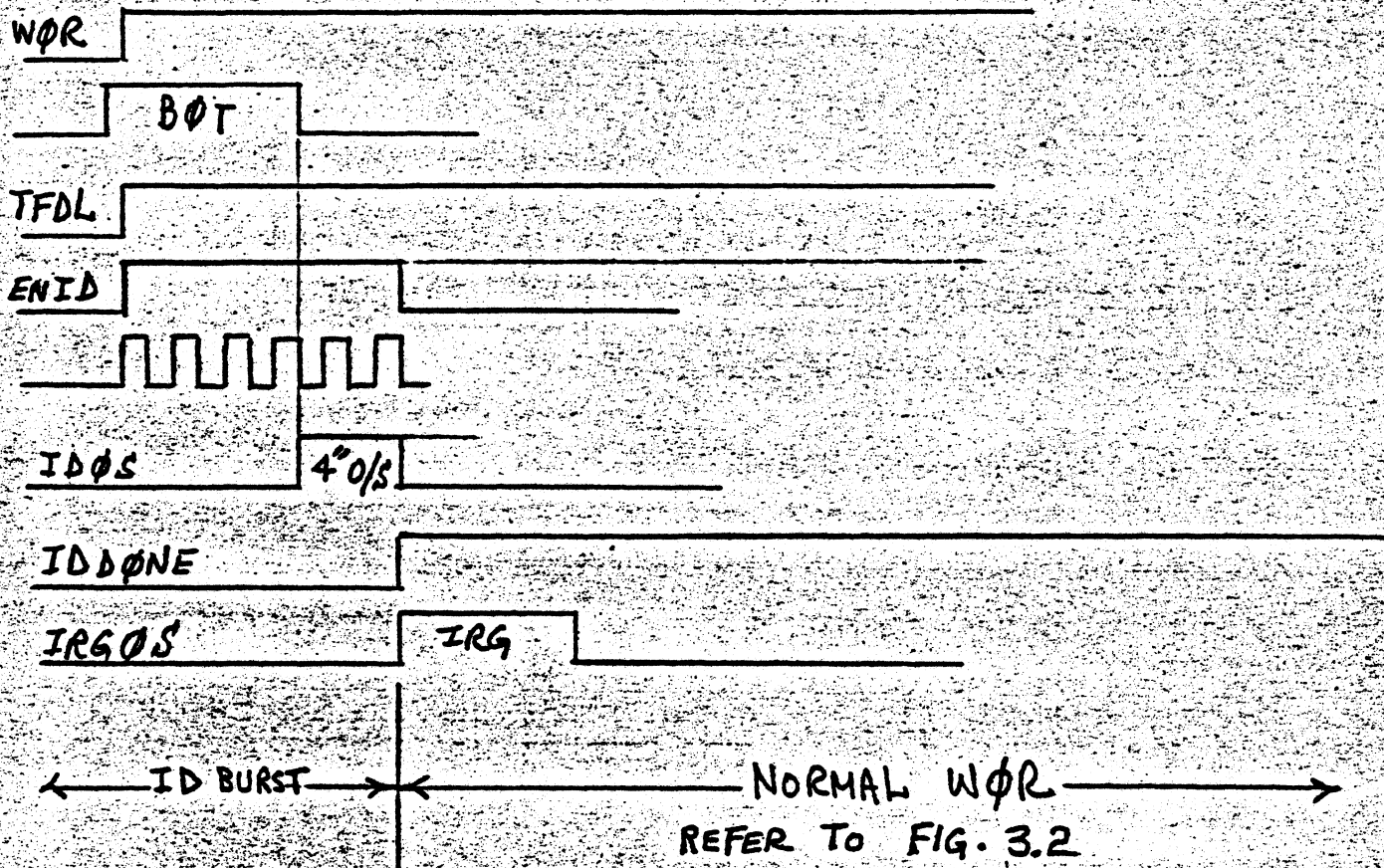
FIGURE 3.3
WOR COMMAND AT LOAD POINT

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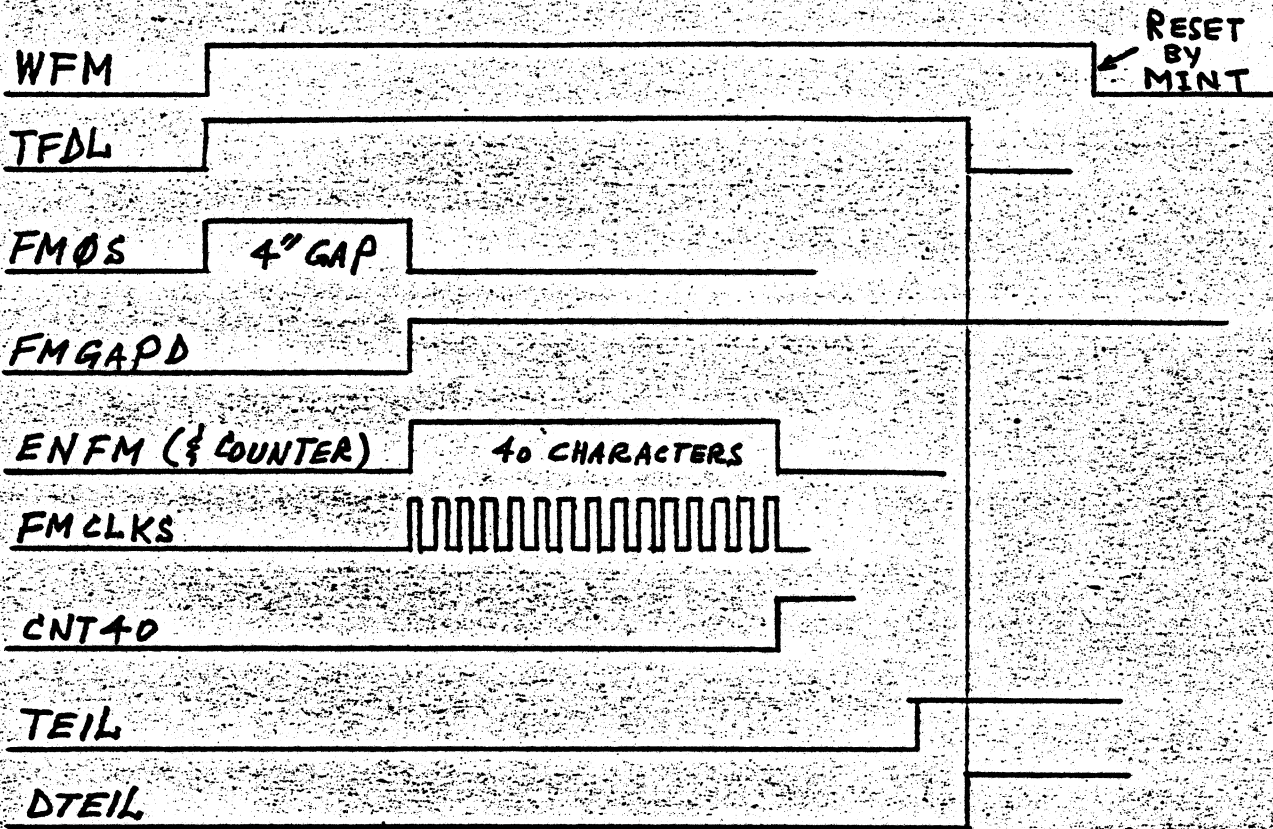
FIGURE 3.4
WFM COMMAND

BØR

TBDL

TEIL

DTEIL

STØPED (O/S)   14ms

MINT

BOR

RWND

TRWL

RGL

STØPED (O/S)   14ms

MINT

RWND

FIGURE 3.5 -   BACKSPACE AND REWIND

3.2   THEORY OF OPERATION (FORMATTER)

The logic diagram for the formatter consists of 3 sheets of general timing, control logic, and 9 sheets of identical circuitry for the 9 channels of tape information. In this theory of operation, reference will be made to the schematics and the title of each logic section contained therein. (Schematics drawing number 91C0424).

In order to understand this description, it is recommended that logic sections referred to be examined while reading the text.

3.2.1   Tracking Oscillator (VCO) Logic

A tracking oscillator is used to track instantaneous and long term variations in data rate due to tape speed variations and bit crowding effects. The logic consists of a variable frequency oscillator and a control logic, which is used to determine whether the oscillator should run faster or slower than the nominal rate. This is done by counting the number of clocks between data transitions.

The signal GATE 3 is a window generated from data on channel 3. This is the primary signal used for tracking. If channel 3 drops out, control is switched to channel 1. GATE 3 is high for 3/4 cell time or 18 clocks and low for 6 clock times. When this signal is low, the VCO control circuit is enabled to count the clocks. If the last stage of the counter is set before GATE 3 is set high again, F/F SPEED will be set. This will result in a decrease in clock frequency of the VCO.

The clock output of the VCO, which runs at 24 times the frequency of incoming data, is distributed throughout the logic for all nine channels of read data.

3.2.2   Sequencing and Control

The basic timing in the read mode is performed by the Read Sequencer and the Character Counter logic.

Each data record consists of a preamble, a data area, and a postamble. The Read Sequencer is used to determine which area of a record is being processed at any particular time (refer to timing diagram, Fig. 3.7).

When envelopes are detected, the character counter is enabled. When a count of 640 is reached, REP flip flop will set. This is 26 character times. REP stays set for one clock time and causes the sequencer SEQ 1 F/F to set. At this point, we are over half way through the preamble.

During the next four character times, a check is made to see if the preamble is truely all zero's. When count 96 is reached by the character counter, SEQ 2 will set by another REP pulse.

All channels are now enabled to look for the preamble all one character.

The channel logics will now take over until the postamble all one character is detected. This will cause SEQ 3 to set. During the next 26 characters, a check is made to see if the postamble is truly consisted of only zero's. After 26 character times, SEQ 4 will be set high. If, after the next 26 characters have been counted, envelopes have not been dropped, an error condition is detected. SEQ 5 will be set after the next 26 character count whether or not the error is detected. 26 character times later, ENDR F/F will be set indicating the end of the read sequence. SEQ 5 resets SEQ 2, SEQ 3, and SEQ 4. Similarly, ENDR resets SEQ 1 and SEQ 5.

3.2.3 Channel Logic

There are 9 identical sets of channel logic on 9 different sheets of schematics. Any one can be used for the purpose of this explanation.

Each channel logic consists of:

1.   A decoder circuit to decode P.E. data.

2.   A Deskew Buffer to allow for differences between channels.

3.   Envelope detector, drop out detector, and gating logic.

4.   A write coder to code write data into phase encoded format.

3.2.3.1 Decoder

The decoder circuit receives data or inverted data through the exclusive or circuit at the input. Two flip flops are used to determine the polarity of change of direction in input data. Two gates are used to detect ones and zeros. During the first half of the preamble, the ones gate is disabled, thus forcing the circuit to synchronize with preamble zeros.

Everytime a transition is detected, the flip flop (GATE) will be set. At the same time, a clock counter is reset to zeros. When this counter reaches a count of 16 (18 data clocks) (3/4 cell time), the GATE flip flop is reset. During the low portion of GATE, the polarity of change of the input data is checked to determine if a one or a zero is being read.

3.2.3.2 Deskew Logic

This logic consists of a 4 bit shift right/left register and a 5 bit shift register. Initially, the 4 bit register is cleared and 26 character times after the start of the preamble, the last stage of this register is set high. The signal SYNC keeps the 5 bit register reset until the first "ONE" is detected. This would be the all one

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character of the preamble.

The 4 bit register is used as a pointer, which points to the next empty location of the deskew buffer. After the detection of the "all one's" character, everytime a one or a zero is detected (a STROBE is generated), the 4 bit pointer register is shifted one place to the left, thus pointing to the next empty spot in the deskew register.

When all channels have detected at least one character, the signal CHFND (character found) is raised. This signal is sent to data control logic, shown together with sequencer logic, where it generates SRONE+ and DSTR (data strobe).

The signal SRONE+ generates SRCLK signal, which will shift the pointer one place to the right and the data in the deskew register out to the 5th position (EOUT). This is the data presented to the controller. This process is repeated throughout the record until the postamble is detected. This is done when the signal EOUT is high and DOUT is low for all nine channels including the parity track, signifying the "all one" character followed by the first all zero character of the postamble.

3.2.3.3   Write Coder Logic

Each channel contains a write coder. This circuit receives the clocks and data in NRZ form from the controller and codes this data into phase encoded form. (Refer to Figure 3.8).

3.2.4   File Mark Detection

A file mark is 40 zeros in channels 1,4, and 7 and no data in channels 2,6, and 5. Channels 3,8, and 9 could have either zeros or be erased.

28 character times after the start of data record, a REP+ pulse will set SEQ 1 and FM true if the file mark conditions are detected by the decode gates.

FM being true causes SEQ 5 to set. This will cause the character counter to reset, thus nothing else will happen until envelopes drop. This will enable the character counter again and 26 character times later ENDR is generated, which resets SEQ 5 and signals the end of read.

3.2.5   Identification Burst

When a read is initiated at BOT, the signal shown on sheet 3 of schematics (called ID TIME- from the controller board) goes low, disabling the signal ENVS+. Thus, the read sequencer and character counter will remain inactive.

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But the channel logic is enabled to detect individual envelopes. A check is made for data in channel 4 (Parity) and no data in other channels, since I.D. is a burst of alternate ones and zeros in parity track and no data in other tracks. After the signal IDITIME-is removed (at the end of the I.D. time out) by the controller board, the signal ENVS+ comes up and the next record is processed as usual.

3.2.6 Error Correction

The drop detection logic (sheet 3) determines if one or more envelopes have dropped.

If only one envelope has dropped, then the signal DRPED1+ is set true. This signal will set ERCOR flip flop. This will cause the parity bit, which is generated by all other channel outputs, to be sent as CORECT+ to the dropped channel. Thus, the parity correction bit is presented as the data from the dropped channel. (Refer to channel logic and signals generating RBX).

3.2.7 Error Detection

A number of error conditions detected will cause TERL flip flop to set. These conditions are:

    1.   Ones in preamble.

    2.   Ones in postamble.

    3.   Postamble "all one" character not found.

    4.   False postamble detected.

    5.   Two or more channels dropped.

The explanation for each of the above conditions follows.

    1.   During the time SEQ 1 is true and SEQ 2 is false, a check for ones is made in the preamble. Any ONE seen will set the error condition.

    2.   When SEQ 3 is true, SEQ 4 is false. If any ONE's are detected, the error condition is set.

    3.   If the character counter reaches a count of 4 (or 26) at any time within data area, it will mean that we are in the post-amble area without having detected the "all one" character.

4. SEQ 4 sets high when we are 28 character times into the postamble. Thus, by the time the next 28 characters are counted, ENVS+ must be dropped; that is, the gap should be found. If this does not happen, the error F/F TERL is set, indicating the detection of a false postamble.

5. If more than one channel has dropped out, we have no means of reconstructing the data. Thus, this condition will also set TERL.

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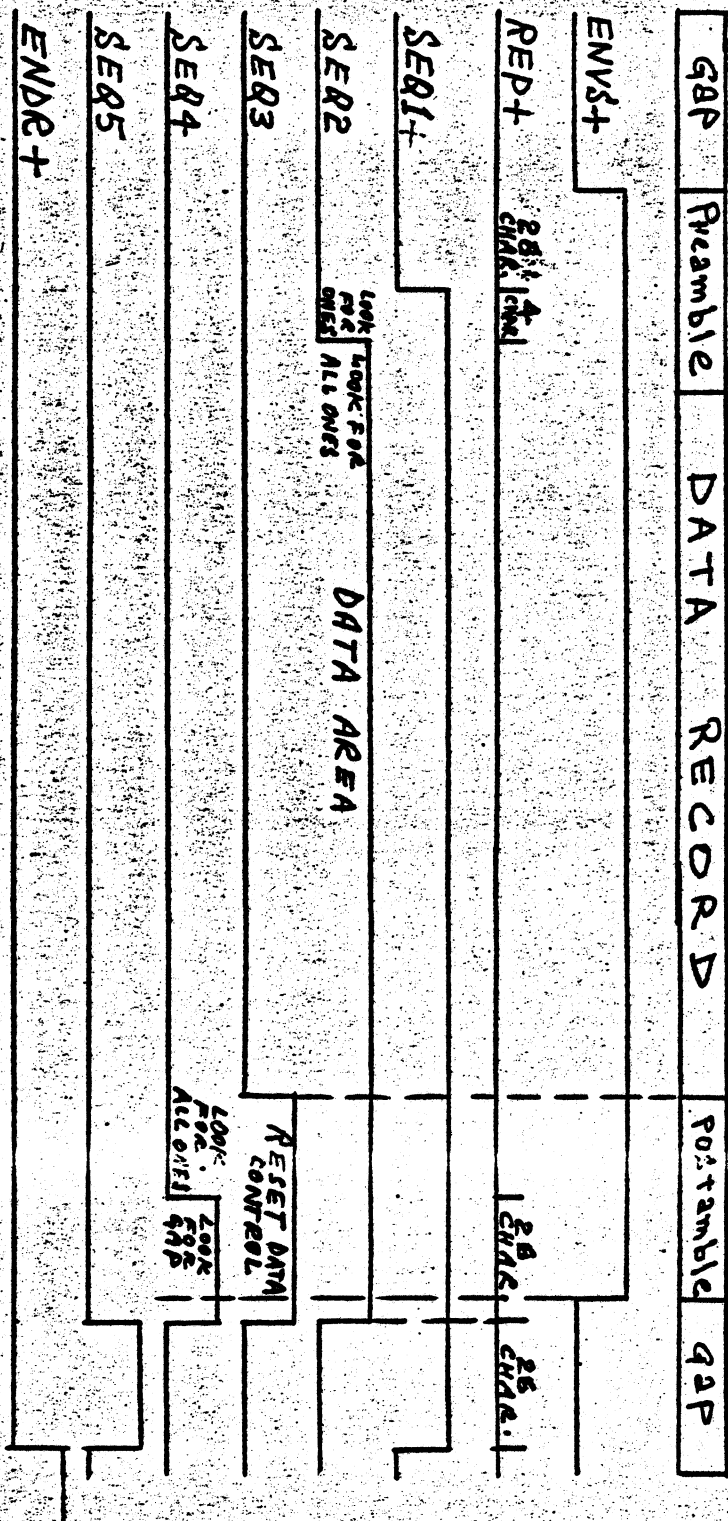
READ SEQUENCER TIMING

FIG. 3.6

| GAP | Preamble | DATA RECORD | Postamble | GAP |

ENVS+
REP+ 25±1 CHAR/CHAR
SEQ1+
SEQ2 LOOK FOR LOOK FOR ALL ONES
SEQ3 DATA AREA
SEQ4
SEQ5
ENDE+

25±1 CHAR 25 CHAR.

LOOK FOR ALL ONES LOOK FOR GAP
RESET DATA CONTROL

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21101

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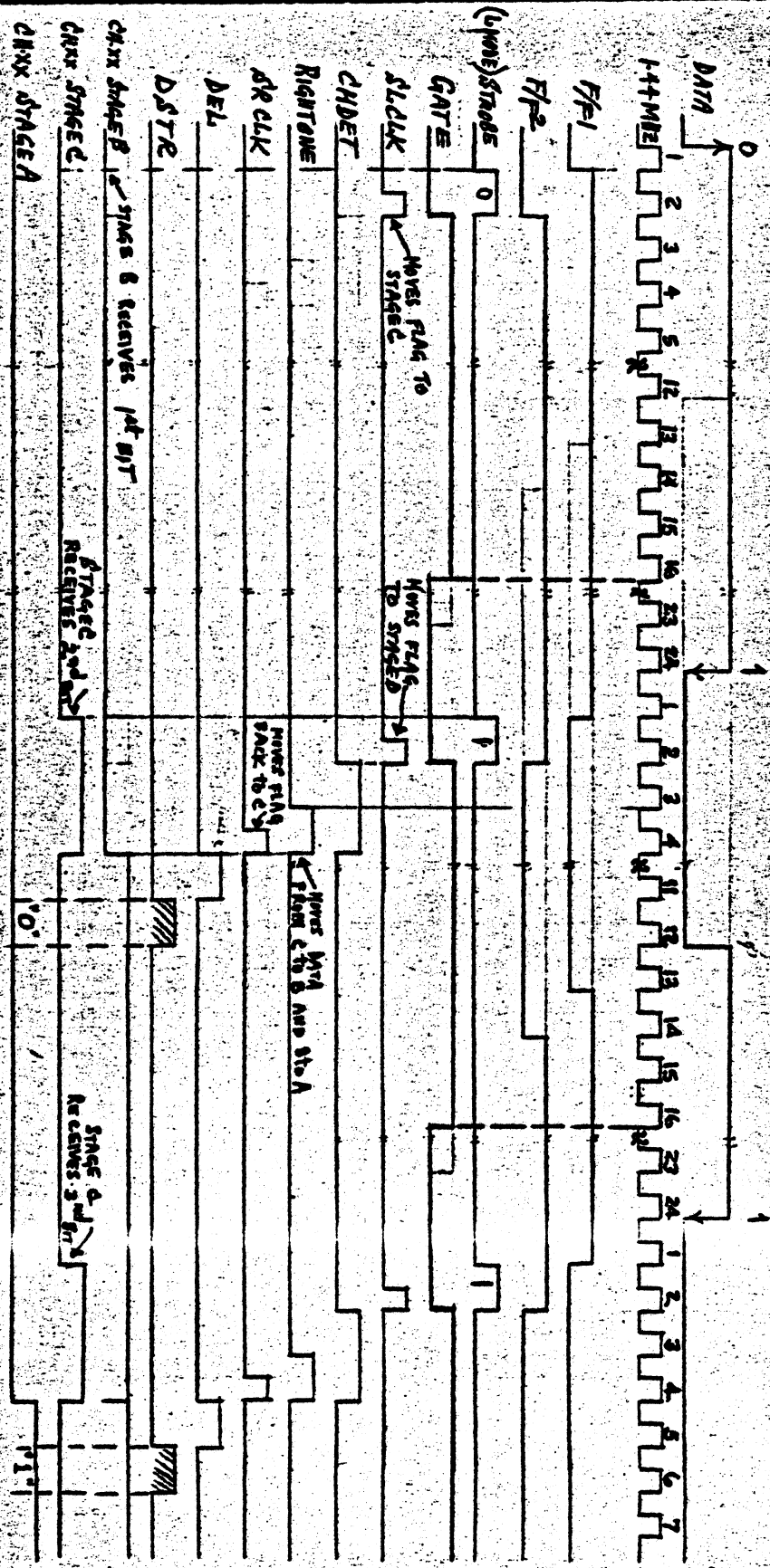SH 26 OF 45
REV X3
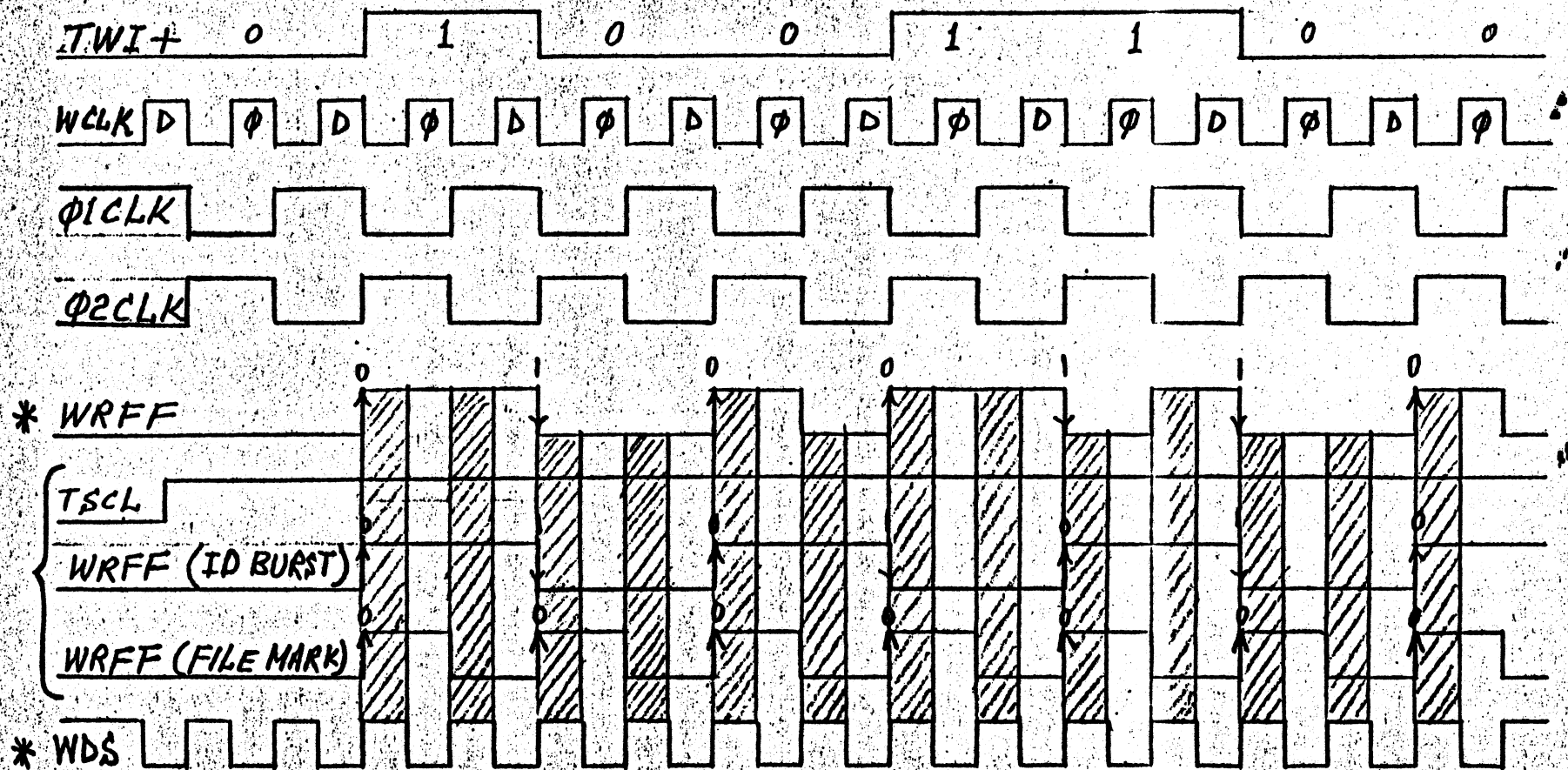
WRITE CODER TIMING

FIG. 3.7

* THESE SIGNALS ARE INVERTED AND SENT TO THE TAPE DRIVE.

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DATA DECODER & DESKEW REGISTER
TIMING
FIG. 3.8

4.1 GENERAL

Characteristics of this magnetic tape system with reference to programming are similar to standard Varian mag tape systems (ref. 98A9902-121) with certain exceptions:

1. The high transfer rate precludes the use of sense response controlled data transfers. All data handling should be done via the BIC and DMA channels.

2. The preamble and postamble automatically generated by the controller make usage of this format for short records (less than 20 words) very inefficient.

4.1.1 Data Format

Figure 4.1 illustrates the data format for converting the 620 data word to mag tape character bytes. Byte A is written and read prior to byte B.

4.2 DESCRIPTIONS OF INSTRUCTIONS

4.2.1 Read One Record (EXC 1010)

This instruction starts the tape, reads characters serially into the MTC registers, and assembles them into two-byte words. It then signals the sensing logic when the buffer is ready to transmit the data to the computer using the BIC.

Reading continues until either the specified number of characters has been read or the end of the record is reached. In either case, the entire record is checked for errors. The record can be a data record or file mark.

4.2.2 Write One Record (EXC 0210)

This instruction starts the tape; signals the computer when the MTC can receive data; transfers the data to the MTC, using the BIC; separates each word into two bytes; generates an odd-parity bit for each byte; and writes the data onto the tape. This continues until no more data are received by the MTC at the normal transfer rate, at which time the postamble is generated and written onto the tape and the tape stopped.

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```
 ┌─────────────────────────┬─────────────────────────┐
 │         BYTE A          │         BYTE B          │
 └─────────────────────────┴─────────────────────────┘
 15              ↑          8 7                      0
           First Out &
           First In
```
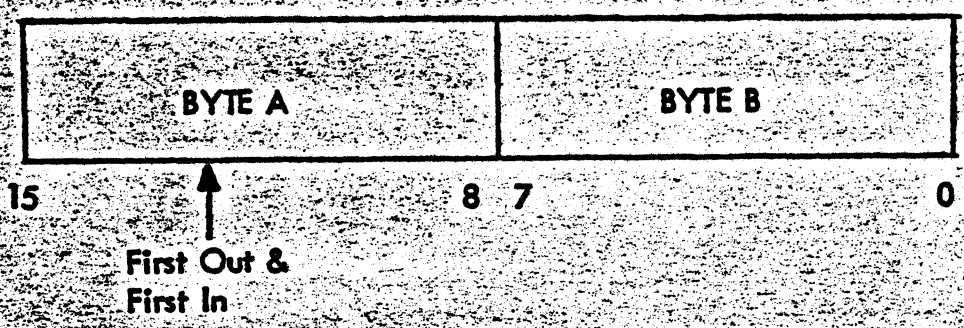
FIGURE 4.1

DATA WORD FORMAT

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4.2.3   Write File Mark (EXC 0410)

This instruction writes a file-mark record, including gaps and check characters. There is no data transfer between the MTC and the computer.

4.2.4   Forward One Record (EXC 0510)

This instruction advances the tape one record. It does not require any computer time or transfer data. However, the record skipped is checked for errors.

4.2.5   Backspace One Record (EXC 0610)

This instruction backspaces the tape one record. It does not require any computer time or transfer data. A check for parity error can be made by a sense tape error instruction, after backspacing.

4.2.6   Rewind (EXC 0710)

This instruction rewinds the tape to the BOT marker.

4.2.7   Sense Tape Error (SEN 010)

This instruction should be issued only when the tape unit is stopped and no motion instruction has been issued, i.e., when the Tape Unit Ready signal is true (section 2.2.9). The Sense Tape Error instruction senses the error signal generated by:

a.   A parity error detected during execution of a Read One Record, Write One Record, Forward One Record, or a Backspace One Record instruction.

b.   A Write One Record or Write File Mark instruction issued when the file-protection ring is not in place on the tape reel.

c.   The tape transport leaving the ready state during the execution of any instruction.

4.2.8   Sense Buffer Ready (SEN 0110)

A true response indicates that the controller is ready to receive or send data (under program control, for low speed mag tapes only).

4.2.9   Sense Tape Unit Ready (SEN 0210)

A true response to this instruction indicates that the tape is stopped and the tape

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transport is ready to receive external control instructions.

4.2.10   Sense File Mark (SEN 0310)

A true response to this instruction indicates that the record checked by the last Read One Record or Forward One Record instruction was a File Mark instruction. The first Motion instruction issued after detection of a file mark resets the FILE MARK indicator.

4.2.11   Sense Odd Length Record (SEN 0410)

A true response to this instruction indicates that a record with an odd number of bytes has been read. The lower byte of the last word read should be ignored.

4.2.12   Sense End of Tape (SEN 0510)

A true response to this instruction indicates that the EOT marker has been detected. The EOT detector is reset by this instruction, or by the Backspace One Record or Rewind instructions.

4.2.13   Sense Beginning of Tape (SEN 0610)

A true response to this instruction indicates that the tape is stopped at the BOT marker.

4.2.14   Sense Rewinding (SEN 0710)

A true response to this instruction indicates that the tape transport is rewinding the tape. Upon completion of the rewinding, the REWIND indicator is reset and the BOT indicator is set (Section 4.2.13).

4.2.15   Select Tape Transport 1 (or 2, e, or 4) (EXC2 Instructions)

4.3   SPECIAL APPLICATION AND DIAGNOSTIC PROGRAMS

Standard Test Program: 92A0107-037
AID II with MTR/BIC Capability: 32A0201-001

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SECTION 5
INSTALLATION & TEST

5.1 INSTALLATION

This option may be installed on any 620 series I/O channel. The two boards (controller & formatter) should be installed adjacent to each other and connected together according to Table 5.1.

Figure 5.1 shows a typical installation.

5.1.1 Device Address

The following pins are used to select the device address on the I/O backpanel.

	Pin	Pin	Example
EB00+	64		Address 10
EB00-	65		would use:
EB0I		66	65 to 66
EB01+	67		68 to 69
EB01-	68		
EB 1I		69	

Note: EB02- is hardwired.

The most significant octal digit of the device address is hardwired, thus the device address is always 1X where X can be from 0 to 3.

5.1.2 Interrupt Driver

Motion interrupt is available on backpanel at pin 75 with return on pin 76 of the controller board.

96A0039-0008

5.2 TESTING

5.2.1 Preliminary Tests

1. Verify that the following timing functions are as shown on controller board:

   a. The basic oscillator frequency MCLK should be 11.52 MHZ ± 1%.

   b. Execute a WOR command and verify that the write clock frequency is twice the normal character rate.

   c. Verify the following O/S durations:
   Adj. Pot K14 for a FM gap = 3.5 in
   Adj. Pot L14 for a IRG gap = .6 in

One Shot	Basic Formula	Actual Timing			
		25 IPS	37.5 IPS	45 IPS	75 IPS
(1) FMOS	$\frac{4 \text{ inches}}{\text{Tape Speed (IPS)}}$	130 msec.	160 msec.	75 msec.	45 msec.
(2) IRGOS	$\frac{0.5 \text{ inches}}{\text{Tape Speed (IPS)}}$	16 msec.	12 msec.	8.5 msec.	5 msec.
(3) IDOS	$\frac{4 \text{ inches}}{\text{Tape Speed (IPS)}}$	155 msec.	106 msec.	108 msec.	65 msec.
(4) STOPED	Tape Stop Time	14.5 msec.	12.4 msec.	9 msec.	5 msec.
(5) TEILOS	$\frac{0.2 \text{ inches}}{\text{Tape Speed (IPS)}}$	2.4 msec.	3 msec.	1.2 msec.	1.8 msec.
(6) STM		11 msec.	7 msec.		3.8 msec.

2. On formatter board, adjust pot so that the VCO center frequency is 24 times the normal data rate. For example, for 75 IPS tape speed, this frequency is:

$$24 \times 120 \text{ KHZ} = 2.88 \text{ MHZ}$$

5.2.2 Acceptance Testing

Perform such acceptance testing as per VDM standard diagnostics with this option (92A0107-037) as is necessary to verify satisfactory operation of the equipment.

5.2.2.1 Deviation From Test Program

Ignore Status Error no. 14 reported just before program halts with U = 666.

TABLE 5.1

BACK-PANEL WIRING

Controller Board		to	Formatter Board	
Signal				
TEIL-	P1-79		P1-79	
TEOF-	-80		-80	
TERL-	-81		-81	
DCLK-	-83		-83	
RB1-	-84		-84	
RB2-	-85		-85	
RB3-	-86		-86	
RB4-	-87		-87	From Formatter
RB5-	-88		-88	
RB6-	-89		-89	
RB7-	-90		-90	
RB8-	-91		-91	
RB9-	-92		-92	
TWRP-	-93		-93	
TWCP-	-94		-94	
TWI-1	-95		-95	To Formatter
TWI-2	-96		-96	
TWI-3	-97		-97	

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Control ler Board		to	Formatter Board	
Signal				
TW1-4	-98		-98	
TW1-5	-99		-99	
TW1-6	-101		-101	
TW1-7	-102		-102	
TW1-8	-103		-103	
TW1-9	-104		-104	To Formatter
BOR+	-105		-105	
A6-3	-106		-106	
TSCL-	-107		-107	
IDTIME-	-108		-108	
	-109		+109	
MCLK	-110		-110	
WOR+	-111		-111	
Ø2CLK+	-112		-112	

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620 I/O
EXPANSION

44A0666
CONTROLLER

44A0667
FORMATTER

53A0712

53A0711
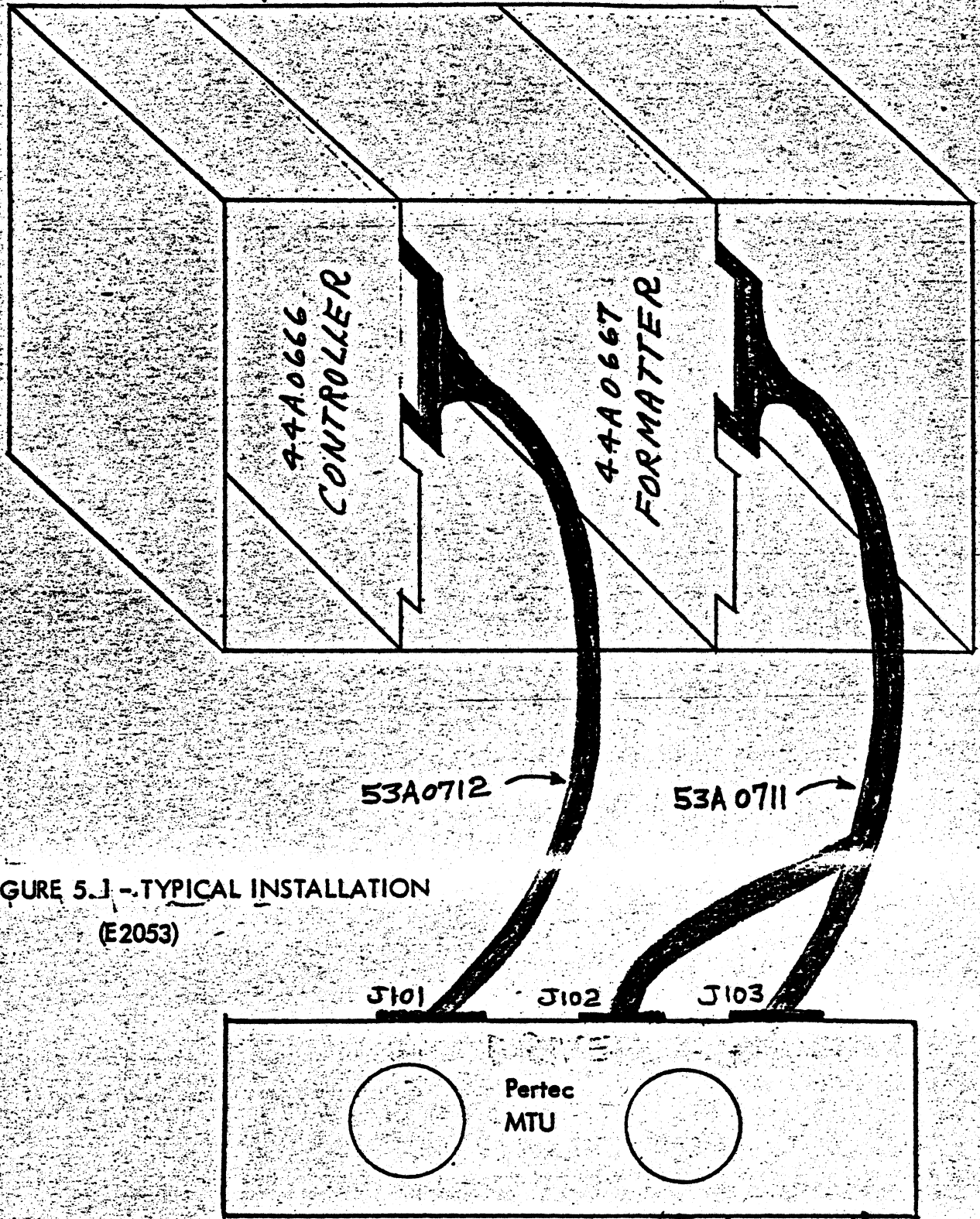
FIGURE 5.1 - TYPICAL INSTALLATION
(E2053)

J101   J102   J103

Pertec
MTU

620 I/O EXPANSION

44A0666 CONTROLLER

44A0667 FORMATTER

53A0712

53A0711

FIGURE 5.1 – TYPICAL INSTALLATION (E3004)

J16-B

J1-A

J6-A

WANGCO MTU
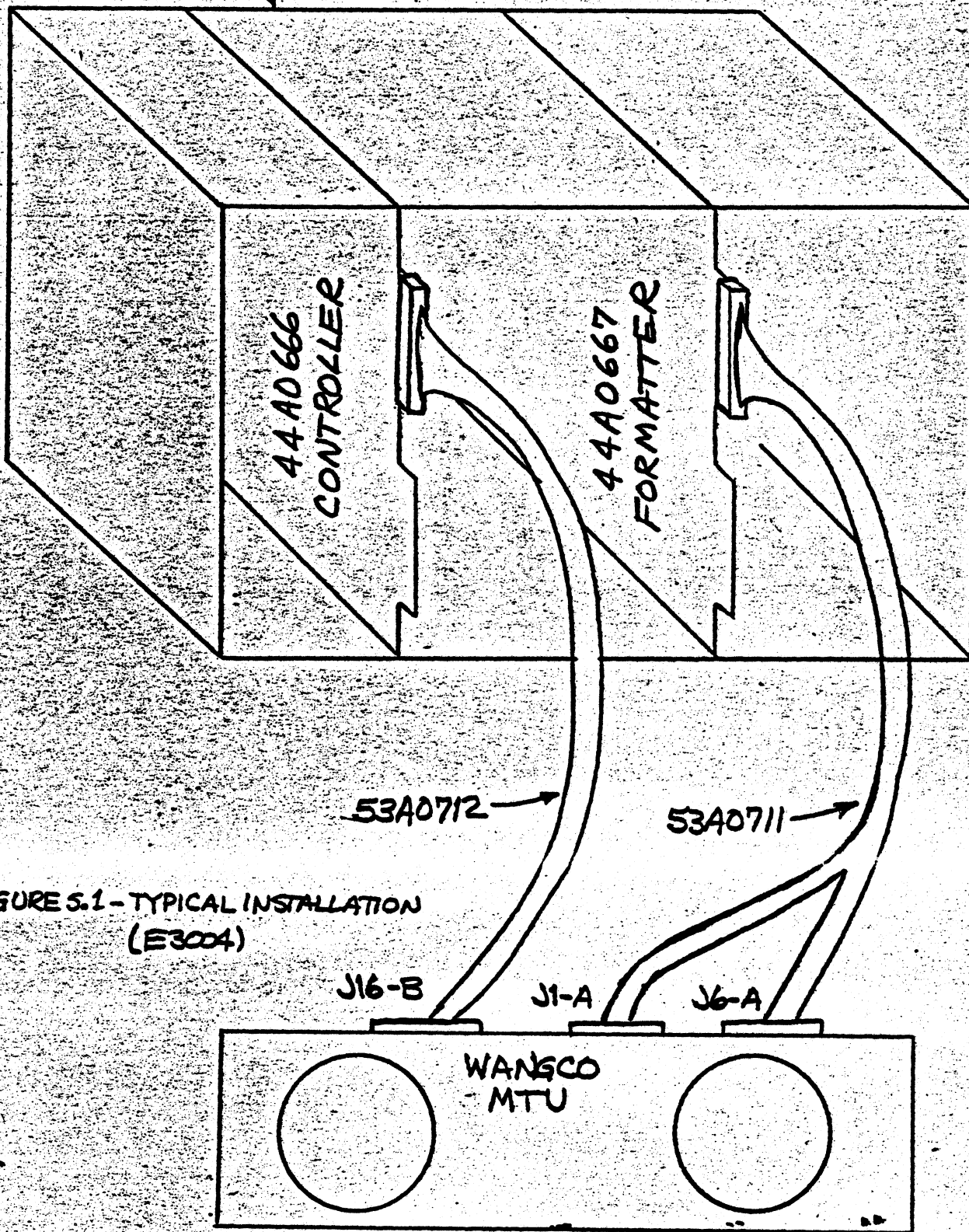
6.1 SIGNAL MNEMONIC DEFINITIONS (CONTROLLER)

ADDX	Decoded Device Address
BCDX	BIC Interface Signal Disconnect Request
BOR	Backspace on record command
BDL	Backward drive F/F (Q side)
BJDTI	Set DTIX F/F signal
BJDTO	Set DTOX F/F
BOTHEM	Signal indicating that both write buffers are empty.
BUFEM 1	Write buffer 1 empty
BUFUL 1	Rd. buffer 1 full
BUSY	Indicates a command is being executed
BYTE 1-4	Strobe signals for write info.
CDCX	BIC interface signal, controller connected
CNT40	Character counter count 40
DCEX	BIC interface signal to connect controller
DCLK	Data clock for read operations
DELCLK	Delayed read strobe
DESX	BIC interface signal to disconnect controller
DRYX	Data strobe from computer
DTEIL	Delayed teil
DTIX	Data input F/F

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DTOX	Data Output F/F
ENALLON	Signal forcing the preamble & postamble all one's character on the data line to the M.T.U.
ENDATA	Signal enabling the write data strobe circuits
ENDRWD	End rewind pulse
EN FM	Signal forcing the file mark pattern on M.T.U. data lines
EN ID	Signal forcing the I.D. pattern on M.T.U. write data lines
FFMOS	Fire file mark one shot
FIDOS	Fire I.D. one shot
FIRG	Fire inter-record gap O/S
FIRST	Signal strobing the first character into the data buffer (read mode)
FMCLK	File mark clock
FMGAPD	File mark gap done
FMOS	File mark one shot
FOURTH	Signal strobing the fourth character into the read data buffer
FRYX	Address strobe from computer
IDCLK	180 KHZ clock used to write the identification burst
IDOS	Identification one shot
INITIAL	Signal used to reset 40 character counter
IRGOS	Inter-record gap one shot
IUAX	Interrupt acknowledge from computer

LOAD	Signal used to load a pre-determined count into the clock divider circuit
MCLK	Master clock
MINT	Motion interrupt
MNCMPL	Motion complete
ODDLEN	Indicates an odd number of characters were read
REL	Ready line from the M.T.U.
RENDATA	Reset en. data F/F
REQOUT	Signal requesting an output data transfer
RERDY	Reset ready F/F
RSTALL	Reset all one's F/F
SECOND	Signal strobing the second read character into the read buffer
SERX	Status sense signal to computer
SETER	Set error F/F
SET REQ	Signal requesting a B.I.C. transfer
SEXC	Synchronized EXC instruction
ST COUNT	Start count to character counter
ST DATA	Signal used to control the TSCL (special character line) to the M.T.U.
STPM	Stop motion
TBDL	Backward drive line to M.T.U.
TEFL	End of tape line from M.T.U.
TEIL	End of information line from M.T.U.
TEILOS	Teil one shot

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TEOF	End of file line from M.T.U.
TER	Tape Error F/F
TERL	Error line from M.T.U.
TFDL	Forward drive line to M.T.U.
THIRD	Signal strobing the third character into the read buffer
TLPL	Load point line from M.T.U.
TREL	Tape ready line from M.T.U.
TRGL	Rewinding status from M.T.U.
TROX	BIC interface signal output request
TRP0-TRP9	Read data lines from M.T.U.
TRQX	Trap request line to BIC
TRWL	Rewind line to M.T.U.
TSCL	Special character line to M.T.U.
TUD1-TUD4	Device select lines to M.T.U.
TWCP	Write clock to M.T.U.
TWI1-TWI9	Write information to M.T.U.
TWLP	Write line selecting write mode in M.T.U.
TWRL	Write ready from M.T.U.
TWRP	Write reset to M.T.U.
TWSL	Write status from M.T.U.
USLC	Extended Exc. command decode
WCLK	360 KHZ write clock
WDCLK	180 KHZ clock

WTA	Write turn around F/F
WONE-WTWO	Signal lines strobing data onto the I/O bus

6.2 SIGNAL MNEMONIC DEFINITIONS (FORMATTER)

CHFND+	Signal indicating the detection of a character by all channels
CHFND 1-CHFND9	Signals indicating the detection of a bit by each channel.
CORECT+	Parity correction bit used to replace data from a dropped channel.
DCLK-	Read clock to controller
DEC-	VCO control signal used to decrease the frequency.
DOUT 1-DOUT9	Stage before last on the data buffer in each channel.
DRPED2	Signal indicating that two or more tracks have dropped out
DRPED 1	Indicates that at least one track has dropped out
EHSCK	Early high speed clock
ENDR	Signal indicating the end of a Read operation
ENFM	Set signal for the file mark flip flop
ENVS	Signal signifying the detection of envelopes on channels 1 or 3
ENV 1-ENV9	Signals from individual channels indicating the presence of data
EOUT 1-EOUT9	Data bit out of each channel's read buffer last stage
FLSPOST	False postamble

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FE	Format error F/F
FM	File mark F/F
GATE1–GATE9	Signal used as a window for data detection
HSCLK1–HSCLK5	Master clock used for timing in all channels.
IDTIME	Indicates the presence of BOT tab
INC	VCO control signal used to increase frequency
MISPREA	Missed preamble
NDATA	Signal made up of $\overline{ENV1}$ or $\overline{ENV2}$
ONES–	An "OR" tie of all nine channels "ONE" detectors which is active for any "ONE" on any channel
$\emptyset1$ CLK – $\emptyset2$ CLK	Outputs of a flip flop that divides the write clocks (TWCP)
POSTA+	Signal which is true when all channels detect a postamble
POSTONE	"ONES" in postamble
PREONE	"ONES" in preamble
RB1–RB9	Read lists going to the controller
RD1–RD9	Read data coming from the tape drive
REP+	Signal generated everytime one of the decodes on the character counter is satisfied
RESYN1–RESYN9	Signals resetting the SYNC flip flop for each channel
RET01–RET04	Twisted pair returned from the J1 connector signals
REV–	Signal indicating reverse tape motion 4 used to invert input data from tape to each channel

RGATE 1-RGATE2	Signals used to enable read logic in all channels
SEQ 1-SEQ5	Sequences outputs
SLCLK 1-SLCLK9	Shift left clocks
SRCLK 1-SRCLK9	Shift right clocks
SRONE	Shift right one place. Signal sent to all channels deskew logic
SSTG4	Set stage 4 of deskew pointer for each channel
STROBE 1-STROBE9	Signal made up of "ONES" or "ZEROS" on each channel
SYNC 1-SYNC9	Sync flip flop outputs for the 9 channels
S2 NS3	Sequencer stage 2 anded with sequencer stage 3 not.
S2 NS4	Sequencer stage 2 anded with sequencer stage 4 not.
TEOF	End of file signal to controller
TERL	Error signal to controller
TSCL	Special character signal from controller
TWCP	Write clock from controller
TWI 1-TWI9	Write data from controller
TWRP	Reset pulse from controller
WDS	Write data strobe to tape drive
WD 1-WD9	Write data to tape drive
WRFF 1-WRFF9	Write coder flip flops for the 9 channels
WRT 1-WRT9	Combined signal at the input of the write coder

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