WANG

6106

VS-85/85-H Computer System

COMPANY PROPRIETARY STATEMENT

Customer Engineering
First Customer Shipment Manual

741-1492

PREFACE

This document is the First Customer Shipment (FCS) Manual for the VS-85/85-H Computer System. It is organized in accordance with the approved FCS outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. Normally, an FCS manual will not include the Introduction, Theory of Operation, Preventive Maintenance, or Schematics chapters; however, if available at FCS time, they may be included. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof).

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the VS-85/85-H Computer System at FCS time. **Information pertaining exclusively to the VS-85-H has been printed in boldface type and underlined so that the CE can readily recognize such information.** It is not planned to update or reprint this FCS Manual.

First Edition (December 1984)

This edition of the VS-85/85-H Computer System FCS manual may only be used for the purpose stated in the Preface.

CUSTOMER ENGINEERING

PUBLICATION UPDATE BULLETIN

DATE: 05/14/85

This PUB: 741-1492-1

Class Code: 6106

Base Document: 741-1492

Previous Notice(s):

REASON FOR CHANGE:

To add 22V36 Async Device Controller description to manual.
NOTE: As of this date, the VS-85 Computer System Manual (WLI P/N 741-1224) is obsolete. Replace it with the VS-85/85-H Manual (WLI P/N 741-1492).

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	xi	xi
2.		C-1 thru C-19
3.		
4.		
5.		
6.		
7.		
8.		
9.		
10.		

This page is to be used as a permanent record of revisions; place it directly following the title page.

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CUSTOMER ENGINEERING

PUBLICATION UPDATE BULLETIN

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Previous Notice(s):

REASON FOR CHANGE:

This PUB provides corrections to the VS-85/85-H manual and information for the installation of the new I/O panel connector plates.

INSTRUCTIONS:

Remove pages and insert attached pages as follows:

	REMOVE	INSERT
1.	xiii	xiii
2.	1-1/1-2	1-1/1-2
3.	1-19/1-20	1-19/1-20
4.	4-23/4-24	4-23/4-24
5.	4-29/4-30	4-29/4-30
6.	4-33 thru 4-42	4-33 thru 4-42A
7.	5-41 thru 5-44	5-41 thru 5-44
8.	7-5/7-6	7-5/7-6
9.	7-9 thru 7-11	7-9 thru 7-11
10.	8-9/8-10	8-9/8-10

This page constitutes a permanent record of revisions; place it directly following title page.

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WARNING

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**************************************************************
*                                                            *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY        *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND          *
*    CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-       *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.   *
*                                                            *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER            *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                   *
*                                                            *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC   *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,       *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO    *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO       *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                    *
*                                                            *
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****
*   *
* THIS COMPUTER EQUIPMENT HAS BEEN VERIFIED AS FCC CLASS A.   *
*   *
****

IN ORDER TO MAINTAIN COMPLIANCE WITH FCC CLASS A VERIFICATION, THE FOLLOWING CONDITIONS MUST BE ADHERED TO DURING NORMAL OPERATION OF EQUIPMENT.

- ALL COVERS MUST BE ON SYSTEM AND SECURED IN THE PROPER MANNER.
- ALL INTERNAL CABLES MUST BE ROUTED IN THE ORIGINAL MANNER WITHIN THE CABLE CLAMPS PROVIDED FOR THAT PURPOSE.
- THE MAINTENANCE PANEL DOOR MUST BE KEPT CLOSED.
- ALL EXTERNAL CABLING MUST BE SECURED AND THE PROPER CABLE USED TO ENSURE THAT CABLE SHIELDING IS PROPERLY GROUNDED TO THE CABLE CLAMPS PROVIDED.
- MAKE SURE CONTACT FINGER STRIP CLIP-ON (WLI P/N 654-2139) IS IN PLACE AND UNDAMAGED. (CONTACT FINGER STRIP MAY BE ORDERED AND CUT TO PROPER LENGTH).
- ALL HARDWARE MUST BE PROPERLY SECURED.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

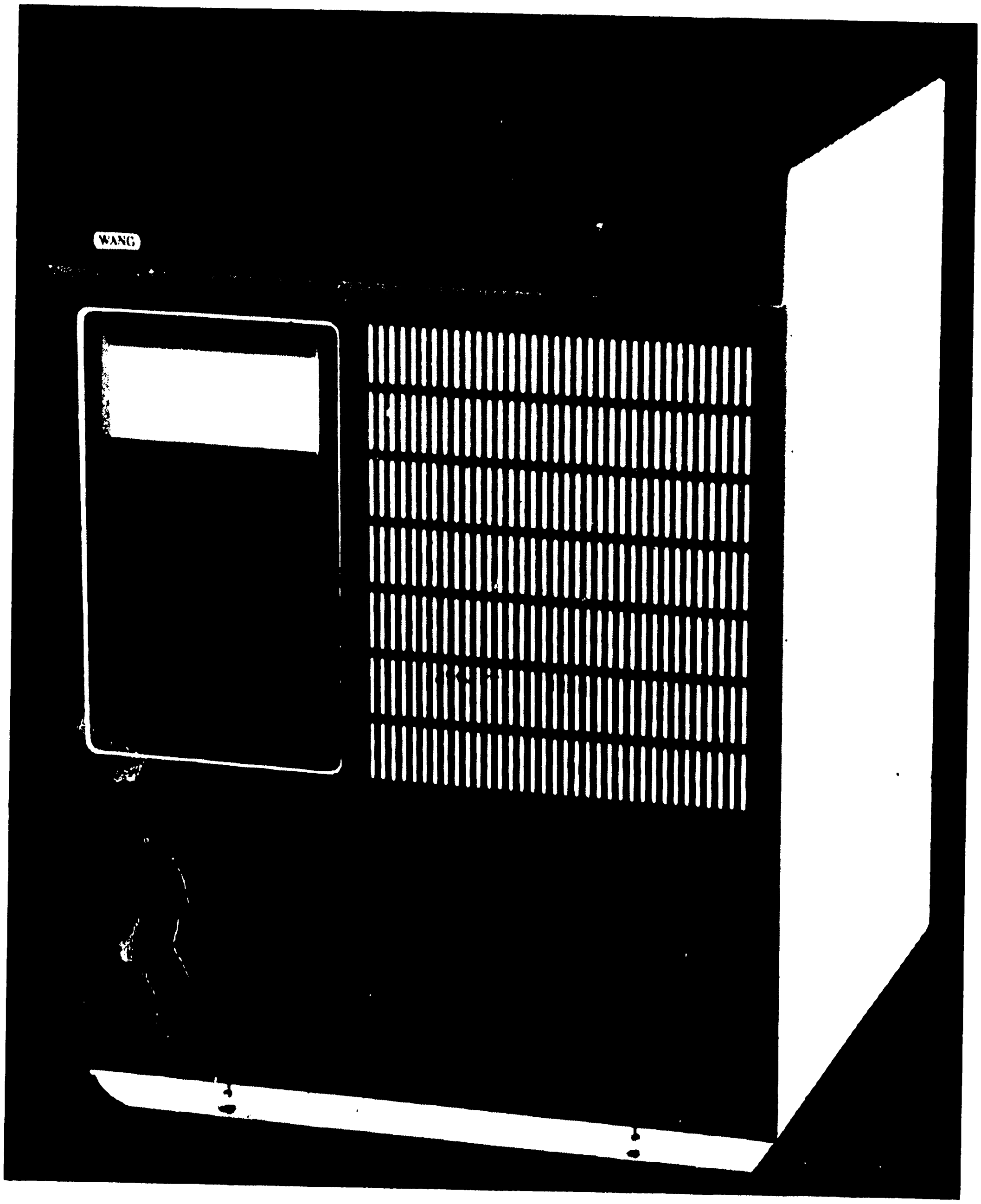
LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

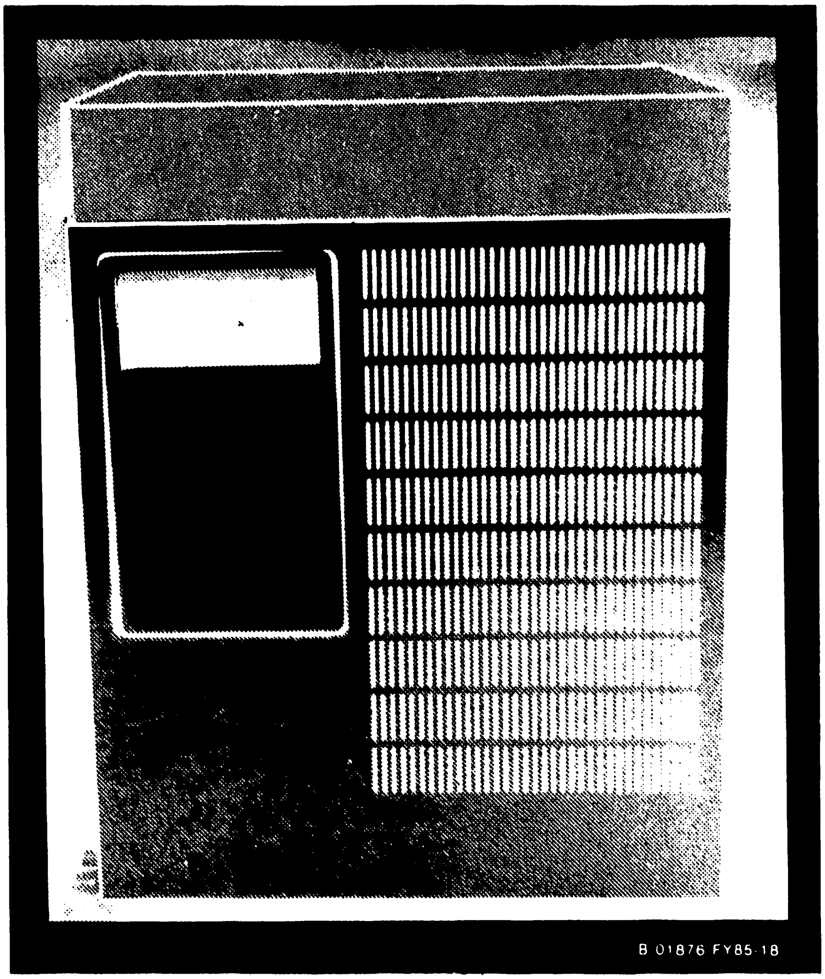
LIST OF ILLUSTRATIONS (Cont'd)

LIST OF TABLES

LIST OF TABLES (Cont'd)



VS-85



VS-85-H

CHAPTER 1

INTRO-DUCTION

CHAPTER 1

INTRODUCTION

1.1 PURPOSE

This manual contains information necessary to install and maintain the VS-85/85-H CPU. As new information becomes available it will be provided as Publication Update Bulletins (PUBs) or subsequent editions.

1.2 SCOPE

This manual is divided into eight chapters, as follows:

Chapter 1: "Introduction" provides information on available VS documentation; gives a brief description of the VS-85/85-H system and system software, system configurations, and associated peripherals; and provides system specification information.

Chapter 2: "Theory of Operation" provides block diagram level theory discussion for the VS-85/85-H CPU and mainframe components.

Chapter 3: "Operation" identifies all VS-85/85-H mainframe switches and indicators, including a functional description of each, together with settings and operating procedures.

Chapter 4: "Installation" gives guidelines necessary to make sure that the installation site conforms to specific requirements of the VS-85/85-H system; provides procedures for unpacking and inspecting the VS-85/85-H mainframe; and provides instructions for initial set-up and operation of the VS-85/85-H, together with associated program-loading and operation-confirmation procedures.

Chapter 5: "Preventive and Corrective Maintenance" gives guidelines and schedules for necessary preventive maintenance routines. Included in this chapter is a list of tools and test equipment required for proper repair and maintenance of the VS-85/85-H system. Also included are removal and replacement procedures pertaining to disassembly and replacement of system components that are field-replaceable.

Chapter 6: Schematics are not provided as part of this Standard Manual. The schematics will be published in the VS-85/85-H/90/100 Computer System Schematics Manual, WLI P/N 729-1462.

Chapter 7: "Illustrated Parts Breakdown" contains the illustrated parts breakdown used for identification when ordering field-replaceable components.

Chapter 8: "Troubleshooting" identifies the available microcode diagnostics, and off-line and on-line diagnostic test programs and gives guidelines for their use. Also provides troubleshooting flow charts for isolating fault locations to field-replaceable or repairable components.

Appendix: The appendix provides the CE with a ready reference of necessary information. The appendix includes a mnemonics listing, signal name definitions, and VS-85/85-H microinstructions.

1.3 RELATED PUBLICATIONS

The following is a list of Customer Engineering and Corporate publications that contain information pertaining to the VS-85/85-H system and related equipment.

Table 1-1. Customer Engineering Publications

SUBJECT	CLASS	PART NUMBER
90 KB Diskette Drive (Shugart SA-400)	3101	729-0123
75-, 288-MB CDC SMD Disk Drive	3106	729-0211-A
90-MB CDC Phoenix Disk Drive	3105	729-0198-B
76-MB NEC WINC Disk Drive (VS-85-H)	3112	729-1452
147-MB NEC WINC Disk Drive (VS-85-H)	3112	729-1503
620-MB CDC FMD Disk Drive	3106	729-1253/54
2209V Tape Drive	3202	729-0249A/50A
2219V Tape Drive	3204	729-1136/37
6554 TC Processor	7303	729-1043
Systems Installation Guide - VS, 2200, WP/OIS	1106	729-0907
Technical Documentation Catalog/Index	1100	741-0000
VS Diagnostics Handbooks	6302	729-XXXX
VS Printers	33XX	729-XXXX
VS Reference Summary Guide	6101	729-0716
VS Workstations	3404	729-XXXX

Table 1-2. Corporate VS Documents

DOCUMENT TITLE	PART NUMBER
Customer Site Planning Guide	700-5978E
VS 3271 Emulation User's Guide (2nd Edition)	800-1306-02
VS ATMSWPS Conversion Guide	800-1499-02
VS Assembler Language Pocket Guide	800-6203-02
VS Assembler Language Reference	800-1200-03
VS BASIC Language Reference	800-1202-04
VS BASIC Quick Reference	800-6205-02
VS Batch Communications User Guide	800-1305-02
VS Batch Communications User Guide Addendum	800-1305-02.01
VS COBOL Quick Reference	800-6200-05
VS COBOL Reference	800-1201-06
VS Card Reader Utility Reference	800-1323-01
VS EZQUERY Reference	800-1129-03
VS Emulation of SNA 3274 and 3777, General Description	800-1326-02
VS FORTRAN Reference	800-1208-02
VS File Management Utilities Reference	800-1308-01
VS General Purpose Asynch. Comm. Programmers Guide	800-1325-01

Table 1-2. Corporate VS Documents (cont'd)

DOCUMENT TITLE	PART NUMBER
VS/IIS Advanced Functions Quick Reference Guide	800-1122-01
VS/IIS List Management Operators Guide	800-1120-01
VS/IIS Supervisors Procedures	800-1110-03
VS KEYENTRY Operator's Guide	800-1113-02
VS KEYENTRY Supervisor's Guide	800-1114-01
VS 2265V-3 Disk Drive Operating Procedures Sum. Card	800-6209
VS 2529V Cartridge Tape Drive Sum. Card 800-6212	800-6212
VS Operating System Services	800-1107-06
VS Operating System Services Pocket Guide	800-6204-03
VS PL/I Language Reference Manual	800-1209-02
VS Principles of Operation, Addendum	800-1100-04
VS Procedure Language Quick Reference	800-6201-03
VS Procedure Language Reference	800-1205-05
VS Program Development Tools Reference	800-1307-03
VS Programmer's Guide to VS/IIS	800-1304-04
VS Programmer's Introduction	800-1101-06
VS RPG II Language Reference Addendum	800-1203-05.01
VS RPG II Language Reference Addendum	800-1203-05.02
VS RPG II Language Reference Addendum	800-1203-05.03
VS Software Bulletin - Release 5.3	800-3109
VS Software Bulletin - Release 5.3 Addendum	800-3109.01
VS Software Bulletin - Release 5.3 Addendum	800-3109.02
VS Software Bulletin - Release 6.0	800-3111-01
VS Software Bulletin - Release 6.20	800-3114-01
VS SNA 3777-3 Emulator User's Guide	800-1330-02
VS System Activity Monitor (SAM) Reference Manual	800-1324-01
VS System Operators Reference	800-1102-08
VS System Utilities Reference	800-1303-04
VS TOTAL Pocket Guide	800-6207-02
VS Teletypewriter Emulation (TTY) User's Guide	800-1314-03
VS USERSUBS Reference	800-1315-01
VS User Aid COMPILE	800-3312
VS User Aid COMPUTE	800-3301-02
VS User Aid LIBRXREF	800-3309-01
VS User Aid MAIL	800-3302-01
VS User Aid PRINTIBM	800-3308-01
VS User Aid PRINTVS	800-3303-01
VS User Aid SORTLINK	800-3310-01
VS User Aid TAPEDUMP	800-3311
VS/WP Introducing Word Processing on VS	800-1407-02

Table 1-3. Corporate VS Data Sheets

Document Title	Part Number
VS 85, VS90, VS 100 Systems Data Sheet	800-2118-08
VS Data Communications	800-2107-03
VS Disk Drives	800-2504-03
VS DMS and DMS/TX	800-2125-01
VS EZQUERY	800-2113-02
VS Graphics Facility	800-1446-02
VS HASP Emulation	800-2308

Table 1-3. Corporate VS Data Sheets (cont'd)

Document Title	Part Number
VS Ideographic Data Processing System (Chinese)	800-2502-01
VS Ideographic Data Processing System (Japanese)	800-2501-02
VS/IIS List Management	800-2407-01
VSKEYENTRY	800-2300-01
VS Languages	800-2201-07
VS MATHPLANNER	800-1484-03
VS PL/I	800-2208-01
VS Printers	800-2507-02
VS Processors	800-2105-03
VS Report	800-2305
VS RPG II	800-2204-01
VS RPG II Conversion Aid	800-2207-01
VS SNA Emulation	800-2307B
VS System Activity Monitor (SAM)	800-2116
VS System Software	800-2101-04
VS Tape Drive	800-2505-02
VS Teletypewriter Emulation (TTY)	800-2109-02
VS Transdata 810	800-2119-02
VS Workstations	800-2503-01
VS/WP Integrated Information System	800-2103-05

1.4 SYSTEM DESCRIPTION

The Wang VS-85/85-H computer system is a high-performance data processor with the programming flexibility of Virtual Storage. The VS-85/85-H supports interactive, multiuser operations in a general purpose computer environment and offers programming capability in BASIC, COBOL, FORTRAN, PL/1, and RPG II languages. The VS-85/85-H also supports Assembler and Procedure languages, allowing operational sequences to be performed without user interaction.

The VS-85/85-H uses the same CP4 processor as the VS-100, but the basic VS-85/85-H does not have the VS-100's Cache memory. Cache Memory is an option and, when installed, must be accompanied by a System Bus Controller (SBC). Cache allows the VS-85/85-H 64-bit main memory accesses. When the Cache/SBC is not installed, it is substituted for with a Memory Controller I (MCI) and a Memory Controller II (MCII) combination. The MCI and MCII combination allows only 32-bit main memory access. The MCI provides all of the normal memory control functions of the Cache, but does not have the 32 Kbytes (KB) of RAM memory. The MCII is similar to the SBC, except that one half of the 64-bit path to Cache has been removed. The Bus Adapter (BA) functions remain the same, except that the BA is signaled as to when a Cache/SBC is or is not installed. This permits the BA to process either 32-bit or 64-bit data words.

The VS-85/85-H minimum Main Memory (MM), without the Cache Memory/SBC option, is 1 MB and the maximum MM is 4 MB . However, a VS-85/85-H with the Cache Memory/SBC option must contain at least 2 MB of MM.

The VS-85/85-H can control up to 2.5 gigabytes (GB) of on-line disk storage (5.1 GB with the optional Cache Memory); a maximum of 48 serial devices, 32 of which may be workstations, (up to 64 workstations with the optional Cache); up to four tape drives; and telecommunications interface capabilities ranging from a single remote terminal to full protocol compatibility with a larger host computer. The VS-85/85-H supports all serial VS peripheral devices. Parallel printers and workstations, except remote TC devices, are NOT supported on the VS-85/85-H.

In addition, the VS-85-H contains either a 76-MB formatted (85-MB unformatted) or 147-MB formatted (167.7-MB unformatted) internal NEC disk drive and can support up to three external drives. Both the 76-MB and the 147-MB models utilize 8-inch fixed disks and Winchester-type technology. Other differences in the VS-85-H include six new CP boards using multilayer technology, new microcode revision 4.58.04, a half-height minifloppy diskette drive, cabinet changes to accommodate the internal drives and accompanying power supply, and design enhancements to the Control Memory (CM) and B-Bus boards.

NOTES

1. Current CP multiwire boards and the new multilayer boards cannot be intermixed within a CP. New part numbers have been assigned to all new units in order to distinguish them from the old units.

2. Existing VS-85 CPs in the field are not upgradeable to the 'H' models (VS-85-76F/147F) nor are the 'H' models upgradeable to the VS-100 since the internal disk drives are not available on the VS-100.

1.4.1 CENTRAL PROCESSOR

Housed in a compact cabinet with the Main Memory (MM) and optional Input/Output Processors (IOPs), the CP4 central processor (CP) is the heart of the VS-85/85-H. (See figure 1-1.) It consists of an A Bus board and a B Bus board. The CP4 processor is a faster, more sophisticated version of the CP3 processor used in the VS-60/80. It supports the same instruction set as the CP3, with the exception of certain privileged instructions related to address translation.

The VS-85/85-H CP supports binary, packed-decimal, and floating-point arithmetic. Included in the CP are sixteen 32-bit general purpose registers and four 64-bit floating-point registers. As in the VS-60/80, the machine instruction set is compatible with the IBM 370 instruction set.

The following features of the CP4 are not found in the CP3. They provide the CP4 processor with much of its expanded processing power.

1. 32-Bit CP Architecture - ALU operations in the CP use 32-bit register operands. The CP also has a 32- or 64-bit data bus to Main Memory.

2. Fast Cycle Time - Processing time in the CP4 is approximately 160 nanoseconds/microinstruction.

3. Overlapped Macroinstruction Decoding - The use of a dedicated, buffered Memory Address Register (MAR0) allows the simultaneous processing of several different macroinstructions.

4. Buffered Operand Access - Allows the 32-bit ALU path to be used in important storage-to-storage macroinstructions (for example, MOVE, COMPARE).

5. Hardware Multiplication and Division Support - Hardware within the CP supports the multiplication of two 16-bit operands to form a 32-bit result within two instruction cycles (320 nsecs). This feature allows floating-point fractional and fixed-point multiplication, and the processing of array-orientated macroinstructions. An efficient non-restoring binary division operation is provided by two microinstructions, ASH and ASL.

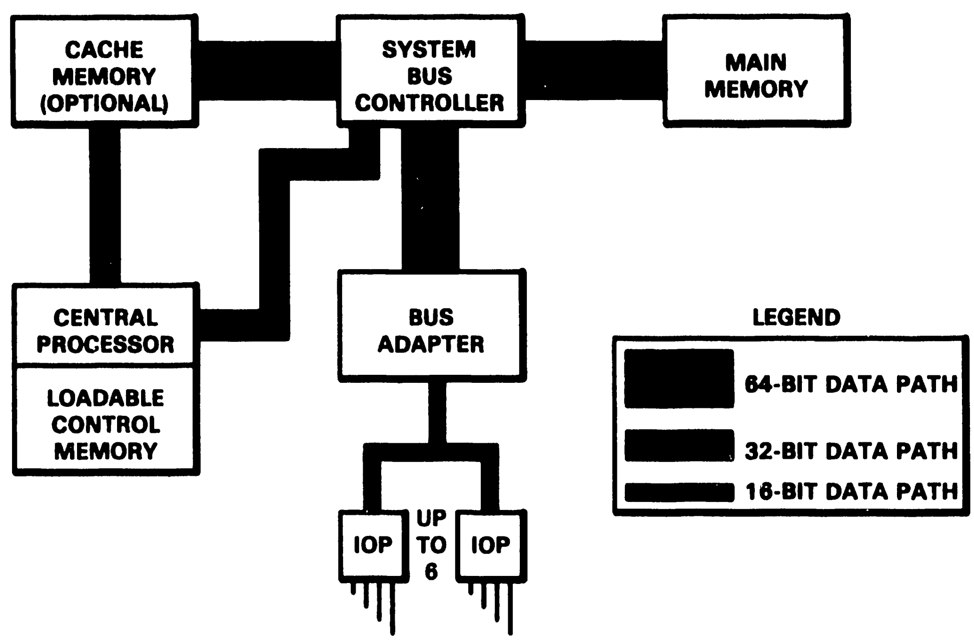


Figure 1-1. VS-85/85-H Central Processing Unit Architecture

1.4.2 CONTROL MEMORY

Control Memory (CM) in the VS-85/85-H is based on 4Kx1-bit loadable RAM chips located on a Control Memory board. To load operational or diagnostic microcode into CM, a mini-diskette drive is provided on the front of the

VS-85/85-H chassis. A loadable CM allows for functional CP expansion, CP microcode updates using a diskette instead of replacing expensive PROMs, and the use of loadable CP microdiagnostics.

CM in the VS-85 is 8 KB <u>(in the VS-85-H, 12 KB)</u> in size. A 1K PROM located on the mini-diskette controller board contains the bootstrap program necessary to load the operational or diagnostic microcode into CM.

1.4.3 MEMORY CONTROLLER I (MCI)

Unlike the VS-100, the standard VS-85/85-H system has a lower cost 32-bit memory data bus. This 32-bit bus is controlled by the Memory Controller I (MCI) board. The MCI contains the same basic memory control and data passing services as the Cache Memory board (described below), but does not contain the 32 KB of Cache RAM.

1.4.4 CACHE MEMORY

An optional feature recently added to the VS-85/85-H is a VS-100 type Cache Memory, a 32-KB block of high-speed (80 nsec) local memory. The Cache option not only decreases the CP's data retrieval time, it also provides a 64-bit Main Memory (MM) data bus.

The cache function is transparent to the user, "cached" or concealed within the depths of the CP. Only the apparent increase in Main Memory access speed is visible to the user. With this feature, the CP is able to access needed data without initiating a full Main Memory read cycle. If the necessary information is found in cache, a considerable savings in processing time is achieved (on the order of 480 nsecs).

Cache Memory is a buffer between the CP and Main Memory. Its main function is to improve memory transfer rate by providing high speed access to needed data. It accomplishes this by storing a copy of the most recently used subset of MM. When the CP does a memory read, it first references the cache. If the needed data is found here, a cache "hit" occurs and no MM cycle is initiated. If the required data is not found in cache, a cache "miss" occurs and a MM cycle is initiated. The data read from memory is then gated to both the CP and the cache, keeping the cache contents current with MM.

Cache Memory operates on the "locality of reference" concept, which is based on two assumptions: once a location in memory is referenced, it is often referenced again within a short period of time; and once a location is referenced, a nearby location will also be referenced. These assumptions hold true for the most part because, in programming, commonly used variables are usually located near each other and much use is made of program loops and common subroutines. The use of sequential instruction indexing and linear data arrays also play a part in the successful incorporation of a Cache Memory. For a detailed look at the cache and its operation, refer to Chapter 2, Theory of Operation.

1.4.5 MEMORY CONTROLLER II

The Memory Controller II (MCII) is used in conjunction with the MCI board. The Memory Controller II contains basically the same logic functions as the System Bus Controller (SBC), described below, but does not support the 64-bit memory data bus.

1.4.6 SYSTEM BUS CONTROLLER

The SBC must be installed in place of the Memory Controller II when the optional Cache Memory board is installed. The SBC acts as the "traffic cop" of the VS-85/85-H CP and controls the routing of data between the CP, the Bus Adapters (BA), and MM. The SBC is also responsible for generating parity on MM writes and correcting single bit errors on MM reads. Other features of the SBC include Error Logging, Read Modify Writes and single byte CP reads, and the use of an External Condition Register to select and record events occurring outside the CP.

1.4.7 MAIN MEMORY

The VS-85/85-H can contain one to two 210-7803 or 210-8203 Main Memory boards. Memory can range in size from 1 MB to a maximum of 4 MB with memory size increasing in 1 or 2 MB increments. Each Main Memory board contains a maximum of 1 MB of data for the 7803 board and 2 MB for the 8203 board.

A VS-85/85-H with no Cache option (MCI installed) can support 1, 2 and 4 MB of MM. A VS-85/85-H with the Cache option only supports 2 and 4 MB of MM.

1.4.8 BUS ADAPTER

The Bus Adapter (BA) is the interface between the VS-85/85-H CP and up to six IOPs and attached peripheral devices. The BA also provides data buffering and routing between the 16-bit IOP data path and the 64-bit Main Memory (MM) data bus (with the optional Cache Memory board installed), or the 32-bit MM data bus (without the optional Cache Memory board). Because the IOPs use a 16-bit path and MM uses a 64 or 32-bit bus, the BA must put data going from the IOP to MM into 64 or 32-bit blocks for transfer to MM. It must also perform the reverse function on data going from MM to an IOP. Only one BA can be installed in the VS-85/85-H, allowing the CP to interface with a maximum of six IOPs.

1.5 CP MOTHERBOARD

The Central Processor Motherboard (210-8508) contains all CP logic circuit boards, the Main Memory (MM) boards, associated bus control logic boards, and I/O Processors.

All circuit boards installed on the VS-85/85-H CP Motherboard, along with a brief description of each board, follows:

1. 210-7600 <u>(210-8568 in VS-85-H)</u> A Bus (CP #1) - Contains all A bus registers, status registers, branch decision logic, multiplier, and the real-time clock.

2. 210-7601 <u>(210-8569-A in VS-85-H)</u> B Bus (CP #2) - Contains all B bus registers, Translation RAM (T-RAM), binary ALU, and the decimal ALU.

3. 210-7602 <u>(210-8204-A in VS-85-H)</u> Control Memory (CM) - Contains microinstruction storage, instruction counter, trap handling logic, and system clock.

4. 210-7803 1-MB Main Memory (MM) Board - Used for storage of software instructions and data.

5. 210-8203 2-MB MM Board - Used for storage of software instructions and data.

6. 210-8230 Memory Controller I (MCI) - Contains memory sequencing controls and buffers for all read data. Only supports a 32-bit memory access.

7. 210-8804 <u>(210-8570-A in VS-85-H)</u> Cache Memory - Optionally replaces the MCI. Contains 32 KB of Cache Memory, memory sequencing controls, and buffers for all read data. Supports a 64-bit memory access. Used for support of a 2nd disk IOP or a tape IOP for the 2219V tape drive.

8. 210-8231 Memory Controller II (MCII) - Controls all Read/Write data to/from MM, Error Correction Code (ECC) generation, correction logic, and error checking. The MCII also contains the External Condition Register (ECR). Only supports a 32-bit memory access.

9. 210-7605 <u>(210-8571-A in VS-85-H)</u> System Bus Controller (SBC) - Must be used with Cache option and replaces MCII. Controls all Read/Write data to/from MM, ECC generation, correction logic, and error checking. The SBC also contains the Bus Transaction Log (BTL) and the External Condition Register (ECR). Supports a 64-bit memory access.

10. 210-8311 <u>(210-8572 in VS-85-H)</u> Bus Adapter (BA) - Contains the logic necessary to interface up to six IOPs with the SBC/MCII.

1.6 INPUT/OUTPUT PROCESSORS

In the VS-85/85-H as in the 60/80/100, the IOPs relieve the CP of the time consuming task of communicating directly with attached peripherals. With this feature, I/O processing and data processing can run concurrently on the VS-85/85-H with the resultant increase in processor job-handling speed. Following is a list of the available IOPs with a description of the individual peripherals each IOP can support.

1. 22V27-1/2 Serial IOPs (WLI P/N 212-3021/22) - Supports the 2246S Serial Workstation, the 2246/56C Combined Workstation, the 2266 S/C Archiving Workstation, or serial printers, in any combination. The 22V27-1 supports up to eight serial devices and the 22V27-2 supports up to 16 serial devices. Also supports the 6554-1/2/3/4 TC Processor.

2. 22V28 Large Disk Drive IOP (WLI P/N 212-3023) - Supports up to four 2265V-1/2265V-2 Storage-Module Disk Drives (SMDs) or 2280V-1/2280V-2/2280V-3 Cartridge Module Disk Drives (CMDs) in any desired combination.

<u>NOTE</u>

<u>The 22V28 IOP is not available in the VS-85-H.</u>

3. 22V88-1/4 Very Large Disk Drive IOP (WLI P/N 212-3050/49/48/47) - Supports up to four 2265V-1/2/3 Storage-Module Disk Drives (SMDs) or Fixed Module Disk Drives (FMDs), or 2280V-1/2/3 Cartridge Module Disk Drives, in any desired combination.

NOTES

1. **The VS-85-H requires the 22V88 IOP with R2 PROMs as well as Operating System software version 6.30 or higher to support the NEC drives.**

2. The 22V65-3 620 MB drive requires support by Operating System software version 6.11 in the VS-85.

4. 22V15-2 Triple-Density Tape Drive IOP (WLI P/N 212-3030) - Supports up to four 2219V-1/2219V-3 Nine-Track Magnetic Tape Transports, in any desired combination. To use this IOP, the optional Cache Memory board must be installed.

5. 22V25-2 Dual-Density Tape Drive IOP (WLI P/N 212-3017) - Supports up to four 2209V-1/2209V-2 Nine-Track Magnetic Tape Transports and 2209V-3 Seven-Track Magnetic Tape Transports, in any desired combination.

6. 22V26-1/2/3 Telecommunications IOP (WLI P/N 212-3018/19/20) - Supports up to three separate synchronous communications lines (including Automatic Calling Units). Currently available line speeds include 1200, 2400, 4800, and 9600 baud. The system can run different protocols on separate lines concurrently from the same IOP. Currently supported industry standard protocols for bisynchronous transmission include 2780/3780 emulation, 3270 emulation, and HASP. Model 2246R Remote Stand-Alone Workstations also can be attached to the system via 22V26 IOPs, either locally through a dummy modem or remotely through a standard modem.

7. 22V67W WangNet IOP (WLI P/N 212-3046) - Supports up to 32 WangNet devices on a single Peripheral Band channel.

1.7 DISPLAY AND MAINTENANCE PANELS

The Display Panel, located in the top left front corner of the mainframe, provides the user with pertinent information concerning the operating condition of all I/O devices connected to the mainframe as well as data concerning the CP status. The panel contains 10 LEDs arranged in one vertical column with four LEDs for CP status and one horizontal row with 6 LEDs for IOP Parity Error status. (See figure 3-3.)

The Display Panel control pushbuttons allow the user to load system or diagnostic microcode, initialize the system, or force it into the Control Mode. These pushbuttons are part of the Display Panel board and are hardwired directly to it.

The Maintenance Panel, located directly below the mini-diskette drive, is used by the CE in conjunction with the microcode diagnostics for troubleshooting the VS-85/85-H mainframe. (Refer to paragraph 8.3.)

1.8 POWER SUPPLY

WARNING

```
*************************************************************
*                                                           *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY       *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND         *
*    CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN       *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.  *
*                                                           *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER           *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                  *
*                                                           *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC  *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,      *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO   *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO      *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                   *
*                                                           *
*************************************************************
```

Power for the VS-85/85-H mainframe is supplied from an OEM switching power supply providing +/-5 Vdc and +/-12 Vdc. The unit is located behind the front cover, directly below the IOP portion of the Motherboard. The unit is not accessible by the customer, and any work involving the unit should be done by a Wang CE. **In addition, the VS-85-H contains a +24 Vdc supply, mounted on the fixed disk drive bracket, which provides power for the NEC drive.** (Refer to Chapter 5, Preventive and Corrective Maintenance.)

1.9 SOFTWARE DESCRIPTION

The VS-85 supports Release 5.03 of the VS Operating System (OS). This software release contains several new features and functional improvements over previous releases. Major areas of change are in the Command Processor, the Operator's Console Menu, and the SYSGEN procedure. Most other features of Release 5.03 are similar to previous releases and are discussed in paragraphs 1.9.3 through 1.9.6.

However, Operating System 5.03 will not support the 22V65-3 620-MB Fixed Module disk drive (FMD). This drive will require a later version of the VS Operating System; e.g. Release 6.10. **The NEC drives in the VS-85-H require OS version 6.30 or higher.**

1.9.1 OPERATING SYSTEM 5.03 DESCRIPTION

Changes in the Command Processor include a slightly changed Main Menu to reflect the combination of two commands, SHOW DEVICE STATUS and MOUNT/DISMOUNT VOLUMES, into one called COMMAND DEVICES. This new command also includes several new options that allow the user to perform such functions as changing mount restrictions and modifying work and spool file eligibility more easily.

Changes in the Operator's Console menu include the displaying and controlling of all devices through separate PF keys (PF9 through PF13), the setting of up to eight workstations as dual operator/user mode terminals with PF14, and the activating of the PRINT I/O ERROR LOG command also with PF14.

Major changes have been made in the SYSGEN Procedure in Release 5.03. These changes include the use of a dynamic procedure as opposed to the assemble and link method of other software releases.

1.9.2 OPERATING SYSTEM 6.10 DESCRIPTION

New operating system release 6.10 includes several new features and functional changes to VS systems. For details, refer to VS Software Bulletin Release 6.10, WLI P/N 800-3111-01. Some of the highlights are listed below.

1. Operating system enhancements:
   a. A Broadcast facility to allow workstation messages to be sent between an Operator's Console and user workstations, including Operator-to-user and user-to-Operator facilities.
   b. Allows assignment of Operator privileges to a User ID as well as to a workstation.
   c. Allows reservation of diagnostic cylinders on 2265V-3 and Q2040 disk drives for stand-alone disk diagnostics.
   d. Extends disk I/O operation timeout period from 60 seconds to 160 seconds.
   e. Changes in the Set Print Mode Default screen to allow spooled print files to be sent to a specific device address (a printer, or a TC device which may be changed to a remote printer) instead of the lowest device-numbered printer available.

2. Networking Operations:
   a. Allows automatically queuing a print file to the Transmit queue so that it can be printed on a remote system.
   b. Allows automatically queuing a print file to the physical system after logging on to a remote VS.

3. COLDSTART:
   a. Can now be used with any VS system.
   b. Permits bringing up a new system by formatting the system disk and copying a minimum system to it.

4. Control Mode Dump:
   a. Is now the same for all VS systems.
   b. Supports an option on VS-24/45/85/90/100 processors to put a dump on a disk volume as a file, using DISKINIT, while preserving the volume's VTOC.

5. System Software:
   a. Enhancements to several utilities, including BACKUP, CONTROL, COPY, DISKINIT, EDITOR, and SECURITY.
   b. Supports a new utility, IOELOG, for examining an I/O error log file.

6. New Devices:
   a. Release 6.10 supports the following new devices - Wang Professional Computer, 6300GM Graphics workstation, 2529V cartridge

tape drive, 2265V-3 620Mb disk drive, SW04(-3) disk switch option, and the 5575 band printer.

1.9.3 OPERATING SYSTEM 6.20 DESCRIPTION

Operating System Release 6.20 contains several new features and functional changes over previous releases. Refer to VS Software Bulletin Release 6.20, WLI P/N 800-3114-01, for a detailed description. The major features are:

1. Operating System Enhancements

   a. A page pool option allows contiguous Segment 2 paging files for reduced access times and improved throughput.
   b. New assignment algorithm and user control permit a more efficient assignment of paging files to volumes.
   c. Automatic workstation logoff disables selected inactive workstations after a predetermined time interval.
   d. The system checks version numbers of operating system program files when IPLed to detect incompatibilities that could interfere with system operation.
   e. The improved IPL procedure recalls configuration file names, optionally provides logon inhibition, and automatically activates remote devices that have been defined.
   f. Control Mode Dump displays two new screens that help to define fatal errors, perform the dump itself, and define the output device.
   g. System task dumps now include Segment 0 control blocks.
   h. Other enhancements include memory parity error recovery, VTOC performance improvement, increased System Queue file size, and remote device support.

2. Release 6.20 SYSGEN Procedure

   a. The General Configuration screen prompts for the number of WangNet workstation lines.
   b. GENEDIT allows the user to define the parameters for remote devices in a configuration file.
   c. The maximum number of open files per task is now 9999.

3. Networking Operations

   a. Release 6.20 supports the Local WangNet Peripheral Band and Wang Systems Networking (WSN) Point-to-Point transport.

4. System Software

   a. Release 6.20 includes enhancements to the following utilities: BACKUP, COPY, DISKINIT, DISPLAY, IOELOG, and SORT. The Symbolic Debugger has also been enhanced.
   b. OS version 6.20 supports the following new utilities: Compress-In-Place (CIP), IOTRACE, POOLSTAT, AND SORTINT.
   c. The Data Management System (DMS) includes support for relative files and shared consecutive files.
   d. Release 6.20 supports the VS Graphics Facility and the VS Multi-Station.

5. New Devices

   a. Release 6.20 supports the following new devices: 4205 workstation, 4220 workstation, 4230 workstation, 4230A workstation, 6300GM graphics Workstation, 2509V serial 9-track tape drive, 2220 disk drive, and the DW/OS-55 daisy printer. OS 6.20 also contains additional TC support and supports new IOPs and device adapters.

1.9.4 OPERATING SYSTEM 6.30 DESCRIPTION

Operating System release 6.30 contains several modifications and enhancements to previous releases. The major functional changes are:

1. Operating System Enhancements

   a. OS 6.30 supports the specification and EXTRACT of several international parameters that allow VS applications to be better translated/customized for international releases.
   b. The Transparent Link allows multiple link levels to be considered as a single link level.
   c. Several Data Management System (DMS) enhancements have been implemented.
   d. The VS transaction recovery and file sharing system (TX) has been enhanced extensively.
   e. Release 6.30 supports CP4 with a maximum physical memory size of up to 16 MB.

2. System Software

   a. The new GENEDIT version, which was rewritten in PL/1, contains extensive changes to the user interface and the addition of a few new fields to the CONFIG file format. Refer to paragraph 4.11 .
   b. Enhancements to the IOTRACE utility include a timer option, allowance for multiple users without duplicate file name conflicts, a print facility for printed or displayed reports, and a menu pick that minimizes the impact of IOTRACE on system resources.
   c. A new utility, SHRSTAT, displays statistics which are continuously collected by the sharing task as it processes user requests.

3. New Devices

NOTE

Multi-workstations have been renamed to a generic 2256MWS with a corresponding microcode file called @2256MWS. The former @EXPMWS microcode file must be renamed to @2256MWS when updating an existing operating system to OS 6.30.

a. Disk Drives

MODEL NUMBER	DEVICE NAME
2267V1	75 MB RSD Disk
2267V1A	75 MB Dual Port
2268V1A	76 MB 8in Dual Port
2268V2A	147 MB 8in Dual Port

NOTE

The 2265V4 was renamed the 2267V1 75 MB RSD Drive. The 2220 was renamed the 2268V1 76 MB 8in Fixed Disk Drive.

b. Printers

MODEL NUMBER	DEVICE NAME	MICROCODE FILE
55731	High Speed Band Printer	@MC55741
55741	High Speed Band Printer	@MC55741

c. IOPs

MODEL NUMBER	DEVICE NAME	MICROCODE FILE
75V02T	Fiberway/Serial IOP	@MC928E

d. Archiver Workstation

MODEL NUMBER	DEVICE NAME	MICROCODE FILE
4250	PC Archiver Workstation	@MC4250
2270V6	5 1/4 Inch Diskette	@MC4250

1.9.5 USER CONVENIENCE FEATURES

The continuing implementation of user convenience features make the VS-85/85-H easy to use by programmers and nonprogrammers alike. These features, along with many others, include a versatile data entry, file maintenance, and report generation facility; an interactive text editor for entering and editing source programs; an easy-to-use symbolic debug facility for program debugging; and a large assortment of system utility programs.

1.9.6 EXPANDED OPERATING SYSTEM FEATURES

Recent changes in the Command Processor include a slightly changed Main Menu to reflect the combination of two commands, SHOW DEVICE STATUS and MOUNT/DISMOUNT VOLUMES, into one called COMMAND DEVICES. This new command also includes several new options that allow the user to perform such functions as changing mount restrictions and modifying work and spool file eligibility more easily.

Changes in the Operator's Console menu include the displaying and controlling of all devices through separate PF keys (PF9 through PF13). PF14 now allows setting up eight workstations as dual operator/user mode terminals, and the activating of the PRINT I/O ERROR LOG command.

1.9.7 ADDITIONAL SYSTEM UTILITIES

The VS-85/85-H system provides a variety of additional system utility programs to support the general programming task. These include, among others, the COPY, SORT, and LINK utilities summarized below.

The versatile COPY utility permits the user to copy a single program or data file, an entire library of such files, or a complete disk volume. For data files, the COPY utility provides an option to change the file organization from sequential to indexed or indexed to sequential.

The SORT utility provides high-speed sorting and merging capabilities for both indexed and sequential files, with either fixed or variable-length records.

The LINK program is used to link together two or more program modules into a single large program, and also offers the option to remove the symbolic debug information previously inserted for debugging purposes.

Other utilities include a translation utility which translates from EBCDIC to ASCII and vice-versa; a special copy utility which copies and automatically translates Wang 2200 program and data files to VS format (and vice-versa); a display utility, which can be used to display and/or print printer files; a procedure language interpreter utility which allows the programming of operational sequences performed without user interaction.

Table 1-4 and table 1-5, below, list currently available VS-85/85-H system utility programs and VS-85/85-H stand-alone utility programs, respectively, with a brief description of the function of each.

Table 1-4. VS-85/85-H System Utility Programs

PROGRAM NAME	DESCRIPTION
ASSEMBLER ...	Assembles a source program written in VS assembler language.
BACKUP	Copies, consolidates, and restores a file, library, volume.
BASIC	Compiles a program written in VS BASIC.
COBOL	Compiles a program written in VS COBOL.
COMPRESS	Consolidates used and free extents on a volume.
CONDENSE	Generates single record type data file from multi-record type.
CONTROL	Creates a Control file that defines all field, record, and file attributes for a specified data file.
COPY	Copies files/libraries/volumes from one location to another. Also modifies/rebuilds file organization or index structures.
COPY2200	Copies and automatically converts files from standard 2200 format to standard VS format, and vice versa.
COPYWP	Copies/deletes/renames/reorganizes/merges documents/libraries from one VS WP system to another. Converts a document to file or a file to document for VS data, source, print, or 2780 TC.
DATENTRY	Creates and/or maintains records in a data file as defined by specifications in Control File(s); also lists or prints files.
DEBUGGER	VS Symbolic Debugger allows user to interactively monitor an executing program, locate and correct errors, and alter flow.
DISKINIT	Initializes, Reformats, Relabels, or Verifies a disk volume. Writes a volume label and optional Volume Table of Contents in VS format. Removes and identifies all bad blocks in VTOC.

Table 1-4. VS-85/85-H System Utility Programs (cont'd)

PROGRAM NAME	DESCRIPTION
DISPLAY	Displays file contents on the workstation screen.
DUMP	Creates a print file from a full Segment 2 memory dump which includes a program's variables, buffers, and control blocks using the DUMP function of the Debug Processor.
EDITOR	Enters, displays, and edits source procedure or program text.
EZFORMAT	Generates a customized data entry and maintenance program corresponding to a user-designed screen format and control file. Alternate to DATENTRY for existing DMS files.
FORMCNTL	Creates Forms Definition file for VS forms-loadable printers.
FORTRAN	Compiles a program written in VS FORTRAN.
FLOPYDUP	Duplicates diskettes, creates/transfers diskette image files.
IBMCOPY	Copies/converts IBM format diskette file to/from VS file for mat soft-sectored diskettes. Translates ASCII to/from EBCDIC.
INFO	A custom on-line help and information documentation facility.
INQUIRY	Interrogates/tests data files for user-specified field values.
IOELOG	Records machine check errors in the I/O error log.
IOTRACE	Monitors the I/O trace table and records I/O information for a range of devices based on user-defined criteria.
LINKER	Combines two or more compiled or assembled program modules into a single executable program.
LISTVTOC	Produces complete or selective listings of a specified volume's Table of Contents, and examines the VTOC for errors.
LISTWP	Generates summary reports of VS WP documents/file attributes.
PL/1	Compiles source programs written in VS PL/1.
PATCH	Modifies specific HEX values or object files. Prints HEX dump.
POOLSTAT	Monitors the utilization of the page pools on a system
PRINT	Places a print file in print queue with user-selected options.
PROCEDURE ...	An Interpreter utilizing a source program written in Procedure Language to perform interactive and/or background operations.
REPORT	Produces customized reports from a data file.
RPG II	Compiles source programs written in VS RPG II.
SAM	Interactive monitor provides performance/usage of VS system.
SECURITY	Protects system resources at System, File, and Access level.
SHRSTAT	Displays statistics which are continuously collected by the sharing task as it processes user requests.
SORT	Sorts records in data file(s) by key values, with optional capability to merge two or more sorted files.
SORTINT	Sorts up to 20 files into a single, ordered output file according to standard ASCII or an external collating sequence.
STABLEMT	Creates or modifies files that define an external collating sequence.
SYSGEN	Generates control blocks that comprise the Operating System nucleus.
TAPECOPY	Copies any combination of files where tape is in/output media.
TAPEINIT	Initializes 7 or 9 track tape to Wang std., IBM , or NO label format; user select Parity, Density, write end-of-tape marker.
TCCOPY	Emulates IBM 2780/3780 protocols for non-VS communication.
TRANSL	Automatically translates files to or from ASCII or EBCDIC character sets. Also translates files according to USER defined translation table.
TTY	Emulates standard, asynchronous (ASCII) teletypewriter device.

Table 1-4. VS-85/85-H System Utility Programs (cont'd)

PROGRAM NAME	DESCRIPTION
VERIFY	Tests primary index, alternate indices, and data chain of indexed files to disclose file structure problems.
VSCOPY	VS to VS communication/manipulation of executable image files.

Table 1-5. VS-85/85-H Stand-Alone Utility Programs

PPROGRAM NAME	DESCRIPTION
COLDSTART ...	Allows operation of a VS system without standard system disk or operating system.
CIP	Consolidates free extents on system disk without full volume backup and restore.

1.9.8 FILE PROTECTION AND SECURITY

All VS-85/85-H system disk and tape files are classified according to a flexible file protection and security system, tailored at installation to the specific needs of the user. This system is under the direct control of the System Security Administrator(s) at each installation. The System Security Administrator(s) are specially recognized users who determine the meaning and use of the file protection classes. They are able to access all files on the system, including the System User List and have unlimited access rights.

1.9.8.1 File Protection Codes

Every program, procedure, and data file on the system can be placed in one of thirty file protection classes. Protection class codes are designated by a capital letter, 'A' through 'Z', which represent protection classes whose meanings are assigned by the System Security Administrator(s). Such assignments normally are given mnemonic relationships, as indicated in the following list of "typical" examples:

Class W = The Work Order File
Class P = The Product File
Class C = The Customer File
Class Q = The Sales Quota File

1.9.8.2 Special Protection Codes

The system also recognizes four special (system) classes, " " (space or blank), "$" (currency symbol), "@" (at sign), and "#" (number or pound sign), each of which are reserved for specific uses:

Class " " - Designates UNPROTECTED FILE: Files in this class may be deleted, executed, read, and/or written to by all users. This is the default class for files that are not assigned a system class.

Class "$" - Designates READ/EXECUTE FILE: This file class allows any system user or program to read and/or execute the file, but only the owner of record (that is, the user who created the file) and the system security administrator can write to it. This class is used for subroutines and macros that can be read and incorporated into other program files, but most be protected against direct modification. All system macros are assigned to this file class.

Class "@" - Designates EXECUTE-ONLY FILE: All users may use the file, but only the owner of record and the system security administrator can read it or write to it. Files which must be protected from modification, should be assigned this classification. All system utility files, at system generation time, should also be assigned to this class.

Class "#" - Designates PRIVATE or SYSTEM SECURITY ADMINISTRATION FILES: These files are not available to any of the normal class codes. The "#" class, unlike the other file protection classes, is used to define one protection class (PRIVATE) for each user. When specified, the "#" class code identifies those files which can be accessed only by the owner of record and by the System Security Administrator.

1.9.8.3 User Access Rights

Before users of the system can access a protected file, they must identify themselves using the LOGON command. At logon time, the user's LOGON ID and PASSWORD are validated by lookup in the SYSTEM USER LIST, and the user's "access rights" are determined relative to the defined file protection classes. Access rights are listed in the SYSTEM USER LIST for each file of a protection class and are used to specify three different levels of privilege in order of increasing responsibility, as follows:

1. BLANK " " - Access by System Security Administrator(s) Only.

2. EXECUTE "E" - Execute-Only Access. Applicable to program files only. User may run files of this class, but may not copy, examine, link, modify, or read them.

3. READ "R" - Read, and Execute Access. Program files may be copied, debugged, and linked. Data files may be opened in INPUT mode only.

4. WRITE "W" - Write, Read, and Execute Access. User has complete access rights and may also Scratch, Protect, Modify, Delete and Debug this classification of files.

These access rights are checked whenever a user attempts to execute a program or procedure, open an existing file, or rename or scratch a file.

1.10 ERROR DETECTION AND CORRECTION

To ensure the integrity of information stored in memory and on external storage devices (disk or tape), the system provides automatic error detection and correction facilities. In physical memory, all single-bit errors are corrected automatically, while multi-bit errors cause an error indication. Similar checks also are performed on information stored on disk or tape.

1.11 CONFIGURATIONS

The modular design of the VS-85/85-H system permits it to be readily expanded with additional physical memory (a maximum of 4 MB), more on-line storage devices (a maximum of 8 devices), and additional workstations and printers (a maximum of 64 serial devices). (See figure 1-2.) Expansion can be carried out with no impact on existing software, except for the need to regenerate the system to update the Operating System software to reflect the newly-added devices. Consequently, the user with distributed data processing requirements can purchase several assorted system configurations of differing size and complexity, and can use a common set of application software on all systems. Typical VS-85/85-H system configurations are as follows:

1.11.1 MODEL NUMBERS

MODEL #	WLI P/N	MEMORY SIZE
VS-85-1	157/177-7225	1 MB
VS-85-2	157/177-7226	2 MB
VS-85-4	157/177-7228	4 MB
VS-85-76F	157/177-7291	1,2, or 4 MB
VS-85-147F	157/177-7292	1,2, or 4 MB

Part number prefix 157 = 50 cps/230 Vac systems
Part number prefix 177 = 60 cps/115 Vac systems

NOTE

The serial numbers of all VS-85/85-H systems contain two-character prefixes. These prefixes have the following meaning:

- AU - indicates a VS-85-H system (AU5000 thru AU9999).
- GL - indicates one of the first 150 VS-85 standard systems (GL5200 thru GL5349).
- OH - indicates a later VS-85 standard system (OH0200 thru OHXXXX).

1.11.2 DOMESTIC UPGRADE KITS

MODEL #	WLI P/N	DESCRIPTION
UJ-3188	206-3188	1MB to 2MB
UJ-3192	206-3192	2MB to 4MB
VS-85 CACHE	VS-85 CACHE	32K Cache Option (MW)
VS-85-H CACHE	177-7336	32K Cache Option (ML)

1.11.3 INTERNATIONAL UPGRADE KITS

MODEL #	WLI P/N	DESCRIPTION
UJ-3188	205-3188	1MB to 2MB
UJ-3192	205-3192	2MB to 4MB
VS-85 CACHE	VS-85 CACHE	32K Cache Option (MW)
VS-85-H CACHE	157-7336	32K Cache Option (ML)

741-1492

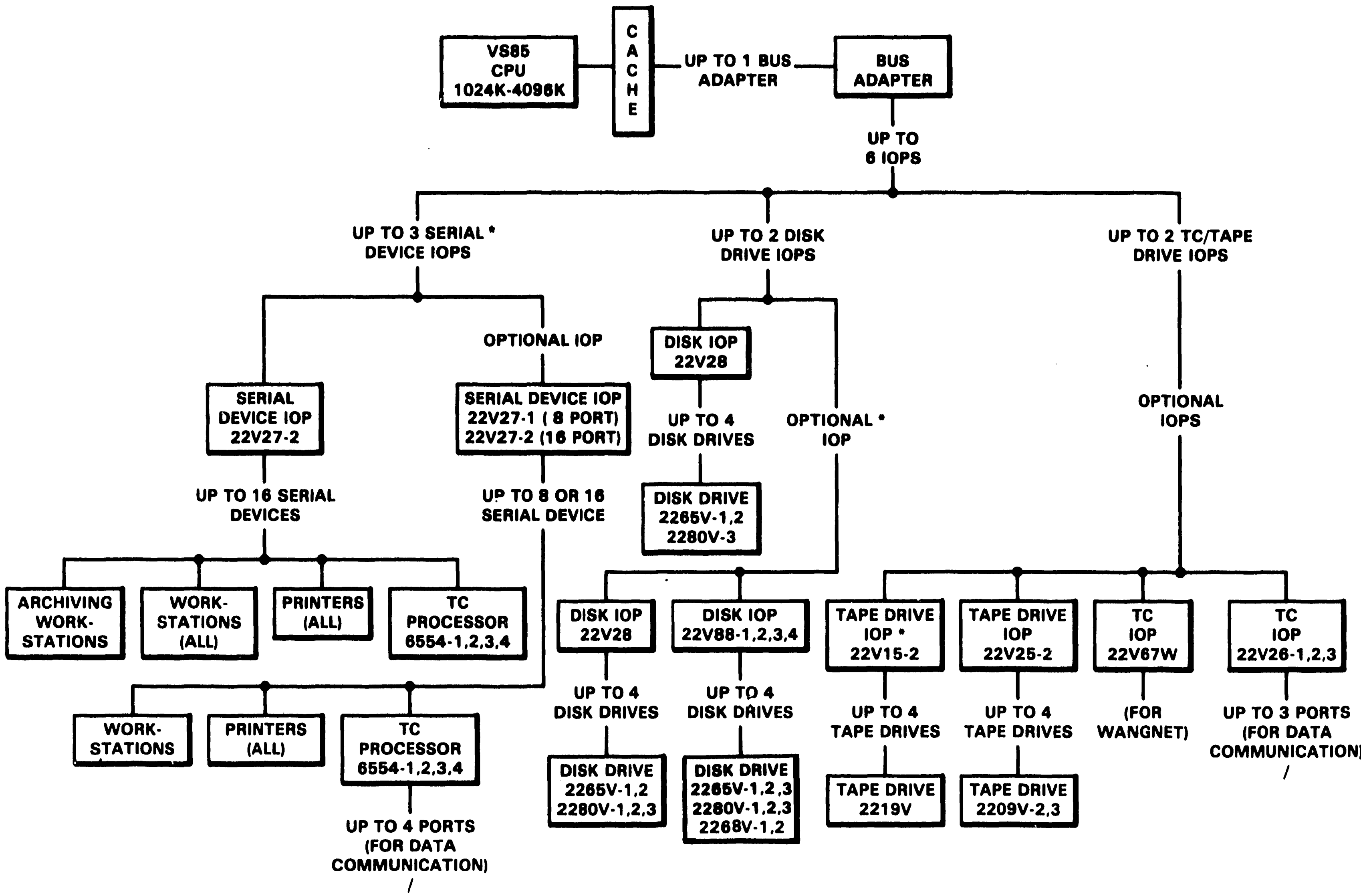


Figure 1-2. VS-85/85-H Configurations

1.12 ASSOCIATED PERIPHERALS

The VS-85/85-H system supports currently offered VS peripheral devices, with the exception of all parallel workstations and printers. The following tables list the peripherals available for the VS-85/85-H.

NOTE

The VS-85-H does not support the 22V28 IOP.

Table 1-6. Serial Devices

DEVICE	MAXIMUM #	IOP	NOTES
Workstations and Printers	32	22V27-1/2	CPU without optional Cache Memory. Supports all VS workstations/Printers
Workstations and Printers	64	22V27-1/2	CPU with optional Cache Memory Supports all VS workstations/Printers

Table 1-7. Disk Devices

DEVICE	MAXIMUM #	IOP	NOTES
2270V-1/2/3	32	22V27-1/2	CPU without optional Cache Memory. Plus 32 Archiving Workstations
2270V-1/2/3	64	22V27-1/2	CPU with optional Cache Memory Plus 64 Archiving Workstations
2280V-1/3	4	22V28	CPU without optional Cache Memory
CMD	(8)	(")	(CPU with optional Cache Memory)
2265V-1	4	22V28	CPU without optional Cache Memory
SMD	(8)	(")	(CPU with optional Cache Memory)
2265V-2	4	22V28	CPU without optional Cache Memory
SMD	(8)	(")	(CPU with optional Cache Memory)
2265V-3	4	22V88-1/4	CPU without optional Cache Memory
FMD	(8)	(")	(CPU with optional Cache Memory)
2267V-1	4	22V88	CPU without optional Cache Memory
RSD	(8)	(")	(CPU with optional Cache Memory)
2268V-1	**4**	**22V88-1/4**	**CPU without optional Cache Memory**
WINC	**4**	**(")**	**(CPU with optional Cache Memory)**
2268V-2	**4**	**22V88-1/4**	**CPU without optional Cache Memory**
WINC	**4**	**(")**	**(CPU with optional Cache Memory)**

Table 1-8. Tape Devices

DEVICE	MAXIMUM #	IOP	NOTES
2209V-2/3	4	22V25-2	Kennedy tape drives, all models
2219V	4	22V15-2	Telex tape drives. Requires optional Cache Memory

Table 1-9. Telecommunications Processors

DEVICE	MAXIMUM #	IOP	NOTES
6554 TCP	1	22V27-1/2 ...	1 TCP with maximum of 4 ports
TC IOP	2	22V26-1/2/3 .	6 data communications ports maximum

1.13 SYSTEM SPECIFICATIONS

DIMENSIONS

	INCHES	CENTIMETERS
Width	27.0	68.6
Height	36.0	91.4
Depth	29.0	73.7

SERVICE CLEARANCES

	INCHES	CENTIMETERS
Front	36	91.4
Rear	24	60.9
Left	0	0
Right	0	0
Top	20	50.8

NET WEIGHT

	POUNDS	KILOGRAMS
VS-85	300	136
VS-85-H	350	159

POWER REQUIREMENTS (DOMESTIC)

	115V/60Hz	208-240/60Hz
Ac Variation	+/-10%	+/-10%
Amps (VS-85)	7.0	3.5
Amps (VS-85-H)	15.0	7.5
Watts (VS-85)	805	805
Watts (VS-85-H)	1388	1388
Dedicated Circuit VS-85/85-H	Yes. With 30 Amp (115 Vac) or 20 Amp (208-240 Vac) circuit breaker in the computer room.	

POWER REQUIREMENTS (INTERNATIONAL)

	230V/50Hz
Ac Variation	+/-10%
Amps (VS-85)	3.5
Amps (VS-85-H)	7.5
Watts (VS-85)	805
Watts (VS-85-H)	1388
Dedicated Circuit	Yes. With 20 Amp circuit breaker in the computer room.

HEAT OUTPUT

	BTU/HR	KCAL/HR
VS-85	2737	690
VS-85-H	4720	1180

TEMPERATURE

	MINIMUM	MAXIMUM
Fahrenheit	+60°	+90°
Celsius	+15.5°	+32.2°

HUMIDITY

	MINIMUM	MAXIMUM
Non-condensing	20%	80%

ALTITUDE (Note)

	FEET	METERS
Maximum	10,000	3048

CABLE LENGTH

	FEET	METERS
Power (VS-85)	8	2.4
(VS-85-H)	9	2.9

NOTE

Tape drives installed above 4000 ft. (1200 meters) and disk drives installed above 6500 ft. (1960 meters) require high-altitude options.

VS-85/85-H ARCHITECTURAL SPECIFICATIONS

Minimum Main Memory	1 MB	Console controller	N/S
Maximum Main Memory	4 MB	Maximum storage/diskette	N/S
Incrmntl Main Mem (VS-85)	1/2 MB	Maximum # of IOPs	6
Incrmntl Main Mem (VS-85-H) ..	1/2 MB	Maximum # serial devices	48
Control Memory size (VS-85) ..	8K Inst	Concurrent serial W/Ss (Note)	32/64
Control Memory size (VS-85-H)	12 KB	Maximum # of disk, no Cache	4
Cache (optional)	32 KB	Maximum # of disk, w/Cache	8
Max disk storage, no Cache ...	2.4 GB	Maximum # of tape drives	4
Max disk storage, w/Cache	5.1 GB	Maximum # of TC lines	6

Main Memory cycle time	480 ns	Microinstruction cycle time ...	160 ns
MCII/SBC cycle time	160 ns	Cache cycle time	160 ns
CP data path	32-bit	Main memory data path	64-bit
CP Address path	24-bit	Main Memory address path	20-bit
CP word length	32-bit	IPC word	32-bit
BA-IOP data path	16-bit	BA-IOP Control path	8-bit
System Clock	25 Mhz	Main Memory refresh cycle	15 us
Memory bandwidth, no Cache .	8.3 MB/s	Virtual address space/user	2 MB
Memory bandwidth, w/ Cache .	16.6 MB/s		

N/S = Not supported.

NOTES

1. Thirty two (32) concurrent serial workstations without Cache option.

2. Sixty four (64) concurrent serial workstations with Cache option.

CHAPTER 2 THEORY OF OPERATION

CHAPTER 2

THEORY OF OPERATION

2.1 INTRODUCTION

The VS-85/85-H consists of eight major board assemblies, as shown in figures 2-1 and 2-2, the System Block diagrams. The System Block diagrams should be used to observe the multitude of interboard signal lines and busses and the direction of data flow while reading the block theory of operation. Because the I/O Processor (IOP) is common to other VS systems, it will only be referred to when necessary in relation to the remaining seven boards. A block diagram of the major logic elements on the other boards accompanies the theory of the board. The theory explains the major logic element functions of each board, but these explanations do not trace specific signals, busses, or microinstructions through the entire system.

The VS-85/85-H architecture is the same as the VS-100, but the basic VS-85/85-H does not have the VS-100's Cache memory. Cache Memory is an option and, when installed, must be accompanied by a System Bus Controller (SBC). Cache allows the VS-85/85-H 64-bit Main Memory access. When the Cache/SBC is not installed, it is substituted by a Memory Controller I (MCI) board and a Memory Controller II (MCII) board combination. The MCI and MCII combination allows only 32-bit Main Memory access. The MCI provides all of the normal memory control functions of the Cache, but does not have the 32 KB of RAM memory. The MCII is similar to the SBC, except that one half of the 64-bit path to Cache has been removed. The Bus Adapter (BA) functions remain the same, except that the BA is signaled as to when a Cache/SBC is or is not installed. This permits the BA to process either 32-bit or 64-bit data words.

The VS-85/85-H minimum Main Memory, without the Cache Memory/SBC option, is 1 MB and the maximum memory is 4 MB. However, a VS-85/85-H with the Cache Memory/SBC option must be configured with a minimum of 2 MB of Main Memory.

2.2 CONTROL MEMORY

The VS-85/85-H Control Memory (CM), (figure 2-3) a loadable Random Access Memory (RAM), stores all Central Processor (CP) microinstructions. The loadable CM permits CP microcode updates, microcode expansion, and use of microlevel diagnostics. The CM board, containing 8K (12K in the VS-85-H) of 50-bit instructions, is separate from the CP to allow flexible CM size. The CP branch field allows 14-bits (16K possible locations) for CM addressing. CP microinstructions are 6 bytes (48 bits) long with a seventh byte containing two parity bits.

All system microcode is recorded on a minifloppy diskette. A simple, low cost, minifloppy diskette drive is used to load the microcode into the CM RAM. A 1K PROM, located on the diskette drive controller, contains microroutines to support the minifloppy Z80 microprocessor during the microcode loading.

Fetching a microinstruction from CM requires a full 48-bit path to the CP. Two microinstructions, Write Control Memory and Read Control Memory, are

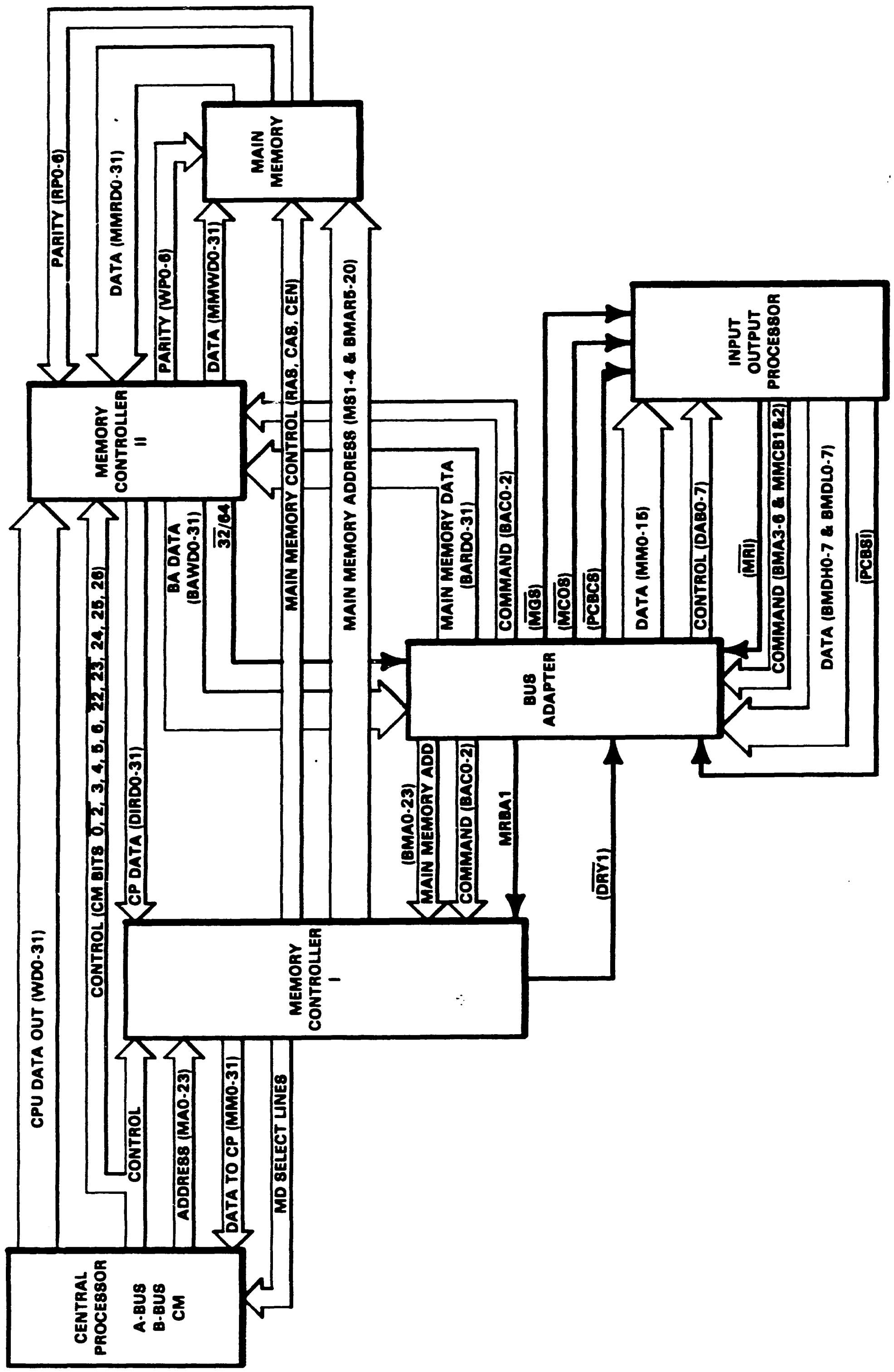


Figure 2-1. VS-85/85-H System Block (with MCI/MCII)

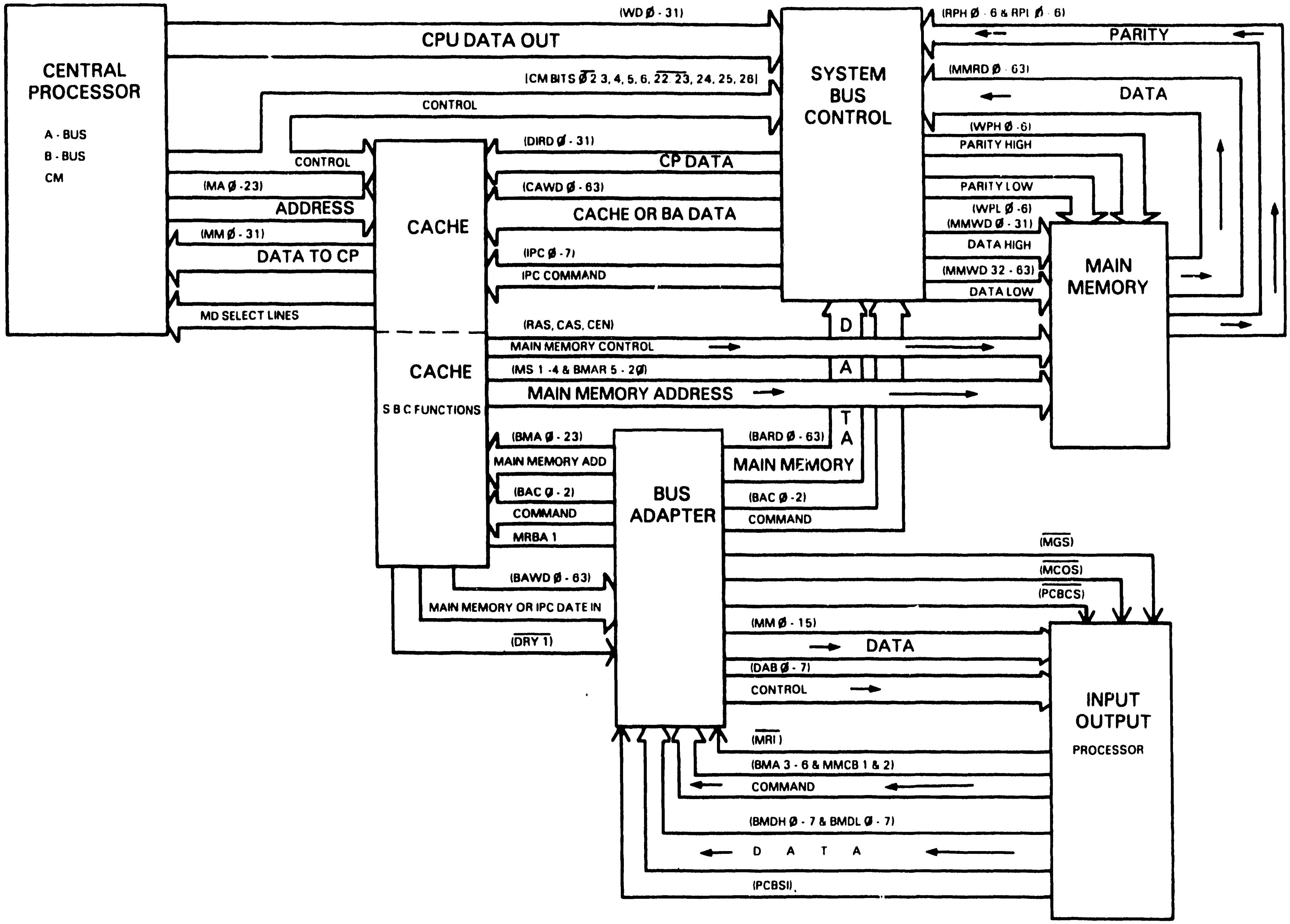


Figure 2-2. VS-85/85-H System Block (with Cache/SBC)

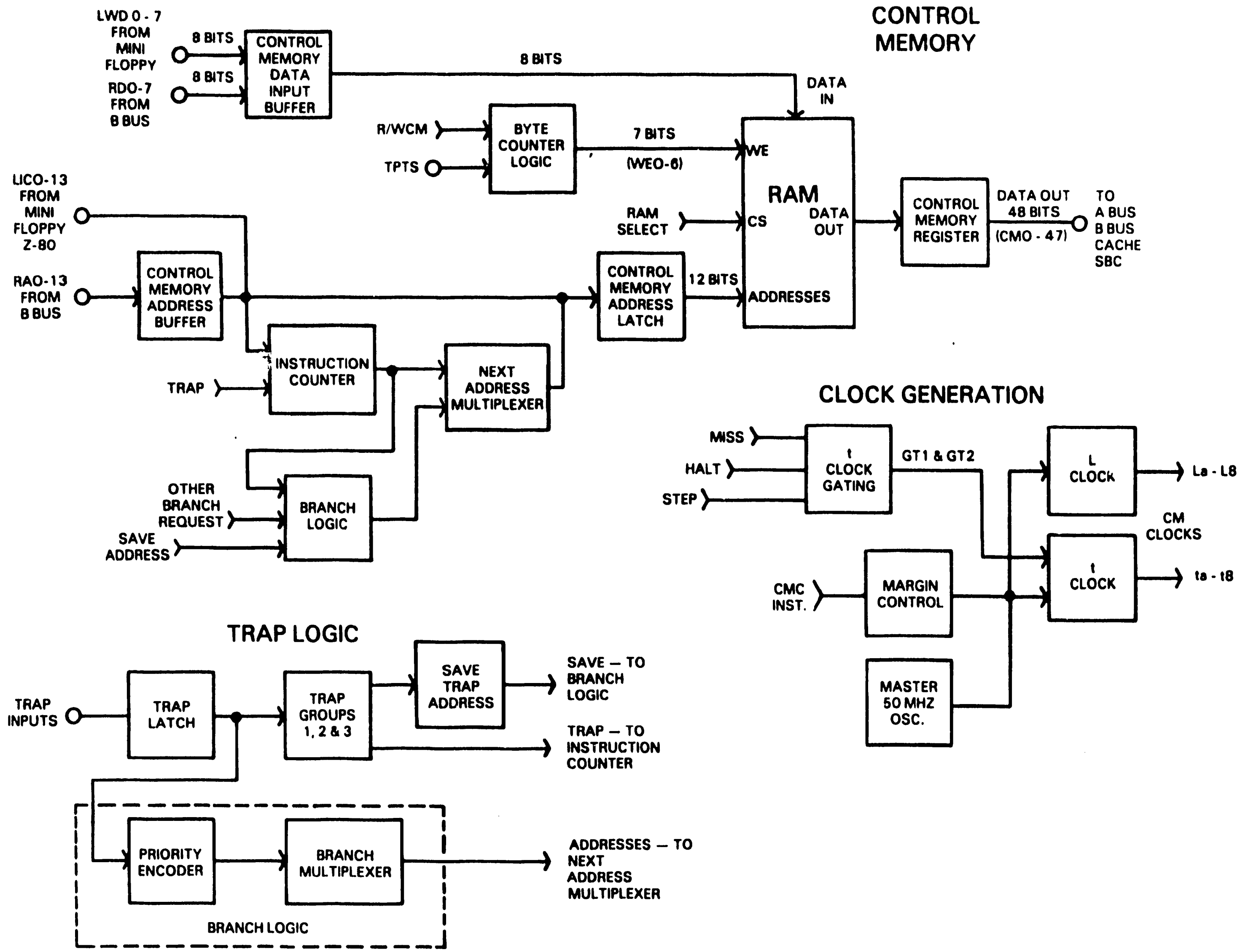


Figure 2-3. VS-85/85-H Control Memory

provided for reading or writing one CM byte at a time. Traps, branching, and master timing are all functions of the CM board, even though not directly related to CM functions.

2.2.1 WRITING CONTROL MEMORY

There are two methods for writing to CM RAM. The first method allows the system microcode to be loaded from the minifloppy diskette using the CP 'BT' (BOOT) button on the front panel. One byte of data read from the minifloppy, as LWD0-7, is written through the CM Data Input Buffer to a RAM location. Addresses (LIC0-13) are supplied to the CM Address Latch from the Z80 microprocessor chip on the minifloppy controller as the data is read from the diskette. A Byte Counter tallies the number of bytes loaded for each CM word. The Byte Counter increments the RAM write enable inputs (WE0-6) each time a byte is written. As each CM word is 50 bits long (48 data and 2 parity), the Byte Counter cycles 7 bytes per word. When the last byte of a word has been written, the counter is reset.

The second method, using an outer level Patch CP microcode instruction, can be used for testing microcode updates. CM is modified one byte at a time using RD0-7 (6 data bits and 2 parity bits) from the Program Mask Register on the B Bus through the CM Data Input Buffer. The byte will be written to the RAM using addresses (RA0-13) from the B Bus Virtual Memory Address Register to the Control Memory Address Buffer and through the Control Memory Address Latch. The Byte Counter tallies the number of bytes loaded for each CM word.

2.2.2 READING CONTROL MEMORY

After the system microcode has been loaded, pressing the System Load button on the front panel causes a trap (see paragraph 2.2.3) and branch to CM location zero to begin system IPL execution. The trap address will be forced into the Branch Multiplexer (BRMX) and sent to the Next Address Multiplexer (NAMX) for loading into the Control Memory Address Latch (CMAL). The Instruction Counter is also loaded with this current address and incremented by one to prepare the next address. The RAM write enable inputs are inactive, allowing the RAM to be read. The Control Memory Register is always output enabled and the data, as CM bits 0-47, is available to the A Bus, B Bus, Cache Memory/MCI, and SBC/MCII. The sequential incrementing of the Instruction Counter and the fetching of microinstructions continues unless interrupted by branch, trap, or write CM operations.

Table 2-1. VS-85/85-H Trap Addresses

TRAP	CONDITION	TRAP ADDRESS
POWERON	CP Power-on	0000
LOAD	CP Initialize	0001
INVA	Invalid (physical) Memory Address	0002
TT0	MAR0 Translation	0003
TT1	MAR1/MAR2 Translation	0004
TT2	Protection (any MAR)	0005
ATR1	Word Alignment (CM27-29 = 001)	0006
ATR2	Word Alignment (CM27-29 = 010)	0007
ATW	Word Alignment (write)	0008

Table 2-1. VS-85/85-H Trap Addresses (cont'd)

TRAP	CONDITION		TRAP ADDRESS
ATMO	Alignment MARO (halfword)		0009
OVFT	Overflow (ACT or SCT instructions)		000A
MMPT	Main Memory Parity		000B
BEX	Execute Target	(EXEC = 1)	000C
PAR	CP Control Memory Parity		000D
BX	External Event	(EXT = 1)	0011
BDEBUG ..	Software	(DEBUG = 1)	0012
BCLKM ...	Clock Maintenance	(CS1 = 1)	0013
BCLKI ...	Clock Interrupt	(CS3 = 1; CS4 = 1)	0014
BIO	IO Interrupt	(IO3 = 1; IOMASK = 1)	0015
BPAGE ...	Pagebreak	(PAGEOV = 0)	0016
BENTRY ..	Entry Pagebreak	(New PAGEOV = 0) and not rr case)	0017

Trap BEX and traps 0011-0017 are Branch to Next Macro-related traps.

2.2.3 TRAPS

Traps, interrupts to the CP microprogram, are caused by conditions not initiated within the CP. (Refer to table 2-1.) CP microtrap conditions can occur due to process, memory, branch field operations, or external conditions. When a trap condition is detected, the hardware forces a branch to a specific CM address, determined by the type of trap, for execution of a routine intended to take action in response to the condition causing the trap. All microtraps branch to locations in the CM RAM. Return addresses can be saved, when necessary, with a microroutine that follows the trap handling routine, so that execution of a program in progress prior to the trap can resume. Traps are first loaded into the Trap Latch for servicing. The trap will be prioritized to produce a specific CM address of the trap handling routine for the BRMX. The address from the BRMX will be sent to the NAMX for loading into the CMAL and the trap routine will begin execution. The Instruction Address Counter is also loaded with this current address and incremented by one.

2.2.4 BRANCHING

Three formats of branching are available to the VS-85: full address, conditional, and status setting. All are dependent on the state of the current microinstruction branch field. The branch field logic decodes the current microinstruction branch field, CM bits 30-33. The BRMX (using CM bits 34-47 and other inputs to determine a branch address) loads the address into the NAMX. The NAMX might also contain the contents of the Instruction Counter (used for status setting and certain types of branching).

The address is loaded from NAMX into the CMAL for instruction execution. The Instruction Counter is also loaded with the address from NAMX and incremented by one. This logic operates much the same as trap logic as far as sequencing is concerned. The branch logic also allows nesting of branch routines to a depth of 16 when certain branch conditions require current or next microinstruction addresses to be saved.

2.2.5 CLOCK GENERATION AND CONTROL

The VS-85/85-H Master Clock is generated by a 50 MHz oscillator and is then divided by two. The clock produces two strings of 40 nanosecond master timing pulses, L times (La-L8) and t times (ta-t8). The t times are activated by the free running L times and are delayed 20 nanoseconds from the L times. A different number of L and t time clocks occur for each microinstruction execution. The instruction length time period is synchronously controlled by a binary counter. This counter is counted up from 0 to 2 and then loaded with the results of the decoding of CM bits 0-6. CM0-6 determines the type of instruction to be executed. The counter then resumes count from this new value. When the counter reaches a count of 15 (F) this signals the end of the instruction length. The counter is reset and the L sequence begins again.

The master clock is distributed to the A and B Bus for generation of their own L and t times in synchronization with the CM board. Gating signals GT1 and GT2 will reset the t time clocks on the CM, A Bus, and B Bus, to halt program execution upon occurrence of certain conditions such as Cache miss, halt, and the run/step maintenance switch.

The clock margin control logic varies the L time and t time clock frequencies within 10% of the standard frequency. Microinstructions are available to increase or decrease the clock speed, or to reset the clock speed to normal. The use of these microinstructions is for detecting marginal hardware problems and not for system performance acceleration.

2.3 CENTRAL PROCESSOR

The Central Processor (also known as CP4) is the heart of the VS-85/85-H system. The primary task of the CP is to execute the machine instruction set and monitor the results of execution. The CP contains facilities for addressing physical main memory, fetching and storing information, arithmetic and logical processing of data, sequencing instructions in the desired order, and initiating communication between MM and external devices. The CP is composed of two boards, the A Bus and the B Bus, with each board containing many standard and unique logical elements.

2.3.1 A BUS

The VS-85/85-H A Bus (figure 2-4) contains all A Bus registers and multiplexers, the status register, multiplier, stac:, and program clock.

2.3.1.1 C Bus Main Memory Multiplexer (CBMMX)

The CBMMX, 32 bits wide, receives C Bus data (CB0-31) from the B Bus board, or Main Memory data (MM0-31). The C Bus inputs are selected by default (no MM read) while the MM data inputs are selected when MM is being read. The data can be transferred to four possible receiving elements: Memory Data Registers 2, 3 or, 4, or Multiplier Buffer Storage 1.

2.3.1.2 Memory Data Registers 2 and 3, and Rotating Multiplexer

The three memory data registers (MDR 2, 3, and 4) are also 32 bits wide. MDR 2 and 3, in conjunction with Memory Address Register 1 (MAR1), provide

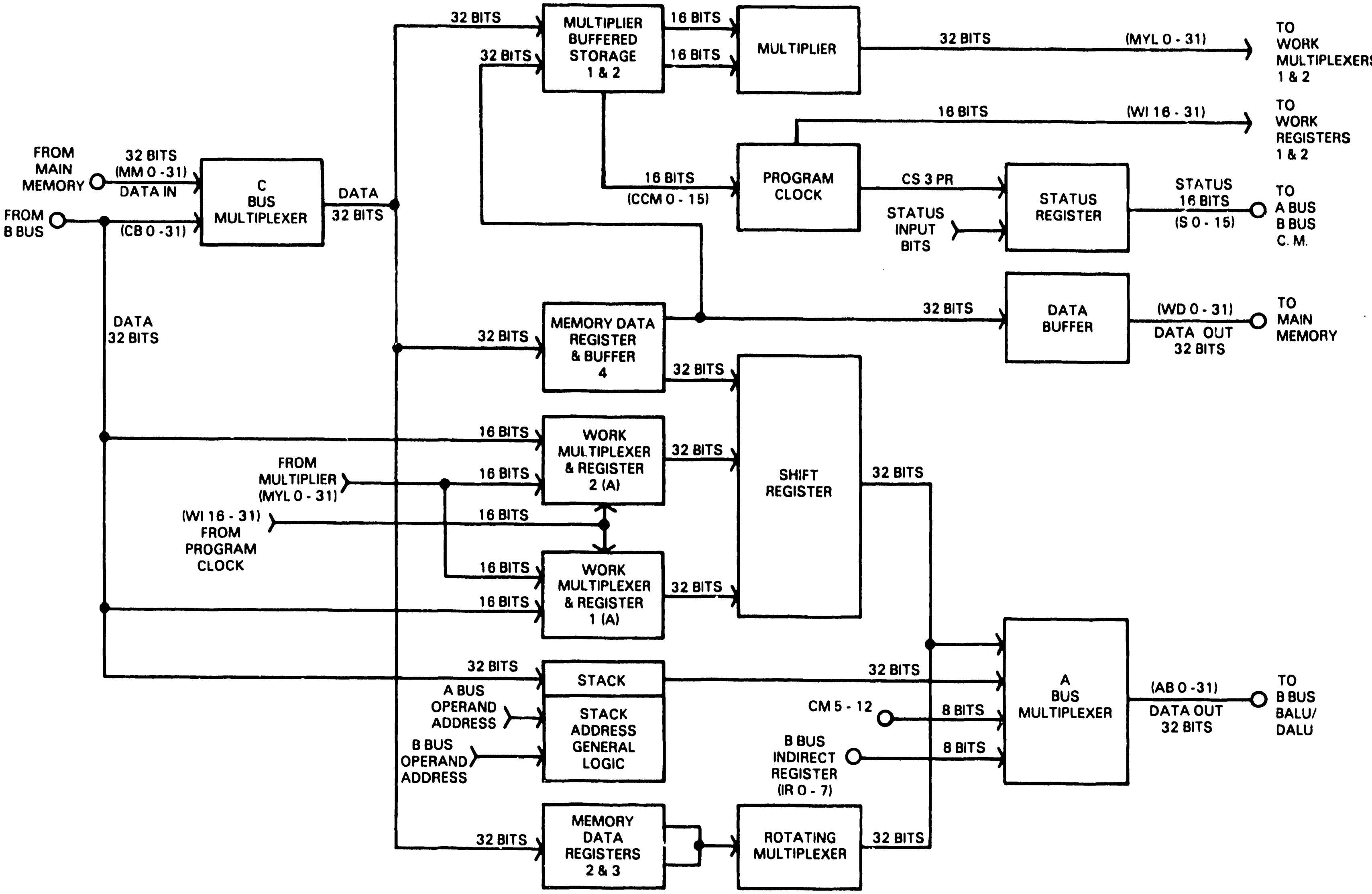


Figure 2-4. VS-85/85-H A Bus

buffered read access of four non-aligned bytes for storage to storage operations. MDR2 is also used for general memory operations. Output data (from MDR2 or MDR3) is sent to the Rotating Multiplexer (RMUX). Two CM bits and three MAR1 address bits determine which data bytes (a maximum of 4) from the available four data bytes will be sent to the RMUX. Whether MDR2 or MDR3 is selected depends upon gating developed on the Cache/MCI board from decoded memory commands.

The RMUX is 32 bits wide and has the ability to shift the four bytes of a word to suit the requirements of the particular instruction being executed. For example, the Switch 16 instruction requires that the high and low halfwords be reversed. The RMUX input data can come from either MDR2 or MDR3. The 32 bits of output data are Or'd with the Shift Register output data and forwarded to the A Multiplexer. The RMUX function select process is used in conjunction with MDR2/MDR3 Byte Selection. Byte selection determines whether one byte or all bytes of MDR2 or MDR3 are sent to the RMUX. The RMUX function select logic determines in what order the bytes are to be transmitted on the RMUX output lines.

2.3.1.3 Memory Data Register 4, Data Buffer, Work Multiplexers/Registers, and Shift Register

Memory Data Register 4 (MDR4), a 32-bit register, along with Memory Address Register 2 is available as a general purpose register for memory data, and Interprocessor Communications data. It is the data output path to Main Memory. Input data comes from the CBMMX and is transferred out by gating developed on the Cache/MCI board from decoded memory commands. The output is forwarded to the Data Buffer (DTBF), Memory Register 4 Buffer (M4BF), and Multiplier Buffer Storage 2 (MBS2).

The 64-bit Data Buffer (DTBF) receives 32 input bits from MDR4 and transfers 32 bits, as WD0-31, to MM via the SBC/MCII. The remaining 32 bits (identical to WD0-31) are used for the CP Tester Interface.

Memory Register 4 Buffer (M4BF) is a buffer between MDR4 and the Shift Register. The buffer is controlled by several process field A Bus operations.

The Work 1 and Work 2 Multiplexers (WMX1 and WMX2) are each 16 bits wide. WMX1 selects bits 16-31 from either the C Bus or the Multiplier for delivery to Work 1 or Work 2 Registers. The C Bus input is selected by a multiply operation decoded from an instruction memory operation field. The outputs are enabled by not performing a Store Counter or Store Comparator operation. WMX2 multiplexer selects bits 0-15 from either the C Bus or the Multiplier for delivery to Work 1 or Work 2 Registers. WMX2 is identical in operation and controls to WMX1.

The Work 1 and Work 2 Registers (WK1-A and WK2-A) are both 32-bit registers. They are used for gating data from WMX1 and WMX2 to the Shift Register (SR) Both can also transfer the Program Clock outputs to the SR as data bits 0-15 or 16-31. The outputs are controlled by Work 1 and Work 2 A Bus operands.

The 32-bit SR operates in three shift modes; shift 1 bit right, shift 4 bits right, or shift 4 bits left. For all other functions, the input data (from MDR4, WK1, or WK2) is gated directly through. The 32-bit output is forwarded to the A Multiplexer. Channel selection for the SR is accomplished using the Shift instruction group.

2.3.1.4 Multiplier

Multiplier Buffered Storage 1 (MBS1) and Multiplier Buffered Storage 2 (MBS2) are 32 and 16-bit storage buffers for the Multiplier. MBS1 input data comes from the CBMMX. MBS2 input data comes from MDR4, and MBS2 forwards 16 of the 32 input bits to the Multiplier. Output of both MBS1 and MBS2 are controlled by the memory field translation and ripple operations.

The Multiplier consists of 4 high-speed 8 X 8 multiplier chips which multiply two 16-bit operands to form a 32-bit output result. The Multiplier inputs are from MBS1 and MBS2. The outputs, after passing thru a 4-bit binary full-adder, are forwarded to WMX1.

2.3.1.5 A Bus Multiplexer

The 32-bit A Bus Multiplexer (AMX) collects data from several sources. It receives its high order 24 input bits from the Stack, or from an Or'd combination of RMUX and the Shift Register. The low order 8 input bits are from five possible sources: Stack bits 24-31, RMUX bits 24-31, Shift Register bits 24-31, B Bus Indirect Register bits 0-7, or CM bits 5-12. Output data, AB0-31, is used at the Binary Arithmetic Logic Unit (BALU) and the Decimal Arithmetic Logic Unit (DALU).

2.3.1.6 CP Stack

The CP Stack, a local RAM storage area, is configured as 256 32-bit registers logically divided into two halves of 128 32-bit registers. The first half of the Stack is again divided into two banks of 64 32-bit registers, containing general registers used for address calculation and accumulation of fixed point arithmetic or logical operations, and floating point registers used for floating point arithmetic operations. Other registers in the Stack include file and auxiliary registers used as temporary storage areas for microprogram functions, and control registers used to store Program Control Word (PCW) trap addresses and the time of day. The second half of the Stack is used for Translation RAM (T-RAM) monitoring. (Refer to paragraph 2.3.2.10.1, the T-RAM.)

The unit of access from the Stack is always 32 bits (one word). Since the Stack access time is significant compared to the total microinstruction cycle time, only one Stack access is performed within a microinstruction. The Stack can be addressed using A Bus operands (read only access) or C Bus operands (read and write access). The Stack is addressed using 8 bits made up of some of the following: Bank Select Status bit, CM bits 8-12 (for A Bus selection), CM bits 17-21 (for C Bus selection), Indirect Register bits 0-7, and Current Halfword bits 0-3.

The A Bus Operand Multiplexer, in the Stack Address General Logic block, selects and delivers the appropriate A Bus operand Stack address value to the Stack via the A/B operand Stack Address Multiplexer. The multiplexer has 8 inputs, one of which can be selected according to the value of CM bits 7,10, and 11. CM bit 7 specifies direct Stack access. Stack write operations are not allowed with A Bus operands (read operations only). Channel 4 of the multiplexer is selected for access to the Operating System File Registers.

The C Bus Operand Multiplier, in the Stack Address General Logic block, selects and delivers the appropriate C BUS operand Stack address value to the Stack via the A/B operand Stack Address Multiplexer. The multiplexer has 4 inputs, any one of which can be selected according to the value of Control Memory bits 16, 19, and 20. Control Memory bit 16 allows direct Stack access and also write enables the Stack. Channel 3 of the multiplexer is selected for access to the Operating System File Registers.

The Stack Address Multiplexer (STKMX) is also part of the Stack Address General Logic. It is used to gate either the A Bus operand or C Bus operand address to the Stack address lines. The multiplexer is always output enabled and A or B half selection depends on the value of Stack Load, decoded from Control Memory bits 16-18.

2.3.1.7 CP Status Register

The CP maintains a 32-bit status register whose contents are designated S0 through S31. The status bits are described in four 4-bit and two 8-bit groups as follows: Loop Control, MAR0 Status, Decode, Indirect Register, Bank Select/MAR2 Translation, and Process Field/ Miscellaneous. (Refer to table 2-2.) The Loop Control status bit group contains the most frequently used status bits. Only status bits S0-S15 can be directly accessed for conditional branch operations. For Status Setting operations, the A and B status bit select fields of the Status Setting portion of the branch field format can indicate any one of the 32 status bits. CM bit 39 indicates A bit usage or A bit inverse usage. (The CP Assembler supports A bit inverse usage through the SSI mnemonic.) The bit operations are indicated by Status Operation Control Memory bits 40-41. The B bit is updated with the resultant bit value. The CM bit 40-41 assignments are Move, And, Or, and Xor. (Refer to Appendix A for a complete list of the CP status bits).

Table 2-2. VS-85/85-H Status Bit Groups

GROUP NAME	STATUS BITS
Loop Control	S0-S3
MAR0 Status	S4, S21-23
Decode	S24-31
Indirect Register	S13-15, S19
Bank Select/MAR2 Translation	S6-7, S16, S20
Process Field/Miscellaneous	S5, S8-12, S17-18

2.3.1.8 Program Clock

The CP supports a 64-bit program clock and comparator at the macrolevel. The hardware provides a 16-bit counter and a 16-bit comparator. These 16 bits correspond to the low order 16 bits of the macrolevel registers. There are four CP status bits (CS1-4) associated with clock operations. A Continuous Counter (CCNT) increments once every 500 nanoseconds and when a carry out at the high order bit of the counter occurs, the hardware will set a Counter

Overflow status bit. The Continuous Comparator (CCMP) is enabled by a Compare Enable status bit. The counter is compared against the comparator for every counter increment. If the counter value is greater than or equal to the comparator, the Clock Interrupt Request status bit is set.

Clock related microinstructions are available to set the counter to zero, store the counter (in WK1-A and WK2-A registers), load the comparator, and store the comparator. The CP can move the counter contents (process field) and counter overflow bit (branch field) within one microinstruction.

There are 2 clock microtraps related to the clock status bits. These traps can occur only within the Branch to Next microinstruction. The Clock Maintenance microtrap (BCLKM) is taken when the Continuous Counter overflows. This microtrap is used to propagate the carry-out from the hardware counter into the high order 48 bits of the macrolevel clock. The Clock Interrupt microtrap (BCLKI) is taken when both the Clock Interrupt Request and the Clock Interrupt Enable status bits are set. This microtrap is used to determine Clock Interrupts at the macrolevel.

2.3.2 B BUS

The VS-85/85-H B Bus (figure 2-5) contains all B Bus registers, buffers and multiplexers and the translation RAM, binary ALU, and decimal ALU.

2.3.2.1 C Bus Main Memory Multiplexer (CBMMX)

The CBMMX, 32 bits wide, receives either main memory data (MM0-31), or C Bus data (CB0-31) for the B Bus. The main memory data inputs are selected when main memory is being read and the C Bus inputs are selected by default (no main memory read). The data can be transferred to three possible receiving elements, Memory Data Register 0, 1, or 4B.

2.3.2.2 Memory Data Registers 0, 1, and 4B, and Current Halfword Buffer

Memory Data Register 0 and 1 (MDR0 and MDR1), both 32-bit registers, are dedicated to accessing halfwords from the macroinstruction stream to provide overlapped macroinstruction fetching. Input is MM data from the C Bus Main Memory Multiplexer (CBMMX). Whether MDR0 or MDR1 is selected depends upon the decoding of process field C Bus destination operands and gating developed on the Cache/MCI board from memory commands.

Multiplexed access of the 16-bit Current Halfword from MDR0 or MDR1 is controlled by Virtual Memory Address Register bits 21-22 passed through the Control Memory Address Buffer (RABF) to the Current Halfword selector. The Current Halfword (CH0-15) is then forwarded to the B Bus Multiplexer (BMX). Also, the high order byte of the Current Halfword will be sent to the Current Halfword Buffer.

The 32-bit Memory Data Register 4B (MDR4B buffered) is a buffer between input data from the CBMMX and the output data to the BMX. The register is selected by decoding of process field C Bus destination operands and by gating developed on the Cache/MCI board from memory commands. The register output is always enabled.

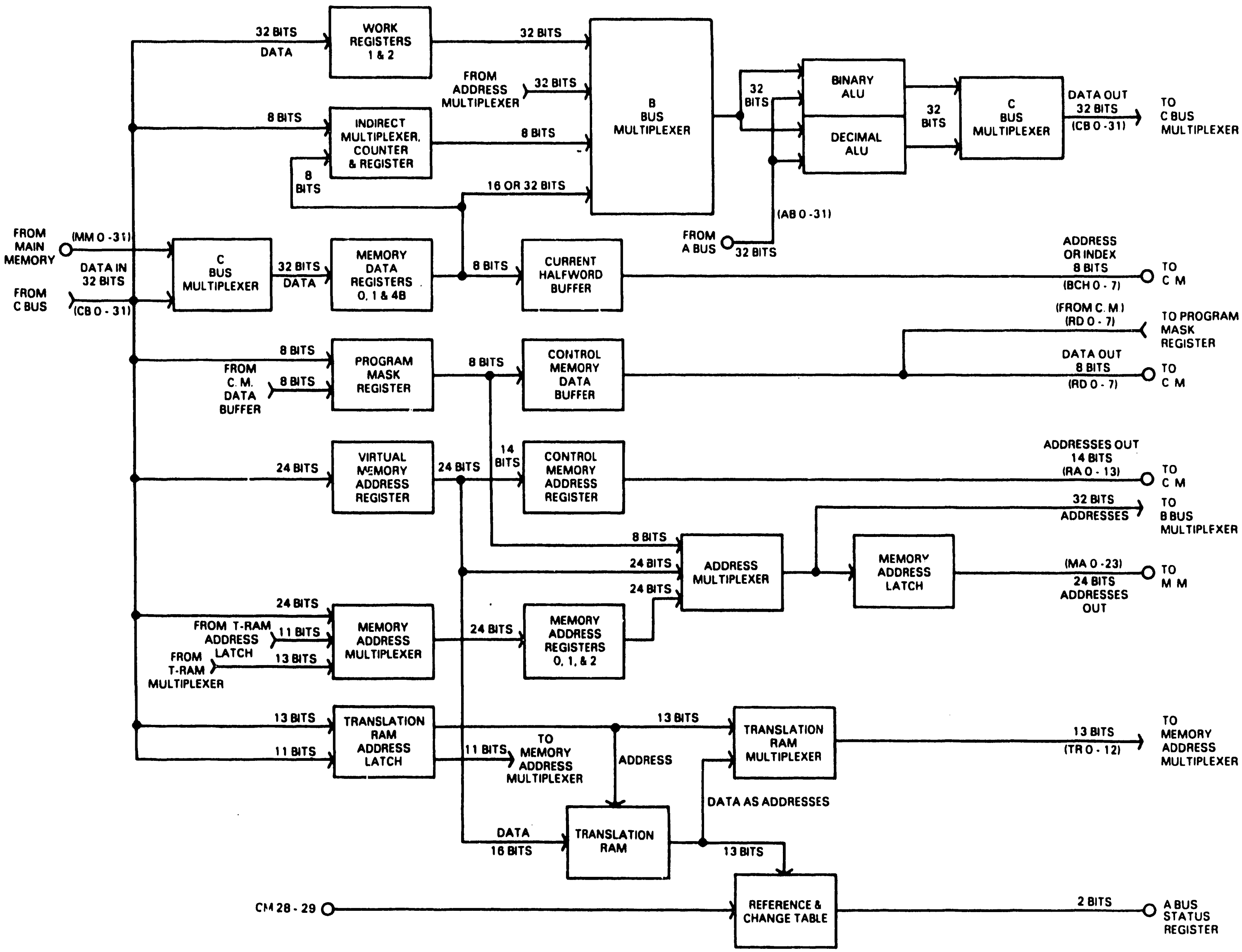


Figure 2-5. VS-85/85-H B Bus

The 8-bit Current Halfword Buffer (CHBF) accepts the high order byte from MDR0 or MDR1 as the CH (Current Halfword). The buffer is always enabled and outputs the data (an address or index for a Branch to Next macroinstruction) as BCH0-7 to the BRMX and Same Address Multiplexer on CM.

2.3.2.3 Work Registers, Indirect Counter, and Indirect Register

The input data to the 32-bit general Work Registers 1 and 2 (WK1 and WK2) is from the C Bus Multiplexer (CB0-31). Whether WK1 or WK2 is selected depends upon the decoding of process field C Bus destination operands. Access to the 32-bit word from WK1 or WK2 is controlled by process field B Bus operand selection and the output data is sent the BMX.

The 8-bit Indirect Register Multiplexer (IREG MUX) input comes from MDR0 or MDR1 via the Current Halfword Buffer as CH8-15, or from the C Bus as CB24-31. A Branch to Next or Branch to Next (Execute) macroinstruction selects the CH8-15 inputs for the Current Halfword. All other instructions select the CB24-31 inputs. The outputs go to the Indirect Register Counter.

The 8-bit binary Indirect Register Counter (IREG Counter) input data comes from the IREG Multiplexer. The counter is disabled during a Branch to Next or Branch to Next (Execute) instruction, or Indirect Register Load instruction, and will cause the outputs to equal the inputs. During a Move and Increment IREG instruction (move A bus operands or B Bus operands to C Bus) the counter is upcounted. A Move and Decrement IREG instruction will cause the counter to be down-counted. Outputs go to the Indirect Register and the A Bus Stack Addressing logic as IR0-7, and to the BMX as IR4-7.

The 8-bit Indirect Register (IREG) is a work register used for indirect Stack addressing. Input data comes from the IREG counter and output data goes to the BMX. The only control for the IREG is the process field B Bus IREG operand.

2.3.2.4 B Bus Multiplexer

The 32-bit B Bus Multiplexer (BMX) collects data from several sources, including WK1, WK2, IREG and IREG Counter, Address Multiplexer (MG0-31), MDR0-1, or MDR4-B. Output data, BB0-31, is used at the Binary Arithmetic Logic Unit (BALU) and the Decimal Arithmetic Logic Unit (DALU).

2.3.2.5 Binary Arithmetic Logic Unit, Decimal Arithmetic Logic Unit, and C Bus Multiplexer

The Binary ALU (BALU) consists of eight 4-bit high speed parallel ALUs. Each ALU has a complexity of 75 equivalent gates per chip. The eight chips are cascaded to allow 32 bits (one word) of data to be acted upon as a whole. Controlled by four function select inputs and a Mode control input, it can perform 16 possible logic operations or 16 different arithmetic operations. The Mode control input will determine whether all internal carries are inhibited and the device performs logic operations (Or, Nor, Exclusive Or, And, Nand, or Compare) on the individual bits, or whether the carries are enabled and the device performs arithmetic operations (Add, Subtract, Compare, or Double) on the two 4-bit words. BALU operations, whether logical or arithmetic, are completed within one system clock period.

The Decimal ALU (DALU) consists of eight 4-bit high speed binary coded decimal (BCD) arithmetic units. The eight chips are cascaded to allow 32 bits (one word) to be acted upon as a whole. Depending on the state of the Add/Subtract control, the unit produces the BCD sum or difference of two decimal numbers. A decimal addition is performed by adding the A Bus to the B Bus and placing the results on the C Bus. A decimal subtract operation (B minus A) is performed by internally adding the 9's complement of the A Bus to the B Bus and placing the result on the C Bus. ALU operations are completed within one system clock period.

The 32-bit C Bus Multiplexer (CMX) receives data from either the DALU or the BALU for transmission on the C Bus as CB0-31. The DALU is selected for output during any of the four decimal instructions. Otherwise, the output will be from the BALU. C Bus data is used at the C Bus Main Memory Multiplexer, Program Mask Register, Work 1 and 2 Registers, Stack, Indirect Register Multiplexer, Virtual Memory Address Register, T-RAM Address Latch, and Memory Address Multiplexer.

2.3.2.6 Program Mask Register and Virtual Memory Address Register

The 8-bit Program Mask Register (PMR) is dedicated to part of the Linkword macro and is used with Linkword as a B Bus operand for ALU input. The C Bus (CB0-7) is used as input to the PMR when the PMR is accessed, along with the Virtual Memory Address Register (VMAR), during Move operations. Together PMR and VMAR compose the Linkword. CB0-7 is also used as data input to the PMR during a Write Control Memory operation. The CM RAM address (CB18-31) is set into the VMAR and then forwarded to the Control Memory Address Buffer to become RA0-13. CB0-7 is moved from the PMR as data to be written and is sent on to CM as RD0-7. PMR bits 0 and 1 are used with Condition Code instructions.

The 24-bit VMAR is dedicated to Virtual Addresses of current halfwords in the macroinstruction stream. Input to the VMAR comes from the C Bus as CB8-31. Used as a B Bus operand source for ALU input, VMAR outputs go to the Address Multiplexer for transfer to the B Bus and ALUs.

As a C Bus operand destination register, VMAR outputs are sent to the T-RAM as a Page Frame number entry or to the Control Memory Address Buffer as addresses. These addresses, in conjunction with data from the PMR, will be used when writing CM.

VMAR can be incremented by two to allow the next halfword to become current. There are several microinstructions which use the current halfword as an ALU input or as the input for a multiway branch. VMAR incremented by two occurs during a Branch to Next or Branch to Next (Execute) microinstruction.

2.3.2.7 Control Memory Address Buffer and Control Memory Data Buffer

The 14-bit Control Memory Address Buffer (RABF) will gate 14 bits of address (VMAR10-19 and CB28-31) from the VMAR to the CM as RA0-13 for a Write Control Memory instruction.

The one-byte Control Memory Data Buffer (RDBF) transfers data as RD0-7 between the PMR and the CM. The buffer is enabled during a Write Control Memory instruction.

2.3.2.8 Memory Operation Overviews, Memory Address Multiplexer, and Memory Address Registers 0, 1, and 2

2.3.2.8.1 General Memory Operations Overview

The CP can initiate only one memory read or write operation for each microinstruction. CP memory read or write requests rely on a physical address contained in a Memory Address Register (MAR) and data contained in a Memory Data Register (MDR). There are three MARs (MAR1, MAR2, and MAR3) and five MDRs (MDR0, MDR1, MDR2, MDR3, and MDR4). The memory operation field (MOP) of the microinstruction will select a MAR and indicate the type of read/write operation, address translation operation, or address ripple operation. Translation, changing virtual memory addresses into physical memory addresses, and Ripple, incrementing or decrementing a MAR value, are mutually exclusive.

A Word Alignment feature is used with MAR2 doubleword writes and translation operations if the virtual addresses are not word aligned. There are three microtrap locations for address translation and three microtrap locations for word alignment. An address translation trap has priority over a word alignment trap. (Refer to table 2-1.)

2.3.2.8.2 Read and Write Overview

The read operation uses the selected MAR contents at the start of the microinstruction. The CP must wait for the data to be returned before resuming microinstruction execution. Error returns for read operations are handled by microtraps during the microinstruction. Buffered read memory support is provided for MAR0 and for MAR1 by having 2 MDRs associated with one MAR. The MDRs receive either the even or odd addressed word when a buffered read operation is performed. The write operation uses MAR2 and MDR4 contents at the start of the microinstruction. The CP can continue program execution without waiting for memory operation completion. Asynchronous error returns for write operations are handled through the External Condition Register on the System Bus Controller/MCII.

2.3.2.8.3 Translation Overview

When a translation operation changing virtual memory addresses into physical memory addresses is performed, no memory read or write operations are allowed. The translation is coded by specifying a No Op in the memory operation portion of the memory operation field and a translation operation in the translation/ripple field of the MOP. The Translation RAM, after translating the virtual address, supplies the physical addresses for the three MARs. The MAR select field indicates the destination MAR of the physical address. MAR0, MAR1, and MAR2 support read translations while MAR2 supports read and write translations.

2.3.2.8.4 Ripple Overview

The MAR ripple operation involves a small increment or decrement of the MAR value. All three MARs support ripple operations. The ripple operation is specified by the Translation/Ripple portion (CM27-29) of the memory operation field format. The ripple operation for the MARs only affects the low order 12 bits of the MAR value and any carry or borrow beyond 12 bits is lost. If a memory read or write operation is also requested, then the ripple occurs after the memory operation has been initiated. A ripple operation always involves a corresponding Page bit to indicate that the MAR address has or has not crossed a 2K memory page boundary. If the 2K boundary has been crossed, a new address must be supplied.

The 32-bit Memory Address Multiplexer (MAMX) supplies data to the MARs from either the Translation RAM and the Translation Address Latch (as a Page Frame number and a location within the page) for Translation operations, or from the C Bus (CB0-31) for read or write operations.

2.3.2.8.5 Memory Address Registers 0, 1, and 2

The CP uses the three Memory Address Registers (MARs) with the five Memory Data Registers (MDRs), grouped as follows:

The 24-bit MAR0, with MDR0 and MDR1, is dedicated to accessing halfwords from the macroinstruction stream. The buffered MDRs provide overlapped macroinstruction fetching. Only three memory operations affect MAR0. A Read Translation operation with halfword alignment check is used when a new physical address is required for current halfword access because a Branch micro causes a new virtual address to be used. The address is a Page Frame number and location within the page. A Buffered Read operation follows a Read Translation and uses that physical address now in MAR0 to point to the data in memory to be read into MDR0 or MDR1. After the operation has been initiated, a count of four will be added to the contents of MAR0. (MAR0 will be rippled plus four.)

A Word Conditional Read operation allows prefetching of the next word in the macroinstruction stream. The condition is that neither MDR0 or MDR1 is full. The word addressed by MAR0 will again be read into MDR0 or MDR1 and MAR0 will be rippled plus four.

The 32-bit MAR1, with MDR2 and MDR3, provides read only access for main memory operands. Several memory read operations, including byte, word, word conditional, and multiconditional reads, are supported by MAR1. A byte read will cause data to be placed in the low order byte position of MDR2 with the three high order byte positions of MDR2 set to zero. Data from a word read will also be placed in MDR2. A word conditional read places the word into MDR2 or MDR3 with the condition that the new MAR address be within the same 2K memory area (Page 1) as the initial MAR address. If the MAR address is not within the same 2K memory area, a Page boundary has been crossed and a new virtual address must be supplied. No read or ripple will be performed. A multiconditional read also places the word into MDR2 or MDR3, again depending on the 2K memory area plus the state of the two low order bits of MAR1. MAR1 supports plus one or four ripples, or minus one or four ripples, as indicated by the memory operation field, for conditional and multiconditional reads.

The 32-bit MAR2, with MDR4, is available for general, non-buffered read and write access of main memory. MAR2 supports byte, word, byte conditional, and word conditional reads as well as byte and word writes. All data is read into and written from MDR4. A byte read will cause the data to be placed in the low order byte position of MDR4 with the three high order byte positions of MDR4 set to zero. The byte and word conditional reads are the same as MAR1 except that the 2K memory area is Page 2.

If the MAR address is not within the same 2K memory area, a Page boundary has been crossed and a new virtual address must be supplied. No read or ripple will be performed. MAR2 supports plus one or four ripples, or minus one or four ripples, as indicated by the memory operation field for conditional reads. A byte write (Read Modified Write) uses the data in low order byte position of MDR4. For a word write operation, the internal counters of MAR2 are disabled. MAR2 then operates as a straight forward gate by allowing its outputs to follow its inputs when the register receives a clock pulse.

2.3.2.9 Address Multiplexer and Memory Address Latch

The 32-bit Address Multiplexer (ADMX) receives input from the Program Mask Register and Virtual Memory Address Multiplexer, or from one of the three MARs. ADMX input selection is based on the microinstruction process field B Bus operand for input from PRM and VMAR, and the MARselect portion of the memory operation field for inputs from the MARs. The ADMX output is sent to the BMX for input to the ALUs, or to the Memory Address Latch as main memory addresses.

The 24-bit Memory Address Latch (MAL) consists of three eight bit latches with the outputs always enabled. Input is from the ADMX and output is transferred to the Cache/MCI as MM addresses, MA0-23.

2.3.2.10 Translation RAM Address Latch, Translation RAM, Reference/ Change Table, and Translation RAM Multiplexer

The input to the 24-bit Translation RAM Address Latch (TAL) is 13 bits (CB8-20) of the virtual address from the C Bus (C Bus microcode operation output), of which 12 bits are used to address a Page Frame in the Translation RAM. The TAL also forwards the 11 low order bits (CB21-31) of the virtual address to the Memory Address Multiplexer as the location within the page. The TAL outputs will be available for the Translation instruction group and two microinstructions (MVN and MVX) from the Move instruction group.

2.3.2.10.1 Translation RAM

The physical main memory storage capacity of the VS-85 is currently limited to 4 MB. Because the VS-85/85-H uses virtual memory techniques, MM can be made to appear much larger. The translation of virtual (disk) addresses to physical (main memory) addresses is performed by the CP. Three elements recognized by the Operating System during translations are segments, pages, and page frames.

A segment is a block of contiguous disk storage. There are three types of segments. The first type (Segment 0) is 512 KB containing supervisory routines and data for the Operation System. The second type (Segment 1) is 1 MB for each user program. The third type (Segment 2) is 4K to 1 MB (in 4K increments) for each user's data. A page is 2K of contiguous bytes of disk storage space within the user program or data segments, and a page frame is a main memory area exactly large enough to contain a disk page.

Since the system is intended to operate in a multitask, multiuser environment, it is necessary to have a mapping mechanism to direct the CP to the pages of the tasks being executed. The CP uses an 4K x 16-bit **(8K x 16-bit in the VS-85-H)** local Translation RAM (T-RAM) to perform the mapping (translation) of a 24-bit virtual memory address into its current corresponding 24-bit physical main memory address. Each T-RAM entry (a C Bus operand destination from the Virtual Memory Address Register) contains a 13-bit page frame number, a fault bit, and read and write protect bits. These correspond to a particular page within the total virtual address space. The Translation operation addresses the T-RAM entry using the 12 bits (TRA0-11), or 4K (in the VS-85-H, 13 bits (TRA0-12), or 8K), of the virtual address (C Bus microcode operation output) from the Translation RAM Address Latch.

Reading and writing the RAM is controlled by the Load T-RAM instruction. The 13-bit page frame number read from the T-RAM is concatenated with the low order 11 bits of the virtual address (location within the page) from the Translation Address Latch at the Memory Address multiplexer to create the 24-bit physical main memory address. If the operation traps on an invalid virtual address (fault), the microinstruction can be restarted if the T-RAM entry can be updated; otherwise, a page fault interrupt is generated. A trap will also be taken if the page is protected against being read or overwritten.

The T-RAM can be monitored to provide rapid clearing of T-RAM entries for a user whose time slice has expired, while allowing entries for other users to remain. Monitoring occurs by segment and is based on a flag bit associated with the segment. The current users entries in the T-RAM are faulted when a different virtual address space is to be accessed. The CP will store these virtual addresses in the second half of the CP Stack when servicing a T-RAM fault. The CP microprogram maintains a counter of the monitored entries. The Stack is read one word at a time to get the virtual address for clearing each T-RAM entry when that users time slice has expired.

The CP maintains a table for each page frame entry in the T-RAM to record a reference bit, indicating a page was recently used, and a change bit indicating the contents of page were modified. An 8K by 2-bit Reference and Change Table (RCT) RAM is responsible for maintaining the table. The reference bits tell the operating system what pages have not been used recently and could be written over with new pages. The change bit allows the operating system to determine what pages have been modified and should be written back onto disk to make room in memory for new pages. These two R and C bits (M2BI and M2HI) are updated to reflect the page frame status during each MOP translation process. Addressing the RCT is done by using the Page Frame Number from the T-RAM entry. An entry can be cleared or inspected by microinstructions.

The 13-bit Translation RAM Multiplexer (TRMUX) normally passes the selected T-RAM entry to the Memory Address Multiplexer. However, if the selected entry should be faulted indicating that it is invalid, then the virtual address from the T-RAM Address Latch used for addressing the T-RAM is routed directly to the Memory Address Multiplexer by the TRMUX.

2.4 MAIN MEMORY

With the MCI/MCII combination, the VS-85/85-H Main Memory (figures 2-6 and 2-7) can contain one to two 210-7803 (1 MB) or two 210-8303 (2 MB) MM boards. Memory can range in size from 1 MB to a maximum of 4 MB, with memory size increasing in 1- or 2-MB increments. If a Cache/SBC combination is installed, a minimum of two 210-7803 boards are required to satisfy the 64-bit word requirement.

The 7803 board contains 256K 32-bit half words and is logically divided into four rows of 64k 32-bit half words for a total of 1 Megabytes. The 8203 board contains 512K 32-bit half words and is logically divided into eight rows of 64k 32-bit half words for a total of 2 MB. Both boards use a 64 Kword x 1-bit Dynamic RAM chip.

2.4.1 CONTROL SIGNALS

Main memory control signals are generated on the Cache/MCI board. (Refer to paragraph 2.5.3, Main Memory Control.) They are RAS (Row Address Strobe), CAS (Column Address Strobe), CEN (Column Enable), R/W (Read/Write), two Write Pulses (WP0-31 and WP32-63 for the Cache and WP for the MCI), Module Select #, and REF (Refresh). The MM cycle runs synchronously with the SBC/MCII cycle.

2.4.2 MEMORY WRITE AND READ

CP or BA data transfer to and from the memory is controlled by the SBC/-MCII. The basic memory data word is 32 bits with a 7 bit ECC (Error Correction Code) field. Write operations allow any board to be accessed separately for word writes, or in pairs for doubleword writes. The SBC/MCII can align units of 1, 2, 4, or, for the SBC, 8 bytes, but only words or doublewords can be written. For the SBC, all read operations cause a doubleword (8 bytes or 64 bits) to be accessed with the first board containing the even addressed word, and the second board containing the odd addressed word. Hence, the necessity of a minimum configuration of two boards for the Cache option.

For a memory write operation, the even word of data (MMWD0-31) and parity (WPH0-6), and/or the odd word of data (MMWD32-63) and parity (WPL0-6) from the SBC will be written into the RAM by the Write Pulse as long as R/W (Read/-Write), CAS (Column Address Strobe), and RAS (Row Address Strobe) are active. For the MCII, only the even word of data (MMWD0-31) and parity (WP0-6) are used. Row and column addresses are available coincident with RAS and CAS. WP is generated on the Cache for the odd and/or even word boards, and on the MCI for the even word. This allows a single word write without having to encode an address to distinguish between boards in a pair. When the Check ECC (Error Correction Code) feature is active, all data RAMs will be disabled and writing will only be allowed into the parity RAMs.

For a memory read operation, the even word of data (MMRD0-31) and parity (RPH0-6), and the odd word of data (MMRD32-63) and parity (RPL0-6) will be read from the RAM and transferred to the SBC, when the Column Address Strobe is active, as long as Read/Write remains inactive. Again, row and column addresses are available coincident with RAS and CAS.

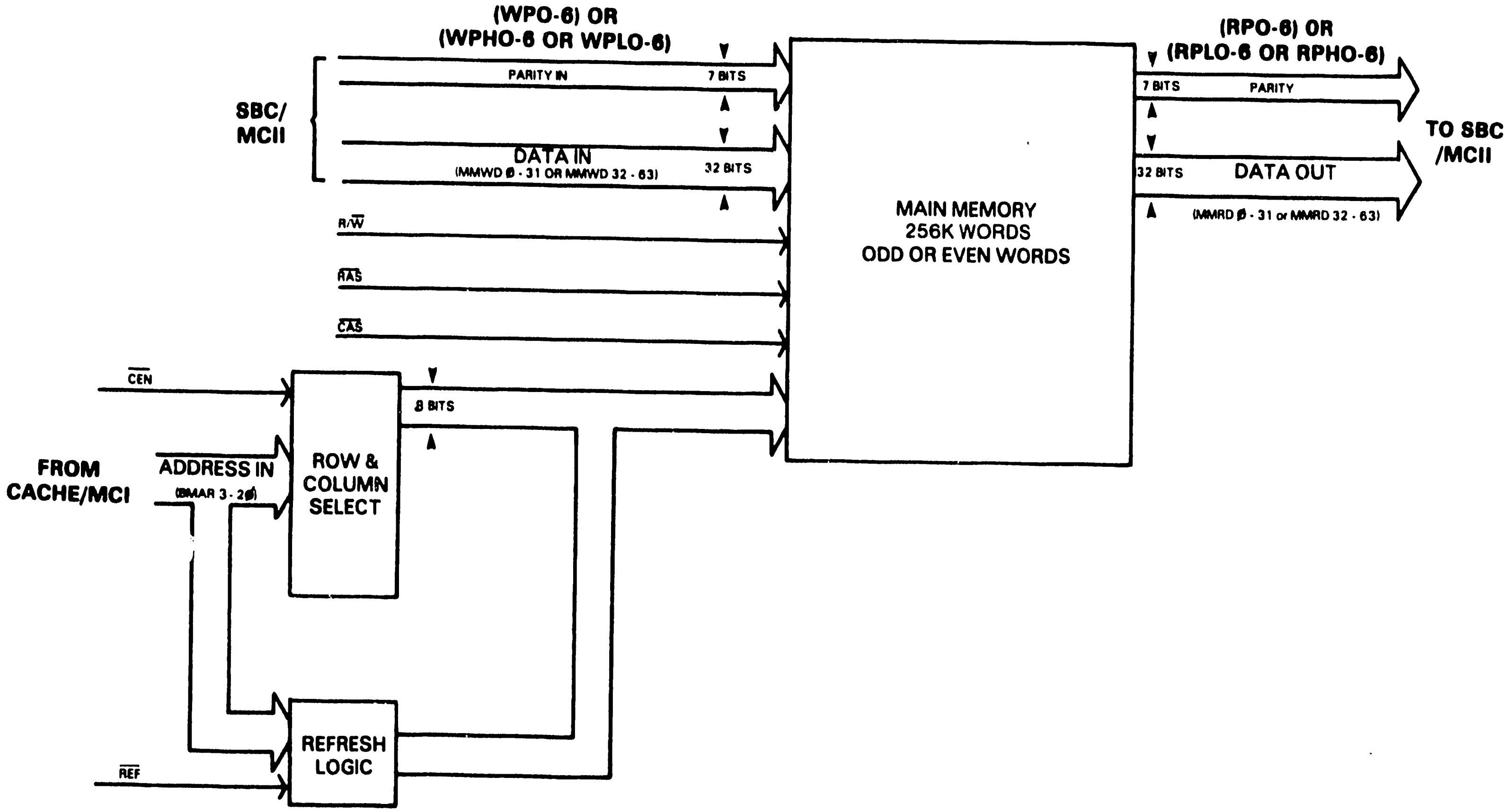


Figure 2-6. VS-85/85-H 1 Megabyte Main Memory

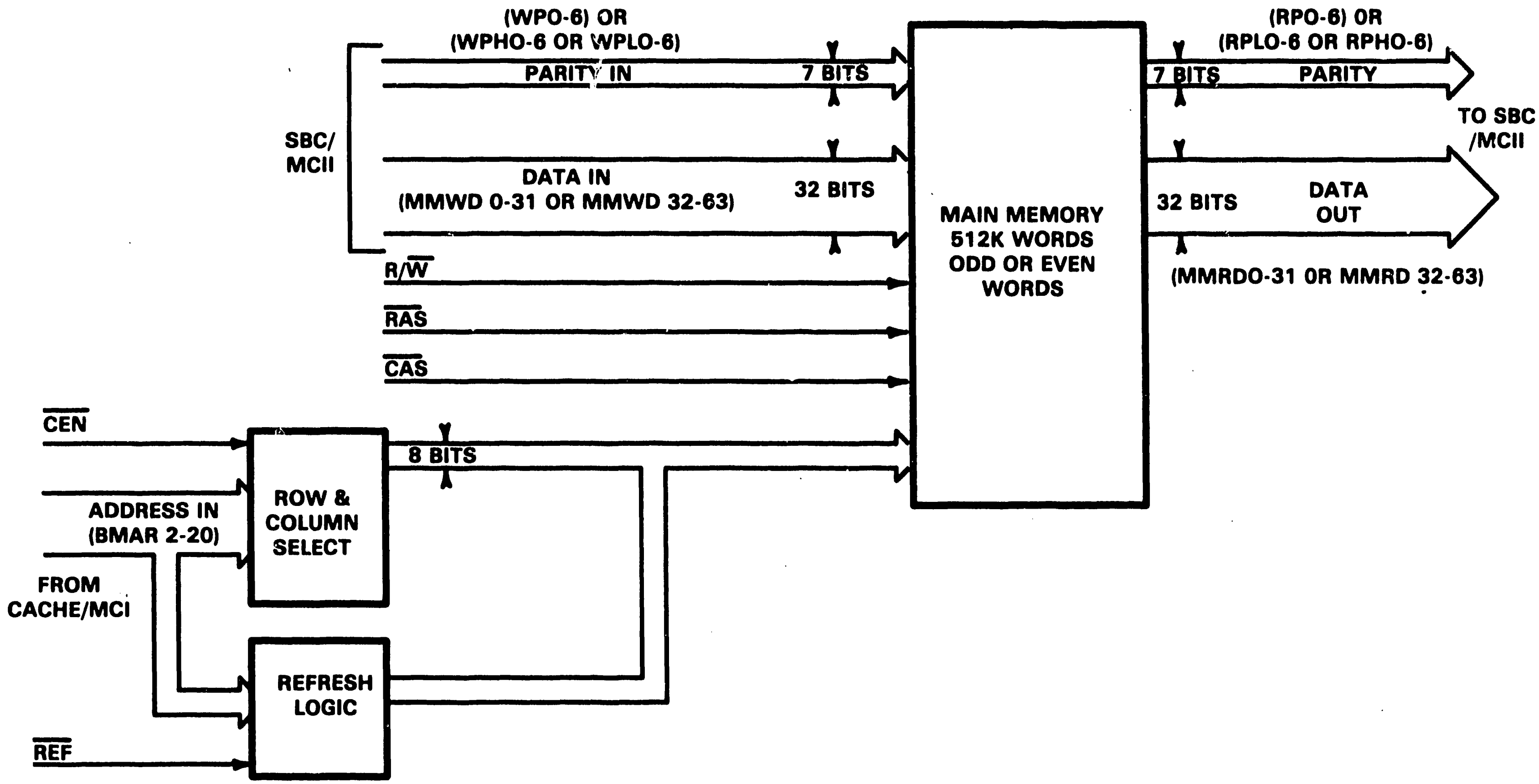


Figure 2-7. VS-85/85-H 2 Megabyte Main Memory

For the MCII, only the even word of data (MMRD0-31) and parity (RP0-6) will be read from memory.

2.4.3 ADDRESSING

Memory addresses are supplied by the CP or the BA. Of the 24 address bits available (BMAR0-23), 18 bits (BMAR3-20) are used at the 210-7803 memory board. (Refer to table 2-3.) BMAR3-4 are used to decode one of four 64K word rows for a total of 1 MB.

For the 210-8203 memory board, 19 bits (BMAR2-20) are used . (Refer to table 2-4.) BMAR2-4 are used to decode one of eight 64 Kword rows for a total of 2 MB.

For either board, sixteen address bits (BMAR5-20) are required to decode one of the 64k memory locations. The eight row addresses (BMAR6-13) are latched into the RAM's internal row address decoder by the Row Address Strobe. The eight column addresses (BMAR5 and BMAR14-20) are selected by CEN (Column Enable). These addresses are then latched into the RAM's internal column address decoder by the Column Address Strobe. BMAR21-23 are not used because the lowest accessible addressed unit is eight bytes (two words).

Table 2-3. VS-85/85-H Main Memory Addresses (1 MB)

BMAR BIT	FUNCTION
BMAR 0	NOT USED
BMAR 1	NOT USED
BMAR 2	NOT USED
BMAR 3	64K ROW SELECT
BMAR 4	64K ROW SELECT
BMAR 5	COLUMN ADDRESS
BMAR 6	ROW ADDRESS
BMAR 7	ROW ADDRESS
BMAR 8	ROW ADDRESS
BMAR 9	ROW ADDRESS
BMAR 10	ROW ADDRESS
BMAR 11	ROW ADDRESS
BMAR 12	ROW ADDRESS
BMAR 13	ROW ADDRESS
BMAR 14	COLUMN ADDRESS
BMAR 15	COLUMN ADDRESS
BMAR 16	COLUMN ADDRESS
BMAR 17	COLUMN ADDRESS
BMAR 18	COLUMN ADDRESS
BMAR 19	COLUMN ADDRESS
BMAR 20	COLUMN ADDRESS
BMAR 21	NOT USED
BMAR 22	NOT USED
BMAR 23	NOT USED

Table 2-4. VS-85/85-H Main Memory Addresses (2 MB)

BMAR BIT	FUNCTION
BMAR 0	NOT USED
BMAR 1	NOT USED
BMAR 2	64K ROW SELECT
BMAR 3	64K ROW SELECT
BMAR 4	64K ROW SELECT
BMAR 5	COLUMN ADDRESS
BMAR 6	ROW ADDRESS
BMAR 7	ROW ADDRESS
BMAR 8	ROW ADDRESS
BMAR 9	ROW ADDRESS
BMAR 10	ROW ADDRESS
BMAR 11	ROW ADDRESS
BMAR 12	ROW ADDRESS
BMAR 13	ROW ADDRESS
BMAR 14	COLUMN ADDRESS
BMAR 15	COLUMN ADDRESS
BMAR 16	COLUMN ADDRESS
BMAR 17	COLUMN ADDRESS
BMAR 18	COLUMN ADDRESS
BMAR 19	COLUMN ADDRESS
BMAR 20	COLUMN ADDRESS
BMAR 21	NOT USED
BMAR 22	NOT USED
BMAR 23	NOT USED

2.4.4 REFRESH

Because a dynamic RAM will not store data indefinitely, the data must be written back at least once every two milliseconds. Rewriting the RAM is done internally and is called "refresh". The VS-85/85-H will refresh every 15 microseconds. This operation has priority over all other memory operations.

When a refresh cycle (REF) is initiated, RAS (Row Address Strobe) will be enabled for all RAMs, as they require refresh with only RAS cycles. Row refresh addresses, BMAR6-13, are supplied by the Cache/MCI. All CAS inputs will be disabled by the refresh. Normal memory operations also accomplish refresh.

2.5 MEMORY CONTROLLER I

The Memory Controller I (MCI) (figure 2-8) contains the same basic memory control and data passing services as the Cache. There is no 32 KB of RAM on the MCI.

2.5.1 MAIN MEMORY ADDRESSES FROM BA AND CP

Both the CP and the BA 24-bit MM addresses, for their respective MM operations, pass through the MCI; CP addresses (MA0-23) through the CP Memory Address Latch and BA addresses (BA0-23)through the BA Address latch. The addresses are sent to the Main Memory Address Multiplexer and the memory operation in progress (CP or BA) will gate the correct set of addresses through to MM as BMAR0-20.

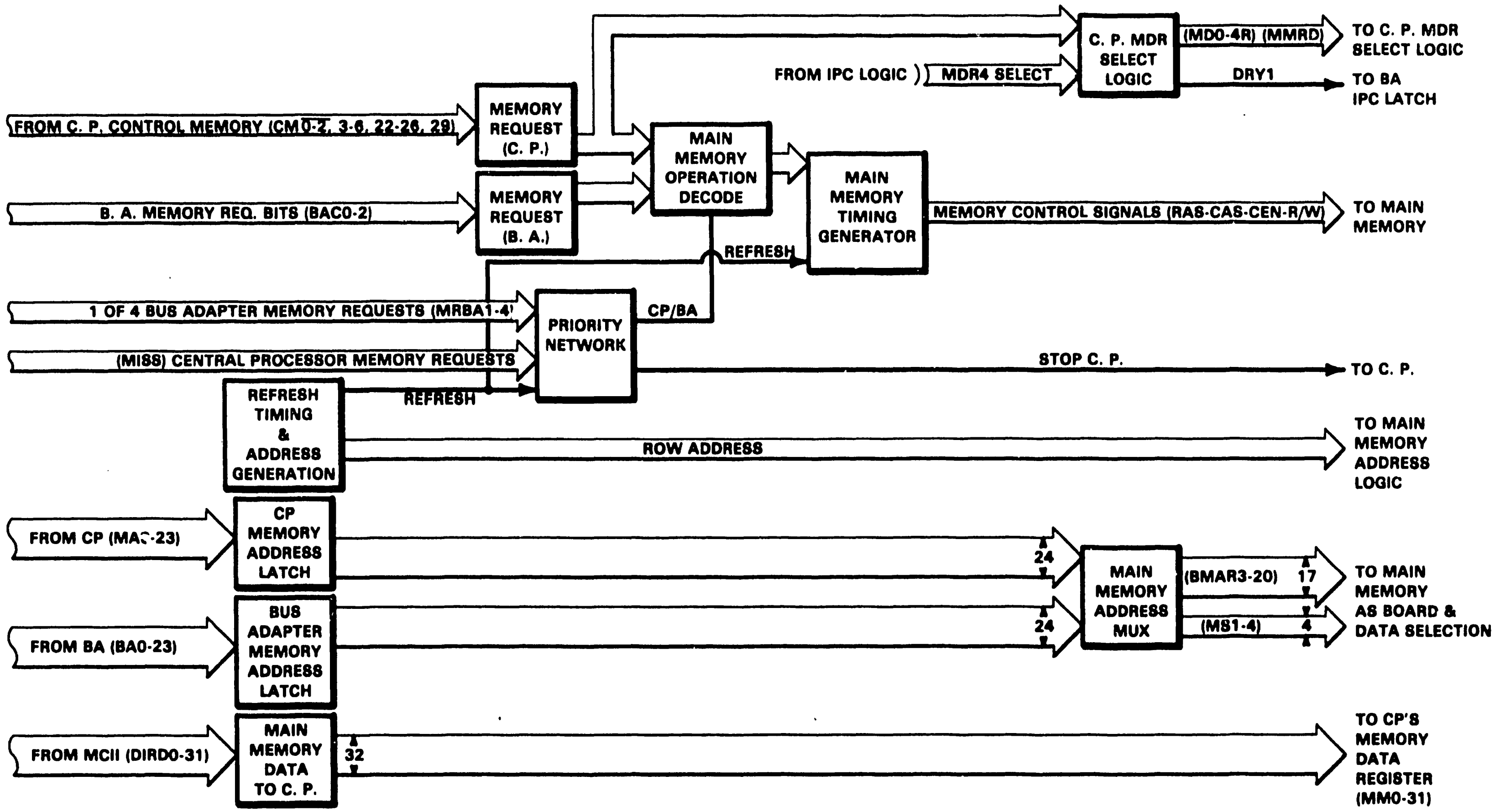


Figure 2-8. VS-85/85-H Memory Controller I

2.5.2 MAIN MEMORY DATA DIRECT TO CP

Data from MM to the CP also passes through the MCI board on the way to the CP. The data word, DIRD0-31, is directed from the MCII. The word can also be IPC data from the BA to the CP.

2.5.3 MAIN MEMORY CONTROL

The Main Memory Control logic on the MCI board is the same as on the Cache board. Refer to paragraph 2.6.8.

2.5.4 INTERPROCESSOR COMMUNICATIONS CONTROL

The Interprocessor Communications Control logic (figure 2-11) on the MCI board is the same as on the Cache board. Refer to paragraph 2.6.9.

2.6 CACHE MEMORY

The Cache RAM (figure 2-9) provides high speed data read access for the CP by acting as a buffer between the CP and MM. Its main function is to improve memory transfer rate by providing high speed access to needed data. Two other sections of the Cache board, although not part of the Cache Memory, are the MM control and the Interprocessor Communications (IPC) control logic. This logic is actually SBC logic, but is placed on the Cache board due to the physical limitations of the SBC board. MM refresh logic is also part of the memory control to provide refresh control and refresh row addresses to the MM.

A complete Cache cycle is 160 nanoseconds while a Cache read only cycle is 80 nanoseconds, compared with the 480 nanosecond cycle time for a MM doubleword read. The Cache is in synchronization with the memory control.

The Cache contains a subset of the same data found in MM and allows the CP to read this subset data, making it unnecessary for the CP to wait for data read from main memory. To accomplish this, the Cache has a write through strategy so when the CP writes to MM, via the SBC, the Cache entry is fully updated.

The effectiveness of the Cache is measured by the "hit" ratio, or how often the requested data is found in Cache. The hit ratio will increase as job execution proceeds because the job tends to reuse data it has already referenced. A "miss" indicates the requested data was not found in Cache. The CP then requests a doubleword read directly from main memory and that doubleword will be written to Cache to keep the Cache updated.

Because of timing constraints, the BA does not write to Cache Memory. When the BA modifies a data word which is also buffered in Cache, the Cache entry is invalidated because it is no longer current.

The Cache can be disabled and enabled by setting a bit (ECR8) in the External Condition Register (ECR) on the SBC. When the Cache is disabled, all CP read accesses are satisfied directly with a main memory doubleword read. When the Cache is enabled, it contains stale data and must be cleared, as it is upon system initialization.

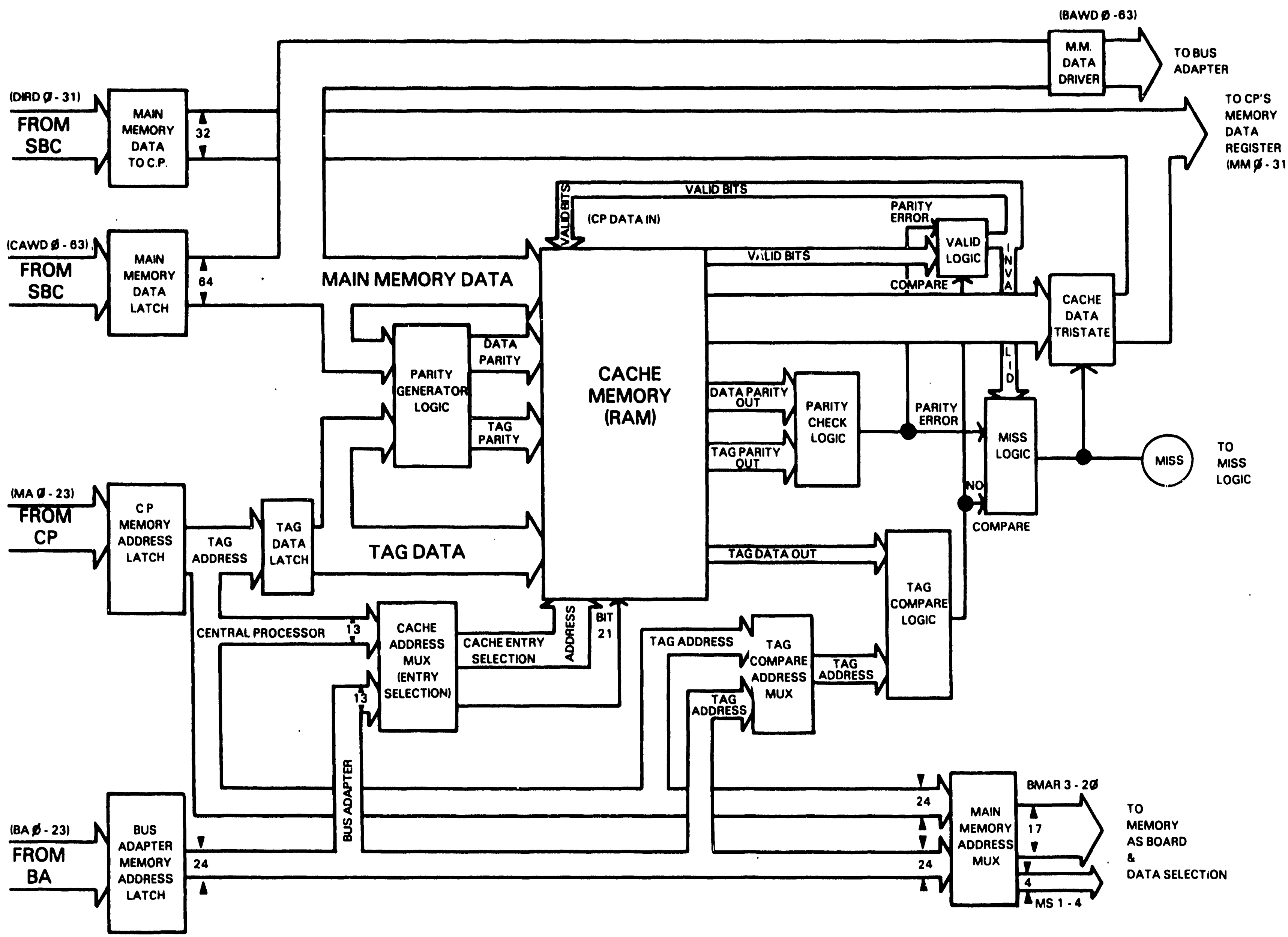


Figure 2-9. VS-85/85-H Cache Memory

Cache parity errors, which also cause a doubleword read, are recorded in the Bus Transaction Log on the SBC, but are otherwise invisible to the CP microprogram. The only indication of Cache parity errors is system access degradation.

2.6.1 CONFIGURATION

There are four thousand Cache Memory entry pairs (32 KB), and each pair contains an even word entry and an odd word entry. Each entry contains a 32-bit data word and a 9-bit "tag" field. The tag, which is used for address comparison, identifies the actual physical address of an entry. As each location in Cache can contain the corresponding MM location and every 32K increment of the location to the end of memory, the tag indicates which 32K increment is resident in Cache.

Of the 24 bits of physical address available, MA0-23 from the CP or BA0-23 from the BA, the 12 "middle" bits (MA9-20 or BA9-20) are used to select a Cache entry pair. One of the remaining 12 bits (MA21 or BA21) is used to select the even or odd Cache entry from the pair, and nine bits, (MA0-8) from the CP address, are used to compare tag fields of the selected entry. The low order 2 bits are ignored because the unit of access is one word.

2.6.2 DATA WRITTEN TO CACHE

Data to the Cache can be written in 1, 4, or 8-byte increments. There are two types of 8-byte writes. This data, appearing at the main memory Data Latch as CAWD0-63, is either one or two words of CP data, or is a doubleword of memory read data, corrected by the SBC. The CP data appears here to update the Cache, and at the SBC for a normal one or two word CP memory write. If the data is a doubleword of read data, then a Cache "miss" occurred and the CP was forced to do a memory read access.

The doubleword of read data can also be for the BA and it will not be written to Cache, but will be sent directly to the BA as CAWD0-63. This route of data to the BA is because of the convenience of locating hardware at this point.

The Cache will generate its own write pulses for 1, 4, or 8-byte writes, decoded from CP memory operation commands. When the Cache writes one byte it overwrites (replaces) one byte of a word already stored in Cache. The location of the byte to be written is software controlled by the tag identification and memory address bits MA21-23. MA21 controls the odd or even word selection while MA22-23 decide on the most or least significant halfword and byte of the word. A 4-byte (word) write is also controlled by the tag and MA21. The 8-byte (doubleword) CP write is accomplished by tag comparison only when the CP transfers two words.

The second type of 8-byte write happens when the tags did not compare, the Cache missed, and the CP was forced to read a doubleword from MM. This operation is done by default, when no CP write operation is decoded and

Control Memory bit 24 (MCM24) is on indicating that the CP requested a Cache read. The tag indicates the correct location to be written and MCM24 produces two write pulses to write the entire doubleword. Four bits of parity are generated and written to Cache for every word.

If the BA writes a doubleword to main memory, the memory address of the write is compared to the corresponding address and tag in Cache, and, if there is a match, the data in the Cache location is invalidated.

2.6.3 DATA READ FROM CACHE

The read instruction for the Cache is a normal memory read operation determined by the decoding of a Control Memory word. The word of data addressed in Cache for transfer to the CP is made available, through the Cache Tristate Drivers, to the CP's Memory Data Register on the MM0-31 lines. Nothing prevents MM from being read, but the data word returned (DIRD0-31) is effectively blocked from the CP at the Tristate Drivers.

2.6.4 MAIN MEMORY ADDRESSES FROM BA AND CP

Both the CP and the BA produce a 24-bit main memory address for their respective main memory operations. The CP addresses (MA0-23) pass through the CP Memory Address Latch while the BA addresses (BA0-23) pass through the BA Address latch. The addresses are sent to the Main Memory Address Multiplexer and the memory operation in progress (CP or BA) will gate the correct set of addresses through to main memory as BMAR1-20.

These addresses are also made available to the Cache Address Multiplexer for Cache entry pair selection in an attempt to locate the subset of data in Cache. Twelve of the "middle" address bits (MA9-20 or BA9-20) pass through the multiplexer for Cache entry selection. The BA addresses are only used to invalidate the cache entry, not to write a new entry.

2.6.5 TAG COMPARE (MISS) AND PARITY

The nine tag bits (TWD0-8) from the CP memory address are written into the Cache RAM, through the Tag Data Latch, at the same time that the Cache word is written. One bit of parity is also written for each tag entry. When the CP requests a Cache read of a selected entry, the tag bits of the current CP memory address are compared, through the Tag Compare Address Multiplexer and Compare Logic, to the tag bits of the selected Cache entry. If the tag comparison is not correct, the MISS signal is generated and sent to the Control Memory to stop the CP t and L clocks, if no BA is requesting a main memory cycle, as a main memory doubleword read must be initiated. The MISS is also recorded in the ECR of the SBC only for diagnostic purposes as the miss will be invisible to the microprogram.

As the tag was being compared, both the tag and data parity bits are being checked in the Parity Check logic. If a parity error occurs, MISS is generated regardless of the tag comparison results as bad parity indicates an unusable word. A MM doubleword read will be initiated.

2.6.6 VALID AND INVALID CACHE LOCATIONS

Because of timing constraints, the BA will not access any data in Cache. But, if the BA writes to MM and that particular MM location's data was in Cache, then the data in Cache will no longer be current or "valid". When the BA does a MM write, the Cache checks to see if that MM location also resides in Cache. If it does, a Cache location "valid" bit is written into the Cache RAM to indicate that the Cache entry is no longer valid. There is an even and odd valid bit for the even and odd cache word. If the CP requests a read of that cache location, the valid bit will cause a Cache MISS and a MM doubleword read will be initiated. The Cache word will be updated and will again become valid.

2.6.7 MAIN MEMORY DATA DIRECT TO CP

Data from MM to the CP, caused by a Cache miss and a doubleword read, passes through the Cache board on the way to the CP. The data word, DIRD0-31, is directed from the SBC at the same time that the doubleword from the SBC for the Cache update arrives at the Cache board. The word can also be IPC data from the BA to the CP. In that case, the word will not be used to update Cache. Any data from the Cache will not be permitted through the Cache Tristate Drivers.

2.6.8 MAIN MEMORY CONTROL

The Main Memory Control logic on the Cache board (figure 2-10) is actually an SBC function, but is located on the Cache board due to the physical limitations of the SBC board. Both the CP and the BA can request a variety of memory read and write operations, and both encode their own memory operations and requests. The BA, because it must support the IOP, is permitted a 16-bit (halfword) memory write that the CP is not allowed. The CP has the lowest memory priority and does not require a request line because the memory control defaults all unused memory requests to the CP. The BA has its own request line.

The Main Memory Operation Decoder decodes the CP memory operation from a Control Memory word when no BA memory requests are present, The Main Memory Operation Decoder decodes the BA operation from bits BAC0-2.

The Main Memory Timing Generator produces all the memory control signals discussed under Main Memory Control Signals, paragraph 2.4.1. The CP MDR Select Logic allows the selection of the appropriate CP Memory data Register for memory read commands. The STOP CP signal, halting the 't' time clocks of the CP, will be present if there was a Cache MISS because the data in the Cache was invalid and must be updated; if control was busy or doing a refresh and a CP write command was issued; or, if a BA memory request was in progress and a CP write command was issued.

Main memory refresh logic is also part of the memory control. It provides refresh control and row addresses (BMAR6-13) to the MM at 15 microsecond intervals. Refresh has priority over all other requesting processors.

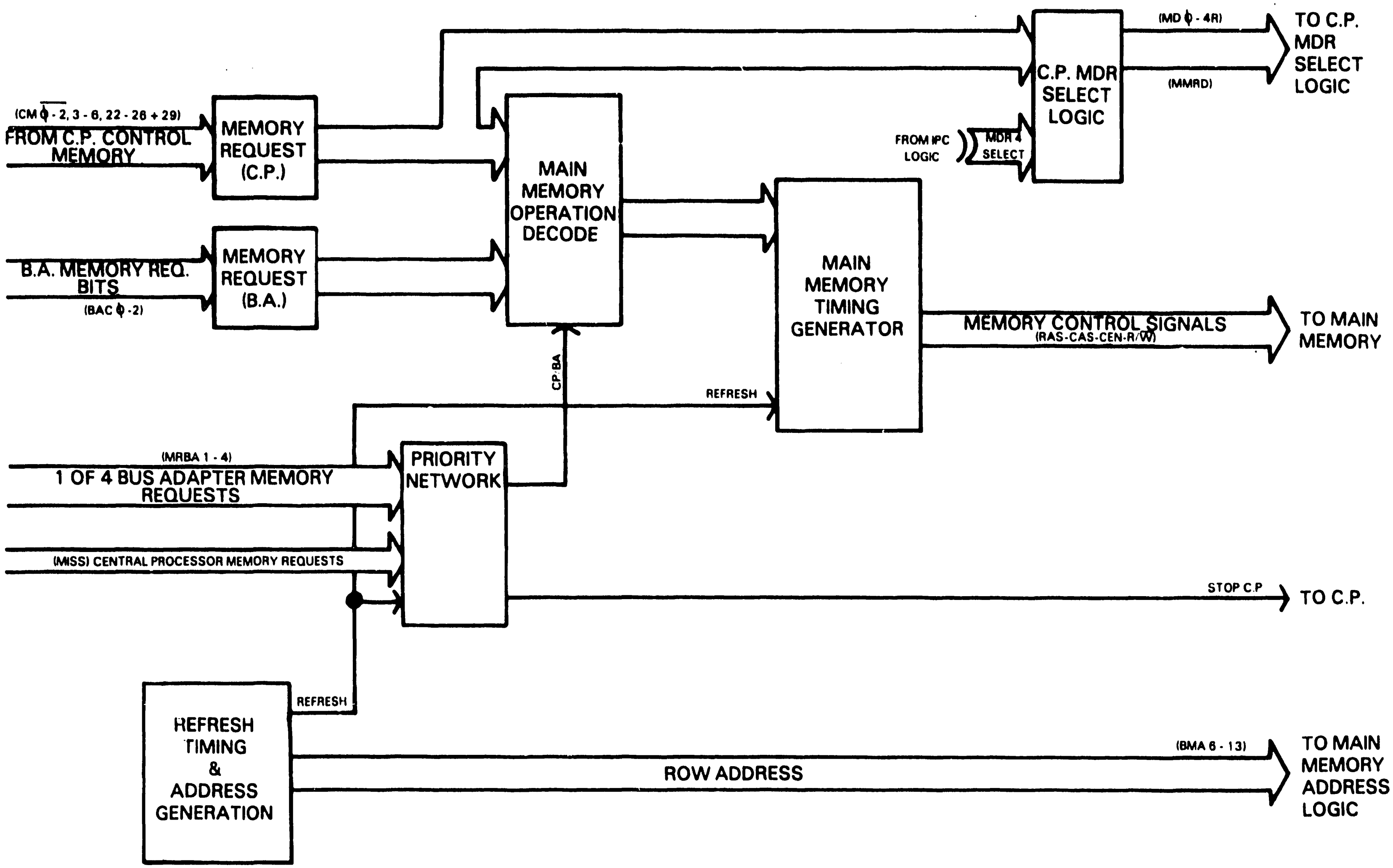


Figure 2-10. VS-85/85-H Memory Timing

2.6.9 INTERPROCESSOR COMMUNICATIONS CONTROL

Interprocessor Communications (IPC) control logic (figure 2-11) is also a SBC function but is located on the Cache board due to the physical limitations on the SBC. The logic is responsible for IPC message send and receipt control. The IPC feature has two basic functions. The first function allows two processors to communicate with each other without using MM facilities, and the second function allows the IOP to interrupt the CP because the CP will not accept asynchronous messages from the IOP. The CP, BA, and SBC are all considered processors.

The IPC data words are 32-bit messages created by a processor. There are two types of messages (dialogs); CP initialization of the BA, and I/O initialization and interrupts. The BA is used for buffering and routing the message.

The IPC receipt RAM stores IPC data bits 0-7 in the form of a message receipt control, a sending processor number, and a destination processor number. The RAM does not store the actual message. The Message Receipt Control Logic allows acceptance or rejection of any IPC message from any processor. The MDR Load Control alerts MDR#4, the IPC memory data register for the CP, of a pending message. The BA IPC Ready Control produces the Data Ready (DRY) signal to the BA. DRY will be used at the BA to gate the IPC data into the BA IPC Data Latch.

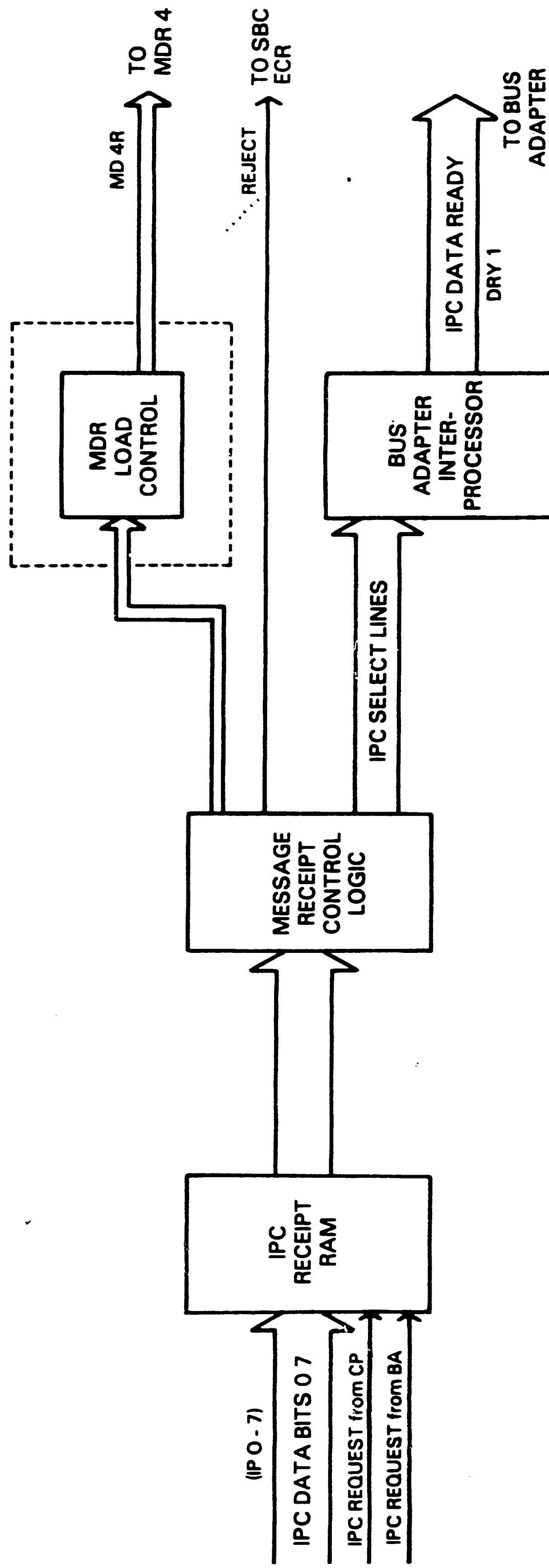


Figure 2-11. VS-85/85-H Interprocessor Communication

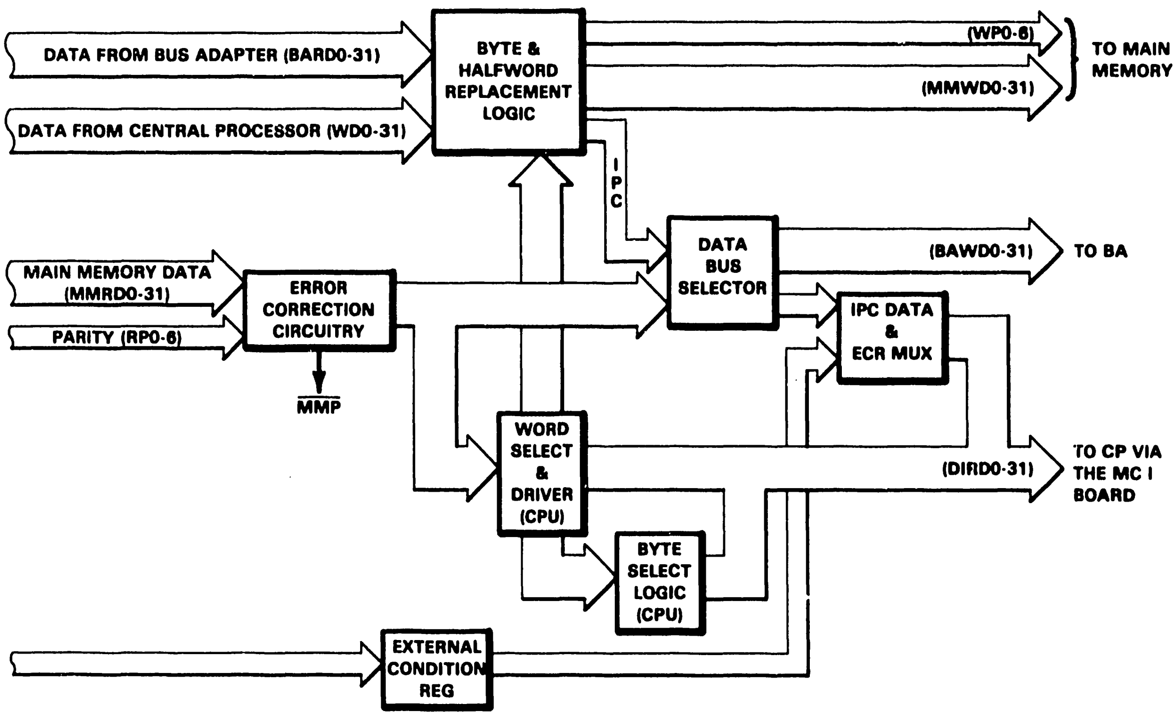


Figure 2-12. VS-85/85-H Memory Controller II

2.7 MEMORY CONTROLLER II

The Memory Controller II (MCII) (figure 2-12) contains basically the same logic functions as the SBC, including; Error Correction, Byte and Halfword Replacement, Word and Byte Select, and the External Condition Register.

The differences between the MCII and the SBC concern the 64-bit data bus. The MCII will send only 32 bits of data (BAWD0-31) to the B.A. and 32 bits of data (MMWD0-31) to the Main Memory; whereas the SBC sends 64 bits (CAWD0-63) to the Cache and the BA, and 64 bits (MMWD0-31 and MMWD31-63) to the MM.

Refer to paragraph 2.8 for the SBC logic functions.

2.8 SYSTEM BUS CONTROLLER

The System Bus Controller (SBC) (figure 2-13) provides a 64-bit data path between the Cache Memory, main memory, and the BA, and acts as a data "traffic cop". It directs a doubleword of data read from MM to the Cache Memory, or to the BA with alignment of any one of four single bytes of one word for the CP; directs and aligns units of 1, 2, 4, or 8 bytes of data to be written to memory from the CP or BA; and directs Interprocessor Communications (IPC) data between the CP and BA.

The SBC is responsible for correcting a single bit memory error for each 32-bit word of the doubleword that is read, notifying the Control Memory or BA if multibit read errors occur, and generating parity for a main memory write. It logs parity errors in the Bus Transaction Log (BTL), and controls and records "external" events using the External Condition Register (ECR).

2.8.1 DATA ERROR CORRECTION

Both the CP and the BA are responsible for generating their own individual memory requests. When a memory read operation is initiated, a doubleword will be transferred to the SBC from memory and the SBC will attempt to correct a single bit error for each 32-bit word of the doubleword. This is done by circulating the doubleword (MMRD0-63) and parity bits (RPH/L0-6) through Error Correction Code (ECC) circuitry. If a bad bit is detected by data and parity bit comparison, it will be corrected by an inversion process.

If an uncorrectable multiple bit error is detected, a Main Memory Parity Error condition will notify the Bus Adapter of the error during a BA operation, or set a trap (MMPT) in Control Memory for a CP read operation. If a CP Read Modify Write (1-byte) is in progress, the error indication will set a bit in the ECR to notify the CP and prevent the memory control portion of the SBC (located on the Cache) from generating Write Pulse.

As a diagnostic feature, the ECC can be disabled by setting a bit (ECR5) in the ECR. If the bit is reset, the SBC reports an error to the CP only if a multiple bit error is detected. Single bit errors are corrected with no indication given to the CP. If the bit is set, then the SBC reports both single and multiple bit errors to the CP as they occur.

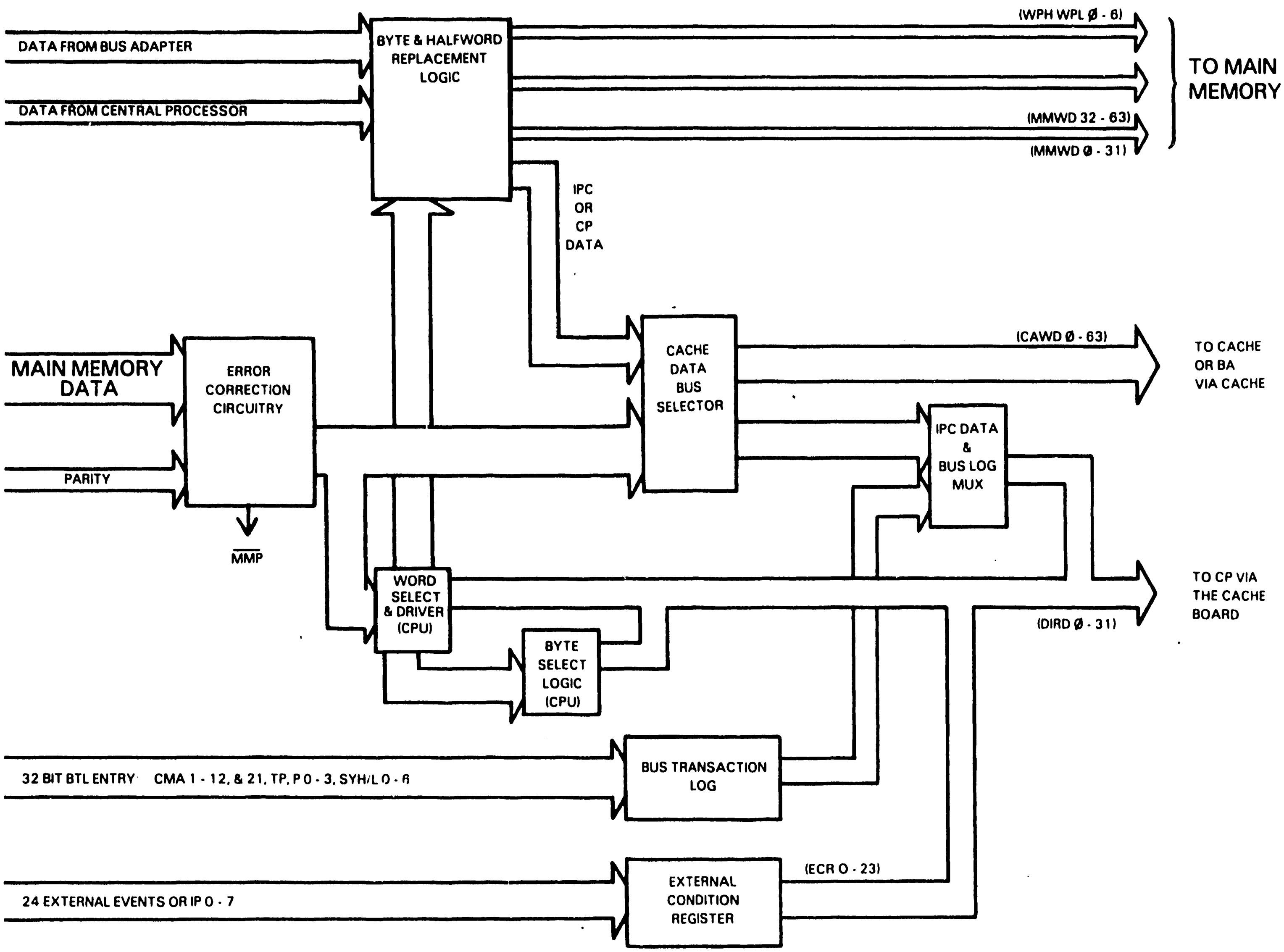


Figure 2-13. VS-85/85-H System Bus Controller

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2.8.2 READ DATA PATH

Data that has been processed by the ECC must be directed to the CP and the Cache, or to the BA. The CP requested a doubleword read because the Cache did not contain the current data. The CP requires one word of the doubleword, but the entire doubleword will be used to update the Cache. A BA request for a doubleword read will deliver the full doubleword of data to the BA.

As the CP needs only one word of the doubleword of corrected data, a decision must be made as to which word the CP will receive. This decision is made at the Word Selector and is software controlled by Memory Address bit 21 (MA21) which was available during the read instruction. If MA21 is reset, the even word of the doubleword will be selected and if MA21 is set, the odd word will be chosen. The selected word can also be used during certain read modify memory write operations.

Following the word selection, an opportunity exists to rotate, or "swap" any one byte of the selected word into the low order byte position. The Byte Selector conveniently manipulates the byte here, otherwise the destination register of the data word (CP Memory Data Register #2) would have to be searched for the selected byte. This feature is software controlled by Memory Address bits 22 and 23 (MA22-23), which are used for selecting bytes and halfwords. Following the word select (and byte "swap", if requested), the word is sent through the IPC Data and Bus Log Multiplexer to the Cache board, as DIRD0-31, for transfer to the CP.

At the same time the CP word is being selected, the doubleword is being transferred to update the Cache. The doubleword will pass through the Cache Data Bus Selector, which can only distinguish between the doubleword or IPC data (or CP data that will update the Cache on a CP write). The SBC does not know the destination of the doubleword, CAWD0-63. It can be for either the Cache or the BA. This decision is controlled by logic on the Cache board.

A BA read request will send the corrected doubleword directly to the Cache Data Bus Selector. Again, the SBC does not know or decide the destination of the doubleword.

2.8.3 DATA TO MAIN MEMORY

Data to be written to main memory is from either the CP or the BA, or it is corrected data, via the Word Selector, to be written back to memory as a replacement byte or halfword. The SBC will align the data in 1, 2, 4, or 8-byte increments, and write a word or doubleword to memory with correct parity. The word of data from the CP will also be made available to the Cache because the Cache must be updated when main memory is written. Because of timing constraints, the BA does not write to Cache Memory. Interprocessor Communications (IPC) data between the CP and BA will also be present, but will not be written to memory.

A CP write memory request allows one word of CP data to be admitted to the Byte and Halfword Replacement logic. It is up to the Byte and Halfword logic to decide on a 1-byte replacement, using read data from the CP Word Select logic, for a Read Modified Write operation, or allow an unmodified CP word write. This is also software controlled by Memory Address (MA) bits 22 and 23.

Another decision here is to permit a CP word or doubleword write. If a single word is to be written, the data will be available to memory as an even word (MMWD0-31) and an odd word (MMWD31-63). The memory control, by decoding the write instruction, will generate the appropriate even or odd word Write Pulse. For a doubleword write, the first word will be latched in the SBC's main memory output drivers while the CP transfers a second word. The memory control will produce both an even and odd word Write Pulse.

As the word(s) are prepared for memory, they will also be made available to the Cache Data Bus Selector to allow updating of the Cache Memory.

A BA write memory operation is similar to the CP write operation. The BA is allowed the normal byte replacement, and also a halfword replacement. The halfword is necessary because the IOP is a halfword device. The halfword or byte will be corrected memory data from the Word Selector and will be aligned by MA22-23.

The BA is also permitted a word or doubleword write. The complete BA doubleword is available to memory as MMWD0-63 and no second data transfer is needed. The memory control will again generate even and/or odd word Write Pulse(s). The word(s) will NOT be made available to the Cache Memory.

2.8.4 INTERPROCESSOR COMMUNICATIONS

Interprocessor Communications are used for generalized message passing and interrupt service between all processors (CP, BA, and SBC). Thirty two bit messages are transferred directly between processors without using main memory facilities. IPC transmission control is generated on the SBC portion of the Cache board.

If no write operations are in progress, the data word appearing at the Byte and Halfword Replacement logic will be Interprocessor Communications data, transmitted on the normal data paths, from the CP or the BA. IPC data is left untouched and is sent to the Cache Data Bus Selector. The Cache Data Bus Selector will select the IPC data word originating at the BA and transfer it through the IPC Data and Bus Log Multiplexer, as DIRD0-31, to the CP via the Cache board.

An IPC data word from the CP for the BA will also pass through the Cache Data Bus Selector, but will be directed to the Cache board as CAWD31-63. Logic on the Cache board will determine that this IPC word will be sent to the BA.

2.8.5 EXTERNAL CONDITION REGISTER

The External Condition Register (ECR) is a 24-bit register (ECR0-23) maintained by the SBC, and a 20-bit register maintained on the MCII, to record or control "external" events. (Refer to Appendix A.) The register is divided into 5 groups on the SBC and 4 groups on the MCII. Events recorded include write parity errors, invalid memory addresses for write operations, Cache hits and misses, rejection of IPC data words, and BA "Attention Needed" requests. The full ECR can be read by the Read ECR microinstruction. The 20 or 24-bit output of the ECR passes through the IPC Data and Bus Log Multiplexer and on to the low order 24-bit positions of CP Memory Data Register #4, as DIRD0-31, via the Cache board.

To control events, the groups can be written by a Write ECR microinstruction. These include initializing the BA, and enabling and disabling Cache or ECC.

2.8.6 BUS TRANSACTION LOG

The Bus Transaction Log (BTL) is a local RAM storage area, configured as 256 32-bit words. It is used to record all hard and soft ECC errors with the associated upper twelve main memory address bits (CMA1-12) generated by the CP or the BA. Main Memory Address bits 3-4 will point to the MM board while bits 5-6 will indicate the row select. Also recorded will be Cache data and tag parity errors, with addresses, and whether the odd or even Cache word is in error. The BTL can be read with the Read BTL diagnostic microinstruction.

2.9 BUS ADAPTER

The Bus Adapter (BA) (figure 2-14) is an intermediate processor serving as an interface between the 16-bit IOP and the 32/64-bit VS-85/85-H system bus. The VS-85/85-H can support only one BA. The BA supports up to eight IOPs, however, the VS-85/85-H contains only a maximum of six IOPs. The BA has access to basic VS-85/85-H memory and Interprocessor Communications (IPC) services, and is synchronized with the SBC/MCII. The main service the BA provides is data buffering. The IOPs use 16-bit write and read operations, while data is transmitted to and from memory 32 or 64 bits at a time. The BA blocks data going from the IOP to memory and unblocks data from memory for the IOP, effectively using the 32/64-bit high speed data bus during I/O operations.

Because the BA must be able to use either the 32-bit or 64-bit bus, it must recognize whether the Cache/SBC or the MCI/MCII combination has been installed. This is done by signal SBC32/64 which basically enables either all or half of the Main Memory Data In Latch, and all or half of the odd or even word buffers.

The BA supports six words per IOP in a local RAM buffer/ register. The words are used to buffer memory or IPC data, and for holding physical addresses through which the IOP will access main memory. The BA generates a 24-bit physical main memory address from the 16-bit word supplied by the IOP.

Four groups of commands are developed by the IOP to control internal BA events and Interprocessor Communications, and to direct main memory operations. Four types of errors, plus other IOP status information, are logged in a one byte Status Register maintained on the BA. The IOP cannot directly set the full Status Register, but it can inspect the status byte. Under direction of the CP, IOP interrupts can be allowed or rejected by the BA. The BA also controls the priority of devices attached to the IOPs.

2.9.1 IOP PRIORITY

The first two IOP positions on BA #1 are always reserved for disk devices. The disk devices, because of their high speed data transfer rates, must have memory access priority over all other I/O devices. The BA must assign priority to the first disk IOP, but still allow the second disk IOP to share every other available memory access. This is accomplished by "conflict resolution" logic. The other IOP priorities are assigned on a descending IOP

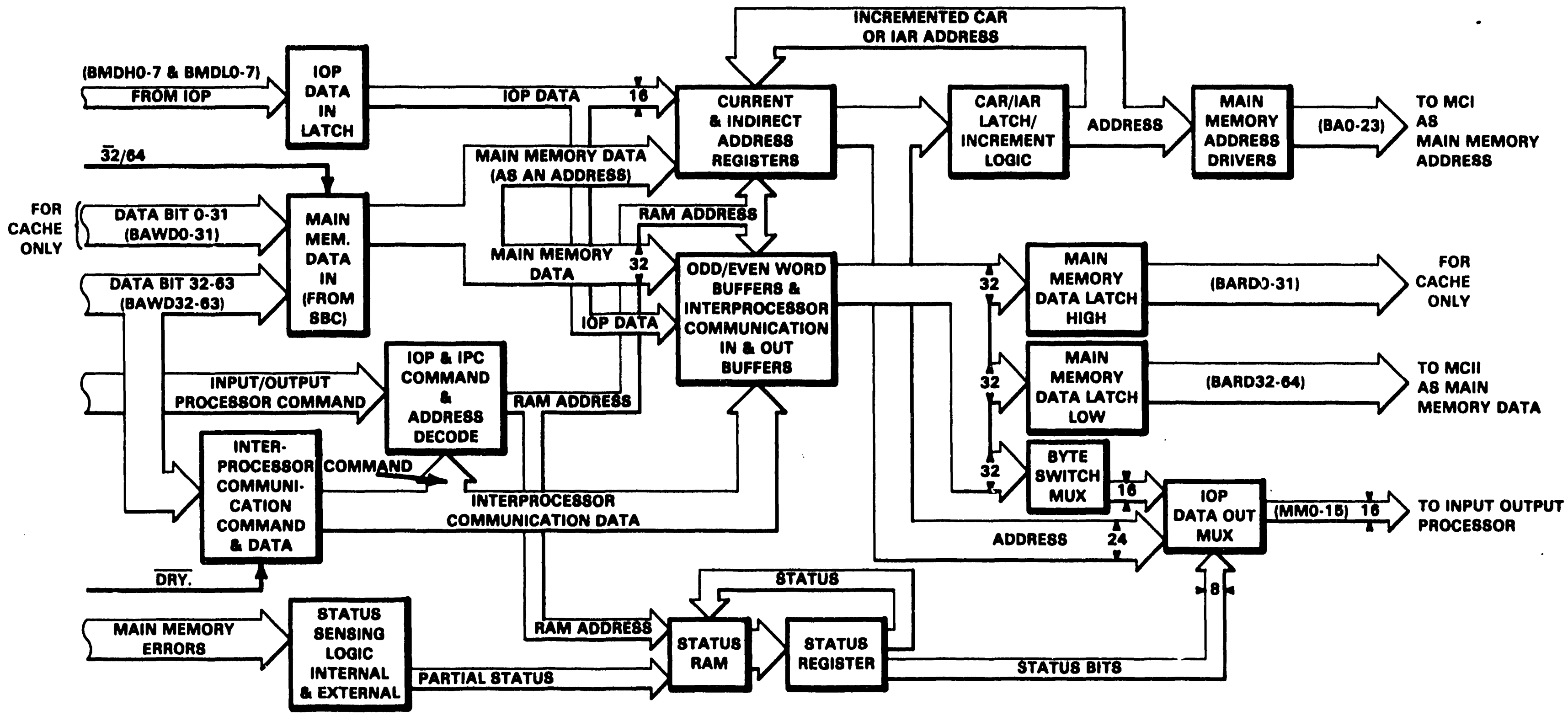

Figure 2-14. VS-85/85-H Bus Adapter

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position basis. The priority assignment process is initiated when an IOP raises its memory request line.

2.9.2 IOP INSTRUCTIONS

After an IOP has requested a memory cycle and has received a memory grant from the BA in return, it can send a command, in the form of a Control Memory Bus Interface (CMBI) instruction, to the BA. The BA will decode the CMBI into one of four instruction groups; Read/Write group, Address Control group, State Control group, or IPC group.

Each group is sub-divided into several instructions. The instructions will be used to control data and address transfers between the IOP and main memory, or in the case of IPC instructions, between the IOP and the CP. Each command contains a number of "type codes" and "qualifier bits" to further define the instruction execution.

2.9.3 ENCODING OF BA MEMORY COMMANDS

The BA must have read and write access to main memory to support the IOPs. The BA memory commands are encoded on the BA from the IOP instructions and are decoded on the main memory control portion of the SBC, located on the Cache board. The BA memory operations include Write 1, 2, 4, or 8 bytes, and Read 8 bytes.

2.9.4 WRITE IOP DATA TO MAIN MEMORY

To accomplish 1, 2, 4, or, for the SBC, 8-byte writes, the IOP will use 1, 2, or 4 halfword data transfers to the BA. The BA will either send a byte directly to the SBC/MCII for writing to MM, or store the halfwords of data in the odd or even word buffers for the Cache, or even word buffer for the MCI, until all transfers are complete.

After the BA has granted the IOP memory request and decoded the IOP instruction, data is received from the IOP as two bytes, BMDL0-7 and BMDH0-7, at the IOP Data In Latch. A 1-byte Read Modified Write will cause the high order byte (BMDH0-7) to be transferred directly to the SBC/MCII with a memory address. The byte will be sent (as the low order byte BARD56-63) through the Main Memory Data Latch Low. The other 24 bits (BARD32-55) will all be zeros. The Main Memory Data Latch Low will be enabled when the BA requests a memory cycle and the data will be transferred to the SBC/MCII when the memory control is ready. This byte replaces a byte in a full word read from memory by the SBC/MCII and the SBC/MCII is responsible for positioning the byte within the word before the word is rewritten to memory.

Because the IOP is a 16-bit device, a halfword (2-byte Read Modified) write is permitted. Only a halfword will be loaded into an odd or even word buffer.

For a 4-byte (word) write, two data transfers from the IOP are required. The first transfer will load the least significant halfword of the odd or even word buffer. The second transfer will load the most significant halfword of the odd or even word buffer.

The loading of odd and or even buffers, for both halfword and word writes, is controlled by Current Address Register bits 21 (buffer select) and 22 (halfword select within the buffer). Address bit 20 causes a write request to be issued to the SBC/MCII using the current address. Half words and word write data passes through Main Memory Data Latch Low.

For an SBC 8-byte (doubleword) write, four transfers from the IOP are needed and four odd and even word buffers are loaded. Memory Data Latch High (BARD0-31) is used for the even word of an 8-byte write.

2.9.5 ADDRESSES TO MAIN MEMORY

Two types of addressing schemes, direct or indirect, are used by the BA to access main memory. Set Address, issued by the IOP, provides the mechanism where the IOP loads a 24-bit direct physical address into the Current Address Register (CAR) before accessing a main memory area for reading or writing. Loading the physical address requires that the IOP load the least significant byte of an IOP halfword, followed by a complete halfword, into the CAR as BMDL0-7 and BMDH0-7 via the IOP Data In Latch.

Set Address Indirect causes a packaged operation, including reading main memory, to be performed. When a Set Address Indirect is issued, the BA will use the 24-bit Indirect Address Register (IAR) as a MM address as long as no other memory operations are in progress. A MM doubleword, consisting of addresses, is read by the BA as BAWD0-63 through the Main Memory Data In Latch from the SBC, or a single word as BAWD0-31 from the MCII. One word from the SBC is selected by CAR bit 22 while the other is discarded. Twenty-four bits of the word are then placed in the CAR and the IAR is rippled plus 4. Set Address Indirect can be used by the IOP for effective access of an Indirect Address List.

The IOP (via the MM0-15 lines) can also fetch a 16-bit address (one of four halfwords) from the IAR/CAR before processing an IOP level interrupt operation. The CAR/IAR Latch/Incrementer can ripple the CAR plus 1 or plus 2 for successive memory operations, and ripple the IAR plus 4 for the next doubleword.

2.9.6 MAIN MEMORY DATA TO IOP WITH BYTE SWITCHING

The IOP read request causes the deblocking of the 32/64-bit data in the BA Odd/Even Word Buffer into 16-bit halfwords. When the main memory read is serviced, using a memory address from the CAR, a doubleword of data is read from main memory and returned as BAWD0-63 to the Main Memory Data In Latch from the SBC, or a single word as BAWD0-31 from the MCII. One odd or even buffer word is selected as determined by the state of CAR address bit 21 (buffer select), while CAR bit 22 selects the halfword from within the buffer. CAR bit 23 determines if the bytes within the halfword will be switched in the Byte Switch Multiplexer. This conforms to the firmware convention in the IOP.

The halfword output of the Byte Switch Multiplexer is sent to the IOP via the IOP Data Out Multiplexer as MM0-15. The CAR address is incremented 1 or 2, and if CAR bit 20 changes, then the next doubleword read is performed. Bit 20 changing indicates that the buffer has been emptied.

2.9.7 INTERPROCESSOR COMMUNICATIONS

Interprocessor Communications (IPC) is used for generalized message passing and interrupt service between all processors (CP and BA). Thirty-two bit messages are transferred directly between processors without using MM facilities. Each message must contain its own routing information. These messages are controlled by "dialogs", which are defined as a CP initiated SEND followed by a BA response. There are two classes and five types of IPC dialogs for loading and unloading registers, reading and disabling IOP interrupts, and performing diagnostic functions. The IOP is not directly involved with the dialogs. The BA maintains an IPC In register and an IPC Out register for buffering the IPC messages. The registers can be written and read on command from the IOP.

The IPC message, controlled by an IPC dialog and by the Send and Receipt logic on the Cache board, (paragraph 2.8.9, Interprocessor Communications Control) enters the BA in the form of a separate word of data (BAWD32-63 from the SBC or BAWD0-31 from the MCII) and transfers to the IPC Command and Data Latch. The message is entered into the correct IPC In register, selected by an IOP number. The register is read and the data is sent to the IOP, via the Byte Swap Multiplexer and the IOP Data Out Multiplexer, as MM0-15. An acknowledgment message is returned by the BA to the CP indicating that either the IPC In Register was loaded and no other message be sent, or that the IPC In Register was busy and the CP should repeat the message.

When the IOP has completed the task, (start I/O, halt I/O, or control I/O, etc.) it returns the IPC message through the IOP Data In Latch to the correct IPC Out register. An IOP interrupt request is activated by the BA and the CP will read the interrupt. The CP responds with a Give IPC Out register dialog and the data word will be sent from the register through the Main Memory Data Latch Low to the CP.

2.9.8 STATUS REGISTER

The BA supports a status byte for each attached IOP. The status byte is held separately from the other IOP register areas. These status bytes are maintained by the BA during the servicing of IOP commands. The IOP cannot set the full status byte directly, but it can inspect the value of the status byte. Main memory command errors, IOP command rejection errors, and status bits ACT, MODE, PB, DWD, TOR, and IPCA are detected by the Status Sensing logic. (Refer to Appendix A, VS-85/85-H Hardware Mnemonics.) The byte is stored in the Status RAM using an address developed from an IOP number. The RAM is updated by the Status Register and the status byte is sent to the IOP, through the IOP Data Output Multiplexer, as MM0-7.

CHAPTER 3 OPERATION

CHAPTER 3

OPERATION

3.1 GENERAL

This chapter provides the CE with tables listing all VS-85/85-H mainframe controls and indicators, daily turn-on, and normal and emergency shut-down procedures. Included in this chapter are the procedures for using these controls and a brief statement on the purpose of each control and indicator.

3.2 CONTROLS

Table 3-1 lists the controls found on the VS-85/85-H followed by a brief description of their purpose. Locations of the controls are shown in figures 3-1, 3-2, and 3-3. Because it is a diagnostic tool, a detailed description of the Maintenance Panel is included in Chapter 8 of this document.

Table 3-1. VS-85/85-H Switches and Controls

CONTROL NAME AND TYPE	LOCATION	PURPOSE	NORMAL POSITION
AC ON/OFF (CIRCUIT BREAKER)	Power Filter Assembly	Applies ac power to mainframe	ON
115V/230V Line Select (Switch)*	Power Controller Board	Must be set to 115V ac position for both 115V and 208-240V systems	115V ac (FOR ALL SYSTEMS)
+5V, -5V +12V, -12V (ADJUSTMENT POTS)	Switching Power Supply front panel	Adjusts voltages up or down as needed. Refer to Chapter 5.	VARIOUS
R135, R136 R137, R138 (ADJUSTMENT POTS)	Control Memory Board (VS-85)	Fast diagnostic clock Slow diagnostic clock Refer to Chapter 8.	VARIOUS
R1, R2 R3, R4 (ADJUSTMENT POTS)	Control Memory Board (VS-85-H)	Fast diagnostic clock Slow diagnostic clock Refer to Chapter 8.	VARIOUS
POWER ON/OFF (SWITCH)	Display Panel	Initializes switching power supply to apply dc power to Motherboard	ON
CM BOOT (YELLOW PUSHBUTTON)	Display Panel	Loads system/diagnostic microcode into Control Memory from mini-floppy	NORMALLY CLOSED
CONTROL MODE (BLUE PUSHBUTTON)	Display Panel	Forces system into Control Mode	NORMALLY CLOSED
INITIALIZE (RED PUSHBUTTON)	Display Panel	Causes system to IPL from primary disk drive. System clock reset.	NORMALLY CLOSED
LOAD (GREEN PUSHBUTTON)	Display Panel	Causes system to IPL from primary disk drive. System clock not reset.	NORMALLY CLOSED
MEMORY SIZE (DIP SWITCHES)	MC I or Cache	Sets main memory size Refer to paragraph 3.2.8.	VARIOUS
IOP ADDRESS (DIP SWITCHES)	IOP circuit boards	Sets device address for each IOP. Refer to paragraph 3.2.9.	VARIOUS
MAINTENANCE (SWITCHES)	Maint Panel	Refer to Chapter 8	OFF

NOTE

The Line Select Switch has been deleted in the VS-85-H system.

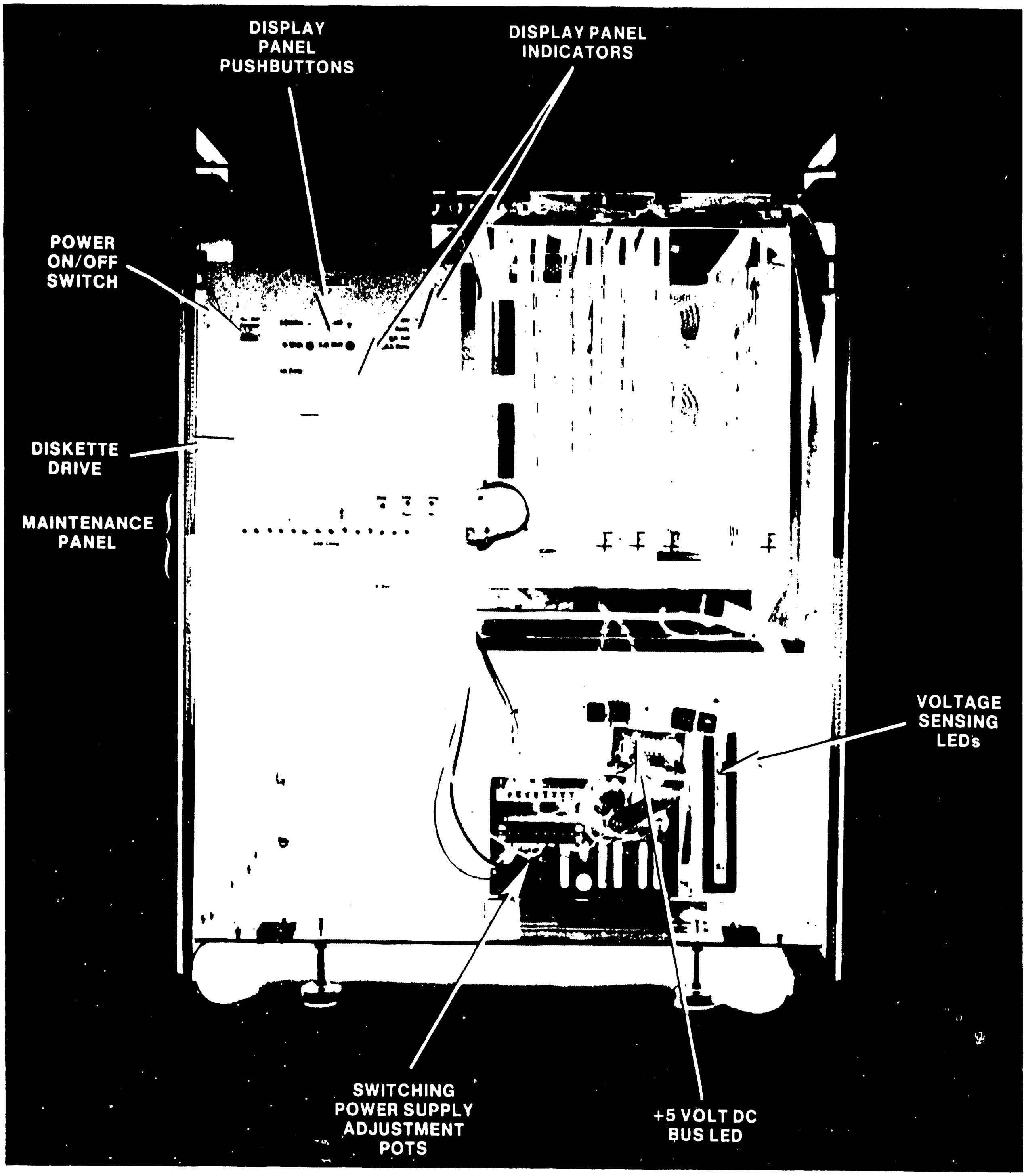


Figure 3-1A. VS-85 Mainframe Switch and Indicator Locations

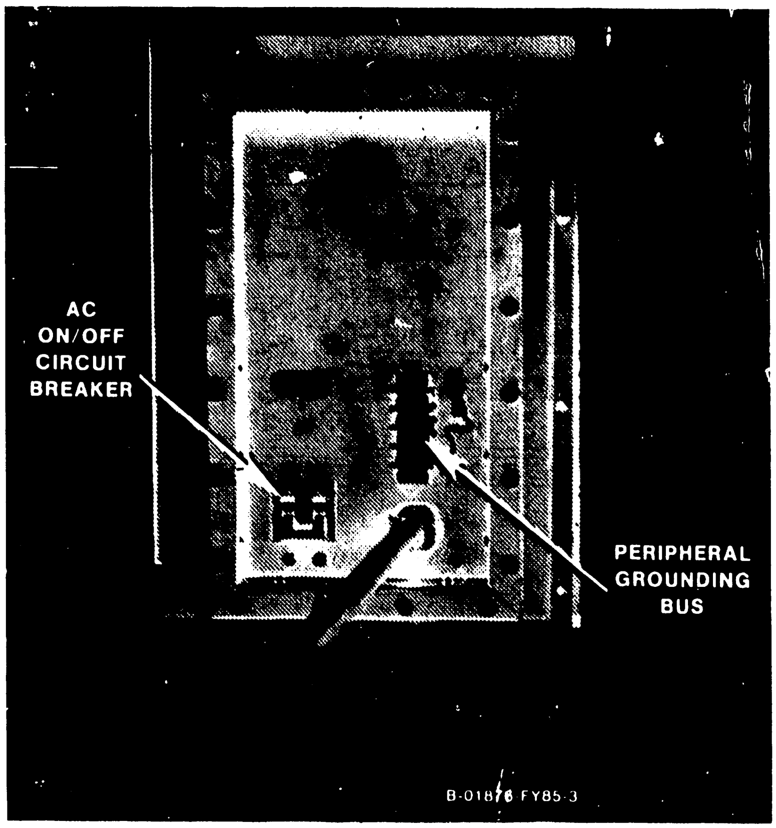


Figure 3-2B. VS-85-H Power Distribution Unit (PDU)

3.2.2 DISPLAY PANEL CONTROL BUTTONS

Located in the top left front corner of the mainframe, the control push buttons allow the user to load system or diagnostic microcode, initialize the system, or force it into the Control Mode. These push buttons are part of the Display Panel board (210-8513) and are hardwired directly to it. The four buttons are as follows: yellow CM Boot push button; blue Control Mode push button; green Load push button; and red Initialize push button. (See figure 3-3.)

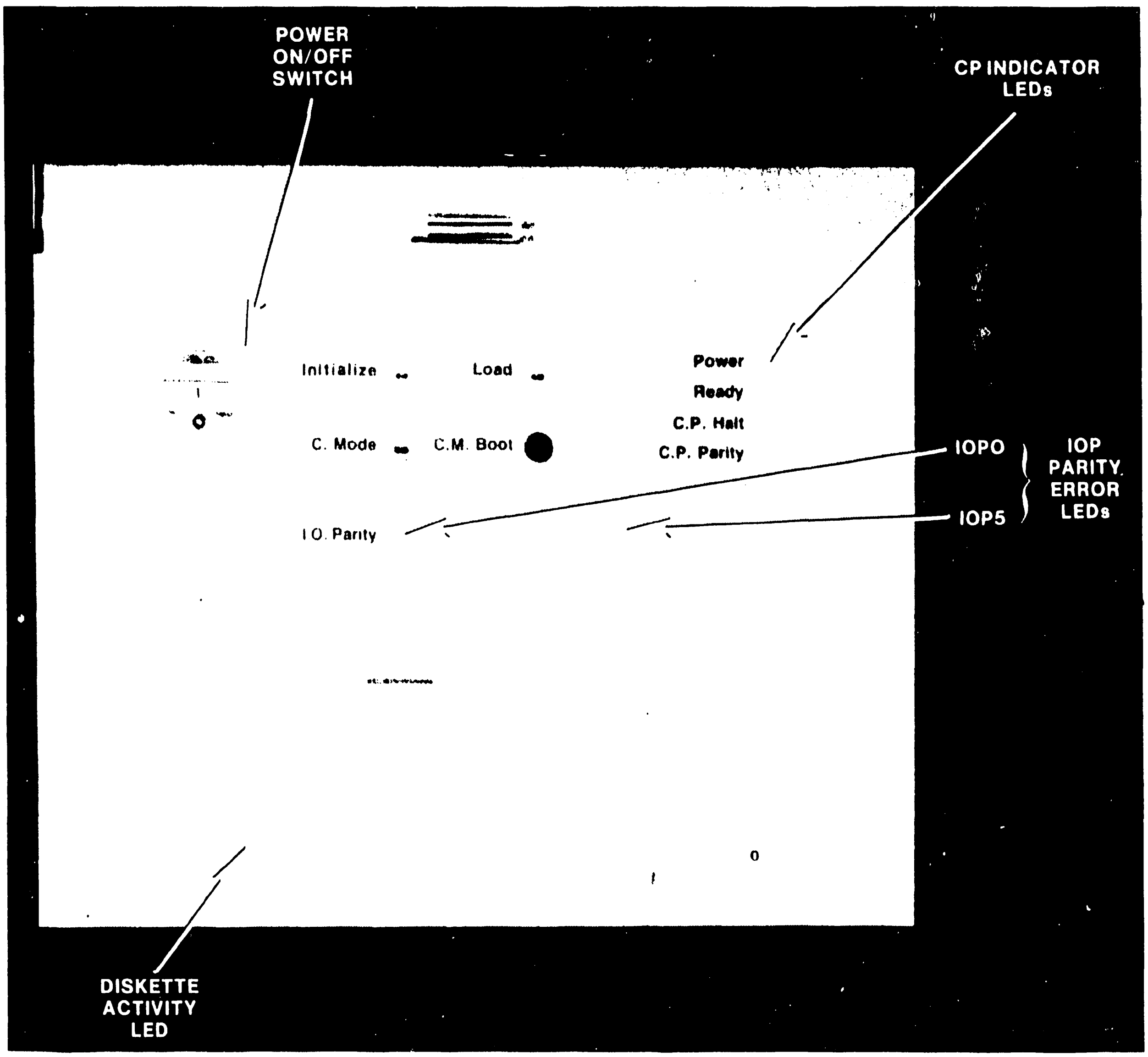


Figure 3-3A. VS-85 Display Panel Switches and Indicators

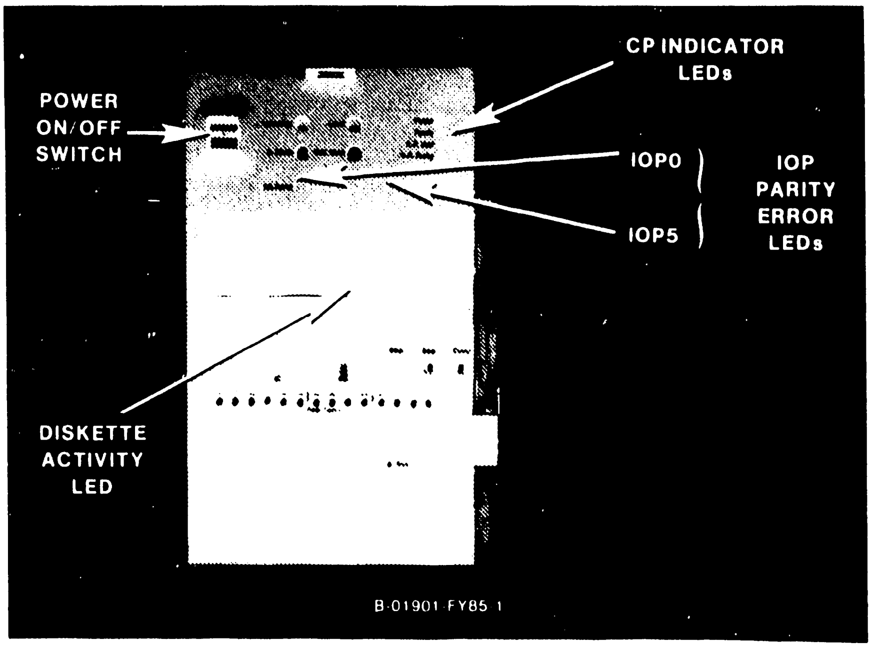


Figure 3-3B. VS-85-H Display Panel Switches and Indicators

3.2.3 BOOT PUSH BUTTON

The yellow Boot button is used whenever operational or diagnostic microcode is loaded into the system. When pressed, this button causes the CP to halt and load microcode from a diskette inserted in the minifloppy drive. Successful loading is indicated by the Ready LED on the Front Panel being lit - a flashing Ready LED indicates the microcode did not load properly.

3.2.4 CONTROL MODE PUSH BUTTON

Pressing the blue Control Mode (CM) button sets the CM bit to one, forcing the CP into the Control Mode. The CP then issues an ALERT command to IOP #2 Port 0 where Workstation 0 must be connected. The VS-85/85-H Control Mode is similar in operation to the VS-60/80/100 Control Mode. Refer to Chapter 8 for details.

3.2.5 INITIALIZE PUSHBUTTON

The red Initialize push button, when pressed, forces the system into the Initialized state. In this state, the status of the system is as follows:

1. Main memory, the Segment Control Registers (SCRs), and the CP Reference and Change Table are all set to zero.
2. The Page Table for Segment Zero (Operating System) is loaded into the T-Ram for access by the CP - remaining T-Ram entries are faulted.
3. The External Condition Register (ECR) is set to zero by the hardware as soon as the CP begins executing microcode instructions. Because zero equals Enable in the ECR, all system features under ECR control become enabled at Initialization.
4. The BA-Inhibit bit IN1 is set to zero. In this case, zero equals inhibit preventing any IOP commands from accessing the BA until the CP acknowledges the BA.
5. The System Clock is zeroed and the Comparator bits are set to one. Because of this, the user must reenter the date and time whenever the system is initialized using the Initialize pushbutton.

3.2.6 SYSTEM LOAD PUSH BUTTON

The green Load push button, when activated, causes the system to perform all functions as stated in paragraph 3.2.5, steps 1 through 4. Because the System Clock is not zeroed and the Comparator bits are not set to one, use of the LOAD button eliminates the need of reentering the date and time at the completion of initialization.

3.2.7 MAIN MEMORY SIZE

The following are the two types of main memory boards that can be installed in the VS-85/85-H: (Refer to table 5-1 for details.)

WLI P/N	CARD CAPACITY
210-7803	1 MB
210-8203	2 MB

Memory can range in size from a minimum of 1 MB (one 210-7803 board) to a maximum of 4 MB (two 210-8203 boards). Memory size can increase in 1 or 2 MB increments.

3.2.8 MAIN MEMORY SIZE SELECTION

The 210-8230 Memory Controller I or the 210-8804 Cache board has three sets of jumpers to determine the largest capacity main memory board installed in the system. The jumpers are clearly labeled 1 Meg, 2 Meg, and 4 Meg. See figures 5-9, 5-12A, and 5-13A for the jumper locations and configurations.

An 8-position DIP switch, also located on the Memory Controller I or the Cache board, and the number of 7803/8203 Main Memory boards on the CP Motherboard determine the size of main memory. Incorrect altering of switch settings, or altering of switch settings without adding the correct number of memory boards, can result in CP hangups and loss of data. Adding a board without altering switch settings results in no change in apparent memory size to the CP. See figures 5-10, 5-12B, and 5-13B for the switch location and settings.

Switch settings on the MC I or Cache board are compared with the high order memory address bits (CMA0-3) in L87 (7485 Comparator). If the switch setting is greater than or equal to the address bits, the system considers the address to be legitimate and IMA* goes High. If the switch setting is less than the address bits, IMA* goes Low (active) and the address is not processed. If the switches are set higher than the actual physical memory, however, the memory address will be accepted as legitimate and the CP will attempt to process the address. This can result in system hang-ups and possible data loss.

3.2.9 IOP SWITCHES

An eight-position DIP switch on each IOP 210-7110 Motherboard determines the location of the IOP in the CP Motherboard. On all boards, except the TC IOP, switches 1, 2, and 3 determine the Bus Adapter selected; switches 4, 5, and 6 determine the IOP slot on the Motherboard; switches 7 and 8 are not used at this time. See figure 5-22 for the switch settings for all IOPs, except the TC IOP, which is shown in figure 5-28.

3.3 INDICATORS

Table 3-2 lists the indicators found on the VS-85/85-H followed by a brief description of their purpose. Locations of the indicators are shown in figures 3-1, 3-3, and 3-4.

Table 3-2. VS-85/85-H Indicators

INDICATOR NAME AND TYPE	LOCATION	PURPOSE	NORMAL INDICATION
+5V, -5V +12V, -12V (VOLTAGE SENSING LEDs)	Power Controller board (VS-85)	Shows voltages are in limits. Four LEDs.	ON
+5V, -5V +12V, -12V (VOLTAGE SENSING LEDs)	Power Sequencer board (VS-85-H)	Shows voltages are in limits. Four LEDs.	ON
+5 VOLT BUS LED	Indicator board	Shows +5 Volt bus to Motherboard ok	ON
POWER LED	Display Panel	Shows power applied to CP	ON
READY LED	Display Panel	Shows good/bad microcode load	ON (GOOD) BLINKING (BAD)
CP HALT LED**	Display Panel	Shows CP is halted/running	ON (HALTED) OFF (RUNNING)
CP PARITY LED**	Display Panel	Shows Control Memory error	OFF
IO PARITY ERROR LEDS	Display Panel above minifloppy drive	Shows IOP parity error. One LED for each IOP (6).	OFF
MAINTENANCE PANEL HEX DISPLAYS	Maint. Panel	Refer to Chapter 8 for details	
ECC INDICATOR LEDS	Top edge MC II or SBC	Shows single-bit main memory parity error detected/ corrected. Keeps continuous count. Eight LEDs.	OFF
IOP ACTIVITY LEDS	Top edge Bus Adapter	Shows which IOP is active. Eight Leds.	FLASHING
DISKETTE ACTIVITY LED	Front of minifloppy drive	Shows drive in use (head loaded)/ not in use	ON (IN USE) OFF (NOT IN USE)

** - CP (Control Memory) Parity and CP Halt LEDs both light during a microcode load operation. Ignore these displays during the load operation. Neither indicator reflects a valid trouble condition until after the VS-85/85-H is initialized.

3.3.1 DISPLAY PANEL

The Display Panel provides the user with pertinent information concerning the operating condition of all I/O devices connected to the mainframe as well as data concerning the CP status. The panel contains 10 LEDs arranged in one vertical column with four LEDs for CP status and one horizontal row with 6 LEDs for IOP Parity Error status. (See figure 3-3.)

3.3.2 CENTRAL PROCESSOR INDICATORS

The four indicators that make up the column of LEDs on the Display Panel provide a quick check of CP status. The top LED (Power), when lit, indicates power has been successfully applied to the CP. The second LED (Ready), when lit, indicates that microcode has been successfully loaded. When this LED is flashing, loading was unsuccessful. The third LED (CP Halt), when lit, indicates that the CP is in the Halt state. The fourth LED (CP Parity lights whenever the CP detects any uncorrectable parity error in Control Memory.

3.3.3 IOP PARITY ERROR INDICATORS

When lit, each of the remaining six Display Panel LEDs indicate the occurrence of a parity error in the control word memory of the IOP associated with that particular LED. The row of LEDs is associated with IOP numbers zero through five. See figure 3-3 for LED assignments.

3.3.4 INTERNAL INDICATORS

Located within the CP chassis (figure 3-4) are several indicators that provide the CE with important system status indications. These indicators are the ECC LEDs and the IOP Activity LEDs. A description of these LEDs follows.

3.3.5 ECC INDICATOR LEDS

Eight LEDs (LED1-8), located on the top edge of the 8231 Memory Controller II or the 210-7605 SBC board, display the system's continuous count of all single-bit parity errors detected and corrected. When maximum count has been reached (all LEDs lit), the error counter is zeroed and counting begins again. On the MC I board, LED8 (the LSB of the counter) is toward the rear of the mainframe and LED1 (the MSB) is toward the front . On the SBC board, the LEDs are reversed.

3.3.6 IOP ACTIVITY LEDS

Eight LEDS (LED1-8), located on the top edge of the 8311 Bus Adapter board, indicate which IOP is active at any given time. However, because the VS-85 contains a maximum of six IOPs (IOP0-5), only six LEDs (LED1-6) are used. Whenever an IOP request for access to the CP (Memory Request In) is granted, the LED associated with that particular IOP lights and remains lit until the transaction is completed. During normal system operation, these LEDs flash briefly. LED1 (for IOP0) is toward the rear of the mainframe and LED6 (for IOP5) is toward the front.

Note LED9, the single LED on the upper right corner of the BA. Even though this LED may light, it is <u>NOT</u> a valid error indication.

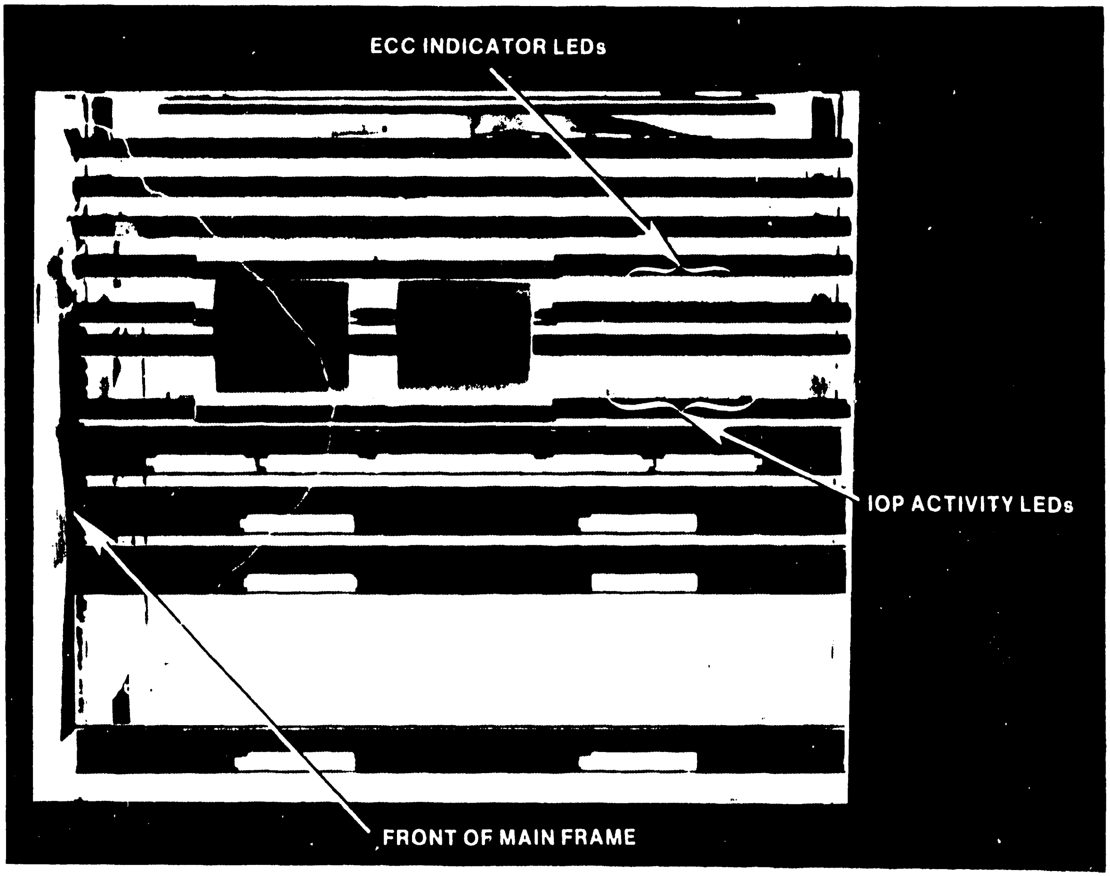


Figure 3-4. Internal Indicator Locations

3.4 SUPPORT MATERIALS

No special support materials are necessary for the VS-85 mainframe.

3.5 DAILY TURN-ON PROCEDURES

After all peripherals are connected to the mainframe, the daily turn-on procedure for the VS-85 system is as follows:

1. Make sure that the mainframe power connector is plugged into the power source receptacle.
2. Turn on the mainframe ac On/Off circuit breaker.
3. Depress the Power On/Off switch, located on the Display Panel, to the "1" position.
4. Power up the primary disk drive and Workstation #0.
5. Make sure that the system microcode diskette is in the minifloppy disk drive and then press the yellow CM Boot pushbutton.
6. After successfully loading the microcode, press the red Initialize button to begin loading the Operating System (OS) from the primary disk drive. (If Ready LED flashes instead of remaining steadily ON, system has failed to load the microcode. Reseat diskette and repeat the loading procedures. If microcode cannot be loaded, insert and load the backup diskette, if available. If this does not correct the problem, Control Memory, the drive or drive controller (210-7610) may be defective. Refer to drive maintenance procedures in Chapter 5.)

7. Workstation 0 will display Control Mode "R00". Press the BACKSPACE key and type in F (for a fixed disk) or R (for a removable disk) and the Physical Device Address of the disk the system will be IPLing from. (Refer to paragraph 4.10 for details.)
8. When system initialization has completed, the VS Operators Console screen will appear and the system is ready for normal operation.
9. After successfully loading the OS, mount the disks and power up all peripherals.
10. If this is a new installation, perform all applicable peripheral diagnostics. Refer to Chapter 8 of this document and appropriate documents in Class 3000 for the necessary instructions. Make sure that all peripherals function correctly.

3.6 DAILY VERIFICATION PROCEDURES

Daily verification procedures are as follows:

1. Perform an IPL from the system disk.
2. Log on to a workstation and and run the WSDKTEST diagnostic located in @SYSTST@ library on the system disk.
3. If there are no errors cancel the diagnostic, log off the system, and let the customer resume normal daily operations.

3.7 DAILY SHUT-DOWN PROCEDURES

The daily shut-down procedure for the VS-85/85-H system is as follows:

CAUTION

> Improperly powering down the system and/or any disk drive can result in damage to the Volume Table of Contents (VTOC) of the affected disk drive(s).

1. Make sure all operators have logged off of the system.
   a) Press PF key 13 (WORKSTATIONs) on an operators console to check that the operators have logged off of the system.
   b) Press PF key 7 (NON-INTERACTIVE Tasks) on an operators console to check the background tasks on the system. Look under the "User" column to identify any operator running a background task.
2. Press the blue Control Mode button. This prevents any disk I/O command in process from being halted prior to completion and prevents possible damage to any disk Volume Table of Contents (VTOC).
3. Power down all peripheral devices according to procedures in the applicable documents in Class 3000.
4. Depress the Power On/Off switch, located on the Display Panel, to the "0" position.
5. Turn off the mainframe circuit breaker.

3.8 EMERGENCY SHUT-DOWN PROCEDURES

In case of an emergency situation when the normal daily shut-down procedure can not be used, perform the following:

1. Press the blue Control Mode button, if possible. This prevents any disk I/O command in process from being halted prior to completion and prevents possible damage to any disk VTOC.
2. Depress the Power On/Off switch to the "0" position.
3. Turn off the mainframe circuit breaker.
4. Disconnect the mainframe power connector from the power source receptacle.

3.9 OPERATOR PREVENTIVE MAINTENANCE

No operator preventive maintenance is necessary on the VS-85/85-H mainframe.

CHAPTER 4 INSTAL-LATION

CHAPTER 4

INSTALLATION

4.1 GENERAL

This chapter describes the procedures for unpacking, inspecting, and installing the VS-85/85-H mainframe. Included in this chapter are instructions for system interconnection and initial power-up. Refer to Chapter 3, Operation; Chapter 5, Preventive and Corrective Maintenance and Removal/Replacement of this manual for more information needed to complete installation. Actual installation should not begin until the site requirements detailed in the following publications have been met.

DOCUMENT TITLE	WLI P/N
Customer Site Planning Guide	700-5978D
Systems Installation Guide for VS, 2200, and WP/OIS Systems	729-0907
VS Customer Planning and Resource Guide	700-6727

Plus any other pertinent documents in Class 1106.

4.2 INSTALLATION SITE CHECK

Prior to installation, the following conditions must have been met:

1. All site plans must have been approved by both the customer and a Wang Service Representative.
2. All building alterations must have been completed and inspected.
3. All electrical wiring, air conditioning, and telecommunications (TC) modifications must have been installed and tested.
4. If the installation is an upgrade only (CP replacement), the salesperson will make sure that serial peripheral devices replace all parallel peripheral devices.
5. The salesperson will also make arrangements to replace all 2260V 10-MB Drives. These drives are NOT supported on the VS-85/85-H system.

NOTE

It is the responsibility of the salesperson to make sure that an upgrade site meets all necessary VS-85/85-H specifications.

6. The CE will perform a preinstallation inspection two weeks prior to delivery. At this time, the CE will check the site for compliance with VS site specifications. The CE will bring any unsatisfactory conditions noted to the attention of the customer for correction.

NOTE

Before installation of a VS-85/85-H can take place, the minimum specifications as described in the previously listed publications should be met. Failure to meet these requirements can be cause for the installing CE to deem a site as unsuitable for the proper functioning of a VS-85/85-H system.

4.3 TOOLS AND TEST EQUIPMENT

TOOL DESCRIPTION	WLI P/N
Standard CE Tool Kit	726-9401

TEST EQUIPMENT DESCRIPTION	WLI P/N
Digital Voltmeter - Fluke #8022A	727-0119

4.4 UNPACKING

Before unpacking the VS-85/85-H, check all packing slips to make sure that the proper equipment has been delivered. Refer to the serial tag information below. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).

4.4.1 CLAIMS INFORMATION

If damage is discovered during inspection, file an appropriate claim promptly with the carrier involved, and notify:

WLI DISTRIBUTION CENTER
Department #90
Quality Assurance Department
Tewksbury, MA. 01876.

State the nature and extent of damage and make arrangements for replacement equipment, if necessary. Make sure to include this information:

WORK ORDER #__________
CUSTOMER NAME__________
CUSTOMER #__________
MODEL #__________
SERIAL #__________

VS-85/85-H models without Cache Memory/SBC option:

MODEL #	WLI P/N	MEMORY SIZE
VS-85-1 (Std)	157/177-7225	1 MB
VS-85-2 (Std)	157/177-7226	2 MB
VS-85-4 (Std)	157/177-7228	4 MB
VS-85-76F (H)	157/177-7323	1, 2, or 4 MB
VS-85-147F (H)	157/177-7323	1, 2, or 4 MB

Part number prefix 157 = 50 Hz/230 Vac systems
Part number prefix 177 = 60 Hz/115 Vac systems

VS-85/85-H Cache Memory/SBC option:

- VS-85 Cache (Standard; Multiwire)
- VS-85-H Cache ('H'; Multilayer))

NOTE

The VS-85/85-H Cache Memory option requires that Main Memory boards be installed in pairs - two 210-7803 1-MB MM boards for a total memory size of 2 MB or two 210-8203 2-MB MM boards for a total of 4 MB.

4.4.2 UNPACKING THE MAINFRAME

1. It is suggested that some assistance be available to help unpack the mainframe cabinet.
2. Cut the strapping that secures the top cover and outside tube to the cushion pallet. (If the strapping is metal, be careful that it does not spring out and away from the shipping container.)
3. Remove the top cover, corrugated/foam top cushion, and outside tube. (See figure 4-1.)
4. Remove the top and front covers from the VS-85/85-H cabinet. (Refer to paragraphs 5.3.6.1 and 5.3.6.2.)
5. Remove the four corner shipping bolts securing the VS-85/85-H cabinet to the cushion pallet.
6. Remove the two foam and wood support blocks from under the mainframe cabinet.
7. Slightly loosen the two nuts on the cushion pallet feet at the front of the pallet.
8. Remove the two nuts from the cushion pallet feet at the rear of the pallet.

WARNING

The mainframe cabinet weighs approximately 300 pounds. Be careful when performing the following steps.

9. While firmly grasping the rear top of the cabinet, lift the cushion pallet up over the right cushion pallet foot bolt and partially swing the foot out away from the pallet. (See figure 4-2.)
10. Repeat the previous procedure for the left cushion pallet foot.
11. Alternate steps 9 and 10 while lowering the cushion pallet until it is resting on the floor.
12. Carefully roll the VS-85/85-H mainframe cabinet off the rear of cushion pallet. (See figure 4-3.)
13. Move the cabinet to its permanent location.
14. Turn the two front leveling pads down until they support the cabinet.
15. Adjust the leveling pads to align the unit with adjacent equipment. Make sure the cabinet is level with no detectable rocking motion,
16. Once the cabinet is in place, check the service clearances as listed below.

SERVICE CLEARANCES	INCHES	CENTIMETERS
Front	36	91.4
Rear	24	60.9
Left	0	0
Right	0	0
Top	20	50.8

4.4.3 UNPACKING THE PERIPHERALS

Before proceeding, carefully unpack all peripherals according to procedures outlined in applicable maintenance manuals in Class 3000. As each unit is unpacked, check it for any obvious shipping damage.

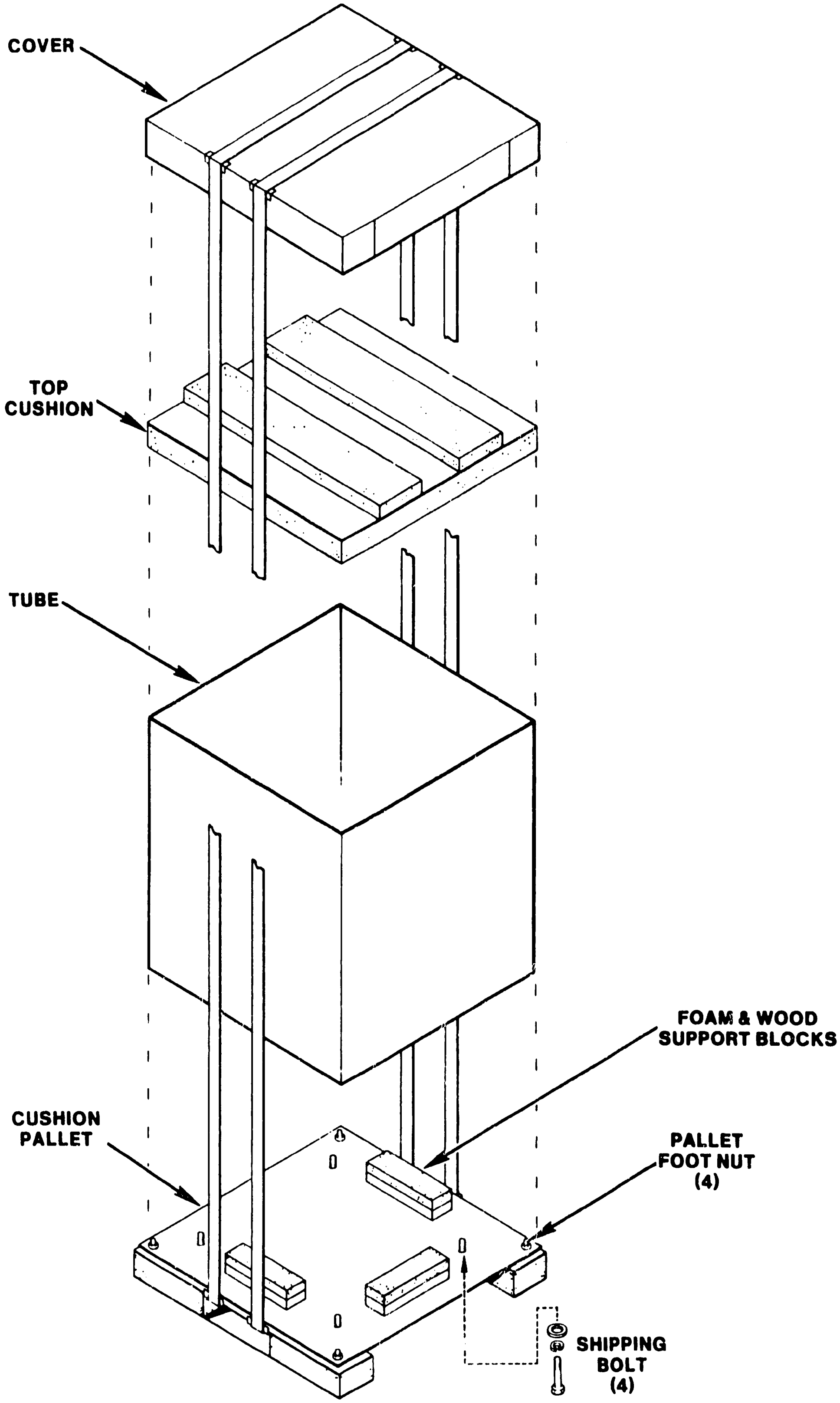


Figure 4-1. VS-85/85-H Shipping Carton

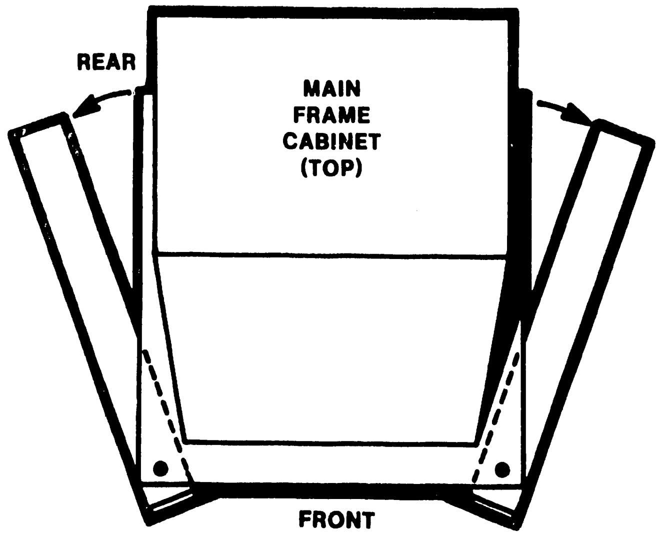


Figure 4-2. Swinging Cushion Pallet Feet

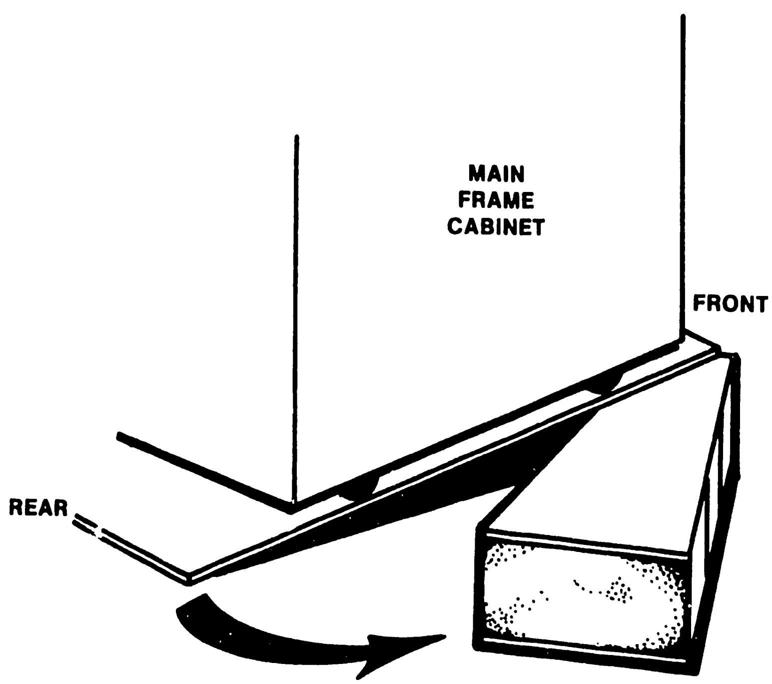


Figure 4-3. Rolling Cabinet Off Cushion Pallet

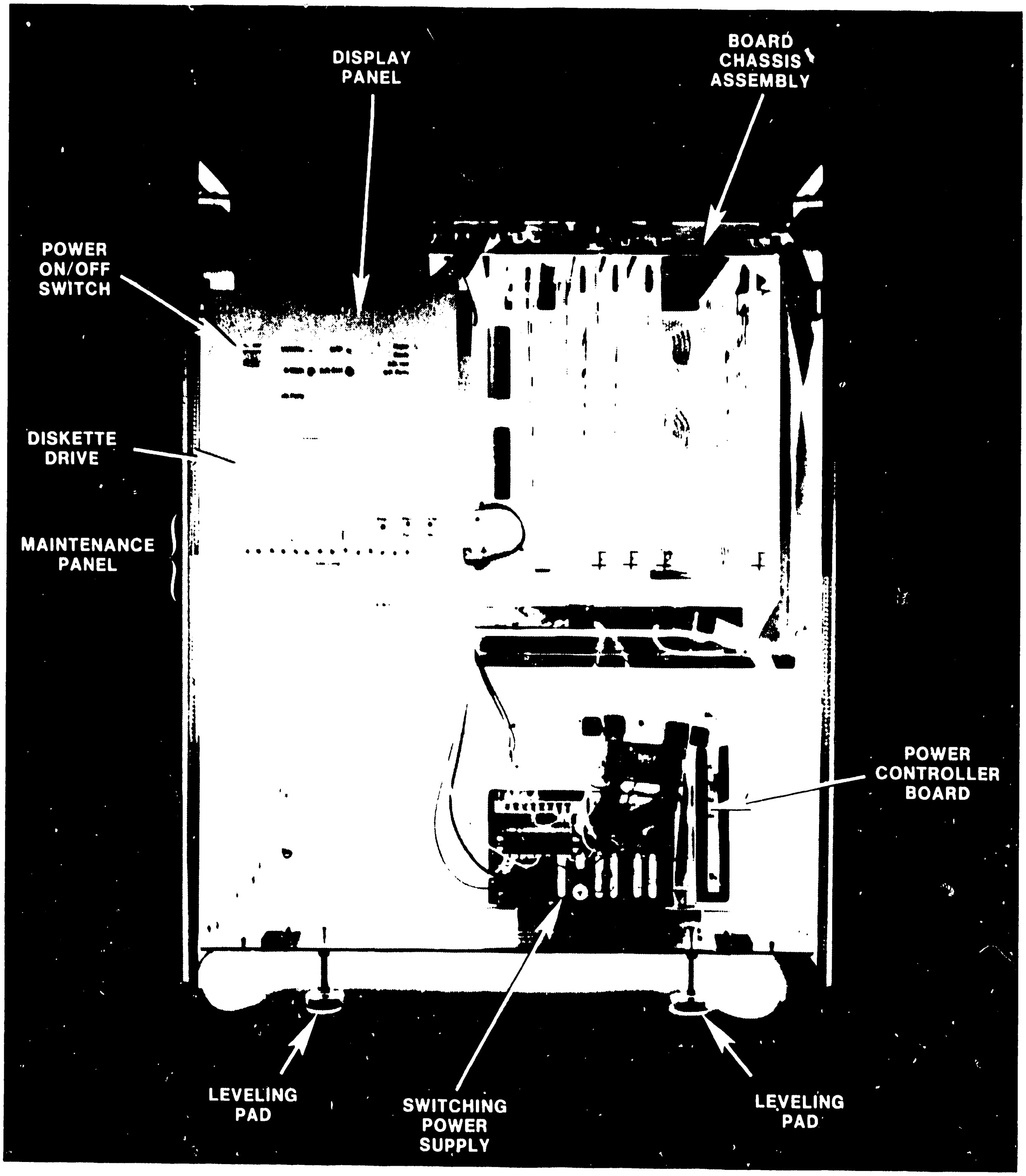
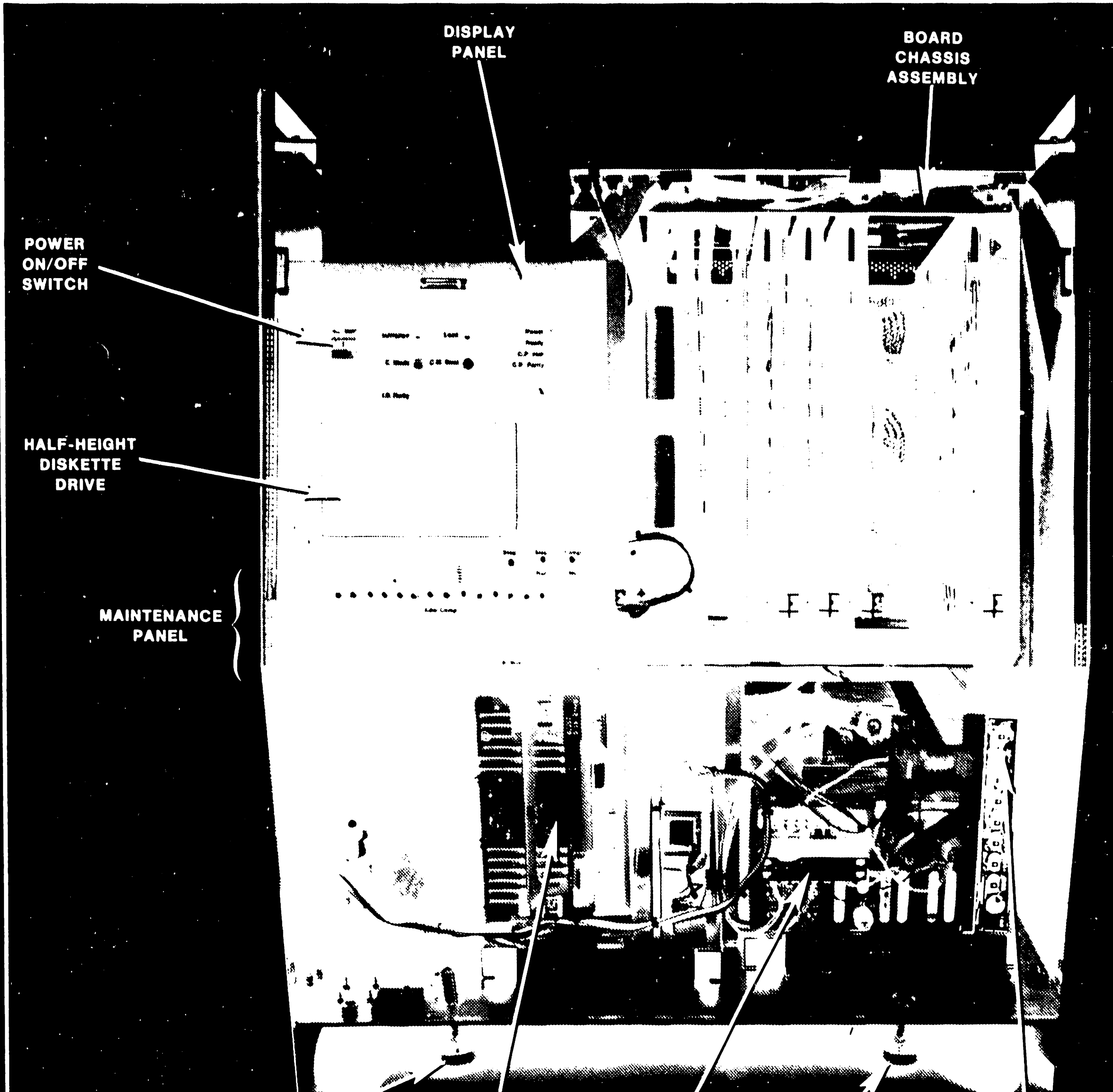


Figure 4-4. VS-85 With Top and Front Covers Removed


DISPLAY PANEL
BOARD CHASSIS ASSEMBLY
POWER ON/OFF SWITCH
HALF-HEIGHT DISKETTE DRIVE
MAINTENANCE PANEL

WARNING

```
*************************************************************
*                                                           *
*  THIS COMPUTER EQUIPMENT HAS BEEN VERIFIED AS FCC CLASS A.  *
*                                                           *
*************************************************************
```

IN ORDER TO MAINTAIN COMPLIANCE WITH FCC CLASS A VERIFICATION, THE FOLLOWING CONDITIONS MUST BE ADHERED TO DURING NORMAL OPERATION OF EQUIPMENT.

- ALL COVERS MUST BE ON SYSTEM AND SECURED IN THE PROPER MANNER.
- ALL INTERNAL CABLES MUST BE ROUTED IN THE ORIGINAL MANNER WITHIN THE CABLE CLAMPS PROVIDED FOR THAT PURPOSE.
- THE MAINTENANCE PANEL DOOR MUST BE KEPT CLOSED.
- ALL EXTERNAL CABLING MUST BE SECURED AND THE PROPER CABLE USED TO ENSURE THAT CABLE SHIELDING IS PROPERLY GROUNDED TO THE CABLE CLAMPS PROVIDED.
- MAKE SURE RFI GASKET FINGER STOCK (WLI P/N 654-2139) IS IN PLACE AND UNDAMAGED. (GASKET FINGER STOCK MAY BE ORDERED AND CUT TO PROPER LENGTH).
- ALL HARDWARE MUST BE PROPERLY SECURED.

4.5 MAINFRAME INSPECTION

NOTE

New quality assurance procedures and tests have shown that VS CPUs arriving on the customer's premises require only visual inspection, voltage checks, software loading, and cabling. Therefore, the following new inspection and installation procedures for all VS CPU products are effective immediately.

DO NOT REMOVE PRINTED CIRCUIT BOARDS FOR INSPECTION

DO NOT CLEAN PRINTED CIRCUIT BOARD CONTACTS WITH AN ERASER

INSPECT CPU MAINFRAME VISUALLY

REPORT INSTALLATION PROBLEMS ON THE INSTALLATION REPORT AND STATE SPECIFIC CAUSES OF FAILURE

1. Inspect the interior of the mainframe for packing material or such shipping damage as broken connectors and loose fastening hardware.
2. Refer to the shipping list to make sure that the correct circuit boards have been shipped. Refer to paragraph 4.6 for the minimum hardware revision levels.
3. Carefully inspect the Motherboard and fans for obvious damage or loose connections.
4. Inspect the power supply assembly for damage and loose connections. At this time, make sure that all power supply connections are tight.
5. If necessary, vacuum clean the unit.
6. Do not reassemble the mainframe at this time.
7. If damage is discovered at any time during the inspection, follow the reporting procedure in paragraph 4.4.1

4.5.1 PERIPHERAL INSPECTION

After inspecting the mainframe, carefully inspect each peripheral according to procedures outlined in the applicable maintenance manuals in Class 3000. If damage is discovered at any time during the peripheral inspection, follow the reporting procedure in paragraph 4.4.1.

4.6 MINIMUM REQUIREMENTS

4.6.1 HARDWARE

BOARD DESCRIPTION	WLI P/N	REV LEVEL
+5 Volt Indicator	210-7706	E0
A Bus (VS-85)	210-7600	E1
A Bus (VS-85-H)	**210-8568**	**E0**
B Bus (VS-85)	210-7601	E3
B Bus (VS-85-H)	**210-8569-A**	**E0**
Bus Adapter (VS-85)	210-8311	E0
Bus Adapter (VS-85-H)	**210-8572**	**E0**
Cache Memory (VS-85, optional)	210-8804	E0
Cache Memory (VS-85-H, optional)	**210-8570-A**	**E0**
Control Memory (VS-85)	210-7602	E1
Control Memory (VS-85-H)	**210-8204-A**	**E4**
Disk Adapter	210-7114	E11
Display Panel	210-8513	E0
IOP Motherboard	210-7110-U	E5
Main Memory (1 MB)	210-7803	E0
Main Memory (2 MB)	210-8203	E0
Maintenance Panel	210-7614	E0
Memory Controller I	210-8230	E0
Memory Controller II	210-8231	E0
Mini Diskette Controller	210-7610	E0
Motherboard	210-8508	E0
Power Controller (VS-85)	210-8250	E0
Power Sequencer (VS-85-H)	**210-8198**	**E0**
Serial Adapter (16-port)	210-7216-A	E4
System Bus Controller (VS-85, optional)	210-7605	E2
System Bus Controller (VS-85-H, optional)	**210-8571-A**	**E0**
TC Adapter (1-port Daughterboard)	210-7427-A	E1
TC Adapter (1-port Motherboard)	210-7826	E5
TC Adapter (2-port Daughterboard)	210-7427-1A	E1
Tape Adapter	210-7217-A	E6
Very Large Disk Adapter (1-port)	210-8318	E5
Very Large Disk Adapter (2-port)	210-8319	E5
Very Large Disk Adapter (3-port)	210-8320	E6
Very Large Disk Adapter (4-port)	210-8321	E5

4.6.2 SOFTWARE

SOFTWARE DESCRIPTION	VERSION	COMMENTS	WLI P/N
VS-85 Microcode	4.57.07	- - -	705-0154-E
VS-85-H Microcode	4.58.04	- - -	705-XXXX X
Operating System	5.00	Minimum	- - -
Operating System	6.10	See Note 1	- - -
Operating System	6.20	- - -	- - -
Operating System	**6.30**	**See Note 2**	- - -

NOTES

1. Control Data (CDC) 620 MB disk drive needs Operating System 6.10 and above.

2. **VS-85-H requires Operating System 6.30 to support NEC disk drive.**

4.6.3 DIAGNOSTICS

MICRODIAGNOSTICS

TEST	DIAGNOSTIC NAME	VERSION	PACK. P/N	DISKETTE P/N
T0010	Microsequencer, Uncond. Branch	7130	-----	702-8001-A
T1010	Instruction Counter	7130	-----	702-8002-A
T2010	Branch Cond. & Status Ops	7130	-----	702-8003-A
T3010	Stack Data Integrity	7130	-----	702-8004-A
T4010	Routine Stack Address	7130	-----	702-8005-A
T4110	Register Data Integrity	7130	-----	702-8006-A
T5000	Visual Verification	7130	-----	702-8007-A
T6010	CM Moving Inversions (Upper)	7130	-----	702-8008-A
T6110**	**CM MOving Inversions (Upper)**	**7470**	**-----**	**702-8036**
T7010	CM Moving Inversions (Lower)	7130	-----	702-8009-A
T7110**	**CM Moving Inversions (Upper)**	**7470**	**-----**	**702-8037**
T8010	Register Data Integrity	7130	-----	702-8010-A
T9010*	Data Stack & T-RAM	7130	-----	702-8011-A
T9110	**Data Stack & T-RAM**	**7470**	**-----**	**702-8038**
TA010	Add & Subtract Group	7130	-----	702-8012-A
TB010	Logical Instructions	7130	-----	702-8013-A
TB110	Move Instructions	7130	-----	702-8014-A
TC010	Shift & Decimal Add & Subtract	7130	-----	702-8015-A
TD010	Condition Code & Arith. Logical	7130	-----	702-8016-A
TAA10	Memory Opcodes & Multiply Group	7350	195-2638-8	-----
TAF10	Enhanced Next Macroinstruction	7356	195-2641-8	-----
TBA10	Bus Adapter	7450	-----	702-8035
TBB10	ECR, Memory Controller/IPC/DMA	7350	195-2639-8	-----
TBB40	SBC Err/BTL	71C1	-----	702-8020-A
TCC10	Cache Board	7454	-----	702-8021-B
TDA10	**Main Memory Board**	**7470**	**-----**	**702-8039**
TDE10	Main Memory Board	7350	195-2640-8	-----

*** T9010 may fail on the VS-85-H due to T-RAM enhancement instruction; use T9110.**
****T6110 and T7110 required for expanded CM in VS-85-H.**

OTHER DIAGNOSTICS

DIAGNOSTIC NAME	VERSION	PACK. P/N	DISKETTE P/N
(TCIOPTST) 22V06 Local Loopback Test	1455	195-2972	-----
ELOGDISP (On-line)	1.0	-----	702-0070
FTU On-Line	6365	195-2652-3	-----
PRTEST1 (On-line)	2.0.1	-----	702-0092
SYSNAME (On-line)	8110	-----	702-0107
TPTEST (On-line)	6224	-----	702-0187
VS On-line Printer Part I Monitor	2242	-----	702-0179A
VS On-line DTOS Printer 2	2211	195-2535-3	-----
VS On-line DTOS Printer 3	2420	195-2899-3	-----
VS On-line DTOS Device 1	2450	195-4036-3	-----
VS On-line DTOS Device 2	2430	195-2615-3	-----
VS On-line DTOS Device 3	2334	195-2604-3	-----
VS On-line DTOS Device 4	2440	195-2976-3	-----
FTUA Stand Alone Simulator	6385	195-2626-3	-----
UNIBOOT (Stand-alone)	8466	195-2479-3	-----
VOLCOPY (Stand-alone)	8181	-----	702-0122A

NOTE: Complete 195 package part numbers include diskette and documentation. Diskette only part numbers are shown if no package part numbers are available.

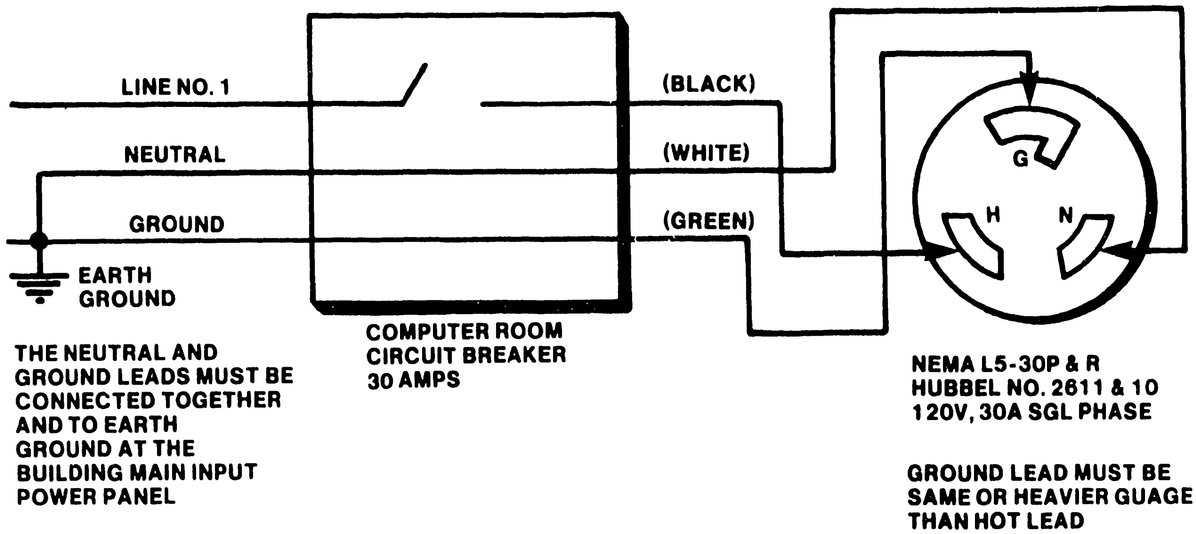
4.7. MAINFRAME POWER SOURCE CHECK

4.7.1 115VAC DOMESTIC POWER SOURCE

Before completing the mainframe reassembly and peripheral equipment installation, use a Digital Voltmeter (DMV) to check the mainframe power source receptacle for proper wiring and service as defined in figure 4-5 and table 4-1. Perform the following electrical checks to make sure that the receptacle meets all specified requirements before proceeding with the installation.

CAUTION

Failure to perform the following check properly can result in serious damage to mainframe circuits and to connected peripherals.



	RECEPTACLE BODY	MATCHING CONNECTOR
NEMA Configuration	L5-30R	L5-30P
Hubbel Part Number	2610	2611

Figure 4-5. 115 Volt AC Power Source Requirements for VS-85/85-H Mainframe

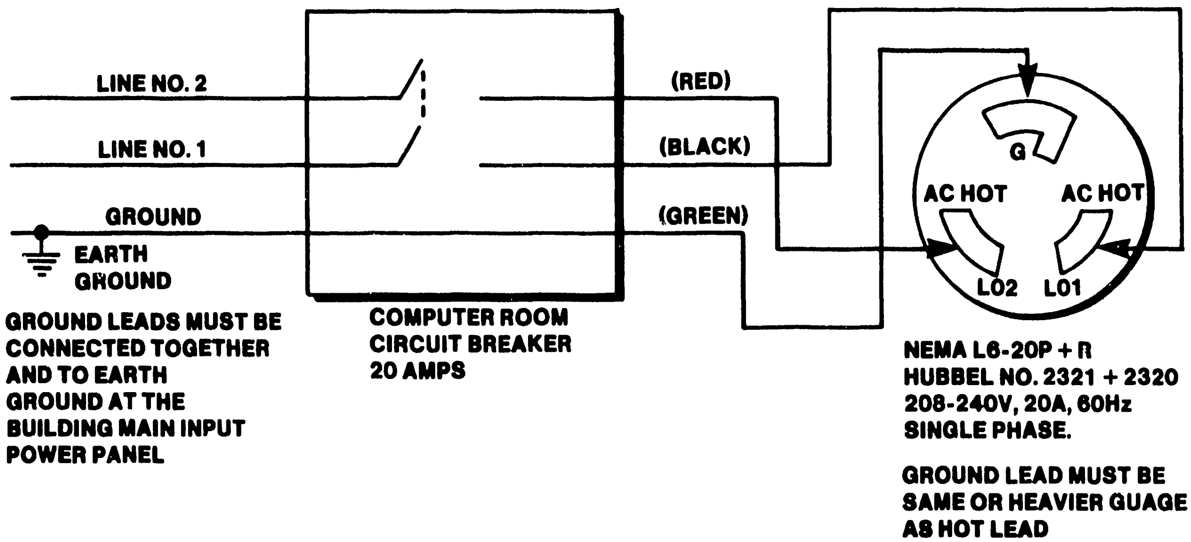
Table 4-1. DVM Voltage Measurements for the 115VAC Receptacle

MEASURE FROM	ACCEPTABLE DMV READINGS
AC HOT to NEUTRAL	115V AC (+/-10%)
AC HOT to GROUND	115V AC (+/-10%)
GROUND to NEUTRAL	0 VOLTS AC (Note)

NOTE

If a difference in potential of more than 0.2 Volts ac exists between neutral and ground, notify the responsible electrician that the power source is NOT ACCEPTABLE.

4.7.2 208-240VAC DOMESTIC POWER SOURCE



	RECEPTACLE BODY	MATCHING CONNECTOR
NEMA Configuration	L6-20R	L6-20P
Hubbel Part Number	2320	2321

Figure 4-6. 208-240 Volt AC Power Source Requirements for VS-85/85-H Mainframe

Table 4-2. DVM Voltage Measurements for the 208-240VAC Receptacle

MEASURE FROM	ACCEPTABLE DVM READINGS
AC HOT (01) to GROUND	120V AC (+/- 10%)
AC HOT (02) to GROUND	120V AC (+/- 10%)
AC HOT (01) to AC HOT (02)	208-240V AC (+/-10%)

NOTE

AC neutral is not used with 208-240VAC VS-85/85-H systems.

4.7.3 INITIAL MAINFRAME POWER-UP

CAUTION

Before powering on a NEC disk drive in the VS-85-H, be sure that the spindle is in the "FREE" position. To free the spindle, move the red lever on the front of the drive to the right, up, and left to the "FREE" position. Failure to perform this step could result in damage to the servo and drive motor components. (Refer to Figure 4-7 below.)

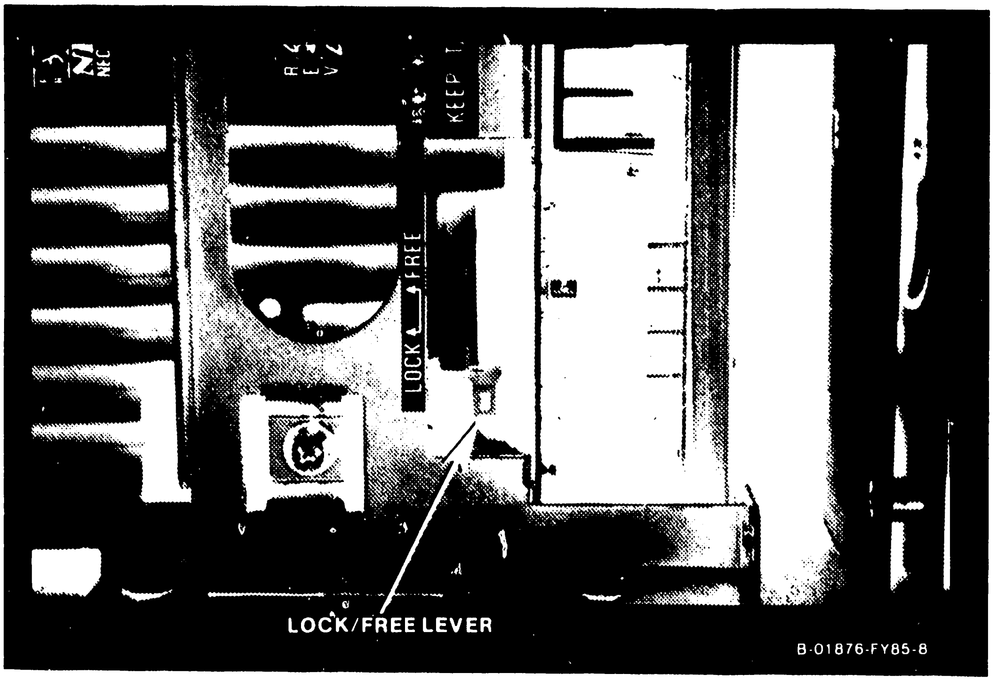


Figure 4-7. NEC Disk Drive LOCK/FREE Lever

1. After making sure that the Power On/Off switch on the Display Panel is in the "0" position and the mainframe ac On/Off circuit breaker on the Power Filter Assembly (figure 3-2A and 3-2B) is OFF, plug the main- frame power connector into the power source receptacle.
2. Make sure the 115/230V Line Select Switch on the 8250 Power Controller board (figure 4-7) is in the 115 vac position for ALL VS-85 systems **(not available on the VS-85-H)**. (Check which switching power supply is installed in the system. If it is a Powertec supply, it also has a 115/230V Line Select Switch. Check the rear of the supply to make sure the switch is in the 115 vac position. This applies to ALL VS-85 systems.)
3. Perform the following in the sequence given:
   a. Turn ON the mainframe ac On/Off circuit breaker.
   b. Make sure the mainframe cooling fans force the air flow into the rear of the mainframe cabinet. If the air flow is out of the rear of the cabinet, power down the mainframe and physically reverse the fans. (Refer to paragraph 5.3.6.30.) Air flow in the wrong direction will cause damage to the circuit boards.

CAUTION

It is critical that only fans that supply 115 cubic feet of air per minute (CFM) are used in the VS-85/85-H mainframe cabinet. These fans should be WLI P/N 400-1028.

c. Depress the Power On/Off switch to the "1" position.

d. Make sure that the Power On LED on the Display Panel and the +5 volt LED on the 210-7706 +5 Volt Indicator board are lit. If the LEDs go out after 2 seconds, there is a problem with the dc voltage compare circuit in the power supply.

4.7.4 DC VOLTAGE CHECKS

1. The following voltages should be checked at the 8250 Power Controller board (figure 4-8A) and at the 8198 Power Sequencer board (figure 4-8B) test points.
2. Adjust the voltages to the test point readings (below) using the potentiometers on the front of the switching power supply (figures 4-9A and 4-9B) and on the side of the 24-volt supply (figures 4-10 and 4-11).

Table 4-3A. DC Voltage Measurements at VS-85 Power Controller Board

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+5.0	+4.9V to +5.1V	35mV RMS or 50mV Pk-to-Pk
+12.0	+11.9V to +12.1V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.9V to -5.1V	35mV RMS or 50mV Pk-to-Pk
-13.6	-13.5V to -13.7V	35mV RMS or 50mV Pk-to-Pk

Table 4-3B. DC Voltage Measurements at VS-85-H Power Sequencer Board

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+5.0	+4.9V to +5.1V	35mV RMS or 50mV Pk-to-Pk
+12.0	+11.9V to +12.1V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.9V to -5.1V	35mV RMS or 50mV Pk-to-Pk
-13.6	-13.5V to -13.7V	35mV RMS or 50mV Pk-to-Pk
+24.0	+21.6V to +26.4V	170mV RMS or 240mV Pk-to-Pk

3. The +5 Vdc adjustment for the LH supply can be done with the system powered up. However, due to the locations of the potentiometers, the -5, +12, and -12 Volts can't be adjusted with the system powered up. Measure the -5, +12, and -12 at the 8250 Power Controller board or 8198 Power Sequencer board test points; power down the system and and adjust the potentiometer(s); power up the system and recheck the voltages. Continue this procedure until the voltage(s) are correct.

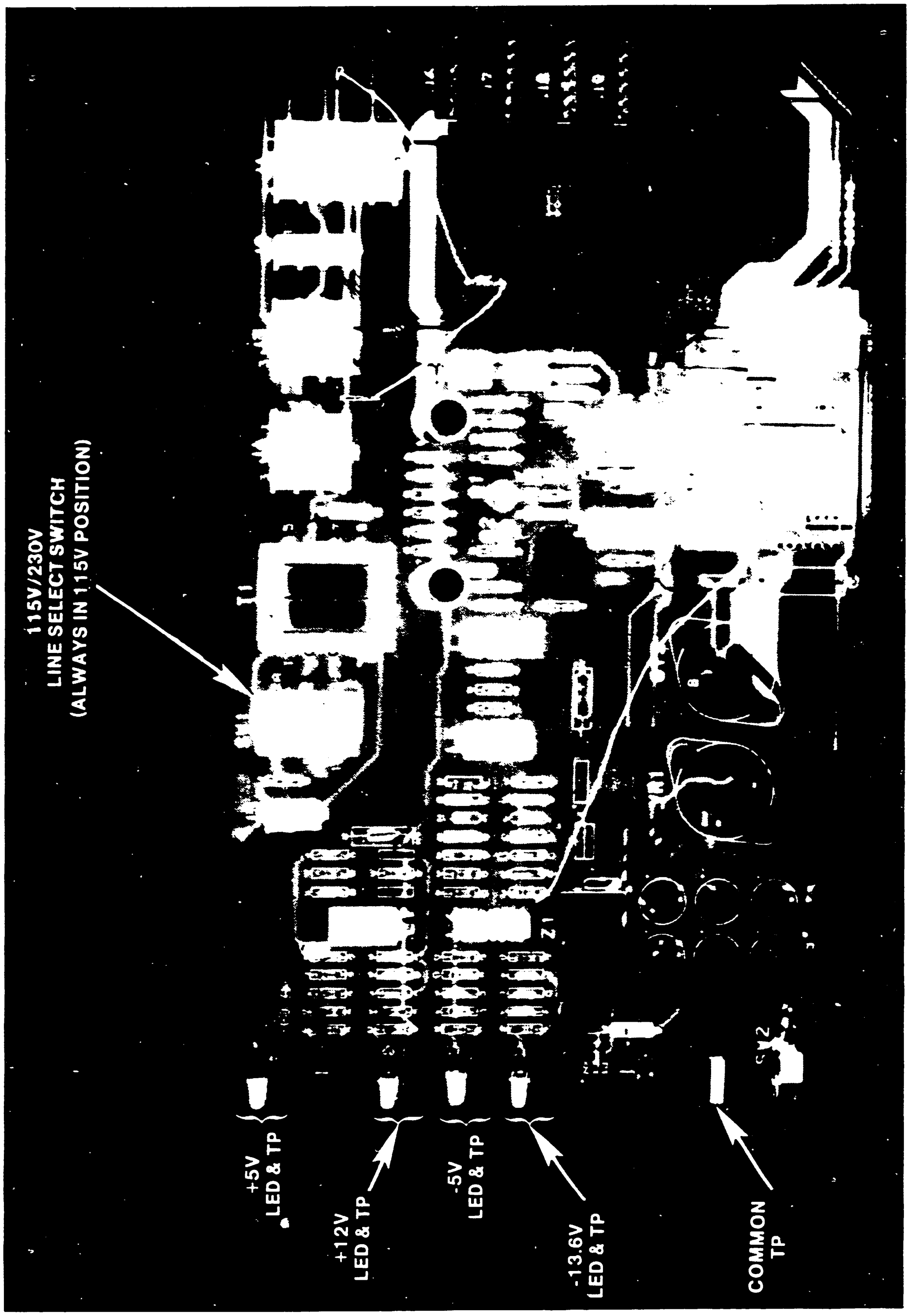


Figure 4-8A. 210-8250 VS-85 Power Controller Board

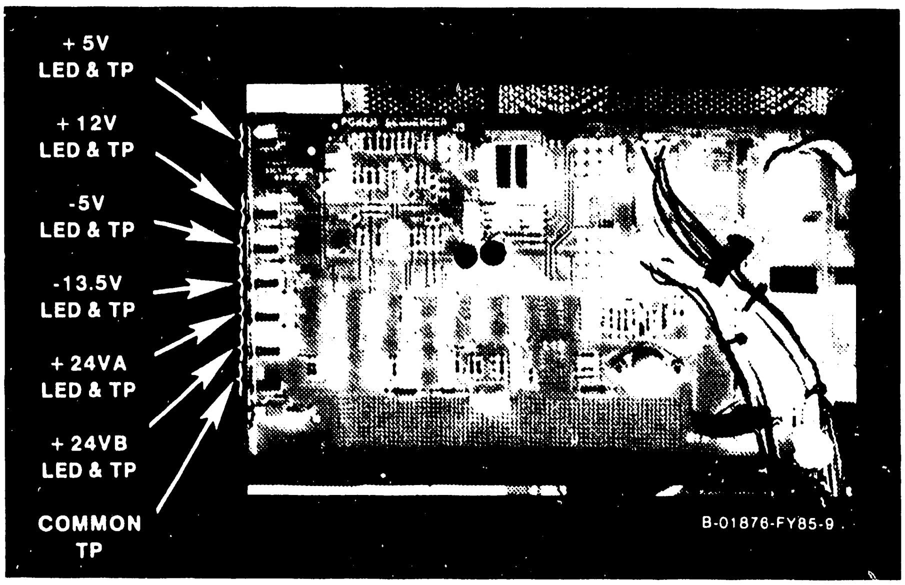


Figure 4-8B. 210-8198 VS-85-H Power Sequencer Board

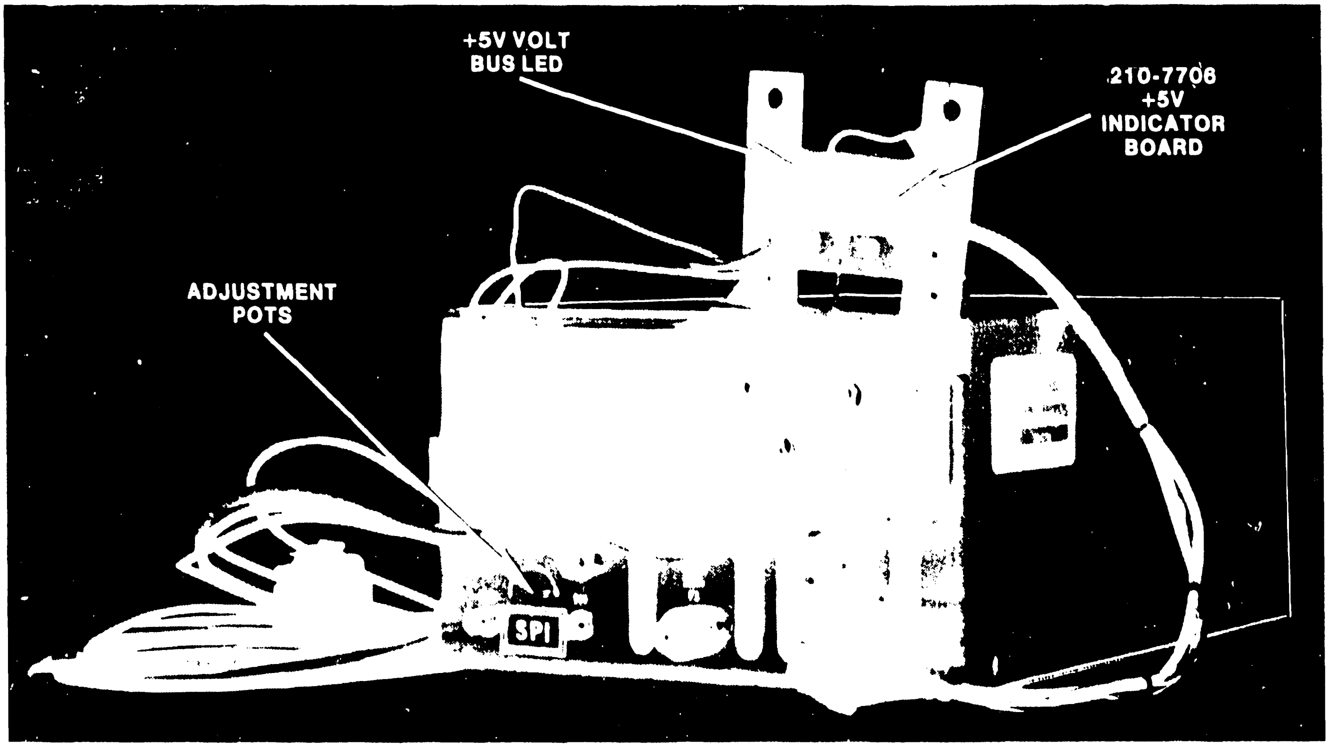


Figure 4-9A. VS-85/85-H Switching Power, Inc. Switching Power Supply

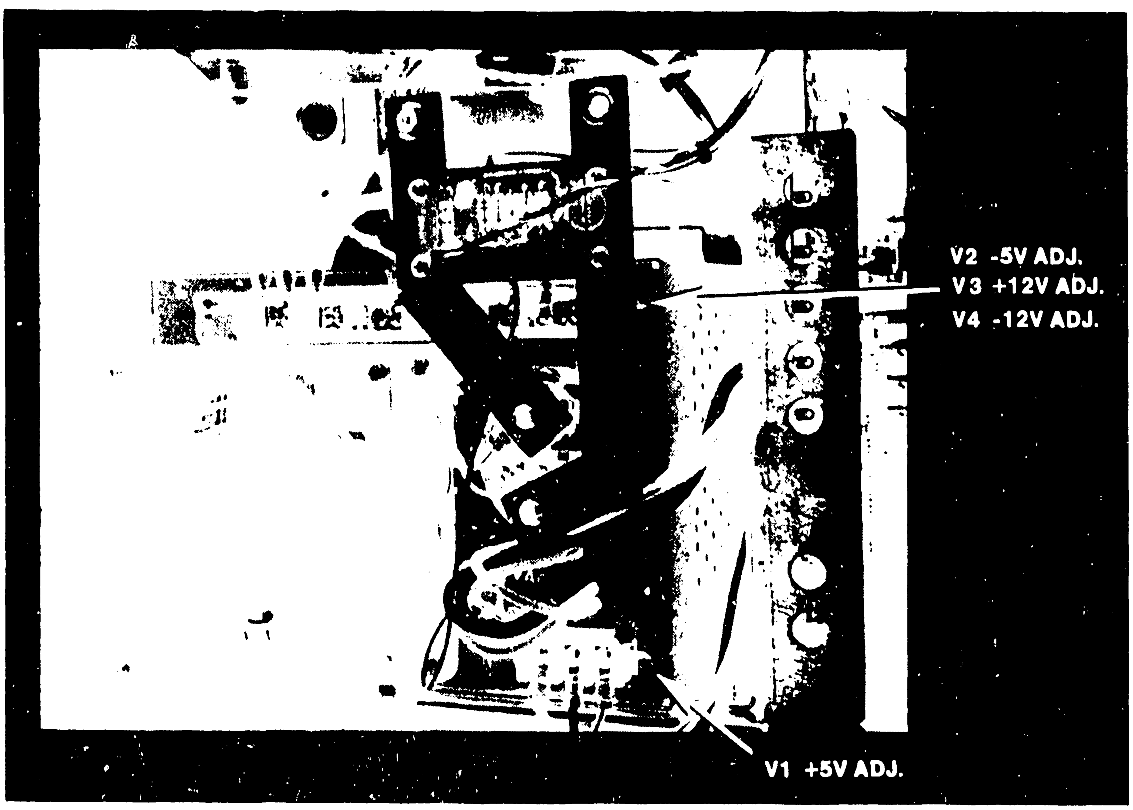


Figure 4-9B. VS-85/85-H LH Switching Power Supply

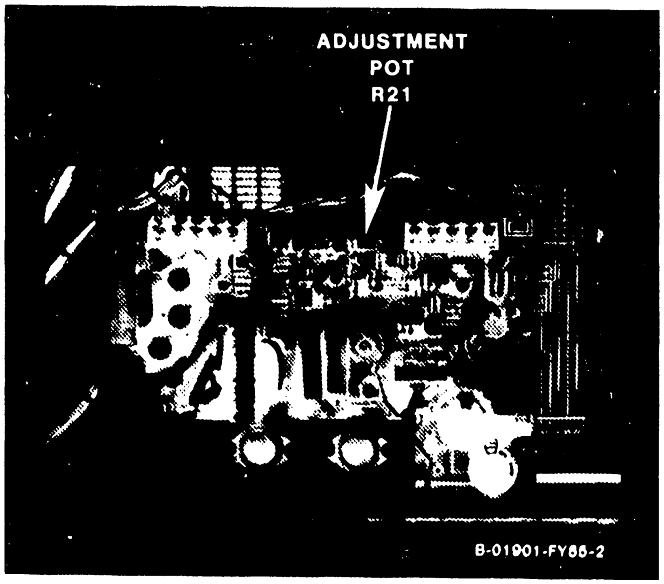


Figure 4-10. VS-85-H Switching Power, Inc. +24-Volt Power Supply

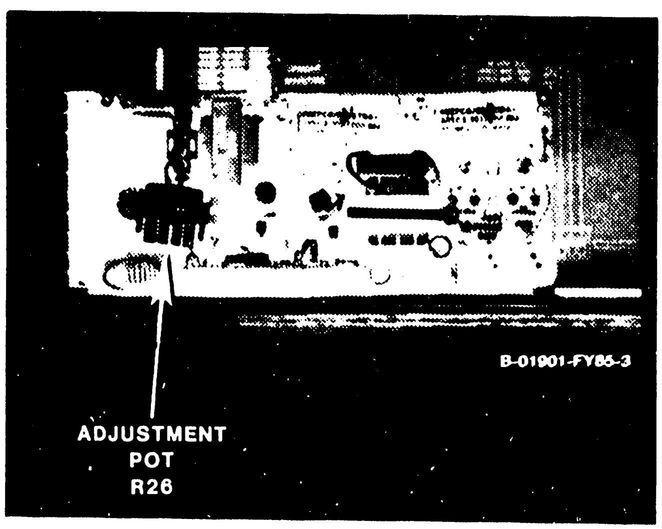


Figure 4-11. VS-85-H LH +24-Volt Power Supply

4.8. RUNNING DIAGNOSTICS

As part of the installation and PM procedures, and at any time CP integrity becomes suspect, the microcode diagnostics must be loaded and run. Refer to Chapter 8 for a complete list of microcode diagnostics and to paragraph 8.3.1 for instructions on running the diagnostics.

4.9 INITIAL MICROCODE LOADING

Once the diagnostics have run successfully, load the system microcode into Control Memory as follows:

1. Power down the mainframe and create a minimum system as follows:

   a. Attach a serial workstation to IOP 2, Port 0. This device will be Workstation 0 (W/S 0).
   b. Connect a disk drive to IOP 0, Port 0 (a 22V28 Large or 22V88 Very Large Disk IOP). **(The 22V28 Large Disk IOP is not supported in the VS-85-H.)** This disk is the system disk and stores the OS software. (There are four versions of the 22V88 Very Large Disk IOP; 1-port, 2-port, 3-port, and 4-port.)
   c. Power up the system.

2. To load the microcode into Control Memory, insert the microcode diskette into the mini-diskette drive, close the drive door, and press the C.M. Boot button on the Display Panel (see figures 4-12A and 4-12B).

3. The Diskette Activity LED on the front of the mini-diskette drive lights to show the drive is in use. When the Diskette Activity LED goes out and the Ready LED on the Display Panel lights, the microcode is loaded.

   NOTE

   If the Ready LED flashes instead of remaining steadily ON, the system has failed to load the microcode. Reseat the diskette and repeat the loading procedures. If the microcode cannot be loaded, insert and load the backup diskette, if available. If this does not correct the problem, Control Memory, the drive, or drive controller (210-7610) may be defective. Refer to drive maintenance procedures in Chapter 5.

   Also, the C.P. (Control Memory) Parity LED or the C.P. Halt LED may light during a microcode load operation. Ignore these displays during the load operation. Neither indicator reflects a valid trouble condition until after the VS-85/85-H is initialized.

4. Press the Initialize pushbutton. Both the C.P. (Control Memory) Parity and C.P. Halt LEDs should go out.

5. Perform the IPL procedure described in paragraph 4.10.

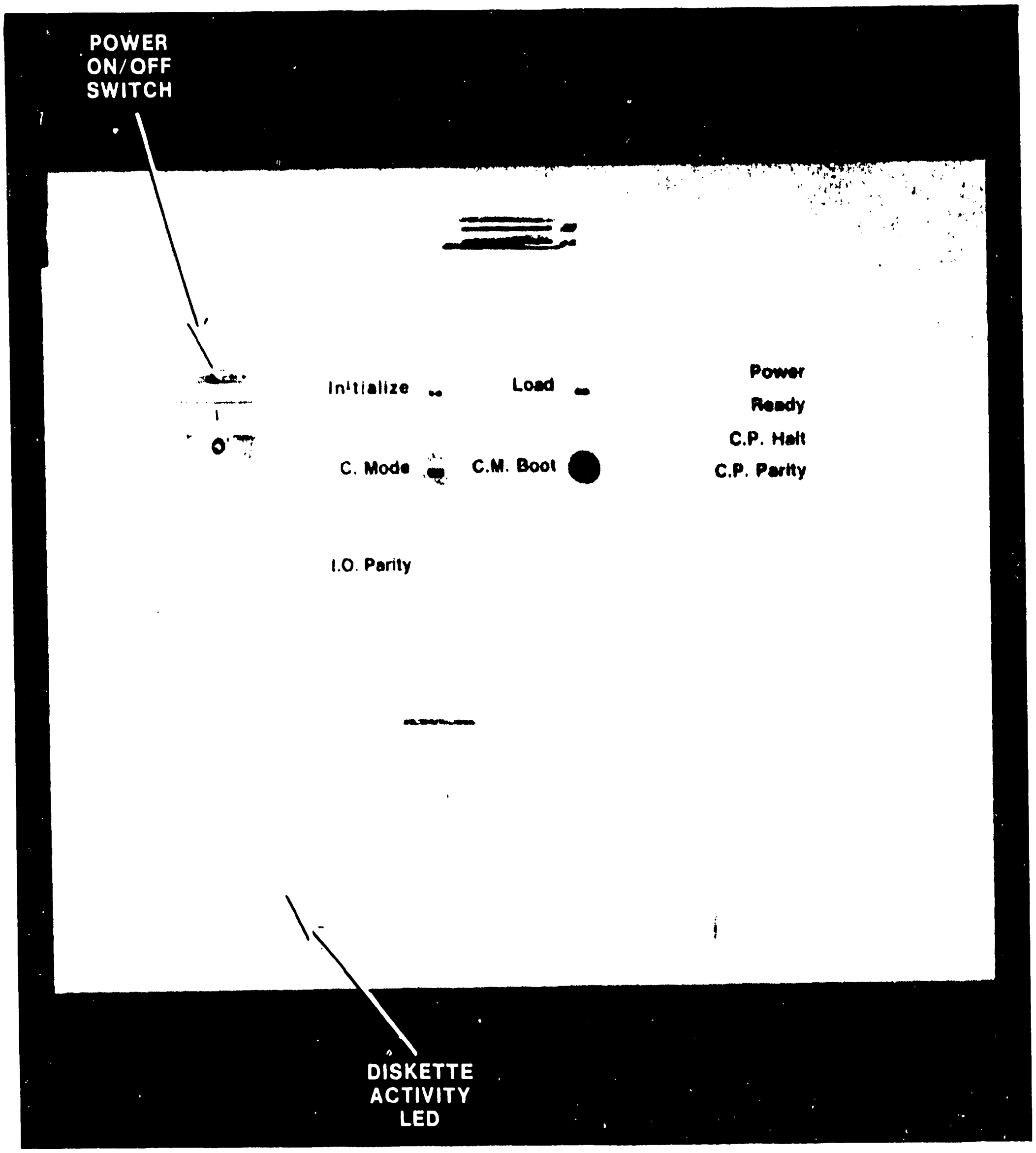


Figure 4-12A. VS-85 Display Panel Controls and Indicators

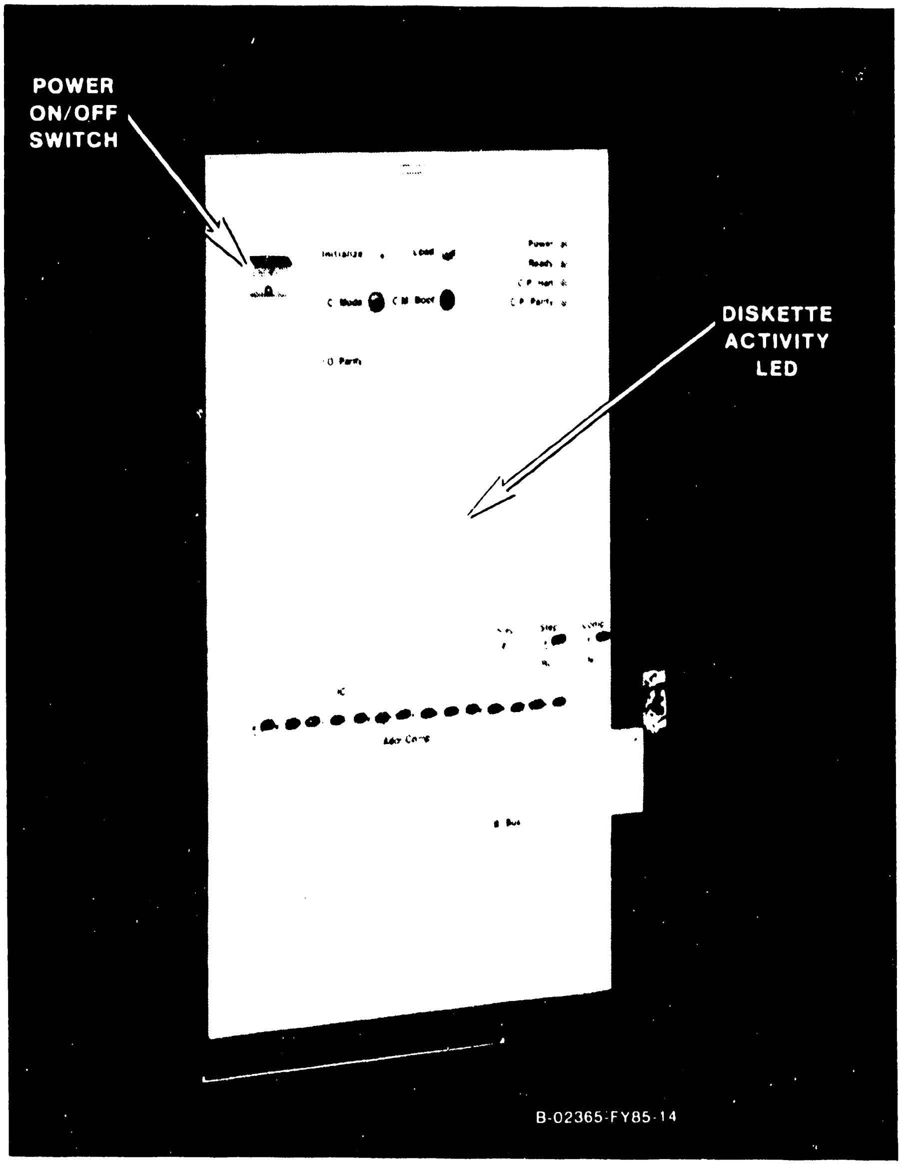


Figure 4-12B. VS-`5-H Display Panel Controls and Indicators

4.10 IPL PROCEDURE

1. After pressing the Initialize pushbutton, W/S 0 will display the following:

   CONTROL MODE R00

2. a. If R00 (the default address) is the Physical Device Address (PDA) of the system disk (or the IPL disk), press ENTER to IPL.
   b. If R00 is not the desired PDA, press the BACKSPACE key and enter F (for a fixed disk) or R (for a removable disk).

   Calculate the PDA as follows:

   (1) Determine the BA, IOP, and Port numbers of the system disk.
   (2) Construct an 8-bit word as follows:

   BIII PPPP

   Where: B = 0 for Bus Adapter (BA)

   III = 000 for IOP 0
   = 001 for IOP 1
   = 010 for IOP 2
   = 011 for IOP 3
   = 100 for IOP 4
   = 101 for IOP 5

   PPPP = 0000 - 1111 for devices 0 thru 15

   3) In the example below, if the disk is located on IOP 1, Port 3, the 8-bit word is 0001 0011. Converting this to HEX gives a PDA of 13.

	BA	IOP#	PORT
BIT POSITION	0	123	4567
8-BIT WORD	0	001	0011
HEX RESULT		1	3

   The LOAD command would then read: CONTROL MODE R13.

   c. Enter the correct PDA into the LOAD command and press ENTER.

3. The OS from the specified disk will now be loaded (IPLed) into Main Memory.

4. After the Control Mode screen is serviced and the system is IPLed, a request for configuration file and library names is displayed. (If this is the first time the system was IPLed, they should be blank.)

   a. If system has previously been IPLed, the default can be accepted by pressing ENTER.
   b. The default can be modified by entering a different file name.
   c. A minimum configuration file of 1 workstation and 1 disk can be requested by pressing PF1.

The configuration file must be on the volume which will be used as the system volume. Once the configuration information is entered, the system is generated.

5. After System Generation, W/S 0 will display a request to set the date and time. Beneath the date and time entries is the memory size block which specifies the maximum memory size that can be used by the generated OS.

   a. Specified values must be in multiples of 1024K.
   b. The lowest allowable value is 1024K
   c. The maximum allowable value for the VS-85/85-H is 4096K.

   The system will default to the memory size specified by the switch settings on the 210-8230 Memory Controller I board (see Chapter 5). If the memory size must be changed for any reason, enter the size of memory desired (must not be higher than actual memory size). If a memory size value is specified without the necessary RAM to support it, the system will NOT run.

   The Control Sta ement for MEMORY should appear typically as follows:

   MEMORY SIZE = 1024K

6. After the date, time, and memory size have been entered, press ENTER and the system will begin the initialization. When complete, the Operators Console screen will appear (if this is W/S 0). Press PF1 and the following will appear on the workstation:

```
                    ***    Wang VS Logon    ***

Workstation  0  Ready      12:34 pm      Wednesday October 31, 1984

                           Hello New User

  Please Identify Yourself by Supplying the Following Information:

                          Your USERID    =
                          Your PASSWORD  =

                     and Press (ENTER) to Logon

            or Press (11) to Enter Operator Mode Immediately
```

NOTE

If the system will not IPL properly, go to paragraph 4.12 and perform the COLDSTART procedure using the REFORMAT option, then reIPL. If the system still does not IPL, repeat COLDSTART and select the INITIALIZE option, then reIPL again. Otherwise, continue with the SYSGEN procedure below, if desired.

4.11 SYSTEM GENERATION (SYSGEN)

These paragraphs give a brief overview of the System Generation (SYSGEN) processes used on the VS-85/85-H system. For a detailed explanation of SYSGEN, refer to VS Release 6.30 SYSGEN Procedure, WLI P/N 800-XXXXSP-XX and VS Software Bulletin, Release 6.30, WLI P/N 800-XXXX.)

SYSGEN is the construction of a system configuration specifically tailored to the installation. A SYSGEN is performed by modifying, according to user demands, the basic configuration loaded into the System Generator. As with all VS systems, the VS-85/85-H uses a dynamic SYSGEN procedure that simplifies the creation of a unique Operating System (OS). The dynamic SYSGEN, using the GENEDIT utility, allows the user to easily change system configurations. These changes can be a one-time modification of the resident Configuration (CONFIG) file, which is lost at the next system IPL; or the building of a new configuration at IPL time, which can be stored on disk for future use.

GENEDIT allows definition of a configuration file. GENEDIT is a menu-based, interactive utility which prompts the user, through a series of screen displays, to select IOPs, the position of devices on the IOPs, and the type of devices on the system. GENEDIT then automatically defines the configuration file. GENEDIT is run on line through the RUN command (PF Key 1) of the Command Processor at any time after the system is IPLed, while other users are on the system. **When using GENEDIT to configure the system, enter device type "2268V1" for the 76 MB NEC drive, and "2268V2" for the 147 MB NEC drive.**

4.12 COLDSTART UTILITY

VS COLDSTART, a stand-alone utility, is used to operate a VS system without a standard system disk or operating system. Its primary purpose is to bring up a system by formatting the system disk and copying a minimum system to it in the event that a new system will not IPL or in case of a system crash.

NOTE

COLDSTART utilizes the six floppy diskettes produced at the District Office during the COLDBILD procedure. If these diskettes have not been generated, refer to paragraph 4.13 and perform the COLDBILD procedure.

There are two modes of COLDSTART operation: the Copy mode and the Backup mode.

4.12.1 COPY MODE

In the Copy mode of COLDSTART, there are three ways to copy data from the input diskettes to the system volume:

- o Initialize the system volume before copying the data.
- o Reformat the system volume before copying the data.
- o Copy only those files you want to add or with which you wish to update the system.

The first method, INITIALIZE, is used to bring up a system when the disk has not already been initialized.

Method two, REFORMAT, is used to bring up a system when the disk has already been initialized. Reformatting clears the volume of existing data and rewrites the volume table of contents (VTOC). This method is required when the system volume is not media-tolerant in order to protect the VTOC in case the disk fails.

The third method, COPY only, allows the user to load system files without reconstructing the entire system. COLDSTART checks for duplicate file names, flags them, and permits you to skip the input file or rename either the old or the new file.

4.12.2 BACKUP MODE

The COLDSTART Backup mode should be used when you can read but not IPL from the system disk. By running the Backup mode prior to reformatting, undamaged data resident on the volume can be preserved. Since Backup is not used during installation, it will not be further described here.

4.12.3 PREPARATION

The following steps are required to prepare the VS-85/85-H to run COLDSTART:

1. Power down the mainframe.
2. Attach a serial workstation to IOP 2, Port 0. This device is workstation 0 (W/S 0).
3. Connect a disk drive to IOP 0, Port 0.
4. Power up the system.
5. Load the microcode into Control Memory by inserting the microcode diskette into the mini-diskette drive, closing the drive door, and pressing the CM Boot button on the Display Panel. (See figure 4-12.) The Diskette Activity LED on the front of the mini-diskette drive lights to show that the drive is in use. When the Diskette Activity LED goes out and the Ready LED on the Display Panel lights, the load is finished.

NOTES

1. If the Ready LED flashes instead of remaining steadily ON, the system has failed to load the microcode. Reseat the diskette and repeat the loading procedure. If the microcode cannot be loaded, insert and load the backup diskette, if available. If this does not correct the problem, Control Memory, the drive, or drive controller (210-7610) may be defective. Refer to drive maintenance procedures in Chapter 5.

2. Also, the CP (Control Memory) Parity LED or the CP Halt LED may light during a microcode load operation. Ignore these displays during the load operation. Neither indicator reflects a valid trouble condition until after the VS-85/85-H is initialized.

Press the Initialize button. Both the CP (Control Memory) Parity and CP Halt LEDs should go out.

6. Load the read/write heads on the external disk drives by pressing the START button on the front panel of the drives. Wait at least five seconds before pressing the START button of the next drive.

7. Press the Control Mode button on the Display Panel. Then press the Initialize button on the Display Panel. After pressing the Initialize button, W/S 0 will display the following:

   CONTROL MODE R00

8. a. If R00 is the Physical Device Address (PDA) of the system disk (or the IPL disk), press ENTER.
   b. If R00 is not the PDA, press the BACKSPACE key and enter F (for a fixed disk) or R (for a removable disk) and the correct PDA of the system disk (or the IPL disk) and press ENTER.

   Calculate the PDA as follows:

   1) Determine the BA, IOP, and Port numbers of the system disk.
   2) Construct an 8-bit word as follows:

      BIII PPPP

      Where: B = 0 for Bus Adapter (BA)

      III = 000 for IOP 0
      = 001 for IOP 1
      = 010 for IOP 2
      = 011 for IOP 3
      = 100 for IOP 4
      = 101 for IOP 5

PPPP = 0000 - 1111 for devices 0 thru 15

3) In the example below, if a removable disk is located on IOP 1, Port 3, the 8-bit word is 0001 0011. Converting this to HEX gives a PDA of 13.

	BA	IOP#	PORT
BIT POSITION	0	123	4567
8-BIT WORD	0	001	0011
HEX RESULT		1	3

The LOAD command would then read: CONTROL MODE R13.

c. Enter the correct PDA into the LOAD command and press ENTER.

9. Insert the FORMAT diskette and proceed with the COLDSTART process below.

4.12.4 RUNNING VS COLDSTART

1. The first screen that appears on W/S 0 (the COLDSTART System Disk Specification screen, below) requests the output device type and the physical device address (PDA) in HEX. Refer to the table at the bottom of the screen for a list of device types and descriptions.

```
                    *** Wang VS Coldstart ***



      Please specify the system disk and press ENTER.

           Device Type                       - ********
           Physical Device Address (Hex)     - ****
```

Device Type	Description	Device Type	Description
2265V1	75 Meg Rem Disk	2265V2	288 Meg Rem Disk
2280V1F	30 Meg F/R Disk (F)	2280V1R	30 Meg F/R Disk (R)
2280V2F	60 Meg F/R Disk (F)	2280V2R	60 Meg F/R Disk (R)
2280V3F	90 Meg F/R Disk (F)	2280V3R	90 Meg F/R Disk (R)
2265V1A	75MB R Dual Port Dk	2265V2A	288M R Dual Port Dk
2265V3	620M R Dual Port Dk	Q2040	34 MB Fixed Disk
2268V2	147 MB Fixed Disk	2268V1	76 MB Fixed Disk

NOTE

COLDSTART works with any drive. However, a system bootstrap must be done from a diskette or the removable part of a fixed/removable disk.

2. Enter the device type and the PDA and press ENTER to continue. W/S 0 displays the COLDSTART Main Menu.

```
                    *** Wang VS Coldstart ***



          Press PF4 to COPY to system disk, or
                PF5 to BACKUP the system disk.
          Press PF1 to return to the previous screen.
```

3. Press PF4 to enter the COPY mode. W/S 0 displays the COLDSTART Select Copy Mode screen shown below.

```
                    *** Wang VS Coldstart ***



          Press PF2 to INITIALIZE the system disk,
                PF3 to REFORMAT the system disk, or
                PF4 to COPY only.
          Press PF1 to return to the previous screen.
```

NOTE

If this is the first time through the COLDSTART procedure, perform the REFORMAT procedure in paragraph 4.12.4.1 below. If the system disk has already been reformatted and did not IPL properly, perform the INITIALIZE procedure in paragraph 4.12.4.1.

4.12.4.1 REFORMAT And INITIALIZE Procedures

1. Press PF3 to select REFORMAT or PF2 to select INITIALIZE. (See note above.) W/S 0 displays the COLDSTART System Disk screen (shown below) for either selection.

```
                  *** Wang VS Coldstart ***

                         System Disk

   The following information is required for volume formatting:

        Volume Name                  - ******
        Volume owner                 - **************
        Date (MM/DD/YY)              - ** / ** / **
        VTOC size (in blocks)        - 112

        Please supply the required parameters and press ENTER.
        Or press PF1 to return to the mode selection screen.
```

2. Enter the requested information and press ENTER. W/S 0 displays the COLDSTART Control Mode Dump and Paging Files screen below.

```
                  *** Wang VS Coldstart ***



          Size of preallocated dump file   = 00000 K

          Size of paging pool              = 00000 K
          Pool location (relative to VTOC) = 0
               0 = Nearest VTOC
               9 = Farthest from VTOC

          Please supply the required parameters and press ENTER.
```

NOTE

For information on control mode dump and paging pools, refer to the VS System Operator's Reference (WLI P/N 800-1102-08) and the VS System Utilities Reference (WLI P/N 800-1303-04), respectively.

3. Enter the requested information and press ENTER. W/S 0 displays the message "Disk Formatting in Progress."

4.12.4.2 COPY Procedure

When REFORMAT or INITIALIZE is complete, COLDSTART requests that you mount the first diskette (SYST01) to be copied. As each diskette is copied, W/S 0 prompts you to mount the next diskette in sequence. The COPY program obtains the name of the next diskette to be mounted from the current one and displays: "All files in this diskette have been copied. Please mount ******," where "******" is the name of the next diskette.

After the last diskette has been copied, W/S 0 displays "IPL when ready." Go to paragraph 4.10 to perform the normal IPL procedure.

4.13 COLDBILD PROCEDURE

COLDBILD is a user-friendly procedure designed to aid the Wang-trained CE in building COLDSTART diskettes for CP3, CP4, and CP5-based systems from official release tapes. This procedure should be done at the District Office.

4.13.1 REQUIREMENTS

The following hardware and software are necessary for the implementation of the COLDBILD Procedure.

4.13.1.1 Hardware

- o VS archiving workstation
- o Six double-sided, double-density (DSDD) 8" diskettes

4.13.1.2 Software

- o Release tape with library COLDPROC, containing the program COLDNAME as well as the procedures COLDBILD, NO5SOCB, NO4SOCB, and NO3SOCB.

- o OS 6.20 or greater with VS Procedure Interpreter version 3.00.05 or greater, minimum BACKUP version of 5.00.23, and minimum DISKINIT version of 5.04.28 in @SYSTEM@ on the system volume.

- o An input disk volume containing the following input libraries found on the release tape:

  @COLD25@ - COLDSTART library
  @SYSTEM@ - Operating system files for CP4

NOTE

The correct contents of the above libraries are displayed in the procedure. Be sure to check the availability of all necessary files before running the procedure.

4.13.2 RUNNING COLDBILD

1. Restore the release tape containing the OS software to a hard disk with a minimum free space of 15 MB. (For details of the RESTORE utility, see the VS System Operation Guide WLI P/N 800-1102-07.)

2. Verify the release levels of software as listed in the Software Release Notice (SRN) for CP4.

NOTE

Failure to perform step 2. may cause undesirable results.

3. Run COLDBILD in COLDPROC on the restored volume.

   a. Enter the restored volume name and the device number of the archiving workstation.

   b. Press the proper PFKey for the desired function and follow the screen prompts.

NOTE

COLDBILD also provides INITIALIZE and REFORMAT options before building diskettes.

4.13.3 MECHANISM

The following table describes the actions of COLDBILD.

Table 4-4. COLDBILD Operation

INPUT LIBRARY	COLDBILD ACTION	OUTPUT VOLUME/LIBRARY
@COLD25@	All files copied; library renamed	@SYSTEM@
@DIAGST@	All files copied	@DIAGST@
@SYSTEM@	Microcode files copied	@SYSTEM@ SYST01, SYST02, SYST03, SYST04, SYST05
@SYSTEM@	Minimum OS copied	@SYSTEM@
@DIAGST@	All files copied	@DIAGST@
@DIAGMN@	All files copied	@DIAGMN@ @SYSWORK@ (This library is created by BACKUP for multi-volume RESTORE.)

4.13.4 OUTPUT

The output of the COLDBILD procedure is six media-tolerant DSDD diskettes as listed below.

FORMAT - The first diskette contains the COLDSTART program, @COLD25@. This program is used to copy files from a set of diskettes to a fixed disk or backup files from a hard disk to a DSDD floppy without OS control. (See the COLDSTART procedure in paragraph 4.12.)

SYST01-05 - COLDBILD creates five system diskettes (SYST01, SYST02, SYST03, SYST04, and SYST05) which contain a minimum IPLable VS OS and several necessary utilities (GENEDIT, SECURITY, and BACKUP).

4.14 SYSTEM INTERCONNECTION

After the microcode is loaded and SYSGEN has been run, power down the mainframe and connect all peripheral devices according to the configuration created during SYSGEN. See figures 4-13 through 4-19, the following paragraphs, and appropriate documents in Class 3000 for cabling procedures.

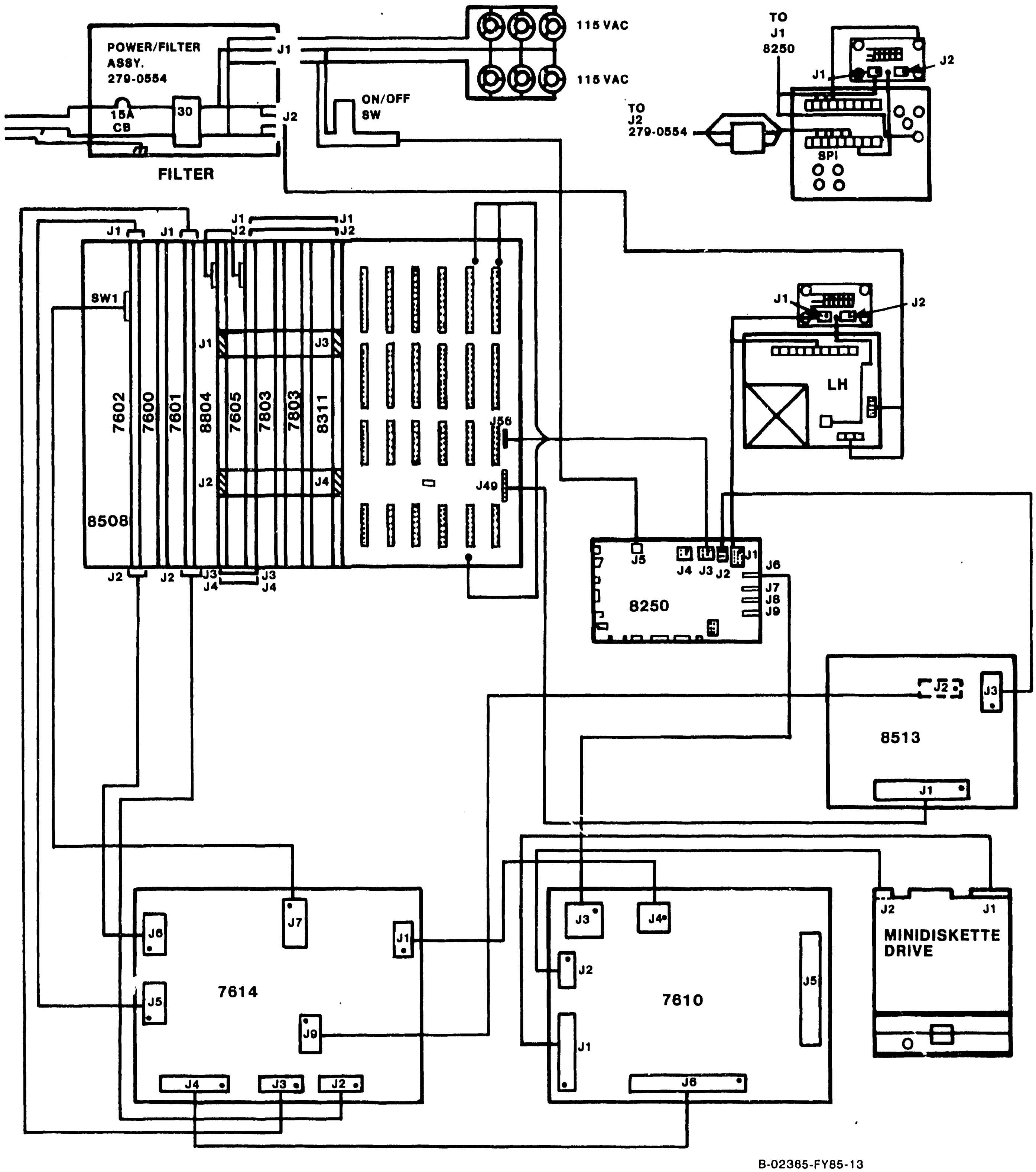


Figure 4-13A. VS-85 System Interconnection Diagram

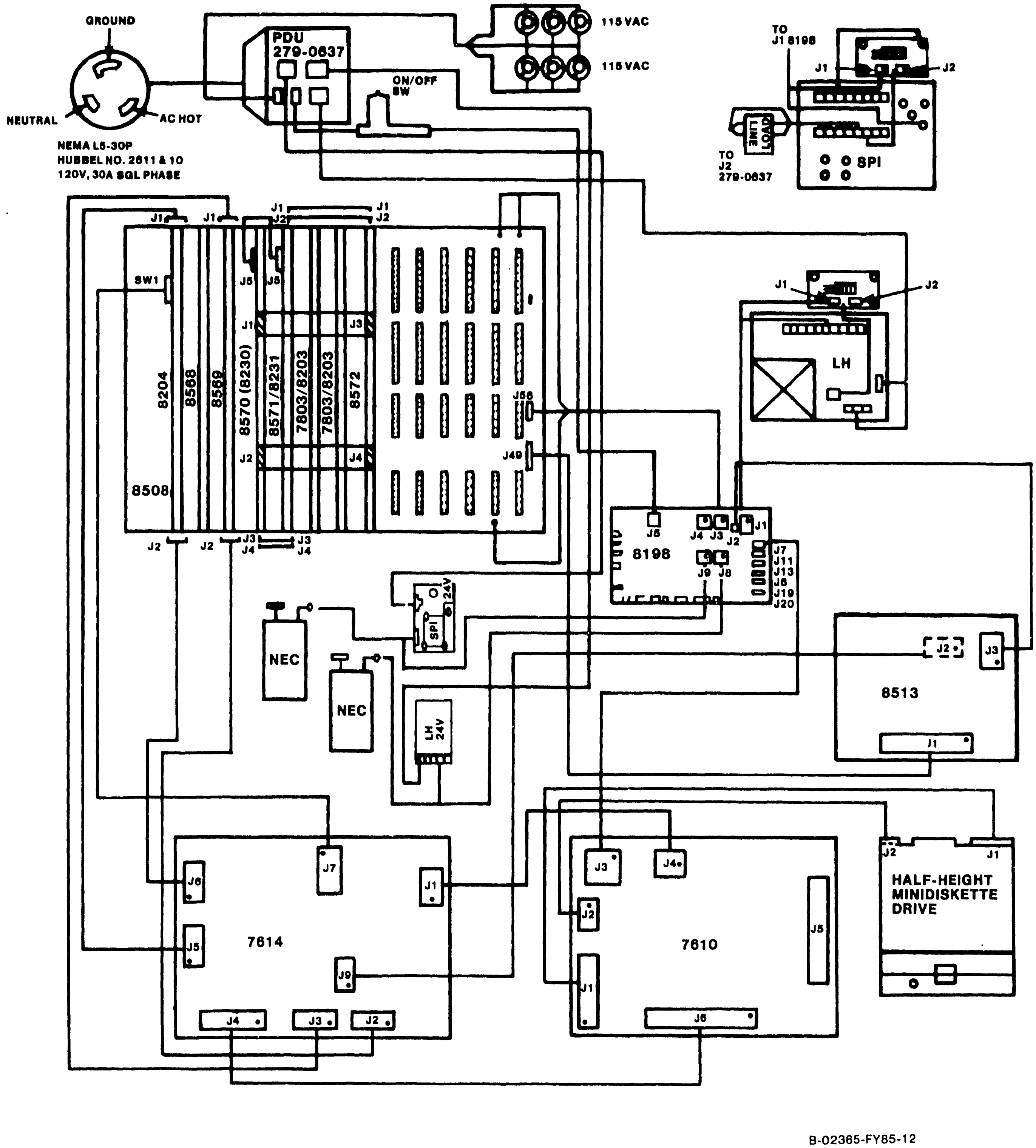


Figure 4-13B. VS-85-H System Interconnection Diagram

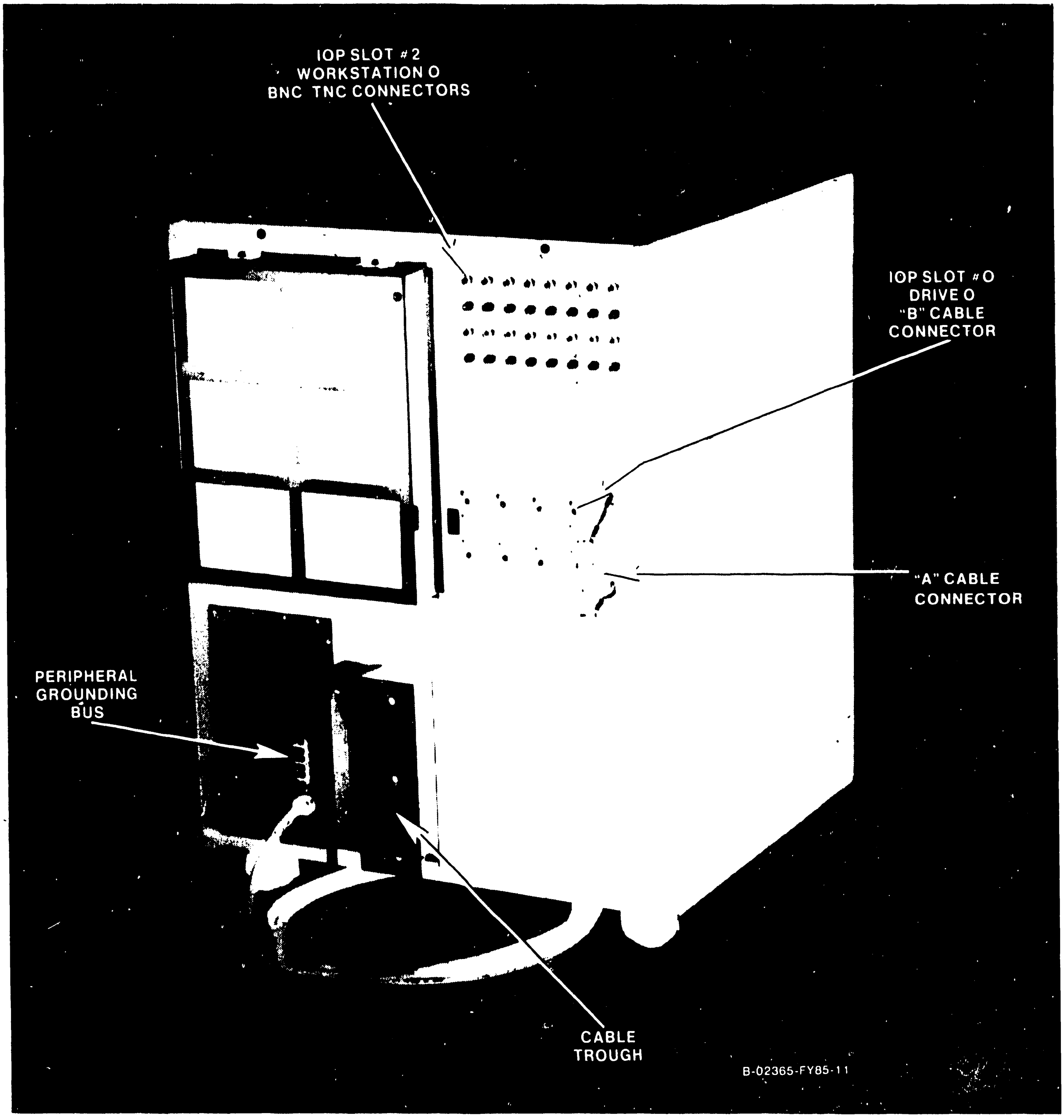


Figure 4-14. VS-85/85-H Rear Panel Connector Plate Locations

4.14.1 CONNECTOR PLATE-TO-IOP CABLING

Before installing cables in the connector plates at the rear of the mainframe, check all cables between the plates and associated IOPs. Make sure that the cable from the connector plate containing workstation 0 connects to J1 of the Serial IOP assembly in IOP slot 2. Make sure that the "B" cable of the system disk is attached to the "B" cable connector next to the "A" cable connector of the disk connector plate for IOP slot 0. The "B" cable from this connector plate must be connected to J2 of the Disk IOP assembly in IOP slot 0.

4.14.2 BNC/TNC CONNECTORS

Serial I/O devices (workstations, printers, etc.) connect to the mainframe by means of standard BNC/TNC connectors mounted on 16-connector plates (WLI P/N 270-0704). Maximum cable length for these devices is 2000 feet. Workstation 0 MUST be attached to Port 0 on IOP #2. The connectors for Workstation 0 are located in the left corner of the top connector plate on the rear of the mainframe. See figure 4-15.

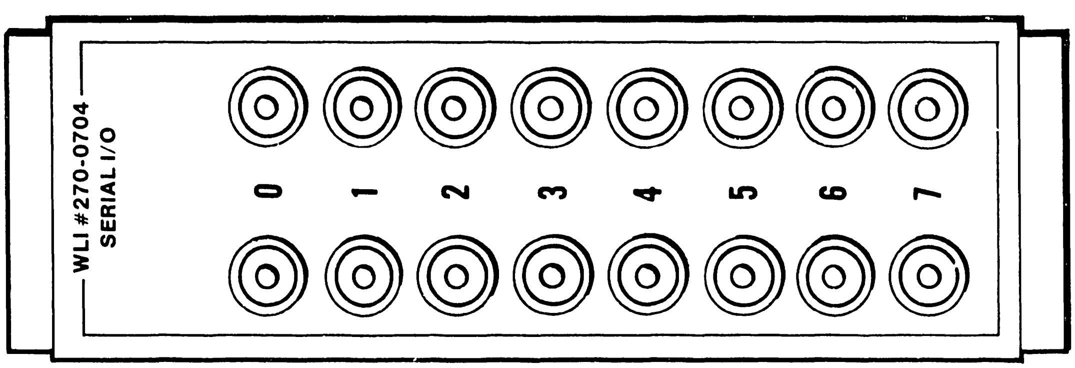


Figure 4-15. BNC/TNC Connector Plates

4.14.3 DISK CABLE CONNECTORS

Two sizes of disk cable connectors and clamps are located on the disk connector plates (WLI P/N 270-0910). The left four (narrow) connectors contain 26-pin sockets for the "B" cable connections; the right (wide) connector contains a 60-pin socket for the "A" cable connection. Both types connect the disk cable to the mainframe in the same manner.

Before connecting an external disk cable, prepare it as follows, if necessary:

1. Remove 6 inches of plastic sheathing from one end of the cable.
2. Fold the copper shield back exposing the disk cable.

Connect the disk cables to the mainframe as follows: (See figures 4-16A and 4-16B.)

1. Disassemble the cable clamp by removing the Phillips screws on either side of the clamp.
2. Lay the copper shielded section of the external disk cable against the piece of the clamp still attached to the mainframe.
3. Reassemble the cable clamp by installing the two Phillips screws removed in step 1. Make sure that pin 1 of the cable is oriented properly and tighten the clamp screws until solid contact with the copper shield is made. <u>DO NOT</u> overtighten, as this could damage the disk cable.
4. Plug the cable into the cable connector on the disk connector plate. The four left connectors of each disk connector plate attach the "B" cable of each drive; the right connector on the plate attaches the "A" cable daisy-chained through each drive to the VS-85/85-H mainframe. The "B" cable connector next to the "A" cable connector attaches to Port 0 of the associated IOP.

NOTE

Sector switch settings for the VS-85/85-H on the 2265V-1/V-2 disk drives are the same as the VS-60/80/100. Refer to the VS Reference Summary (WLI P/N 729-0716) for switch settings.

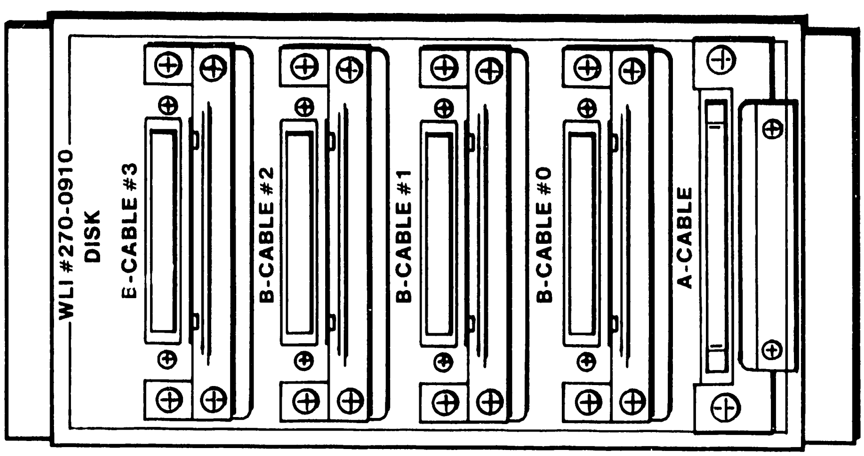


Figure 4-16. VS-85/85-H "B" and "A" Cable Connections

4.14.4 TELECOMMUNICATION CONNECTORS

If the TC option is to be installed, the TC cables must be attached to a an RS-232 connector plate (WLI P/N 270-0705 for 1-port, 270-0705-2 for 2-port, 270-0705-3 for 3-port) at the rear of the mainframe. This plate supports as many as three TC connections, providing plugs for both the modem and Automatic Calling Unit (ACU) cables for each installation. This connector plate then attaches to a 22V26-series TC IOP. The left connectors (modem and ACU cables) on this plate attach to Port 1, the middle connectors attach to Port 2, and the right connectors attach to Port 3. (See figure 4-17.)

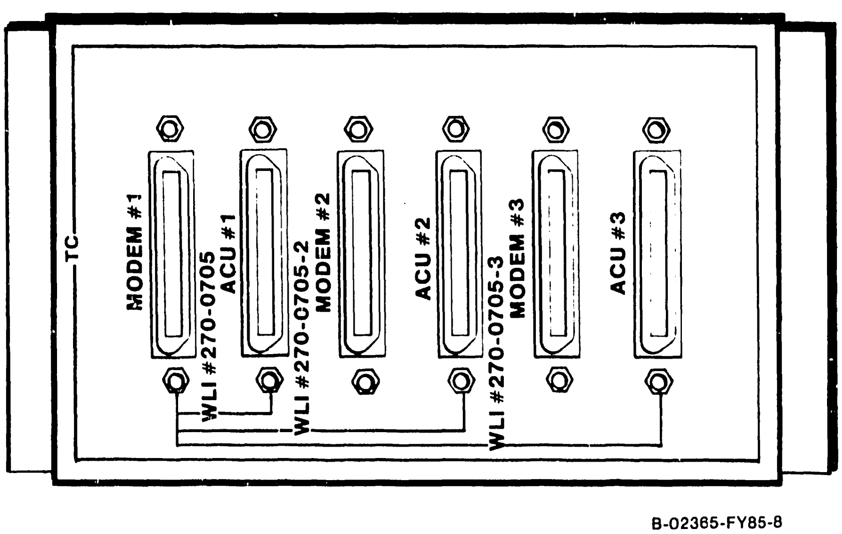


Figure 4-17. Telecommunications Connector Plate

4.14.5 TAPE CABLE CONNECTORS

Two types of tape connector plates are available to attach magnetic tape drives to the mainframe. The two types of tape connectors are: Kennedy tape drive plate (WLI P/N 270-0911) and Telex tape drive plate (WLI P/N 270-0741).

For the Kennedy tape drive, two sockets are located on the plate for attachment to the drives. The left socket receives the data cable and the right socket receives the control cable. Note the orientation of the cable plug when inserting it into the socket. See figure 4-18.

For the Telex tape drive, three sockets are located on the plate for attachment to the drives. The left socket (I/O #1) receives the control cable, the middle socket (I/O #2) receives the data cable, and the right socket (I/O #3) receives the status cable. Note the orientation of the cable plug when inserting it into the socket. See figure 4-18A.

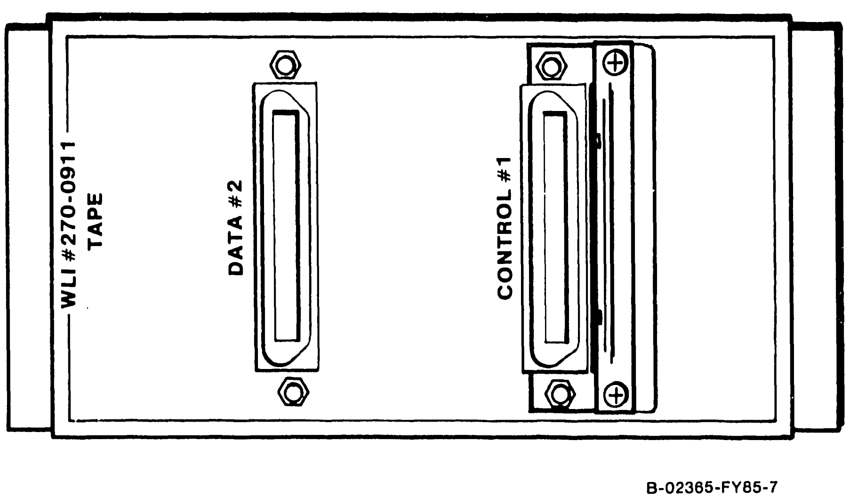


Figure 4-18. Kennedy Tape Cable Connections

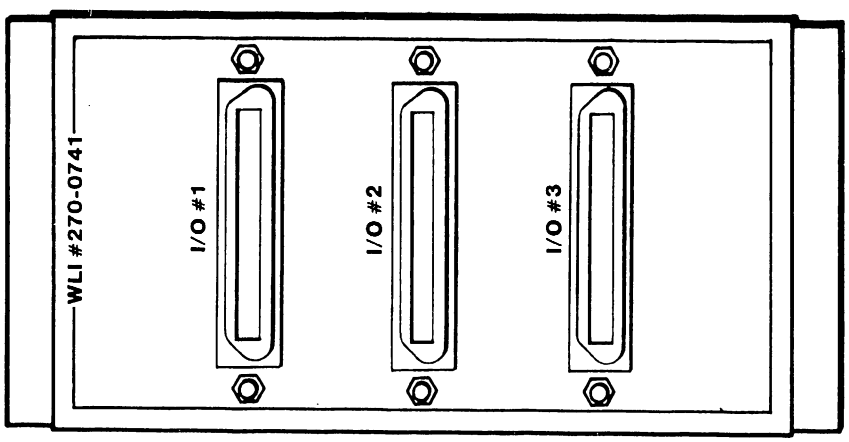


Figure 4-18. Telex Tape Cable Connections

4.14.6 INSTALLING THE ARCHIVING WORKSTATION

All VS-85/85-H systems are equipped with an Archiving Workstation (VS-AWS) as standard equipment. The VS-AWS, which consists of an Archiver Terminal and an Archiver Master Unit, provides the user with remote batch storage facilities that allow the archiving of WP documents (when used with suitable software and a "C"-type keyboard), the storing and processing of VS/DP files, and the usage of IBM compatible diskettes.

The VS-AWS connects to the VS-85/85-H through a WLI P/N 120-2300 paired coax signal cable assembly of up to 2000 feet in length, connecting to one port of a 22V27 Serial IOP assembly (see figure 4-19). The only restriction when connecting a VS-AWS is that the two devices making up the Archiver must be assigned to consecutive device numbers on a common port with the Archiver Terminal ("S" or "C" workstation) assigned to the first number and the Disk Unit assigned to the second number. Refer to Chapter 5 for IOP switch settings on the VS-85/85-H. Refer to Class 3403 for more detailed information concerning the AWS-1.

NOTE

If the AWS-1 is used as W/S 0, the WP function cannot be used.

4.14.7 CIU/WANGNET INSTALLATION (22V67W)

The VS-85 modem mounting bracket (WLI P/N 452-4566) may be placed in one of the two I/O full panel positions.

The VS-85-H modem mounting bracket (WLI P/N 452-0382) is positioned against the inside of the left-hand side panel with existing screws.

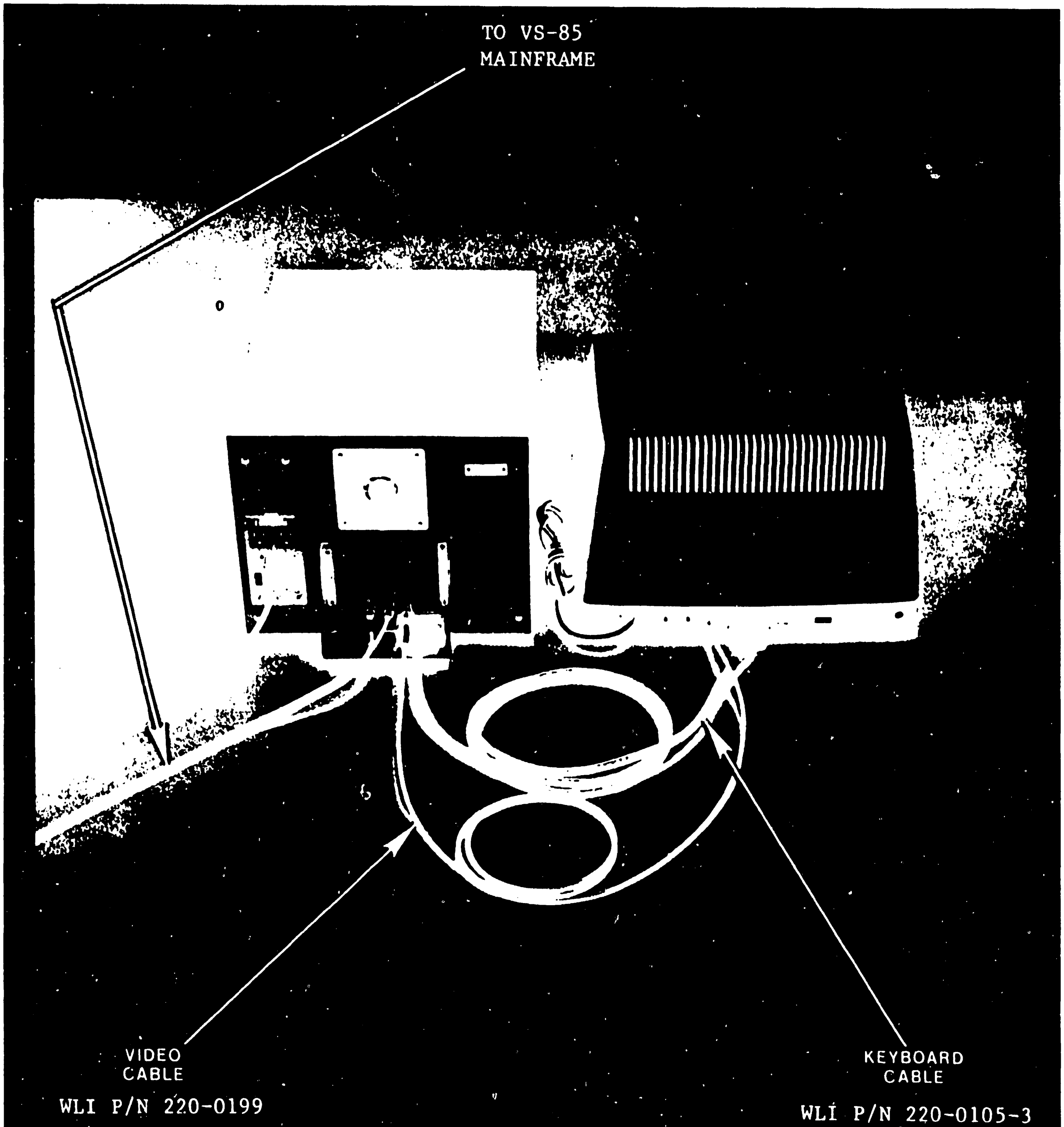


Figure 4-19. Connecting the Archiving Workstation

4.15 SYSTEM CHECKOUT

At this point, all peripherals should be installed and attached to their respective IOPs. Before proceeding, perform the following checkout procedure:

1. Visually inspect all mainframe circuit boards for the proper cabling configuration. (Table 5-2.)
2. Visually inspect all peripheral devices to make sure that I/O cabling is correctly installed, all switch settings are correct, and all covers and panels are in place.
3. Make sure that all devices are powered off.

4.16 ON-LINE CHECKOUT

Begin the on-line checkout procedure by first confirming that the system configuration is correct according to the work request, with all peripherals connected to their respective IOPs. Once this is done, the checkout procedure continues by successively powering up and verifying the functional integrity of different elements of the system, and then running all applicable diagnostic test programs to verify the operation of each element. If results do not occur as described during performance of any step, perform appropriate system level troubleshooting procedures.

1. To make sure that the addition of peripheral equipment has not affected operation of the CP, execute the CP4 Microcode diagnostics.
2. After successfully completing these diagnostics, load the system microcode into Control Memory and IPL the system.
3. At the System Console, run PRTEST from the library @SYSTEST@. Running this test successfully indicates that normal communications are taking place between the CP and the printer. (Refer to paragraph 4.16.2.)
4. Turn on all workstations.
5. Clear workstations by pressing the green LOAD button on the VS-85/85-H.

4.16.1 DISK DRIVE CHECKOUT

After completing the previous procedure, power up all remaining peripherals, including all disk drives.

1. Mount the CE OS pack on a selected disk drive.
2. Mount a scratch pack on any other drive, if installed. Bring drive(s) up to a ready state and IPL the system from the CE OS pack.
3. Workstation 0 will display a prompt menu requesting the date, time, and the size of main memory. Type in the requested information and then press the ENTER key.
4. Make sure that the generated OS matches the actual system hardware configuration.
5. Perform initialize and compatibility checks on systems with a single 75/288 megabyte disk drive attached as follows:
   a. Using the stand-alone VERIFY option of the INITDISK program from a diskette mounted in the Archiving Workstation, verify the CE OS pack. The VERIFY sequence should complete with no errors.
   b. Next, mount a CE scratch pack and use the INITIALIZE option of the INITDISK program to initialize the scratch pack. Following completion of the initialization process, run VERIFY on the pack.

The system should complete both of these functions without error.

c) Mount a CE OS pack and IPL.

6. Perform initialize and compatibility checks on multiple disk systems as follows:

NOTE

No I/O failures should be reported in the system Error Log list during performance of the following steps.

a. Execute the DISKINIT program and use its INITIALIZE option to initialize the scratch pack mounted on the additional drive.
b. Following completion of the initialization process, verify the scratch pack using the VERIFY option of DISKINIT.
c. Dismount the scratch pack, mount it on the next drive to be checked, and repeat steps (a) and (b). Repeat this procedure until the INITIALIZE and VERIFY functions have been performed on all disk drives in the system.
d. Following initialization and verification of all disk drives, mount the scratch pack on one drive and mount a CE OS pack on another drive.
e. IPL from the second drive containing the CE OS, execute the DISKINIT program and use its VERIFY option to verify the CE scratch pack.
f. Following successful completion of the VERIFY function, perform both INITIALIZE and VERIFY operations on the drive containing the scratch pack.
g. Execute the BACKUP program to copy the active volume from the drive containing the scratch pack to the drive containing the CE OS. Following program completion, IPL from the CE OS drive by pressing the LOAD button on the front panel of the VS-85/85-H mainframe, and the ENTER key on the System Console.
h. Perform a VERIFY operation on the drive containing the CE OS.
i. Following completion of the VERIFY operation, dismount the system pack from this drive and successively mount and verify that pack on each drive in the system. This will check compatibility between all disk drives.

4.16.2 PRINTER CHECKOUT

Check out all printers attached to the system as follows:

1. At the System Console, release all printers from the System Spooler as follows:
   a. Select the CONTROL PRINTERS display (PF3).
   b. Move the cursor to the desired printer and press PF6. The system should respond with a prompt menu designating the following options for the selected printer:
      (1) Return to Main Status Display
      (7) IDLE
      (9) Release Printer
      (11) Change Form #

c. Press PF9 to release the printer.

2. After the printer is released, execute the PRTEST diagnostic from the @SYSTEST@ library. (PRETEST will not run on a printer that is registered as being in use by the System Spooler.)
   a. Press PF1 to print the character set "ripple one character at a time".
   b. After several pages have printed, terminate the PRTEST program and acquire the printer by pressing PF10.
   c. Check print quality on the resulting printout.
   d. Repeat the PRTEST sequence for all printers attached to the system.

4.16.3 TAPE DRIVE CHECKOUT

Check out all tape drives attached to the system as follows:

NOTE

> No I/O failures should be reported in the system Error Log list during performance of the following steps.

1. Mount a CE scratch tape on a tape drive.
2. Run the TPTEST diagnostic from the @SYSTEST@ library. Perform the Miscellaneous Tests routine (PF5) a minimum of 20 times.
3. Following completion of the test passes, dismount the CE tape and mount it on another tape drive, if installed.
4. Repeat steps 1 and 2, continuing until the operational integrity of all tape drives in the system has been confirmed.

4.16.4 WORKSTATION CHECKOUT

Check out all workstations attached to the system as follows:

NOTE

> In order to check out all attached workstations simultaneously, the OS must be provided with valid User ID assignments for each terminal. If sufficient user IDs are not available, run the SECURITY program and add enough user IDs for every attached workstation (including any 2246R Remote Stand-alone Workstations but excluding the System Console).

1. Log onto the system at any data entry workstation.
2. Run WSTEST from the @SYSTEST@ library and test each alphameric key on the keyboard in the various operating modes. In addition, check the display for proper focus and character display in the following modes:

Low intensity mode	Blank mode
Numeric only mode	Nondisplay mode
Upper case mode	Lower case mode

3. Using the ERASE, INSERT and DELETE keys, test the operation of all alphameric workstation keys (expect for PF keys). To test lower case PF keys, access different functions from the Command Processor.
4. After testing all applicable keys at a given workstation, press the ENTER Key on that same workstation to allow the WSTEST program to continue automatically.
5. Repeat steps 1 through 4 on all other attached workstations. Continue testing until all keys on each workstation have been checked, and WSTEST has run error-free on all workstations.

4.16.5 FINAL CHECKS

1. If not done during preinstallation procedure, attach a line analyzer (WLI P/N 727-0135) to the VS-85/85-H mainframe power source to monitor ac power for transients, sags, surges, and dropouts.
2. Mount scratch packs on all additional disk drives attached to the system. Make sure that the CE OS pack is mounted on a disk drive.
3. WSTEST diagnostic program must be terminated at three or more data entry workstations in order to execute the following diagnostic programs and routines:

   o Perform COPY program(s) to exercise each disk.
   o PRTEST (maximum of two continuous hours for any one printer)
   o WSTEST (on remainder of workstations)

4. Run COPY program and make sure that the COPY program exercises all additional volumes on any multi-volume disk drive in the system. Finally, make sure that TPTEST can be run on all tape drives at the same time other programs are operating.
5. Except for PRTEST, which should never be run continuously on any one printer for more than two hours, allow the system to run with all diagnostic programs operating simultaneously on different peripherals for a period of at least eight hours.
6. If all of these tests are completed error-free, prepare the system for turnover to the customer. If any error indications have been discovered during the checkout sequence, isolate the failure condition through these of the diagnostic programs and normal troubleshooting procedures, repair that fault, and recheck the system.

4.17 CLOSE UP MAINFRAME

1. Make sure that all cables connected to CPU and IOP boards are securely attached.
2. Reinstall the top and front covers on the VS-85/85-H cabinet. (Refer to paragraphs 5.3.6.1 and 5.3.6.2)

4.18 DAILY SYSTEM POWER-UP/POWER-DOWN PROCEDURES

After all peripherals are connected to the mainframe, the power-up from a cold start and power-down procedures for the VS-85 system are as follows:

1. POWER-UP

   a. Make sure that the mainframe power connector is plugged into the power source receptacle.
   b. Turn on the mainframe ac On/Off circuit breaker.
   c. Depress the Power On/Off switch, located on the Display Panel, to the "1" position.
   d. Power up the primary disk drive and Workstation #0.
   e. Make sure that the system microcode diskette is in the minidiskette drive, and press the yellow CM Boot button.
   f. After successfully loading microcode, press the red Initialize button to begin loading the Operating System.
   g. Workstation 0 will display Control Mode R00. Press the BACKSPACE key and type in F (or R) and the Physical Device Address of the disk the system will be IPL'ing from.
   h. After successfully loading the OS, mount the disks and power up all peripherals.
   i. If this is a new installation, perform all applicable peripheral diagnostics. Refer to Chapter 8 of this document, the VS Service Program Guide, the VS Central Processor Microdiagnostic Test manual, and appropriate documents in Class 3000 for the necessary instructions. Make sure that all peripherals function correctly.

2. POWER-DOWN
   a. Make sure all operators have logged off of the system.
      1) Press PF key 13 (WORKSTATIONs) on an operators console to check that the operators have logged off of the system.
      2) Press PF key 7 (NONINTERACTIVE Tasks) on an operators console to check the background tasks on the system. Look under the "User" column to identify any operator running a background task.
   b. Press the blue Control Mode button. This prevents any disk I/O command in process from being halted prior to completion and prevents possible damage to any disk Volume Table of Contents (VTOC).
   c. Power down all peripheral devices according to procedures in the applicable documents in Class 3000.
   d. Depress the Power On/Off switch to the "0" position.
   e. Turn off the mainframe circuit breaker.

4.19 SYSTEM TURNOVER

1. Remove any scratch or Customer Engineering OS disk packs from the system disk drives.
2. Mount the customer's OS pack and perform an IPL from this pack.
3. Log on to a Workstation and use the Command Processor display functions to display the files in the @SYSTEM@ library on the customer's Operating System pack. Check through the listed files to make sure the presence of all customer-purchased options. If the BASIC compiler was purchased by the customer, for example, the following files should be present in the @SYSTEM@ library:
   a) BASIC
   b) WB1PASS1
   c) WB2PASS2

   If the COBOL compiler was purchased, conversely, the following files should be present:

a) COBOL
b) WC1PASS1
c) WC1PASS2

If the RPG compiler was purchased, only the following file should be present:

a) RPGII

4. Delete any of the above compilers not purchased by the customer from the related files using the Command Processor SCRATCH function.
5. Mount customer scratch packs on all additional disk drives. (The customer determines which packs will be scratch packs.) Perform a disk initialization procedure on each of the customer's scratch packs.

CAUTION

Make sure that the customer's scratch packs have no files on them before performing the initialize procedure. Also, demonstrate to the customer or to the responsible computer operator how the disk initialization procedure is performed. Include in the demonstration a description of disk drive operations - including loading and unloading of disk packs, emergency power-down of the disk drive, and disk drive fault recovery.

6. Perform the following Evening Shut-down Procedure and explain each step to applicable customer personnel:
   a. Make sure all workstations have been logged off.
   b. Press the blue Control Mode button on the VS-85/85-H front panel.
   c. Place all drives in the Load Mode condition (heads unloaded).
   d. Power down all workstations.
   e. Power down all printers.
   f. Unload and power down all tape drives.
7. Perform the following Daily Start-up Procedure and explain each step to applicable customer personnel:
   a. Bring all disk drives up to the ready condition.
   b. On Workstation #0, press the "X" key and then the ENTER key.
   c. Power on all other workstations and press the HELP key at each workstation (a LOG-ON screen should be displayed on each CRT).
   d. Power on all printers.
   e. Power on all tape drives.
8. Allow the customer to test the system using his programs. If the customer is satisfied with the operation of the system, officially turn the system over to the customer. (As of this printing, there is no official form to sign which effects turnover, nor has one been proposed. This should be merely a verbal notification given by the CE performing installation.)

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

CHAPTER 5

PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 GENERAL

This chapter consists of preventive maintenance requirements, adjustments, and removal and replacement procedures for field-replaceable components in the VS-85/85-H mainframe.

5.2 PREVENTIVE MAINTENANCE

Periodic maintenance is essential to the proper operation of the VS-85/85-H mainframe and associated peripherals. Because of its design, the mainframe requires a minimum amount of maintenance to ensure continued efficient operation.

5.2.1 TOOLS

TOOL DESCRIPTION	WLI P/N
Standard CE Tool Kit	726-9401
Alcohol Pads for R/W head cleaning	660-0130
Portable Vacuum	726-7131

5.2.2 TEST EQUIPMENT

TEST EQUIPMENT DESCRIPTION	WLI P/N
Digital Voltmeter - Fluke #8022B	727-0119
Oscilloscope - Tektronix 2445	727-0001

5.2.3 MATERIALS

No special materials are necessary to perform mainframe preventive maintenance.

5.2.4 PREVENTIVE MAINTENANCE SCHEDULE

Scheduled maintenance for the mainframe will be performed quarterly, and is as follows:

PROCEDURE	ITEM	NOTES
Inspect/clean	Mainframe filters	If necessary
Inspect	Mainframe interior	Look for dust & loose hardware. Clean.
Inspect/clean	Mini-diskette read/ write heads	Clean if oxide buildup seen. Paragraph 5.2.5
Inspect	Mainframe fans	Replace damaged fans. Paragraph 5.3.6.30
Check/adjust	Mainframe voltages	Paragraph 5.2.6.1
Run diagnostics	Mainframe & peripherals	Refer to Chapter 8 & Class 3000

NOTE

No preventive maintenance is required for the NEC disk drives in the VS-85-H.

5.2.5. CLEANING THE MINI-FLOPPY DRIVE HEADS

As part of the normal maintenance routine, the mini-diskette drive heads will be inspected for dirt or damage. If an oxide build up is seen during this inspection, the heads must be cleaned to ensure continued proper operation of the drive. Clean the heads as follows:

CAUTION

Cleaning methods and materials other than those specified below can permanently damage the head and must be avoided.

1. Remove the top and front covers. (Paragraphs 5.3.6.1 and 5.3.6.2.)
2. Remove the mini-diskette drive as described in paragraph 5.3.6.14.
3. Lift the load arm off the head, but do not to touch the load button.
4. With an alcohol pad (WLI P/N 660-0130), lightly wipe the head.
5. After the alcohol has evaporated, lightly polish the head with a clean, lint-free tissue.
6. Gently lower the load arm onto the head. DO NOT let the load arm snap back into place as this could permanently damage the drive head.

5.2.6 ELECTRICAL ADJUSTMENTS

5.2.6.1 Mainframe Voltage Adjustments

1. The following voltages should be checked at the 8250 Power Controller board test points (figure 4-8A) in the VS-85, and at the 8198 Power Sequencer board test points (figure 4-8B) in the VS-85-H.
2. Adjust the voltages to the test point readings (below) using the potentiometers on the front of the switching power supply (figures 4-9A through 4-9B).
3. The +5 Vdc adjustment for the LH supply can be done with the system powered up. However, due to the locations of the potentiometers, the -5, +12, and -12 Volts can't be adjusted with the system powered up. Measure the -5, +12, and -12 Volts at the 8250 Power Controller board or the 8198 Power Sequencer board test points; power down the system and adjust the potentiometer(s); power up the system and recheck the voltages. Continue this procedure until the voltage(s) is correct.
4. The +24 Vdc can be adjusted at R21 on the SPI 24-volt power supply and at R26 on the LH 24-volt supply in the VS-85-H (figures 4-10 and 4-11).

TEST POINT VOLTS	OPERATING LIMITS	AC RIPPLE LIMITS
+5.0	+4.9V to +5.1V	35mV RMS or 50mV Pk-to-Pk
+12.0	+11.9V to +12.1V	35mV RMS or 50mV Pk-to-Pk
-5.0	-4.9V to -5.1V	35mV RMS or 50mV Pk-to-Pk
-13.6	-13.5V to -13.7V	35mV RMS or 50mV Pk-to-Pk
+24.0 (VS-85-H)	+21.6V to +26.4V	170mV RMS or 240mV Pk-to-Pk

5.2.7 PERIPHERAL PREVENTIVE MAINTENANCE

Refer to the appropriate documents in Class 3000 for PM procedures for all VS-85/85-H associated peripherals.

5.3 CORRECTIVE MAINTENANCE

5.3.1 TOOLS

TOOL DESCRIPTION	WLI P/N
Standard CE Tool Kit	726-9401
8-inch clip lead	

5.3.2 TEST EQUIPMENT

TEST EQUIPMENT DESCRIPTION	WLI P/N
Digital Voltmeter - Fluke #8022B	727-0119
Oscilloscope - Tektronix #2445	727-0001
Diagnostic Panel - NEC DKU000-HLOG	**727-0317**

5.3.3 MATERIALS

MATERIAL DESCRIPTION	WLI P/N
System Microcode Diskette	Any version

5.3.4 ALIGNMENTS

5.3.4.1 Mini-floppy Drive Data Separator Adjustments

Because data and clock signals enter the Mini-diskette Drive Controller board combined in one signal called READ DATA*, the clock pulses must be separated from the data. This is done in the Data Separator circuit. The two separator pulses are outputs of a Voltage Controlled Oscillator (VCO), and must be in sync with READ DATA* for the Data Separator to work correctly. This procedure details the steps required to align the separator pulses with READ DATA*.

5.3.4.2 Preliminary Mini-floppy Drive Adjustment Procedures

Before adjusting the separator pulses, do the following:

1. Depress the Power On/Off switch to the "0" position.
2. Turn off the mainframe ac On/Off circuit breaker.
3. Remove the top and front covers from the mainframe. (Paragraph 5.3.5.1 and 5.3.5.2)
4. Insert the System Microcode diskette.
5. If a dual trace oscilloscope is being used, set it up as follows:
   a. Power up the oscilloscope.
   b. Set Volts/Division to 2 Volts.
   c. Set Time/Division to 1 microsecond.
   d. Set Slope negative.
   e. Set Source to Channel one.

f. Set coupling to DC.
g. Set AC-GND-DC to DC.
h. Set Vert. Mode to CHOP.
i. Make sure that probes are grounded.
j. Connect the clip lead from TP_3 (L19-6) to ground.
k. Connect probe 1 to TP_1 (L6-7). (Figure 5-1.)
l. Connect probe 2 to TP_2 (L6-9). (Figure 5-1.)

5.3.4.3 Performing the Adjustment

Adjust the Clock Separator pulse as follows:

1. The display obtained from TP_1 is the Clock Separator signal. The total waveform period must be 8 microseconds from the trailing edge of the first pulse to the trailing edge of the second pulse.
2. Adjust potentiometer R2 on the Mini-diskette Drive Controller board until the negative portion of the waveform is exactly six microseconds long. The positive-going portion of the waveform must be two microseconds long.
3. If an 8 microsecond pulse cannot be obtained, either the diskette is defective or the drive itself is bad. Try the adjustment procedure using a new mini-diskette. If no change in waveform occurs, replace the drive.

Adjust the Data Separator pulse as follows:

1. The display obtained from TP_2 is the inverse of the actual Data Separator pulse. The total waveform period of this pulse must be 8 microseconds from trailing edge to trailing edge.
2. Adjust potentiometer R1 on the Mini-diskette Drive Controller board until the negative portion of the waveform is exactly five microseconds long. This portion is the window that allows the data bits to be gated through the NAND gate. The positive-going waveform must be three microseconds long. It prevents Clock signals from passing through the NAND gate.
3. If an 8 microsecond pulse cannot be obtained, either the diskette is defective or the drive itself is bad. Attempt the adjustment procedure using a new mini-diskette. If no change in waveform occurs, replace the drive.

If a single trace oscilloscope is used, the procedures remain essentially the same. The oscilloscope settings must be changed, however, when going from TP_1 to TP_2. Refer to the settings given in paragraph 5.3.4.2.

5.3.5 NEC DISK DRIVE CORRECTIVE MAINTENANCE

The DKU000-HLOG Diagnostic Panel (WLI P/N 727-0317) is used to aid in the maintenance of the NEC disk drives. The Diagnostic Panel functions as a seek exerciser and fault logger when the disk is off-line and as a status monitor and fault logger when the disk is on-line. The logged data is retained for approximately 80 hours after the power supply is turned off. For detailed information on the operation and use of the Diagnostic Panel, refer to the NEC disk drive maintenance manuals, WLI P/N 729-1452 and 729-1503.

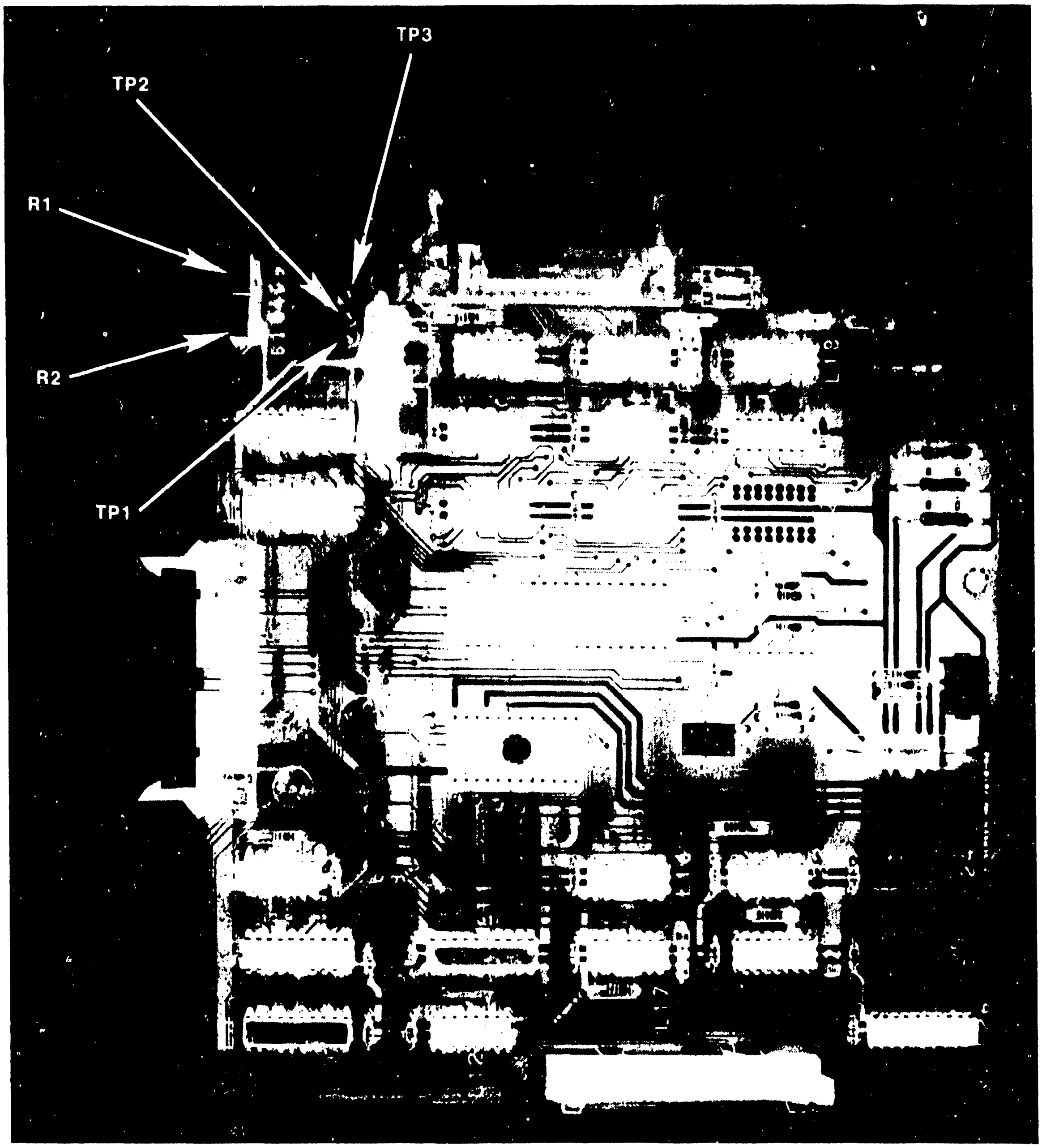


Figure 5-1. 210-7610 Mini-diskette Drive Controller Testpoint Locations

WARNING

```
****************************************************************
*                                                              *
*  THIS COMPUTER EQUIPMENT HAS BEEN VERIFIED AS FCC CLASS A.   *
*                                                              *
****************************************************************
```

IN ORDER TO MAINTAIN COMPLIANCE WITH FCC CLASS A VERIFICATION, THE FOLLOWING CONDITIONS MUST BE ADHERED TO DURING NORMAL OPERATION OF EQUIPMENT.

- ALL COVERS MUST BE ON SYSTEM AND SECURED IN THE PROPER MANNER.
- ALL INTERNAL CABLES MUST BE ROUTED IN THE ORIGINAL MANNER WITHIN THE CABLE CLAMPS PROVIDED FOR THAT PURPOSE.
- THE MAINTENANCE PANEL DOOR MUST BE KEPT CLOSED.
- ALL EXTERNAL CABLING MUST BE SECURED AND THE PROPER CABLE USED TO ENSURE THAT CABLE SHIELDING IS PROPERLY GROUNDED TO THE CABLE CLAMPS PROVIDED.
- MAKE SURE RFI GASKET FINGER STOCK (WLI P/N 654-2139) IS IN PLACE AND UNDAMAGED. (GASKET FINGER STOCK MAY BE ORDERED AND CUT TO PROPER LENGTH).
- ALL HARDWARE MUST BE PROPERLY SECURED.

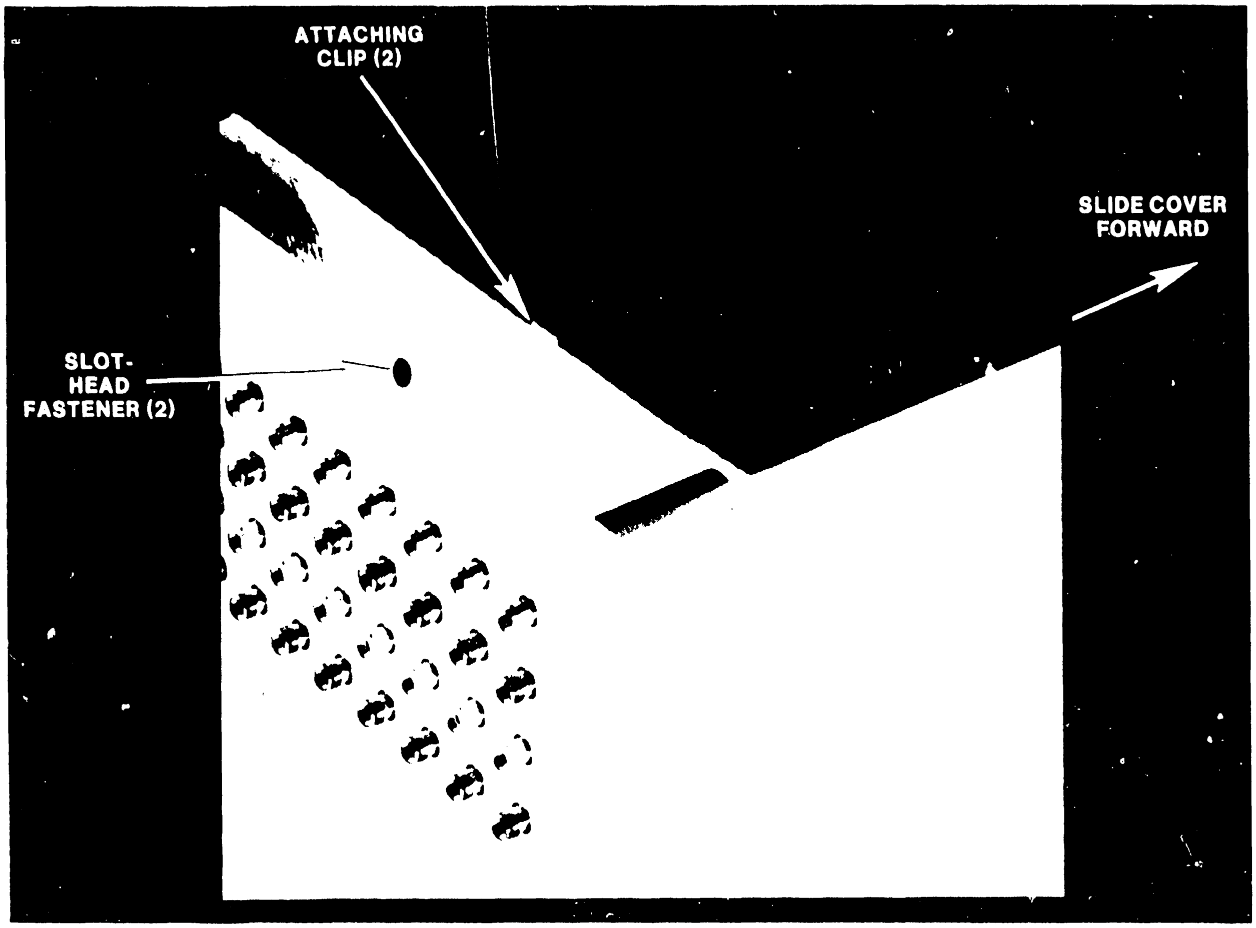


Figure 5-2A. Top Cover Removal

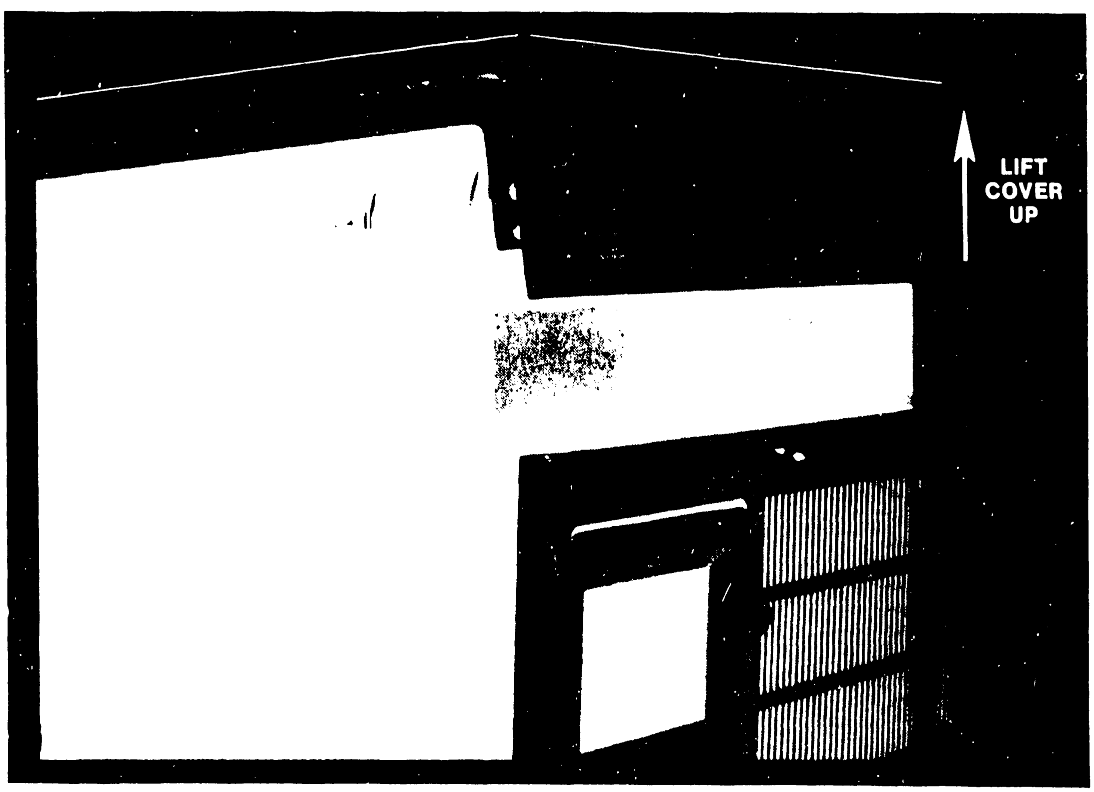


Figure 5-2B. Top Cover Removal

5.3.6 REMOVAL AND REPLACEMENT

These paragraphs describe the steps involved in removing and replacing or reinstalling all major field-replaceable components in the VS-85/85-H mainframe.

5.3.6.1 Top Cover Removal

Remove the top cover as follows: (See figures 5-2 and 5-2A.)

1. At the rear of the cabinet, two slot-head fasteners secure the top cover to the back panel. Using a wide-blade screwdriver, disengage the fasteners by turning them 1/2-turn counterclockwise.
2. With the fasteners free, slide the top cover 2-3 inches to the front to disengage the top cover from the front cover catch. This frees the top cover from the main cabinet.
3. At the front of the cabinet, firmly grasp the top cover on each side and lift up and away from the cabinet.

Reinstall the top cover by reversing this procedure.

5.3.6.2 Front Cover Removal

Remove the front cover as follows: (See figures 5-3 and 5-3A.)

1. Remove the top cover as described above.
2. The front cover is attached to the upper and lower part of the cabinet by metal tabs inserted into slots on the cabinet. Firmly grasp the top of the front cover and lift up and out of the cabinet.

Reinstall the front cover by reversing this procedure.

5.3.6.3 CP Circuit Board Removal and Replacement

There are seven different CP boards found in the VS-85/85-H. The removal and replacement procedures for the different boards are given in the order in which they are found on the Motherboard. (See figures 5-4A and 5-4B.)

CAUTION

> Be careful when replacing the large, flexible VS-85/85-H boards. Make sure that all boards are seated properly in the correct Motherboard sockets. Do not damage the sockets when inserting the boards. Make sure all boards have their component sides facing left when viewed from the chassis front.

5.3.6.3.1 210-7602 Control Memory Removal and Replacement

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.

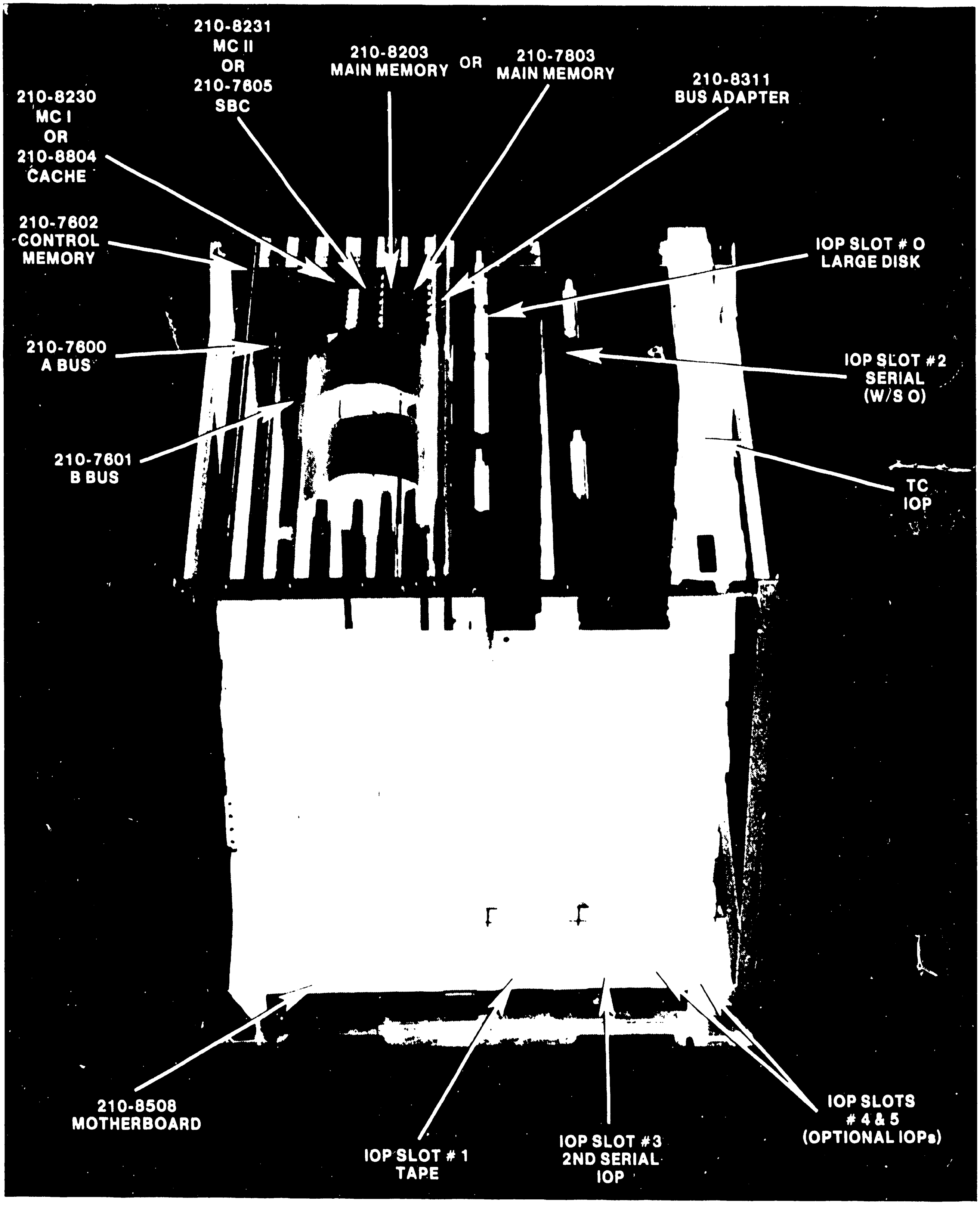


Figure 5-4A. VS-85 Motherboard With Circuit Boards

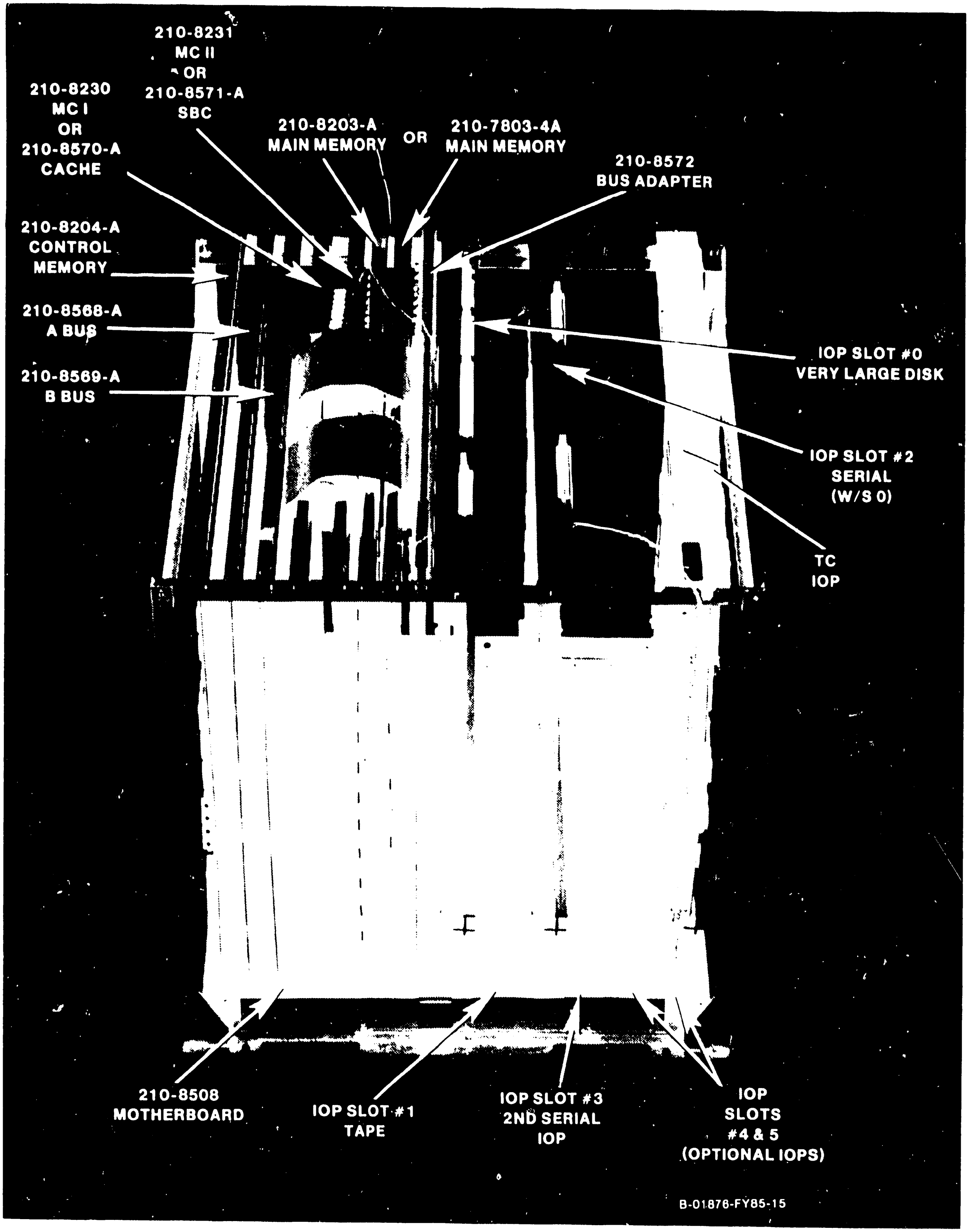


Figure 5-4B. VS-85-H Motherboard With Circuit Boards

2. W'th a 1/4" nut-driver, remove the two screws securing the top of the Display/Maintenance panel assembly to the top chassis rail.
3. Tilt the top of the Display/Maintenance panel assembly down for access to the Control Memory board cables.
4. Lower the fan assembly as described in paragraph 5.3.6.30. Remove the two Phillips screws securing the hinged cover over the fan safety screen inside the cabinet. Raise the cover, remove the screen, and turn the vertical air flow baffle (figure 5-39) to the right. This allows access to the connectors on the rear of the circuit boards.
5. Disconnect the 60-pin connectors from J1 and J2 and the 16-pin ribbon cable from location SW1 of the Control Memory board (figures 5-5A and 5-5B).
6. Once the cables are disconnected, remove the board by grasping the top corners and gently rocking it from side-to-side while exerting a steady upward pressure. Once the board is free of the slot, ease it up and out of the mainframe.
7. Install the new Control Memory board.
8. Reconnect the 60-pin connectors and the 16-pin ribbon cable.

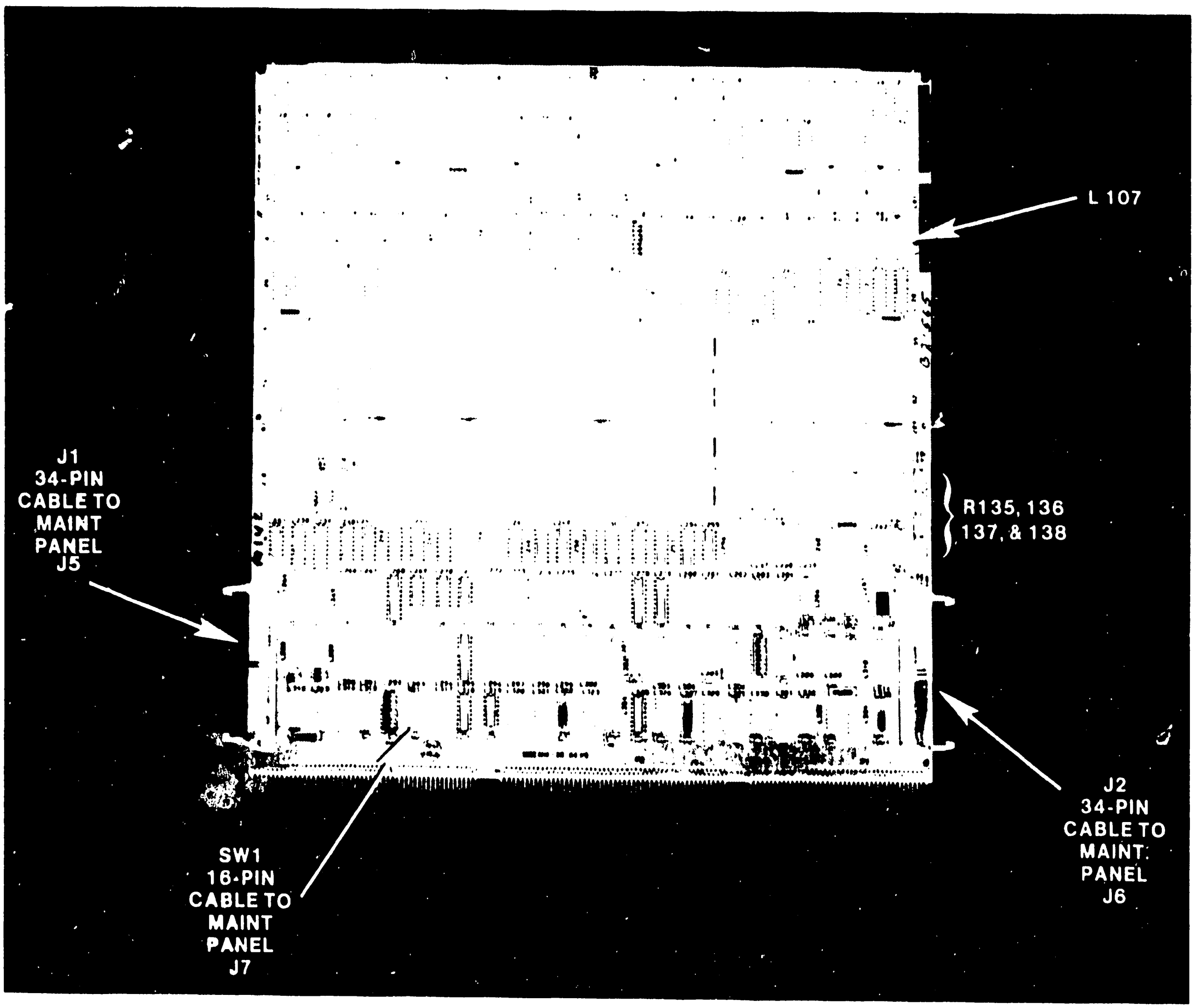


Figure 5-5A. 210-7602 VS-85 Control Memory Board

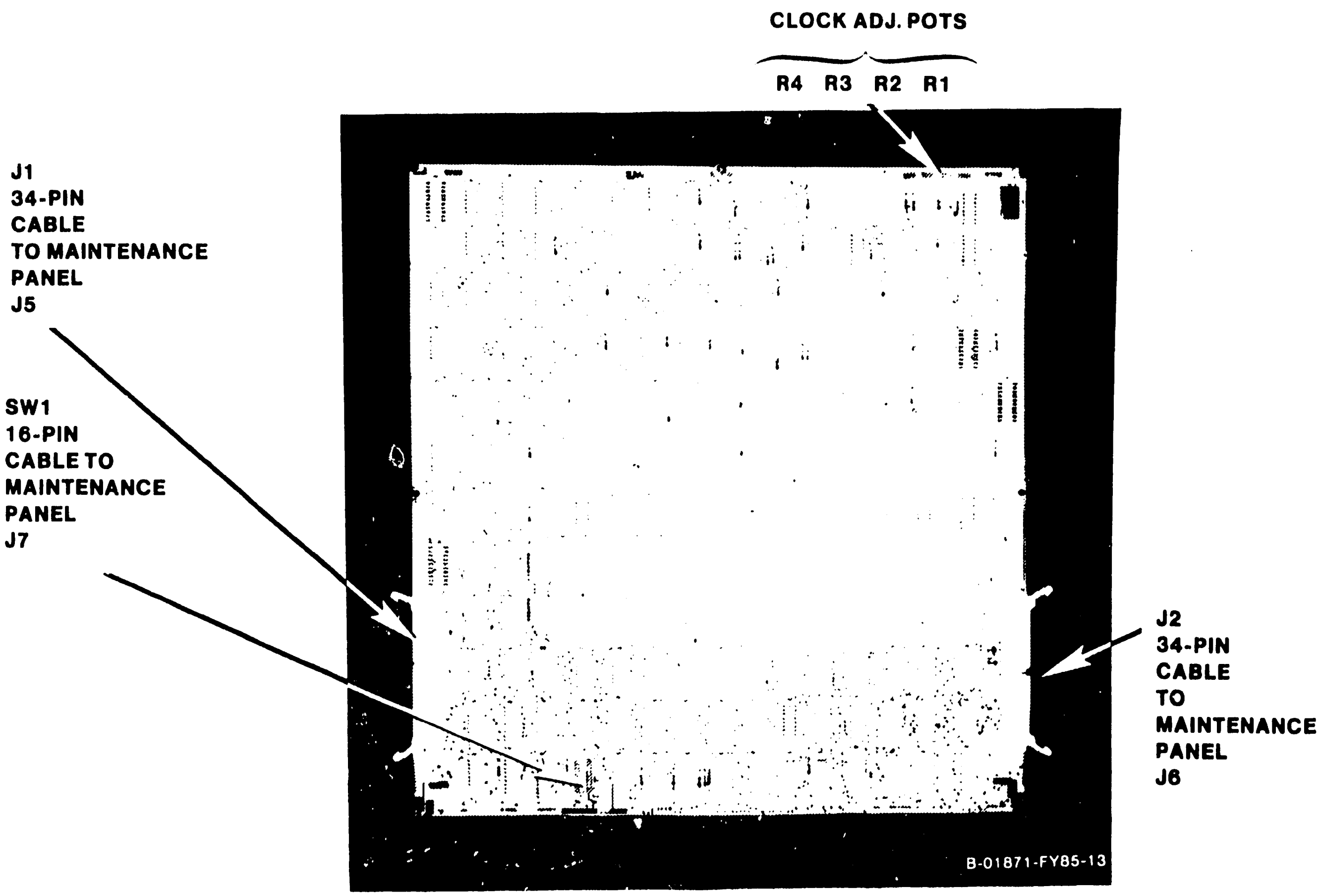


Figure 5-5B. 210-8204 VS-85-H Control Memory Board

5.3.6.3.2 210-7600 A Bus Removal and Replacement

1. Remove the A Bus board (figures 5-6A and 5-6B) from Motherboard slot #2 in the manner described in 5.3.6.3.1. (There are no cables connected to the A Bus.)
2. Install the new A Bus board.

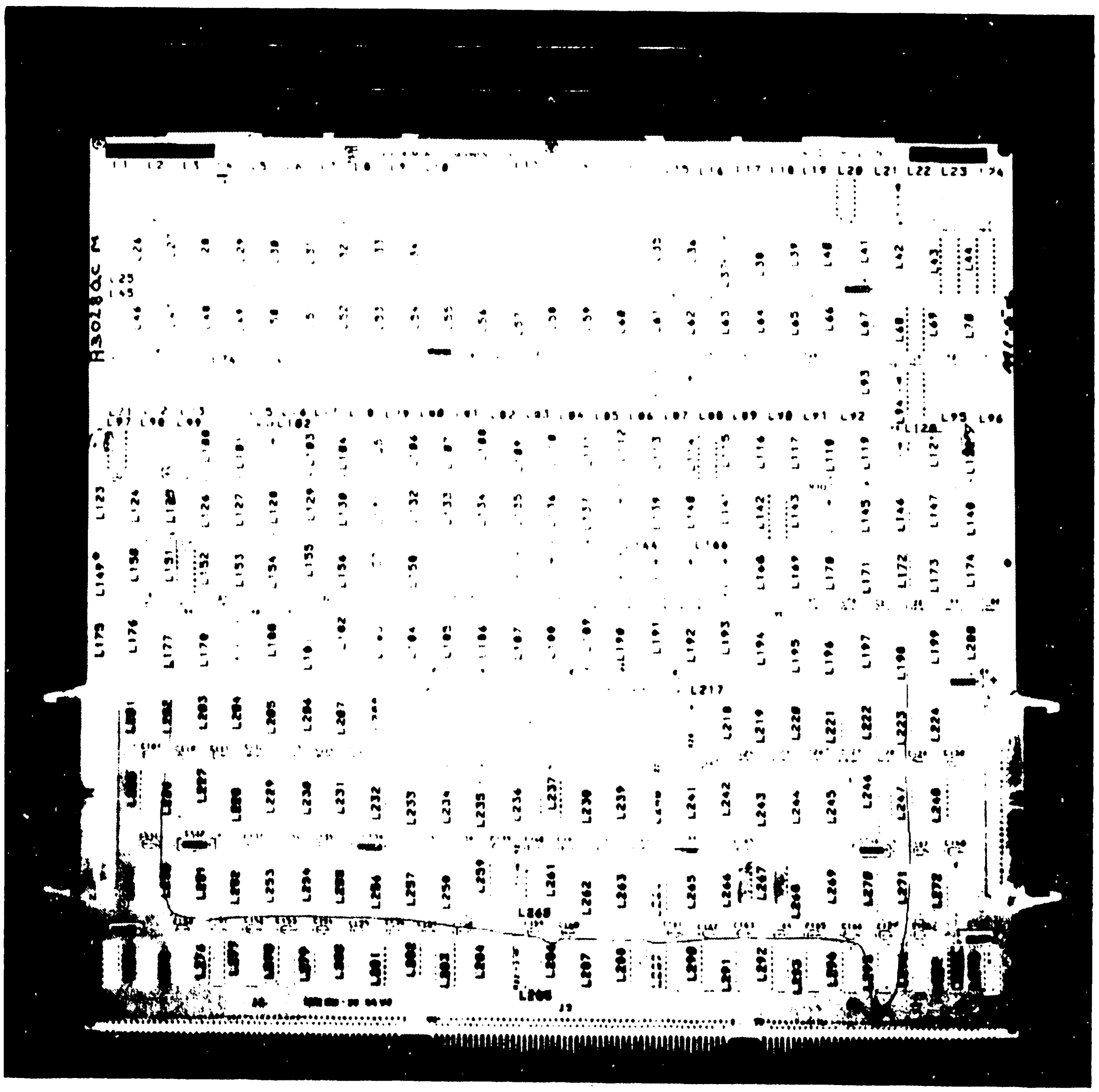


Figure 5-6A. 210-7600 VS-85 A Bus Board

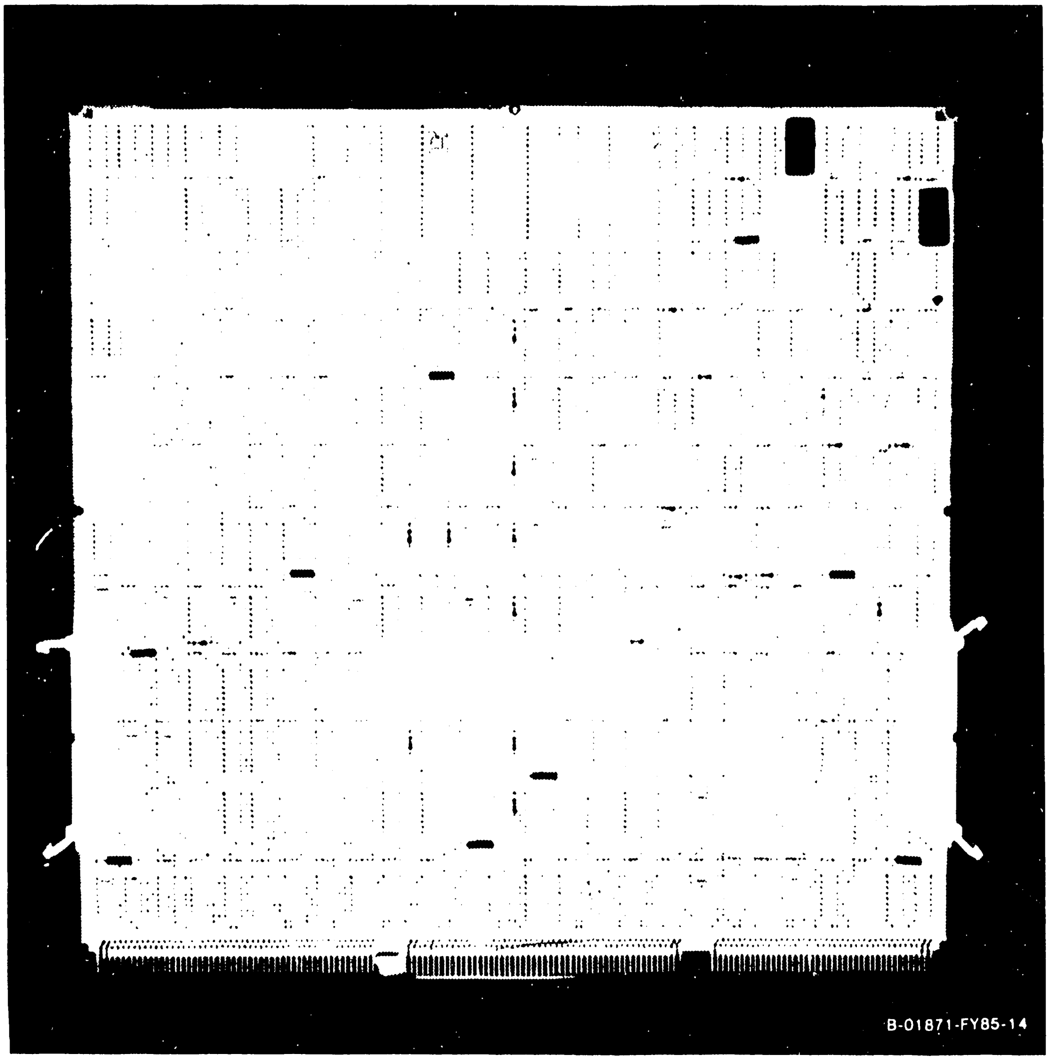


Figure 5-6B. 210-8568 VS-85-H A Bus Board

5.3.6.3.3 210-7600 B Bus Removal and Replacement

1. Before removing the B Bus board (figures 5-7A and 5-7B) from Motherboard slot #3, lower the fan assembly as described in paragraph 5.3.6.30. Remove the two Phillips screws securing the hinged cover over the fan safety screen inside the cabinet. Raise the cover, remove the screen, and turn the vertically mounted air flow baffle to the right. This allows access to the connectors on the rear of the circuit boards.
2. Disconnect the 60-pin connectors from from J1 and J2 of the board.
3. Remove the board in the manner described in 5.3.6.3.1.
4. Install the new B Bus board.
5. Reconnect the 60-pin connectors.

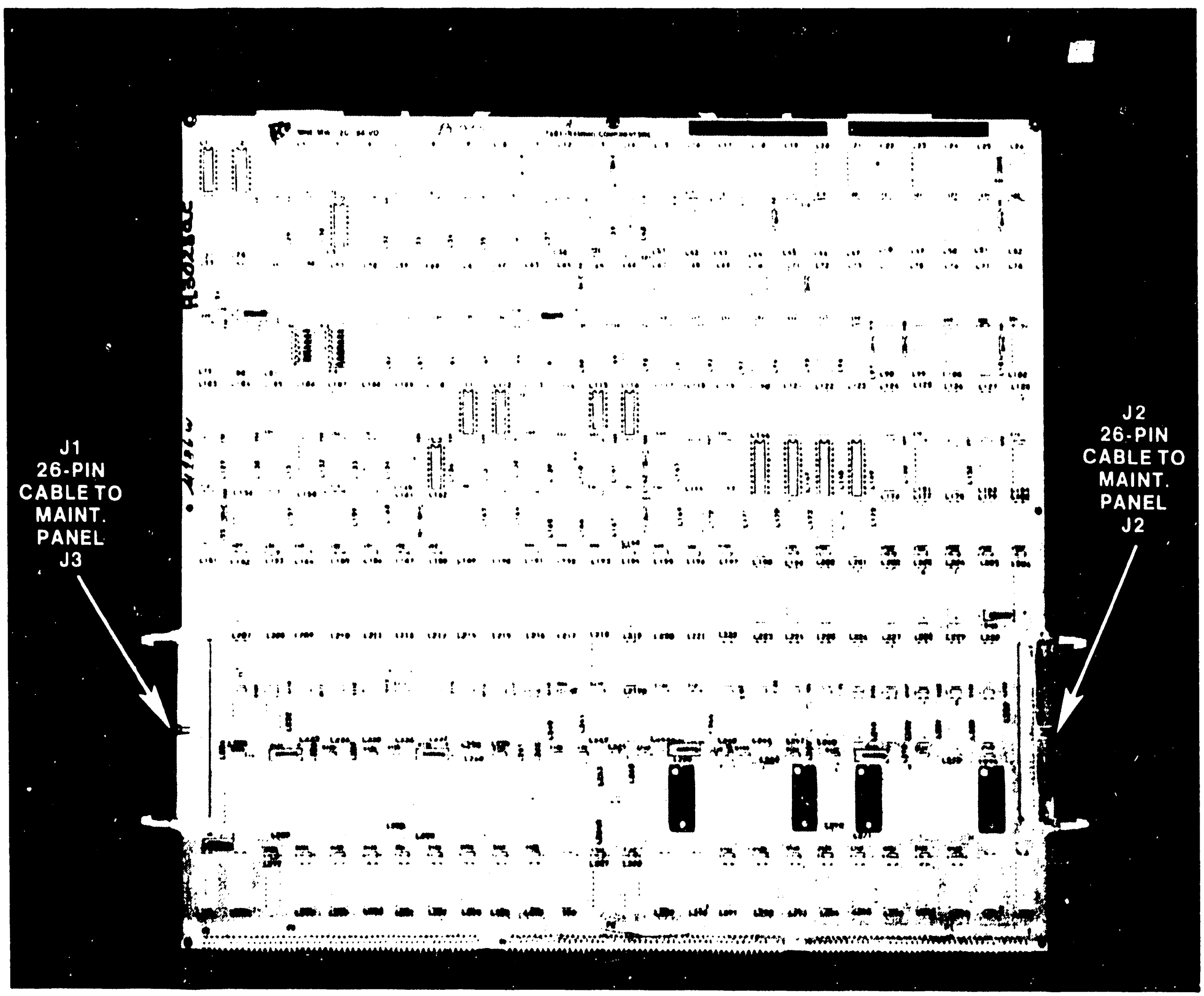


Figure 5-7A. 210-7601 VS-85 B Bus Board

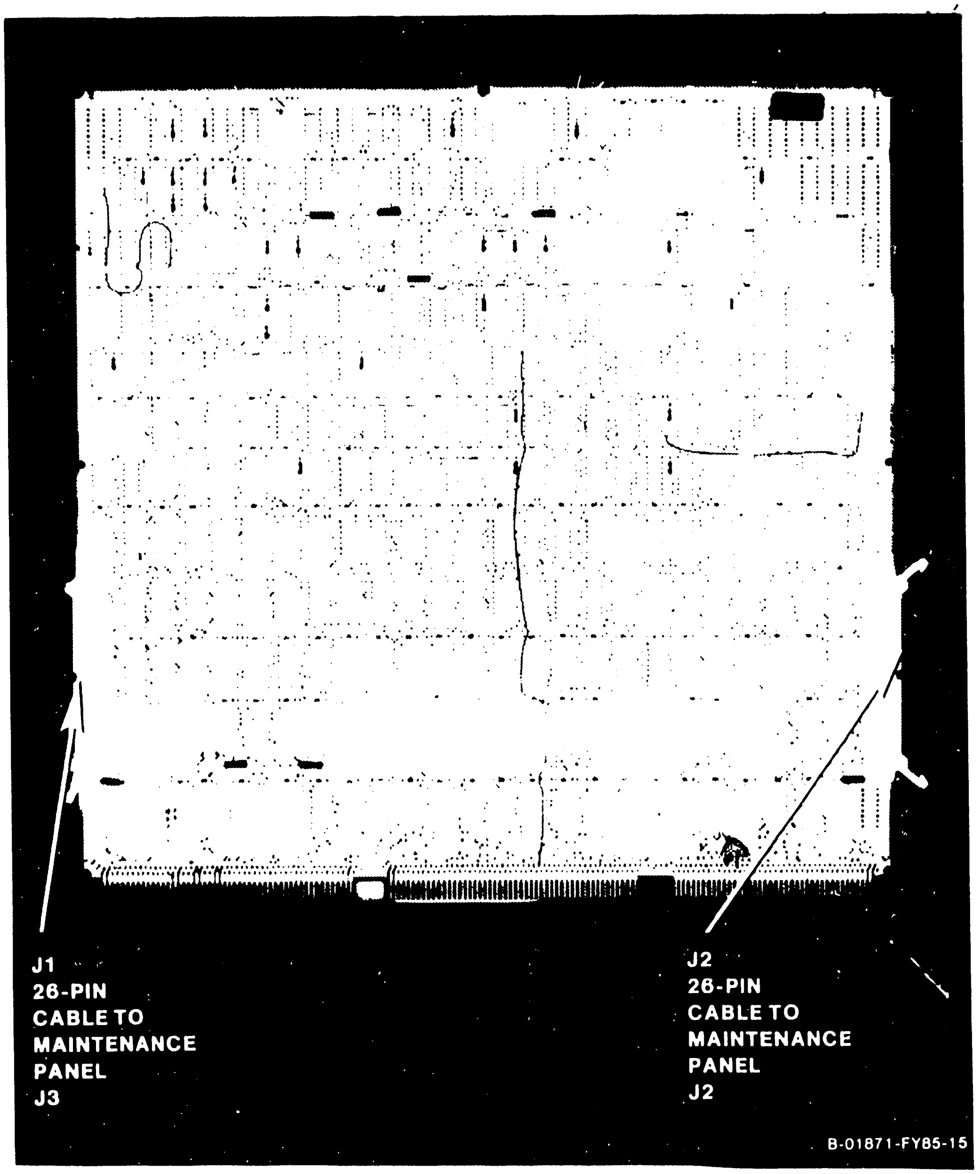


Figure 5-7B. 210-8569-A VS-85-H B Bus Board

5.3.6.3.4 210-8230 Memory Controller I Removal and Replacement

1. If the system has a Memory Controller I board (figure 5-8) in Motherboard slot #4, disconnect the 64-pin connectors from J3 and J4 on the front of the board.
2. Remove the board in the manner described in 5.3.6.3.1.
3. After checking the main memory board size selection jumpers and the memory size switch settings on the Memory Controller I board as shown in figures 5-9 and 5-10, install the new board. Remember to install the jumpers for the largest capacity memory board, not for total memory capacity.
4. Reconnect the 64-pin connectors.

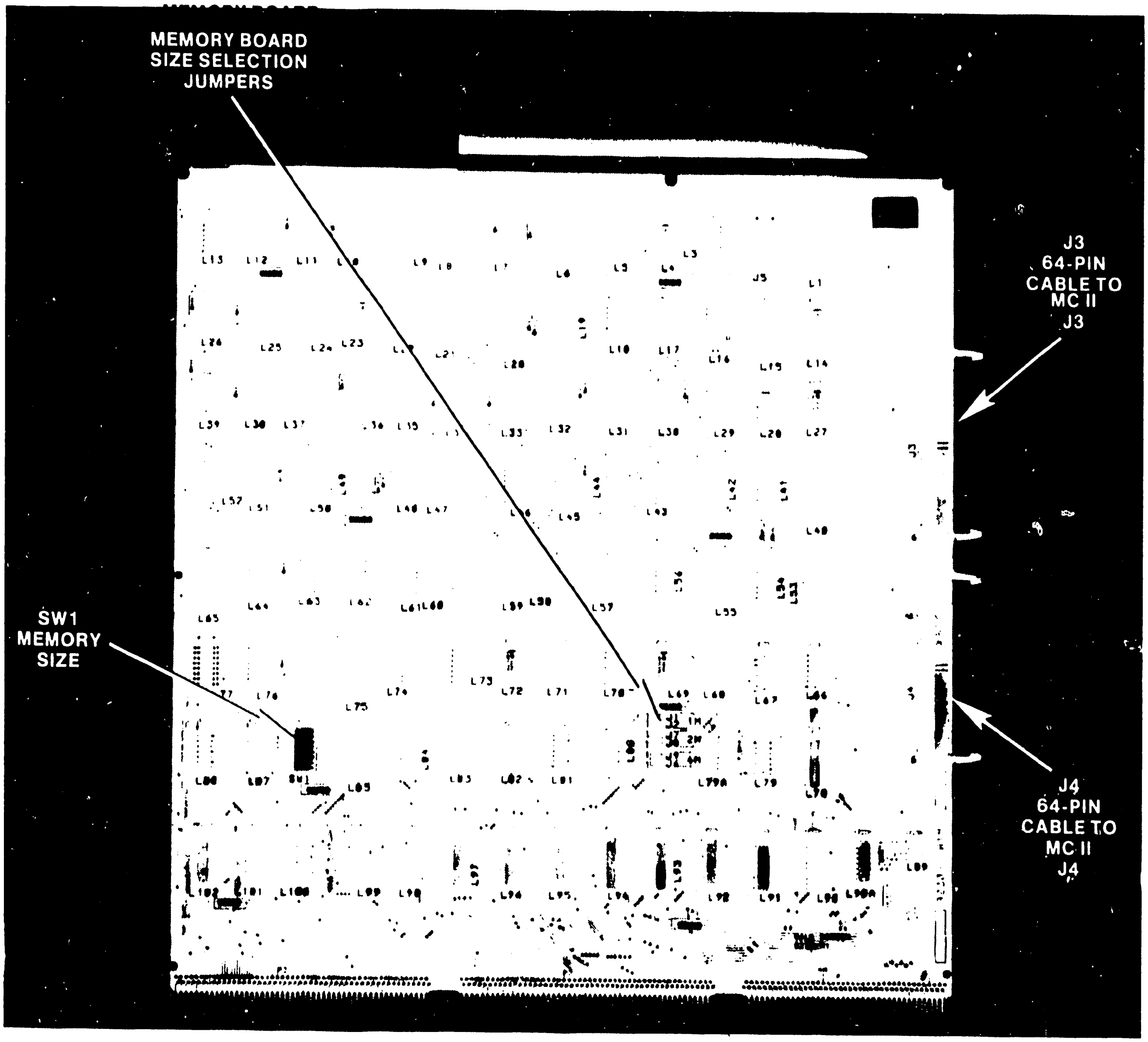


Figure 5-8. 210-8230 Memory Controller I Board

LARGEST CAPACITY BOARD	INSTALL JUMPERS AT
1 MEG	J1-J2
2 MEG	J7-J8
4 MEG*	J9-J6

Jumpers are horizontal

* - Not supported.

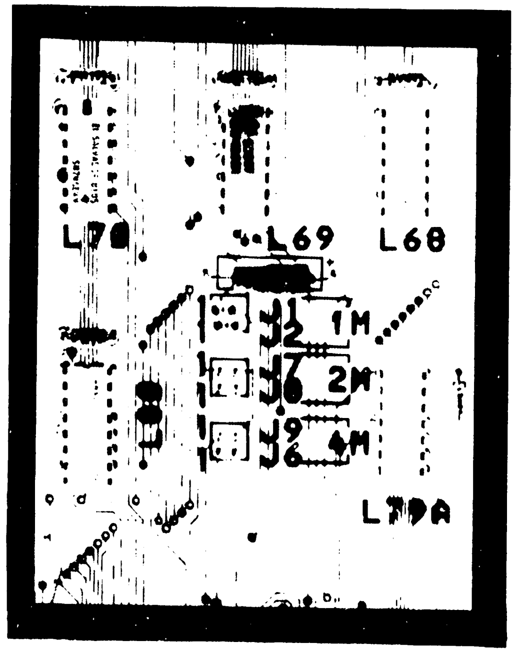
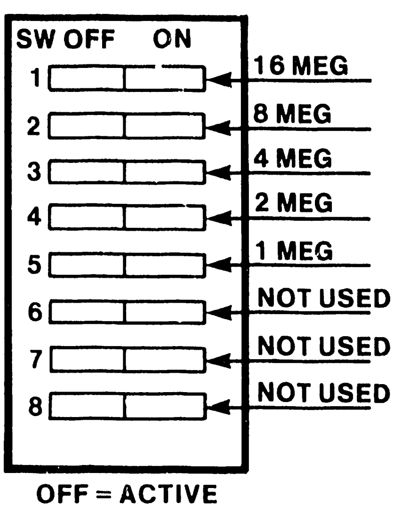


Figure 5-9. Main Memory Board Size Selection Jumpers



SW NO. 8 7 6	5	4	3	2	1	MEMORY SIZE IN BYTES
NOT USED	1	0	0	0	0	1 MEG
	0	1	0	0	0	2 MEG
	1	1	0	0	0	3 MEG
	0	0	1	0	0	4 MEG
	1	0	1	0	0	5 MEG
	0	1	1	0	0	6 MEG
	1	1	1	0	0	7 MEG
	0	0	0	1	0	8 MEG
	0	0	0	0	1	16 MEG

OFF = 1
ON = 0

Figure 5-10. Main Memory Size Selection

5.3.6.3.5 210-8804 Cache Memory Removal and Replacement

1. If the system has a Cache Memory board (figures 5-11A and 5-11B) in Motherboard slot #4, disconnect the 64-pin connectors from J1 and J2 on the top of the board, and from J3 and J4 on the front of the board.
2. Disconnect the 16-pin cable from L46 (J5).
3. Remove the board in the manner described in 5.3.6.3.1.
4. After checking the main memory board size selection jumpers and the memory size switch settings on the Cache Memory board as shown in figures 5-12A, 5-12B, 5-13A, and 5-13B, install the new board. Remember to install the jumpers for the largest capacity memory board, not for total memory capacity.
5. Reconnect the 64-pin connectors and the 16-pin cable.

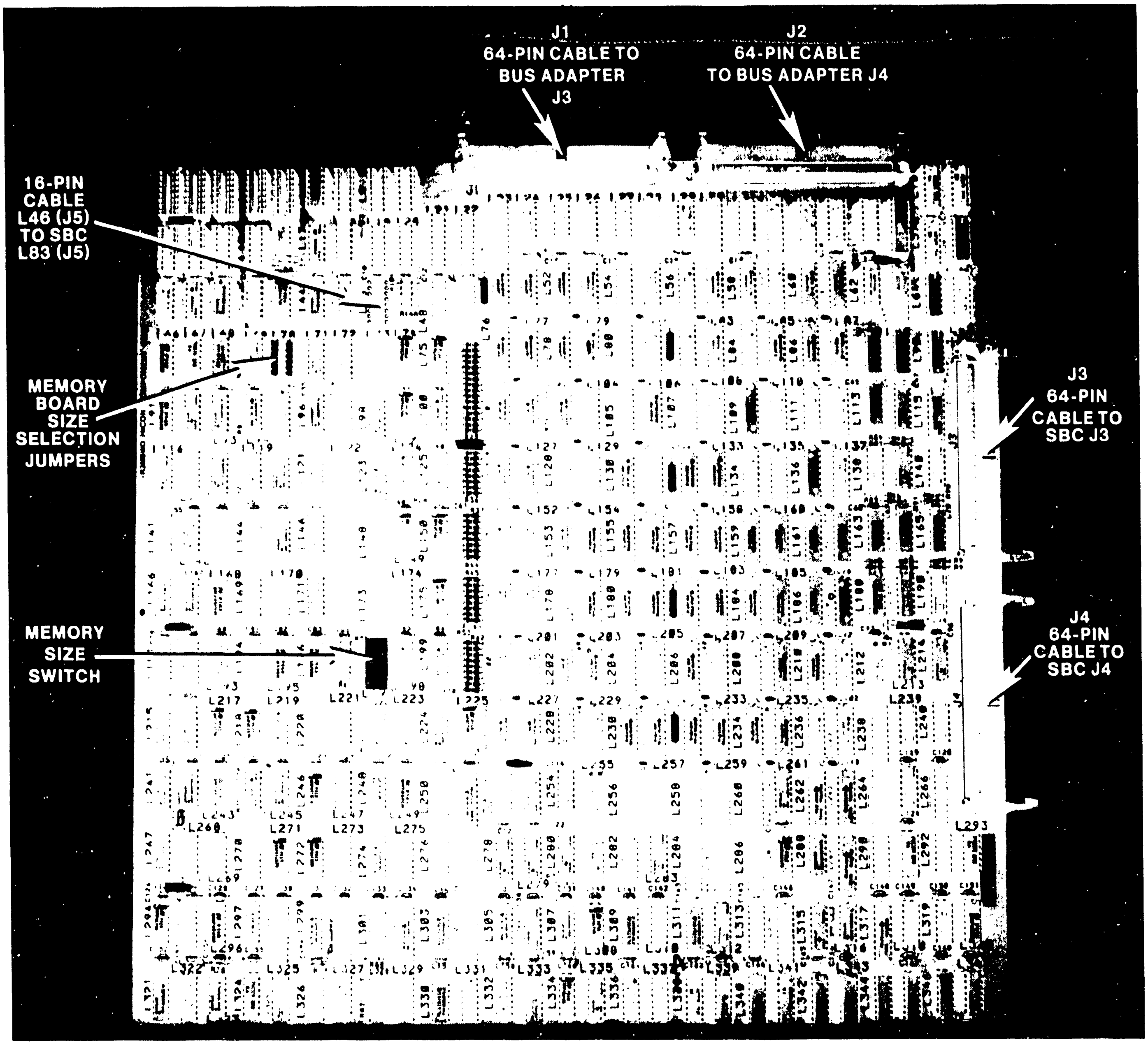


Figure 5-11A. 210-8804 VS-85 Cache Memory Board

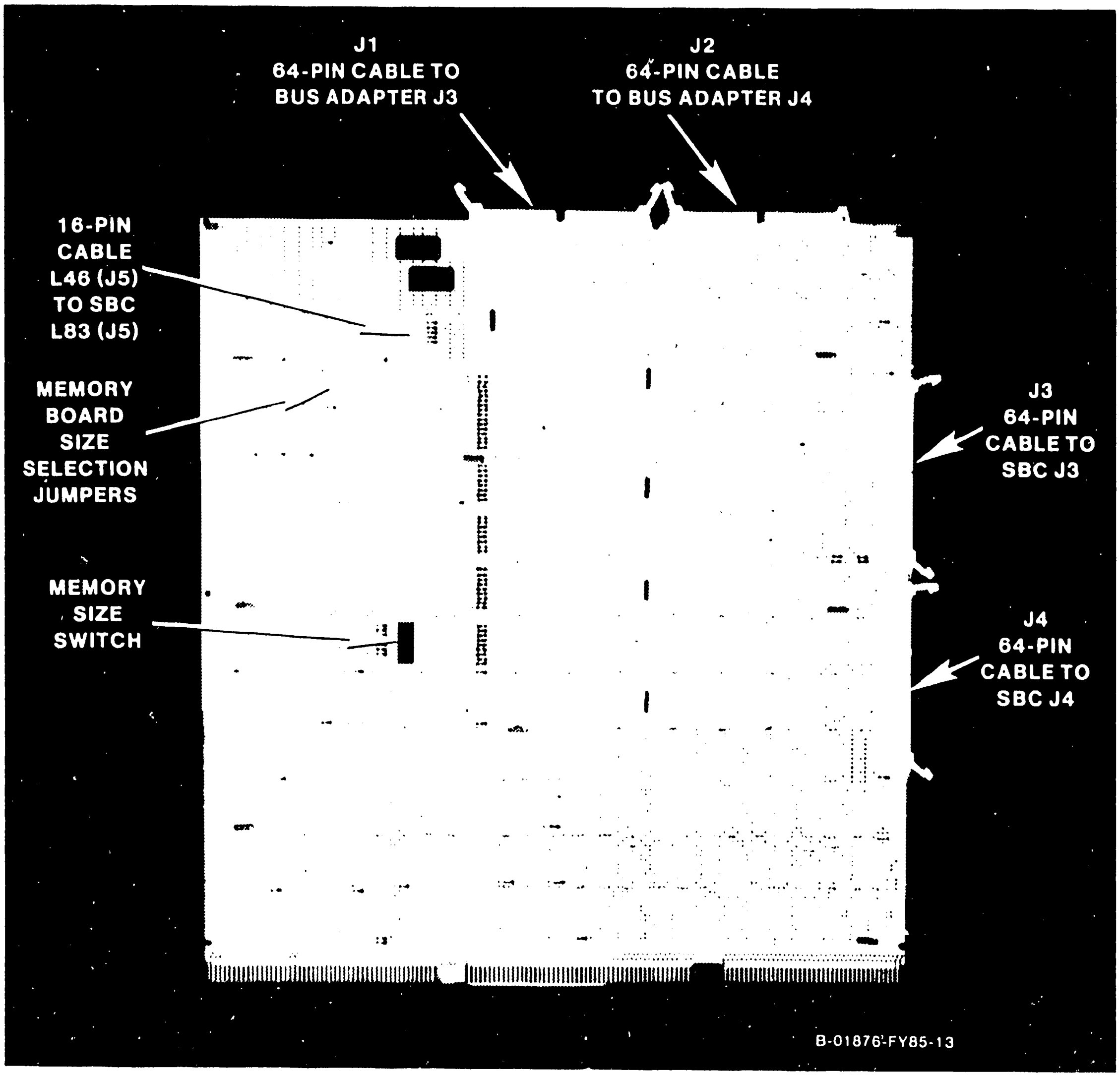


Figure 5-11B. 210-8570-A VS-85-H Cache Memory Board

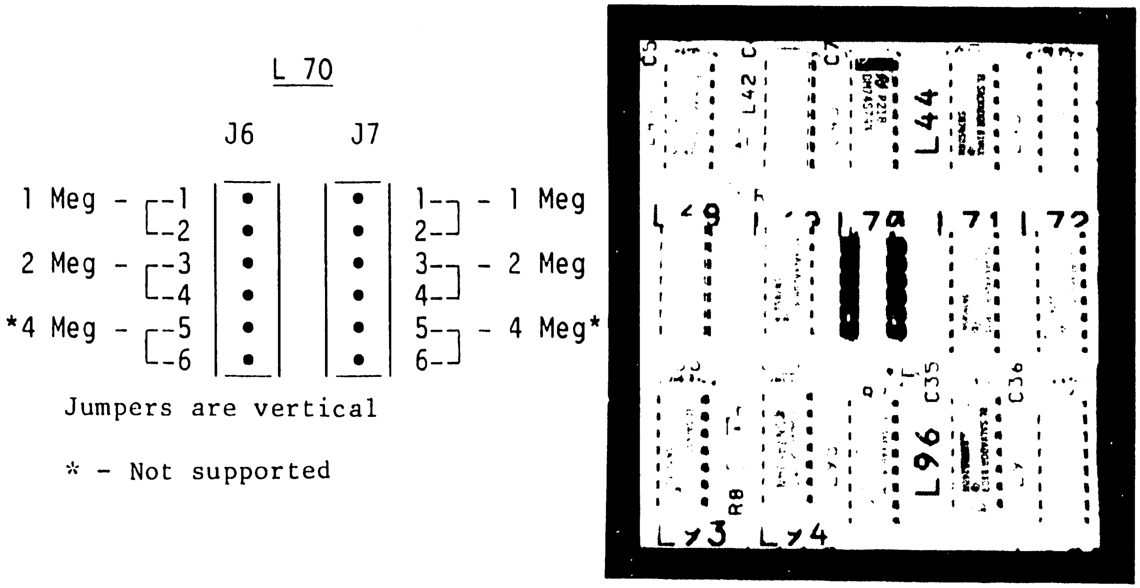
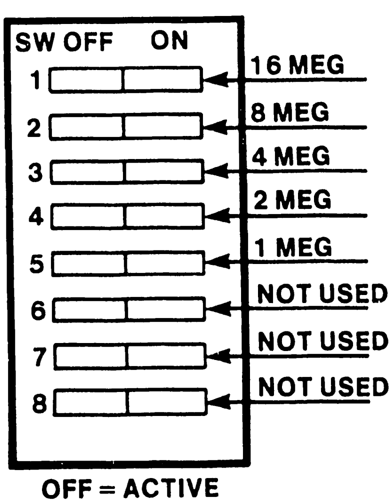


Figure 5-12A. VS-85 Main Memory Board Size Selection Jumpers



SW NO. 8 7 6	5	4	3	2	1	MEMORY SIZE IN BYTES
	1	0	0	0	0	1 MEG
	0	1	0	0	0	2 MEG
	1	1	0	0	0	3 MEG
	0	0	1	0	0	4 MEG
NOT USED	1	0	1	0	0	5 MEG
	0	1	1	0	0	6 MEG
	1	1	1	0	0	7 MEG
	0	0	0	1	0	8 MEG
	0	0	0	0	1	16 MEG

OFF = 1
ON = 0

Figure 5-12B. VS-85 Main Memory Size Selection

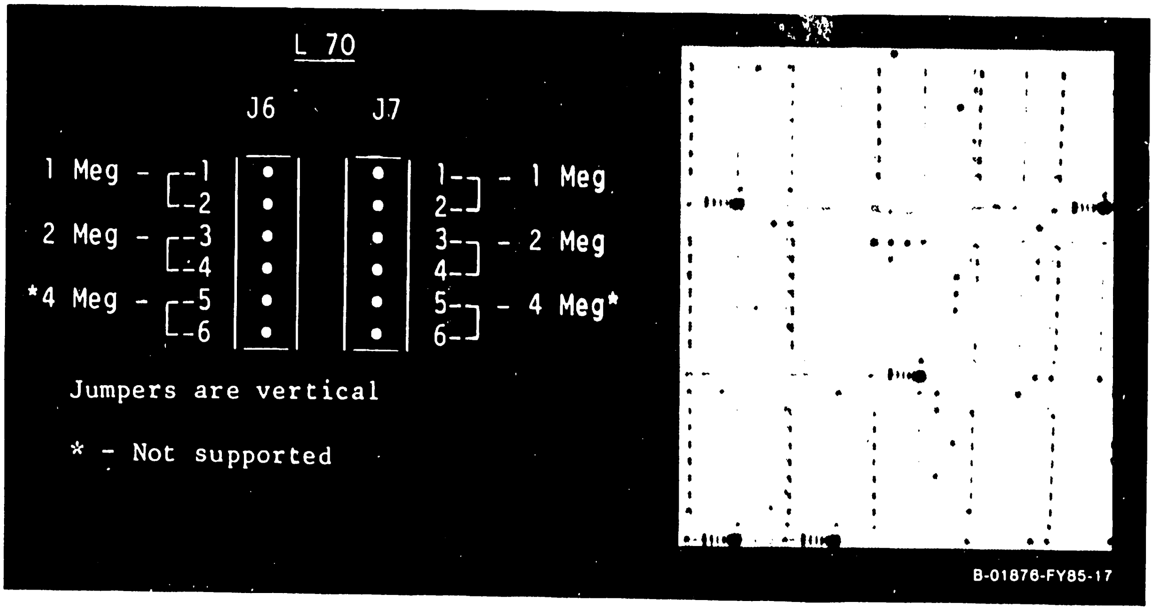
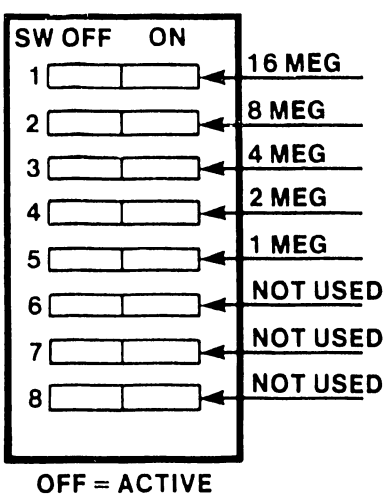


Figure 5-13A. VS-85-H Main Memory Board Size Selection Jumpers



SW NO. 8 7 6	5	4	3	2	1	MEMORY SIZE IN BYTES
NOT USED	1	0	0	0	0	1 MEG
	0	1	0	0	0	2 MEG
	1	1	0	0	0	3 MEG
	0	0	1	0	0	4 MEG
	1	0	1	0	0	5 MEG
	0	1	1	0	0	6 MEG
	1	1	1	0	0	7 MEG
	0	0	0	1	0	8 MEG
	0	0	0	0	1	16 MEG

OFF = 1
ON = 0

Figure 5-13B. VS-85-H Main Memory Size Selection

5.3.6.3.6 210-8231 Memory Controller II Removal and Replacement

1. If the system has a Memory Controller II board (figure 5-14) in Motherboard slot #5, lower the fan assembly as described in paragraph 5.3.5.22. Remove the two Phillips screws securing the hinged cover over the fan safety screen inside the cabinet. Raise the cover, remove the screen, and turn the vertically mounted air flow baffle to the right. This allows access to the connectors on the rear of the circuit boards.
2. Disconnect the 64-pin connectors from J1, J3, J4, J5, and J6 of the board.
3. Remove the board in the manner described in 5.3.6.3.1.
4. Install the new Memory Controller II board.
5. Reconnect the 64-pin connectors.

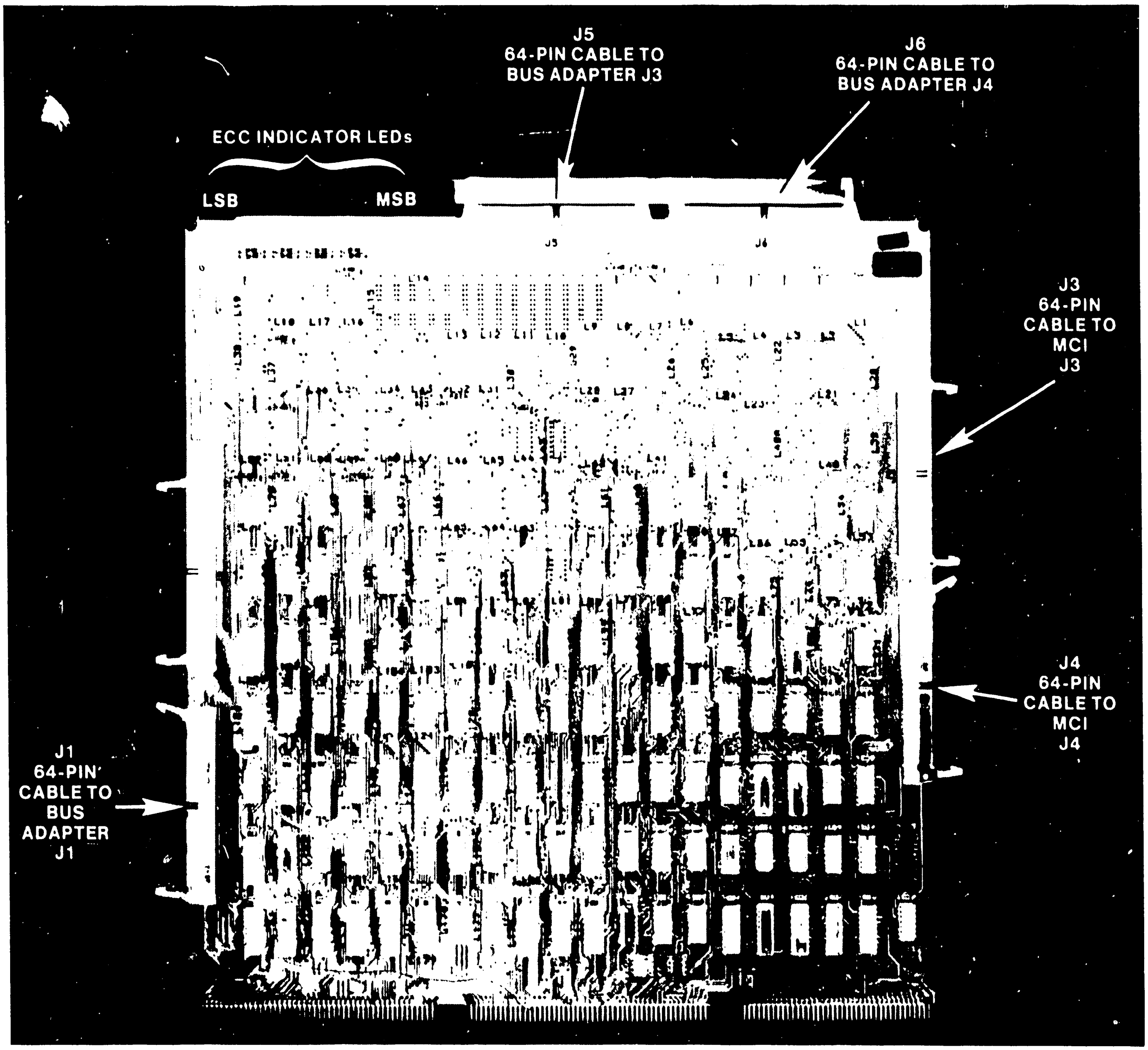


Figure 5-14. 210-8231 Memory Controller II Board

5.3.6.3.7 210-7605 System Bus Controller Removal and Replacement

1. If the system has a System Bus Controller board (figure 5-15A and 5-15B) in Motherboard slot #5, lower the fan assembly as described in paragraph 5.3.6.30. Remove the two Phillips screws securing the hinged cover over the fan safety screen inside the cabinet. Raise the cover, remove the screen, and turn the vertically mounted air flow baffle to the right. This allows access to the connectors on the rear of the circuit boards.
2. Disconnect the 64-pin connectors from J1, J2, J3, and J4 of the board.
3. Disconnect the 16-pin cable from L83 (J5).
4. Remove the board in the manner described in step 5.3.6.3.1.
5. Install the new System Bus Controller board.
6. Reconnect the 64-pin connectors and the 16-pin cable.

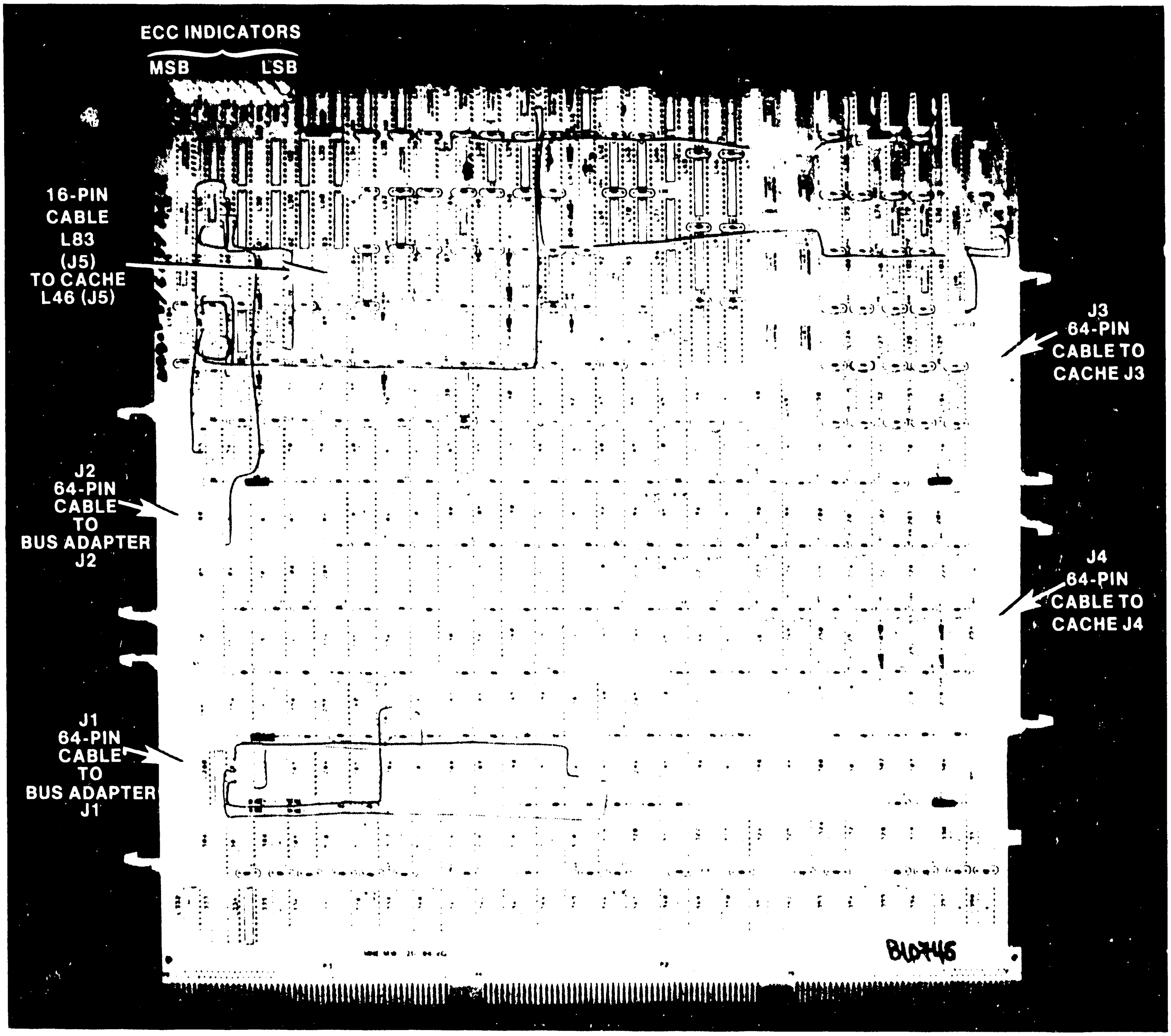


Figure 5-15A. 210-7605 VS-85 System Bus Controller Board

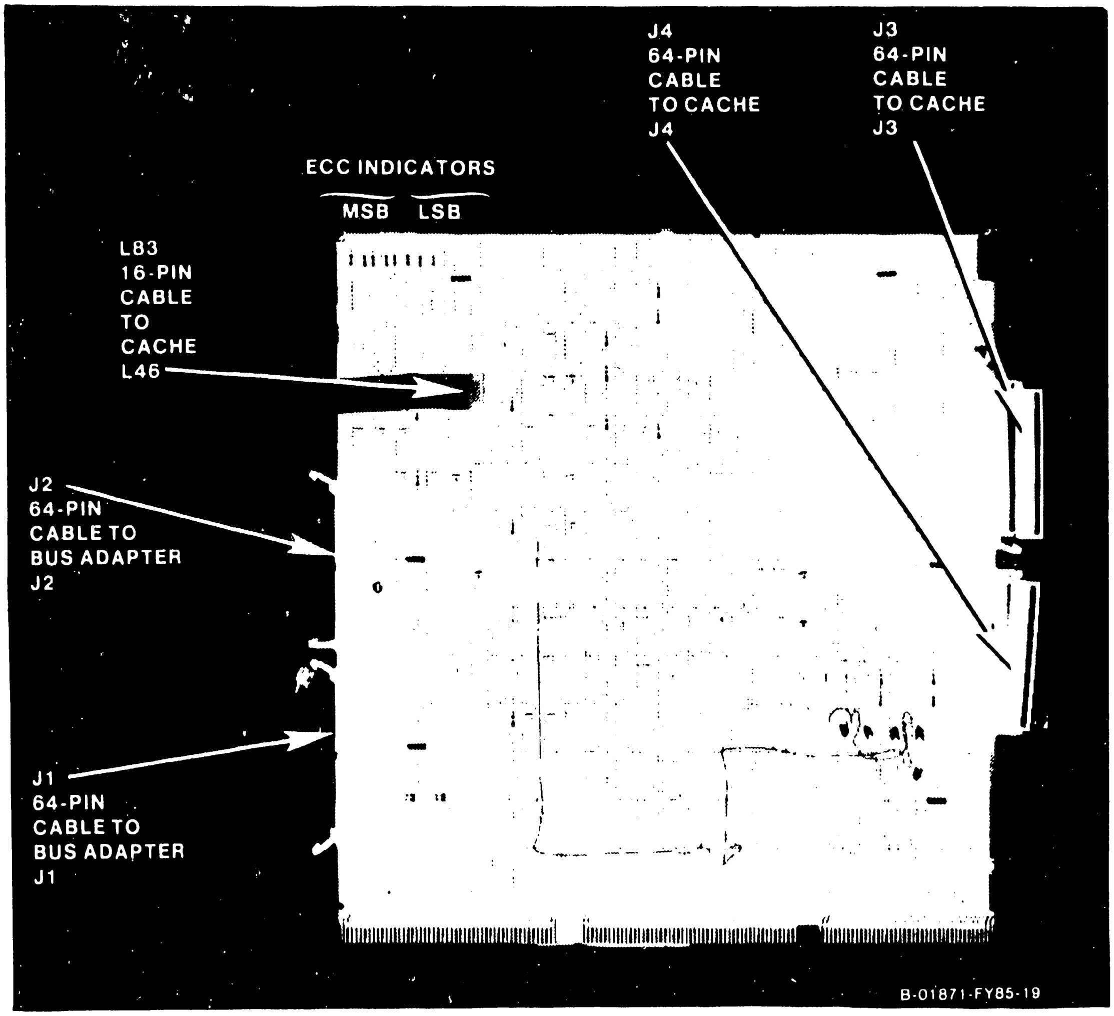


Figure 5-15B. 210-8571 VS-85-H System Bus Controller Board

5.3.6.3.8 210-7803/8203 Main Memory Removal and Replacement

1. Remove the Main Memory boards (figures 5-16, 5-17, and 5-18) from Motherboard slot(s) 6 and/or 7 as described in step 5.3.6.3.1.
2. Refer to table 5-1 and install the new Main Memory board(s). If installing a new board means the main memory capacity will change, see figures 5-8, 5-9, and 5-10, or 5-11A & B, 5-12A & B, and 5-13A & B.

Table 5-1. Main Memory Size

MEMORY CAPACITY	SLOT #	WLI P/N
1 Megabytes	6	210-7803
2 Megabytes *	6	210-7803
	7	210-7803
4 Megabytes	6	210-8203
	7	210-8203

* - Minimum main memory size for a VS-85/85-H with optional Cache Memory/SBC.

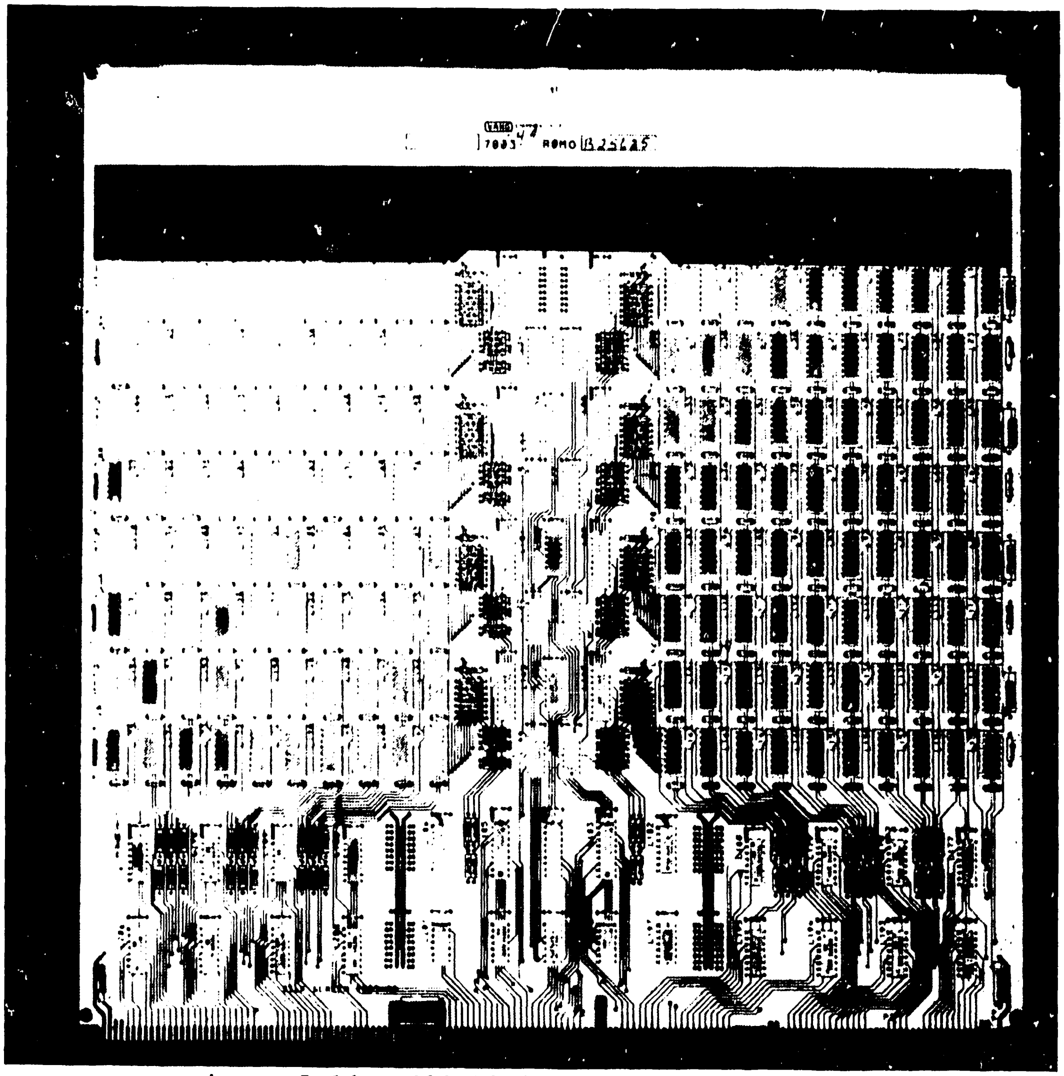


Figure 5-16. 210-7803 1MB Main Memory Board

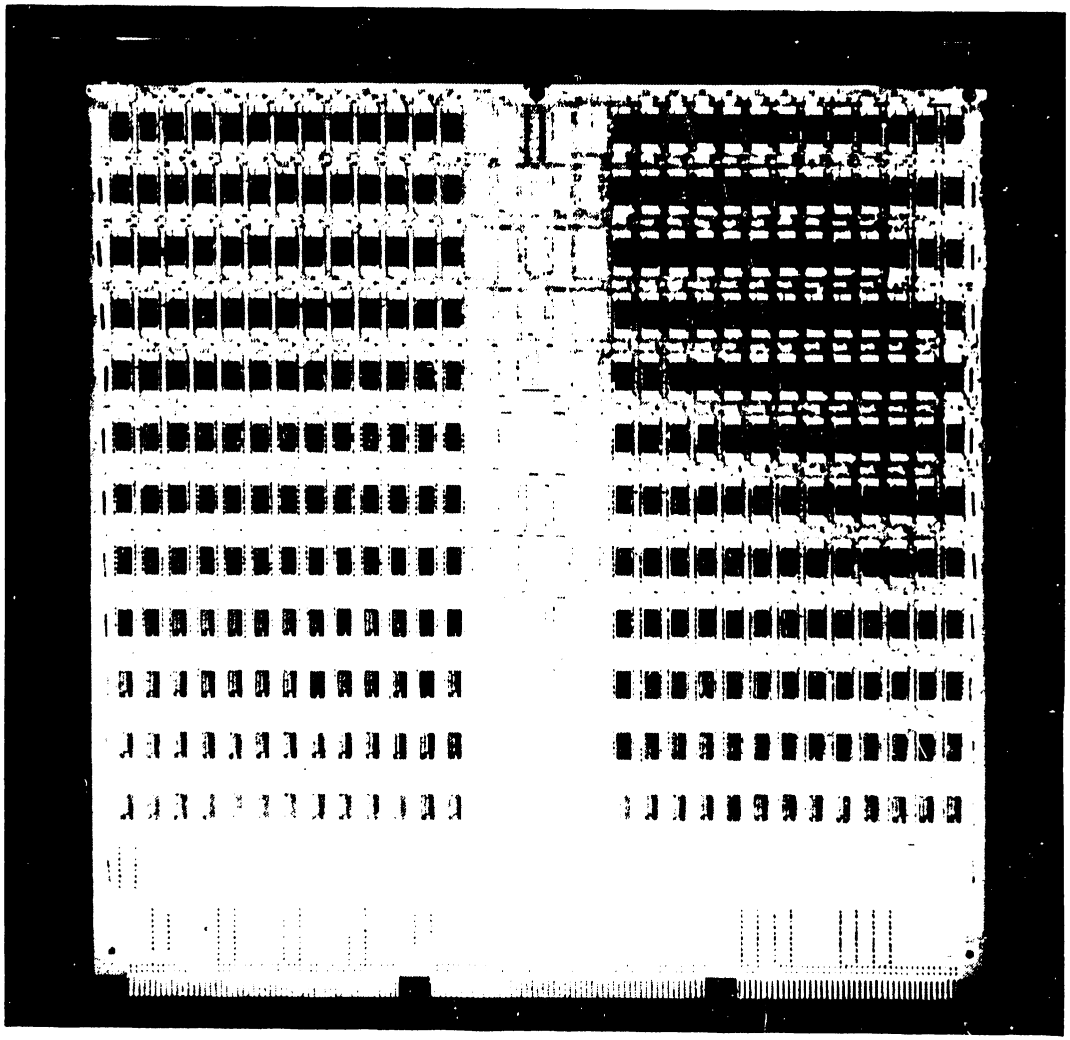


Figure 5-17. 210-8203 2MB Main Memory Board

5.3.6.3.9 210-8311 Bus Adapter Removal and Replacement

1. Before removing the Bus Adapter (BA) board (figures 5-19A and 5-19B) from Motherboard slot #8, lower the fan assembly as described in paragraph 5.3.6.30. Remove the two Phillips screws securing the hinged cover over the fan safety screen inside the cabinet. Raise the cover, remove the screen, and turn the vertically mounted air flow baffle to the right. This allows access to the connectors on the rear of the circuit boards.
2. Disconnect the 64-pin connectors from J1; (and J2 if Cache is installed), J3, and J4 of the board.
3. Due two space constrictions, it may be necessary to remove any 2nd memory board from Motherboard slot # 7 before removing the BA board.
4. Remove the BA board in the manner described in step 5.3.6.3.1.
5. Install the new BA board.
6. Reconnect the 64-pin connectors and return the fan assembly to normal.

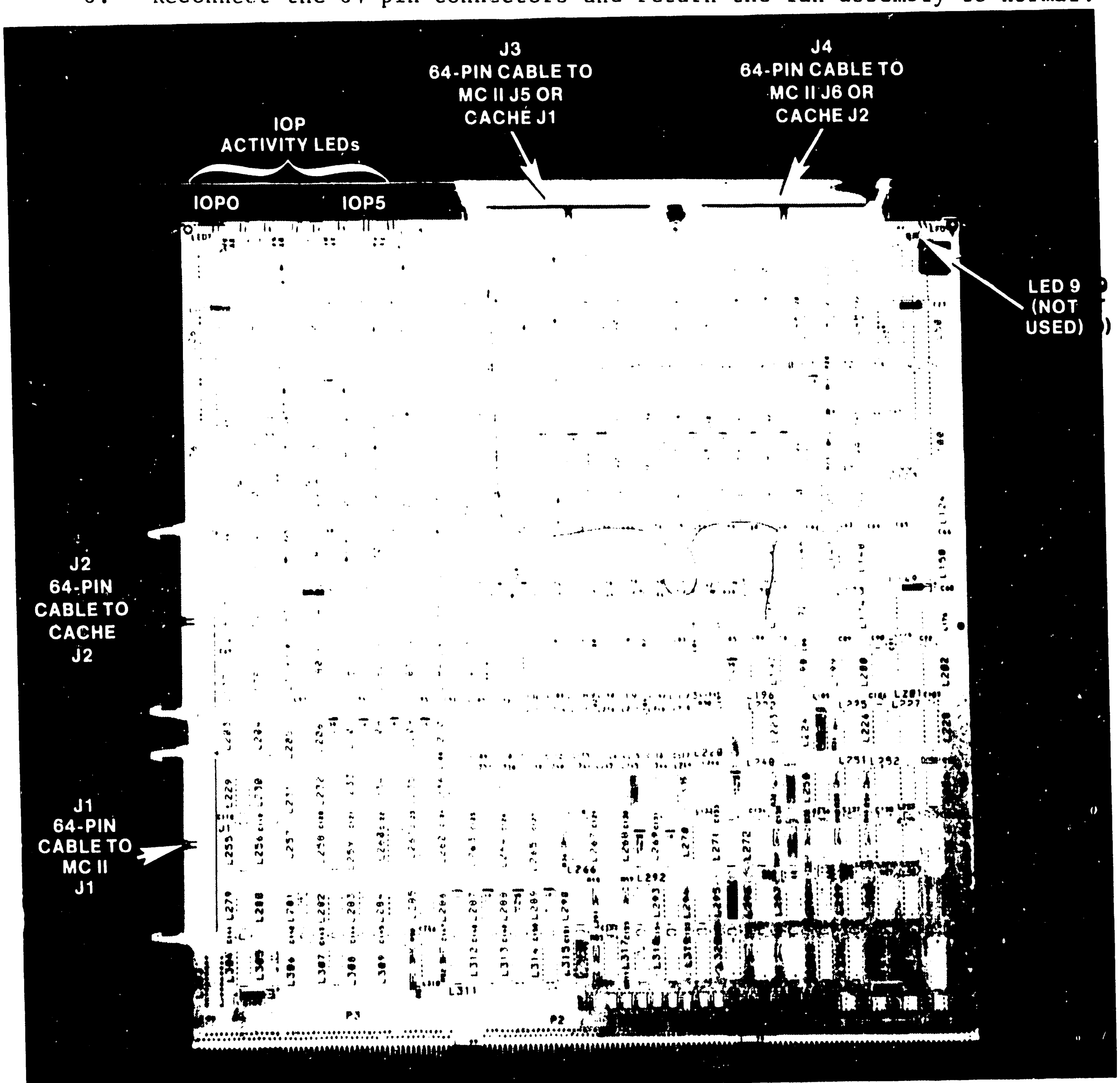


Figure 5-18A. 210-8311 VS-85 Bus Adapter Board

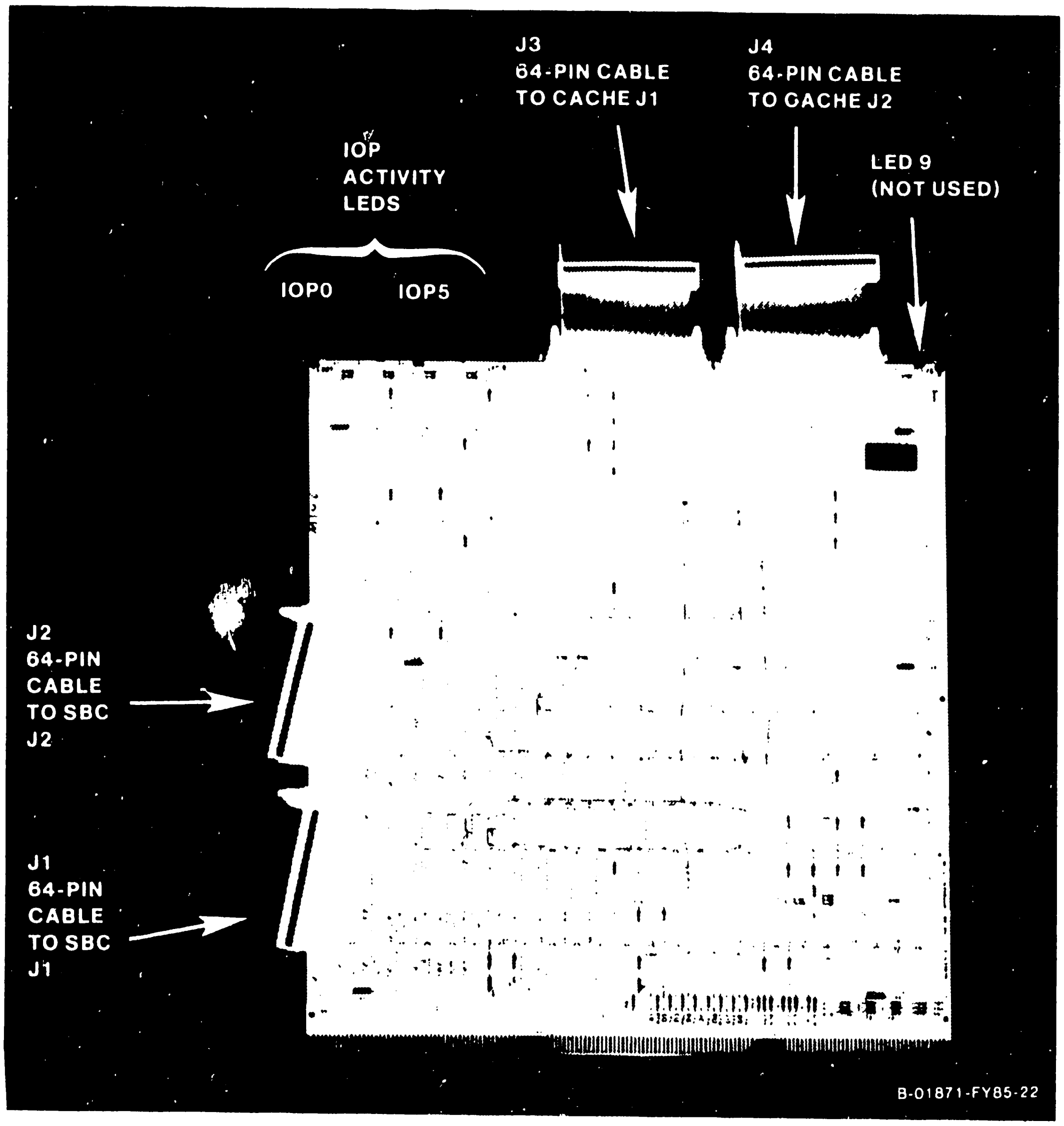


Figure 5-18B. 210-8572 VS-85-H Bus Adapter Board

5.3.6.3.10 Internal Cable Connections

Once the CP circuit board(s) has been replaced, make sure that all internal interconnection cables have been reconnected according to tables 5-2A and 5-2B. Make sure that all board cables are secured in place. See figure 5-20 for the 210-7614 Maintenance Panel and figure 5-21 for proper cable configurations for the 210-8513 Display Panel.

Table 5-2A. VS-85 Internal Signal Cable Connections

PC BOARD	CONNECTOR	TO	CONNECTOR	PC BOARD
210-7602	SW1	16-pin connector	J7	210-7614
"	J1	60-pin connector	J5	"
"	J2	60-pin connector	J6	"
210-7601	J1	60-pin connector	J3	210-7614
"	J2	60-pin connector	J2	"
210-8230	J3	64-pin connector	J3	210-8231
"	J4	64-pin connector	J4	"
210-8804	J1	64-pin connector	J3	210-8311
(Optional	J2	64-pin connector	J4	"
Cache	J3	64-pin connector	J3	210-7605
Memory)	J4	64-pin connector	J4	"
"	J5	16-pin connector	J5	"
210-8231	J1	64-pin connector	J1	210-8311
"	J5	64-pin connector	J3	"
"	J6	64-pin connector	J4	"
210-7605	J1	64-pin connector	J1	210-8311
(Optional	J2	64-pin connector	J2	"
SBC)	J3	64-pin connector	J3	210-8804
"	J4	64-pin connector	J4	"
"	J5	16-pin connector	J5	"
210-7614	J9	16-pin connector	J2	210-8513
"	J4	34-pin connector	J6	210-7610
210-8513	J1	26-pin connector	J49	210-8508
210-7610	J1	34-pin connector	J1	Mini Diskette Drive

Table 5-2B. VS-85-H Internal Signal Cable Connections

PC BOARD	CONNECTOR	TO	CONNECTOR	PC BOARD
210-8204	SW1	16-pin connector	J7	210-7614
"	J1	60-pin connector	J5	"
"	J2	60-pin connector	J6	"
210-8569	J1	60-pin connector	J3	210-7614
"	J2	60-pin connector	J2	"
210-8230	J3	64-pin connector	J3	210-8231
"	J4	64-pin connector	J4	"
210-8570	J1	64-pin connector	J3	210-8572
(Optional	J2	64-pin connector	J4	"
Cache	J3	64-pin connector	J3	210-8571
Memory)	J4	64-pin connector	J4	"
"	J5	16-pin connector	J5	"
210-8231	J1	64-pin connector	J1	210-8572
"	J5	64-pin connector	J3	"
"	J6	64-pin connector	J4	"
210-8571	J1	64-pin connector	J1	210-8572
(Optional	J2	64-pin connector	J2	"
SBC)	J3	64-pin connector	J3	210-8570
"	J4	64-pin connector	J4	"
"	J5	16-pin connector	J5	"
210-7614	J9	16-pin connector	J2	210-8513
"	J4	34-pin connector	J6	210-7610
210-8513	J1	26-pin connector	J49	210-8508
210-7610	J1	34-pin connector	J1	Mini Diskette Drive

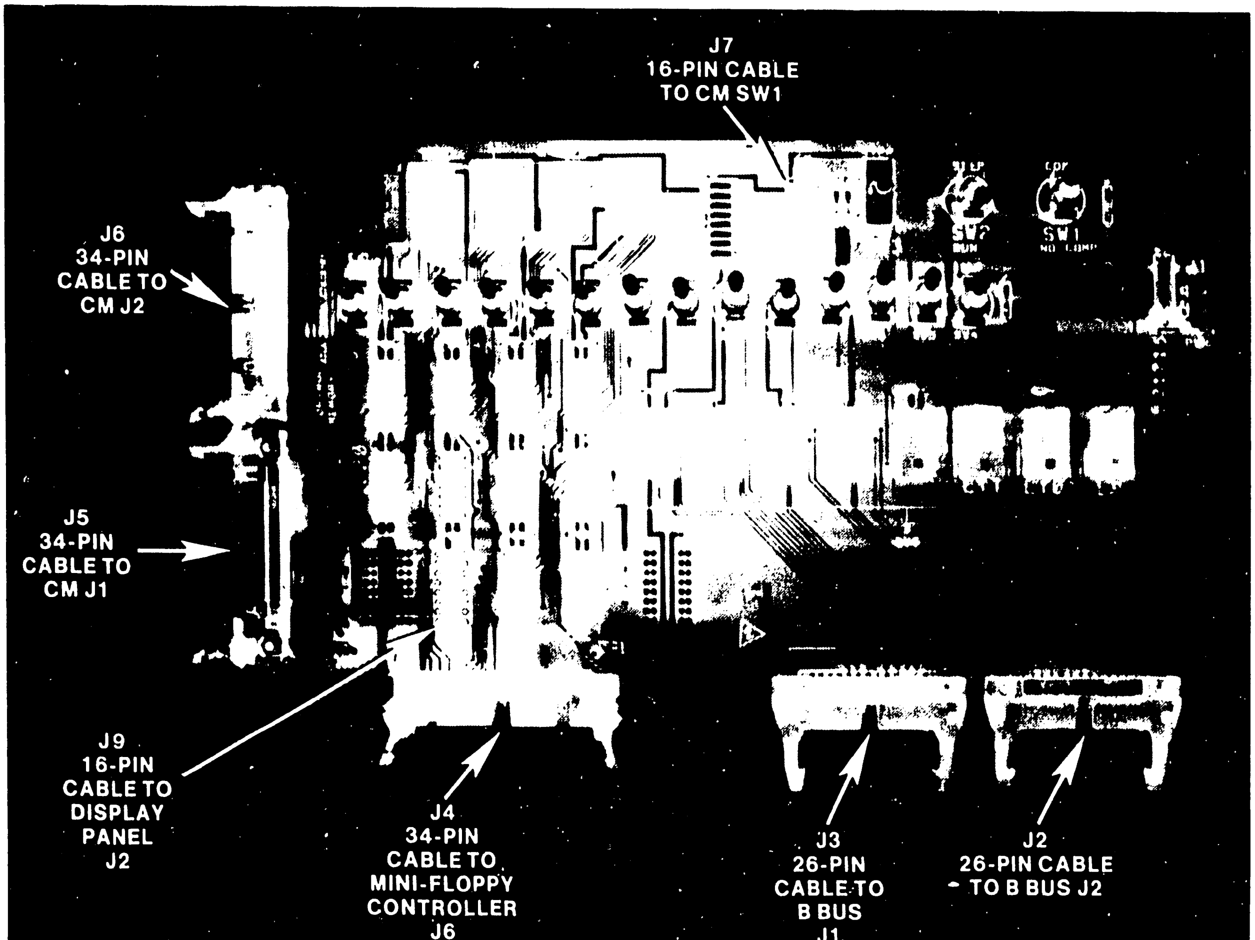


Figure 5-19. 210-7614 Maintenance Panel Board

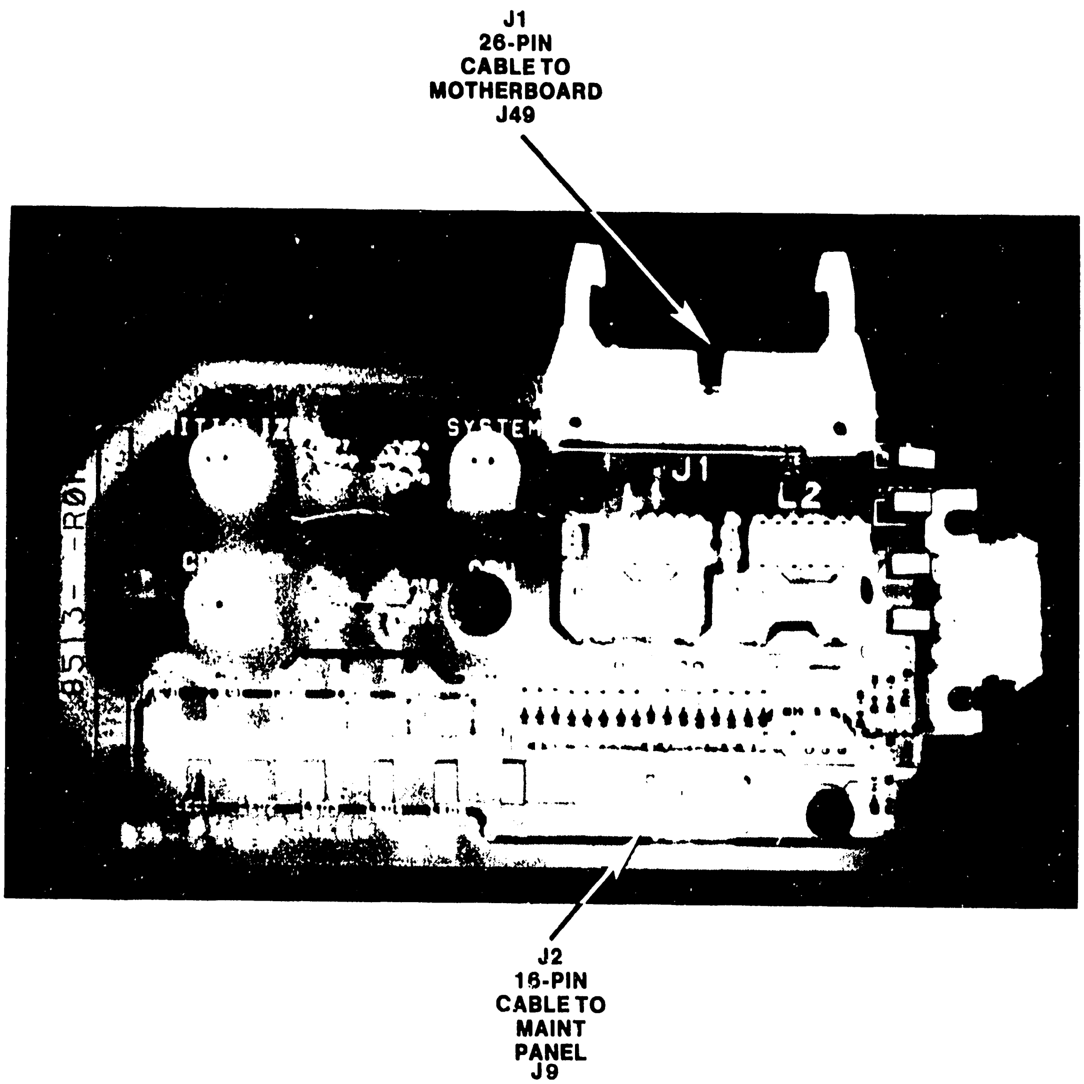


Figure 5-20. 210-8513 Display Panel Board

5.3.6.4 IOP Circuit Board Removal and Replacement

There are four different IOP assemblies used in the VS-85. The VS-85-H requires the 22V88 IOP for the NEC drive. Other IOPs are possible in the VS-85-H except the 22V28 which is not supported. The removal and replacement procedures for the different assemblies are given in the order in which they are found on the Motherboard. (Figure 5-4.)

See figure 5-22 and the appropriate documents in Class 6200 for information pertaining to IOP switch settings (except TC IOPs, figure 5-29). Make sure that the device address for each IOP is unique to that assembly.

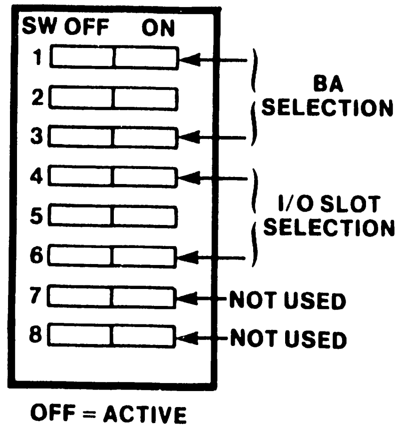
IOPs are assigned to the Motherboard slots on a priority basis, as follows:

NOTE

In the VS-85, the Operating System (OS) requires that IOP slot #0 be reserved for a 22V28 Large or 22V88 Very Large Disk Drive IOP. **The VS-85-H OS (6.30) requires a 22V88 IOP with R2 PROMs for NEC drive support. The 22V28 IOP is not supported in the VS-85-H.**

Table 5-3. VS-85/85-H IOP Priority List

IOP TYPE	WLI PART NUMBER	MOTHERBOARD PRIORITY	PHYSICAL MOTHERBOARD IOP SLOT NUMBER
22V28 Large Disk	212-3023	1	0 (4-port IOP)
22V88 Very Large Disk	212-3050	1	0 (1-port IOP)
22V88 Very Large Disk	212-3049	1	0 (2-port IOP)
22V88 Very Large Disk	212-3048	1	0 (3-port IOP)
22V88 Very Large Disk	212-3047	1	0 (4-port IOP)
22V15-2 Tape Drive	212-3030	2	1
22V25-2 Tape Drive	212-3017	2	1
22V27-2 16-Port Serial	212-3022	3	2 (1st 16-port IOP)
Workstation/Printer		4	3 (2nd 16-port IOP)
22V26-1 TC	212-3018	5	4 or 5
22V26-2 TC	212-3019	5	4 or 5
22V26-3 TC	212-3020	5	4 or 5



SW NO	4	5	6	IOP NO
	0	0	0	0
	1	0	0	1
	0	1	0	2
	1	1	0	3
	0	0	1	4
	1	0	1	5

SW NO	1	2	3	BA NO.
	1	0	0	1

OFF = 1
ON = 0

Figure 5-21. IOP Switch Settings (Except TC)

5.3.6.4.1 22V28/22V88 Disk Drive IOP Removal and Replacement

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove all connectors from the top of the 22V28 Large or 22V88 Very Large Disk IOP assembly (figures 5-23 or 5-24) in IOP slot #0 of the Motherboard. Note all the connector positions for later reassembly. (Also note that there are four versions of the 22V88 Very Large Disk IOP; 1-port, 2-port, 3-port, and 4-port. Refer to table 5-3.)
3. Once the cables are disconnected, remove the IOP assembly by grasping the top corners and gently rocking it from side-to-side while exerting a steady upward pressure. Once the assembly is free of the slot, ease it up and out of the mainframe.

NOTE

The 22V88 IOP requires R2 PROMs for NEC drive support in the VS-85-H.

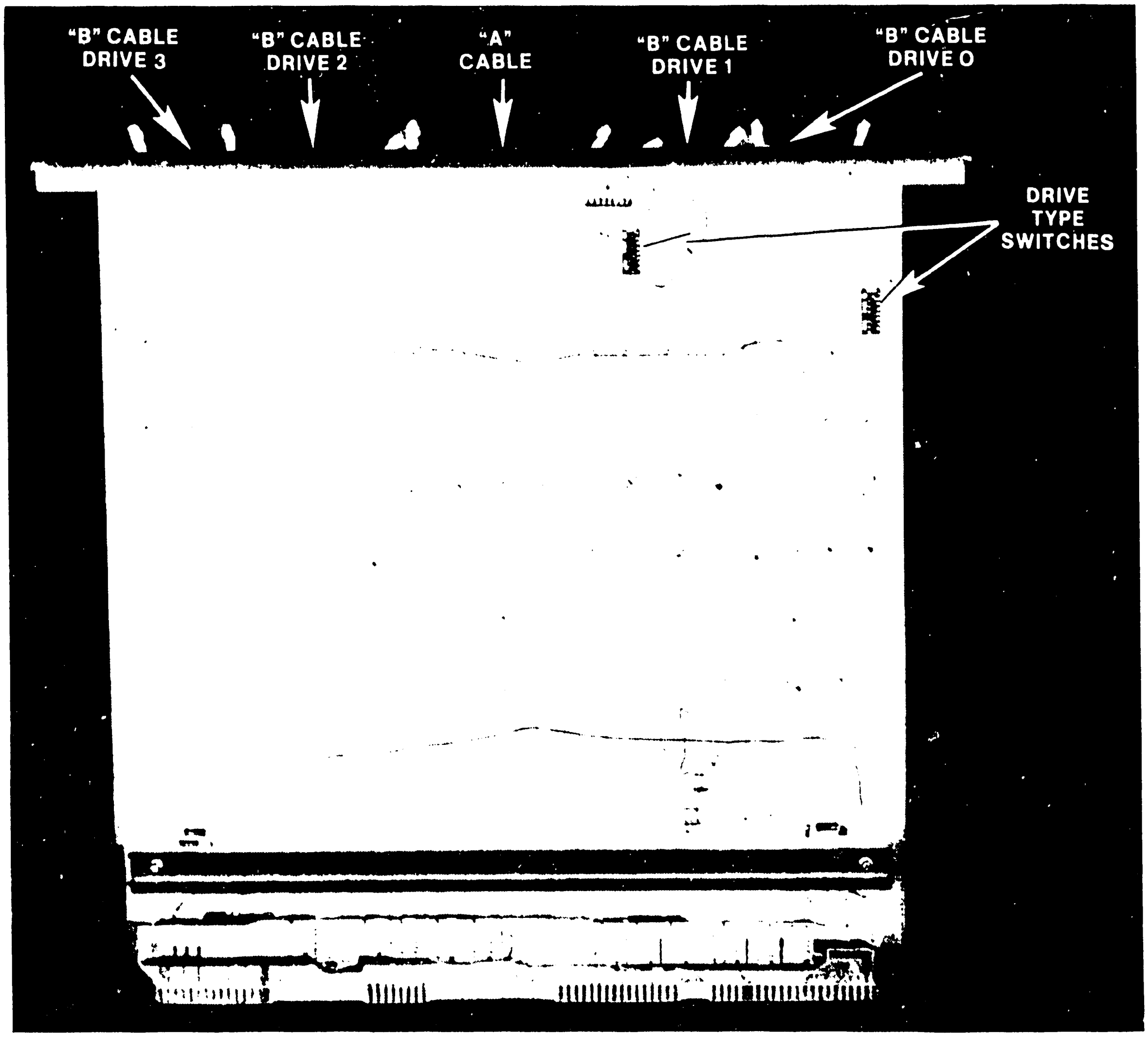


Figure 5-22. 22V28 Large Disk Drive IOP

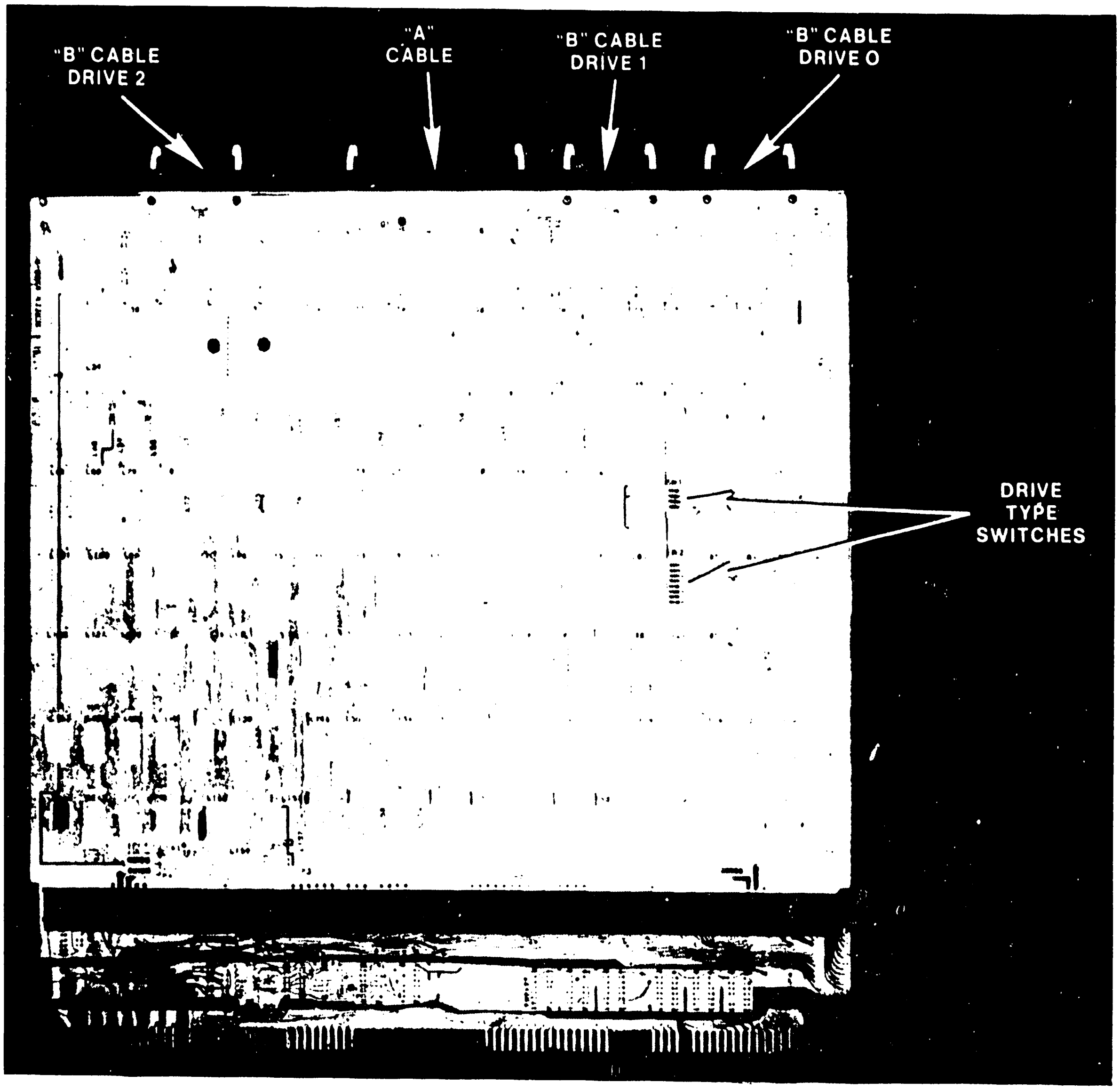
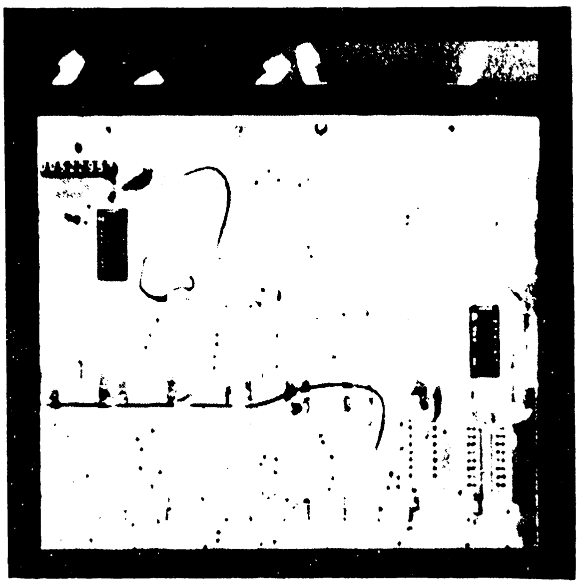


Figure 5-23. 22V88 Very Large Disk Drive IOP (3-Port Version)

4. Check the device type switches (figure 5-23 and 5-25, and table 5-4) for the type of drives connected to a 22V28 IOP. (Refer to step 9 for the 22V88 IOP device type switches.)
5. The two 8-position disk device type switches, SW1 and SW2, define the type of drive connected to the 22V28 IOP, Ports 0-3. Set the switches for the type of drive(s) connected to the IOP.
6. Check the IOP device address switch (figure 5-22).
7. Install the new 22V28 IOP assembly.
8. Reconnect all cables.



OFF	SW1	ON
PORT 0	1	L1
PORT 1	2	
PORT 2	3	
PORT 3	4	
PORT 3	5	L0
PORT 2	6	
PORT 1	7	
PORT 0	8	

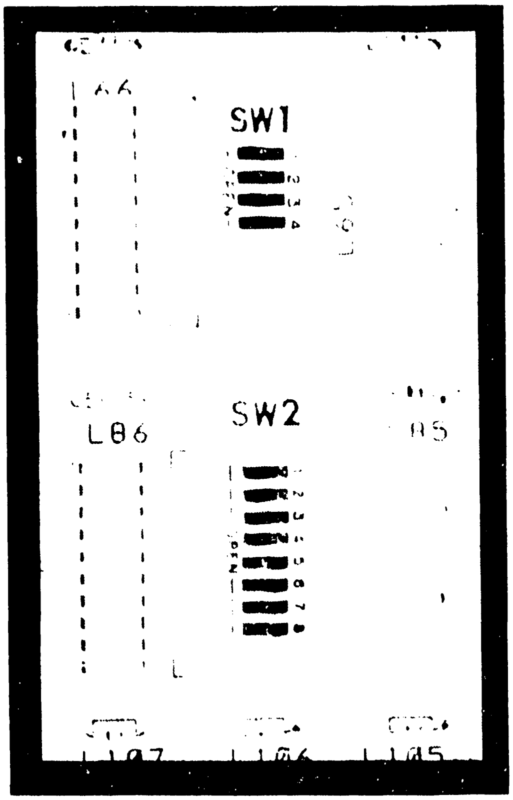
OFF	SW2	ON
PORT 0	1	L2
PORT 1	2	
PORT 2	3	
PORT 3	4	
N/A	5	NOT USED
N/A	6	
N/A	7	
N/A	8	

Figure 5-24. 22V28 Large Disk Drive
Disk Device Type Switch Settings.

Table 5-4. 22V28 Disk Drive IOP Switch Settings

DRIVE TYPE	L0	L1	L2
75MEG SMD	ON	ON	ON
288MEG SMD	ON	ON	OFF
30MEG CMD	OFF	ON	OFF
60MEG CMD	OFF	OFF	ON
90MEG CMD	OFF	OFF	OFF
NO DRIVE	ON	ON	ON

9. Check the device type switches (figure 5-24 and 5-26, and table 5-5) for the type of drives connected to a 22V88 IOP.
10. The two 8-position disk device type switches, SW1 and SW2, define the type of drive connected to the 22V88 IOP, Ports 0-3. Set the switches for the type of drive(s) connected to the IOP. On the #212-3042 (1-port) IOP, SW2 may be a half switch and SW1 may not be installed; on the #212-3043 (2-port) IOP, SW1 may not be installed; and on the #212-3044 (3-port) IOP, SW1 may be a half switch.
11. Check the IOP device address switch (figure 5-22)
12. Install the new 22V88 IOP assembly.
13. Reconnect all cables.



OPEN	SW1	CLOSED
DRIVE 3 TYPE	1	BIT 3
	2	2
	3	1
	4	0
DRIVE 2 TYPE	5	BIT 3
	6	2
	7	1
	8	0

OPEN	SW2	CLOSED
DRIVE 1 TYPE	1	BIT 3
	2	2
	3	1
	4	0
DRIVE 0 TYPE	5	BIT 3
	6	2
	7	1
	8	0

Figure 5-25. 22V88 Very Large Disk Drive Disk Device Type Switch Settings.

Table 5-5. 22V88 Disk Drive Types.

DRIVE TYPE	BIT 3	BIT 2	BIT 1	BIT 0
75 MB SMD	OPEN	OPEN	OPEN	OPEN
288 MB SMD	OPEN	OPEN	OPEN	CLOSED
30 MB CMD	OPEN	CLOSED	OPEN	OPEN
60 MB CMD	OPEN	CLOSED	OPEN	CLOSED
90 MB CMD	OPEN	CLOSED	CLOSED	OPEN
76 MB WINC	CLOSED	OPEN	OPEN	CLOSED
147 MB WINC	CLOSED	OPEN	CLOSED	OPEN
620 MB FMD	CLOSED	OPEN	CLOSED	CLOSED
NO DRIVE	CLOSED	CLOSED	CLOSED	CLOSED

5.3.6.4.2 22V27-2 Serial Device IOP Removal and Replacement

1. Remove all connectors from the top of the 22V27-2 16-Port Serial Device IOP assembly (figure 5-26) in IOP slot #2 of the Motherboard (for the first 16 serial devices) or IOP slot #3 (for the 2nd 16 serial devices). Note the position of all connectors for later reassembly. (Workstation 0 must be connected to Port #0 of IOP slot #2. This is a microcode convention and MUST be adhered to.)
2. Remove the assembly in the manner described in 5.3.5.4.1.
3. Install the new 22V27-2 IOP assembly.
4. Reconnect all cables.

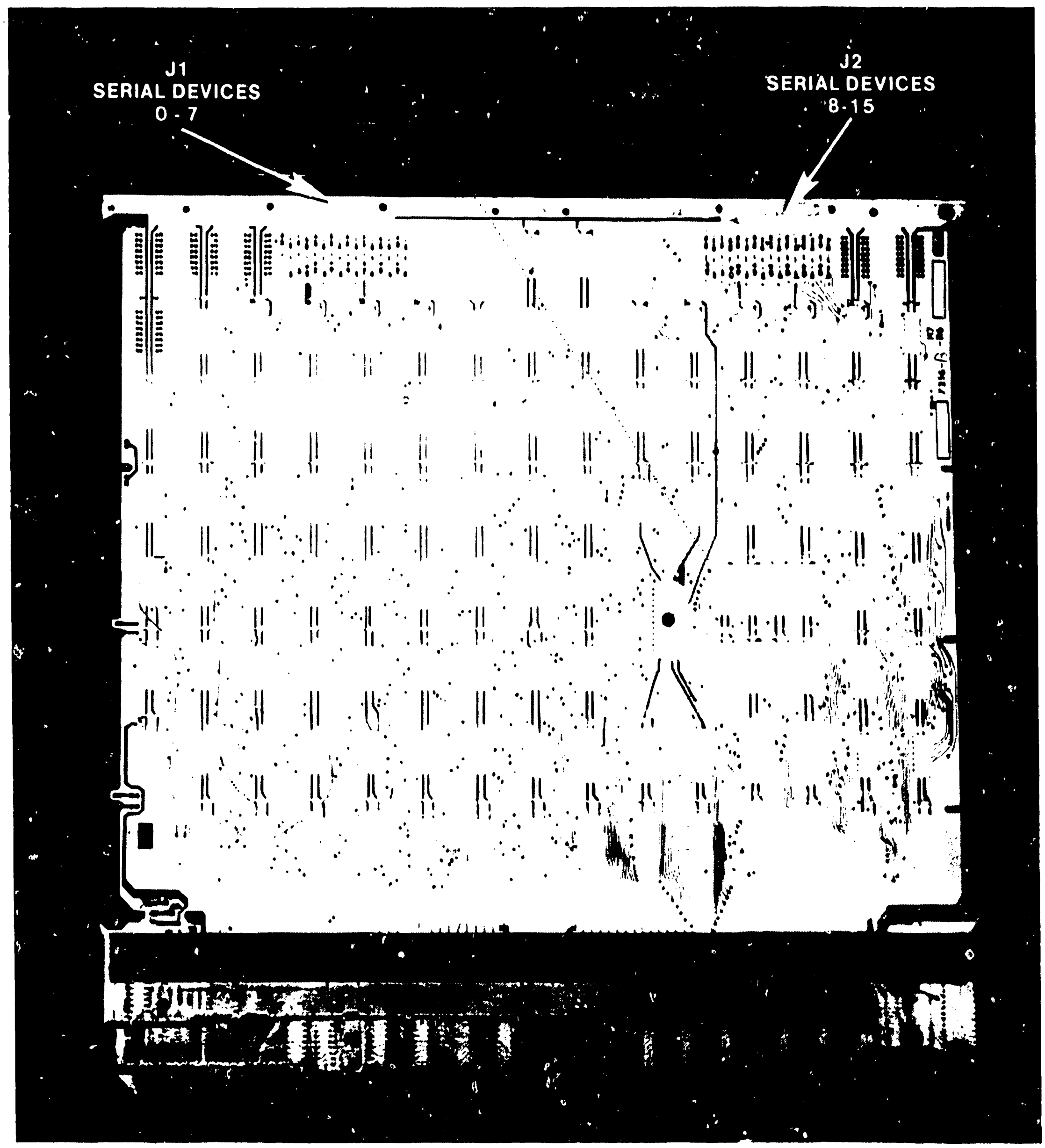


Figure 5-26. 22V27-2 16-Port Serial IOP

5. Remove and replace any other IOPs in the manner previously described, making sure of the switch settings and the position according to the Priority Table 5-3 on page 5-35.

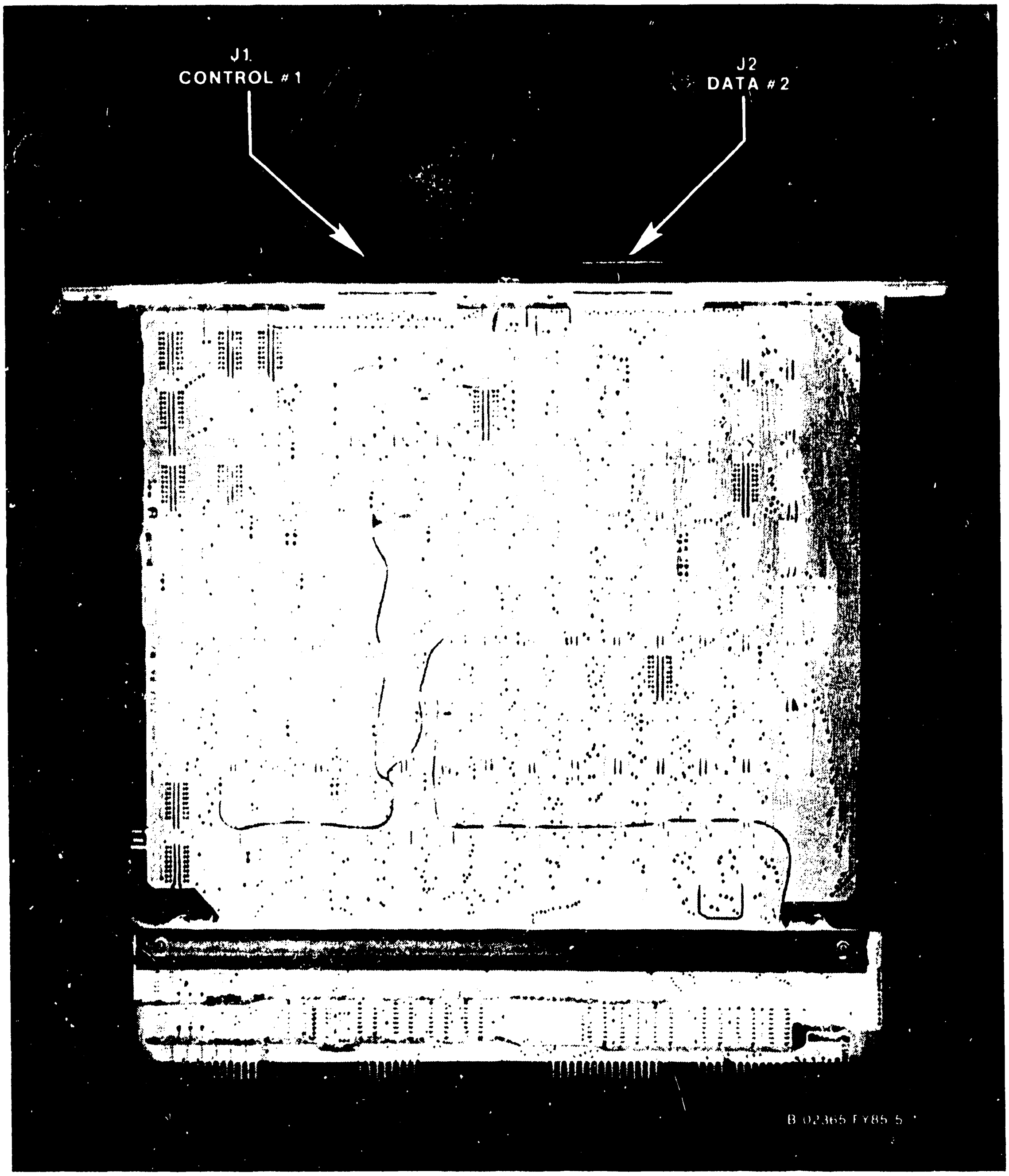


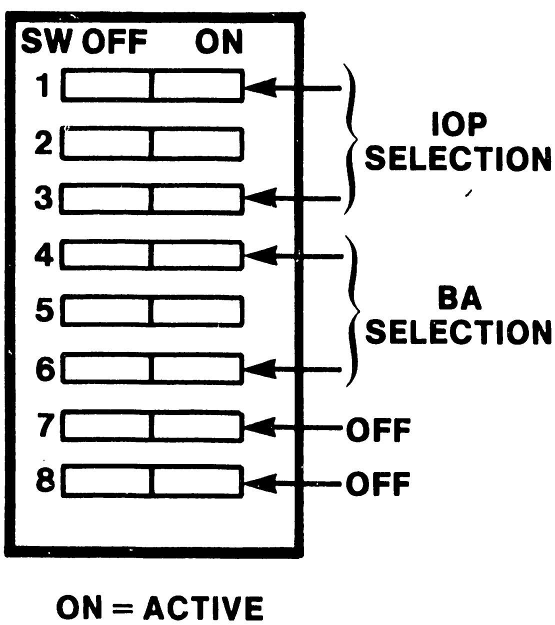
Figure 5-27. 22V25-2 Tape Drive IOP

6. Before installing the 22V26-1/2/3 TC IOP, check the TC IOP switch settings as shown in figures 5-28 and 5-29.
7. After the IOP is installed and the system has been powered on, the -12 Volt supply on the 210-7826 TC Motherboard must be checked as follows:
   a. Connect the negative lead of a digital voltmeter to the -12 Volt test point and the positive lead to the +/- 0 Volt bus. (Figure 5-29.)
   b. Adjust the trimpot (figure 5-29) until the meter reads -12 Volts, +/- 0.5 Volts.

NOTES

1. The system power supply must be adjusted to -13.6V to obtain the necessary -12V on the TC board.

2. TC I/O panels must be mounted in the top positions of the back panel where applicable.



SW NO	1	2	3	IOP NO
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5

SW NO	4	5	6	BA NO.
	0	0	1	1

ON = 1
OFF = 0

Figure 5-28. TC IOP Switch Settings

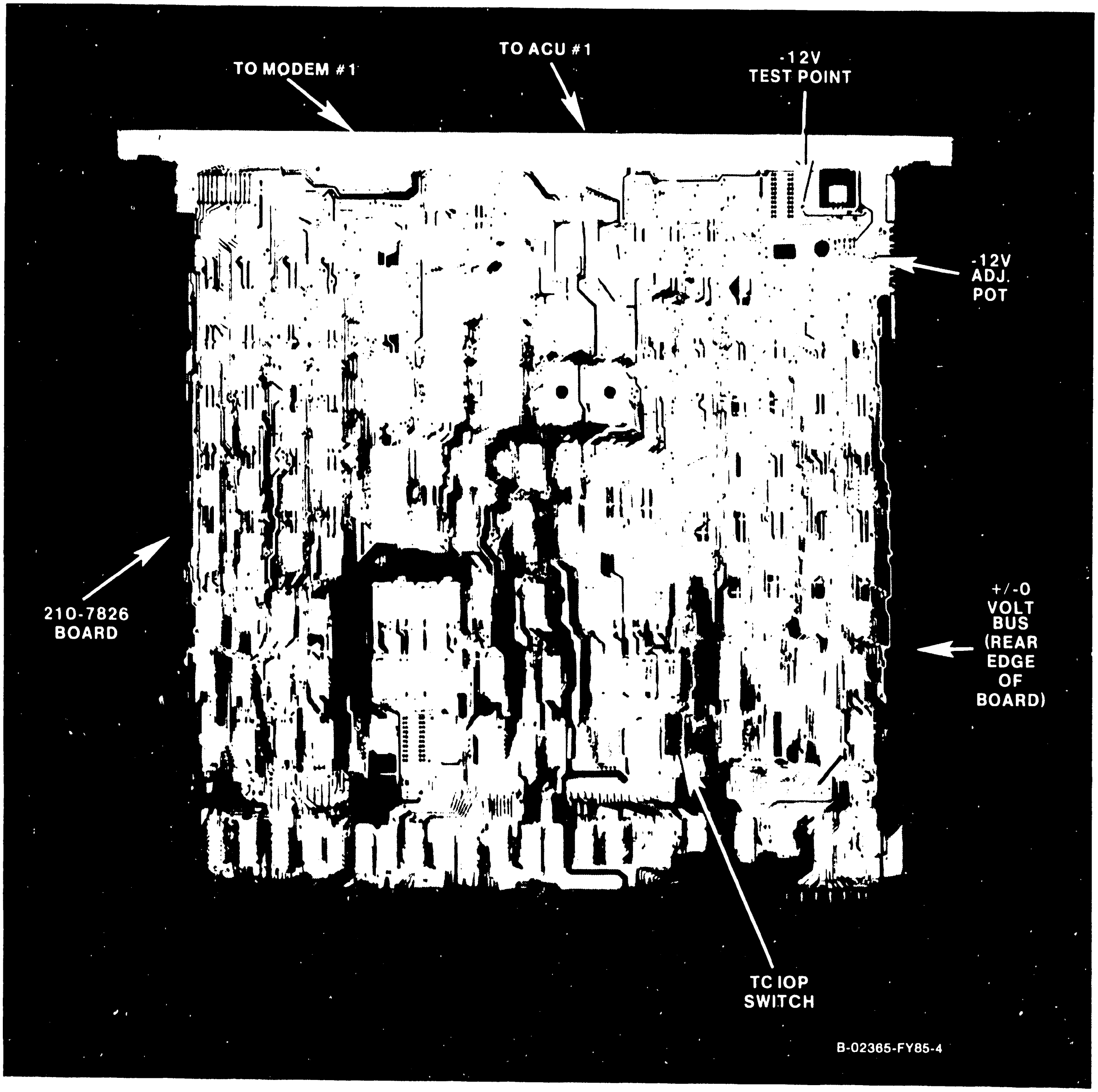


Figure 5-29. 22V26-3 TC IOP

5.3.6.5 Motherboard Removal and Replacement

Removal of the Motherboard should be done only if it has been determined conclusively that the fault is in the Motherboard. The following paragraphs describe the procedures involved in removing the VS-85/85-H Motherboard.

CAUTION

When reinstalling the Motherboard, make sure that no conductive (metal) parts of the Motherboard come in contact with the mainframe chassis. This could cause a short to ground on the Motherboard resulting in serious damage to CP boards or IOP assemblies.

5.3.6.5.1 Motherboard Removal

Remove the 210-8508 Motherboard as follows: (See figure 5-30.)

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. Remove all CP and IOP circuit boards from the Motherboard. Note the position of all cables for later reassembly. (Tables 5-2A and 5-2B.)
4. Disconnect the 4-pin power connector from J50 and the 26-pin signal connector from J49, both on the Motherboard.
5. Remove the 3/8" bolt and the 7/16" inch locknut securing the black #1/0 cable and the green wire to the +/- 0 Volt bus at the front of the Motherboard assembly.
6. With a Phillips screwdriver, loosen the screw securing the black wire to the +/- 0 Volt bus at the front of the Motherboard assembly. Remove the black wire.
7. With a 1/4" nut-driver, remove the two screws securing the top of the Display/Maintenance panel assembly to the top chassis rail. Let the top of the panel assembly tilt out and away from the mainframe.
8. With a 5/16" nut-driver, remove the two front bolts holding the Motherboard and chassis assembly to the mainframe.
9. Lower the fan assembly as described in paragraph 5.3.6.28. Remove the two Phillips screws securing the hinged cover over the fan safety screen inside the cabinet. Raise the cover, remove the screen, and turn the vertically mounted air flow baffle to the right. This allows access to the cables on the rear of the chassis assembly.
10. The rear of the Motherboard and chassis assembly is attached to the mainframe by two tabs. Pull the assembly forward about 1" to clear the tabs and allow access to the +5 Volt dc bus on the rear of the assembly.
11. Remove the 3/8" bolt and the 7/16" inch locknut securing the black #1/0 +5 Volt dc cable to the +5 Volt dc bus at the rear of the Motherboard assembly.
12. With a Phillips screwdriver, loosen the screws securing the red wire and the red/white striped wire to the +5 Volt dc bus at the rear of the Motherboard assembly. Remove the wires.

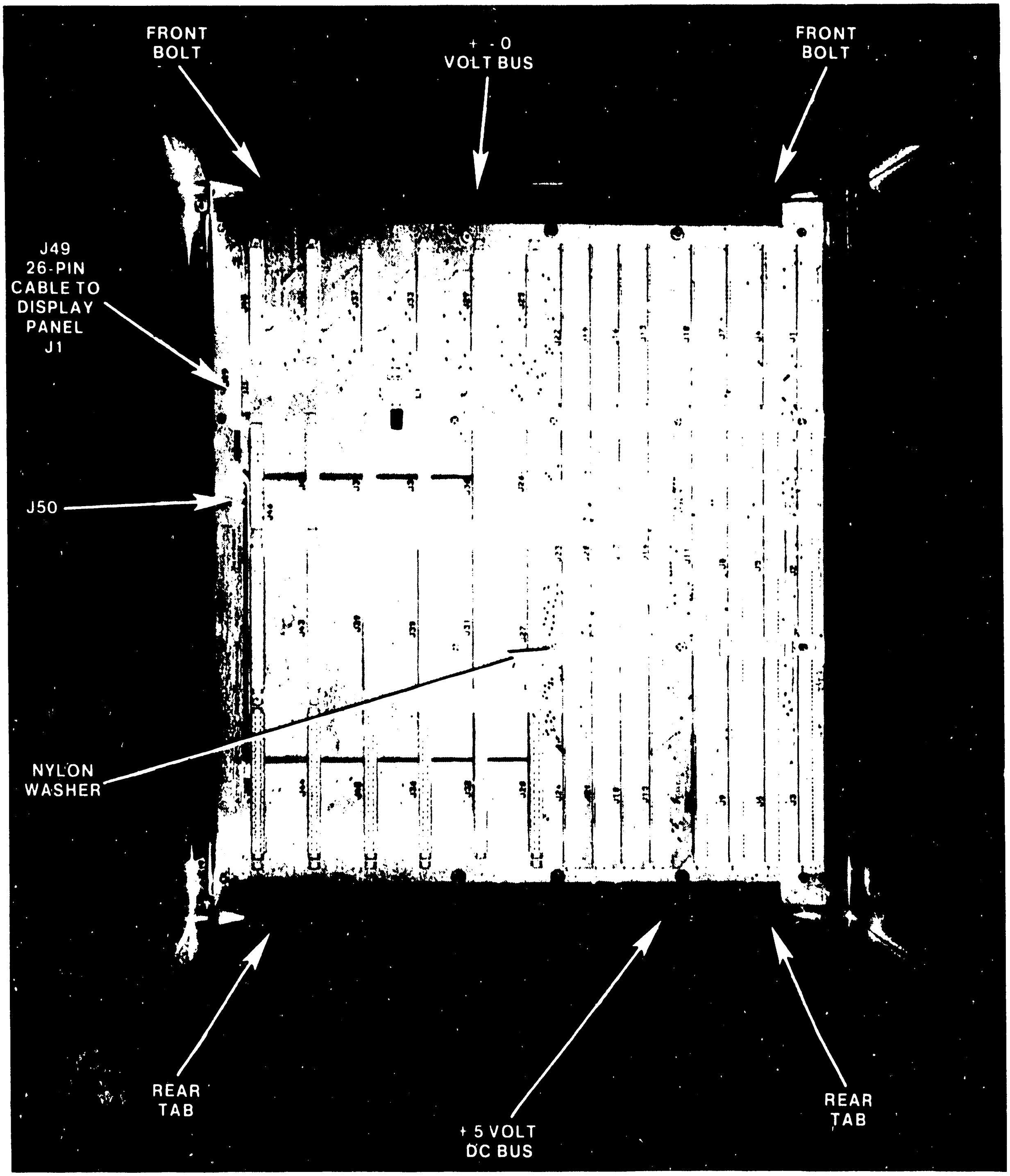


Figure 5-30. Motherboard Removal

13. Lift the Motherboard and chassis assembly straight up and out of the mainframe and place it on the floor.
14. With a Phillips screwdriver, remove the 24 screws located on the outer edges and between the the card slots of the Motherboard. (Note that the screw located between J23, J24, and J27 has a nylon insulating washer.)
15. Separate the Motherboard from the rest of the assembly.

5.3.6.5.2 Motherboard Replacement

1. To reinstall the Motherboard, reverse the removal procedure.
2. Make sure that all screws and nuts are reinstalled in their proper locations. Do not overtighten the 24 phillips screws or they will strip the nylon stand-offs on the Motherboard assembly. Remember that the screw located between J23, J24, and J27 has a nylon insulating washer.
3. Make sure that all wires, cables, and connectors are installed correctly.
4. Make sure that the black #1/0 +5 Volt dc cable on the rear of the Motherboard assembly does not touch the mainframe chassis.
5. Make sure that no metal part of the Motherboard touches the mainframe chassis (see CAUTION in paragraph 5.3.6.5).
6. Carefully reinstall all circuit boards according to figure 5-4 and make sure that all board cabling is installed correctly.

5.3.6.6 Display/Maintenance Panel Assembly Removal

The top of the Display/Maintenance panel assembly in the VS-85/85-H is attached to the top chassis rail of the mainframe by two screws and a chain cable. The bottom of the assembly rests in a slot that allows the top of the assembly to tilt out and away from the mainframe. Remove the Panel Assembly as follows: (See figures 5-31, 5-32, 5-33, and 5-34.)

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. With a 1/4" nut-driver, remove the two screws securing the top of the Display/Maintenance panel assembly to the top chassis rail. Let the top of the panel assembly tilt out and away from the mainframe.
4. Disconnect the chain cable.
5. Disconnect the 3-pin power connector from J3 and the 26-pin signal connector from J1, both on the 210-8513 Display Panel board.
6. Disconnect the 2-pin power connector from J1 and the 26-pin signal connectors from J2 and J3, all on the 210-7614 Maintenance Panel board.
7. Disconnect the 16-pin connector at location SW1 of the 210-7602 Control Memory board. (Figure 5-5.)
8. Disconnect the 60-pin connectors from J1 and J2 of the 210-7602 Control Memory board. (Figure 5-5.)
9. Disconnect the 6-pin power connector from J3 and the 2-pin power connector from J4, both on the 210-7610 Mini-diskette Drive Controller board.

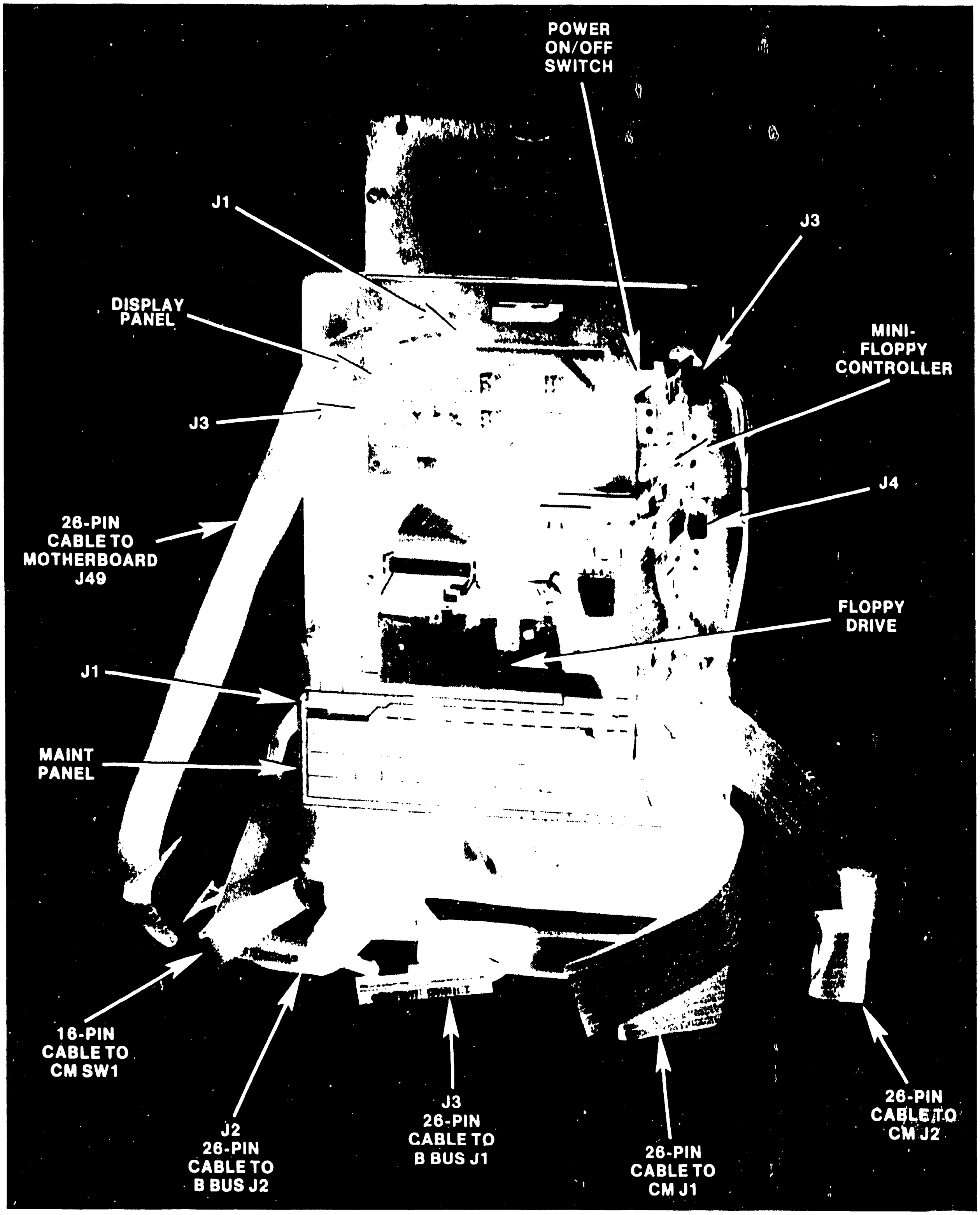


Figure 5-31. Rear View of Display/Maintenance Panel Assembly

10. Disconnect the two wires from the Display Panel Power On/Off switch.
11. Being careful of the cables still attached, lift the entire Display/-Maintenance panel assembly up and out of the mainframe. Lay the assembly face down on the floor on a piece of padded material.

5.3.6.7 Display/Maintenance Panel Assembly Replacement

1. To reinstall the Display/Maintenance Panel Assembly, reverse the removal procedure. Secure the assembly, before reconnecting the cables, by reinstalling the chain cable as soon as the assembly is put back into the mainframe.
2. Make sure that all wires and connectors are installed correctly.

5.3.6.8 Display Panel Board Removal

Remove the 210-8513 Display Panel board as follows: (Figure 5-32)

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. With a 1/4" nut-driver, remove the two screws securing the top of the Display/Maintenance panel assembly to the top chassis rail. Allow the top of the panel assembly to tilt out and away from the mainframe.
4. Disconnect the 3-pin power connector from J3 of the 210-8513 Display Panel board.
5. Disconnect the 16-pin connector from J2 and the 26-pin connector from J1, both on the board.
6. Remove the five Phillips screws from the stand-offs on the board.
7. Remove the board.

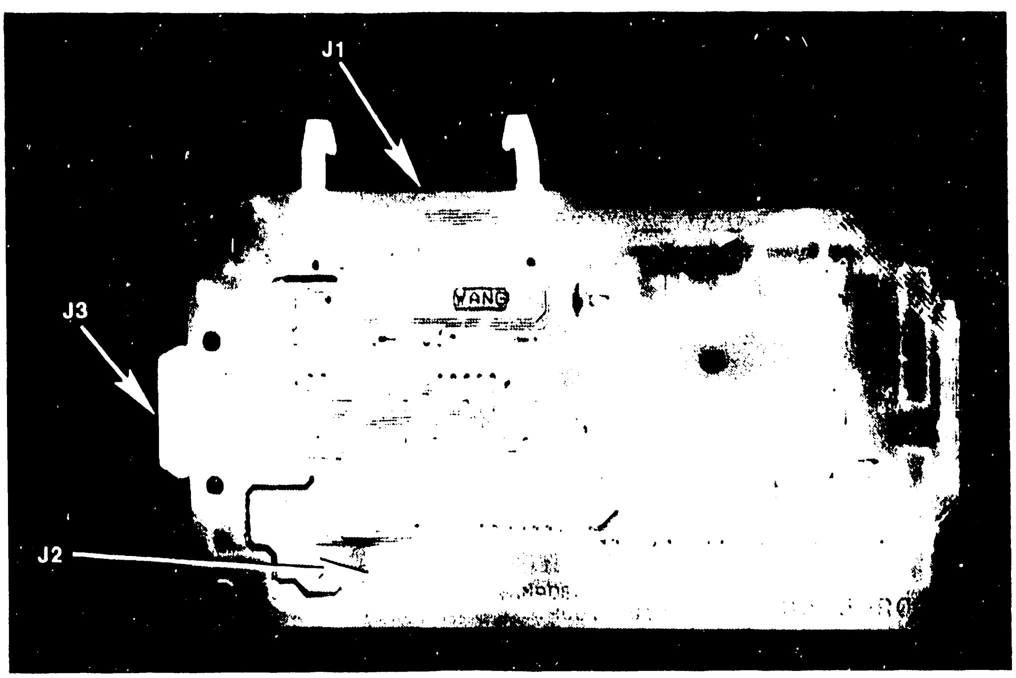


Figure 5-32. Display Panel Board Removal

5.3.6.9 Display Panel Board Replacement

1. To reinstall the Display Panel board, reverse the removal procedure.
2. Make sure that all connectors are installed correctly.

5.3.6.10 Maintenance Panel Board Removal

Remove the 210-7614 Maintenance Panel board as follows: (See figure 5-33.)

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. Remove the complete Display/Maintenance panel assembly as described in paragraph 5.3.6.6.
4. With the Display/Maintenance panel assembly out on the floor, unscrew the black Step pushbutton cap from the front of the Maintenance Panel board.
5. Remove the 210-7610 Mini-diskette Drive Controller board (paragraph 5.3.6.12).
6. Remove the six Phillips screws from the 210-7614 Maintenance Panel board stand-offs and carefully lift off the board with the cables still connected.
7. Disconnect the 16-pin connectors from J7 and J12 of the board.
8. Disconnect the 34-pin connectors from J4, J5, and J6 of the board.
9. Remove the board.

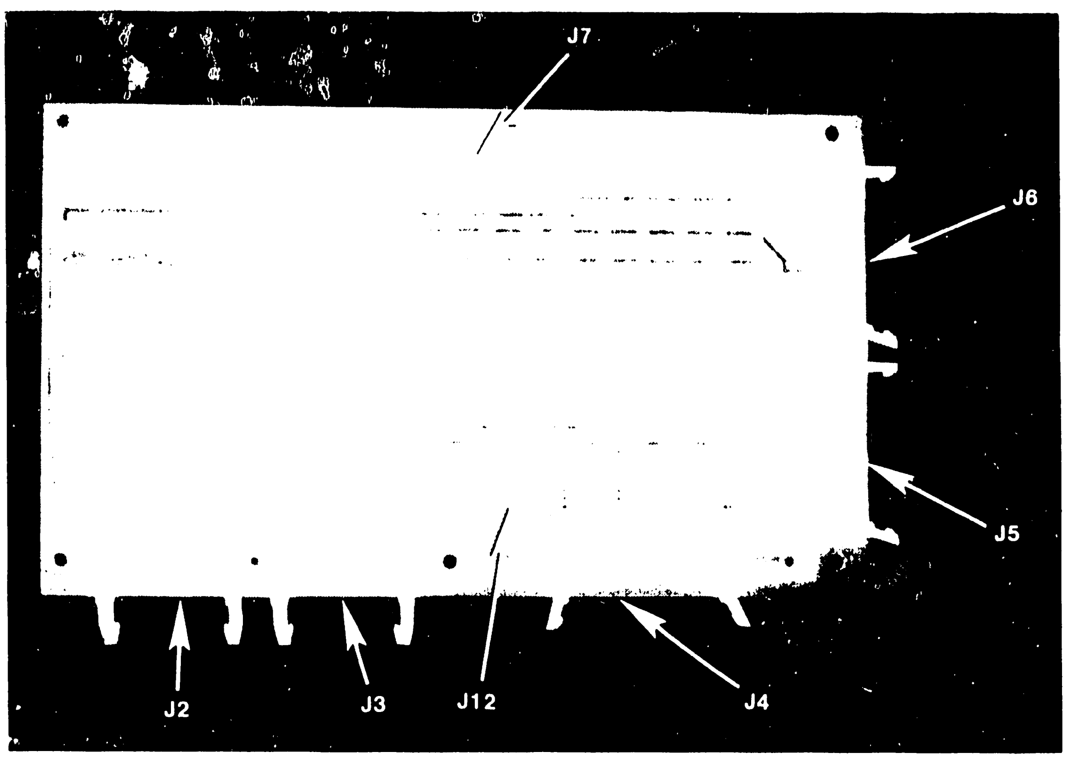


Figure 5-33. Maintenance Panel Board Removal

5.3.6.11 Maintenance Panel Board Replacement

1. To reinstall the Maintenance Panel board, reverse the removal procedure.
2. Reinstall the 210-7610 Mini-diskette Drive Controller board.
3. Reinstall the Display/Maintenance panel assembly.
4. Make sure that all wires and connectors are installed correctly.

5.3.6.12 Minifloppy Drive Controller Board Removal

Remove the 210-7610 Minidiskette Drive Controller board as follows: (See figure 5-34.)

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. Remove the complete Display/Maintenance panel assembly as described in paragraph 5.3.6.6.
4. Disconnect the 4-pin power connector from J2 of the 210-7610 Minidiskette Drive Controller board.
5. Disconnect the 34-pin connector from J1 on the top of the board and the 34-pin connector from J6 on the left side of the board.
6. Remove the four Phillips screws from the board. (Note that the screw located above L9 has a nylon insulating washer.)
7. Remove the board.

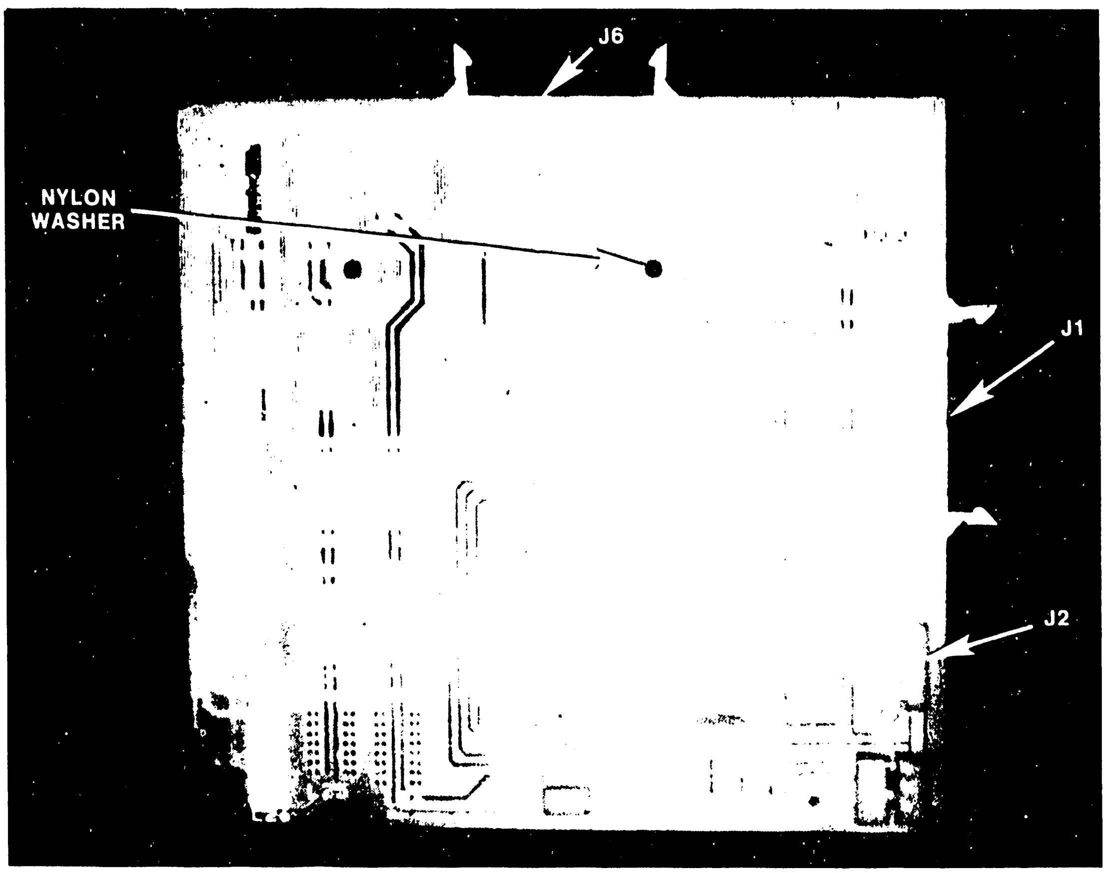


Figure 5-34. Minidiskette Drive Controller Board Removal

5.3.6.13 Minifloppy Drive Controller Board Replacement

1. To reinstall the Controller board, reverse the removal procedure.
2. Remember the screw located above L9 has a nylon insulating washer.
3. Reinstall the Display/Maintenance panel assembly.
4. Make sure that all wires and connectors are installed correctly.

5.3.6.14 Minifloppy Drive Removal

Remove the Minidiskette Drive as follows: (See figure 5-35.)

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. Remove the complete Display/Maintenance panel assembly as described in paragraph 5.3.6.6.
4. Remove the 210-7610 Minidiskette Drive Controller board as described in paragraph 5.3.6.12.
5. Disconnect the 4-pin power connector from J2 and the 34-pin signal connector from J1, both on the minidiskette Drive.
6. Loosen the four Phillips screws (in the VS-85-H, two screws, cross-corner) securing the drive to the bracket.
7. Slide the whole drive assembly up far enough to allow the screws to clear the screw slots.
8. Remove the drive.

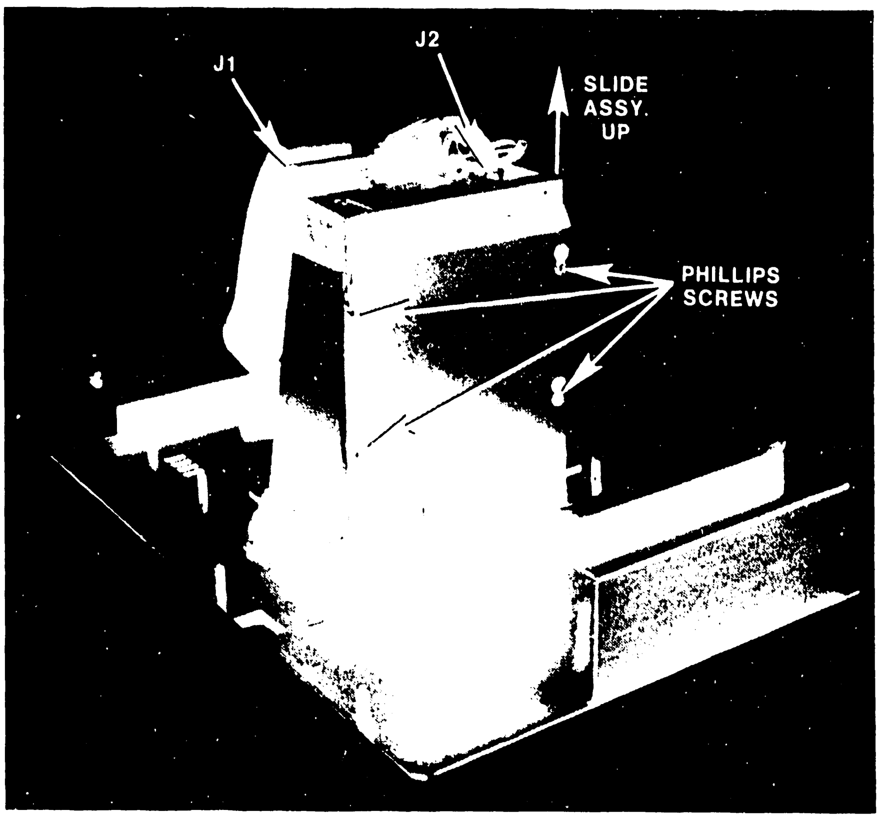


Figure 5-35A. VS-85 Minidiskette Drive Removal

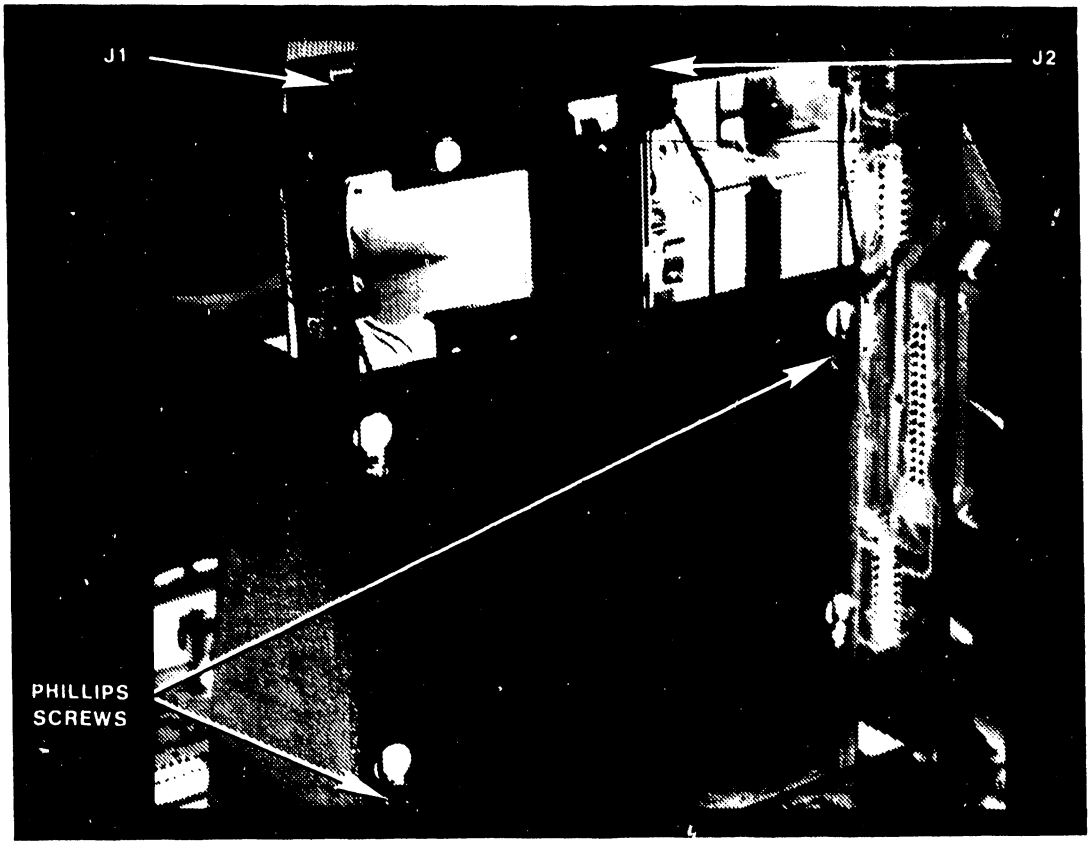


Figure 5-35B. VS-85-H Half-height Minidiskette Drive Removal

5.3.6.15 Minifloppy Drive Replacement

CAUTION

In the VS-85-H, be sure to reinstall the half-height drive with only two screws in a cross-corner manner. Otherwise, the drive will not be level on the mounting bracket.

1. To reinstall the Minidiskette Drive, reverse the removal procedure.
2. Reinstall the Minidiskette Drive Controller board.
3. Reinstall the Display/Maintenance panel assembly.
4. Make sure that all wires and connectors are installed correctly.

5.3.6.16 NEC Disk Drive Removal

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. Loosen the two screws at the top of the Display/Maintenance Panel and slide the Control Panel up and over to the right. Retighten the screws to secure the Control Panel in this position.
4. Remove the two screws that secure the drive bracket to the baseplate. (Refer to figure 5-36.)
5. Slide the drive assembly forward and lift it out of the cabinet.

6. Unplug the "A" cable from connector P1.
7. Disconnect the "B" cable from connector P2.
8. Unplug the adapter cable from P3.
9. Remove the four screws that secure the disk drive to the bracket and remove the drive.

NOTE

1. The entire NEC disk drives are NOT field replaceable units (FRUs). Refer to Table 7-1 for a list of FRUs within the disk drives and to the NEC disk drive maintenance manuals (WLI P/N 729-1452 and 729-1503) for instructions on how to replace the FRUs.

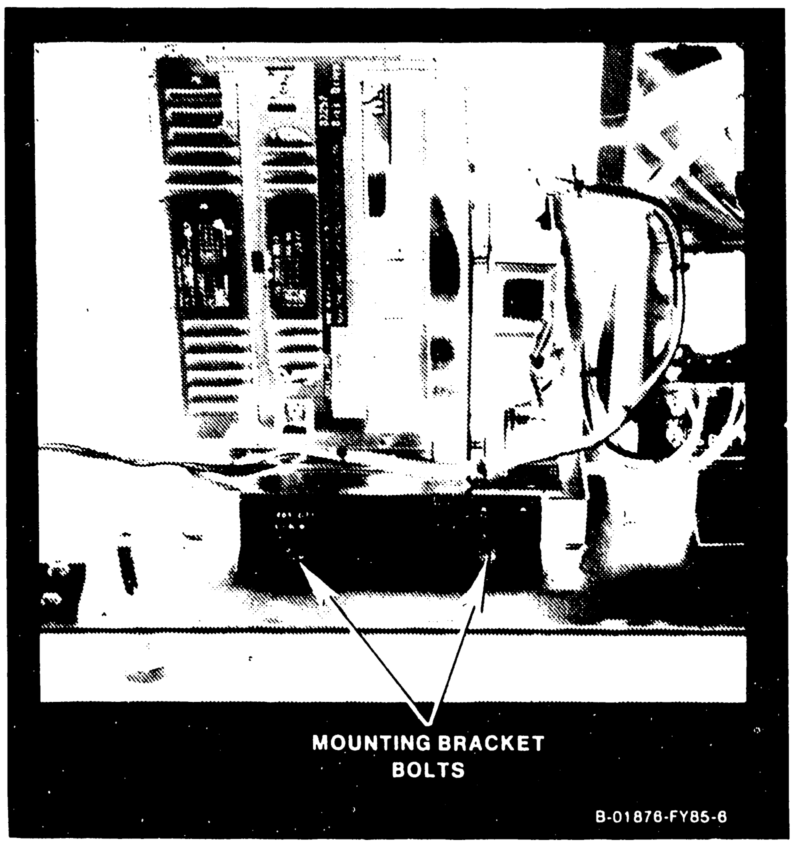


Figure 5-36. NEC Disk Drive Removal

5.3.6.17 NEC Disk Drive Replacement

1. To reinstall the NEC disk drives, reverse the removal procedure.
2. Ensure that all connectors are properly seated.
3. The back of the drive bracket fits into a bracket mounted at the rear of the baseplate.
3. Refer to paragraph 4.12 and perform the COLDSTART procedure.
4. IPL the system and check disk drive for proper operation.

5.3.6.18 +24-Volt Power Supply Removal

WARNING

Electrical shock hazard. Power down mainframe, unplug power cable, and wait one to two minutes before removing the +24-volt power supply.

1. Remove the Power Distribution Unit (PDU) as described in paragraph 5.3.6.28. It is only necessary to unplug the +24-volt plug at the DISK 1 connector on the PDU.
2. Remove the fixed disk drive as described in paragraph 5.3.6.16, excluding step 9.
3. Slide out the Power Sequencer board to the right of the Switching Power Supply and disconnect the plug at J8 on the board.
4. Carefully tip the disk drive assembly on its left side and remove the four screws (three if LH supply) that secure the +24-volt supply to the disk drive bracket.
5. Remove the power supply.

5.3.6.19 +24-Volt Power Supply Replacement

1. To reinstall the +24-volt power supply, reverse the removal procedure.
2. Ensure that the connectors are properly seated.
3. If the supply is an LH, be sure to install the lexan shield.
4. Power up mainframe and check voltage (paragraph 5.2.6.1).

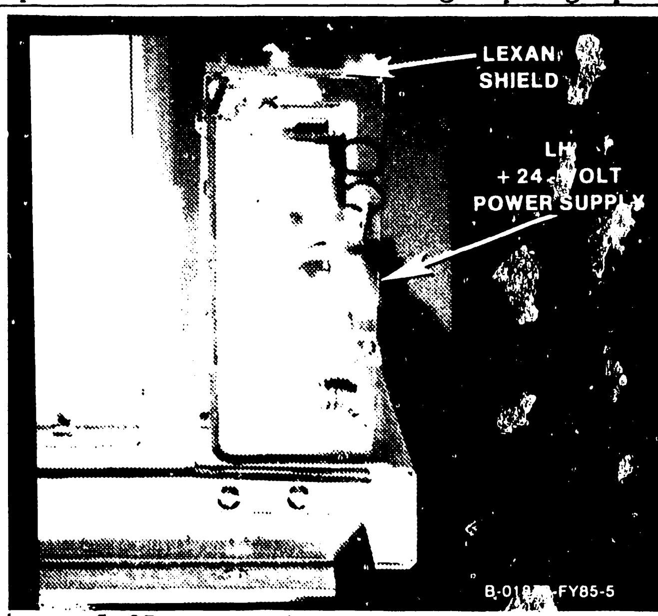


Figure 5-37. LH +24-volt Power Supply Replacement

5.3.6.20 Switching Power Supply Removal

Remove the power supply as follows: (Figures 5-30, 5-38A, 5-38B, 5-39.)

WARNING

```
*****************************************************************
*                                                               *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY           *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND             *
*    CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN           *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.      *
*                                                               *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER               *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                      *
*                                                               *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC      *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,          *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO       *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO          *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                       *
*                                                               *
*****************************************************************
```

1. After depressing the Power On/Off switch to the "0" position and turning off the mainframe ac On/Off circuit breaker, remove the top and front covers.

2. With a 5/16" open end wrench, remove the two bolts securing the front of the power supply assembly to the base of the mainframe cabinet. These are bolt and locknut combinations. Hold the locknuts underneath the cabinet while removing the bolts.
3. The rear of the assembly is attached to the mainframe by two tabs. Pull the assembly forward about 1" to clear the tabs. In the VS-85, turn the supply to the left to allow access to the #1/0 +/- 0 vdc cable, the #1/0 +5 Volt dc cable, and the cables on the 210-8250 Power Controller board. **(In the VS-85-H, slide the 210-8198 Power Sequencer board out of its board guides to access the connectors.)**
4. Remove the 3/8" bolts and the 7/16" inch locknuts securing the black #1/0 +/- 0 Volt cable and the black #1/0 +5 Volt dc cable to the "antler" assembly on the front of the power supply.
5. Disconnect the 4-pin power connector from J50 of the Motherboard.
6. Disconnect the 12-pin connector from J2 **(SPS in the VS-85-H)** of the Power Filter Assembly.
7. Note the orientation of the 6-pin connector at J6 of the 210-8250 Power Controller board **(J11 of the 210-8198 Power Sequencer board)** and then remove the connector from J6/**J11**.
8. Disconnect the 3-pin connector from J2, the 9-pin connector from J4/**J3**, and the 2-pin connector from J5, all on the Power Controller/**Power Sequencer** board.
9. Remove the power supply assembly.
10. Disconnect the 15-pin connector from J1 of the Power Controller board.
11. Tip the power supply assembly on it's side.

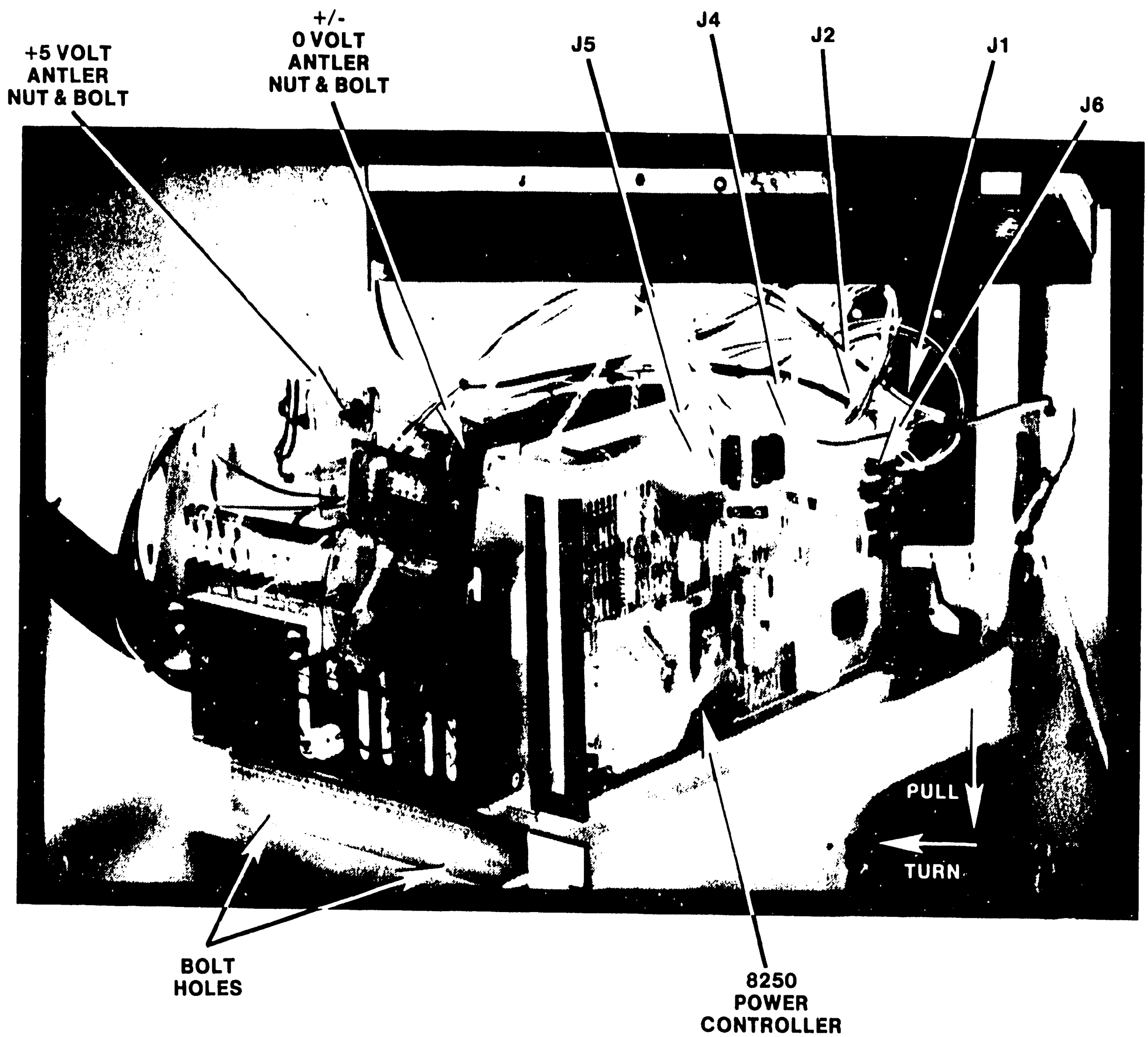


Figure 5-38A. VS-85 Switching Power Supply Removal

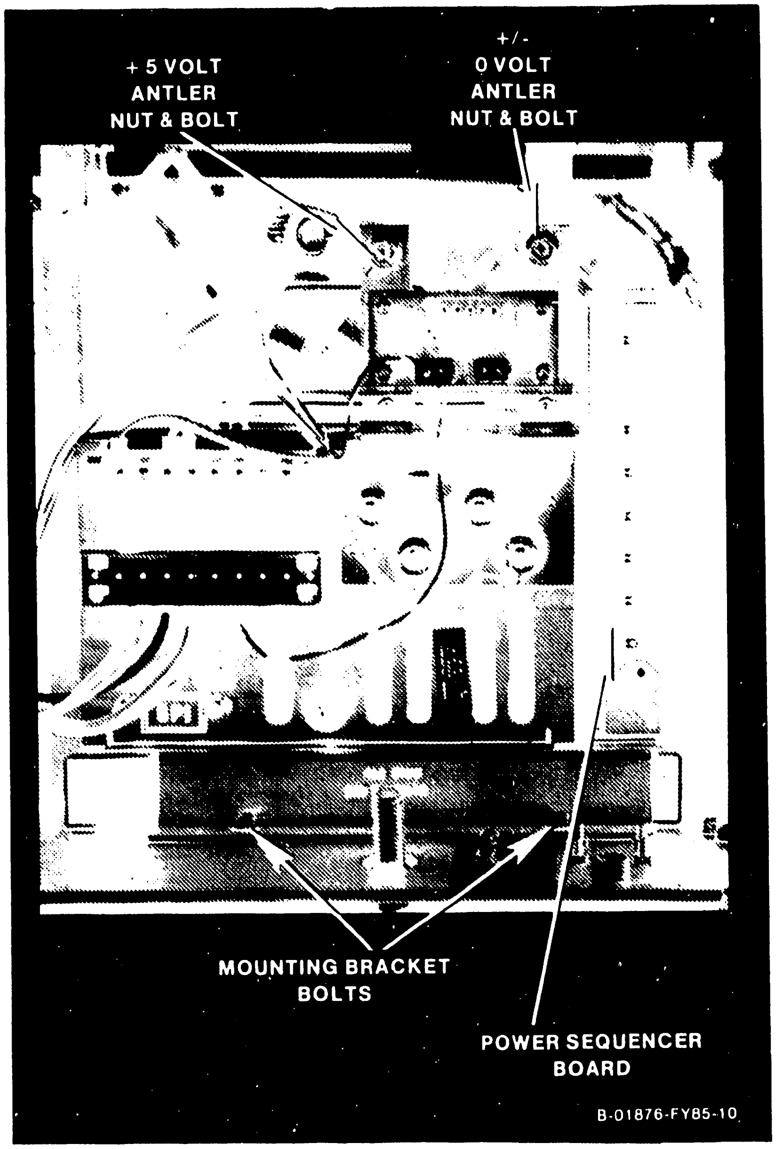


Figure 5-38B. VS-85-H Switching Power Supply Removal

12. With a 1/4" nut-driver, remove the four screws from the bottom of the power supply.
13. Remove the power supply.

NOTE

Retain the Power Controller Board or Power Sequencer Board and the power supply base plate for reinstallation of the Switching Power Supply.

5.3.6.21 Switching Power Supply Replacement

1. To reinstall the Switching Power Supply, reverse the removal procedure.
2. Note which vendor's switching power supply is the replacement supply. If it is a Powertec supply, it has a 115/230V Line Select Switch. Check the switch at the rear of the supply to make sure it is set to the 115 Vac position. This applies to VS-85 systems.
3. Make sure that the 6-pin connector at J6 of the Power Controller board is reinstalled in the correct orientation. This connector can be forced on upside down. (Even though connectors J6 through J9 are common connectors, use J6.)
4. Make sure that all other wires and connectors are installed correctly. (Even though connectors J3 and J4 of the Power Controller board are common connectors, use J4.)
5. Power up the system and check and adjust, if necessary, the power supply voltages as described in paragraph 5.2.6.1

5.3.6.22 Power Controller Board Removal

Remove the 210-8250 Power Controller board as follows:

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the top and front covers.
3. Remove the power supply assembly as described in paragraph 5.3.6.20. There is no need to do steps 11 through 13 of the power supply removal procedure.
4. Remove the six Phillips screws from the stand-offs on the Power Controller board.
5. Remove the board.

5.3.6.23 Power Controller Board Replacement

1. To reinstall the Power Controller board, reverse the removal procedure.
2. Set the 115/230V Line Select Switch on the Power Controller board to the 115 Vac position. This applies to ALL VS-85 systems.
3. Make sure that the 6-pin connector at J6 of the Power Controller board (figure 5-38A) is reinstalled in the correct orientation. This connector can be forced on upside down. (Even though connectors J6 through J9 are common connectors, use J6.)

4. Make sure that all other wires and connectors are installed correctly. (Even though connectors J3 and J4 of the Power Controller board are common connectors, use J4.)
5. Reinstall the power supply assembly.
6. Power up the system and check and adjust, if necessary, the power supply voltages as described in paragraph 5.2.6.1

5.3.6.24 Power Sequencer Board (210-8198) Removal

1. **Depress the Power On/Off switch to the "O" position and turn off the mainframe ac On/Off circuit breaker.**
2. **Remove the top and front covers.**
3. **Slide out the Power Sequencer board from the board guides to the right of the switching power supply. (Figure 5-38B.)**
4. **Unplug the connectors from the board and remove the board.**

5.3.6.25 Power Sequencer Board Replacement

1. **To reinstall the Power Sequencer board, reverse the removal procedure.**
2. **Be sure that all connectors are installed properly.**
3. **Power up the system and check and adjust, if necessary, the power supply voltages as described in paragraph 5.2.6.1.**

5.3.6.26 Power Filter Assembly Removal

The Power Filter Assembly is mounted in the back panel of the VS-85. Remove the Power Filter Assembly as follows: (See figure 5-39A.)

WARNING

Because of the high operating voltages passing through the Power Filter Assembly, power down the mainframe and disconnect the mainframe power connector from the power source receptacle before performing the following removal/replacement procedures.

1. After powering down the mainframe and disconnecting the mainframe power connector from the power source receptacle, remove the 20 Phillips screws securing the Power Filter Assembly to the rear of the mainframe cabinet.
2. Pull the assembly out far enough to the rear to access the cables connected to the front of the assembly.
3. Remove the 3-pin connector from J1 and the 12-pin connector from J2, both on the assembly.
4. Remove the assembly.

5.3.6.27 Power Filter Assembly Replacement

1. To reinstall the Power Filter Assembly, reverse the removal procedure.

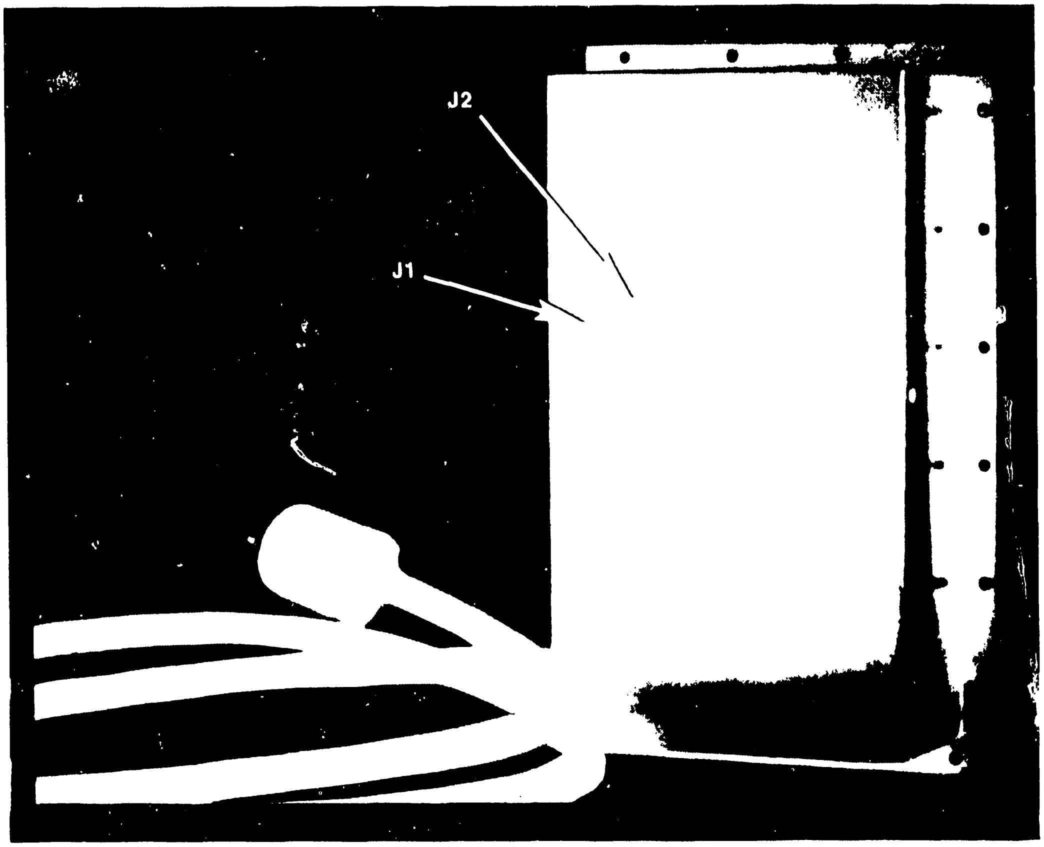


Figure 5-39A. VS-85 Power Filter Assembly Removal

5.3.6.28 Power Distribution Unit Removal

The Power Distribution Unit (PDU) is mounted on the lower left part of the back panel of the VS-85-H. Remove the PDU as follows: (See figure 5-39B.)

WARNING

Because of the high operating voltages passing through the PDU, power down the mainframe and disconnect the mainframe power connector from the power source receptacle before performing the following removal/replacement procedures.

1. After heeding the warning above, remove the 20 nuts that secure the PDU to the studs on the rear panel.
2. Pull the PDU out of the back panel far enough to access the five connectors attached to the PDU.
3. Unplug the 24-volt disk drive connector, the fan connector, the Power Sequencer board connector, and the On/Off Switch connector from the PDU.
4. Remove the PDU.

5.3.6.29 Power Distribution Unit Replacement

1. To replace the VS-85-H PDU, reverse the removal procedure.
2. Ensure that all connectors are reinstalled.
3. Power up the mainframe and ensure proper operation.

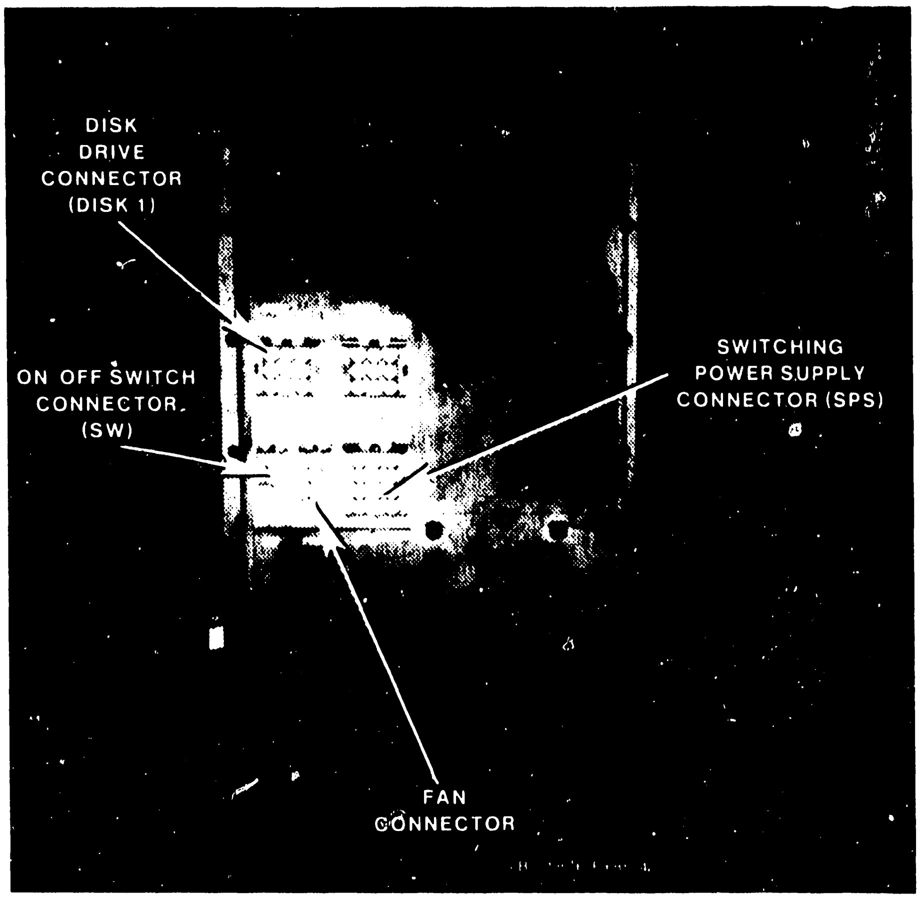


Figure 5-39B. VS-85-H Power Distribution Unit Removal

5.3.6.30 Fan Removal

WARNING

> Because of the high current passing through the fans at the rear of the chassis, power down the mainframe and place the circuit breaker in the OFF position before performing the following procedures.

The six cooling fans used in the VS-85/85-H are mounted on a hinged panel assembly. Before an individual fan can be removed, the panel assembly must be lowered. The following paragraphs describe the procedures involved in lowering the panel and removing a fan.

Remove a damag.d or defective muffin fan as follows:

1. Depress the Power On/Off switch to the "0" position and turn off the mainframe ac On/Off circuit breaker.
2. Remove the four Phillips screws securing the fan filter assembly to the back panel. (Figure 5-40.) Remove the filter assembly.
3. Grasp the catch inside the top of the panel and pull the top out. Lower the panel down to the horizontal position. (Figure 5-41.)
4. Disconnect the plug on the lower right corner of the fan to be removed.
5. Remove the four Phillips screws securing the fan to the fan panel.
6. Remove the fan.

5.3.6.31 Fan Replacement

1. To install a fan, reverse the above procedure.
2. Power up the system and check that all the fans are operating properly.

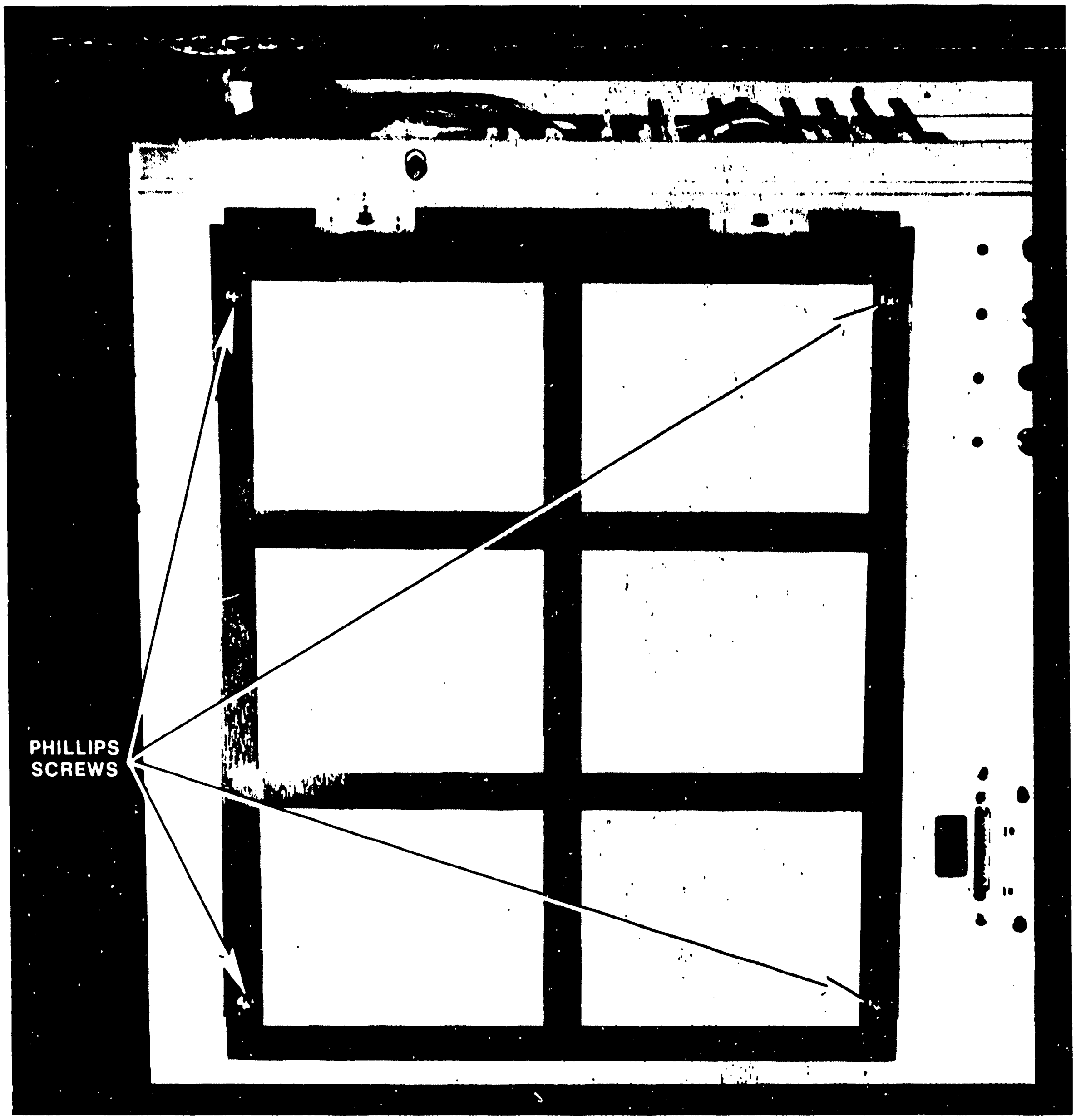


Figure 5-40. Fan Filter Assembly

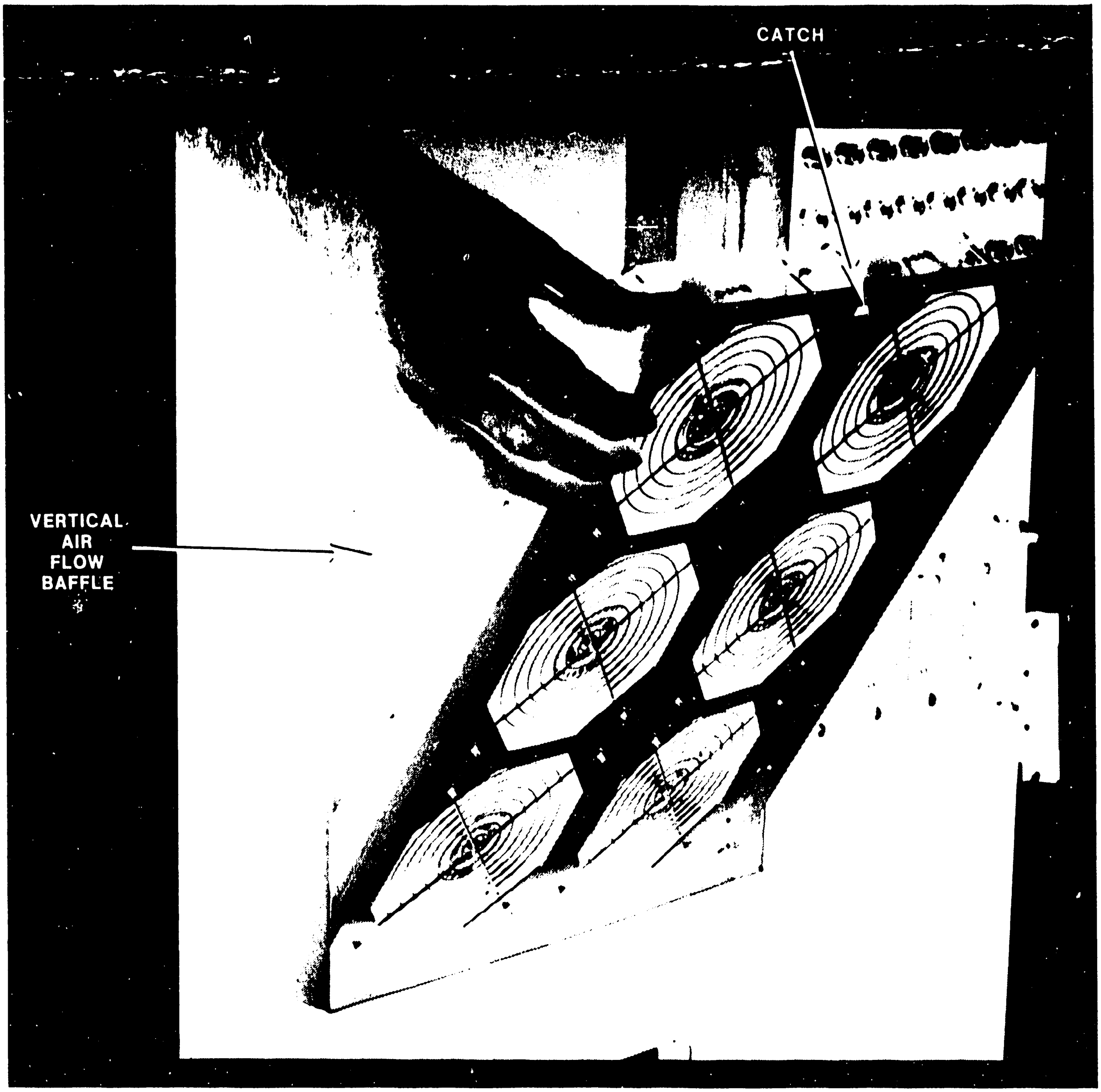


Figure 5-41. Lowering Fan Assembly

CHAPTER 6 SCHE- MATICS

CHAPTER 6

SCHEMATICS

Schematics are not provided as part of this Standard Manual. The schematics will appear in the VS-85//90/100 Computer System Schematics Manual, WLI P/N 741-1462.

CHAPTER 7

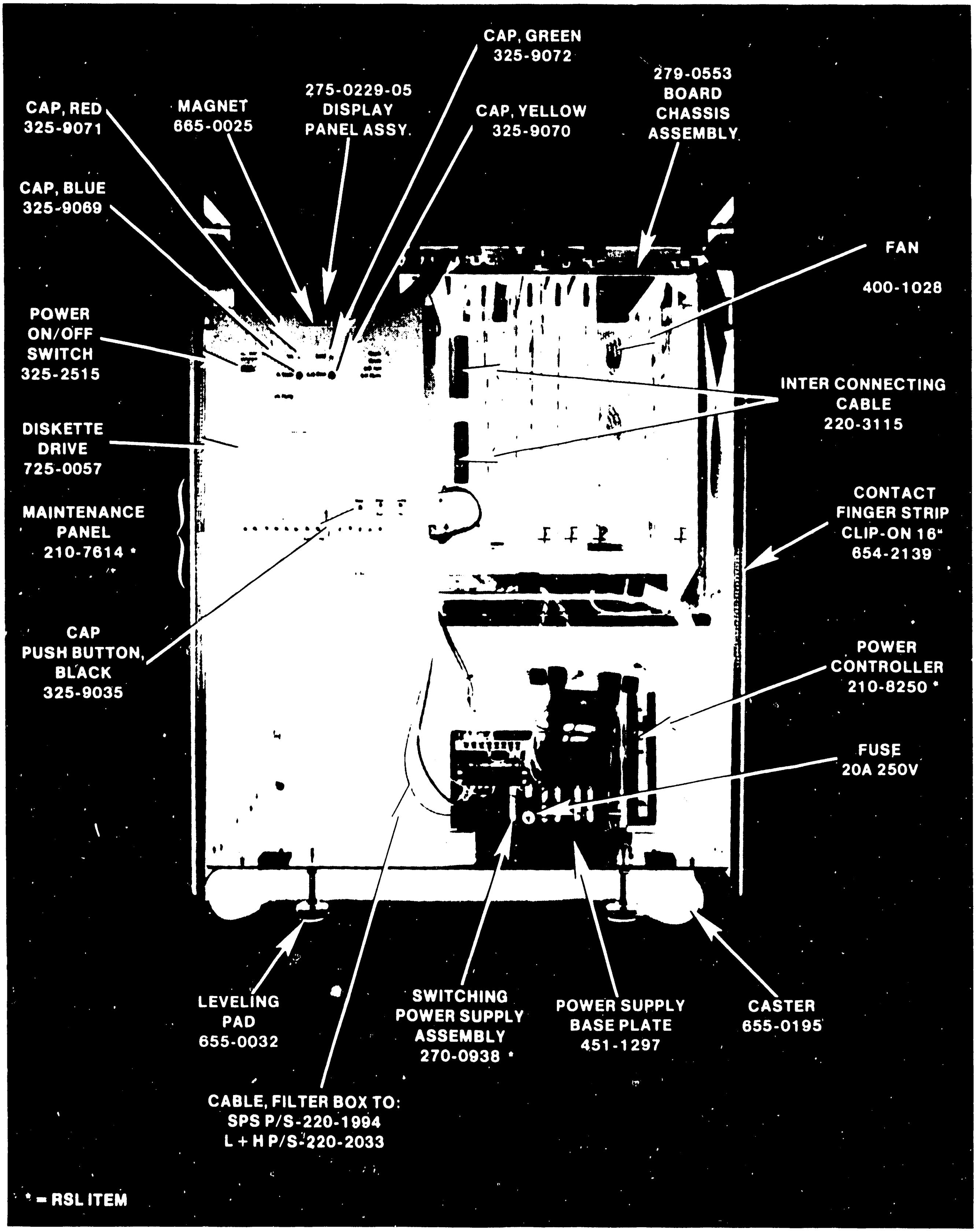
ILLUSTRATED PARTS BREAKDOWN

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

7.1 SCOPE

This chapter contains the illustrated parts breakdown for the VS-85/85-H Computer System. Use this breakdown for part number identification when ordering field-replaceable components. Also included is a list of all field replaceable units (FRUs) in the VS-85/85-H System. (See Table 7-1.)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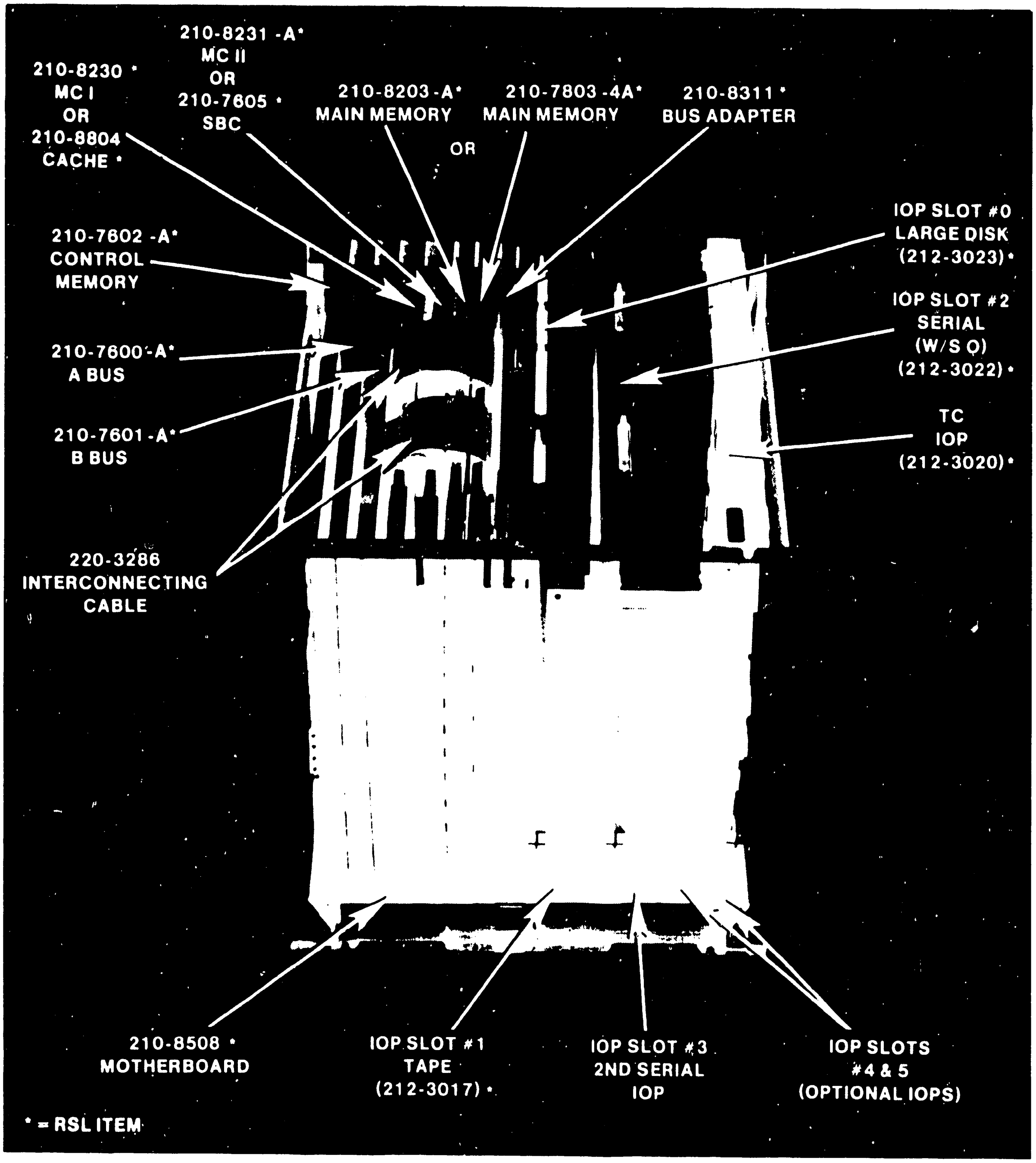
279-0553
BOARD
CHASSIS
ASSEMBLY
275-0229-05
DISPLAY
PANEL ASSY.
CAP, YELLOW
325-9070
CAP, RED
325-9071
MAGNET
665-0025
CAP, BLUE
325-9069
FAN
400-1028
POWER
ON/OFF
SWITCH
325-2515
INTER CONNECTING
CABLE
220-3115
DISKETTE
DRIVE
725-0057
CONTACT
FINGER STRIP
CLIP-ON 16"
654-2139
MAINTENANCE
PANEL
210-7614 *
CAP
PUSH BUTTON,
BLACK
325-9035
POWER
CONTROLLER
210-8250 *
FUSE
20A 250V
LEVELING
PAD
655-0032
SWITCHING
POWER SUPPLY
ASSEMBLY
270-0938 *
POWER SUPPLY
BASE PLATE
451-1297
CASTER
655-0195
CABLE, FILTER BOX TO:
SPS P/S-220-1994
L + H P/S-220-2033
* = RSL ITEM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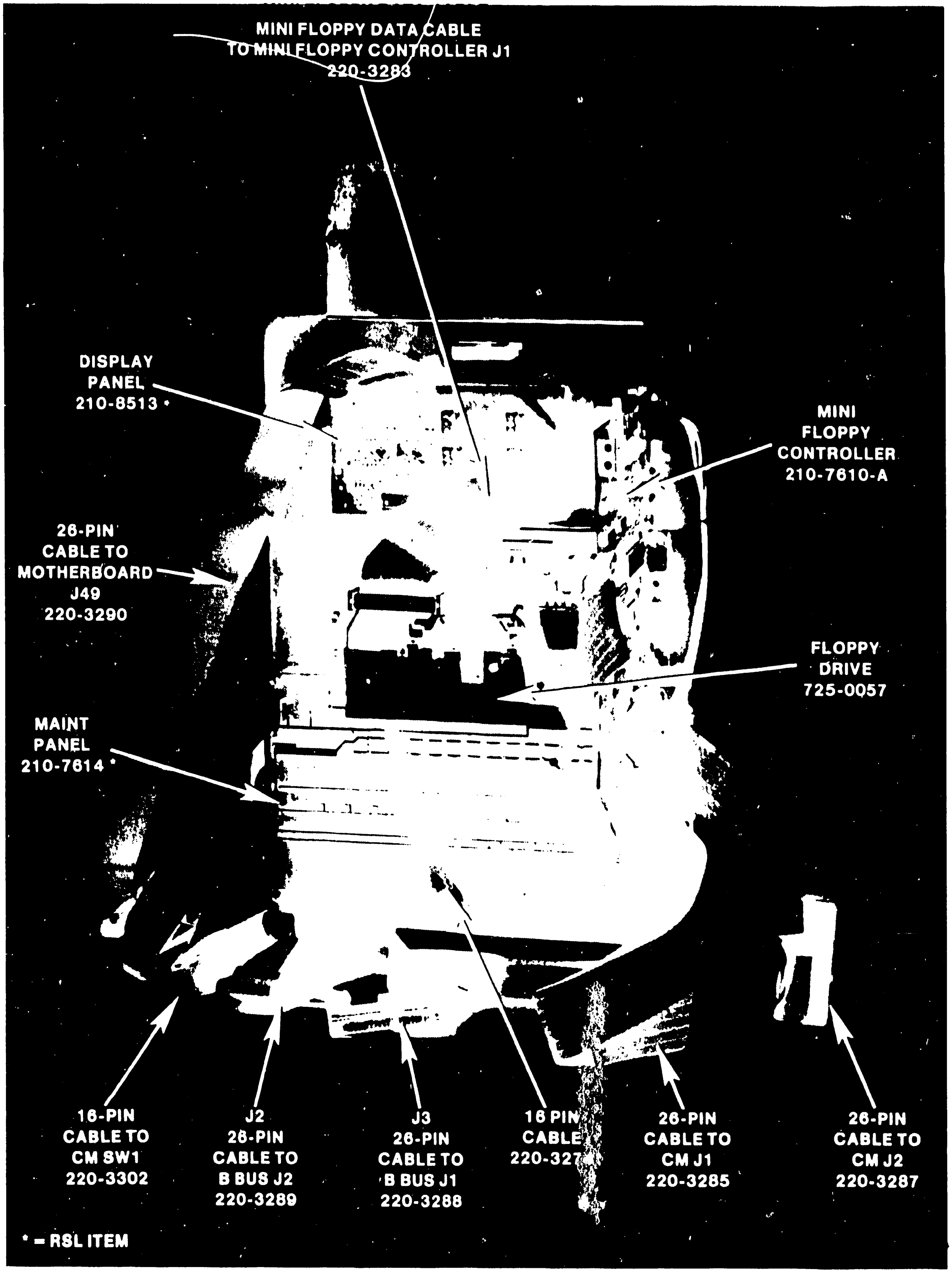
MC II
OR
210-7605 *
SBC
210-8230 *
MC I
OR
210-8804
CACHE *
210-8203 -A*
MAIN MEMORY
OR
210-7803 -4A*
MAIN MEMORY
210-8311 *
BUS ADAPTER
210-7602 -A*
CONTROL
MEMORY
IOP SLOT #0
LARGE DISK
(212-3023)*
IOP SLOT #2
SERIAL
(W/S O)
(212-3022)*
210-7600-A*
A BUS
210-7601-A*
B BUS
TC
IOP
(212-3020)*
220-3286
INTERCONNECTING
CABLE
210-8508 *
MOTHERBOARD
IOP SLOT #1
TAPE
(212-3017)*
IOP SLOT #3
2ND SERIAL
IOP
IOP SLOTS
#4 & 5
(OPTIONAL IOPS)
* = RSL ITEM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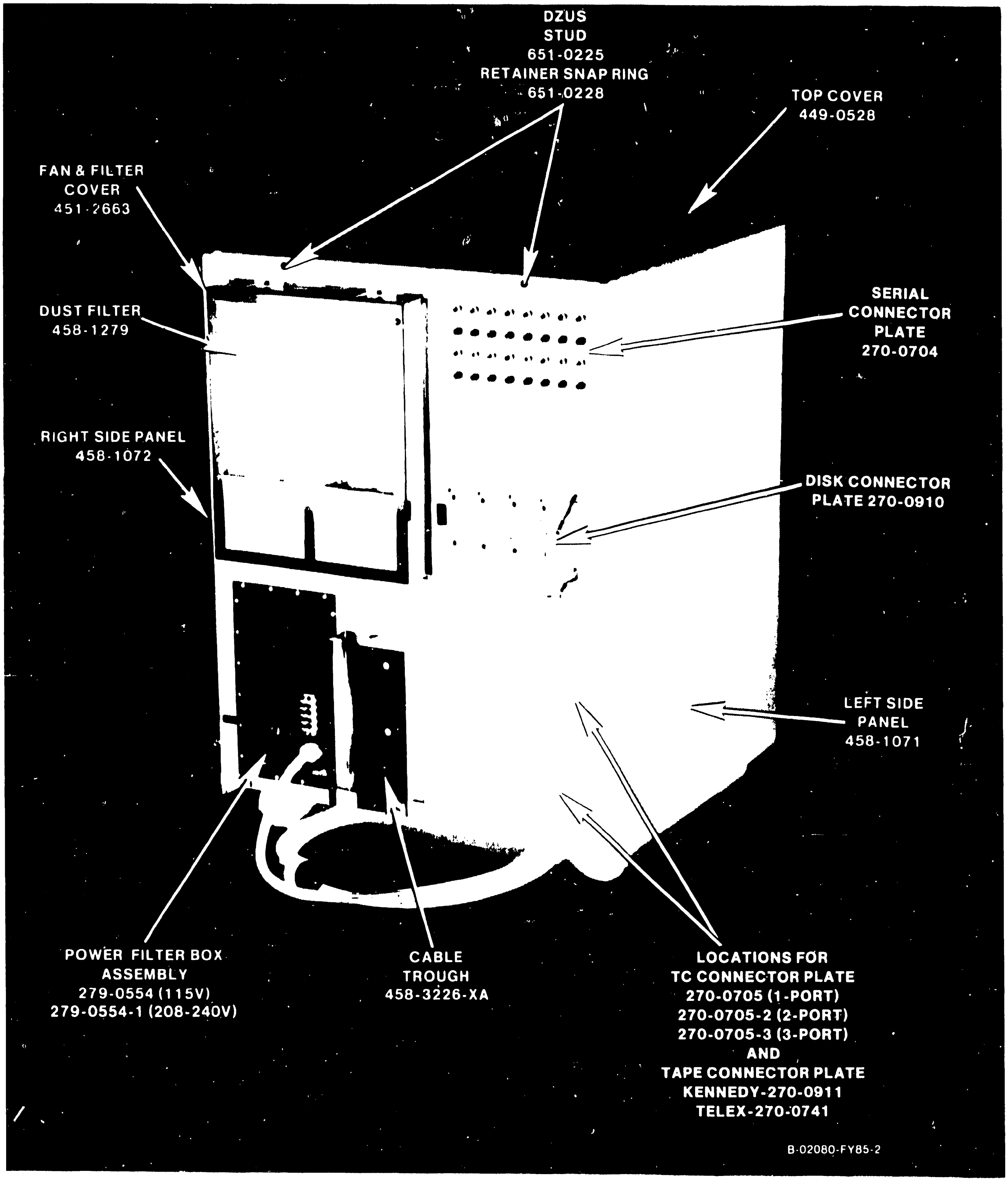
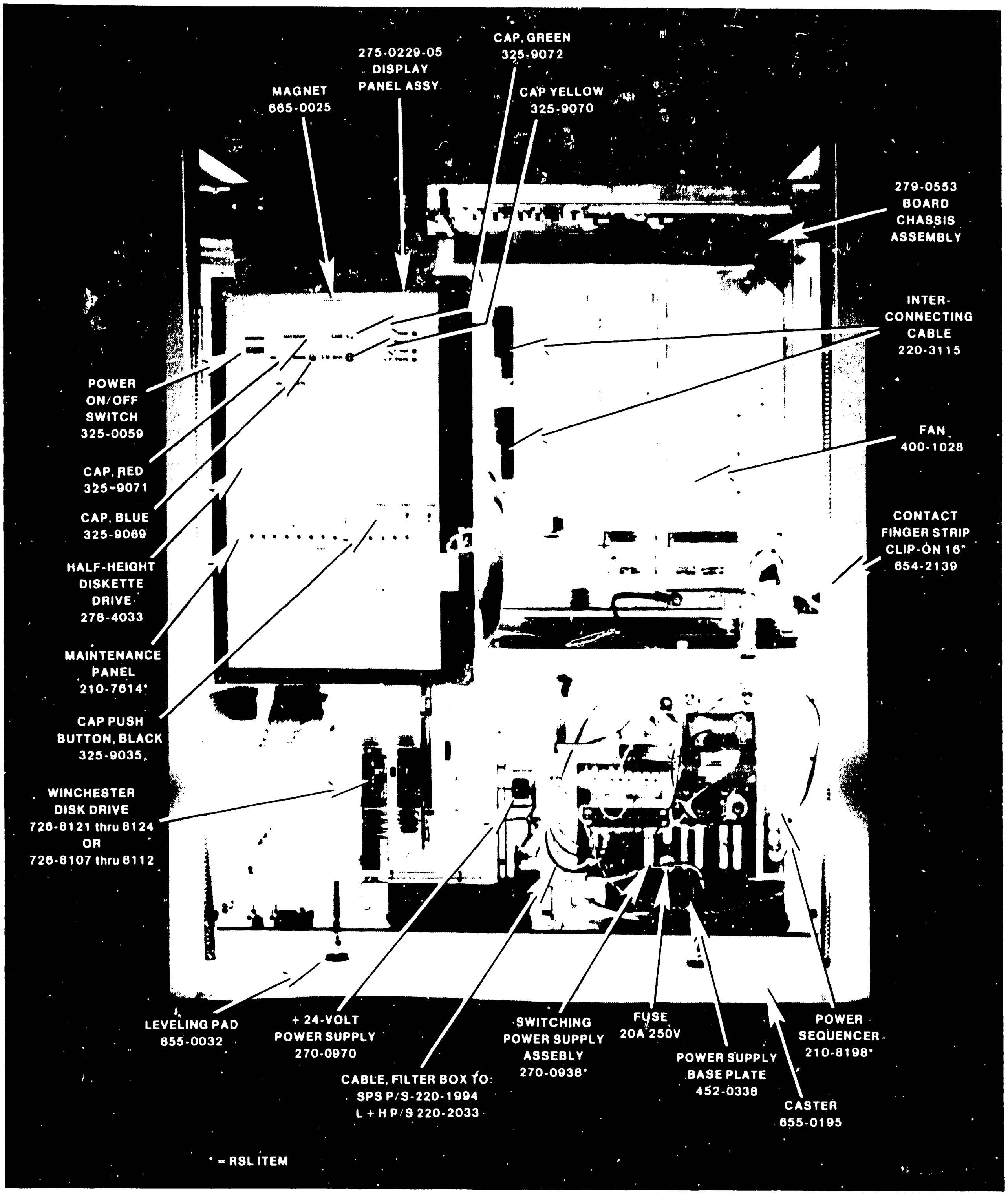
TO MINI FLOPPY CONTROLLER J1
220-3283
DISPLAY
PANEL
210-8513 *
MINI
FLOPPY
CONTROLLER
210-7610-A
26-PIN
CABLE TO
MOTHERBOARD
J49
220-3290
FLOPPY
DRIVE
725-0057
MAINT
PANEL
210-7614 *
16-PIN
CABLE TO
CM SW1
220-3302
J2
26-PIN
CABLE TO
B BUS J2
220-3289
J3
26-PIN
CABLE TO
B BUS J1
220-3288
16 PIN
CABLE
220-327
26-PIN
CABLE TO
CM J1
220-3285
26-PIN
CABLE TO
CM J2
220-3287
* = RSL ITEM


DZUS
STUD
651-0225
RETAINER SNAP RING
651-0228
TOP COVER
449-0528
FAN & FILTER
COVER
451-2663
DUST FILTER
458-1279
SERIAL
CONNECTOR
PLATE
270-0704
RIGHT SIDE PANEL
458-1072
DISK CONNECTOR
PLATE 270-0910
LEFT SIDE
PANEL
458-1071
POWER FILTER BOX
ASSEMBLY
279-0554 (115V)
279-0554-1 (208-240V)
CABLE
TROUGH
458-3226-XA
LOCATIONS FOR
TC CONNECTOR PLATE
270-0705 (1-PORT)
270-0705-2 (2-PORT)
270-0705-3 (3-PORT)
AND
TAPE CONNECTOR PLATE
KENNEDY-270-0911
TELEX-270-0741
B-02080-FY85-2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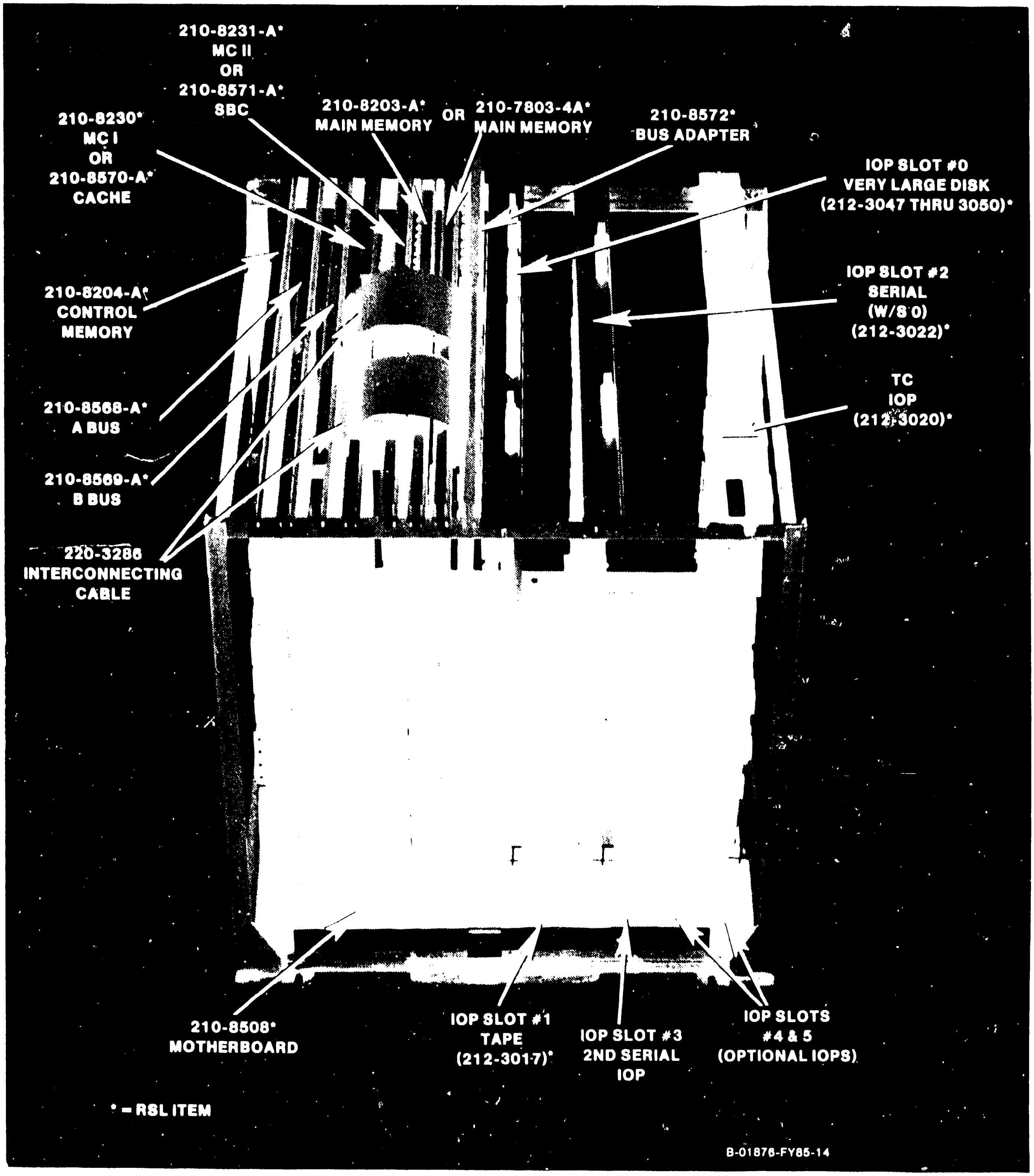
DISPLAY
PANEL ASSY.
CAP, GREEN
325-9072
MAGNET
665-0025
CAP YELLOW
325-9070
279-0553
BOARD
CHASSIS
ASSEMBLY
INTER-
CONNECTING
CABLE
220-3115
POWER
ON/OFF
SWITCH
325-0059
FAN
400-1028
CAP, RED
325-9071
CAP, BLUE
325-9069
CONTACT
FINGER STRIP
CLIP-ON 16"
654-2139
HALF-HEIGHT
DISKETTE
DRIVE
278-4033
MAINTENANCE
PANEL
210-7614*
CAP PUSH
BUTTON, BLACK
325-9035
WINCHESTER
DISK DRIVE
726-8121 thru 8124
OR
726-8107 thru 8112
LEVELING PAD
655-0032
+ 24-VOLT
POWER SUPPLY
270-0970
SWITCHING
POWER SUPPLY
ASSEBLY
270-0938*
FUSE
20A 250V
POWER
SEQUENCER
210-8198*
POWER SUPPLY
BASE PLATE
452-0338
CABLE, FILTER BOX TO:
SPS P/S-220-1994
L + H P/S 220-2033
CASTER
655-0195
* = RSL ITEM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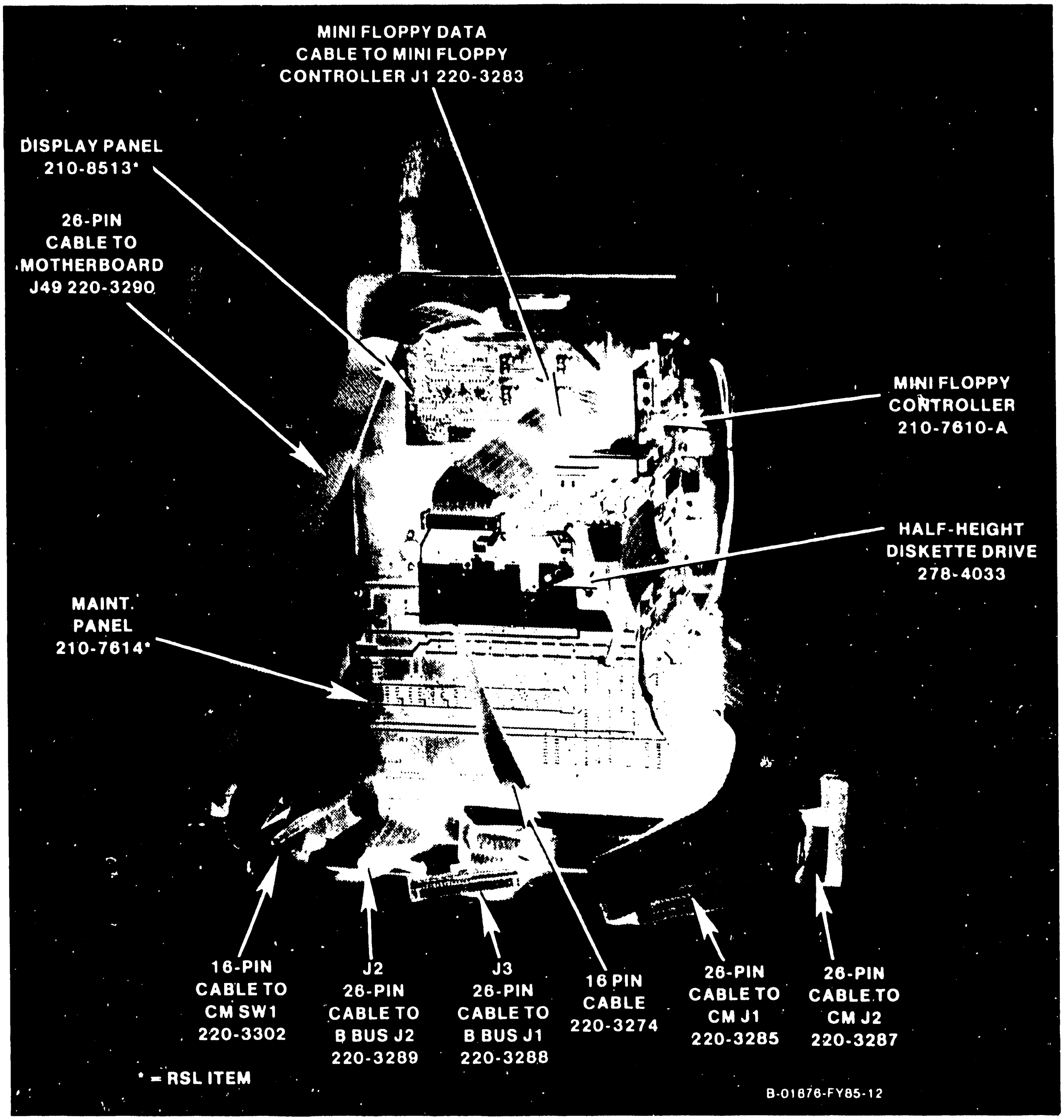
OR
210-8571-A*
SBC
210-8230*
MC I
OR
210-8570-A*
CACHE
210-8203-A*
MAIN MEMORY
OR
210-7803-4A*
MAIN MEMORY
210-8572*
BUS ADAPTER
IOP SLOT #0
VERY LARGE DISK
(212-3047 THRU 3050)*
210-8204-A*
CONTROL
MEMORY
IOP SLOT #2
SERIAL
(W/S 0)
(212-3022)*
TC
IOP
(212-3020)*
210-8568-A*
A BUS
210-8569-A*
B BUS
220-3286
INTERCONNECTING
CABLE
210-8508*
MOTHERBOARD
IOP SLOT #1
TAPE
(212-3017)*
IOP SLOT #3
2ND SERIAL
IOP
IOP SLOTS
#4 & 5
(OPTIONAL IOPS)
* = RSL ITEM
B-01876-FY85-14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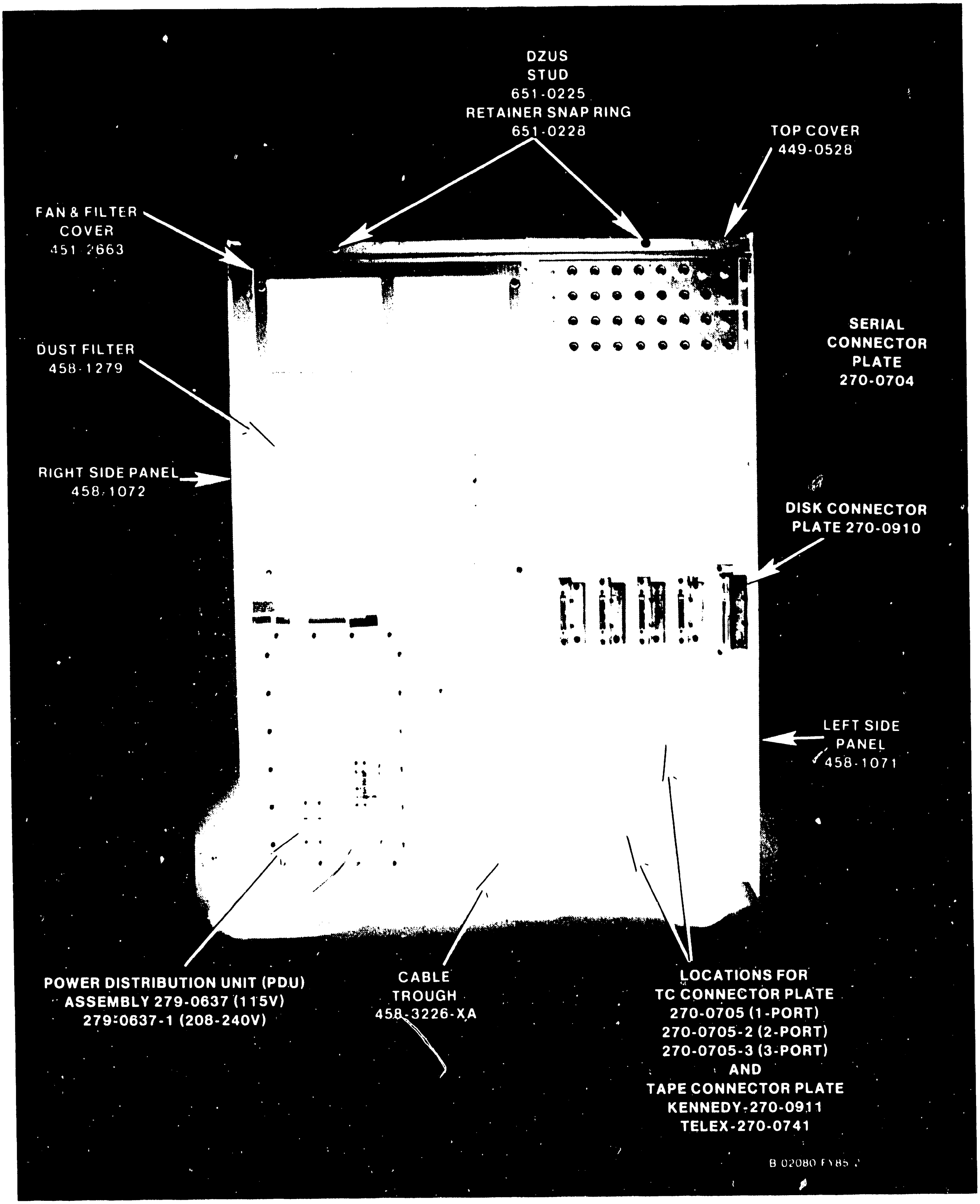
DISPLAY PANEL 210-8513*
26-PIN CABLE TO MOTHERBOARD J49 220-3290
MINI FLOPPY CONTROLLER 210-7610-A
HALF-HEIGHT DISKETTE DRIVE 278-4033
MAINT. PANEL 210-7614*
16-PIN CABLE TO CM SW1 220-3302
J2 26-PIN CABLE TO B BUS J2 220-3289
J3 26-PIN CABLE TO B BUS J1 220-3288
16 PIN CABLE 220-3274
26-PIN CABLE TO CM J1 220-3285
26-PIN CABLE TO CM J2 220-3287
* = RSL ITEM
B-01676-FY85-12


DZUS
STUD
651-0225
RETAINER SNAP RING
651-0228
TOP COVER
449-0528
FAN & FILTER
COVER
451-2663
SERIAL
CONNECTOR
PLATE
270-0704
DUST FILTER
458-1279
RIGHT SIDE PANEL
458-1072
DISK CONNECTOR
PLATE 270-0910
LEFT SIDE
PANEL
458-1071
POWER DISTRIBUTION UNIT (PDU)
ASSEMBLY 279-0637 (115V)
279-0637-1 (208-240V)
CABLE
TROUGH
458-3226-XA
LOCATIONS FOR
TC CONNECTOR PLATE
270-0705 (1-PORT)
270-0705-2 (2-PORT)
270-0705-3 (3-PORT)
AND
TAPE CONNECTOR PLATE
KENNEDY-270-0911
TELEX-270-0741
B 02080 FY85

7.2 FIELD REPLACEABLE UNITS

The following table lists all of the Field Replaceable Units (FRUs) in the VS-85/85-H Computer System. FRUs are arranged by part number followed by a description of the part, the FRU type, and the model to which it belongs.

Table 7-1. VS-85/85-H Field Replaceable Units

WLI P/N	DESCRIPTION	FRU	VS-85	VS-85-H
210-7600	A Bus	PCB	X	---
210-7601	B Bus	PCB	X	---
210-7602	Control Memory	PCB	X	---
210-7605	System Bus Controller	PCB	X	---
210-7610	Mini Disk Controller	PCB	X	X
210-7614	Maintenance Panel	PCB	X	X
210-7706	+5 V Indicator	PCB	X	X
210-7803	1-MB Main Memory	PCB	X	X
210-8198	Power Sequencer Board	PCB	X	X
210-8203	2-MB Main Memory	PCB	X	X
210-8204-A	Control Memory (ML)*	PCB	---	X
210-8230	Memory Controller I	PCB	X	X
210-8231	Memory Controller II	PCB	X	X
210-8250	Power Controller	PCB	X	---
210-8311	Bus Adapter	PCB	X	---
210-8508	Motherboard	PCB	X	X
210-8513	Display Panel	PCB	X	X
210-8568-A	A Bus (ML)*	PCB	---	X
210-8569-A	B Bus (ML)*	PCB	---	X
210-8570-A	Cache (ML)*	PCB	---	X
210-8571-A	System Bus Controller (ML)*	PCB	---	X
210-8572	Bus Adapter (ML)*	PCB	---	X
210-8804	Cache Memory (optional)	PCB	X	---
212-3017	Tape IOC 22V25 (Kennedy)	ASSY	X	X
212-3018	TC IOP 22V26-1	ASSY	X	X
212-3019	TC IOP 22V26-2	ASSY	X	X
212-3020	TC IOP 22V26-3	ASSY	X	X
212-3022	Serial IOP 22V27	ASSY	X	X
212-3023	Large Disk IOP 22V28	ASSY	X	---
212-3030	Tape IOC V15 (Telex)	ASSY	X	X
212-3047	Very Large Disk IOP 22V88-4	ASSY	X	X
212-3048	Very Large Disk IOP 22V88-3	ASSY	X	X
212-3049	Very Large Disk IOP 22V88-2	ASSY	X	X
212-3050	Very Large Disk IOP 22V88-1	ASSY	X	X
220-1995	Pwr Cont Bd-Motherboard Cable	CBL	X	---
220-2006	Mini-floppy Power Cable, 14"	CBL	X	X
220-2031	AC Power Cable	CBL	X	---
220-2058	5-Volt Power Cable, 34"	CBL	X	X
220-2152	Fan Cable	CBL	---	X
220-2153	AC Power Cable	CBL	---	X
220-2176	Sequencer-Motherboard Power Cable	CBL	---	X
220-2177	80 Meg Adapter Cable	CBL	---	X
220-2178	160 Meg Adapter Cable	CBL	---	X
220-3032	"A" Cable IOP to Adapter	CBL	---	X

*ML indicates a multi-layer board used in the VS-85-H.

Table 7-1. VS-85/85-H Field Replaceable Units (cont'd)

WLI P/N	DESCRIPTION	FRU	VS-85	VS-85-H
220-3115	64 Position Socket-Socket, 1.5"	CBL	---	X
220-3274	16 Pin DIP to DIP, 20.5"	CBL	X	X
220-3283	34 Position Socket-edge, 12"	CBL	X	X
220-3284	34 Position Socket-socket, 24"	CBL	X	X
220-3285	34 Pos Sock-60 Pos Sock pin 34-60, 28"	CBL	X	X
220-3286	64 Position Socket-Socket, 4.5"	CBL	X	X
220-3287	34 Pos Sock-60 Pos Sock Pin 1-1, 13"	CBL	X	X
220-3288	26 Pos Sock-60 Pos Sock Pin 26-60, 26"	CBL	X	X
220-3289	26 Pos Sock-60 Pos Sock Pin 1-1, 12"	CBL	X	X
220-3290	26 position socket-socket, 50"	CBL	X	X
220-3302	16 pin DIP to DIP, 24"	CBL	X	X
220-3331	"B" Cable	CBL	---	X
220-3390	"A" Cable I/O Panel/Adapter	CBL	---	X
220-3400	NEC Adapter Cable	CBL	---	X
270-0938	Multi-Vdc Switch. Power Supply	ASSY	X	X
270-0970	+24-Volt 1st Disk Drive Power Supply	ASSY	---	X
270-0971	+24-Volt 2nd Disk Drive Power Supply	ASSY	---	X
270-3305	Main Power Harness	ASSY	X	X
278-4033	Half-Height Diskette Drive	ASSY	---	X
279-0554	Power Filter Assembly 110V	ASSY	X	---
279-0554-1	Power Filter Assembly 230V	ASSY	X	---
279-0637	Power Distribution Unit 110V	ASSY	X	X
279-0637-1	Power Distribution Unit 230V	ASSY	X	X
458-1558	Half-height Diskette Drive Adapter	ASSY	X	X
726-8107	76 MB Read/Write Amp	PCB	---	X
726-8108	76 MB Power Amp	PCB	---	X
726-8109	76 MB Logic and Servo	PCB	---	X
726-8110	76 MB 3DC Input Option	PCB	---	X
726-8111	76/147 MB Earth Pad Assembly	ASSY	---	X
726-8112	76 MB Disk Enclosure	ASSY	---	X
726-8121	147 MB Read/Write PCB	PCB	---	X
726-8122	147 MB Power Amp	PCB	---	X
726-8123	147 MB Logic and Servo	PCB	---	X
726-8124	147 MB Disk Enclosure Assembly	ASSY	---	X

CHAPTER 8

TROUBLE-SHOOTING

CHAPTER 8

TROUBLESHOOTING

8.1 GENERAL

Two types of diagnostics are available to the VS-85/85-H: inner-level CP microcode diagnostics, and outer-level memory and peripheral diagnostics. With these diagnostics, the CE is able to locate and repair most problems that occur in the system. All available diagnostics should be run as a check for system integrity before turning the system over to the customer.

8.2 VS-85/85-H MICROCODE DIAGNOSTICS

An important diagnostic tool for testing the VS-85/85-H CP is a series of microcode diagnostics available on mini-diskettes which are loaded by means of the mini-diskette drive built into the mainframe. Used in conjunction with the Maintenance Panel (paragraph 8.3 and figure 8-1), these diagnostics enable the CE to test all major CP functions.

When a fault (or successful completion) is detected by the microcode diagnostics, the results are displayed as a HEX code halt on the IC (Instruction Counter) Register display. The known good IC halts are shown in table 8-1. Table 8-1 also shows the most likely failing PCBs if an unknown halt occurs. It is also possible that the unknown halt was caused because an ECO has not been installed.

Once the CE has identified the failing board and recorded the error code, the board is sent to a repair depot. At the depot, repair personnel will run the same diagnostics to verify the observations of the CE. This duplicating of trouble conditions results in fast turn-around time in the ultimate repair of the board.

The microcode diagnostics consist of five different testing levels. The five levels and the CP functions tested by each are as follows:

1. LEVEL 1--Tests opcodes needed for higher test levels.

OPERATION/COMPONENT TESTED	TEST #
Microsequencer, Branch Unconditional	T0010
Instruction Counter	T1010
Branch Cond. & Status Opcodes	T2010
Stack Data Integrity	T3010
Routine Stack Address	T4010
Register Data Integrity	T4110

2. LEVEL 2--Tests additional opcode levels.

OPERATION/COMPONENT TESTED	TEST #
Visual Verification	T5000

3. LEVEL 3--Tests process and Control Memory (CM) opcodes. From this point on all diagnostics are supported by the Monitor program.

OPERATION/COMPONENT TESTED	TEST #
CM Moving Inversions (Upper)	T6010
CM Moving Inversions (Upper) (85-H)	**T6110**
CM Moving Inversions (Lower)	T7010
CM Moving Inversions (Lower) (85-H)	**T7110**
Register Data Integrity	T8010
Data Stack & T-RAM	T9010
Data Stack & T-RAM (85-H)	**T9110**

4. LEVEL 4--Completes process and opcode tests.

OPERATION/COMPONENT TESTED	TEST #
Add & Subtract Group	TA010
Logical Instructions	TB010
Move Instructions	TB110
Shift & Decimal Add & Subtract	TC010
Conditional Code & Arith. Logical Group	TD010

5. LEVEL 5--Tests outer level of CP.

OPERATION/COMPONENT TESTED	TEST #
Memory Opcodes and Multiply Group	TAA10
Enhanced Branch Next Macroinstruction	TAF10
ECR, Memory Controller, IPC, and DMA	TBB10
Main Memory Board (85-H; 256K Chips)	**TDA10**
Main Memory Board	TDE10

Table 8-1. VS-85/85-H Microdiagnostic Packages

DIAGNOSTIC NUMBER	DIAGNOSTIC NAME	KNOWN GOOD IC HALTS	MOST LIKELY BAD PCB
T0010	Microsequencer, Uncond. Branch	0000--1FFF	Control Memory
T1010	Instruction Counter	1FFF	Control Memory
T2010	Branch Cond. & Status Ops	1FFF	Control Memory
T3010	Stack Data Integrity	1FFF	Control Memory
T4010	Register Data Integrity	1FFF	Control Memory
T4110	Register Integrity	1FFF	A Bus, B Bus
T5000	Visual Verification	0020--006F	A Bus, B Bus
T6010	CM Moving Inversions (upper)	001F, 0FFF	Control Memory
T6110**	**CM Moving Inversions (upper)**	**001F, 0FFF**	**Control Memory**
T7010	CM Moving Inversions (lower)	101F, 1FFF	Control Memory
T7110**	**CM Moving Inversions (lower)**	**101F, 1FFF**	**Control Memory**
T8010	Register Data Integrity	001F, 1FFF	A Bus, B Bus
T9010	Data Stack and T-RAM	001F, 1FFF	B Bus, A Bus
T9110**	**Data Stack and T-RAM**	**001F, 1FFF**	**B Bus, A Bus**
TA010	Add and Subtract Group	001F, 1FFF	B Bus, A Bus
TBA10	Bus Adapter	0FFF, 01FF	Bus Adapter
TB010	Logical Instructions	001F, 1FFF	B Bus, A Bus
TB110	Move Instructions	001F, 1FFF	B Bus, A Bus
TC010	Shift & Decimal Add & Subtract	001F, 1FFF	B Bus, A Bus
TD010	Condition Code & Arith Logic Group	001F, 1FFF	B Bus, A Bus

Table 8-1. VS-85/85-H Microdiagnostic Packages (cont'd)

DIAGNOSTIC NUMBER	DIAGNOSTIC NAME	KNOWN GOOD IC HALTS	MOST LIKELY BAD PCB
TAA10*	Memory Opcodes & Multiply Group	001F, 1FFF	MM, MCII, A Bus, or B Bus
TAF10	Enhanced Next Macroinstruction	001E, 1FFF	CM, B Bus, A Bus
TBB10*	ECR, Memory Controller, IPC, & DMA	001F, 1FFF	MCI, MCII, BA, or IOPO
TDA10**	**Main Memory Board (256K Chips Only)**		**MM**
TDE10*	Main Memory Board	001F, 1FFF	MM

* For diagnostic packages TAA10, TBB10, and TDE10 **(TDA10 in the VS-85-H with 256K chips)** with the Cache option installed, use VS-100 Level 5 diagnostics listed below in table 8-1A.

** **In the VS-85-H, these tests replace T6010, T7010, T9010, and TDE10, respectively.**

Table 8-1A. VS-100 Level 5 Diagnostics

DIAGNOSTIC #	WLI P/N	REV LEVEL
TAA10	702-8017-A	7140
TBB10	702-8019-A	7140
TBB40	702-8020-A	71C1
TCC10	702-8021-A	7454
TDE10	702-8026-A	7255

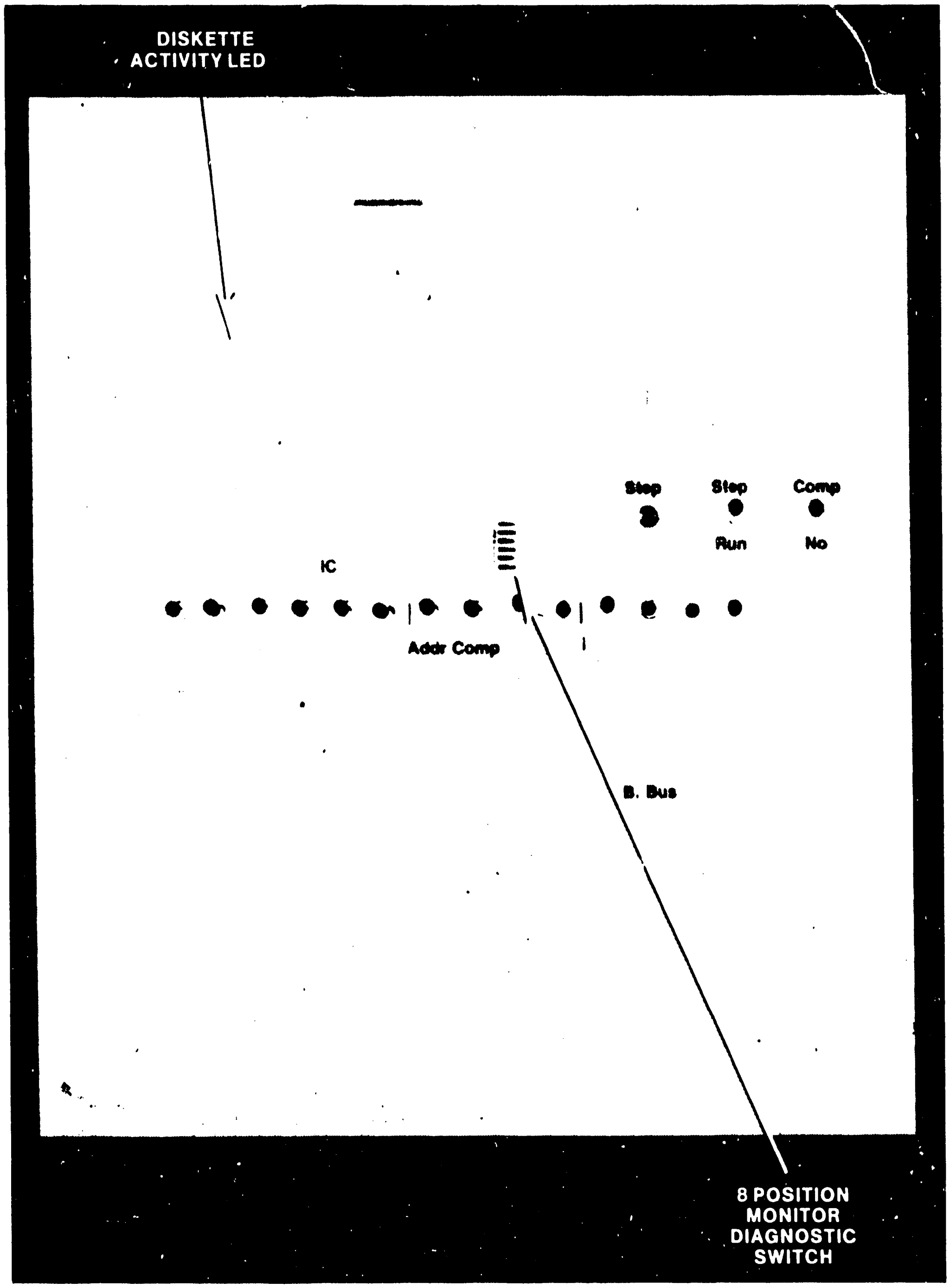


Figure 8-1. Maintenance Panel

8.3 THE MAINTENANCE PANEL

The Maintenance Panel, located directly below the mini-diskette drive, is used by the CE in conjunction with the microcode diagnostics for troubleshooting the VS-85/85-H mainframe. (See figure 8-1 above.) The Maintenance Panel contains the following controls and indicators:

Table 8-2. VS-85/85-H Maintenance Panel Controls

CONTROL NAME AND TYPE	PURPOSE	NORMAL POSITION
MONITOR DIAGNOSTIC SW (8-POSITION DIP)	Refer to paragraph 8.3.2	ON
STEP SWITCH (BLACK PUSHBUTTON)	Controls t-time clocks on CM/A Bus/B Bus for single-stepping diagnostics	RELEASED (NC)
STEP/RUN (TOGGLE SW)	STEP - enables single stepping RUN - disables single stepping	RUN
COMPARE/NO COMPARE (TOGGLE SW)	Allows comparison of contents (location) of Instruction Counter with ADDRESS COMPARE SWITCHES for diagnostic halts	NO COMPARE
ADDRESS COMPARE (14 TOGGLE SWs)	Sets up addresses for COMPARE/ NO COMPARE SWITCH	OFF (DOWN)

Table 8-3. VS-85/85-H Maintenance Panel Indicators

INDICATOR NAME AND TYPE	PURPOSE	NORMAL INDICATION
INSTRUCTION COUNTER DISPLAY (4 HEX LEDS)	Displays contents (location) of Instruction Counter	VARIES
B-BUS DISPLAY (8 HEX LEDS)	Displays contents of B Bus	VARIES

8.3.1 RUNNING MICROCODE DIAGNOSTICS

Load the microcode diagnostics into Control Memory as follows:

1. Insert the first microcode diagnostic diskette (WLI P/N 702-8001A) into the mini-diskette drive and press the yellow CM Boot button on the Display Panel. (See Figure 3-3). The Diskette Activity LED on the front of the diskette drive lights to show that the microcode is being loaded into Control Memory.
2. When the microcode is loaded, the Ready LED on the Front Panel will light and the Diskette Activity LED will go out.

NOTE

If Ready LED flashes instead of remaining steadily ON, system has failed to load the microcode. Reseat diskette and repeat the loading procedures. If microcode cannot be loaded, insert and load another diagnostic diskette. If this does not correct the problem, Control Memory (210-7602), the drive, or the drive controller (210-7610) may be defective. Refer to drive maintenance procedures in Chapter 5.

3. Set switch SW1 on the Maintenance Panel Monitor Diagnostic switch (figure 8-2) to the OFF position, all other switches ON.
4. Press and hold the red Initialize button.
5. Set the Step/Run switch to the Step position.
6. Release the Initialize button.
7. Place the Step/Run switch to Run position and press the Step button. This causes the diagnostic program to begin executing. The program will halt at Instruction Counter (IC) location XXXX (halt may not be consistent). There are some exceptions, such as TEST5000 - Visual Verification Test - which stops at location 0020. Refer to table 8-1 for known good IC halts.
8. After the diagnostic has completed successfully, insert the next diskette and repeat steps 4 through 6.
9. Any unknown IC halts are error conditions (or an ECO has not been installed.) Repeat the test with a backup diskette. If an unknown halt still occurs, refer to table 8-1 to determine the most likely bad PCB.
10. Refer to paragraph 8.3.2 for an explanation of the 8-position Monitor Diagnostic DIP switch. The switch is used in conjunction with the microdiagnostics which support the Monitor program.

8.3.2 MONITOR DIAGNOSTIC SWITCH

Table 8-4 describes the switch settings for the Monitor Diagnostic switch located on the Maintenance Panel. (OFF is ACTIVE.)

NOTE

This switch is used with Level 3 and above microdiagnostics only. Even though Levels 1 and 2 of the microcode diagnostics are <u>not</u> supported by the Monitor Program, all known error halts are documented. Levels 3 and 4 are supported by the Monitor Program. Level 5 is also supported by the Monitor Program, except in situations where the system can't recover from an error condition caused by the hardware failing to respond to the CP.

Table 8-4. Diagnostic Switch Settings

SWITCH #	NAME	FUNCTION
1	HALT ON ERROR	If error occurs, test halts and ERROR CODE appears on B Bus display.
2	DATA DISPLAY	Displays expected/received results of operations whenever error has been detected. Used with Halt On Error to display contents of File Register (FR) specified by switches five through eight.
3	LOOP ON ERROR	Prevents test from halting when error occurs. Loop On Error function puts system in tight loop using only those instructions necessary to generate fault condition. Switch 1 must be ON. (Because LOOP ON ERROR can be used with an oscilloscope, this function useful when troubleshooting chip level on a circuit board.)
4	LOOP ON TEST	Used to troubleshoot intermittent error. Causes specified subtest to cycle repeatedly from beginning to end until error reoccurs. Setting switch 4 ON causes routine to proceed to next subtest. Loop On Test can be used with Halt On Error (SW1) or Loop On Error (SW3).
5	SLOW CLOCK	Provides means of proving marginal system errors. To use this function, CP must be halted at CM location 0000. For diagnostic and troubleshooting purposes only.
6	FAST CLOCK	Same function as slow clock.
7	EXECUTE SINGLE TEST	Run test once and halt. After halt, B bus displays number of test that was run. Monitor Program ignores other switches when this switch OFF.
8	LOOP ON DISKETTE	Repeatedly run diagnostic routines stored on diskette. To stop looping, set Switch 8 ON. Monitor Program ignores other switches when this switch OFF.
5, 6, 7, and 8	FILE REGISTER SELECT	To display contents of a particular FR, switches 5 through 8 must be set to the number of the specific register. Contents of register are displayed on B Bus LEDs. Display represents expected data from execution of a specific opcode. To use this function, switches 1 & 2 must be OFF. EXAMPLES: Switches 1,2,7,8 OFF (HEX C3) displays contents of File Reg 3. Switches 1,2,6 OFF (HEX C4) displays contents of File Reg 4. See Table 8-5.

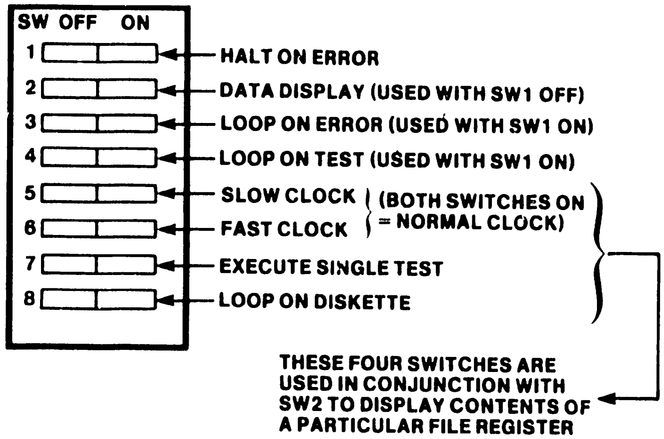


Figure 8-2. Monitor Diagnostic Switch

Table 8-5. File Register Contents

FILE REGISTER	CONTENTS
FR00	Test number
FR01	Error code
FR02	Expected data
FR03	Received data
FR04 through FR11	Error data
FR12 FR13 FR14	Save area for WK1, WK2, and MDR4
FR15 through FR31	Unused

NOTE

Table 8-1 is an example. It is not applicable to all tests.

8.3.3 USING THE MONITOR DIAGNOSTIC SWITCH

The following steps outline basic procedures of how the Monitor Diagnostic switch is used in actual practice.

1. While a Level 3 or higher diagnostic test is halted at Location 0000, set switches 5 and 6 (figure 8-2) to regulate the System Clock for either slow, fast, or normal cycle time. If an intermittent CPU problem exists, the Slow/Fast diagnostic clocks may be used for troubleshooting. However, the Slow/Fast clocks must not be used to enhance system performance.
2. Press the black Step pushbutton on the maintenance panel and the test will halt at Location 001F.

3. Reset all switches to the ON position and place those switches that pertain to the desired Monitor function to OFF. For example, placing switch 1 in the OFF position causes the test being run to halt if an error occurs (Halt On Error) during test execution.
4. If an error occurs while using the Halt On Error function, the test will halt and an error code will appear on the B Bus display.
5. Consult the program listings for an explanation of the cause of the fault and what area of the CP in which the trouble occurred.

8.3.3.1 Diagnostic Clock Adjustment

To help diagnose intermittent CPU problems, the Slow/Fast diagnostic clocks may be used for troubleshooting. The following describes the adjustments to make sure that the clocks are accurate.

1. Insert the diskette (WLI P/N 732-8008A) containing microcode diagnostic T6010 (CM Moving Inversions - Upper, version 7130) into the diskette drive.
2. Load the diagnostic with the yellow CM Boot pushbutton.
3. When the diagnostic has successfully loaded, set Monitor Diagnostic switch #5 OFF to enable the slow clock.
4. Press the red Initialize pushbutton. (The system must be initialized to set the clock to a new speed.) The diagnostic should halt at IC (Instruction Counter) location 001F.
5. Set up the oscilloscope as follows:
   a. Power up the oscilloscope.
   b. Set Vert. Mode to CH1.
   c. Set Volts/Division to 2 Volts.
   d. Set AC-GND-DC to DC.
   e. Set Time/Division to 0.05 microseconds.
   f. Set Horiz Display to A.
   g. Set Trig Mode to Auto.
   h. Set Slope positive.
   i. Set Source to Channel one.
   j. Set Coupling to AC.
   k. Make sure that probe is grounded.
   l. Connect channel one probe to L107, pin 2 on the 210-7602 Control Memory board. **For the VS-85-H, use L7, pin 9, on the 210-8204-A Control Memory board.**
6. For the VS-85, adjust R138 (slow clock coarse adjustment) and R137 (slow clock fine adjustment) on the 210-7602 Control Memory board (figure 8-3A) until the leading edge-to-leading edge time of the slow clock pulse is 176 nanoseconds. **For the VS-85-H, adjust R4 (slow clock coarse) and R3 (slow clock fine) on the 210-8204-A Control Memory board (figure 8-3B).**
7. Set Monitor Diagnostic switch #5 ON and switch #6 OFF to enable the fast clock.
8. Press the red Initialize pushbutton again. The diagnostic should halt at IC location 001F.
10. For the VS-85, adjust R136 (fast clock coarse adjustment) and R135 (fast clock fine adjustment) until the leading edge-to-leading edge time of the fast clock is 144 nanoseconds. **For the VS-85-H, adjust R2 (fast clock coarse) and R1 (fast clock fine).**
11. Set Monitor Diagnostic switch #6 ON.
12. Press the red Initialize pushbutton again to return the clock to the normal speed.

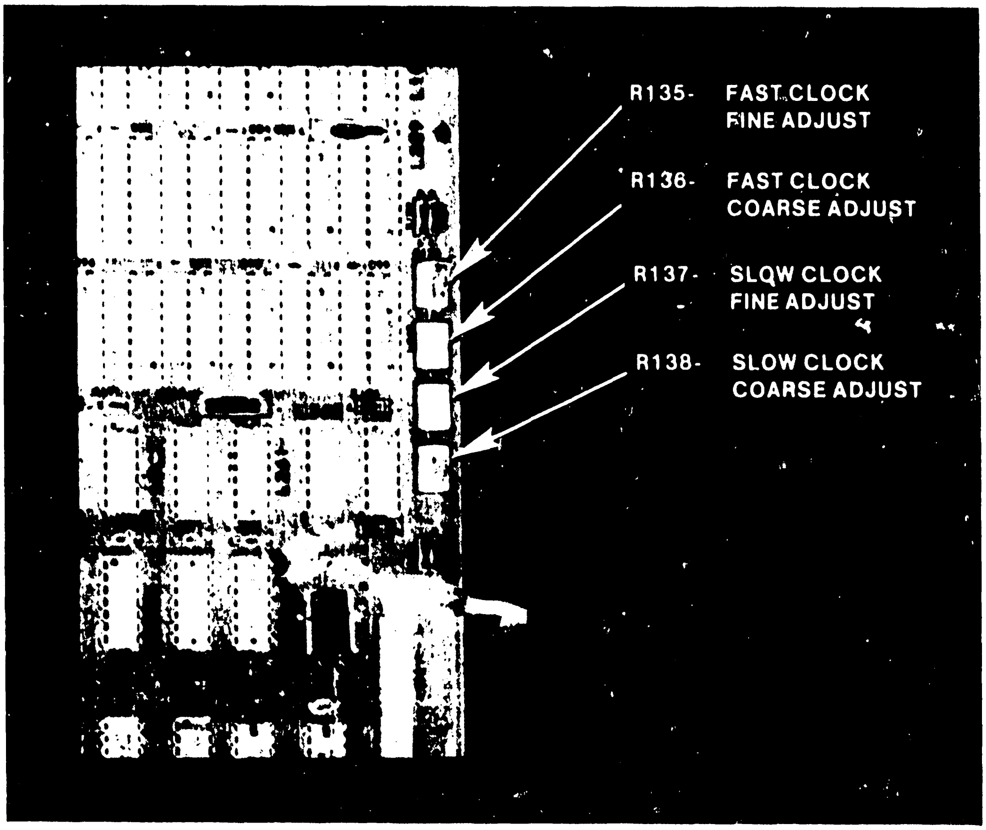


Figure 8-3A. 210-7602 VS-85 Diagnostic Clock Adjustment Pots

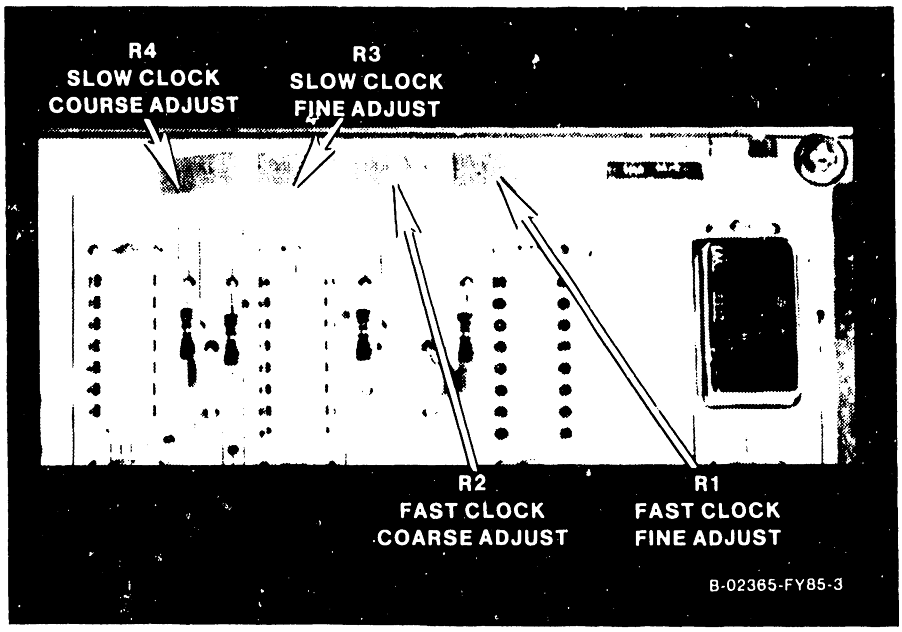


Figure 8-3B. 210-8204-A VS-85-H Diagnostic Clock Adjustment Pots

8.3.4 USING THE DATA DISPLAY

The Data Display routine is used to display expected and received results of operations whenever an error has been detected. It is run in combination with the Halt On Error function. To use the Data Display:

1. Once a test has halted with an error code shown on the B Bus LEDs, set switch 2 to the OFF position to display data.
2. The configuration of switches 5 through 8 determine which File Register contents will be displayed on the B Bus LEDs.
3. For example, switches 1,2,7 and 8 in the OFF position (C3) displays the contents of File Register 3 (FR3), which is the expected data from the execution of a certain opcode. By leaving switches 1 and 2 OFF, resetting switches 7 and 8 ON, and setting switch 6 OFF (representing a C4 configuration) the contents of File Register 4 will be displayed. This is the received data from the execution of a certain opcode.

8.3.5 USING THE LOOP ON ERROR

Once an error has been detected and the test halted, the Loop On Error function can be run. To use Loop On Error:

1. Place switch 3 in the OFF position and switch 1 to the ON position. This prevents the test from halting when an error occurs and puts the system in a very tight loop using only those instructions necessary to generate the fault condition.

2. With this function an oscilloscope can be used to locate the problem. The Loop On Error function is useful when troubleshooting defective boards down to the chip level.

8.3.6 USING THE LOOP ON TEST

If an intermittent error occurs, the Loop On Test function is used. To use the Loop On Test:

1. Place switch 4 in the OFF position. This causes the specified subtest to cycle repeatedly from beginning to end until the error reoccurs.
2. Resetting switch 4 to the ON position causes the routine to proceed to the next subtest.
3. The Loop On Test function can be used in conjunction with the Loop On Error function or the Halt On Error function for fault isolation routines.

8.4 VS-85/85-H MEMORY AND PERIPHERAL DIAGNOSTICS

Memory and peripheral diagnostics available to the VS-85/85-H are divided into three categories: On Line, Stand-alone, and Control Mode. The following paragraphs provide a brief description of these diagnostics.

8.4.1 ON LINE DIAGNOSTICS

With On Line diagnostics (located in library @SYSTST@), the CE logs on to the system through a workstation and executes a specific test routine, which runs under control of the Operating System (while customer is running). All currently available VS-60/80/100 on line test routines will be available on the VS-85. Diagnostic programs currently available for individual peripherals are as follows:

Table 8-6. On Line Diagnostics

DIAGNOSTIC NAME	WLI P/N	VERSION	FUNCTION
ELOGDISP	702-0070	1.0	Utility used to interrogate and display VS I/O Error Log.
TPTEST	702-0187	6224	Magnetic tape diagnostic for Kennedy and Telex tape drives. Requires OS version 5.01.51 or later.
FTU On-line	195-2652-3	6365	On-line version of FTU simulator. Supports all current VS disk drives including soft-sector. Allows CE to do most disk read, write, and control functions. CE can do most disk alignment procedures without removing disk drive from system. Requires OS version 5.0 or later.
PRTEST1	702-0092	2.0.1	Provides full character set ripples on all 132 print positions, character broadsides, printing specific characters in specific columns, and test of spacing and format functions. Will attempt things unique to printer under test (i.e., variable pitch, loadable forms control, etc.).
VS On-line Printer Part I Monitor	702-0179A	2242	Low speed serial printers including 5521,5531, 5535, 5581WD, 6581WC and DW20.
VS On-line DTOS Printer 2	195-2535-3	2211	High speed serial printers, including 5570/71, 5573/74, 5575, 5577, and 5531W6.
VS On-Line Dtos Printer 3	195-2899-3	2420	LPS-12, Ziyad Feeder, Slave Upper RAM, Z-80 CPU Instruction Test.
VS On-Line DTOS Device 1	195-4036-3	2450	Z80 Instr, CRT RAM, Display & Kybd, PSKD Wkstn, PS WS CRT Cntrlr, Audio Wkstn, Slave Upper RAM, Model 6300 Painter Bd Rpr Aid, Arabic WS Scan Direction Exer, Dagwood 6300 WS Display & Kybd, Teletex Date/Time Bd.
VS On Line DTOS Device 2	195-2615-3	2430	Slave Upper RAM, Z80 Instr, CRT RAM, Display & Kybd, TC Black Box, Z80 Typesetter, T1C4/LS4, I/D Exerciser, Cable Interface Unit, Fixed Frequency Modem, TCB-1 & DLP 64/128.
VS On-Line DTOS Device 3	195-2604-3	2334	Archiving Wkstn TC & Disk, Nine Track Tape Controller & Functions, Kennedy Tape Drive, and Archiving Cartridge 22XX Workstations.
VS On-Line DTOS Device 4	195-2976-3	2440	Serial Display & Keyboard; 4205, 4210 Graphics, 4230, 4245 Color; 4210 & 4245 CRT Alignment.

Table 8-6. On-Line Diagnostics (cont'd)

DIAGNOSTIC NAME	WLI P/N	VERSION	FUNCTION
22V06 Local Loopback (TCIOPTST)	195-2972	1455	Tests VS TC IOP & associated memory. Requires loop-back connector, WLI P/N 420-1040.
SYSNAME	702-0107	8110	Utility for renaming of an Operating System's start-up file (@SYS000@).

8.4.2 STAND-ALONE DIAGNOSTICS

Using the stand-alone diagnostic routines (located in library (@DIAGS@), the CE creates a mini-operating system with a menu display of all currently available stand-alone test routines. The CE then selects and executes the desired test. The customer cannot access the system while these tests are being performed. Currently available diagnostics are as follows:

Table 8-7. Stand-alone Diagnostics

DIAGNOSTIC NAME	WLI P/N	VERSION	FUNCTION
UNIBOOT	195-2479-3	8466	Displays diagnostic menu on W/S 0. @SYS000@ first loads the microcode file @MC2246S into the WS, then displays the diagnostic menu.
FTUA	195-2626-3	6385	Allows exercising disk units still connected to the system. Permits verifying, reading and writing, initializing, positioning heads, and alternate seeks.
VOLCOPY	702-0122A	8181	Performs same functions as On-line version of the COPY program.

8.4.3 CONTROL MODE

Control Mode is a state in which normal CP programming activities are suspended and certain other facilities (mainly diagnostic and initialization) are made available to the user. These facilities are divided into two groups of commands as follows:

1. Load Group -- contains commands for initializing the OS, loading a stand-alone program, loading a diagnostic program, or restarting a program from an initialized state.

2. Debug Group -- contains commands for displaying or modifying main memory, general registers, control registers, or the PCW. Also included in this group are commands for single step program execution, hard copy dump of memory and registers, and virtual address translation.

Control Mode uses Workstation 0 for communications between the operator and the system. To enter Control Mode, Workstation 0 must be powered on. Control Mode uses only the top line (line 1) of the CRT display. The contents of the line are saved on entry and restored at exit. Control Mode is transparent to any program that may be using Workstation 0. For a detailed discussion of Control Mode commands, refer to Chapter 8 of the VS Principles of Operation manual (800-1100PO). All standard VS-60/80/100 Control Mode functions are available on the VS-85.

Table 8-8. Operating System Error Codes

IPL Errors

PCW DISPLAY	CAUSE
00000001 FFFFFF00	Not enough memory for IPL
00000002 FFFFFF00	IPL I/O error
00000003 FFFFFF00	No system file on volume
00000004 FFFFFF00	Bad VTOC on IPL volume
00000005 FFFFFF00	OS code spans more than 3 extents

Resident SYSINIT Errors

PCW DISPLAY	CAUSE
00000011 FFFFFF00	SYSINIT I/O error - OS cannot be read
00000012 FFFFFF00	Not enough memory for resident system
00000013 FFFFFF00	SYSINIT program check
00000014 FFFFFF00	IPL device not included in SYSGEN

Machine Check Errors

PCW DISPLAY	CAUSE
00000021 FFFFFF00	Main memory parity error
00000022 FFFFFF00	I/O Processor malfunction - device
00000023 FFFFFF00	I/O Processor malfunction - time out

Nonresident SYSINIT Errors

PCW DISPLAY	CAUSE
00000031 FFFFFF00	OS file (@SYSSVC@) not found
00000032 FFFFFF00	Cannot create/scratch paging file, task 0
00000033 FFFFFF00	Link to SYSGEN module failed (for dynamic SYSGEN only)

Table 8-8. Operating System Error Codes (cont'd)

Miscellaneous Errors

PCW DISPLAY	CAUSE
00FFFFFF FFFFFF00	Wrong machine (VS-80 OS on VS-85 or vice versa)

Notes:

1. Status portion of PCW is always FFFFFF00
2. First 3 bytes of PCW are always 000000
3. First 4 bits of 4th byte identifies error source:
   0 = IPLTEXT
   1 = Resident SYSINIT
   2 = Machine check handler
   3 = Nonresident SYSINIT

4. Second 4 bits of 4th byte identifies the error number from a particular source

Table 8-9. Machine Check Error Codes

MACHINE CHECK CODE	CAUSE
001	ECC Error on Main Memory Read by CPU
003	ECC Error on Main Memory One Byte Write by CPU
017	Bus Transaction Log Overflow
018	IPC Data Word Rejected (Sender = CP or BA)
019	Machine Checks 017 and 018
020	IPC Data Word Rejected (Sender = CP)
021	Machine Checks 017 and 020
022	Machine Checks 018 and 020
023	Machine Checks 017, 018, and 020

8.5 CONTROL MODE DUMP

This procedure allows the user to dump the contents of certain areas of main memory to a specified disk drive or tape for later analysis.

NOTE

This dump procedure is for 5.0 Operating Systems. For Operating System 6.0, refer to VS Software Release Bulletin 6.0, WLI P/N 800-3111-01, which consolidates dump procedures for all VS systems.

CAUTION

Control Mode dump will destroy the Volume Table of Contents (VTOC) on the pack being dumped to; it will NOT destroy the label.

To begin a Control Mode dump, do the following:

1. Press the blue Control Mode (CM) button.
2. Record the current Program Control Word (PCW) as displayed on W/S 0.
3. Key in: P 000070 (ENTER) -- Where "P" is the Physical Memory Address. This displays the Master Control Block (MCB) pointer, as follows:
   AAAAxxxx xxxxxxxx
   Where AAAA is address of the MCB and x = "don't care".
4. Key in: P 00AAAA (ENTER) -- Where AAAA is address of MCB from step 3. This displays the first 8 bytes of the MCB, as follows:
   xxxxxxxx xxxxDDDD
   Where DDD is the address of the dump program in main memory and x = "don't care".
5. Key in: W (ENTER)
   This will display the present PCW.
6. Key in: M 0000DDDD 00000000 (ENTER) -- Where DDDD is the address of the dump program from step #4. All other places must be zero-filled.

7. Key in: P 00DDD(D-2) (ENTER) -- Where DDD(D-2) is the dump program address from step #4 minus two. This will display a portion of memory as follows:

   QQQQxxxx xxxxxxxx

   Where QQQQ is the Physical Device Address (PDA) of the device receiving the memory dump. Construct QQQQ as follows:

   BBBI IIPP PPPP PPPP

   Where: BBB = BA #; III = IOP #; PP PPPP PPPPP = Port #

   Example: 0401 = BA, IOP #1, Port #1.

	BBBI	IIPP	PPPP	PPPP
BIT POSITION	0000	0100	0000	0001
HEX RESULT	0	4	0	1

8. Make sure that the device being dumped to is not ready.
9. Key in: W (ENTER).
10. Key in: X (ENTER). At this point the DUMP program assumes control and forces the CP back into Control Mode.
11. Remove the Control Mode bit from the PCW as follows:

    xxxxxxxx Zxxxxxxx is the PCW where Z is the digit containing the Control Mode bit -- bit 3 of the digit. Remove the bit by typing M, spacing to the Control Mode digit, and modifying it to turn off (set to zero) the Control Mode bit. Make sure that only the Control Mode bit is changed -- i.e., If digit = 4 change it to 0; if digit = C change it to 8.
12. Key in: X (ENTER). This will start the dump waiting for pack or tape mount on drive. The dump will go to that drive upon unsolicited interrupt, and the system will fall into the Control Mode with:

    PCW = xxxxxxxx C000C000

    This completes a memory dump.

8.6 FILING A MEMORY DUMP

In order to obtain a hard copy of an Operating System 5.0 memory dump, or to allow the dump to be backed up onto tape, diskette, or another disk, the data obtained from a dump must be filed from the disk receiving the original dump to another disk. This converts the dump data into a form usable by the system. To create a disk file from a memory dump, do the following:

1. Mount the dump disk pack on a previously IPL'd system as an SL (Standard Label) pack.
2. Execute the FLOPYDUP program.
3. Using option "C" OF FLOPYDUP program, copy the dump onto the previously mounted pack (make sure pack has a VTOC on it).
4. When output file is requested, change number of records to 1026.
5. The FLOPYDUP program will reply with a reverify query to make sure that change is wanted. Confirm this.
6. This file can now be backed up on an individual basis (or as part of regular backups) to tape or other disk packs.

8.7 FLOW CHARTS

The flow charts on the following pages are designed to aid the operator and the CE in troubleshooting the VS-85/85-H. (See figures 8-4 and 8-5.)

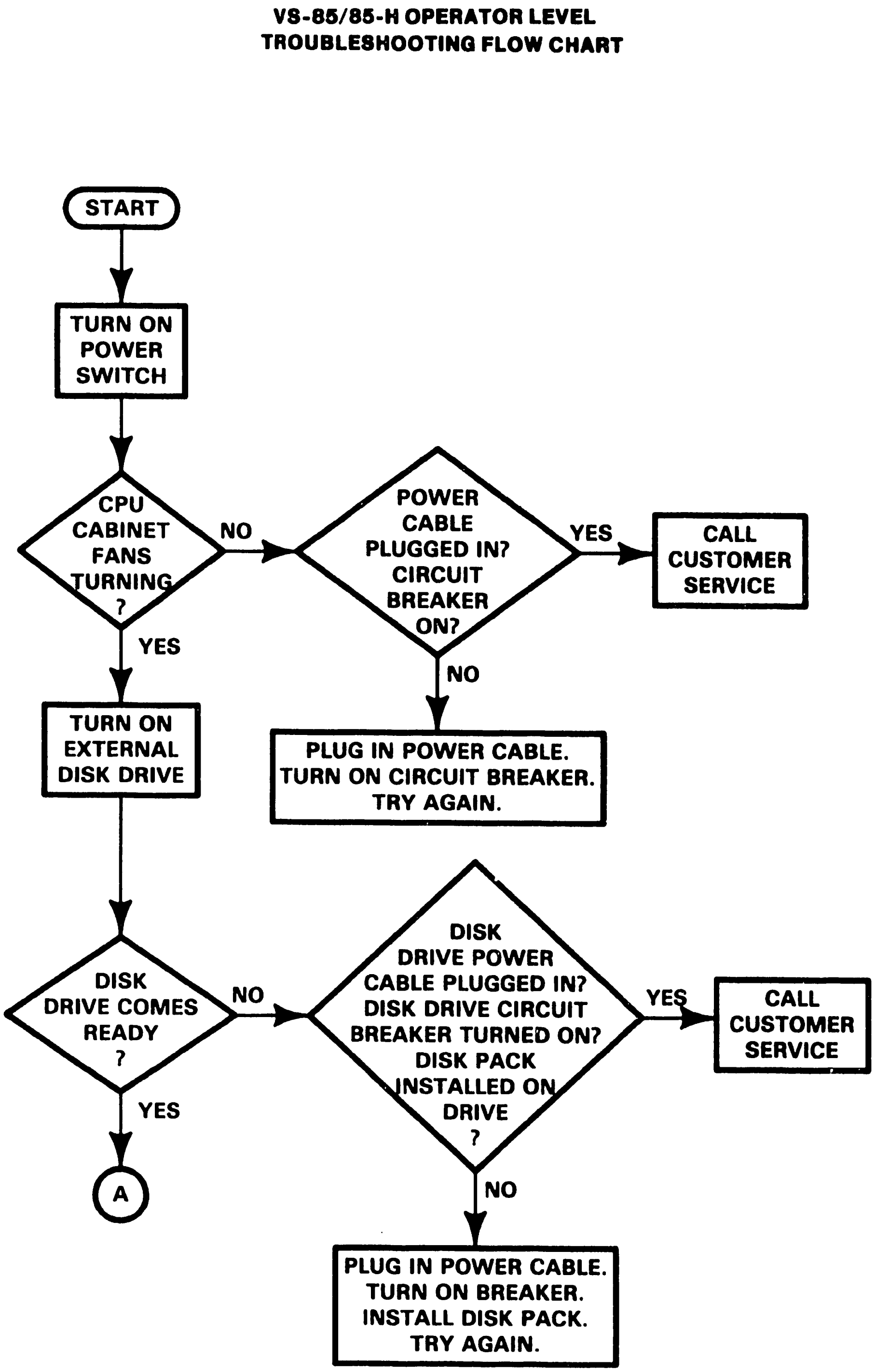


Figure 8-4. Operator Troubleshooting Flowchart (1 of 3)

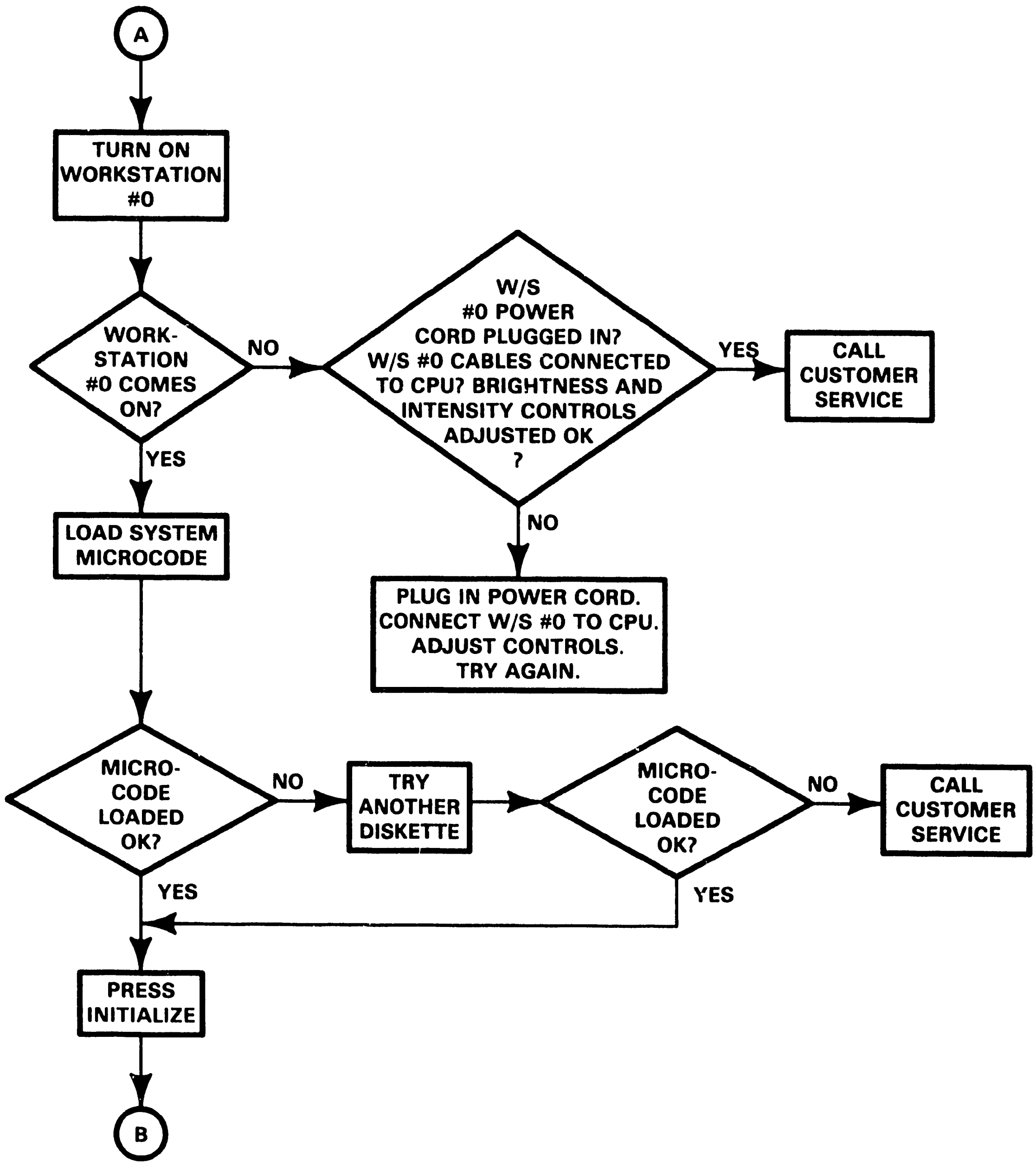


Figure 8-4. Operator Troubleshooting Flowchart (2 of 3)

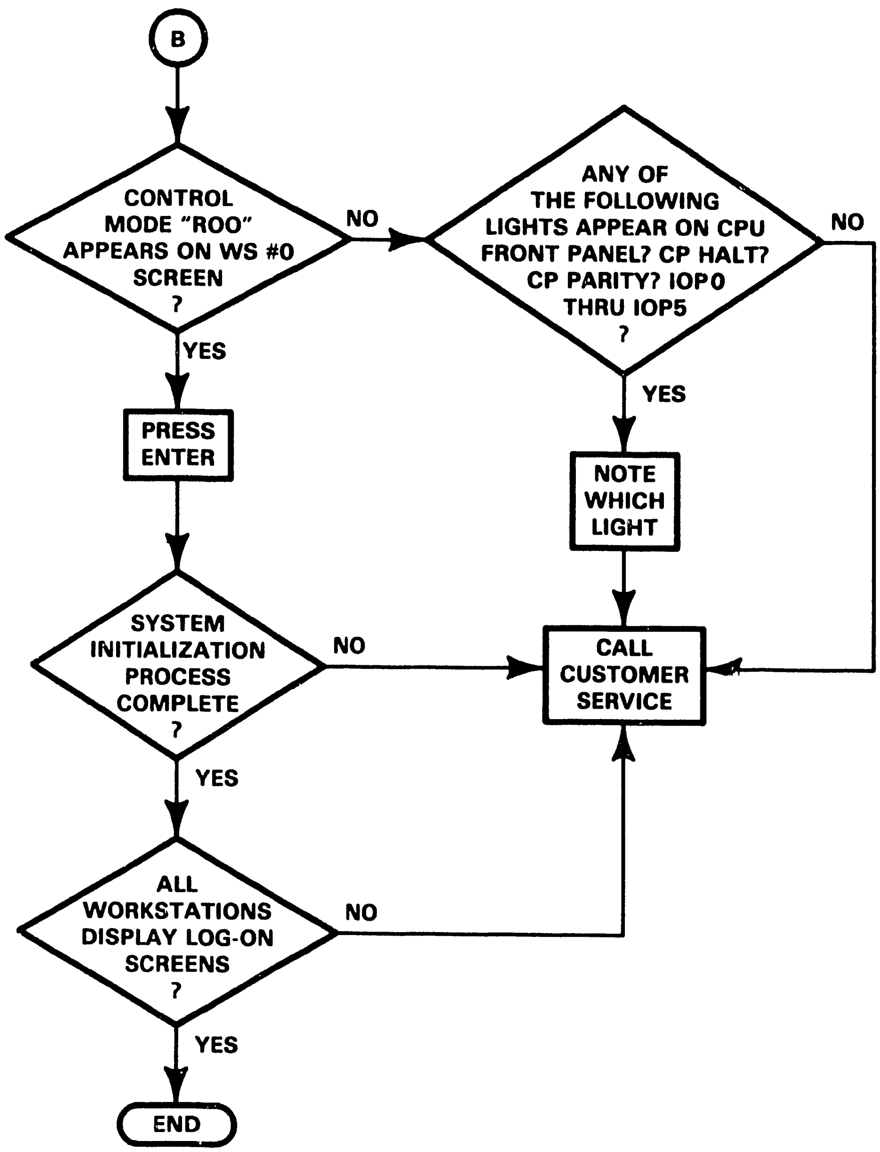


Figure 8-4. Operator Troubleshooting Flowchart (3 of 3)

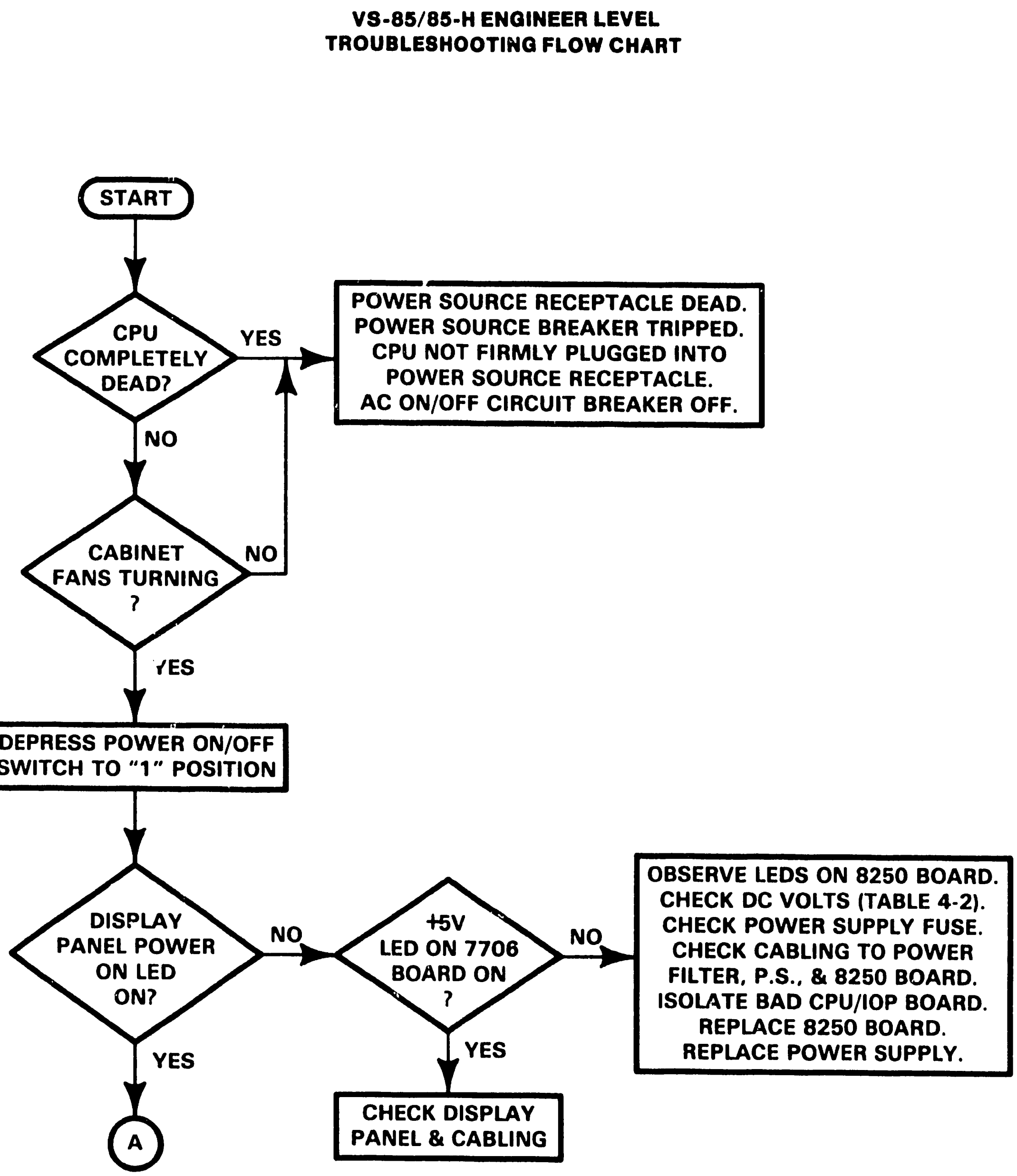


Figure 8-5. CE Troubleshooting Flowchart (1 of 5)

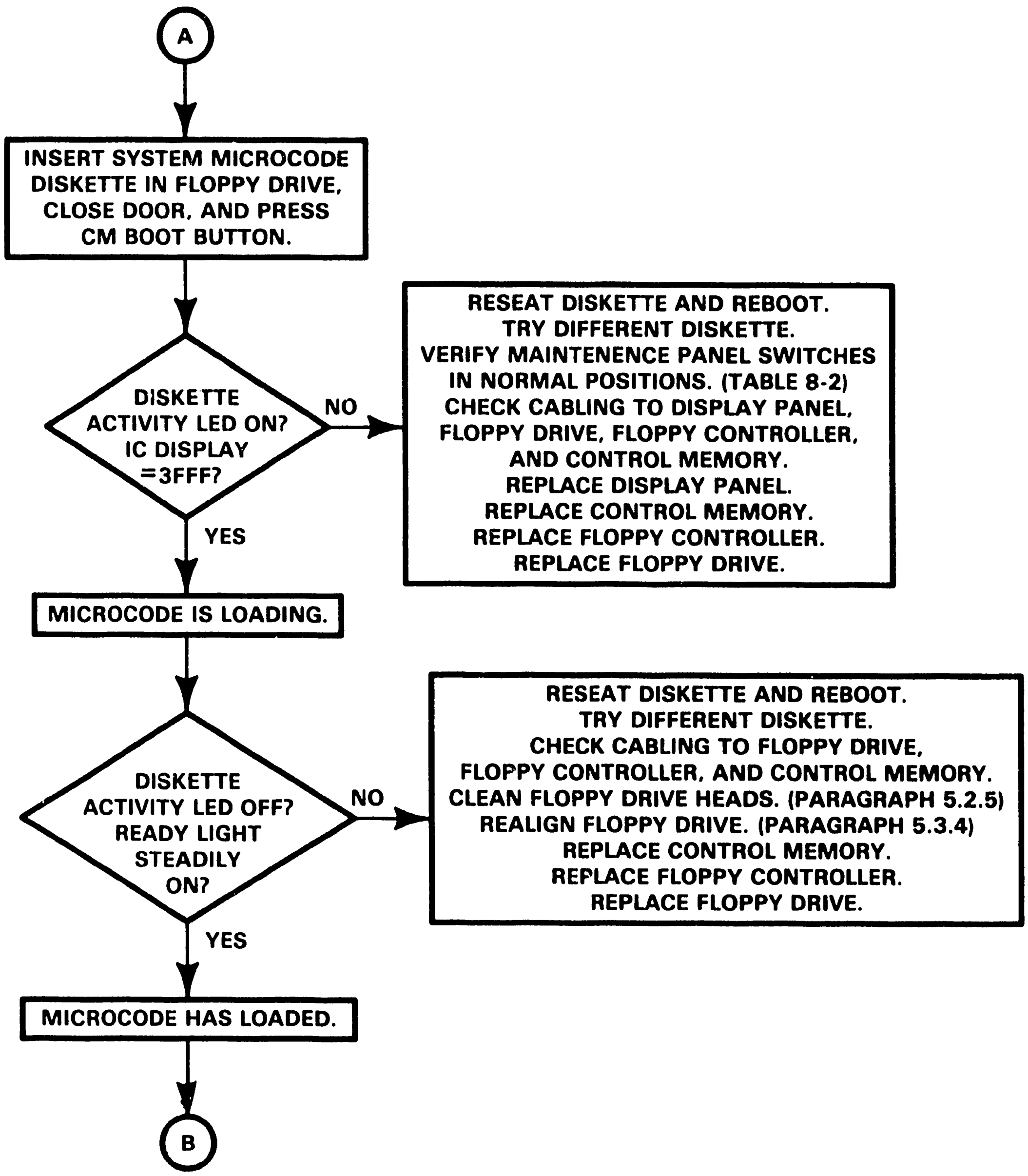


Figure 8-5. CE Troubleshooting Flowchart (2 of 5)

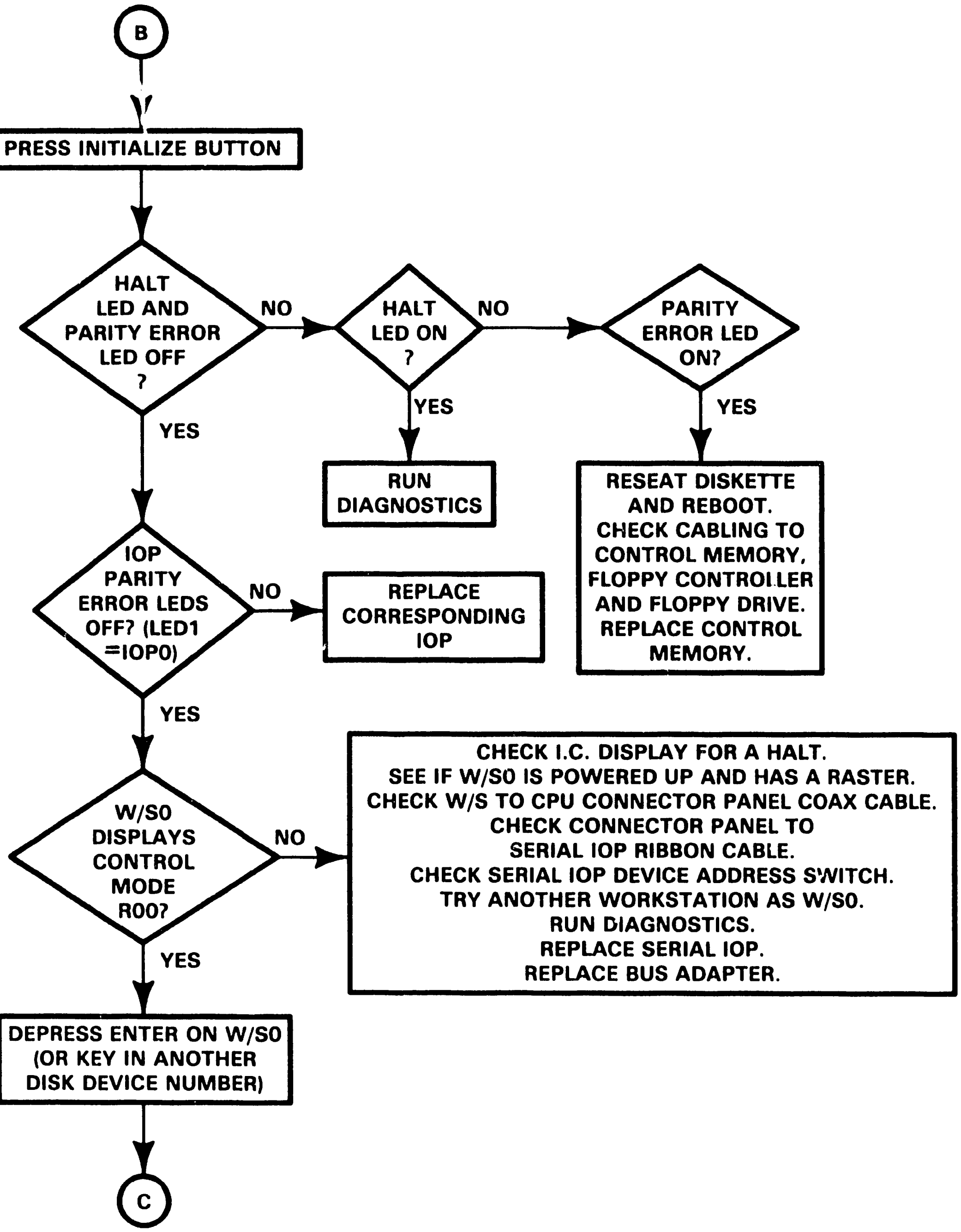


Figure 8-5. CE Troubleshooting Flowchart (3 of 5)

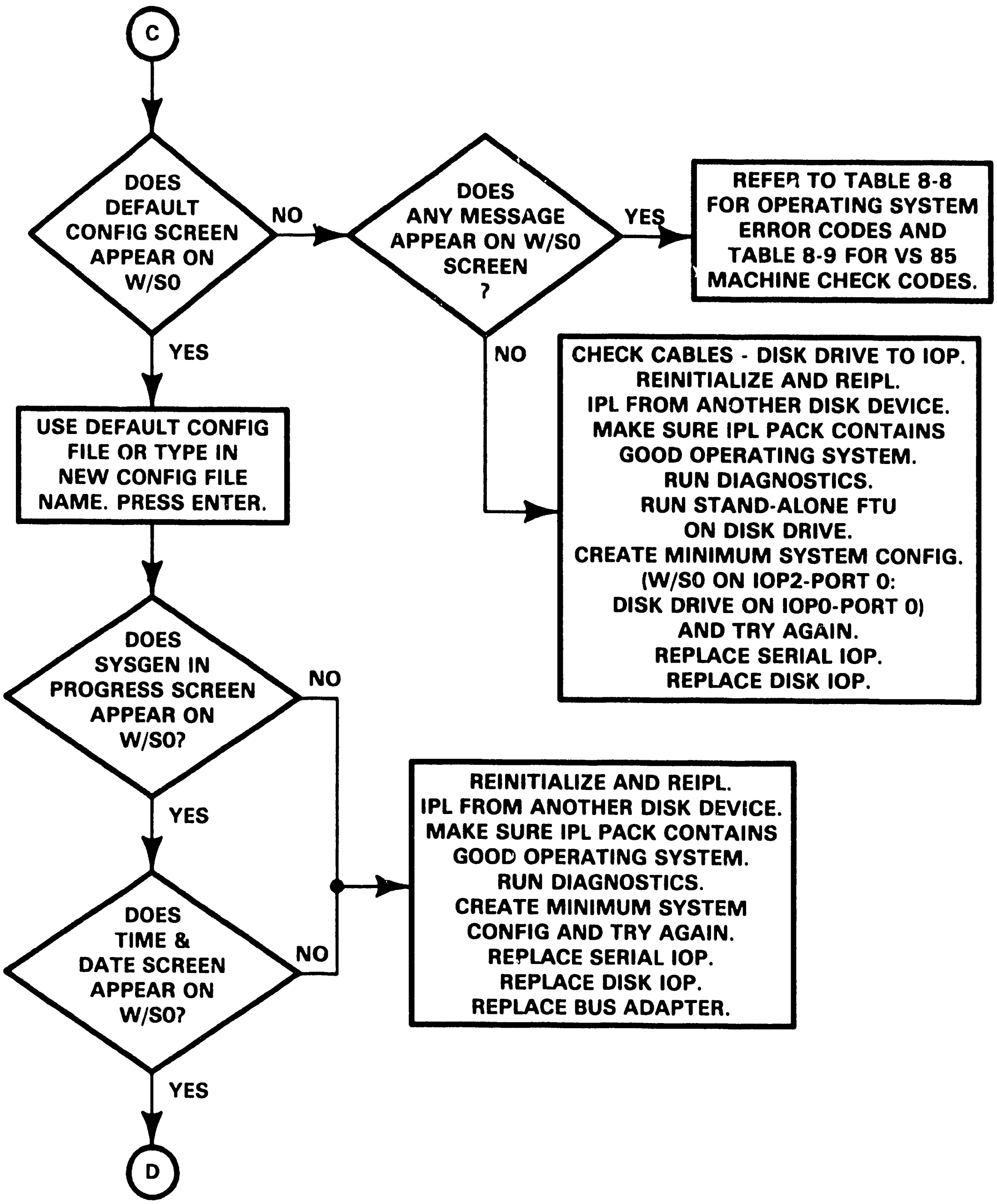


Figure 8-5. CE Troubleshooting Flowchart (4 of 5)

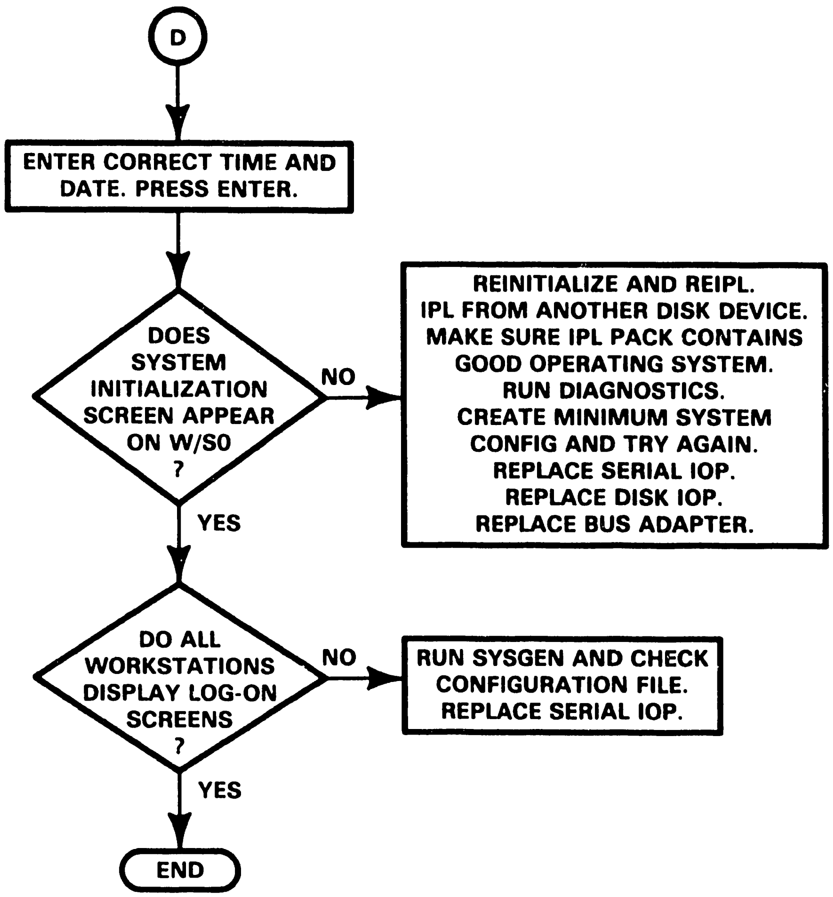


Figure 8-5. CE Troubleshooting Flowchart (5 of 5)

APPENDIX
A

APPENDIX A

MNEMONICS, WORDS/PHRASES, MICROINSTRUCTIONS, & MISCELLANEOUS HARDWARE RELATED FUNCTIONS

VS-85/85-H MNEMONIC LISTS

MNEMONIC	HARDWARE ORIENTATED DEFINITION
ACT	B.A. Active status bit. Accept/reject IOP memory commands
ADMX	Memory Address Multiplexer
ALU	Arithmetic Logic Unit
AMX	A Bus Multiplexer
ATMO	Alignment Trap Memory Address Register 0
ATR1-2	Alignment Trap 1 & 2 Read
ATW	Alignment Trap Write
BA	Bus Adapter
BAAR	Bus Adapter Address Register
BALU	Binary Arithmetic Logic Unit
BAM	Bus Adapter Multiplexer
BAMAL	Bus Adapter Memory Address Latch
BARDLA	Bus Adapter Read Data Latch 'A'
BARDLH	Bus Adapter Read Data Latch High
BARDLL	Bus Adapter Read Data Latch Low
BARDM	Bus Adapter Read Data Multiplexer
BAWDL	Bus Adapter Write Data Latch
BEN	Bus Enable
BMDL	Bus Adapter Memory Data Latch
BMX	B Bus Multiplexer
BRMX	Branch Multiplexer
BS	Buffer Word Select
BSM	Byte Swap Multiplexer
BTA-2	BA Timing Pulses
CABF	Control Memory Address Buffer
CAIN	Carry In
CAR	Current Address Register
CAR/IAR	Current/Indirect Address Register
CAR/IAR L/I	Current/Indirect Address Register Latch/Incrementor
CAS	Column Address Strobe
CBL	C Bus Latch
CBMMX	C Bus/Main Memory Data Multiplexer
CCB1-2	Control Command Bits 1 & 2
CCPMAL	Current CP Memory Address Latch
CDIBF	Control Memory Data Input Buffer
CDOBF	Control Memory Data Output Buffer
CDOMX	Control Memory Data Output Multiplexer
CEN	Column Enable
CH	Current Halfword
CHBF	Current Halfword Buffer
CM	Control Memory
CMAL	Control Memory Address Latch
CMBF	Control Memory Buffer
CMBI	Control Memory Bus Interface. IOP memory control micro inst.
CMPE	Control Memory Parity Error
CMR	Control Memory Register
CMX	C Bus Multiplexer
CMnn	Control Memory bits CMO through CM47
COB	Carry Out Bit
CP/BADM	CP/Bus Adapter Data Multiplexer
CPDL	CP Data Latch

MNEMONIC	HARDWARE ORIENTATED DEFINITION
CPLD	CP Load
CPMAL	CP Memory Address Latch
CPWDR	CP Write Data Latch
CPWSM	CP Word Swap Multiplexer
DALU	Decimal Arithmetic Logic Unit
DCA	CP Decimal Carry status bit
DCAIN	Decimal Carry In
DEC	CP Invalid Decimal Digit status bit
DRY	Data Ready
DTBF	Data Buffer, to Main Memory
ECC	Error Correction Circuitry
ECR	External Condition Register
F	Fault
FA/BSM	FA (Signal FAnn)/Byte Swap Multiplexer
FAM	FA (Signal FAnn) Multiplexer
GT1	Gate Time 1
GT2	Gate Time 2
HS	Halfword Select
IAR	Indirect Address Register
IC	Instruction Counter
ICLD	Instruction Counter Load
IMA	Invalid Memory Address
INIT	Initialize
INVE	Invalid Even
INVO	Invalid Odd
IREG	Indirect Register
IREG COUNTER	Indirect Register Counter
IREG MUX	Indirect Register Multiplexer
IRL	Indirect Register Load
IRM	Interrupt Request Mask
LD	Load
LD	Load
LDOK	Load Disk OK
LDRY	Load Data Ready
LEN1-4	Instruction Length 1-4
M	Monitor (status flag bit)
M4BF	Memory Register 4 Buffer
MAL	Memory Address Latch
MAMX	Memory Address Mux
MAR0	Memory Address Register #0
MAR1	Memory Address Register #1
MAR2	Memory Address Register #2
MBS1	Multiplier Buffer Storage 1
MBS2	Multiplier Buffer Storage 2
MCOS	Memory Complete Out Strobe
MD0-4L	Memory Data Register 0, 1, & 4 Load
MD0-4R	Memory Data Register 0-4 Read
MDR0	Memory Data Register #0
MDR1	Memory Data Register #1
MDR2	Memory Data Register #2
MDR3	Memory Data Register #3
MDR4	Memory Data Register #4
MDR4B	MDR4, Buffered
MLPY	Multiplier Unit

MNEMONIC	HARDWARE ORIENTATED DEFINITION
MMAM	Main Memory Address Multiplexer
MMDL	Main Memory Data Latch
MMOSD	Main Memory Output Selector/Driver
MMP	Main Memory Parity
MMPT	Main Memory Parity Trap
MMRD	Main Memory Read
MODE	B.A. Mode status bit. Allow IOP Write/Read to main memory
MRBAn	Memory Request BA #
MRC	Message Receipt Control
MRI	Memory Request In
MS1-4	(Memory) Module Select 1-4
NAMX	Next Address Multiplexer
NZE	Non Zero
O/EWDM	Odd/Even Word Data Multiplexer
OE/BSM	Odd/Even Byte Swap Multiplexer
OVF	CP Overflow status bit
PB	B.A. Pagebreak status bit. Terminate/continue thru PB
PCBCS	PCB Control Out Strobe
PCBGS	PCB Grant Strobe
PCBRI	PCB Request In
PCBSI	PCB Strobe In
PDA	Physical Device Address
PMR	Program Mask Register
PMX	PMR Multiplexer
PR	Purge Buffer
Q	Qualifier
R	Ripple
R/B	Ready/Busy
R/RMW	Read/Read Modify Write
R/W	Read/Write
RABF	Control Memory Address Buffer
RAS	Row Address Strobe
RBS	Ready/Busy Status IOP bit
RBYT	Read Byte
RCM	Read Control Memory (Deliver byte to PMR)
RCT	Reference & Change Table
RDBF	Control Memory Data Buffer
RDSTR	Read Strobe
REF	Refresh
REQ	Request
RMUX	Rotating Multiplexer
RWMP	Reset Memory Write Pulse
SAMX	Subroutine Address Multiplexer
SCR	Segment Control Register
SR	Shift Register
SSTK	Subroutine Address Stack
STCP	Stop CP
STKMX	Stack Address Multiplexer
SW	Byte Switch
Snn(0-31)	CP Status bits
T	Termination
T-RAM	Translation Random Access Memory
TAL	T-RAM Address Latch
TC	Type Code

MNEMONIC	HARDWARE ORIENTATED DEFINITION
TCAM	Tag Compare Address Multiplexer
TDL	Tag Data Latch
TINT	Tester Interface
TOR	B.A. 'To Be Written Out' status bit. Allow a write to be completed.
TP	Tag Parity
TRMUX	T-RAM Multiplexer
TT	Translation Trap
VMAR	Virtual Memory Address Register
VML	Virtual Memory Address Register load
WA	Write Address Error
WCM	Write Control Memory (Set CM byte from PMR)
WK1	Work Register #1
WK1-A	Work Register 1--A Bus
WK2	Work Register #2
WK2-A	Work Register 2--A Bus
WMX1	WK1 Multiplexer
WMX2	WK2 Multiplexer
WP	Write Pulse

VS-85/85-H MNEMONIC LISTS

MNEMONIC	SOFTWARE ORIENTATED DEFINITION
ARS	Activate Read State
ATR	Word Alignment, Read
ATW	Word Alignment, Write
AWS	Activate Write State
BOP	Branch field of CP micro instruction
CC	Condition Code
CMD	Command
DCT	Device Configuration table
FA	Fetch Address
FLUB	File Length and User Block
IEM	Interrupt Enable Mask
INVA	Invalid Address
IO	Input/Output
IOCA	I/O Command Address
IOCW	I/O Control Word
IOSW	I/O Status Word
LRA	Load Real Address
LRU	Least Recently Used
M	Monitor bit
MMPFT	Main Memory Page Frame Table
MOP	Memory Operation field of CP micro instruction
NOP	No Operation
OS	Operating System
OVF	Overflow
PA	Physical Address
PCW	Program Control Word
PF	Page Frame
PFN	Page Frame Number
POP	Process field of CP micro instruction
PT	Page Table
PTA	Page Table Address
PTE	Page Table Entry
R/C	Reference and Change status bits
RP	Read Protect
RS	Reset State
SA	Set Address
SAI	Set Address Indirect
SIO	Start I/O
SQB	Status Qualifier Byte
VA	Virtual Address
WP	Write Protect

VS-85/85-H WORDS/PHRASES

WORD/PHRASE	DEFINITION
Background Processing	The automatic execution of batched lower priority programs by the Operating System whenever no higher priority programs are being handled.
Base Address	Starting address of a page frame.
Byte Index	A value, when added to a base address, that results in the true physical address of a byte in main memory.
Command Processor	A special program used to call up all system functions.
Concatenated	Linked together in a series.
Current PCW	The active or controlling PCW--the one that pertains to the instruction that is currently being executed.
Data Base Management System	Process (program) that allows multiple users to access common data files.
Demand Paging	A memory management feature where portions of a program are called into memory as they are needed.
Displacement	See Byte Index.
Distributed Processing	Technique of sharing a Central Processor among more than one user.
Dynamic Access Mode	A technique which lets a program switch back and forth between sequential access and random access in the same data file.
File	A logical unit of data records.
Indexed Filing	A technique which stores data records in the order of specified key values.
Interactive	Process to allow users to communicate directly with a system (eg; from a workstation).
Linking	Connecting or tying together.
Locality Of Reference	Quality of a program prepared for maximum execution speed by means of remaining on one page frame as long as possible before branching elsewhere.

WORD/PHRASE	DEFINITION
Macro	A named routine that is called up for processing whenever the corresponding name is specified as part of a high level instruction.
Macro (Inner-layer type)	A series of microinstructions which, when executed, accomplish the purpose of the Macro ... equivalent to a machine instruction, IBM instruction, or Assembler instruction).
Macro (Outer-layer type)	An instruction which, when executed, calls up a sequence of instructions (a subroutine) for execution, and then branches back to the original program.
Macroassembler	A computer having the capability to process defined macros.
Macroinstruction	The name of a routine, prepared in Assembler language, that gets called up for execution whenever the name is used as part of a high level instruction.
Menu	Generally, a list of available options displayed on the CRT when the system is turned on or after an operation has been completed. The term menu should be used to define the presence (existing or desired) of a list of two or more program branching possibilities OR parameter identification inputs that the system must solicit from the operator.
Multiprogramming	Quality of a computer to process more than one program simultaneously.
Outboard Side	External to (away from) the CP.
Page	A block of 2,048 contiguous one-byte virtual memory locations that begin at an address of zero, 2048, or some multiple of 2048.
Page Fault	An indication that a particular page is not in main memory.
Page Fault Exception	An error condition indicating that a page is invalid.
Page Frame	2K blocks of contiguous one-byte physical memory locations that begin at a physical (main) memory address of zero, 2048, or some multiple of 2048.
Page In	Read from disk into main memory.
Page Out	Write to disk from main memory.

WORD/PHRASE	DEFINITION
Page Table	A entry into Translation RAM containing the starting address of a physical page boundary.
Paging Task	That portion of the operating system that controls paging.
Print File	A disk file that is to be printed by a specific printer at the convenience of the Operating System and/or the System Console operator.
Print Queue	A collection of print file records pertaining to one or more printers (also, the sequence list identifying those records and the order in which they are to be printed).
Print Spooling	Temporarily storing print jobs on disk until a printer is available.
Procedure (Language)	A language used to create special text functions to perform operations normally executed interactively at a workstation.
Program Interrupt	A break in the normal sequence of instruction execution because of an error or request for assistance. The supervisory system seizes control to take action.
Prompt	The name of a message (usually a one-liner) directing the operator to perform some action.
Relocatability	Capability of a program to be initiated at any page frame and to randomly occupy any number of additional page frames as a consequence of a linkage of its subsequent parts by an address pointer.
Segment	A block of contiguous one-byte virtual memory locations, with the block beginning on a decimal value virtual address of zero, 1,048,576, or some multiple of that value.
Segment Control Register	A CP register containing the page table virtual address and the page table length.
Sequential Filing	A technique which stores data records in the order in which they are written or entered.
Stack	Local RAM area used for temporary storage by the CP.
Swapped Into	When an entire program is brought into main memory and allowed to run for a certain amount of time.

WORD/PHRASE	DEFINITION
Swapped Out	When an entire program is replaced in main memory by another program which is allowed to run for a certain amount of time.
System Console	The workstation that additionally or alternatively controls special functions not available to other, regular workstations of the system.
Thrashing	The phenomenon of excessively moving pages back and forth between memory and secondary storage (particularly because of removing a page from memory and then immediately needing it again due to a page fault referencing that page).
Type 1 Dialog	Interprocessor Communications dialog used by the VS-85/85-H to support I/O initiation and interrupts.
Type 0 Dialog	Interprocessor Communications dialog used by the VS-85/85-H to support Bus Adapter initialization and diagnostics.
Virtual Address	A disk address containing the location of a page. The disk address will be translated to a physical main memory address by the CP so the page will be read into the correct main memory location for a particular user.

VS-85/85-H CP STATUS BITS

STATUS BITS	BIT NAME	DEFINITION
S0	ALU	Result Bit for last ALU C bus value (=0 or nonzero)
S1	CA	Carry Bit (Carry Out from arithmetic operations)
S2	PAGE1	MAR1 page bit (set on ripple)
S3	PAGE2	MAR2 page bit (set on ripple)
S4	PAGEOV	VMARO page bit (set on ripple)
S5	EXEC	Execute Flag; Stop after Target if EXEC = 1 (in BNM)
S6	M2H	Bit is set = to MAR2 bit 30 when MAR2 is destination MAR for translation operation
S7	M2B	Bit is set = to MAR2 bit 31 when MAR2 is destination MAR for translation operation
S8	SGN	Set from high order bit of 32-bit C bus, etc. Value = 0/1 indicates two's complement sign bit
S9	DEC	Invalid decimal digit bit. (Set = 1 by hardware if invalid decimal digit found)
	OVF	Overflow bit (2's complement arithmetic). OVF = (CA-out) XOR (CA-out at bit position 1)
S10	DCA	Carry bit for Decimal process operations
S11	PCA	Carry out bit set by microopcode = ACP only
	SPX	Result bit (inverse) set only on microopcode = CL. Also set as comparison bit for microopcode = COMP.
S12	ALUS	Zero/non Zero status bit for 4-bit Shift-hold register. Set only on 4-bit shift instructions.
S13	X2	This bit = 0 if IREG 4-7 = 0; else = 1
S14	R1ODD	This bit is set = IREG bit 3
S15	FLT	This bit is set based on IREG and ILC (CH0-CH1). (ILC = instruction length code in Current Halfword).
	RR Case	ILC = 00; set FLT = IRG0 or IRG3 or IRG4 or IRG
	RX Case	ILC not = 00; set FLT = IRG0 or IRG3
S16	CS2	Comparator enable bit (Set by CP4; inspected by hardware)
S17	STATE	Software bit for privileged status (on translation)
S18	MS1	MAR select bit for translation fault involving MAR1 or MAR2 (MS1=0 for VA in MAR1; MS1=1 for VA in MAR2). Note - MS1 is always set = 0/1 for translation operations involving MAR1 or MAR2
S19	STK	This bit = 0 if IREG 0-3 = 0; else = 1
S20	BNK	Used as CP4 stack address bit. (Set by BNM)
S21	PAGE0	MAR0 page bit (set on ripple)
S22	M0F	MDR0 full bit (empty = 0, full = 1)
S23	M1F	MDR1 full bit (empty = 0, full = 1)
S24	DEBUG	One or more Software Traps enabled if set = 1
S25	IOMASK	IO Interrupts enabled if set = 1
S26	CS4	Clock Interrupt enabled if set = 1
S27	ISET	Bit 1 of the multi-way BNM microaddress
S28	CS1	Hardware Counter Overflow bit
S29	CS3	Clock Interrupt Request Pending if set = 1
S30	EXT	External Event bit (see ECR for setting)
S31	IO3	BA Interrupt Request Pending if bit = 1

VS-85/85-H MICRO-INSTRUCTIONS

MNEMONIC	MICRO-INSTRUCTION ORIENTATED DEFINITION
A	Add
AC	Add with Carry
ACO	Add with Carry (CA in = 1)
ACP	Add for Pagespan Check
ACT	Add with Carry (Overflow Trap option)
ACV	Add with Carry (Overflow bit set)
ACZ	Add with Carry (CA in = 0)
AND	Logical AND
ANDI	Logical AND Immediate
ANDS	Logical AND (with SGN bit set)
ASH	Add/Subtract High
ASL	Add/Subtract Low
AZH	Add High with Zeros
AZL	Add Low with Zeros
BD	Generate Base Displacement Address
CAR	Compare Arithmetic and set CC
CCK	Clear Counter (Program Clock support)
CCS0	Set Logical CC (1-2 on SPX)
CCS1	Set Arithmetic CC (0-2 on ALU + SGN)
CCS2	Set Full Logical CC (0-3 on CA / ALU)
CCSET	Set Explicit CC Value (0-3)
CKECC	Check ECC (Read or Write control)
CL	Compare Logical and set CC
CMC	Clock Margin Control (Reset)
CMCF	Clock Margin Control Fast
CMCS	Clock Margin Control Slow
COMP	Compare Arithmetic
DAC	Decimal Add with Carry
DACZ	Decimal Add with Carry (DCA in = 0)
DSC	Decimal Subtract with Carry
DSCO	Decimal Subtract with Carry (DCA in = 1)
HALT	Halt Microprogram Execution
INIT	Initialize an IOP
LCOMP	Load Comparator (Program Clock support)
LTRAM	Load a T-RAM entry
MCA	Move and set Arithmetic CC
MCH	Move Current Halfword
MCHX	Move Current Halfword and Extend
MCL	Move and set Logical CC
MDEC	Move and Decrement IREG
MINC	Move and Increment IREG
MNUM	Move Numeric
MV	Move
MVA	Move Address (high byte = 0)
MVH	Move Halfword
MVN	Move (without setting ALU or C Bus Latch)
MVS	Move (with sgn bit set)
MVX	Move (with nonstandard B Bus)
OR	Logical OR
ORI	Logical OR Immediate
RBCL	Read a BCL entry (hi-part) (also RBCLL - low part)

MNEMONIC	MICRO-INSTRUCTION ORIENTATED DEFINITION	
RBTL	Read a BTL entry (hi-part)	(also RBTLL - low part)
RCM	Read Control Memory	
RECR	Read ECR	
RIPC	Read IPC Data	
RRCT	Reset an RCT entry	
RSW	Read Switches	
S	Subtract	
SC	Subtract with Carry	
SCO	Subtract with Carry	(CA in = 1)
SCOMP	Store Comparator	(Program Clock support)
SCT	Subtract with Carry	(Overflow Trap option)
SCV	Subtract with Carry	(Overflow bit set)
SCZ	Subtract with Carry	(CA in = 0)
SEND	Send IPC data to another Processor	
SHL4	Shift Left 4 bits	
SHLO4	Shift Left 4 bits	(4 bits in = 1111)
SHLZ4	Shift Left 4 bits	(4 bits in = 0000)
SHR	Shift Right 1 bit	
SHR4	Shift Right 4 bits	
SHRO	Shift Right 1 bit	(SCA in = 1)
SHRO4	Shift Right 4 bits	(4 bits in = 1111)
SHRZ	Shift Right 1 bit	(SCA in = 0)
SHRZ4	Shift Right 4 bits	(4 bits in = 0000)
STAT	Move IREG to Status bits	(IREG 4-7 to S12-S15)
STCK	Store Counter	(Program Clock support)
SW16	Move and Switch	
TRCT	Test an RCT entry	(set M2H, M2B)
WCM	Write Control Memory	
WECR	Write ECR	(5-bit unit)
WIPC	Write IPC Data	
XOR	Logical Exclusive OR	
XORI	Logical Exclusive OR Immediate	

DEFINITIONS FOR VS-85/85-H SIGNAL NAMES

SIGNAL	DEFINITION	SOURCE	DESTINATION	DESCRIPTION
AB0-AB31	A Bus	A Bus	B Bus	Data for Binary & Decimal ALUs
BA0-23	Bus Adapter Memory Address	BA	MCI	Bus Adapter main memory addresses via MCI
BAC0-2	Bus Adapter Command	BA	MCI	Bus Adapter command bits
BARD0-31	Bus Adapter Read Data	BA	MCII	One word of data from BA to be written to main memory
BAWD0-31	Bus Adapter Write Data	MCII	BA	One word of data from main memory to BA
BCH0-7	Byte Of Current Halfword	B Bus	CM	Address or index for Branch to Next macroinstruction
BMA3-6	Bus-Main Memory Address	IOP	BA	IOP command bits for the BA
BMAR0-21	Buffered Memory Address	MCI	Main Memory	Main Memory addresses from either CP or the BA
BMDH0-7	Bus-Memory Data High	IOP	BA	One byte of IOP data for BA
BMDL0-7	Bus-Memory Data Low	IOP	BA	One byte of IOP data for BA
CB0-CB31	C Bus	B Bus	A Bus	C Bus output data
CM0-47	Control Memory Data Bits	CM	A Bus B Bus MCI MCII	Micro Instruction (Uses CM0-26) (" " ")
DAB0-7	Device Address Bits	BA	IOP	Device Address for IOP
DIRD0-31		MCII	MCI	One word of main memory data for CP
INIT0-7	Initialize	BA	IOP	Initialize (each) IOP
IR0-7	Indirect Register Counter	B Bus	A Bus	Indirect Stack addressing
LIC0-13		Mini-Disk Control	CM & Maint Panel	Addresses for writing CM RAM during microcode load

SIGNAL	DEFINITION	SOURCE	DESTINATION	DESCRIPTION
LWDO-7		Mini-Disk Control	CM	Data for writing CM RAM during microcode load
MA0-23	Memory Address	B Bus	MCI	CP memory addresses for main memory
MGS0-7	Memory Grant Strobe	BA	IOP	IOP (each) is granted main memory access
MM0-15	Main Memory	BA	IOP	Data or status returned to IOP along with IAR/CAR addresses
MM0-31	Main Memory	MCI	A Bus B Bus	Word of data from main memory for CP
MMCB1-2	Main Memory Bits Control	IOP	BA	IOP command bits for the BA
MMRD0-31	Main Memory Read Data	Main Memory	MCII	One word of memory read data
MMWD0-31	Main Memory Write Data	MCII	Main Memory	One word of data to be written to main memory
MRI0-7	Memory Request In Strobe	IOP	BA	IOP (each) is requesting main memory access
MS1-2	Module Select	MCI	Main Memory	Main memory board select from either CP or the BA
PCBGS0-7	Processor Communications Bus Grant Strobe	BA	IOP	IOP (each) has been granted a CP interrupt
PCBRI0-7	Processor Communications Bus Request In	IOP	BA	IOP (each) is requesting a CP interrupt
RA0-13	RAM Addresses	B Bus	CM	Addresses for Control Memory write
RD0-7	RAM Data	B Bus	CM	Data for Control Memory write
WD0-31	Write Data	A Bus	MCII	CP write data to main memory
WP0-6	Write Parity	MCII	Main Memory	Parity bits for word of write data
XL0-6	Read Parity	Main Memory	MCII	Parity bits for word of read data

VS-85/85-H MICRO-INSTRUCTION FIELDS

48 BIT MICRO-INSTRUCTION (CONTROL MEMORY BITS)		
PROCESS FIELD (POP)	MEMORY FIELD (MOP)	BRANCH FIELD (BOP)
CM0	CM22	CM30 — CM47

Process field (CM0-CM21)
1. Microopcode field
2. A Bus operand field
3. B Bus operand field (restricted operands)
4. C Bus operand field

PROCESS FIELD FORMAT			
MICRO OPCODE	A BUS OPERAND	B BUS OPERAND	C BUS OPERAND
CM0	CM7	CM13	CM16 — CM21

Memory field (CM22-CM29)
1. Memory Address Register (MAR) select
2. Memory operation
3. Translation and MAR ripple

MEMORY FIELD FORMAT		
MAR SELECT	MEMORY OPERATION	TRANSLATION AND MAR RIPPLE
CM22	CM24	CM27 — CM29

MEMORY ADDRESS REGISTER (MAR) SELECT FIELD		
CM22	CM23	MAR REGISTER SELECTED
0	0	MAR0
0	1	MAR1
1	0	MAR2
1	1	MAR2X

VS-85/85-H MICRO-INSTRUCTION FIELDS

MEMORY OPERATIONS FIELD				
CM24	CM25	CM26	MEMORY OPERATION	MAR SELECTION
0	0	0	NO OPERATION (NOP)	ANY MAR SELECTION
0	0	1	MULTIPLY	ANY MAR SELECTION
0	1	0	WRITE BYTE	MAR2 ONLY
0	1	1	WRITE WORD	MAR2 ONLY
0	1	1		
1	0	0	READ BYTE	MAR1 OR MAR2
1	0	1		
1	0	1		
1	1	0	READ WORD	MAR1, MAR2, OR MAR2X
1	1	0		
1	1	1		

MEMORY TRANSLATION AND MAR RIPPLE FIELD			
CM27	CM28	CM29	TRANSLATION AND RIPPLE
0	0	0	NO TRANSLATION OR RIPPLE
0	0	1	READ TRANSLATION (USE ART1)
0	1	0	READ TRANSLATION (USE ATR2)
0	1	1	WRITE TRANSLATION
1	0	0	RIPPLE +1
1	0	1	RIPPLE -1
1	1	0	RIPPLE +4
1	1	1	RIPPLE -4

NOTE: ATR1 = Address Translation Trap 1
ATR2 = Address Translation Trap 2

VS-85/85-H MICRO-INSTRUCTION FIELDS

Branch field (CM30-CM47)
1. Branch operation field
2. Microaddress (or other operands)

BRANCH FIELD FORMAT 1 - FULL-ADDRESS BRANCH		
BRANCH OPCODE	MICROADDRESS (14 BITS)	
CM30	CM34	CM47

BRANCH FIELD FORMAT 2 - CONDITIONAL BRANCH			
BRANCH OPCODE	STATUS SELECT	MICROADDRESS (8 LOW BITS)	
CM30	CM34	CM40	CM47

BRANCH FIELD FORMAT 3 - STATUS BIT MANIPULATION				
BRANCH OPCODE	STATUS SELECT A SELECT	STATUS OPCODE	STATUS BIT B SELECT	
CM30	CM34	CM39	CM42	CM47

VS-85/85-H STACK ORGANIZATION AND REGISTER LOCATION

REGISTER LOCATION	32 BITS WIDE	
0–15	GENERAL REGISTERS	BANK '0'
16–31	F-P REGISTER	BANK '0'
32–63	FILE REGISTER (0-31)	BANK '0'
64–79	AUXILIARY CP REGISTER	BANK '1'
80–95	CONSTANTS	BANK '1'
96–127	CONTROL REGISTER (0-31)	BANK '1'
128–256	T-RAM MONITORING	

VS-85/85-H EXTERNAL CONDITION REGISTER STATUS BITS (MCII)

STATUS BIT	BIT NAME	DEFINITION
ECR0	IN1	Initialize/enable B.A. #1.
ECR1	IN2	Initialize/enable B.A. #2.
ECR2	IN3	Initialize/enable B.A. #3.
ECR3	EXT HDWR	VS hardware present (always on)
ECR4	MON	Monitor System Code.
ECR5	ECC E/D	Enable/disable ECC.
ECR6	Reserved	
ECR7	Reserved	
ECR8	Cache	Enable/disable Cache (C$\overline{E}$/D)
ECR9	Reserved	
ECR10	WP	C.P. write parity error (preset by MMP and $\overline{CP8W}$).
ECR11	WA	Incorrect C.P. write address (preset by UNVA and CPW).
ECR12	RJ	Reject IPC data from C.P. (preset by RJ and CP).
ECR13	Interlock	CPU to BA communications.
ECR14	Reserved	
ECR15	Reserved	
ECR16	Reserved	
ECR17	Reserved	
ECR18	Reserved	
ECR19	CM	Control mode button (preset by CM).

VS-85/85-H EXTERNAL CONDITION REGISTER STATUS BITS (SBC)

STATUS BIT	BIT NAME	DEFINITION
ECR0	IN1	Initialize/enable B.A. #1.
ECR1	IN2	Initialize/enable B.A. #2.
ECR2	IN3	Initialize/enable B.A. #3.
ECR3	IN4	Initialize/enable B.A. #4.
ECR4	MON	Monitor System Code.
ECR5	ECC E/D	Enable/disable ECC.
ECR6	BTL	Enable/disable BTL.
ECR7	BCL	Enable/disable BCL.
ECR8	Cache	Enable/disable Cache ($C\overline{E}$/D)
ECR9	Reserved	
ECR10	WP	C.P. write parity error (preset by MMP and $\overline{CP8W}$).
ECR11	WA	Incorrect C.P. write address (preset by UNVA and CPW).
ECR12	RJ	Reject IPC data from C.P. (preset by RJ and CP).
ECR13	Reserved	
ECR14	HM	Cache hit (preset by $\overline{MISS}$ high.
ECR15	CAM	Cache miss (preset by MISS low.
ECR16	RJO	Reject IPC data sent from any processor (preset by RJ and CP).
ECR17	BTLA	BTL active, stored error entry.
ECR18	BTLO	BTL overflowed.
ECR19	CM	Control mode button (preset by CM).
ECR20	BA1	B.A. #1 requested attention ($\overline{REQ1}$).
ECR21	BA2	B.A. #2 requested attention ($\overline{REQ2}$).
ECR22	BA3	B.A. #3 requested attention ($\overline{REQ3}$).
ECR23	BA4	B.A. #4 requested attention ($\overline{REQ4}$).

VS-85/85-H TRAPS

TRAP NAME	CONDITION		TRAP ADDRESS
POWERON	CP4 Initial Power-on trap		0000
LOAD	CP4 Initialize trap		0001
INVA	Invalid (physical) Memory Address		0002
TT0	MAR0 Translation trap		0003
TT1	MAR1/MAR2 Translation trap		0004
TT2	Protection trap (any MAR)		0005
ATR1	Word Alignment trap	(CM27-29 = 001)	0006
ATR2	Word Alignment trap	(CM27-29 = 010)	0007
ATW	Word Alignment trap (write)		0008
ATM0	Alignment trap MAR0 (halfword)		0009
OVFT	Overflow Trap (ACT or SCT instructions)		000A
MMPT	Main Memory Parity trap		000B
BEX	Execute Target trap	(EXEC = 1)	000C
PAR	CP Control Memory Parity trap		000D
BX	External Event trap	(EXT = 1)	0011
BDEBUG	Software trap	(DEBUG = 1)	0012
BCLKM	Clock Maintenance trap	(CS1 = 1)	0013
BCLKI	Clock Interrupt	(CS3 = 1; CS4 = 1)	0014
BIO	IO Interrupt	(IO3 = 1; IOMASK = 1)	0015
BPAGE	Pagebreak trap	(PAGEOV = 0)	0016
BENTRY	Entry Pagebreak	(new PAGEOV = 0) and not rr case)	0017

Note: - Trap BEX and traps 0011-0017 are Branch to Next Macro-related traps.

VS-85/85-H CP MEMORY OPERATIONS DECODING (MEMORY CONTROL)

CP REQUEST FOR MEMORY OPERATIONS			
CM24	CM25	CM26	CP OPERATION
0	0	0	NO OPERATION
0	0	1	MPLY
0	1	0	WRITE 8
0	1	1	WRITE 32
1	0	0	READ 8
1	0	1	
1	1	0	READ 32
1	1	1	

CP commands decoded into following memory instructions
1. NOP - No memory operation
2. MPLY - Multiply operation
3. Write 8 - Write byte. Write the low order byte of MDR4 to memory
4. Write 32 - Write word. Write the MDR4 word to memory
5. Read 8 - Read byte into MDR2 or MDR4
6. Read 32 - Read word into MDR2 or MDR4

VS-85/85-H CP MEMORY OPERATIONS DECODING (MEMORY CONTROL)

BUS ADAPTER REQUEST FOR MEMORY OPERATIONS			
BAC0	BAC1	BAC2	BUS ADAPTER OPERATION
0	0	0	NO OPERATION
0	0	1	IPCB
0	1	0	WRITE 8
0	1	1	WRITE 16
1	0	0	
1	0	1	READ 32
1	1	0	WRITE 32
1	1	1	

BA commands decoded into following memory instructions
1. NOP - No memory operation
2. IPCB - Interprocessor Communications
3. Write 8B - Write byte. (Read Modified Write-1). Direct nonbuffered IOP write
4. Write 16B - Write halfword. (Read Modified Write-2). Standard buffered halfword IOP write
5. Write 32B - Write word. Buffered IOP word write
6. Read 32B - Read word

APPENDIX B

APPENDIX B

VS-85 TO VS-100 CONVERSION

INTRODUCTION

Customers who have either VS-85-2 or VS-85-4 model CPUs (with Cache Memory/SBC combination), and who have outgrown their VS-85 system, now have the option of converting the VS-85 CPU to a VS-100 CPU.

NOTE

The VS-85-H is not upgradeable to a VS-100 since the VS-100 does not support the internal fixed disk drive.

Basically the procedure involves bringing in a new VS-100 chassis with power supplies and an extended IOP Motherboard; removing the CPU and IOP circuit boards, and the I/O panels from the VS-85; and installing them in the VS-100 chassis.

The procedure will not be detailed in this PUB. Instead, references to paragraphs and figures in the documentation listed below will be made. These documents contain all the necessary removal, installation, and verification procedures for both the VS-85 and the VS-100. These documents should be on hand during the conversion.

1. Related Documents

DOCUMENT TITLE	WLI PART NUMBER
VS-85/85-H Product Maintenance Manual	741-1492-A
VS-100 Product Maintenance Manual	729-0871-A
VS-100 Service Handbook	729-1098-A
VS-85/90/100 Microdiagnostics Handbook	729-1309
VS Diagnostics Handbook, Volume 2	729-1257-A
VS Software Bulletin - Release 5.3	800-3109
VS Software Bulletin - Release 5.3 Addendum	800-3109.01
VS Software Bulletin - Release 5.3 Addendum	800-3109.02
VS Software Bulletin - Release 6.0	800-3111-01
VS Software Bulletin - Release 6.20	800-3114-01
VS Software Bulletin - Release 6.30	800-XXXX-XX

2. Hardware Requirements

a. First option:

DESCRIPTION	PART NUMBER	COMMENTS
VS-85-2 CPU (With Cache)	157/177-7226	Must have Cache Memory/SBC and 2 megabytes of main memory
VS-100 CPU	UJ-4001	Chassis with power supplies

b. Second option:

DESCRIPTION	PART NUMBER	COMMENTS
VS-85-4 CPU (With Cache)	157/177-7228	Must have Cache Memory/SBC and 4 megabytes of main memory. (Two 2-megabyte main memory boards.)

b. Second option: (cont'd)

DESCRIPTION	PART NUMBER	COMMENTS
VS-100 CPU	UJ-4002	Same as UJ-4001, except contains four 1-megabyte main memory boards to replace two 2-megabyte main memory boards.

NOTES

a. Part number prefix 157 = 47-63 cps/230 Vac systems.
b. Part number prefix 177 = 47-63 cps/115 Vac systems.

3. Software Requirements

DESCRIPTION	WLI P/N
Microdiagnostic Package (VS-100)	195-2754-8
Operating System 5.03.90 or above	

PROCEDURE

1. Unpack the VS-100 main frame cabinet (paragraph 3.4, VS-100 Product Maintenance Manual).
2. Check the source power supplied for the VS-100 (paragraph 3.7, VS-100 Product Maintenance Manual).
3. Power up the unloaded VS-100 cabinet and check the dc voltages at the power supplies (paragraph 6.4, VS-100 Product Maintenance Manual, or VS-100 Service Handbook). Make any necessary adjustments.
4. Power off the VS-100.
5. Power down the peripherals and power off VS-85 main frame (paragraph 3.7, VS-85/85-H Product Maintenance Manual).
6. Remove the top and front covers from VS-85 (paragraphs 5.3.6.1 and 5.3.6.2, VS-85 Product Maintenance Manual).
7. Remove the card rails from VS-85.
8. Remove the IOP to I/O panel cables from the VS-85 IOPs (paragraph 5.3.6.4, VS-85 Product Maintenance Manual).
9. Remove the I/O panels from the VS-85 (figure 4-14A, VS-85 Product Maintenance manual) and install them in the proper locations on the VS-100 (figure 3-19, VS-100 Product Maintenance Manual).
10. Remove all cables from the VS-85 boards (paragraphs 5.3.6.3 and 5.3.6.4, VS-85 Product Maintenance manual), except the three Cache to System Bus Controller (SBC) cables. Save any interboard cables.
11. Remove the Control Memory board from the VS-85 (paragraph 5.3.6.3, VS-85 Product Maintenance Manual) and install it in the proper location in the VS-100 CPU Motherboard (paragraph 3.6.1, VS-100 Product Maintenance Manual). Connect the cables to the Control Memory board (paragraph 3.6.3, VS-100 Product Maintenance Manual).

NOTE

As the boards are removed from the VS-85, the edge connectors may be cleaned with an alcohol pad, WLI P/N 660-0130. Do NOT clean the edge connectors with an eraser.

12. Continue removing the boards from the VS-85, installing them in the VS-100, and connecting the cables. Do this one board at a time and install them in the correct order. The Cache and SBC boards can be removed and installed as a pair.

13. If the VS-85 has any 2 Megabyte Main Memory boards (WLI P/N 210-8203), they must be replaced with 1 Megabyte Main Memory boards (WLI P/N 210-7803). Install two 1 Megabyte boards for each 2 Megabyte board removed. (Memory size switches on the Cache Memory board should remain the same unless Main Memory size will increase or decrease. Refer to VS-100 Service Handbook.)
14. The Bus Adapter must be installed in the last slot of the CPU Motherboard as BA 1.

NOTE

210-7911 and 210-8311 Bus Adapters are compatible and interchangeable only in the VS-100 configuration.

15. The four Cache/SBC to BA jumper cables removed from the VS-85 can't be used in the VS-100 because they are too short to bridge the space over the Main Memory board slots. Replace these cables with four VS-100 Cache/SBC to BA cables, WLI P/N 220-3116, included in the upgrade kit.
16. Make sure that the BA number and I/O slot selection switches on the IOP conform to the IOP position in the IOP Motherboard. (See figure 3-7 and refer to paragraph 3.6.2 of the VS-100 Product Maintenance Manual, or to the VS-100 Service Handbook, for the proper locations of the IOP's.)
17. Connect the I/O panel cables to the proper IOPs (paragraph 5.3.6.4, VS-85 Product Maintenance Manual).
18. Power up the VS-100 (paragraph 3.7.2, VS-100 Product Maintenance Manual) and check the dc voltages again.
19. Run the VS-100 microdiagnostics (VS85/90/100 Microdiagnostics Handbook).
20. Create a minimum system by connecting a serial workstation to IOP #2, Port 0, BA#1, and the system disk drive to IOP #0, Port 0, BA#1.
21. Load the system microcode and IPL the system (paragraph 3.7.3, VS-100 Product Maintenance Manual).
22. Run SYSGEN to reconfigure the system, if necessary.
23. Connect the rest of the peripherals (figure 3-19 and paragraph 3.8.1, VS-100 Product Maintenance Manual) and run on-line peripheral diagnostics (VS Diagnostics Handbook, Volume 2).
24. Send the VS-85 chassis back to "Return Products".

APPENDIX
C

APPENDIX C

VS-85/85-H ASYNC DEVICE CONTROLLER

C.1 GENERAL

This appendix describes the VS-85/85-H 22V36 Async Device Controller (ADC). Included in this appendix is information on theory of operation, installation, maintenance, troubleshooting, and field replaceable units (FRUs).

C.2 HARDWARE DESCRIPTION

The heart of the ADC is an Intel 8086 Microprocessor, which supervises eight RS-232-C I/O channels with programmable baud rate (1200-19.2 KB) and protocol for each channel, and one Wang PC-compatible parallel printer port . The ADC can support eight Wang 2110 workstations or eight async devices with RS-232-C interface. The eight serial devices are driven through an async serial link via a full duplex RS-232-C connector. The ADC communicates with the host VS through a 2K-word direct memory access (DMA).

The ADC consists of the following four pc boards:

- TCP/IOP Motherboard (WLI P/N 210-7826) -- This previously existing 16 x 16.5 inch board plugs directly into the VS-85/85-H motherboard and contains the IOP hardware. The 7826 is used as the motherboard for the 210-8168 device adapter (see below) in order to maintain compatibility with the existing IOP software.

- Controller Board (WLI P/N 210-8168) -- This 16 x 14 inch 8086-based device adapter board plugs directly into the TCP/IOP Motherboard and contains the electronics and logic (except for transceivers and IOP). The controller board also has four 40-pin cable connectors and one 26-pin cable connector to carry the signals for the eight RS-232-C ports via ribbon cables to the back panel assembly.

- Line Driver/Receiver Daughterboard (WLI P/N 210-8324) -- Discrete drivers and receivers, which support the eight RS-232-C ports and the printer port and provide communications up to 2000 feet, are located on this 5 x 9 inch board. It plugs into the 210-8323 connector board and is located just inside the back panel of the system. The transceiver board interfaces the connector board to the controller board via ribbon cables.

- Line Driver/Receiver Motherboard (WLI P/N 210-8323) -- This 5 x 9 inch board fastens directly to the back panel of the system and provides the eight RS-232-C connectors to the user. It is the motherboard into which the 8324 board plugs. The 8323 and the 8324 boards fasten together to form the Async Rear Panel Assembly.

C.3 SOFTWARE DESCRIPTION

The ADC requires Operating System (OS) Release 6.4X.XX to provide the support to load a microcode file to the ADC and to support the eight async workstations.

C.4 FUNCTIONAL DESCRIPTION

The following paragraphs give a brief overview of the operation of the VS-85/85-H ADC. An upper level block diagram (figure C-2) is provided to aid the reader in understanding the workings of and the relationship between the different functional areas.

C.4.1 MEMORY

ADC memory is organized in three parts (see figure C-1):

- Code RAM
- DMA Memory
- PROM Memory

1024K		FFFFF
1016K	8K Bytes PROM	FE000
1012K	Not Used	FD000
1008K	2K Words DMA Static Memory	FC000 FBFFF
	Extended Code RAM	
256K		40000 3FFFF
	256K Bytes Dynamic Code RAM	
0 Bytes		00000

Figure C-1. ADC Memory Organization

C.4.1.1 Code RAM

Code RAM is a 256K, 640K, or 1 Meg (depending on whether and to what extent 256K chips are used) dynamic random access memory, accessible to both the 8086 microprocessor and the direct memory access (DMA) controller. The 8086 uses code RAM to buffer data to and from the I/O ports. The DMA controller

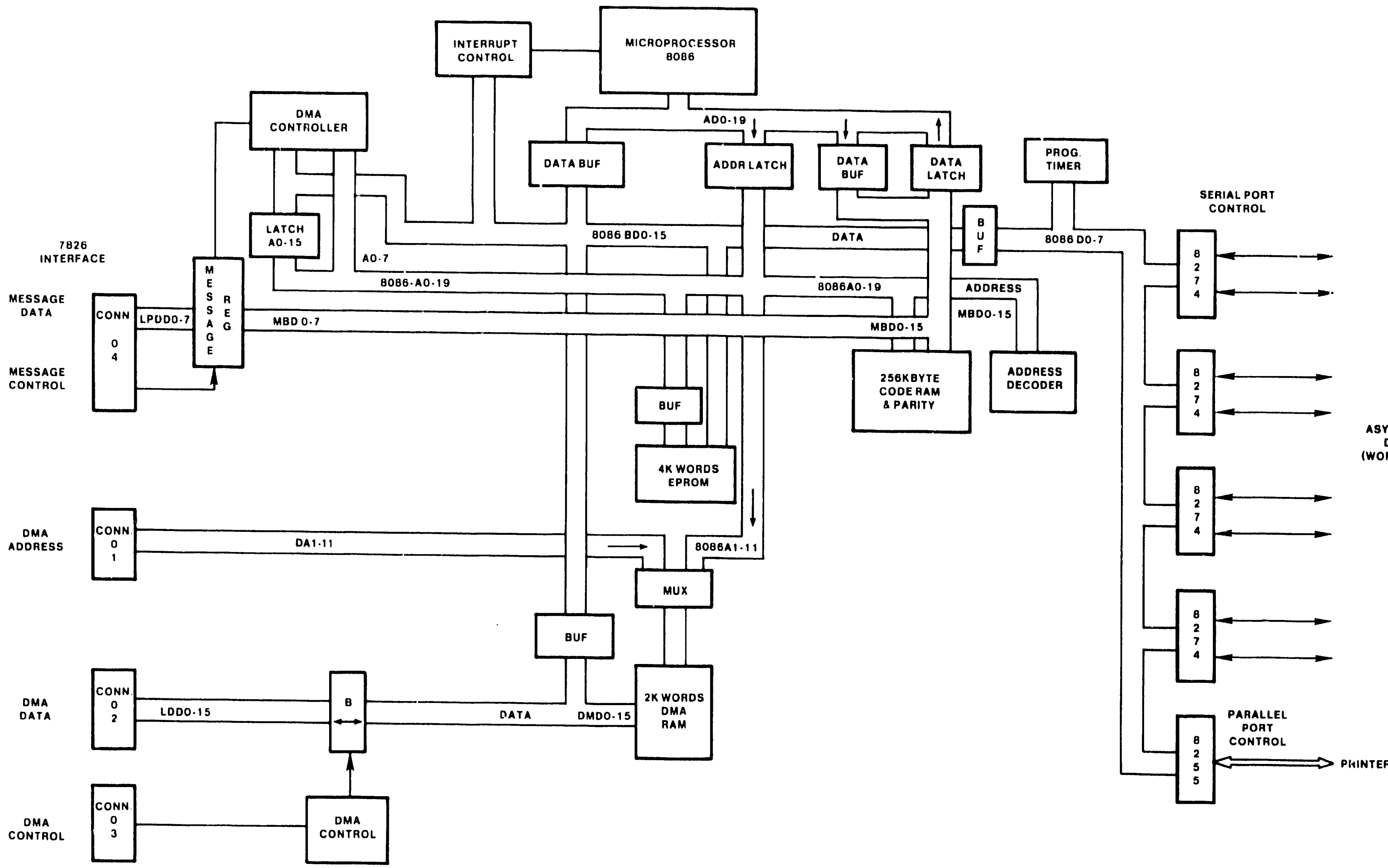


Figure C-2. ADC Functional Block Diagram passes messages to and from the IOP via this RAM under the control of the 8086. Arbitration between the 8086 and the DMA and refresh are hardware controlled and all non-contended accesses occur without wait states.

C.4.1.2 DMA Memory

DMA memory can be accessed directly by the 8086 or the host VS via the IOP's DMA circuitry. This memory allows the 8086 to initiate the transfer of data to or from the host VS while simultaneously handling the incoming data from terminals. Hardware arbitration allows the 8086 to access the DMA memory while a DMA is in progress. The DMA itself, even when initiated by the ADC, is controlled by the IOP mother board. All accesses to this RAM are word (16 bit) oriented.

C.4.1.3 PROM Memory

Two 2732A PROMs reside at addresses FE000 to FFFFF Hex. These PROMs are accessible only to the 8086 and are used for diagnostics and IPL.

C.4.2 ADC/IOP COMMUNICATION

There are two communication paths between the ADC and the IOP -- one for messages and one for data.

C.4.2.1 Message Transfer

IOP to ADC Messages:

- START I/O
- HALT I/O
- CONTROL I/O
- RESET
- GRANTED (TASK COMPLETED)
- INIT

ADC to IOP Messages:

- READ DATA
- WRITE DATA
- WRITE I/O STATUS
- QUIT

Message transfer is accomplished over an eight-bit bus between the ADC code RAM and the IOP. When the ADC wishes to send a message to the IOP, the 8086 sets up the message in code RAM and programs the DMA controller. The DMA controller will interrupt the 8086 only at the completion of a message transfer to the IOP. Because the DMA controller has only 16 address bits and paging is not supported, message transfer must use the lower 128K words of code RAM. Also, the RAM address will be twice the value in the address register of the DMA controller.

C.4.2.2 Data Transfer

Data transfers between the IOP and the ADC include microcode loads to the ADC as well as communication to and from the ADC I/O ports. The IOP initiates the microcode load, but thereafter all transfers are initiated by the ADC, using the Read Data and Write Data messages to pass the parameters of the transfer to the DMA hardware on the IOP. The IOP DMA hardware then takes control of the transfer of data between the ADC's DMA RAM and the system I/O bus. The 8086 may access the DMA RAM during such a transfer.

C.4.3 SERIAL I/O CHANNELS

Four 8274 multi-protocol communication chips support eight full duplex serial I/O channels which are routed to the RS-232-C interface for both short (up to 2000 feet) distance direct communication and longer distance connection via modems. The basic function of the 8274 is serial-to-parallel and parallel-to-serial conversion. The 8086 accomplishes single byte data transfers between the 8274s and memory via I/O. Each 8274 has an interrupt request line to a slave 8259 interrupt controller.

Power on or software reset enables the baud rate generators (BRG) to the transmit and receive clocks. An I/O command may be issued to switch the clock selection to external. In this mode, the transmit and receive clocks are enabled to the RS-232-C connectors.

C.4.4 BAUD RATE GENERATOR

There are four Motorola K1135C Dual Baud Rate Generators (BRGs) on the 8168 Board. Each BRG simultaneously generates two output frequencies for the 8274s. Each frequency is selectable in baud rates from 50 to 19200.

C.4.5 PROGRAMMABLE TIMER

An Intel 8253 Programmable Timer has three independent 16-bit counters. The 8086 sends out control words to initialize the counters with the desired mode. A 1.228 MHz signal is applied to the clock input of counter 0 and the output of this counter is tied to the master 8259 interrupt controller. Counter 0 is used for software timer applications. Counters 1 and 2 are not used.

C.4.6 INTERRUPTS

The 8168 board contains two 8259A Programmable Interrupt Controllers. The slave interrupt controller has as inputs the four interrupts from the 8274 communication chips. These interrupts are given highest priority by directing the slave output into the master request level 1 and not using request level 0. The interrupts to the 8086 are listed below in order of decreasing priority.

Table K-1. ADC Interrupts

INTERRUPT NAME	DESCRIPTION
Master IR0	Not used
Master IR1	Slave interrupts (8274s)
Master IR2	Parallel I/O port interrupt for printer
Master IR3	Interrupt from the 8253 timer
Master IR4	Message In interrupt
Master IR5	Message Out interrupt
Master IR6	Code RAM parity error
Master IR7	Not used
Slave IR0	8274-1
Slave IR1	8274-2
Slave IR2	8274-3
Slave IR3	8274-4

C.4.7 DIAGNOSTIC STATUS LAMP

The 8168 Controller board contains a LED (located at the top edge of the board between connectors J2 and J3) that is used to indicate the status of the power-up built-in test (BIT). A flip-flop (diagnostic status register) turns the LED on at power up. When the BIT is successfully completed, the flip-flop is reset and the LED is turned off.

C.4.8 WAIT STATE GENERATORS

There are two wait state generators associated with 8086 accesses. One generates two wait states for the EPROMS and all I/O devices, and the other provides six wait states for the parallel port data.

C.5 INSTALLATION

The following paragraphs describe the unpacking, inspection, and installation instructions for the VS-85/85-H Async Device Controller. Refer to Chapter 4 of the VS-85/85-H Computer System Product Maintenance Manual for more details.

C.5.1 UNPACKING

Before unpacking the VS-85/85-H Async Device Controller, check all packing slips to ensure that the proper equipment has been delivered. Inspect all shipping containers for damage (crushed corners, punctures, etc.). Open the boxes and remove the Async Controller boards.

C.5.2 INSPECTION

Inspect the boards for packing material and such shipping damage as broken connectors. If damage is discovered, follow the reporting procedure in paragraph 4.4 of the VS-85/85-H Product Maintenance Manual.

C.5.3 MINIMUM REQUIREMENTS

C.5.3.1 Hardware

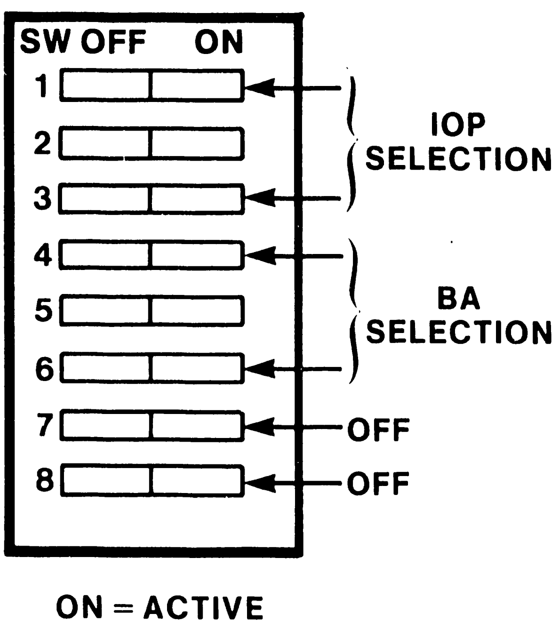
Hardware minimum requirements are listed in paragraph 4.6 of the Product Maintenence Manual.

C.5.3.2 Software

The VS-85/85-H Async Device Controller requires a minimum of OS Release 6.4X.XX.

C.5.4 ASYNC CONTROLLER INSTALLATION

1. Power down the system.
2. Remove the top cover.
3. Ensure that the switch settings, on the 210-7826 TCP/IOP motherboard to be inserted, are correct (see figures C-3 and C-4).



SW NO	1	2	3	IOP NO
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5

SW NO	4	5	6	BA NO.
	0	0	1	1

ON = 1
OFF = 0

B-0180-FY85-2

Figure C-3. TCP/IOP Board Switch Settings

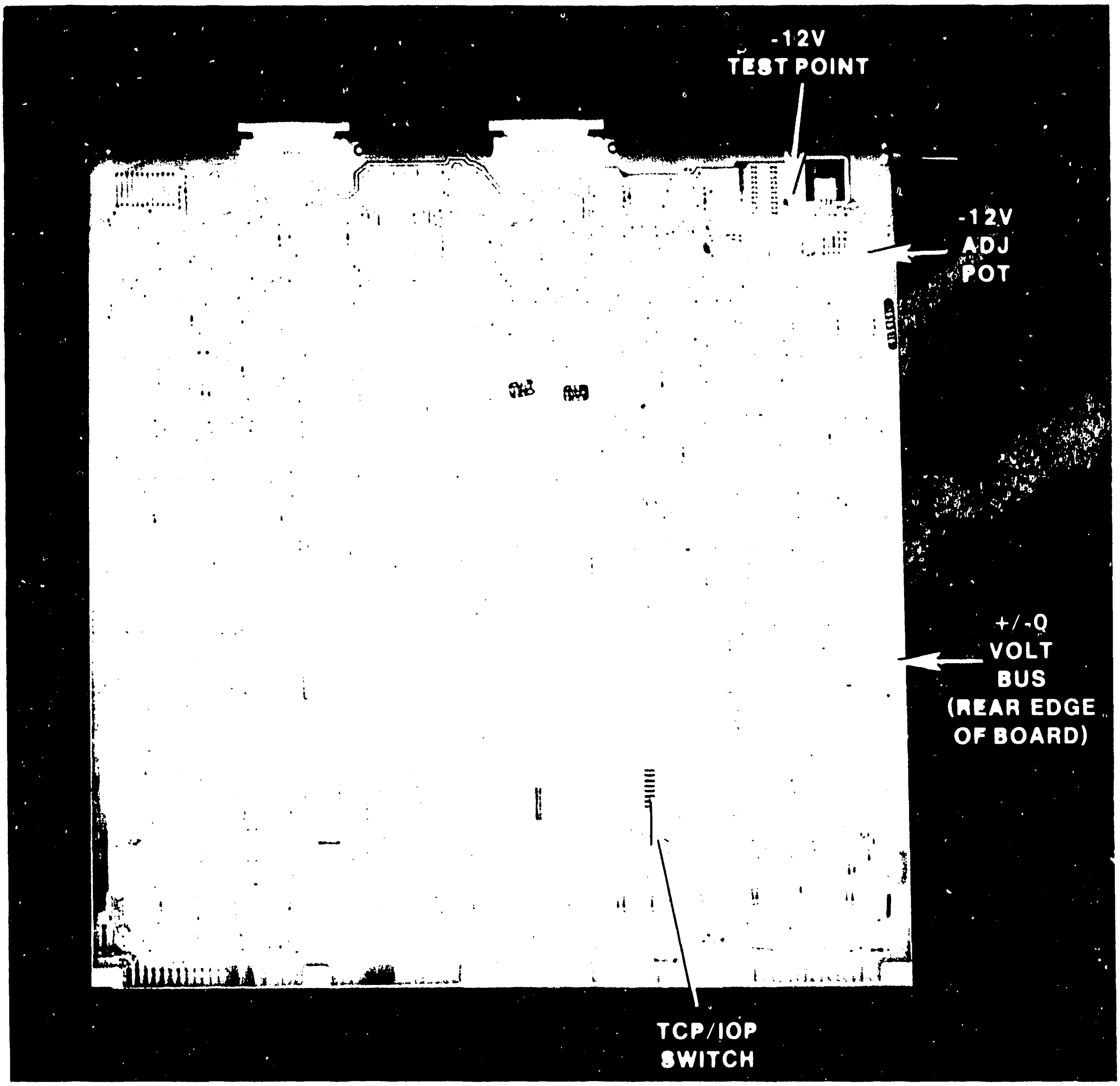


Figure C-4. 210-7826 TCP/IOP Motherboard

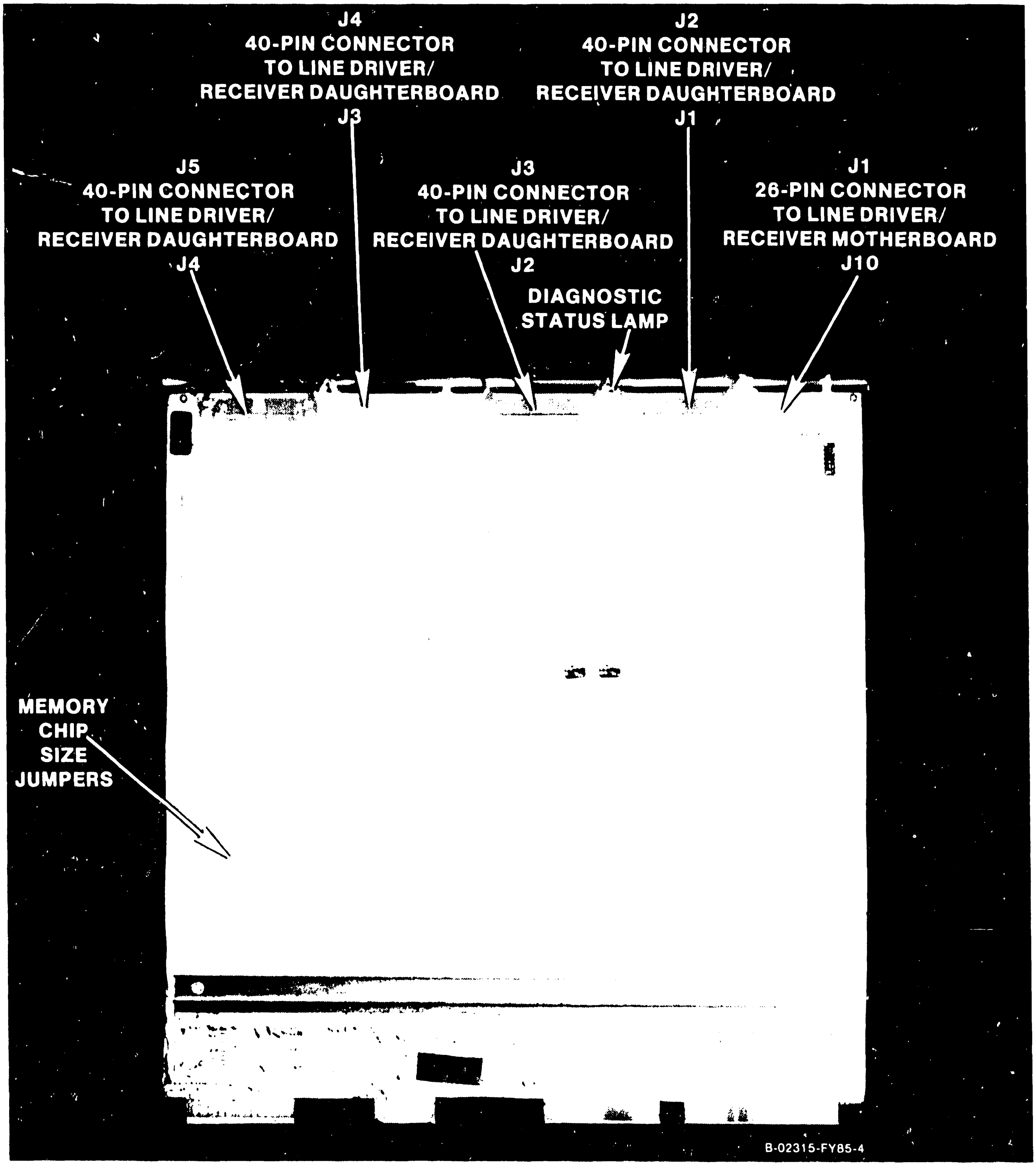


Figure C-5. 210-8168 Controller Board

4. Ensure that the memory chip size jumpers on the controller board (figure C-5 above) are in the position shown below in figure C-6. These jumpers determine the type of memory chip used. Presently only 64K RAM chips are supported.

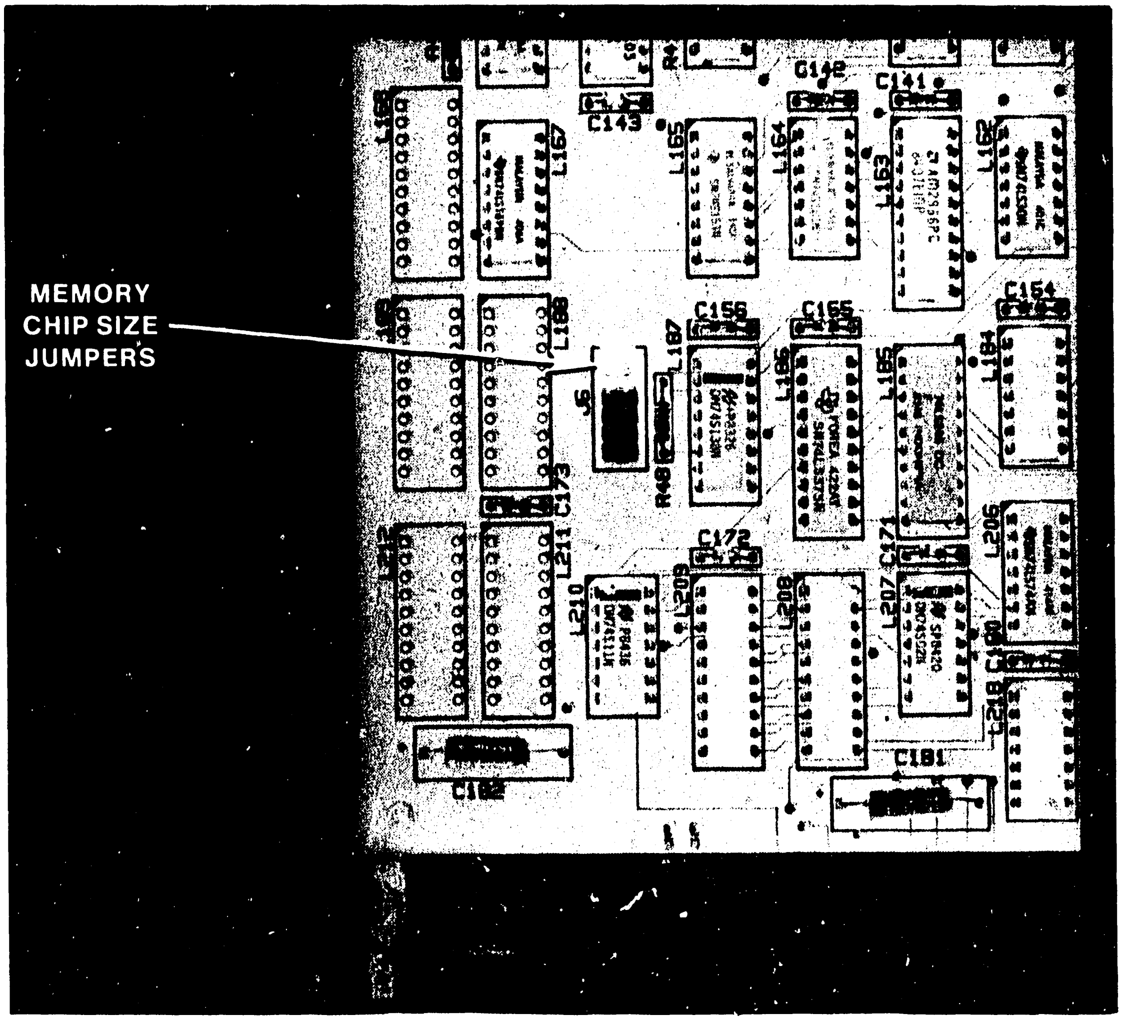


Figure C-6. 210-8168 Memory Chip Size Jumpers

5. Insert the TCP/IOP Motherboard/Controller Board assembly into an available TCP/IOP slot in the motherboard. Ensure that the connectors are mated before pushing down on board.
6. Install the Rear Panel Assembly, consisting of the 8324 Line Driver/Receiver Daughterboard (figure C-7) and the 8323 Line Driver/Receiver Motherboard (figure C-8), in the blank connector plate location (shown in figure C-9) in the rear of the mainframe using the hardware provided.

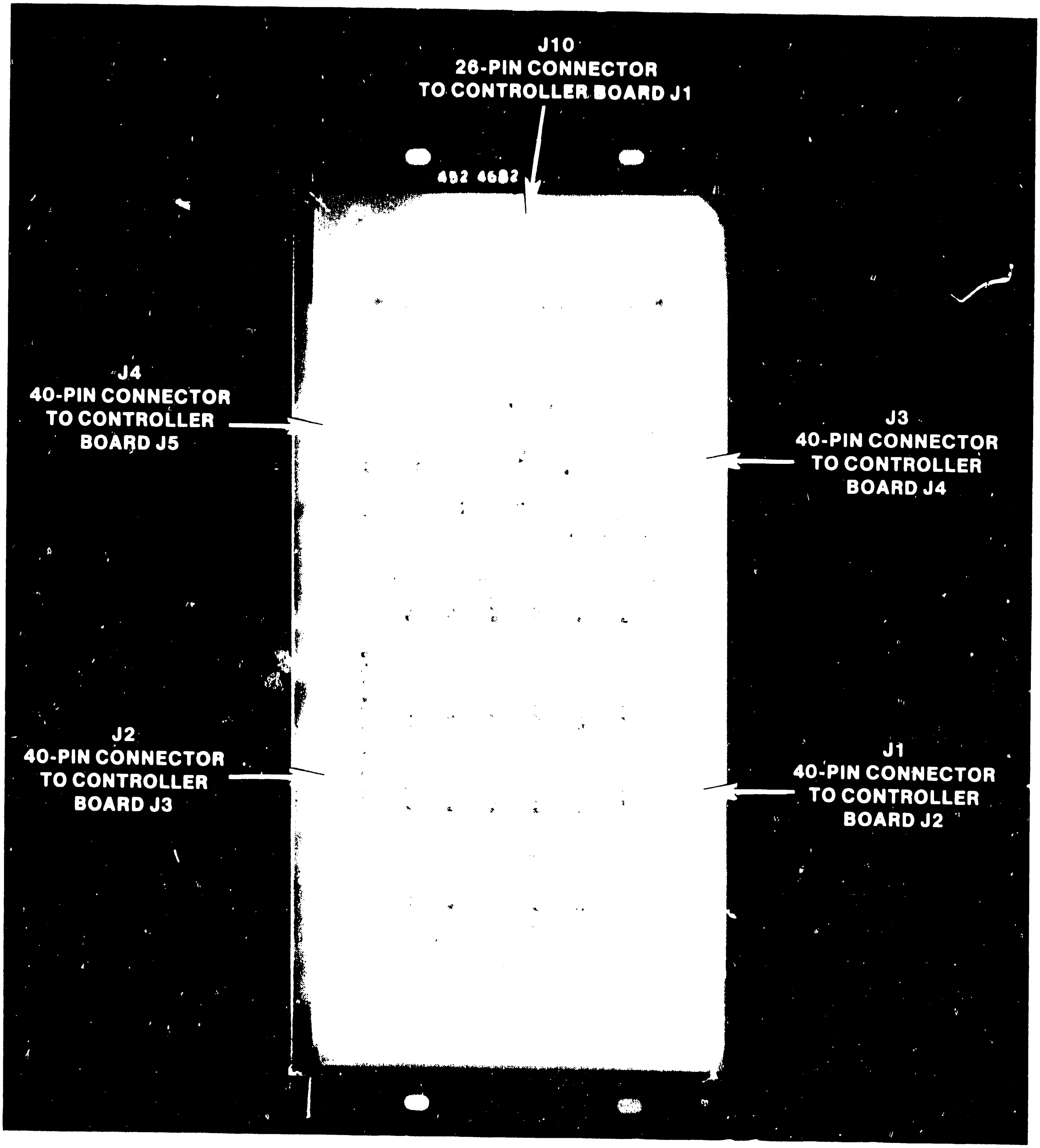


Figure C-7. Async Rear Panel Assembly (210-8324 Daughterboard Side)

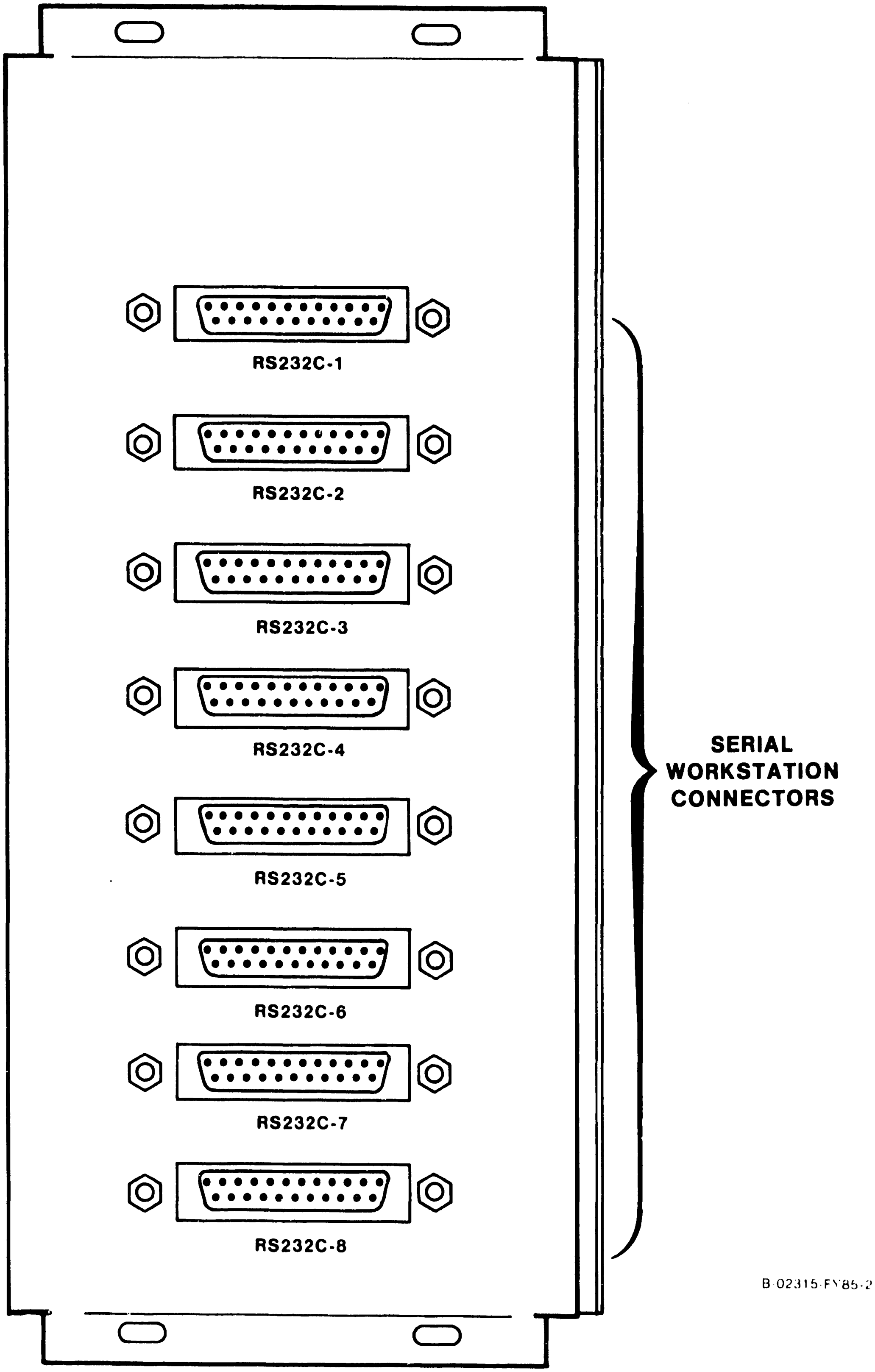


Figure C-8. Async Rear Panel Assembly (Connector Side)

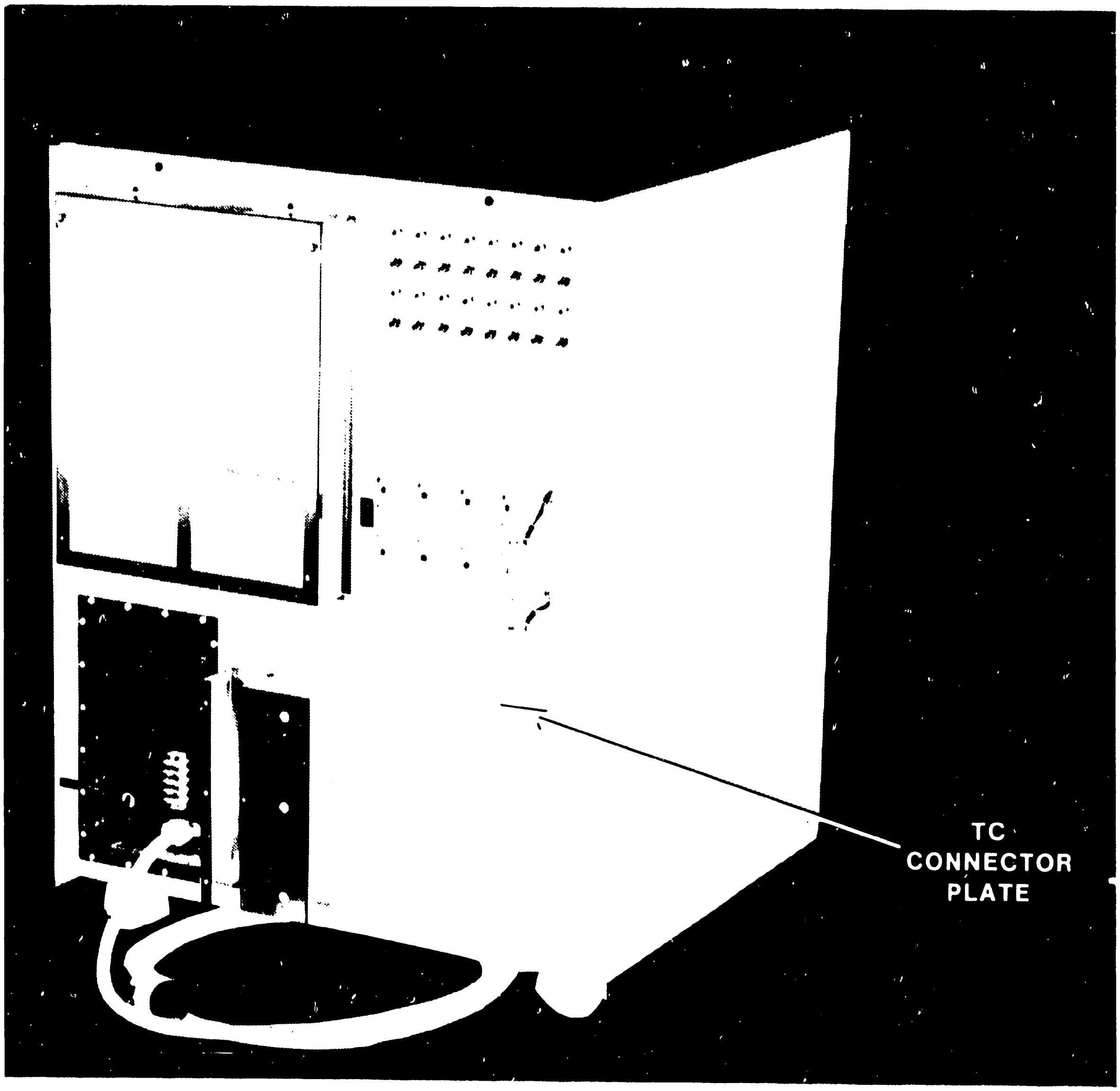
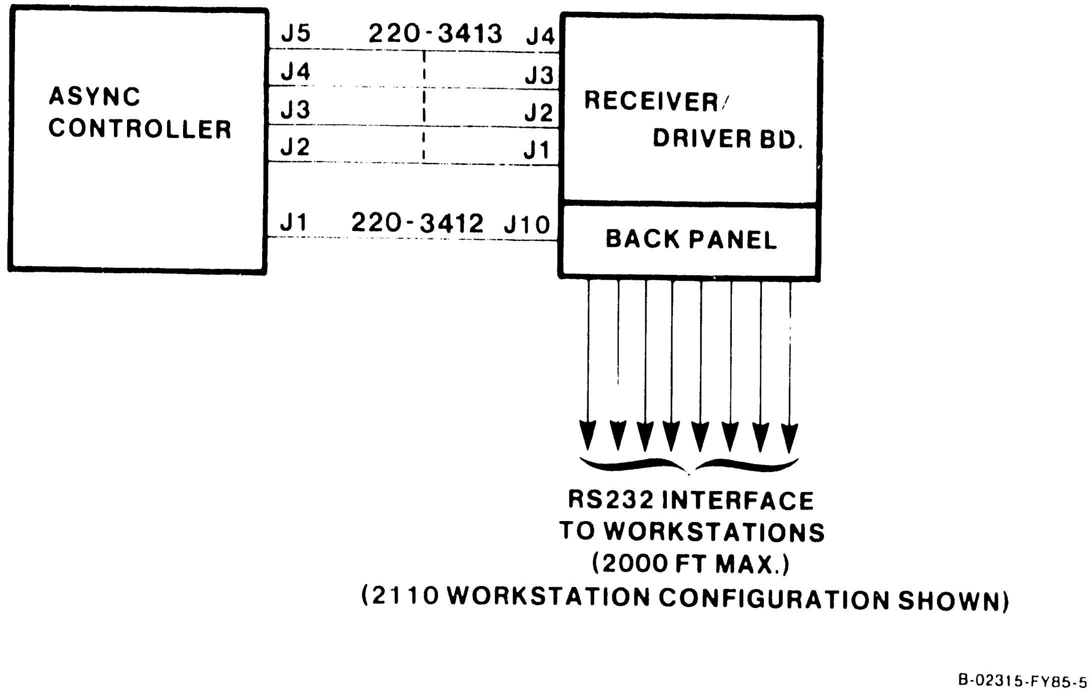


Figure C-9. Blank Connector Plate for Rear Panel Installation

7. Connect the cables as shown in figure C-10.



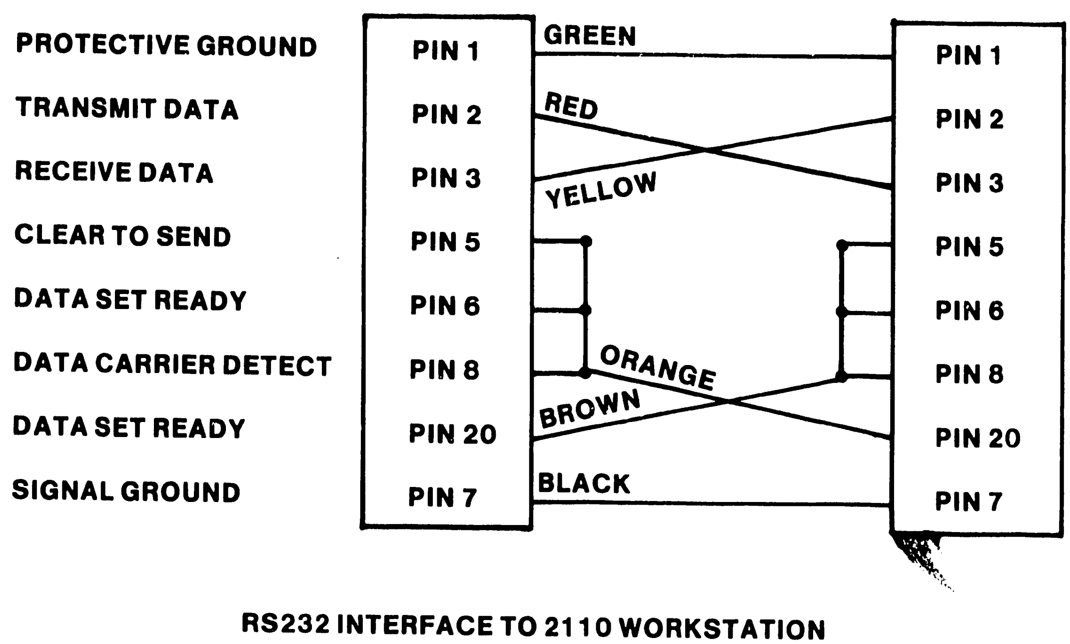


Figure C-10. Cable Connections

8. Connect all workstations.
9. Power on the mainframe and check the -12 Volt supply on the 7826 TC Motherboard as follows:
   a. Connect the negative lead of a digital voltmeter to the -12 Volt test point and the positive to the $\pm$0 Volt bus. (See figure C-4.)
   b. Adjust trimpot (figure C-4) until the meter reads -12 V $\pm$0.5 V.

C.5.5 SYSTEM CHECKOUT

1. Power up the system.
2. Load microcode and IPL the system.
3. Power on all peripherals.
4. Ensure that all workstations configured through the Async Controller display the logon screen.
5. Ensure that logon is possible from each workstation.
6. Turn the system over to the customer.

C.6 PREVENTIVE MAINTENANCE

There is no preventive maintenance for the VS-85/85-H Async Device Controller.

C.7 CORRECTIVE MAINTENANCE

Corrective maintenance for the VS-85/85-H ADC consists of removal and replacement of defective parts.

C.7.1 ASYNC CONTROLLER BOARD ASSEMBLY REMOVAL AND REPLACEMENT

1. Power down the mainframe.
2. Remove the top cover.
3. Remove the cables from the top of the controller board.
4. Lift the TCP/IOP/Controller Board assembly straight up and out of the card cage.
5. To replace the Controller Board Assembly, reverse the removal procedure.
6. Power on the mainframe and check the -12 Volt supply on the 7826 TC Motherboard as follows:
   a. Connect the negative lead of a digital voltmeter to the -12 Volt test point and the positive to the $\pm$0 Volt bus. (See figure C-4.)
   b. Adjust trimpot (figure C-4) until the meter reads -12 V $\pm$0.5 V.

NOTE

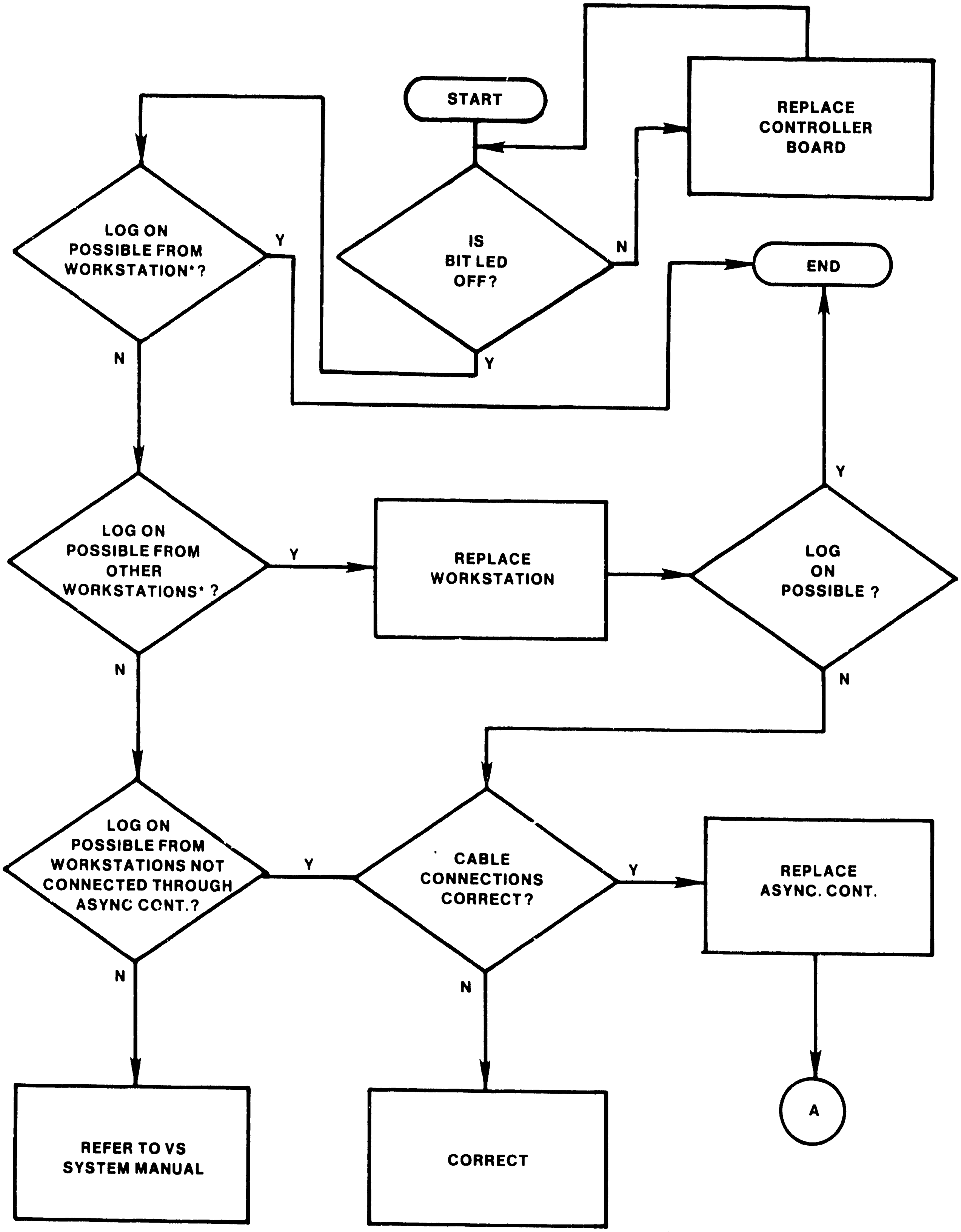
The system power supply must be adjusted to -13.6 V to obtain the necessary -12 V on the TC board.

C.7.2 REAR PANEL ASSEMBLY REMOVAL AND REPLACEMENT

1. Power down the mainframe.
2. Remove the top cover.
3. Remove the cables from the Line Driver/Receiver Daughterboard and Motherboard of the rear panel.
4. Remove and save the hardware securing the Rear Panel to the mainframe.
5. To replace the Async Rear Panel Assembly, reverse the removal procedure.

C.8 TROUBLESHOOTING THE ADC

This paragraph describes, in flow chart form, procedures for fault isolation in the VS-85/85-H Async Device Controller. Refer to the flow chart in figure C-11.



* DENOTES DEVICE CONFIGURED THROUGH THE ASYNC CONTROLLER

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Figure C-11. ADC Troubleshooting Flow Chart (Sheet 1 of 2)

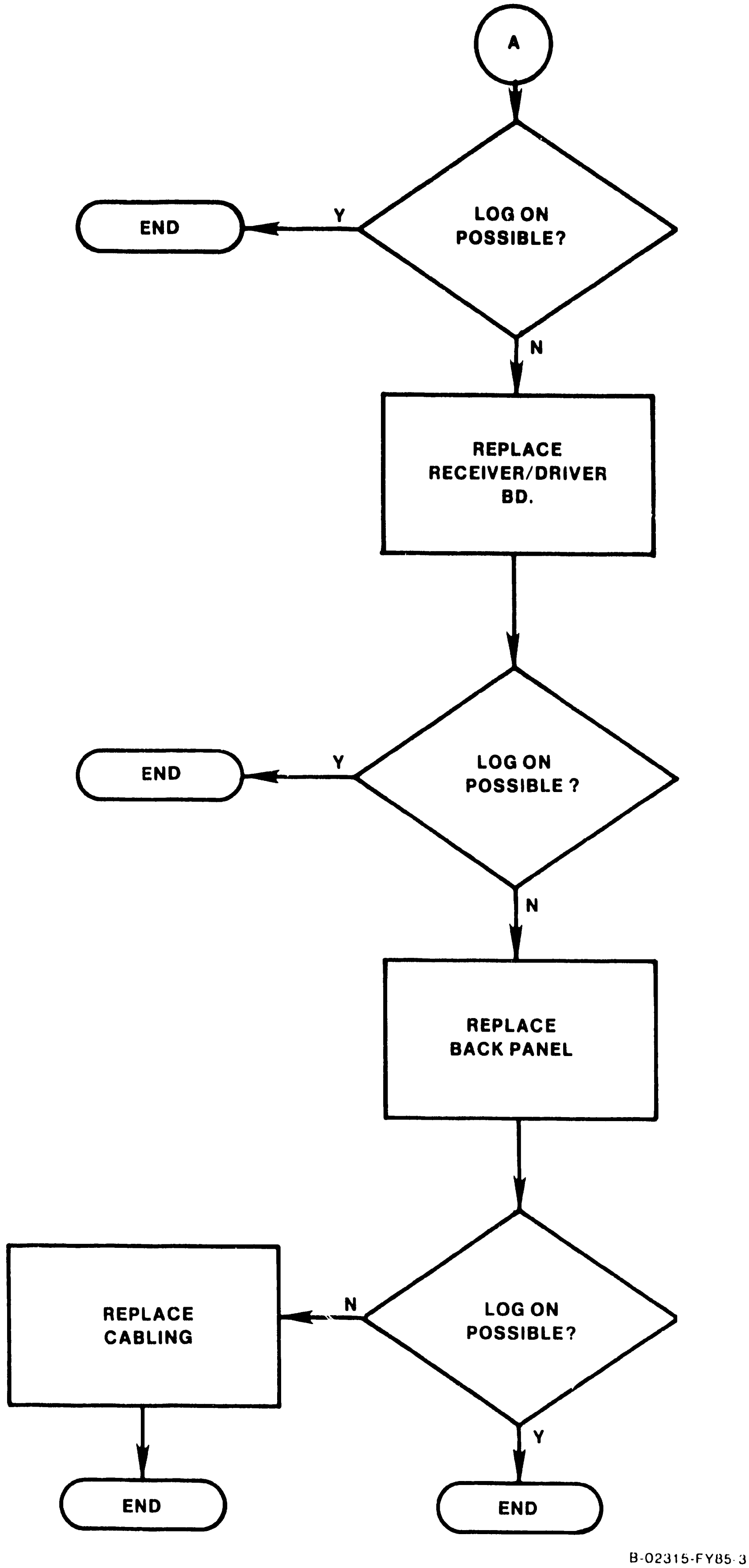

Figure C-11. ADC Troubleshooting Flow Chart (Sheet 2 of 2)

C.9 FIELD REPLACEABLE UNITS

The following table lists the field replaceable units (FRUs) for the VS-85/85-H Async Device Controller.

Table C-2. VS-85/85-H ADC Field Replaceable Units

WLI P/N	DESCRIPTION	FRU
220-0521	25-ft 2110 Workstation Cable	CBL
120-2381-01	50-ft 2110 Workstation Cable	CBL
120-2381-02	100-ft 2110 Workstation Cable	CBL
120-2381-03	500-ft 2110 Workstation Cable	CBL
120-2381-04	1000-ft 2110 Workstation Cable	CBL
120-2381-05	2000-ft 2110 Workstation Cable	CBL
210-8324	Driver/Receiver Daughterboard	PCB
212-3104	Async Controller	ASSY
220-0113	12-ft RS-232-C TC Cable	CBL
220-0219	25-ft RS-232-C TC Cable	CBL
220-0220	50-ft RS-232-C TC Cable	CBL
220-3412	26-pin Ribbon Cable	CBL
220-3413	40-pin Ribbon Cable	CBL
272-0043	Async Rear Panel Assembly	ASSY

WANG LABORATORIES, INC

ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

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