6105

VS-300 Computer System

Customer Engineering
Product Maintenance Manual

741-1634

COMPANY CONFIDENTIAL

CUSTOMER ENGINEERING

PUBLICATION UPDATE BULLETIN

TITLE: VS-300 Computer System

DATE: 03/21/86

This PUB affects: 741-1634
742-1634

CLASS CODE: 6105

Previous Notice(s): None

REASON FOR CHANGE:

This PUB updates VS-300 IPL procedures and SCU software installation; adds Peripheral Band installation, a second dc distribution board, and diagnostics (including service log); updates the Illustrated Parts Breakdown; and makes general corrections.

INSTRUCTIONS:

Remove and insert attached pages and/or microfiche as follows:

	REMOVE PAGES	INSERT PAGES
1.	v thru xv	v thru xvi
2.	3-1 thru 3-10	3-1 thru 3-10
3.	3-19/20	3-19/20
4.	3-25 thru 3-31	3-25 thru 3-32
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6.	4-21 thru 4-34	4-21 thru 4-34
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8.	5-7/8	5-7/8
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15.	None	5-50a/b/c
16.	5-55/56	5-55/56
17.	None	5-56a

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19.	6-1 thru 6-5	6-1 thru 6-5
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21.	None	6/15
22.	7-1 thru 7-12	7-1 thru 7-12
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24.	7-57	7-57 thru 7-61

	REMOVE FICHE	INSERT FICHE
1.	1 thru 4	1 thru 4
2.		
3.		
4.		

These pages constitute a permanent record of revisions; place them directly following title page.

PREFACE

This document is the Product Maintenance Manual (PMM) for the Wang VS-300 Computer System. The manual is organized in accordance with Customer Engineering Technical Documentation's approved PMM outline. The scope of this manual reflects the type of maintenance philosophy selected for this product.

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with sufficient instructions to operate, troubleshoot, and repair the VS-300 Computer System. The manual will be updated on a regular schedule or as necessary. Such updates will be published either as Publication Update Bulletins (PUBs) or as full revisions.

First Edition (September, 1985)

WARNING

```
*****************************************************************
*                                                               *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY           *
*    CIRCUMSTANCE.  EXTREMELY DANGEROUS VOLTAGE AND             *
*    CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-          *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.      *
*                                                               *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER               *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                      *
*                                                               *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC      *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,          *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO       *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO          *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                       *
*                                                               *
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WARNING

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*****************************************************************
*                                                               *
*  THIS COMPUTER EQUIPMENT HAS BEEN VERIFIED AS FCC CLASS A.    *
*                                                               *
*****************************************************************
```

IN ORDER TO MAINTAIN COMPLIANCE WITH FCC CLASS A VERIFICATION, THE FOLLOWING CONDITIONS MUST BE ADHERED TO DURING NORMAL OPERATION OF EQUIPMENT.

- ALL COVERS MUST BE ON SYSTEM AND SECURED IN THE PROPER MANNER.
- ALL INTERNAL CABLES MUST BE ROUTED IN THE ORIGINAL MANNER WITHIN THE CABLE CLAMPS PROVIDED FOR THAT PURPOSE.
- ALL EXTERNAL CABLING MUST BE SECURED AND THE PROPER CABLE USED TO ENSURE THAT CABLE SHIELDING IS PROPERLY GROUNDED TO THE CABLE CLAMPS PROVIDED.
- ALL HARDWARE MUST BE PROPERLY SECURED.

The last page before the back cover is a comment sheet.
Please take the time to fill out the comment sheet and return it, via the Home Office mail pouch, addressed to:

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Customer Engineering Technical Documentation
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Lawrence, Mass.
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CHAPTER 1

INTRODUCTION

Chapter 1 information is not provided as part of this Product Maintenance Manual, but will appear in the Illustrated Maintenance Manual.

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CHAPTER 2

THEORY OF OPERATION

Chapter 2 information is not provided as part of this Product Maintenance Manual, but will appear in the Illustrated Maintenance Manual.

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CHAPTER 3

OPERATION

3.1 GENERAL

This chapter provides tables listing all VS-300 mainframe controls and indicators, power control and battery backup description, main memory size selection, power-on, IPL, and power-off procedures.

3.2 CONTROLS

Table 3-1 lists the controls found on the VS-300 followed by a brief description of their purpose. Locations of the controls are shown in figures 3-1 through 3-15.

Table 3-1. VS-300 Controls

Control Name And Type	Location	Purpose	Normal Position
Ac On/Off (Circuit breaker)	Power Distribution Assembly	Provides ac power to power supplies, Power Supply Controller board, and mainframe fans.	On
Power On (Lighted pushbutton)	Control Panel	Turns dc power on.	Open (not active)
Power Off (Lighted pushbutton)	Control Panel	Turns dc power off.	Open (not active)
System Reset (Pushbutton)	Control Panel	Resets system, clears main memory, enters control mode.	Open (not active)
Operator Console Reset (Pushbutton)	Control Panel	Resets SCU (PC) only.	Open (not active)
1. Remote Service 2. Remote Admin. 3. Normal Control	Control Panel	Remote diagnostics. RSAF operation. All Cntrl Panel controls function when power on.	Normal Control
4. Control Lock (Key switch)		Disables power on.	

Table 3-1. VS-300 Controls (Cont'd)

Control Name And Type	Location	Purpose	Normal Position
V1 (+5A), V2 (+12) V3 (-5) V4 (-12) 5V (+5B) (Adjustment pots)	Multioutput SPS " " " SPS Booster SPS	Adjusts power supply voltages up or down as needed.	Various (Chapters 4 and 5)
SW1 (Power On) (Pushbutton)	Power Supply Controller	Turns dc power on. Parallel to Control Panel On pushbutton.	Open (not active)
SW2 (Power Off) (Pushbutton)	Power Supply Controller	Turns dc power off. Parallel to Control Panel Off pushbutton.	Open (not active)
SW3 - Voltage Address (DIP switch)	Power Supply Controller	Addresses hex displays that are used to zero A/D converter.	Various
SW4 - Battery Backup Time (DIP switch)	Power Supply Controller	Set length of time backup batteries supply power to power supplies after ac input line failure.	100 seconds (Rev. 0) 96 seconds (Rev.1) (Currently)
R11, R12 (Adjustment pots) (Rev. 0 only)	Power Supply Controller	Calibrates Power Supply Controller.	Various
R18 through R22 (Five adjustment pots)	Power Supply Controller	Calibrate A/D (Analog/ Digital) converter for individual dc voltages.	Various (Chapters 4 and 5)
R70A (adjustment pot)	Power Supply Controller	Low Battery Voltage Dropout adjustment.	Various (Chapter 5)
R23 (adjustment pot)	Battery Backup Charging P/S	Sets proper battery charging voltage.	Various (Chapter 5)
Local/Remote (Toggle switch)	SCU (PC) Local Comm Data Link board	Selects PC IPL operation (Local) or workstation operation (Remote)	Local
Main Memory Size (Jumpers)	MCU board	Selects maximum main memory size.	Various (Chapter 5)
Main Memory DRAM loading (Jumpers)	Main Memory board	Selects half or fully loaded MM boards.	Various (Chapter 5)
IOC Diagnostic Switch (DIP switch)	All IOCs	Permits IOC diagnostic functions.	All Off (open) (Chapter 5)

Table 3-1. VS-300 Controls (Cont'd)

Control Name And Type	Location	Purpose	Normal Position
Disk Drive Device Type (DIP switch)	Disk Drive IOC	Selects disk drive types connected to system.	Various (Chapter 5)
Port Select (DIP switch)	Multiline TC (MLTC) IOC	Selects TC ports on MLTC for loopback test.	All Closed (On)
Gate Array Clear (Pushbutton)	Gate Array TC Connector Assembly	ReIPL CPU/Gate Array (210-8714 board)	Open (not active)
Gate Array Switch (DIP switch)	CPU/Gate Array (210-8714) board	Memory configuration and loopback test selection.	5,6 closed, rest open
CIU IOC Functions (DIP switch)	BLANC IOC	Selects configuration, diagnostics, and repair functions.	All Open (Off) (Chapter 5)
5-Channel CIU 10MBPS Modem Reset (Pushbutton)	5-Channel CIU 10MBPS Duo-binary Modem	Clears transmit fault.	Open (not active)

3.3 INDICATORS

Tables 3-2 through 3-9 lists the indicators found on the VS-300 followed by a brief description of their purpose. Locations of the indicators are shown in figures 3-1 through 3-15. There are no indicators on any of the circuit boards comprising the VS-300 mainframe PCB chassis. Any errors are displayed on the SCU screen.

Table 3-2. VS-300 Indicators

Indicator Name And Type	Location	Purpose	Normal Indication
Power On lamp (Power On pushbutton)	Control Panel	Shows dc power is on.	On
Power Off lamp (Power Off pushbutton)	Control Panel	Shows dc power is off.	Off
LED1 - LED5 (Five voltage sensing LEDs)	Power Supply Controller	Shows dc voltages are on. Does not show accuracy.	On

Table 3-2. VS-300 Indicators (Cont'd)

Indicator Name And Type	Location	Purpose	Normal Indication
L3, L4 (Two Hex displays)	Power Supply Controller	Used to zero A/D converters.	Hex 7E (Minus) Hex 80 (Zero) Hex 82 (Plus)
LED1	Battery Backup Board	Indicates +240 V dc battery voltage is on line.	On
Diskette Activity LED	Front of SCU minidiskette drive	Shows drive in use (head loaded)/ not in use.	On (in use) Off (not in use)
TC Displays (Up to 4 LED displays)	MLTC Connector Assembly	Shows interchange signals between modem and controller.	Refer to Tables 3-3 thru 3-6.
TC Display (One display with 8 LEDs)	Gate Array TC Back Panel	Shows interchange signals between modem and controller.	Refer to Tables 3-7 thru 3-9.
5-Channel CIU 10MBPS Modem Display (4 LEDs)	5-Channel CIU 10MBPS Duobinary Modem	1. Channel Select. 2. Fault.	3 LEDs - Various 1 LED - Off

NOTES

1. Tables 3-3 to 3-5 show EIA (Electronic Industries Association) interchange signals between the modem and the MLTC controller.
2. For the MLTC, all LEDs are normally on or blinking during the BIT (Built In Test). If the BIT fails, the software controlled LED will go off.

Table 3-3. Multiline TC Back Panel Displays (RS232 Operation)

Indicator Name And Type	Purpose
LED1	Data Set Ready
LED2	Data Terminal Ready
LED3	Carrier Detect
LED4	Software Controlled
LED5	Transmitted Data
LED6	Request-to-Send
LED7	Clear-to-Send
LED8	Received Data

Table 3-4. Multiline TC Back Panel Displays (RS366 Operation)

Indicator Name And Type	Purpose
LED1	Data Line Occupied
LED2	Call Origination Status
LED3	Present Next Digit
LED4	Abandon Call and Retry
LED5	Digit Present
LED6	Call Request Present
LED7	Software Controlled

Table 3-5. Multiline TC Back Panel Displays (X.21 Operation)

Indicator Name And Type	Purpose
LED1	Transmitted data
LED2	Data Terminal Ready
LED3	Received Data
LED4	Indication
LED5	Software Controlled

Table 3-6. Multiline TC Back Panel Displays (RS449 Operation)

Indicator Name And Type	Purpose
LED1	Carrier Detect
LED2	Clear-to-Send

NOTE

Tables 3-7 to 3-9 show EIA (Electronic Industries Association) interchange signals between the modem and the Gate Array controller. Read the Gate Array LEDs from left to right.

Table 3-7. Gate Array Back Panel Displays (3270 Operation)

Indicator Name And Type	Purpose
LED1	Received Data
LED2	Transmitted Data
LED3	Clear-to-Send
LED4	Request-to-Send
LED5	Data Carrier Detect
LED6	Data Terminal Detected
LED7	Data Set Ready
LED8	Power Indicator

Table 3-8. Gate Array Back Panel Displays
(Remote WangNet [WSN] Point to Point and Multipoint Operation)

Indicator Name And Type	Purpose
LED1	System Activity
LED2	Received Valid Data
LED3	Transmitter Active
LED4	Data Carrier Detected
LED5	Virtual Circuit Active
LED6	Activity to VS
LED7	TC Controller Refusing New Traffic
LED8	Diagnostic Mode

Table 3-9. Gate Array Back Panel Displays (Teletex Operation)

Indicator Name And Type	Purpose
LED1	Document Received
LED2	Receive Memory Full
LED5	Transmitting Document
LED6	Receiving Document
LED7 (Note 1)	O.S. Code Active
LED8 (Note 2)	Normal Operation

NOTES

1. Blinks at a 3-second rate when Operating System code is active.
2. On for normal operation. Blinks for a hardware problem or fatal software error.

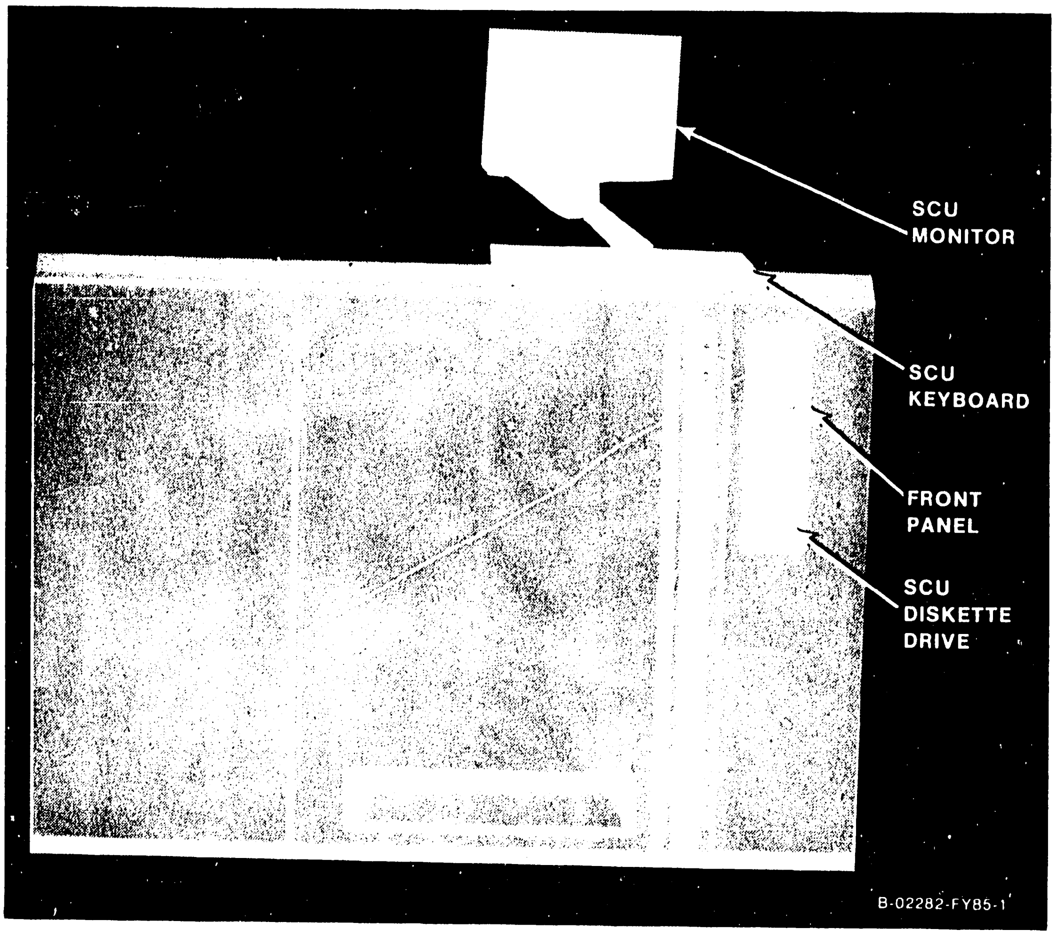


Figure 3-1. Front View of Mainframe

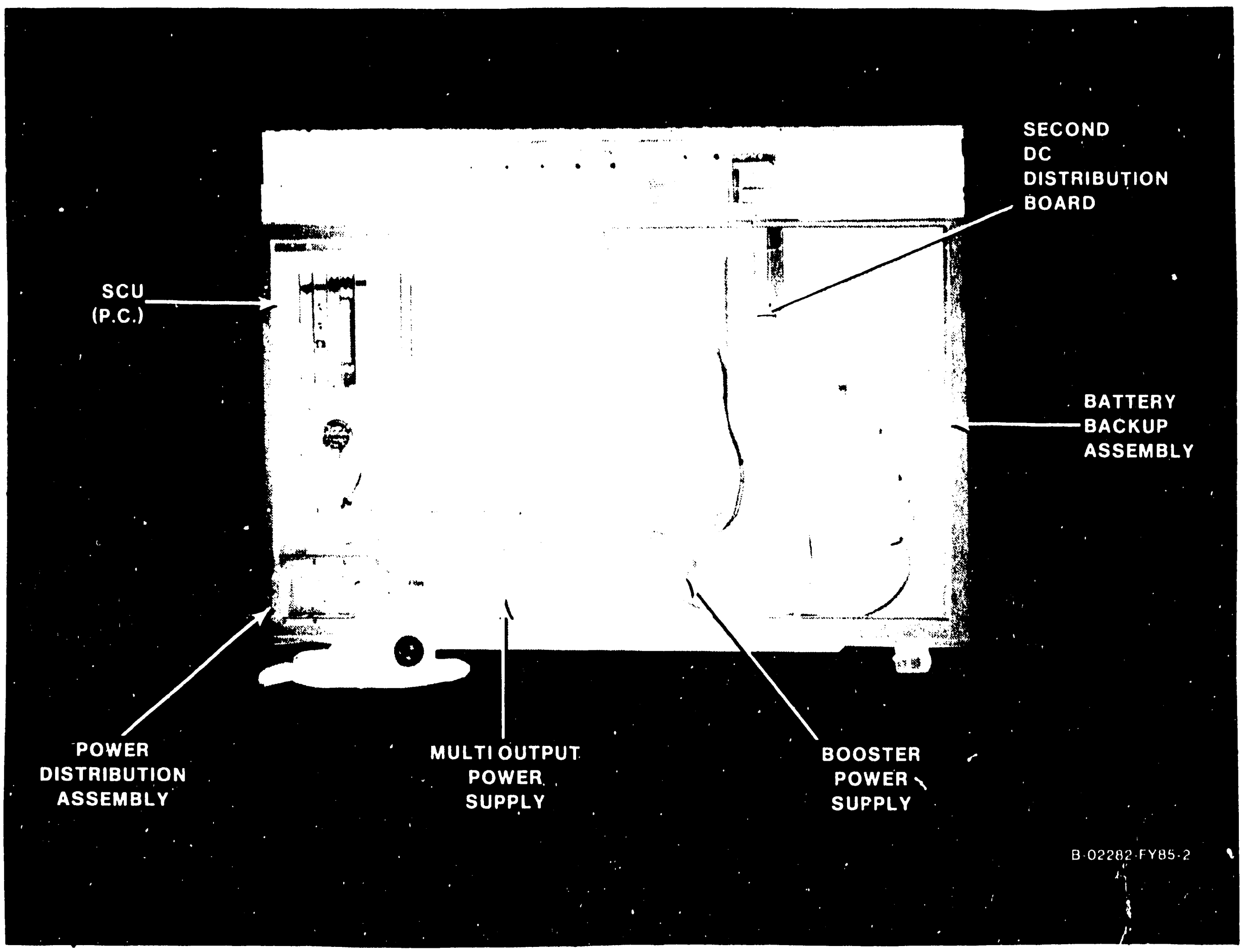


Figure 3-2. Rear View of Mainframe

3.4 POWER DISTRIBUTION ASSEMBLY AND CONTROLS

Ac input power to the VS-300 is 208-240 volts ac, split (single) phase. Ac neutral is not used in domestic mainframes. (Refer to Chapter 4.) The ac is supplied to the mainframe through the Power Distribution assembly, figure 3-3. The assembly is mounted on the lower right rear of the mainframe and contains a 30 amp mainframe ac On/Off circuit breaker, the ac line filter, and the ac and dc voltage distribution terminal boards.

To handle the increased dc voltage load requirements of the Active Port Assemblies and other back panel assemblies, a second DC Distribution board has been added to the system. The board is mounted on the left rear side of the card cage assembly, to the upper right of the Power Supply Controller board. (Figure 3-2.)

Moving the ac On/Off circuit breaker up turns on 16 card cage fans and two back panel fans and supplies ac to the Power Supply Controller board and to the dc switching power supplies. However, the power supplies are not activated.

Ac power is removed from the mainframe by moving the ac On/Off circuit breaker down.

3.5 POWER SUPPLIES AND CONTROLS

The VS-300 contains two switching power supplies, figures 3-4 and 3-5. The primary supply is a multioutput 1600 watt supply generating +5 V (+5A) at 200 amps, -5 V at 10 amps, +12 V at 20 amps, and -12 V at 10 amps. The secondary supply is a 1500 watt booster supply and the output is +5 V (+5B). The booster supplies the added power needed to share the heavy load that would have been placed on the +5 volt section of the multioutput supply. Each voltage is adjusted and regulated at the individual power supply (Figures 3-6 and 3-7.)

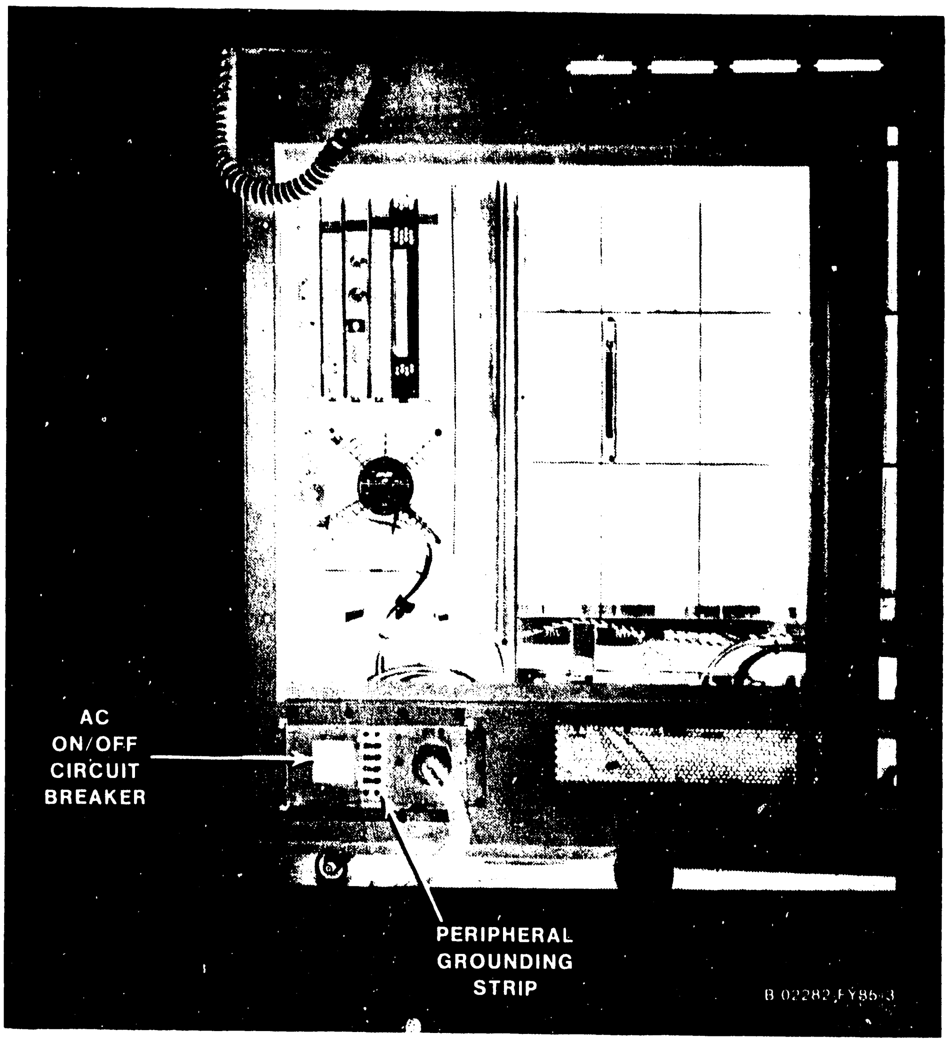


Figure 3-3. Power Distribution Assembly

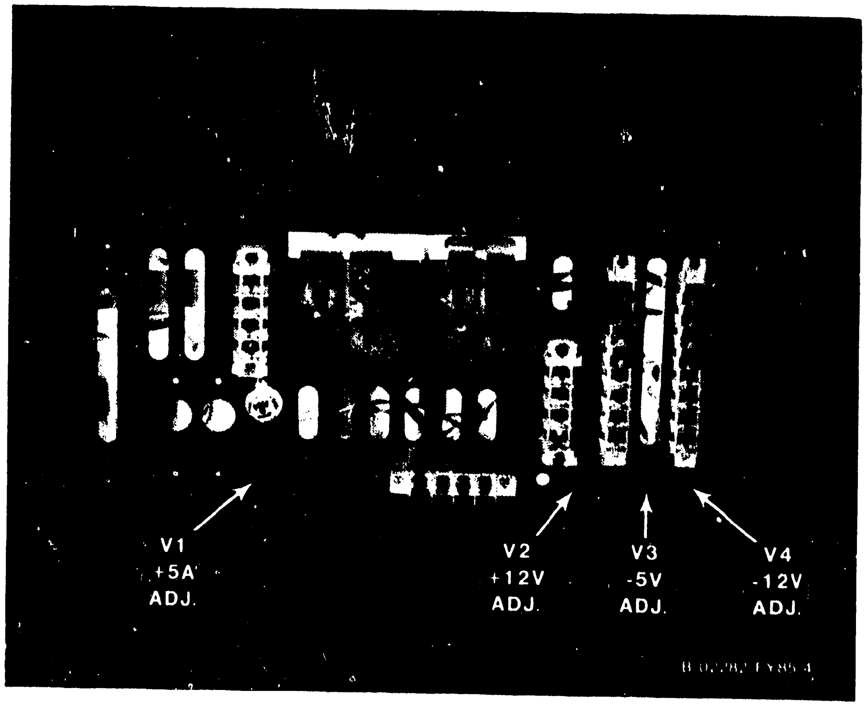


Figure 3-4. Multioutput Power Supply

PHOTO NOT AVAILABLE

Figure 3-5. Booster Power Supply

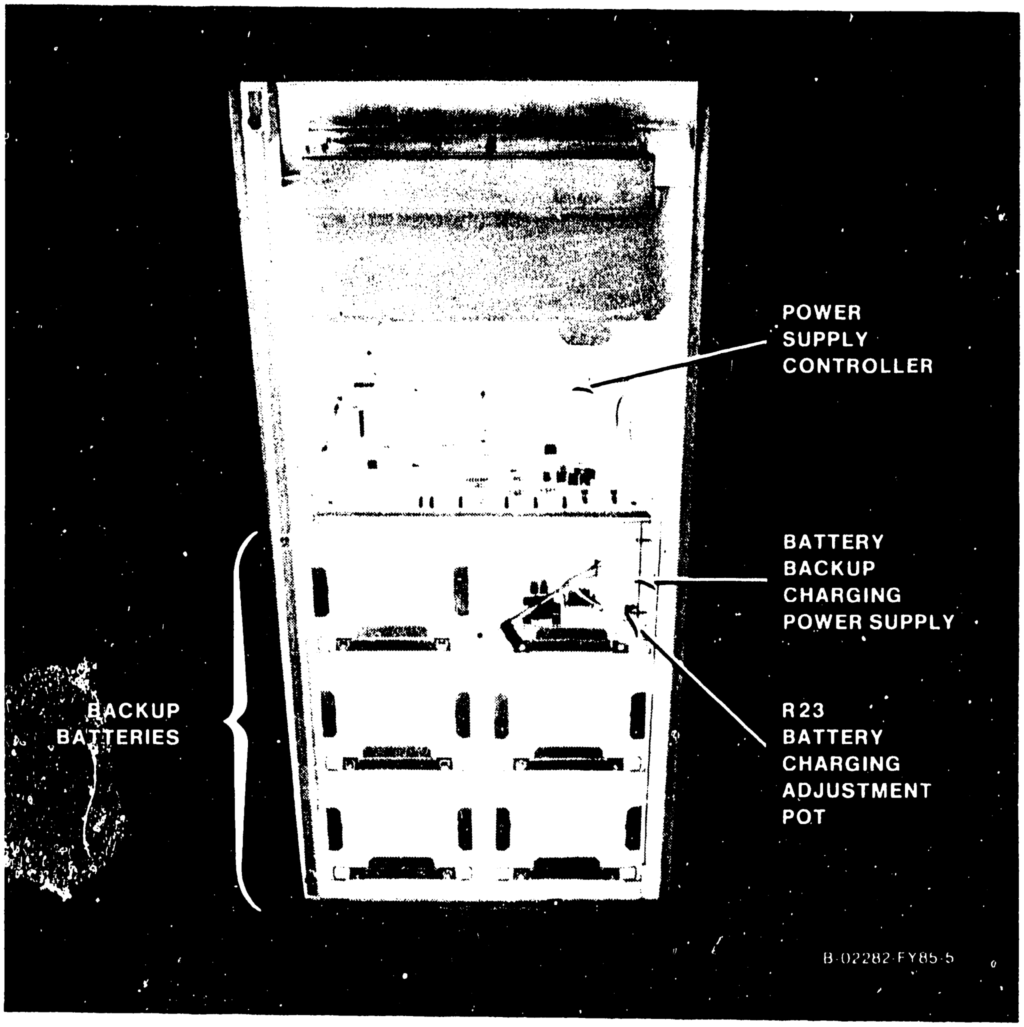
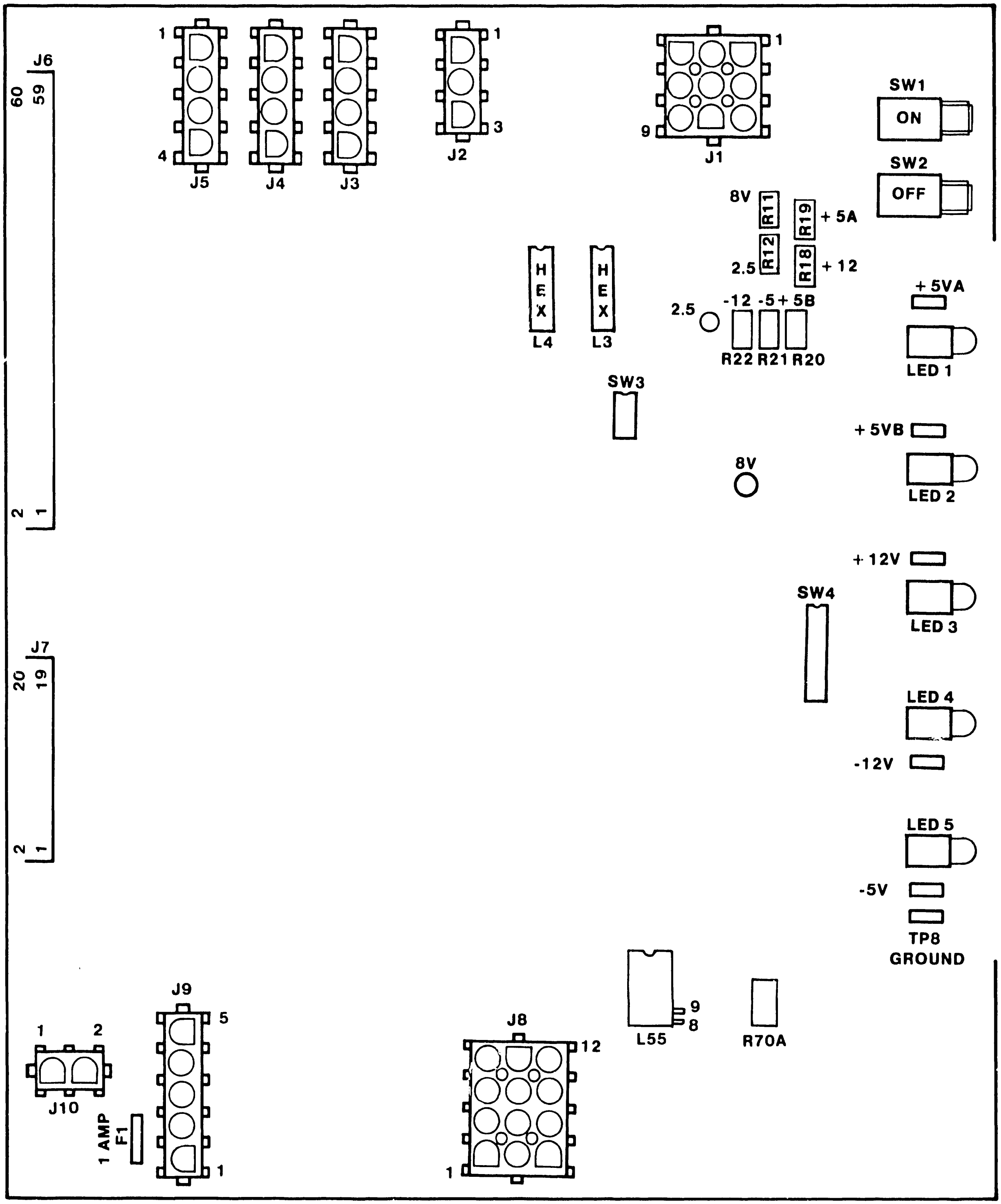


Figure 3-6. Front View - Power Supply Controller
and Battery Backup Assembly



B-02080-FY85-14

Figure 3-7. Power Supply Controller Board. (Rev. 0 Version)

3.6 OPTIONAL BATTERY BACKUP

In the event of an input ac power failure, five rechargable lead acid battery packs, figure 3-8, supply sufficient dc power to the power supplies to permit an orderly shut down of the mainframe. (Presently, the batteries do not supply power to any peripheral devices except the Support Control Unit (SCU) which is powered by the mainframe power supplies.) The length of time that the batteries provide power to the power supplies is preset by Switch 4 on the Power Supply Controller board. Currently, the time is set for 100 seconds for the Rev. 0 board, and 96 seconds for the Rev. 1 board, which represents approximately 90 percent of all expected power failures.

When the power fails, an alarm sounds at the SCU to alert the operator that a power outage is being experienced and the battery backup unit is providing power. The message "<Power Supply Failure>" appears on the SCU screen as well. The Battery Backup board, figure 3-9, notifies the SCU to start a software shutdown of the system.

Each battery pack weighs 22 pounds and is rated at 48 V dc, 5.5 amp. hours. The expected operating life span is between 18 and 24 months, with a shelf life of 5 years when stored at 40° F. When one pack becomes defective, all five packs must be replaced at the same time.

The packs are mounted below the Power Supply Controller board behind the left mainframe cabinet panel. They are connected in series to supply an average of 240 V dc and can be fully charged to 264-270 V dc. The packs are constantly being trickle charged by a modified Professional Computer switching power supply located beneath the Power Supply Controller board.

Normally, the power supplies rectify the 208-240 volts input ac line voltage to dc. When the Power Supply Controller senses an input line voltage of less than 195 volts ac, it signals the Battery Backup board to connect the batteries to the mainframe power supplies. The power supplies can regulate input voltages of between 180 and 325 volts.

Should the battery output drop below 192 V dc, the Power Supply Controller senses this and will power down the mainframe.

A LED, mounted on the Battery Backup board, indicates that the dc battery voltage is applied to the power supplies from the Battery Backup board. When the power supplies have been turned off, the battery voltage output from the Battery Backup board will turn off and the LED should go out. If the LED remains on when the power is turned off, there is a fault on the Battery Backup board.

WARNING

Even when the LED is off, battery voltage remains present on the input connectors from the batteries and other locations on the Battery Backup board.

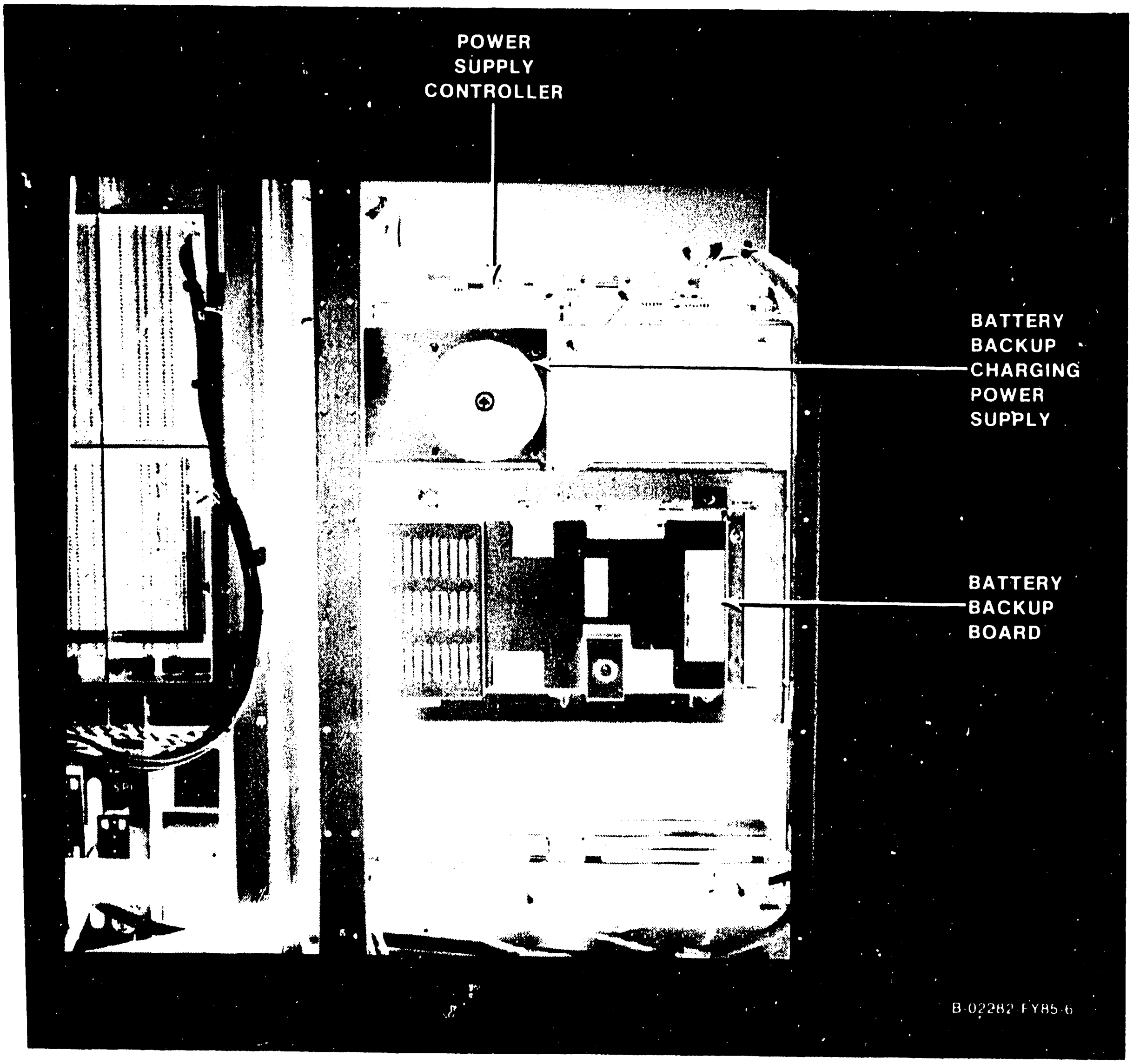


Figure 3-8. Rear View - Battery Backup Assembly

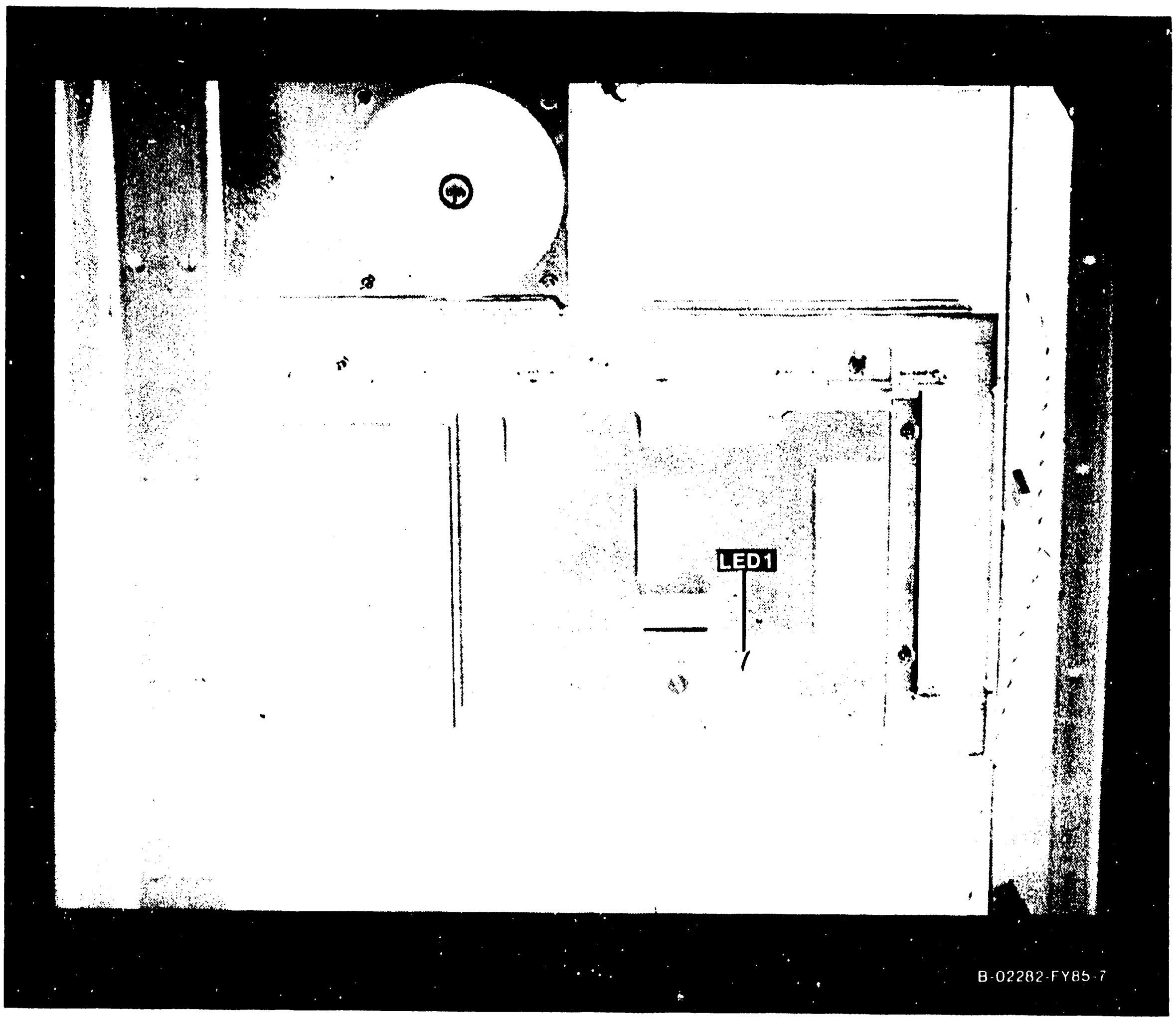


Figure 3-9. Battery Backup Board

3.7 CONTROL PANEL

Located in the top right corner of the front cover, the Control Panel, figures 3-10 and 3-11, contains four buttons and one key switch as follows: Power On pushbutton; Power Off pushbutton; System Reset pushbutton; Operator Console Reset pushbutton, and Remote Service/Remote Admin./Normal Control/-Control Lock switch.

3.7.1 POWER ON/OFF PUSHBUTTONS

Pressing the Power On pushbutton causes the Power Supply Controller to energize the switching power supplies. Pressing the Power Off pushbutton causes the Power Supply Controller to deenergize the switching power supplies.

3.7.2 SYSTEM RESET PUSHBUTTON

The System Reset pushbutton, when pressed, resets the system, clearing main memory and entering Control Mode.

3.7.3 OPERATOR CONSOLE RESET PUSHBUTTON

The Operator Console Reset pushbutton, when pressed, resets only the SCU, clearing SCU memory. It does not affect the CPU mainframe. It also resets the Z80 on the Local Comm. Processor. The Z80 then starts executing from memory location 0000.

3.7.4 KEY SWITCH

The 4-position Control Panel key switch controls the following functions:

a. Remote Service position permits running Remote diagnostics, and viewing the system error log.

b. Remote Admin. position permits the Remote System Administrator Facility features to be run. Other users can log on and run any available VS functions.

c. Normal Control permits all Control Panel controls to function once power is applied. All SCU functions can be run, as well as all Operator Console functions. Users can log on and run any available VS functions. Power Fail/Auto Restart functions are disabled.

d. Control Lock disables Power On when the system is powered off. Power Fail/Auto Restart functions are enabled. No SCU tasks can be run from the Operator's Console, but system activity can be monitored. Other workstation users can log on and run any available VS functions. The key can be inserted and removed in this position only.

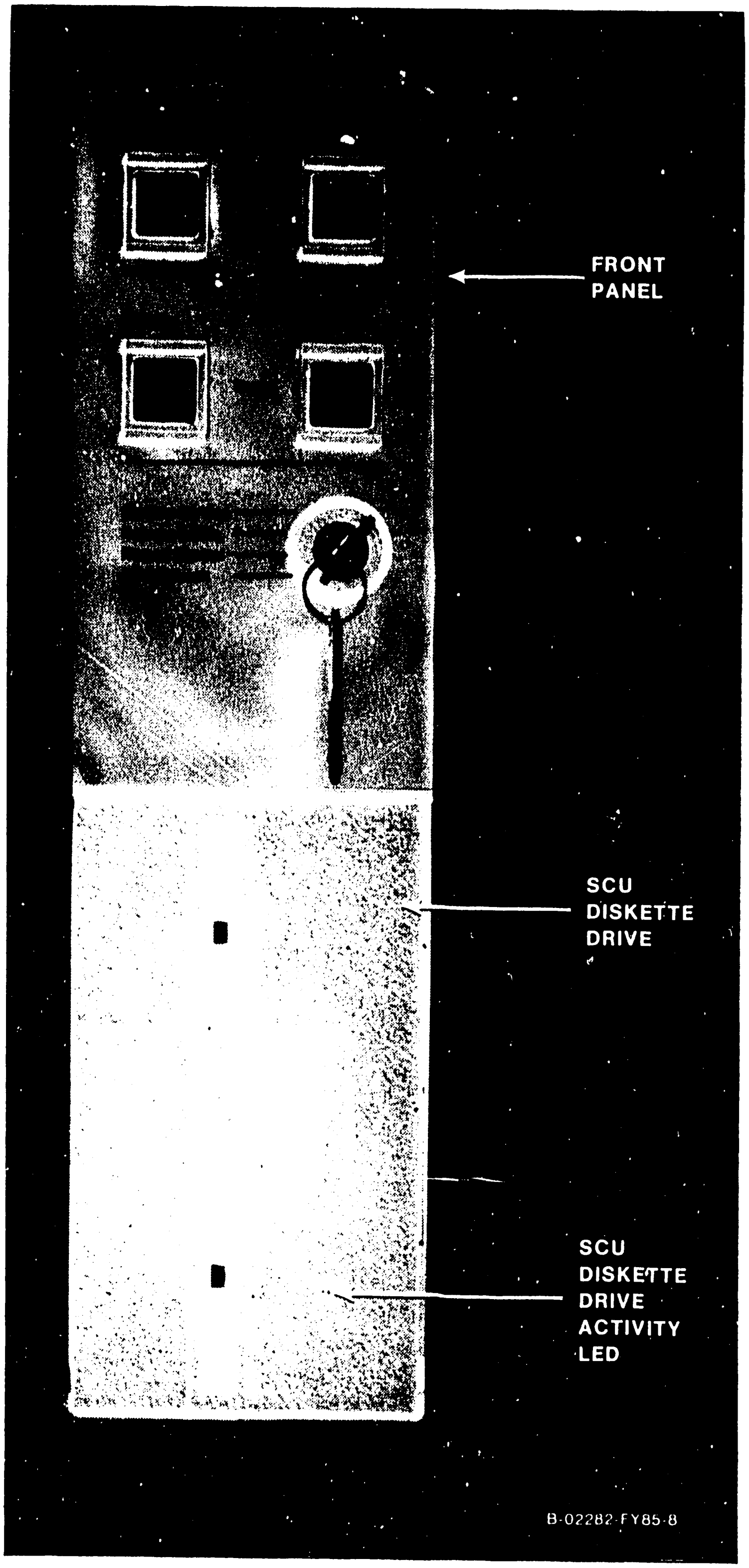


Figure 3-10. Control Panel And Diskette Drive

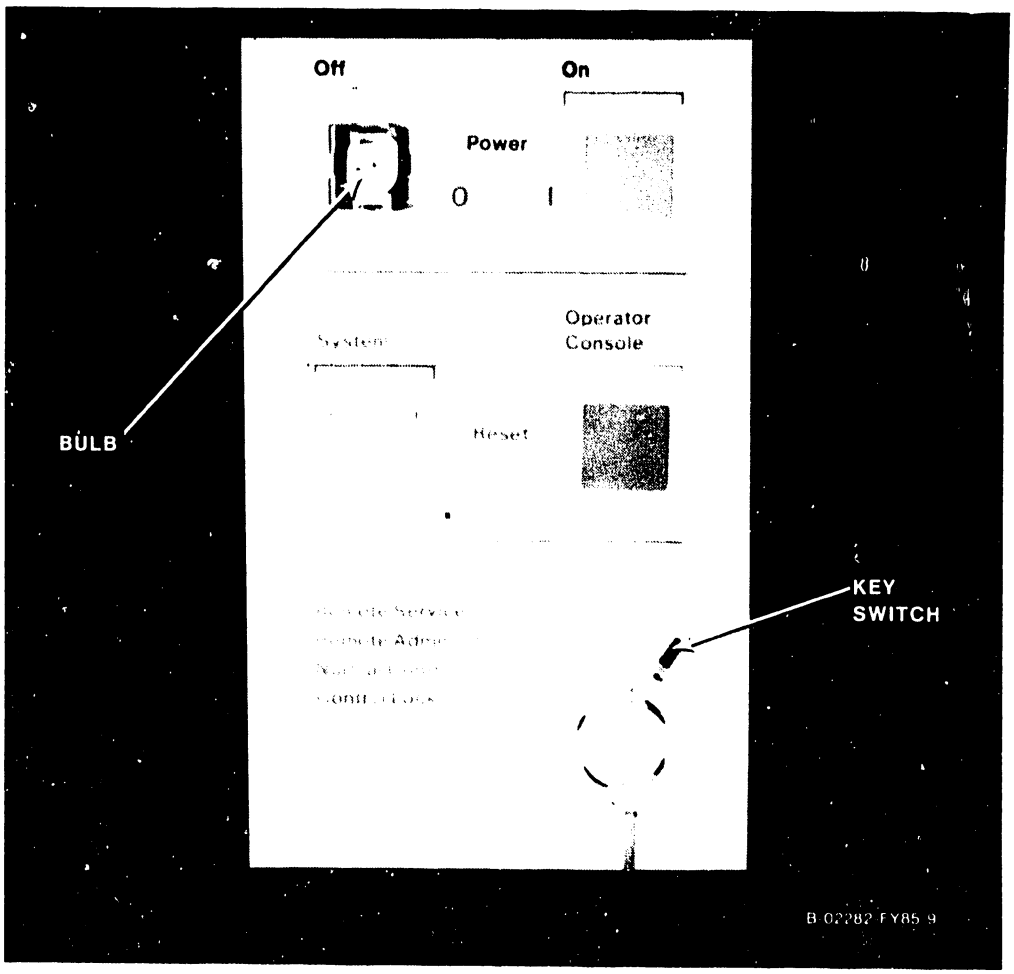


Figure 3-11. Control Panel Controls and Indicators

3.8 MAIN MEMORY SIZE

Memory can range in size from a minimum of 4 megabytes to a maximum of 16 megabytes, using 256K byte x 1 bit RAM chips. Each main memory board contains either 4 megabytes half-loaded (210-8703), or 8-megabytes fully loaded (210-8703-1).

3.8.1 MAIN MEMORY SIZE SELECTION

The Memory Control Unit (MCU) board has an 8-position jumper block, of which five positions are used to determine the maximum size of main memory. Refer to Chapter 5 for the jumper locations and configurations. Incorrect altering of the jumpers, or altering of the jumpers without adding the correct number of memory boards, can result in CP hangups and loss of data. Adding a board without altering the jumpers results in no change in apparent memory size to the CP.

Each main memory board also contains a 10-position jumper block used to determine whether the board is half-loaded or fully loaded with 256K byte x 1 bit RAM chips. Refer to Chapter 5 for the jumper locations and configurations.

3.9 IOC SWITCHES

The IOCs do not have the Bus Adapter and I/O slot selection DIP switches that are used on the VS-85/VS-100. Each IOC has an Identification (ID) Register that is set by the position of the IOC in the backplane. The CPU reads the ID Register to determine the type and position of the IOC.

The only switch common to each IOC is a 4-position diagnostic DIP switch. Refer to Chapter 5 for the normal switch settings and Chapter 7 for the switch functions and test positions.

The 23V98 Disk Drive IOC does have two 8-position disk device type DIP switches; the 23V96 Multiline TC IOC has an 8-position port select DIP switch for loopback tests; and the 23V79 CIU BLANC IOC has an 8-position CIU Functions DIP switch. Refer to Chapter 5 for the switch settings.

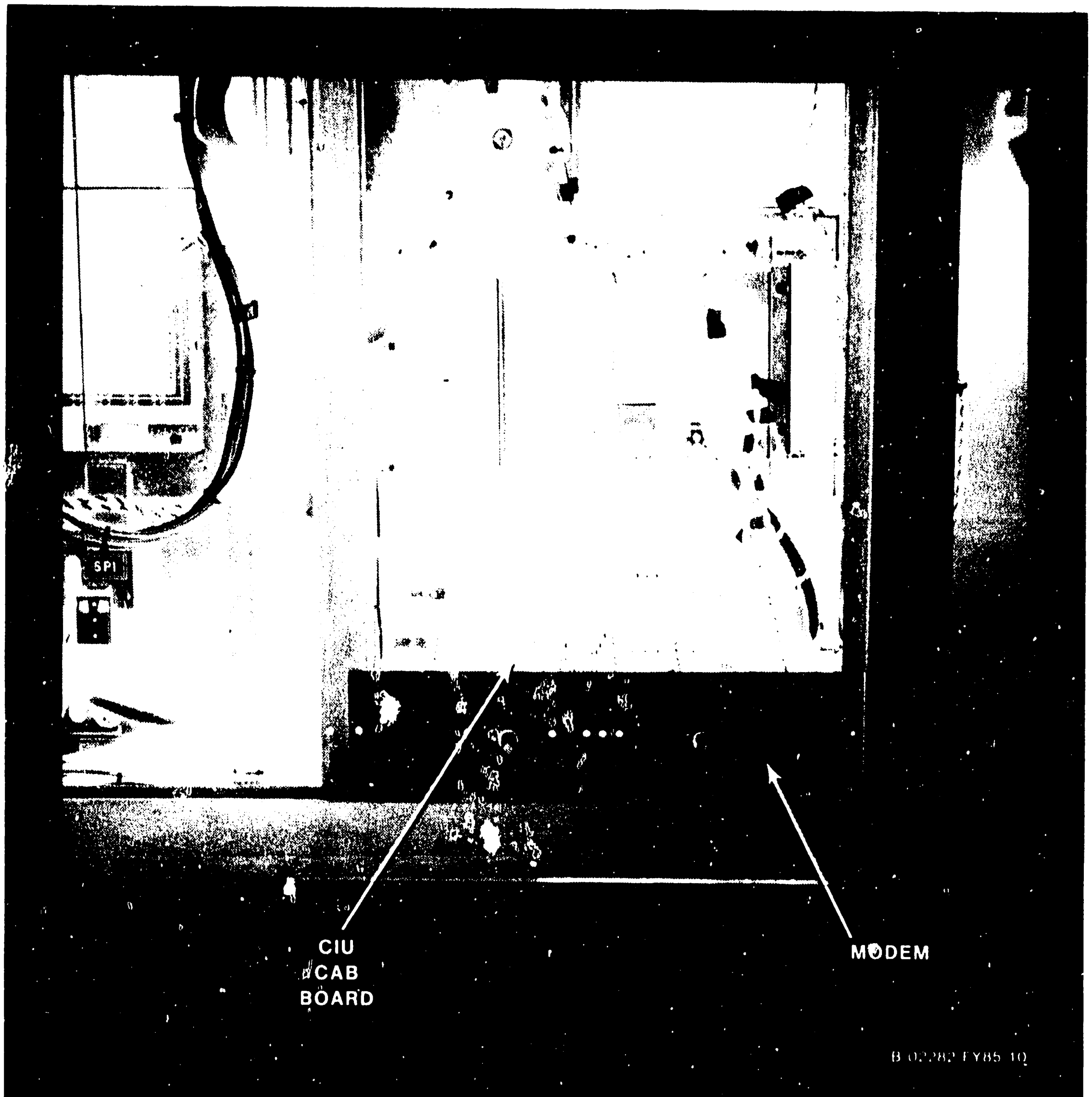


Figure 3-12. 10 MBPS Modem Back Panel Assembly

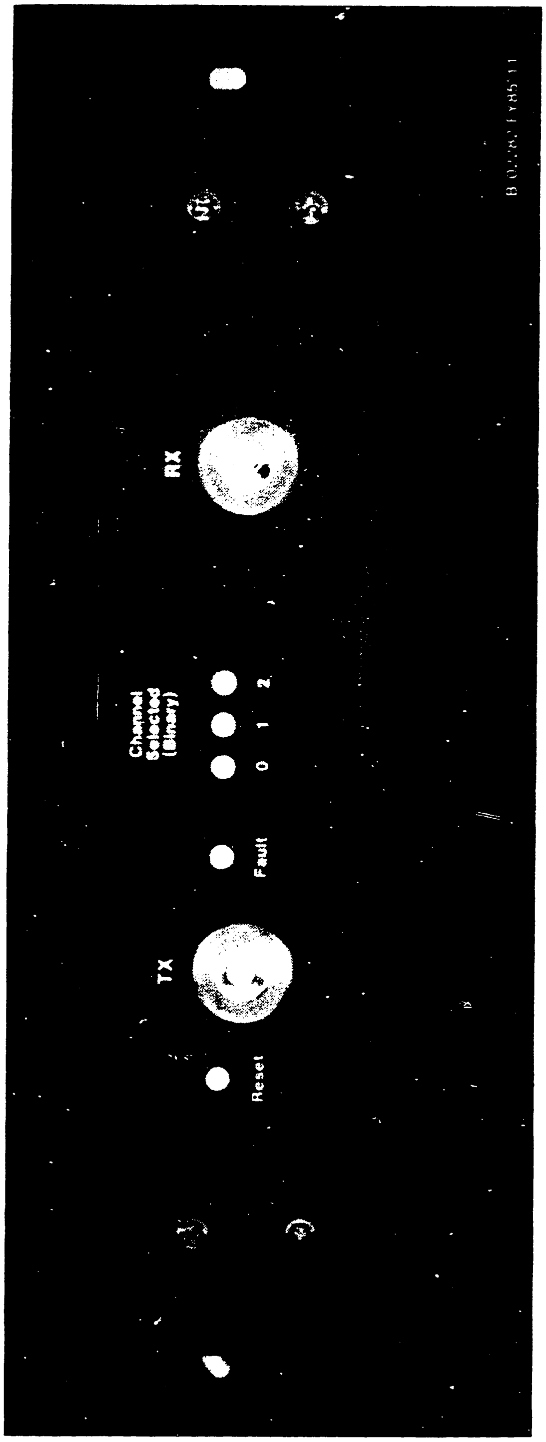


Figure 3-13. 10 MBPS Modem Controls and Indicators

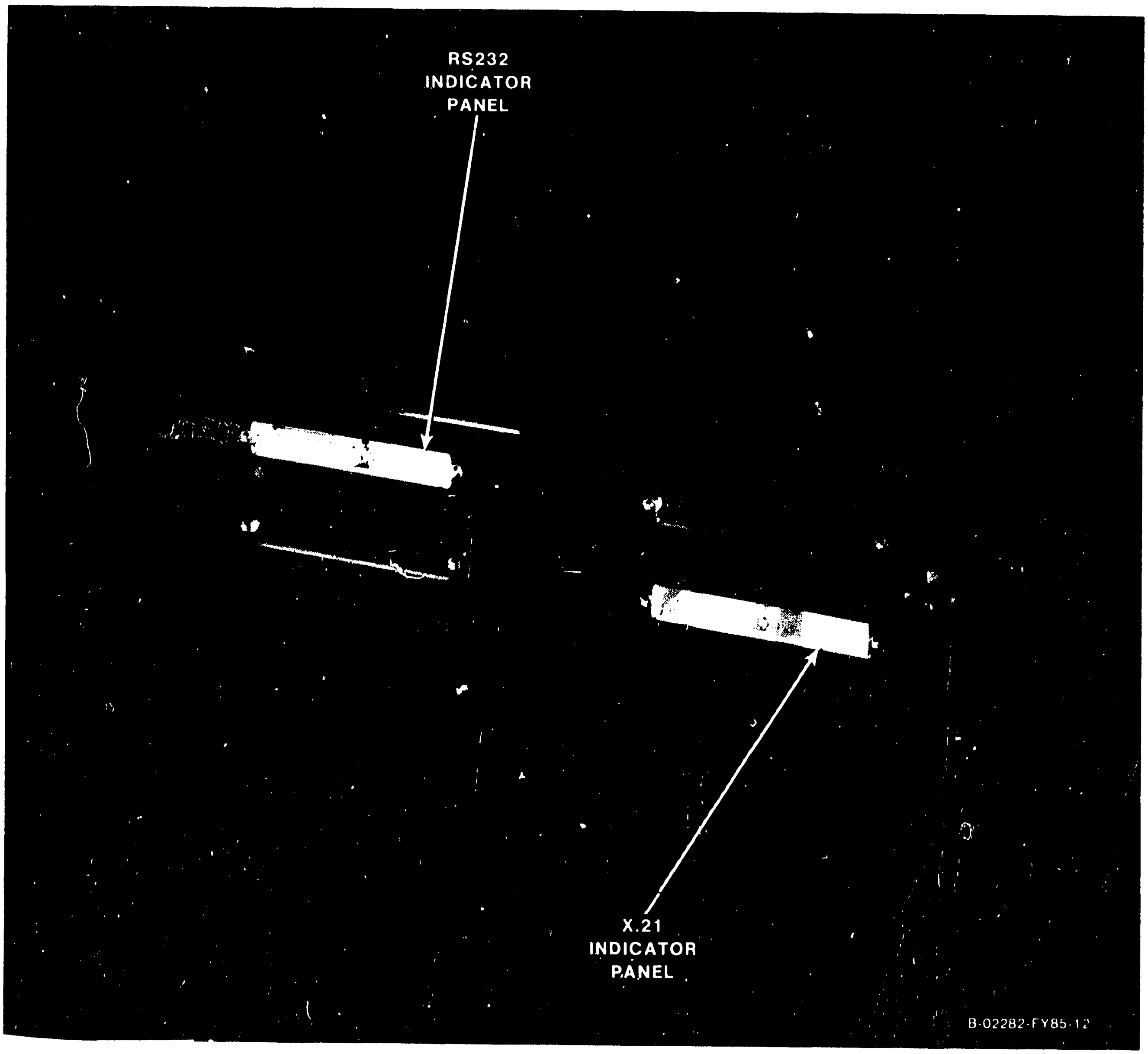


Figure 3-14. Multiline TC Back Panel Indicators

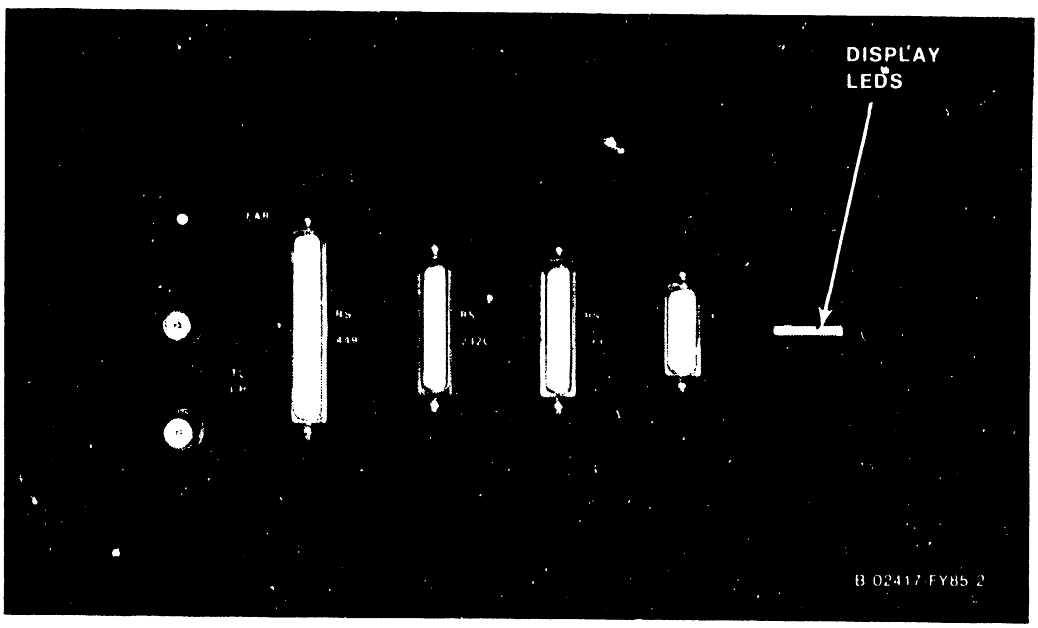


Figure 3-15. 6550 Gate Array TC Back Panel Indicators

3.10 IMPORTANCE OF FOLLOWING POWER UP OR DOWN PROCEDURES

The following summary describes general rules that must be followed when powering a VS-300 system up or down:

- When powering down, the system must be in Control Mode.
- Always power the mainframe up before powering up disk drives and tape drives. Always power the mainframe down after powering down the disk drives and tape drives. Failure to follow this procedure can result in disk or tape VTOC damage or data loss.

The Volume Table of Contents (VTOC) resides at the beginning of each disk pack. If the VTOC is damaged, two conditions may occur: I/O errors occur upon IPL and the VS Workstation Emulation - Initialization In Progress screen remains displayed. Although many of the original files may remain intact, the VTOC is inaccessible.

NOTE

Crash-tolerant or media-tolerant volumes can help protect VTOC integrity.

In addition to this VTOC integrity problem, other conditions may cause the writing of random blocks of data to the disk. These conditions include power failures, surges, or fluctuations, or a possible hardware malfunction.

3.11 POWER-UP AND IPL PROCEDURES

This section describes standard power-up and IPL procedures for the VS-300.

1. Power up all workstations and printers.
2. Turn ON the mainframe ac On/Off circuit breaker.
3. Make sure the Front Panel key switch is in Normal Control position.
4. Power up the mainframe and the SCU by pressing the Control Panel On pushbutton, located above the diskette drive door.
5. Power up the disk drives.
6. Press the System Reset pushbutton and then press the Operator Console Reset pushbutton.
7. After a pause, the SCU start-up sequence is invoked and start-up messages appear on the SCU screen:

   "WANG SUPPORT CONTROL UNIT REV. X.XX"
   "01 Start From Winchester"

8. Followed by:

"Wang Support Control Unit - BIOS X.XX"
"MS-DOS Version X.XX"

```
                 SYSCON X.X.X

     Copyright Wang Laboratories, Inc. 1985
```

9. The Console Processor screen then appears.

```
                    <<< System in Control Mode >>>

                    *** Wang VS System Console ***

   SYSCON Version X.XX        11:06 AM          Monday, January 6, 1986


          Press (HELP) for online system console information.


               Use the function keys to select a command:

     (1) ENTER Workstation Emulation    (8)  RESET System
     (2) ENTER Control Mode             (9)  RESET Console


                                        (12) SET Console Defaults
     (5) AUTO IPL                       (13) SET Time and Date
```

Figure 3-16. Console Processor Screen

NOTE

The functions that the key switch allows in any one of the four key switch positions are highlighted on the Console Processor screen.

10. If necessary, press HELP for an explanation of the PF key functions.

11. a. Press PF5 (AUTO IPL). This message appears:

"WARNING: This function resets the system, RETURN to proceed or PF16 to abort"

b. Press RETURN. (If the console defaults need modifying, or if the CPU code has not been loaded, a CPU or IPL error may appear. Go to step 12. If there are no changes necessary, or no CPU or IPL errors appear, go to step 13.)

12. a. Press PF12 (SET Console Defaults). The System Console Default screen appears.

```
                    <<< System in Control Mode >>>

                    *** System Console Defaults ***


IPL Device Address: R 0100

CPU Microcode File: /SCU/OBJVSE.CP8
FPU Microcode File:

WS Emulator Options: -PC

Give Console Date/Time to VSOS: N
Warning message before a reset: Y

(9) Modify Defaults     (10) Load System Microcode            (16) Exit
```

Figure 3-17. System Console Default Screen

1) If defaults are incorrect, press PF9 (Modify Defaults), make corrections as shown in figure 3-17, press RETURN, and/or:

2) Whether defaults were corrected or not, press PF10 (Load System Microcode).

b. Press PF16 (Exit). and the Console Processor screen (figure 3-16) reappears.

c. Press PF5 (AUTO IPL). This message appears:

"WARNING: This function resets the system, RETURN to proceed or PF16 to abort"

d. Press RETURN.

13. The Workstation Initialization Screen, figure 3-18, appears.

```
                              Wang
                               VS
                      Workstation Emulation
                          Version X.XX

            Initialization in Progress - Please Wait
```

Figure 3-18. Workstation Initialization Screen

14. The SYSGEN Configuration Screen appears.

```
***MESSAGE M001 BY SYSGEN

                INFORMATION REQUIRED BY PROGRAM

                 ACTIVE SUBPROGRAM IS @SYSGEN@

  Specify the name of the system configuration file and press (ENTER)
                              -or-
           Press (1) to use one workstation and one disk.

                      SYSFILE = @CONFIG@
                      SYSLIB  = @SYSTEM@

    Specify the communications configuration file to be use, if any

                      COMMFILE = ********
                      COMMLIB  = @SYSTEM@

Inhibit logons at all workstations?               LOGONS = NO■

Load Micro Code to all devices?                   LMCODE = NO■

Inhibit dumping continuable halts?                CMDUMP = NO■
```

Figure 3-19. SYSGEN Configuration File Screen

NOTE

If the IPL was unsuccessful and an "IPL failed" message is received, refer to paragraph 4.9.3, IPL Errors

15. a. On the SYSGEN Configuration File screen, enter the names of the configuration files and the system library to be used. The field for the communications configuration file is blank. Fill in the communications configuration file field only if communications are going to be used. To change one of these values, move the cursor to the appropriate field and enter in the new information. Then, press RETURN.

NOTE

If the system is being IPLed for the first time, the default values of @CONFIG@ and @SYSTEM@ are used for the configuration file and system library, respectively. After IPLing for the first time, configuration files can be created using GENEDIT. Refer to the VS Software Bulletin Release 7.06.

b. After the values have been entered, the VS-300 stores them in a start-up file. At the next IPL the system displays the stored values and allows them to be changed.

c. The prompt "Inhibit logons at all workstations?" allows workstation logons to be inhibited. If "YES" is entered, only the SCU user can log on. The default value is "NO", which allows logons at all workstations, which were enabled before this IPL.

d. The prompt "Load Micro Code to all devices" lets microcode be loaded to each workstation (including remote workstations) as part of the IPL procedure. If "Yes" is entered, microcode is loaded to each workstation and the IPL process is significantly slower. This option is used when a workstation is hung up or when the workstation configuration has been changed. The default value is "No".

e. The prompt "Inhibit dumping continuable halts" allows disabling of the Continuable Dump for errors that do not require reIPL. If "Yes" is entered, Continuable Dumps which do not reIPL the system are not performed and system processing continues with the system error in effect. If "No" is entered, all Continuable Dumps occur. The default value is No. Refer to Chapter 7 for more information on the Continuable Dump.

16. Press RETURN when finished with the SYSGEN Configuration File screen. (Or, to bring up a minimum configuration of one workstation [W/S0] and one disk, without changing the default values, just press PF1.)

NOTE

> The IPL procedure automatically activates any remote workstations that have been configured via the remote workstation parameters in the GENEDIT procedure.

17. After pressing RETURN from the SYSGEN Configuration File screen, the VS-300 checks to determine if any of the critical operating system components are obsolete or incompatible. If no problems are detected, the IPL continues and the message "System Generation in Progress" appears on the SCU.

    a. If incompatibilities exist that can cause problems, the IPL is stopped and a warning message is displayed by @SYSGEN@.

18. The message "I/O Subsystem Load in Progress" appears on the SCU screen.

19. a. If the SCU real time clock is not usable, the date and time screen appears. Enter the correct date and time, and press RETURN.

    b. This screen also allows changing the amount of memory available for use. The default value is the total amount of physical memory for the system. To change the value, move the cursor to the field, enter the new value, and press RETURN.

20. The message "System Initialization in Progress" appears on the SCU screen.

The VS-300 is now initialized and ready for operation. VS workstation emulation is running on the SCU and the Operator's screen is displayed. To log on from the SCU;

1. Press PF1 and the VS Logon screen appears.

2. Enter the User ID and Password. (As this is the first time that the system has been IPLed and logged onto, use "CSG" for the User ID and leave the Password field blank.)

3. Press RETURN. The User screen is displayed.

3.12 STANDARD POWER-DOWN PROCEDURE

The VS-300 can be either partially or completely powered down.

CAUTION

It is essential to power the mainframe up before powering up disk drives and tape drives, and to power the mainframe down after powering down disk drives and tape drives. Failure to power the system up and down correctly may result in disk and tape information loss.

NOTE

Always power down all workstations before powering down the mainframe. The 4200 Series workstations cause Error 7203 (read and test data error)if they are not powered down before the mainframe. Power down the workstations and continue with the system power-down procedure.

To completely power down the system, perform the following from Workstation 0, the SCU:

1. Inhibit further logons by pressing PF6 (INTERACTIVE Tasks) or PF13 (WORKSTATIONs) from the Operator's Console menu.

2. Notify all users to log off the system by pressing PF14 (SYSTEM Options - Broadcast SYSTEM MESSAGE). Use PF6 from the Operator's Console to verify that all users have done so.

3. Inhibit the execution of any pending background procedures by pressing PF3 (PROCEDURE Queue) on the Operator's Console menu.

4. Press PF9 (PRINTERs) on the Operator's Console menu to idle all printers by changing their status.

5. Press PF7 to deactivate the background task through the Control Proc Initiation command (NON-INTERACTIVE Tasks) on the Operator's Console menu.

6. Log off from the SCU.

7. Press CONTROL, then press SHIFT and CANCEL simultaneously to exit workstation emulation. The Workstation Emulation menu appears. Use the space bar to select Suspend Emulation and press EXEC.

8. The Console Processor screen appears. Press PF2, ENTER Control Mode.

9. Power down all workstations.

10. Unload the cartridge tape drive, if any, by pressing the Online pushbutton on the front of the drive.

11. Unload the nine-track tape drives, if any, by pressing the Online and then the Rewind pushbuttons. When the nine-track tape drive has reached its load point, press the Rewind pushbutton again and wait until it is rewound. Once rewound, finish powering down tape drives by pressing the Power pushbutton on each drive.

12. Power down all disk drives.

13. Power down the mainframe and SCU by pressing the Power Off pushbutton.

If a partial power-down procedure is being performed, the system can be left in Control mode without powering down every device. For a partial power-down of the system, perform steps 7 and 8, and 10 through 13.

To bring a system up from a complete power-down state, follow the complete standard procedure in paragraph 3.11 for powering up the system. To bring a system up from a partial power-down state, follow the power-up procedure described in paragraph 3.11, starting with step 4.

3.13 POWER FAILURE PROCEDURE (WITHOUT OPTIONAL BATTERY BACKUP)

Once power is restored, bring the VS-300 back up by pressing the On pushbutton and reIPL. Follow the IPL procedure in paragraph 3.11, starting with step 4.

CHAPTER 4 INSTAL-LATION

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INSTALLATION

4.1 GENERAL

This chapter describes the procedures for unpacking, inspecting, and installing the VS-300 mainframe. Included in this chapter are instructions for system interconnection and initial power-up. Refer to Chapter 3, Operation; Chapter 5, Preventive and Corrective Maintenance and Removal/Replacement; and Chapter 7, Troubleshooting, of this manual for more information needed to complete installation. Actual installation should not begin until the site requirements have been met. Refer to the following two sources for publications concerning site requirements.

Publication Title	WLI P/N
Customer Site Planning Guide	700-5978
Technical Documentation Catalog/Index	741-0000
Wang Customer Resource Catalog	700-7647

4.2 INSTALLATION SITE CHECK

Prior to installation, the following conditions must have been met:

1. All site plans should have been approved by both the customer and a Customer Service Representative.

2. All building alterations must have been completed and inspected.

3. All electrical wiring, air conditioning, and telecommunications (TC) modifications must have been installed and tested. (The following TC equipment should have been ordered for remote maintenance support:)

    a. Telephone line. (A dedicated line is not required.)

    b. Telephone.

    c. Either of the following modular connecting blocks for the telephone:

        1) RJ11C jack for desk top telephones

        2) RF11W jack for flush mounted wall telephones

NOTE

RF11W flush mount wall phone jack can be used with the "T" connector and a desk top phone, but a wall mounted phone cannot be used.

4. The preinstallation inspection is to be performed two weeks prior to delivery. At this time, the service representative will check the site for compliance with VS site specifications. The service representative will bring any unsatisfactory conditions noted to the attention of the customer for correction.

NOTE

Before installation of a VS-300 can take place, the minimum specifications as described in publications listed in the Customer Site Planning Guide (700-5978), the Technical Documentation Catalog/Index (741-0000), and the Customer Resource Catalog (700-7647) should be met. Failure to meet these requirements can be cause for the service representative to deem a site as unsuitable for the proper functioning of a VS-300 system.

4.3 PUBLICATIONS

Refer to the following source for publications containing information that will be helpful in installing the VS-300.

Publication Title	WLI P/N
Technical Documentation Catalog/Index	741-0000

4.4 TOOLS AND TEST EQUIPMENT

1. No special tools or test equipment are required.

4.5 UNPACKING

Before unpacking the VS-300, check all packing slips to make sure that the proper equipment has been delivered. Refer to the model number information below. After checking packing slips, inspect all shipping containers for damage (crushed corners, punctures, etc.).

4.5.1 CLAIMS INFORMATION

If damage is discovered during inspection, the customer should file an appropriate claim promptly with the carrier involved, and notify your service manager.

Table 4-1. VS-300 Models

Model Number	WLI/P/N	Description
VS300-4	157/177-7301	4096KB Main Memory
VS300-8	157/177-7302	8192KB Main Memory
VS300-12	157/177-7303	12,288KB Main Memory
VS300-16	157/177-7304	16,384KB Main Memory

NOTES

1. Part number prefix 157 = 50Hz. ac line frequency mainframes.
2. Part number prefix 177 = 60Hz. ac line frequency mainframes.

4.5.2 UNPACKING THE MAIN FRAME

1. Cut and remove the strapping that secures the top cover and outside tube to the shipping pallet. (If the strapping is metal be careful that it does not spring out and away from the shipping container.)

2. Remove the top cover and the outside tube.

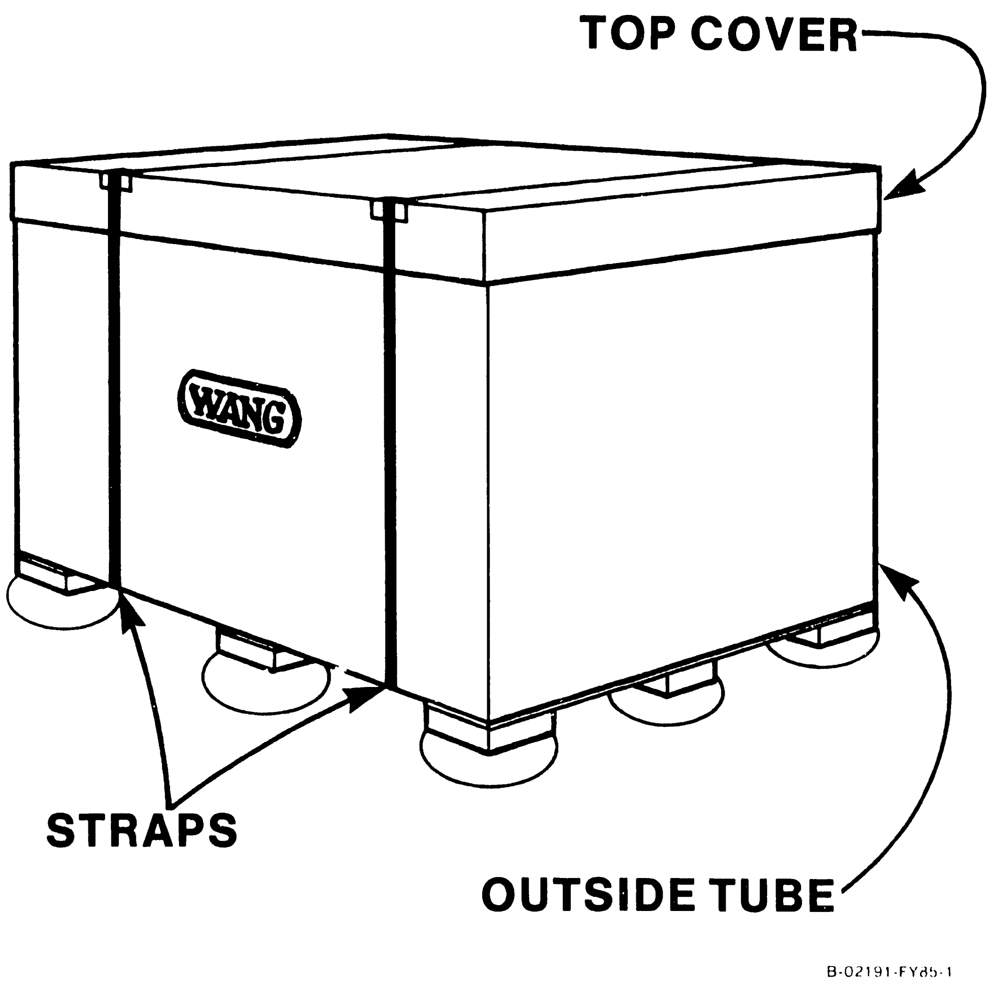


Figure 4-1. Unpacking the Main Frame (1 of 6)

3. Remove the top cushion pad and plastic wrap covering the mainframe cabinet.

4. Remove the shipping bolts securing the mainframe cabinet and the support assembly to the pallet.

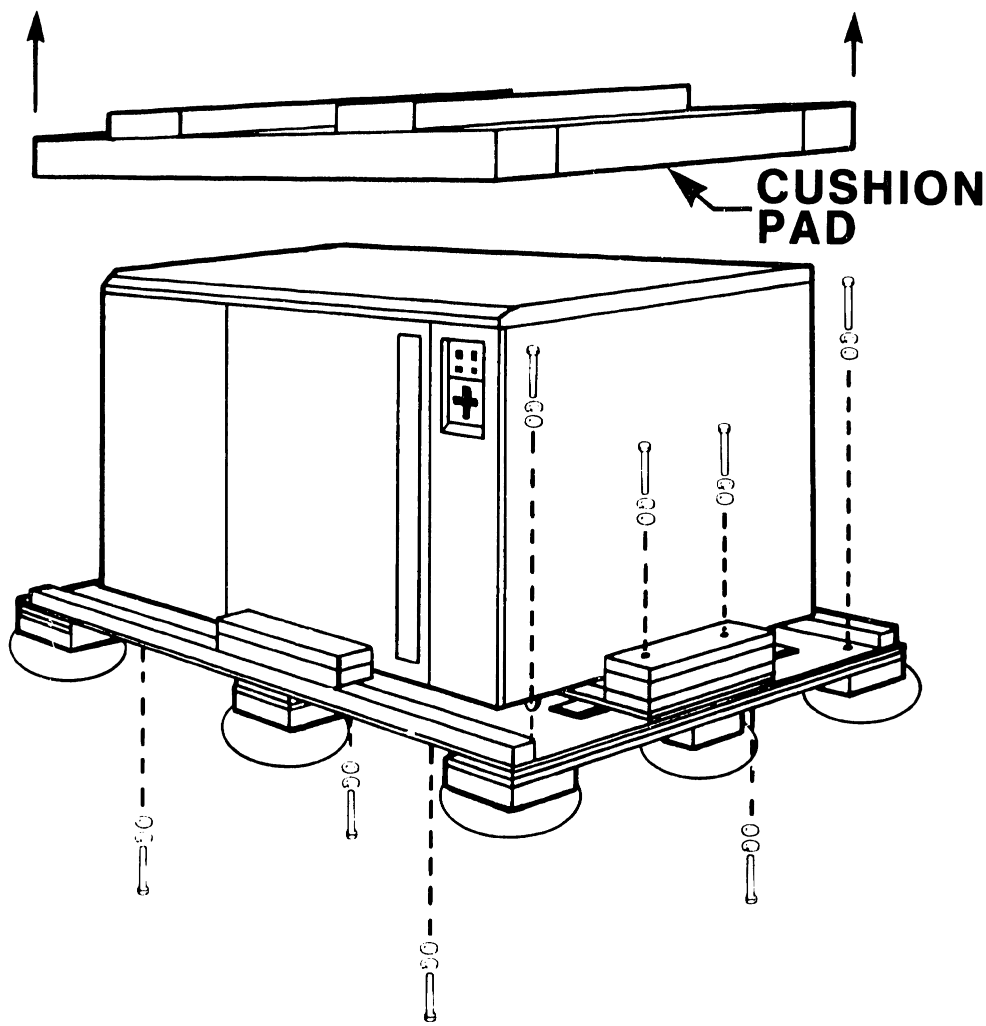


Figure 4-2. Unpacking the Main Frame (2 of 6)

WARNING

The mainframe cabinet weighs between 750 and 850 pounds (340-385kg). Be careful when performing the following steps.

5. Push the mainframe 1" or 2", enough to position the casters on the wheel blocks.

NOTE

An alternate method is to pry up each corner of the mainframe cabinet at a time with a piece of 2"x4" lumber (if available) and swivel each caster up onto the wheel blocks.

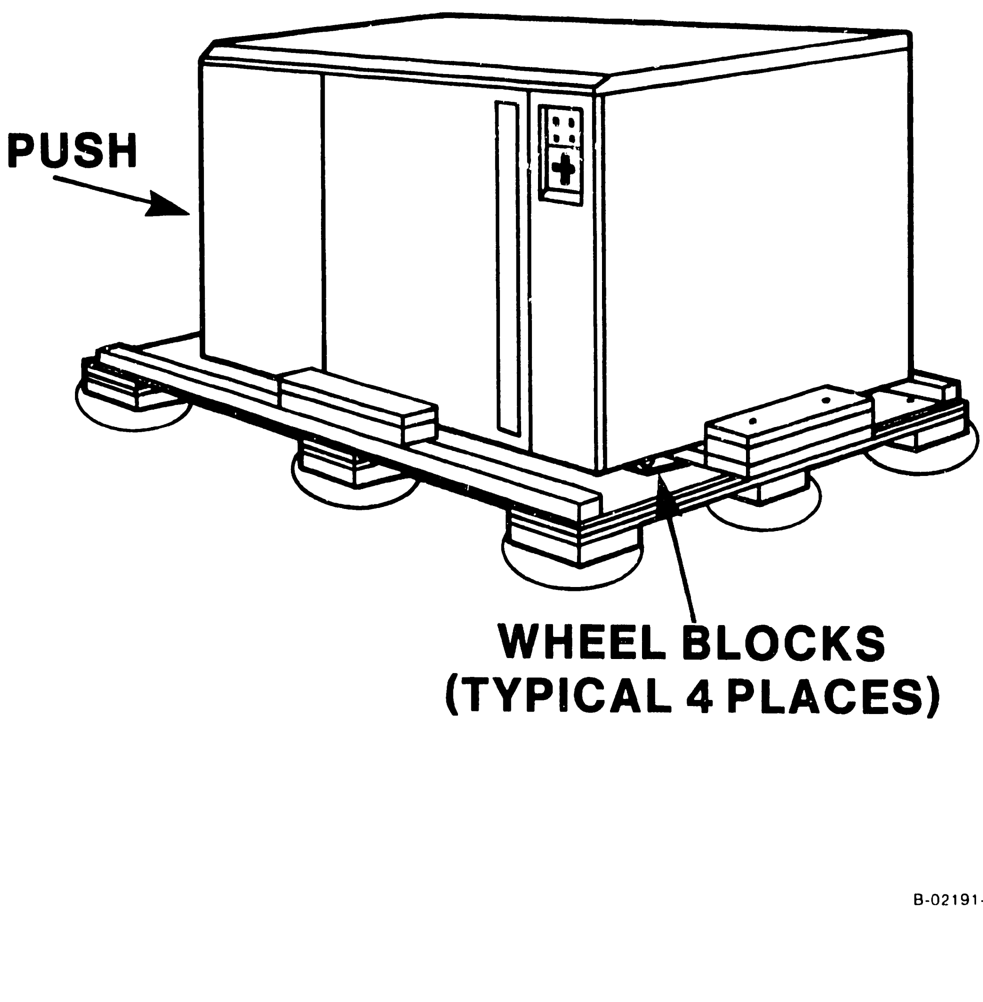


Figure 4-3. Unpacking the Main Frame (3 of 6)

6. Pull out and remove the support assembly.

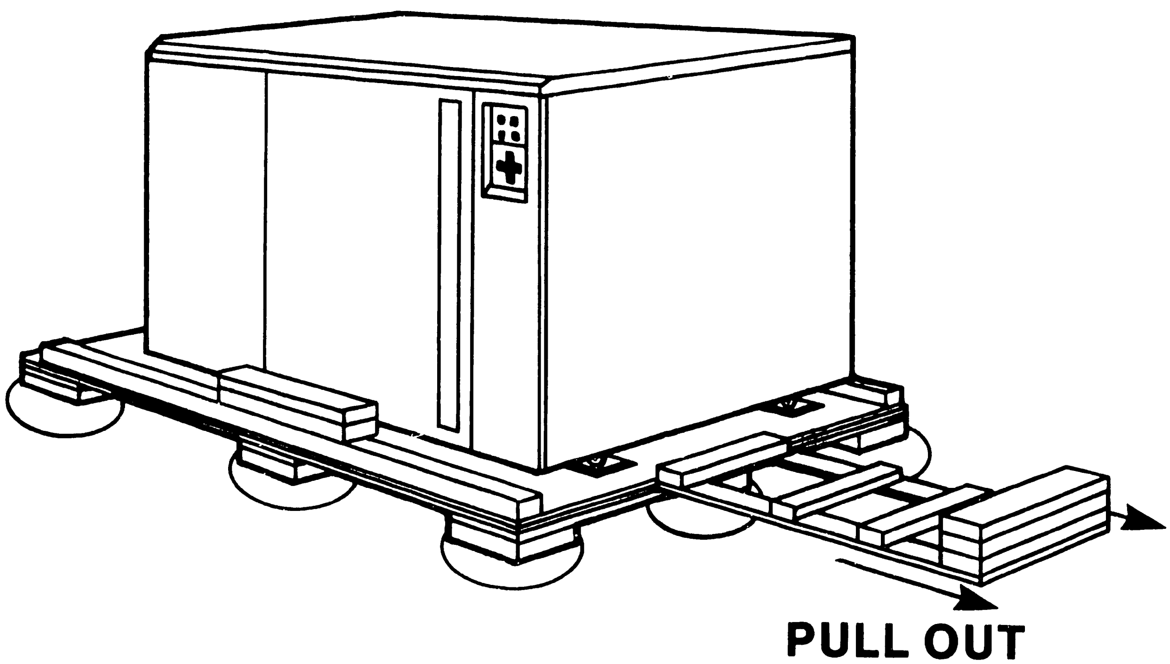


Figure 4-4. Unpacking the Main Frame (4 of 6)

WARNING

The mainframe cabinet will begin to tilt down when the cushion assembly is pulled out from under the pallet.

7. Pull the cushion assembly out from under the pallet.

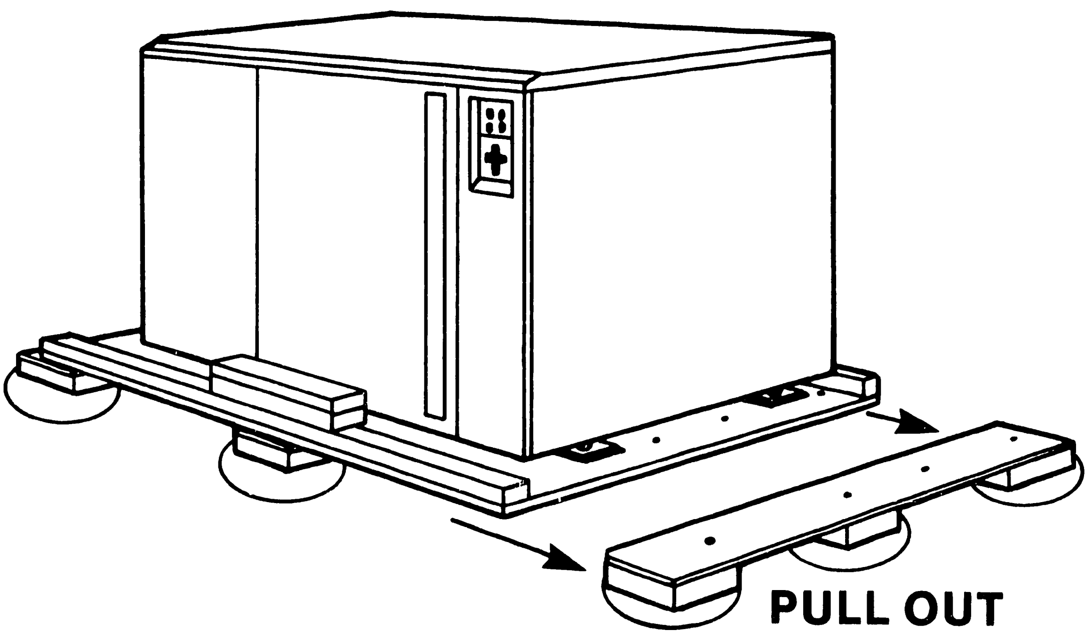


Figure 4-5. Unpacking the Main Frame (5 of 6)

8. Carefully push the cabinet off the pallet.

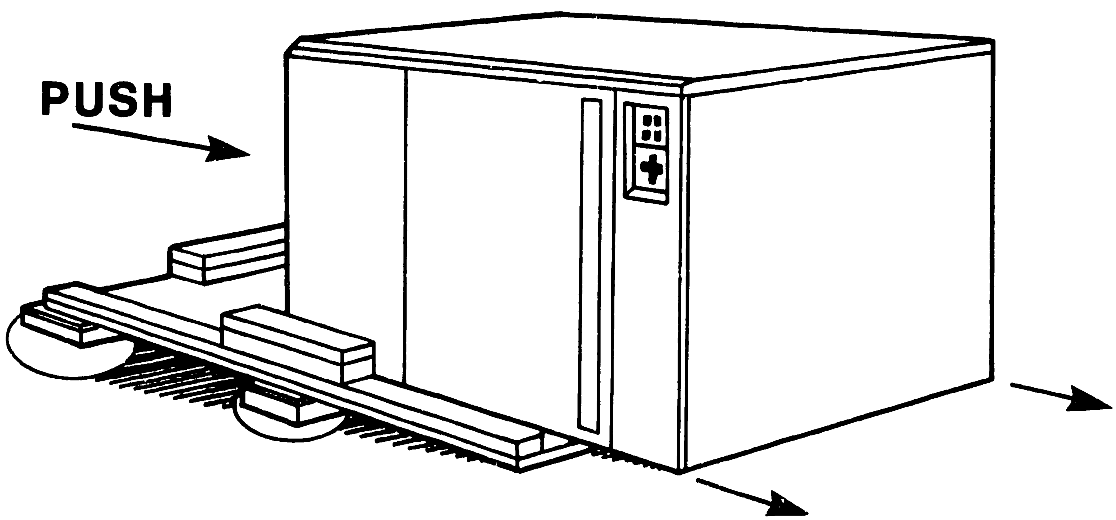


Figure 4-6. Unpacking the Main Frame (6 of 6)

9. Move the cabinet to it's permanent location.
10. Once the cabinet is in place, check the service clearances as listed below.

Service Clearances	Inches	Centimeters
Front	36	91.4
Rear	36	91.4
Left	24	60.9
Right	24	60.9
Top	36	91.4

4.5.3 UNPACKING THE PERIPHERALS

Before proceeding, carefully unpack all peripherals according to procedures outlined in applicable maintenance manuals. As each unit is unpacked, check it for any obvious shipping damage. Refer to paragraph 4.5.1 if any damage is seen.

CAUTION

```
*****************************************************************
*                                                               *
*  THIS COMPUTER EQUIPMENT HAS BEEN VERIFIED AS FCC CLASS A.    *
*                                                               *
*****************************************************************
```

IN ORDER TO MAINTAIN COMPLIANCE WITH FCC CLASS A VERIFICATION, THE FOLLOWING CONDITIONS MUST BE ADHERED TO DURING NORMAL OPERATION OF EQUIPMENT.

- ALL COVERS MUST BE ON SYSTEM AND SECURED IN THE PROPER MANNER.
- ALL INTERNAL CABLES MUST BE ROUTED IN THE ORIGINAL MANNER WITHIN THE CABLE CLAMPS PROVIDED FOR THAT PURPOSE.
- ALL EXTERNAL CABLING MUST BE SECURED AND THE PROPER CABLE USED TO ENSURE THAT CABLE SHIELDING IS PROPERLY GROUNDED TO THE CABLE CLAMPS PROVIDED.
- ALL HARDWARE MUST BE PROPERLY SECURED.

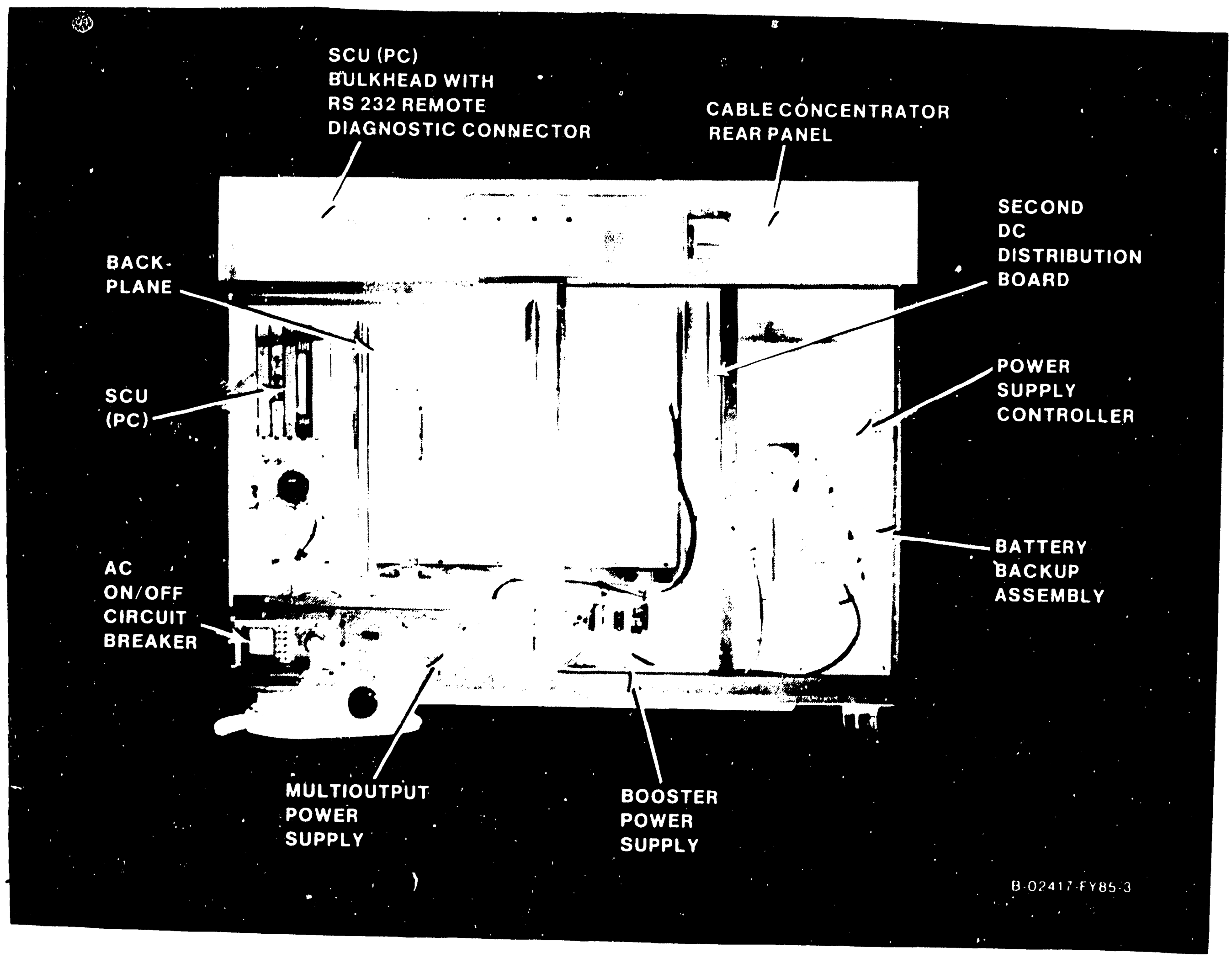


Figure 4-7. Rear View of Mainframe

4.6 MAINFRAME INSPECTION

NOTE

Quality assurance procedures and tests have shown that VS mainframes arriving on the customer's premises require only visual inspection, voltage checks, software loading, and cabling. Therefore, the following inspection and installation procedures for all VS mainframe products are in effect.

DO NOT REMOVE PRINTED CIRCUIT BOARDS FOR INSPECTION

DO NOT CLEAN PRINTED CIRCUIT BOARD CONTACTS WITH AN ERASER

INSPECT CPU MAINFRAME VISUALLY

REPORT INSTALLATION PROBLEMS ON THE INSTALLATION REPORT AND STATE SPECIFIC CAUSES OF FAILURE

1. Remove the top and front covers from the VS-300 cabinet. (Refer to paragraph 5.3.2.1)
2. Remove the shipping protector from the SCU floppy diskette drive.
3. Inspect the interior of the mainframe for packing material or such shipping damage as broken connectors and loose fastening hardware.
4. Refer to the shipping list to make sure that the correct circuit boards have been shipped.
5. Make sure all circuit boards are properly seated in the backplane.
6. Carefully inspect the backplane and the power supply and Support Control Unit (SCU) fans for obvious damage.
7. Inspect the power supply assemblies for damage and loose connections. At this time, make sure that all power supply connections are tight.
8. If necessary, vacuum clean the unit.
9. Do not reassemble the mainframe at this time.
10. If damage is discovered at any time during the inspection, follow the reporting procedure in paragraph 4.5.1

4.6.1 PERIPHERAL INSPECTION

After inspecting the mainframe, carefully inspect each peripheral according to procedures outlined in the applicable maintenance manuals. If damage is discovered at any time during the peripheral inspection, follow the reporting procedure in paragraph 4.5.1.

4.7 SOFTWARE/DIAGNOSTIC REQUIREMENTS

4.7.1 SOFTWARE

Table 4-2. Minimum Software Requirements

Software	Version	Comments	WLI P/N
VS-300 SCU	1.02.00	Has CP8 CPU ucode & DCS package	195-4682-9
	1.03.XX	" " " " " " " (Includes FPU ucode)	195-XXXX-X
Operating System	7.06.46		195-4681-7

NOTE

Use of SCU Software versions 1.03.XX and above requires installation of FCO #1189, Real Time Clock function reliability.

4.7.2 DIAGNOSTICS

Table 4-3. Built-In Test (BIT) Programs

Diagnostic Name	PROM Rev.	Package P/N
928 Serial IOC	5560	195-4721-D
SMD Disk IOC	5570	195-4724-D
Kennedy Tape IOC	5560	195-4730-D
Telex Tape IOC	5560	195-4731-D
Multiline TC IOC	5590	195-4729-D

Table 4-4. Other Diagnostics

Diagnostic Name	Version	Package P/N
Uniboot (Boot Loader)	846C	195-2479-3
FTU Off-line	6385	195-2759-3
VOLCOPY	8181	702-0122-A

NOTES

1. Complete 195 package part numbers include diskette and documentation.
2. Diskette only part numbers (702) are shown if no package part numbers are available.

4.8 MAINFRAME POWER SOURCE CHECK

4.8.1 208-240VAC DOMESTIC POWER SOURCE

There are two options for VS-300 input power service; using existing VS-100 service or installing a new service. Both are discussed below. Before completing the mainframe reassembly and peripheral equipment installation, use a Digital Voltmeter (DMV) to check the mainframe power source receptacle for proper wiring and service as shown in figures 4-8 and 4-9, and table 4-5. Make sure that the receptacle meets all specified requirements before proceeding with the installation.

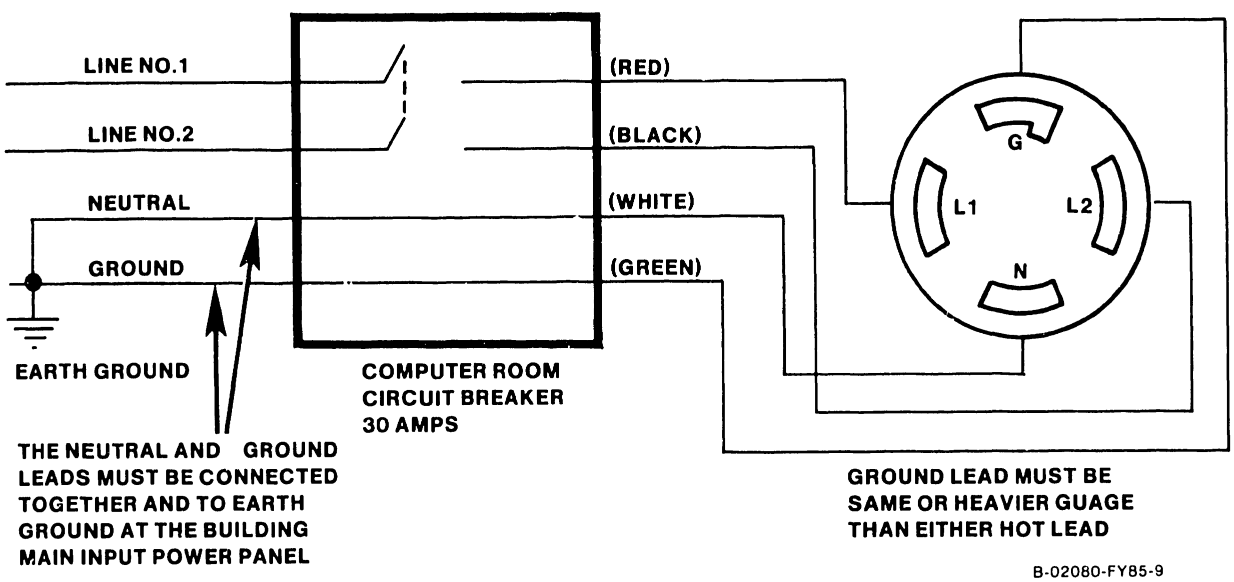
CAUTION

Failure to verify the input power service can result in serious damage to mainframe circuits and to connected peripherals.

4.8.1.1 Using Existing VS-100 Power Service

NOTE

Even though ac neutral is not used in domestic VS-300 mainframes, previously properly installed VS-100 mainframe power service can be used without modifications.



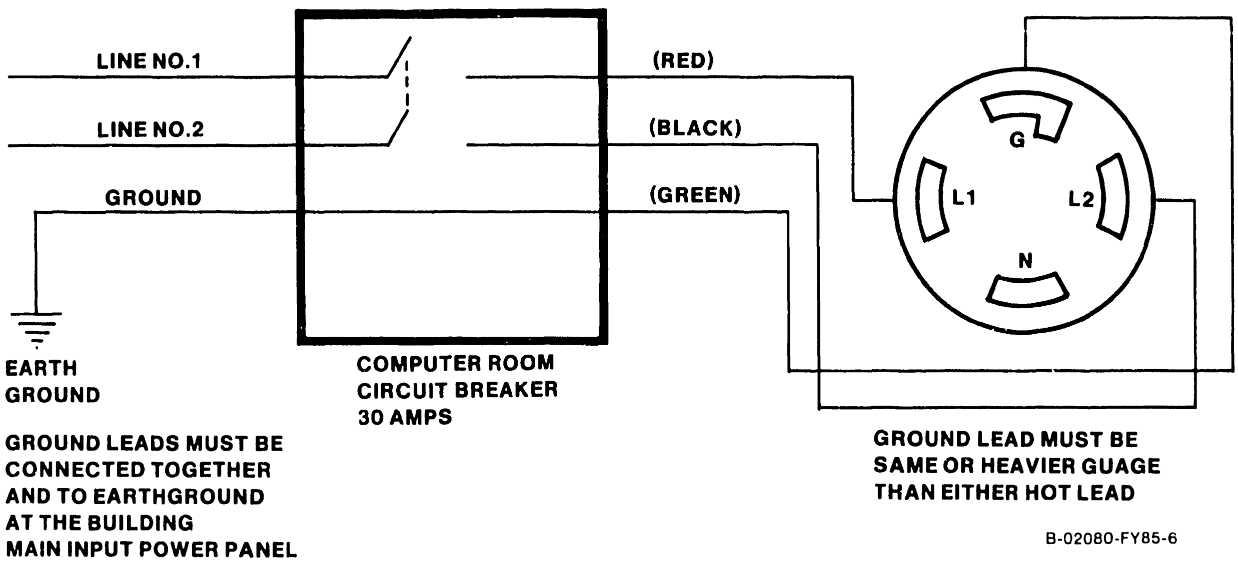
	RECEPTACLE BODY	MATCHING CONNECTOR
NEMA Configuration	L14-30R	L14-30P
Hubbel Part Number	2710	2711

Figure 4-8. 208-240 Volt AC Power Source Requirements for VS-300 Mainframes Using Existing VS-100 Power Service.

4.8.1.2 Installing New Power Service For VS-300s

NOTE

New power service for VS-300s can be installed as shown in either figure 4-8 or 4-9, whichever is more convenient. However, if the service shown in figure 4-9 (without a neutral line) is installed, it cannot be reused for a VS-100 mainframe.



	RECEPTACLE BODY	MATCHING CONNECTOR
NEMA Configuration	L14-30R	L14-30P
Hubbel Part Number	2710	2711

Figure 4-9. 208-240 Volt AC Power Source Requirements for New Power Service For VS-300 Mainframes.

Table 4-5. DVM Voltage Measurements 208-240VAC Receptacle

Measure From	Acceptable DMV Readings
Ac Hot (L1) to Ground	120 V ac (+/- 10%)
Ac Hot (L2) to Ground	120 V ac (+/- 10%)
Ac Hot (L1) to Ac Hot (L2)	208-240 V ac (+/-10%)

4.8.2 INITIAL MAINFRAME POWER-UP

1. After making sure that the ac On/Off circuit breaker is OFF, plug the mainframe power connector into the power source receptacle.

2. Perform the following:

   a. Turn ON the mainframe ac On/Off circuit breaker.

4.8.3 DC VOLTAGE CHECKS

4.8.3.1 Power Supply Adjustments

1. Remove the left front panel (paragraph 5.3.2.2)

2. Remove the screws from the rear fan panel, disconnect the two fans and set aside the panel.

3. Press the Control Panel On button or SW1 (On) on the Power Supply Controller. Make sure the On lamp on the Control Panel and the voltage sensing LEDs 1 → 5 on the Power Supply Controller are lit. If the LEDs are not lit or go out after a few seconds, there is a problem with either of the power supplies, or the Power Supply Controller board. No adjustments can be done until the problem is corrected. Do the following:

   a. Remove the 4-pin connector from either J5 (multioutput power supply control) or J4 (booster power supply control) of the Power Supply Controller board. (Figure 4-12.)

   WARNING

   Inserting the test jumper as described in step b (below) will immediately turn on the switching power supplies if the ac On/Off circuit breaker is on.

   b. Insert the Power Supply Test Plug (WLI P/N 220-2342) into P5 (cable to the multioutput p/s) or P4 (cable to the booster p/s).

   c. If the power supply comes up and stays up, the power supply is good. (Refer to Chapter 7 for troubleshooting procedures for the 210-8709 Power Supply Controller board.) If the power supply still does not come up, replace the supply. (Paragraph 5.3.2.22 or 5.3.2.24.)

   d. Disconnect the test jumper and reconnect the cable to J4 or J5 on the Power Supply Controller.

4. The following power supply voltages should be measured at the test points on the Power Supply Controller. Adjust the voltages to the readings listed below using the potentiometers on the front of the particular switching power supply at the rear of the mainframe (figures 4-10 and 4-11).

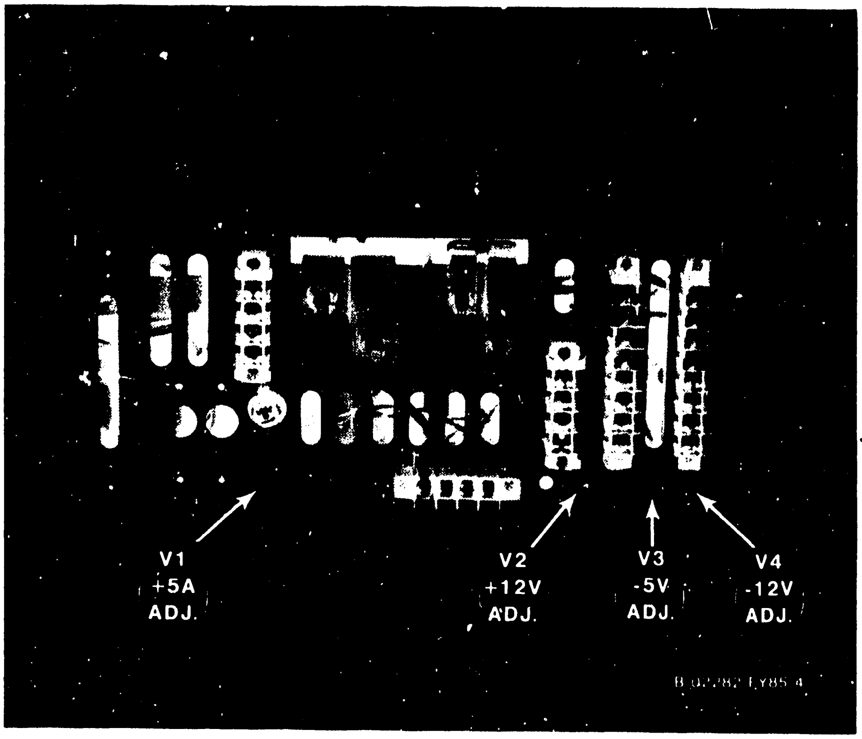


Figure 4-10. Multioutput Power Supply

PHOTO NOT AVAILABLE

Figure 4-11. Booster Power Supply

Table 4-6. Power Supply Voltage Measurements

Test Point	Adjust (P/S)	Volts	Minimum	Maximum	AC Ripple Limits
TP+5VA	V1 (P/S 1)	+5.0A	+4.96	+5.04	35mV RMS or 50mV Pk-to-Pk
TP+5VB	5V (P/S 2)	+5.0B	+4.96	+5.04	35mV RMS or 50mV Pk-to-Pk
TP+12V	V2 (P/S 1)	+12.0	+11.96	+12.04	35mV RMS or 50mV Pk-to-Pk
TP-5V	V3 (P/S 1)	-5.0	-4.96	-5.04	35mV RMS or 50mV Pk-to-Pk
TP-12V	V4 (P/S 1)	-12.0	-11.96	-12.04	35mV RMS or 50mV Pk-to-Pk
TPGROUND		+/-0	+/-0	+/-0	

NOTE

1. P/S 1 is the multioutput supply.
2 P/S 2 is the booster supply.
3. It is better to have the +5 V adjusted more toward the maximum than toward the minimum.

4.8.3.2 Power Supply Controller Adjustments

1. On the Power Supply Controller board (figure 4-12), measure/adjust the calibration voltages at:

   a. TP 8 for 8 volts. On Rev. 0 boards, adjust R11. (There is no TP 8 or adjustment on Rev. 1 boards.)

   b. TP 2.5 for 2.5 volts. On Rev. 0 boards, adjust R12. (There is no TP 2.5 or adjustment on Rev. 1 boards.)

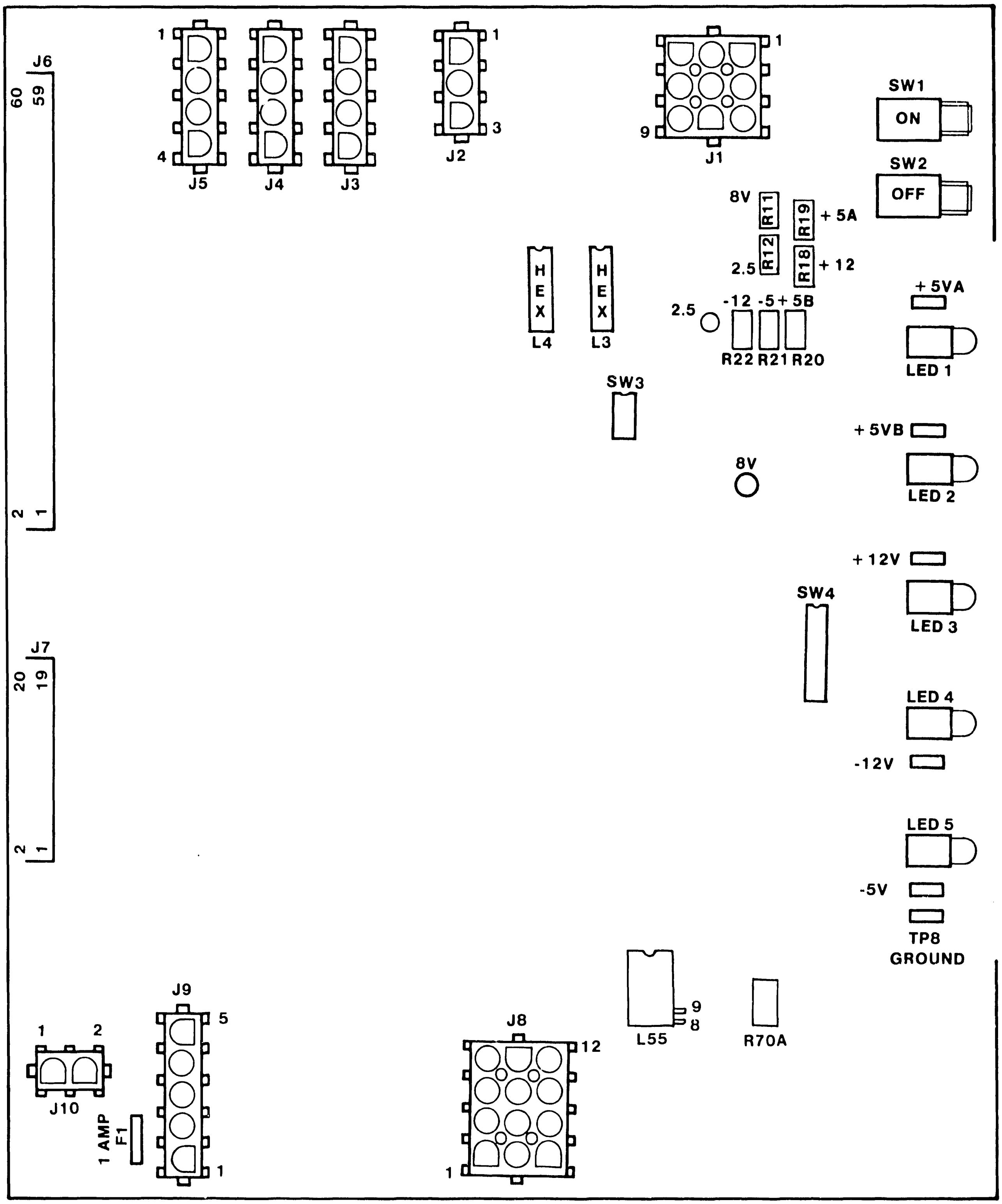
2. Set the 4-bit Voltage Address switch SW3 (table 4-7) on the Power Supply Controller board to the A/D input be adjusted.

Table 4-7. DC Voltage Address Switch SW3 Settings

Voltage	Bit 1	Bit 2	Bit 3	Bit 4
-5.0	On	Off	Off	X
-12.0	Off	On	Off	X
+12.0	On	On	Off	X
+5.0B	Off	Off	On	X
+5.0A	On	Off	On	X

NOTES

1. X = don't care (position 4 not used)



B-02080-FY85-14

Figure 4-12. Power Supply Controller Board. (Rev. 0 Version)

3. Look at the two hex displays on the Power Supply Controller board. Using the potentiometers on the Power Supply Controller board, adjust the A/D outputs to the hex display values as shown in table 4-8. Change the Voltage Address switch for each voltage to be measured/-adjusted.

Table 4-8. A/D Output Values At Hex Displays

Voltage	Adjust	Minimum Hex Value	Exact Hex Value	Maximum Hex Value
-5.0	R21	7E	80	82
-12.0	R22	7E	80	82
+12.0	R18	7E	80	82
+5.0B	R20	7E	80	82
+5.0A	R19	7E	80	82

4. From the SCU DCS Test Selection Menu, select the VS XXX Environment.

```
mm/dd/yy            Wang VS Diagnostic Control System            hh/mm/ss
                          prerelease 5.03.14p
                          □□□□ □□□□ □□□□ □□□□

  Sequence: 1                                              Error Cnt: 0
Diagnostic: R1530 VSXXX Environment
      Test: Display

| DCS Status: Diagnostic Executing                                        |

Voltage Readings = +5.000  +5.000  -5.000  +12.00  -12.00  Air Flow = 01

SCU Control Registers = 4700 ACFF                 SCU Registers = C804 5000

CPU SCR = 4400      FPU SCR = EEEE      MCU SCR = 0000      SBI SCR = 0000

Control Panel Key switch is set to NORMAL

System Reset has been pressed

AC power has been cycled
```

Figure 4-13. Environment Test Screen

5. Look at the Environment Test Screen on the Support Control Unit (SCU) screen. (Figure 4-13.) The voltages shown in table 4-9 will appear on the screen.

NOTE

Do not use the Environment Test Screen on the SCU to adjust the voltages. It is strictly a monitor and will not respond quickly enough to do a reliable voltage adjustment. Adjust the A/D outputs while viewing the hex display.

Table 4-9. DC Voltages On SCU Screen

Voltage	Minimum	Maximum
+5.0(A)	+4.96	+5.04
+5.0(B)	+4.96	+5.04
-5.0	-4.96	-5.04
+12.0	+11.96	+12.04
-12.0	-11.96	-12.04

4.9 IPL PROCEDURES

If the voltage checks are correct, the system can be IPLed. If the system fails to IPL, the software may have to be installed on the SCU. Refer to paragraph 4.9.2. Make sure that the following have been connected to the system.

1. The SCU must be connected to J9 and J10 of the rear panel labeled "Cable Concentrator". J9 and J10 connect to Port 0 of the APA panel for the first SIO IOC. (Figures 4-22 and 4-24.)

2. The "B" cable of the system disk is attached to the top left "B" cable connector, labeled "0", of the disk connector assembly in the rear panel for the first disk IOC. (Figure 4-26.) The "B" cable from this connector assembly must be connected to J4 of the 23V98 Disk IOC in card cage slot 17.

4.9.1 IPLING THE VS-300

Follow this procedure to perform an IPL.

1. Make sure the Front Panel key switch is in Normal Control position.

2. Power up the system disk drive.

3. Press the System Reset pushbutton and then press the Operator Console Reset pushbutton.

4. After a pause, the SCU start-up sequence is invoked and start-up messages appear on the SCU screen:

   "WANG SUPPORT CONTROL UNIT REV. X.XX"
   "01 Start From Winchester"

5. Followed by:

   "Wang Support Control Unit - BIOS X.XX"
   "MS-DOS Version X.XX"

```
                SYSCON X.X.X

   Copyright Wang Laboratories, Inc. 1985
```

6. The Console Processor screen then appears.

```
                  <<< System in Control Mode >>>

                  *** Wang VS System Console ***

   SYSCON Version X.XX        11:06 AM          Monday, January 6, 1986

          Press (HELP) for online system console information.


               Use the function keys to select a command:

      (1) ENTER Workstation Emulation    (8)  RESET System
      (2) ENTER Control Mode             (9)  RESET Console


                                         (12) SET Console Defaults
      (5) AUTO IPL                       (13) SET Time and Date
```

Figure 4-14. Console Processor Screen

NOTE

The functions that the key switch allows in any one of the four key switch positions are highlighted on the Console Processor screen.

Certain elements of the System Console Menu are password-protected to prevent unauthorized use of some SYSCON facilities. These elements are not immediately displayed.

7. If it is necessary to load any SCU software, do step 7. If no software is to be loaded, go to step 8.

   a. Place the Front Panel key switch in the "Remote Service" position.

   b. Type in the following password:

      CSG, plus the current four digit time as displayed on the System Console screen. Example: If time is 9:30 (am or pm), enter 0930.

NOTE

The password will not appear on the screen. Also, while entering the password, the keyboard beeper will sound as each key is pressed. This is normal. It is intended to keep unauthorized personnel from enabling the full System Console menu.

   c. A modified Console Processor screen in service mode, figure 4-14a, will appear.

```
                  *** WANG VS System Console ***

SYSCON Version X.X.X          2:44 PM       Monday  February 11, 1986

          Press (HELP) for on-line system console information.

               Use the function keys to select a command:

 (1) ENTER Workstation Emulation          (8) RESET System
 (2) ENTER Control Mode                   (9) RESET Console
 (3) ENTER Service Log Mode              (10) Terminate Service Mode
 (4) ENTER Off-line Diagnostics          (11) Show Error Log
                                         (12) SET Console Defaults
 (5) AUTO IPL                            (13) Set Time and Date
(29) Install Software                    (32) Wang PC Emulation
```

Figure 4-14a. Modified System Console Screen in Service Mode

d. Insert the diskette to be loaded in the diskette drive and close the door.

e. Press PF29 (Shift + Command), for Install Software. The diskette will begin loading onto the SCU disk drive.

f. Upon a successful load, a "Diskette installed" message will appear and the system will return to the modified Console Processor screen in service mode.

g. If no more software is to be loaded, press PF10, Terminate Service Mode, and return the key switch to the "Normal Control".

8. a. Press PF5 (AUTO IPL). This message appears:

"WARNING: This function resets the system, RETURN to proceed or PF16 to abort"

b. Press RETURN. (If the console defaults need modifying, or if the CPU code has not been loaded, a CPU or IPL error may appear. Go to step 9. If there are no changes necessary, or no CPU or IPL errors appear, go to step 10.)

9. a. Press PF12 (SET Console Defaults). The System Console Default screen appears.

```
                    <<< System in Control Mode >>>

                    *** System Console Defaults ***


IPL Device Address: R 0100

CPU Microcode File: /SCU/OBJVSE.CP8
FPU Microcode File:

WS Emulator Options: -PC

Give Console Date/Time to VSOS: N
Warning message before a reset: Y


(9) Modify Defaults     (10) Load System Microcode              (16) Exit
```

Figure 4-15. System Console Default Screen

1) If defaults are incorrect, press PF9 (Modify Defaults), make corrections as shown in figure 4-15, press RETURN, and/or:

2) Whether defaults were corrected or not, press PF10 (Load System Microcode).

b. Press PF16 (Exit). and the Console Processor screen (figure 4-14) reappears.

c. Press PF5 (AUTO IPL). This message appears:

"WARNING: This function resets the system, RETURN to proceed or PF16 to abort"

d. Press RETURN.

10. The Workstation Initialization Screen, figure 4-16, appears.

```
                    Wang
                     VS
           Workstation Emulation
               Version X.XX


   Initialization in Progress - Please Wait
```

Figure 4-16. Workstation Initialization Screen

11. The SYSGEN Configuration Screen (figure 4-17) appears.

```
***MESSAGE M001 BY SYSGEN

                    INFORMATION REQUIRED BY PROGRAM

                     ACTIVE SUBPROGRAM IS @SYSGEN@

   Specify the name of the system configuration file and press (ENTER)
                                 -or-
          Press (1) to use one workstation and one disk.

                         SYSFILE = @CONFIG@
                         SYSLIB  = @SYSTEM@

    Specify the communications configuration file to be use, if any

                        COMMFILE = ********
                        COMMLIB  = @SYSTEM@

Inhibit logons at all workstations?                  LOGONS = NO■

Load Micro Code to all devices?                      LMCODE = NO■

Inhibit dumping continuable halts?                   CMDUMP = NO■
```

Figure 4-17. SYSGEN Configuration File Screen

NOTE

If the IPL was unsuccessful and an "IPL failed" message is received, refer to paragraph 4.9.3, IPL Errors

12. a. On the SYSGEN Configuration File screen, enter the names of the configuration files and the system library to be used. The field for the communications configuration file is blank. Fill in the communications configuration file field only if communications are going to be used. To change one of these values, move the cursor to the appropriate field and enter in the new information. Then, press RETURN.

NOTE

If the system is being IPLed for the first time, the default values of @CONFIG@ and @SYSTEM@ are used for the configuration file and system library, respectively. After IPLing for the first time, configuration files can be created using GENEDIT. Refer to the VS Software Bulletin Release 7.06.

b. After the values have been entered, the VS-300 stores them in a start-up file. At the next IPL, the system displays the stored values and allows them to be changed.

c. The prompt "Inhibit logons at all workstations?" allows workstation logons to be inhibited. If "YES" is entered, only the SCU user can log on. The default value is "NO", which allows logons at all workstations, which were enabled before this IPL.

d. The prompt "Load Micro Code to all devices" lets microcode be loaded to each workstation (including remote workstations) as part of the IPL procedure. If "Yes" is entered, microcode is loaded to each workstation and the IPL process is significantly slower. This option is used when a workstation is hung up or when the workstation configuration has been changed. The default value is "No".

e. The prompt "Inhibit dumping continuable halts" allows disabling of the Continuable Dump for errors that do not require reIPL. If "Yes" is entered, Continuable Dumps which do not reIPL the system are not performed and system processing continues with the system error in effect. If "No" is entered, all Continuable Dumps occur. The default value is No. Refer to Chapter 7 for more information on the Continuable Dump.

13. Press RETURN when finished with the SYSGEN Configuration File screen. (Or,to bring up a minimum configuration of one workstation [W/S0] and one disk, without changing the default values, just press PF1.)

NOTE

The IPL procedure automatically activates any remote workstations that have been configured via the remote workstation parameters in the GENEDIT procedure.

14. After pressing RETURN from the SYSGEN Configuration File screen, the VS-300 checks to determine if any of the critical operating system components are obsolete or incompatible. If no problems are detected, the IPL continues and the message "System Generation in Progress" appears on the SCU.

a. If incompatibilities exist that can cause problems, the IPL is stopped and a warning message is displayed.

15. The message "I/O Subsystem Load in Progress" appears on the SCU screen.

16. a. If the SCU real time clock is not usable, the date and time screen appears. Enter the correct date and time, and press RETURN.

    b. This screen also allows changing the amount of memory available for use. The default value is the total amount of physical memory for the system. To change the value, move the cursor to the field, enter the new value, and press RETURN.

17. The message "System Initialization in Progress" appears on the SCU screen.

The VS-300 is now initialized and ready for operation. VS workstation emulation is running on the SCU and the Operator's screen is displayed. To log on from the SCU;

1. Press PF1 and the VS Logon screen appears.

2. Enter the User ID and Password. (As this is the first time that the system has been IPLed and logged onto, use "CSG" for the User ID and leave the Password field blank.)

3. Press RETURN. The User screen is displayed.

Usually, the SCU is Workstation 0; while workstation emulation is running, perform all Workstation 0 tasks from the SCU. See Chapter 3 of the VS-300 Processor Handbook for information on running the SCU; see Chapter 4 for procedures for running Operator's tasks.

Once workstation emulation is running on the SCU, it is interrupted when one of several conditions occur. When workstation emulation is suspended, Workstation 0 functions are maintained by the SCU; however, they are not displayed on the screen. The conditions interrupting workstation emulation are:

1. Exiting workstation emulation (press CONTROL, then press SHIFT and CANCEL simultaneously, then select Suspend Emulation and press EXEC). (Returns to figure 4-14, the Console Processor Screen.)

2. The VS-300 enters Control mode automatically.

If a system element, such as an IOC, fails, the VS-300 does not automatically enter Control mode. Rather, it displays the problem on the screen and continues operation.

After Control mode is manually invoked and then exited, workstation emulation has to be selected from the Console Mode menu to reenter Operator's mode.

4.9.2 1.03 SCU SOFTWARE INSTALLATION

The SCU and SCU Installation utility software are stored on the floppy diskettes that are auto-enclosed with the VS-300. Generally, SCU software need only be installed if the system failed to IPL, or if the SCU fixed drive (the SCU Winchester) is damaged (e.g., during a power outage).

1. If the system is not already powered up:

   a. Make sure that the key switch on the Control Panel is turned to the Normal Control position.

   b. Power up the mainframe and W/S 0 (SCU) by pressing the Power On pushbutton on the Control Panel. Don't power on external disk drives.

2. If the system is already powered up, enter Control Mode, power off any external disk drives, and exit Control Mode. Then, press the Operator Console Reset pushbutton.

3. Watch the SCU keyboard. As soon as the keyboard lights go out and the beep signal sounds, press the HELP key.

4. When the Options menu appears on the SCU screen:

   a. Insert the Install diskette in the diskette drive and close the door.

   b. Press D. (Re-direct Start)

   c. Press A.

   d. Press Return.

5. The start-up message appears on the SCU screen:

   "01 Start From Drive A"

6. Followed by:

   "Wang Support Control Unit - BIOS X.XX"
   "MS-DOS Version X.XX"
   "Loading Menu"

7. The SCU Install Utility menu appears. (See figure 4-18.)

```
mm/dd/yy               Wang Laboratories, Inc.           hh:mm:ss
                  Support Control Unit Install Utility
                           Version XX.XX.XX

Select an Item and Proceed

                           ■ Analyze Winchester Disk
                           _ Format Winchester Disk
                           _ Realign and Format Winchester
                           _ Install SCU Software

                                    SPACE BAR - Item Select
                                    EXECUTE   - Proceed
                                    CANCEL    - Previous Menu
```

Figure 4-18. SCU Install Utility Menu

This menu presents four choices:

a. Analyze Winchester Disk - This utility checks the Winchester disk; it corrects inconsistencies in the File Allocation Table (FAT) and reports the number of extents.

b. Format Winchester Disk - This utility erases all existing files and prepares the Winchester to accept new files. It takes about 6 minutes.

c. Realign and Format Winchester - This utility does a complete reformatting of the Winchester, including several passes across the disk to erase current files and file information. It takes about 1 hour and 40 minutes to complete.

d. Install SCU software - This utility loads the SCU software onto the Winchester.

8. a. Press the space bar (or press "F") to select Format Winchester Disk. (Formatting takes about six minutes.)

   b. Press EXEC. The following message appears on the screen:

   "Format version X.X.XX"
   "Type 'Winchester' to begin formatting C:"

   c. Enter Winchester and press RETURN. The following messages appear on the screen during formatting:

   "Formatting..."
   "Writing Winchester"
   "Building Winchester FAT table..."

d. When formatting is complete, this request appears on the screen:

"Volume label (11 characters, RETURN for none)?"

Either label the volume or press RETURN for no label.

e. The following message appears on the screen:

"Format Completed..."
"_______ bytes total disk space"
"_______ bytes available on disk"

f. Figure 4-18, the SCU Install Utility Menu, reappears.

9. Select the Install SCU Software option from the Support Control Unit Install Utility menu and press EXEC. The "Setting Up Winchester" message appears, followed by the SCU Install Utility screen, figure 4-19.

```
                    Wang Laboratories Inc.
              Support Control Unit Install Utility
                       Version XX.XX.XX


      Please insert floppy to be installed.
      SCU must be Re-booted after last disk is installed.
      (i.e. push the blue pushbutton)


      Strike a key when ready . . .
```

Figure 4-19. SCU Install Utility Screen

10. Remove the Install diskette from the diskette drive. Insert any one of the other SCU software diskettes in the diskette drive. It does not matter which one is used first, or if the same diskette is accidentally inserted twice. Close the diskette drive door.

NOTE

Once the Install has been used to start up the Install utility, do not copy it. If it is accidentally copied, terminate the Install utility (step 15) and repeat the installation procedure.

11. Press any key to initiate the installation. The message "Copying ......" with the list of files as they are being copied appear on the screen.

    a. If this error message appears:

       "Not ready reading drive A
       Abort, Retry, Ignore?"

       1). Check the arrows on the diskette to make sure that the diskette has been inserted properly in the drive.

       2). Make sure that the diskette door is completely closed.

       3). Restart the Install utility by pressing "R".

    b. If this error message appears:

       "Write protect error writing drive A
       Abort, Retry, Ignore?"

       1). Remove the diskette from the drive, remove the write-protect tab, and insert the diskette into the drive. Close the door.

       2). Restart the Install utility by pressing "R".

12. After the files from the diskette are copied to the Winchester, the following message appears:

    "Disk installed.
    Please remove floppy from drive.
    Strike a key when ready."

13. Remove the diskette from the drive and press any key. The Install utility screen, figure 4-19, reappears. Insert another diskette and press any key. Repeat this step until the files from all the diskettes have been copied.

14. After the files from the last diskette have been copied, remove any diskette from the diskette drive and leave the diskette drive door open. Terminate the Install utility.

15. Press the Operator Console Reset pushbutton on the Control Panel. The SCU start-up messages appear, followed by the Command Processor screen.

4.9.3 IPL ERRORS

There are four major errors that can be encountered in an unsuccessful IPL. Table 4-10 lists the errors and the action necessary to correct them.

Table 4-10. IPL Errors

Error	Description	What To Do
IPL Failed, No SQB (Status Qualifier) Byte) received from IOC	The request to the IOC was made, but not acknowledged.	Check the second digit of the 4-digit hexadecimal IPL device number; it may reference an invalid IOC. Change the number and re-IPL. Press System Reset pushbutton.
IPL failed, no interrupt received from IOC	This indicates a system bus problem.	Check all four digits of the hexadecimal IPL device number to see if the number is valid. Change the number and reIPL. Press the System Reset pushbutton.
IPL failed, invalid SQB (Status Qualifier Byte)	The IOC may be experiencing a a problem.	IPL from another device; change the 4-digit hexadecimal IPL device number for the new device and reIPL. Press the System Reset pushbutton.
IPL failed: Intervention required.	The IPL drive is not powered on, the disk be damaged, or the drive may be defective.	Power on the drive, change the disk, or change the IPL drive. If changing the IPL drive, change the 4-digit hexadecimal IPL device number. ReIPL the system. Press the System Reset pushbutton.

4.9.4 VERSION CHECKING DURING IPL

If any operating system component cannot be found or has no version number or too low a version number, the system displays the Version Warning screen (figure 4-20) on the SCU.

The Version Warning screen lists all the operating system and bus processor components checked, up to and including the component that causes the "Fatal Error" message to appear on the screen. The sample Version Warning screen (figure 4-20) lists the entire set of operating system and bus processor components to be checked. The entry for any component causing a version number problem is blinking. The current version of the NUCLEUS file is listed at the top of the screen. This screen also lists component information, such as component name, the minimal (oldest) version that will run with the current NUCLEUS file, and the current version number for that component and its status.

```
                              WARNING

Some components of the WANG VS OPERATING SYSTEM could not be identified
as the latest versions for the current NUCLEUS file (rel X.XX.XX)


Component       Minimal Version     Current Version     Status

@SYSGEN@        07.06.02            07.06.03
@SYSSVC@        07.06.06            07.06.06
@SYSTSK@        07.06.06            06.30.57            FATAL ERROR
@TSKMGR@        07.06.03            07.06.03
@OPER@          07.06.05            07.06.05
@SYSCPR@        07.06.02            07.06.02
@SHARER@        07.06.03            07.06.03
@PRTTSK@        07.06.02            07.06.02
@MCBP@          07.06.03            07.06.03
DEVLST          07.06.30            07.06.25            WARNING

                  You may continue by pressing ENTER
```

Figure 4-20. Sample Version Warning Screen

The Status field located on the Version Warning screen indicates a status error message if the component is in error. The status error messages are listed in table 4-11.

Table 4-11. Version Checking Status Error Messages

Message	Definition	Components
(blank)	No problems are detected.	
WARNING	A version problem exists with this component, though it is not critical enough to halt system initialization.	@PRTTSK@ @SHARER@ DEVLIST
FATAL ERROR	IPL procedures cannot continue. Obtain a current, compatible version of the component and then reIPL.	@SYSGEN@ @SYSTSK@ @OPER@ @SYSCPR@ @TSKMGR@

If the VS-300 cannot determine a component's version number, the Current Version field displays UNKNOWN as the version number. This error usually occurs if the file does not exist. If no fatal problems exist (i.e., "NonFatal Error"), continue the IPL procedure by pressing RETURN. If, when pressing RETURN, there is a "Fatal Error", the VS-300 enters Control mode.

If the system detects a version number problem with the @SYSSVC@ component, it may not display the Version Warning screen and it may enter Control mode. Depending on the version numbers of @SYS000@ and @SYSSVC@, the following message is displayed on the workstation screen:

CURRENT @SYS000@ CANNOT SUPPORT CURRENT @SYSSVC@

When the system enters Control mode, the Control Mode Dump procedure may have to be performed, as described in Chapter 7.

4.10 PERIPHERAL INTERCONNECTION

After the system has been IPLed and GENEDIT has been run, power down the mainframe and connect all peripheral devices according to the configuration created during GENEDIT. See figures 4-21 through 4-30, the following paragraphs, and appropriate documents for cabling procedures.

PANEL #					PANEL #
1	OPTIONAL	(e)	OPTIONAL	(e)	11
2	OPTIONAL	(e)	OPTIONAL	(e)	12
3	OPTIONAL	(e)	OPTIONAL	(e)	13
4	OPTIONAL	(e)	OPTIONAL	(e)	14
5	WS24 SIOC1	(a)	CIU	(c)	15
6	WS16 SIOC1	(a)	OPTIONAL	(e)	16
7	WS8 SIOC1	(a)	OPTIONAL	(e)	17
8	WS0 SIOC1	(a)	OPTIONAL	(e)	18
9	BLANK	(f)	DIOC1	(b)	19
10	BLANK	(f)	PERIPHERAL BAND	(d)	20

Figure 4-21. VS-300 I/O Panel Basic Positions

NOTES

a. Panel position 8 reserved for W/SO. Panel positions 5 through 7 used for remaining daisy chained Active Port Assembly (APAs) on first SIOC. Cable Concentrator(s) (CC) configured with next eight SIO panels (second & third SIOCs) for total of 64 ports per CC. CCs will be shipped with all cables necessary to fully populate the CC. Additional SIO panels, over the 64-port mainframe limit, will require additional CCs be ordered.

b. Panel position 19 allocated to first 4-port disk IOC panel.

c. Panel position 15 allocated for Cable Interface Unit (CIU) modem & CAB (Contention Access Board).

d. Panel position 20 allocated for WangNet Peripheral Band (P-Band) modem, if physically possible.

e. Remaining panel positions may be used for remaining disk, tape, SIO IOC panels, and WangNet P-Band modems. MLTC panels should be mounted on the right side only.

f. Panel positions 9 & 10 will normally be blank panels. This will permit access to the +5V(B) booster power supply for adjustment or replacement.

4.10.1 I/O CONNECTOR ASSEMBLY TO IOC CABLING

Before installing cables in the connector assemblies at the rear of the mainframe, check all cables between the assemblies and associated IOCs. The SCU must be connected to J9 and J10 of the rear panel labeled "Cable Concentrator". J9 and J10 connect to Port 0 of the APA panel for the first SIO IOC.

Make sure that the "B" cable of the system disk is attached to the top left "B" cable connector, labeled "0", of the disk connector assembly in the rear panel for the first disk IOC. The "B" cable from this connector assembly must be connected to J4 of the 23V98 Disk IOC in card cage slot 17.

4.10.2 SERIAL CONNECTORS

Serial I/O devices (workstations, printers, etc.) connect to the mainframe by means of standard BNC/TNC connectors mounted on 16-connector (8-port) Active Port Assembly (APA), WLI P/N 270-0975. Maximum cable length for these devices is 2000 feet. The APAs connect to J2 of the 23V97 Serial IOCs through a 34-pin ribbon cable. Four APAs are supported by each 23V97 IOC. See figure 4-22.

The APAs can also be mounted in the free standing Cable Concentrator unit.

The 23V97 IOC also supports the 6550 Gate Array TC controller (paragraph 4.10.5), and the existing WangNet P-Band 19-channel Global modem and the new 28-channel Global modem (paragraph 4.10.8). Connector J1 on the IOC is always reserved for P-Band. No other type of devices should be connected to J1.

The 6550 Gate Array TC controller, and the WangNet P-Band Global modems can also be housed in the Cable Concentrator unit. (See figures 4-23, 4-24 and 4-25.)

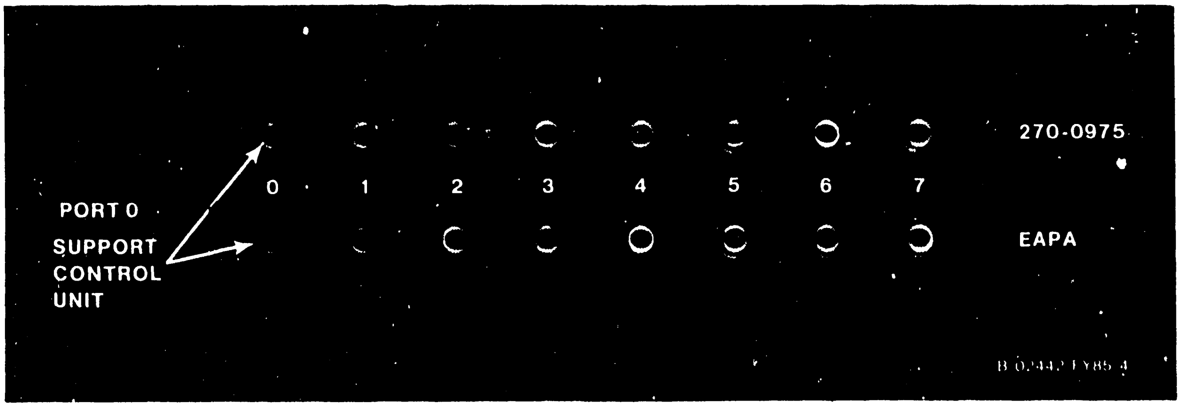


Figure 4-22. First Active Port Assembly BNC/TNC Connector Assembly

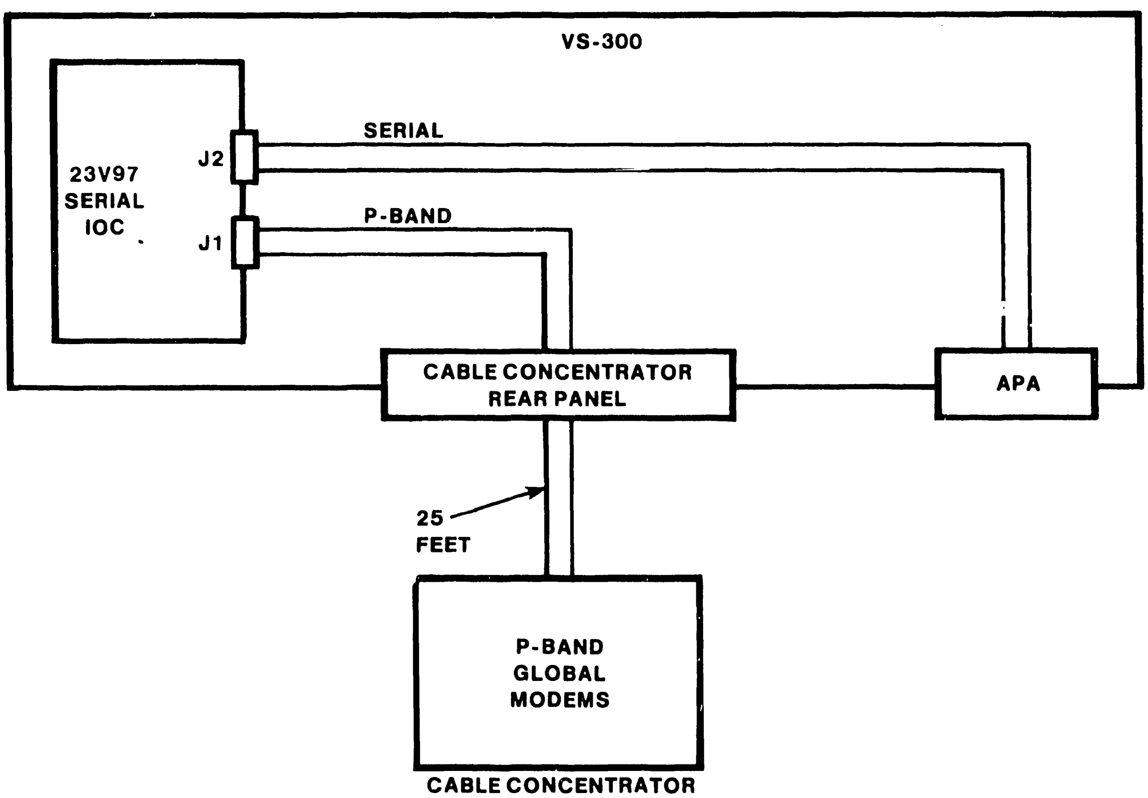


Figure 4-23. P-Band Modem Connections

4.10.3 CABLE CONCENTRATOR

The Cable Concentrator is a free standing unit used to house APA and Gate Array TC connector panels, and WangNet P-Band modems.

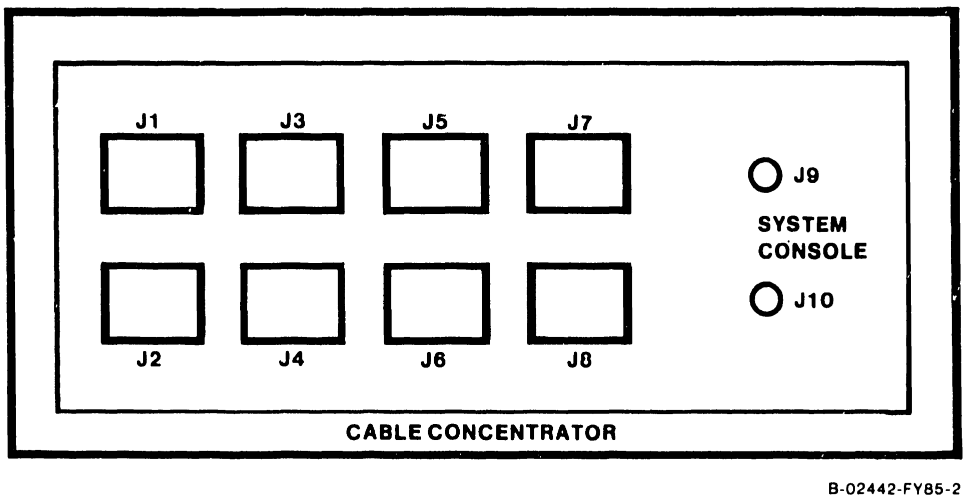


Figure 4-24. VS-300 Cable Concentrator Rear Panel

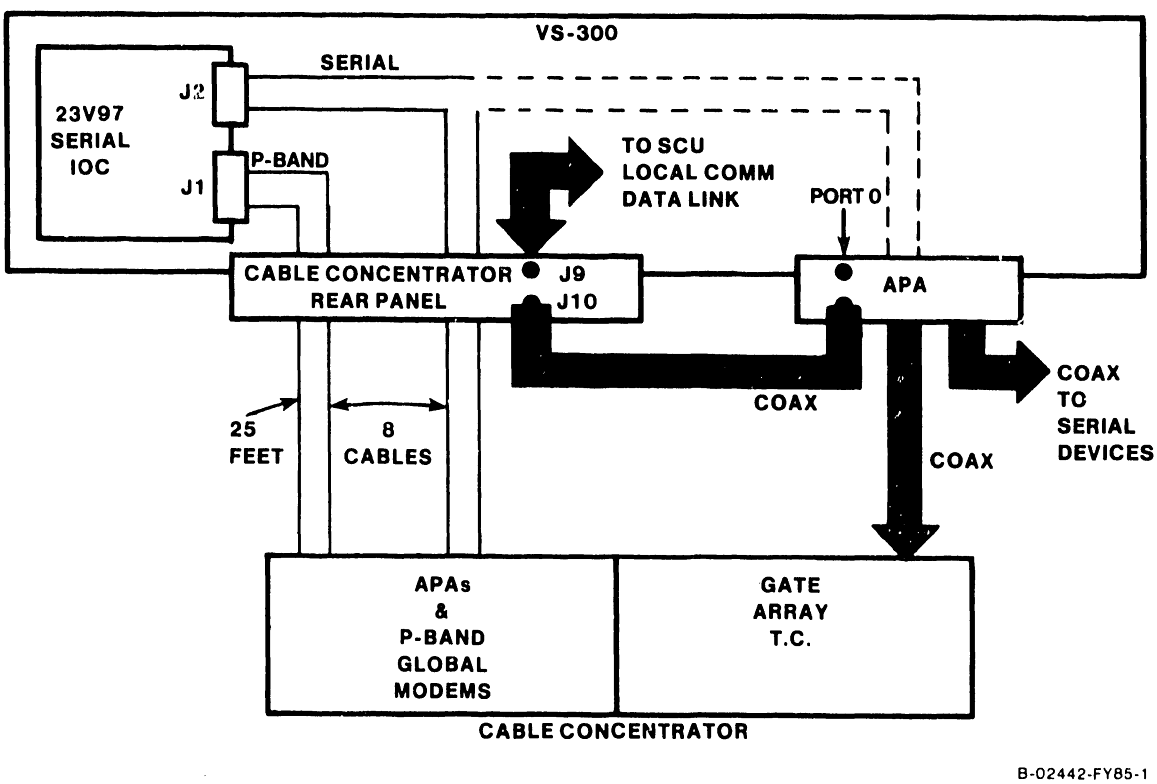


Figure 4-25. Cable Concentrator Connections

4.10.4 DISK CABLE CONNECTORS

Two types of disk cable connectors are located on the disk connector assembly, WLI P/N 270-1006. The four narrow connectors are 26-pin sockets for the "B" cable connections; the wide connector is a 60-pin socket for the "A" cable connection.

Before connecting an external disk cable, prepare it as follows, if necessary:

1. Remove the cover plate from the disk connector assembly.

2. Remove 4 inches of plastic sheathing from one end of the cable.

3. Disassemble the cable clamps on the cover plate by removing the Phillips screws on either side of the clamp. (Figure 4-26.)

4. Lay the shielded section of the external "A" disk cable against the face of the clamp at the right side of the plate. Leave 1/4 inch of foil exposed.

5. Lay the shielded section of the external "B" disk cable(s) against the face of the clamp at the left side of the plate. Group all four "B" cables on the left side. Leave 1/4 inch of foil exposed.

6. Reassemble the cable clamps by installing the two Phillips screws removed in step 3. Make sure that pin 1 of the cables are oriented properly and tighten the clamp screws until solid contact with the shield is made. DO NOT overtighten the Phillips screws, as this could damage the disk cables.

7. Plug the cables into the cable connectors on the disk connector assembly. The top left "B" cable connector attaches to Port 0 of the associated 23V98 Disk IOC, the bottom left "B" cable connector attaches to Port 1, and so forth. The extreme left connector on the assembly attaches the "A" cable daisy-chained through each drive to the VS-300 mainframe.

8. Reinstall the disk connector assembly cover plate.

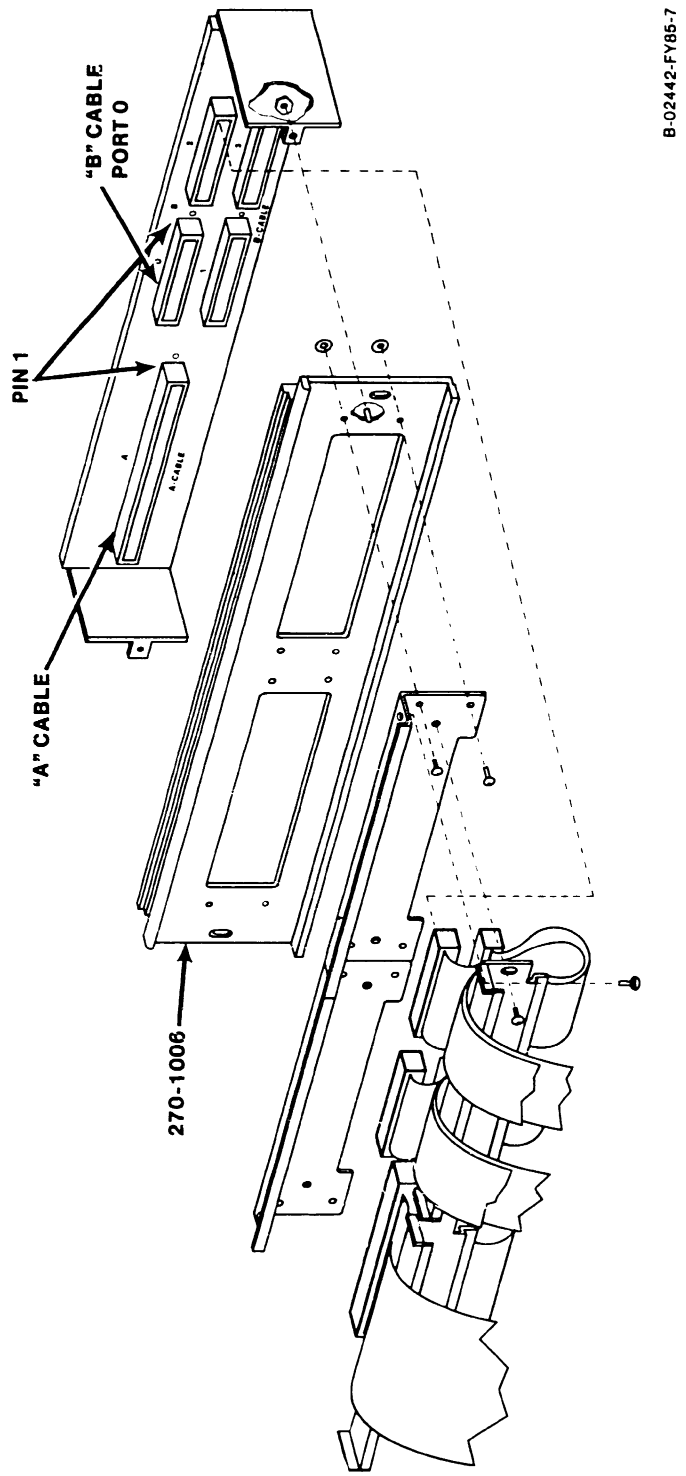


Figure 4-26. 270-1006 "A" and "B" Cable Connector Assembly

4.10.5 TELECOMMUNICATION CONNECTORS

If either the Multiline TC (MLTC) or the Gate Array option is to be installed, the TC cables must be attached to a MLTC connector assembly, WLI P/N 270-1003, or Gate Array connector assembly, WLI P/N 270-1016, at the rear of the mainframe (or on the Cable Concentrator).

Each MLTC assembly provides 16 ports in support of only one type of TC protocol at a time. If the customer's TC requirement calls for support of Automatic Calling Units (ACU), each ACU requires one RS232C port link and one RS366 port link. Currently, each VS-300 supports two MLTC options for a total of 32 ports.

The Gate Array supports only one type of TC protocol at a time. Support of two types of protocols requires a second Gate Array asembly. A single Gate Array assembly must be reinitialized (reIPL'ed) to support another type of protocol.

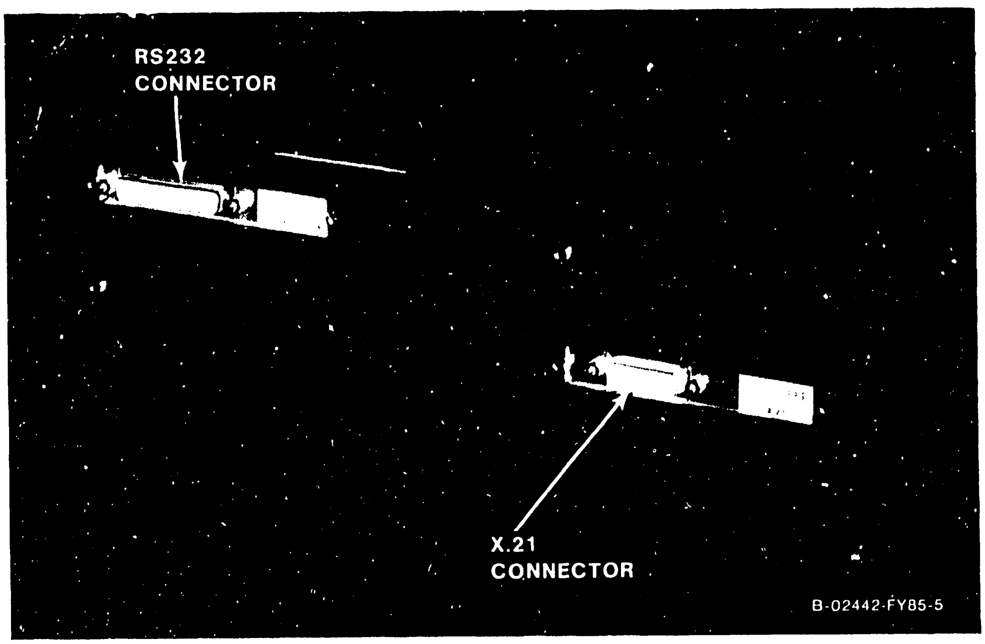


Figure 4-27. Multiline TC (MLTC) Connector Panel

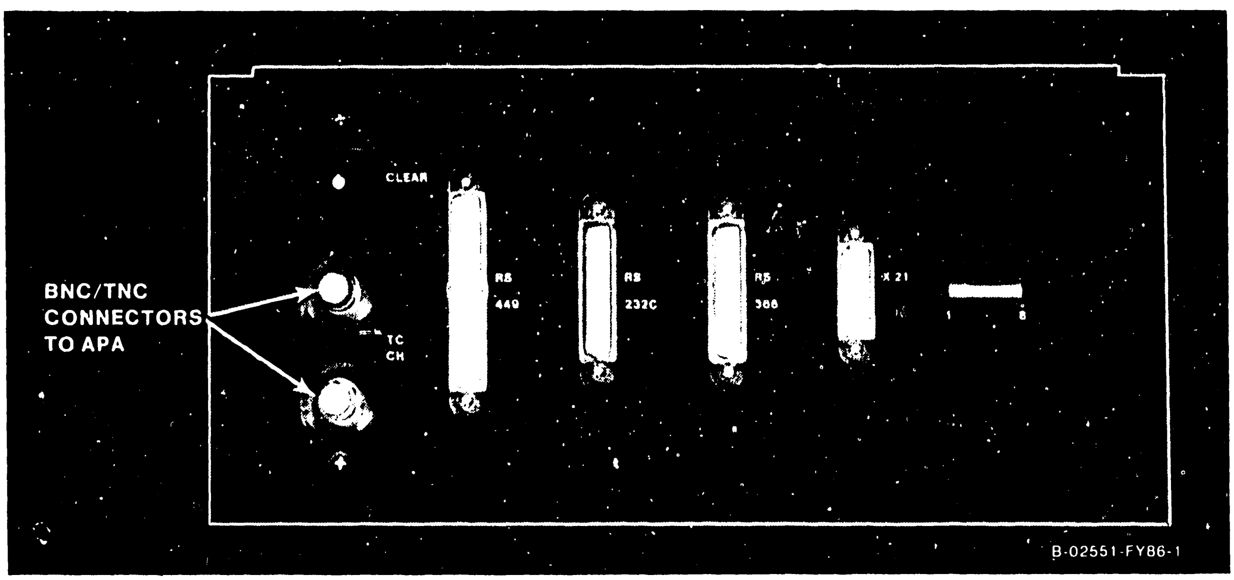


Figure 4-28. Gate Array TC Connector Panel

4.10.6 KENNEDY TAPE DRIVE CONNECTORS

The Kennedy tape connector assembly (WLI P/N 270-1005) is used when one or more Kennedy tape drives are connected to the mainframe. Two 50-pin sockets (labeled Control #1 and Data #2) are located on the assembly for connection to the drives. Note the orentation of the cable plugs when inserting them into the 50-pin sockets.

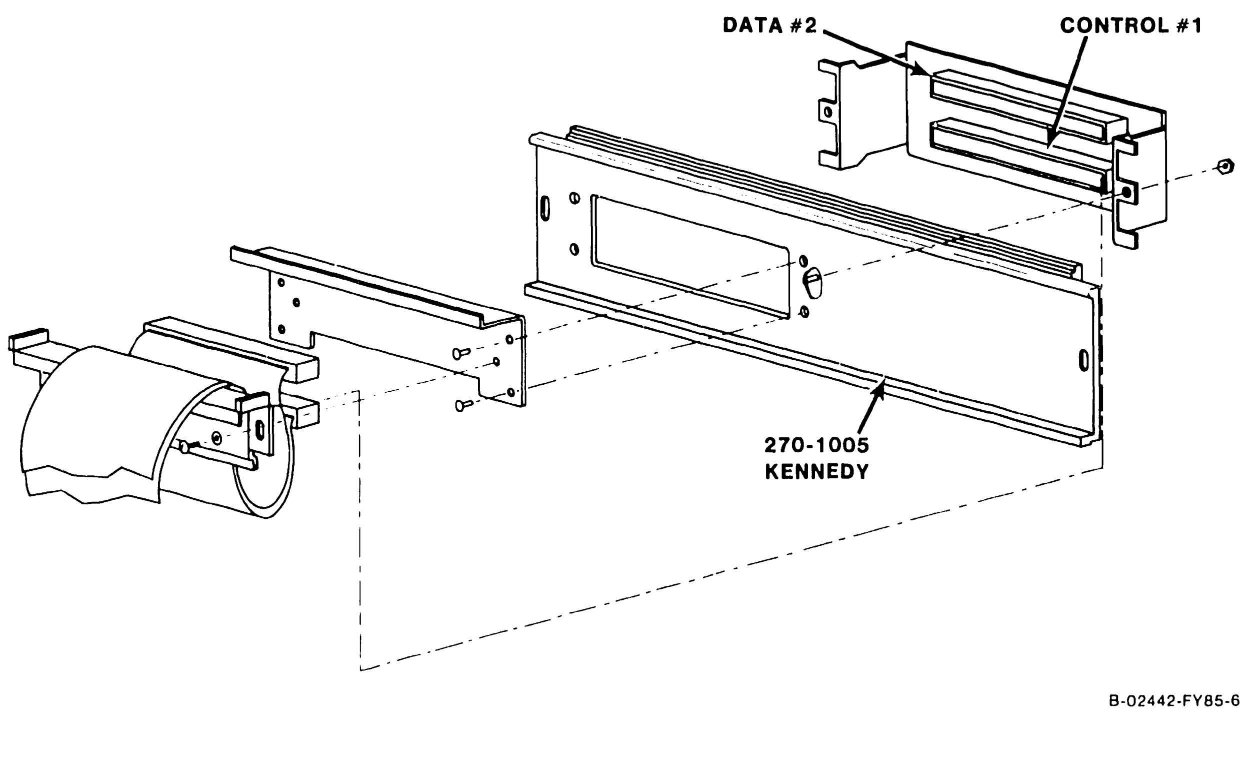


Figure 4-29. 270-1005 Kennedy Tape Drive Connector Assembly

4.10.7 TELEX TAPE DRIVE CONNECTORS

The Telex tape connector assembly (WLI P/N 270-1007) is used when one or more Telex tape drives are connected to the mainframe. Three 50-pin sockets (labeled 0, 1, and 2) are located on the assembly for connection to the drives. Note the orientation of the cable plugs when inserting them into the 50-pin sockets.

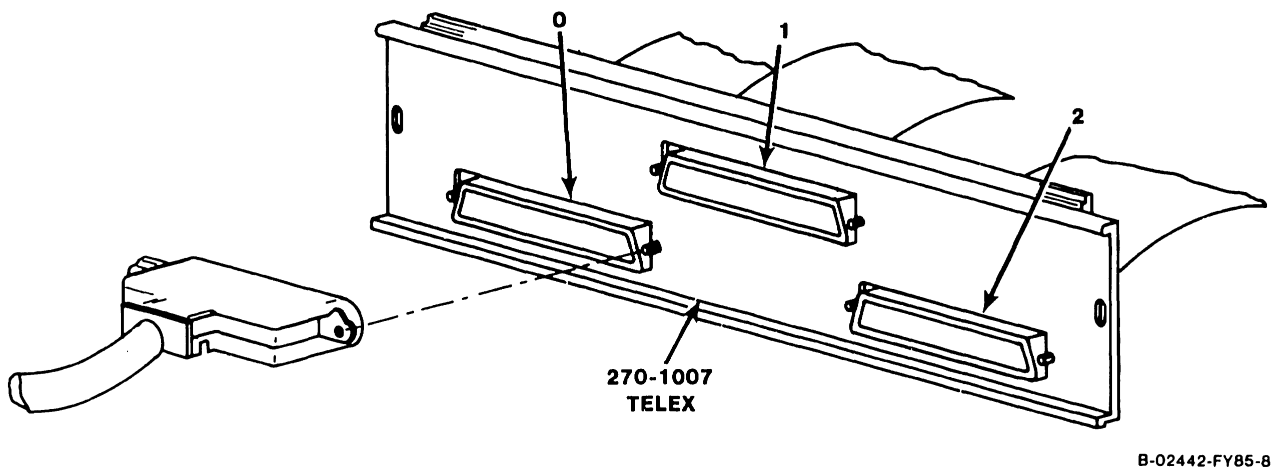


Figure 4-30. 270-1007 Telex Tape Drive Connector Assembly

4.10.8 P-BAND CONNECTORS

The WangNet Peripheral Band (P-Band) is supported by the 23V97 Serial IOC. Connector J1 on the IOC is always reserved for the P-Band. P-Band supports Ergo Workstations and Netmux.

The complete Peripheral Band assembly model number is 23V67W-19, which includes the Serial IOC, Global Modem assembly, all interconnecting cables, and hardware.

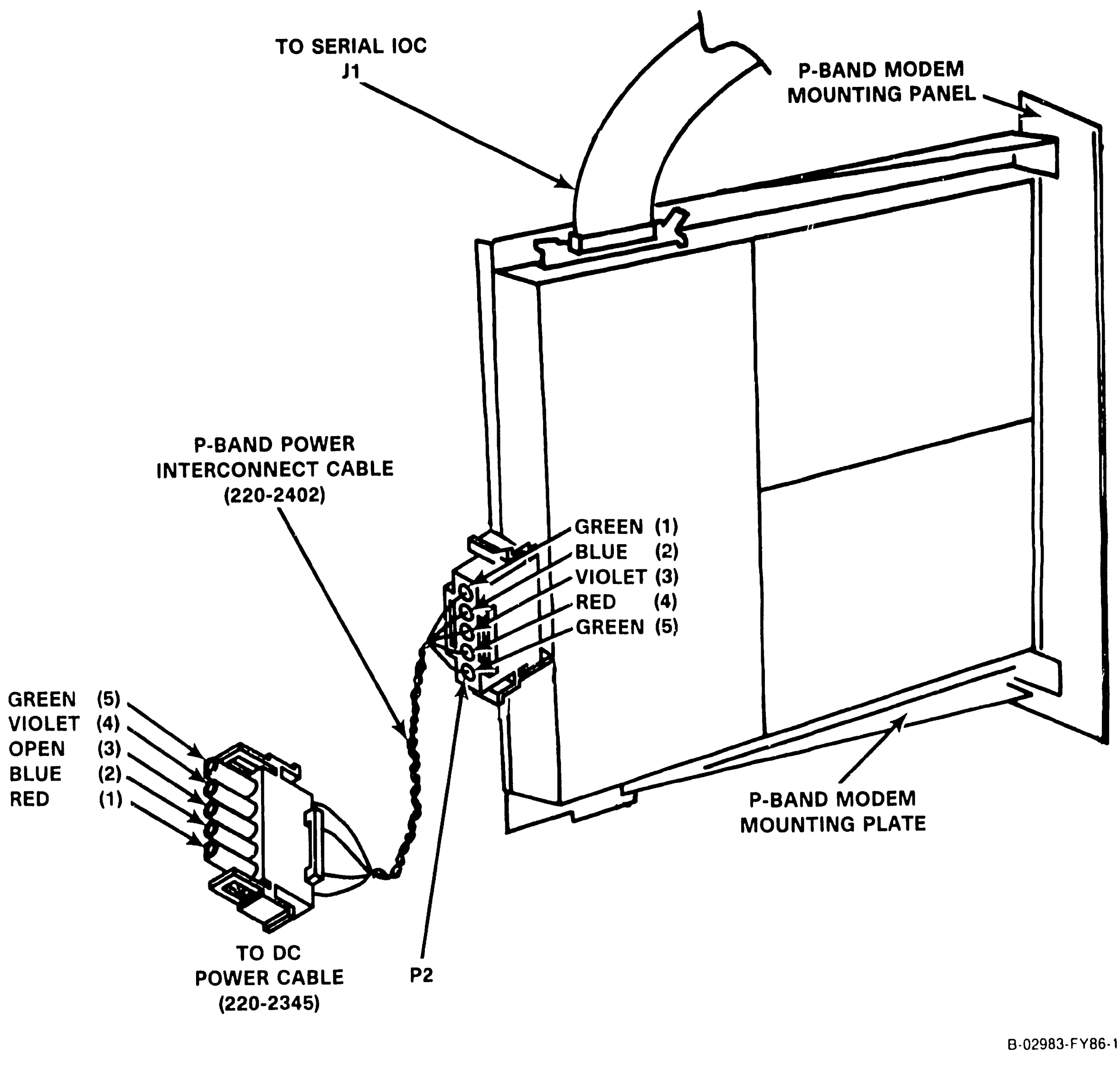


Figure 4-30a. WangNet P-Band Modem Assembly

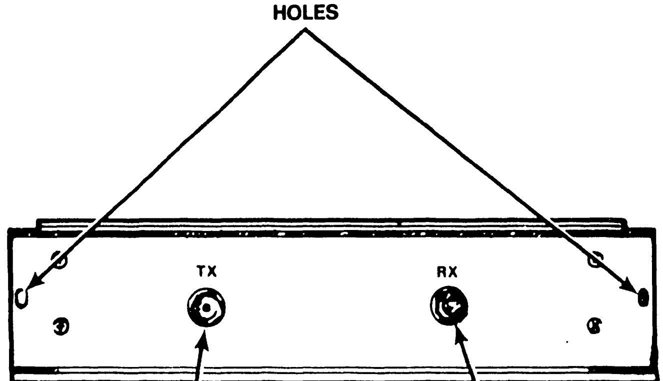


Figure 4-30b. WangNet P-Band Modem Rear Panel Assembly

4.11 REMOTE LINK (FOR 1.02 SCU SOFTWARE)

Remote Link will be used on initial VS-300 systems for remote maintenance support. The following provides installation and remote link verification information for version 1.02 of the SCU software.

4.11.1 REMOTE LINK SPECIFICATIONS

1. Capabilities:

   a. Remote operator console and workstation 0 emulation.

   b. Access to error log and all online diagnostics.

2. Restrictions:

   a. Can't use Control Mode or run offline diagnostics. System must be running to use Remote Link.

3. Remote Site Requirements:

   a. Hardware.

      1) Phone line - supplied by customer for remote hookup.

      2) VS-300 Support Control Unit (SCU) - supplied with the VS-300.

      3) Wang WA3451 modem - supplied with the VS-300.

      4) "T" connector - supplied with the modem.

   b. Software.

      1) Modified console menu - Remote Link selection added.

      2) Remote Link Home Interface program - installed on SCU disk drive.

4.11.2 SITE PREPARATION FOR REMOTE LINK

1. During the site installation check, verify that the following order has been placed with the local telephone company by the customer:

   a. Telephone line for remote maintenance support. (A dedicated line is not required.)

   b. Telephone for remote maintenance support

   c. Either of the following modular connecting blocks for the telephone:

      1) RJ11C jack for desk top telephones

      2) RF11W jack for flush mounted wall telephones

NOTE

RF11W flush mount wall phone jack can be used with the "T" connector and a desk top phone, but a wall mounted phone cannot be used.

4.11.3 REMOTE LINK INSTALLATION AND VERIFICATION

1. Connect the modem to the phone line, supplied by the customer, through the "T" connector. (Figure 4-31.) (If the phone line is not available, indicate this on the call report. If the installation is among the first 50 systems, the Technical Assistance Center [TAC] should also be notified when status is reported.)

2. Connect the modem to the SCU RS232 connector located on the rear of the mainframe, on the bulkhead below the monitor arm, using the RS232 cable that is supplied with the VS-300.

3. Make sure that the modem switches are set as shown in figure 4-31.

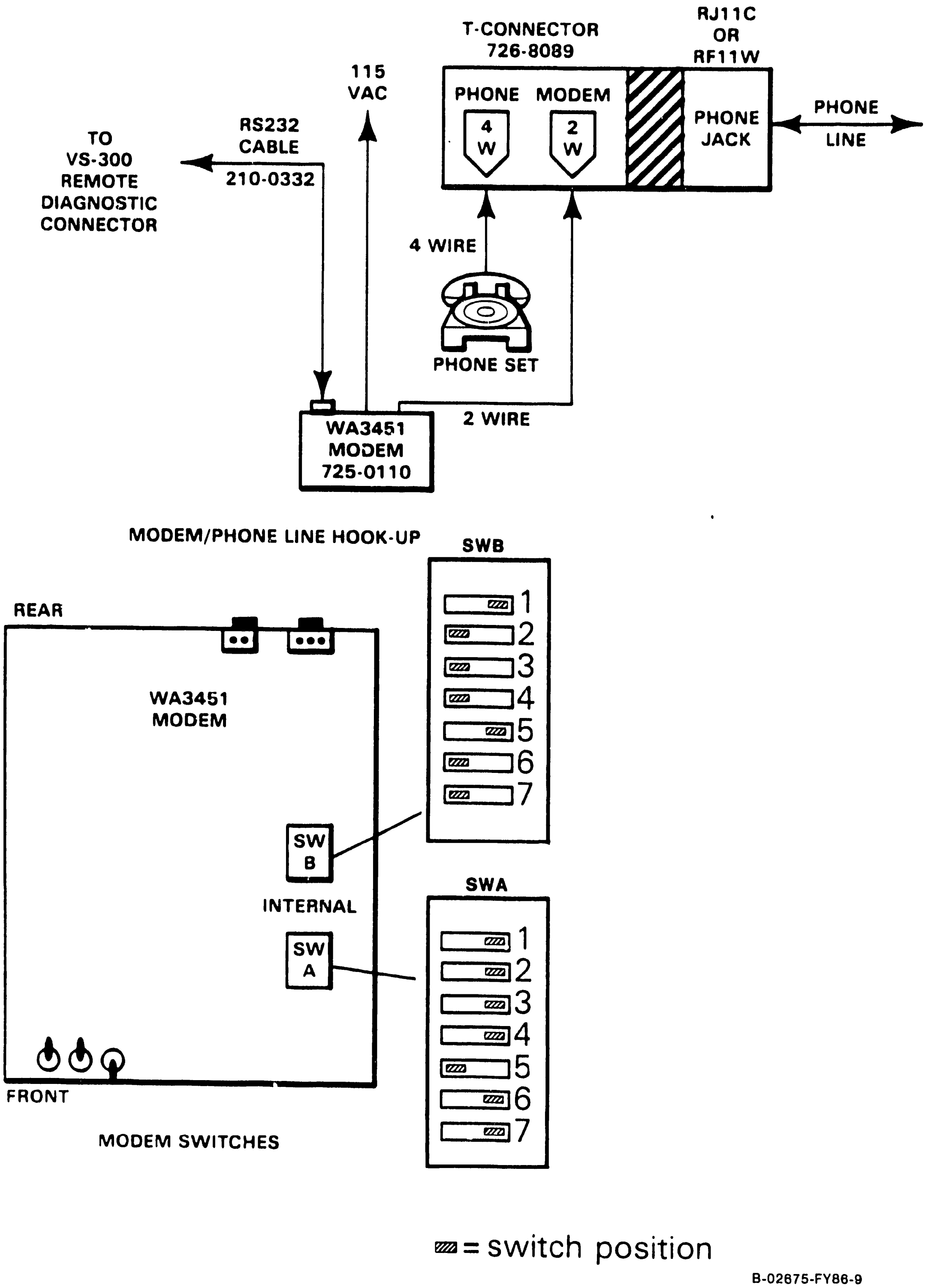


Figure 4-31. Modem/Phone Connections and Modem Switch Settings

4. After the system is powered up and IPLed, press the space bar until Console Mode on the SCU screen is highlighted. (Figure 4-32.)

```
mm/dd/yy            Wang Laboratories, Inc.          hh:mm:ss
                     Support Control Unit
                   Main Menu Version 1.02.00

Select an Item and Proceed

                        ■ Console Mode
                        _ Maintenance

                                       SPACE BAR - Item Select
                                       EXECUTE   - Proceed
                                       Cancel    - Previous Menu
```

Figure 4-32. SCU Main Menu

5. Press execute.

6. Check the menu for the Remote Link choice. (Figure 4-33.) If Remote Link has not been installed, there will be only two menu choices. (Figure 4-34). If Remote Link has not been installed, go to step 7. If Remote Link has been installed, go to step 11.

```
mm/dd/yy            Wang Laboratories, Inc.          hh:mm:ss
                     Support Control Unit
                   Console Mode Version 1.02.00


Select an Item and Proceed


                          _ Control Mode
                          _ Workstation Emulation
                          ■ Remote Link Host Interface 2.3


                                    SPACE BAR - Item Select
                                    EXECUTE   - Proceed
                                    Cancel    - Previous Menu
```

Figure 4-33. SCU Console Mode Menu With Remote Link

```
mm/dd/yy            Wang Laboratories, Inc.          hh:mm:ss
                     Support Control Unit
                   Console Mode Version 1.02.00


Select an Item and Proceed


                          ■ Control Mode
                          _ Workstation Emulation


                                    SPACE BAR - Item Select
                                    EXECUTE   - Proceed
                                    Cancel    - Previous Menu
```

Figure 4-34. SCU Console Mode Menu Without Remote Link

7. If Remote Link has not been loaded onto the SCU disk drive, press Cancel and select Maintenance Mode on the SCU Main Menu.

```
mm/dd/yy              Wang Laboratories, Inc.            hh:mm:ss
                       Support Control Unit
                     Main Menu Version 1.02.00


Select an Item and Proceed


                          _ Console Mode
                          ■ Maintenance


                                         SPACE BAR - Item Select
                                         EXECUTE   - Proceed
                                         Cancel    - Previous Menu
```

Figure 4-35. SCU Main Menu

8. Press Execute. The SCU Maintenance Menu will appear.

```
mm/dd/yy              Wang Laboratories, Inc.            hh:mm:ss
                       Support Control Unit
                    Maintenance Version 1.02.00


Select an Item and Proceed


                          _    Diagnostics
                          _    Set Time and Date
                          _    Initialize CPU/MCU/SBI
                          _    Change/Load CP Microcode
                          _    Reset VS System
                          ■    Install SCU Software
                          _    System Element Status Display


                                         SPACE BAR - Item Select
                                         EXECUTE   - Proceed
                                         Cancel    - Previous Menu
```

Figure 4-36. SCU Maintenance Menu

9. Select Install SCU Software on the SCU Maintenance Menu and press Execute.

10. Copy the Remote Link software to the SCU disk from the Remote Link diskette, SCU diskette number six. Upon completion of this step the SCU Console Menu will have Remote Link for a third menu choice. (Figure 4-33.)

11. When the installation is complete, notify the Technical Assistance Center (TAC) that the system is ready for remote maintenance certification. Supply TAC with the modem phone number and a backup phone number for voice communication. Place the modem offline to allow conformation of the system status.

12. Place the Control Panel key switch in the Remote Service position.

13. A TAC engineer will call back using the modem phone number. The system should be IPLed and running. Workstation 0 must be logged on, or TAC must be provided with a valid logon. Workstation emulation on workstation 0 must be suspended or terminated and Remote Link selected. (Figure 4-33.) The modem is now put into data position and the link verification started.

14. Upon completion of the link verification, TAC will disconnect the Remote Link link and release workstation 0. To exit Remote Link, press the 2ND key and select TERMINATE. The workstation will return to the Console Menu.

CHAPTER 5

MAINT-ENANCE

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CHAPTER 5

MAINTENANCE

5.1 GENERAL

This chapter consists of preventive maintenance (PM), adjustments, and removal and replacement procedures for field-replaceable components in the VS-300 mainframe.

5.2 PREVENTIVE MAINTENANCE

Periodic maintenance is essential to the proper operation of the VS-300 mainframe and associated peripherals. Because of its design, the mainframe requires a minimum amount of maintenance to ensure efficient operation.

5.2.1 SPECIAL TOOLS

Description	WLI P/N
Low Battery Voltage Dropout Jumper	220-2341
Power Supply Test Jumper	220-2342

5.2.2 MATERIALS

No special materials are necessary to perform mainframe PM.

5.2.3 PREVENTIVE MAINTENANCE SCHEDULE

PM for the mainframe should be performed at six month intervals, (in conjunction with a service call if no PM has been performed within six months), and is as follows:

Procedure	Item	Notes
Inspect	Mainframe interior	Look for dust & loose hardware. Clean.
Inspect/clean	SCU (PC) diskette read/write heads	Refer to Professional Computer Manual
Inspect	Power supply(s) fan(s) (3) & SCU (PC) fan	Replace power supply. Replace SCU (PC) fan
Check/adjust	Power supply voltages	Paragraph 5.2.4.1
Check (Note)	Backup batteries	Paragraph 5.2.4.3
Run diagnostics	Mainframe & peripherals	Refer to Chapter 7 or applicable maintenance manuals.

NOTE

The backup batteries should be replaced every 18 months. Replace all five battery packs at the same time. (Paragraph 5.3.2.10.)

5.2.4 ELECTRICAL ADJUSTMENTS

5.2.4.1 Power Supply Adjustments

1. Remove the left front panel (paragraph 5.3.2.2)

2. Remove the screws from the rear fan panel, disconnect the two fans and set aside the panel.

3. Press the Control Panel On button or SW1 (On) on the Power Supply Controller. Make sure the On lamp on the Control Panel and the voltage sensing LEDs 1 → 5 on the Power Supply Controller are lit. If the LEDs are not lit or go out after a few seconds, there is a problem with either of the power supplies, or the Power Supply Controller board. No adjustments can be done until the problem is corrected. Do the following:

   a. Remove the 4-pin connector from either J5 (multioutput power supply control) or J4 (booster power supply control) of the Power Supply Controller board. (Figure 5-3.)

   WARNING

   Inserting the test jumper as described in step b (below) will immediately turn on the switching power supplies if the ac On/Off circuit breaker is on.

   b. Insert the Power Supply Test Plug (WLI P/N 220-2342) into P5 (cable to the multioutput p/s) or P4 (cable to the booster p/s).

   c. If the power supply comes up and stays up, the power supply is good. (Refer to Chapter 7 for troubleshooting procedures for the 210-8709 Power Supply Controller board.) If the power supply still does not come up, replace the supply. (Paragraph 5.3.2.22 or 5.3.2.24.)

   d. Disconnect the test jumper and reconnect the cable to J4 or J5.

4. The following power supply voltages should be measured at the test points on the Power Supply Controller. Adjust the voltages to the readings listed below using the potentiometers on the front of the particular switching power supply at the rear of the mainframe (figures 5-1 and 5-2).

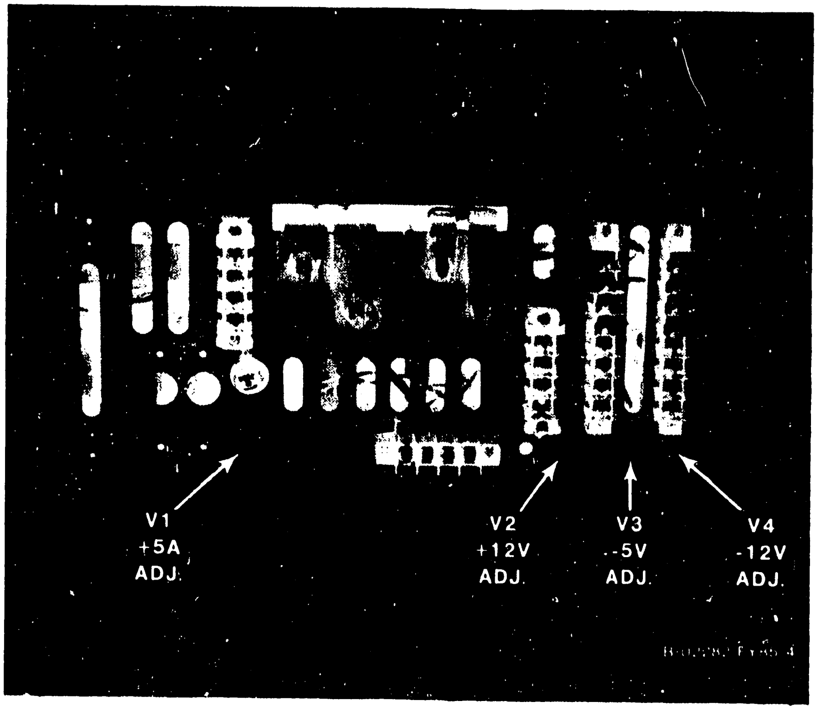


Figure 5-1. Multioutput Power Supply

PHOTO NOT AVAILABLE

Figure 5-2. Booster Power Supply

Table 5-1. Power Supply Voltage Measurements

Test Point	Adjust (P/S)	Volts	Minimum	Maximum	AC Ripple Limits
TP+5VA	V1 (P/S 1)	+5.0A	+4.96	+5.04	35mV RMS or 50mV Pk-to-Pk
TP+5VB	5V (P/S 2)	+5.0B	+4.96	+5.04	35mV RMS or 50mV Pk-to-Pk
TP+12V	V2 (P/S 1)	+12.0	+11.96	+12.04	35mV RMS or 50mV Pk-to-Pk
TP-5V	V3 (P/S 1)	-5.0	-4.96	-5.04	35mV RMS or 50mV Pk-to-Pk
TP-12V	V4 (P/S 1)	-12.0	-11.96	-12.04	35mV RMS or 50mV Pk-to-Pk
TPGROUND		+/-0	+/-0	+/-0	

NOTE

1. P/S 1 is the multioutput supply.
2 P/S 2 is the booster supply.
3. It is better to have the +5 V adjusted more toward the maximum than toward the minimum.

5.2.4.2 Power Supply Controller Adjustments

1. On the Power Supply Controller board (figure 5-3), measure/adjust the calibration voltages at:

   a. TP 8 for 8 volts. On Rev. 0 boards, adjust R11. (There is no TP 8 or adjustment on Rev. 1 boards.)

   b. TP 2.5 for 2.5 volts. On Rev. 0 boards, adjust R12. (There is no TP 2.5 or adjustment on Rev. 1 boards.)

2. Set the 4-bit Voltage Address switch SW3 (table 5-2) on the Power Supply Controller board to the A/D input to be calibrated.

Table 5-2. DC Voltage Address Switch SW3 Settings

Voltage	Bit 1	Bit 2	Bit 3	Bit 4
-5.0	On	Off	Off	X
-12.0	Off	On	Off	X
+12.0	On	On	Off	X
+5.0B	Off	Off	On	X
+5.0A	On	Off	On	X

NOTES

1. On = 1
2. Off = 0
3. X = don't care (position 4 not used)

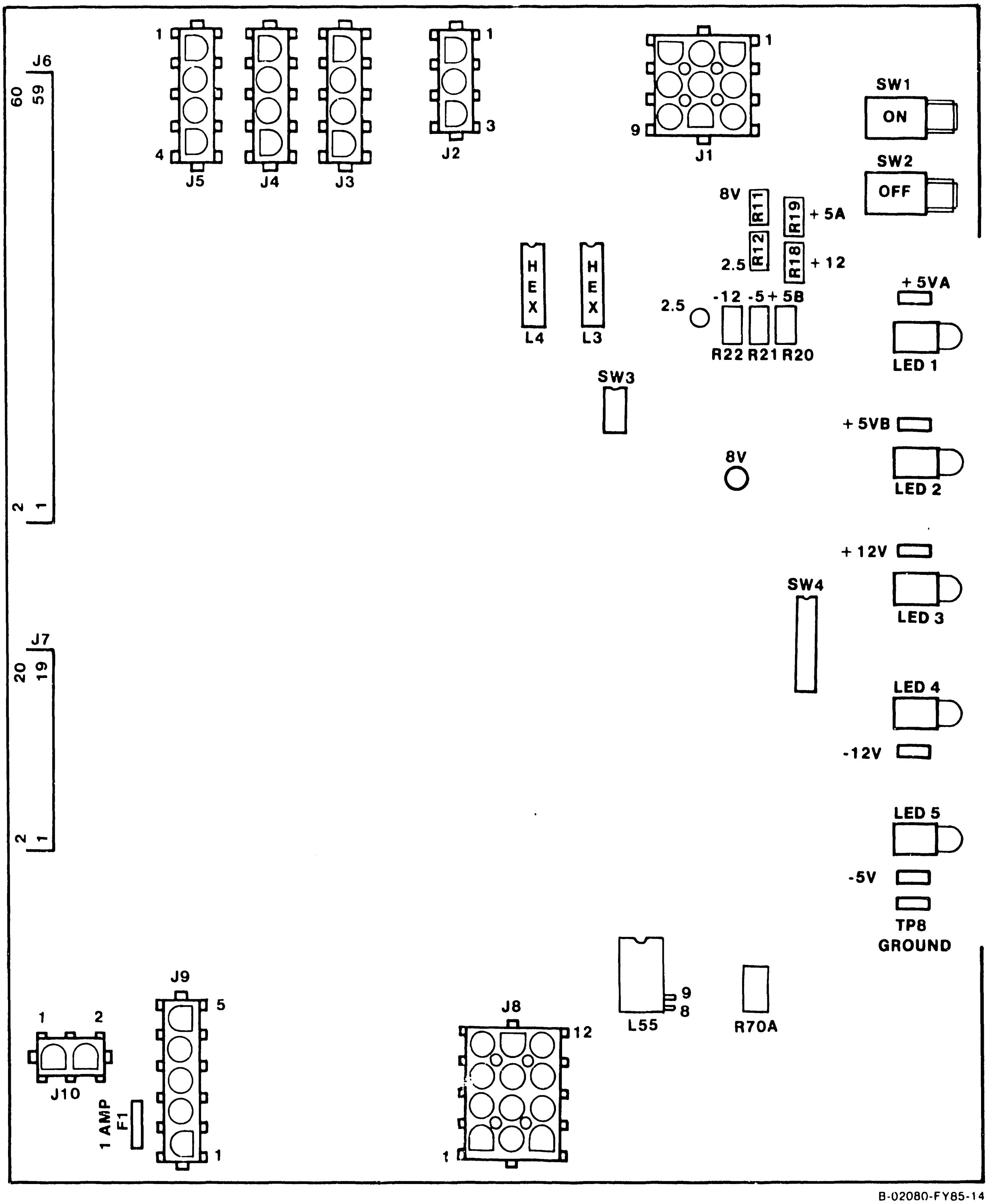


Figure 5-3. Power Supply Controller Board. (Rev. 0 Version)

3. Look at the two hex displays on the Power Supply Controller board. Using the potentiometers on the Power Supply Controller board, adjust the A/D outputs to the hex display values as shown in table 5-3. Change the Voltage Address switch for each voltage to be calibrated.

Table 5-3. A/D Output Values At Hex Displays

Voltage	Adjust	Minimum Hex Value	Exact Hex Value	Maximum Hex Value
-5.0	R21	7E	80	82
-12.0	R22	7E	80	82
+12.0	R18	7E	80	82
+5.0B	R20	7E	80	82
+5.0A	R19	7E	80	82

4. From the SCU DCS Test Selection Menu, select the VS XXX Environment.

```
mm/dd/yy          Wang VS Diagnostic Control System              hh/mm/ss
                         prerelease 5.03.14p
                        □□□□ □□□□ □□□□ □□□□

  Sequence: 1                                            Error Cnt: 0
Diagnostic: R1530 VSXXX Environment
      Test: Display

| DCS Status: Diagnostic Executing                                      |

Voltage Readings = +5.000  +5.000  -5.000  +12.00  -12.00  Air Flow = 01

SCU Control Registers = 4700 ACFF                SCU Registers = C804 5000

CPU SCR = 4400     FPU SCR = EEEE     MCU SCR = 0000     SBI SCR = 0000

Control Panel Key switch is set to NORMAL

System Reset has been pressed

AC power has been cycled
```

Figure 5-4. Environment Test Screen

5. Look at the Environment Test Screen on the Support Control Unit (SCU) screen. (Figure 5-4.) The voltages shown in table 5-4 will appear on the screen.

NOTE

Do not rely on the Environment Test Screen on the SCU to adjust the voltages. It is strictly a monitor and will not respond quickly enough to do a reliable voltage adjustment. Adjust the A/D outputs while viewing the hex display.

Table 5-4. DC Voltages On SCU Screen

Voltage	Minimum	Maximum
+5.0(A)	+4.96	+5.04
+5.0(B)	+4.96	+5.04
-5.0	-4.96	-5.04
+12.0	+11.96	+12.04
-12.0	-11.96	-12.04

5.2.4.3 Battery Backup Check

To check the length of time and the capacity of the backup batteries to provide power for the mainframe, perform the following:

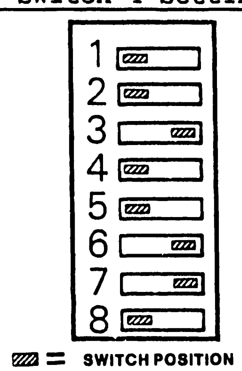
1. Make sure that all operators have logged off the system, inhibit further logons from the Operator's Console menu, and enter Control Mode.

2. Power down the disk drives. Also power down all workstations and other peripheral devices, if possible.

3. Leave the ac On/Off circuit breaker (located on the Power Distribution Unit) in the On position and disconnect the ac power input connector from the power source receptacle.

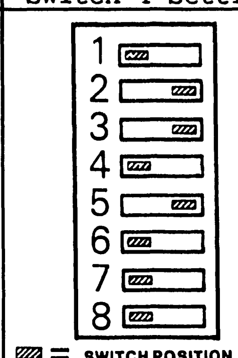
4. The mainframe should stay powered up for 100 seconds. If the mainframe drops power before 100 seconds time has expired, check the setting of Switch 4 on the Power Supply Controller board. Switch 4 should be set for 100 seconds of backup time for Rev. 0 boards, and (currently) 96 seconds for for Rev. 1 boards.

Switch 4 Settings (Rev. 0 Board)



Designations	
1	
2	
4	Battery
8	Backup
16	Time
32	(Seconds)
64	
128	

Switch 4 Settings (Rev. 1 Board)



Designations	
16	Battery
32	Backup
64	Time
128	(Seconds)
32	Minor
64	Voltage
128	Time
256	(Seconds)

Figure 5-5. Battery Backup Time Switch SW4 Settings

B-02675-FY86-8

5. If Switch 4 is set correctly, the batteries may not be properly charged (refer to paragraph 5.2.4.5, charging p/s adjustment); or the Power Supply Controller board may be defective (refer to paragraph 7.5.1, Power Supply Controller board fault isolation).

5.2.4.4 Low Battery Voltage Dropout Adjustment

1. Turn OFF the mainframe ac On/Off circuit breaker.

WARNING

120 V ac remains on J3 if the mainframe ac On/-Off circuit breaker is not turned OFF.

2. On the Battery Backup Charging Power Supply, disconnect the 3-pin ac input power cable connector from J3. (Figure 5-5a.)

CAUTION

If the mainframe ac On/Off circuit breaker is not turned OFF and J3 is not disconnected before inserting the jumper described below in step 3, the charging p/s will be damaged.

3. On the Battery Backup board disconnect J7, one of the 2-pin battery input cables. Insert the 2-pin Low Battery Voltage Dropout jumper (WLI P/N 220-2341) into J7 of the board.

4. Turn ON the mainframe ac On/Off circuit breaker and press the Control Panel On button or SW1 (On) on the Power Supply Controller. Observe one of the following:

   a. If the system powers up, carefully adjust R70A on the Power Supply Controller counterclockwise until the system just powers down. Leave R70A in this position.

   b. If the system does not power up, adjust R70A on the Power Supply Controller clockwise, while pressing the Control Panel On button or SW1 (On), until the system just powers up. Carefully adjust R70A counterclockwise until the system just powers down. Leave R70A in this position.

5. Turn OFF the mainframe ac On/Off circuit breaker.

6. On the Battery Backup board remove the jumper from the battery input cable connector J7 and reconnect this connector and also reconnect the 3-pin connector on J3 on the Battery Backup Charging Power Supply.

7. Turn ON the mainframe ac On/Off circuit breaker and press the Control Panel On button or SW1 (On) on the Power Supply Controller. The system should power up and stay powered up.

5.2.4.5 Battery Backup Charging Power Supply Adjustment

The battery backup charging power supply is adjusted as follows:

1. Set the dc voltage scale on a digital voltmeter for 200 volts.

2. Measure across the two top wires (the black wire, pin 1, and the brown wire, pin 2) of the 6-pin cable connector (J4) on the power supply. (Figure 5-5a.)

3. Turn the power supply adjustment pot, R23, until the meter reads +53.5 volts, +/-1.0 volt.

4. Measure between the other wires of J4 connector as follows:
   a. Brown (pin 2) and red (pin 3).
   b. Red (pin 3) and orange (pin 4).
   c. Orange (pin 4) and yellow (pin 5).
   d. Yellow (pin 5) and blue (pin 6).

5. If the voltage reading(s) deviate greater then +/-1.0V from 53.5 volts, either the power supply or one of the batteries is defectve. (Replace all five battery packs at the same time.)

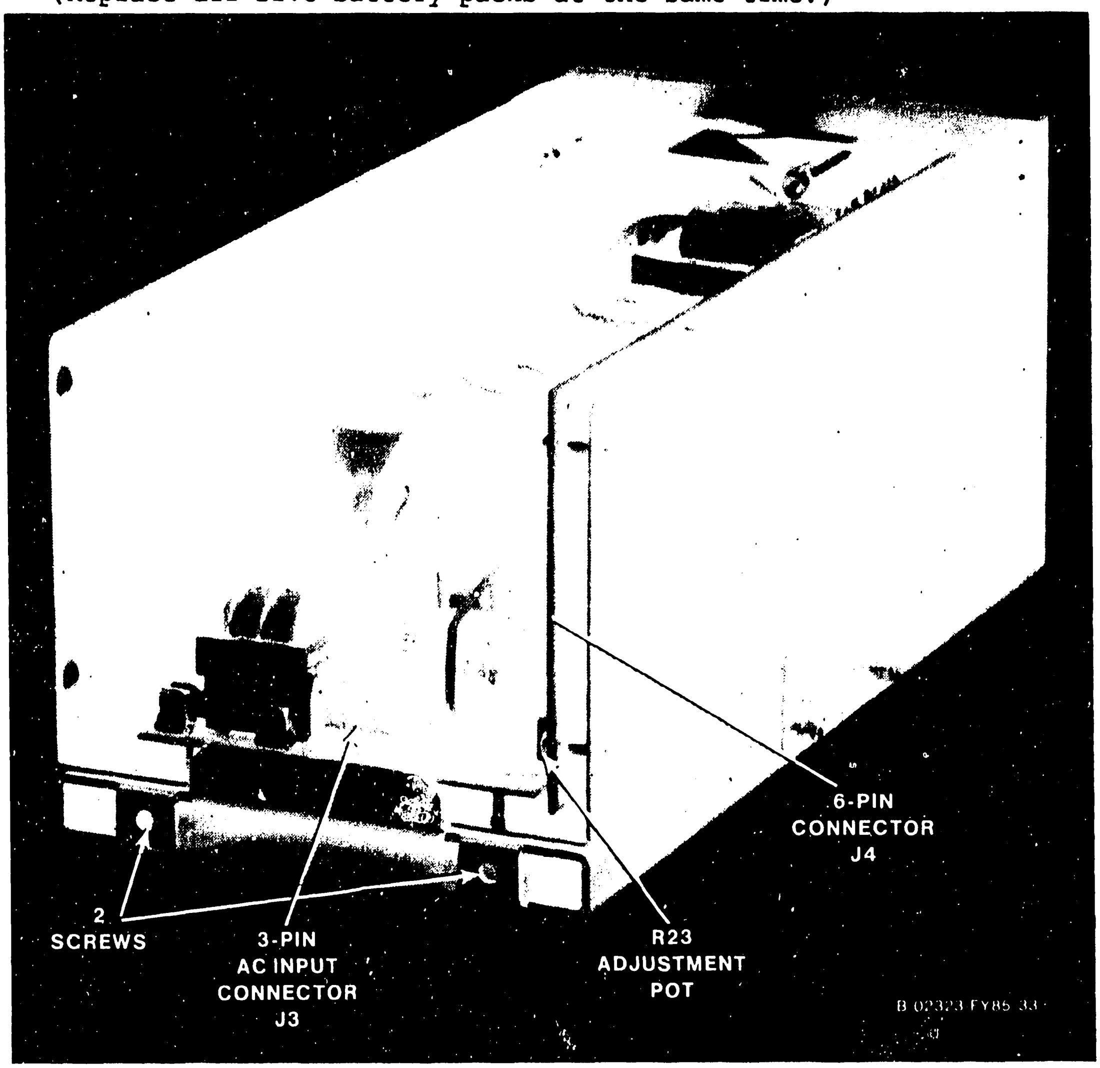


Figure 5-5a. Battery Backup Charging Power Supply Adjustment

5.2.5 PERIPHERAL PREVENTIVE MAINTENANCE

Refer to the appropriate documents for PM procedures for all VS-300 associated peripherals.

5.3 CORRECTIVE MAINTENANCE

5.3.1 SPECIAL TOOLS

Description	Part Number
RS232 Loopback Plug	421-0025
RS232/366 Loopback Plug	420-1041
RS449 Loopback Plug	270-3193
X.21 Loopback Plug	421-0010
Low Battery Voltage Dropout Jumper	220-2341
Power Supply Test Jumper	220-2342

CAUTION

```
*****************************************************************
*                                                               *
*  THIS COMPUTER EQUIPMENT HAS BEEN VERIFIED AS FCC CLASS A.    *
*                                                               *
*****************************************************************
```

IN ORDER TO MAINTAIN COMPLIANCE WITH FCC CLASS A VERIFICATION, THE FOLLOWING CONDITIONS MUST BE ADHERED TO DURING NORMAL OPERATION OF EQUIPMENT.

- ALL COVERS MUST BE ON SYSTEM AND SECURED IN THE PROPER MANNER.
- ALL INTERNAL CABLES MUST BE ROUTED IN THE ORIGINAL MANNER WITHIN THE CABLE CLAMPS PROVIDED FOR THAT PURPOSE.
- ALL EXTERNAL CABLING MUST BE SECURED AND THE PROPER CABLE USED TO ENSURE THAT CABLE SHIELDING IS PROPERLY GROUNDED TO THE CABLE CLAMPS PROVIDED.
- ALL HARDWARE MUST BE PROPERLY SECURED.

5.3.2 REMOVAL AND REPLACEMENT

These paragraphs describe the steps involved in removing and replacing or reinstalling all major field-replaceable components in the VS-300 mainframe.

5.3.2.1 Top Cover Removal and Replacement

Remove the top cover as follows: (See figures 5-6, 5-7, and 5-8.)

WARNING

The top cover is heavy. Be careful when performing the following steps.

1. At the rear of the cabinet, three Phillips head bolts secure the top cover to the mainframe. Loosen and remove the bolts.
2. Push on the cover until the cover starts to move forward. (Don't pry the cover with a screwdriver and don't let the cover become cocked.)

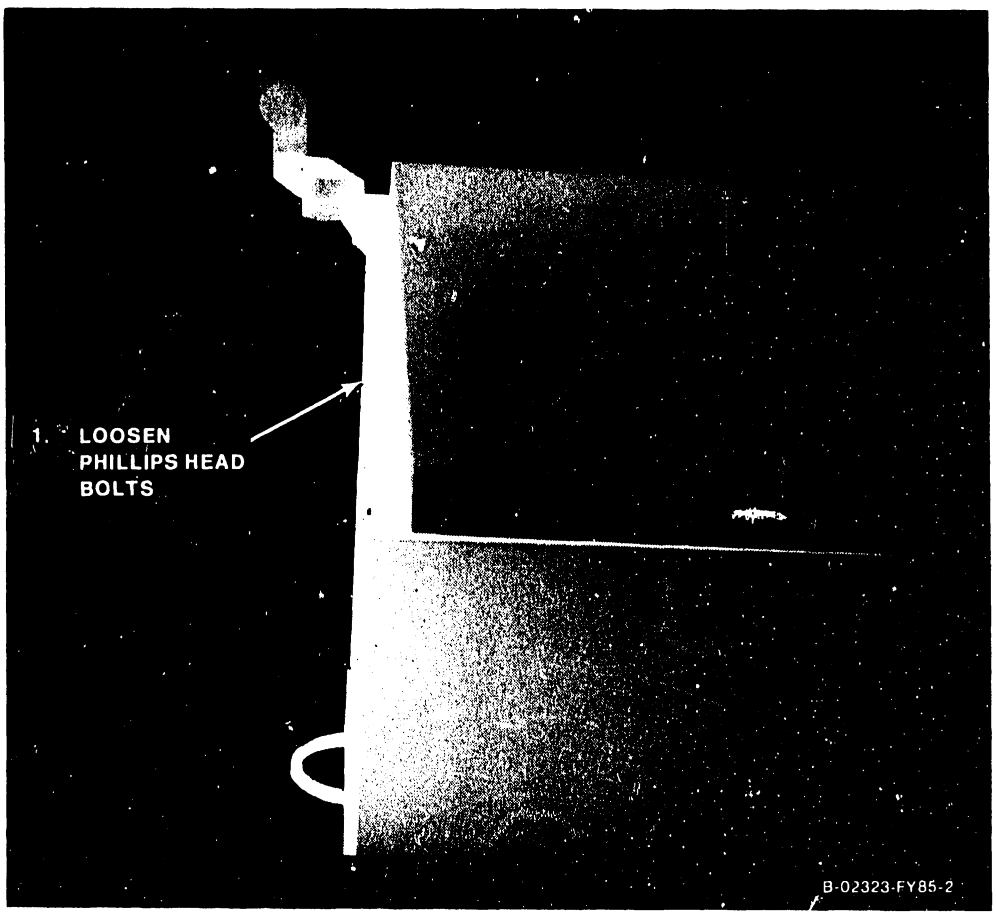


Figure 5-6. Top Cover Removal

3. From the front of the mainframe, grasp the front and rear of the cover and pull it forward about 6".

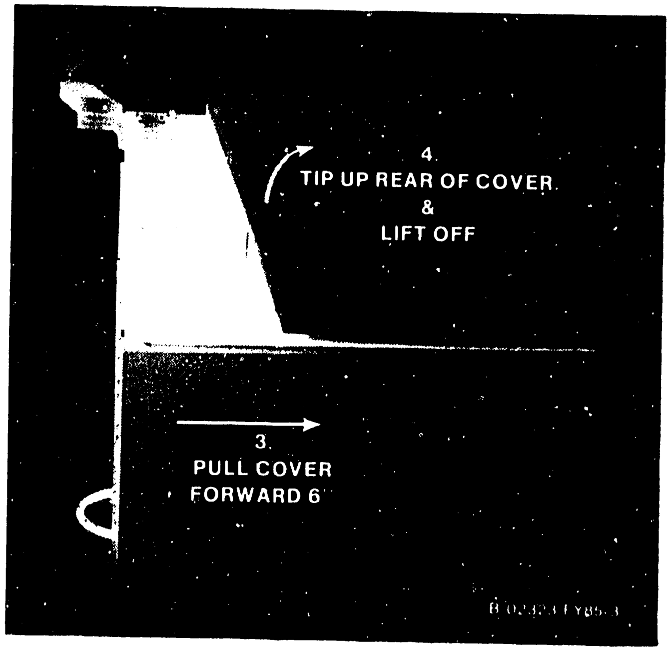


Figure 5-7. Top Cover Removal

4. As the cover moves forward, it will rise in the left and right cam brackets. When the cover is free of the cam brackets, tip it up, and carefully lift it off the mainframe.

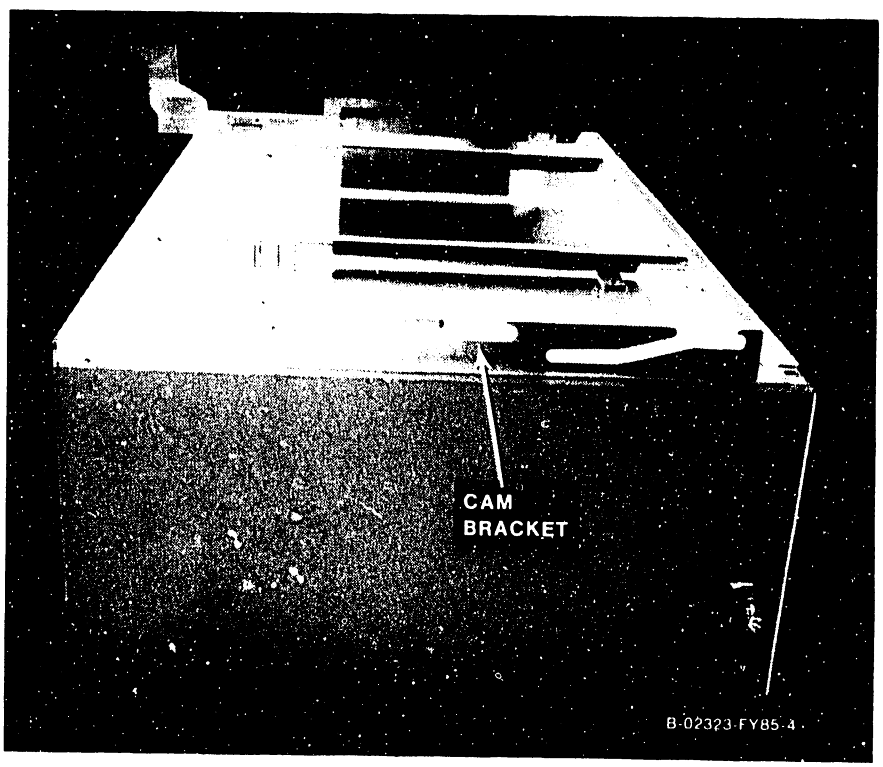


Figure 5-8. Top Cover Removal

Reinstall the top cover as follows:

1. Reinstall the top cover by reversing the removal procedure.
2. Carefully slide the top cover back into the cover cam brackets.
3. Alternately tighten the bolts. Don't let the cover become cocked.

5.3.2.2 Left Front Panel Removal and Replacement

Remove the left front panel as follows: (See figures 5-9, 5-10, 5-11.)

1. Open the front hinged door by turning the top and bottom keyed latches counterclockwise, then unlock the slam latch.

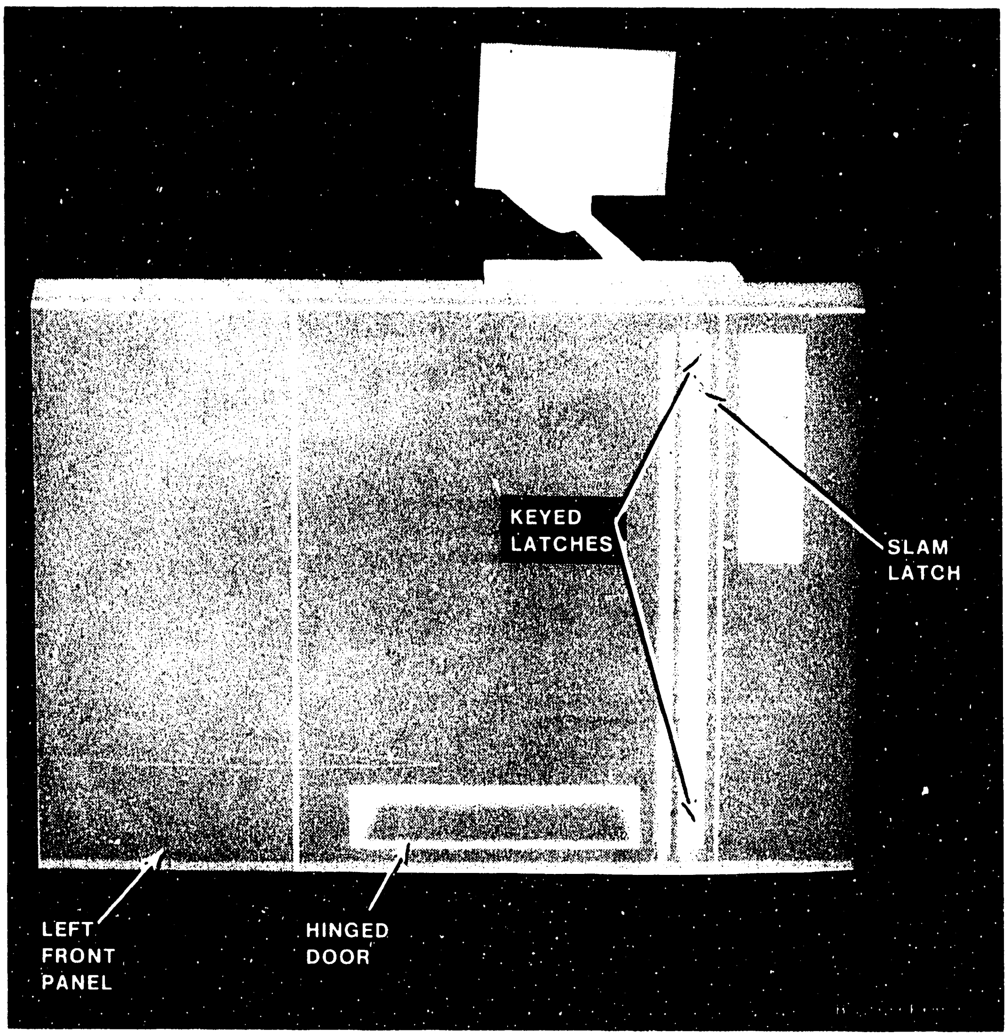


Figure 5-9. Left Front Panel Removal

2. Remove the two Phillips head screws (top and bottom) that secure the left front panel to the vertical frame.

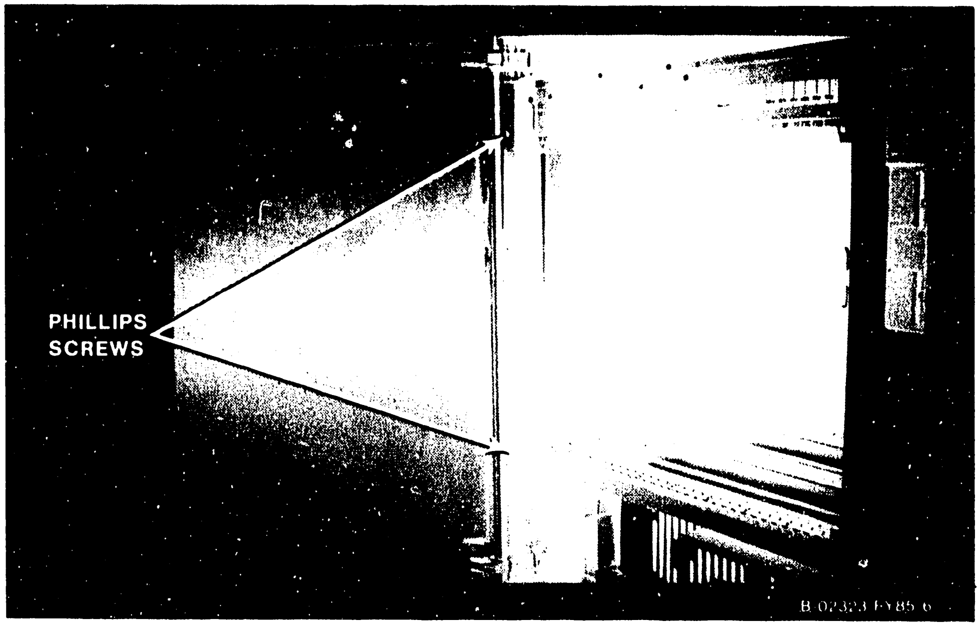


Figure 5-10. Left Front Panel Removal

3. The panel rests on three latch buttons. Slide the panel to the left, off the latch buttons, and off the mainframe.

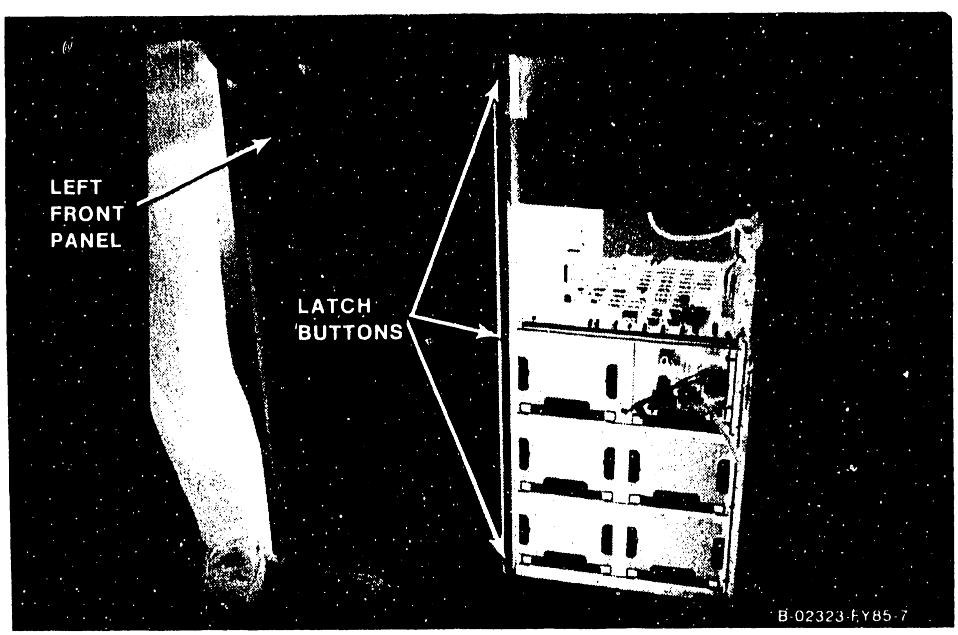


Figure 5-11. Left Front Panel Removal

Reinstall the left front panel as follows:

1. Reinstall the left front panel by reversing the removal procedure.

5.3.2.3 Left and Right Side Panel Removal and Replacement

Remove the left or right side panel as follows: (See figure 5-12.)

1. Remove the top cover as described in paragraph 5.3.2.1.
2. Each side panel rests on four latch buttons. Slide the panel(s) up, off the latch buttons, and off the mainframe.

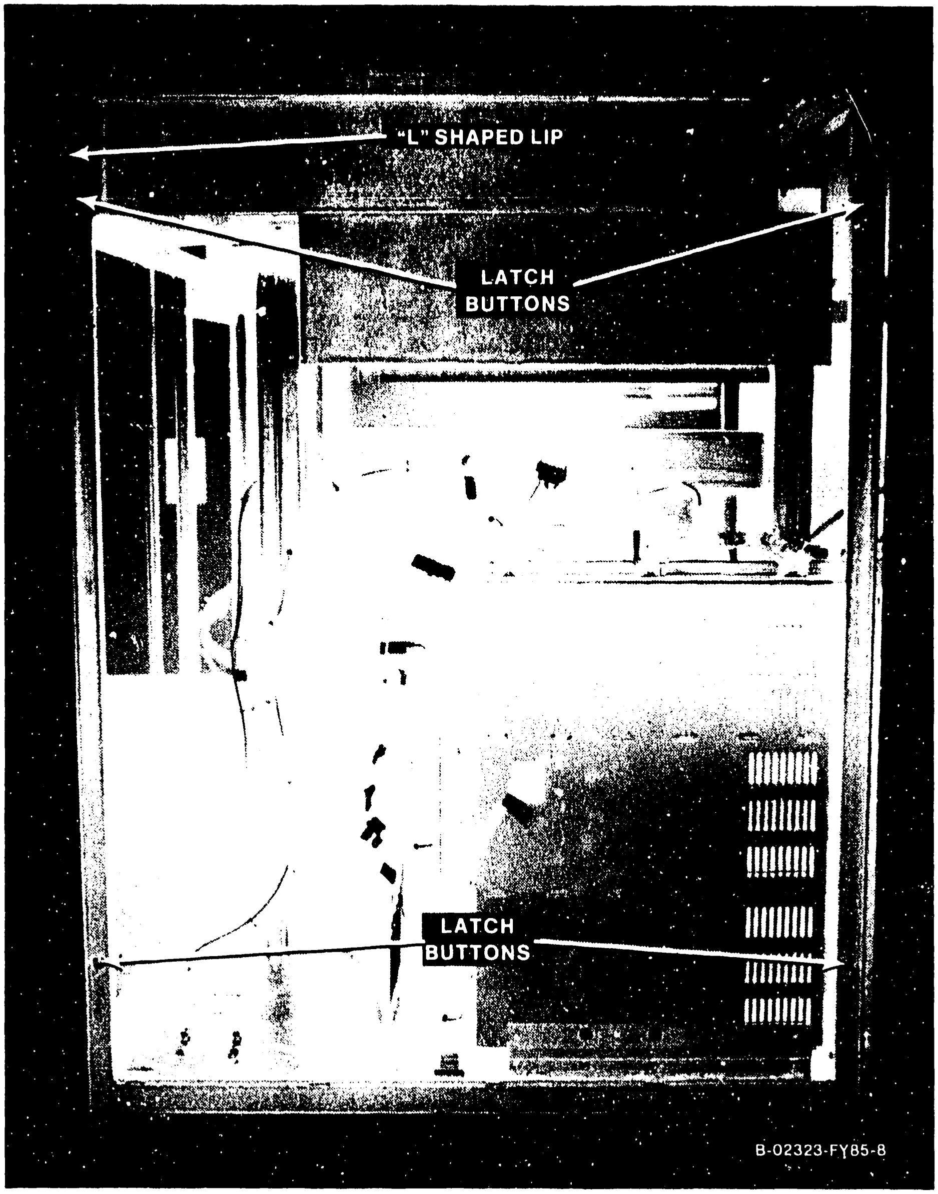


Figure 5-12. Left and Right Side Panel Removal

Reinstall the side panels as follows:

1. Reinstall the side panels by reversing the removal procedure.
2. The panels must be reinstalled with the "L" shaped lip edge toward the rear of the mainframe.

5.3.2.4 CP Circuit Board Removal and Replacement

There are eight different CP boards found in the VS-300. The removal and replacement procedures for the different boards are given in the order in which they are found in the backplane (figure 5-13). A board locator label is mounted on the front of the card cage.

CAUTION

Be careful when replacing the large, flexible VS-300 boards. Make sure that all boards are seated properly in the correct backplane slots. Don't damage the sockets when inserting the boards. Make sure all boards have their component sides facing to the left when viewed from the chassis front.

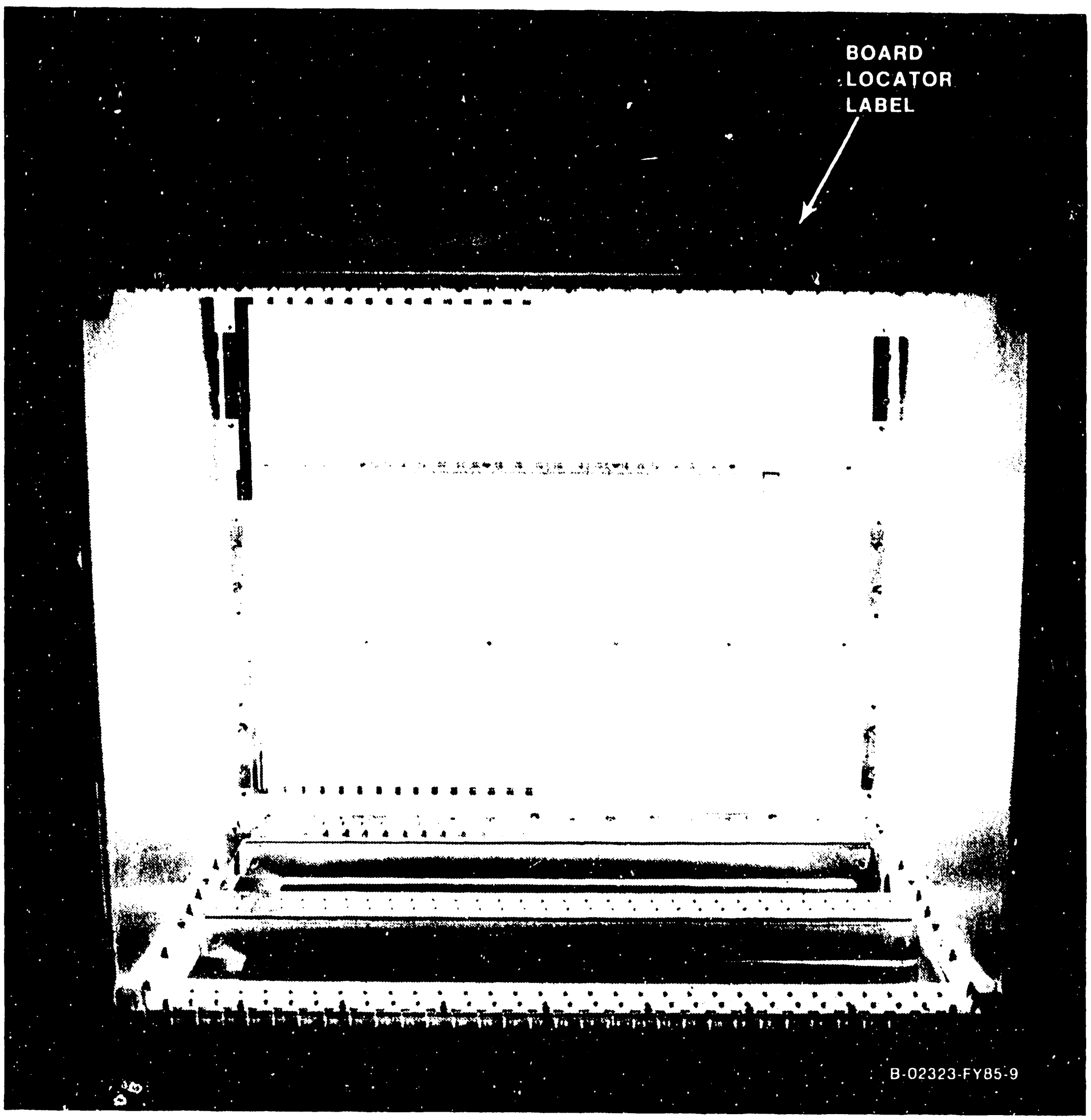


Figure 5-13. VS-300 Card Cage

5.3.2.4.1 210-8830 Floating Point Unit Removal and Replacement

1. Enter Control Mode from the Support Control Unit (SCU) Console Mode Menu, and power down the disk drives.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Open the front hinged door by turning the top and bottom keyed latches (figure 5-9) counterclockwise, unlock the slam latch, and remove the black card cage cover by turning the 1/2 turn fasteners.
4. Each circuit board is held in place by two snap locks. One snap lock tab fits under the edge of the top board guide plate and the second snap lock fits under the edge of the bottom board guide plate.
5. Remove the Floating Point Unit (FPU) (figure 5-14) from backplane slot #1 by lifting the snap locks to free the board from the card cage connectors. Once the board is free of the connectors, ease it forward in the board guides and out of the board cage.
6. Insert the new Floating Point Unit in the board guides and slide it back to the backplane.
7. Make sure the board edge connectors are lined up with the backplane connector slots and the snap lock tabs are under the guide plates.
8. Push back on the snap locks to seat the board in the backplane.

Figure 5-14. 210-8830 Floating Point Unit

5.3.2.4.2 210-8831 Central Processing Unit Removal and Replacement

1. Before removing the Central Processing Unit (CPU), figure 5-15, from backplane slot #2 disconnect the 50-pin cable from J1.
2. Remove the CPU in the manner described in 5.3.2.4.1.
3. After checking the CPU System Address ID jumpers at L50 of the board, install the new CPU.
4. Reconnect the 50-pin cable to J1.

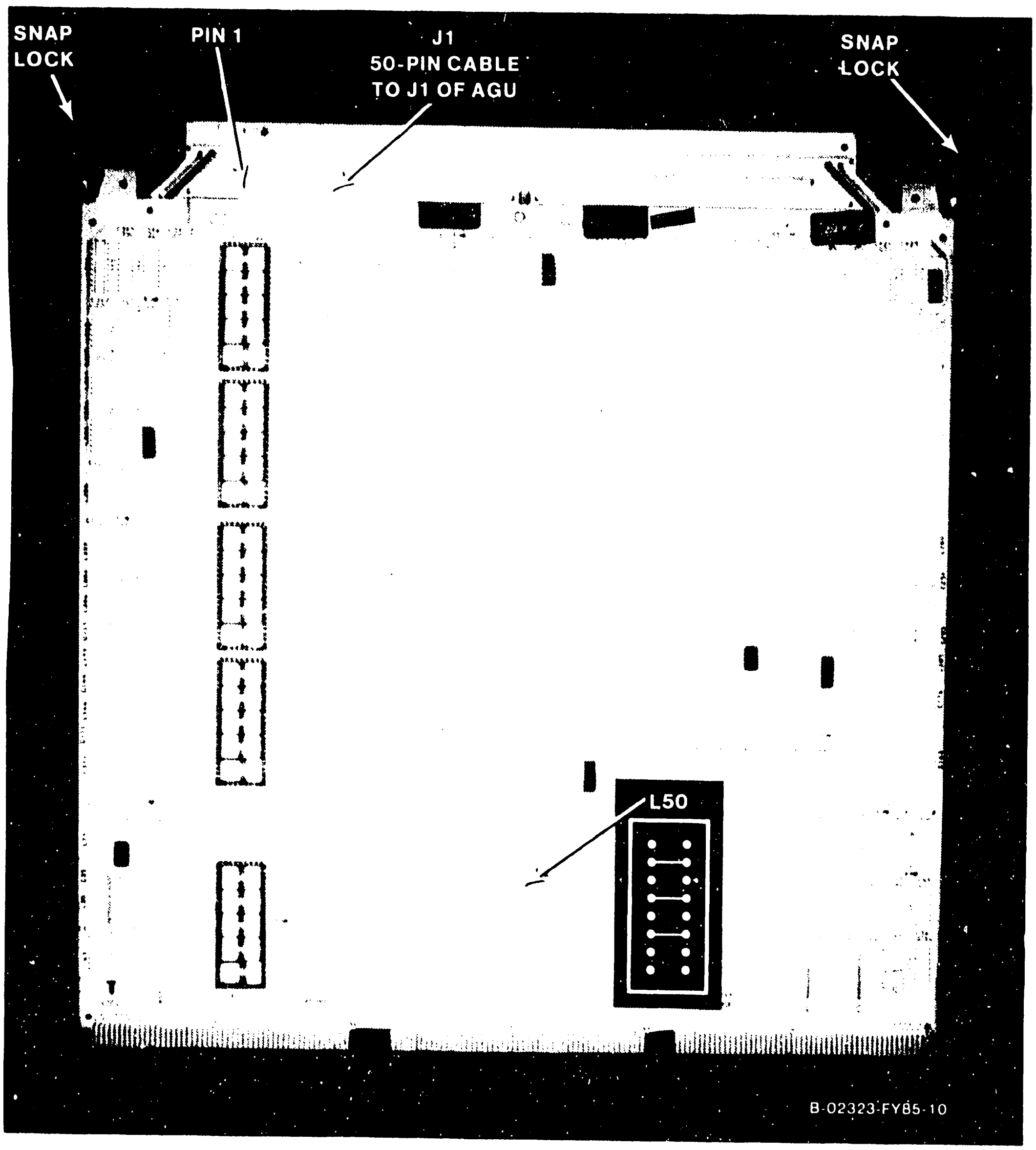


Figure 5-15. 210-8831 Central Processing Unit

5.3.2.4.3 210-8832 Address Generation Unit Removal and Replacement

1. Before removing the Address Generation Unit (AGU), figure 5-16, from backplane slot #3 disconnect the 50-pin cables from J1 and J2.
2. Remove the AGU in the manner described in 5.3.2.4.1.
3. Install the new AGU board.
4. Reconnect the 50-pin cables to J1 and J2.

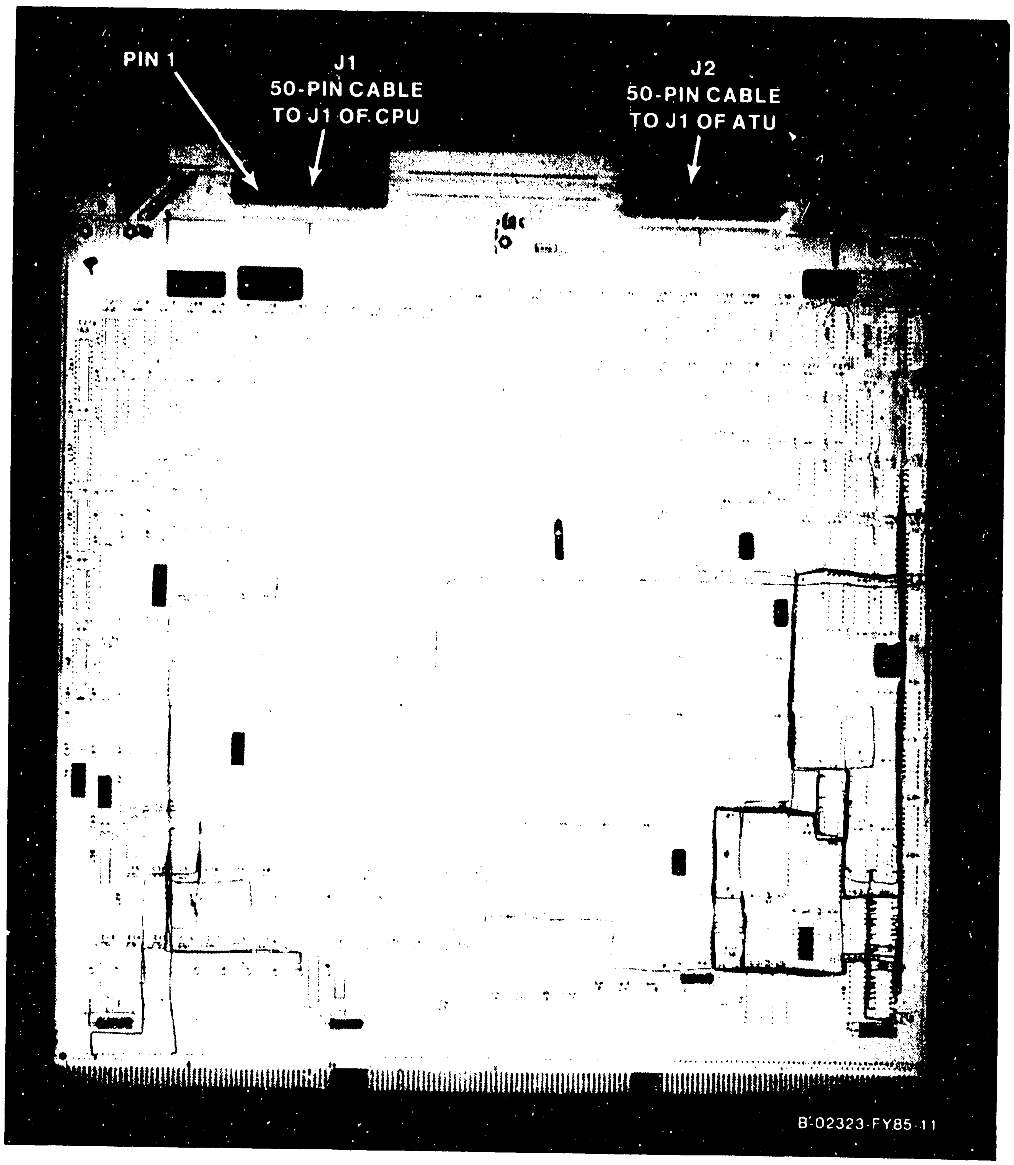


Figure 5-16. 210-8832 Address Generation Unit

5.3.2.4.4 210-8833 Address Translation Unit Removal and Replacement

1. Before removing the Address Translation Unit (ATU), figure 5-17, from backplane slot #4 disconnect the 50-pin cable from J1.
2. Remove the ATU in the manner described in 5.3.2.4.1.
3. After checking the IPC Destination Processor jumpers at L364 or SW1 as shown in figure 5-17, install the new ATU.
4. Reconnect the 50-pin cable to J1.

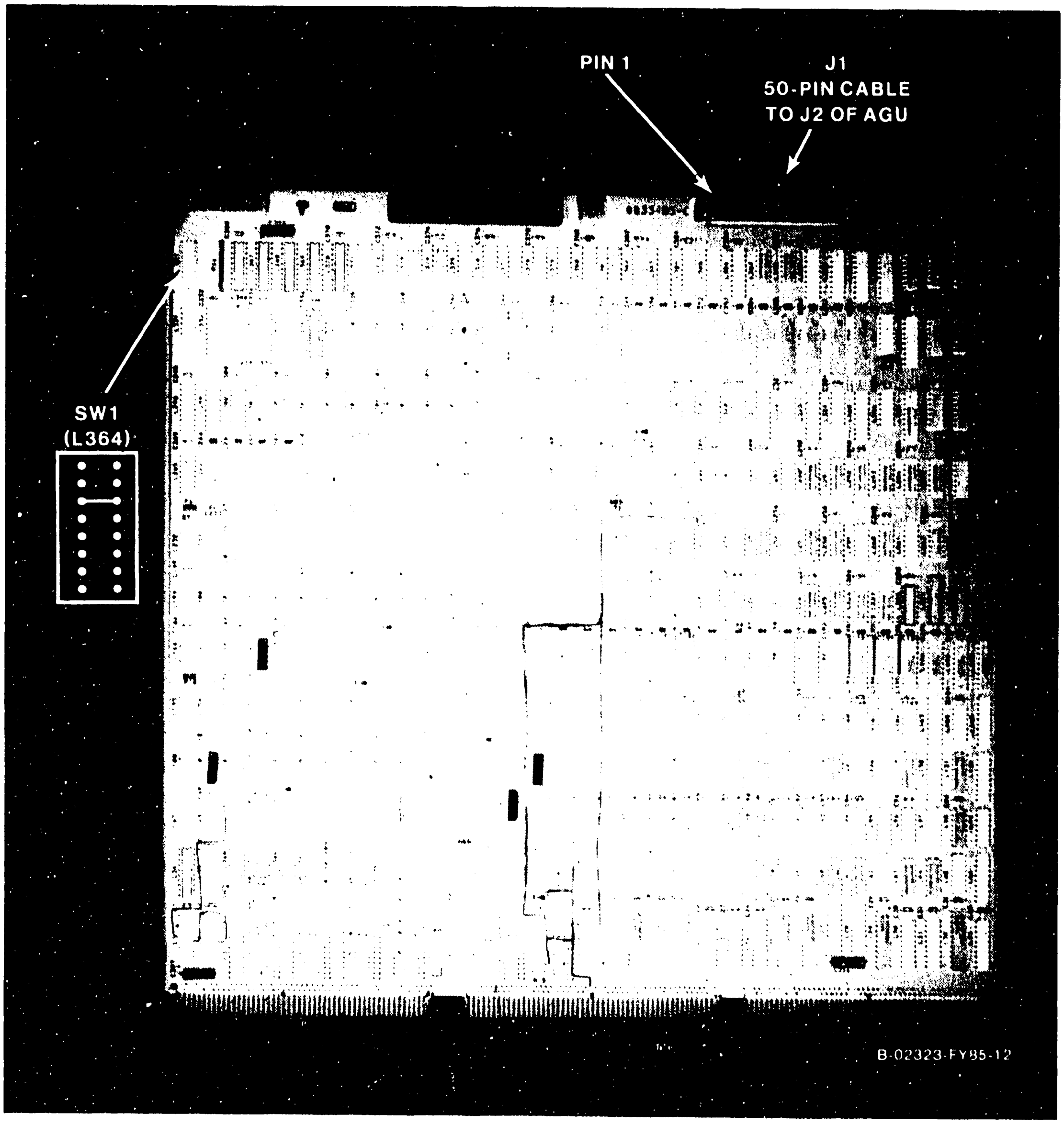


Figure 5-17. 210-8833 Address Translation Unit

5.3.2.4.5 210-8835 Support Control Unit Removal and Replacement

NOTE

The diagnostics refer to this board as the Support Control Unit Interface (SCUI).

1. Remove the Support Control Unit (SCU) (figure 5-18) from backplane slot #5 in the manner described in 5.3.2.4.1. There are no cables, switches, or jumpers on the SCU.
2. Install the new SCU.

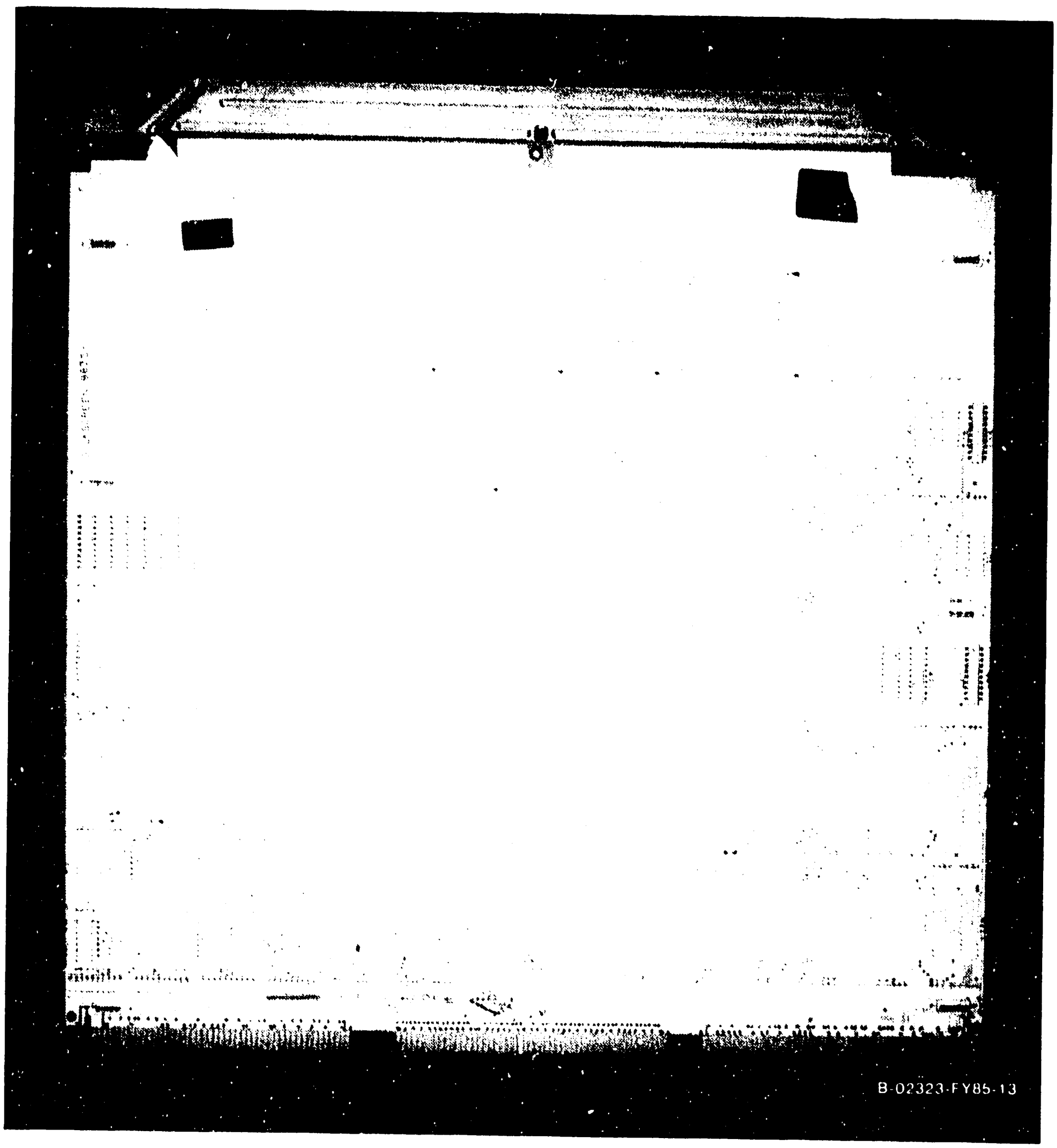


Figure 5-18. 210-8835 Support Control Unit

5.3.2.4.6 210-8834 Memory Control Unit Removal and Replacement

1. Remove the Memory Control Unit (MCU) (figure 5-19) from backplane slot #6 in the manner described in 5.3.2.4.1. No cables are on the MCU.
2. After checking the MCU System Address ID jumpers at L67, MCU Support Packet Bus ID jumpers at L133, and Main Memory Size Selection jumpers at L133 (figure 5-19 and table 5-5), install the new MCU.

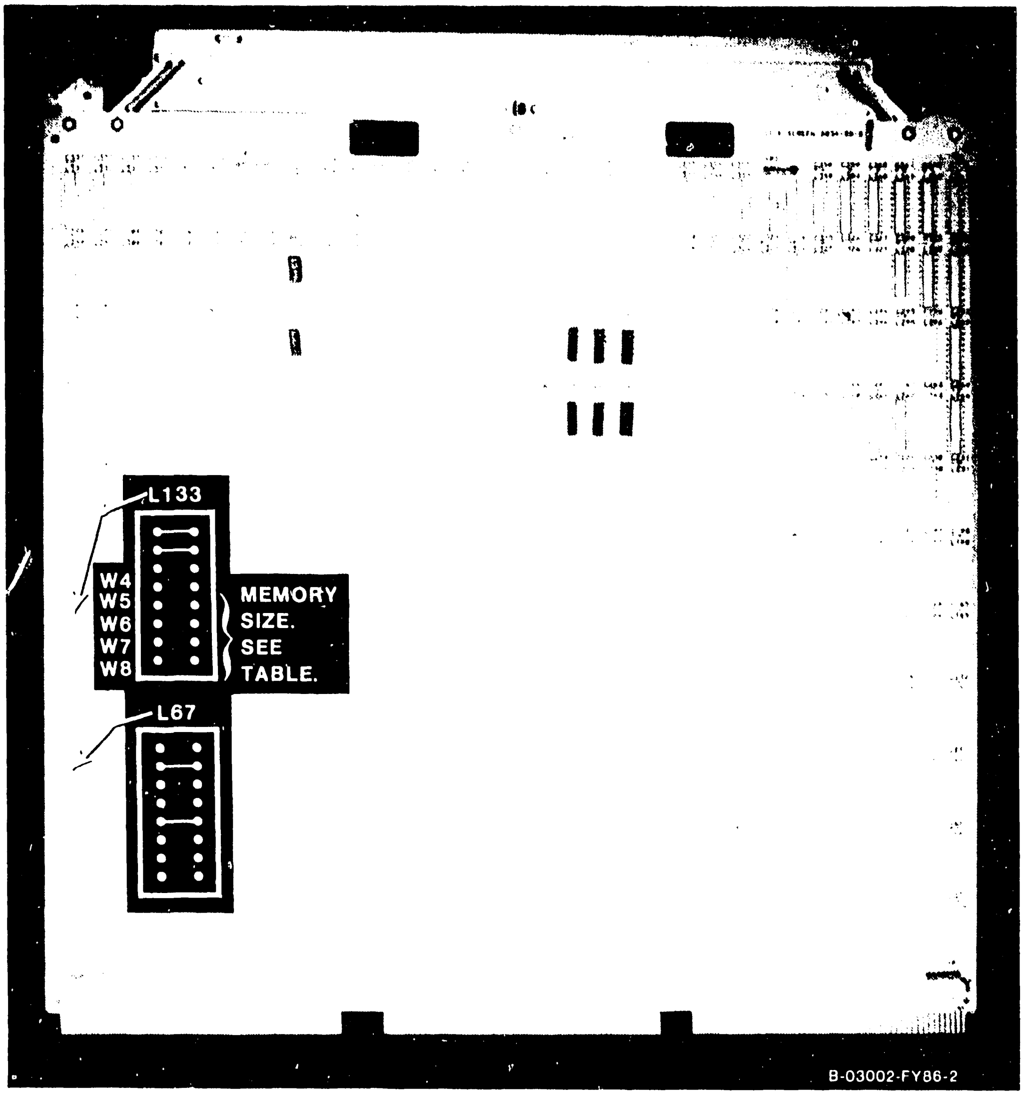


Figure 5-19. 210-8834 Memory Control Unit

Table 5-5. Main Memory Size Selection Jumpers (L133)

Memory Size		4 MEG	8 MEG	12 MEG	16 MEG	20 MEG	24 MEG	28 MEG	32 MEG	36 MEG	40 MEG	44 MEG	48 MEG	52 MEG	56 MEG	60 MEG	64 MEG
Jumper	W4	■		■		■		■		■		■		■		■	
Jumper	W5		■	■			■	■			■	■			■	■	
Jumper	W6				■	■	■	■					■	■	■	■	
Jumper	W7								■	■	■	■	■	■	■	■	
Jumper	W8																■

5.3.2.4.7 210-8703/210-8703-1 Main Memory Removal and Replacement

1. Remove the Main Memory board(s) (figure 5-20) from backplane slot(s) #7 through 14 in the manner described in 5.3.2.4.1.
2. After checking the Memory Module DRAM Loading (table 5-6), install the new Main Memory board. (A 210-8703 board is half-loaded and contains 4 megabytes, while a 210-8703-1 is fully loaded and contains 8 megabytes.)
3. If installing a new board means the main memory capacity will change, refer to paragraph 5.3.2.4.6 for Main Memory Size Selection Jumpers.

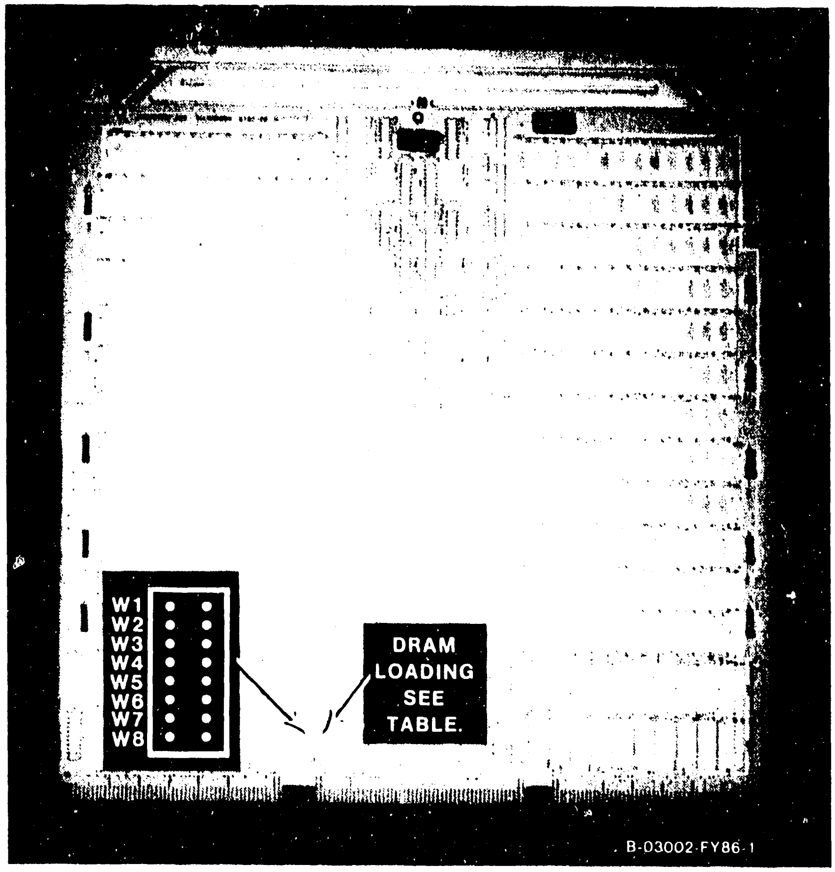


Figure 5-20. 210-8703 Main Memory

Table 5-6. Main Memory Jumper Configurations

Memory Module DRAM Loading	W1	W2	W3	W4	W5	W6	W7	W8
256K Full Load (8 Meg.)		■				■		■
256K Half Load (4 Meg.)			■	■	■			■

NOTE

■ = Jumper in.

5.3.2.4.8 210-8836 System Bus Interface Removal and Replacement

1. Remove the System Bus Interface(s) (SBI) (figure 5-21) from SBI backplane slot(s) #0 or #1 in the manner described in 5.3.2.4.1.
2. After checking the I/O Clock Speed jumpers at L125, I/O Data Speed jumpers at L182, SBI Identification jumpers at L74, and the SPB (Support Packet Bus) Target ID jumpers at L113 (figure 5-21), install the new SBI.

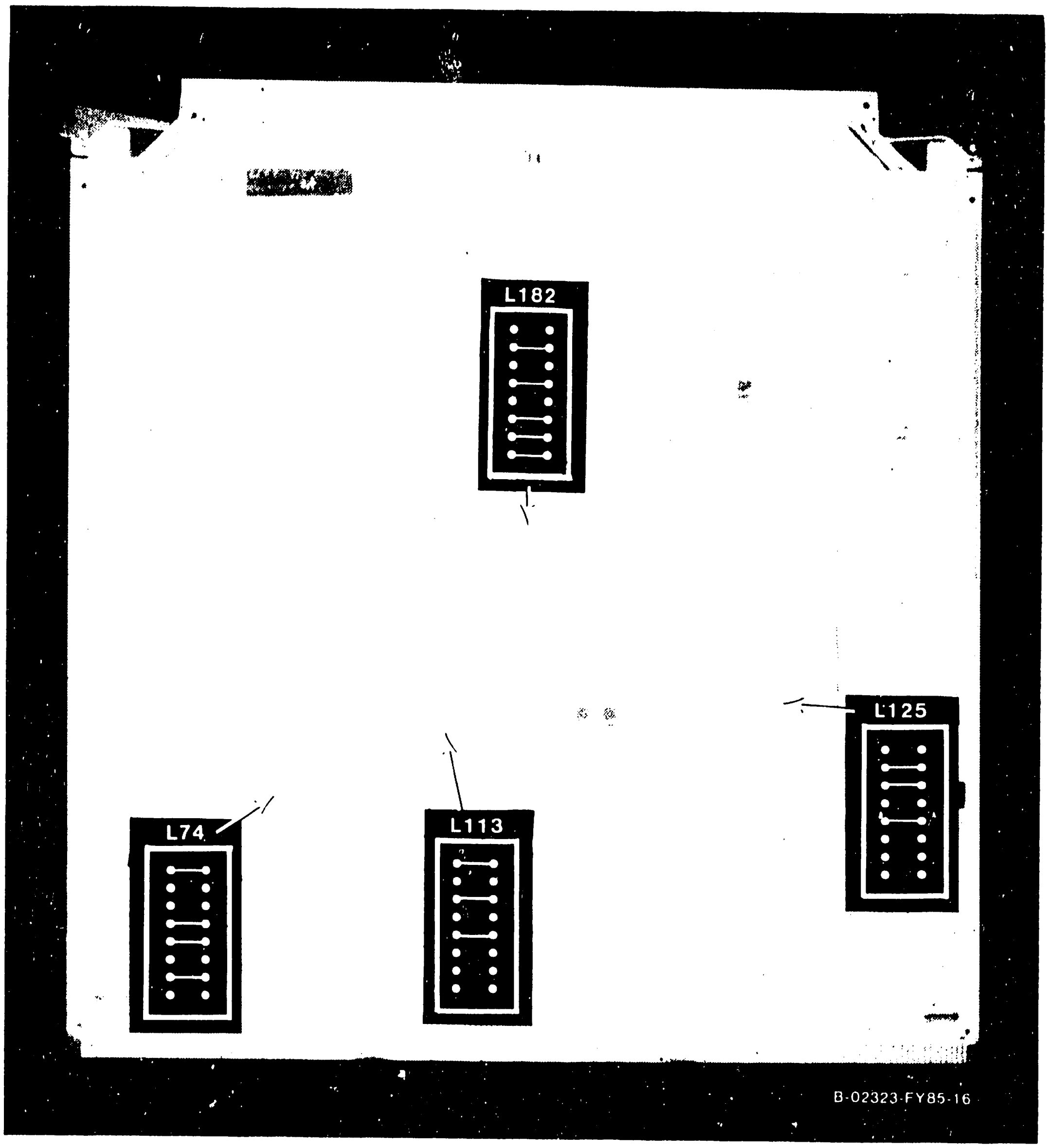


Figure 5-21. 210-8836 System Bus Interface

5.3.2.5 IOC Circuit Board Removal and Replacement

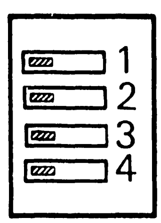
There are six different IOC assemblies used in the VS-300. The removal and replacement procedures for the different assemblies are given in the order in which they are found in the backplane, table 5-7.

NOTE

In the VS-300, the Operating System (OS) requires that I/O slot #1 be reserved for a 23V98 Disk Drive IOC, and I/O slot #3 be reserved for a 23V97 Serial IOC.

Table 5-7. VS-300 IOC List

IOC Type	WLI Part Number	IOC Priority	Physical Backplane Slot Number
System Bus Interface	210-8836		SBI #0 (SBI #1 for 2nd SBI)
SMD (23V98-1/2/3/4)	210-8785	1	I/O #1
32-Port Serial (23V97)	210-8609	3	I/O #3
Kennedy Tape (23V95-1)	210-8790		
Telex Tape (23V95-2)	210-8789		
Multiline TC (23V86/96)	210-8491A		
CIU BLANC (23V79)	210-8392A		



= switch position

B-02675-FY86-11

NOTE

This switch is set the same for all IOCs except the 23V79 CIU BLANC IOC. See each IOC for the location of the switch.

Figure 5-22. IOC Diagnostic Switch Setting For Power Up (Except 23V79 [210-8392] CIU BLANC IOC)

5.3.2.5.1 23V97 (210-8609) Serial IOC Removal and Replacement

1. The 23V97 drives up to four Active Port Assemblies mounted on the rear panel or in the Cable Concentrator unit. Each APA drives up to eight serial device ports. The IOC also supports the 6550 Gate Array TC controller and the P-Band WangNet modems, via the Cable Concentrator. Connector J1 on the IOC is always reserved for P-Band. No other type of devices should be connected to J1.
2. Disconnect all cables from the top of the 23V97 Serial IOC (figure 5-23). Note the position of all cables for later reassembly.
3. Remove the IOC in the manner described in 5.3.2.4.1.
4. After checking the Diagnostic switch setting at L194 as shown in figure 5-22, install the new 23V97.
5. Reconnect all cables.

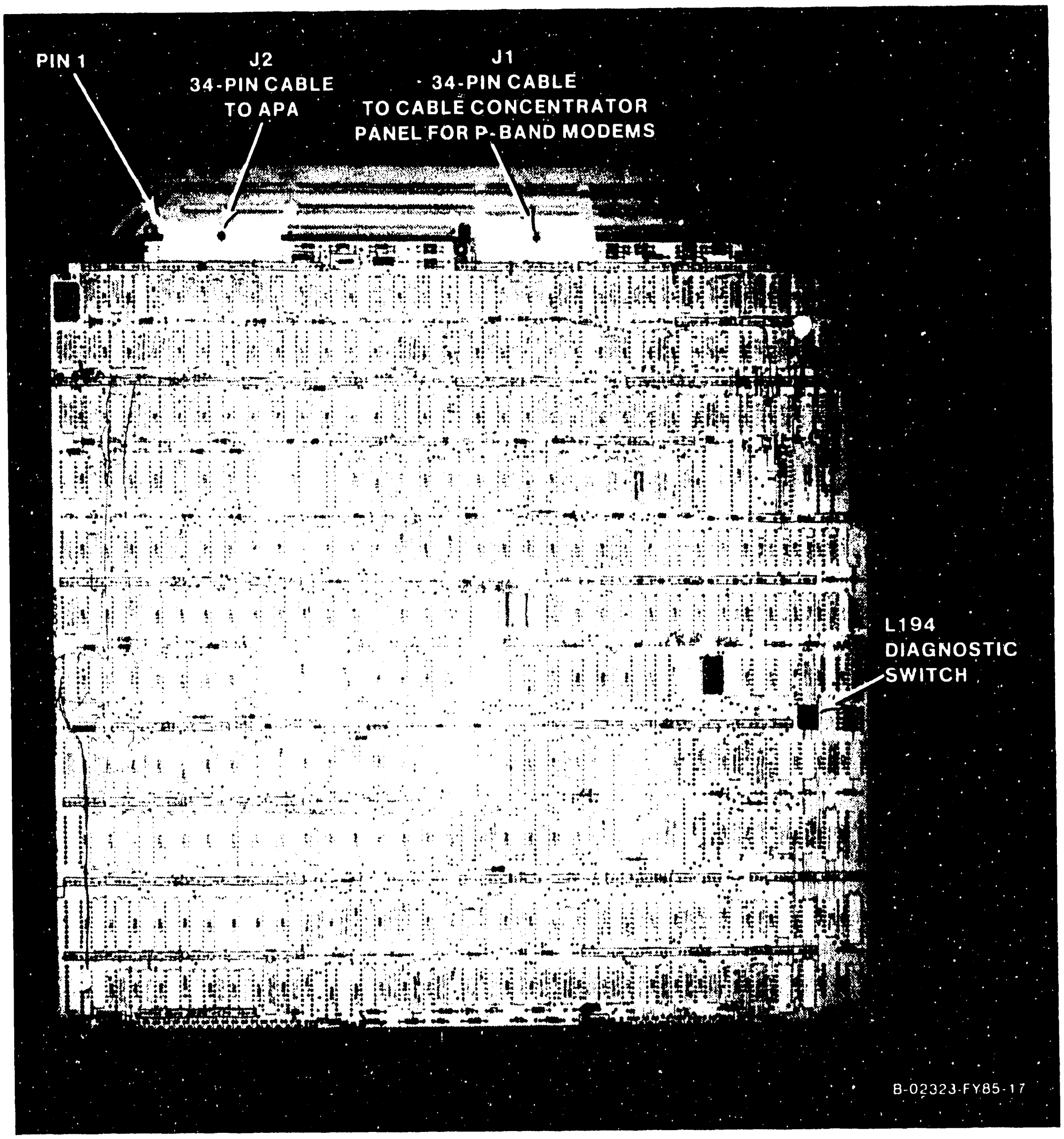


Figure 5-23. 23V97 Serial IOC

5.3.2.5.2 270-0975 Serial IOC APA

1. The 270-0975 Serial Active Port assembly (APA) consists of the 210-8504 APA board and the 210-8509 BNC/TNC board. The assembly is daisy chained to include up to four APA back panels.
2. Figure 5-24 shows one assembly and figure 5-25 shows four assemblies daisy chained. The last APA must be terminated at J2 with a 210-8503 terminator board.

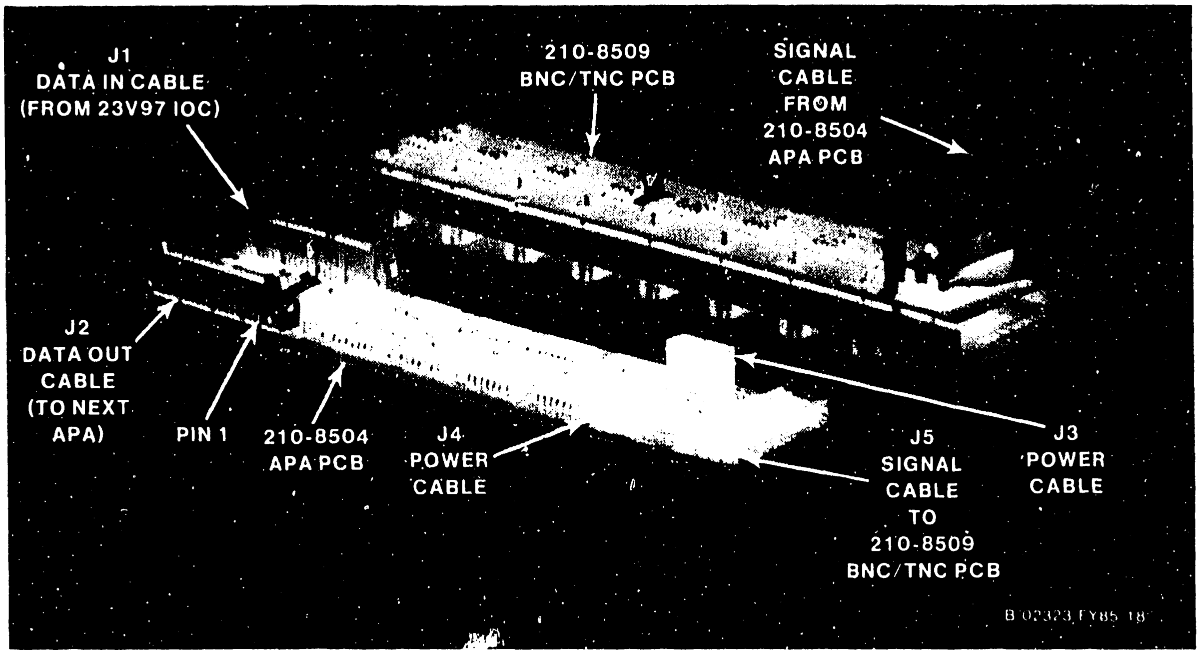


Figure 5-24. 270-0975 APA Assembly

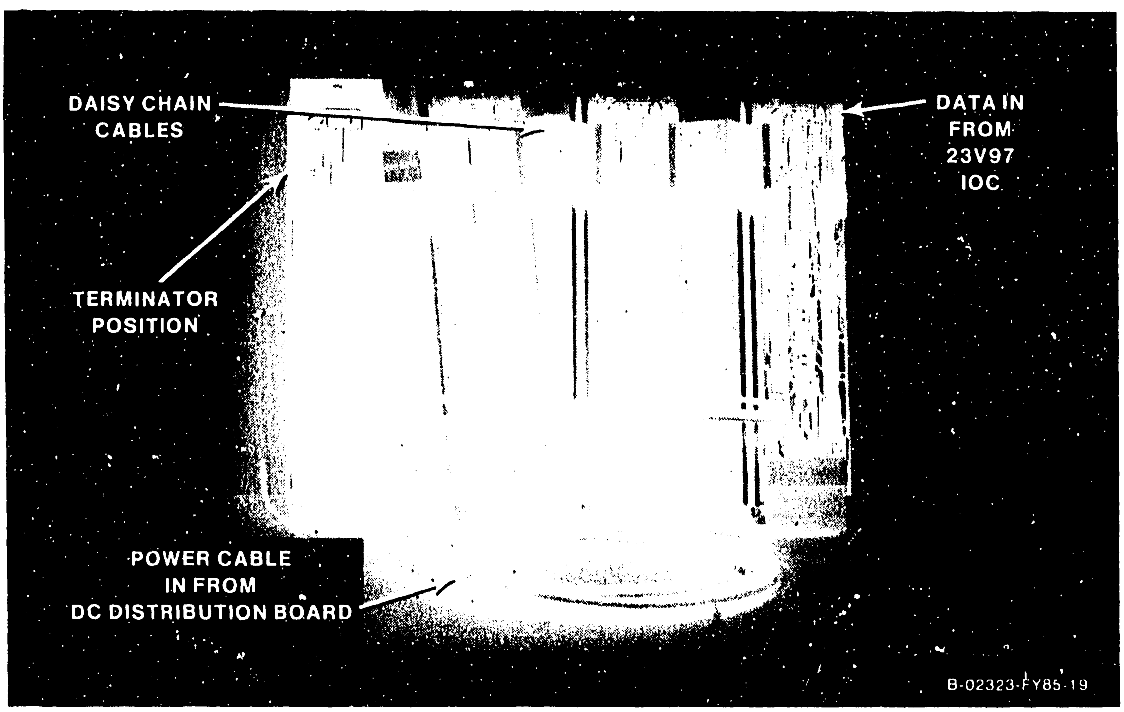


Figure 5-25. Daisy Chained APA Assemblies

5.3.2.5.3 6550 Gate Array TC Controller Assembly Removal and Replacement

1. The 6550 Gate Array TC assembly consists of one 210-8714 CPU/Gate Array board, one 210-8713 Receiver/Driver board, and one 210-8712 Connector board. Order and replace the entire 6550 Gate Array assembly (WLI P/N 270-1016). Do not replace individual PC boards.
2. Figure 5-26 shows the Gate Array TC back panel assembly, figure 5-27 shows the 210-8714 CPU/Gate Array board, and figure 5-28 shows one CPU/Gate Array board with cabling. Power cabling is not daisy-chained to a second Gate Array back panel assembly.
3. Before installing the new 6550 Gate Array TC back panel assembly, check the 8-position DIP switch at SW1, and the jumpers at J5 and J6 as shown in figure 5-27. (Switches 5 and 6 are On for support of 128K byte Gate Array without X.21 protocol; switches 5, 6, and 7 are On for support of 128K byte Gate Array with X.21 protocol; all other switches should be off.)

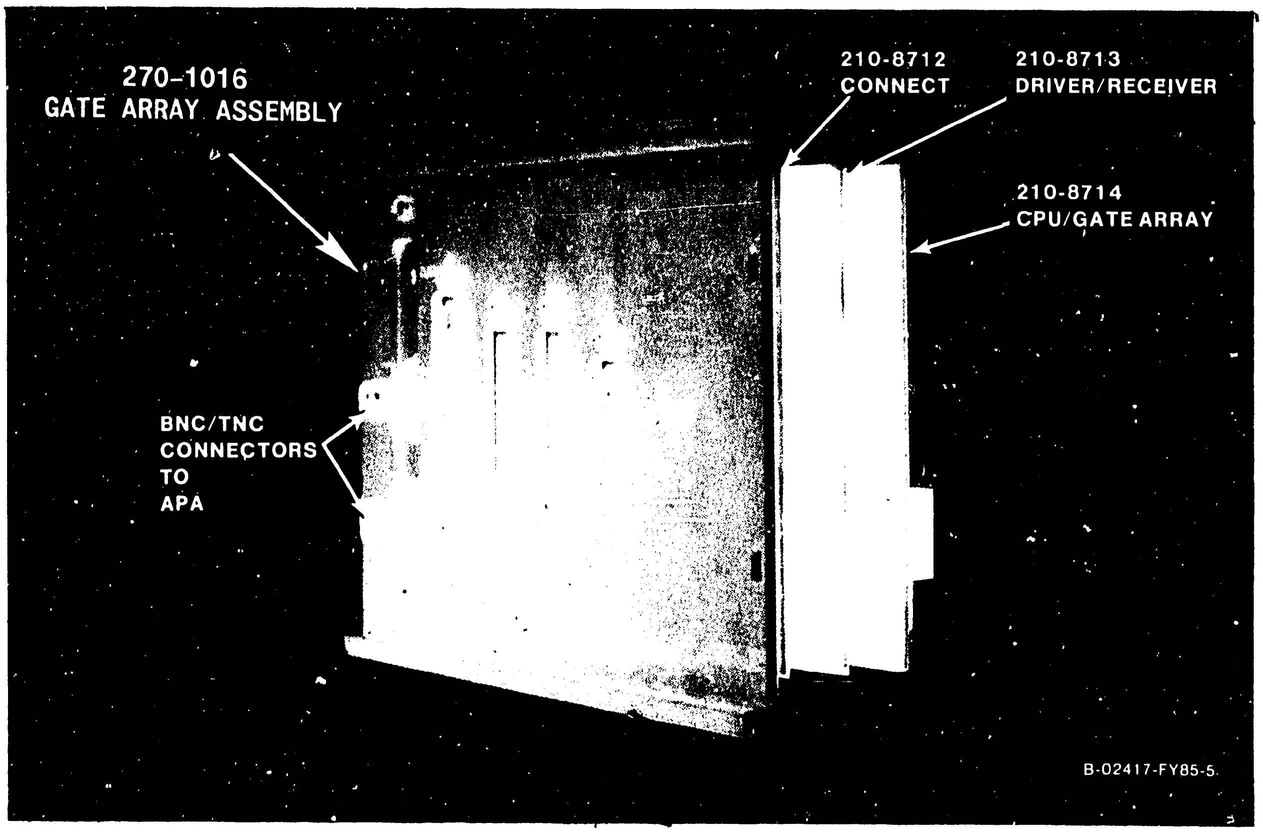


Figure 5-26. 270-1016 6550 Gate Array TC Back Panel Assembly

NOTE

Revisions are being made to the 210-8714 CPU/Gate Array board for RS232 E.I.A. interface compatibility, as follows:

1. Operational

a. Existing 210-8714 E0/R0 board now provides a clock on RS232 non-standard interface pin 11. This board is compatible only with existing Wang 2228N Null Modems.

b. New 210-8714 E1/R0 board will provide a clock on RS232 standard interface pin 24. This board will be compatible only with the new Null Modem, WLI P/N XXX-XXXX.

c. Future 210-8714 E1/R1 board will have a jumper to allow selection of either a clock on RS232 interface pin 24, or on both pin 11 and pin 24. This board will be compatible with existing 2228N Null Modems and the new Null Modem.

2. Test Fixtures

a. Existing 210-8714 E0/R0 board is supported by the existing RS232/366 Loopback Plug, WLI P/N 420-1041.

b. New 210-8714 E1/R0 board will not be supported by any Loopback Plug. However, the EIA Interface Test Set (breakout box), WLI P/N 727-0122, may be used. (The breakout box is required because the Loopback Plug - WLI P/N 420-1041 - cannot support clock on RS232 pin 24.) This requires the following pins on the breakout box to be strapped together, as follows:

1) Pins 2 and 3.
2) Pins 4, 5, and 8.
3) Pins 11, 15, 17, and 24
4) Pins 6 and 20

c. Future 210-8714 E1/R1 board will be supported by the existing RS232/366 Loopback Plug. To use the RS232/366 Loopback Plug, DTE clock on pin 11 must be enabled. However, when this board is used with a modem that has internal clock selected, DTE clock must be disabled.

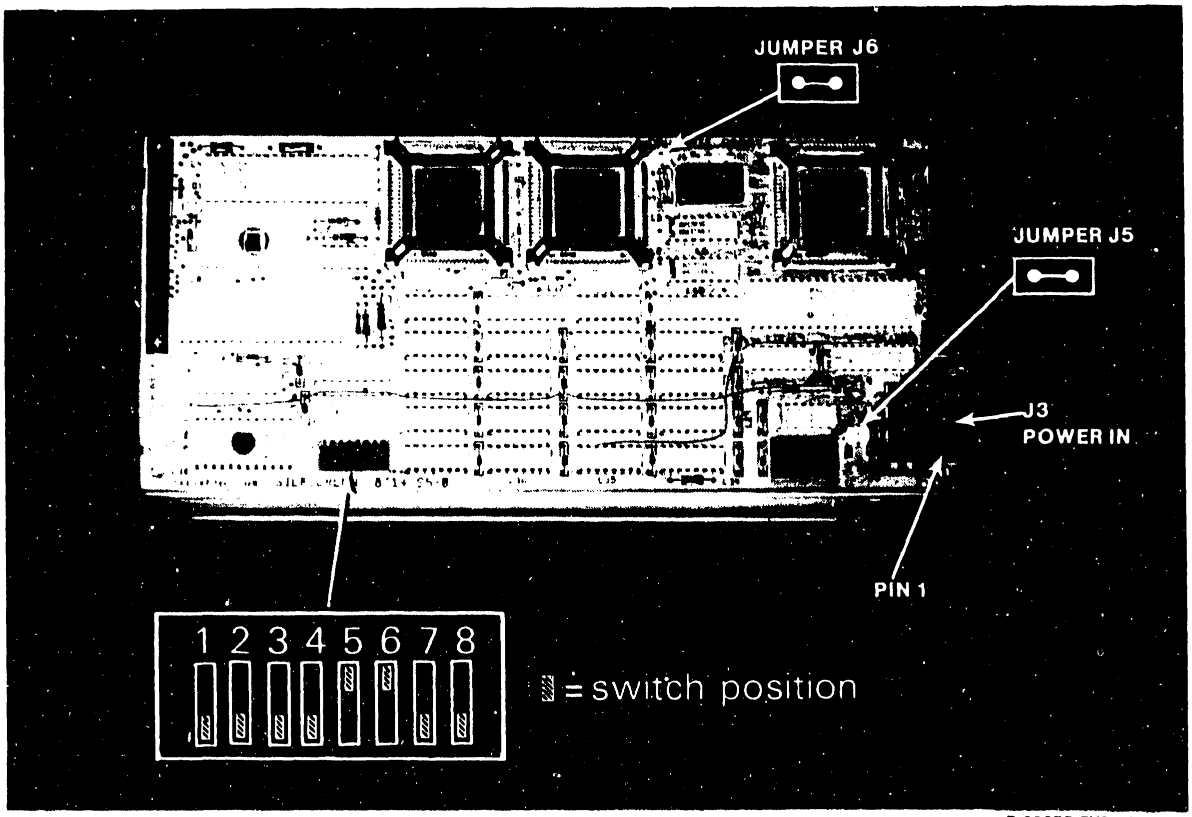


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Figure 5-27. 210-8714 CPU/Gate Array Board

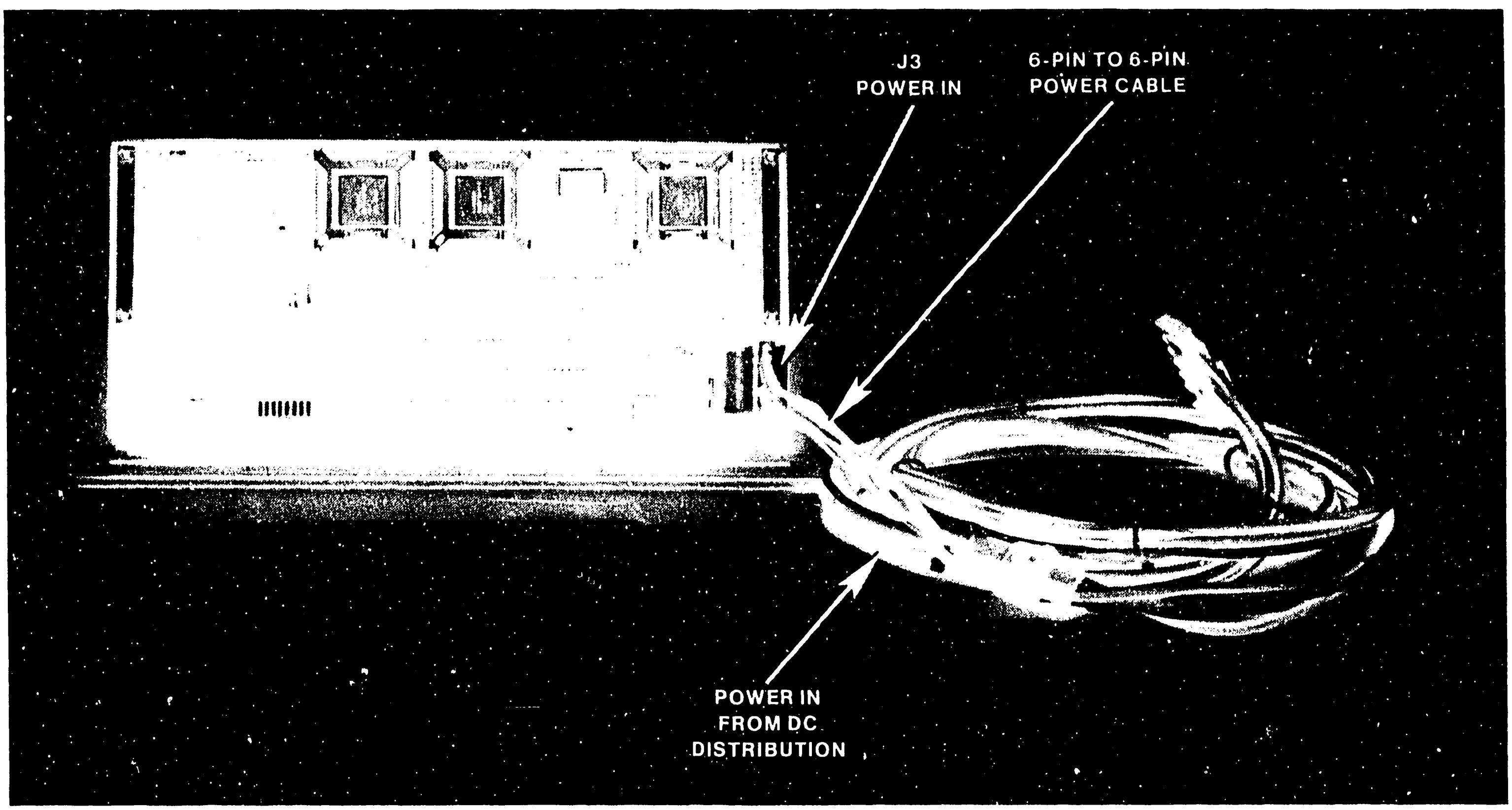

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Figure 5-28. 210-8714 CPU/Gate Array Board with Cabling

5.3.2.5.4 23V98-1/2/3/4 (210-8785) Disk Drive IOC Removal and Replacement

1. Disconnect all cables from the top of the 23V98 Disk Drive IOC (figure 5-29). Note the position of all cables for later reassembly.
2. Remove the IOC in the manner described in 5.3.2.4.1.
3. Check the device type switches (figures 5-29 and 5-30, and table 5-8). The two 8-position disk device type switches, SW1 (L76) and SW2 (L51), define the type of drive connected to the 23V98 IOC, ports 0-3. Set the switches for the type of drive(s) connected to the IOC.
4. After checking the Diagnostic switch setting at L247 as shown in figure 5-22, install the new 23V98.
5. Reconnect all cables.

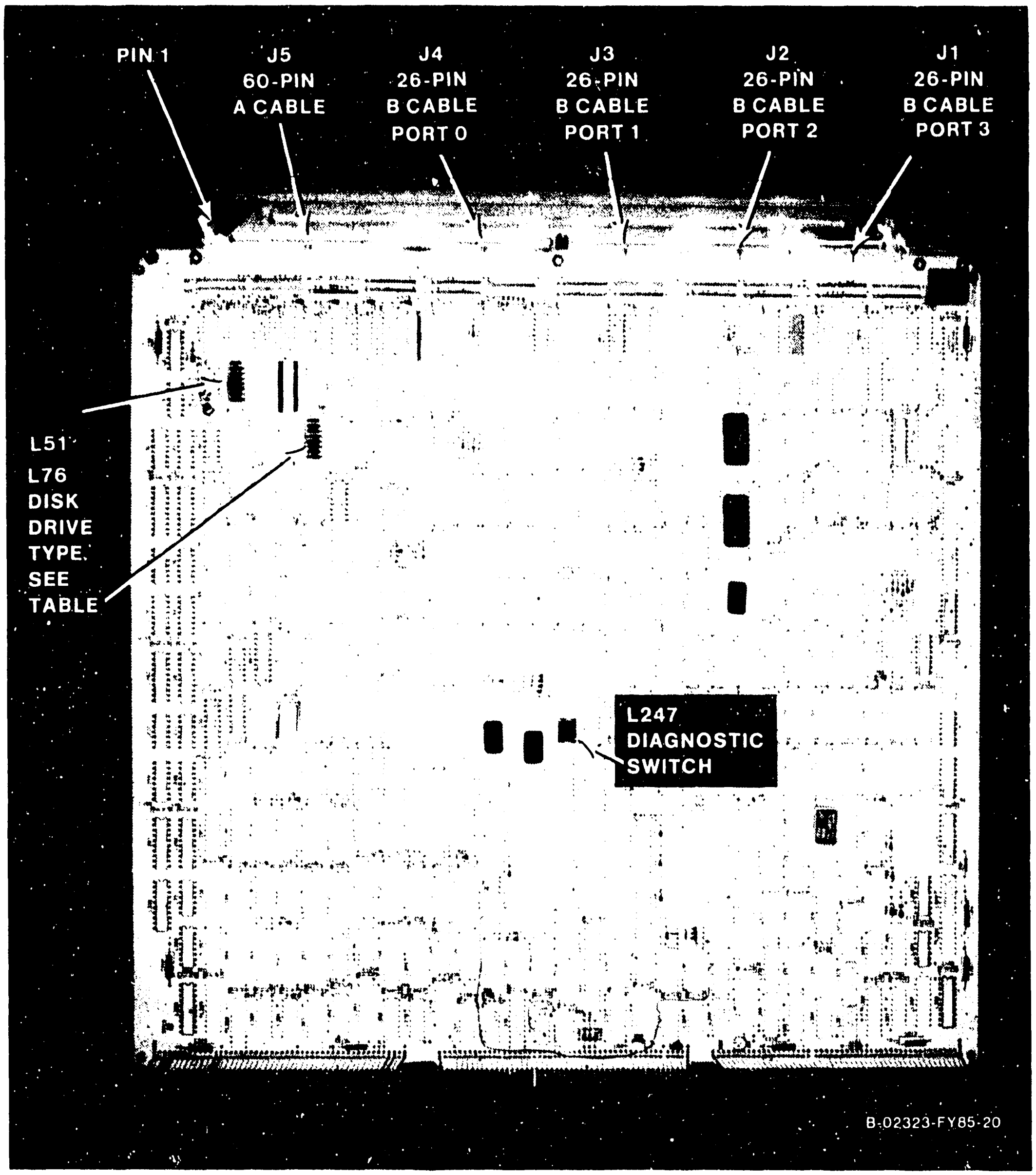

Figure 5-29. 23V98 Disk Drive IOC

	Open (Off)		Closed (On)
Bit 1		1	Port 0
Bit 2		2	
Bit 3		3	
Bit 4		4	
Bit 1		5	Port 1
Bit 2		6	
Bit 3		7	
Bit 4		8	

SW2 (L51)

	Open (Off)		Closed (On)
Bit 1		1	Port 2
Bit 2		2	
Bit 3		3	
Bit 4		4	
Bit 1		5	Port 3
Bit 2		6	
Bit 3		7	
Bit 4		8	

SW1 (L76)

Figure 5-30. Disk Drive Device Type Switch Settings.

Table 5-8. Disk Drive Types (Formatted)

Drive Type	Bit 1	Bit 2	Bit 3	Bit 4	Hex Code
75Meg SMD/76Meg RSD	Closed	Closed	Closed	Closed	0
288Meg SMD	Open	Closed	Closed	Closed	1
30Meg CMD	Closed	Closed	Open	Closed	4
60Meg CMD	Open	Closed	Open	Closed	5
90Meg CMD	Closed	Open	Open	Closed	6
76Meg NEC	Open	Closed	Closed	Open	9
147Meg NEC	Closed	Open	Closed	Open	A
600Meg FMD	Open	Open	Closed	Open	B
454Meg CDC/FSD	Closed	Closed	Open	Open	C
No Drive	Open	Open	Open	Open	F

5.3.2.5.5 23V95-1 (210-8790) Kennedy Tape IOC Removal and Replacement

1. Disconnect all cables from the top of the 23V95-1 Kennedy Tape IOC (figure 5-31). Note the position of all cables for later reassembly.
2. Remove the IOC in the manner described in 5.3.2.4.1.
3. After checking the Diagnostic switch setting at L130 as shown in figure 5-22, install the new 23V95-1.
4. Reconnect all cables.

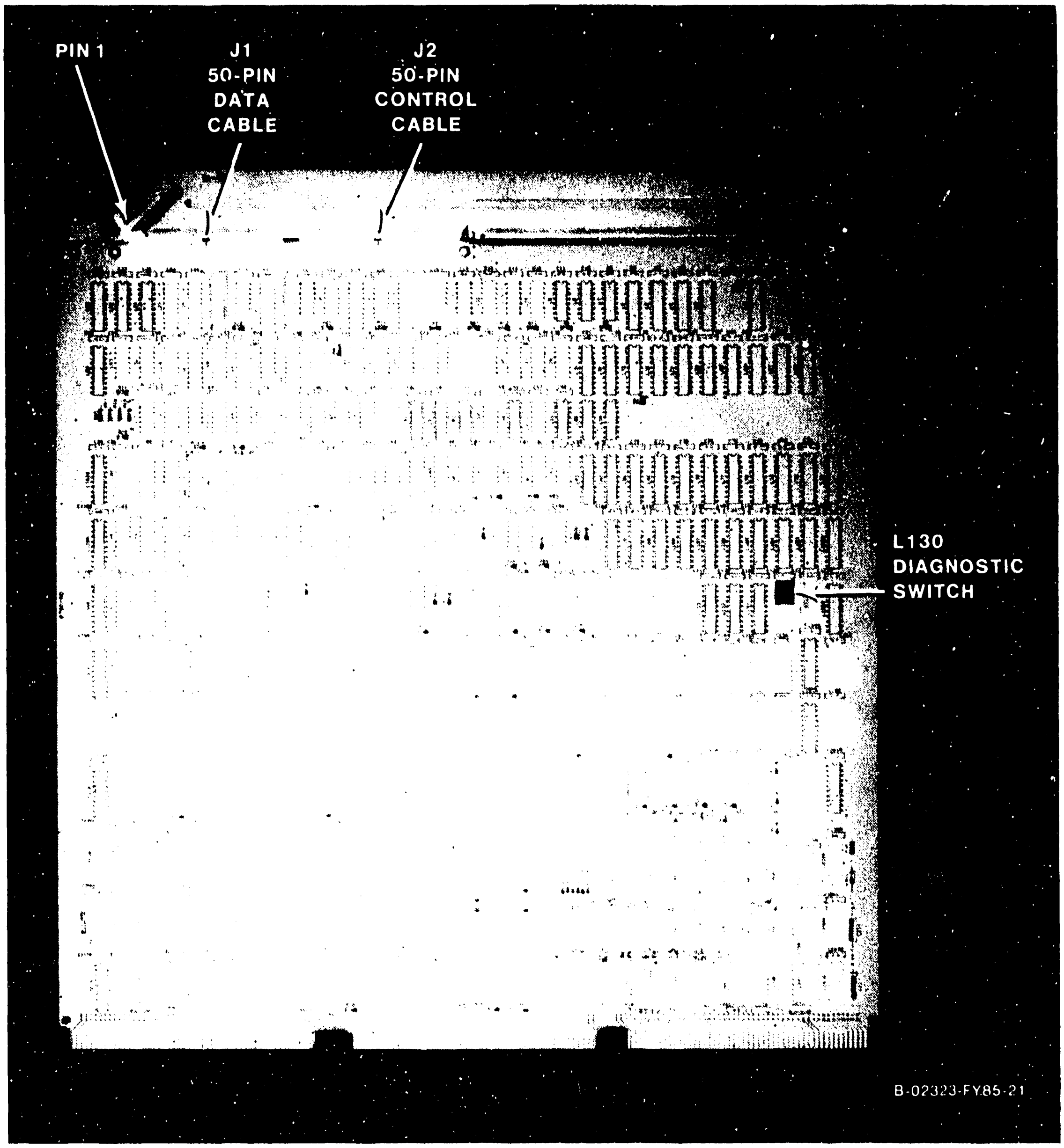

Figure 5-31. 23V95-1 Kennedy Tape IOC

5.3.2.5.6 23V95-2 (210-8789) Telex Tape IOC Removal and Replacement

1. Disconnect all cables from the top of the 23V95-2 Telex Tape IOC (figure 5-32). Note the position of all cables for later reassembly.
2. Remove the IOC in the manner described in 5.3.2.4.1.
3. After checking the Diagnostic switch setting at SW1 as shown in figure 5-22, install the new 23V95-2.
4. Reconnect all cables.

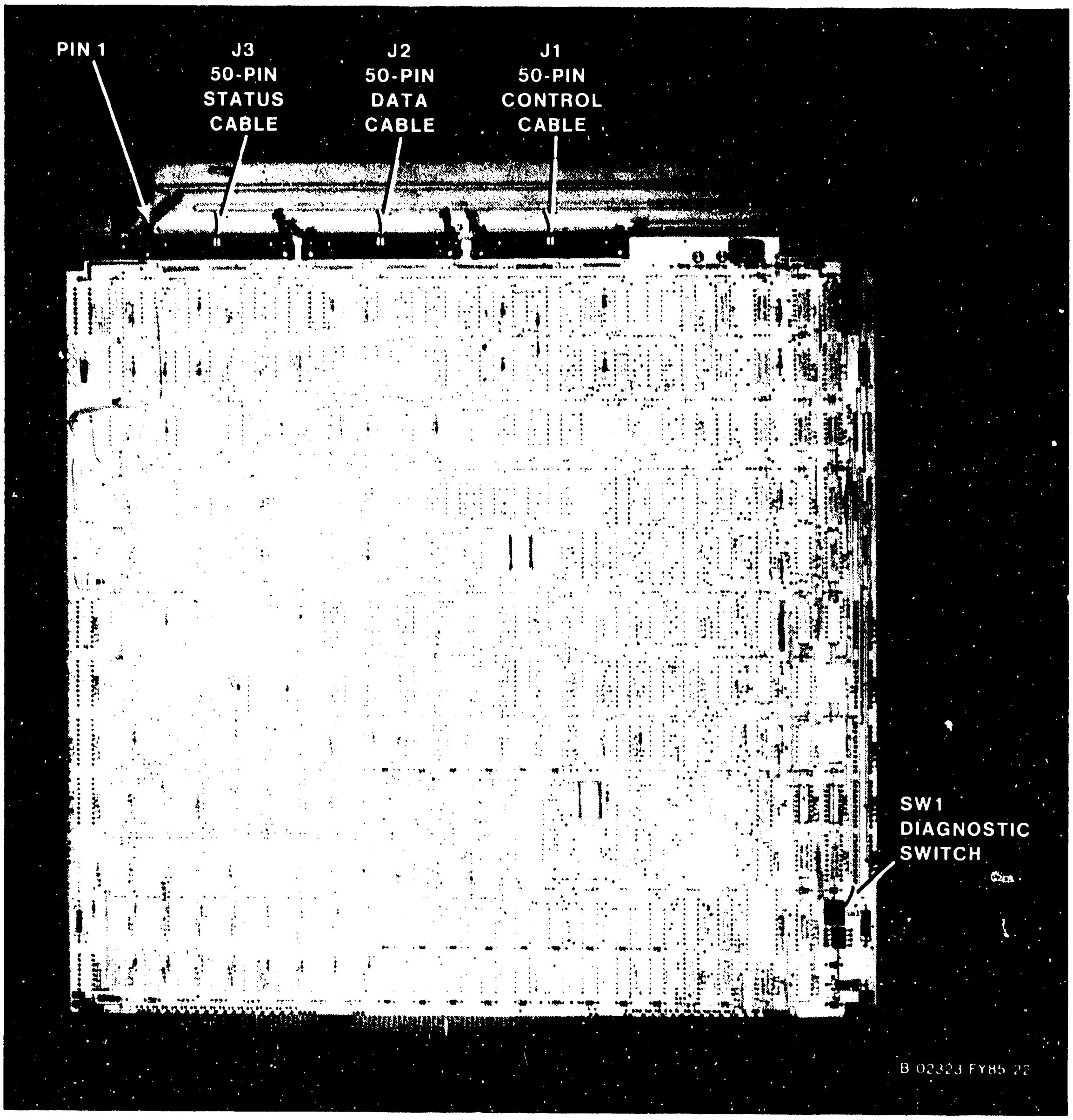

Figure 5-32. 23V95-2 Telex Tape IOC

5.3.2.5.7 23V96 (210-8491) Multiline TC IOC Removal and Replacement

1. The 23V96 drives up to four Multiline TC (MLTC) back panels. Each back panel drives up to four TC lines.
2. Disconnect all cables from the top of the 23V96 Multiline TC IOC (figure 5-33). Note the position of all cables for later reassembly.
4. Remove the IOC in the manner described in 5.3.2.4.1.
5. Check the 8-position port select loop back test switch at L228. (Figure 5-33, and table 5-9.) For normal power up, all switches are on.
6. After checking the Diagnostic switch setting at L202 as shown in figure 5-22, install the new 23V96.
7. Reconnect all cables.

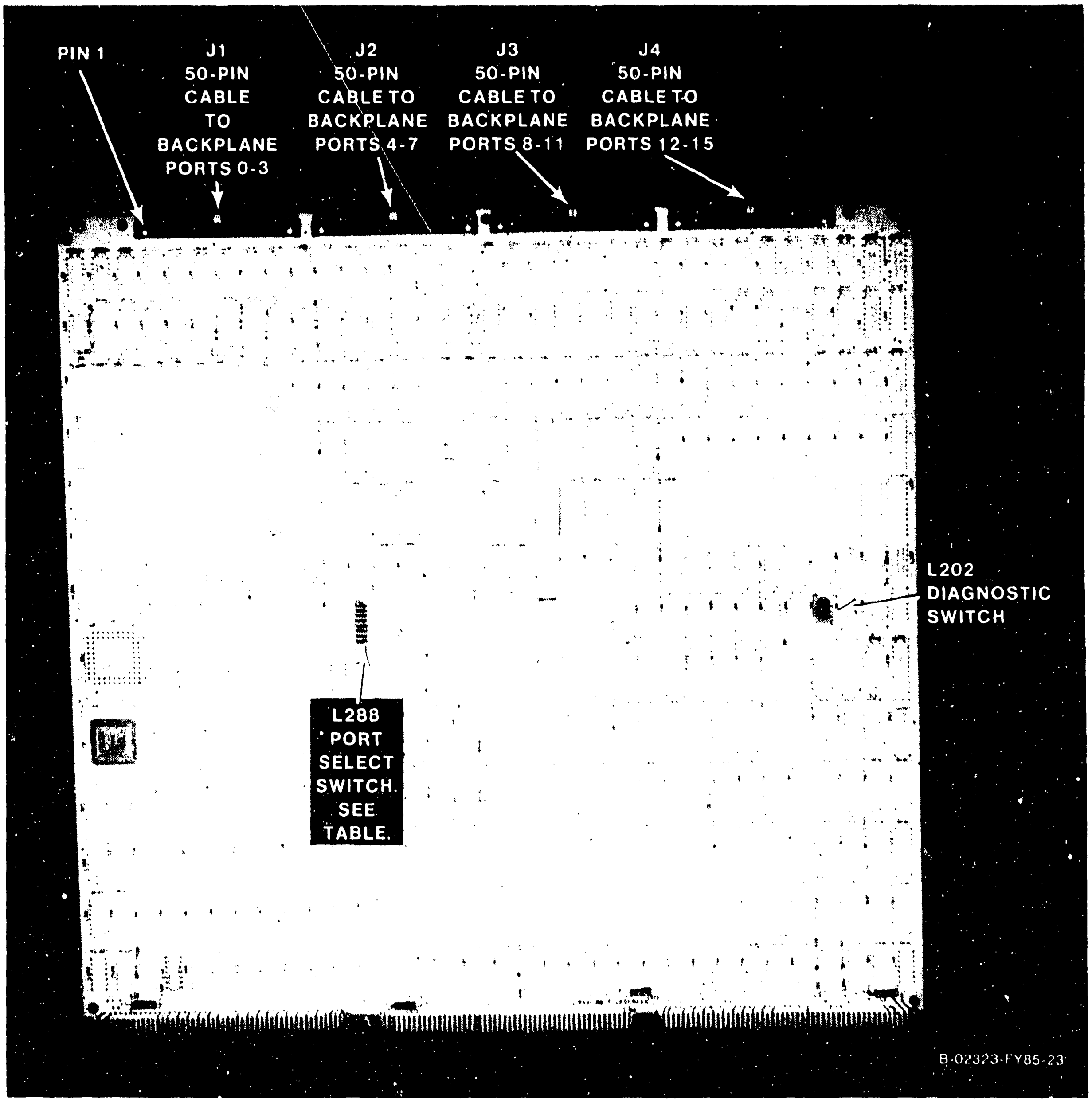

Figure 5-33. 23V96 Multiline TC (MLTC) IOC

Table 5-9. 23V96 Multiline TC IOC Port Select Switch Settings For Loopback Test

S8	S7	S6	S5	S4	S3	S2	S1	
				Closed	Closed	Closed	Closed	Select Port 0 (If 5 Open)
				Closed	Closed	Closed	Open	Select Port 1 (")
				Closed	Closed	Open	Closed	Select Port 2 (")
				Closed	Closed	Open	Open	Select Port 3 (")
				Closed	Open	Closed	Closed	Select Port 4 (")
				Closed	Open	Closed	Open	Select Port 5 (")
				Closed	Open	Open	Closed	Select Port 6 (")
				Closed	Open	Open	Open	Select Port 7 (")
				Open	Closed	Closed	Closed	Select Port 8 (")
				Open	Closed	Closed	Open	Select Port 9 (")
				Open	Closed	Open	Closed	Select Port 10 (")
				Open	Closed	Open	Open	Select Port 11 (")
				Open	Open	Closed	Closed	Select Port 12 (")
				Open	Open	Closed	Open	Select Port 13 (")
				Open	Open	Open	Closed	Select Port 14 (")
				Open	Open	Open	Open	Select Port 15 (")
			Closed					Deselects single channel mode.
			Open					Selects single chan. mode (Sws. 1 → 4 select chan.)
								Not used
Closed								Deselects burn-in
Open								Selects burn-in

NOTES

1. Location of switch is L228.
2. For normal operation, all L202 Diagnostic switches must be as shown in figure 5-22, and all L228 switches must be Closed (on).
3. To select burn-in, switch 8 Open (off), all others Closed (on).

5.3.2.5.8 270-1003 Multiline TC Back Panel Assembly

1. The 270-1003 Multiline TC back panel assembly consists of one 210-8496 Serial Communications Link (SCL) board, two 210-8497 Block Connector boards, and up to four interface boards with displays. Replace individual PC boards. Do not order or replace the entire assembly.
2. Figure 5-34 shows the Multiline TC back panel assembly, and figure 5-35 shows one assembly with cabling. Power cabling is daisy-chained to a second MLTC back panel assembly.

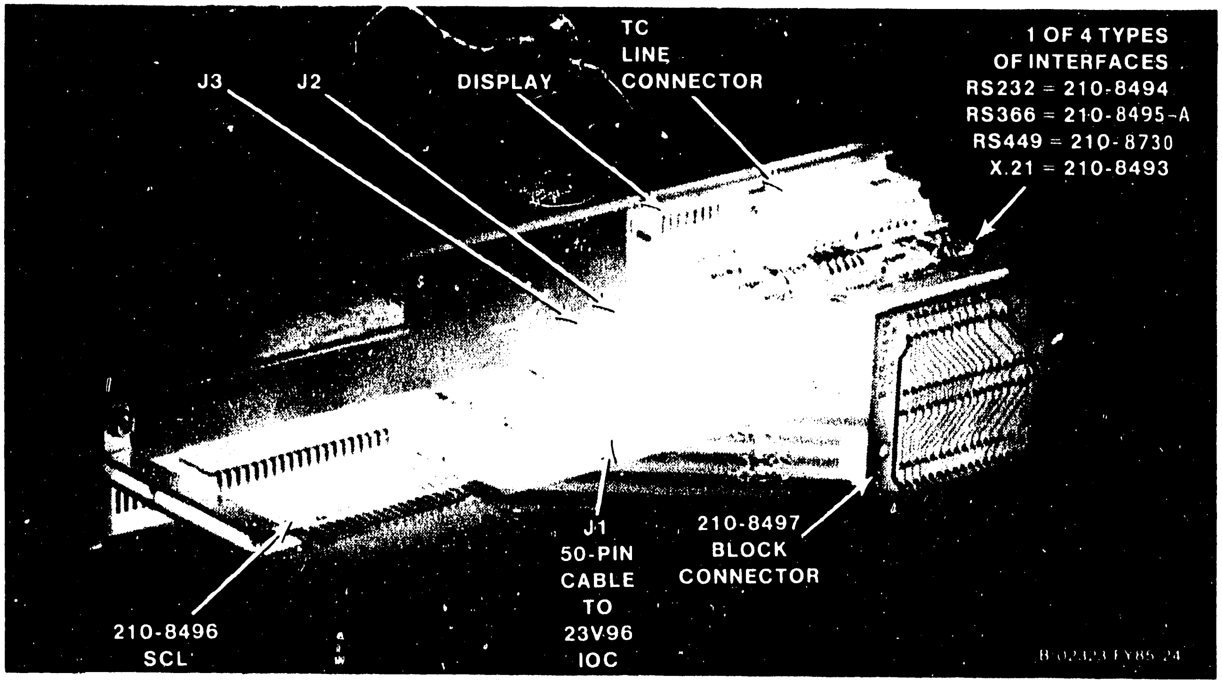

Figure 5-34. 270-1003 Multiline TC Back Panel Assembly

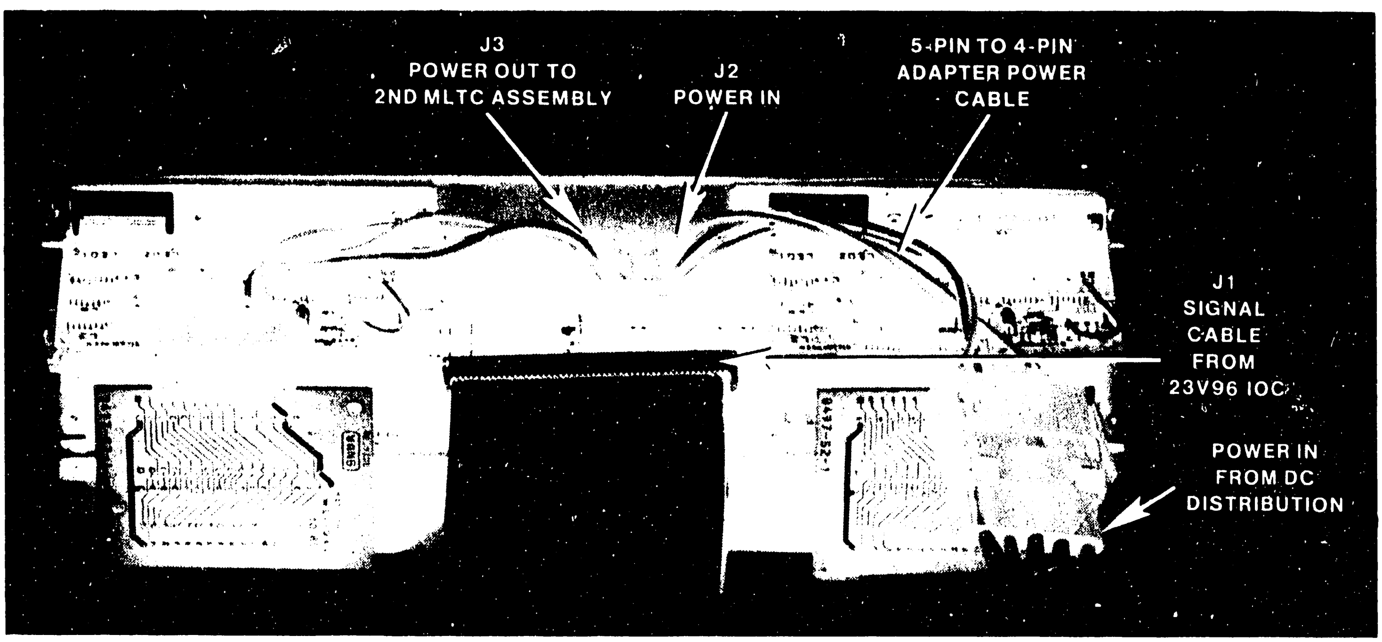

Figure 5-35. 270-1003 Multiline TC Back Panel Assembly with Cabling

NOTE

Revisions are being made to the dc power cabling between the DC PDU and the 270-1003 Multiline TC back panel assembly, as follows:

1. Current DC Power Cabling

a. From the DC PDU (210-8716 - J1/J10) to the 5-pin to 4-pin MLTC adapter cable (220-2372) using the 5-pin dc power cable 220-2343. (Figure 5-35.)
b. The 5-pin to 4-pin MLTC adapter cable connects to the dc power input connector J2 of the 210-8496 Serial Communications Link (SCL) board on the first 270-1003 Multiline TC back panel assembly.
c. The dc power output connector J3 of the SCL board on the first Multiline TC back panel assembly connects to the dc power input connector J2 of the SCL board on the second Multiline TC back panel assembly, using 4-pin daisy cable, 220-2373.
d. Up to four back panel assemblies could be powered this way.

2. Revised DC Power Cabling

a. From the DC PDU (210-8716 - J1/J10) to the 5-pin to 4-pin MLTC "Y" adapter dc power cable (WLI P/N 220-2400) using the 5-pin dc power cable 220-2343.
b. One leg of the 5-pin to 4-pin "Y" adapter cable (220-2400) connects to the dc power input connector J2 of the 210-8496 Serial Communications Link (SCL) board on the first 270-1003 Multiline TC back panel assembly. The second leg of the 5-pin to 4-pin "Y" adapter cable connects to the dc power input connector J2 of the SCL board on the second Multiline TC back panel assembly.
c. A second 5-pin to 4-pin "Y" adapter cable (220-2400) and a second 5-pin dc power cable (220-2343) are needed to power the third and fourth Multiline TC back panel assembly as described above.

3. Test Fixtures

a. For loopback testing, use Loopback Plug WLI P/N 421-0025 only. The pin-out of this connector is as follows:

From Pin	To/From Pin	To/From Pin	To/From Pin
2	3		
4	5	22	
6	8	20	
11	15	17	24
12	13	19	
14	16		

5.3.2.5.9 23V79 (210-8392) CIU BLANC IOC Removal and Replacement

1. Disconnect the cable from the top of the 23V79 CIU BLANC IOC (figure 5-36). Note the position of all cables for later reassembly.
2. Remove the IOC in the manner described in 5.3.2.5.1.
3. After checking the 8-position CIU Functions switch setting at L272 as shown in figures 5-36 and 5-37, install the new 23V79.
4. Reconnect the cable.

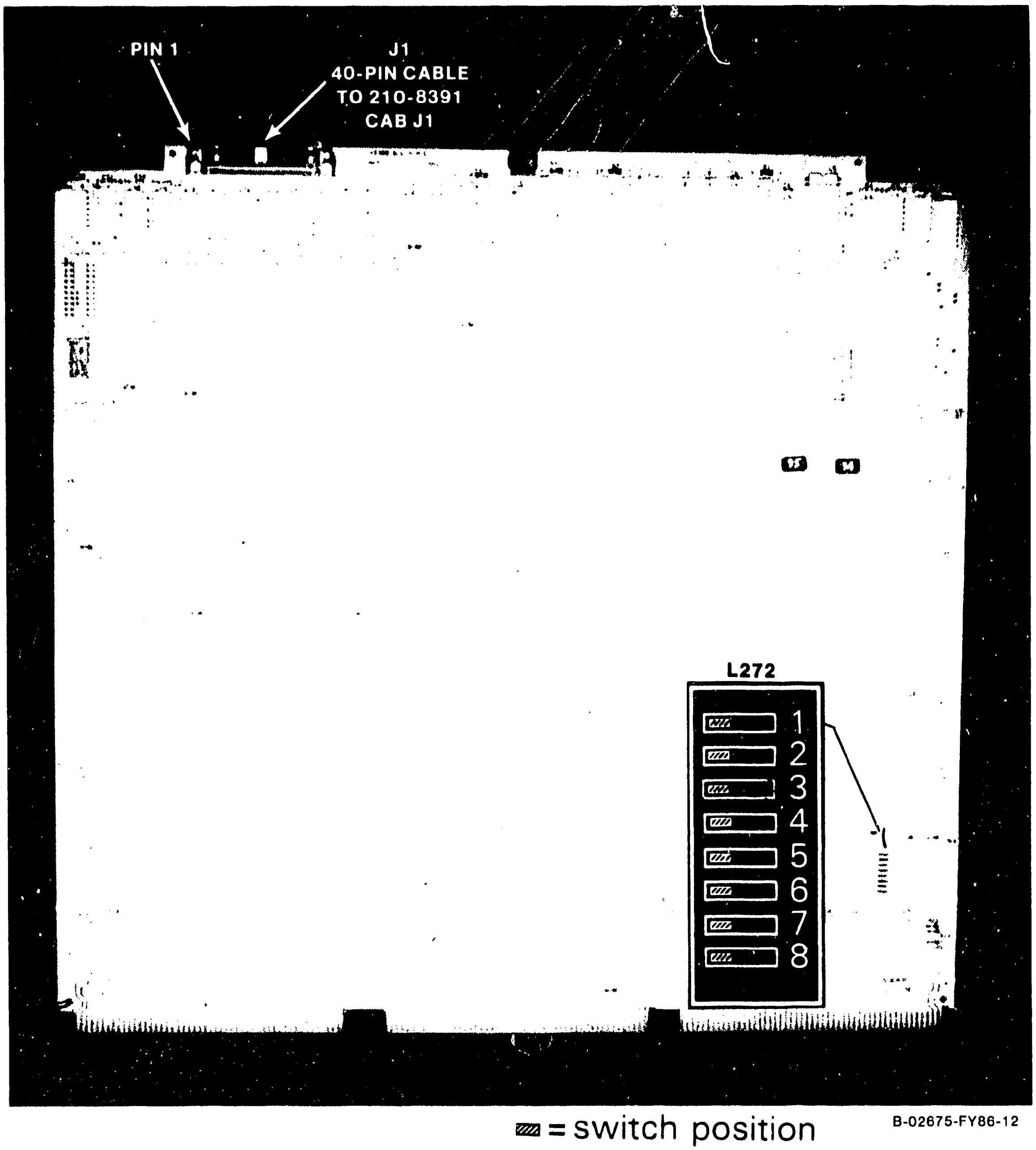

Figure 5-36. 23V79 CIU BLANC IOC

Table 5-10. BLANC ICC Functions Switch (L272)

SW#	Function
SW1	Not used
SW2	Not used
SW3	
Open	CAB/modem present
Closed	CAB/modem not present
SW4	Not used
SW5	
Open	Don't loop on BIT test
Closed	Loop on BIT test
SW6	
Open	CIU installed in VS
Closed	CIU installed in testbed
SW7	Not used
SW8	
Open	All other switches not valid
Closed	All other switches valid

CAUTION

Do not run the External Loopback test with live WangNet cables connected to the modem. The test will cause the WangNet contention fields to drop out of synchronization. To run the test, connect either a 40db. loopback test pad or a Cable Simulator to the transmit and receive connectors of the modem. (Refer to Chapter 7, Troubleshooting.)

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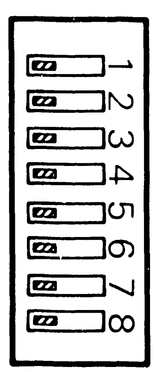


= switch position

Figure 5-37. BLANC IOC Functions Switch (L272) Normal Settings

5.3.2.5.10 210-8391 CIU CAB Board Removal and Replacement

1. The 210-8391 CIU CAB board is part of the 279-0687 CAB/Modem assembly. Do not order or replace the entire assembly.
2. Remove the top cover as described in paragraph 5.3.2.1 and the left side panel as described in paragraph 5.3.2.3.
3. The CIU CAB board (figure 5-38) is mounted on top of the 10 megabit per second (MBPS) duobinary modem. The modem and the CAB board are located behind the CIU connector panel at the rear of the mainframe. Refer to figure 3-12. Disconnect all cables from the CAB board. It may be necessary to remove the CIU connector panel from the back panel to allow access to the rear power cable on the CAB board.
4. Remove the six Phillips head screws securing the CAB board to the modem and remove the CAB board.
5. After checking the 3-position jumper shown in figure 5-38, install the new CAB board.
6. Reconnect all cables.

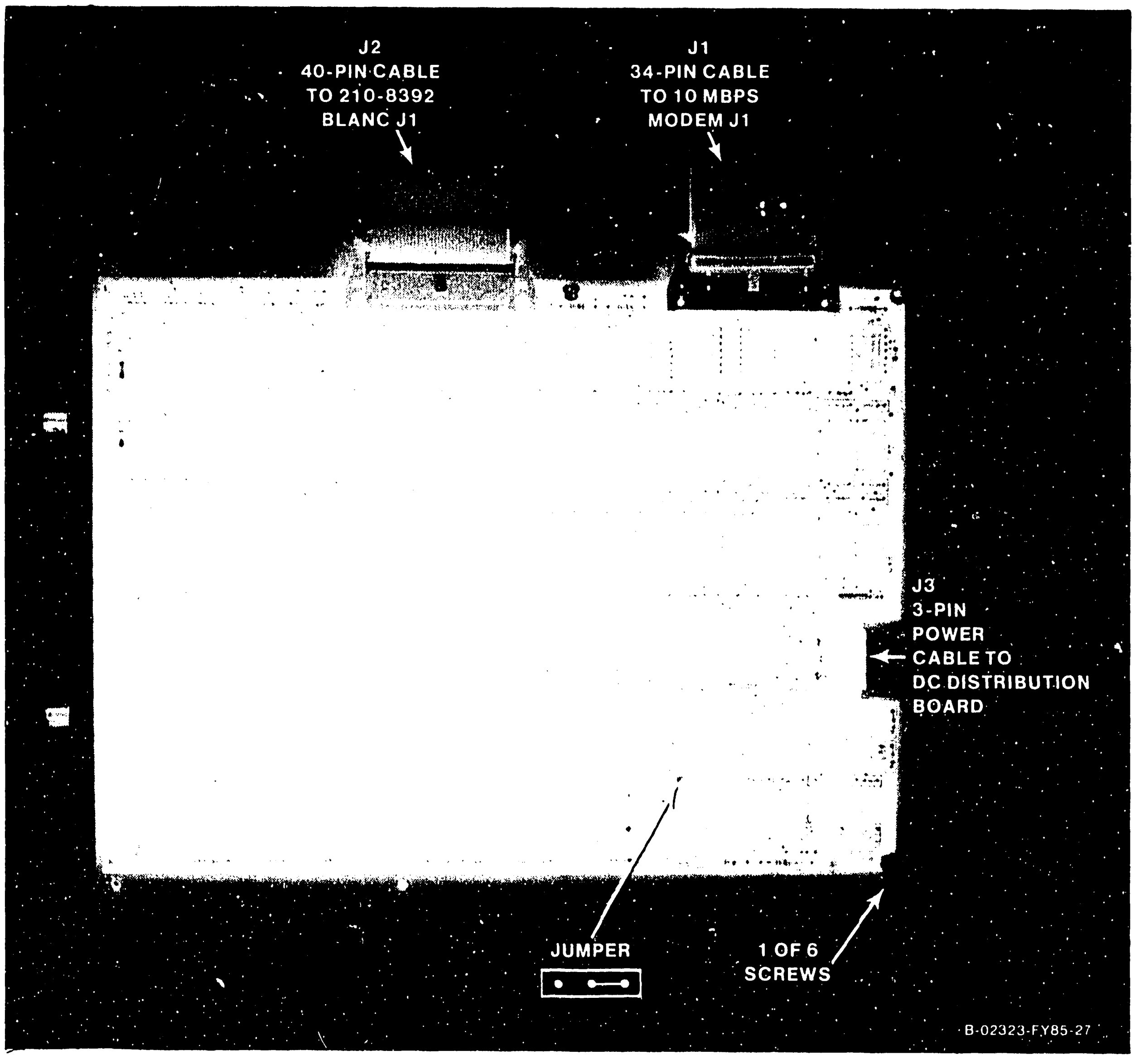


Figure 5-38. 23V79 CIU CAB Board

5.3.2.5.11 210-8142 5-Channel 10MBPS Modem Removal and Replacement

1. The 210-8142 5-channel 10MBPS Duobinary Modem is part of the 279-0687 CAB/Modem assembly. Do not order or replace the entire assembly.
2. Remove the top cover as described in paragraph 5.3.2.1 and the left side panel as described in paragraph 5.3.2.3.
3. The 10 megabit per second (MBPS) duobinary modem (figure 5-39) has the 210-8391 CIU CAB board (figure 5-38) mounted on top. The modem and the CAB board are located behind the CIU connector panel at the rear of the mainframe. Refer to figure 3-12. Disconnect all cables from the modem. It may be necessary to remove the CIU connector panel from the back panel to allow access to the CAB and modem.
4. Remove the CAB board as described in paragraph 5.3.2.5.10.
5. Remove the modem (with the front panel).
6. After checking the four 3-position jumpers shown in figure 5-39, install the new modem. (Refer to Appendix A for 10MBPS modem channel allocations and device types that should not be used on the same channels or frequencies.)
7. Remount the CAB board.
8. Reconnect all cables.

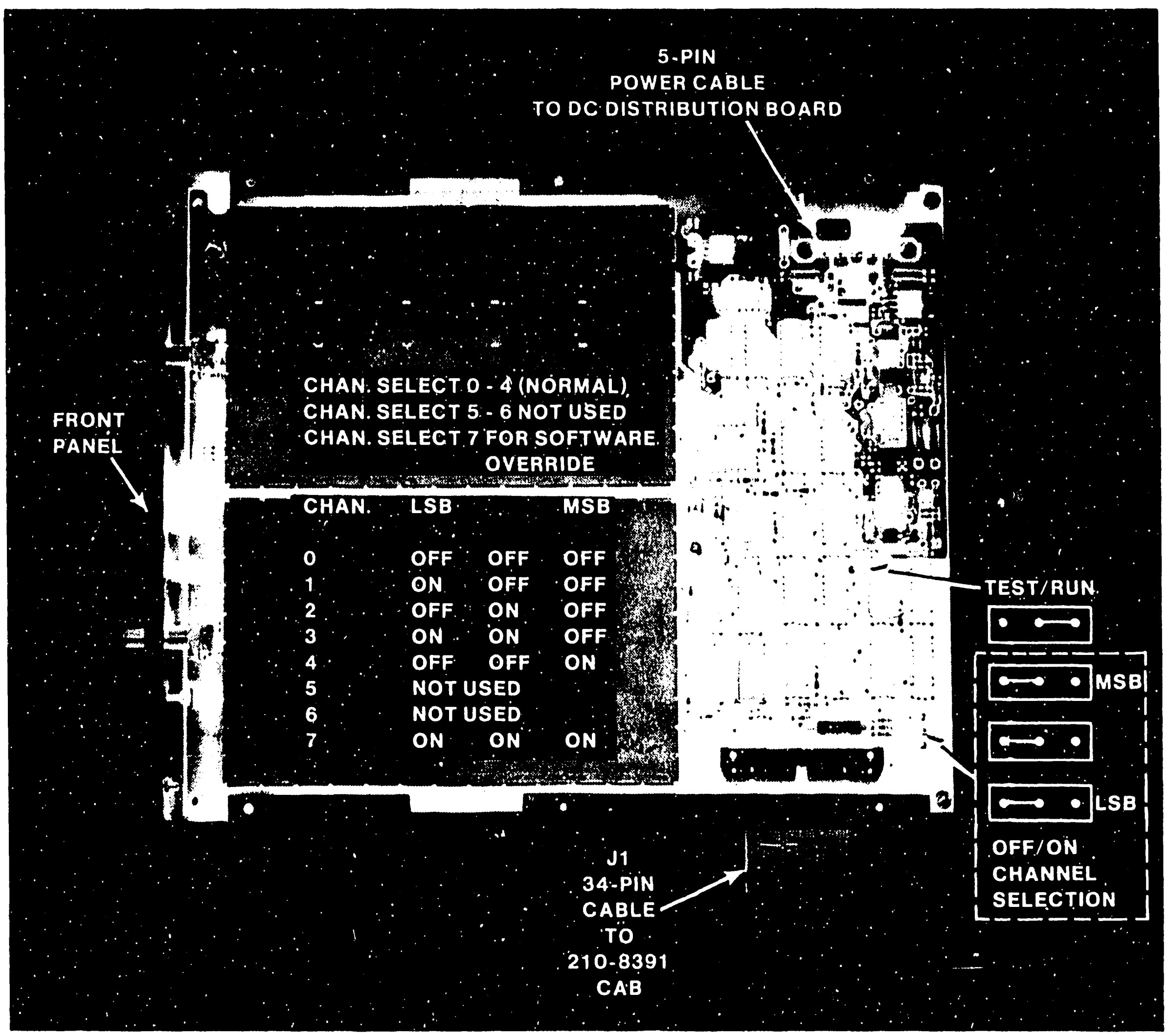


Figure 5-39. 5-Channel 10 Megabit Duobinary Modem

5.3.2.5.12 270-0787 Single Channel 10MBPS RF Modem Removal and Replacement

1. The 270-0787 single channel 10 MBPS RF Modem is also supported on the VS-300. It is part of the 279-0687 CAB/Modem assembly. Replace either the modem or the CAB board.
2. Remove six screws securing the modem to the modem mounting plate.
3. Remove the CAB board from the modem by removing six Phillips head screws and stand-offs.
4. Remove the 11" shielded ribbon cable (WLI P/N 220-3529) that is routed between the CAB board and and the modem.
5. There are no jumpers on the single channel modem.

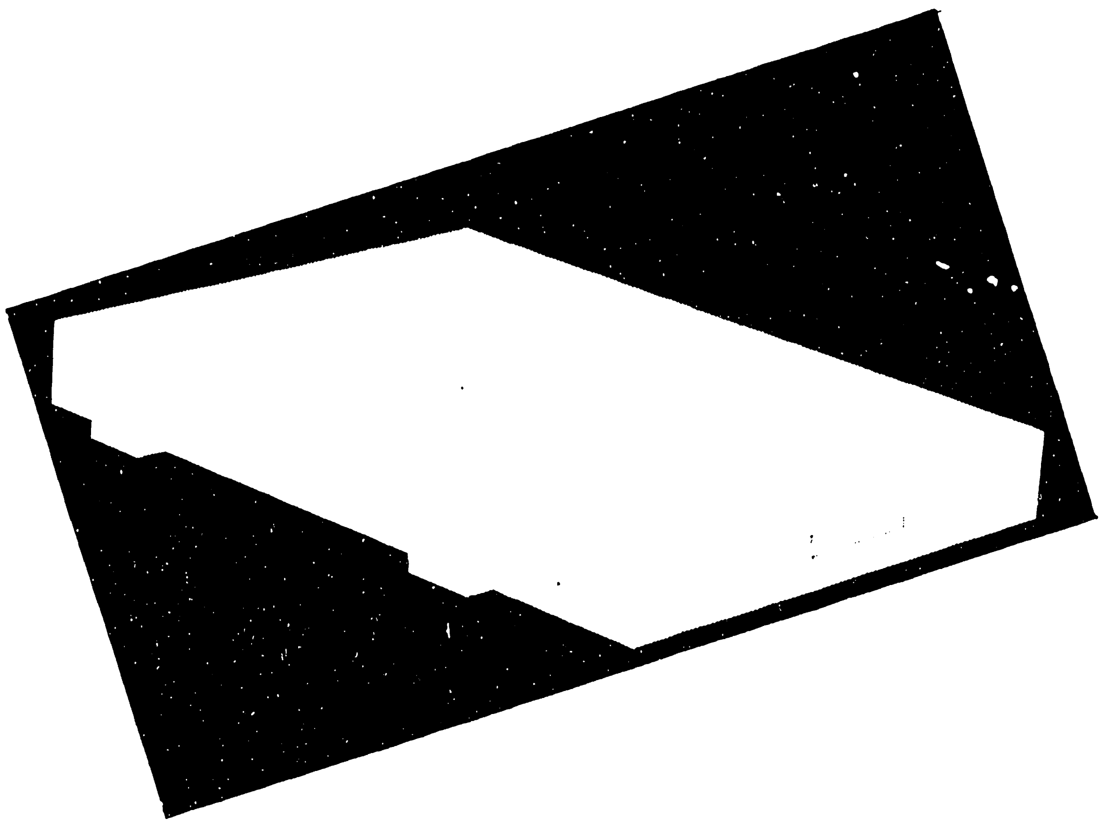


Figure 5-39a. Single Channel 10 Megabit Duobinary Modem

5.3.2.5.13 WangNet P-Band Modem Removal and Replacement

1. Remove the top cover as described in paragraph 5.3.2.1 and the left side panel as described in paragraph 5.3.2.3.
2. Disconnect the cables from the transmit (gold) and the receive (silver) connectors on the front of the P-Band modem panel assembly. (Figure 5-39b.)
3. Disconnect the power cable from J2 on the P-Band modem panel assembly. (Figure 5-39c.)
4. Disconnect the 32-pin ribbon cable from P1 on the P-Band modem panel assembly.
5. Remove the modem panel assembly.
6. Remove the two Phillips head screws that secure the P-Band modem to the rear panel of the VS-300. (Figure 5-39b.)
7. Do not replace the entire assembly; only the modem. Remove the six screws that secure the modem to the mounting plate and remove the plate. Remove the four screws that secure the modem to the mounting panel and remove the panel. (Figure 5-39c.)
8. Remount the modem.
9. Reinstall all cables.

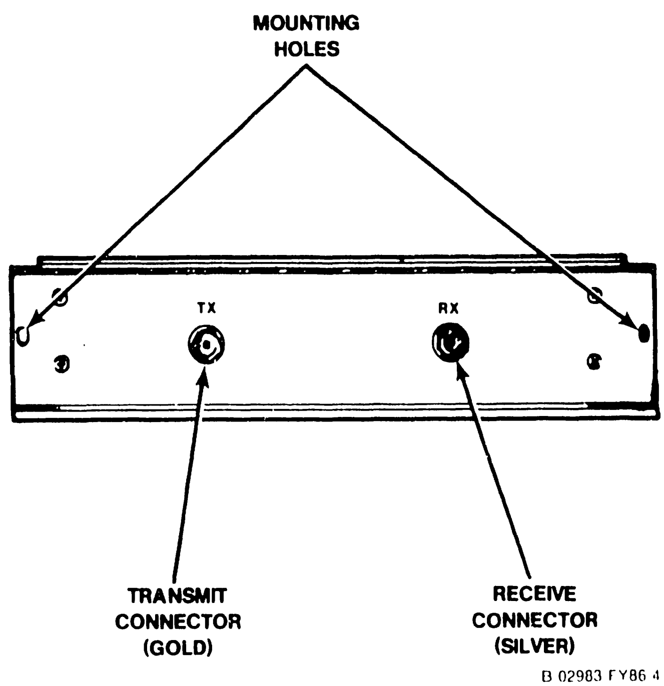


Figure 5-39b. Wangnet P-Band Modem Panel Assembly

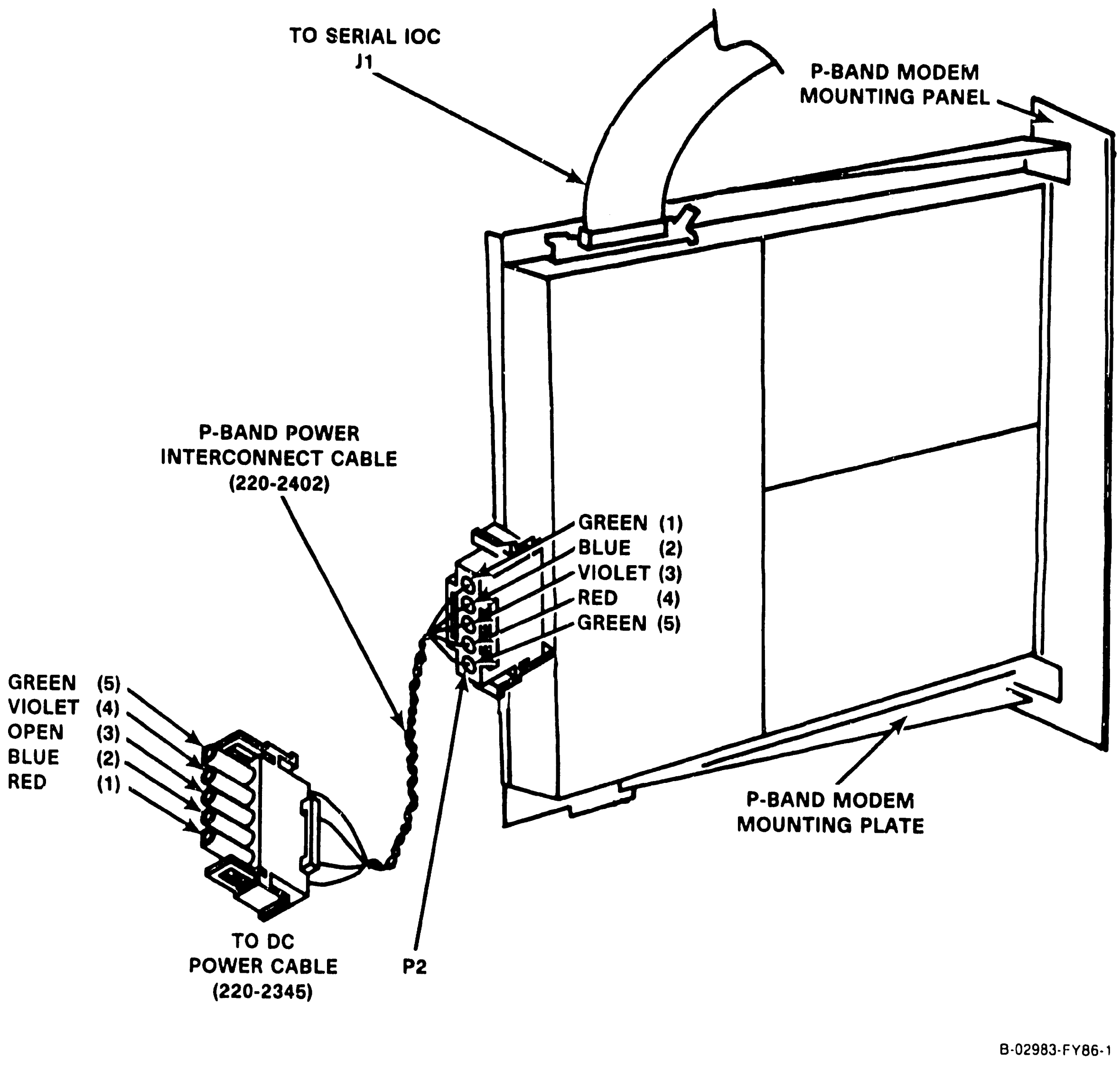


Figure 5-39c. Wangnet P-Band Modem Removal

5.3.2.6 Power Supply Controller Board Removal

Remove the 210-8709 Power Controller board as follows:

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Remove the left front cover.
5. Disconnect the 9-pin cable connector from J1 of the Power Controller board.
6. Disconnect the 3-pin cable connector from J2.
7. Disconnect the 4-pin cable connectors from J4 and J5.
8. Disconnect the 60-pin cable connector from J6.
9. Disconnect the 20-pin cable connector from J7.
10. Disconnect the 12-pin cable connector from J8.
11. Disconnect the 5-pin cable connector from J9.
12. Disconnect the 2-pin cable connector from J10.
13. Remove the six Phillips head screws from the Power Controller board plastic cover standoffs and remove the plastic cover.
14. Remove the six standoffs.
15. Remove the three Phillips head screws from the Power Controller board.
16. Remove the board.

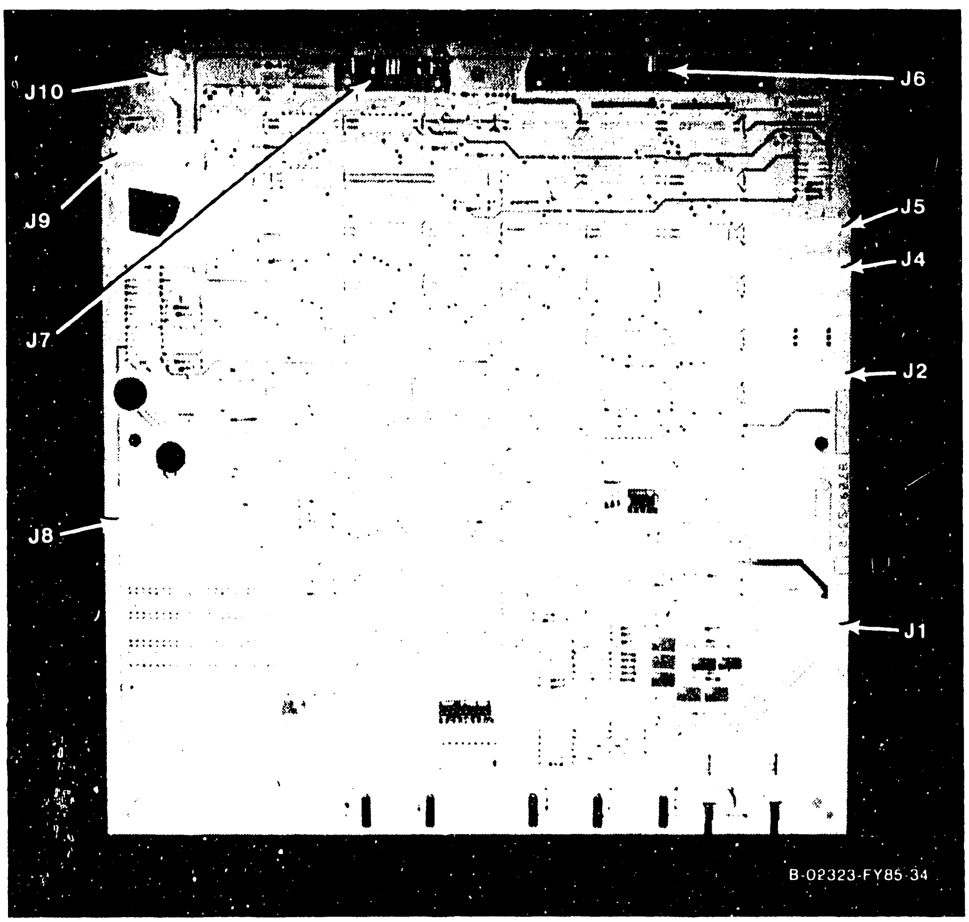
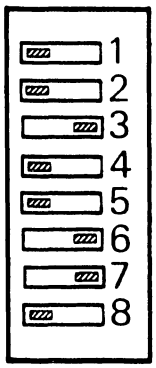
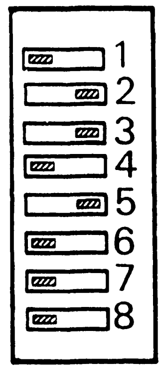


Figure 5-40. Power Supply Controller Board. (Rev. 0 Version)

5.3.2.7 Power Supply Controller Board Replacement

1. To reinstall the Power Controller board, reverse the removal procedure.
2. Set the Battery Backup Time switch (SW4) for 100 seconds for the Rev. 0 board, or 96 seconds (currently) for the Rev. 1. board. (Figure 5-41.)

Switch 4 Settings (Rev. 0 Board)		Switch 4 Settings (Rev. 1 Board)	
= SWITCH POSITION 	Designations 1 2 4 Battery 8 Backup 16 Time 32 (Seconds) 64 128	= SWITCH POSITION 	Designations 16 Battery 32 Backup 64 Time 128 (Seconds) 32 Minor 64 Voltage 128 Time 256 (Seconds)

B-02675-FY86-3

Figure 5-41. Battery Backup Time Switch SW4 Settings.

3. Make sure that all cable connectors are reconnected correctly.
4. Power up the system and check and adjust the Power Supply, paragraph 5.2.4.1, and the Power Supply Controller, paragraph 5.2.4.2. Also check the Low Battery Voltage Dropout adjustment, paragraph 5.2.4.4.

5.3.2.8 Battery Backup Board Removal

The Battery Backup board (figures 5-42 and 5-43) is mounted on the rear of the battery pack assembly. Remove the Battery Backup board:

WARNING

Battery voltage is on the battery input connectors (J3 through J7) to the board at all times.

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Remove the top cover and left side panel.
5. Remove the four Phillips head screws that secure the sheet metal safety cover over the Battery Backup board and remove the cover.

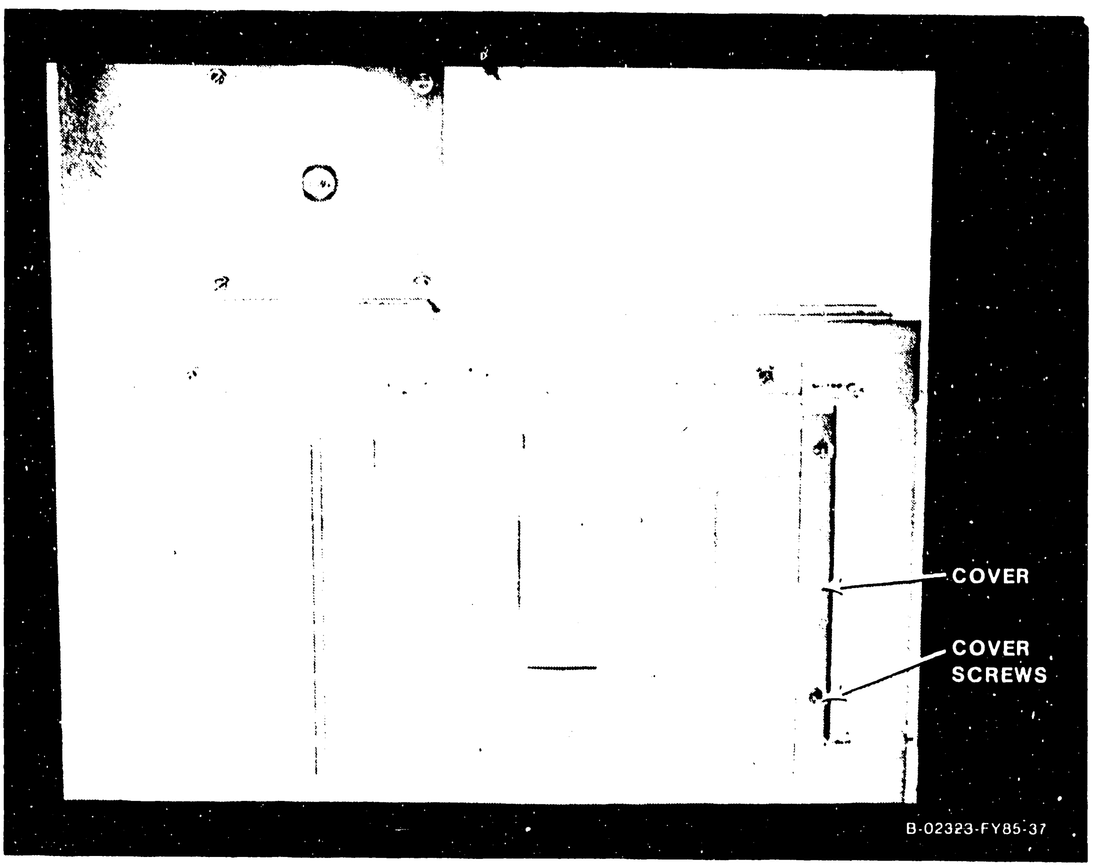


Figure 5-42. 210-8717 Battery Backup Board Removal

6. Disconnect the 6-pin power cable connectors from J1 and J2.
7. Disconnect the 2-pin battery input cable(s) connectors J3 through J7 of the board.
8. Disconnect the yellow 3-pin battery power cable connector from J8.

CAUTION

> If it is necessary to reconnect the yellow 3-wire battery power cable to J8, wait several seconds for the power supply capacitors to discharge or the Battery Backup board will be damaged. The red LED on the Battery Backup board must be out.

9. Remove the six Phillips head screws from the board standoffs and remove the board.

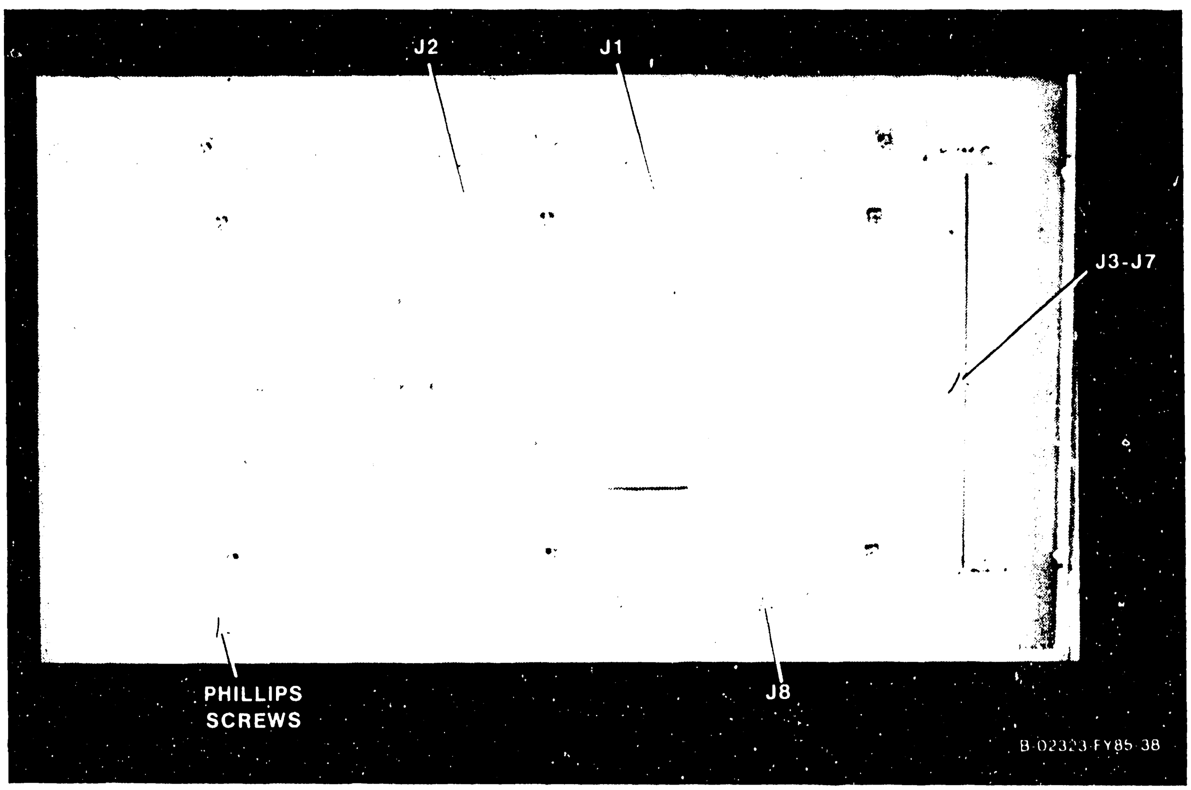


Figure 5-43. 210-8717 Battery Backup Board Removal

5.3.2.9 Battery Backup Board Replacement

1. To reinstall the Battery Backup board, reverse the removal procedure.

5.3.2.10 Battery Backup Pack Removal

The five optional battery backup packs are located behind the left front panel. This procedure describes removing a single battery pack, WLI P/N 666-1011. All packs are removed in the same manner.

NOTE

When one pack becomes defective, all five packs must be replaced at the same time.

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker on the Power Distribution Unit.
4. Remove the top cover, the left front cover, and the left side cover.
5. Disconnect the 2-pin battery cable(s) connector(s) from J3 through J7 of the Battery Backup board.
6. At the front of the battery pack, remove the two Phillips head screws securing the battery pack baseplate to the battery pack housing.
7. Carefully remove the battery pack while guiding the 2-wire battery cable(s) out. (Make sure the pack stays in the baseplate guides.)
8. Once the battery pack is out, remove the battery cable from the battery pack (red is plus [+] and black is minus [-].), and remove the four screws (two on each side) securing the battery pack hold down clamp to the battery pack mounting shelf baseplate.
9. Remove the battery pack.

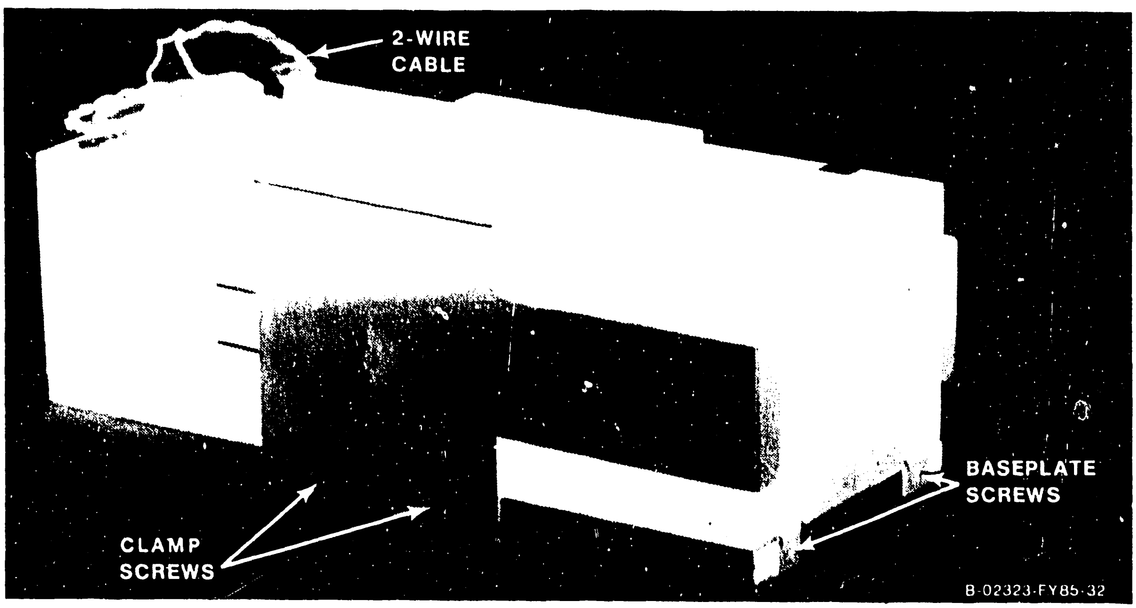


Figure 5-44. Battery Pack Removal

5.3.2.11 Battery Backup Pack Replacement

1. To reinstall the battery pack(s), reverse the removal procedure.
2. Make sure that all cable(s) are reconnected.

5.3.2.12 Battery Backup Charging Power Supply Removal

Remove the battery backup charging power supply as follows:

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Remove the left front cover.
5. Disconnect the 3-pin ac power input cable connector (J3) and the 6-pin cable connector (J4) from from the power supply.
6. Remove the two Phillips head screws securing the power supply to the battery mounting shelf base and remove the power supply.

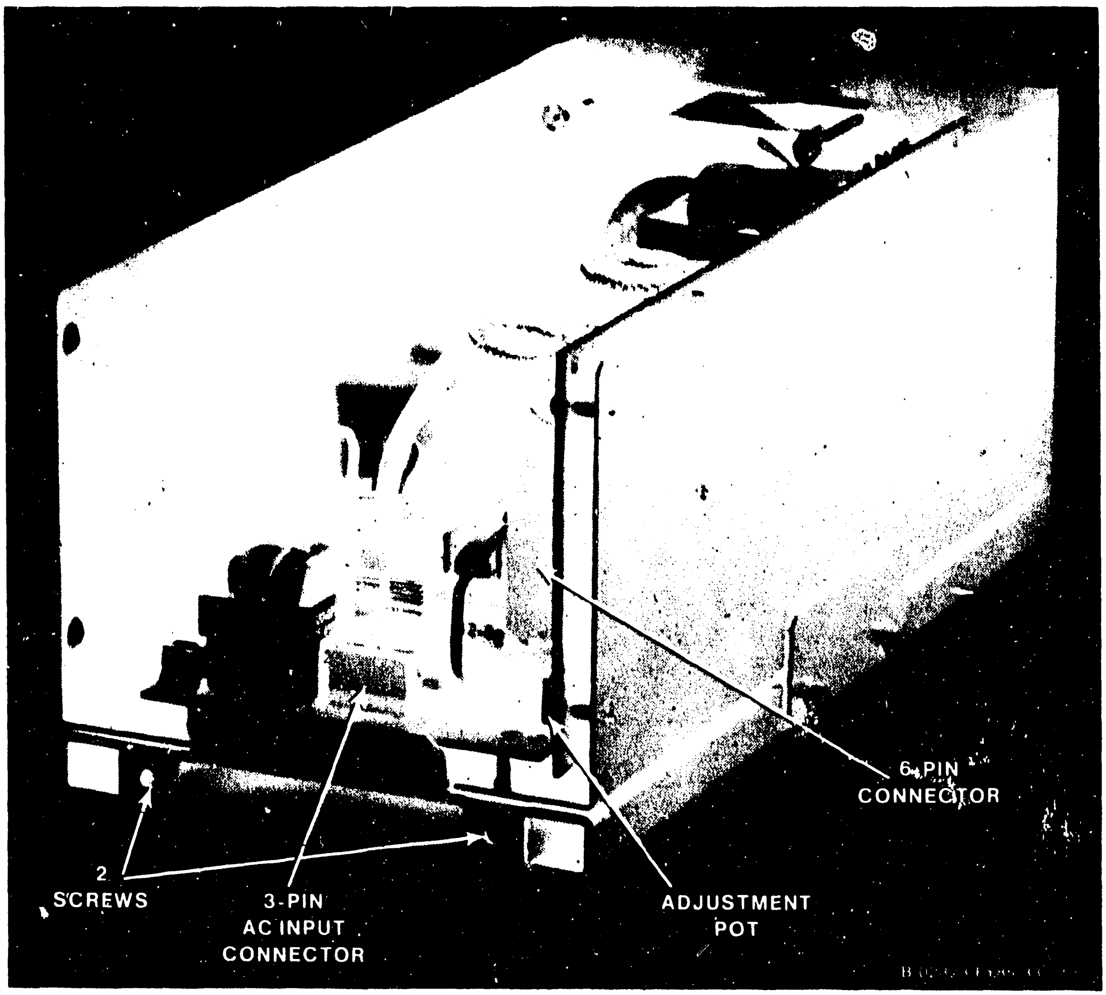


Figure 5-45. Battery Backup Charging Power Supply Removal

5.3.2.13 Battery Backup Charging Power Supply Replacement

1. To reinstall the power supply, reverse the removal procedure.
2. Make sure that all cables are reconnected.
3. Power up the system and adjust the power supply as described in paragraph 5.2.4.5.

5.3.2.14 Power Distribution Unit and AC On/Off Circuit Breaker Removal

The Power Distribution Unit (PDU) is mounted on the right rear of the mainframe, below the SCU. (See figures 5-46 and 5-47.)

The ac On/Off circuit breaker is mounted inside the PDU (figure 5-48) and can be replaced without replacing the entire PDU.

WARNING

Because of the high operating voltages passing through the PDU, power down the mainframe and disconnect the mainframe power connector from the power source receptacle before performing the following removal/replacement procedures.

Remove the PDU as follows:

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Disconnect the ac power input connector from the power source receptacle.
5. Remove the top cover, rear fan panel, and right side panel.

NOTE

Note the orientation of the dc power supply wiring of TB1 before proceeding with step 6.

6. Remove the dc power supply wiring from TB1 on the DC Distribution board on top of the PDU.
7. Disconnect all dc distribution cable(s) connectors from the DC Distribution board on top of the PDU.
8. Disconnect all ac distribution cable(s) connectors from the AC Distribution board at the rear of the PDU. Note the 5-wire cable connected to J1 (the standalone connector) of the AC Distribution board. This cable must be reconnected to J1 only.
9. Remove the 14 hex head screws securing the PDU to the mainframe and remove the PDU and ac input power cable.

Remove the circuit breaker as follows: (See figure 5-48.)

1. Remove the hex head screws securing the PDU cover and remove the cover.
2. Disconnect the power input cable wiring to the circuit breaker. Make sure to note the orientation and color coding of the power wiring to the circuit breaker for reinstallation of the new circuit breaker.
3. Remove the four Phillips head screws securing the circuit breaker to the front of the PDU and remove the circuit breaker.

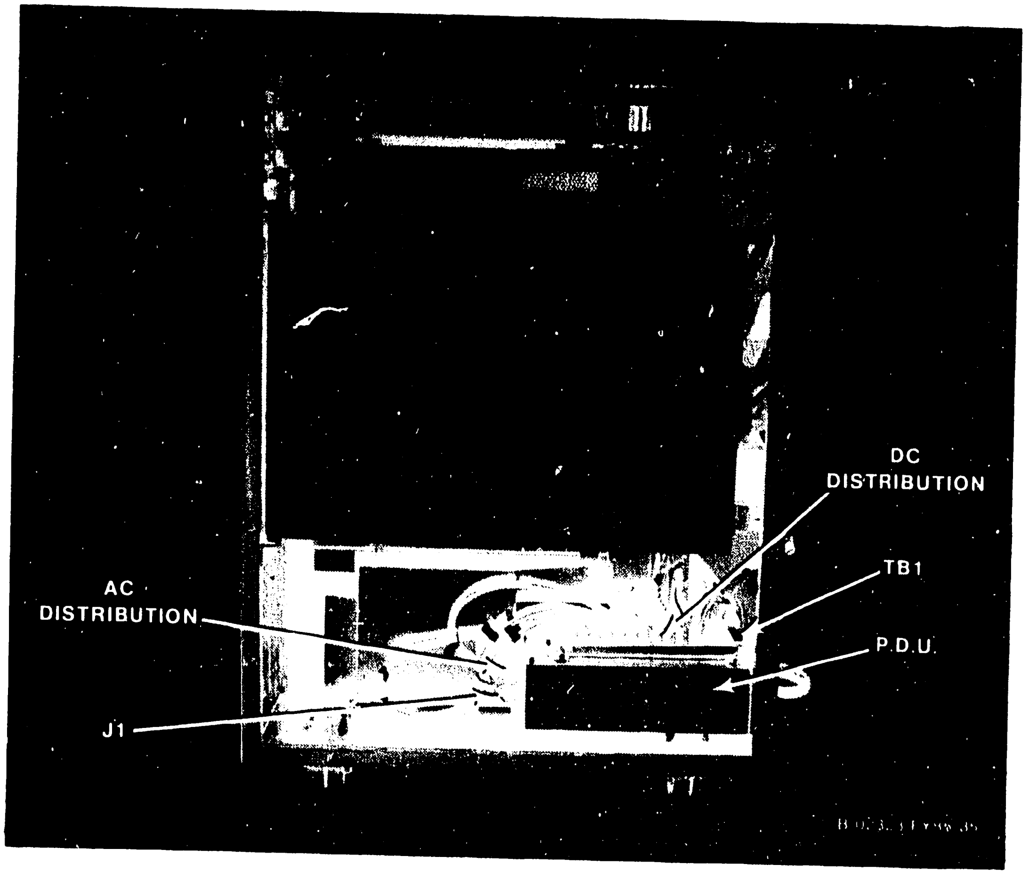


Figure 5-46. PDU Removal

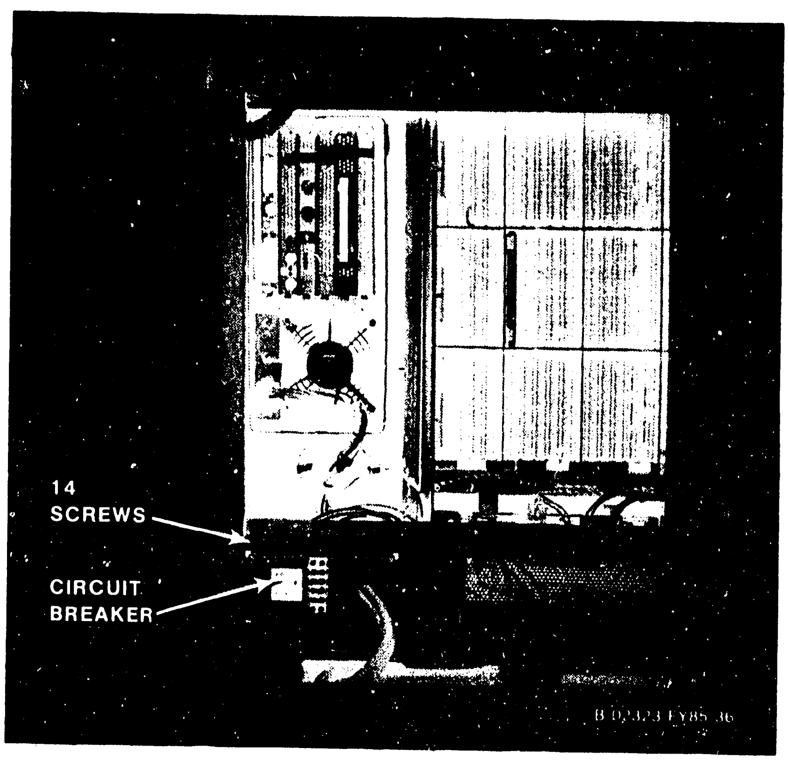


Figure 5-47. PDU Removal

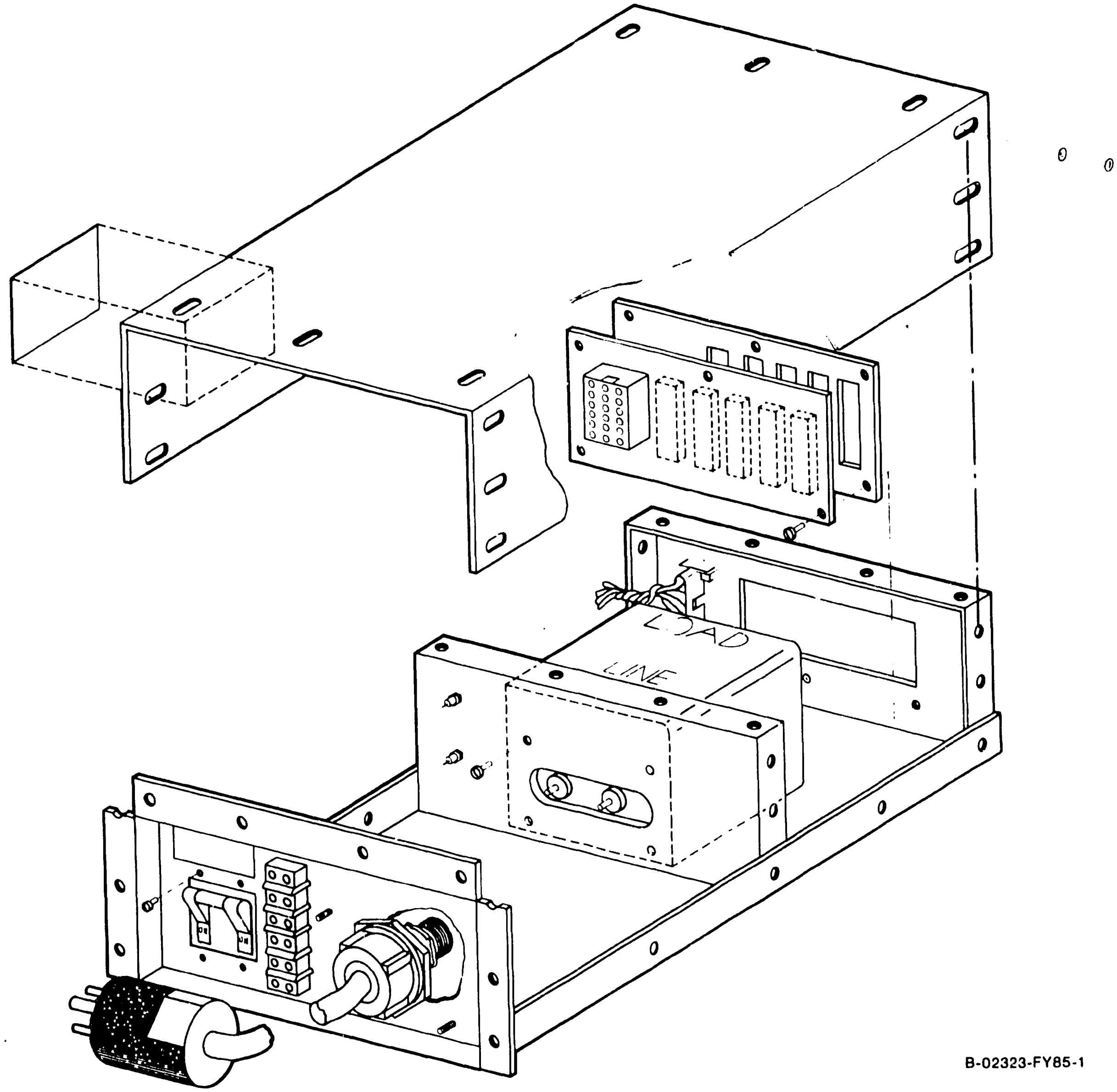


Figure 5-48. AC On/Off Circuit Breaker Removal

5.3.2.15 AC On/Off Circuit Breaker Replacement

1. To reinstall the circuit breaker, reverse the removal procedure.
2. Make sure the power input cable wiring to the circuit breaker is rewired correctly.
3. Make sure the circuit breaker is ON when pushed up and OFF when pushed down.

5.3.2.16 Power Distribution Unit Replacement

1. To reinstall the PDU, reverse the removal procedure.
2. Make sure that the 5-wire cable is reconnected to J1 of the AC Distribution board.

5.3.2.16.1 Second DC Power Distribution Board Removal

The second (new) DC Power Distribution board is mounted on the left rear side of the card cage assembly, to the upper right of the Power Supply Controller board. (See figure 5-48a.)

Remove the DC Distribution board as follows:

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Remove the top cover and left side panel.
5. Disconnect the yellow 3-pin battery power cable connector from J8 of the Battery Backup board.

CAUTION

If it is necessary to reconnect the yellow 3-wire battery power cable to J8, wait several seconds for the power supply capacitors to discharge or the Battery Backup board will be damaged. The red LED on the Battery Backup board must be out.

6. Disconnect all cable connectors from the DC Distribution board.
7. Disconnect all wires from the 7-connector terminal strip at the bottom of the board.
8. Remove the four locknuts securing the board cover and remove the cover.
9. Remove the six Phillips screws from the board standoffs, (figure 5-48b) and remove the board.

5.3.2.16.2 Second DC Power Distribution Board Replacement

1. To reinstall the DC Distribution board, reverse the removal procedure.
2. Make sure that all cables and wires are correctly reconnected to the DC Distribution board, and the yellow 3-pin battery power cable is reconnected to J8 of the Battery Backup board.

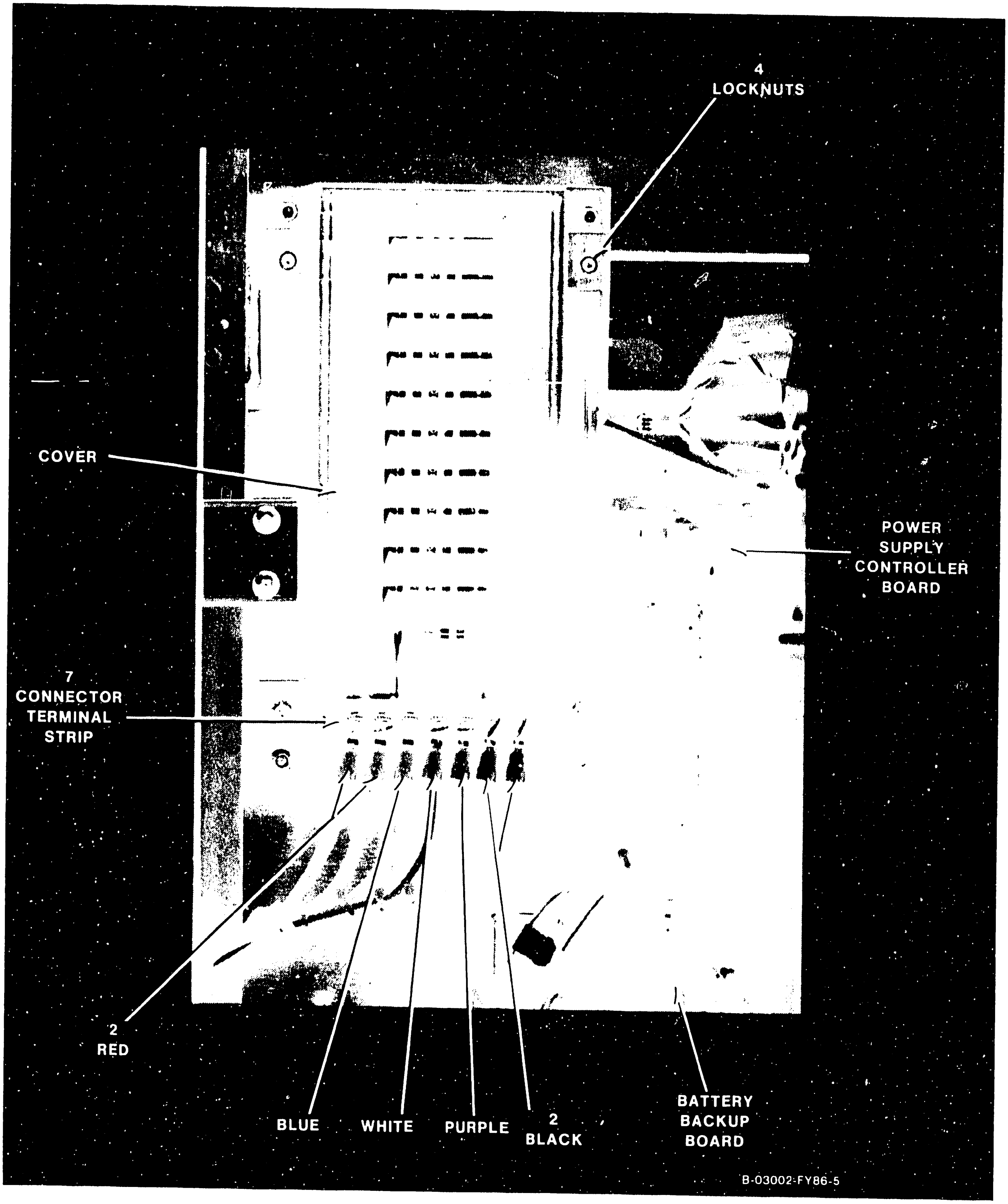


Figure 5-48a. Second DC Distribution Board Removal

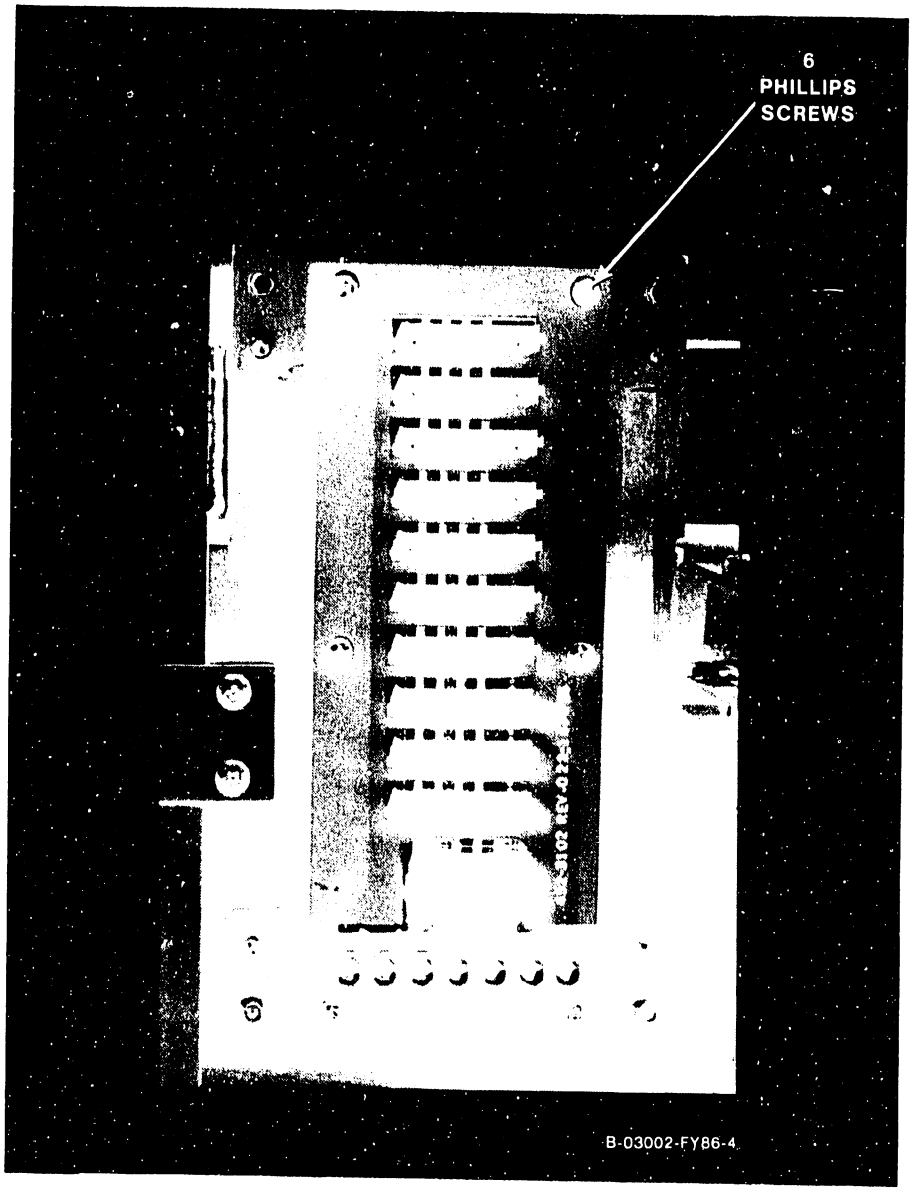


Figure 5-48b. Second DC Distribution Board Removal

5.3.2.17 SCU Professional Computer (PC) Removal

The SCU (PC) is mounted internally at the right side of the mainframe, behind the Control Panel. Remove the SCU as follows: (See figures 5-49.)

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Remove the screws from the rear fan panel, disconnect the two fans and set aside the panel.
5. Disconnect the 4-pin keyboard cable connector from J3 of the SCU CPU board.
6. Disconnect the 25-pin remote diagnostic cable connector from J4 (RS232 connector) of the SCU CPU board.
7. Disconnect the 8-pin monitor video cable connector from J1 of the SCU Monochrome Monitor board.
8. Disconnect the 5-pin monitor power cable connector from J2 of the SCU Monochrome Monitor board.
9. Disconnect the coax cable from the BNC/TNC connectors of the Local Comm. Data Link board.
10. Disconnect the 60-pin signal cable connector from the SCU Professional Computer Interface (PCI) option board.
11. Disconnect the 15-pin power cable connector mounted on a bracket to the left of the SCU fan.
12. Remove the four black anodized Phillips head screws (two top and two bottom) securing the SCU to the case.
13. Carefully slide the SCU toward the rear of the mainframe and out of the case.
14. Refer to the Professional Computer Product Maintenance Manual for disassembly/reassembly procedures and replacement parts.

5.3.2.18 SCU Professional Computer (PC) Replacement

1. To reinstall the SCU, reverse the removal procedure.
2. Reach through the Control Panel cutout (at the front of the mainframe) for the SCU's floppy drive and try to guide the front of the SCU into it's final position. Be careful of the RF gaskets surrounding all four sides of the floppy drive cutout.
3. Make sure that all cable connectors are reconnected correctly.
4. Make sure that the Local/Remote switch on the Local Comm. Data Link board is in the Local position.

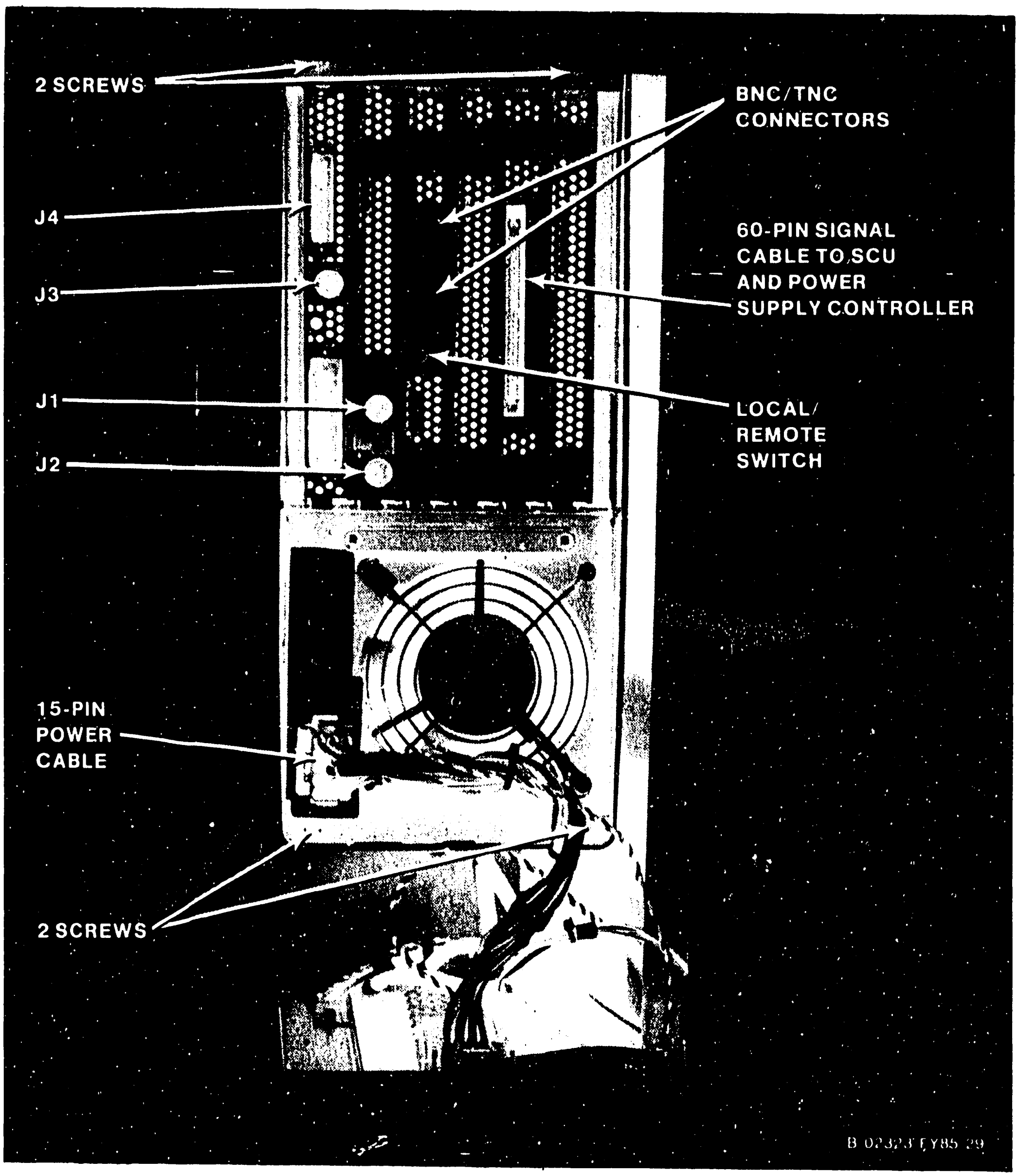


Figure 5-49. SCU Professional Computer Removal and Replacement

5.3.2.19 Control Panel Pushbutton Bulb Removal and Replacement

Each of the Control Panel pushbuttons contains an incandescent bulb. Remove and replace the bulbs as follows: (Figure 5-50)

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. With a small screwdriver, pry (top and bottom) the lens cap out of the pushbutton.
5. Pull the small silver lever on the bottom of the pushbutton forward until the bulb pops out.
6. Replace the bulb by pushing it into the pushbutton.
7. Replace the lens cap.

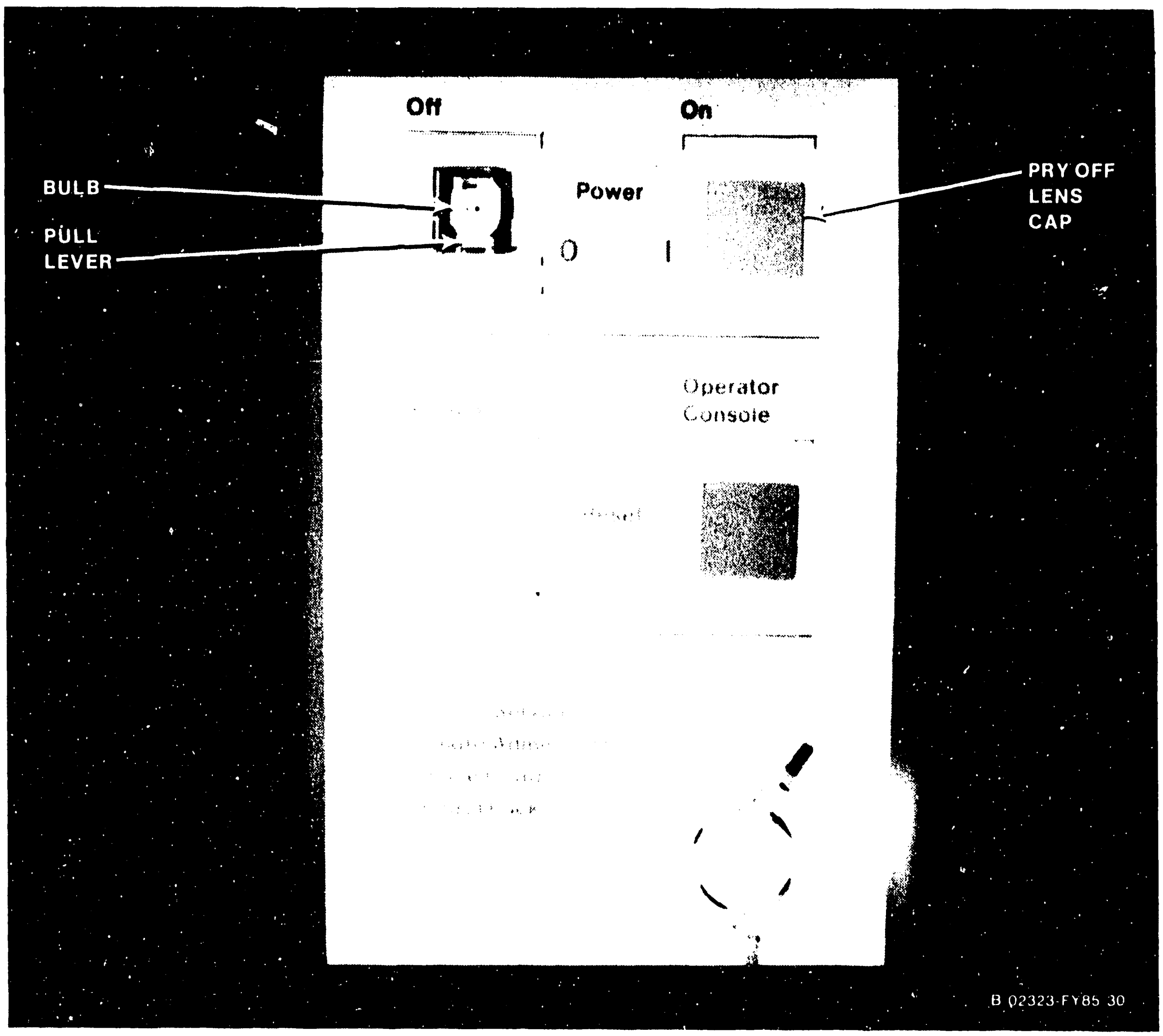


Figure 5-50. Control Panel Pushbutton Bulb Removal and Replacement

5.3.2.20 Control Panel Assembly Removal

The Control Panel assembly is mounted inside the right front panel. Remove the 272-0044 Control Panel assembly as follows: (Figure 5-51)

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Control Panel Power Off pushbutton (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker located on the Power Distribution Unit at the right rear of the mainframe.
4. Remove the top cover.
5. Disconnect the 20-pin signal cable from the Control Panel assembly.
6. Remove the four hex nuts securing the Control Panel assembly to the right front panel and remove the assembly.

5.3.2.21 Control Panel Board Assembly Replacement

1. To reinstall the Control Panel assembly, reverse the removal procedure.
2. Make sure that the 20-pin signal cable is reconnected correctly.

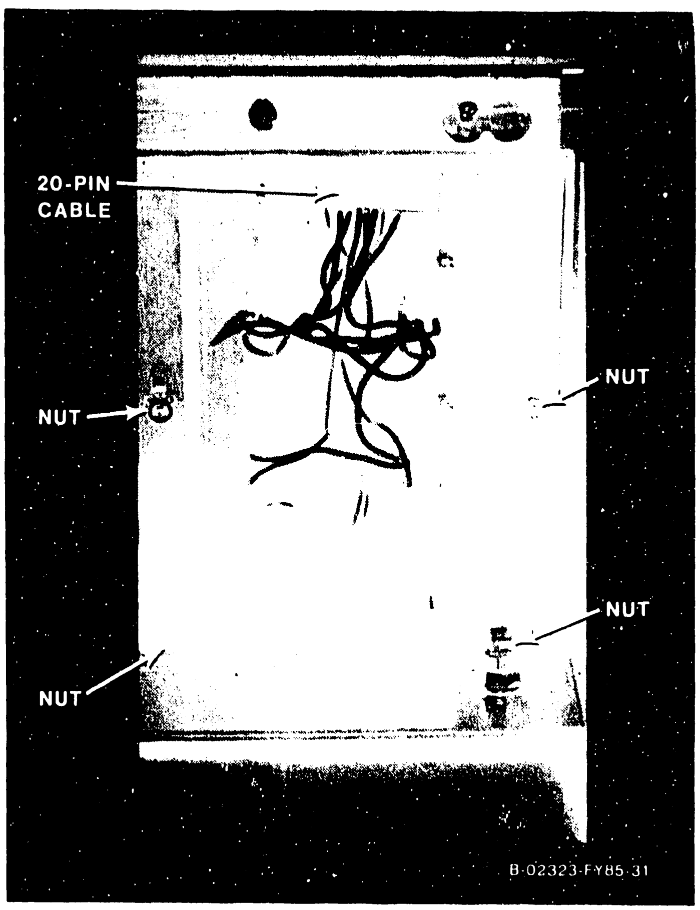


Figure 5-51. 210-8711 Control Panel Board Removal

5.3.2.22 Multioutput Switching Power Supply Removal

Remove the multioutput switching power supply as follows:

WARNING

```
***************************************************************
*                                                             *
*    DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY         *
*    CIRCUMSTANCE. EXTREMELY DANGEROUS VOLTAGE AND            *
*    CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-        *
*    LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.    *
*                                                             *
*    DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER             *
*    SUPPLY; IT IS FIELD REPLACEABLE ONLY.                    *
*                                                             *
*    AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC    *
*    POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,        *
*    ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO     *
*    PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO        *
*    DRAIN THROUGH THE BLEEDER RESISTORS.                     *
*                                                             *
***************************************************************
```

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Front Panel Power Off push-button (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker.
4. Remove the top cover and left side panel.
5. Open the front hinged door.
6. Remove the screws from the rear fan panel, disconnect the two fans and set aside the panel.

CAUTION

If it is necessary to reconnect the yellow 3-wire battery power cable to J8 (below), wait several seconds after the LED on the Battery Backup board goes out or the Battery Backup board will be damaged.

7. Disconnect the yellow 3-pin battery power cable connector from J8 of the 210-8717 Battery Backup Board.
8. All wiring is color coded as listed in table 5-11. Using figures 5-52 (for systems with only the original single DC Distribution board) or 5-52a (for systems with both the original and the new second DC Distribution board), and table 5-11, disconnect the bus bars and wiring from the power supply terminals.

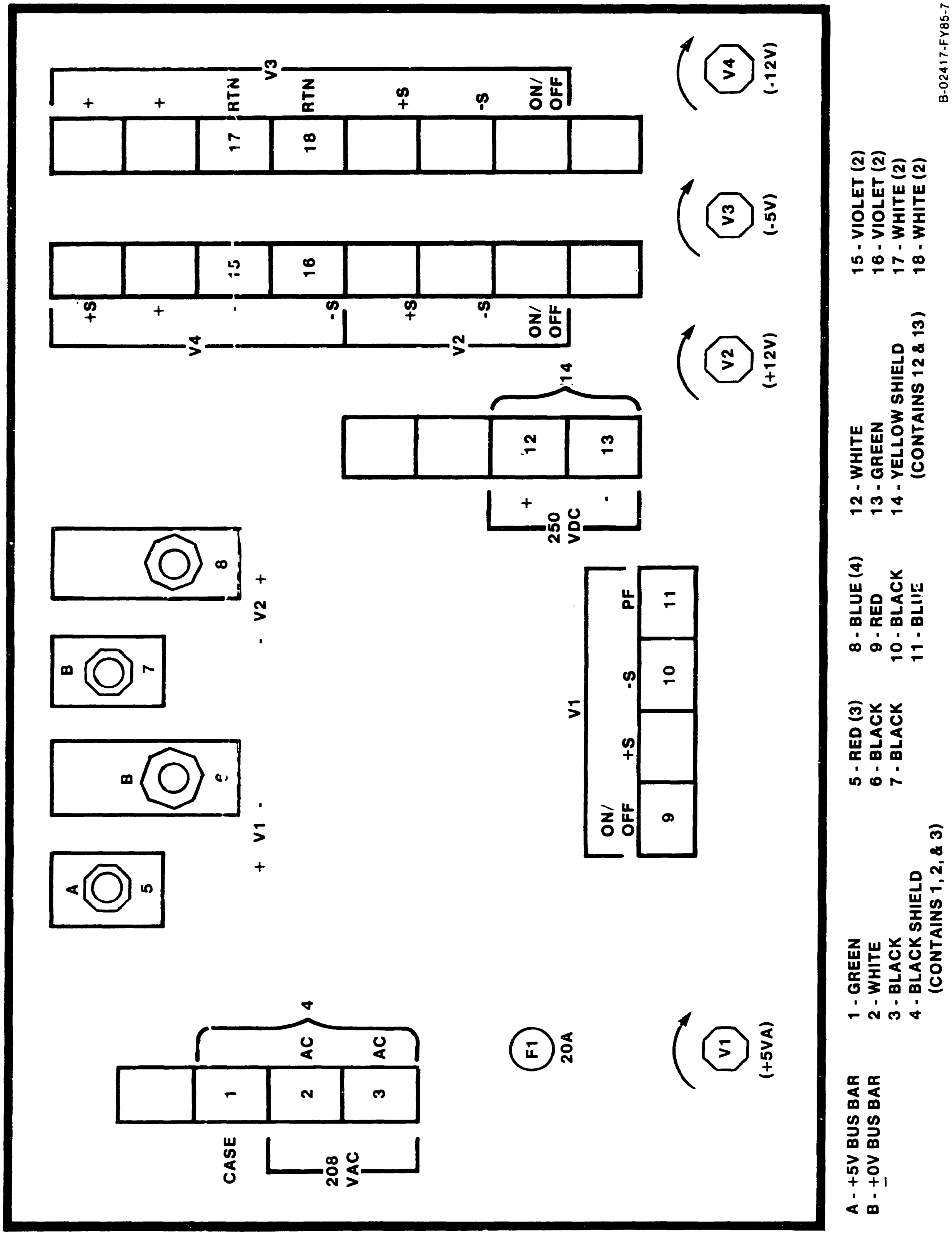
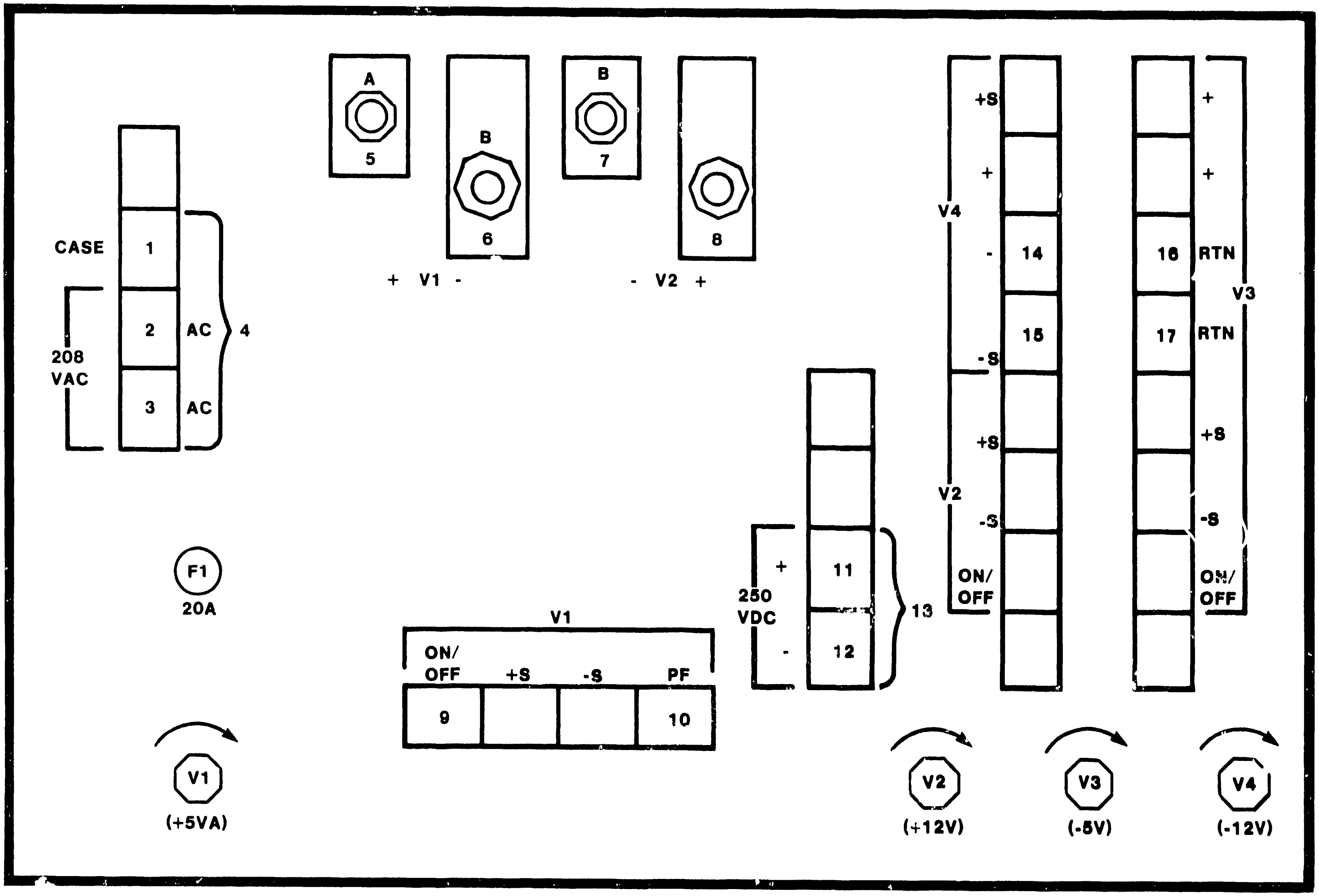


Figure 5-52. Multioutput Power Supply Wiring Connections (With Original Single DC Distribution Board)

Figure 5–52a. Multioutput Power Supply Wiring Connections (With New Second DC Distribution Board)



A- +5V BUS BAR
B- ±OV BUS BAR

1-GREEN
2-WHITE
3-BLACK
4-BLACK SHIELD
(CONTAINS 1, 2, & 3)

5-RED (5)
6-BLACK (2)
7-BLACK (2)

8-BLUE (3)
9-RED
10-BLUE

11-WHITE
12-GREEN
13-YELLOW SHIELD
(CONTAINS 11 & 12)

14-VIOLET (1)
*15-VIOLET (1)
16-WHITE (1)
*17-WHITE (1)

* FINAL VERSION SHOULD BE (1)
BUT FCO'D VERSION MAY BE (2).

B-02983-FY86-3

Table 5-11. Multioutput Power Supply Wiring Color Codes

Voltage	Color Code
240 dc	Yellow shield
220 ac	Black shield
+5	Red
-5	White
+12	Blue
-12	Violet
+/- 0	Black

9. Loosen the two hex head screws securing the base clamping plate at the rear (connection side) of the power supply.
10. Remove the two hex head screws securing the power supply assembly to the mainframe base at the front of the cabinet.
11. Pull the assembly forward and out of the mainframe.

5.3.2.23 Multioutput Switching Power Supply Replacement

1. To reinstall the multioutput power supply, reverse the removal procedure.
2. Reinstall all of the power supply wiring as shown in figures 5-52 or 5-52a, and table 5-11.
3. Reconnect the yellow 3-pin battery power cable connector to J8 of the 210-8717 Battery Backup board.
4. Power up the system and check and adjust the power supply voltages as described in paragraph 5.2.4.1.
5. Reinstall all covers and panels.

5.3.2.24 Booster Switching Power Supply Removal

Remove the booster switching power supply as follows:

WARNING

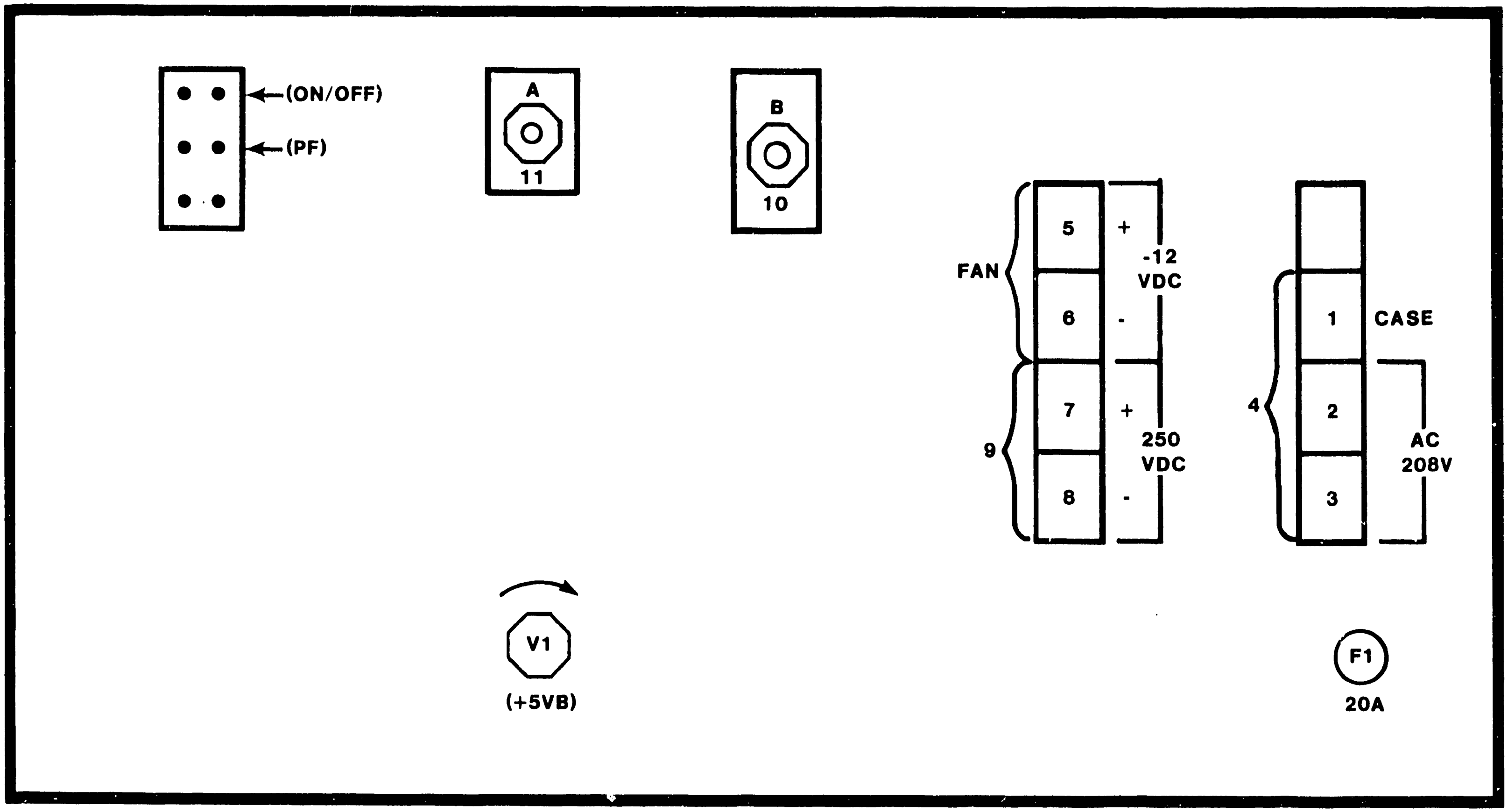
```
*****************************************************************
*                                                               *
*     DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY          *
*     CIRCUMSTANCE. EXTREMELY DANGEROUS VOLTAGE AND             *
*     CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-         *
*     LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.     *
*                                                               *
*     DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER              *
*     SUPPLY; IT IS FIELD REPLACEABLE ONLY.                     *
*                                                               *
*     AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC     *
*     POWER CONNECTOR FROM THE POWER SOURCE RECEPTACLE,         *
*     ALLOW ONE MINUTE BEFORE REMOVING THE POWER SUPPLY TO      *
*     PROVIDE ADEQUATE TIME FOR ANY RESIDUAL VOLTAGE TO         *
*     DRAIN THROUGH THE BLEEDER RESISTORS.                      *
*                                                               *
*****************************************************************
```

1. Enter Control Mode from the SCU Console Mode Menu.
2. Power down the mainframe by pressing the Front Panel Power Off push-button (or SW2, Off, on the Power Supply Controller).
3. Turn off the ac On/Off circuit breaker.
4. Remove the top cover and left side panel.
5. Open the front hinged door.
6. Remove the screws from the rear fan panel, disconnect the two fans and set aside the panel.
7. Remove the two bottom left blank I/O panels on the rear of the main frame.

CAUTION

If it is necessary to reconnect the yellow 3-wire battery power cable to J8 (below), wait several seconds after the LED on the Battery Backup Board goes out or the Battery Backup board will be damaged.

8. Disconnect the yellow 3-pin battery power cable connector from J8 of the 210-8717 Battery Backup Board.
9. All wiring is color coded as listed in table 5-12. Using figure 5-53 and table 5-12, disconnect the bus bars, the wiring from the power supply terminals, and the 6-pin connector on the front of the supply.



A - +5V BUS BAR
B - $\pm$0V BUS BAR

1 - GREEN
2 - WHITE
3 - BLACK
4 - BLACK SHIELD
(CONTAINS 1, 2, & 3)
5 - BLACK
6 - BLUE

7 - RED
8 - BLACK
9 - YELLOW SHIELD
(CONTAINS 7 & 8)
10 - BLACK (2)
11 - RED (2)

B-02417-FY85-1

Figure 5-53. Booster Power Supply Wiring Connections

Table 5-12. Booster Power Supply Wiring Color Codes

Voltage	Color Code
240 dc	Yellow shield
220 ac	Black shield
+5	Red
-12 (fan)	Blue
+/- 0	Black

10. Loosen the two hex head screws securing the base clamping plate at the rear (connection side) of the power supply.
11. Remove the two hex head screws securing the power supply assembly to the mainframe base at the front of the cabinet.
12. Pull the assembly forward and out of the mainframe.

5.3.2.25 Booster Switching Power Supply Replacement

1. To reinstall the booster power supply, reverse the removal procedure.
2. Reinstall all of the power supply wiring as shown in figure 5-53 and table 5-12.
3. Reconnect the yellow 3-pin battery power cable connector to J8 of the 210-8717 Battery Backup Board.
4. Power up the system and check and adjust, if necessary, the power supply voltages as described in paragraph 5.2.4.1.
5. Reinstall all covers and panels.

CHAPTER 6 ILLUSTRATED PARTS BREAKDOWN

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CHAPTER 6

IPB

6.1 SCOPE

This chapter contains the illustrated parts breakdown and power and signal cable part numbers for the VS-300 Computer System. Use this IPB for part number identification when ordering field-replaceable components.

Table 6-1. VS-300 PCB Complement

Board Description	WLI P/N
5-Channel, Duo-Binary RF Modem (10MBPS)	210-8142-A
AC Distribution	210-8715
APA (Active Port Assembly)	210-8504
APA Terminator	210-8503
Address Generation Unit	210-8832
Address Translation Unit	210-8833
BNC/TNC (APA)	210-8509
Backplane (Motherboard) (Note)	210-8837
Battery Backup	210-8717
Block Connector (MLTC)	210-8497
CIU BLANC IOC (23V79)	210-8392-A
CIU CAB IOC (23V79)	210-8391
Central Processing Unit	210-8831
Control Panel	210-8711
DC Distribution (2 boards)	210-8716
Floating Point Unit	210-8830
Kennedy Tape IOC (23V95-1)	210-8790
Main Memory (4 megabytes)	210-8703
Main Memory (8 megabytes)	210-8703-1
Memory Control Unit	210-8834
Multiline TC Controller IOC (23V96)	210-8491-A
Power Supply Controller	210-8709
RS232A Interface (MLTC)	210-8494
RS366 Interface (MLTC)	210-8495-A
RS449 Interface (MLTC)	210-8730
SMD IOC (23V98-1/2/3/4)	210-8785
Serial IOC (23V97)	210-8609
Serial Communications Link (MLTC)	210-8496
Support Control Unit	210-8835
System Bus Interface	210-8836-A
Telex Tape IOC (23V95-2)	210-8789
X.21 Interface (MLTC)	210-8493

NOTE

Order motherboard assembly WLI P/N 270-5017.

Table 6-2. SCU (PC) PCB Complement

Board Description	WLI P/N
CPU (256KB) (P/N is unique to VS-300)	210-9521-1B
Local Comm. Data Link (2-board Local Comm. option)	210-9245-A
Local Comm. Processor (2-board Local Comm. option)	210-9246-A
Monochrome Monitor	210-9343-A
PCI (PC to SCU Interface) (P/N is unique to VS-300)	210-8377
Single Board Local Comm. Option	210-8310
Winchester Controller	210-9225

Table 6-3. VS-300 Power Cables

Source	Destination	Description	P/N
220-2343 APA cable	APA (J3)	3-pin	220-2339
220-2343 MLTC cable	SCL (MLTC) (J2)	5-pin → 4-pin	220-2372
220-2343 MLTC cable	SCL (MLTC) (J2) (new type)	"Y" cable	220-2400
220-2343 P-Band	P-Band modem (J2)	5-pin	220-2402
220-2375 G/A cable	CPU/Gate Array (J1)	6-pin	220-2374
220-2383 fan cable	Bottom card cage fans	3-pin	220-2386
220-2383 fan cable	Top card cage fans	3-pin	220-2385
APA (J3)	APA (J4) (2nd APA)	3-pin	220-2346
Ac Dist.	Battery charging p/s (ac in)	3-pin	220-2293
Ac Dist.	Booster p/s (ac in)	3-pin	220-2297
Ac Dist.	Card cage fan cable	3-pin	220-2383
Ac Dist.	Multioutput p/s (ac in)	3-pin	220-2296
Ac Dist.	Rear panel fan assy.	3-pin	220-2384
Ac Dist. (J1)	P/S Controller (J9)	5-pin	220-2294
Bat. Backup (J1)	Battery charging p/s	6-pin	220-2302
Bat. Backup (J3-J7)	Battery pack (5 cables)	2-pin	220-2301
Bat. Backup (J8)	Multioutput & booster p/s	2-pin	220-2292
Cable Concen. p/s	APAs (Cable Concentrator)	3-pin	220-2345
Dc Dist. (J1)	Booster p/s	2-pin	220-2299
Dc Dist. (J1-J10)	APA cable	5 pin	220-2343
Dc Dist. (J1-J10)	CIU CAB and CIU Modem	"Y" cable	270-3380
Dc Dist. (J1-J10)	G/A cable	6-pin	220-2375
Dc Dist. (J1-J10)	MLTC cable	5-pin	220-2343
Dc Dist. (J1-J10)	P-Band modem cable	5-pin	220-2343
Dc Dist. (J11)	SCU (PC)	15-pin	220-2298
Dc Dist. (J2)	P/S Controller (J1)	6-pin	220-2300
Dc Dist. (second)	Backplane (J32 & J33)	Dc power out	270-3359
Multioutput p/s	Dc Dist. (first) (TB1)	Dc power out	270-3376
Multioutput p/s	Dc Dist. (second) (TB1)	Dc power out	270-3350
P/S Controller (J2)	P/S Controller (J2)	2-pin jumper	220-2344
Power receptacle	Cable Concentrator unit	Ac power in	420-2040
Power receptacle	VS-300 PDU	Ac power in	220-0503
SCL (MLTC) (J3)	SCL (MLTC) (J2) (2nd SCL)	4-pin daisy	220-2373

Table 6-4. VS-300 Signal Cables

Source	Destination	Description	P/N
AGU (J2)	ATU (J2)	50-pin	220-3472
APA (J2) (1st APA)	APA (J1) (2nd APA)	36-pin daisy	220-3319
APA (J5)	BNC/TNC (J1) (APA)	40-pin jumper	220-3344
APA Port 0	C.C. J9&J10 (panel)	Coax	220-0216
Bat. Backup (J2)	P/S Controller (J8)	6-pin	220-2303
Bat. Backup (J7)	Bat. Backup (J7) (low bat.)	Test jumper	220-2341
Booster p/s	P/S Controller (J4)	3-pin	220-2306
Bulkhead	Remote diagnostic modem	25-pin	220-0332
C.C (panel)	Cable Concentrator	34-pin (25')	220-0510
C.C. J9&J10 (panel)	SCU Local Comm.	Coax	220-0522

Table 6-4. VS-300 Signal Cables (Cont'd)

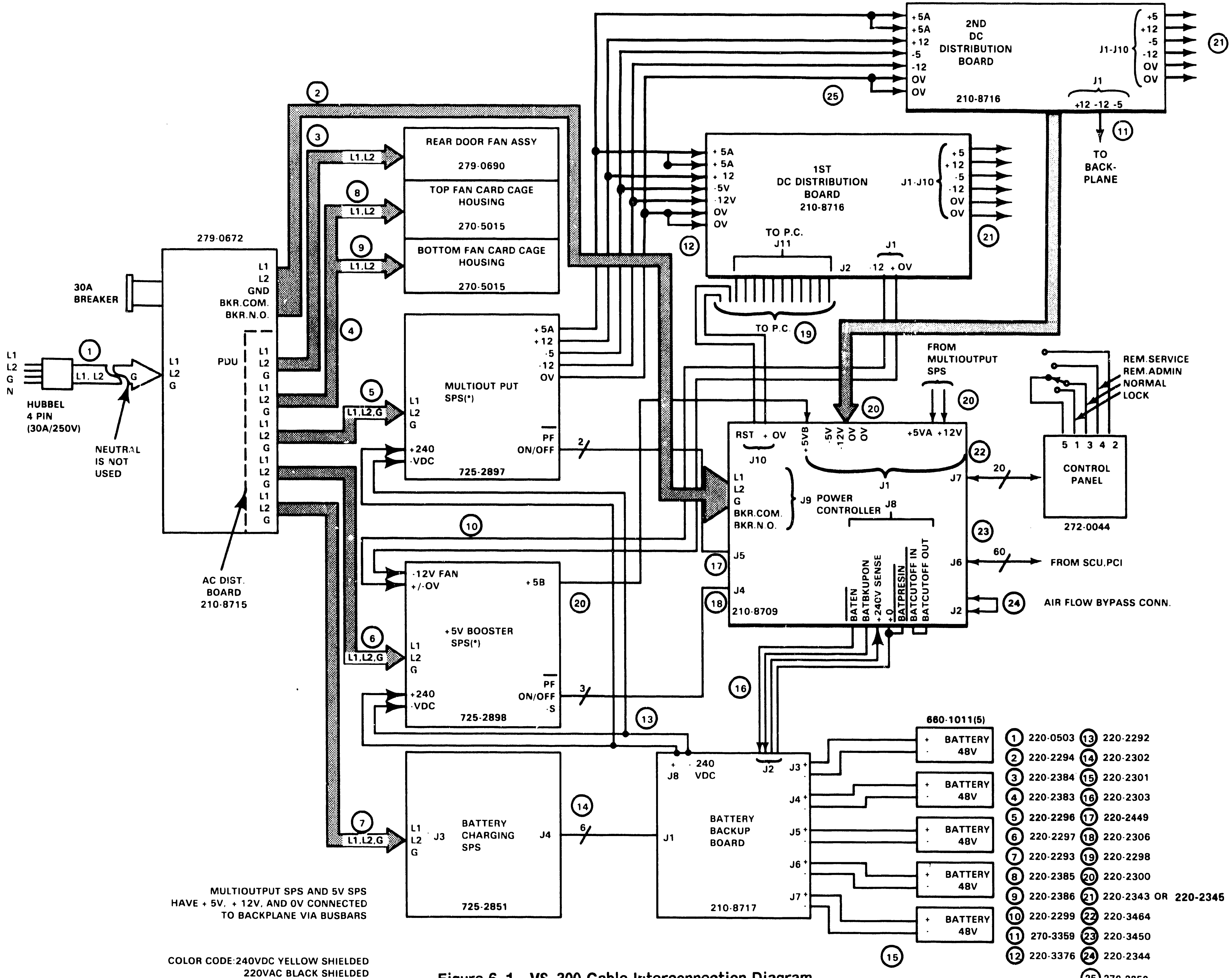
Source	Destination	Description	P/N
CIU BLANC IOC (J1)	CIU CAB (J2)	40-pin	220-3463
CIU CAB (J1)	CIU Modem (J1) (5-channel)	34-pin (2")	220-3456
CIU CAB (J1)	CIU Modem (J1) (1-channel)	34-pin (11")	220-3529
CPU (J1)	AGU (J1)	50-pin	220-3472
Cable Concentrator	Global modems (P-Band)	36-pin	220-3471
Control Panel	Control Panel (internal)	26-pin	220-3465
Control Panel (J1)	P/S Cont. (J7)	20-pin → 26-pin	220-3464
Kennedy (J1,2)	Tape panel (Kennedy)	50-pin	220-3462
MLTC IOC (J1 → J4)	SCL (MLTC) (J1)	50-pin	220-3484
Multioutput p/s	P/S Controller (J5)	3-pin	220-2449
P/S Cont. (J6)	SCU (backplane) → SCU (PCI)	60-pin	220-3450
P/S Cont. (P4/P5)	P/S Cont. (P4/P5) (p/s test)	Test jumper	220-2342
SCU CPU (J3)	Bulkhead	4-pin	220-0498
SCU CPU (J4)	Bulkhead (Remote Diag.)	25-pin	220-3448
SCU Monochrome (J1)	Bulkhead	8-pin	220-0499
SCU Monochrome (J2)	Bulkhead	5-pin	220-0499
SMD IOC (J1)	Disk panel B-cable (drive 0)	26-pin B-cable	220-3457
SMD IOC (J2)	Disk panel B-cable (drive 1)	26-pin B-cable	220-3458
SMD IOC (J3)	Disk panel B-cable (drive 2)	26-pin B-cable	220-3459
SMD IOC (J4)	Disk panel B-cable (drive 3)	26-pin B-cable	220-3460
SMD IOC (J5)	Disk panel A-cable	60-pin A-cable	220-3390
Serial IOC (J1)	C.C (panel)	36-pin	220-3470
Serial IOC (J2)	APA (J1)	36-pin	220-3455
Telex IOC (J1,2,3)	Tape panel (Telex)	50-pin	220-3462

NOTES

1. C.C. (panel) is the Cable Concentrator output connector panel on the top rear of the VS-300 main frame.
2. Cable Concentrator is the actual free standing Cable Concentrator unit.

Table 6-5. VS-300 Disk Drive Cables

Source	Destination	Description	Length	P/N
I/O panel	Any drive	B signal cable	15 feet	220-3355
I/O panel	Any drive	B signal cable	25 feet	220-3356
I/O panel	Any drive	B signal cable	50 feet	220-3357
I/O panel	First drive	A signal cable	15 feet	220-3358
I/O panel	First drive	A signal cable	25 feet	220-3359
I/O panel	First drive	A signal cable	50 feet	220-3360
Drive	Drive	A signal cable ("Daisy chain")	10 feet	220-3361



MULTIOUTPUT SPS AND 5V SPS HAVE + 5V, + 12V, AND 0V CONNECTED TO BACKPLANE VIA BUSBARS

COLOR CODE: 240VDC YELLOW SHIELDED
220VAC BLACK SHIELDED
+5VDC RED
-5VDC WHITE
+12VDC BLUE
-12VDC VIOLET
+/-OVDC BLACK

Figure 6-1. VS-300 Cable Interconnection Diagram

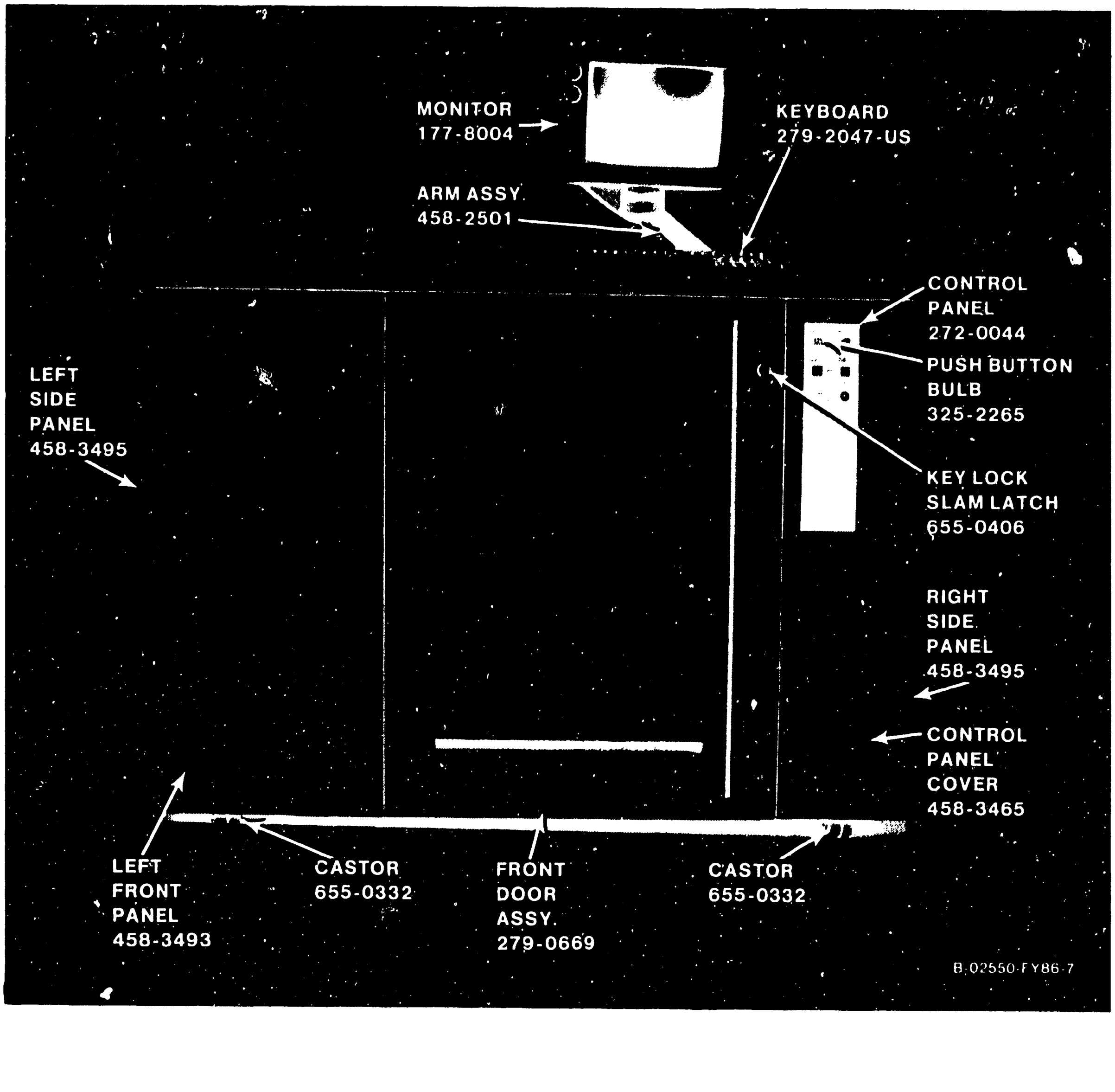


Figure 6-2. VS-300 Front View

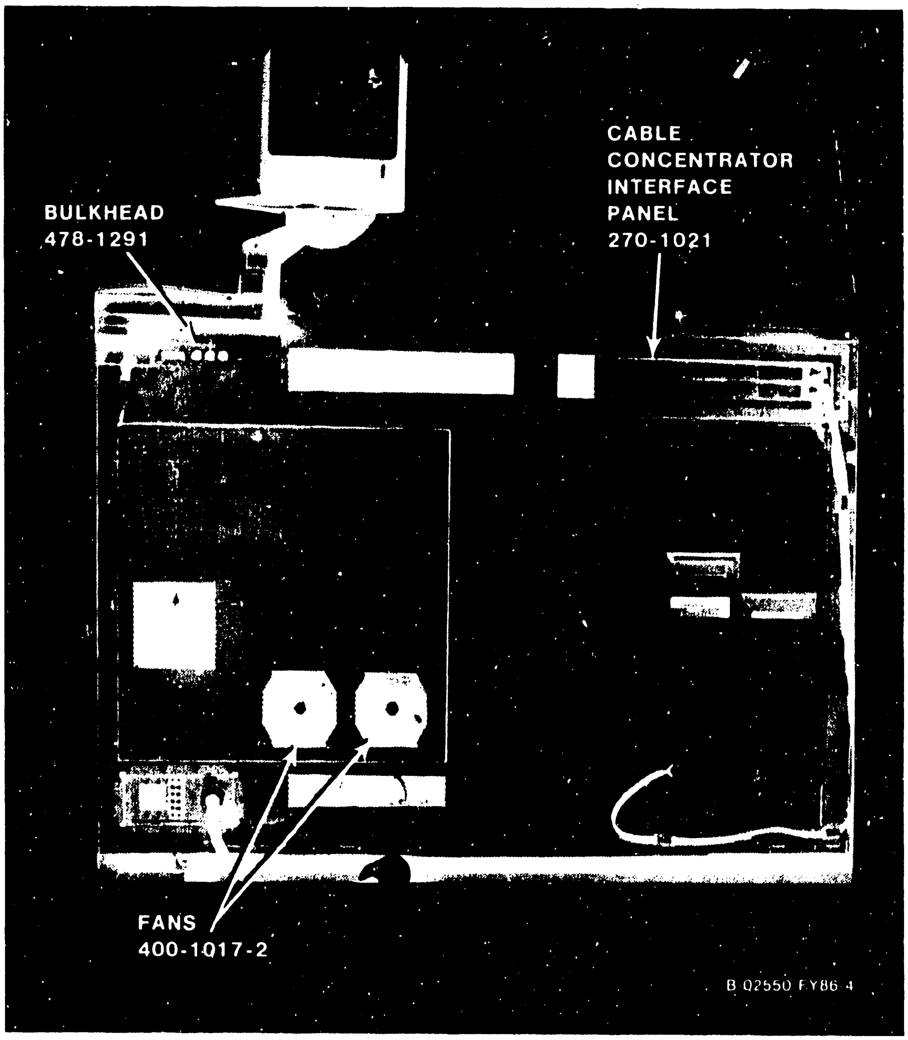


Figure 6-3. VS-300 Rear View With Covers On

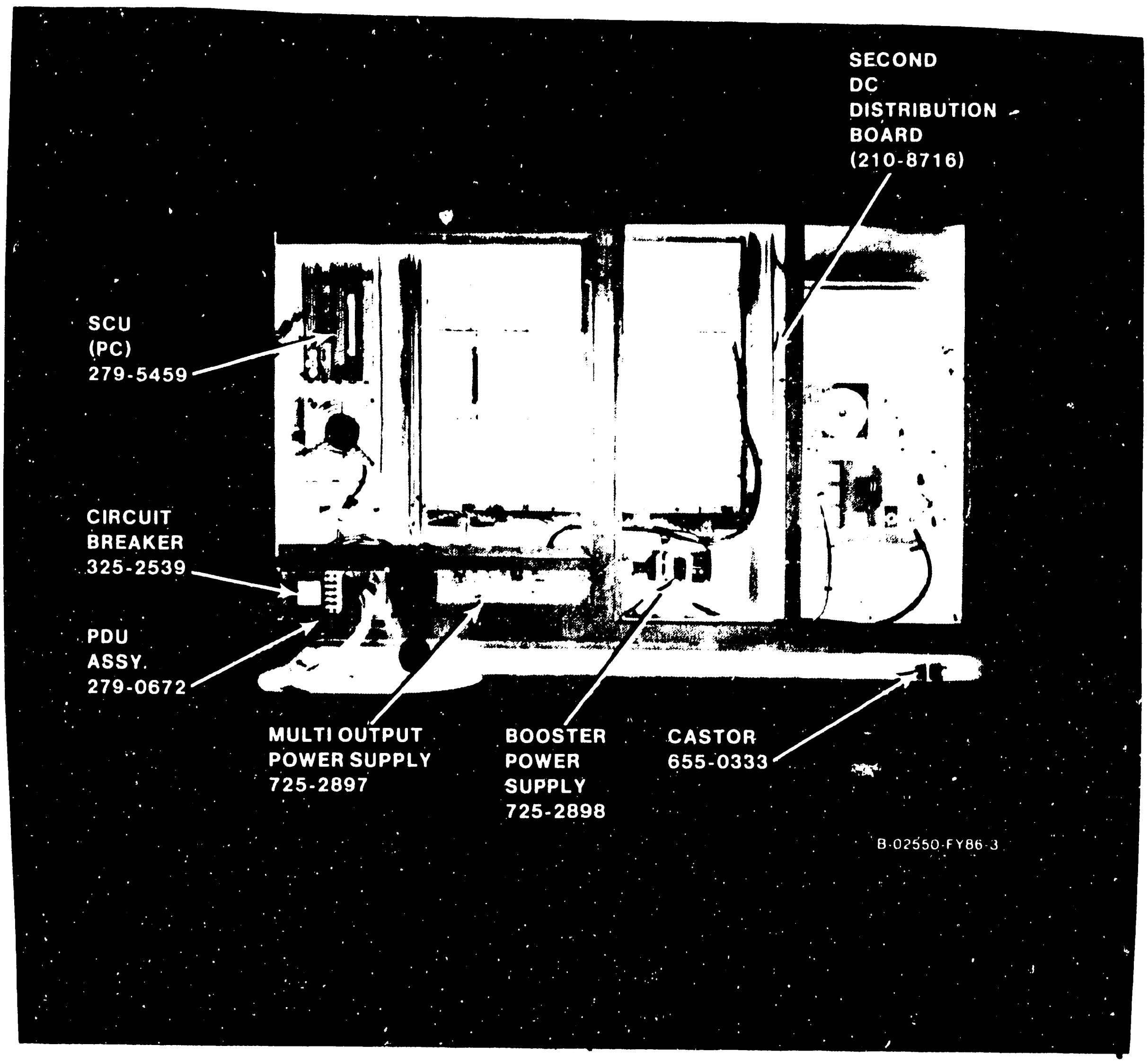


Figure 6-4. VS-300 Rear View With Covers Off

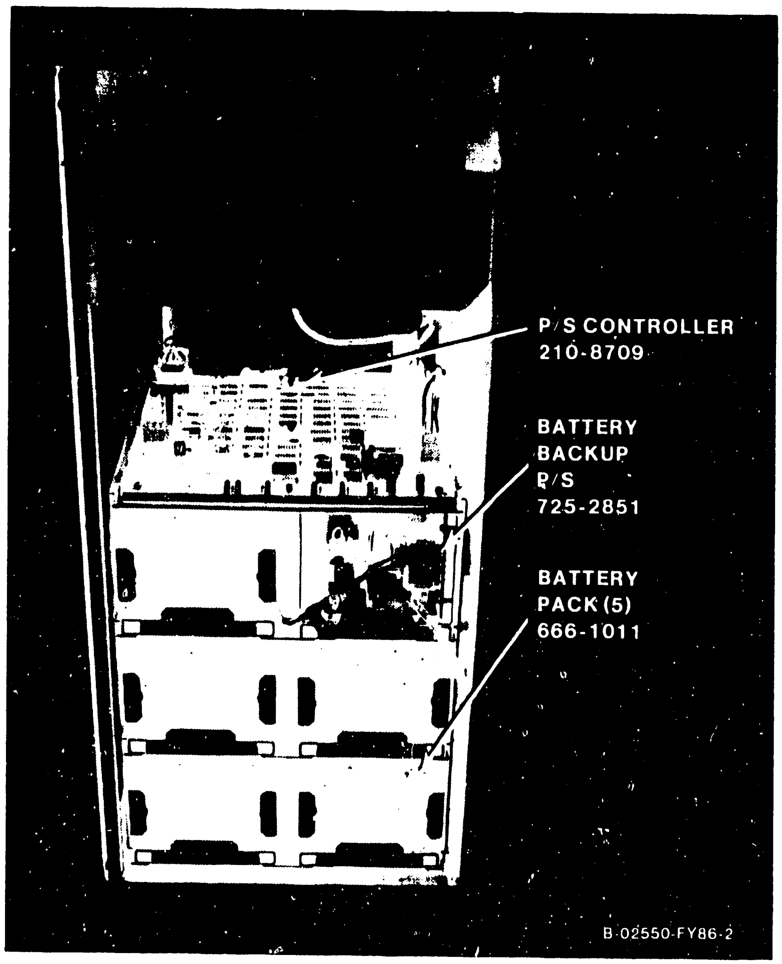


Figure 6-5. VS-300 Battery Backup Section

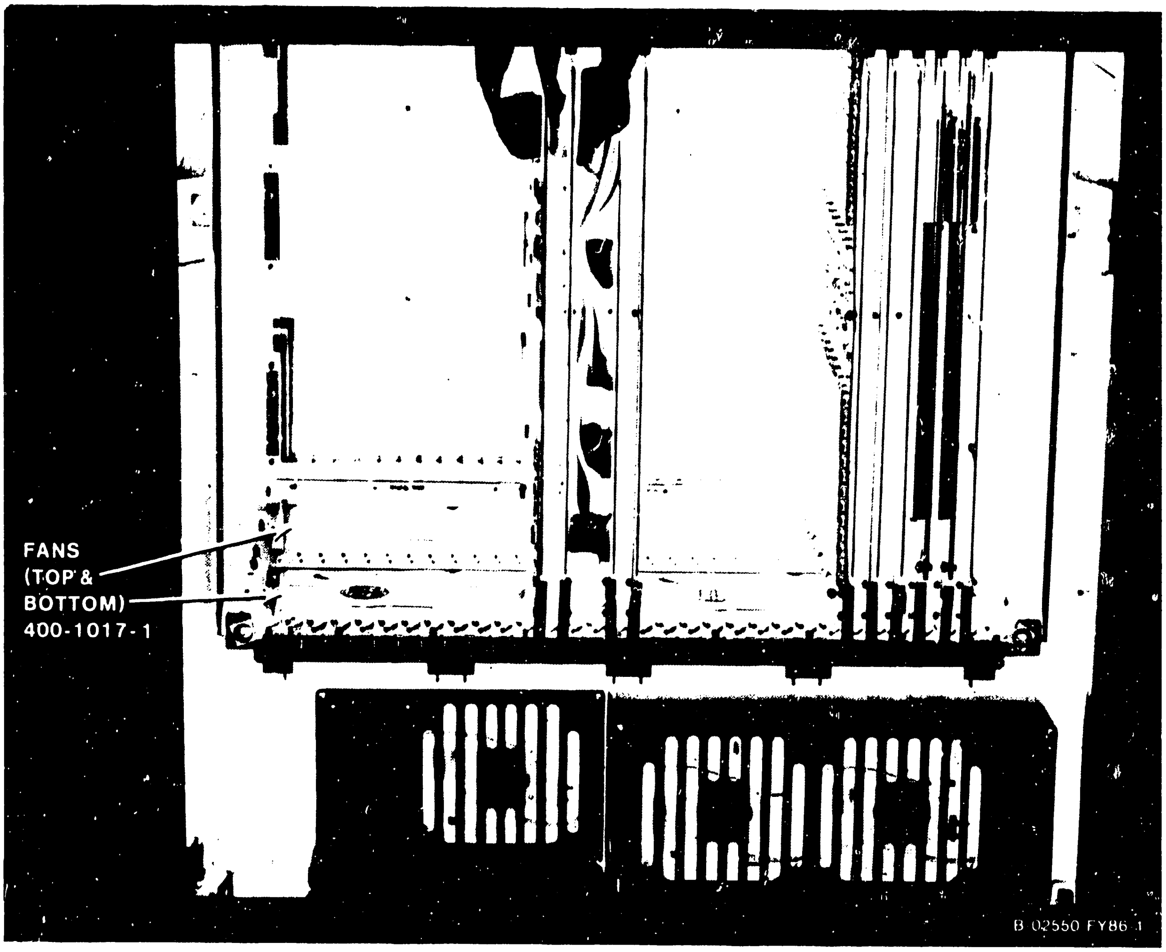


Figure 6-6. VS-300 Card Cage

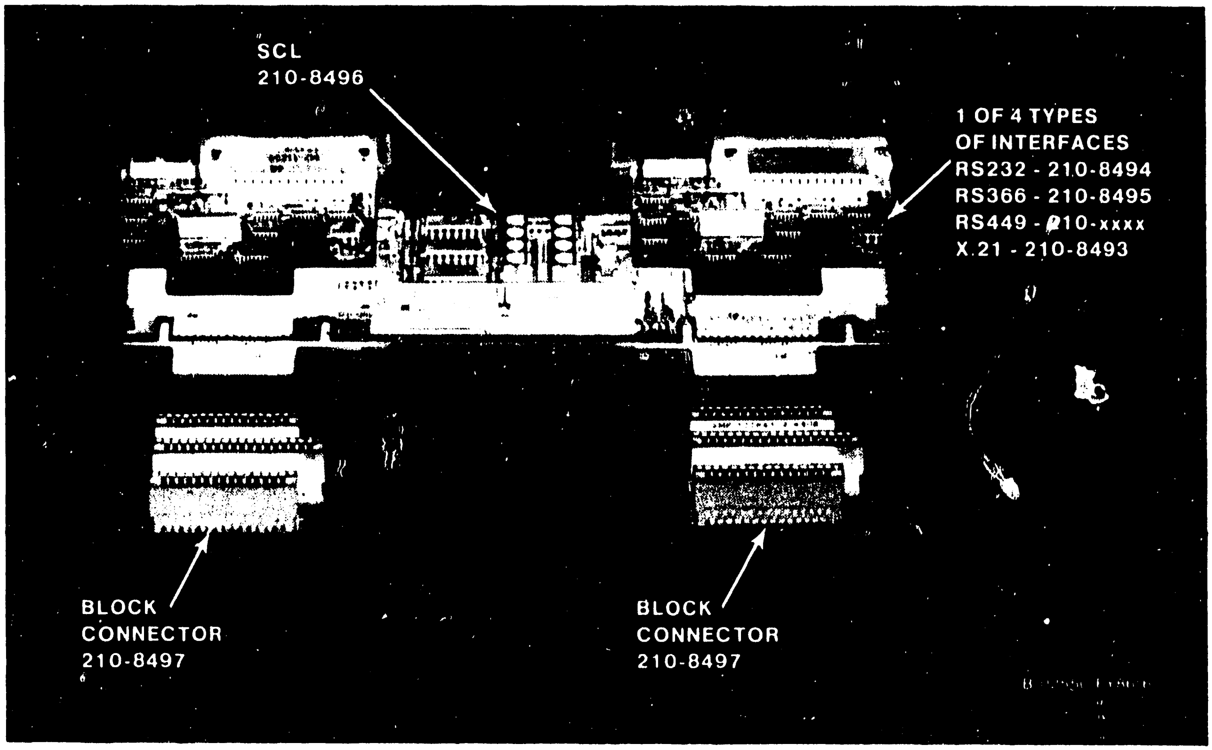


Figure 6-7. VS-300 Multiline TC Back Panel Without Cables

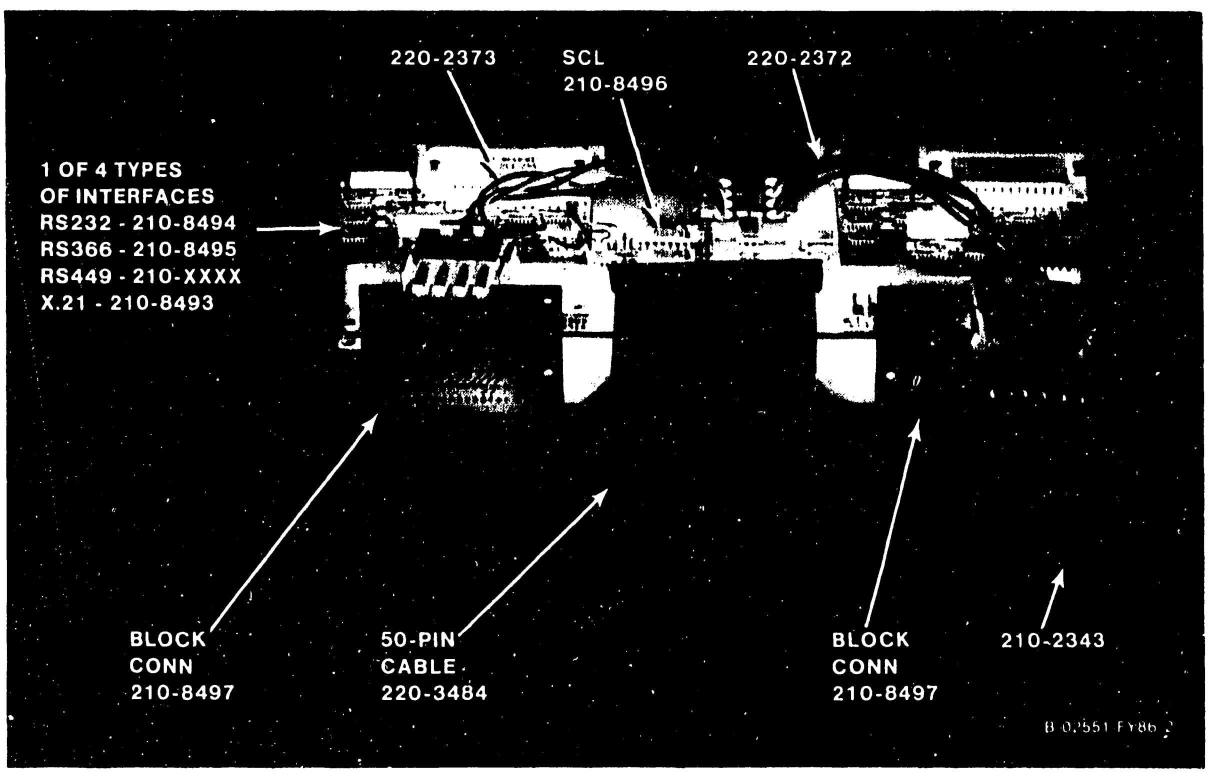


Figure 6-8. VS-300 Multiline TC Back Panel With Cables

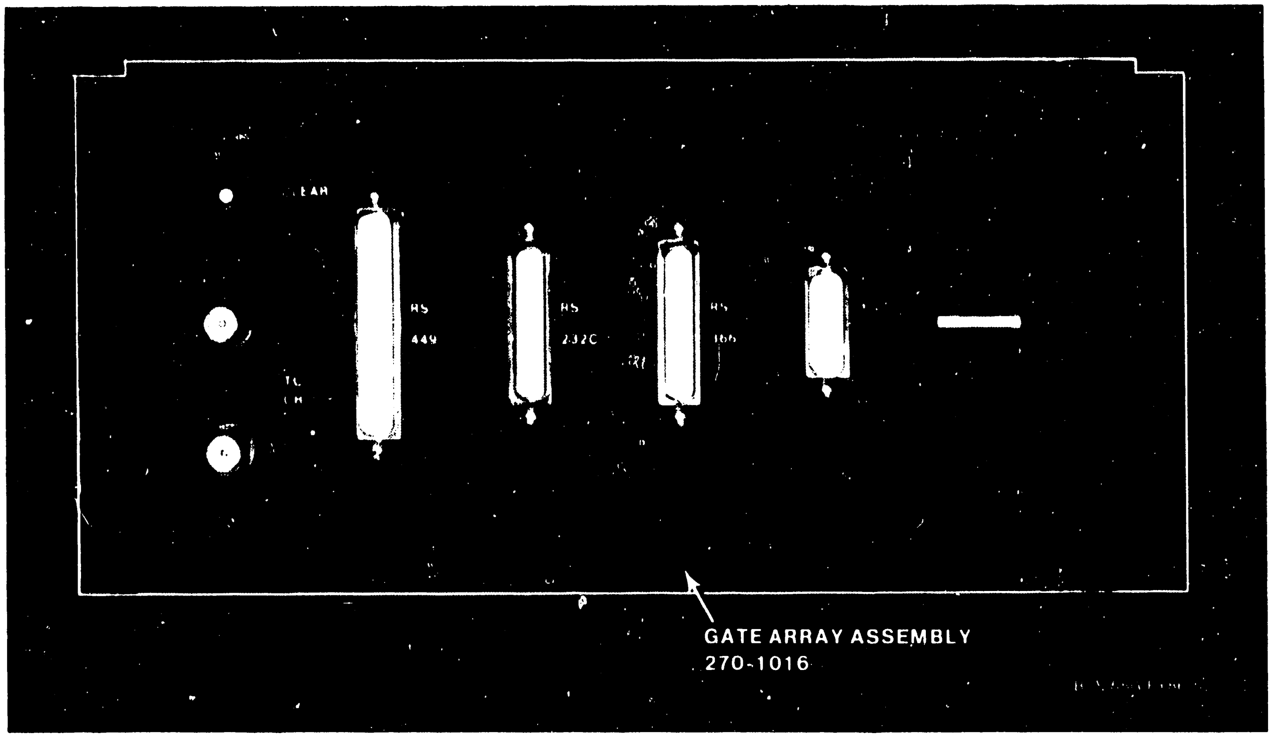


Figure 6-9. VS-300 Gate Array TC Back Panel Assembly

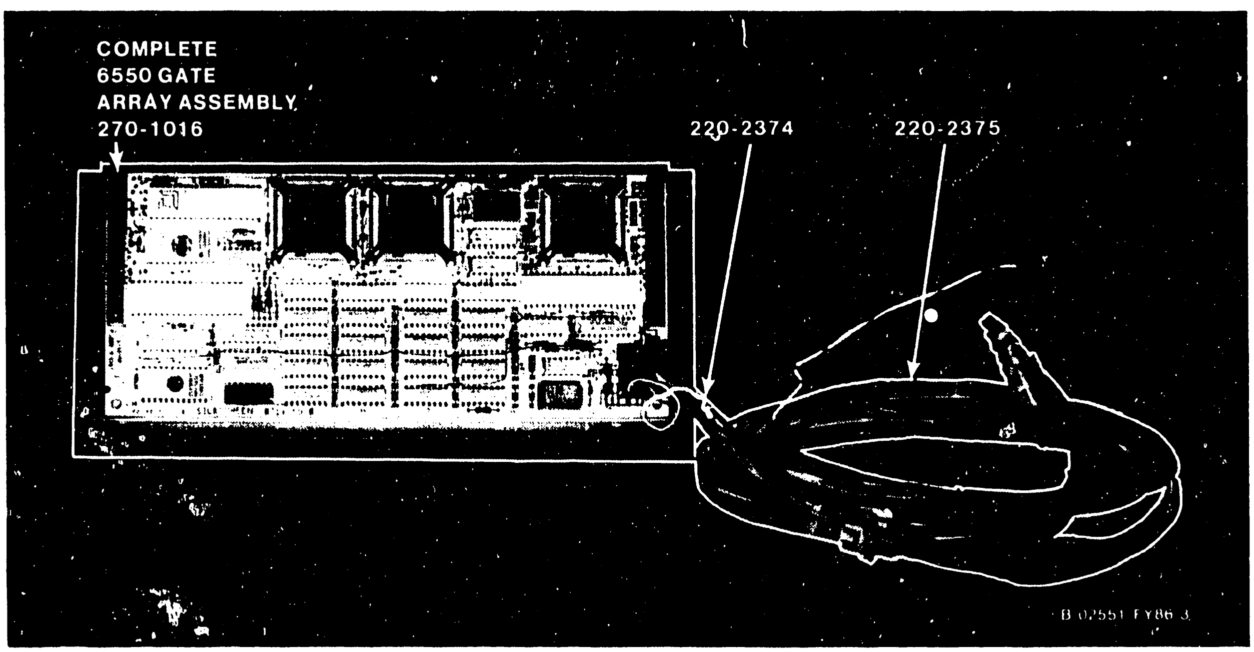


Figure 6-10. VS-300 Gate Array TC Back Panel Assembly With Cables

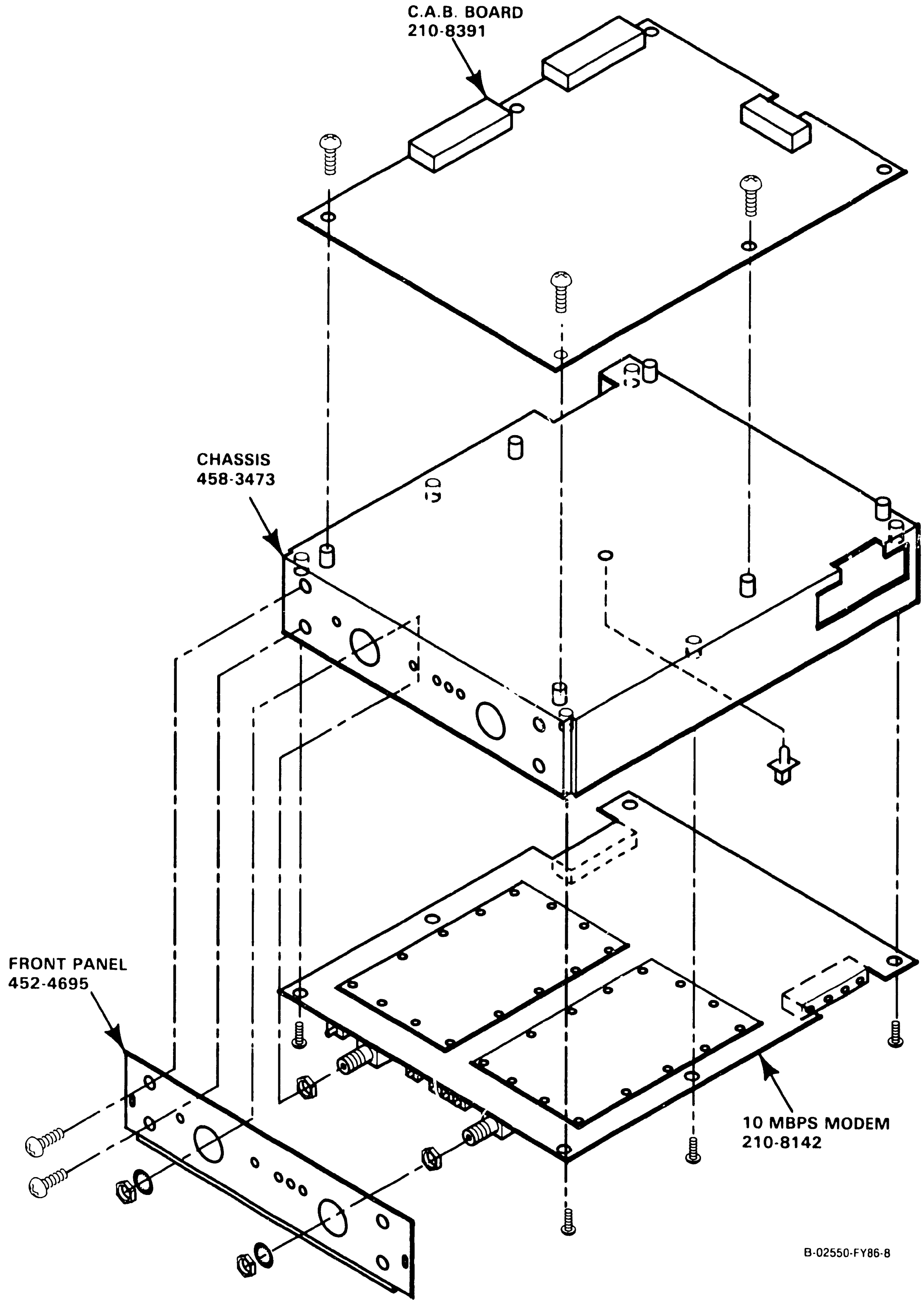


Figure 6-11. VS-300 CIU C.A.B./Modem Back Panel Assembly

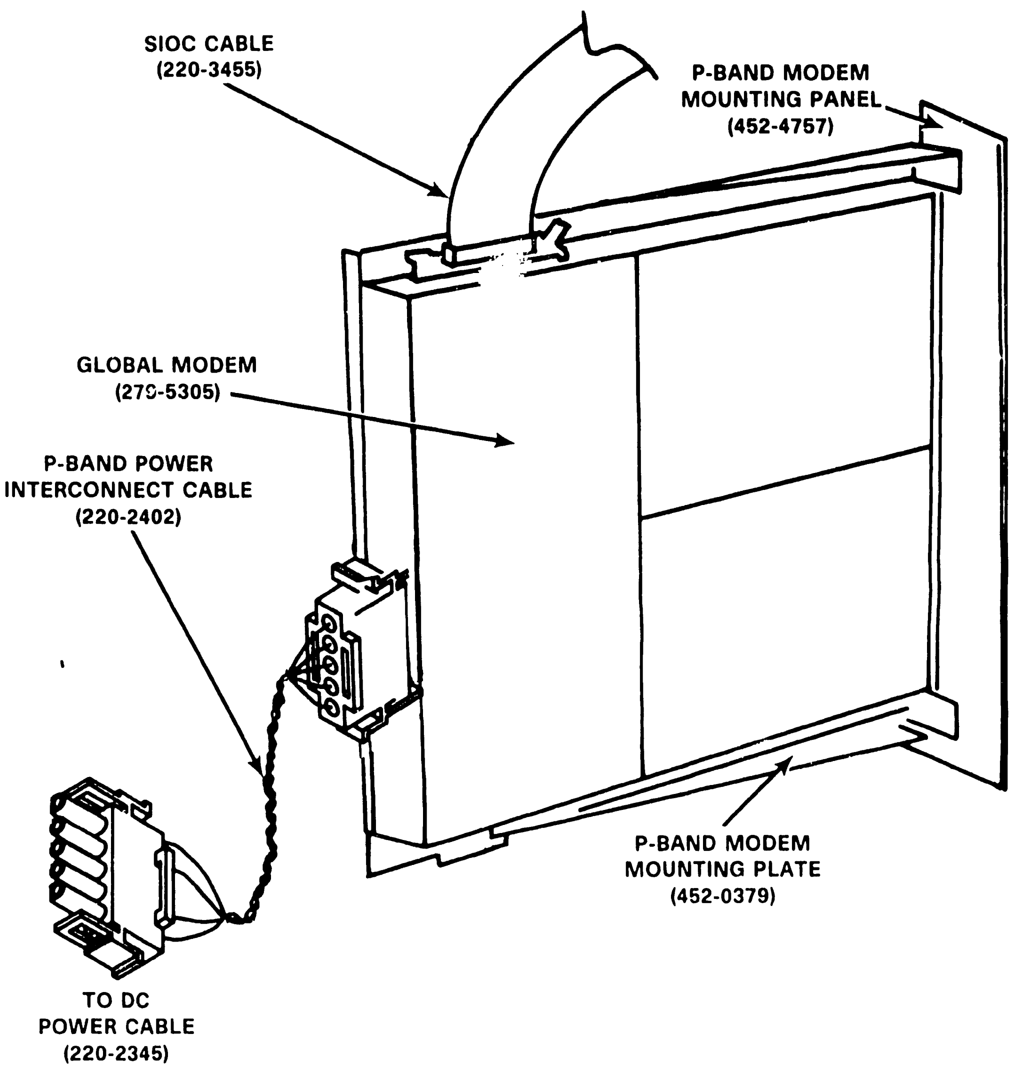


Figure 6-12. VS-300 Global Modem Assembly 270-1020

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CHAPTER 7

TROUBLESHOOTING

7.1 GENERAL

This chapter provides information on diagnostics, memory dumps, power fault isolation, error log, and the service log. With these troubleshooting tools, most of the problems that occur in the system can be located and repaired. Two types of diagnostics are available in the VS-300: off-line diagnostics which are used to test the central processor (CP), memory, and input/output controllers (IOCs) at power up or front panel reset prior to initial program load (IPL) or after board replacement; and on-line diagnostics which provide general purpose utilities and exercisers for peripherals. All diagnostics should be run before turning the system over to the customer at installation or whenever system integrity is questionable.

7.2 OFF-LINE DIAGNOSTICS

The VS-300 off-line diagnostics are contained in an application program called the Diagnostic Control System (DCS), which runs under MSDOS in the Support Control Unit (SCU). The DCS is a collection of Central Processor (CP), Memory, and IOC diagnostics that resides on the Winchester fixed disk within the Professional Computer (PC) section of the SCU. DCS diagnostics may be run from the SCU, which consists of the PC and the SCU interface board, even when the VS system is not functioning.

NOTE

The customer cannot use the system while the off-line diagnostics are running.

7.2.1 POWER-UP DIAGNOSTICS

At power up (or front panel reset), the DCS automatically invokes the Confidence Diagnostic, which determines, to a high degree of certainty, whether the system will IPL and run. The Confidence Diagnostic consists of the CPU Unit Diagnostic and the I/O Built-in Test (BIT) Monitor.

The CPU Unit Diagnostic is a partial test of the central processor, targeting primarily the interboard signals. The I/O BIT Monitor tests all of the IOCs installed in the system, including both the controller and device adapter sections of the boards.

If an error occurs at any point in the Confidence Diagnostic, the diagnostic halts and an error message is displayed on workstation 0, including the error code and the most likely failing field-replaceable unit (FRU).

7.2.2 ACCESSING DCS DIAGNOSTICS

The DCS diagnostics are accessed from the Wang VS System Console menu. Refer to figure 7-1 below. The System Console screen appears at power up after the SCU software is loaded.

```
                     *** WANG VS System Console ***

SYSCON Version X.X.X           2:44 PM        Monday  February 11, 1986



          Press (HELP) for on-line system console information.



                Use the function keys to select a command:

(1) ENTER Workstation Emulation           (8) RESET System
(2) ENTER Control Mode                    (9) RESET Console

                                          (12) SET Console Defaults
(5) AUTO IPL                              (13) Set Time and Date
```

Figure 7-1. System Console Menu

NOTE

The position of the front panel key switch determines which of the items in the above menu are available. Available items will be highlighted. To access off-line diagnostics, the key must be in the "Remote Service" position.

The System Console screen may also be reached by the following method:

1. Press CONTROL then SHIFT + CANCEL simultaneously from the VS Operator's Console, VS Command Processor menu, or the VS Logon screen to exit workstation emulation.

2. The Workstation Emulation screen appears. Refer to figure 7-2 below.

3. Space down to "Suspend Emulation" and press EXEC.

4. The Wang VS System Console screen appears.

```
                  Wang Professional Computer
              D I S K  O P E R A T I N G  S Y S T E M
                              VS
                     Workstation Emulation
                         Version X.XX

Select an Item and Proceed

                    _ Return to Emulation
                    ■ Suspend Emulation
                    _ Terminate Emulation
                    _ Restart Emulation

                                          SPACE - Item Select
                                          EXEC  - Proceed
```

Figure 7-2. Workstation Emulation Menu

Certain elements of the System Console Menu are password-protected to prevent unauthorized use of some SYSCON facilities. These elements are not immediately displayed. They include (3) ENTER Service Log mode and (4) ENTER Off-line Diagnostics. To enable these and other menu picks, perform the following steps:

1. Go to the System Console screen.

2. Ensure that the keyswitch is in the "Remote Service" position.

3. Enter the following password:

   CSG + current time (four digits) as displayed on the System Console screen. Example: If time is 9:30 (am or pm), enter 0930.

NOTE

> While entering the password, the keyboard beeper will sound as each key is pressed. This is normal. It is intended to discourage unauthorized personnel from enabling the full System Console menu.

4. Several previously undisplayed menu picks will appear. Refer to figure 7-2a below. The System Console is now in the "service mode." (The service mode can be terminated by pressing PF key 10 or turning the keyswitch out of the "Remote Service" position.)

```
                    *** WANG VS System Console ***

SYSCON Version X.X.X            2:44 PM        Monday  February 11, 1986



          Press (HELP) for on-line system console information.



                Use the function keys to select a command:

 (1) ENTER Workstation Emulation             (8) RESET System
 (2) ENTER Control Mode                      (9) RESET Console
 (3) ENTER Service Log Mode                 (10) Terminate Service Mode
 (4) ENTER Off-line Diagnostics             (11) Show Error Log
                                            (12) SET Console Defaults
 (5) AUTO IPL                               (13) Set Time and Date
(29) Install Software                       (32) Wang PC Emulation
```

Figure 7-2a. System Console Screen in Service Mode

Press PF key 4 from the System Console menu and the diagnostics disclaimer screen appears. Refer to figure 7-3 below.

```
                    Wang VS Diagnostic Control System
        REV XXXX      (c) Copr. Wang Laboratories, Inc. 1985


------------------------------N O T I C E--------------------------------

  This diagnostic package is the property of Wang Laboratories, Inc. and
is provided for System diagnostic use only.  Improper use may cause loss
or damage to programs and/or data.  This package and related materials
may not be disclosed or otherwise made available to third parties with-
out the prior permission of Wang.

  In no event shall Wang Laboratories, Inc. or its subsidiaries be liable
for incidental or consequential damages in connection with or arising
from the use of the diagnostic package, the accompanying manual, or any
related materials.

-------------------------------------------------------------------------




                      Press EXEC to continue, CANCEL to exit
```

Figure 7-3. Diagnostics Disclaimer Screen

From the diagnostics disclaimer screen, press EXEC to bring up the DCS Diagnostic Selection menu. Refer to figure 7-4 below.

NOTE

The AGU and FPU diagnostics require DCS Rev 2604 or higher.

```
mm/dd/yy              Wang VS Diagnostic Control System               hh:mm:ss
            REV XXXX      (c) Copr. Wang Laboratories, Inc. 1985


                            _ PCI Diagnostic
                            _ SCUI Diagnostic
                            _ CP8 Static Diagnostic
                            _ CP8 Self Test Diagnostic
                            _ AGU, ESU Diagnostic
                            _ ATU Diagnostic
                            _ SCU-based MCU & Memory Diagnostic
                            _ CPU-based MCU & Memory Diagnostic
                            _ SBI Diagnostic
                            _ I/O BIT Monitor
                            _ CPU Unit Diagnostic
                            _ FPU Diagnostic

                            _ VS Environment


                                                SPACE  - Item Position
                                                INSERT - Select
                                                DELETE - Deselect
                                                EXEC   - Proceed


HELP is available
```

Figure 7-4. DCS Diagnostic Selection Menu

7.2.3 RUNNING OFF-LINE DIAGNOSTICS

NOTE

For best results, the diagnostics should be run in the order in which they are listed on the menu.

To choose a particular diagnostic from the DCS menu (figure 7-4 above), position the cursor next to the desired diagnostic using the SPACE BAR, press INSERT to select the diagnostic (diagnostic will be highlighted), and press EXEC to run the diagnostic. More than one diagnostic or all diagnostics may be selected at one time.

To deselect a single diagnostic, go to the DCS menu, position the cursor next to the diagnostic to be deselected, and press DELETE. The diagnostic will be dehighlighted on the DCS menu and will not execute until it is reselected. To deselect all selected diagnostics, press CANCEL. To terminate a diagnostic, press SHIFT + CANCEL. Also use SHIFT + CANCEL to exit the DCS program from the selection menu.

7.2.3.1 HELP Menu

The DCS HELP menu (figure 7-5 below) is an operator aid that allows the user to display the DCS help text file, display the currently executing diagnostic's help text file, display the DCS log file, and employ the VS Interface Utility. HELP is accessed by pressing the HELP key or SHIFT + HELP keys at any time. The function keys have no effect during the help feature but their state can be changed.

```
mm/dd/yy          Wang VS Diagnostic Control System             hh/mm/ss
            REV XXXX      (c) Copr. Wang Laboratories, Inc. 1985
                           □□□□ ■□□□ □□□□ □□□□
                               H E L P   M E N U

                 ■ Display DCS help file
                 _ Display current diagnostic's help file
                 _ Display Log
                 _ VS Interface Utility

                                                     SPACE  - item select
                                                     EXEC   - proceed
                                                     CANCEL - exit menu

  X.XX.XXi
```

Figure 7-5. DCS HELP Menu Screen

7.2.3.2 DCS Test Screens

Once a diagnostic is selected and EXEC is pressed, a screen specific to that diagnostic is displayed. This screen provides information including the sequence number, the diagnostic rev number and name, the error count, the currently executing diagnostic or test, and the DCS status.

Most of the DCS diagnostic screens are similar with the exception of the VS Environment Diagnostic and the I/O BIT Monitor. Some diagnostics contain menus of their own which allow the user to select or deselect one or more tests within the diagnostic. Tests on these menus are selected and deselected the same way that diagnostics are selected and deselected from the DCS Selection menu. A possible diagnostic screen is shown below in figure 7-6.

```
mm/dd/yy              Wang VS Diagnostic Control System              hh/mm/ss
             REV XXXX     (c) Copr. Wang Laboratories, Inc. 1985
                              □□□□ ■□□□ □□□□ □□□□

      Sequence: 1                                          Error Cnt: 1
    Diagnostic: R1560 CP8 Diagnostics
          Test: Part Two
    Error Code: 201033
  Failing Unit: (1) ATU0 (2) AGU0 (3) CPU0

  | DCS Status: Reporting Diagnostic Error                                  |

    Error detected by diagnostic

         CPU halted at MIA = 07D3

                                         Press PF6 to continue from error
    HELP is available
```

Figure 7-6. Possible DCS Diagnostic Screen

The row of boxes on the third line of the screen indicates which optional functions (if any) are enabled. The boxes correspond to function keys 1 thru 16. Each function key acts as an on/off switch to enable or disable the particular action that the key controls. A filled box indicates the function is enabled; an empty box indicates the function is disabled. Table 7-1 below lists the controlling function keys, the function name, and a description of each function.

Table 7-1. Special Diagnostic Functions

PF KEY	FUNCTION	DESCRIPTION
2	Loop on Error	When an error is reported, the DCS will instruct the diagnostic to loop on the error. The DCS will also count and display the number of times the loop is executed.
3	Loop on Test	The DCS instructs the diagnostic to loop on the just completed test. The DCS counts and displays the number of times the loop is executed.

Table 7-1. Special Diagnostic Functions (Cont'd)

PF KEY	FUNCTION	DESCRIPTION
4	Loop on Diagnostic	The DCS instructs the diagnostic to loop on itself. The DCS counts and displays the number of times the loop is executed.
5	Stop on Error	When an error is reported, the DCS stops and waits for the user to press PF key 6 before continuing the diagnostic.
6	Continue	This key is used to continue from a stop on error, to disable the current looping function without using the loop function key, and to continue from a pause state without turning off the pause function.
7	Log Screen	Enters current screen into the log.
8	Pause	The DCS will pause on requests (calls) from the diagnostic to the DCS before the requested function is performed. PF key 6 can be used to continue or the function can be disabled.
9	Diagnostic Defined	It is not used by the DCS and is dependent upon the executing diagnostic for function definition. If not defined by the diagnostic it has no effect.
10	Diagnostic Defined	
11	Diagnostic Defined	
12	Diagnostic Defined	
13	Undefined	
14	Undefined	
15	Undefined	
16	Next Diagnostic	Abort the currently executing diagnostic and load and execute the next diagnostic in the sequence.

7.2.3.3 IOC Diagnostic Switch Settings

Each VS-300 IOC board is equipped with a 4-position diagnostic DIP switch which is used in conjunction with the I/O Built-in Test (BIT) Monitor. The switch settings and functions are shown below in figure 7-7.

NOTE

For normal BIT operation, all switch positions should be OFF (left).

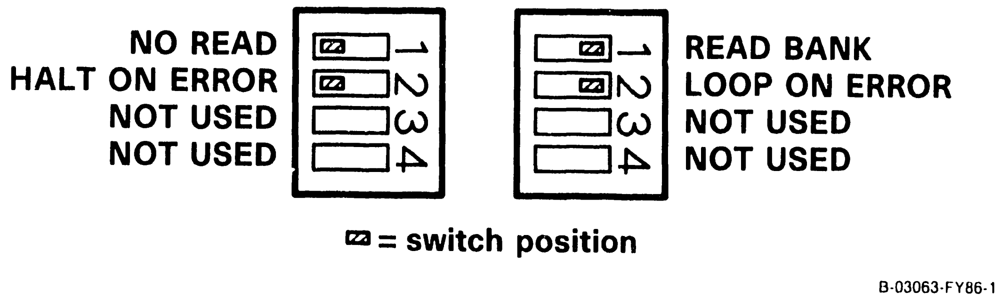

Figure 7-7. VS-300 IOC 4-Position Diagnostic Switch Settings

7.2.3.3.1 Multiline TC IOC Diagnostic Switch Settings

The Multiline Telecommunications (MLTC) board contains an 8-position switch (in addition to the 4-position diagnostic switch) which is used in conjunction with the BIT. All positions of the 8-position switch must be closed (ON) to execute normal BIT routines. Refer to figure 7-8.

Two modes of operation for the Multiline BIT are selectable via the 8-position switch: Single Channel Mode and Burn In Mode.

Single Channel Mode allows the testing of one channel at a time. This mode requires that the correct loopback connector plug be installed on the channel being tested: RS-232 Loopback Connector - WLI P/N 421-0025, RS-366 (ACU) Loopback Connector - WLI P/N 420-1104, or X.21 Loopback Connector - WLI P/N 421-0010.

Burn-In Mode repeatedly executes the BIT tests until an error is encountered or the BIT is terminated by the user. To select Burn-In Mode, open switch position 8 and close all other switch positions. This mode requires 16 channels (any type) with loopback plugs installed in each channel.

7.2.3.3.2 Gate Array TC Controller Loopback Test Switch Settings

CAUTION

Do NOT run the X.21 loopback test with the RS-449 loopback connector in place. Do NOT run the RS-449 loopback test with the X.21 loopback connector in place. Failure to observe this caution will result in destruction of the board.

```
| 8     7     6     5     4        3        2        1       |
  |     |     |     |     |        |        |        |
  |     |     |     |     Closed   Closed   Closed   Closed - Select Port 0  (If 5 Open)
  |     |     |     |     Closed   Closed   Closed   Open   - Select Port 1       "
  |     |     |     |     Closed   Closed   Open     Closed - Select Port 2       "
  |     |     |     |     Closed   Closed   Open     Open   - Select Port 3       "
  |     |     |     |     Closed   Open     Closed   Closed - Select Port 4       "
  |     |     |     |     Closed   Open     Closed   Open   - Select Port 5       "
  |     |     |     |     Closed   Open     Open     Closed - Select Port 6       "
  |     |     |     |     Closed   Open     Open     Open   - Select Port 7       "
  |     |     |     |     Open     Closed   Closed   Closed - Select Port 8       "
  |     |     |     |     Open     Closed   Closed   Open   - Select Port 9       "
  |     |     |     |     Open     Closed   Open     Closed - Select Port 10      "
  |     |     |     |     Open     Closed   Open     Open   - Select Port 11      "
  |     |     |     |     Open     Open     Closed   Closed - Select Port 12      "
  |     |     |     |     Open     Open     Closed   Open   - Select Port 13      "
  |     |     |     |     Open     Open     Open     Closed - Select Port 14      "
  |     |     |     |     Open     Open     Open     Open   - Select Port 15      "
  |     |     |     |
  |     |     |     Closed ------------------------------ Deselects single
  |     |     |     |                                     channel mode
  |     |     |     Open  ------------------------------- Selects single chan. mode
  |     |     |                                           (pos. 1-4 select chan.)
  |     |     |
  |     ------------------------------------------------- Not used
  |
Closed ---------------------------------------------------- Deselects burn-in
Open  ----------------------------------------------------- Selects burn-in
```

Figure 7-8. Multiline TC IOC 8-Position Diagnostic Switch

SW1, an 8-position DIP switch on the Gate Array Telecommunications (GATC) controller, is used to enable loopback testing and to select the interface(s) to be used for loopback testing. Refer to table 7-1a for appropriate switch settings.

Table 7-1a. GATC Loopback Diagnostic Switch Settings

SWITCH POSITION								FUNCTION
1	2	3	4	5	6	7	8	
1*	0	0	0	1	1	0	1	RS-232-C external loopback
0	1	0	0	1	1	0	1	RS-232-C/RS-366 external loopback
0	0	1	0	1	1	0	1	RS-449 external loopback
1	1	1	0	1	1	0	1	RS-232-C/RS-366/RS-449 external loopback
0	0	1	0	1	1	1	1	X.21 external loopback
1	1	1	0	1	1	1	1	RS-232-C/RS-366/X.21 external loopback

*1 = switch closed; 0 = switch open

NOTE

1. If loopback test is selected (switch 8 in "1" closed position), ensure that appropriate loopback connectors are installed.

2. When performing external RS-232-C loopback test, shunt P1 on the 210-8712 board (R1) must be in the NULL/LOOPBACK position. If it is not, the test will fail. For R0 boards, the CLKO pin must be reconnected with a short jumper wire. Refer to schematics.

Use only the following loopback connectors for the GATC:

- RS-232-C (WLI P/N 420-1041)
- RS-232-C/RS-366 (WLI P/N 420-1041)
- RS-449 (WLI P/N 270-3193)
- X.21 (WLI P/N 421-0010)

NOTE

An option for external loopback testing on power up can be exercised provided that SW1 switch settings are correct and loopback connectors are installed prior to power up or system reset.

7.2.3.3.3 CIU BLANC IOC Switch Settings

CAUTION

Do NOT run the external loopback test with live WangNet cables connected to the modem. The test will cause the WangNet contention fields to drop out of synchronization. To run the test, connect either a 40 db loopback test pad, consisting of two 20 db pads (WLI P/N 336-2002) and one 1-ft cable (WLI P/N 220-0314), or a cable simulator (WLI P/N 190-0744) to the transmit and receive connectors of the modem.

For normal power-up BIT switch settings, refer to chapter 5. For external loopback testing, use the switch settings shown in figure 7-8a.

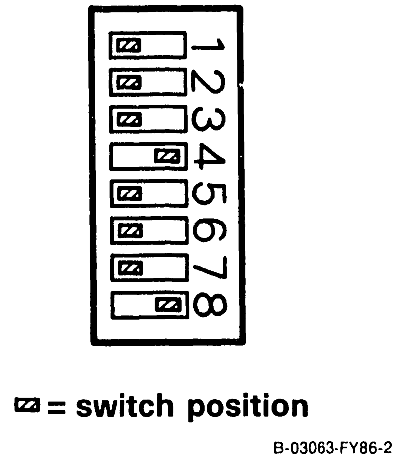

Figure 7-8a. CIU BLANC IOC External Loopback Test Switch Settings

7.2.4 OFF-LINE DIAGNOSTICS ERROR MANAGEMENT

When an error occurs while the off-line diagnostics are running, the DCS displays the following additional information on the diagnostic screen:

- Error Code - a six-character code (3 bytes) consisting of the diagnostic number, the test number, and the error code.
- Failing Unit - the three most likely defective field-replaceable units (FRUs), listed in descending order of probability.
- Detailed Error Message

In addition, the DCS log will be updated and the error count will be incremented (unless DCS is looping on error). If Stop on Error is selected, the DCS will stop and wait until PF key 6 (continue) is pressed. When the DCS continues, it will check to see if Loop on Error is selected. If so, the error loop count will be adjusted and control returned to the diagnostic indicating loop on error. The appropriate status messages will be displayed by the DCS.

7.2.4.1 Intermittent Error Looping

When a diagnostic comes to the end of a test, the DCS will check to see if the diagnostic was looping on error (an error occurred and Loop on Error is set). If so, this indicates that the error did not occur again. The DCS will then initiate the Loop on Test function, display an Intermittent Loop status, and indicate to the diagnostic to loop on test. When looping on an intermittent error, the test loop count and the error loop count will be affected.

7.2.4.2 I/O BIT Monitor Errors

I/O BIT Monitor Diagnostic errors are indicated on the diagnostic screen by an error code and the word "fail" next to the IOC slot number. An error code which may be encountered from time to time is FFFF. This code indicates that the IOC did not respond.

When the I/O BIT Monitor does not recognize an IOC, N/A (not available) will be displayed on the I/O BIT Monitor Diagnostic screen next to the I/O slot number. If an IOC board is physically present in a slot and N/A is displayed next to its slot number, the 8086 (or associated circuitry) on the board is bad and the IOC must be replaced. Some IOC failures put garbage on the I/O bus thus causing other IOCs to fail the BIT diagnostic. The bad IOC in this case will have "N/A" next to its slot number.

7.2.4.2.1 MLTC IOC Loopback Test Error Codes

The following table explains error codes XX51 thru XX55, which may be encountered during the IOC loopback test. The first two digits of the error code identify the interface port number and half-panel. The table uses error code XX52 (failure in RS-232 tests) as an example.

Table 7-1b. MLTC IOC Loopback Test Error Codes

ERROR CODE	PORT NUMBER	HALF-PANEL NUMBER
0152	0	1
0252	1	1
0352	2	1
0452	3	1
0552	0	2
0652	1	2
0752	2	2
0852	3	2
0952	0	3
1052	1	3
1152	2	3
1252	3	3
1352	0	4
1452	1	4
1552	2	4
1652	3	4

7.2.4.2.2 GATC Front Panel LED BIT Error Display

NOTE

If switch 8 of SW1 is ON (closed), the loop on program function is enabled, allowing for continuous looping through all of the tests in the diagnostic PROM. Run time is approximately 30 seconds. Successful completion of each loop is indicated by LED 7 ON and LED 8 flashing. LED 7 will be turnrd OFF after the memory tests have been ccmpleted on each consecutive loop.

The GATC controller assembly contains an eight-LED display that indicates the pass/fail status of the GATC BIT. The following LED display indicates a successful BIT execution:

1	2	3	4	5	6	7	8
OFF	OFF	OFF	OFF	OFF	OFF	ON	FLASHING

If any other combination is displayed, the BIT has failed. When an error occurs, the operating system (OS) cannot access the GATC.

7.2.4.3 DCS Log

The DCS log is used to keep a record of errors that occur while running the diagnostics. Two types of log entry formats are possible. The first format consists of what will automatically be logged at the occurrence of an error, including: the current time, the diagnostic name, test, error code, failing unit, and a condensed copy of what was displayed in the message area. The second format is a picture of the DCS screen at the time the error occurred. This screen will be logged when the PF 7 key is pressed.

7.3 ON-LINE DIAGNOSTICS

In addition to the off-line and stand-alone diagnostics described above, the VS-300 contains several on-line programs that may be executed while the customer is running. These programs are a series of four exercisers that test the following peripherals: workstations, disk drives, tape drives, and printers. The diagnostics, along with a monitor program, are part of a VS on-line test package called "VSTEST" located in library @SYSTST@.

7.3.1 VS ON-LINE VSTEST MONITOR

The VS On-line Monitor is the user interface for VSTEST. The monitor runs under the control of Operating System (OS) Release 6.20 and later releases. With releases prior to Release 7.20.00, however, the monitor cannot be used to do the following:

- Test workstations and printers unless they are first released via the operator's console.
- Test the disk ECC function.
- Do seek tests on disks in shared use.

The monitor allows the user to test in either of two modes:

- Non-interactive - no user intervention is required. Once started, tests run to completion automatically.
- Interactive - user intervention required to control and monitor tests.

The advantage of the non-interactive mode is its ease of use. The advantage of the interactive mode is its list of options; it allows the user to test individual device functions. The non-interactive mode is used to test workstations, disk drives, tape drives, and printers. The interactive mode is used to test only workstations, disk drives, and tape drives. Help screens displayed while the monitor is in a particular mode relate only to that mode.

The VS On-line Monitor provides a series of screens which allows the user to initiate, control, and monitor the testing process. These screens include:

- Main Screen
- Log Program Output Screen
- Device Class Selection Screen
- System Configuration Screens
- Message Screen

7.3.1.1 Main Screen

The Main Screen is displayed whenever the user enters the Monitor. From it the user can go to the Log Program Output Screen, the Device Class Selection Screen, or the Message Screen. These three screens give the user access to any feature offered by the Monitor.

7.3.1.2 Log Program Output Screen

This screen allows the user to select options for logging messages received by the Monitor from VSTEST diagnostic programs during the testing process. From this screen the user can return to the Main Screen.

7.3.1.3 Device Class Selection Screen

This screen allows the user to deal with all devices at a time in one or more device classes. Options include: (1) initiate non-interactive testing, (2) cancel testing, or (3) select the class of devices for which to view the System Configuration Screens. From the Device Class Selection Screen, the user can go to the System Configuration Screens, the Message Screen, or back to the Main Screen.

7.3.1.4 System Configuration Screens

These screens allow the user to deal with one or more devices at a time in a single device class. Options include: (1) initiate non-interactive testing, (2) cancel testing, or (3) initiate interactive testing on one device at a time. From the System Configuration Screens the user can go to the Message Screen or back to the Device Class Selection Screen.

The following messages (table 7-2) may appear in the status columns of the System Configuration Screens. These messages provide information about the device or the test program associated with the device.

Table 7-2. System Configuration Screen Status Messages

STATUS MESSAGE	DEFINITION
AL	Standard ANSI-type labels (tape only).
CNCLNG	The program which has been testing the device is being cancelled.
DT	The device is detached.
ERR004	The volume on which the requested test program file resides is not mounted.
ERR008	The volume on which the requested test program file resides is being used exclusively by another task.
ERR012	The Monitor is unable to initiate the requested test program.
ERR016	The library in which the requested test program file resides cannot be found.
ERR020	The requested test program file cannot be found.
ERR024	Not used.
ERR028	Not used.
ERR032	A disk VTOC error has occurred on the volume on which the test program file resides. FDX1 and FDX2 do not agree.
ERR036	A disk VTOC error has occurred on the volume on which the test program file resides. FDX2 and FDR do not agree.

Table 7-2. System Configuration Screen Status Messages (Cont'd)

STATUS MESSAGE	DEFINITION
ERR040	The name of the file, library, or volume associated with the requested test program has been incorrectly specified.
ERR044	The VTOC for the volume on which the requested program file resides is unreliable.
ERR048	An attempt to scratch a procedure that spawned a test program requested at an earlier time has failed.
ERR052	The requested test program is already in progress.
EX	Exclusive use (tape or disk). The volume may be accessed (read or written to) and dismounted by the mounting user only. This program is not the mounting user.
F	Fixed disk.
IL	Standard IBM-type labels (tape only).
LOADING	The requested test program is being loaded (initiated).
NL	No labels are present on the volume (disk or tape).
NM	Not mounted (disk or tape).
PR	Protected use (disk only). The volume may be read by any user but updated and dismounted by the mounting user only. This program is not the mounting user.
PRTTSK	The device (printer only) is under the control of the system printer task. It can not be determined if the device is idle, waiting for a print file, or printing.
R	Removable disk.
RLSD	The device (workstation or printer) is released from operating system control and may be acquired by any task.
RR	Restricted removal (disk only). The volume may be accessed (read or written to) by any user but dismounted by the mounting user only. This program is not the mounting user.
SH	Shared access (disk and tape). The volume may be accessed (read and written to) and dismounted by any user.
SL	Standard Wang VS labels (disk only).
SYSTEM	The device (printer only) is under the control of an unknown system task.
TESTING	The device is now being tested by a program initiated by this monitor.
TSKMGR	The device (workstation only) is under the control of the system task manager.
WP	The device (printer only) is under the control of the word processor printer task.

7.3.1.5 Message Screen

This screen displays the messages received by the Monitor from the test programs. From this screen the user can return to the last screen viewed.

7.3.2 VS ON-LINE WORKSTATION EXERCISER (WSEX)

The VS On-line Workstation Exerciser (WSEX) is a test program that verifies proper operation of workstations by exercising workstation functions. WSEX tests both the controller and the workstation.

7.3.2.1 Hardware Tested

All devices which have a device class equal to "WORKSTATION" and which support normal WS I/O are supported by this program.

7.3.2.2 Running WSEX

WSEX operates under the control of the VS On-line Monitor, and all user interface is through the Monitor. To run WSEX, select WORKSTATIONS from the On-line Monitor Device Class Selection screen and press RETURN. Position the cursor next to the workstation(s) you wish to test on the System Configuration screen, press PF1 (Select), type a non-blank character, and press RETURN. Normally the test program requires no user interaction other than initiating the tests. However, by pressing the HELP key at the workstation under test, options are made available to terminate testing, continue with automatic testing, or enter the interactive mode which requires user intervention. Refer to figure 7-9.

```
                    WSEX/WORKSTATION EXERCISER INTERRUPTED

PLEASE SELECT ONE OF THE FOLLOWING:

         PF1/INDENT - TO CONTINUE AUTOMATIC DISPLAY TESTS.

         PF4/FORMAT - TO SELECT INTERACTIVE TESTS.

         PF16/GO TO PAGE - TO TERMINATE TESTING OF THIS WORKSTATION.


     THIS WORKSTATION IS CURRENTLY BEING TESTED.  IF YOU WISH TO USE
THIS WORKSTATION NORMALLY THEN PLEASE PRESS THE PF16 OR THE GO TO
PAGE KEY.  IF YOU WANT THE AUTOMATIC TESTING TO RESUME THEN PRESS THE
PF1 OR THE INDENT KEY.  TO TEST THE KEYBOARD AND RUN OTHER NON-AUTO-
MATIC TESTS THEN PRESS PF4 OR THE FORMAT KEY.
```

Figure 7-9. Workstation Interrupted by HELP Screen

The tests are divided into two parts: automatic tests consisting of screen display and functional tests, and interactive tests including keystroke verification and visual attribute displays.

7.3.2.3 WSEX Automatic Tests

1. Screen Display Tests

   a. Even Parity Bit Cell Test - verifies ability of every location of display memory to hold even parity data patterns.

   b. Odd Parity Bit Cell Test - verifies ability of every location of display memory to hold odd parity data patterns.

   c. Row Count Test - verifies that each can hold data different from another row.

   d. Column Count Test - verifies that each column can hold data different from another column.

2. Display Control Tests

   a. Write and Read Tab Stops - verifies that the correct maximum number of tab stops can be programmed and that tab stops are reset correctly when reprogrammed.

   b. Write and Read Field Attribute Characters - verifies that fields, written with various attributes and then read, are set correctly.

   c. Write with Roll Down - verifies the ability of the workstation to correctly roll down rows and to not alter the rows above the roll down row.

   d. Write with Erase Modifiable Field to Pseudoblanks - ensures that modifiable fields can be erased to pseudoblanks by command.

   e. Write with Erase and Protect Rest of Screen - ensures that rows below the designated row are erased and protected by the Erase and Protect command.

   f. Read Altered with Selected Fields - verifies that selected and only selected fields can be read with the Read Altered command.

   g. Read and Read Altered with Blinking Fields - ensures that the link attribute changes to normal when the screen is read.

   h. Read and Read Altered with Pseudoblanks - verifies that when modifiable fields are read, all pseudoblanks within the fields are changed to blanks.

   i. Write Selected - ensures that data, written into selected fields in first and last rows, are changed.

j. Rotating Character Test - verifies that all locations of the display can hold all possible patterns of data.

7.3.2.4 WSEX Interactive Tests

These tests are invoked either by selecting I/A Tests from the On-line Monitor Device Class screen or by pressing the HELP key on the workstation under test and pressing either PF4 or the FORMAT key from the WSEX INTERRUPTED screen. All of the automatic tests are available from the interactive test screen in addition to the three interactive tests described below. The difference is that the user now has the choice of selecting one, several, or all of the automatic tests. Several options are also made available to the user including: loop on test, halt on error, continue on error, pause, etc. The three tests that require user intervention are:

1. Data Entry Into Selected Attribute Test - validates data entry into fields with various attributes. The test verifies that protected fields have not been changed, upper-case only fields contain only upper case, and numeric only fields contain only numbers, "+" and/or ".".

2. Keystroke Verification/Selected Fields Modification Test - verifies the correct recognition of function keys, confirmation of changes to field, and positioning to tab stops.

3. Cursor Positioning Test - ensures that the cursor is correctly positioned under program control.

7.3.2.5 WSEX Error Codes

WSEX error codes (tables 7-3 thru 7-6) are four characters long and are divided into two subfields. The first character defines the subtest that was active at the time the error occurred, the second character defines the error type, and the last two characters are type qualifiers.

```
Error Code                    Definition of Field
  S T Q Q
  | | |_|__________________  Type qualifier characters
  | |______________________  Type or class of error
  |________________________  Active subtest
```

Table 7-3. WSEX Subtest Codes

SUBTEST CODE	TEST NAME	RUN SEQUENCE
A	Write/Read Field Attribute Test	6
B	Write with Erase to Pseudoblanks Test	9
C	Cursor Position Test (I)	18
D	Data Entry into Selected Fields Test (I)	16

Table 7-3. WSEX Subtest Codes (Cont'd)

SUBTEST CODE	TEST NAME	RUN SEQUENCE
E	Even Parity Display Test	1
F	Read Altered with Selected Fields Test	11
G	Read/Read Altered with Blink Test	12
H	Read/Read Altered with Pseudoblank Test	13
I	Column Count Test	4
J	Row Count Test	3
K	Keystroke Verification Test (I)	17
O	Odd Parity Display Test	2
P	Write with Erase and Protect Test	10
R	Rotating Character Test	15
S	Initial Setup Code	
T	Tab Stop Write/Read Test	5
U	Write with Roll Down Test	7
V	Write with Roll Up Test	8
W	Write Selected Test	14

Table 7-4. WSEX Error Type Codes

TYPE CODE	DEFINITION
V	System service (cannot acquire resource or inconsistent)
S	IOSW soft status (corrected error)
T	XIO check timeout error after 10 seconds
H	IOSW hard status (non-corrected error)
F	IOSW fatal status (hard error - cannot continue)
X	XIO return code error
C	Missing XIO check (never received check on XIO)
D	Data miscompare

The following error codes apply to all WSEX tests. Replace the asterisk with one of the subtest codes from table 7-3.

Table 7-5. WSEX Error Codes For All Tests

ERROR CODE	DEFINITION
*D00	Data Miscompare (read after write)
*F00	Fatal IOSW Error (cannot continue)
*H00	Hard IOSW Error
*S00	Soft IOSW Error
*T00	XIO Timed out after 20 seconds
*X??	XIO Return Code Error (??=decimal ret code)

Table 7-6. Additional WSEX Error Codes

ERROR CODE	DEFINITION
CD80	Cursor position test; cursor in wrong position
DD10	Data entry test; lower-case entry in upper case field
DD20	Data entry test; non-numeric entry in numeric field
System-related Error Codes	
SV00	Get heap memory SVC failed
SV01	Get heap memory SVC failed
SV02	Get heap memory SVC failed
SV03	Get heap memory SVC failed
SV04	Get heap memory SVC failed
SV08	Not a workstation at specified address
SV09	Not a supported workstation at specified addres
SV10	Cannot reserve a workstation
SV20	Device address > 255
SV30	Cannot create message port (SYSTEM getheap problem)

7.3.2.6 WSEX Error Messages

WSEX error messages consist of lines of up to six fields. These fields are: unit under test address, program identifier code, error code, program title/function, routine or subtest that was active at the time of failure, and error description. Refer to the sample below in figure 7-10.

```
        UNIT ADDRESS                PROGRAM TITLE
       /    PROGRAM IDENTIFIER    /                  ACTIVE SUBTEST
      /    /     ERROR CODE      /                  /                ERROR DESCRIPTION
     /    /    /                /                  /                /
0065 WSX0 RH00 WSEX/Workstation Test, Rotating Characters, Hard Error
```

Figure 7-10. WSEX Error Message Format

7.3.3 VS ON-LINE DISK EXERCISER (DISKEX)

The VS On-line Disk Exerciser (DISKEX) is a test program that verifies proper disk operation by exercising disk drive functions. DISKEX tests both the controller and the drive.

7.3.3.1 Hardware Tested

All devices which have a device class equal to "DISK" are supported by this program. For a device with a removable volume, DISKEX will attempt to mount a volume on that drive. If no volume is physically present, no testing is done. Only volumes which have a standard label and which allow read/write access to the exerciser are tested. If a device contains both a fixed and a removable volume, each is treated as a separate device.

7.3.3.2 Running DISKEX

DISKEX operates under the control of the VSTEST On-line Monitor, and all user interface is through the Monitor. To run DISKEX, select DISKS from the On-line Monitor Device Class Selection screen and press RETURN. Position the cursor next to the disk(s) you wish to test on the System Configuration screen, press PF1 (Select), type a non-blank character, and press RETURN. No user interaction is required once the tests have been initiated.

NOTE

An extended disk test is performed if the operating system release is 7.10 or higher. For releases below 7.10, testing may be abridged.

7.3.3.3 DISKEX Tests

The following tests are currently supported by the DISKEX program:

1. Seek Max/Min Test - ensures that the OS, microcode, controller, and drive support positioning of the heads on the first and last cylinders of the disk. This test also ensures that seeks to a cylinder which does not exist are detected and inhibited.

   NOTE

   Under the current implementation, this test is performed only if the volume can be remounted Bypass Label Processing.

2. Command Test - verifies data transfer commands by ensuring that the correct block and length was written and read.

3. Cylinder Address Test - performs a butterfly pattern cylinder address test (convergent/divergent) that checks the mechanical positioning hardware, the analog controlling circuits, and the digital seek circuits.

   NOTE

   Under the current implementation, this test is performed only if the volume can be remounted Bypass Label Processing.

4. Random Data Test - consists of three subtests which ensure that all blocks within the file can hold unique data, check the write/verify and read commands, and ensure correctness of randomly written and generated data by reading it and comparing it to the original data.

7.3.3.4 DISKEX Error Codes

DISKEX error codes (tables 7-7 thru 7-13) are four characters long and are divided into two subfields. The first character defines the subtest that was active at the time the error occurred, the second character defines the error type, and the last two characters are type qualifiers.

```
Error Code                          Definition of Field

S T Q Q
| | |_|___________________________ Type qualifier characters
| |_______________________________ Type or class of error
|_________________________________ Active subtest
```

Table 7-7. DISKEX Subtest Codes

SUBTEST CODE	TEST NAME
I	Command Test
D	Data Test
E	ECC Test
M	Seek to Max/Min Test
C	Cylinder Address Test
S	Initial Set Up Code

Table 7-8. DISKEX Error Type Codes

TYPE CODE	DEFINITION
V	System service (cannot acquire resource or inconsistent)
S	IOSW soft status (corrected error)
H	IOSW hard status (non-corrected error)
F	IOSW fatal status (hard error - cannot continue)
X	XIO return code error
Z	XIO return code error (expected code is not 12)
C	Missing XIO check (never received check on XIO)
D	Data transfer incorrect
R	Read VTOC error
M	Volume remount return code error

Table 7-9. DISKEX Cylinder Address Test Error Codes

ERROR CODE	DEFINITION
CC00	XIO complete is missing
CF00	Fatal IOSW error (intervention required)

Table 7-9. DISKEX Cylinder Address Test Error Codes (Cont'd)

ERROR CODE	DEFINITION
CH00	Hard IOSW error
CS00	Soft IOSW error
CX??	XIO return code error (VOL XIO)
CM??	Volume remount error (EXIT vol IO)

Table 7-10. DISKEX Data Test Error Codes

ERROR CODE	DEFINITION
DC00	XIO complete is missing
DD00	Data miscompare (read data which was not written)
DF00	Fatal IOSW error (intervention required)
DH00	Hard IOSW error
DS00	Soft IOSW error
DX??	XIO return code error (FILE XIO)

Table 7-11. DISKEX Command Test Error Codes

ERROR CODE	DEFINITION
IC00	XIO complete is missing
ID00	Data miscompare (read data which was not written)
ID80	Read of 1 BLK modified more than 1 BLK of memory
ID90	Wrote 1 BLK but modified more than 1 file BLK
IF00	Fatal IOSW error (intervention required)
IH00	Hard IOSW error
IS00	Soft IOSW error
IR??	VTOC return code error
IX??	XIO return code error (FILE XIO)

Table 7-12. DISKEX Seek Max/Min Test Error Codes

ERROR CODE	DEFINITION
MC00	XIO complete is missing
MF00	Fatal IOSW error (intervention required)
MH00	Hard IOSW error
MS00	Soft IOSW error
MZ??	XIO return code should be 12, but is not
MX??	XIO return code error (VOL XIO)
MM??	Volume remount error (EXIT vol IO)

Table 7-13. DISKEX System Error Codes

ERROR CODE	DEFINITION
SV00	Get Heap memory SVC failed (buffer 0)
SV01	Get Heap memory SVC failed (buffer 1)
SV02	Get Heap memory SVC failed (buffer 2)
SV08	Not a disk device at specified address
SV20	Device address greater than 255
SV30	Cannot create message port (SYSTEM getheap problem)

7.3.3.5 DISKEX Error Messages

DISKEX error messages consist of lines of up to six fields. These fields are: unit under test address, program identifier code, error code, program title/function, routine or subtest that was active at the time of failure, and error description. Refer to the sample below in figure 7-11.

```
        UNIT ADDRESS                PROGRAM TITLE
      /     PROGRAM IDENTIFIER    /                 ACTIVE SUBTEST
     /    /     ERROR CODE       /                 /             ERROR DESCRIPTION
    /    /    /                 /                 /             /
0065 DKX0 ID00 DISKEX/Disk Exerciser, Command Test, Data Miscompare Error
```

Figure 7-11. DISKEX Error Message Format

7.3.4 VS ON-LINE PRINTER EXERCISER (PREX)

The VS On-line Printer Exerciser (PREX) is a test program that verifies proper printer operation by exercising printer functions. PREX tests all daisy wheel, matrix, band, and chain train printers currently recognizable by the operating system. It also attempts to support experimental printers.

The printer exerciser program requires that at least one printer recognizable to the operating system be attached to the system. The program also requires that the status of the printer to be tested is RELEASED. Beginning with OS Release 7.3 this will be done by PREX. With prior releases, the user can release a printer from either the Command Processor Menu or the Operator's Console Menu.

7.3.4.1 Hardware Tested

The following printers are currently supported by PREX:

2221V	2281V	5533K	5577
2231V2	2281WR	5535	5581WD
2233	2281WCR	5535K	6581W
2233K	5521	5570	6581WC
2235	5521I	5571	DWOS20
2235K	5521IK	5573	DWOS55
2263V1	5521K	5573-1	OK555
2263V2	55312	5574	TPI1
2263V3	55312K	5574-1	XPRTW
2273V1	5533	5575	XPPRT

The following printers are NOT supported by PREX:

LPS12	IP41D	5590

7.3.4.2 Running PREX

PREX operates under the control of the VSTEST On-line Monitor, and all user interface is through the Monitor. To run PREX, select PRINTERS from the On-line Monitor Device Class Selection screen and press RETURN. Position the cursor next to the unit number of the printer you wish to test on the System Configuration screen, press PF1 (Select), type a non-blank character, and press RETURN. No user interaction is required once the tests have been initiated.

The program produces hard copy output on the printer under test. This output should be checked and verified by the CE. The standard format for the output is as follows:

- Three blank lines
- Underscored test name
- Two blank lines
- Test header line(s) describing what will be done
- Test output
- One blank line
- Test trailer line(s) providing information on how to evaluate test output

7.3.4.3 PREX Tests

The VS On-line Printer Exerciser consists of the following tests:

1. HOF (Channel 1) Test - checks the ability of a printer to respond correctly to print control bytes that specify vertical format spacing to head of form.

2. Data Bus Test - checks the output of the serial interface unit and the integrity of the parallel data bus. All bit positions are tested

in both the ON and OFF positions. Compare test output with the bit specifications in the test headers.

3. Character Set Test - prints the entire character set of the printer and the corresponding hexadecimal values (00 thru 7F) of the characters in a four column format with appropriate header lines. Compare the output against the specifications in the appropriate printer user manual.

4. Spiral Pattern Test - prints the entire character set in consecutive print positions on a line. Succeeding lines are printed with each character shifted by one print position to produce a spiral or diagonal effect until all characters are printed in every print position. Inspect the output for alignment, bad print positions, and any other apparent abnormality.

5. Overstrike Test - prints three full lines, each line consisting of a different pair of dissimilar characters in the same print position. This test also verifies the ability of the printer to correctly respond to print control bytes which specify vertical movement of zero lines. Inspect the output for proper registration of the overstruck characters form one end of the line to the other.

6. Carriage Width Test - demonstrates the carriage width of the printer by printing a series of increasing length test records which are less than, equal to, or greater than the actual carriage width. The test pattern consists of repeating groups of the characters "123456789-". Count the complete groups and add the partial groups on the right (if any) to find the actual printable line length.

7. Vertical Format Test - checks the ability of the printer to respond correctly to print control bytes that specify spacing to a vertical tab position (channel 5). Vertical tab positions occur every six lines from top of form.

NOTE

> If the printer being tested is equipped with a Vertical Format Unit (VFU), correct results from this test depend upon having the Wang-supplied Vertical Format Tape mounted (the paper must be properly aligned). The use of any non-standard Vertical Format Tape will produce ambiguous results.

8. Print Quality Test - prints series of full-width "M" and full-height "Z" characters to aid the user in determining if the print quality adjustments are set correctly. The test informs the user about what specific faults to look for in each part of the test.

9. Matrix Pattern Test - prints a pattern consisting of 5 x 5 character blocks on matrix printers. Characters are chosen so that all elements of the dot matrix are activated.

10. Worst Case Pattern Test - prints a series of lines consisting of a character pattern chosen to maximize print wheel rotation on daisy wheel printers.

11. Expanded Print Test - checks the ability of most matrix printers to correctly respond to print control bytes which specify double-width characters.

7.3.4.4 PREX Error Codes

PREX error codes (table 7-14) consist of four characters. The first two characters define the area of the program in which the error occurred:

- IN - error occurred during program startup (initialization).
- OP - error occurred in the routine that sets up the User File Block and opens the printer file.
- XP - error occurred in the routine that performs I/O to the printer.
- RP - error occurred in the routine that builds print records.

The last two characters are sequence designators and have no special significance. The most likely type of errors to occur will be I/O errors, especially error code XP05.

Table 7-14. PREX Error Codes

ERROR CODE	DEFINITION
IN00	The monitor has specified an invalid device address at task creation time. (The text portion of the error message will display the invalid device address as received from the monitor in the parameter passing area.)
IN01	The program is not able to reserve the device to be tested. The UNITRES SVC has failed for some reason. (The text portion of the error message will include the return code.)
IN02	The program is not able to create a port for the receipt of messages from the monitor. The CREATE SVC has failed for some reason other than the specification of a port name which already exists on the system. If a duplicate port name is specified, the program will retry the CREATE with other port names until successful.
IN03	The program is not able to obtain memory space required for a print buffer. The GETHEAP SVC has failed for some reason. (The text portion of the error message will include the return code.)
OP00	The device specified by the monitor for testing is not a printer.
OP01	The User File Block for the printer to be tested indicates that the file is open when it should be closed.

Table 7-14. PREX Error Codes (Cont'd)

ERROR CODE	DEFINITION
OP02	The program is unable to open the file for the printer. The OPEN SVC has failed for some reason. (The text portion of the error message will include the UFB file status bytes which are analyzed for some values in order to provide additional information.)
XP00	The program has determined that the file is not open or the User File Block is bad.
XP01	The data length specified for the call to XIO is negative.
XP02	The data length specified for the call to XIO is greater than 2048 bytes.
XP03	The call to XIO was unsuccessful. The XIO SVC has failed for some reason. (The text portion of the error message will include the return code which is analyzed for some values in order to provide additional information.
XP04	I/O completion did not occur within the time limit.
XP05	Unexpected IOSW bit(s) set. (The IOSW is analyzed bit by bit in order to present additional text information in the message.)
RP00	Attempt to move text string into work buffer was unsuccessful.
RP01	Attempt to build a print record in the print buffer was unsuccessful.

7.3.4.5 PREX Error Messages

PREX error messages consist of lines of up to five fields. These fields are: error code, program identifier code, program title/function, area of the program where the error occurred, and error description. Refer to the sample error message below in figure 7-12.

```
      ERROR CODE                  PROGRAM TITLE
     /    PROGRAM IDENTIFIER /                     PROGRAM AREA
    /    /                  /                     /             ERROR DESCRIPTION
   /    /                  /                     /             /
IN00  PRX0  PREX/Printer Exerciser, Program Startup, Parameter Error
```

Figure 7-12. PREX Error Message Format

7.3.5 VS ON-LINE TAPE EXERCISER (TPEX)

The VS On-line Tape Exerciser (TPEX) is a test program that verifies proper operation of tape drives by exercising tape drive functions. TPEX tests the tape drive, the formatter, and the VS tape Input/Output Controller (IOC).

7.3.5.1 Hardware Tested

TPEX tests all Kennedy and Telex tape drives configured in the VS-300 System.

7.3.5.2 Running TPEX

TPEX operates under the control of the VSTEST On-line Monitor, and all user interface is through the monitor. To run TPEX, select TAPES from the On-line Monitor Device Class Selection screen and press RETURN. Position the cursor next to the unit number of the tape drive you wish to test on the System Configuration screen, press PF1 (Select), type a non-blank character, and press RETURN.

NOTE

To decrease the time it takes to run this program, use a tape reel with 600 feet of tape.

Normally no user interaction is required once the tests have been initiated. However, TPEX may also be run in the interactive mode. In this mode, a Test Selection screen allows the selection of one or more tests.

7.3.5.3 TPEX Tests

1. Basic Command Code Test - performs a comprehensive check of command decode and execution circuitry and a limited check of the data transfer circuitry of the tape unit and IOC.

2. Tape Movement Test - executes all of the tape movement commands to verify that they are working. This test verifies that the tape drive is able to sense the Tape Mark character and position itself anywhere on tape.

3. Variable Data Length Test - writes and reads variable length data patterns (18 bytes to 30K bytes) to ensure that the tape drive can position the tape head and read the data correctly.

4. Tape Creep Test - exercises the ability of the tape to properly position the tape at records. Functions checked include the tape capstan servo circuitry and areas of the mechanical feed path. This test is divided into two subtests:

   - The first subtest checks for record overlap when a number of Backspace/Write commands are issued.

   - The second subtest checks the start/stop timing between records.

5. Random Operations Test - verifies correct operation of the tape subsystem using a series of commands, data, and data length values. Functions tested include Write, Read, spacing commands, random data

values (0 - 65536), and random data count values (0 - 32512).

6. Rewind Test - verifies proper rewind of the tape after End of Tape (EOT) has been sensed.

7. Write at High Density and Read at Low Density - tests the Kennedy dual density tape drive by writing at high density (1600 bpi PE mode for nine track and 800 bpi NRZI for seven track) and reading at low density (800 bpi NRZI for nine track and 556 bpi NRZI for seven track).

8. Write at Low Density and Read at High Density - tests the Kennedy dual density tape drive by writing at low density (800 bpi NRZI for nine track and 556 bpi NRZI for seven track) and reading at high density (1600 bpi PE mode for nine track and 800 bpi NRZI for seven track).

7.3.5.4 TPEX Error Codes

TPEX error codes (tables 7-15 thru 7-22) are four characters long and are divided into the following three categories:

- 0000 - All characters numeric. The first character is the test number, the second character is the routine number, and the third and fourth characters are the number of the error in that routine. Most of the error codes are of this type.

- S000 - Character "S" indicates a Supervisor Call (SVC), the normal interface between user programs and and supervisory routines. The second and third characters indicate the number of the supervisor call and the last character indicates the number of the error in that supervisor call.

- DV00 - "DV" indicates a device error. The last two characters are the error number.

Table 7-15. TPEX Initialization Error Codes

ERROR CODE	DEFINITION
DV00	Device address given by user is beyond range for devices.
S000	Tried to open the tape drive and received an error indication from the Open SVC00.
S280	Device given by the user is not a tape.
S300	Tried to mount the tape drive and received an error indication from the mount SVC30.
S360	Program is unable to find a message port that is not in use.
S361	Create macro tried to create a port but received a getmem error.

Table 7-16. Test 0 Command Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Write, Read, and Rewind Verification	
0000	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0001	Write of 2048 bytes to the tape drive using the data 0000 was attempted but a tape I/O error occurred.
0002	Write of 2048 bytes to the tape drive using the data A95B was attempted but a tape I/O error occurred.
0003	Write of 2048 bytes to the tape drive using the data FF00 was attempted but a tape I/O error occurred.
0004	Rewind to load point and check the load point bit in the Input Output Status Word (IOSW).
0005	Read of 2048 bytes from the tape drive expecting data 0000 was attempted. A tape I/O error or data compare error occurred.
0006	Read of 2048 bytes from the tape drive expecting data A95B was attempted. A tape I/O error or data compare error occurred.
0007	Read of 2048 bytes from the tape drive expecting data FF00 was attempted. A tape I/O error or data compare error occurred.
Subtest 1 - Erase Command Test	
0100	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0101	Write of 2048 bytes to the tape drive using the data 3A3A was attempted. A tape I/O error or data compare error occurred.
0102	Erase Tape Command was issued to attempt to write an erase gap on tape but a tape I/O error occurred.
0103	Write of 2048 bytes to the tape drive using the data FFFF was attempted but a tape I/O error occurred.
0104	Write of 2048 bytes to the tape drive using the data 5B5B was attempted but a tape I/O error occurred.
0105	Erase Tape Command was issued to attempt to write an erase gap on tape but a tape I/O error occurred.

Table 7-16. Test 0 Command Test Error Codes (Cont'd)

ERROR CODE	DEFINITION
0106	Write of 2048 bytes to the tape drive using data C5C5 was attempted but a tape I/O error occurred.
0107	Read of 2048 bytes from the tape drive expecting data 3A3A was attempted. A tape I/O error or data compare error occurred.
0108	Read of 2048 bytes from the tape drive expecting data FFFF was attempted. A tape I/O error or data compare error occurred.
0109	Read of 2048 bytes from the tape drive expecting data 5B5B was attempted. A tape I/O error or data compare error occurred.
010A	Read of 2048 bytes from the tape drive expecting data C5C5 was attempted. A tape I/O error or data compare error occurred.
Subtest 2 - Back Space Block Test	
0200	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0201	Write of 2048 bytes to the tape drive using the data FFFF was attempted but a tape I/O error occurred.
0202	Write of 2048 bytes to the tape drive using the data 0000 was attempted but a tape I/O error occurred.
0203	Write of 2048 bytes to the tape drive using the data A95B was attempted but a tape I/O error occurred.
0204	Back Space Block Command was attempted but a tape I/O error occurred or read of 2048 bytes from the tape drive expecting A95B was attempted and a tape I/O or data compare error occurred.
0205	Back Space Block Command was attempted twice but a tape I/O error occurred or a read of 2048 bytes was attempted twice. The first read expected data 0000 and the second read expected data A95B. A tape I/O error or a data compare error was detected.
0206	Back Space Block Command was attempted three times but a tape I/O error occurred or a read of 2048 bytes was attempted three times. The first read expected data FFFF, the second expected data 0000, and the third expected data A95B. A tape I/O error or a data compare error occurred.

Table 7-16. Test 0 Command Test Error Codes (Cont'd)

ERROR CODE	DEFINITION
Subtest 3 - Forward Space Block Test	
0300	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0301	Read of 2048 bytes from the tape drive expecting data FFFF was attempted. A tape I/O error or a data compare error occurred.
0302	Forward Space Block Command gave a tape I/O error when executed.
0303	Read of 2048 bytes from the tape drive expecting data A95B was attempted. A tape I/O error or data compare error occurred.
Subtest 4 - Write Tape Mark Test	
0400	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0401	Write of three records of 2048 bytes each using the data patterns FF00, 0000, and 5BA9 was attempted but a tape I/O error occurred.
0402	Indicates a rewind and read of two records. A tape I/O error or data compare error occurred.
0403	Write Tape Mark Command was attempted at record three but a tape I/O error occurred.
0404	Tape was rewound to load point and the first two records were read expecting data FF00 and 0000. Third record, written over by the tape mark, was read and the read buffer was checked to see if data was transferred. The command in error is displayed.
Subtest 5 - Forward Space File Command Test	
0500	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0501	Write of 2048 bytes to the tape drive using the data A95B was attempted but a tape I/O error occurred.
0502	Write Tape Mark Command was attempted at record three but a tape I/O error occurred.

Table 7-16. Test 0 Command Test Error Codes (Cont'd)

ERROR CODE	DEFINITION
0503	Write of 2048 bytes to the tape drive using the data 00FF was attempted but a tape I/O error occurred.
0504	Rewind to load point and forward space to file mark was attempted but a tape I/O error occurred or the load point status bit was not as expected.
0505	Read of 2048 bytes from the tape drive expecting data 00FF was attempted. A tape I/O error or data compare error occurred.
Subtest 6 - Back Space File Command Test	
0600	Rewind to load point and check for load point bit in the Input/Output Status Word (IOSW). If bit not set, additional message is displayed.
0600	Rewind to load point and check load point bit in IOSW.
0601	Write of 2048 bytes to the tape drive using data FFFF or Write Tape Mark Command was attempted but a tape I/O error occurred.
0602	Write of 2048 bytes to the tape drive using data 0000 or Write Tape Mark Command was attempted but a tape I/O error occurred.
0603	Write of 2048 bytes to the tape drive using data A9A9 or Write Tape Mark Command was attempted but a tape I/O error occurred.
0604	Tape I/O error occurred after the Back Space File Command was issued or the tape mark bit in the IOSW is not set.
0605	Read Tape Mark and checked to see if Tape Mark bit in IOSW was set. Read record three expecting data A9A9, performed two Back Space Files, and sensed the Tape Mark. Tape Mark status bit not as expected or incorrect length status bit not as expected.
0606	Read Tape Mark and checked to see if Tape Mark bit in the IOSW was set. Read record 2 expecting data 0000. Tape Mark status bit not as expected or incorrect length status bit not as expected.
0607	Back Space File command executed until load point sensed. If load point not sensed, additional error message displayed.

Table 7-17. Test 1 Tape Movement Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Write Two Files for Testing	
1000	Rewind to load point was attempted to start Tape Movement Test and failed because of rewind command error or load point bit in IOSW was not sensed.
1001	Attempted to write a file (File 1), consisting of two 2048 byte records and a Tape Mark, for the Tape Movement Test.
1002	Attempted to write a file (File 2), consisting of two 2048 byte records, a Tape Mark, an Erase gap, two more records, and two Tape Marks.
1003	Attempted to read a 2K block from File 1 and checked to see if data was correct.
1004	Attempted to back space to load point and sense the load point bit in the IOSW but a tape I/O error occurred. If load point bit not set, additional message is displayed.
1005	Attempted to position the tape at the first tape mark by issuing the Forward Space Block Command twice, but a tape I/O error occurred.
1006	Attempted to read a tape mark and checked to see if any data was transferred. Then a Back Space File to Tape mark was executed. A tape I/O error occurred after executing one of these commands.
1007	Attempted to read and check record 2 of File 1 by issuing the Back Space Block Command or the Read Command. A tape I/O error resulted.
1008	Attempted to Forward Space file to the next Tape Mark But a tape I/O error occurred.
1009	Attempted to read and check record 1 of File 1 but a tape I/O error occurred.
100A	Attempted to Forward Space File to the first Tape Mark of File 2 but a tape I/O error occurred.
100B	Attempted to sense a Tape Mark after forward spacing but a tape I/O error occurred.
100C	Attempted to sense a Tape Mark after back spacing but a tape I/O error occurred.
100D	Attempted to place the tape at the first Tape Mark of File 2 by issuing the Back Space File Command but a tape I/O error occurred.

Table 7-17. Test 1 Tape Movement Test Error Codes (Cont'd)

ERROR CODE	DEFINITION
100E	Attempted to read record 1 of File 2 after a Back Space Block and a Forward Space File to position the tape.
100F	Attempted to rewind to load point, write a record, read the record, and sense the Phase Encode (PE) ID Burst on the tape. If the ID Burst is sensed, then the PE bit in the IOSW will be set. (This is only for Telex tape drives.)
1010	Attempted to rewind to load point, write a record, read the record, and sense the Phase Encode (PE) ID Burst on the tape. If the ID Burst is sensed, then the PE bit in the IOSW will be set. (This is only for Kennedy tape drives.)

Table 7-18. Test 2 Variable Data Length Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Write and Read Various Data Lengths	
2000	In an attempt to write and read variable length records, a tape I/O error occurred while executing a Write, Back Space Block, or Read command.
2100	In an attempt to write a 2048 byte record and read it with a data length of 256 bytes, a tape I/O error occurred while executing a Write, Back Space Block, or Read command. If the Illegal Length (IL) bit in the IOSW is not set after the read, an additional message is displayed.

Table 7-19. Test 3 Tape Creep Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Capstan Servo Circuitry Check	
3000 3001 3002	Attempted to write and read records with different data lengths of 2048, 4096, 8192, and 16384 bytes. A tape I/O error occurred while executing a Write, Back Space Block, or a Read command.
Subtest 1 - Mechanical Feed Path Check	
3100 3101	Attempted to write and read records with different data lengths of 2048, 4096, 8192, and 16384 bytes. A tape I/O

Table 7-19. Test 3 Tape Creep Test Error Codes (Cont'd)

ERROR CODE	DEFINITION
3102	error occurred while executing a Write, Back Space Block, or a Read command.

Table 7-20. Test 4 Random Operations Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Random Writes and Reads	
4000 4001 4002	Attempted to write and read records of random data lengths and random data until end of tape was sensed. A tape I/O error occurred while executing a Write, Back Space Block, or Read command.

Table 7-21. Test 5 Rewind Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Timed Rewind from End of Tape	
5000	Attempted to rewind the tape from end of tape to beginning of tape and checked to ensure that the time to do it did not exceed seven minutes. A tape I/O error occurred while executing the Rewind Command. If the rewind to load point exceeds seven minutes, an additional message is displayed.

Table 7-22. Test 6 Density Check Test Error Codes

ERROR CODE	DEFINITION
Subtest 0 - Write at High Density and Read at Low Density	
6000 6001 6002	Attempted to write a 2048 byte record in high density and read it at low density. A tape I/O error occurred while executing the Write, Back Space Block, or Read Command.
Subtest 1 - Write at Low Density and Read at High Density	
6100 6101 6102	Attempted to write a 2048 byte record in low density and read it at high density. A tape I/O error occurred while executing the Write, Back Space Block, or Read Command.

7.4 MEMORY DUMP PROCEDURES

In the VS-300, there are three procedures for completing memory dumps:

- Control Mode Dump
- Continuable Dump
- Snapshot Dump

7.4.1 CONTROL MODE DUMP

Control Mode is a central processor state in which normal program execution is suspended and certain other facilities (mainly diagnostic and initialization) are made available to the user. The system automatically enters Control Mode when problems are encountered that prevent it from proceeding with normal operations. These problems may be either hardware or software related. The user may also force the system into Control mode. Once in Control mode, the VS-300 uses the SCU (as Workstation 0) to communicate with the user. While in Control Mode, the user may initiate a Control Mode dump. After completing the Control Mode dump, the user must reIPL the system.

The Control mode dump program copies the entire contents of main memory to another storage medium to capture the state of the system when a problem occurred. The VS-300 can use magnetic tape (except cartridge tape, 25V29), floppy diskettes, or disks for the storage medium. An analyst will use this dump information to determine the cause of the system problem.

There are two conditions under which a Control mode dump should be taken:

- The machine has experienced a fatal error and a message de- scribing that error is displayed on Workstation 0.

- The system appears to be hung, to be looping, a task has been abnormally terminated, a dedicated system task is can- celled, or a situation has occurred where the system manager or Wang customer engineer determines a dump is necessary.

NOTE

All required workstation operations must be performed from Workstation 0.

7.4.1.1 Errors Requiring Control Mode Dump

Table 7-36 below lists the IPL errors that require a Control Mode dump be performed. The table lists the program Control Words (PCWs) displayed on Workstation 0 as well as an explanation of each. If any one of these errors occurs, follow the Control Mode dump procedure in paragraph 7.4.1.2.

Table 7-23. IPL Errors Requiring Control Mode Dump

PCW DISPLAY	ERROR MESSAGE
IPL ERRORS	
00000001 FFFFFF**	NOT ENOUGH MEMORY FOR IPL
00000002 FFFFFF**	IPL I/O ERROR
00000003 FFFFFF**	NO SYSTEM FILE ON VOLUME
00000004 FFFFFF**	BAD VTOC ON IPL VOLUME
00000005 FFFFFF**	O/S CODE SPANS 3 EXTENTS
RESIDENT SYSTEM INITIALIZATION ERRORS	
00000011 FFFFFF**	SYSINIT I/O ERROR--OPERATING SYSTEM CANNOT BE READ
00000012 FFFFFF**	NOT ENOUGH MEMORY FOR RESIDENT SYSTEM
00000013 FFFFFF**	SYSINIT PROGRAM CHECK
00000014 FFFFFF**	IPL DEVICE NOT INCLUDED IN SYSGEN
00000015 FFFFFF**	MICROCODE VERSION TOO LOW
MACHINE CHECK ERROR MESSAGES	
00000021 FFFFFF**	MAIN MEMORY PARITY ERROR
00000022 FFFFFF**	I/O PROCESSOR MALFUNCTION DEVICE XXX
00000023 FFFFFF**	I/O PROCESSOR TIME OUT
NON-RESIDENT SYSINIT ERRORS	
00000031 FFFFFF**	OPERATING SYSTEM FILE (@SYSSVC@) NOT FOUND
00000032 FFFFFF**	PAGING FILE FOR TASK 0 CANNOT BE CREATED/SCRATCHED
00000033 FFFFFF**	LINK TO SYSGEN MODULE FAILED
00000041 FFFFFF**	INVALID VERSION NUMBER FOR @SYSSVC@
MISCELLANEOUS	
FFFFFFFF FFFFFF**	WRONG MACHINE (VS-100 OS ON VS-300 OR VICE VERSA)

NOTE: ** = undefined last two bits in PCW.

NOTE

For a list of Operating System errors that require a Control mode dump, refer to Appendix A. If one of these errors occurs, follow the procedure in paragraph 7.4.1.2.

The following machine check error codes are defined for the VS-300:

Table 7-24. VS-300 Machine Check Error Codes

HEX CODE	REASON
01	Main memory multiple bit ECC error.
0F	Default trap taken.
10	AGU error received. Invalid state in instruction queue.
20	I/O interrupt line received with no active IOSW in the I/O processor status table.
21	Power fail interrupt received.
22	Spare control exception trap taken.
81	Translation buffer parity error.
82	Illegal state - external cache probe.
84	Illegal state - internal cache probe
90	System bus parity error.

The following conditions result in the micromachine hanging (branch to self):

- Control store parity error (IC = FE1)
- Single step microinstruction trap (IC = FE2)
- Microinstruction address compare trap (IC = FE3Z)

7.4.1.2 Control Mode Dump Procedure

Throughout this procedure the following rules apply:

- Zeroes must be entered where indicated.
- When entering information defined in the procedure, begin at the current cursor position. Do not reposition the cursor.
- The asterisk (*) represents the value of a position and must not be changed during the process of preparing the dump.
- In any place in these procedures where an instruction says "enter 0000****0000", enter the zeroes and skip over the asterisks by using the cursor control keys.

Any data on the disk or tape will be written over by the dump program, so ensure that data stored on the dump medium are no longer needed. If the system has been configured with an optional dump file by using the DISKINIT program, the dump may be placed onto a disk volume as a file. Use the dump file if possible. If the dump is to be written to a preallocated dump file there is no need to be concerned about the other data stored on the medium. They will not be overwritten. However, data stored by a previous dump in a pre-allocated dump file will be overwritten. As a standard procedure after performing the dump, copy the data from the preallocated dump file to another area on disk or to another magnetic tape and then run the PATCH utility on the preallocated dump file.

When the system experiences a fatal error and enters Control mode, the screen freezes and the keyboard locks. The message "<<<Machine Check>>>" appears on the top line of the SCU screen.

NOTE

On W/S 0, a Control Mode dump procedure will be displayed below the "<<<Machine Check>>>" message. Ignore this procedure; it is not correct for the VS-300.

1. When the 4-letter error code appears at the top of the screen, write it down. Refer to Appendix A for an explanation of the error code. From the SCU, press CONTROL, then press SHIFT and CANCEL simultaneously to exit workstation emulation. The Workstation Emulation menu appears. Press the SPACE BAR to select "Suspend Emulation." Press EXEC and the VS-300 Console Processor menu appears. Refer to figure 7-13.

```
                    *** WANG VS300 CONSOLE PROCESSOR ***

SYSCON Version 1.3.0                11:06 AM          Monday  August 5, 1985


          Press (HELP) for on-line system console information.


                  Use the function keys to select command:

(1) ENTER Workstation Emulation            (8) RESET System
(2) ENTER Control Mode                     (9) RESET Console
(3) ENTER Service Log Mode
(4) ENTER Off-line Diagnostics             (10) SHOW System Elements Status
                                           (11) SET Time and Date
(5) AUTO IPL                               (12) SET Console Defaults
```

Figure 7-13. Console Processor Menu

2. From the VS-300 Console Processor menu, press PF key 2 to select "ENTER Control Mode." The VS Enhanced Control Mode screen appears. Refer to figure 7-14.

```
                          VS Enhanced Control Mode
                             Release 1.03.00
<Enter Command>
:

PCW: 00000000 00000000    R0:   00000000 00000000  CR0:   00000000 00000000
                          R2:   00000000 00000000  CR2:   00000000 00000000
@PC: 00000000 00000000    R4:   00000000 00000000  CR4:   00000000 00000000
                          R6:   00000000 00000000  CR6:   00000000 00000000
                          R8:   00000000 00000000  CR8:   00000000 00000000
                          R10:  00000000 00000000  CR10:  00000000 00000000
                          R12:  00000000 00000000  CR12:  00000000 00000000
                          R14:  00000000 00000000  CR14:  00000000 00000000

                    Physical Memory Display  Phys. addr = 00000000

00000000:  00000000 00000000 00000000 00000000          |................|
00000010:  00000000 00000000 00000000 00000000          |................|
00000020:  00000000 00000000 00000000 00000000          |................|
00000030:  00000000 00000000 00000000 00000000          |................|
00000040:  00000000 00000000 00000000 00000000          |................|
00000050:  00000000 00000000 00000000 00000000          |................|
00000060:  00000000 00000000 00000000 00000000          |................|
00000070:  00000000 00000000 00000000 00000000          |................|
```

Figure 7-14. VS Control Mode Screen

The cursor is on the command line, which is the colon below the message "<Enter Command>".

Enter M and press RETURN. Use the cursor control keys to move the cursor to the first digit of the second block of numbers that are directly next to the PCW prompt. For example, if the PCW number is 0000AAAA 40030000, move the cursor to the "4". Enter 0 (zero) and press RETURN.

The cursor automatically returns to the command line. Enter X and press RETURN.

3. When the VS-300 Console Processor menu appears, press PF 1 to select "ENTER Workstation Emulation." Press EXEC.

4. The message "DUMP TO PREALLOCATED FILE? YES/NO" appears on the screen. If a disk dump file, preallocated by the DISKINIT utility, is available and ready, enter YES. Otherwise, enter NO and go to Step 6.

NOTE

Ensure that the dump disk contains a dump file, that the dump file is large enough to hold the memory contents of the system, and that the disk is ready.

5. If you responded YES to Step 4, this message appears: "PLEASE ENTER DISK LABEL". Enter the label of the disk with the preallocated dump file. If the label is good, the disk is ready, and the file is large enough, the program proceeds to Step 8.

6. If you responded NO to the question in Step 4, the SCU displays a screen similar to the one shown in Figure 7-15.

```
At this point, it is necessary to indicate the output device address
for the dump program.

Use the default address or enter another one:  2C01

Press the ENTER key.
```

Figure 7-15. Control Mode Dump Device Address Screen

Press RETURN to use the default dump address or change the Physical Device Address (PDA) and press RETURN. The VS-300 has a default dump device set at IPL which is the lowest numbered tape. Calculate a new PDA as follows:

a. Determine the IOC and write down the first six bits from the IOC list below.

IOC	Binary Representation
IOC 1	0010 00
IOC 2	0010 01
IOC 3	0010 10
IOC 4	0010 11
IOC 5	0011 00
IOC 6	0011 01
IOC 7	0011 10

b. Determine the device number and write down the last ten bits. Convert the binary number to a four-digit hexadecimal number. The result is the PDA. Refer to the example below.

If the IOC used is IOC 2 (binary 0010 01) and the device number is 1 (binary 00 0000 0001), the PDA is determined as follows:

	IOC Number (high 6 bits)		Device Number (low 10 bits)	
Binary	0 0 1 0	0 1 0 0	0 0 0 0	0 0 0 1
Hexadecimal	2	4	0	1

The Physical Device Address = 2401.

7. The program displays the following message: "PLEASE MOUNT DUMP MEDIA". Physically mount the requested media.

8. The Dump program begins execution when it detects that the device is ready. The Dump program displays a blinking message: "DUMP IN PROGRESS".

9. The Dump program continues to execute. It may stop for one of three reasons:

   a. The dump has successfully completed. This is indicated by the message: "DUMP COMPLETE -- PLEASE PRINT I/O ERROR LOG AFTER IPL". Dismount the dump volume and proceed to Step 10.

   b. An I/O error has occurred. This is indicated by the display: "I/O ERROR DUMP NOT POSSIBLE TO COMPLETE". The dump cannot continue, but a partial dump has been completed. Dismount the dump volume and proceed to Step 10. If the dump device is tape and it is write protected, you must return to Step 1.

   c. The mounted volume is full. Another dump volume is required. This is indicated by the display: "PLEASE MOUNT ADDITIONAL DUMP MEDIA". Dismount the full volume and proceed to Step 7 to mount another volume.

10. ReIPL the system, and print the I/O Error Log.

11. Run the LISTVTOC utility to verify the VTOCs of all disk volumes that were on-line at the time of the system failure. Do not verify the dump disks.

12. If you used a preallocated dump file, run the PATCH utility on that file. The PATCH utility frees the dump file to be automatically overwritten at the time of the next dump. To run the PATCH utility, follow these steps:

    a. From the VS Command Processor, press PF1, Run Program or Procedure. Specify PATCH in the PROGRAM field and press ENTER.

    b. On the first PATCH utility screen, enter the dump file filename, library, and volume. For the preallocated dump file, the filename is @CMDUMP@ and the library is @SYSDUMP. For the OPTION field, enter VERIFY. For the ADDRESS field, enter 0. Press ENTER.

    c. The data parameter field on the screen shows the hexadecimal code for the first 16 bytes of the file. Change the first eight digits to 0. For the OPTION field, enter REPLACE. Press ENTER.

    d. To exit from PATCH, enter QUIT at the OPTION field.

13. Call the local Wang software analyst and send the following information:

    - The dump in machine-readable form.
    - A task dump, if one was generated.
    - The error code you wrote down in Step 1.
    - A Software Problem Report Form (800-5104).
    - The I/O Error Log.
    - An explanation of what was happening at the time the system malfunctioned and the present status of hardware and software. If the dump was a partial one, indicate that on the dump report.

7.4.1.3 Forcing the System Into Control Mode for Dump

If the system appears to be hung or a Control mode dump is required for some other reason, the system may be forced into Control mode by using the following procedure:

1. Exit workstation emulation. Press CONTROL, then press SHIFT and CANCEL simultaneously. From the Workstation Emulation menu, press the space bar to select Suspend Emulation and press EXEC. From the VS-300 Console Processor menu, press PF key 2 (ENTER Control Mode). The Enhanced Control Mode screen appears.

2. Record the displayed PCW for future reference.

3. Enter M 00000700 00000000 on the PCW line, and press RETURN. The starting address of the dump program is 0700.

4. Type X and press RETURN to exit from Control Mode and begin execution of the dump program. To return to workstation emulation, select Workstation Emulation from the Console Mode menu and press EXEC.

5. Follow instructions in paragraph 7.4.1.2 from Step 3.

7.4.1.4 Control Mode Dump Stops

If the system encounters a problem at some point in the Control Mode dump program, a Control Mode stop will occur. The system notifies the user by displaying the PCW in one of the following formats:

- ******** SSSS**** where ** is valid PCW information and SSSS is a code that indicates the dump program status.

- ****AAAA SSSS**** where ** and SSSS have the same meaning as above. AAAA is the resume PCW address and a pointer to a storage location. The user must modify this location in order for the dump program to continue.

NOTE

There may be up to a thirty second delay between Control Mode stops.

The status codes are summarized below in table 7-25.

Table 7-25. Control Mode Stops

PCW/STATUS CODE	DESCRIPTION
0000AAAA 40000000	Dump completed successfully.
0000AAAA 40010000	Dump in progress; continue from here.
0000AAAA 40020000	Please mount additional dump media.
0000AAAA 40030000	Please mount dump media.
0000AAAA 40040000	Dump to preallocated file? The options are YES and NO.
0000AAAA 40050000	Please enter disk label.
0000AAAA 40060000	Enter Dump Device PDA.

Table 7-25. Control Mode Stops (Cont'd)

PCW/STATUS CODE	DESCRIPTION
0000AAAA 40070000	Must enter YES or NO only.
0000AAAA 40080000	Volume Name must be alphanumeric.
0000AAAA 400B0000	Disk selected not found or not available.
0000AAAA 400C0000	Disk selected does not have Dump file.
0000AAAA 400D0000	Selected Disk Dump file is too small.
0000AAAA 400F0000	I/O error; dump not possible to complete.

For more detailed information on Control Mode Stops and instructions on how to continue the dump after a stop has occurred, refer to the VS Field Guide WLI P/N 741-1265.

7.4.2 CONTINUABLE AND SNAPSHOT DUMPS

A continuable dump is a type of memory dump that occurs automatically (if enabled) when certain system errors are encountered. The continuable dump provides information similar to that provided by the Control mode dump but in less time. A continuable dump does not cause system operation to halt. Instead, system operation is suspended, the continuable dump is completed, and system operation continues. During most continuable dumps, users notice only a 15-second workstation freeze. Logging off is not necessary and reIPL is not required for most continuable dump errors. For those errors requiring reIPL, an automatic reIPL is performed at the end of the dump and all users must log on again.

The snapshot dump is a continuable dump that the user invokes manually when memory dump information is needed. VS-300 operations are suspended, the dump is completed, and operations are automatically continued.

On the SYSGEN Configuration File screen of the IPL procedure (refer to paragraph 4.9.1), the prompt "Inhibit dumping continuable halts?" allows the user to enable or disable the continuable dump. If you answered NO, all continuable dumps proceed as described below. If you answered YES, continuable halts that do not require reIPL are not run. The error remains and system operations may be affected.

The continuable dump is invoked automatically when the system errors listed in Appendix A occur.

7.4.2.1 Requirements for Continuable and Snapshot Dumps

Both continuable and snapshot dumps require the allocation of a special file for storing the dump information. All continuable and snapshot dump information must be dumped to disk. Run DISKINIT to set up the file @CMDUMP@ in library @SYSDUMP. This file must be available on at least one volume at all times to ensure that the continuable or snapshot dump can be completed. If the default dump file is on a number of available volumes, the dump information is stored in the first default file that the system finds.

7.4.2.2 Invoking the Snapshot Dump

The snapshot dump executes in a similar manner and provides the same information as the continuable dump. The difference between them is that the user invokes the snapshot dump manually.

To invoke the snapshot dump, perform the following procedure:

- From the VS Command Processor, press PF11 to enter Operator's Mode.
- From the Operator's Console menu, press PF14 to enter System Options.
- From the System Options menu, press PF10 to initiate the snapshot dump.

7.4.2.3 Running Continuable and Snapshot Dumps

Under most conditions, the continuable dump and the snapshot dump are completed without user intervention. After they are invoked, either automatically or manually, the screen in figure 7-16 appears on Workstation 0. All other workstations freeze for the duration of the dump.

```
System Halt:  CPNB
Dumping on device:  MGR
```

Figure 7-16. Sample Continuable Dump Screen

When either dump is complete, the message "Dump Completed Successfully" appears on Workstation 0. Press HELP to return to the Operator's Console and the task that was running before the dump. Work can also continue as usual on other users' workstations when the dump is complete, . All dump information is available through the @CMDUMP@ file on library @SYSDUMP. To save the information, run COPY from VS Command Processor PF1, Run Program. Send the dump file information to the local software analyst to report the system error.

To make the @CMDUMP@ file available for the next continuable or snapshot dump, run PATCH. This utility changes the first four bytes of a file to indicate that the file can be overwritten.

To run PATCH, follow these steps:

1. From the VS Command Processor, press PF1, Run Program or Procedure. Specify PATCH in the PROGRAM field and press ENTER.

2. On the first PATCH utility screen, enter the dump file name, library, and volume. If you used the preallocated dump file, the filename is @CMDUMP@ and the library is @SYSDUMP. For the OPTION field, enter VERIFY. For the ADDRESS field, enter 0. Press ENTER.

3. The data parameter field on the screen shows the hexadecimal code for the first 16 bytes of the file. Change the first eight digits to 0. For the OPTION field, enter REPLACE. Press ENTER.

4. To exit from PATCH, enter QUIT at the OPTION field.

If you do not run PATCH on @CMDUMP@, the next continuable or snapshot dump is interrupted. Before it can continue, you have to specify what is to be done with the dump information. Four options appear on the continuable (or snapshot) dump screen:

- Press PF1 -- Ignore the current dump and continue processing.

- Press PF3 -- Overwrite the previous dump information with the current information; the previous information would be lost.

- Press PF16 -- Enter Control mode.

- Specify another device to send the dump information; it must have the @CMDUMP@ file already allocated on library @SYSDUMP.

Once you make a selection, the continuable or snapshot dump proceeds normally. After a continuable dump is completed, send the information to the software analyst. The analyst uses the dump information to determine what caused the error.

7.4.2.4 Continuable Dump and Automatic IPL

There are some system errors that require reIPL after the continuable dump. In those situations, the continuable dump proceeds as described in paragraph 7.4.2.3. At its completion, the dump automatically reIPLs the system.

During an automatic reIPL after a continuable dump, Workstation 0 displays the message "ReIPLing from device XXXXXXX." This message remains on the screen until the Wang VS logon screen appears. Then, the standard information messages appear. The configuration files last specified on the SYSGEN configuration file screen are used and the date and time are automatically updated.

When the operator's console or logon screen appears, the system is ready for use again. All users are required to log on again.

7.5 TROUBLESHOOTING PROCEDURES

This section provides procedures, in flow chart form (figure 7-19), for troubleshooting power problems in the VS-300 Computer System. These flow charts are intended as a guide and not a comprehensive treatment of all possible power troubleshooting techniques. Use figures 7-17 and 7-18 below for ease in locating the various connectors on the power controller board and for cable identification. Heed the warnings that precede two of the steps in the flow charts.

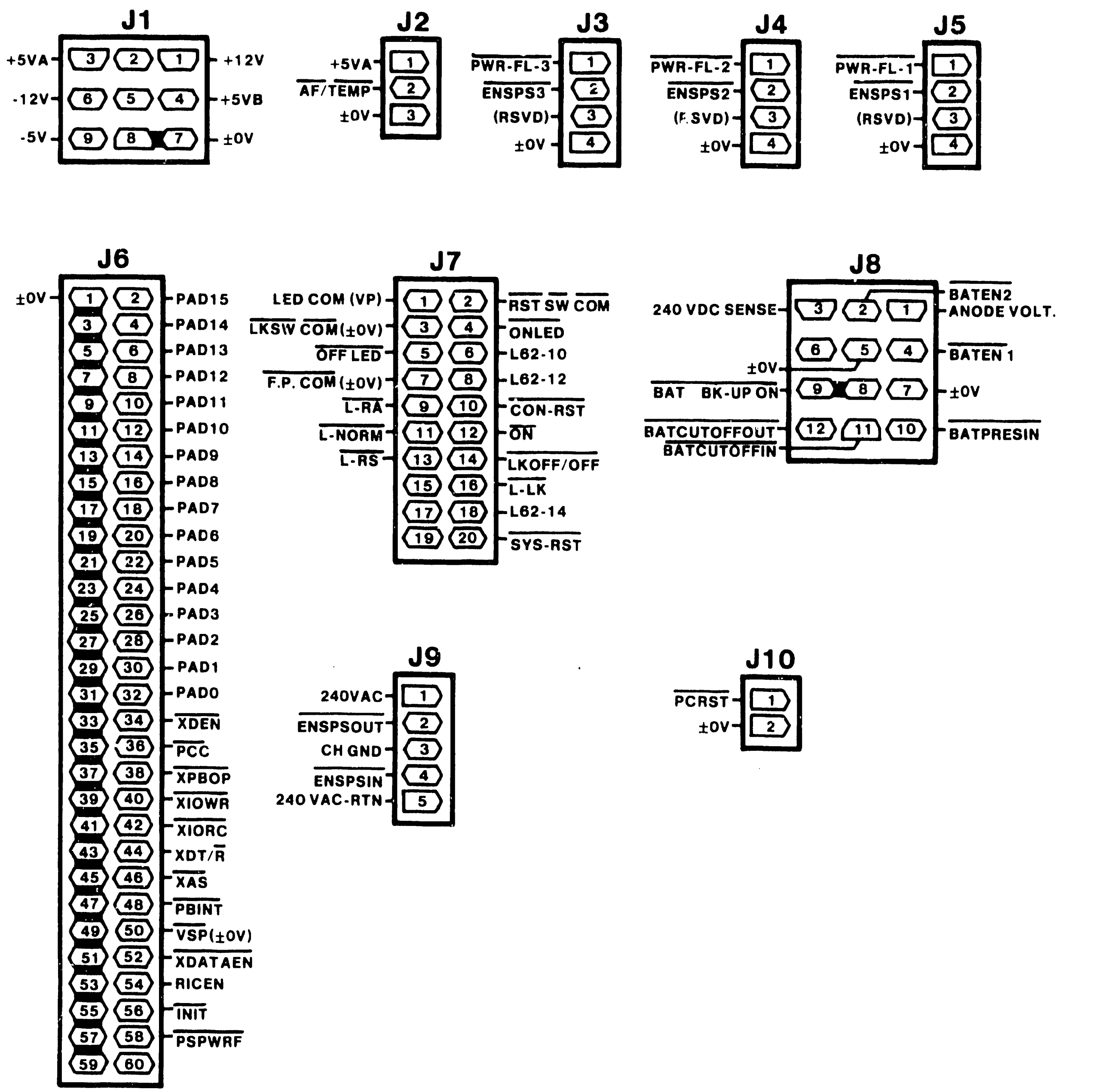

Figure 7-17. VS-300 Power Controller Board Connectors

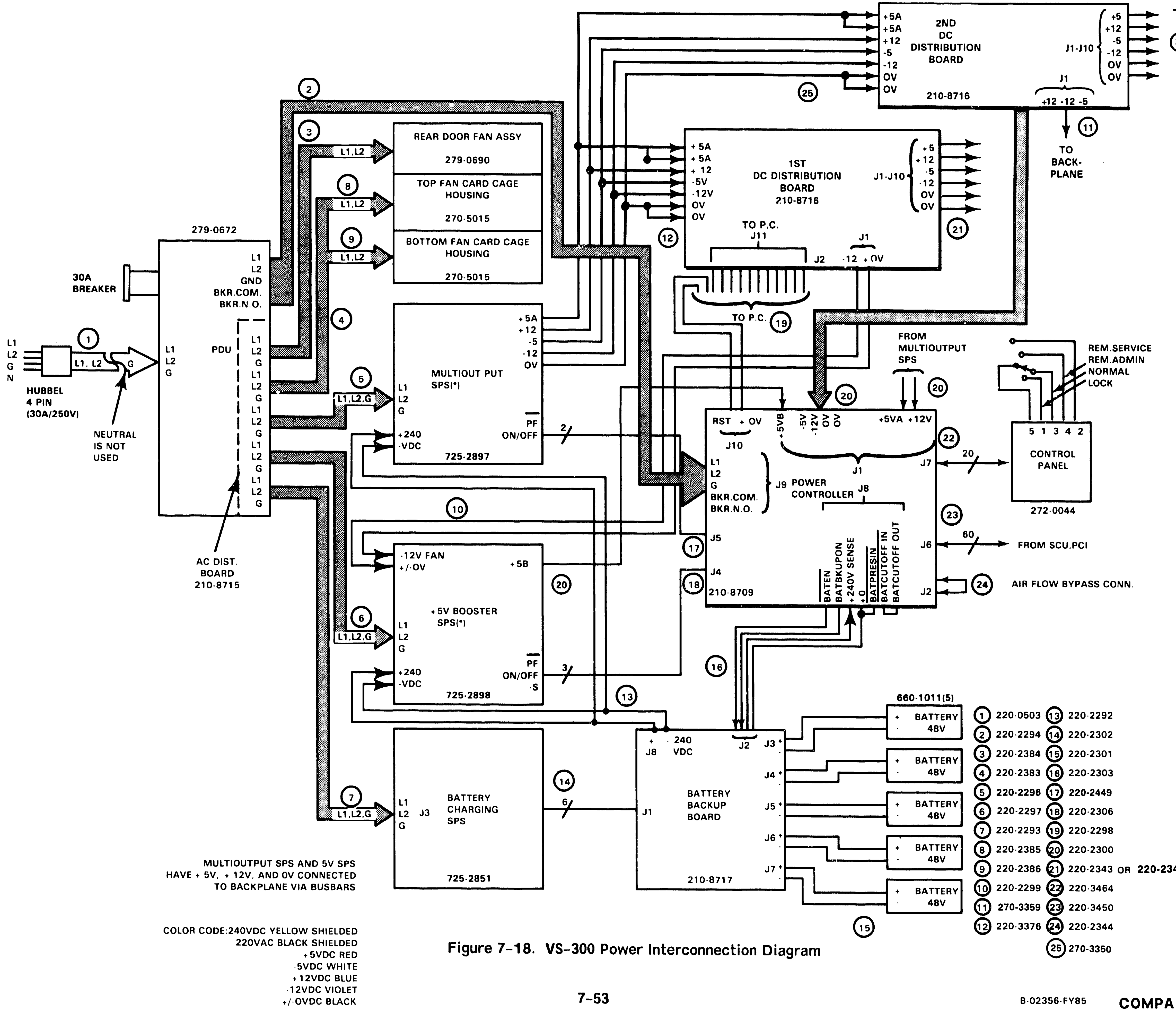

Figure 7-18. VS-300 Power Interconnection Diagram

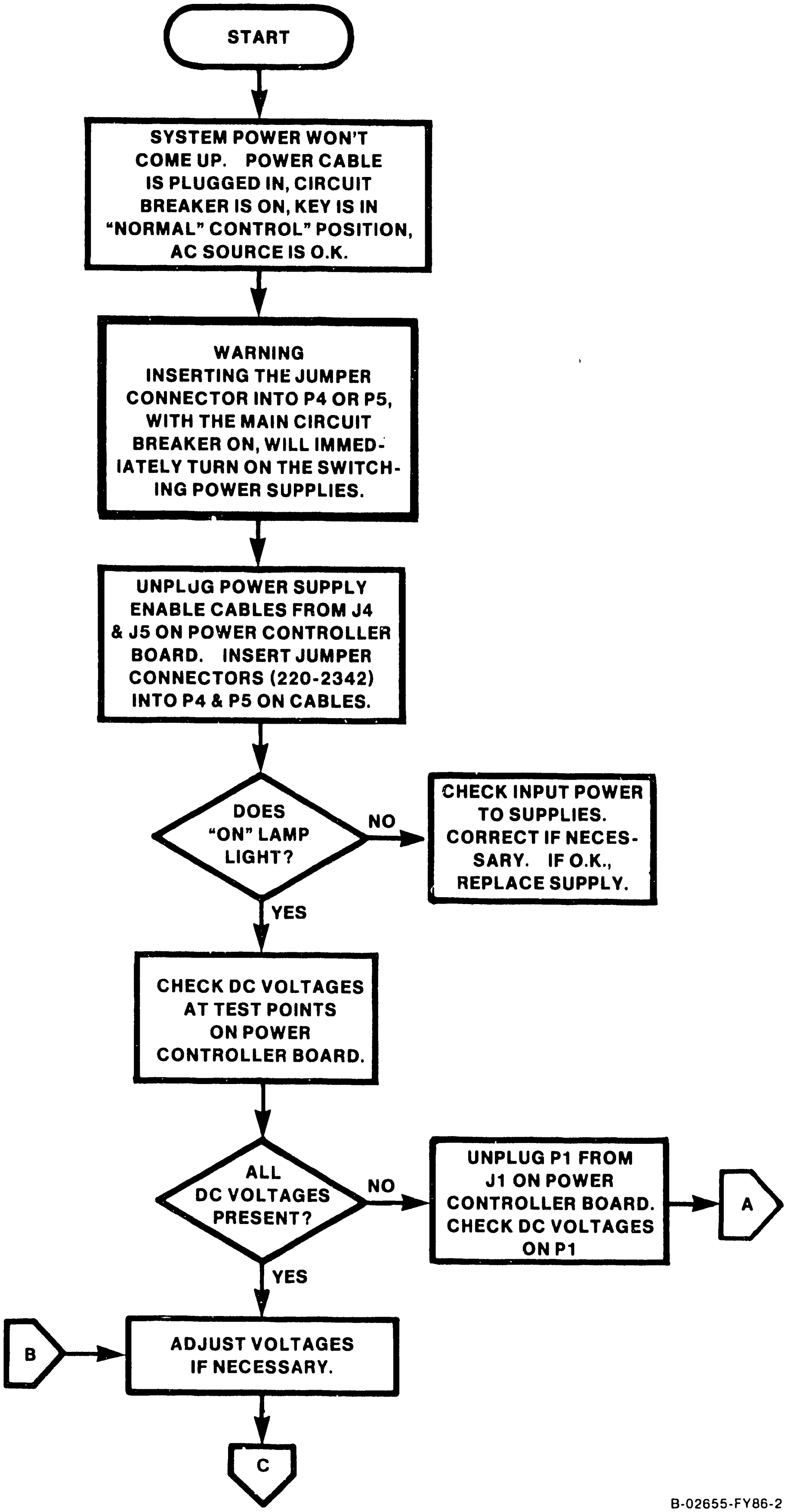

Figure 7-19. Power Troubleshooting Flow Chart (1 of 4)

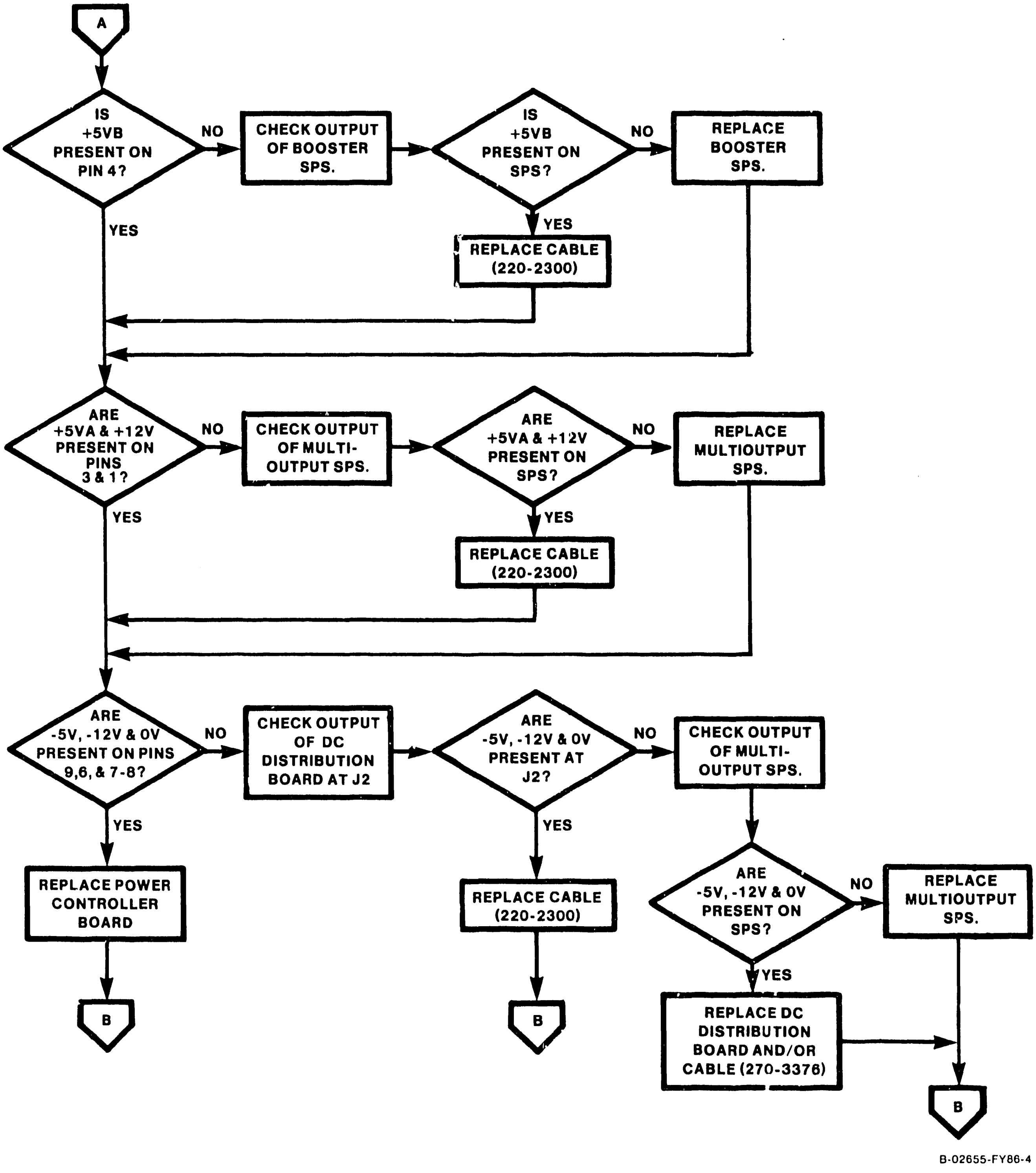

Figure 7-19. Power Troubleshooting Flow Chart (2 of 4)

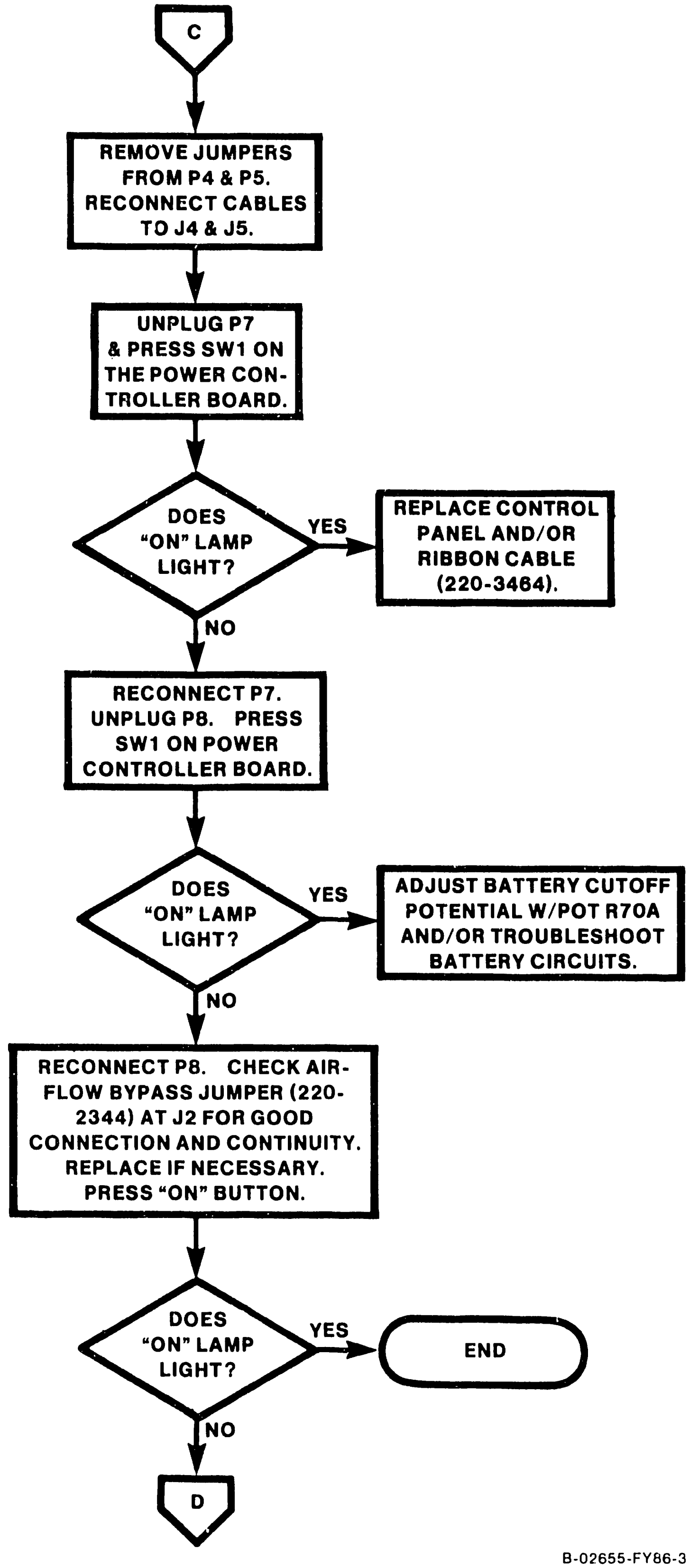

Figure 7-19. Power Troubleshooting Flow Chart (3 of 4)

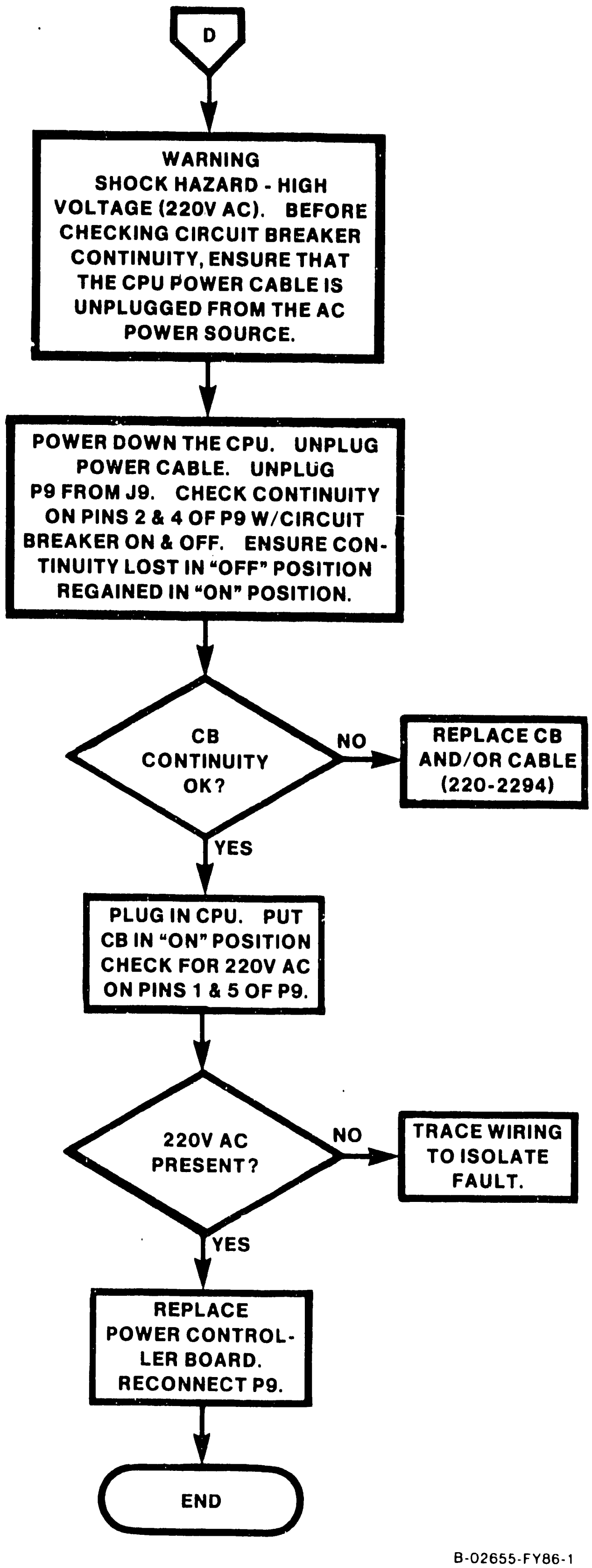

Figure 7-19. Power Troubleshooting Flow Chart (4 of 4)

7.6 ERROR LOG

The error log provides a means of tracking system errors and their frequency in the following areas: main memory (MM), central processor (CP), and power supply (PS). The error log is accessed from the System Console screen in the service mode. To enter the error log, perform the following:

1. Go to the System Console screen.

2. Turn the keyswitch to the "Remote Service" position.

3. Enter the following password:

   CSG + current time (four digits), as displayed on the System Console screen. Example: If time is 9:30 (am or pm), enter 0930.

NOTE

While entering the password, the keyboard beeper will sound as each key is pressed. This is normal. It is intended to discourage unauthorized personnel from enabling the full Sytem Console menu.

4. Several previously undisplayed menu picks will appear. Refer to figure 7-2A above. The System Console is now in the "service mode." (The service mode can be terminated by pressing PF key 10 or turning the keyswitch out of the "Remote Service" position.)

5. Press PF key 11 to access the error log.

   The following screen appears:

```
                    Main Memory Error Log                      Page 1

Memory Operation  Level  Address   Time      Date      Count  Comments

Refresh           03     00000000  00:02:53  01-01-86  01     Multiple Bit

-------------------------------------------------------------------------

  (1) MM error log      (PREV)       Previous entries
  (2) CP error log      (NEXT)       Next entries
  (3) PS error log      (DELETE)     Delete entries
  (4) Set defaults      (16)         Exit
```

Figure 7-20. Error Log Screen

Use the various keys indicated on the screen to access other error logs, set defaults, page through a particular error log, delete entries, or exit screen.

To set error log defaults, press PF key 4. The following screen appears.

```
                         Set Error Log Defaults

Memory Error Rate and Error Counts

MER = X error every XXX hours          MEC = XXX errors
PCR = X check every XXX hours          PEC = XXX errors

Voltage Ranges                                   Interrupt Status

Power Supply        High      Low        Level     Element    Status

     +5VA          +0.000    +0.000        1         CPU      Enabled
     +5VB          +0.000    +0.000        1         MCU      Enabled
     -5V           -0.000    -0.000        1         SBI      Disabled
     +12V         +00.000   +00.000        1         SCU      Enabled
     -12V         -00.000   -00.000        1         PWR      Enabled
                                                     SYSR     Enabled

 (1) MM error log   (9) Modify defaults        (13) Enable/disable SCU
 (2) CP error log  (10) Enable/disable CPU     (14) Enable/disable PWR
 (3) PS error log  (11) Enable/disable MCU     (15) Enable/disable SYSR
 (4) Set defaults  (12) Enable/disable SBI     (16) Exit
```

Figure 7-21. Set Error Log Defaults Screen

This screen displays the count of various types of memory errors, allows entering high and low power supply voltage values, and allows enabling/disabling various system elements.

7.7 SERVICE LOG

The VS-300 provides a facility for documenting the system's hardware configuration, software configuration, and maintenance history. This facility is called the "Service Log." The Service Log contains an easily accessible and modifiable database, which can prove to be a valuable aid in tracking system problems.

7.7.1 ACCESSING THE SERVICE LOG

Because of the nature of the data contained in the Service Log, its access, along with several other System Console menu picks, is password-protected to prevent entry by unauthorized personnel. To enter the Service Log, perform the following:

1. Perform steps 1 thru 4 in paragraph 7.6.

2. Press PF key 3 to bring up the Service Log Database Options screen. Refer to figure 7-22 below.

```
Professional Computer Database                         Database Options


       Record Definitions
         View Definitions            Comment

       Hardware Config
         Hardware Config
       Software Config
         Software Config
       Maintenance History           Instructions Here
         Maintenance History         Instructions Here



■ Access Data           _ Create Record Definition
_ Edit Definition       _ Create View Definition     REPLC - Change Database
_ Delete Definition                                EXECUTE - Select Option
                                                    CANCEL - Exit
```

Figure 7-22. VS-300 Service Log Database Options Screen

7.7.2 DATABASE OPTIONS

The following database options (refer to figure 7-22 above) allow the user to retrieve, modify, create, and delete service log definitions and data.

1. Access Data - allows user to retrieve, create, update, and delete information pertaining to the system's hardware configuration, software configuration, and maintenance history. Press SPACEBAR to position acceptance block and cursor, and press EXEC. Press SPACEBAR to select View Definition and press EXEC. Page through multiple screenloads using the NORTH and SOUTH cursor movement keys. Use "Maintenance History" to record system problems and fixes.

2. Edit Definition - allows user to modify record definitions and comments. Also allows user to create, update, and delete field name, data type, and record length. Press SPACEBAR to position acceptance block and cursor, and press EXEC.

3. Delete Definition - allows user to erase record definitions. Press SPACEBAR to position acceptance block and cursor, and press EXEC.

4. Create Record Definition - allows user to add new record definitions and comments, as well as field name, data type, and record length. Press SPACEBAR to position acceptance block and cursor, and press EXEC.

5. Create View Definition - allows user to add new view definitions and comments, as well as field names. Press SPACEBAR to position acceptance block and cursor, and press EXEC. Use INSERT to select record definition and press EXEC.

APPENDIX
A

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APPENDIX A

APPENDIX A

VS-300 Signal Mnemonics, System Errors Requiring a Control Mode Dump, System Errors Causing Continuable Dump, Version Checking Status Error Messages, I/O Controllers and Supported Devices, VS-300 10 Megabyte Duo-binary Modem Channel Allocations

VS-300 SIGNAL MNEMONICS

SIGNAL	DEFINITION
A-Port	Selects which operand is fed to A-Port
ACK	Acknowledge
AGRF	Address Generator Register File (AGU)
AGU	Address Generation Unit
ALU	Arithmetic Logic Unit
APA	Active Port Assembly
ATU	Address Translation Unit
AWS	Archiving Workstation
B-Port	Selects which operand is fed to B-Port
BCR	Bus Control Register
BLANC	Broadband Local Area Network Controller
BSR	Bus Status Register
C OUT R	Command Out Register
CA GEN	Case branch address Generator (CPU)
CAB	Contention Access Based
CHG	Page Changed flag (ATU)
CID	Command Identification
CIU	Cable Interface Unit
COMP	Comparator
CPU	Central Processing Unit
CRE	Current Ring of Execution
CSMA/CD	Carrier Sense Multiple Access Collision Detection
CSPA	Carry Save Propagate Adder
Clock	Controls instruction cycle time (microinstruction field)
DA GEN	Dispatch Address Generator
DAG	Dispatch Address Generator
DB BUFF	D-Bus Buffer. Buffers virtual address to D-Bus
DCC	Decimal Correction Constant register (CPU)
DMA	Direct memory Access
DMUX	Switches MIBR or MAC0 data to MAC1
DR	Display Register
DSA	Data Store Address
DSBS	Data Store Block Select
DSL	Data Store Latch
DVR	Diagnostic Visibility Register
DWBX	Double Word Cache Block crossing
DXAG	Dispatch Exception Address Generator
E-APA	Electric Active Port Assembly
ESU	Exponent Sign Unit. Performs exponent and sign operations
FPU	Floating Point Unit
HDLC	High Data Link Control (CIU)
IAE	Instruction Address Execute Register
ICTRL	Interrupt Controller
IDR	Identification Register
IIOC	Illegal I/O Command (SBI)
ILLMGS	Illegal Message type. SBI status
IOC	Input/Output Controllers

VS-300 SIGNAL MNEMONICS

SIGNAL	DEFINITION
IPC-SBP	Sysbus parity error SBI status
IPCC	InterProcessor Communication Control
IPCR	InterProcessor Communication Register
IPCR	IPC Register
IQ	Instruction Queue (Latches, MUXs, and IR0-3 an the SGU)
IR MUX	Input Register Multiplexers
IR0-3	Instruction Registers 0 through 3
IR1,2	Input Registers 1 and 2
IRE	Instruction Registers Execute
IRE	Instruction Registers
ISMA	Illegal System Memory Address
ISMPA	Illegal System Memory Page Access
ITMR	Interval Timer
IVEAD	Invalid Effective Address Detect
LAT	Long Address Translation
MAC0	Microaddress Control 0 (CPU)
MAC1	Microaddress Control 1 (CPU)
MAG COMP	Magnitude Comparator. Compares CRE to read/write page protect
MC Bus	Memory Control Bus
MCIB	Memory Control Input Buffer
MCU	Memory Control Unit
MIA BUFF	Microinstruction Address Buffer
MIA DRVR	Microinstruction Address Driver
MIAC	Microinstruction Address Comparator
MIAC	Microinstruction Address Comparator (CPU)
MIBR	Microinstruction Address Branch Address Register (CPU)
MIR	Microinstruction Register
MOP-SBP	Memory Operation System Bus Parity Error. SBI status
MSRX	Microstate Register Transceiver
MSRX	Microstate Register Transceiver. Holds microaddress (CPU)
NACK(NAK)	Negative Acknowledge
NIA	Next Instruction Address
NMI	Nonmaskable Interrupt
NVRAM	NonVolitile Random Access Memory
OR1-3	Output Registers 1 through 3
PAR	Physical Address Register
PC	Professional Computer
PCI	Processor Control Interface
PCW	Program Control Word
PFLT	I/O Protection Fault. SBI status
PIAR	Physical Instruction Address Register
PRMD	Protection RAM Data
PSR	Processor State Register
PTENB	Protection RAM ENaBle
R/C MUX	Reference/Change Multiplexer
RAM	Random Access Memory
REF	Page Referenced flag (ATU)

VS-300 SIGNAL MNEMONICS

SIGNAL	DEFINITION
RTRB	Read Transport Reordering Buffer
SAIR	System Address bus Input Register
SAOR	System Address bus Output Register
SBI	System Bus Interface
SBMRPE	System Bus Memory Read Parity Error (SBI)
SBT	Start Bus Transfer. An 8086 I/O initialization command (IOC)
SCM	Support Command Mode. Single microinstruction sequencing
SCR	Support Command Register
SCR	Segment Control Register (ATU)
SCU	Support Control Unit
SCUI	Support Control Unit Interrupt Trap. Microlevel interrupt
SDIR	System Data bus Input Register
SDOR	System Data bus Output Register (SCU)
SMDE	System Memory Data Error (SBI)
SPB	Support Packet Bus. SCU diagnostic control bus
SPDR	Support Packet Data Register (CPU)
SPDR	Support Packet Data Register
SPU	Satellite Processing Unit (same as IOC or CPU)
SR REG	Save Return microaddress REGister (CPU)
SRMR	Save Return Microinstruction REGister (CPU)
SX BUFF	Sign Extend Buffer
TBBP	Translation Buffer ByPass buffer
TBTA	Translation Buffer Tag Address
TM BUFF	Translation/Memory Buffer
TRA	Trap Return Address
TSA MUX	Tag Store Address Multiplexer
TSPL	Tag Store Pipe Line
TV GEN	Trap Vector Generator (CPU)
VA BUFF	Virtual Address Buffer. Buffers address to VARs
VA MUX	Virtual Address Multiplexer
VAR	Virtual Address Register
VAR1,2	Virtual Address Registers 1 and 2
VMAD	Virtual Address illegal Address Detection. SBI status
VTPM	Valid Tag Parity Memory
WCSX	Writable Control Store register/transceiver
WIQD	Write Instruction Queue
WR-A	Working register for ALU calculations
WR-B	Working register for ALU calculations
WS0	Workstation number zero
XMAL	External Memory Address Latch
XMIA	Execute Microinstruction Address register

SYSTEM ERRORS REQUIRING A CONTROL MODE DUMP

ERROR HALT	EXPLANATION
CLMM	An attempt has been made to set the clock comparator from the first TQEL on the timer queue, but the TQEL time value is for the next day (ie: the midnight TQEL is missing).
CLQE	An attempt has been made to set the clock comparator from the first TQEL on the timer queue, but the queue is empty.
FMIP	While searching through the available block list, the next-in-chain link was found to be pointing to the current block.
FMRC	While searching through the available block list, the next-in-chain link was found to be pointing to the current block.
FMRN	While searching through the available block list, the next-in-chain link was found to be pointing to the current block.
GMIC	An attempt has been made to obtain a block from the nonresident memory pool, but the memory chain links were found to be invalid.
GMIP	A memory block of sufficient size was found to satisfy the request, however, the block was page-aligned but not a complete page.
GMRL	While searching through the available block list, the next-in-chain link was found to be pointing to the current block.
GMRN	While searching through the available block list, the next-in-chain link was found to be pointing to the current block.
IOBA	Invalid physical address found in IAL.
IOIH	TCBFLGS3IGIGH is set. Ignore 'HELP'
IOIP	Invalid PPB chain. In attempting to locate the PPB for an IOP (for a given device), the PPB chain was found to be empty.
IOMQ	An IORE has been queued more than once on the IOQ for a device; IORE Address = IORECHN Address.
IOPS	An SIO has been attempted to a device that requires Presentation Services.

SYSTEM ERRORS REQUIRING A CONTROL MODE DUMP (CONT'D)

ERROR HALT	EXPLANATION
PCNR	The program check interrupt handler was activated, but no TCB is active.
PCNT	A program check has occurred in a 'nucleus' task (pager, IO timeout task).
PCPR	A page fault program check interrupt has occurred which is a page fault recursion error.
PGBI	Block number beyond the last extent in the pagefile. (In converting from block-in-file to block-on-volume an invalid block number was obtained.)
PGBT	The paging task was unable to block the faulting task on page frame semaphore.
PGFS	The paging task was unable to find a free page frame semaphore for the faulting task.
PGIP	An attempt has been made to reload the SCRs for the faulting TCB, however, the physical address of the RN table is invalid (indicated from the LPA instruction).
PGIV	A request has been made to mark the paging file with 'No Info' for the input virtual address (VA), but the VA is invalid (cannot be located within the RN table).
PGNS	The paging task was unable to find the required page frame semaphore in the PFSA list.
PGNW	The paging task has detected the nonreentrant use of a reentrant file (i.e., an attempt to page out to a nonwritable file).
PGPS	The paging task was unable to locate the PF semaphore used to block tasks waiting for the current page-in completion.
PGPT	The paging task was unable to locate the page table associated with this file (i.e., the block is beyond the end of the file).
PGQE	The paging task has been activated, however, all of the pager queues are empty.
PPBA	An attempt has been made to return a block to the system page pool but the block is not in use (in use bit already clear).
PPPE	A free block has been requested from the system page pool but none is available.

SYSTEM ERRORS REQUIRING A CONTROL MODE DUMP (CONT'D)

ERROR HALT	EXPLANATION
SCEE	A nonreturnable entry has been made to the scheduler to dispatch a task and the scheduler has returned to the caller.
SCIE	The scheduler was activated but the event code supplied to the scheduler was invalid.
SCIS	A task (TCB) is being unblocked from a semaphore (SEMA) and the semaphore has an invalid type.
SGCT	While setting up and initializing the VTOC cache, a call to GETMEM to obtain space for the cache descriptor table has failed.
SGDD	The system was unable to destroy the TC scan work area after DLP initialization.
SGDI	The system was unable to destroy the IOP scan work area after IOCT initialization.
SGIS	The system was unable to create a block in heap storage for use as an IOP specification block.
SGIW	The system was unable to create a block in heap storage for use as an IOP scan work area.
SGLU	The system was unable to locate the UCB for the specified device.
SGNP	While setting up and initializing the VTOC cache, the available PFT chain was found to be empty.
SGSP	The system was unable to obtain a block through the GETBLK interface to use as a PPB for an IOP.
SGTS	The system was unable to create a block in heap storage for use as a TC specification block.
SGTW	The system was unable to create a block in heap storage for use as a TC scan work area.
SI3J	The FDR1 block for the JSI system services file indicates that there are more than three extents for the file.
SI3S	The FDR1 block for the Segment 1 SVC file indicates that there are more than three extents for the file.
SIFV	The system was unable to free the Segment 0 memory used as the volume label work area.

SYSTEM ERRORS REQUIRING A CONTROL MODE DUMP (CONT'D)

ERROR HALT	EXPLANATION
SIGV	The system was unable to allocate Segment 0 memory to prepare for volume IO (used as a volume label work area to mount accessible disks).
SIIE	An IO Error has occurred while loading the disk IOC microcode. The error is contained within LOWIOSW general and error status fields (i.e., failure was defined as 'Normal Completion' not being obtained).
SIIV	The VCB chain was discovered to be broken while the system was searching the chain during the mounting of accessible disks.
SILF	The FDR1 block for the translation library JSI system services file could not be found.
SIMB	The system was unable to allocate segment memory to read the fault tolerant bit map of a mounted volume.
SIMD	The system was unable to allocate Segment 0 memory to read FDX1 of a mounted disk volume.
SIMF	An attempt to obtain memory for the FLUB for a paging file has failed.
SIMP	An attempt to obtain memory for the system page pool descriptors (SPPD) has failed.
SIRF	During system initialization, a read fail occurred when trying to read FDR1 from the system VTOC.
SIRL	A disk read fail has occurred during disk IOC load. The reason for the error is contained within LOWIOSW general and error status fields (i.e., failure was defined as 'Normal Completion' not being obtained).
SIVC	While attempting to scratch any existing Segment 2 paging files, the system VCB chain was found to be invalid. The VCB end-of-chain was detected without locating the required VCB.
SIWS	The system was unable to release Workstation 0 to the task manager after the completion of system initialization.
USNT	An attempt was made to cancel a task on the system via ZAPTASK, but an unrecoverable error makes continuation of this service questionable (probably task not found).
BLIP	Invalid PPB chain. The PPB chain in the MCB was to be accessed to insert the newly created PPB, but the first entry on the PPB chain was zero.

SYSTEM ERRORS CAUSING CONTINUABLE DUMP

ERROR HALT	EXPLANATION
BLNP	The system was unable to locate the PPB for the specified device.
BLNT	A call to GETBLK was made for individual block allocation but no TCB address was given in the parameter list.
CHFE	The CHECK post wait handler was unable to destroy the sub-task.
CHII	An invalid IOSW has been received from the IOP.
CHLT	The CHECK post wait handler was unable to locate the parent TCB for the requested task number.
CHNP	An attempt to locate the PPB associated with this device (R1) has failed.
CHTL	An attempt to locate the linkage table entry for translation library routine WV17STRT was unsuccessful.
CPNB	An error has been returned from GETHEAP after an attempt to obtain the command processor's buffers from the system pool.
CPPS	Presentation services failed to establish a connection with the remote system and the LOGOFF SVC was entered. However, the logoff was unsuccessful.
CPTM	For the task manager, a false logoff was set and LOGOFF SVC was entered. However, the logoff was unsuccessful.
DBIV	VCB chain invalid. While searching through the VCB chain and sorting the available volumes for paging eligibility, the system volume VCB was not located.
DPPT	The system was unable to locate the page table for a file. Given that multiple page tables exist, the system has searched all PTs chained into this FLUB and has been unable to locate the required page number within the file.
DTIB	DTI has encountered a failure in converting block-in-file to block-on-volume for Segment 2 paging file.
DTIF	DTI has encountered a FLUB not belonging to the SHARER that does not match a Segment 2 paging file FLUB owned by the user task.

SYSTEM ERRORS CAUSING CONTINUABLE DUMP (CONT'D)

ERROR HALT	EXPLANATION
DTIP	While attempting to unmap a physical page, the page frame number was found to be invalid.
DTLP	Given that multiple page tables exist, an attempt to locate a page table for a file (FLUB) has failed.
DTXE	DTI has received an error return code from XIO on attempting to write out the paging file block.
DUMP*	WM27 calls snapshot dump if the task that PC'd was a system task.
GHNP	No PFB was found within the ETCB for this GETHEAP call.
IDMA	IPC destroy was unable to cancel a mailbox alias.
IKSV	During the invoke task for one of the system tasks, a search of the VCB chain for the system volume was unsuccessful.
IRG2	A call to IWAIT to wait on a temporary mailbox did not result in a return message.
IRMM	IPC retrieve was unable to move a message body from the message buffer to the user specified area. The error response code from FAGRMAP is still held in the local variable area RETCODE (referenced through R11)
MLNF	While searching the FLUB chain, no FLUB with a name matching the file name in work area was found.
MLNO	While searching the OFB file chain, no OFB with OFDTCB = CPUTCB was located.
MLNP	The system was unable to locate the PPB for the specified device.
MLQI	During the close phase of microcode load, prior to freeing the OFB and IORE, a check was made to see if the IORE was still queued on the UCB and the IORE was found to be queued.
PCDU*	WS50 causes a task to suspend, then calls a continuable dump. It Will result in a task crash.
RAOR*	It is not possible to open or read the alias file.
*	After the continuable Dump is completed, the system continues without a reIPL.

SYSTEM ERRORS CAUSING CONTINUABLE DUMP (CONT'D)

ERROR HALT	EXPLANATION
RARB	An attempt to obtain nonresident memory as a read buffer for the alias file has failed.
RARF*	It is not possible to read the alias file.
RAUM	An attempt to allocate memory from the heap for use in the open alias file routine as a UFB has failed.
RRMB	No message buffer was found chained to the TCB for this XTERM call.
RRNP	No PFB was found within the ETCB for this XTERM call.
RSIS	An invalid Segment 1 SVC invocation during system initialization has occurred.
SRCN	TCBINSMC is negative. The only legal values are nonnegative.
SRSN	TCBSMECBK for the resource in question is negative. The only legal values are nonnegative.
TIDC	After attempting to map the debugger code for this task, an error response was returned from the MAP SVC.
TIDD	After attempting to unmap the debugger data for this task, an error response was returned from the UNMAP SVC.
TIDU	After attempting to unmap the DMS shared area for this task, an error response was returned from the UNMAP SVC.
TIID	After successfully mapping the debug code for this task, it is the wrong debug file. This was determined by checking the address at which debug should have been mapped against the address at which it was actually mapped.
TIIE	After completing the necessary task initialization, control has been returned to SYSINIT when it should not have been possible to return.
TILT	After attempting to map the linkage table for this task, an error response was returned from the MAP SVC.
*	After the continuable Dump is completed, the system continues without a reIPL.

SYSTEM ERRORS CAUSING CONTINUABLE DUMP (CONT'D)

ERROR HALT	EXPLANATION
TIMD	After attempting to map the DMS services for this task, an error response was returned from the MAP SVC.
TIMH	After attempting to map the IPC header buffers for this task, an error response was returned from the MAP SVC.
TIMS	After attempting to map the Segment 1 system SVCs for this task, an error response was returned from the MAP SVC.
TIS1	After attempting to unmap the Segment 1 SVCs for this task, an error response was returned from the UNMAP SVC.
TISA	After successfully mapping the system services for this task, it was impossible to find the system services address in the linkage table.
TISD	An attempt to obtain memory for the DMS vector table has failed. This table is allocated only once, when the first task is initialized.
TISM	After attempting to map the DMS shared area for this task, an error response was returned from the MAP SVC.
TISS	After attempting to map the system services for this task, an error response was returned from the MAP SVC.
TIST	An attempt to obtain memory for the TRN vector table has failed. This table is allocated only once, when the first task is initialized.
TITL	After attempting to map the translation library for this task, an error response was returned from the MAP SVC.
TIUB	After attempting to unmap the IPC bodies region for this task, an error response was returned from the UNMAP SVC.
TIUD	After attempting to unmap the DMS file for this task, an error response was returned from the UNMAP SVC.
TIUE	After completing the necessary termination functions and invoking UNLINK, control has been returned to SYSINIT when it should not have been possible to return. Exit from UNLINK should have been to the task quit code.
TIUL	After attempting to unmap the linkage table for this task, an error response was returned from the UNMAP SVC.

SYSTEM ERRORS CAUSING CONTINUABLE DUMP (CONT'D)

ERROR HALT	EXPLANATION
TIUS	After attempting to unmap the system services for this task, an error response was returned from the UNMAP SVC.
TIUT	After attempting to unmap the translation library for this task, an error response was returned from the UNMAP SVC.
TIWD	After successfully mapping the DMS services for this task, it is shown to be the wrong SVC file. This was determined by checking the address at which DMS should have been mapped against the address at which it was actually mapped.
TIWS	After successfully mapping the Segment 1 system SVCs for this task, further checking shows it to be the wrong SVC file. This could mean that either the original 8-MB file was incorrectly mapped in or an attempt to subsequently map the 16 MB version also failed.
ULDM*	UNLINK has invoked the system service to destroy a mailbox and an error response has been returned.
ULDT	UNLINK has invoked the system service to destroy the trace buffers and an error response has been returned.
ULFP	UNLINK has invoked the system service to unfix the disk diagnostics pages that were allocated to this task and received an error response.
ULNF	UNLINK was unable to locate the current Segment 1 FLUB on the system FLUB chain in order to free the FLUB.
ULNL	UNLINK decremented the task's current link level (ETCB) and the resulting link level was negative.
ULNP	A PFB SAVE area has not been located in a level stack. A search of all this task's active process level stacks for for one which contains the PFB (comparing against stack minimum and maximum values in the stack header) has failed.
ULPC	Having adjusted the necessary stack(s), it is now no longer possible to locate any PFB via the ETCB PFB chain.
ULUM	UNLINK was attempting to unmap each MAPB on the specified MAPB chain when, for one MAPB, an error response was received from UNMAP.

* After the continuable Dump is completed, the system continues without a reIPL.

VERSION CHECKING STATUS ERROR MESSAGES

MESSAGE	DEFINITION	COMPONENTS
(blank)	No problems are detected.	
WARNING	A version problem exists with this component, though it is not critical enough to halt system initialization.	@PRTTSK@ @SHARER@ DEVLIST
FATAL ERROR	IPL procedures cannot continue. Obtain a current, compatible version version of the component and then reIPL.	@SYSGEN@ @SYSTSK@ @OPER@ @SYSCPR@ @TSKMGR@

VS-300 I/O CONTROLLERS AND SUPPORTED DEVICES

This appendix lists, according to the input/output controller (IOC), the supported devices for the VS-300.

VS-300 IOC	TYPE OF IOC	DEVICES SUPPORTED
23V98-1	Disk	2280V-1 30 MB fixed and removable drive
23V98-2		2280V-2 60 MB fixed and removable drive
23V98-3		2280V-3 90 MB fixed and removable drive
23V98-4		2265V-1 75 MB removable drive (SMD)
		2265V-2 288 MB removable drive (SMD)
		2265V-3 620 MB fixed drive (FMD)
		2267V-1 76-MB removable drive (RSD)
		2268V-1 76 MB fixed drive (WINC)
		2268V-2 147 MB fixed drive (WINC)
		2375V-1, C3 454 MB fixed drive (FSD)
		SW04 Disk Switch for all drives (except 2280V drives)
23V97	32 port serial	2509, 9-track serial tape drive
		2529V 6400 bpi cartridge tape drive
		2238V1 Streamer tape
		2276C-1 64KB combined archiving workstation
		2276C-3 Combined archiving workstation
		2860-6 Combined archiving workstation
		2860-7 Combined archiving workstation
		4250-VS Combined archiving workstation
		WPC Combined archiving workstation
		2256C 64KB combined workstation
		4205 Monochrome combined workstation
		4210 Monochrome DP workstation
		4230 64KB monochrome combined workstation
		4245 Color combined workstation
		5300/VS-IIS64 Combined workstation
		5300W/VS Combined workstation
		5300/VS-AL-AUD Combined workstation
		5300/VS-AUD Combined workstation
		6300/VS-64 Combined workstation, including graphics
		5533 100-cps matrix printer
		5535 180-cps matrix printer
		5573 250-lpm band printer
		5574 600-lpm band printer
		5575 Printer-IIS/DP
		5577V High density matrix printer
		5577A High density matrix printer
		6581W 40-cps daisy printer

I/O CONTROLLERS AND SUPPORTED DEVICES

VS-300 IOC	TYPE OF IOC	DEVICES SUPPORTED
		6581WC-1 Printer-IIS/DP/ALLIANCE
		5581WD-1 Printer-ALLIANCE
		DW/OS-20 20-cps daisy printer
		DW/OS-55 55-cps daisy printer
		LPS-12 Laser printer (WP only)
		LIS-12V Printer-IIS/DP
		LIS-12A Printer-ALLIANCE
		6554/TCB Telecommunications Processor
		CIU-B WangNet SystemBand Modem
		6550 Gate Array TCB
23V96	Multiline Telecommunications	2110 Workstation
		4220 Binary synchronous remote workstation
		2246R Remote workstation
		2281 Remote daisy printer
		2233 Remote matrix printer
		2235 Remote matrix printer
		2273V-1 Remote band printer
23V95-1	Tape	2209V tape drive
23V95-2	Tape	2219V tape drive
23V79	WangBand CIU	

VS-300 10 MEGABYTE DUO-BINARY MODEM CHANNEL ALLOCATIONS

NOTE

When the 10 megabyte modem is used on the channel listed in the first column, devices listed under device type should not be used on the channels listed under the channel/frequency column.

10 MBPS CHANNEL	DEVICE TYPE	CHANNEL/FREQUENCY	
CHANNEL 0	Global:	CH14	(209 - 217 MHz)
(216 - 228 MHz)	Global:	CH15	(217 - 225 MHz)
	Global:	CH16	(225 - 233 MHz)
	TV:	CH J	(216 - 222 MHz)
	TV:	CH K	(222 - 228 MHz)
	Old Modem		(216 - 243 MHz)
CHANNEL 1	Global:	CH16	(225 - 233 MHz)
(228 - 240 MHz)	Global:	CH17	(233 - 241 MHz)
	TV:	CH L	(228 - 234 MHz)
	TV:	CH M	(234 - 240 MHz)
	Old Modem		(216 - 243 MHz)
CHANNEL 2	Global:	CH17	(233 - 241 MHz)
(240 - 252 MHz)	Global:	CH22	(241 - 249 MHz)
	Global:	CH19	(249 - 257 MHz)
	TV:	CH N	(240 - 246 MHz)
	TV:	CH O	(246 - 252 MHz)
	Old Modem		(216 - 243 MHz)
CHANNEL 3	Global:	CH19	(249 - 257 MHz)
(252 - 264 MHz)	Global:	CH20	(257 - 265 MHz)
	TV:	CH P	(252 - 258 MHz)
	TV:	CH Q	(258 - 264 MHz)
	SIMS:		(258 - 264 MHz)
CHANNEL 4	Global:	CH20	(257 - 265 MHz)
(264 - 276 MHz)	Global:	CH21	(265 - 273 MHz)
	Global: (Note)	CH22A	(273 - 281 MHz)
	TV:	CH R	(264 - 270 MHz)
	TV:	CH S	(270 - 276 MHz)

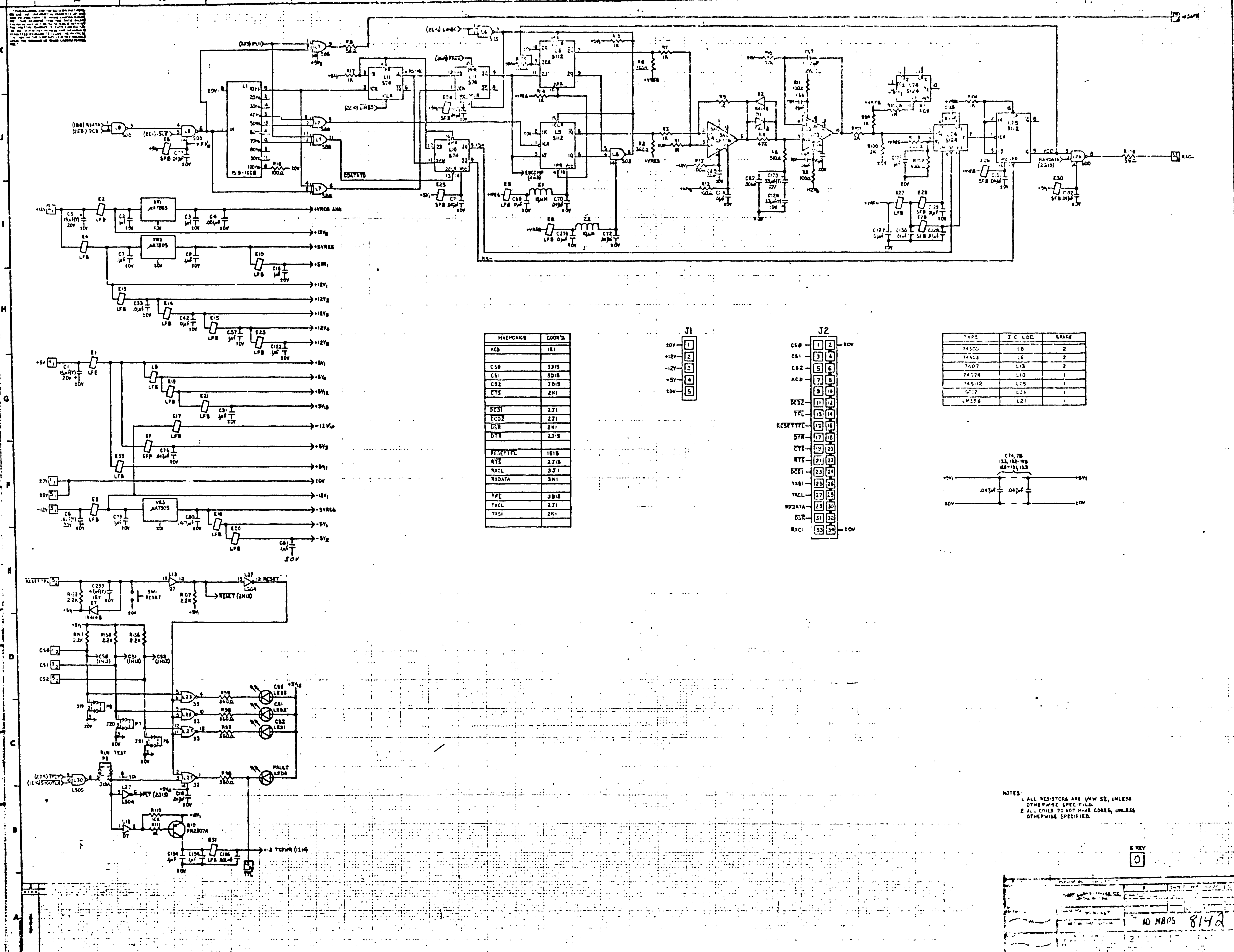
NOTE

This channel not presently available.

SCHE-
MATICS

VS-300 SCHEMATICS

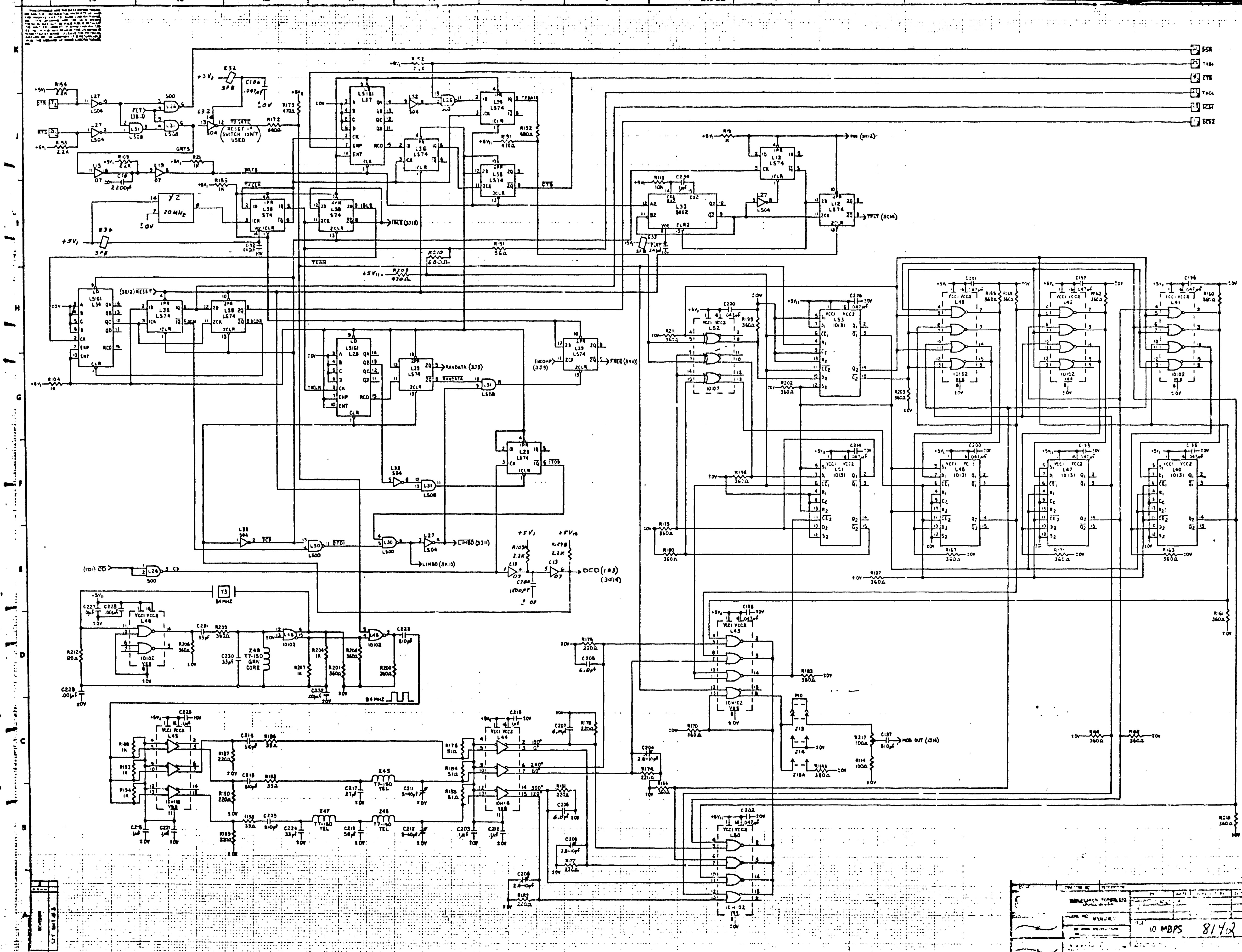
WLI P/N	Description	Number Of Sheets
210-8142	10MBPS, 5-Channel RF Modem	3
210-8310	SCU Local Comm. Option	6
210-8377	PC/LVS (PC to SCU Interface)	5
210-8391	CIU CAB (23V79)	7
210-8392	CIU BLANC IOC (23V79)	9
210-8491	MLTC IOC (23V96)	16
210-8494	RS232A Dr./Rcv. (MLTC)	2
210-8495	RS366 Dr./Rcv. (MLTC)	2
210-8496	Serial Communications Link	2
210-8497	Block Connector	2
210-8503	APA (Muxbus) Terminator	2
210-8504	APA (Active Port Assembly) (SE 8P Multiplex XCVR)	3
210-8509	BNC/TNC Active Port Assembly	3
210-8514	Low-Cost 12" Monitor	2
210-8609	Serial IOC (23V97)	8
210-8703/8703-1	Main Memory (4/8-Megabytes)	16
210-8709	Power Supply Controller	5
210-8710	SCU/PC Adapter	2
210-8715	AC Distribution	3
210-8716	DC Distribution	3
210-8717	Battery Backup	2
210-8785	SMD IOC (23V98-1/2/3/4)	9
210-8789	Telex Tape IOC (23V95-2)	6
210-8790	Kennedy Tape IOC (23V95-1)	7
210-8831	CPU	23
210-8832	Address Generation Unit	21
210-8833	Address Translation Unit	21
210-8834	Memory Control Unit	18
210-8835	Support Control Unit	15
210-8836	System Bus Interface	23
210-8837	Backplane	5
210-9225	SCU Winchester Controller	6
210-9231	CPU	23
210-9236	System Bus Interface	23
210-9237	SCU Motherboard	2
210-9245	SCU Local Comm. Data Link	9
210-9246	SCU Local Comm. Processor	6
210-9343	SCU Character Resolution	5
210-9521	SCU CPU/Memory (256K)	7

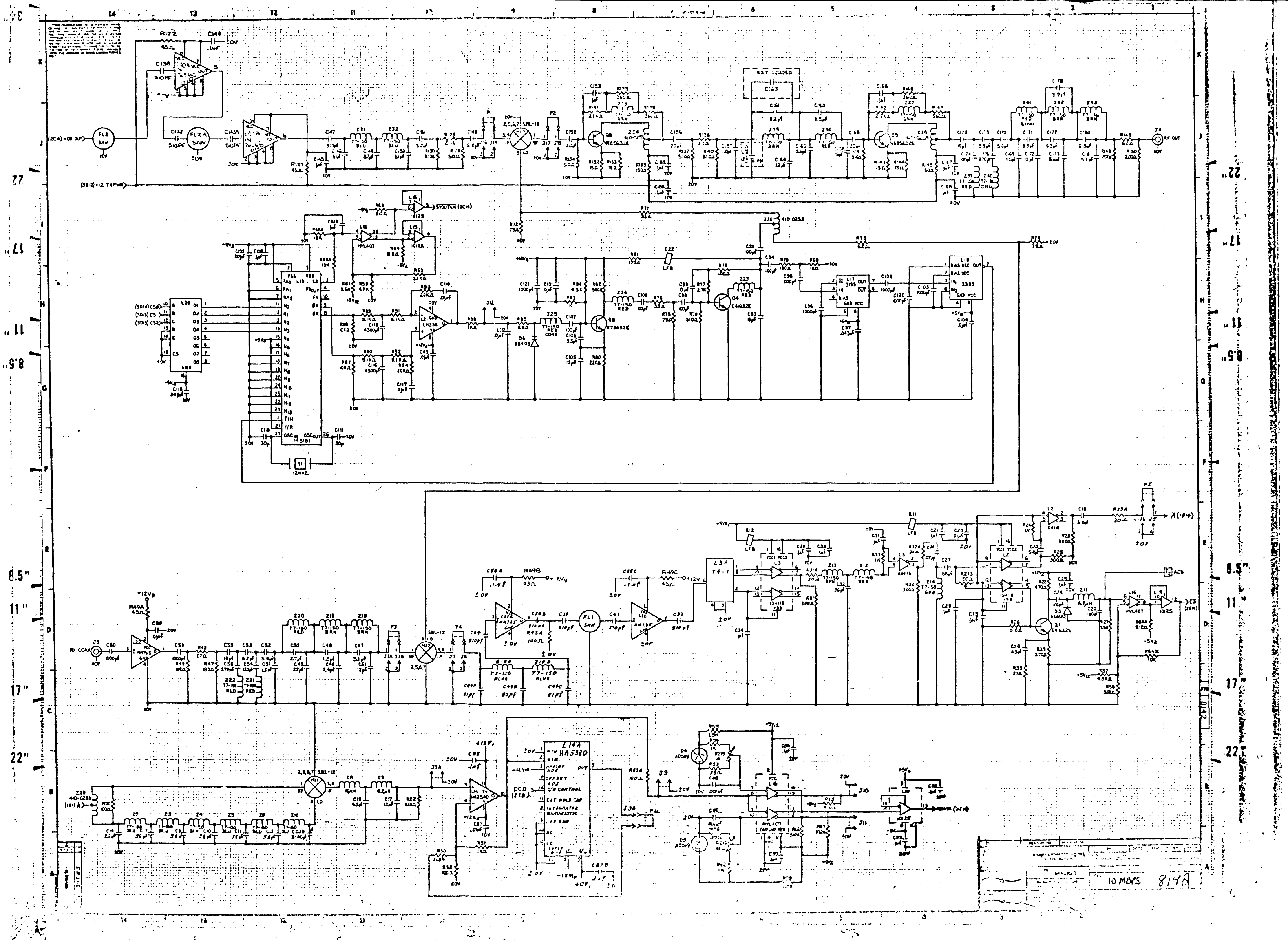


MNEMONICS	COOR'D.
ACD	1E1
CSØ	3D15
CS1	3D15
CS2	3D15
CTS	2K1
DCD1	2J1
DCD2	2J1
DSR	2K1
DTR	2J15
RESETTFL	1E1B
RTS	2J1B
RXCL	3J1
RXDATA	3K1
TFL	3B12
TXCL	2J1
TXS1	2K1

TYPE	I C LOC.	SPARE
74S00	L8	2
74S03	L6	2
7407	L13	2
74S74	L10	1
74S112	L25	1
[illegible]	L33	1
LM358	L21	1

NOTES:
1. ALL RESISTORS ARE 1/4W 5%, UNLESS OTHERWISE SPECIFIED.
2. ALL COILS DO NOT HAVE CORES, UNLESS OTHERWISE SPECIFIED.

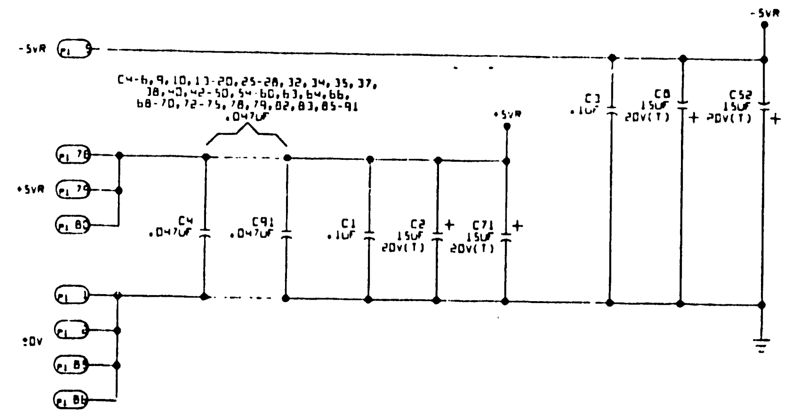

10 MBPS
8142
RANDATA (3J3)
DCD (1E3)
84 MHZ



RF OUT
RX COAX
HA5320
10 MBPS
8142

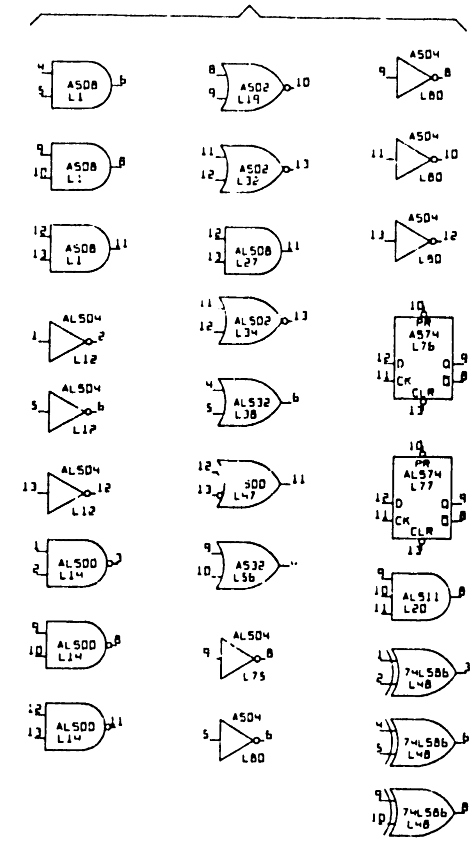
NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



MNEMONICS	COORD.
AIOWC	5E14
AMWC	2K11
BHE	2A14
CLK	5G14
DATRD	2K12
+GA	4I1
+GB	4J1
HACK	5F14
IOERROR	3G1
IORC	5D14
IORQ0-IORQ7	5A12
MRDC	2K11
PA0-PA19	5I14
PD0-PD7	3E1
PD8-PD15	3F1
-RA	4K1
-RB	4J1
RDY	5J1
RESET	2B14
SXD	5G14
SID0-SID3	5G14
HCLK	5F14

SPARES



E REV 2 N

WANG LABORATORIES, INC.

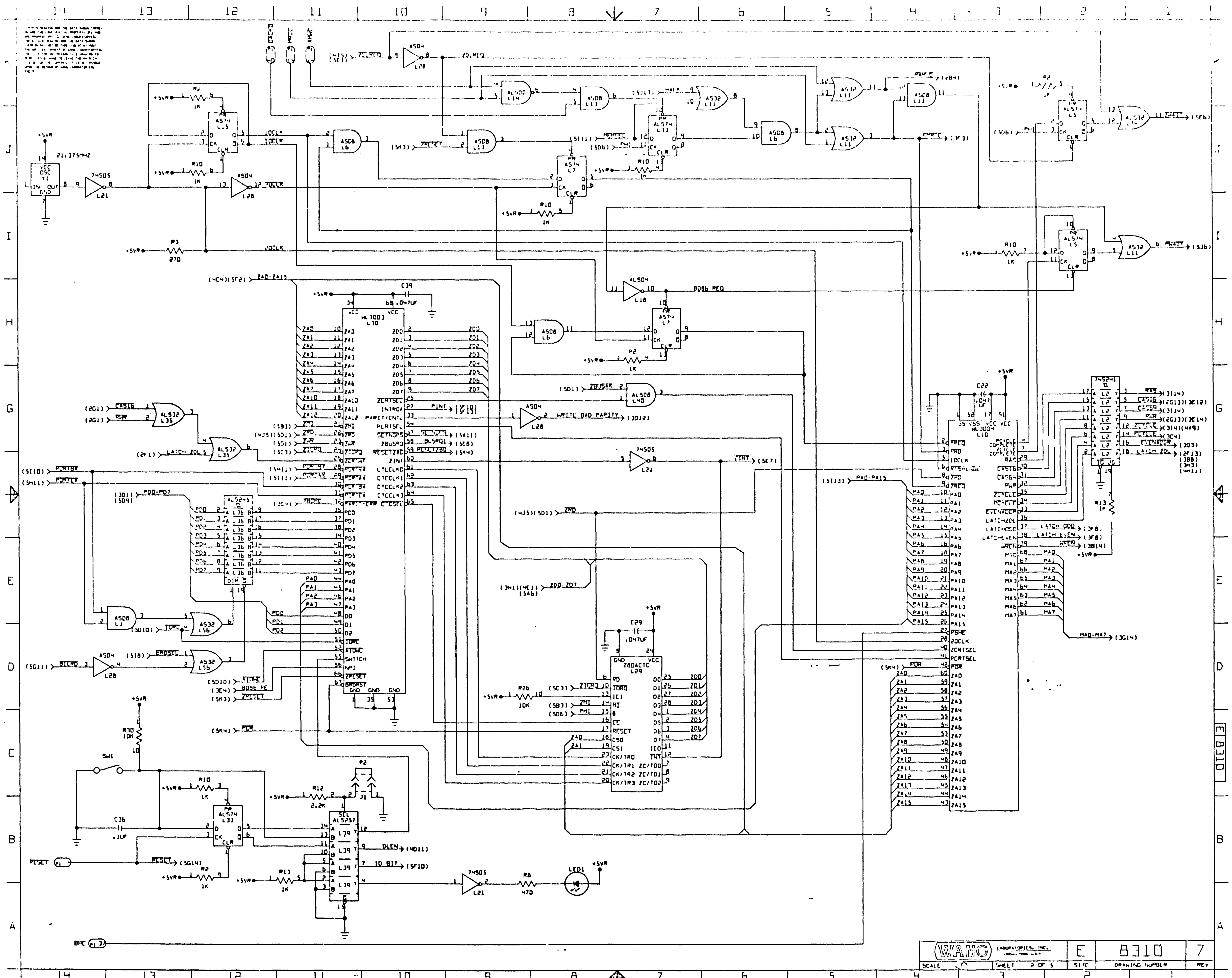
SCHEMATIC DIAGRAM

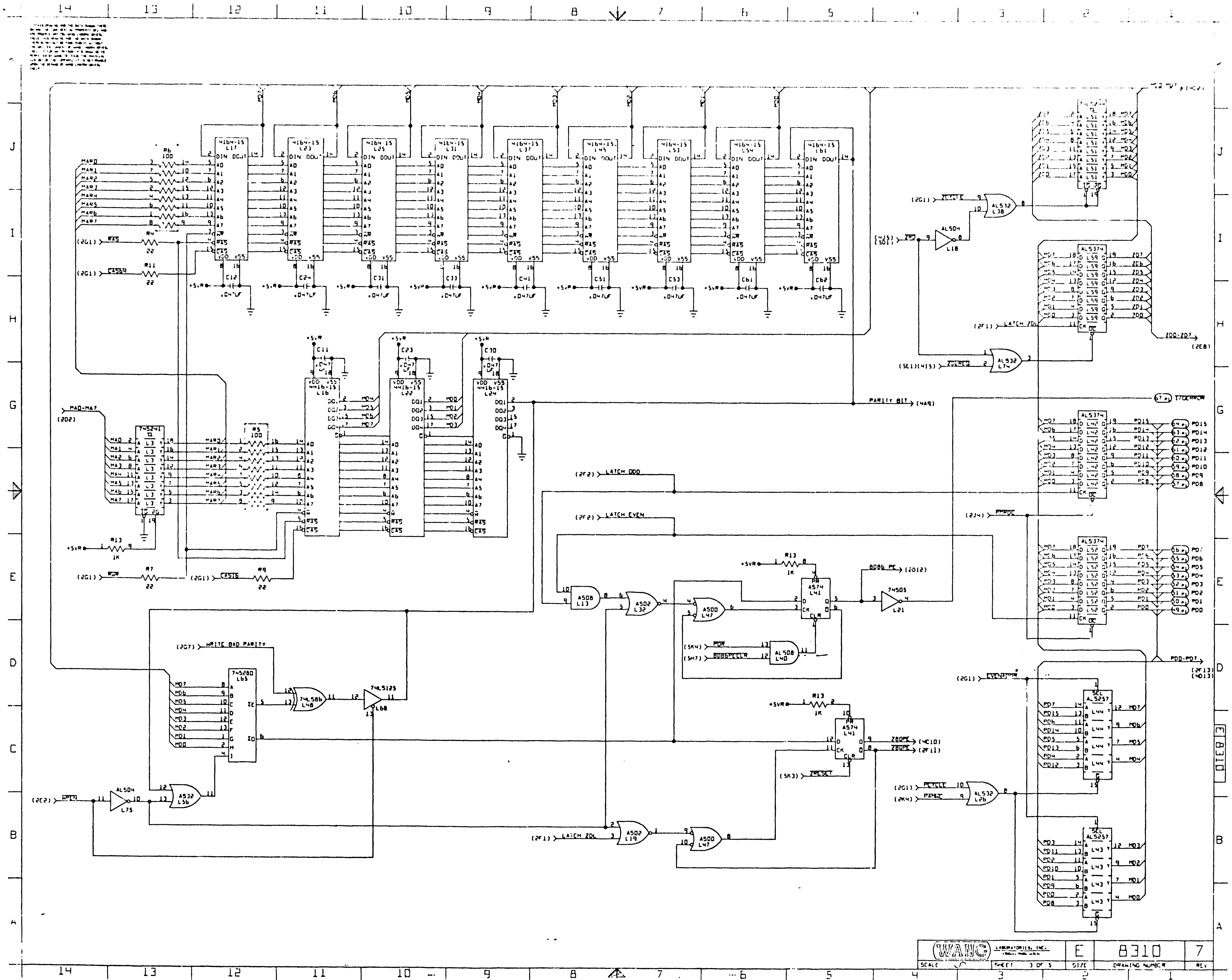
TITLE SINGLE BD. LOCAL COMM OPTION M/L

PBC | WANG PART NUMBER SEE CHART

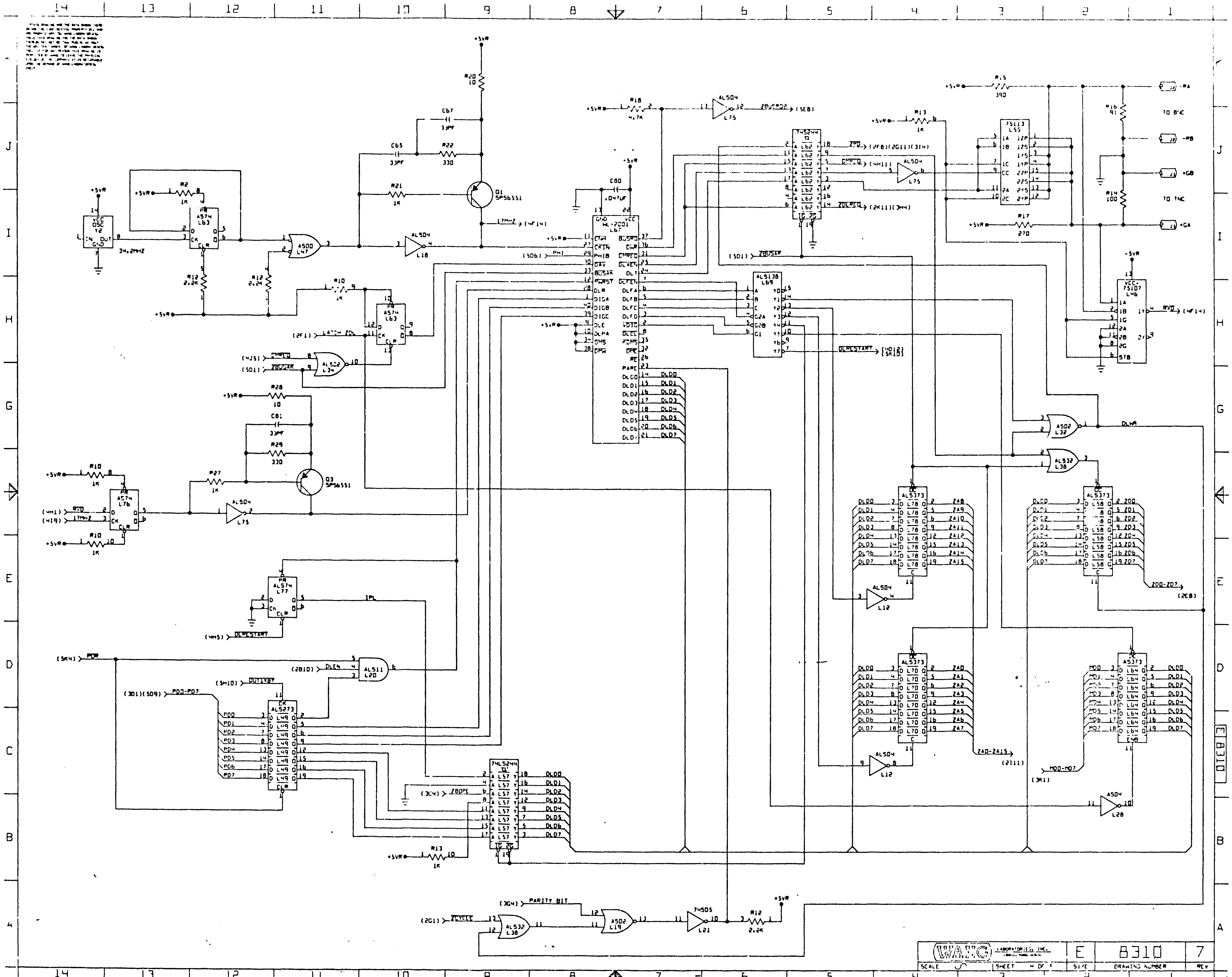
SIZE E | DRAWING NUMBER 8310 | REV 7

SHEET 3 OF 5

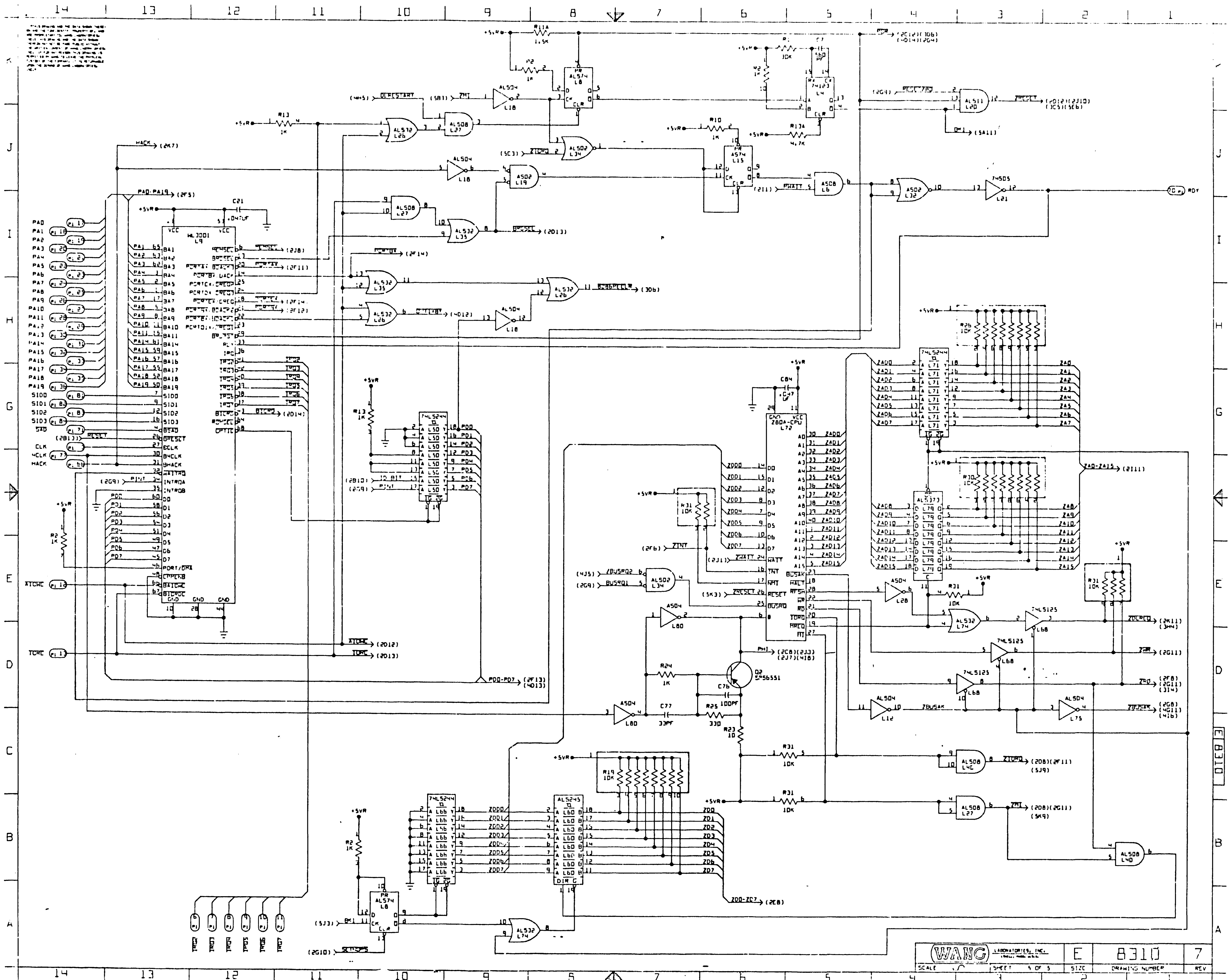

WANG
E
8310
7
SHEET 2 OF 5
SCALE
SIZE
DRAWING NUMBER
REV



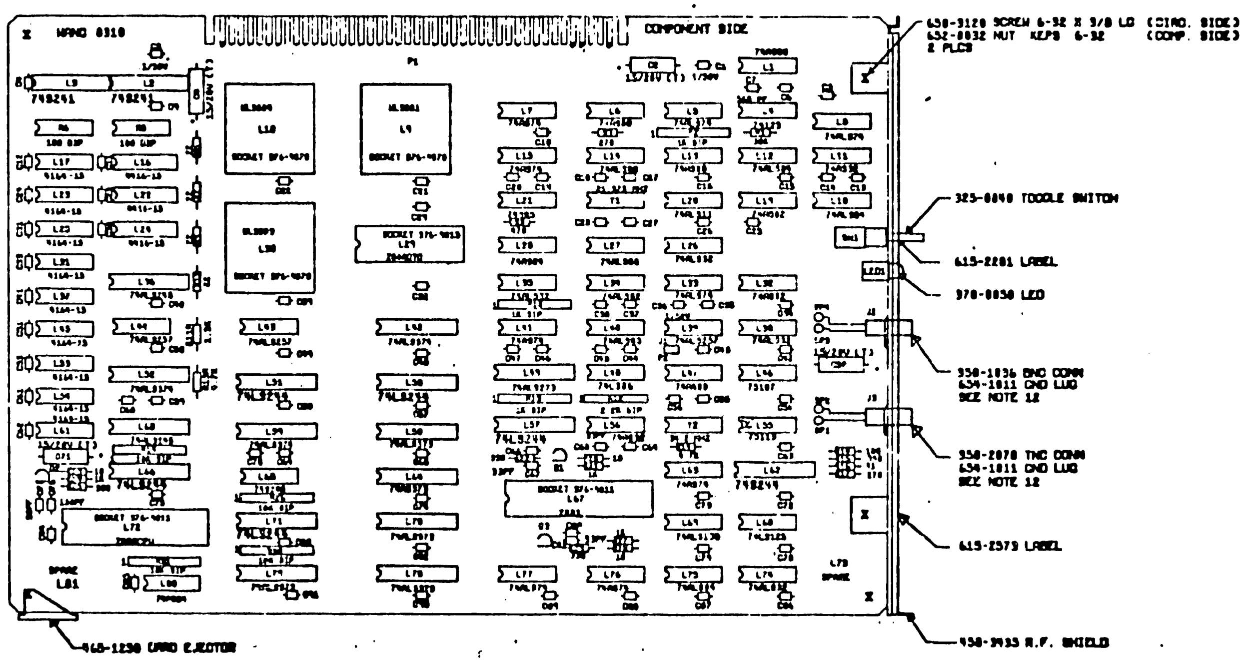
WANG LABORATORIES, INC.
E
8310
7
SCALE
SHEET 3 OF 5
SIZE
DRAWING NUMBER
REV
4164-15
4416-15
74S241
74S280
74LS86
74LS125
AL504
AL532
AL508
AL5374
AL5257
AS02
AS08
AS00
AS74
74S05
LATCH ODD
LATCH EVEN
LATCH ZDL
WRITE BAD PARITY
PARITY BIT
8086 PE
Z80PE
MAD-MA7
ZDD-ZD7
PDD-PD7



TO BNC
TO TNC
Q1 SP56551
Q3 SP56551
34.2MHZ
PARITY BIT
E
8310
7
SCALE
SHEET
SIZE
DRAWING NUMBER
REV



WANG LABORATORIES, INC.
E
8310
7
SCALE
SHEET 4 OF 5
SIZE
DRAWING NUMBER
REV
Z80A-CPU



NOTES: UNLESS OTHERWISE SPECIFIED.

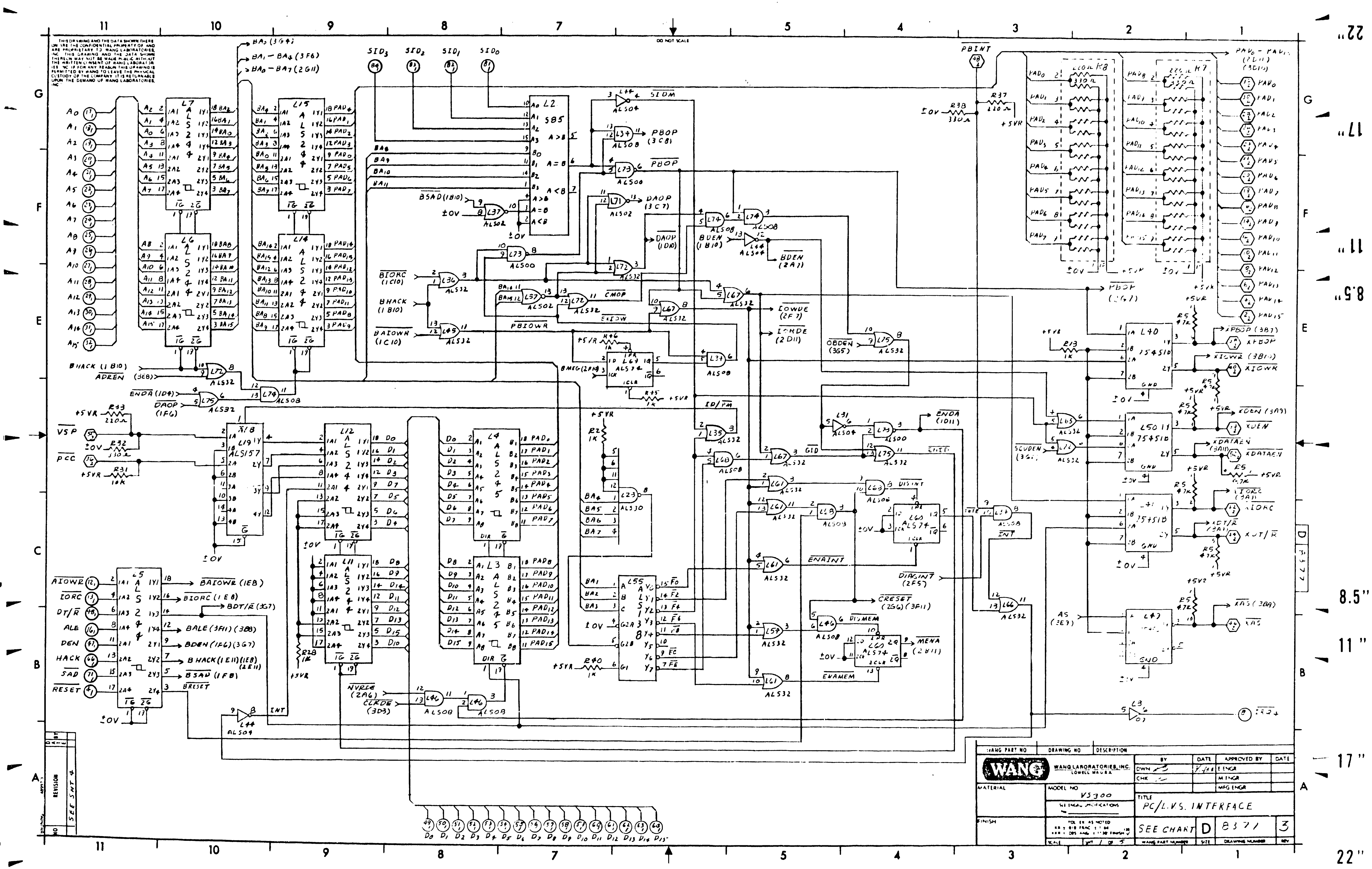
1. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W 5 PERCENT EXPRESSED IN OHMS.
3. Q1,Q2,Q3 2N5771 TRANSISTOR W.P NO 375-1050.
4. J1 2PIN HEADER CONN W.P NO. 350-0203, WITH SHUNT P2, W.P.NO. 350-4506.
5. Y1,Y2 LOAD TEKNA INSULATOR W.P.NO. 376-9000.
6. ALL 10K SIPS ARE W.P NO 333-0009.
7. ALL 1K SIPS ARE W.P NO. 333-0037.
8. ALL 2.2K SIPS ARE W.P NO. 333-0006.
9. ALL 100 DIPS ARE W.P NO. 333-0051.
10. Y1 21 375 MHZ CRYSTAL W.P NO. 321-0099.
11. Y2 34 2 MHZ CRYSTAL W.P NO. 321-1009.
12. WIRE USED ON BNC,TNC CONNECTIONS ARE TO BE AS FOLLOWS:
    20 GAUGE RED P/N 600-0302.
    20 GAUGE BLACK P/N 600-0300.

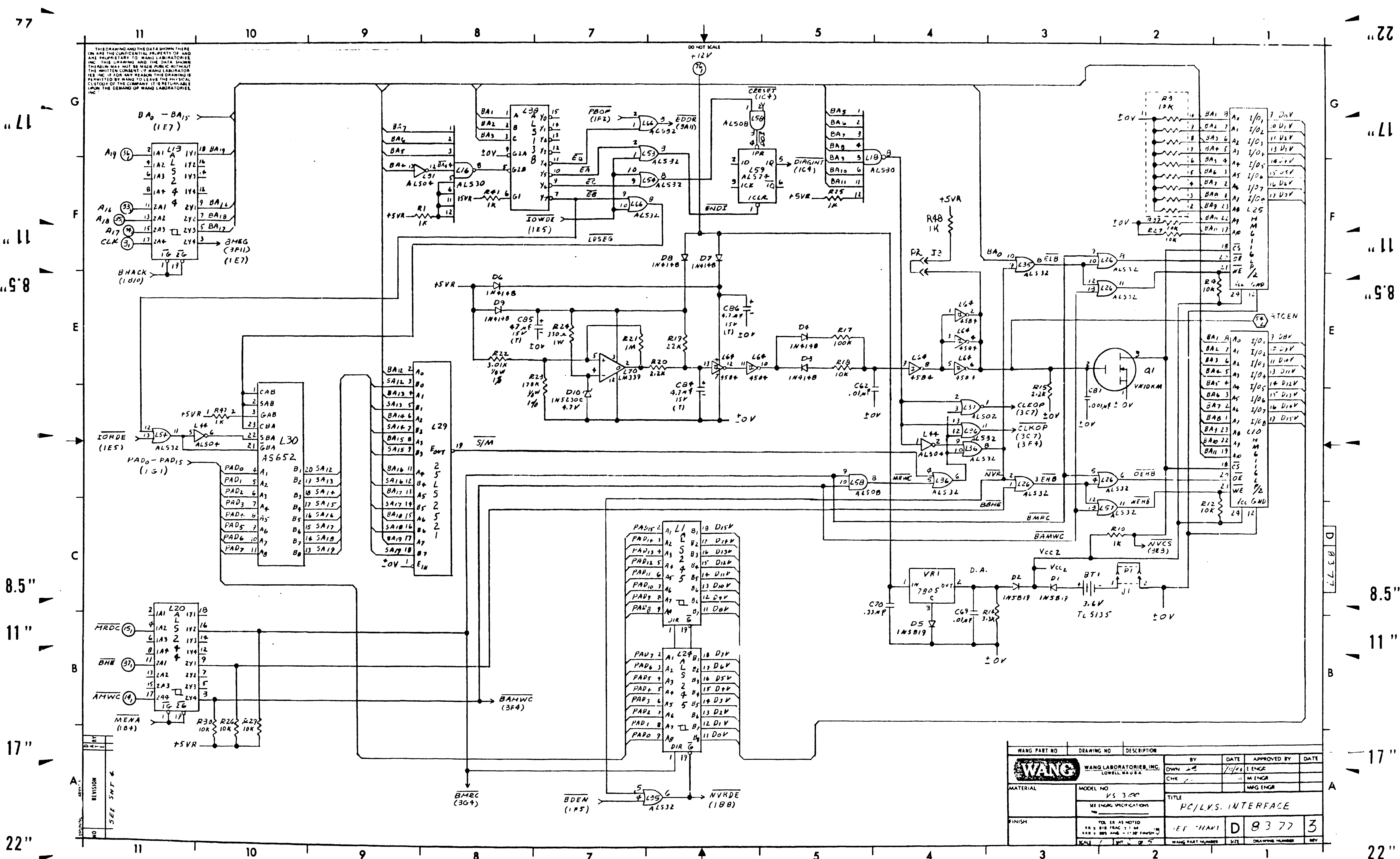
8310-2
SINGLE BOARD LOCAL COMM. OPTION N/L
FOR ALL ASSOCIATED DOCUMENTS, SEE HISTORY SHEET

WANG LABORATORIES, INC.

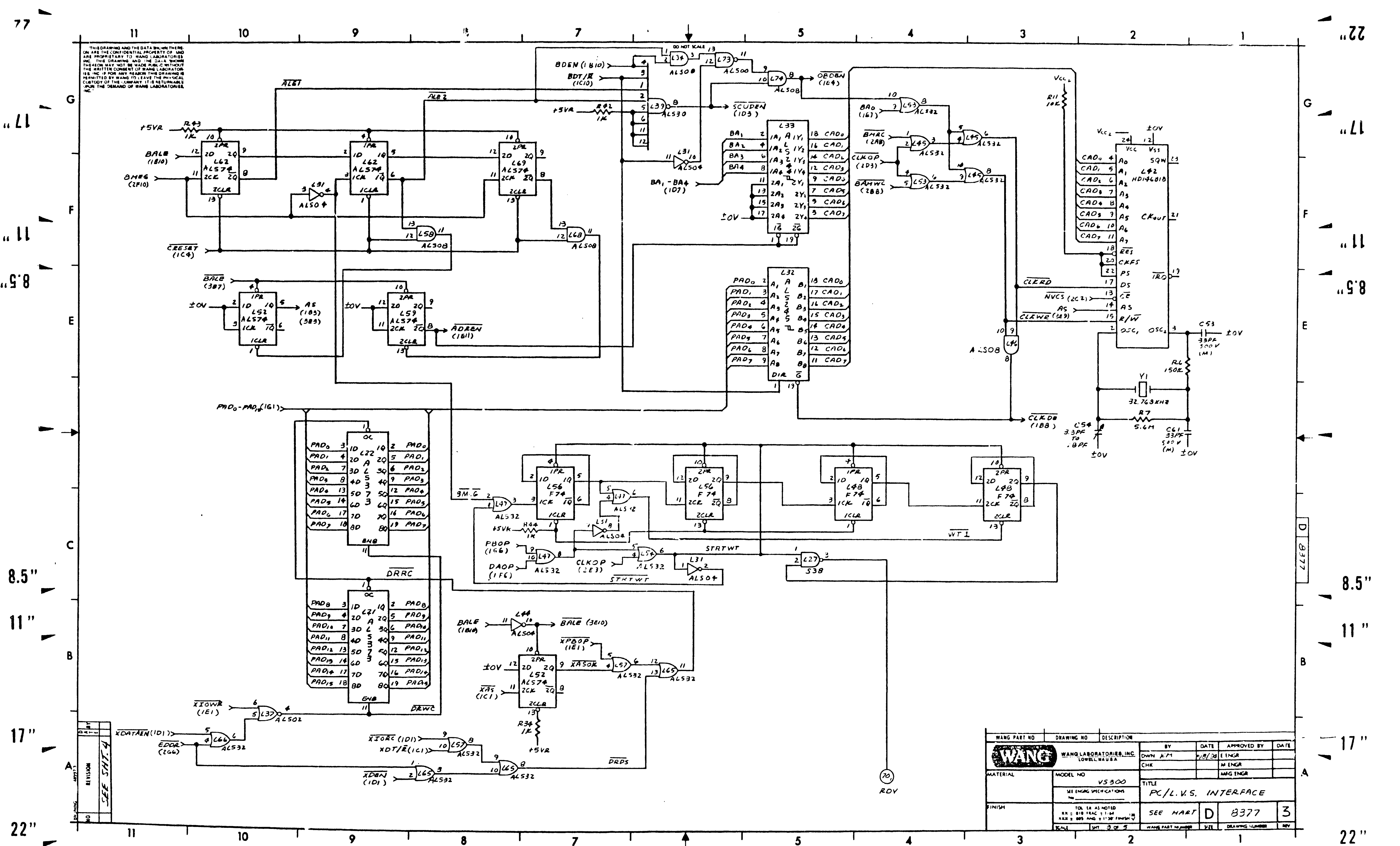
TITLE SINGLE BD LOCAL COMM OPTION N/L
ASSEMBLY DRAWING

210-8310 D 8310 6


WANG
WANG LABORATORIES, INC.
LOWELL MASS.
MODEL NO
VS300
TITLE
PC/L.V.S. INTERFACE
SEE CHART
D
8371
3
DO NOT SCALE



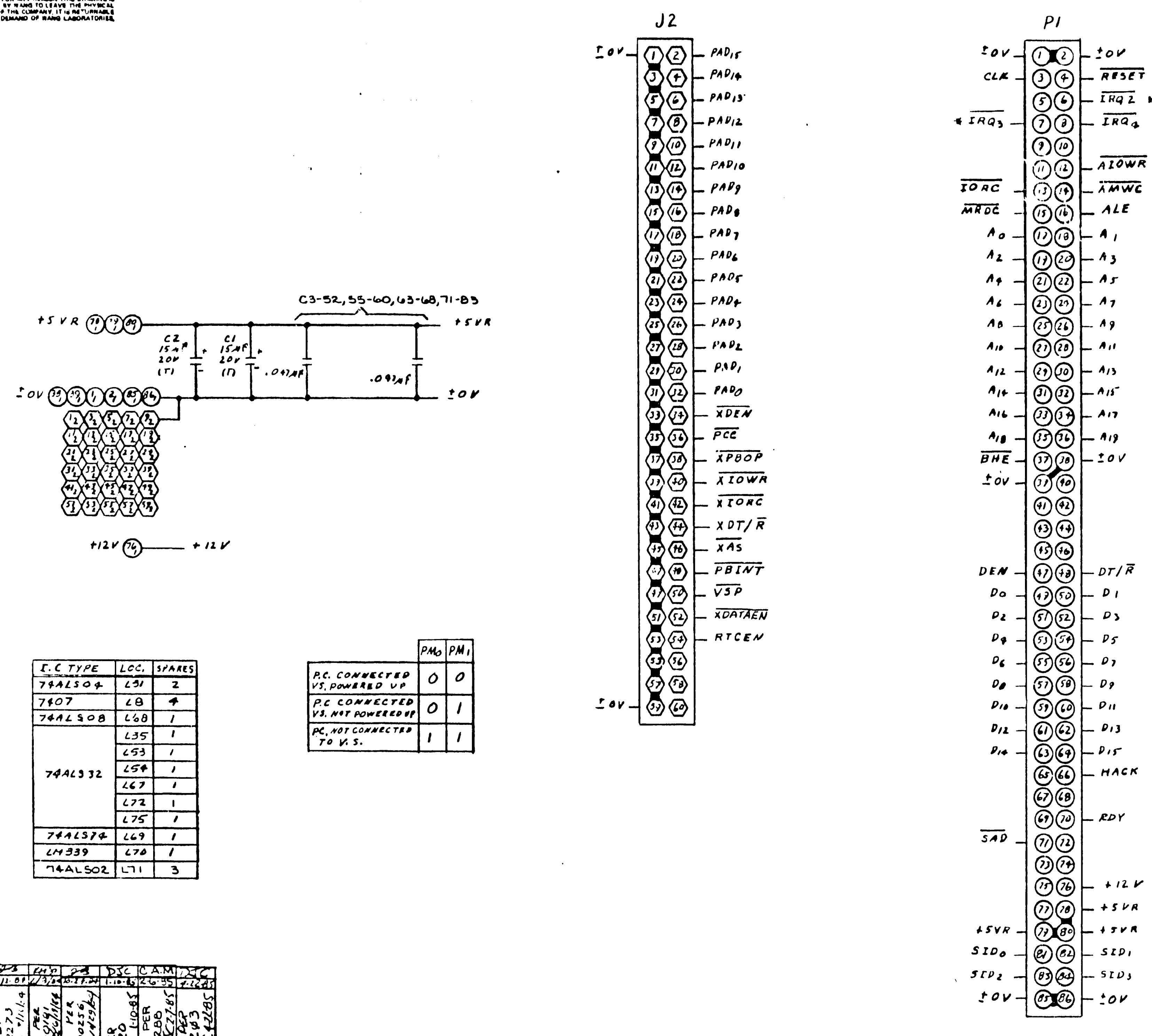
DO NOT SCALE
WANG LABORATORIES, INC.
LOWELL, MASS.
MODEL NO VS 300
TITLE PC/LVS. INTERFACE
D 8377 3


WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
MODEL NO VS300
TITLE PC/L.V.S. INTERFACE
D 8377 3
SEE SHT. 4

THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC.

DO NOT SCALE

* NOT USED AT THIS TIME



MNEUMONICS	COORD
$A_0 - A_{15}$	1F11
$A_{16} - A_{19}$	2F11
ALE	1B11
AIOWR	1C11
AMWC	2B11
BHE	2B11
CLK	2F11
$D_0 - D_{15}$	1A7
DEN	1B11
DT/R	1B11
HACK	1B11
IORC	1C11
IRQ_4	1B1
MRDC	2B11
$PAD_0 - PAD_5$	1F1
PBINT	1G3
PCC	1D11
RTCEN	2E1
RESET	1B11
RDY	3A4
SAD	1B11
$SI_0 - SI_3$	1G8
VSP	1D11
XAS	1B1
XDEN	1D1
XDT/R	1C1
XIOWR	1E1
XIORC	1C1
XPBOP	1E1
XDATAEN	1D1

I.C TYPE	LOC.	SPARES
74ALS04	L31	2
7407	L8	4
74ALS08	L68	1
74ALS32	L35	1
	L53	1
	L54	1
	L67	1
	L72	1
	L75	1
74ALS74	L69	1
LM339	L70	1
74ALS02	L71	3

	PM_0	PM_1
P.C. CONNECTED VS. POWERED UP	0	0
P.C CONNECTED VS. NOT POWERED UP	0	1
PC, NOT CONNECTED TO V.S.	1	1

210 = 209 + 377 OR 378		
210	209	L2
8377-A	8377	377-0903

E - REV

2

NOTE:

1. ALL RESISTORS ARE 1/4 W 5 % UNLESS SPECIFIED OTHERWISE

REV	REVISION
A	ORIG PER DWR # E2273 APP'D
B	REVISED PER DCR-K# 00141
C	REVISED PER DCN-K# 00256 APP'D
1	REVISED PER ECO# 34720 APP'D: DTC 1-10-85
2	REVISED PER ECO# 35288 APP'D: DTC 2-27-85
3	REVISED PER ECO# 36203 APP'D: DTC 4-12-85

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

WANG PART NO | DRAWING NO. | DESCRIPTION

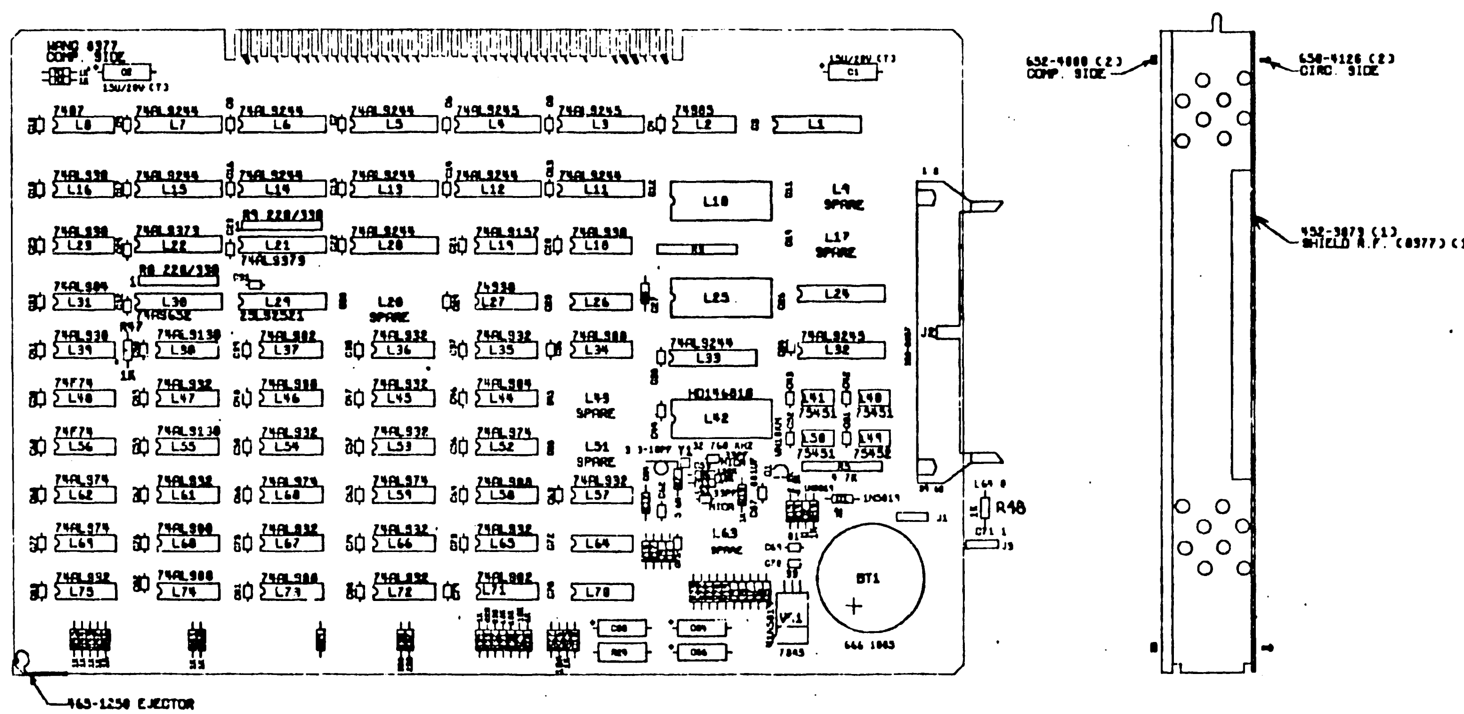
MODEL NO: VS 300

TITLE: PC/L.V.S INTERFACE

SEE CHART | D | 8371 | 3

D 8371

DO NOT SCALE



NOTES: UNLESS OTHERWISE SPECIFIED

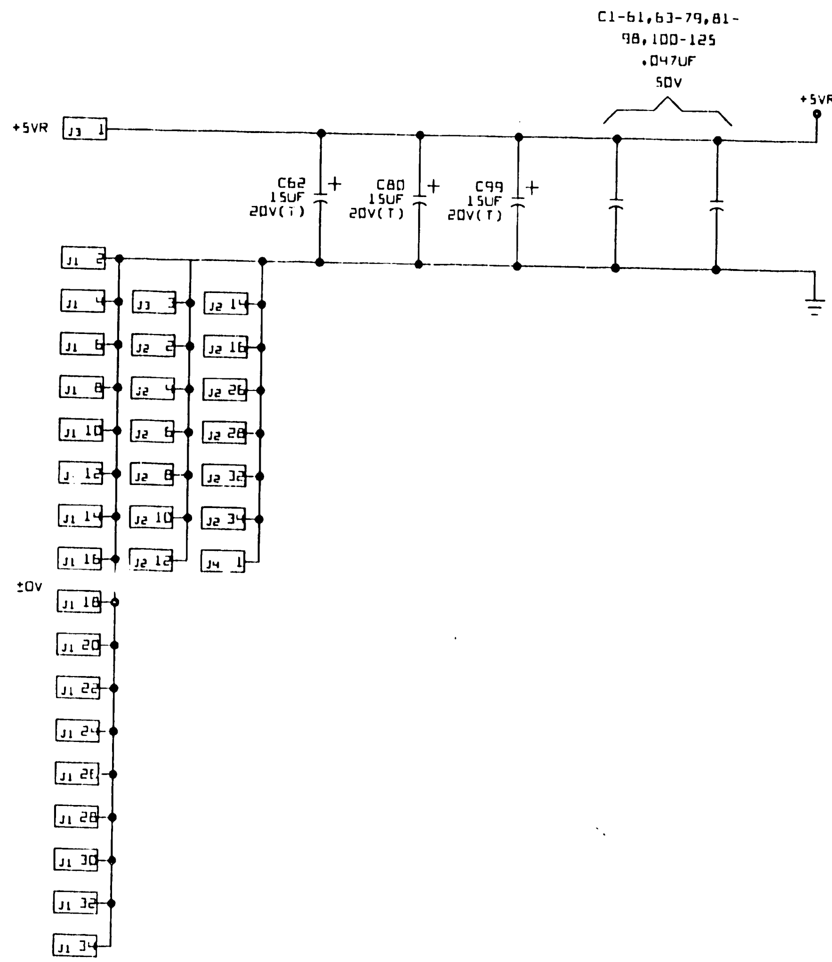
1. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W 5 PERCENT EXPRESSED IN OHMS.
3. C62,C84,C85,C86,D3,D4,D6,D7,D8,D9,D10, L1,L24,L26, L10,L25,L64,L70,R3,R4,R12,R17,R18,R19,R20, R21,R22,R23,R24,R27,R39. COMPONENTS WILL BE LOADED ONLEY IF NON VOLITILE RAM IS USED.
4. VR1 ADD INSULATOR (375-9034),SCREW (650-2120),NUT (652-2005).
5. LOAD 2 POS. SHUNT (350-4506) AT J3.

WANG LABORATORIES, INC. LOWELL, MASS U.S.A.	BY	DATE	APPROVED BY
	DWN J. BOZEMAN	5/84	E ENGR
	CHK		M ENGR
			MFG ENGR
MATERIAL	MODEL NO. VS-300	TITLE	ASSEMBLY DRAWING PC/L V. S INTERFACE
	NO. 18-219		
FINISH		210-8377	D 8377 2
	SCALE 1:1	WANG PART NUMBER	SIZE / DRAWING NUMBER / REV

THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC.

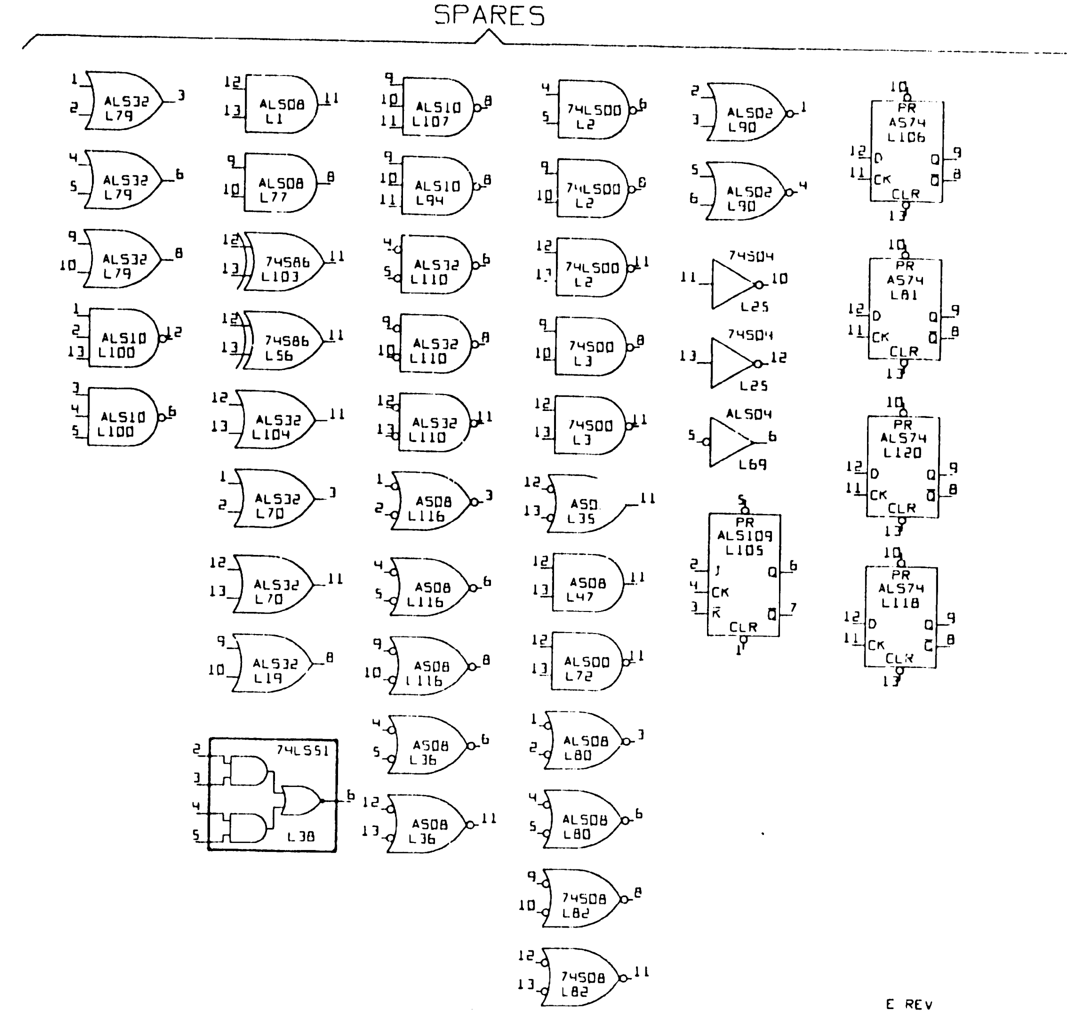
NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.
4. PARTS LIST APPEARS ON SHEET 7.



MNEMONICS	COORD
ALE	6G6
CABPBIT	6A4
CABPERR	6A4
CRASH	6C1
CTLRPBIT	6G6
CTS	2C11
DAMATCH	6A1
DCDI	5F11
DCDI	6B1
DCD2	5F11
DSR	2C11
DTR	2A4
ENDDHARD	6G5
EOR	6B1
EOT	6C1
INIT	6G6
IORD	6G6
IOWR	5G7
MEMRD	6C1
MEMWR	6C1
MCS0-MCS2	2A5
ON/OFF	6G6
RESETTFC	2A7
RTS	3A11
RXC	5F11
RXERR	5B1
RXSD	5F11
SPARE1	6C6
SPARE2	6A4
SPARE3	6A4
TFC	2C11
TRI0-TRI7	6F1
TXC	4E11
TXNRZI	4E1

SPARES



E REV 2 N

JSW 6-18-84 — 0 ORIGINATED PER DWR NO. E2236 APPR:
KTH 02-19-85 — 1 REVISED PER ECO NO. 35241D CHKR:
R.B.P. 04-24-85 — 2 REVISED PER ECO NO. 36061D CHKR:

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

SCHEMATIC DIAGRAM

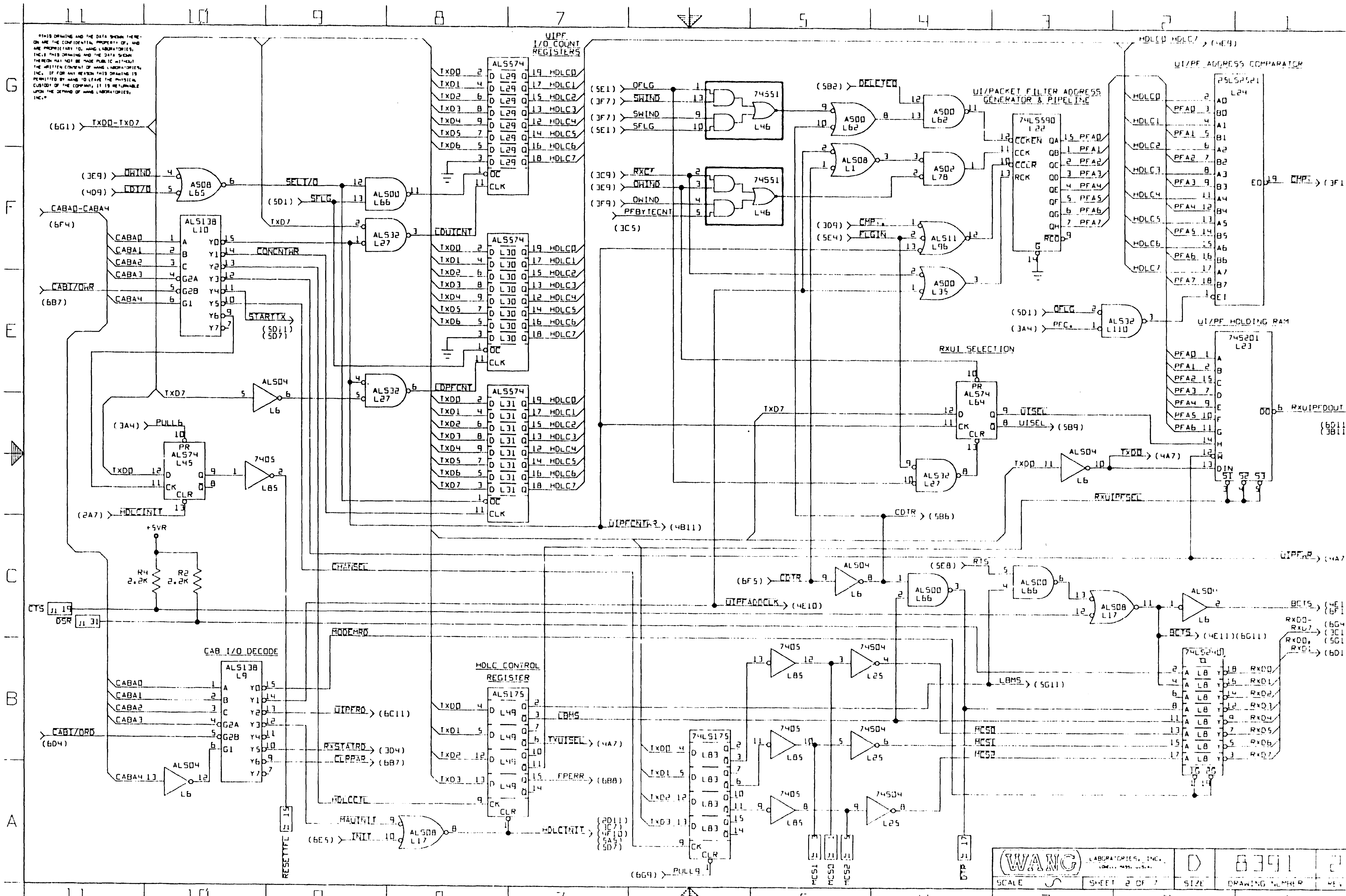
TITLE CONTENTION ACCESS BD M/L

MODEL NUMBER 911A | WANG PART NUMBER 210-8391

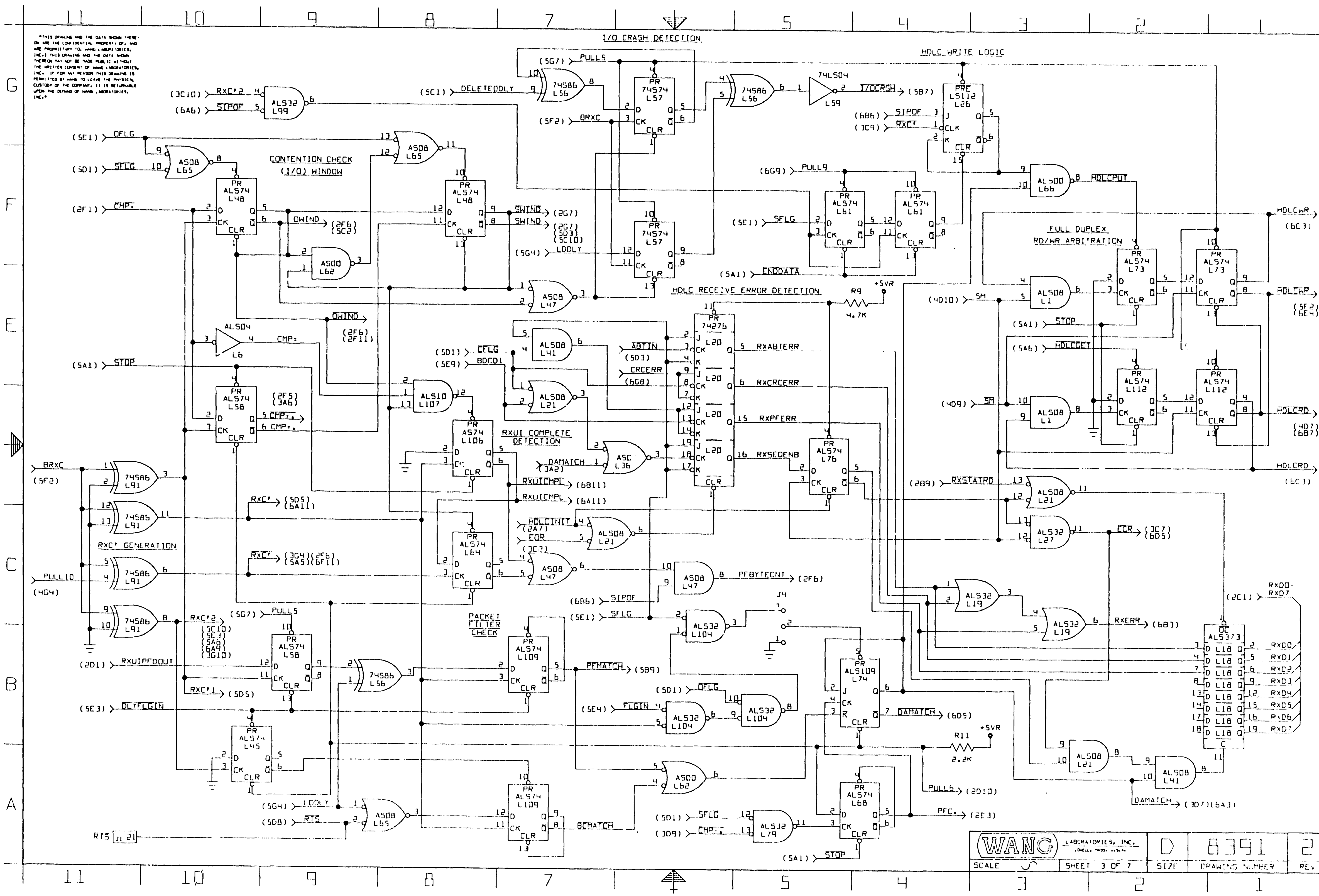
DWN JSW | CHK | ENG PB | DIR

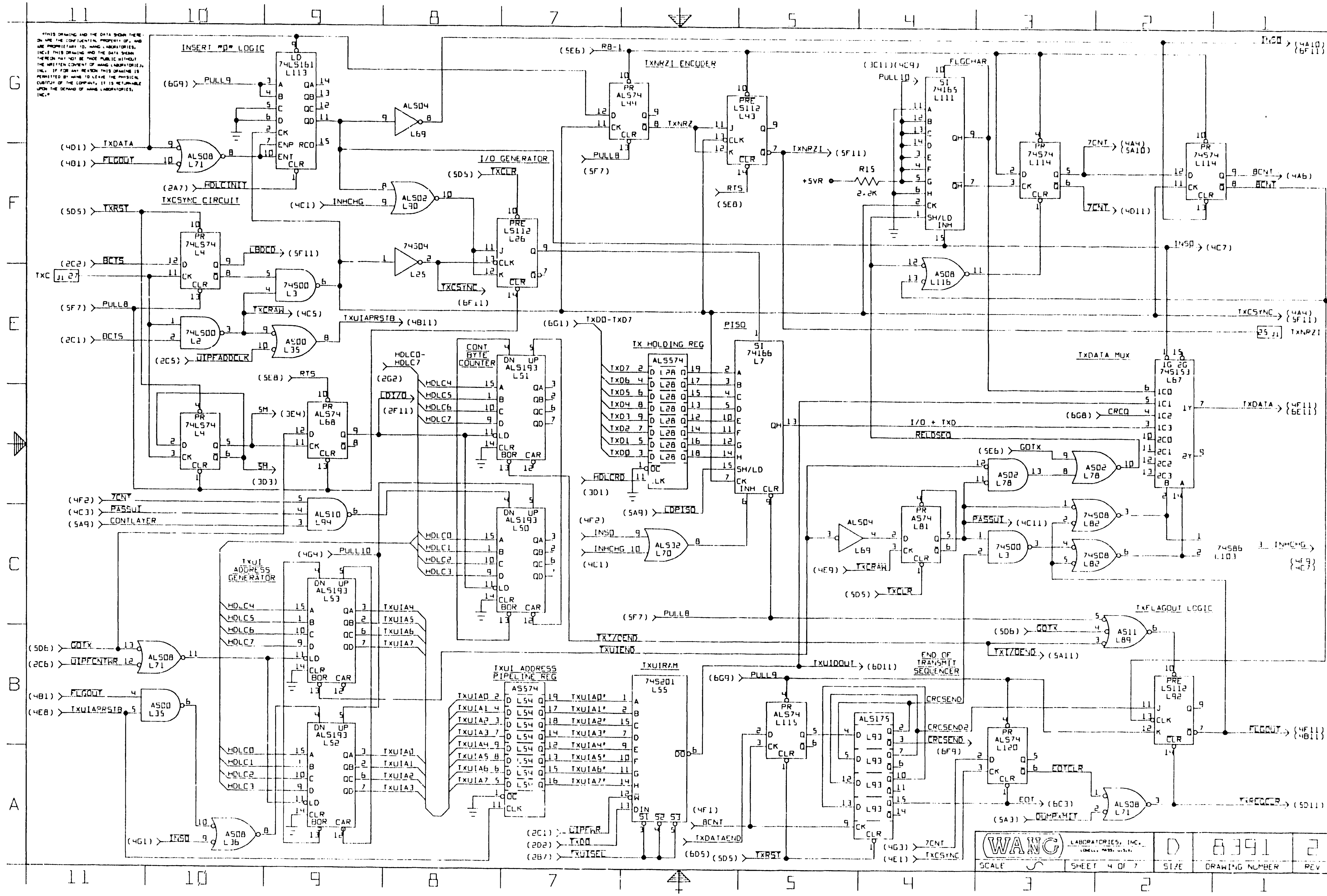
SIZE D | DRAWING NUMBER 8391 | REV 2

SCALE | SHEET 1 OF 7

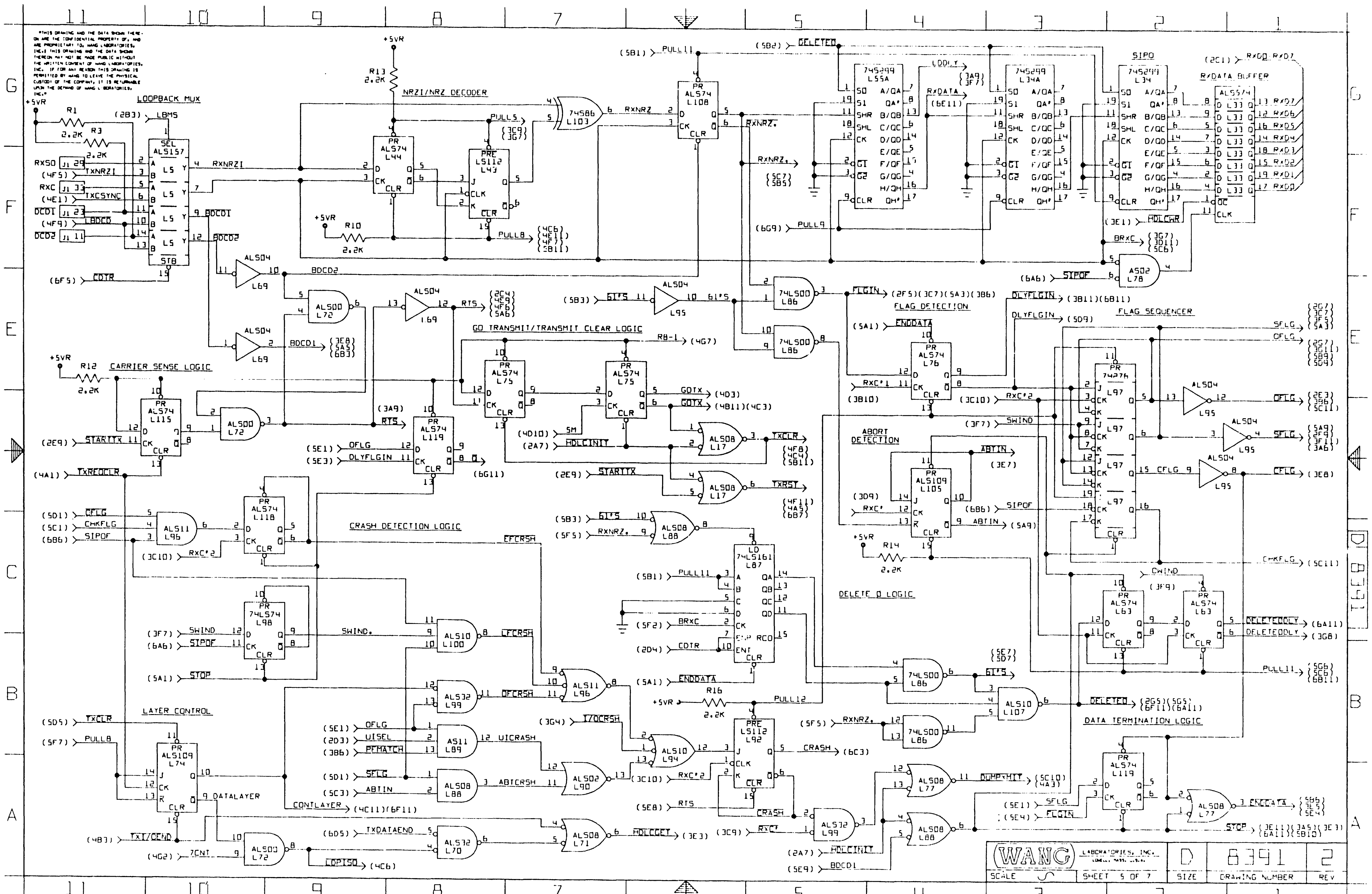


UIPF I/O COUNT REGISTERS
UI/PF ADDRESS COMPARATOR
UI/PACKET FILTER ADDRESS GENERATOR & PIPELINE
UI/PF HOLDING RAM
RXUI SELECTION
CAB I/O DECODE
HDLC CONTROL REGISTER
WANG LABORATORIES, INC.
SCALE
SHEET 2 OF 7
SIZE D
DRAWING NUMBER 6391
REV.

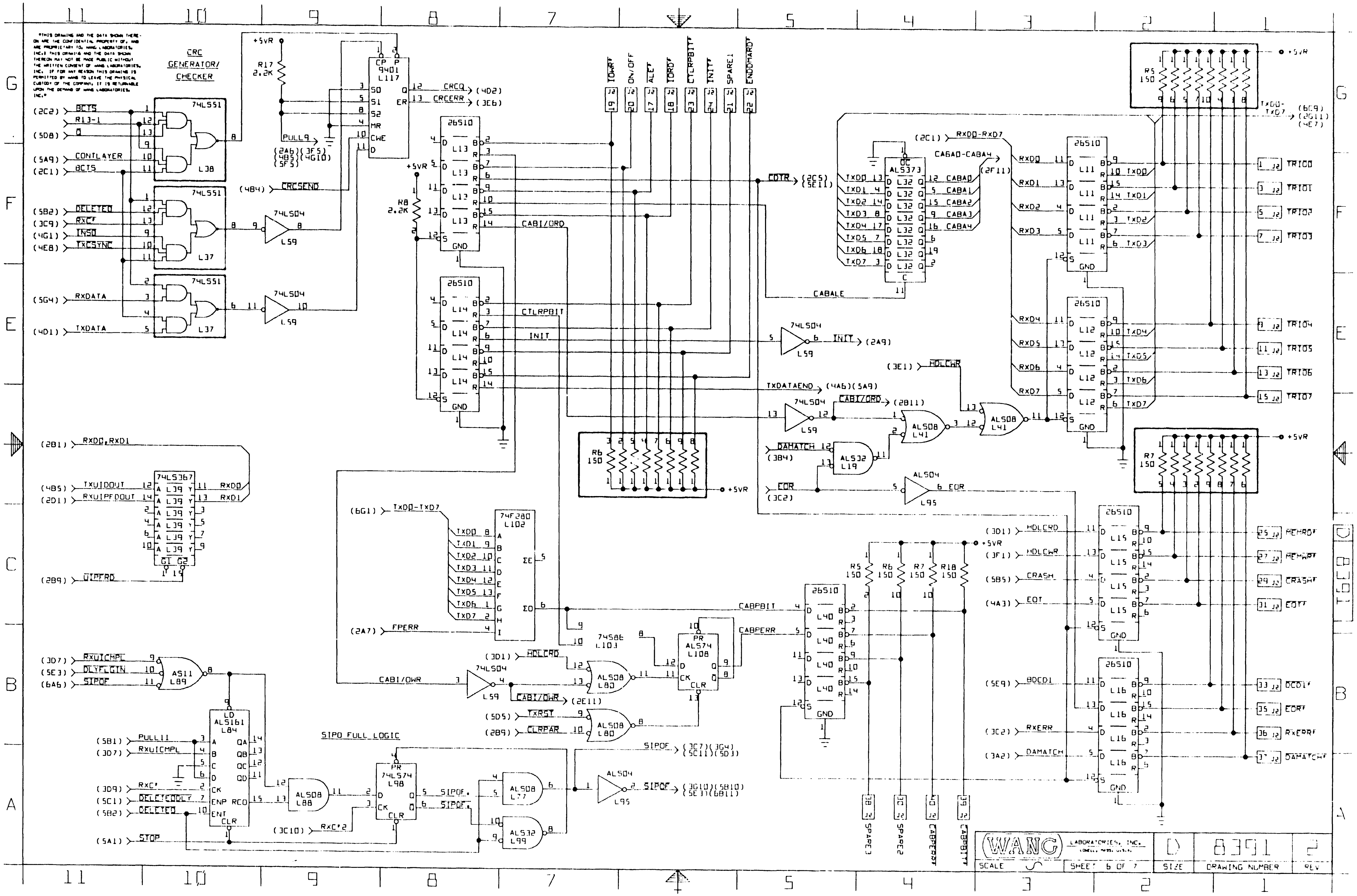

I/O CRASH DETECTION
HDLC WRITE LOGIC
CONTENTION CHECK (I/O) WINDOW
FULL DUPLEX RD/WR ARBITRATION
HDLC RECEIVE ERROR DETECTION
RXUI COMPLETE DETECTION
RXC* GENERATION
PACKET FILTER CHECK
WANG LABORATORIES, INC.
D
8391
2
SCALE
SHEET 3 OF 7
SIZE
DRAWING NUMBER
RL.



INSERT "0" LOGIC
TXNRZI ENCODER
I/O GENERATOR
TXCSYNC CIRCUIT
CONT BYTE COUNTER
TX HOLDING REG
PISO
TXDATA MUX
TXUI ADDRESS GENERATOR
TXUI ADDRESS PIPELINE REG
TXUIRAM
END OF TRANSMIT SEQUENCER
TXFLAGOUT LOGIC
WANG LABORATORIES, INC.
SCALE
SHEET 4 OF 7
SIZE D
DRAWING NUMBER 8391
REV 2

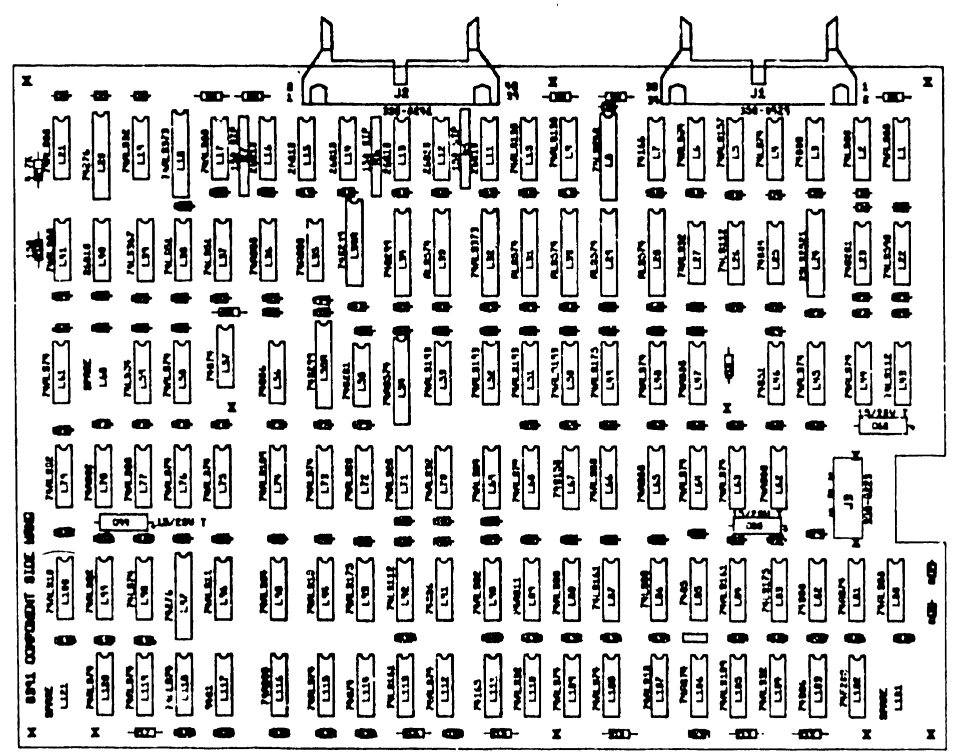


LOOPBACK MUX
NRZI/NRZ DECODER
SIPO
RxDATA BUFFER
CARRIER SENSE LOGIC
GO TRANSMIT/TRANSMIT CLEAR LOGIC
FLAG DETECTION
FLAG SEQUENCER
ABORT DETECTION
CRASH DETECTION LOGIC
DELETE 0 LOGIC
LAYER CONTROL
DATA TERMINATION LOGIC
WANG LABORATORIES, INC.
SCALE
SHEET 5 OF 7
D
SIZE
6391
DRAWING NUMBER
2
REV



CRC GENERATOR/CHECKER
SIPO FULL LOGIC
WANG LABORATORIES, INC.
SCALE
SHEET 6 OF 7
SIZE D
DRAWING NUMBER 8391
REV 2

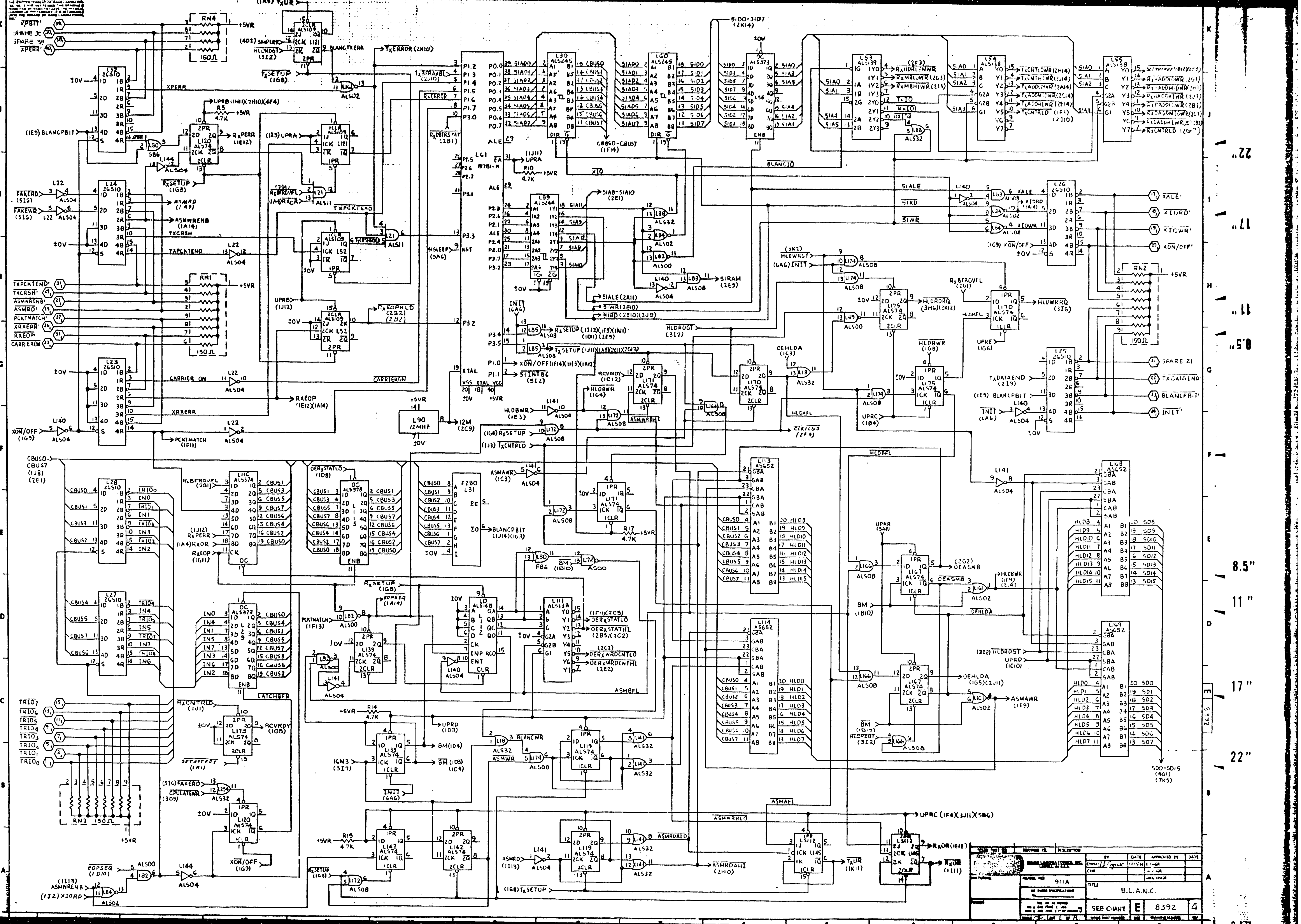
DO NOT SCALE

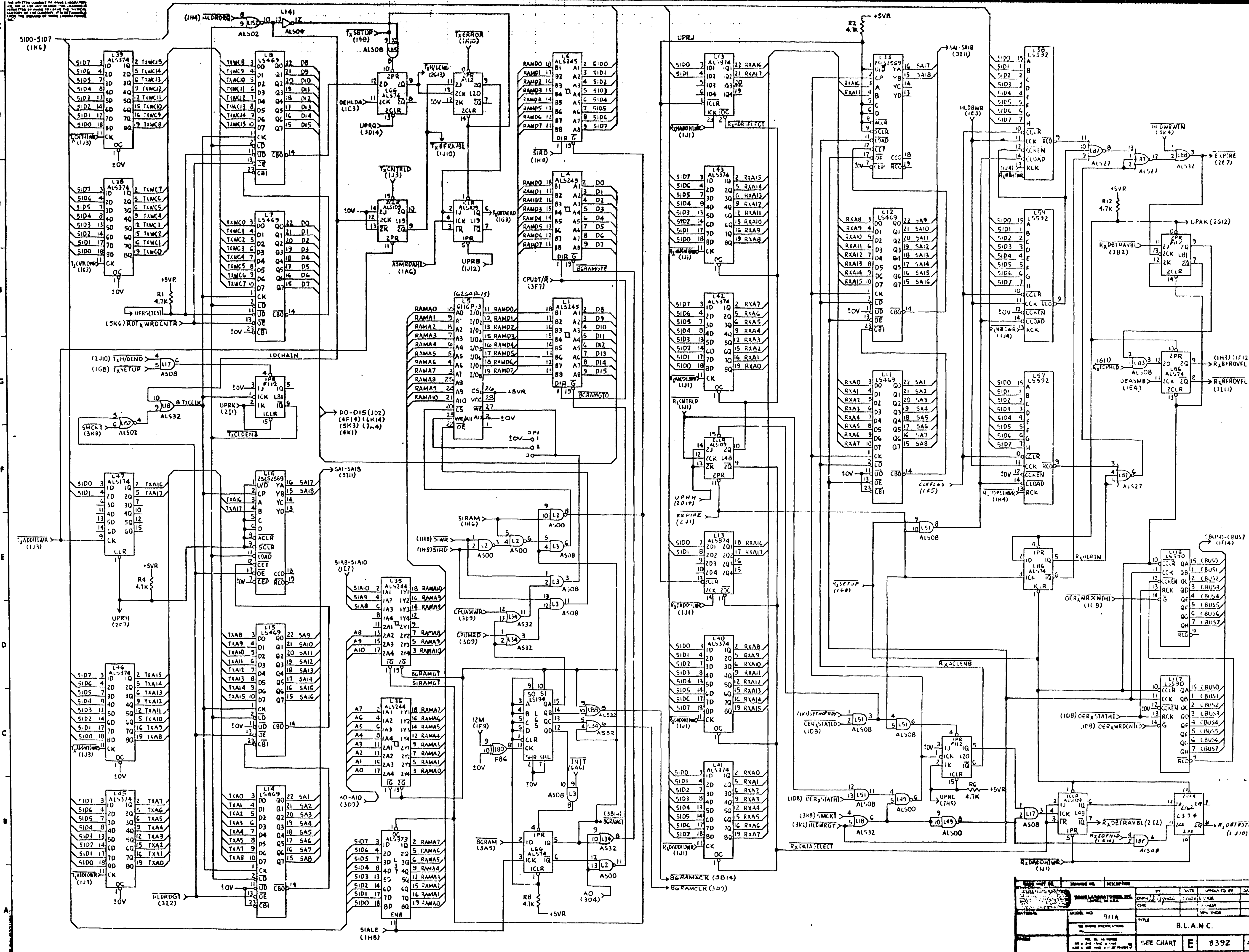


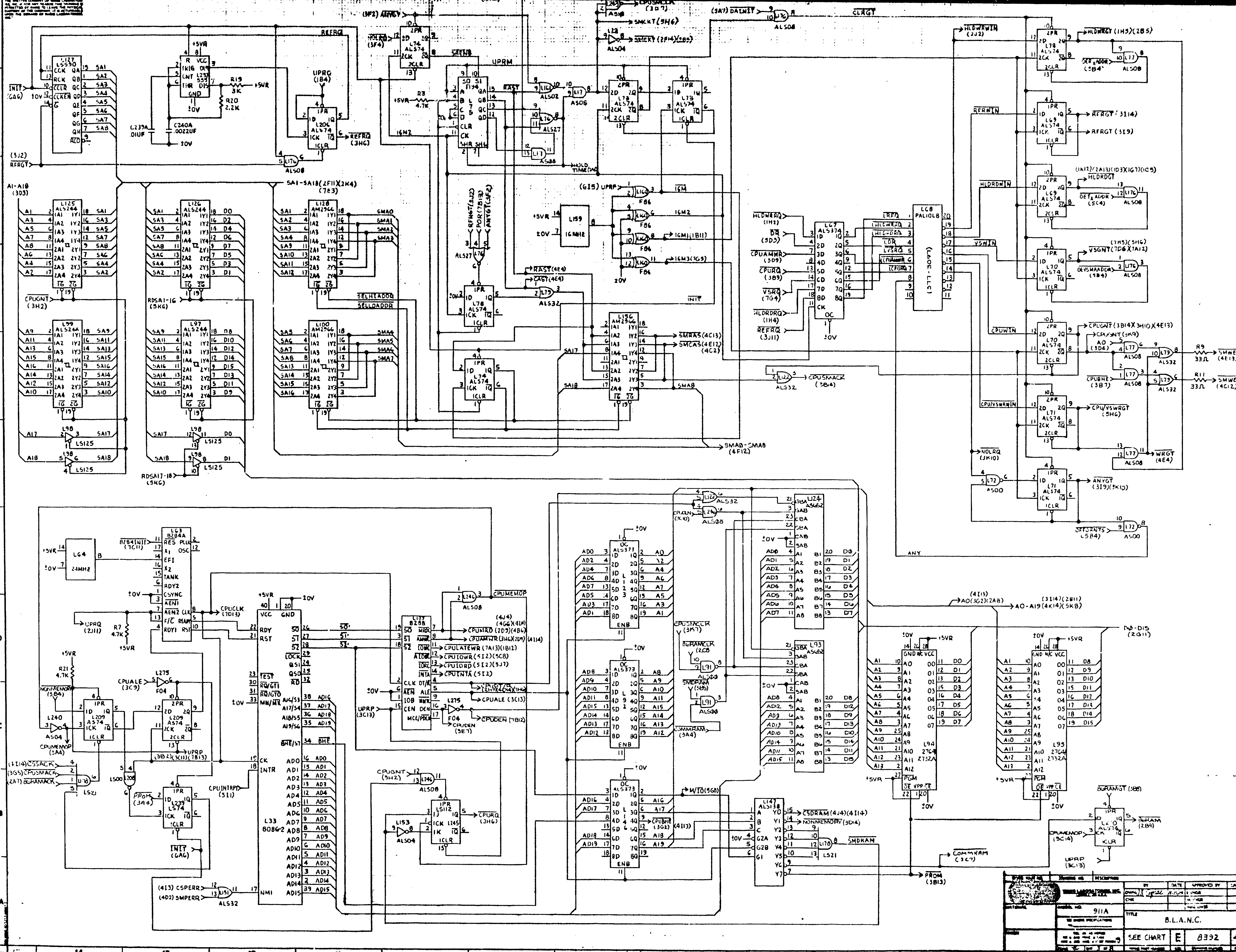
NOTES: UNLESS OTHERWISE SPECIFIED

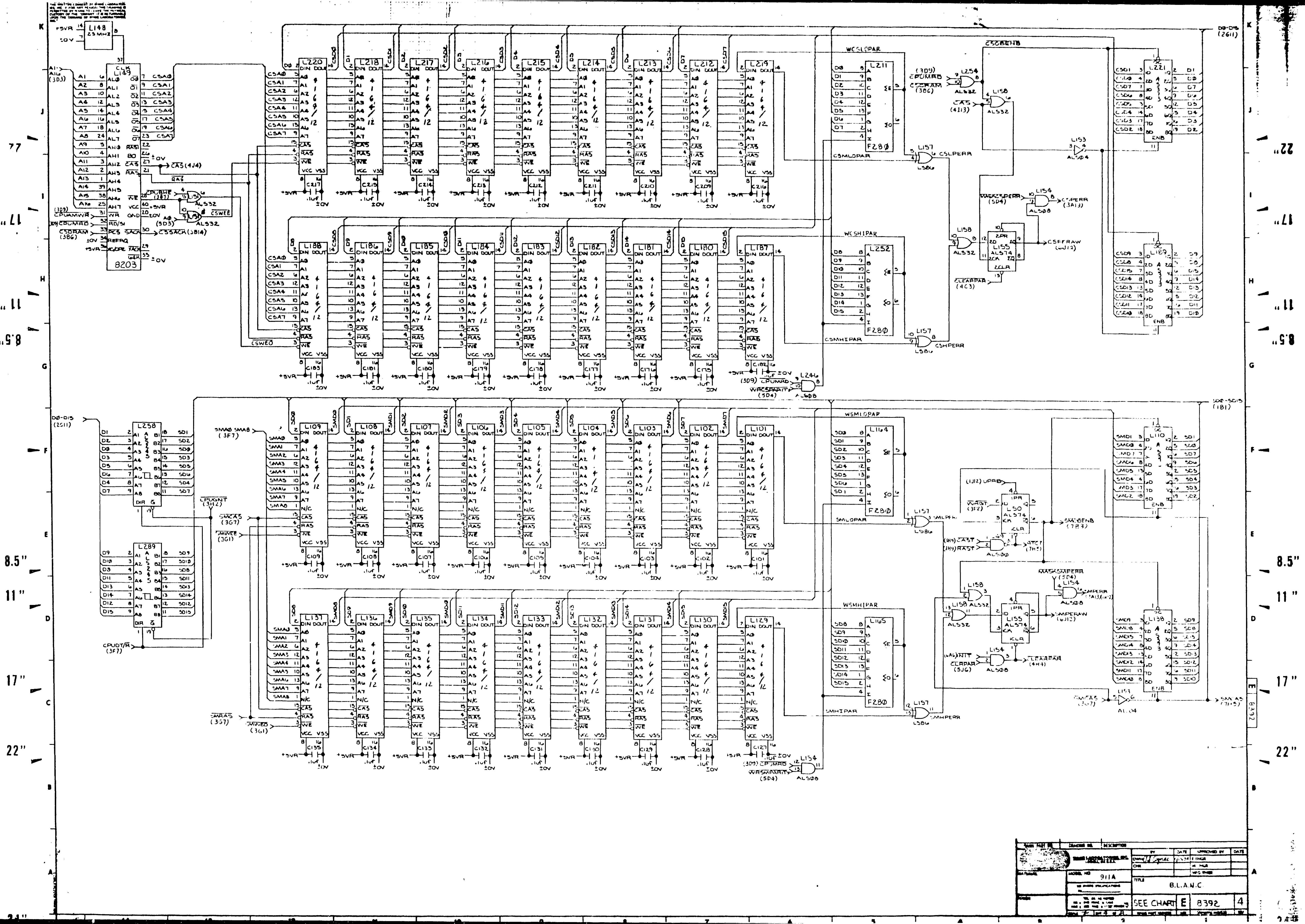
1. ALL RESISTORS ARE 2.2K 1/4W 5 PERCENT EXPRESSED IN OHMS.
2. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
3. SIPS ORIENTED WITH PIN 1 AT TOP

WANG LABORATORIES, INC. LOWELL, MASS U.S.A.	BY	DATE	APPROVED BY
	DWN J RIDON	2/85	E CHGR
	CHK		M CHGR
			MFG CHGR
MODEL NO. 911A	TITLE ASSEMBLY DRAWING CONTENTION ACCESS BOARD M/L		
210-8391	D	8391	3
SCALE 1:1			

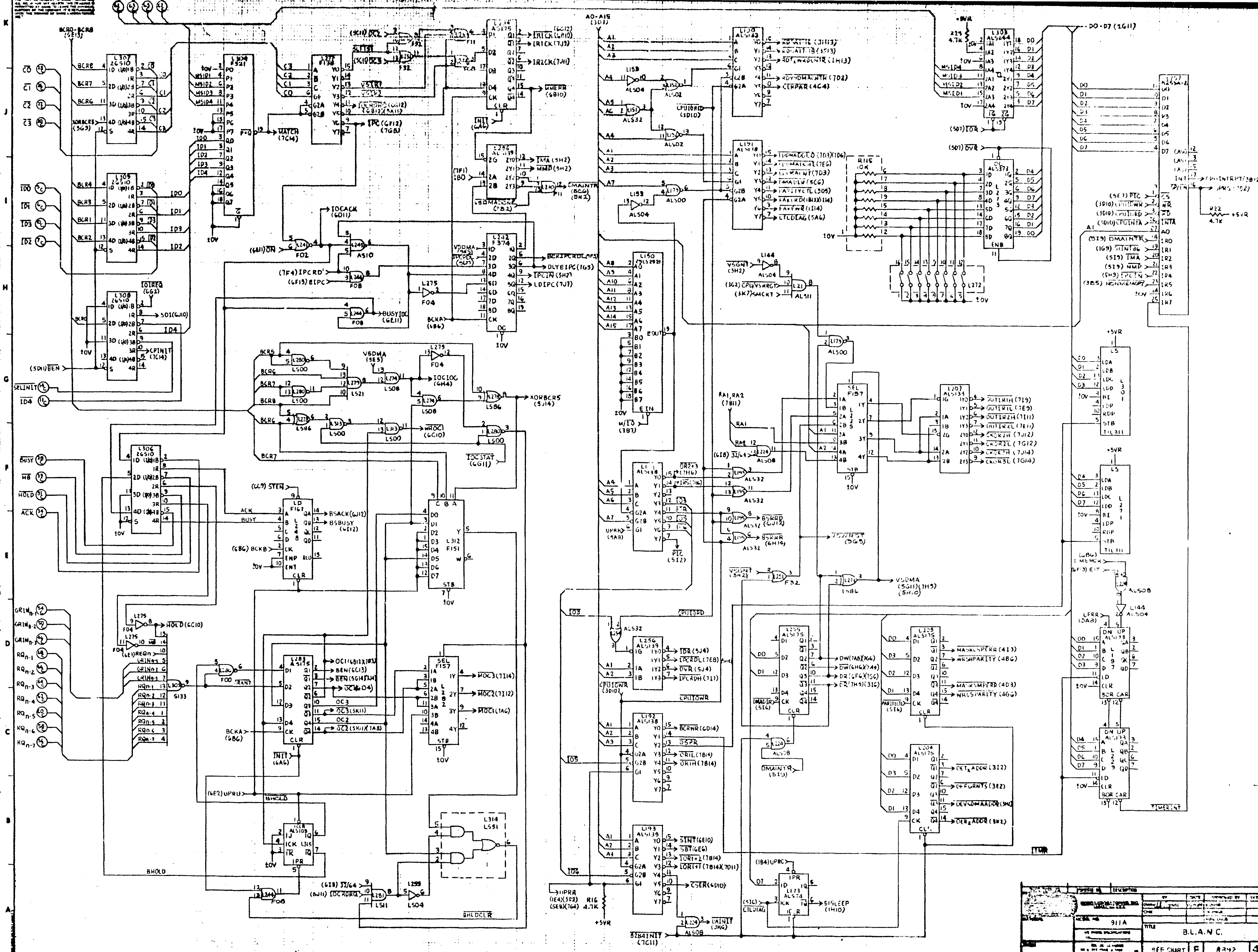

B.L.A.N.C.
911A
SEE CHART
E
8392
4

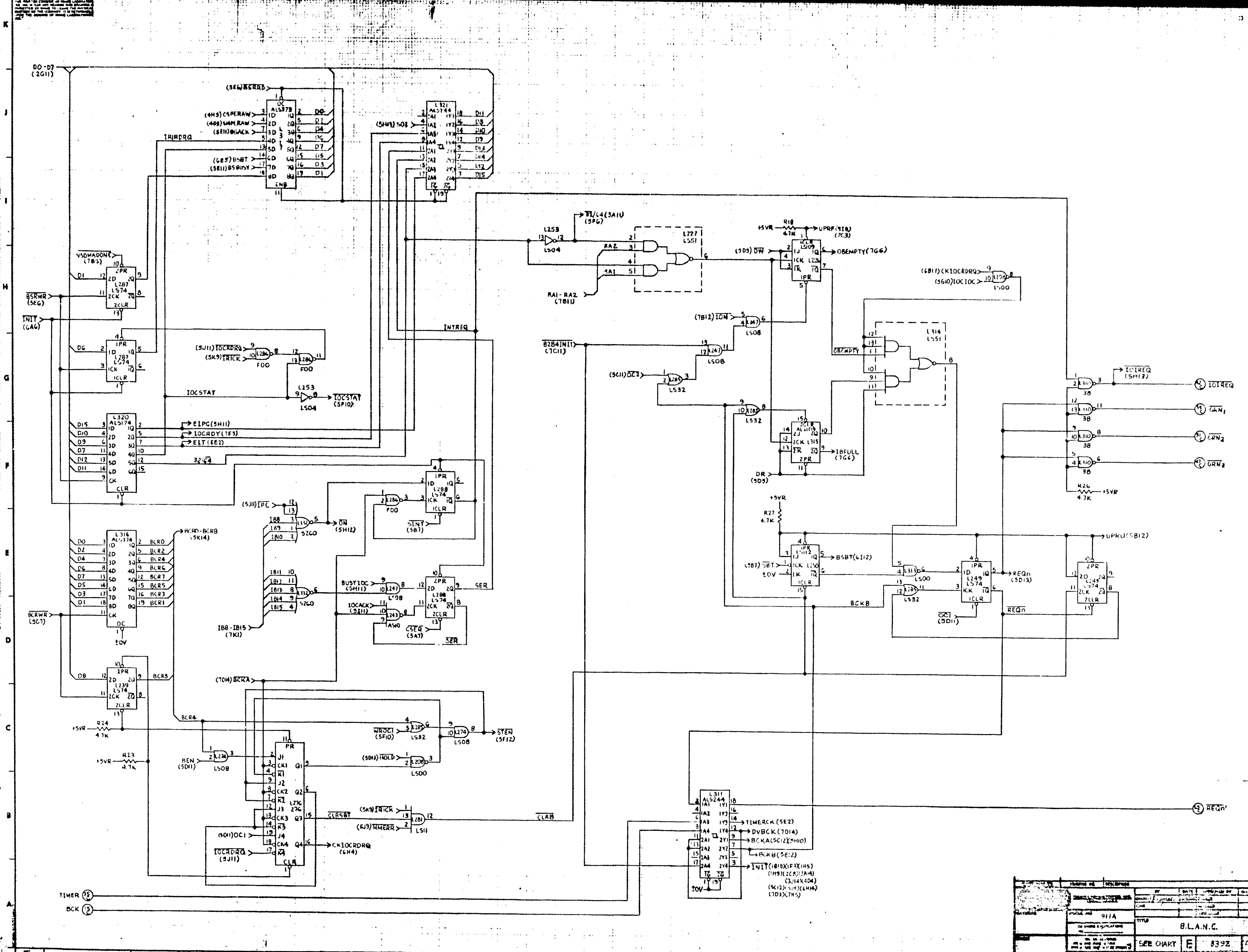

911A
B.L.A.N.C.
SEE CHART
E
8392
4

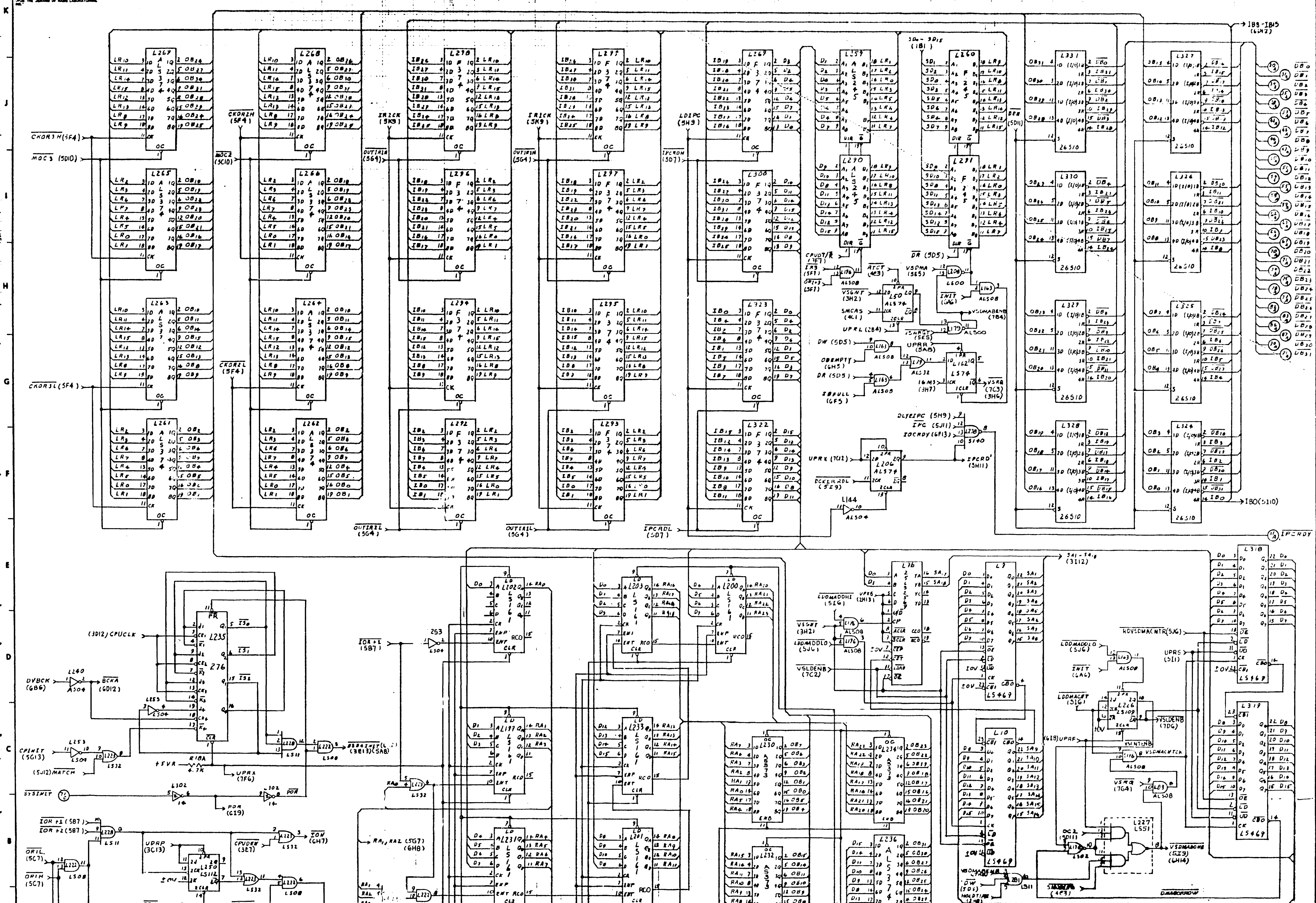

911A
B.L.A.N.C.
SEE CHART
E
8392
4



8203
WCSLOPAR
WCSHIPAR
WSMLOPAR
WSMHIPAR
CSLPERR
CSHPERR
SMLOPAR
SMHIPAR
SMHPERR
CLEARPAR
F280
ALS32
ALS08
ALS74
911A
B.L.A.N.C
SEE CHART
E
8392
4


911A
B.L.A.N.C.
SEE CHART
E
8392
4

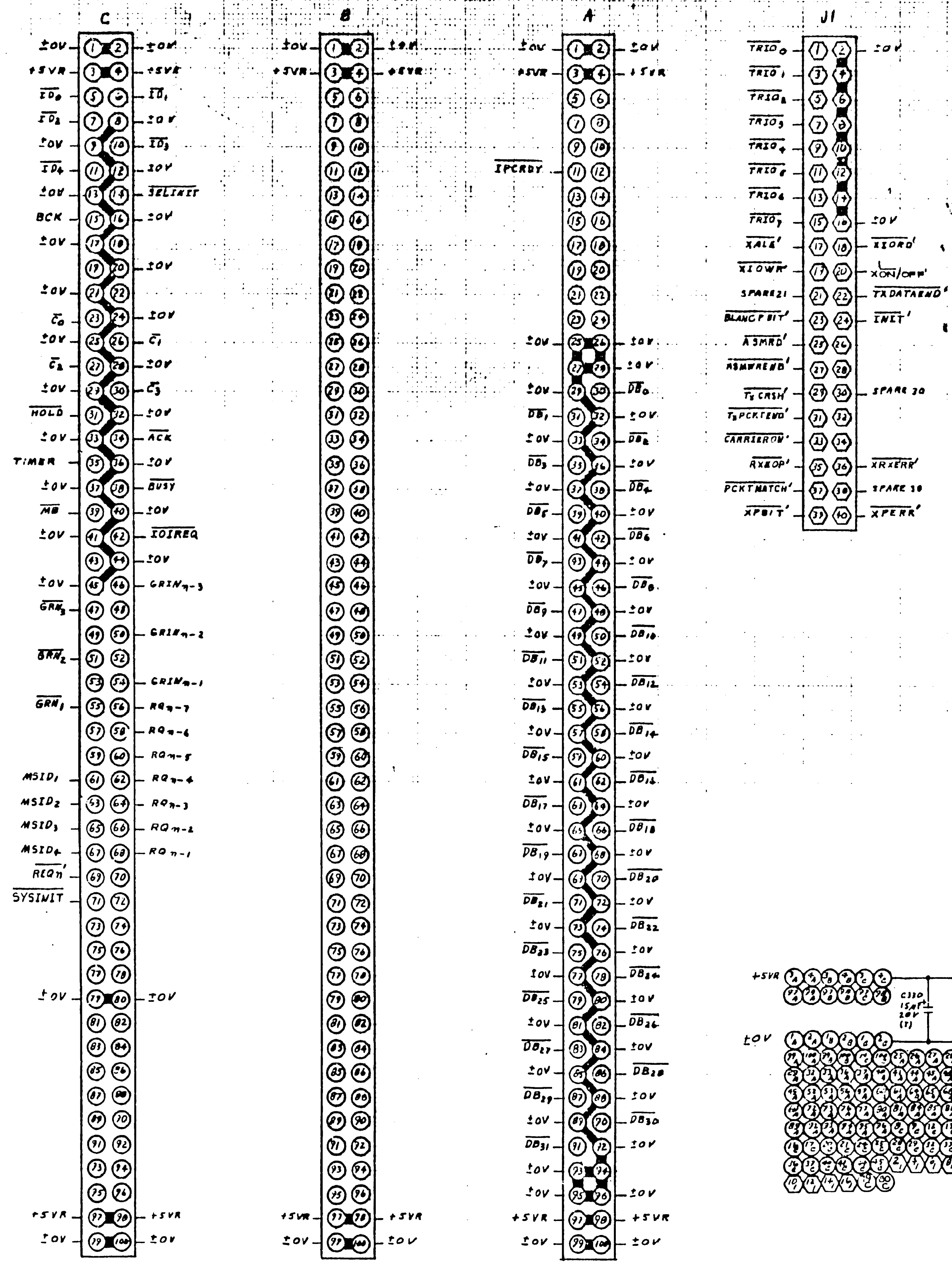

D0-D7 (2G11)
(5E6) BCRRD
ALS373
(4H3) CSPERAW
(4D8) SMPLRAW
(6E11) BSACK
IBIRDRQ
(6E5) BSBT
(5E11) BSBUSY
ENB
L321 ALS244
(5H13) SOB
VSDMADONE (7B5)
BSRWR (5E6)
INIT (6A6)
L287 LS74
IOCSTAT
L253 LS04
IOCSTAT (5F10)
(5J11) IOCRDRQ
(5K9) TRICK
L320 ALS174
EIPG (5H11)
IOCRDY (7F5)
ELT (5E2)
INTREQ
L316 ALS374
BCR0-BCR8 (5K14)
BCRWR (5C7)
L239 LS74
(5J11) IPC
ON (5H12)
IB8-IB15 (7K1)
BUSYIOC (5H11)
IOCACK (5J11)
CSEQ (5A7)
SER
(7D14) BCKA
BCR4
WRQCI (5F10)
L274 LS08
STEN (5F12)
BEN (5D11)
(5D13) HOLD
LS00
(5K9) TRICK
(6J9) MMERR
CLRSBT
CLRB
LS11
(5D11) OC1
IOCRDRQ (5J11)
CKIOCRDRQ (6H4)
TIMER
BCK
T1/C4 (5A11) (5F6)
L227 LS51
RA2
RA1
RA1-RA2 (7B11)
(5D5) DW
R18 4.7K
UPRF (9I8) (7C3)
L309
OBEMPTY (7G6)
(6B11) CKIOCRDRQ
(5G10) IOCIOC
LS00
(7B12) ION
LS08
8284 INIT (7C11)
L314 LS51
OBEMPTY
(5C11) OC2
LS32
IBFULL (7G6)
DR (5D5)
R27 4.7K
BSBT (6I12)
(5B7) SBT
L250
L313 LS00
L249 LS74
REQn (5D13)
OC1 (5D11)
BCKB
REQn
UPRU (5B12)
IOIREQ (5H13)
IOIREQ
GRN1
GRN2
GRN3
R26 4.7K
+5VR
R24 4.7K
R23 4.7K
L311 ALS244
TIMERCK (5E2)
DVBCK (7D14)
BCKA (5C12)(5H10)
BCKB (5E12)
INIT (1B10)(1F3)(1H5) (1H9)(2C8)(3A4) (3J14)(4D4) (5C12)(5J4)(6H4) (7D3)(7H5)
REQn'
911A
B.L.A.N.C.
SEE CHART
E
8392
14



911A

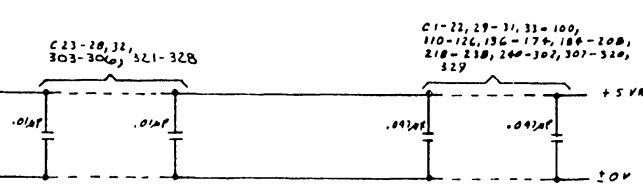
B.L.A.N.C

SEE CHART E 8392 4



IC TYPE	LOC.	SPARES
SPARES	L62	
74LS00	L313	1
74LS21	L279	1
74LS112	L245	1
74ALS00	L91	2
74S140	L238	1
74ALS00	L179	1
74F02	L241	3
74LS02	L178	3
74ALS04	L144	1
	L153	1
74F86	L80	1
74S04	L240	4
74ALS08	L85	1
74ALS74	L270	1
7414	L302	4
74ALS32	L254	1
	L122	2
74F32	L231	1
74AS00	L72	1
74ALS21	L76	1
74F08	L244	3
74LS74	L162	1

MNEMONICS	COORD
ACK	5E14
ASMRD'	1H14
ASMWRENB'	1H14
BCK	6A14
BLANC P BIT'	1G1
BUSY	5F14
CARRIER ON'	1G14
$C_0 - C_3$	5J14
$DB_0 - DB_{31}$	7J1
$GRN_1 - GRN_3$	6F1
$GRIN_{n-1}$, $GRIN_{n-3}$	5D14
HOLD	5F14
ID4	5G14
$ID_0 - ID_3$	5I14
IOIREQ	6G1
INIT'	1F1
IPCRDY	7E1
MB	5F14
$MSID_1 - MSID_4$	5K13
PCKTMATCH'	1H14
REQn'	6A6
$RQ_{n-1} - RQ_{n-7}$	5D14
RXEOP'	1G14
SELINIT	5G14
SPARE 21	1G1
SPARE 30	1K14
SPARE 38	1K14
SYSINIT	7B14
TIMER	6A14
$TRIO_0 - TRIO_7$	1C14
TXCRSH'	1H14
TXDATAEND'	1G1
TXPCKTEND'	1H14
XALE'	1I1
XIORD'	1I1
XIOWR'	1I1
XON/OFF'	1H1
XPBIT'	1K14
XPERR'	1K14
XRXERR'	1G14

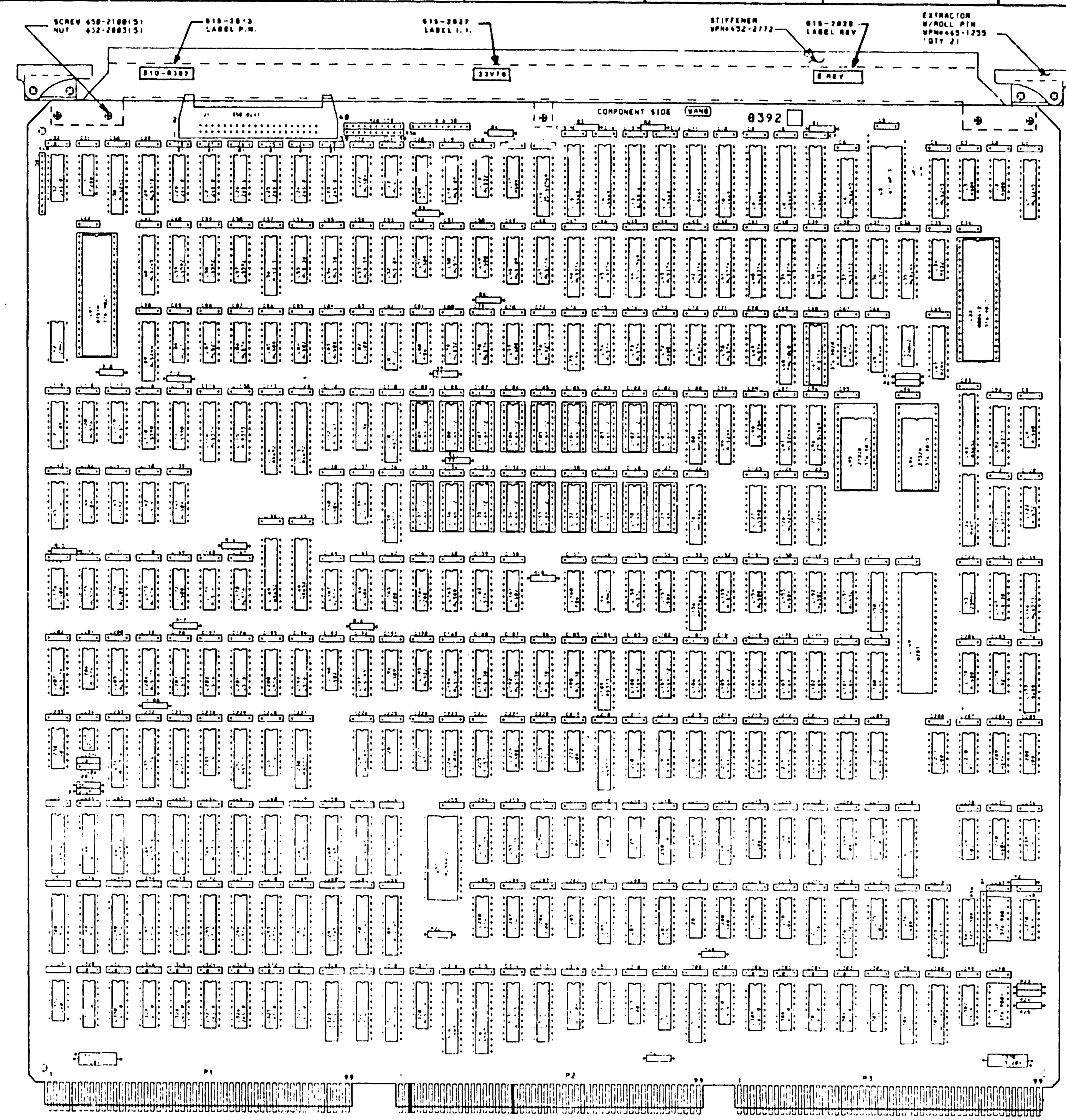


210 = 209 + 377 OR 378							
210	209	1.5	L101-109, 129-137,	L33	L68	L94, 95	L61
8392-A	8392		377-0417	377-0437	377-3097	377-C452	377-0512

NOTE:
1 ALL RESISTORS ARE 1/4W 5% UNLESS SPECIFIED OTHER WISE

E-REV 2

911A
B.L.AN.C
SEE CHART E 8392 4



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
2. ALL RESISTERS ARE 4.7K 1/4W 5% EXPRESSED IN OHMS.
3. WIRED JUMPER TO BE CONNECTED FROM JP1 PIN 2 TO JP1 PIN 3.
4. USE SOCKET 376-9877 FOR [illegible]

WANG

MATERIAL	MODEL NO. VS300	BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
	10-213	CHK		M ENGR	
FINISH		E C CONTROL		MFG ENGR	

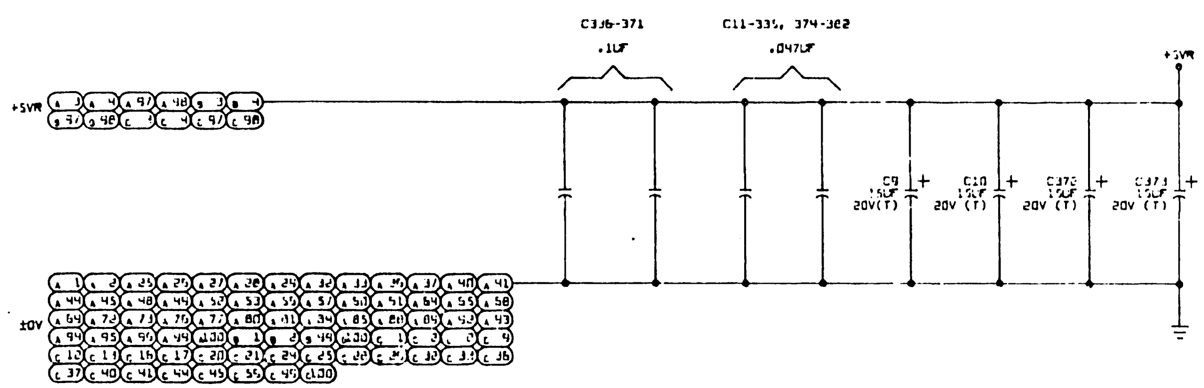
TITLE: INBOARD CPU (BLANC) ASSEMBLY DRAWING

210-8392 | C | 8392 | 4

NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.
4. CONNECTORS SHOWN ON SHEET 15.

MNEMONICS	COORD.
ACK	12A13
SCK	12E14
BCSY	12A13
C0-C3	12K1
CB0-CB3I	7J1
GRINN-1 - GRINN-3	12I14
GR0I-GR03	12A11
ROCD	12A12
TO0-TO4	12K1
INIT	4A14
TRCRDY	12A8
TOT/REQ	12F1
PTS	3C1
RUN-1 - RUN-7	12J14
ROD	12A11
SBTBCSY	12A10
SFLINIT	12F1
TIMER	12E14



IC TYPE	LOCATION	SPARES
74AS00	L357	2
74F00	L34	3
74LS00	L55	1
	L188	1
	L245	1
	L422	3
74AS02	L176	2
	L249	3
	L264	3
	L358	2
74LS02	L122	2
	L405	2
7403	L244	2
74AS04	L66	2
	L248	2
	L273	1
	L325	4
74F04	L37	5
74LS04	L52	1
	L57	2
	L76	2
	L123	4
	L175	1
7408	L120	2
74AS10	L189	1
	L266	1
74F08	L332	2
74LS08	L42	1
	L200	3
	L276	2
	L342	1
74AS10	L167	1
	L278	1
	L279	2
74LS10	L43	3
	L84	2
	L115	1
	L170	1
	L180	2
	L231	2
74LS11	L424	1
7414	L49	2
74LS20	L393	1
74AS27	L117	1
74LS27	L126	1
74AS32	L54	1
	L77	2
	L183	1
	L277	2
74F32	L320	2
74LS32	L209	1
	L229	3
	L265	1
	L376	1
7438	L395	1
	L423	3
74LS51	L259	1
74AS74	L171	1
74LS74	L402	1
	L406	1
74AS86	L205	3
	L250	3
74F86	L50	1
74LS86	L391	3
	L404	3
SPARES	L340	-
	L421	-

E REV 3 N

WANG LABORATORIES, INC.

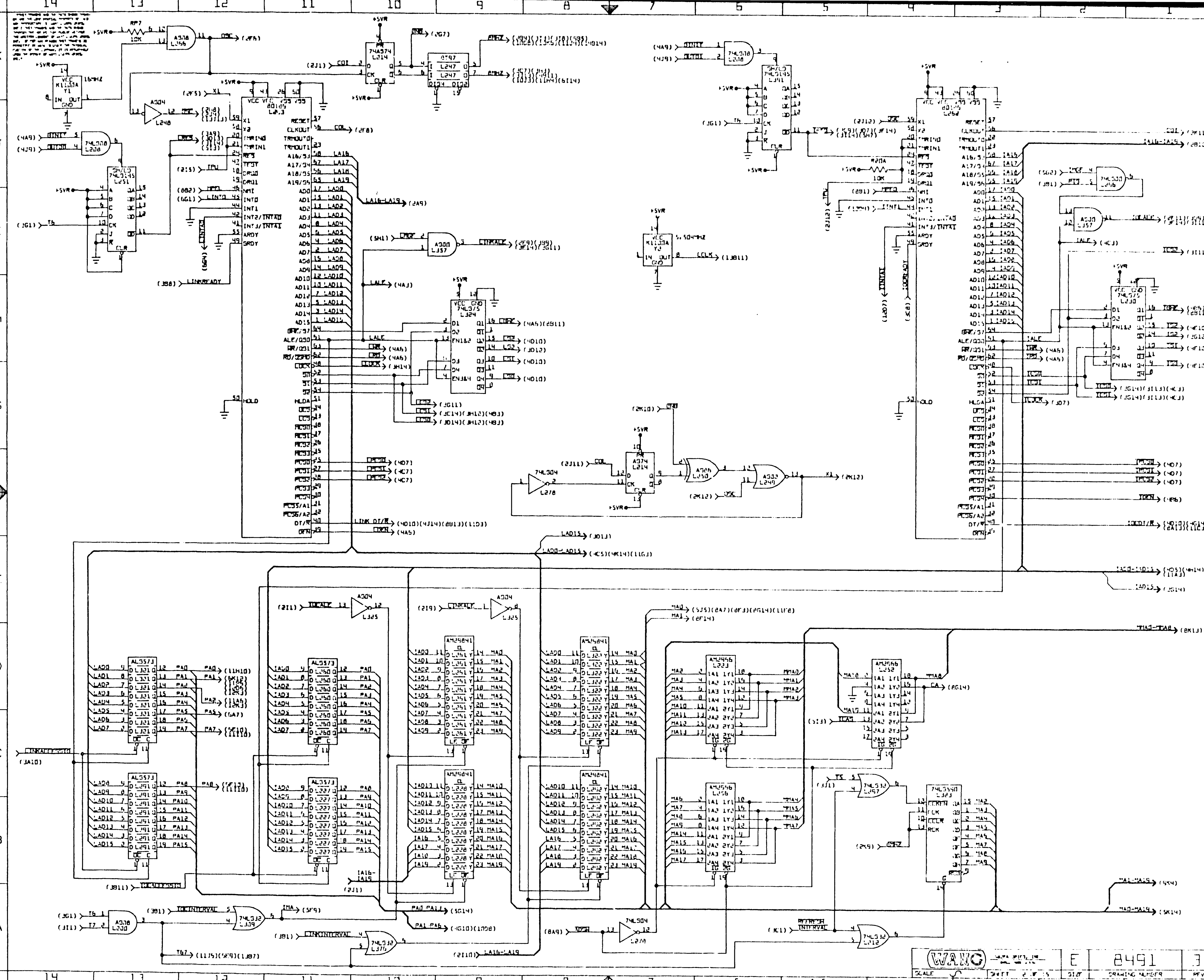
SCHEMATIC DIAGRAM

TITLE ML TC CONTRL BD TDC VS-300

MODEL NUMBER	WANG PART NUMBER	DWN CALMA	CHK J.C.	ENG F.H.	DIR
VS300	210-8491				

SIZE	DRAWING NUMBER	REV
E	8491	3

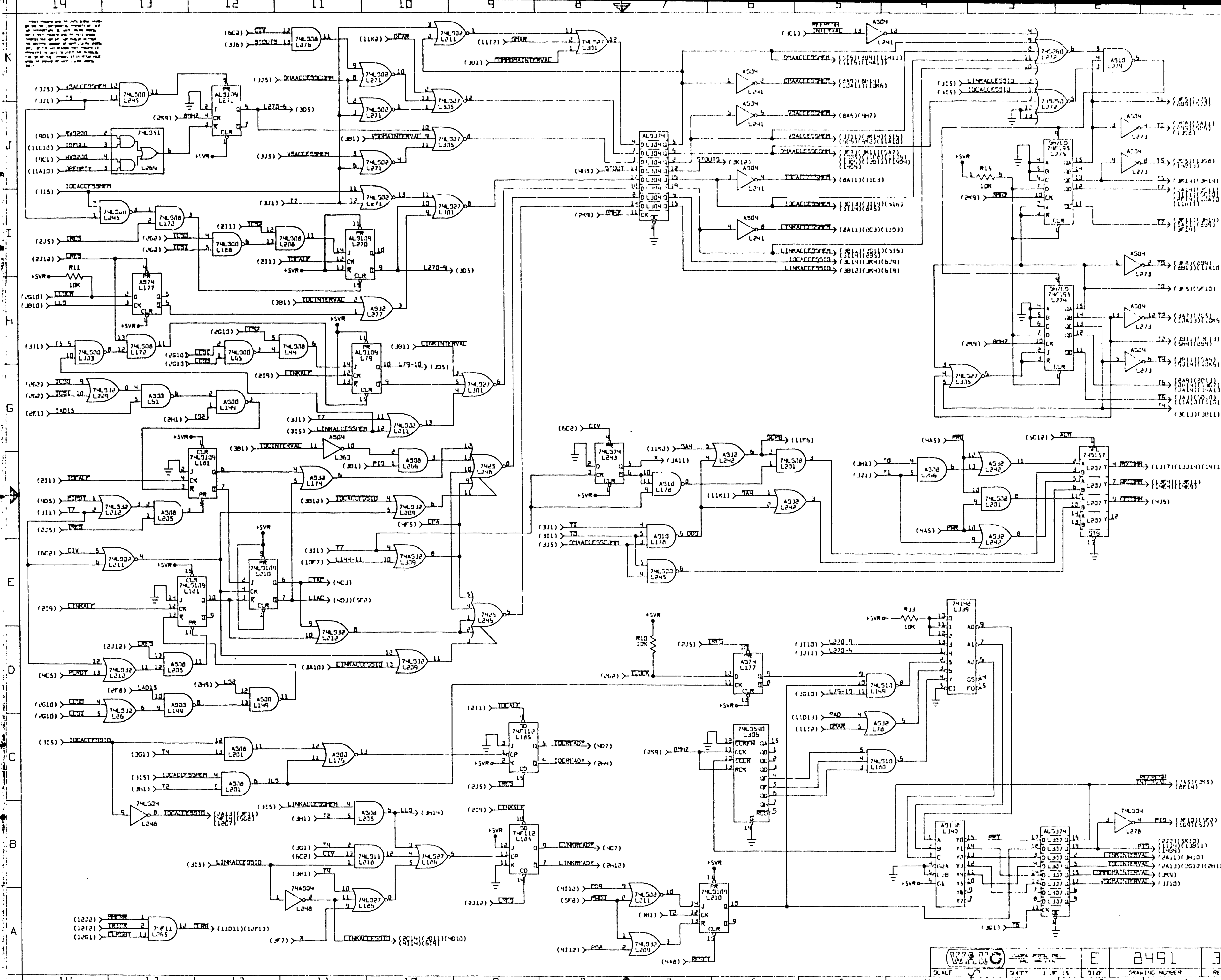
SCALE — SHEET 1 OF 15


WANG
E
8491
3

17"

11"

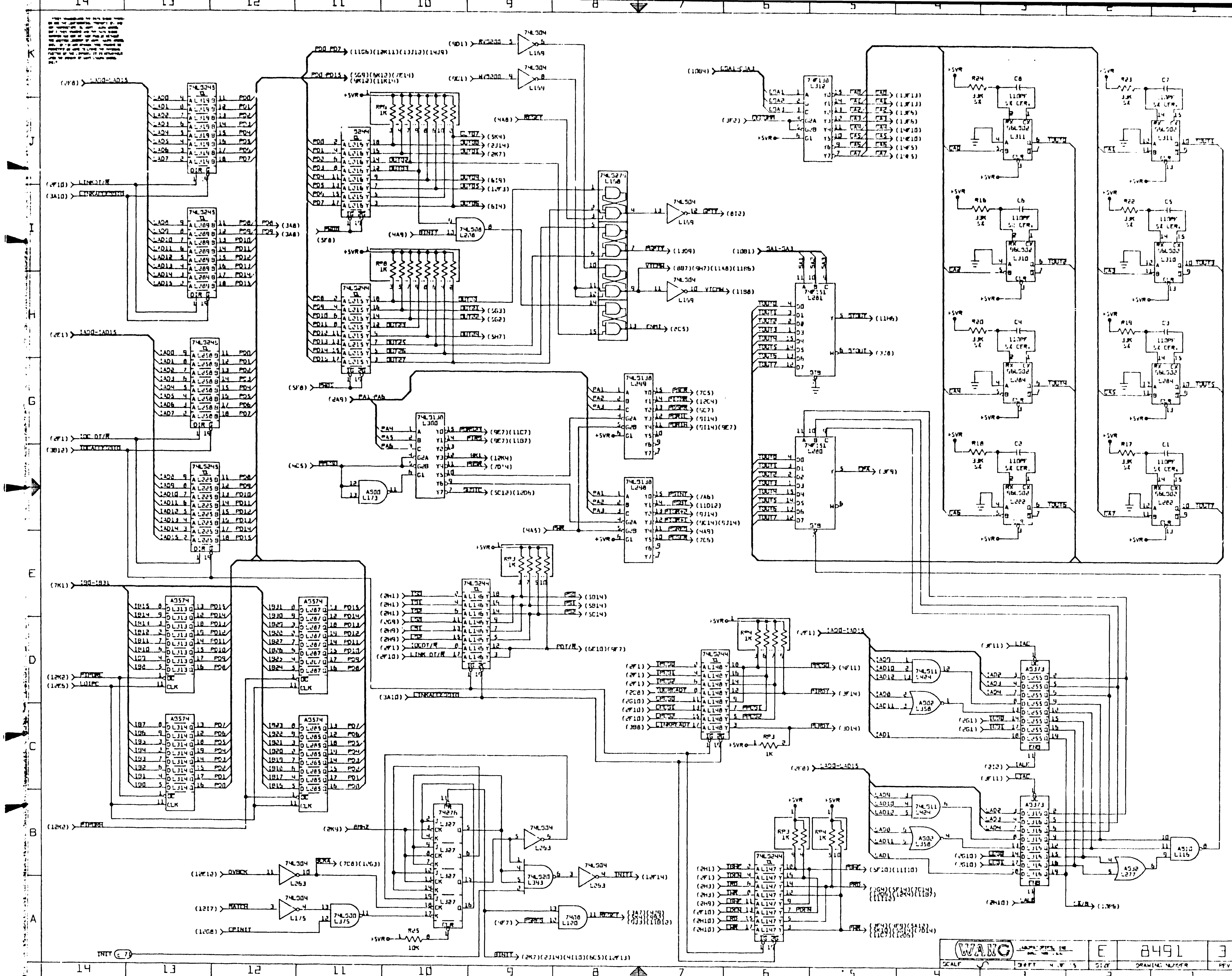
8.5"



8.5"

11"

17"

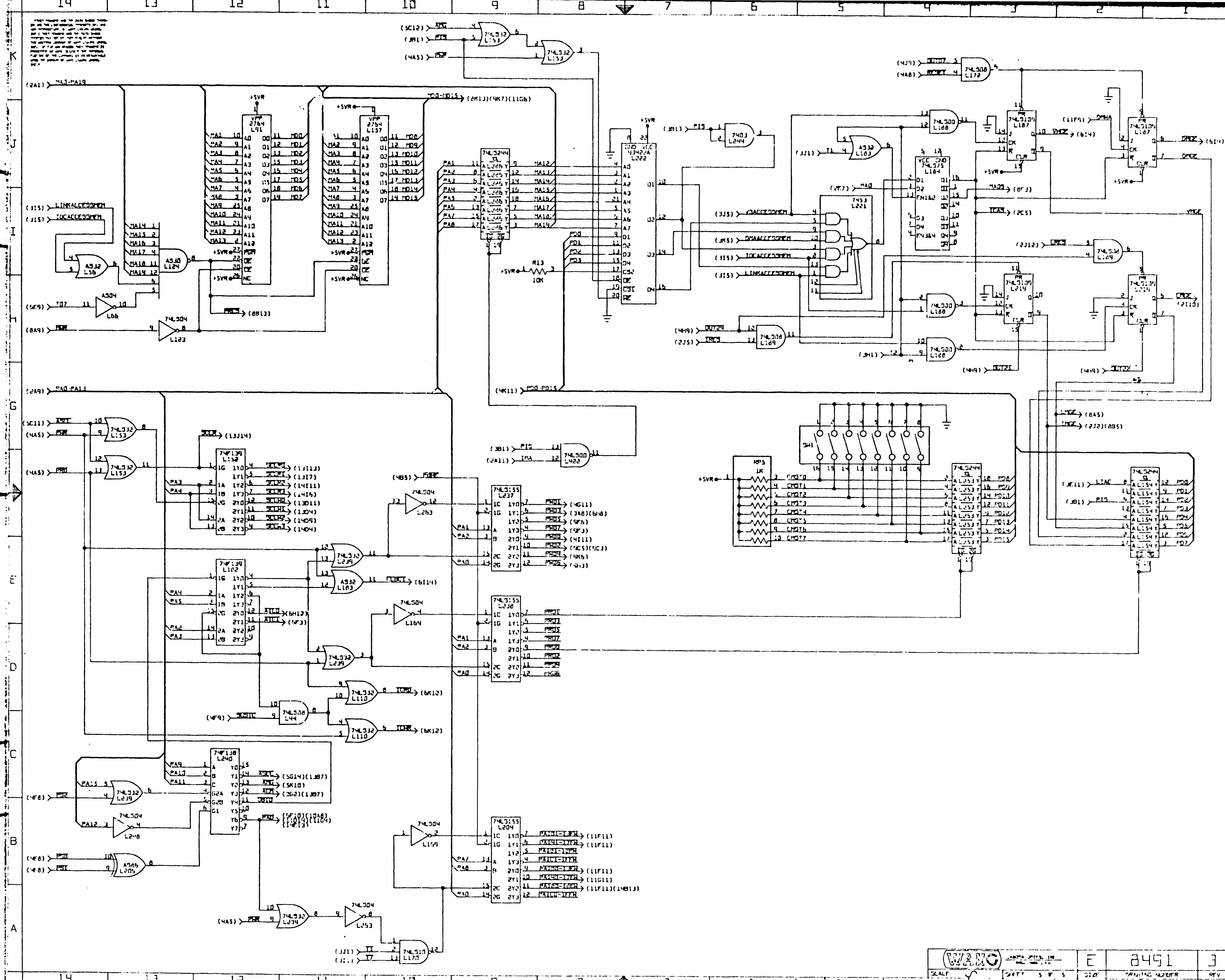


WANG
E
8491
3

17"

11"

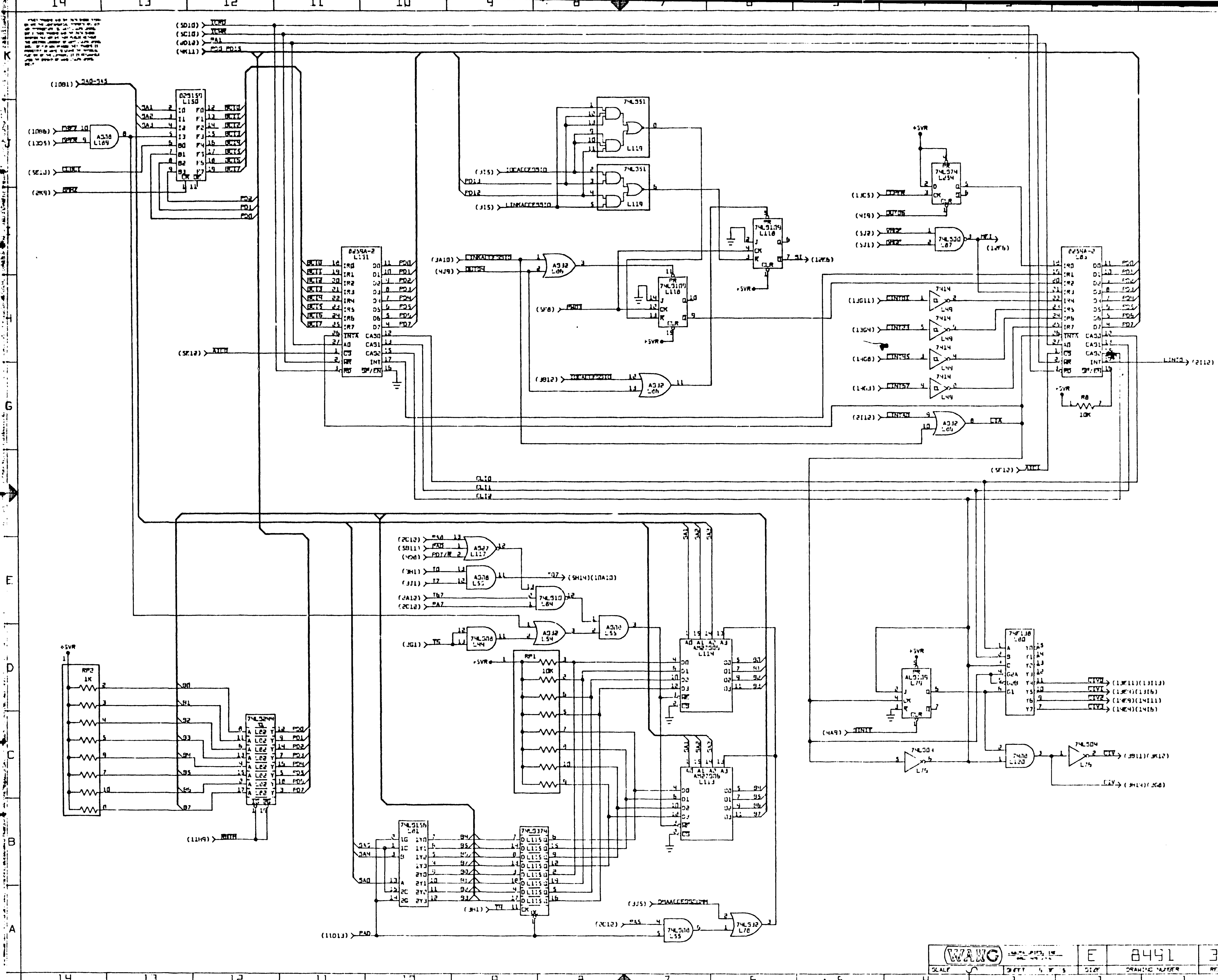
8.5"



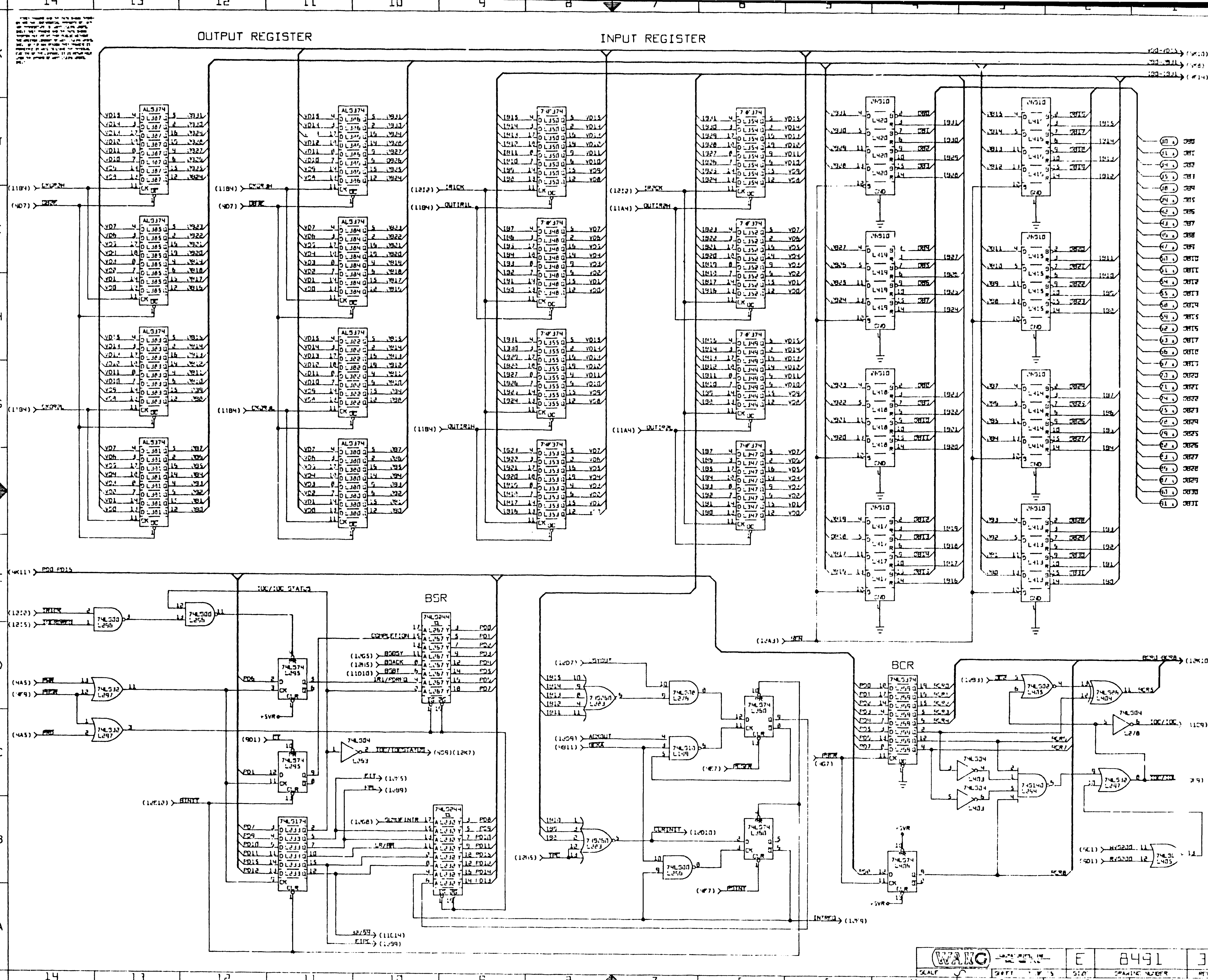
8.5"

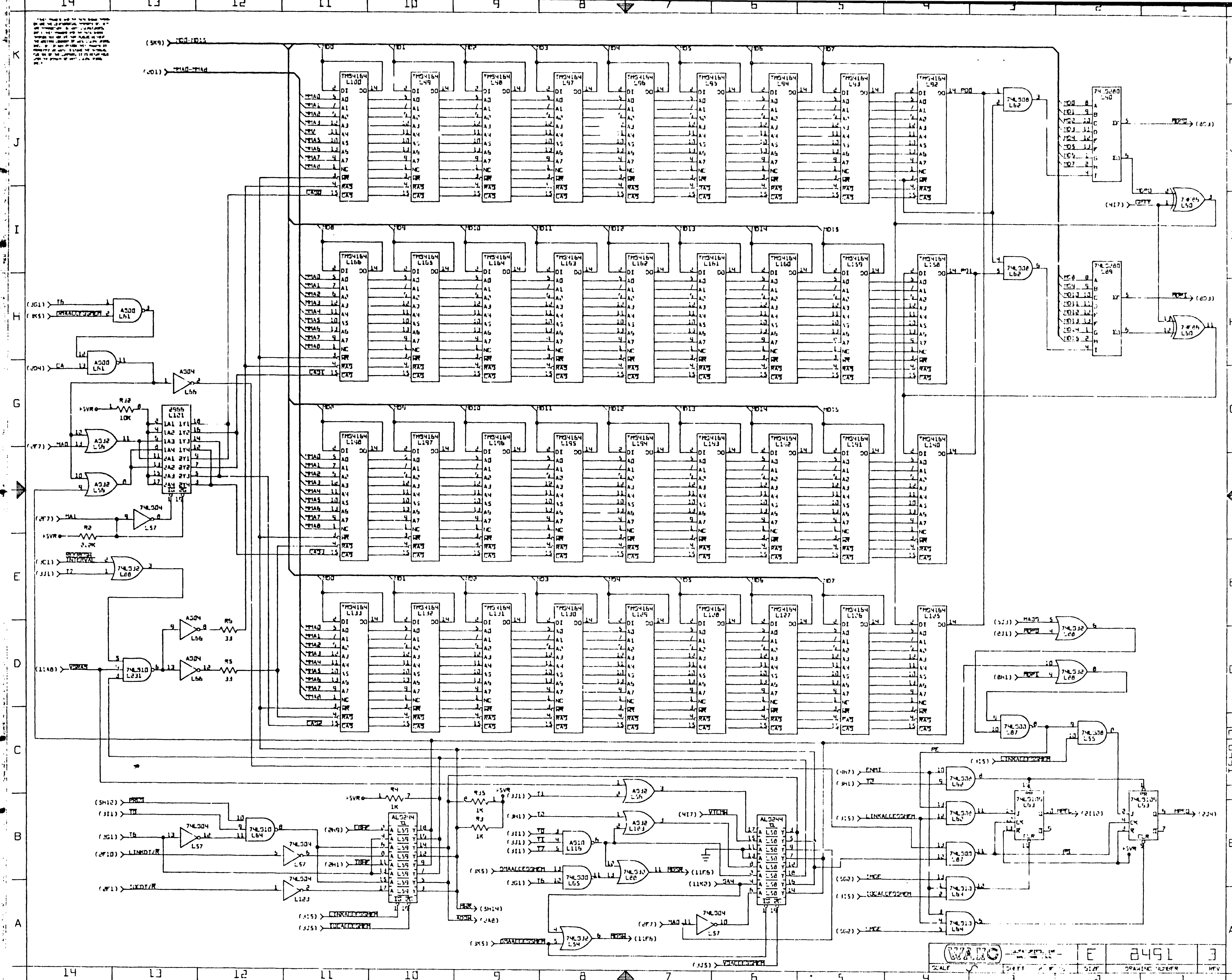
11"

17"



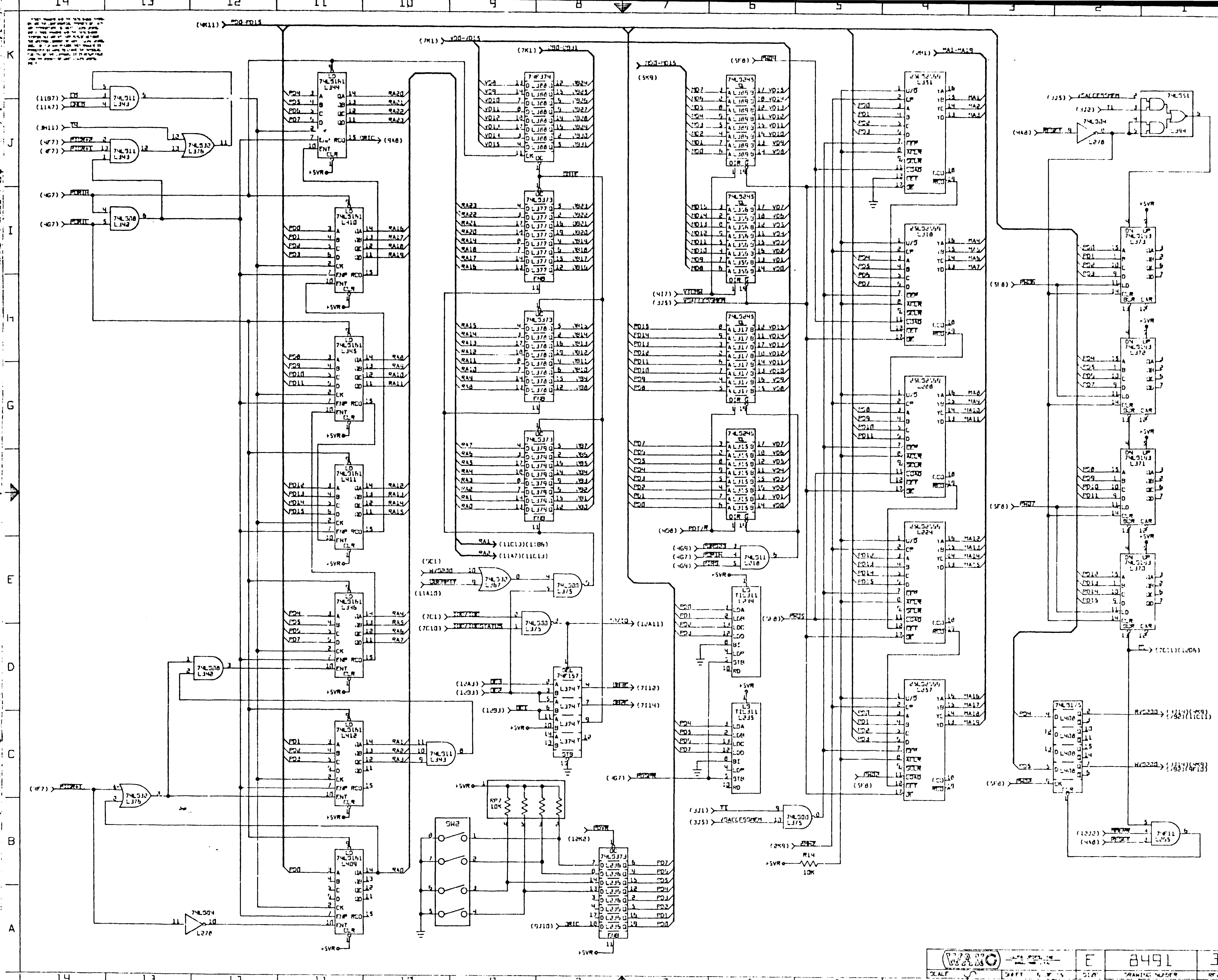
17"
11"
8.5"


OUTPUT REGISTER
INPUT REGISTER
BSR
BCR
WANG
E
8491
3

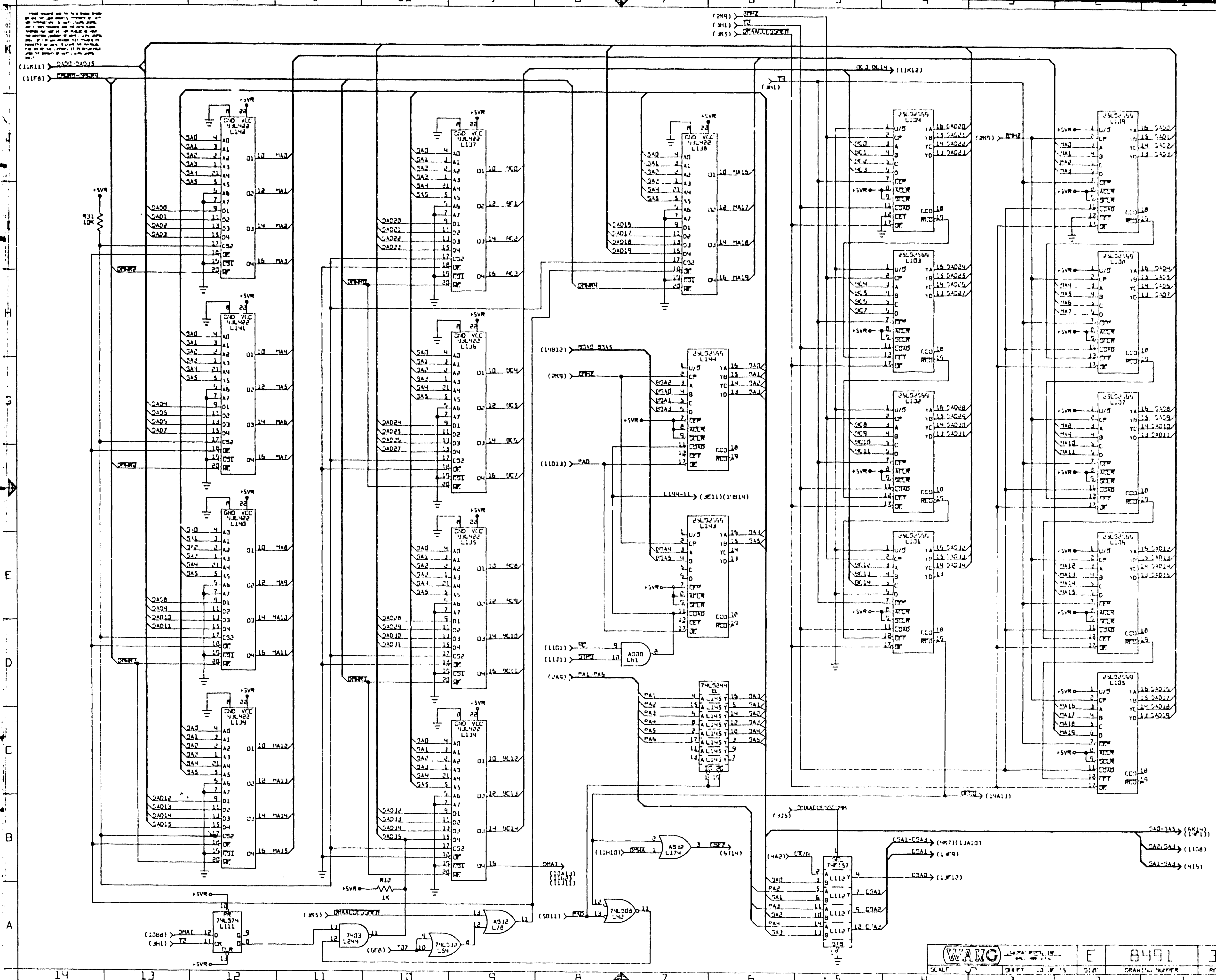


TMS4164
AL5244
74LS00
74LS32
74LS04
74LS10
74LS280
74LS86
74LS109
WANG
E
8451
3

17"
11"
8.5"



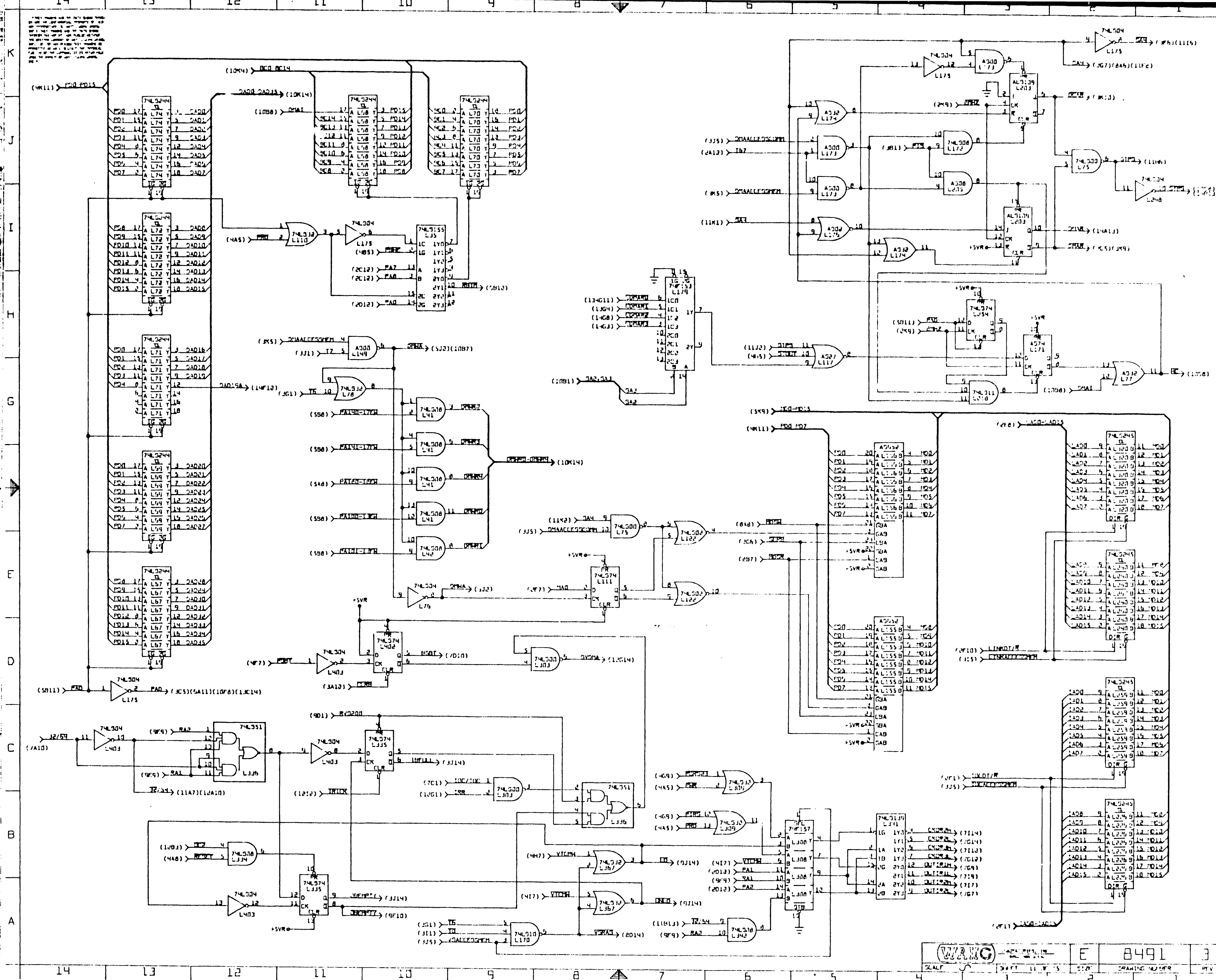
WANG
E
8491
3


WANG
E
8491
3
74LS374
74F157
74LS00
74LS32
74LS244

17"

11"

8.5"



8.5"

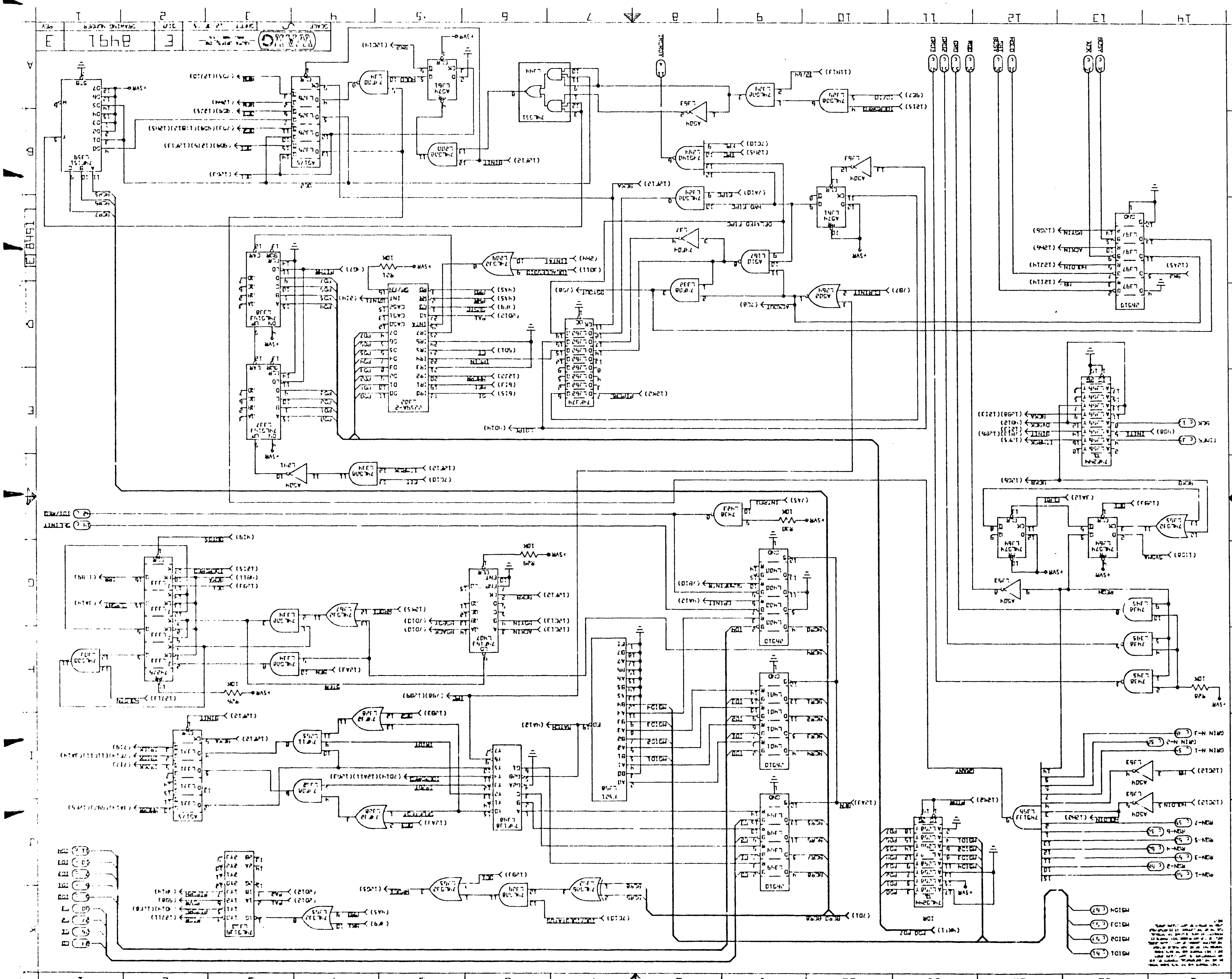
11"

17"

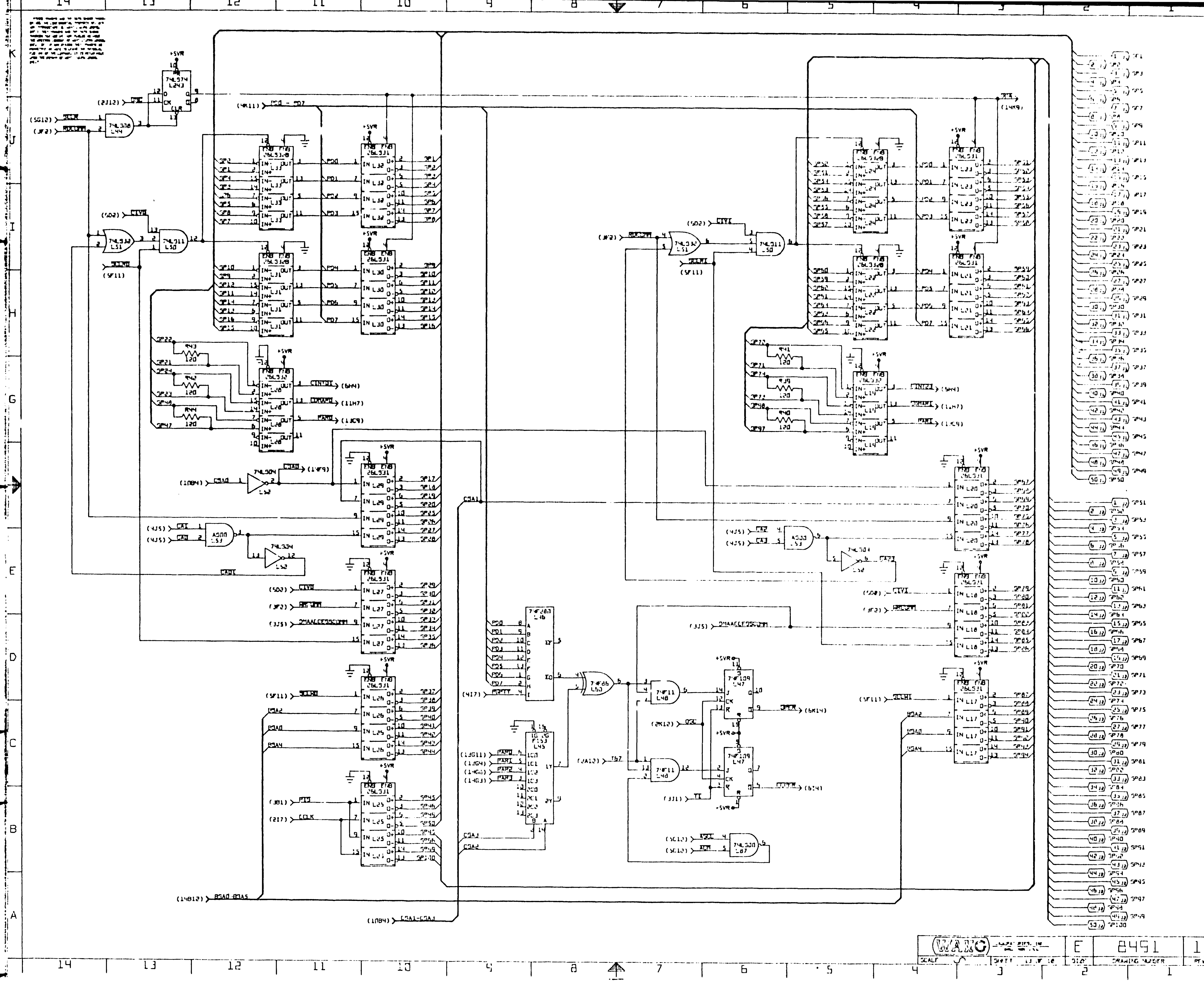
8.5"

11"

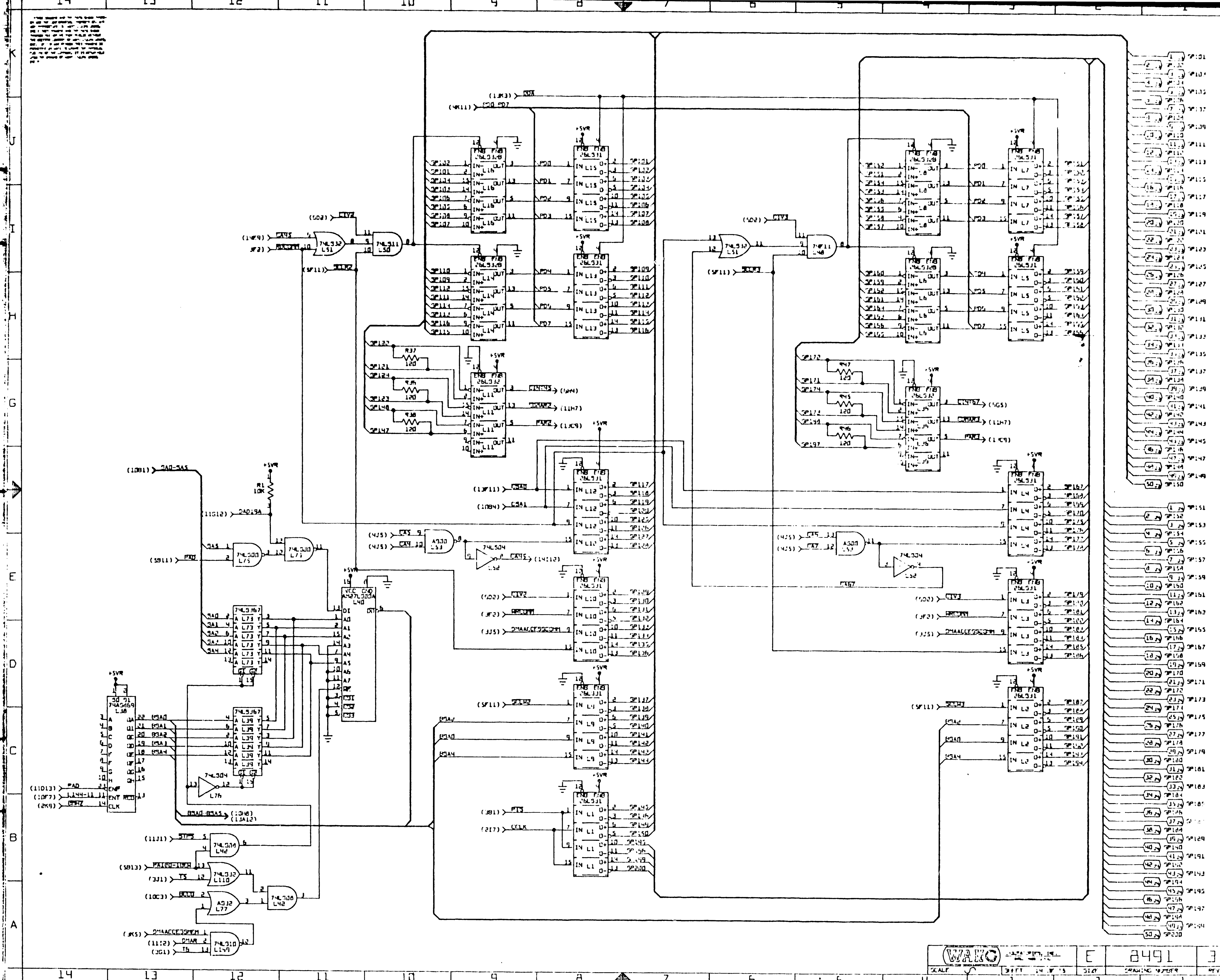
17"



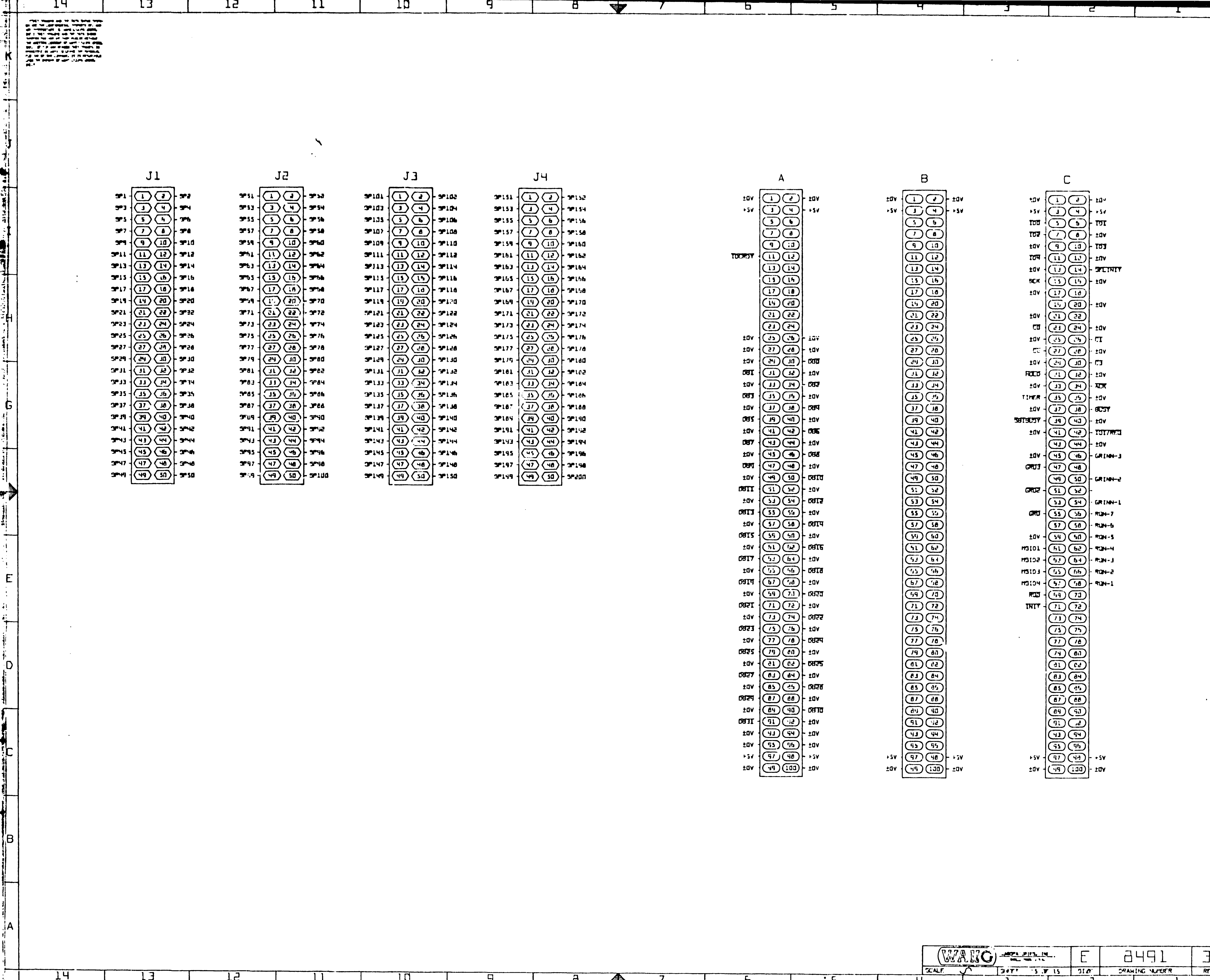
17" 11" 8.5"



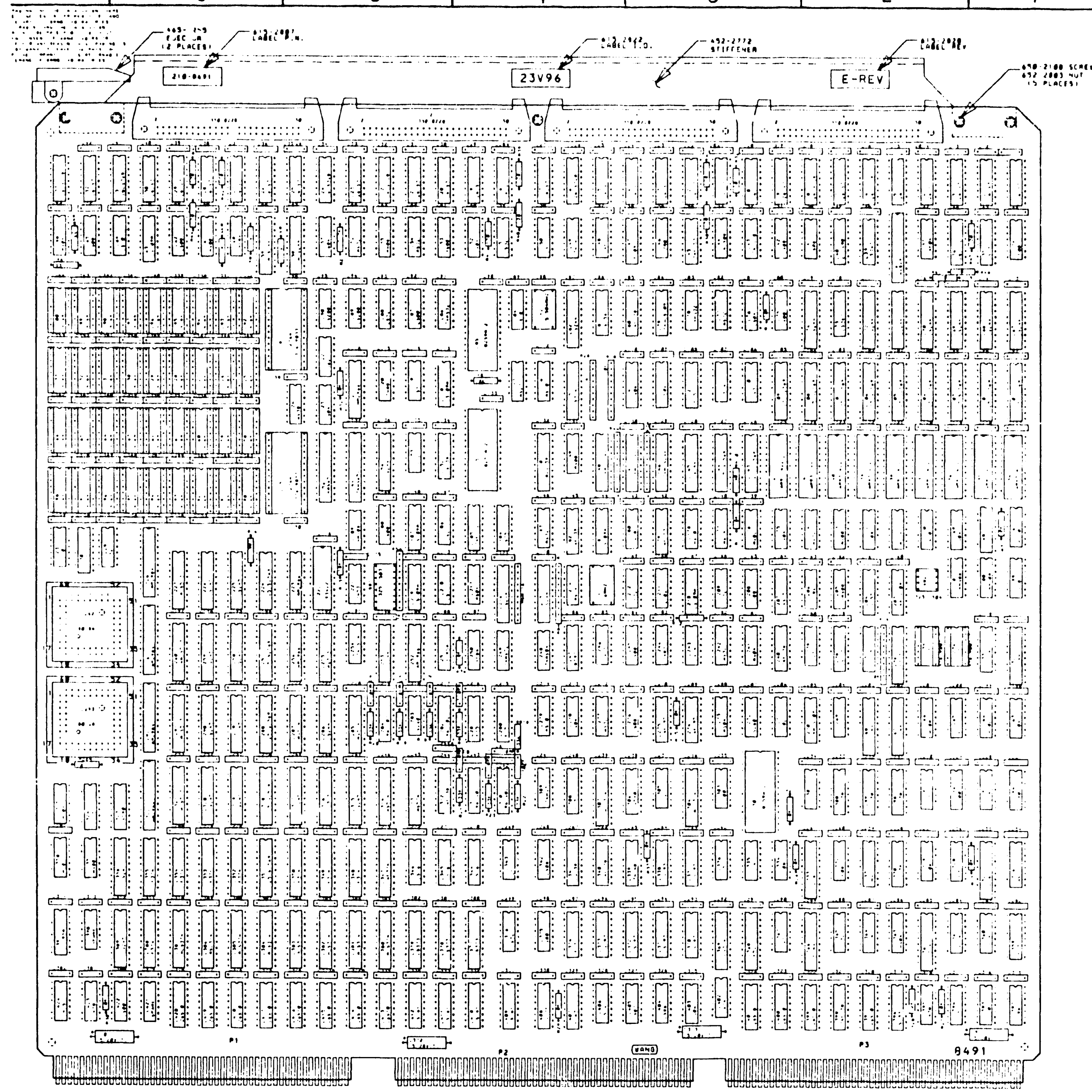
8.5" 11" 17"



8.5"
11"
17"

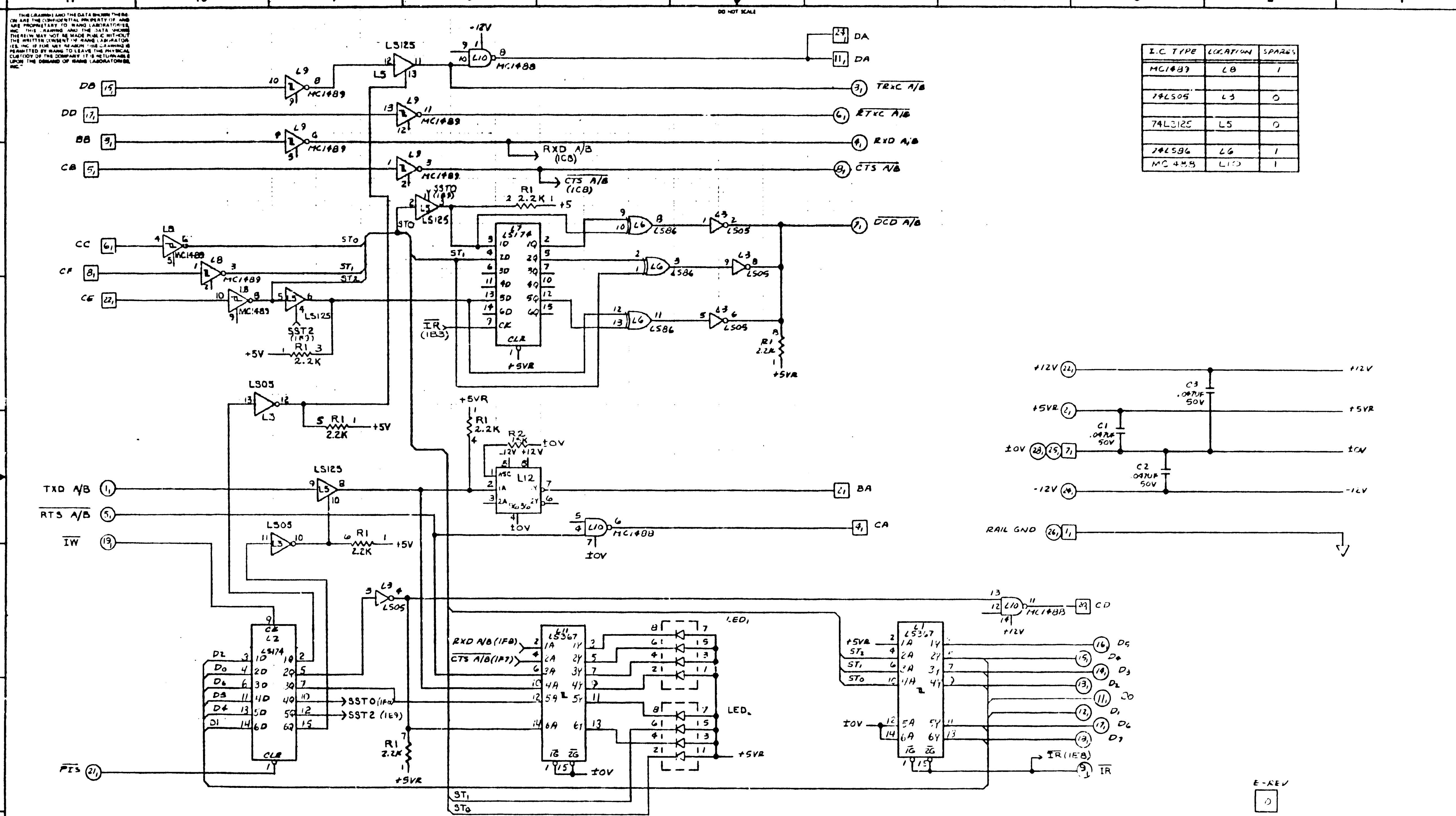


J1
J2
J3
J4
A
B
C
WANG
E
8491
3



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W 5% EXPRESSED IN OHMS.
3. C336-C371 ARE .1/50V.
4. LOAD 16 PIN SOCKETS WPN 376-9002-T IN THE FOLLOWING LOCATIONS:
L92-L100 L125-L133 L158-L166 AND L190-L198.
5. LOAD 68 PIN SOCKET WPN 376-9094 IN LOCATION L262.L293.

WANG		BY	DATE	APPROVED BY	DATE
		DWN HSL		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS 300	E C CONTROL		MFG ENGR	
	NO. 10-213	TITLE MULTILINE TC ML ASSEMBLY DRAWING			
FINISH		210-8491	C	8491	3
	SCALE 1/1				



I.C TYPE	LOCATION	SPARES
MC1489	L8	1
74LS05	L3	0
74LS125	L5	0
74LS86	L6	1
MC 488	L10	1

E-REV 0

REVISION		
A	ORIGINATED PER DWR#2251 APP'D:	KM
B	REVISED PER DCR#00154 APP'D:	KM
9	REVISED PER DCR# D0287 APP'D	RSE
1/0	REVISED PER ECO#35350 APP'D	
2/0	REVISED PER ECO#35414 APP'D	
3/0	REVISED PER ECO#35766D APP'D	DJC
4/0	REVISED PER ECO 36413 APP'D	

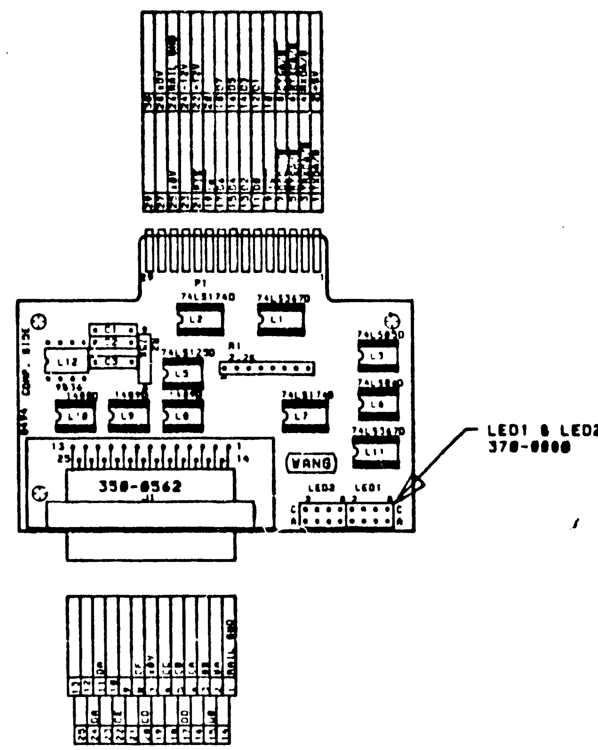
WANG LABORATORIES, INC. LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	KM		E ENGR	
CHK			M ENGR	
			MFG ENGR	

MODEL NO VS 300

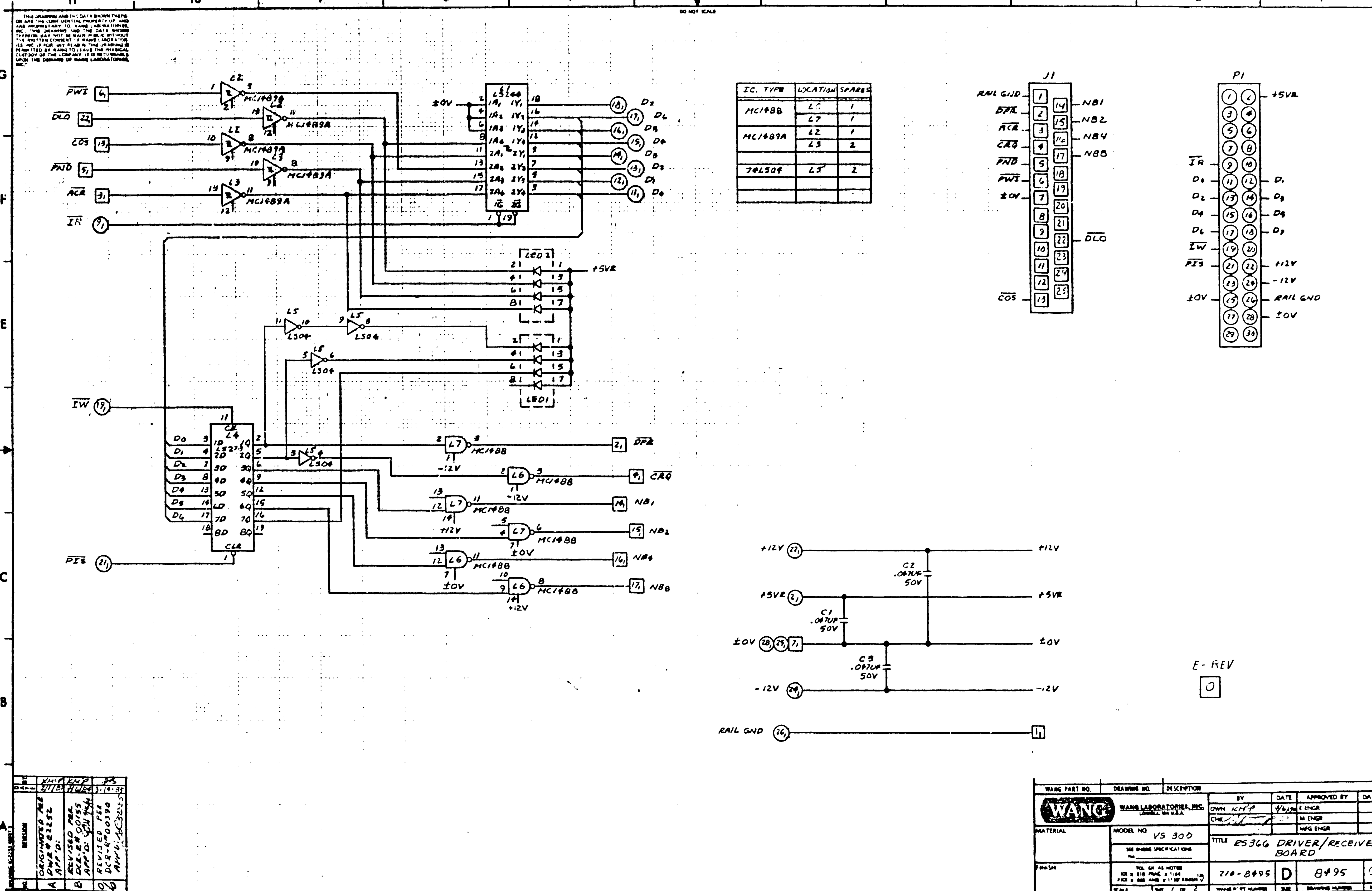
TITLE RS232 DRIVER/RECEIVER BOARD

WANG PART NUMBER 210-8494 SIZE D DRAWING NUMBER 8494 REV 4



NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITORS ARE .047. EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W.5%.EXPRESSED IN OHMS.

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN DAL	12/05/84	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS 300/MLTC	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-213	TITLE RS232 DRIVER/RECEIVER BD ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC.+/-1/64 .XXX+/-.005 ANG +/- 1 30'	210-8494	C	8494	5
	SCALE 1/1 SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV



IC. TYPE	LOCATION	SPARES
MC1488	L6	1
	L7	1
MC1489A	L2	1
	L3	2
74LS04	L5	2

REV	REVISION		
A	ORIGINATED PER DWR# 62252 APP'D:	KMP 2/1/83	
B	REVISED PER DCR-RM00155 APP'D:	KMP 4/1/84	
0	REVISED PER DCR-R#00390 APP'D:	RS 3-14-85	

WANG PART NO. | DRAWING NO. | DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	KMP	4/6/84	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO VS 300

SEE ENGRG SPECIFICATIONS

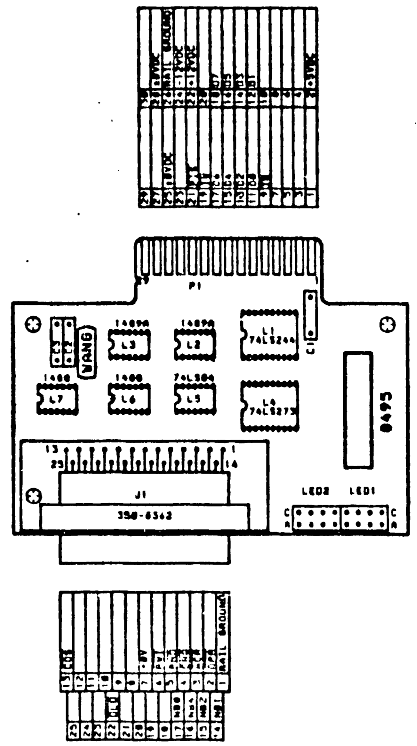
FINISH

TITLE RS366 DRIVER/RECEIVER BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-8495	D	8495	0

SHT 1 OF 2

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC., THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."



NOTES:
1. UNLESS OTHERWISE SPECIFIED;
ALL CAPACITORS ARE .047, EXPRESSED IN MICROFARADS.

BY	GWC	MRM	FVZ
DATE	1/20/84	3/22/84	3/14/85
CHECKER	BF	DB	DB
REVISION	DWR#E2252	DCR-R#00155 DCR#00274	DCR-R#00390
NO.	A\A	B\B	C

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.

BY		DATE	APPROVED BY	DATE
DWN	GWC	1/20/84	E ENGR	
CHK			M ENGR	
E C CONTROL			MFG ENGR	

MATERIAL

MODEL NO. VS 300

SEE ENGRG SPECIFICATIONS NO. 10-213

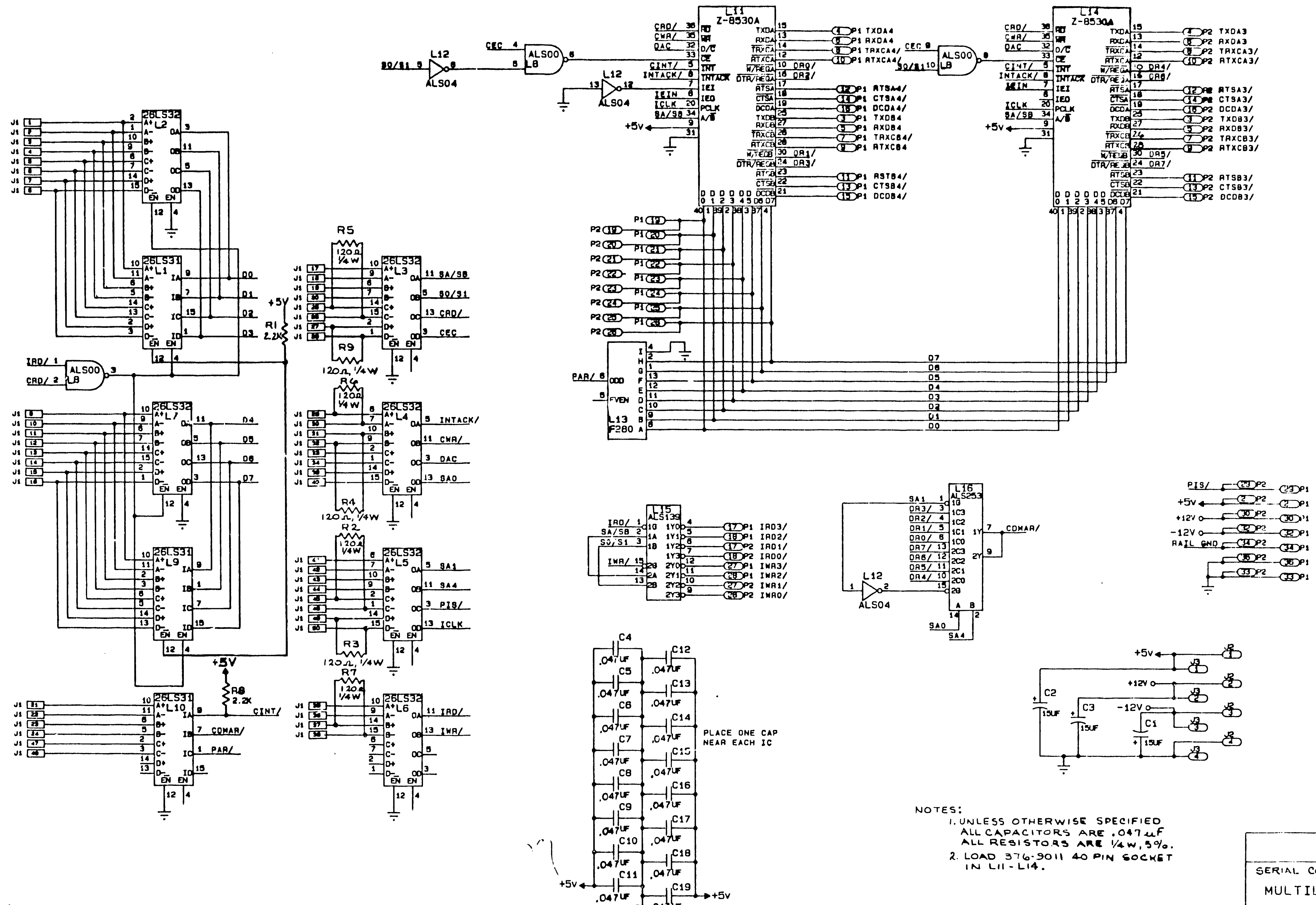
FINISH

TOL. EX. AS NOTED
.XX+/- .010 FRAC.+/-1/64
.XXX+/-.005 ANG +/- 1 30'

SCALE 1/1 SHT 1 OF 1

TITLE RS366 DRIVER/RECEIVER BD. ASSEMBLY DRAWING

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-8495	C	8495	Ø



NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE .047 uF ALL RESISTORS ARE 1/4 W, 5%.
2. LOAD 376-9011 40 PIN SOCKET IN L11-L14.

ORIGINATED PER DWR # E2664 APP'D:	1-6-85
REVISED PER ECO # 35989, 36746 APP'D:	5/21/85
REVISED PER ECO # 36200 APP'D:	5/28/85

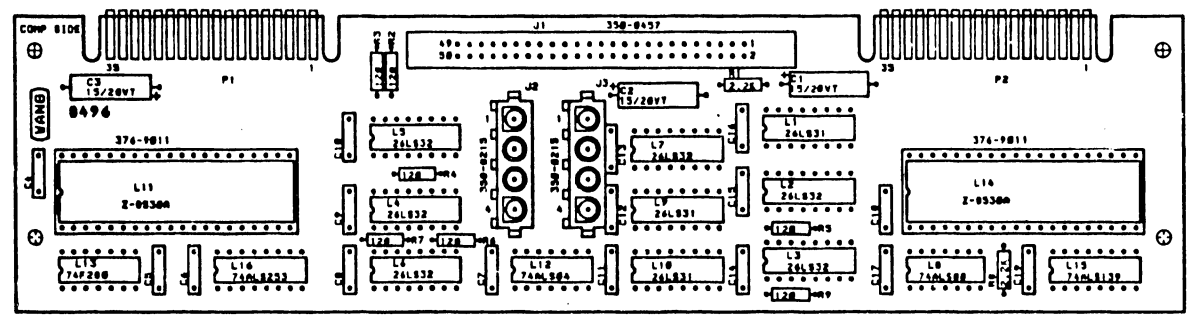
WANG

SERIAL COMMUNICATION LINK

MULTILINE BD

D 1/28/85 210-8496 REV 3

AA#2898 SHEET 1 OF 2



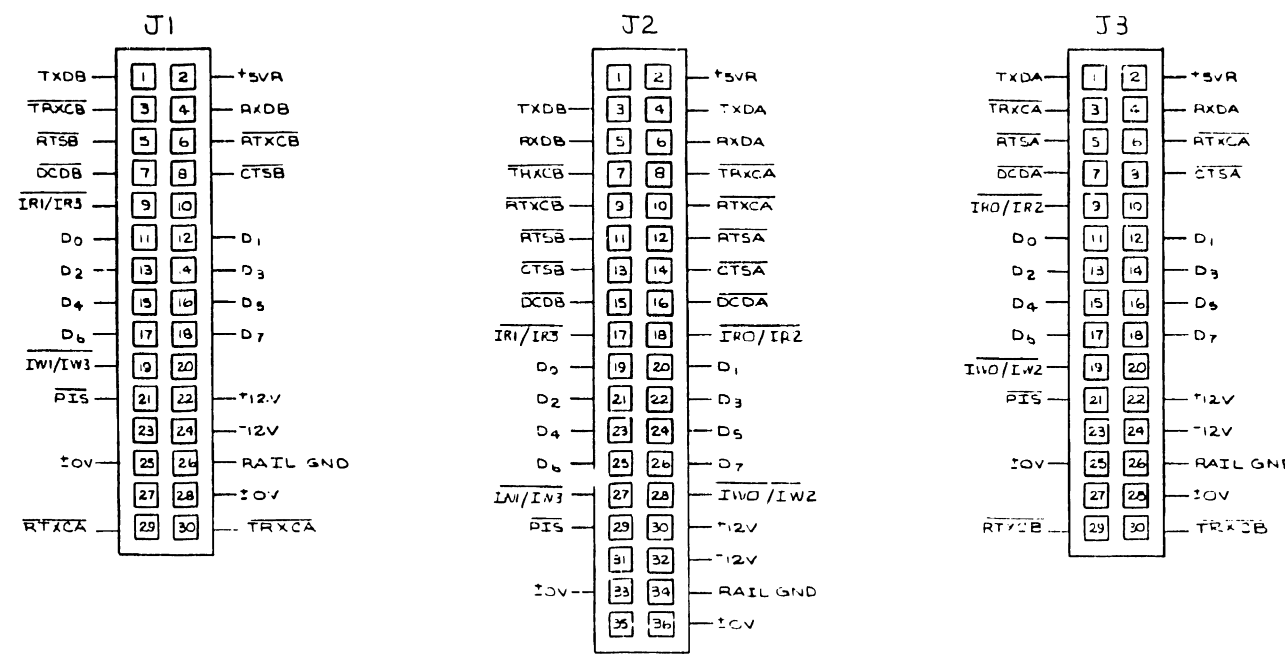
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL CAPACITORS ARE .047, EXPRESSED IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%, EXPRESSED IN OHMS.

N

		BY	DATE	APPROVED BY	DATE
WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		DWN ANTAL	4/12/85	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS300	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-213	TITLE SERIAL COMM ML ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC.+/-1/64 .XXX+/-.005 ANG +/- 1 30'	210-8496	C	8496	3
	SCALE 1/1 SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC.

DO NOT SCALE



E-REV

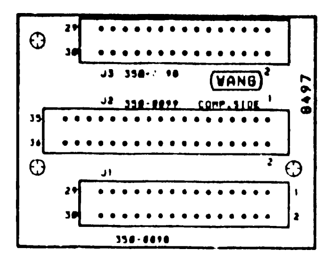
1

WANG LABORATORIES, INC. LOWELL, MA U.S.A.	BY	DATE	APPROVED BY	DATE
	DWN C.A.M.	2-10-84	E ENGR	
	CHK		M ENGR	
MATERIAL / MODEL NO. VS-300 / SEE ENGRG SPECIFICATIONS			MFG ENGR	
TITLE	BLOCK CONNECTOR			
FINISH / TOL. EX. AS NOTED	210-8497 (WANG PART NUMBER)	D (SIZE)	8497 (DRAWING NUMBER)	2 (REV)
SCALE / SHT / OF				

REVISION

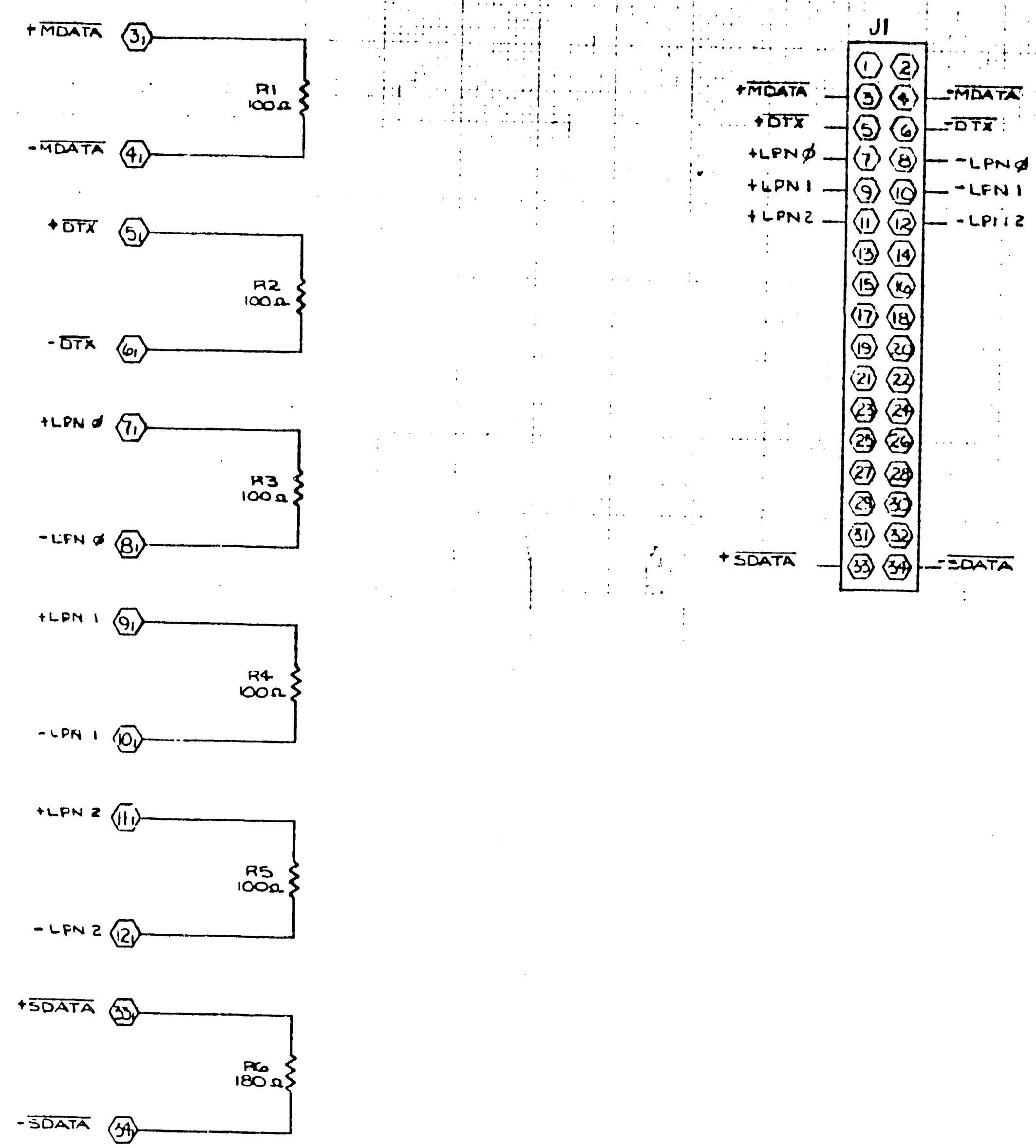
D 8497

"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

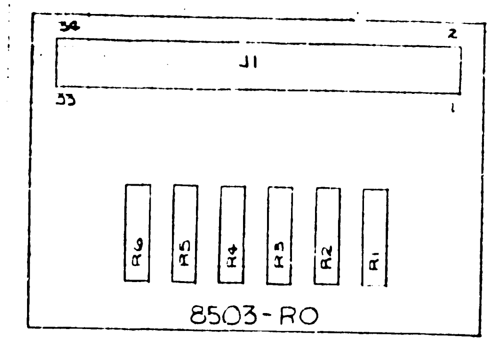


NOTES: 1. MAX.LEAD PROTRUSION ON CIRCUIT SIDE .005.

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN DAL	11/02/84	E ENGR	
		CHK JDL	11/09/84	H ENGR	
MATERIAL	MODEL NO. VS-300	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE BLOCK CONNECTOR ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC.+/-1/64 .XXX+/-.005 ANG +/- 1 30'	210-0497	C	8497	2
	SCALE 1/1 — SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV



COMPONENT	TYPE	W.L. PT. NO.
R1-5	100Ω 1/4W 5%	330-2011
R6	180Ω 1/4W 5%	330-2019
J1	34 PIN CONN	350-0494



E-REV 0

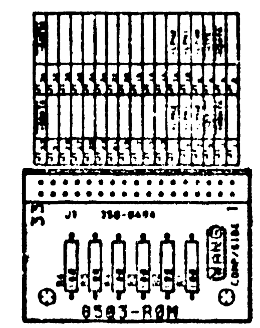
NOTE: ALL RES. ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

MODEL NO. F191A

TITLE: MUX BUS TERMINATOR BD

210-8503 D 8503 1

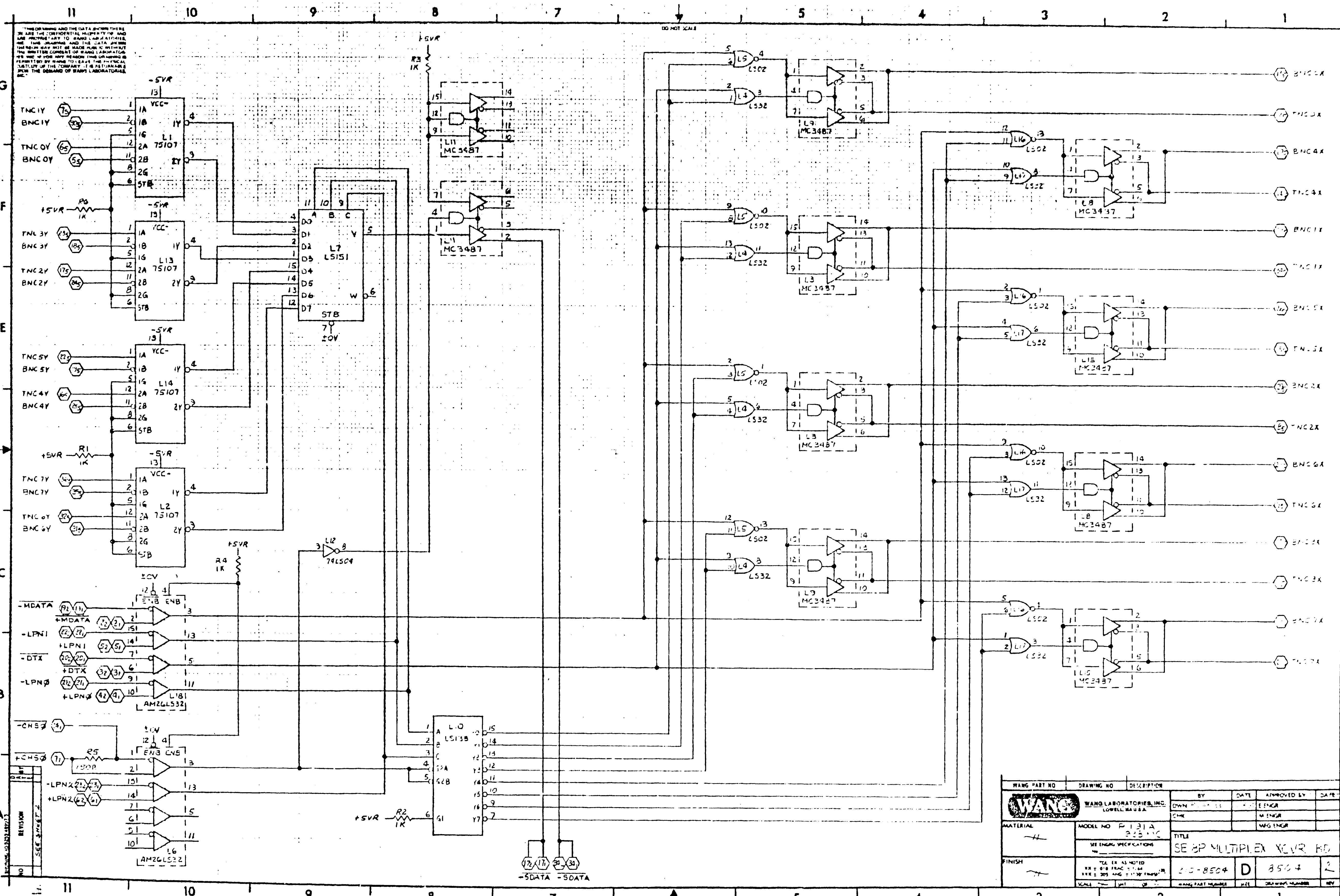


NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4W, 5%, EXPRESSED IN OHMS.

NO.	REVISION	BY	DATE	CHK BY
0/0	DWR=E1812	H.H.	11/01/82	J.L.
0/1	ECO=29866	BAH	6-24-83	

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY
		DWN H.H.	11/01/82	E ENGR
		CHK J.L.	11/02/82	M ENGR
MATERIAL	MODEL NO. P191A 928 MC	E C CONTROL		MFG ENGR
	SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE MUX BUS. TERMINATOR BOARD ASSEMBLY DRAWING		
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC.+/-1/64 .XXX+/-.005 ANG +/- 1 30'	WANG PART NUMBER 210-8503-R0	SIZE C	DRAWING NUMBER 8503 REV 1
	SCALE 1/1 SHT 4 OF 6			

N

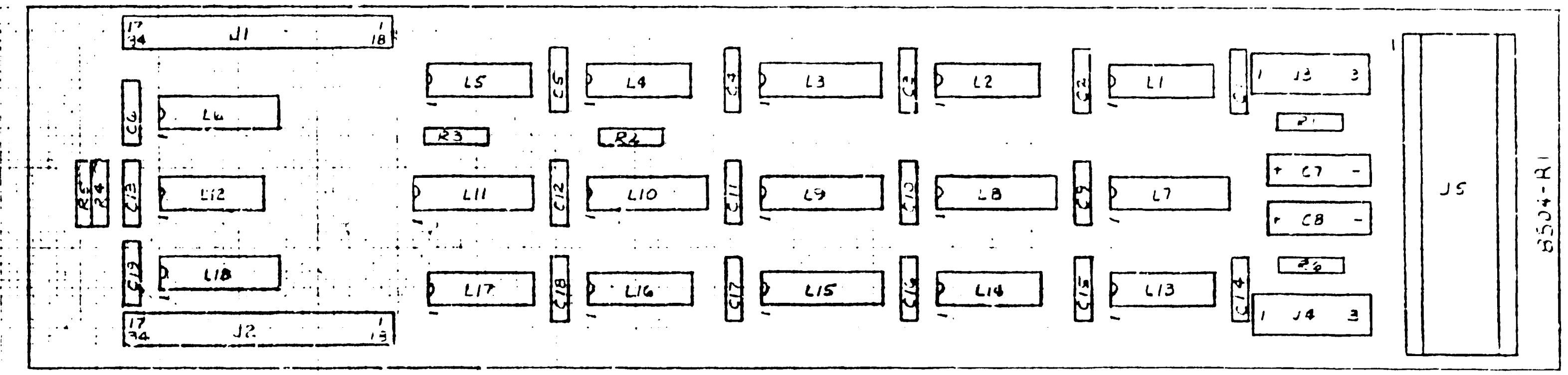


TNC1Y
BNC1Y
TNC0Y
BNC0Y
TNC3Y
BNC3Y
TNC2Y
BNC2Y
TNC5Y
BNC5Y
TNC4Y
BNC4Y
TNC7Y
BNC7Y
TNC6Y
BNC6Y
L1 75107
L13 75107
L14 75107
L2 75107
L7 LS151
L11 MC3487
L12 74LS04
L10 LS138
L3 MC3487
L8 MC3487
L9 MC3487
L15 MC3487
L18 AM26LS32
L6 AM26LS32
-MDATA
+MDATA
-LPN1
+LPN1
-DTX
+DTX
-LPNØ
+LPNØ
-CHSØ
+CHSØ
-LPN2
+LPN2
-5DATA
BNC4X
TNC4X
BNC1X
TNC1X
BNC2X
TNC2X
BNC6X
TNC6X
DO NOT SCALE
WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.
TITLE SE 8P MULTIPLEX XCVR BD
D
8504
2

DO NOT SCALE

IC LOCATION	TYPE	W.L. PART NO.
L1,2,13,14	75107	376-0146
L3,8,9,11,15	MC3487	376-0577
L4,17	74LS32	376-0211
L5,16	74LS02	376-0208
L6,18	AM26LS32	376-0471
L7	74LS161	376-0214
L10	74LS138	376-0294
L12	74LS04	376-0180

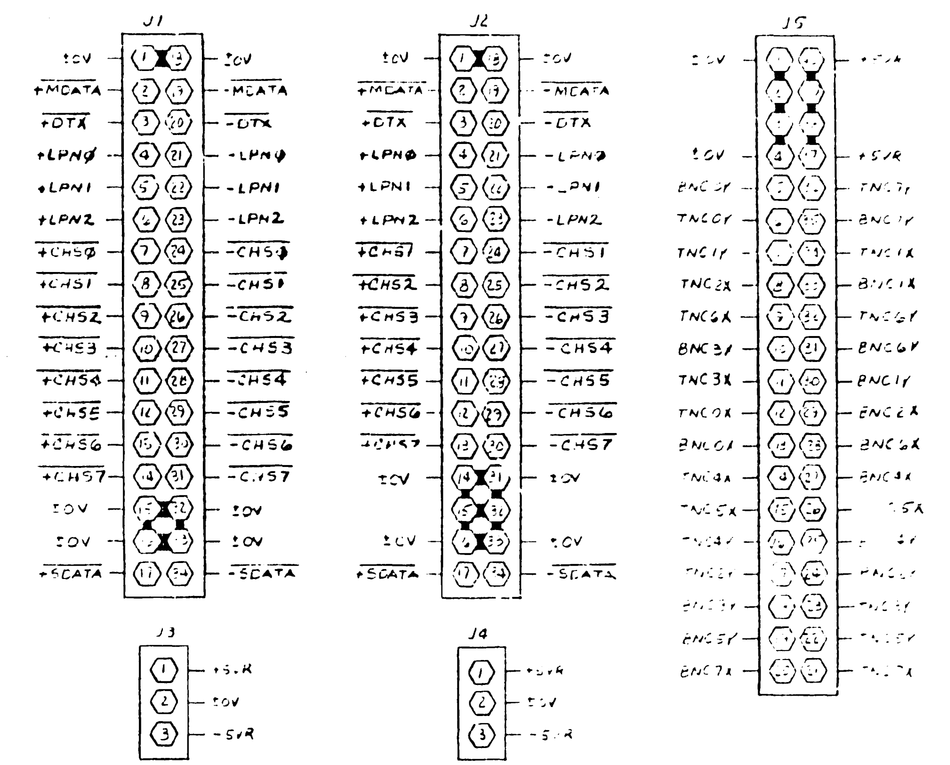
COMPONENT	TYPE	W.L. PART NO.
R1-4,6	1K 1/4W 5%	330-3011
R5	150Ω 1/4W 5%	330-2016
C1-6,9-19	.047uF 50V	300-1366
C7,8	15uF 20V(T)	300-4022
J1,2	34 POS CONN HDR	350-0453
J3,4	3 POS HEADER	350-0217
J5	40 PIN SKT	376-9065

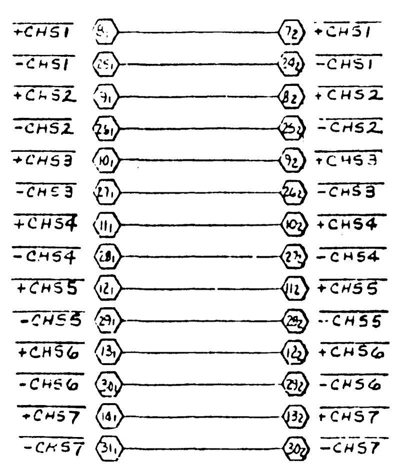


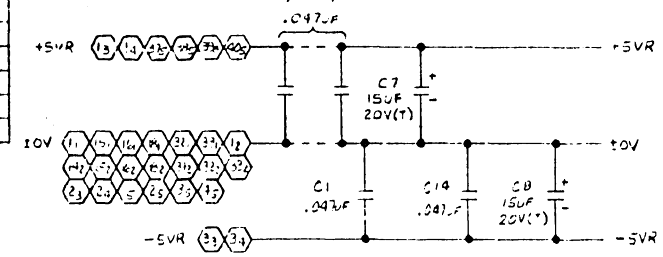
IC TYPE	LOC	SPARES
74LS04	L12	5

MNEMONICS	COORD.
+LPNØ	1B11
-LPNØ	1B11
+LPN1	1B11
-LPN1	1B11
+LPN2	1A11
-LPN2	1A11
BNC0X	1G1
BNC0Y	1F11
BNC1X	1F1
BNC1Y	1G11
BNC2X	1E1
BNC2Y	1E11
BNC3X	1C1
BNC3Y	1F11
BNC4X	1F1
BNC4Y	1D11
BNC5X	1E1
BNC5Y	1E11
BNC6X	1D1
BNC6Y	1C11
BNC7X	1C1
BNC7Y	1D11
+DTX	1B11
-DTX	1B11
+MDATA	1C11
-MDATA	1C11
+CHSØ	1A11
-CHSØ	1B11
+CHS1	2C11
-CHS1	2C11
+CHS2	2C11

MNEMONICS	COORD.
-CHS2	2C11
+CHS3	2C11
-CHS3	2C11
+CHS4	2C11
-CHS4	2B11
+CHS5	2B11
-CHS5	2B11
+CHS6	2B11
-CHS6	2B11
+CHS7	2B11
-CHS7	2B11
+SDATA	1A7
-SDATA	1A7
TNC0X	1G1
TNC0Y	1F11
TNC1X	1F1
TNC1Y	1G11
TNC2X	1D1
TNC2Y	1E11
TNC3X	1C1
TNC3Y	1F11
TNC4X	1F1
TNC4Y	1D11
TNC5X	1E1
TNC5Y	1E11
TNC6X	1D1
TNC6Y	1C11
TNC7X	1B1
TNC7Y	1D11







NOTES:
1. ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

E-REV
2

LTR	REVISION		
	DESIGNATED PER ... APP'D: DJC		
1	REVISED PER ECO # 25339 APP'D: DJC		
2	REVISED PER ECO # 2906T APP'D		

WANG PART NO	DRAWING NO	DESCRIPTION		

WANG LABORATORIES, INC.
LOWELL, MA U.S.A.

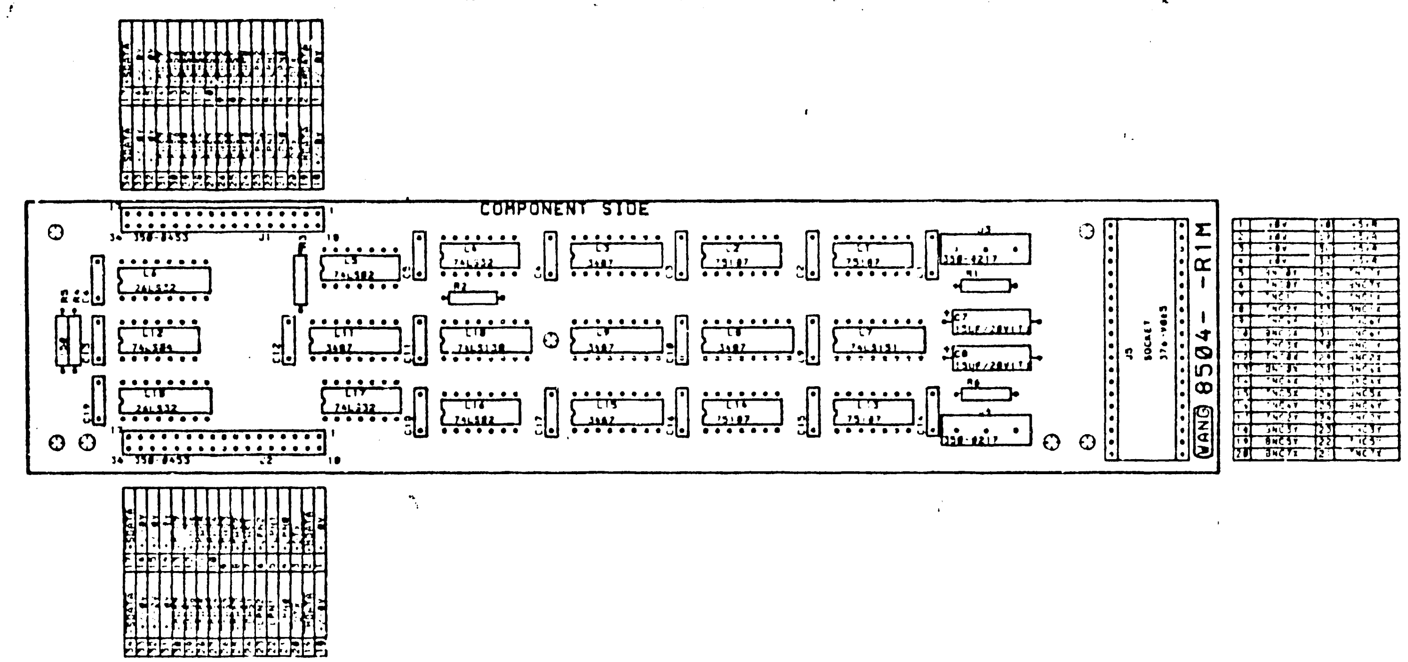
BY	DATE	APPROVED BY	DATE
DWN		E ENGR	
CHK		M ENGR	
		MFG ENGR	

MATERIAL —
FINISH —
MODEL NO
SEE ENGRG SPECIFICATIONS No.
TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30'
SCALE — SHT 1 OF 2

TITLE
SE SP MULTIPLEX XCVR

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-3504	D	3504	2

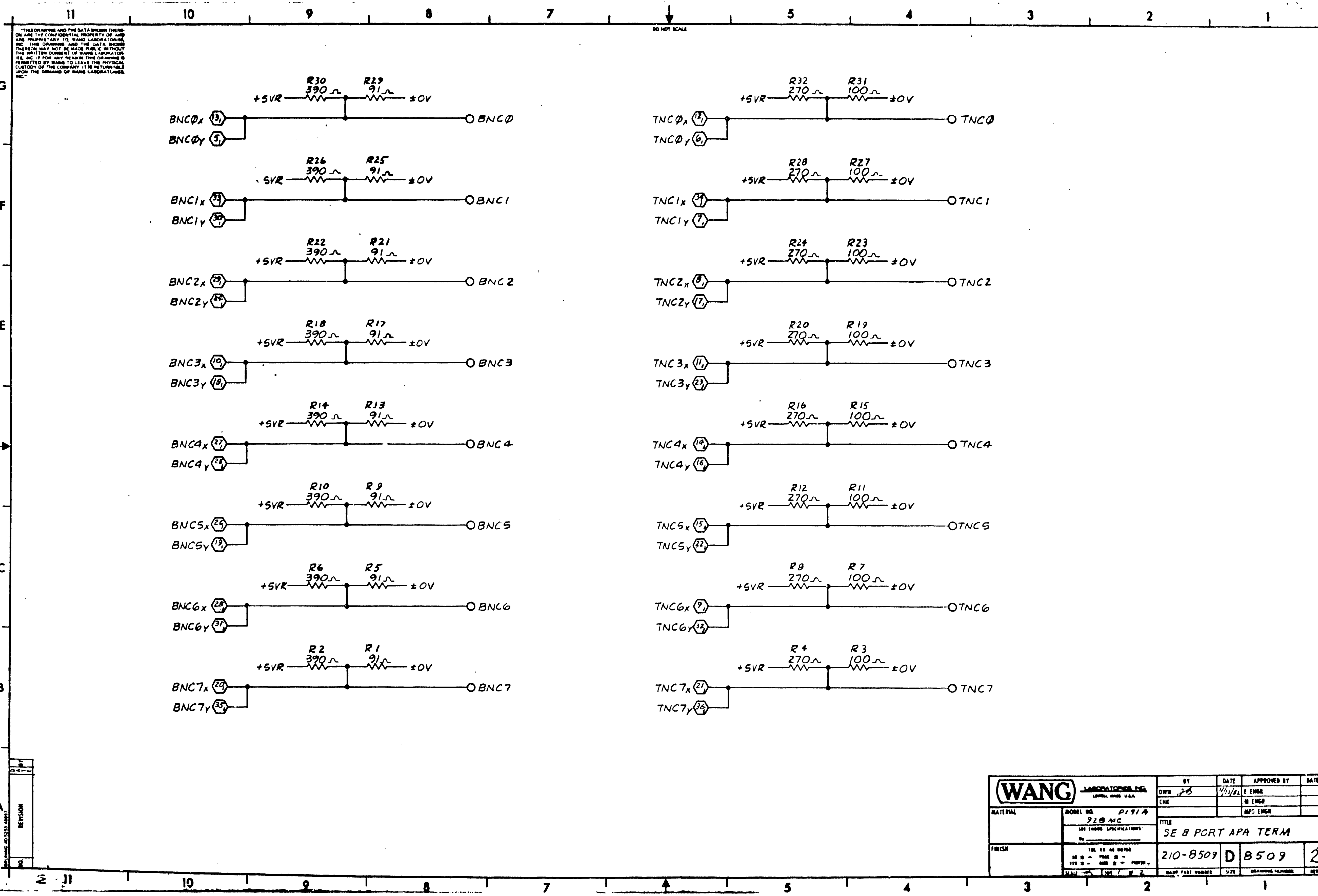
"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF, AND ARE PROPRIETARY TO, WANG LABORATORIES, INC.. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE .047UF, 300-1966.
ALL RESISTORS ARE 1K, 1/4W, 5%, EXPRESSED IN OHMS.

	SC OPW	M.M.	SC
	9/20/82	11/10/82	8/23/83
CHECKER			
REVISION	DWR#E1781	ECO#25339D	ECO#29067D
NO.	0/0	1/1	1/2

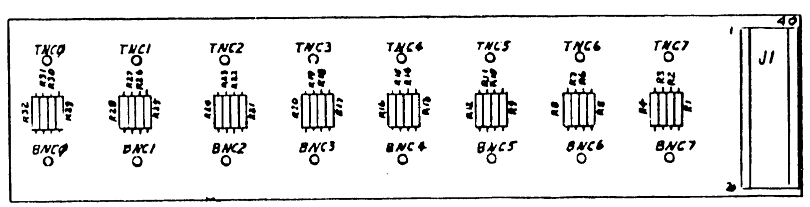
WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY / DATE
		DWN L.L.	82	E ENGR R.L. 82
		CHK		M ENGR
MATERIAL	MODEL NO. 928MC P191A	E C CONTROL		MFG ENGR
	SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE SE 8P MULTIPLEX XCVR BOARD ASSEMBLY DRAWING		
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC.+/-1/64 .XXX+/-.005 ANG +/- 1 30	210-8504-R1 (WANG PART NUMBER)	C (SIZE)	8504 (DRAWING NUMBER) 2 (REV)
	SCALE 1/1 SHT 4 OF 6			



DO NOT SCALE
R30 390Ω R29 91Ω +5VR ±0V BNCØx 13 BNCØy 5 BNCØ
R26 390Ω R25 91Ω +5VR ±0V BNC1x 33 BNC1y 30 BNC1
R22 390Ω R21 91Ω +5VR ±0V BNC2x 29 BNC2y 34 BNC2
R18 390Ω R17 91Ω +5VR ±0V BNC3x 10 BNC3y 18 BNC3
R14 390Ω R13 91Ω +5VR ±0V BNC4x 27 BNC4y 28 BNC4
R10 390Ω R9 91Ω +5VR ±0V BNC5x 25 BNC5y 19 BNC5
R6 390Ω R5 91Ω +5VR ±0V BNC6x 20 BNC6y 37 BNC6
R2 390Ω R1 91Ω +5VR ±0V BNC7x 24 BNC7y 35 BNC7
R32 270Ω R31 100Ω +5VR ±0V TNCØx 12 TNCØy 6 TNCØ
R28 270Ω R27 100Ω +5VR ±0V TNC1x 31 TNC1y 7 TNC1
R24 270Ω R23 100Ω +5VR ±0V TNC2x 8 TNC2y 17 TNC2
R20 270Ω R19 100Ω +5VR ±0V TNC3x 11 TNC3y 23 TNC3
R16 270Ω R15 100Ω +5VR ±0V TNC4x 14 TNC4y 16 TNC4
R12 270Ω R11 100Ω +5VR ±0V TNC5x 15 TNC5y 22 TNC5
R8 270Ω R7 100Ω +5VR ±0V TNC6x 9 TNC6y 32 TNC6
R4 270Ω R3 100Ω +5VR ±0V TNC7x 21 TNC7y 36 TNC7
D 8509
WANG LABORATORIES INC.
MODEL NO. P1914 928MC
TITLE SE 8 PORT APA TERM
210-8509 D 8509 2

DO NOT SCALE

COMPONENT	TYPE	W.L. PART NO.
R1,5,9,13,17,21, 25,29	91Ω, 1/4W, 5%	330-1092
R2,6,10,14,18, 22,26,30	390Ω, 1/4W, 5%	330-2040
R3,7,11,15,19,23, 27,31	100Ω, 1/4W, 5%	330-2011
R4,8,12,16,20 24,28,32	270Ω, 1/4W, 5%	330-2028
J1	CONN., 40 PIN	376-9065



MNEMONIC	COORD
BNC0x	1G10
BNC0y	1G10
BNC1x	1F10
BNC1y	1F10
BNC2x	1E10
BNC2y	1E10
BNC3x	1E10
BNC3y	1E10
BNC4x	1D10
BNC4y	1D10
BNC5x	1C10
BNC5y	1C10
BNC6x	1C10
BNC6y	1C10
BNC7x	1B10
BNC7y	1B10
TNC0x	1G6
TNC0y	1G6
TNC1x	1F6
TNC1y	1F6
TNC2x	1E6
TNC2y	1E6
TNC3x	1E6
TNC3y	1E6
TNC4x	1D6
TNC4y	1D6
TNC5x	1C6
TNC5y	1C6
TNC6x	1C6
TNC6y	1C6
TNC7x	1B6
TNC7y	1B6

J1

±0V	1	40	+5VR
	2	39	
	3	38	
±0V	4	37	+5VR
BNC0y	5	36	TNC7y
TNC0y	6	35	BNC7y
TNC1y	7	34	TNC1x
TNC2x	8	33	BNC1x
TNC6x	9	32	TNC6y
BNC3x	10	31	BNC6y
TNC3x	11	30	BNC1y
TNC0x	12	29	BNC2x
BNC0x	13	28	BNC6x
TNC4x	14	27	BNC4x
TNC5x	15	26	BNC5x
TNC4y	16	25	BNC4y
TNC2y	17	24	BNC2y
BNC3y	18	23	TNC3y
BNC5y	19	22	TNC5y
BNC7x	20	21	TNC7x

+5VR (40)(39)(38)(37) —— +5VR

±0V (1)(2)(3)(4) —— ±0V

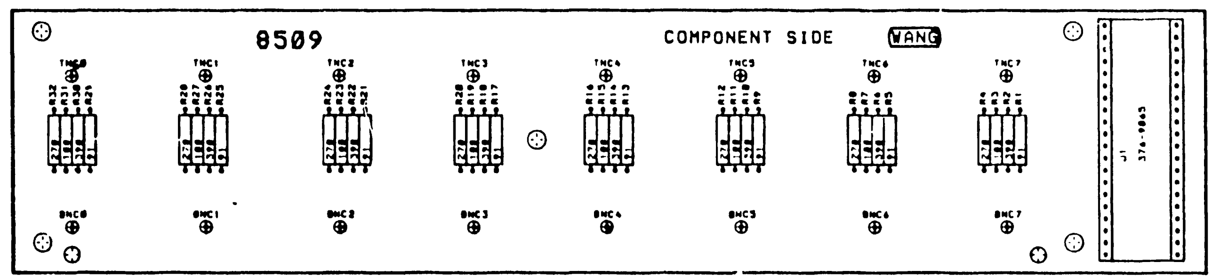
NOTE:
1 ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED

E-REV
0

WANG LABORATORIES, INC.		BY	DATE	APPROVED BY	DATE
MATERIAL	MODEL NO. P191A 928MC	DWN		E ENGR	
FINISH	SEE ENGRG SPECIFICATIONS	CHK		M ENGR	
		TITLE SE 8 PORT APA TERM			
	SCALE	8509	D	8509	2
	SHT 2 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

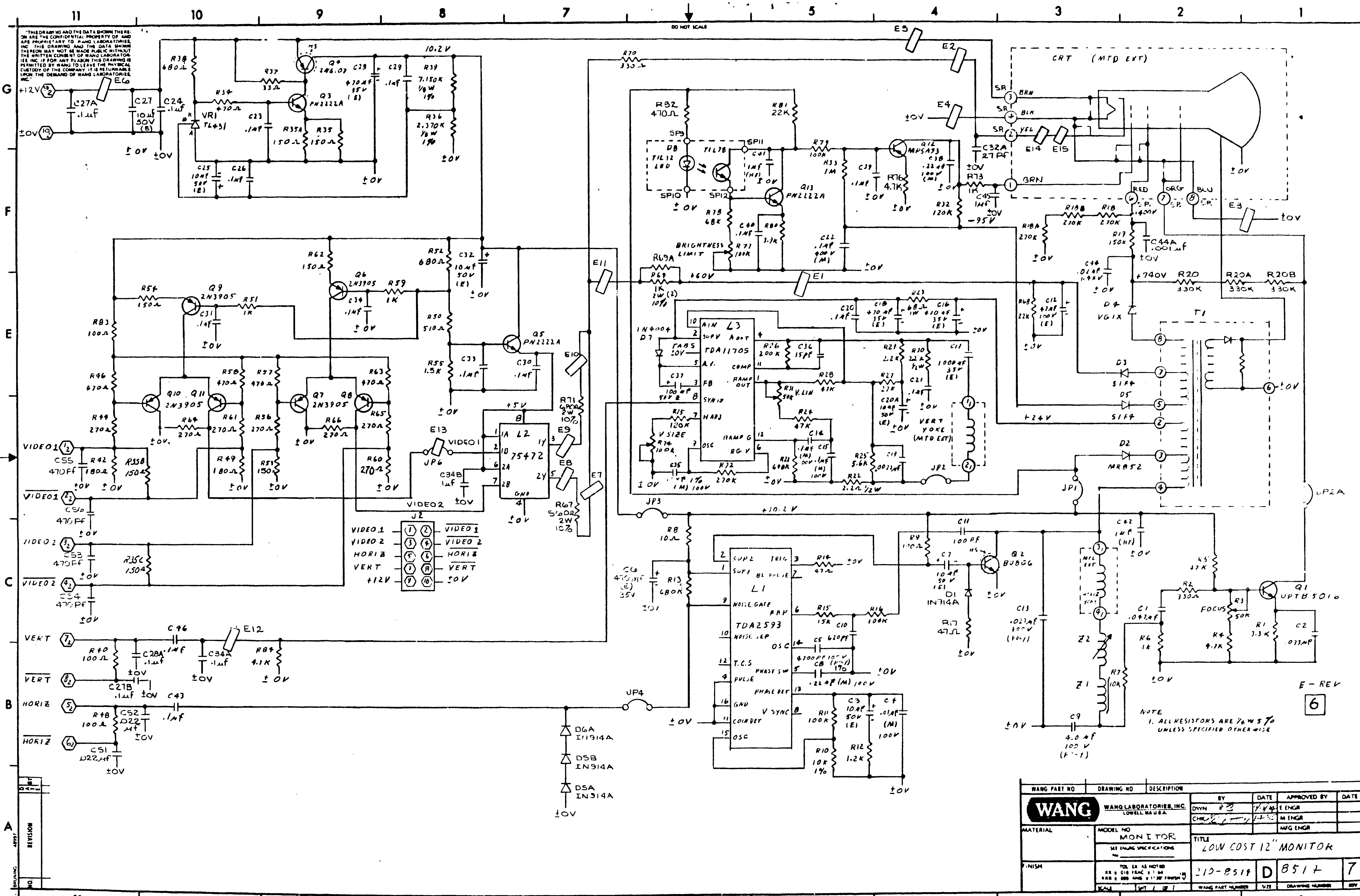
D 8509

REVISION

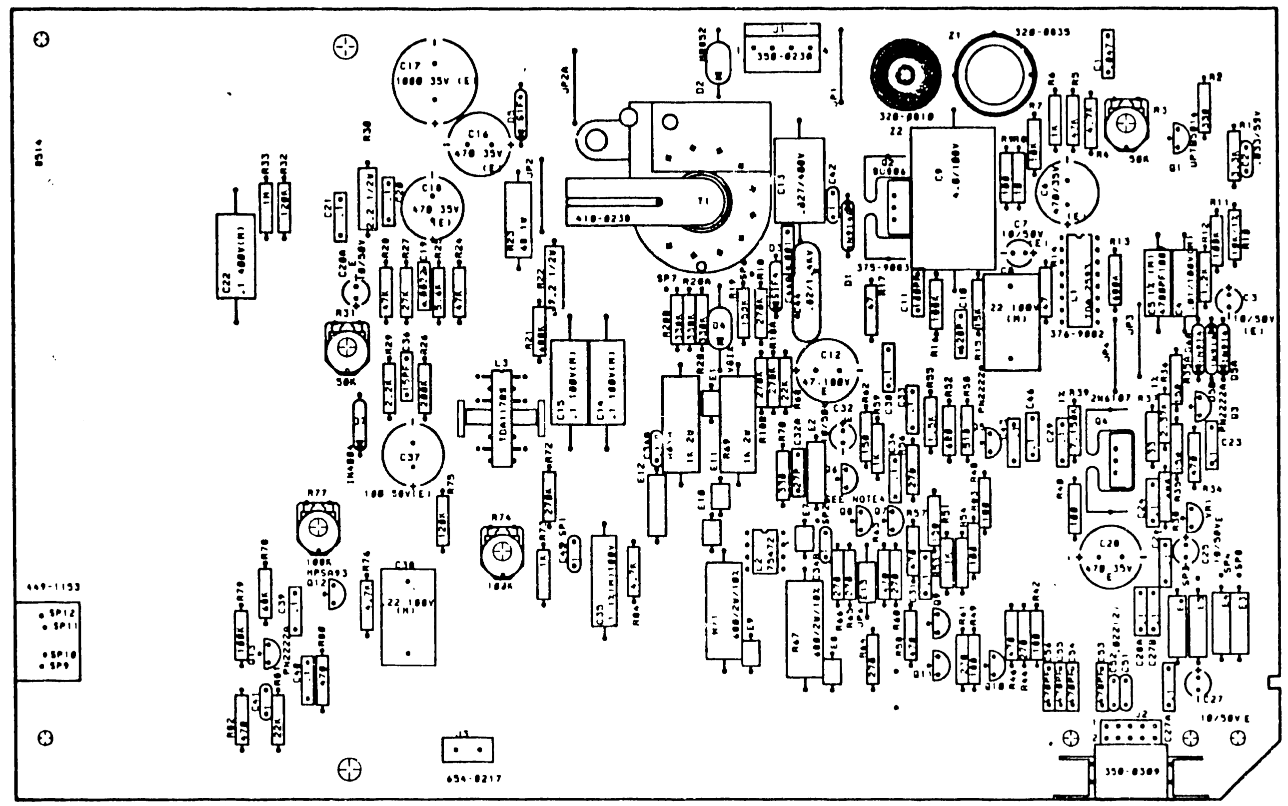


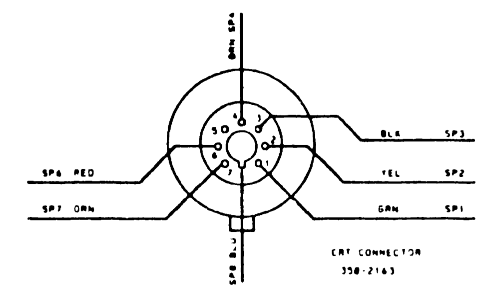
NOTE: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTORS ARE 1/4W, 5%, EXPRESSED IN OHMS.

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN M.T.	10/82	E ENGR	
		CHK		M ENGR	
		E C CONTROL		MFG ENGR	
MATERIAL	MODEL NO. 928MC PH0217C SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE SE 8 PORT APA TERM ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED	210-8509 (WANG PART NUMBER)	C (SIZE)	8509 (DRAWING NUMBER)	4 (REV)
	SCALE 1/1 SHT OF				



DO NOT SCALE
CRT (MTD EXT)
NOTE
1. ALL RESISTORS ARE 1/4W 5% UNLESS SPECIFIED OTHERWISE
E-REV
6
WANG
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
MODEL NO
MONITOR
TITLE
LOW COST 12" MONITOR
210-8514
D
8514
7



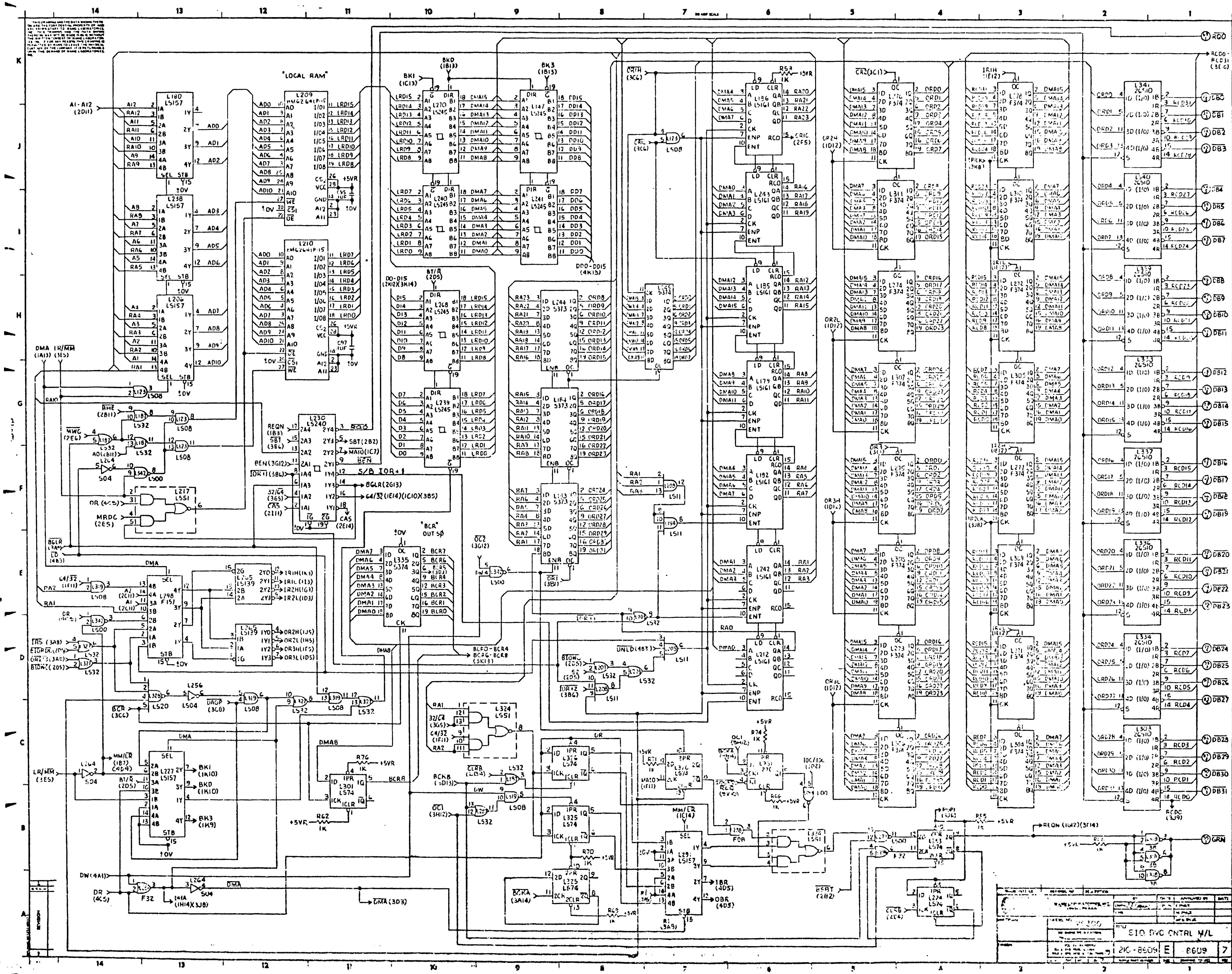


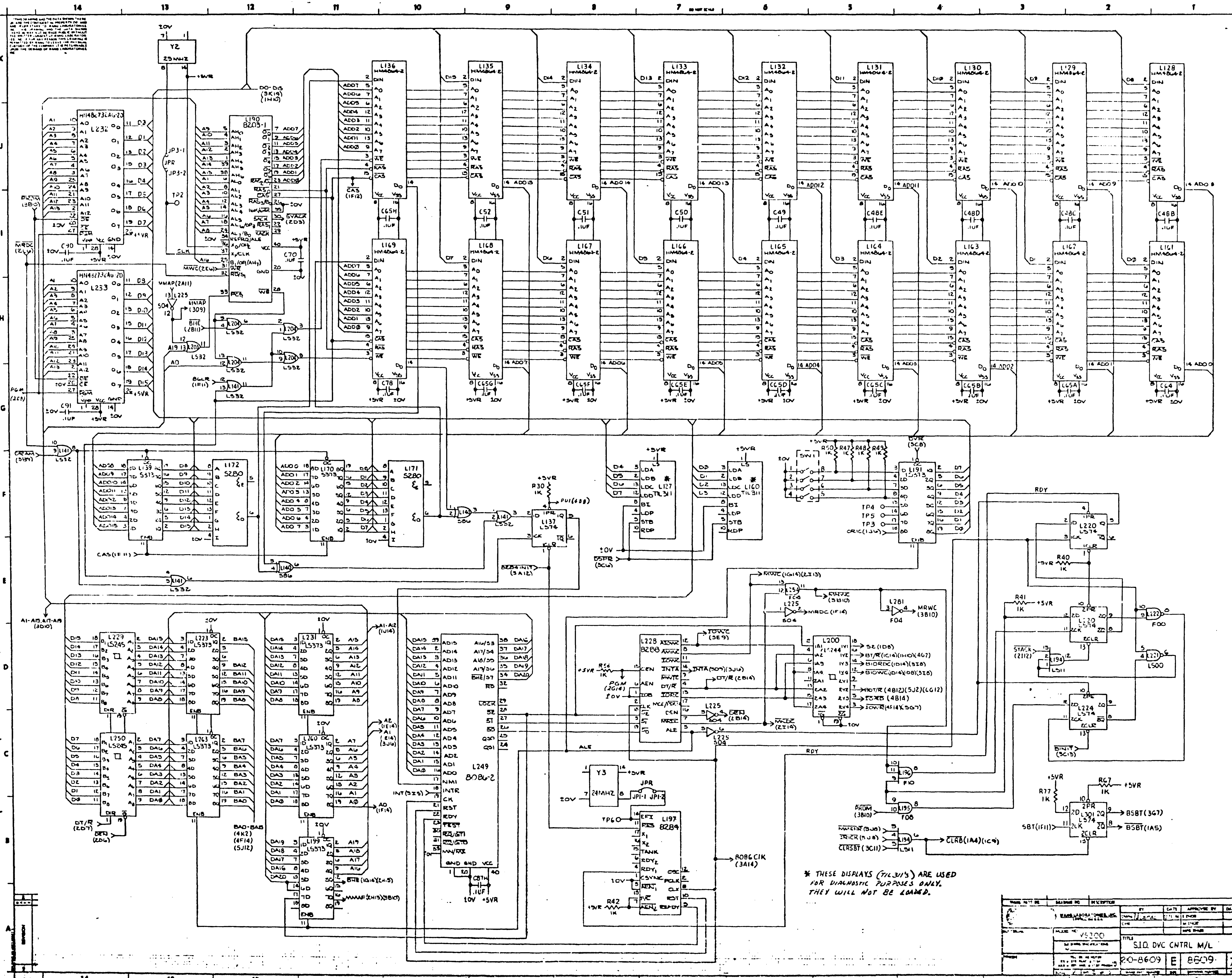
J2.2 — R35B 150 — J2.1

J2.4 — R35C 150 — J2.3

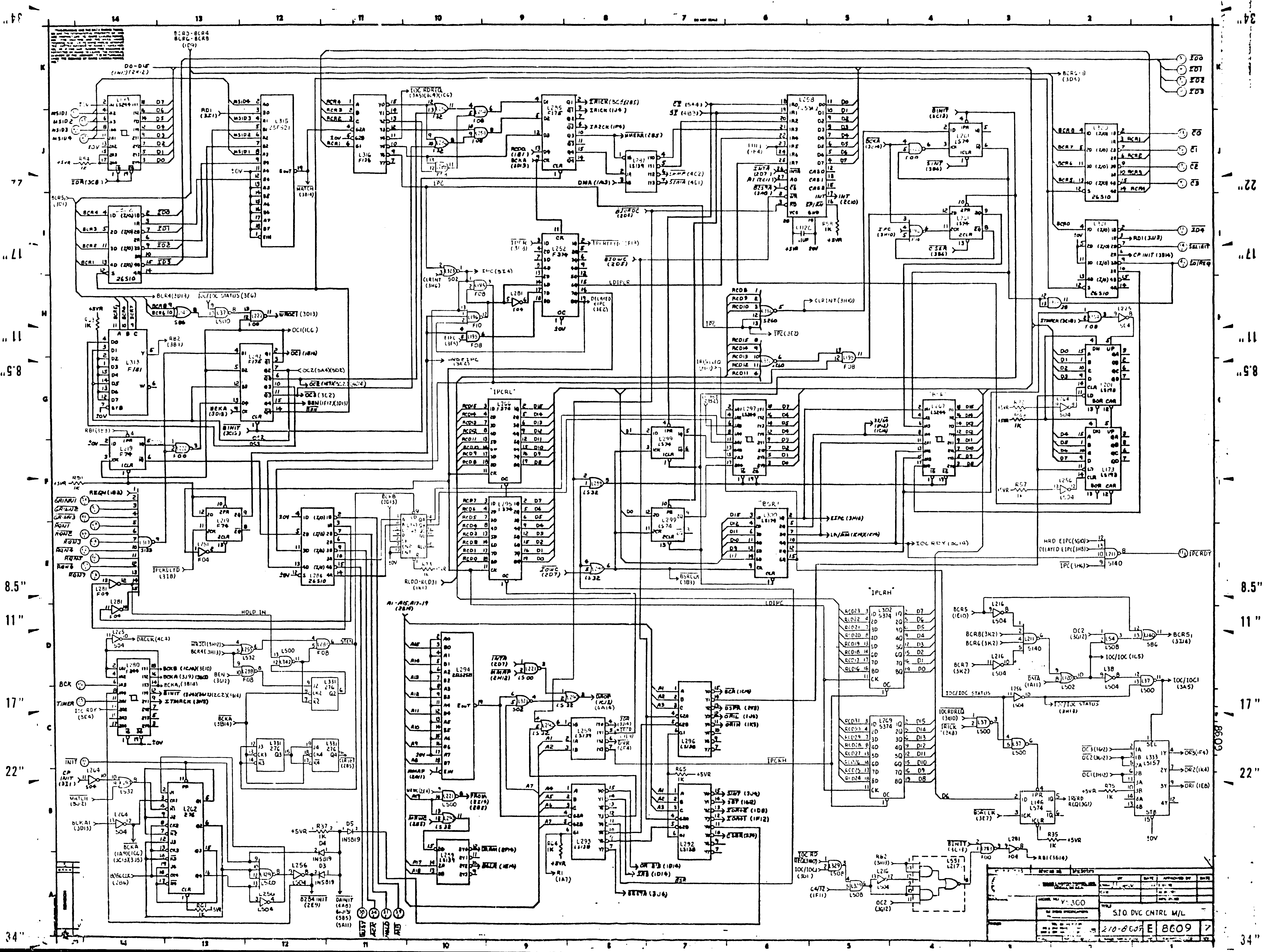
NOTES.
1. UNLESS OTHERWISE SPECIFIED.
ALL CAPACITORS ARE EXPRESSED IN MICROFARADS.
ALL RESISTORS ARE 1/4W 5% EXPRESSED IN OHMS.
ALL TRANSISTORS ARE 2N3905.
2. INSTALL HEATSINK 376-9066 AT L3.
3. E2-E6, E12 ARE WPN 410-1016 (6PLCS).
E1, E7-E11 ARE WPN 410-1017 (6PLCS).
4. INSTALL FERRITE BEAD (410-1023) TO E13, AT JP6 AND E14, 15 AT SP2.

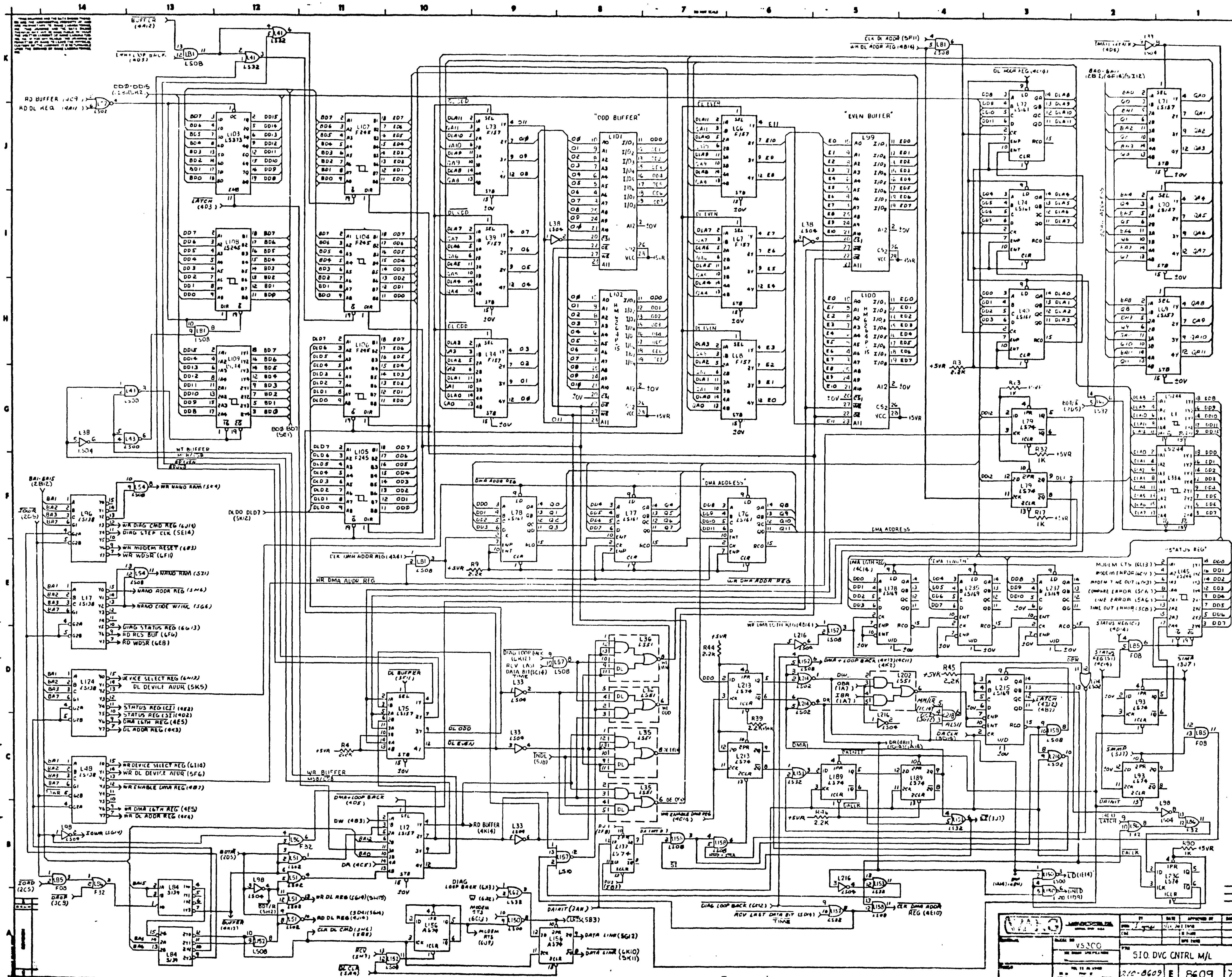
WANG LABORATORIES INC. LOWELL MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN TCP	12/10/84	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. MONITOR	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE LOW COST 12" MONITOR ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED	210-8514	C	8514	6
	SCALE 1/1 SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV


"LOCAL RAM"
L209 HM6264P-15
L210 HM6264P-15
L180 LS157
L238 LS157
L206 LS157
L230 LS240
L270 LS245
L147 LS245
L240 LS245
L241 LS245
L268 LS245
L239 LS245
L244 S373
L164 S373
L335 S374
"BCR" OUT S0
L298 F151
L245 LS139
L265 LS139
L227 LS157
L301 LS74
L324 LS51
L217 LS51
L186 LS161
L243 LS161
L185 LS161
L179 LS161
L192 LS161
L242 LS161
L212 LS161
L291 LS157
L341 26S10
L340 26S10
L337 26S10
L333 26S10
L336 26S10
L334 26S10
L303 26S10
REQN (1G12)(3F14)
GRN
VS 300
S10 DVC CNTRL M/L
210-8609
E
8609
7

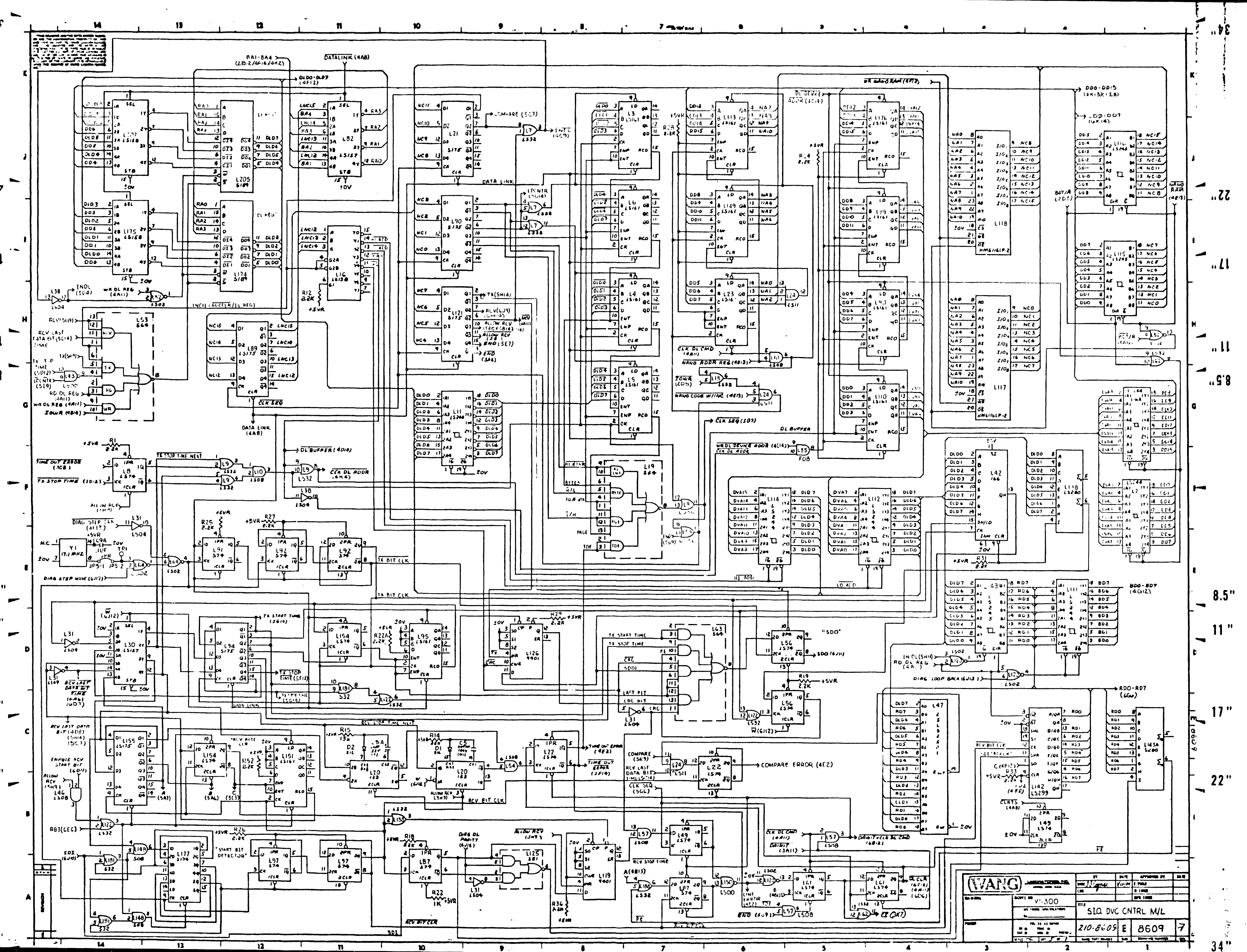


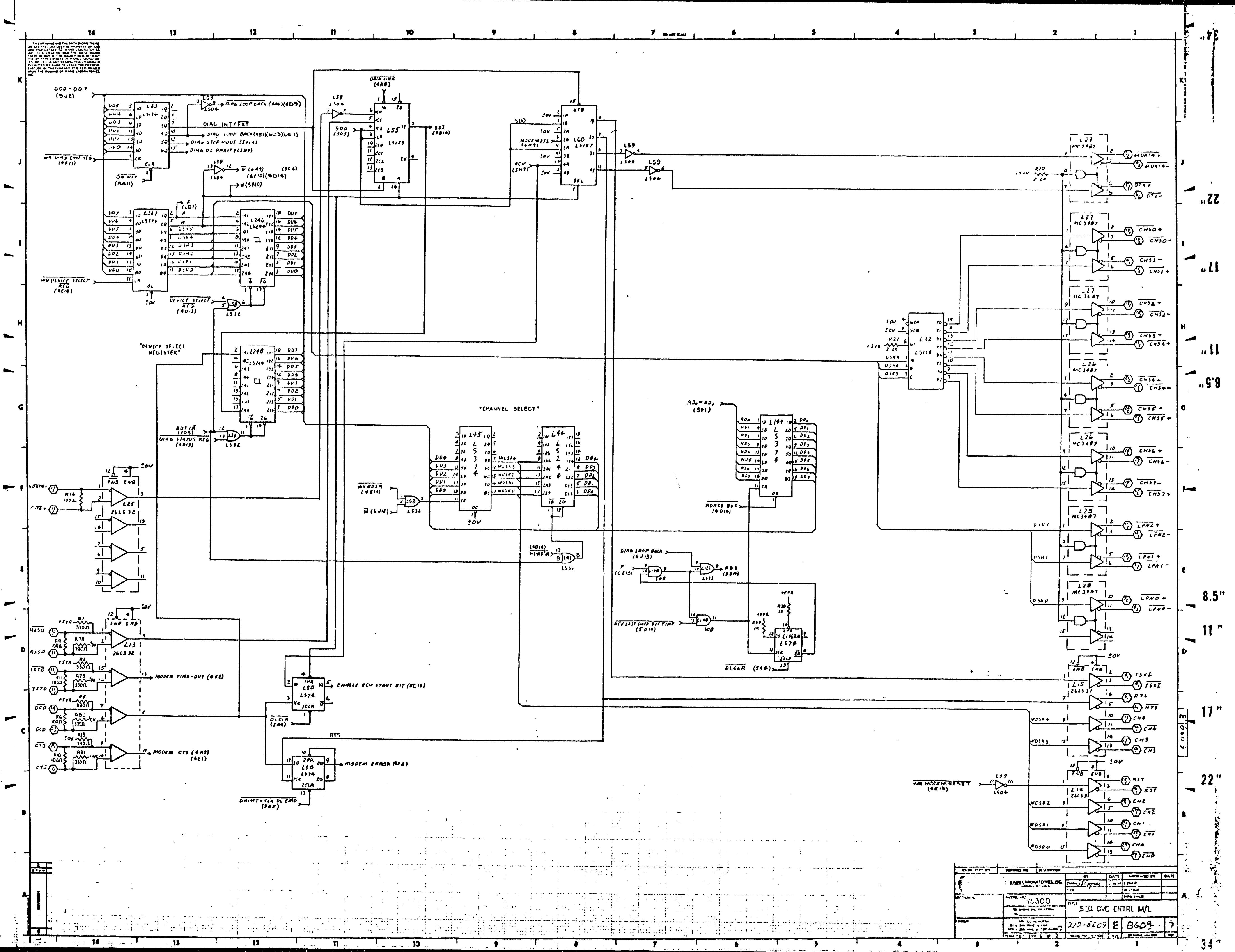
* THESE DISPLAYS (TIL311'S) ARE USED FOR DIAGNOSTIC PURPOSES ONLY. THEY WILL NOT BE LOADED.
L232 HN46273CAU-20
L233 HN46273CAU-20
L190 8203-1
L139 LS373
L172 5280
L170 LS373
L171 5280
L137 LS74
L127 TIL311
L160 TIL311
L191 LS373
L220 LS74
L228 8288
L200 LS244
L249 8086-2
L197 8284
L229 LS245
L250 LS245
L223 LS373
L263 LS373
L231 LS373
L260 LS373
L199 LS373
Y2 25MHZ
Y3 24MHZ
8086 CLK (3A14)
WANG LABORATORIES, INC.
MODEL NO. VS300
TITLE SIO DVC CNTRL M/L
20-8609
E
8609
7


SIO DVC CNTRL M/L
210-8609
E
8609
7



"ODD BUFFER"
"EVEN BUFFER"
"DMA ADDRESS"
"STATUS REG"
DMA ADDRESS
VS300
S.I.O. DVC CNTRL M/L
210-8609
E
8609
7

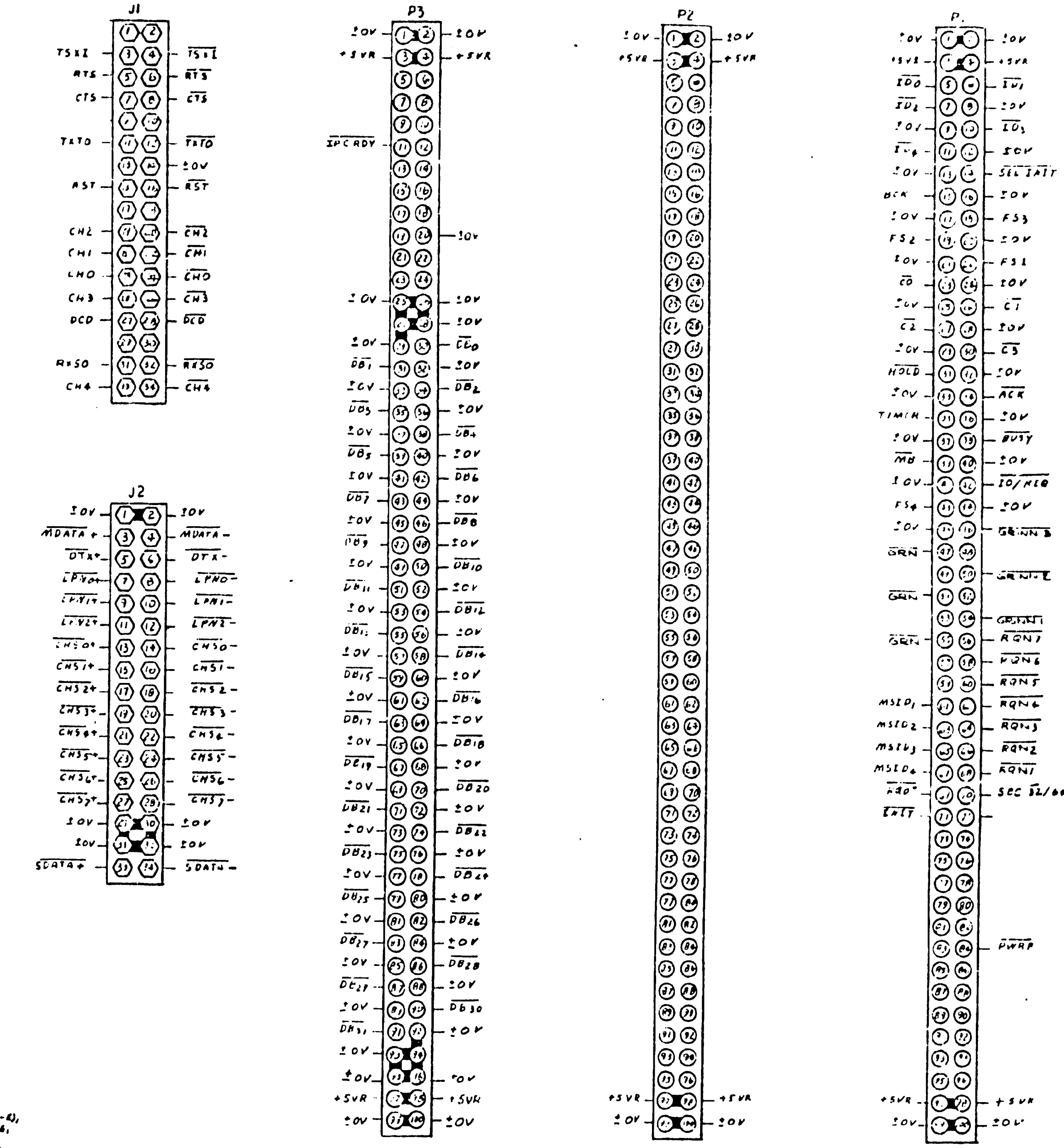

WANG
V-300
SIO DVC CNTRL M/L
210-8609
E
8609
7

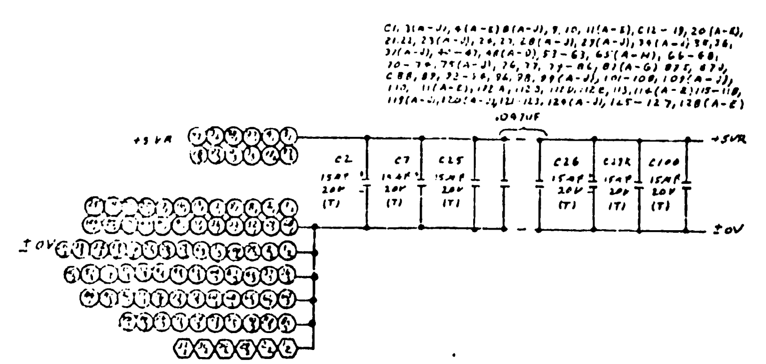


"DEVICE SELECT REGISTER"
"CHANNEL SELECT"
DIAG INT/EXT
DIAG LOOP BACK
DIAG STEP MODE
DIAG DL PARITY
ENABLE RCV START BIT
MODEM TIME-OUT
MODEM CTS
MODEM ERROR
WR MODEM RESET
DLCLR
RTS
300
SIO DVC CNTRL M/L
210-6609
E
8609
7

IC TYPE	LOCATION	SPARES
74LS00	L43	3
	L239	1
74S02	L123	1
74LS02	L32	2
	L64	2
	L323	3
74S04	L225	1
	L291	1
74LS04	L31	1
	L33	3
	L98	4
	L256	1
74S08		
	L289	1
74LS08	L10	2
	L46	3
	L329	2
74LS10	L157	2
74S32	L191	1
74LS32	L?	1
	L62	2
	L141	2
	L128	2
	L255	3
74F32	L96	1
74S51	L125	1
74LS51	L202	1
74S74	L91	1
74LS74	L3	1
	L49	1
	L146	1
	L224	1
	L308	1
74S139	L84	1
MC3487	L29	1
74ALS11	L218	2

MNEMONICS	COORD.
ACK	3A11
ADO- - AD2	6E1
ADO+ - AD2+	6D1
ACK	3D11
BUSY	3A11
[illegible] - C3	3J11
CHO - CH4	6B1
CHO - CH4	6B1
CTS	6C14
CTS	6C14
DBO - DB31	1K1
DCD	6C14
DCD	6C14
DTX+	6J1
DTX-	6J1
GRINN1 - GRINN3	3F14
GRN	1B1
HOLD	3A11
ID0 - ID3	3K1
ID4	3I1
INIT	3C14
IO/REG	3I1
ATP	3A11
MDATA+	6J1
MDATA-	6J1
MSID0 - MSID4	3J14
PGA0+ - PGA7+	6I1
PGA0- - PGA7-	6I1
REQN	1K1
RQN1 - RQN7	3E14
[illegible]	6B1
RST	6B1
RTS	6C1
RTS	6C1
RXSO	6D14
RXSO	6D14
SEC 32/64	3I1
SEL INIT	3I1
SDATA+	6F14
SDATA-	6F14
TIMER	3C14
TXST	6D1
TXST	6D1
TXTO	6D14
TXTO	6D14





NOTE:
1. ALL RES ARE 1/4W 5%
UNLESS OTHERWISE
SPECIFIED

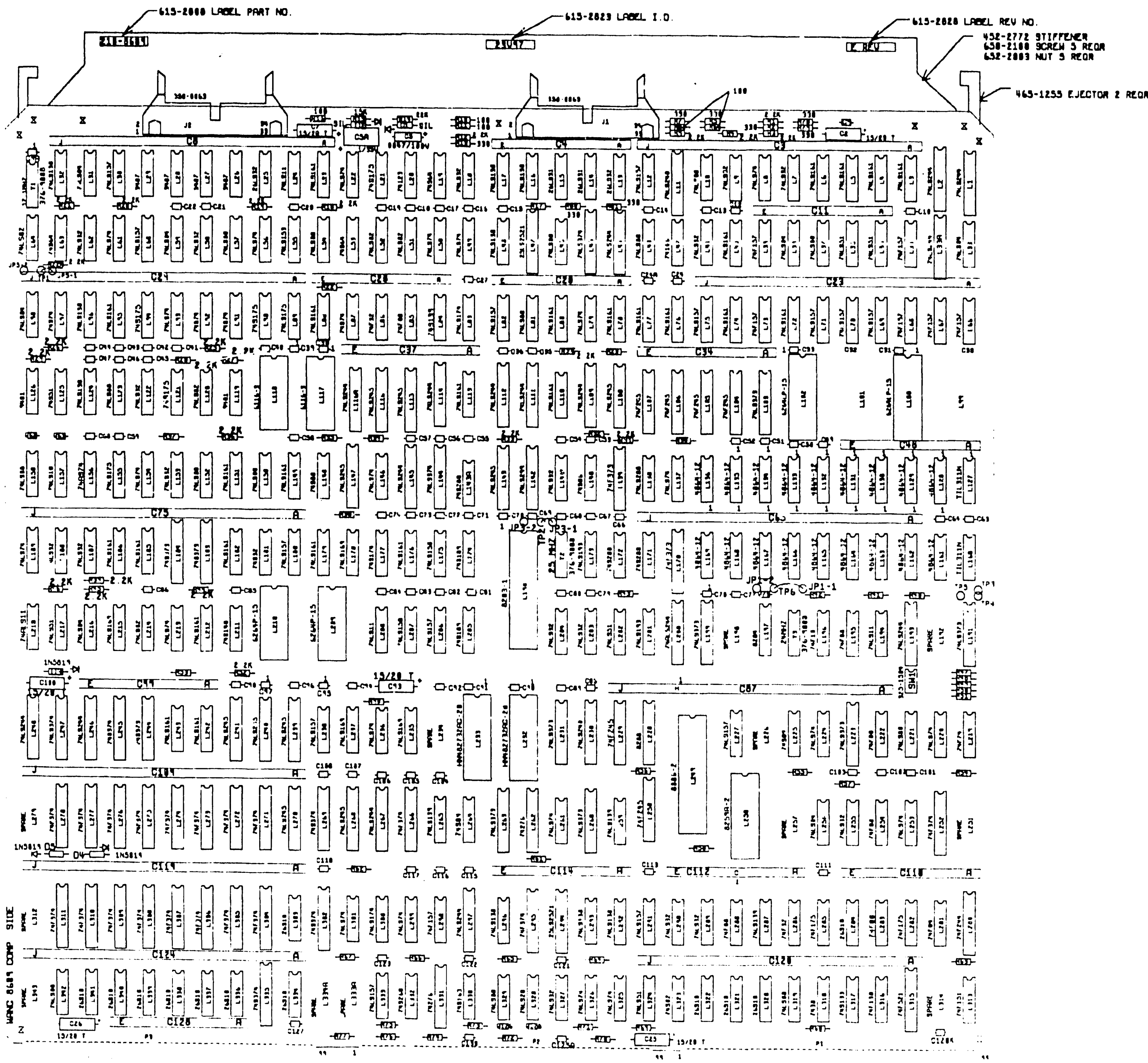
E-REV 4

VS300

SIO DVC CNTRL M/L

210-8607 E 8609 7

DO NOT SCALE



NOTES: UNLESS OTHERWISE SPECIFIED

1 ALL CAPACITORS ARE .047, EXPRESSED IN MICROFARADS
2 ALL RESISTORS ARE 1K, 1/4W, 5 PERCENT, EXPRESSED IN OHMS
3 L127, L160 LOAD 14 PIN SOCKETS WPN 376-9001
L232, L233 LOAD 28 PIN SOCKETS WPN 376-9015
L249 LOAD 40 PIN SOCKET WPN 376-9011
4 ALL JUMPERS ARE 24GA
5 USE TENKA PADS WPN 376-9008 UNDER Y1, Y2 AND Y3

WANG LABORATORIES, INC.		DRN D C	5/83	
		CHK D J CORBIN	5/85	
MATERIAL	MODEL NO VS300	TITLE ASSEMBLY DRAWING 910 DVC CNTRL M/L		
	SEE (WORD) SPECIFICATIONS NO 10-213			
FINISH	SCALE 1:1 SHT 1 OF 1	218-8609	D	8609 8

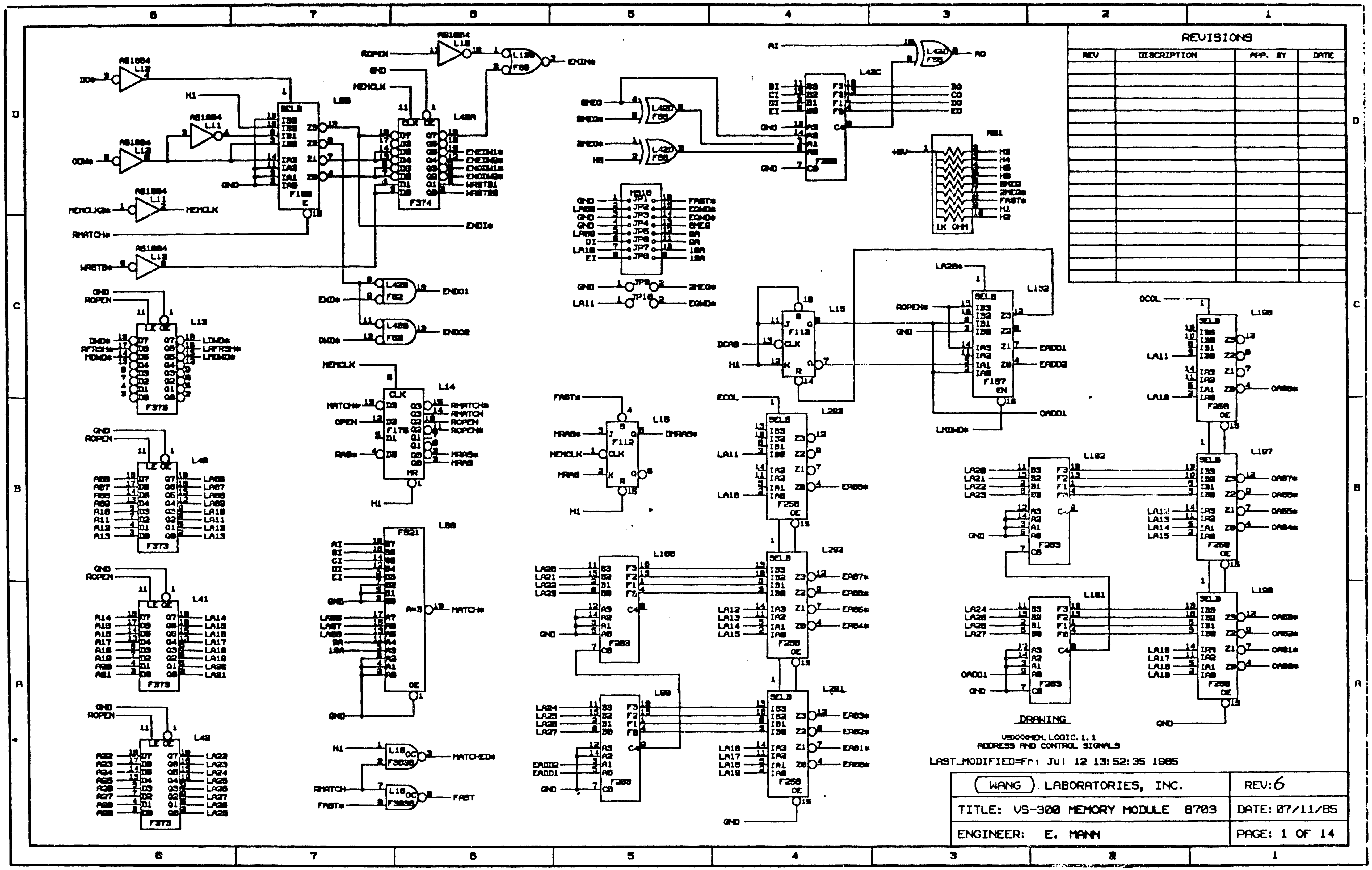
VS-300 MEMORY MODULE INDEX

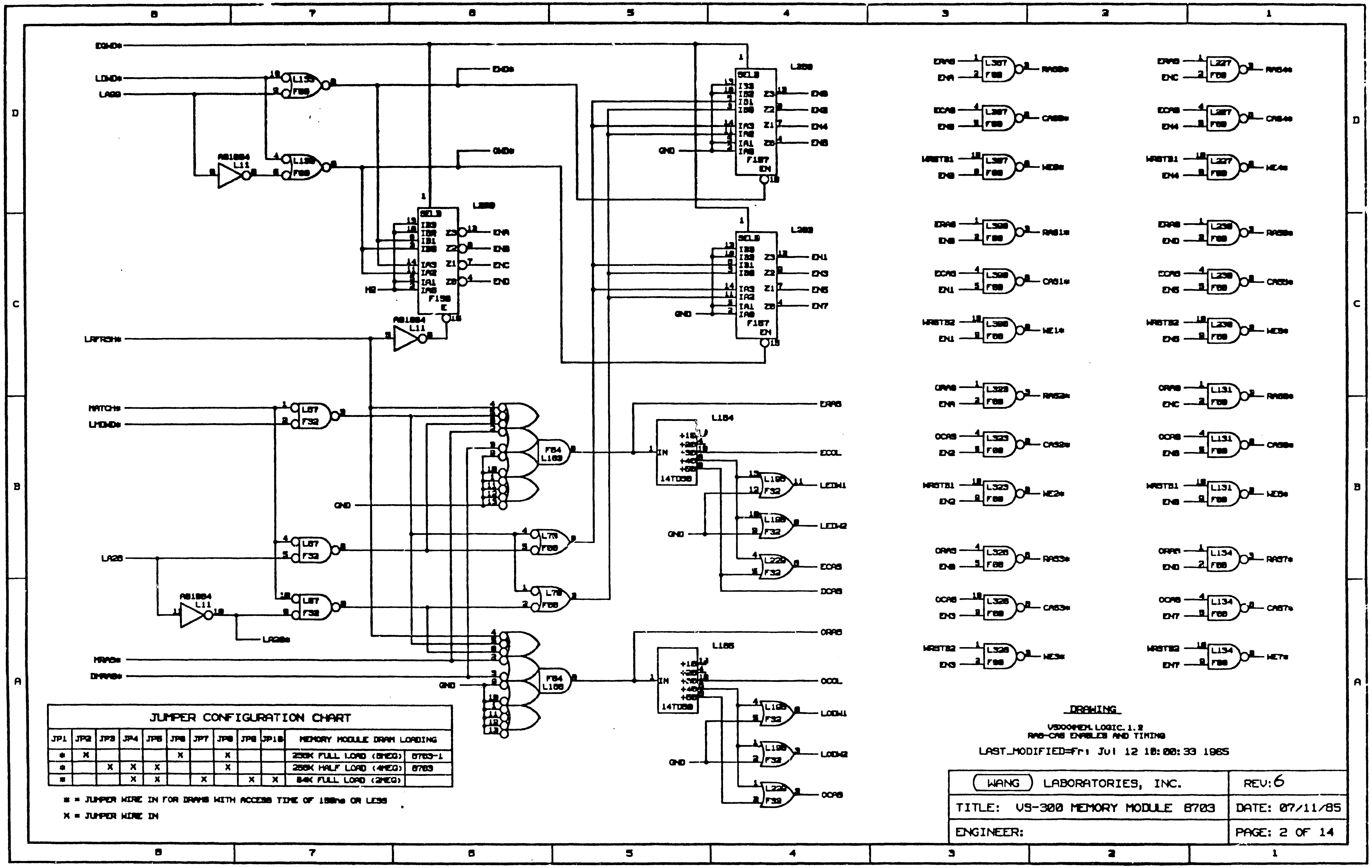
PAGE	CONTENTS
1.	ADDRESS MULTIPLEXERS AND CONTROLS
2.	RAS/CAS ENABLES AND TIMING CONTROLS
	JUMPER CONFIGURATION CHART
3.	DATA-IN LATCHES
4.	DATA-OUT LATCHES
5.	DATA-OUT MEMORY BUS DRIVERS
6.	39-BIT WORD ARRAY 0
7.	39-BIT WORD ARRAY 1
8.	39-BIT WORD ARRAY 2
9.	39-BIT WORD ARRAY 3
10.	39-BIT WORD ARRAY 4
11.	39-BIT WORD ARRAY 5
12.	39-BIT WORD ARRAY 6
13.	39-BIT WORD ARRAY 7
14.	INPUT/OUTPUT PIN LIST

E-REV 87Ø3 $\boxed{3}$ E-REV 87Ø3-1 $\boxed{3}$

DRAWING
VS300MEM.IDX.1.1
INDEX PAGE
LAST_MODIFIED=Fri Jul 12 08:35:18 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 0 OF 14


REVISIONS
REV
DESCRIPTION
APP. BY
DATE
DRAWING
VSXXXMEM.LOGIC.1.1
ADDRESS AND CONTROL SIGNALS
LAST_MODIFIED=Fri Jul 12 13:52:35 1985
WANG LABORATORIES, INC.
REV:6
TITLE: VS-300 MEMORY MODULE 8703
DATE: 07/11/85
ENGINEER: E. MANN
PAGE: 1 OF 14



JUMPER CONFIGURATION CHART											
JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8	JP9	JP10	MEMORY MODULE DRAM LOADING	
*	X				X		X			256K FULL LOAD (8MEG)	8703-1
*		X	X	X			X			256K HALF LOAD (4MEG)	8703
*			X	X		X		X	X	64K FULL LOAD (2MEG)	

* = JUMPER WIRE IN FOR DRAMS WITH ACCESS TIME OF 150ns OR LESS

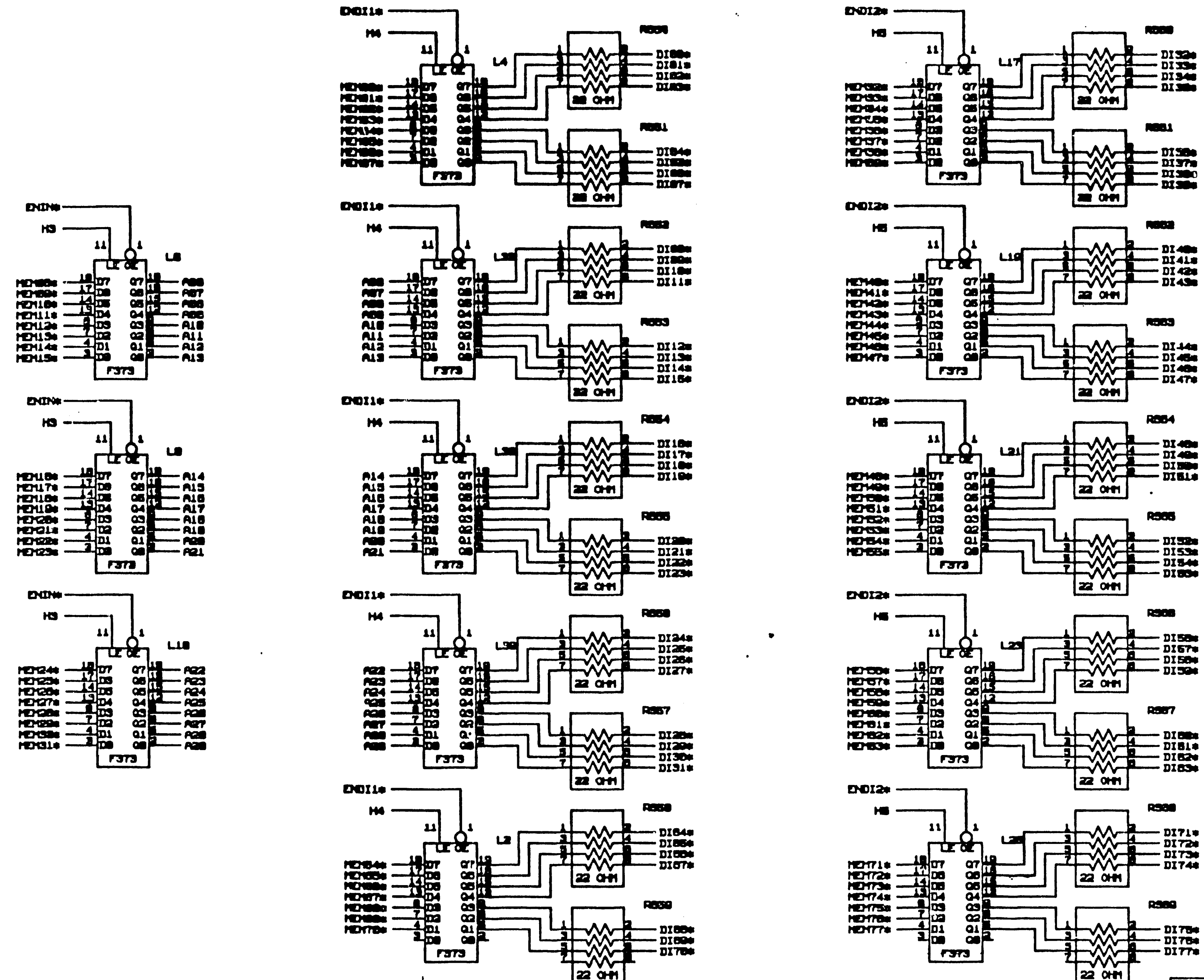
X = JUMPER WIRE IN

DRAWING

VS300MEM.LOGIC.1.2
RAS-CAS ENABLES AND TIMING

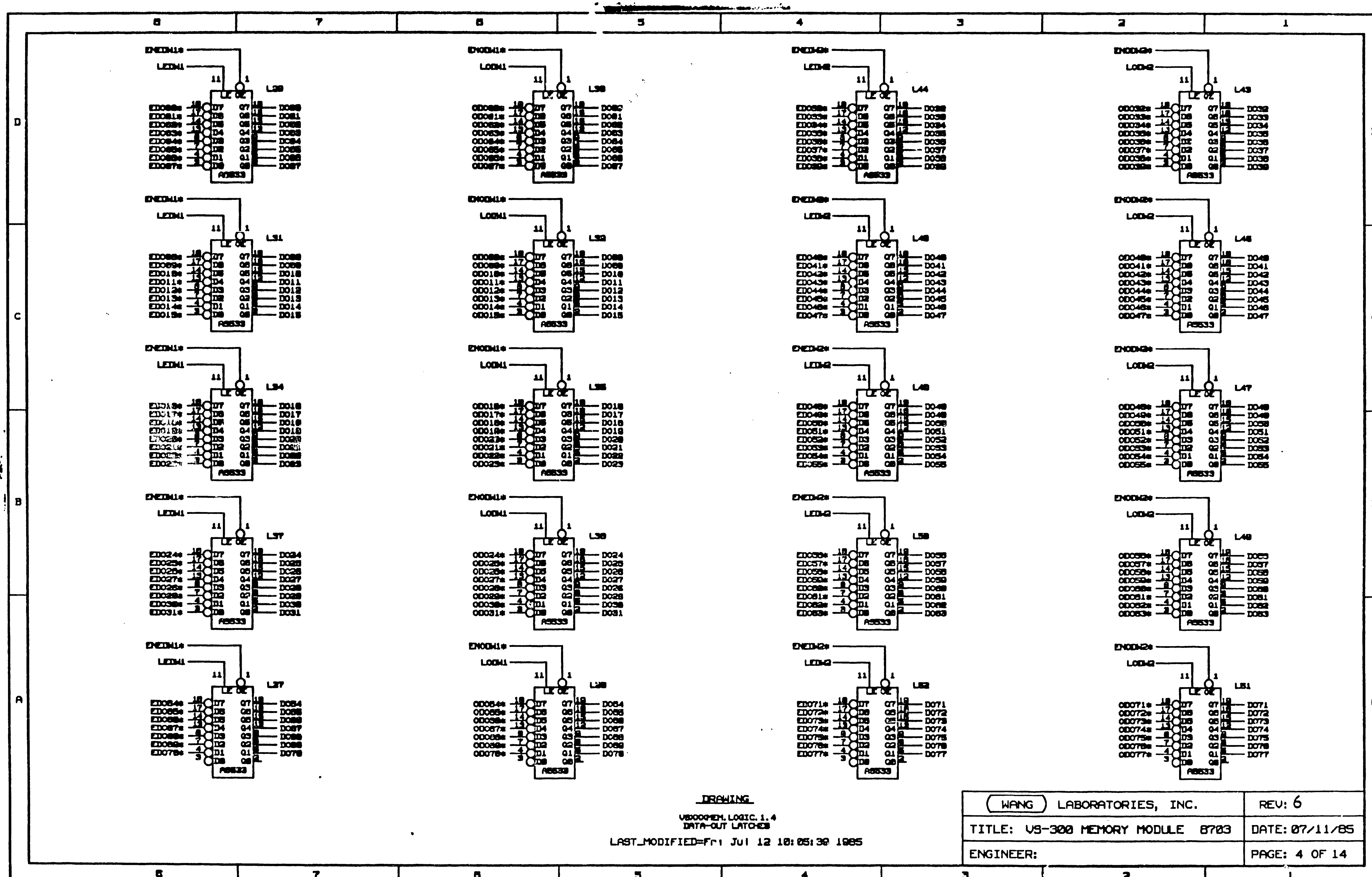
LAST_MODIFIED=Fri Jul 12 10:00:33 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 2 OF 14



DRAWING
VS300MEM.LOGIC.1.3
DATA-IN LATCHES
LAST_MODIFIED=Fri Jul 12 10:03:01 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 3 OF 14

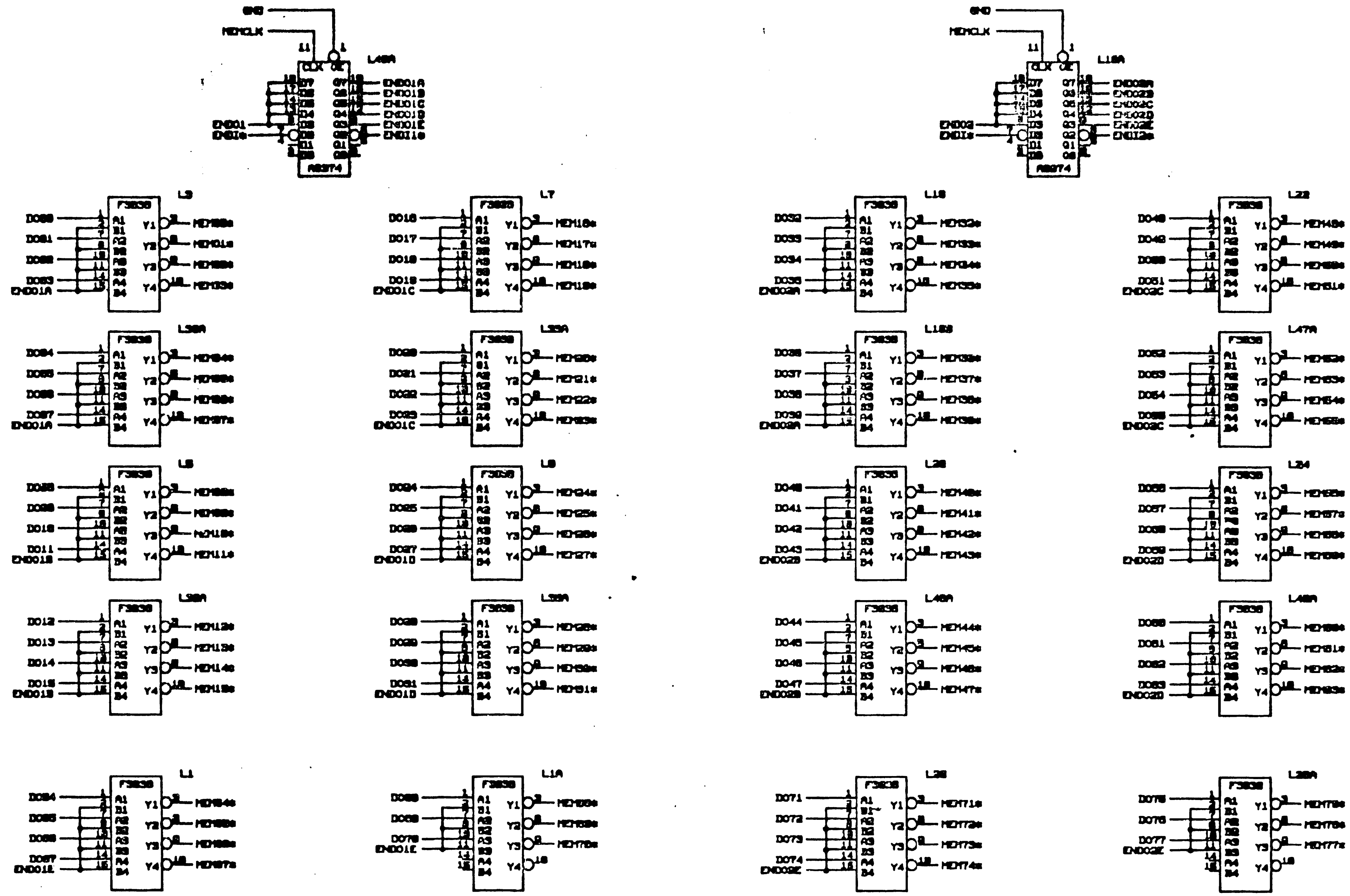


DRAWING

VS00XMEM.LOGIC.1.4
DATA-OUT LATCHES

LAST_MODIFIED=Fri Jul 12 10:05:30 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 4 OF 14

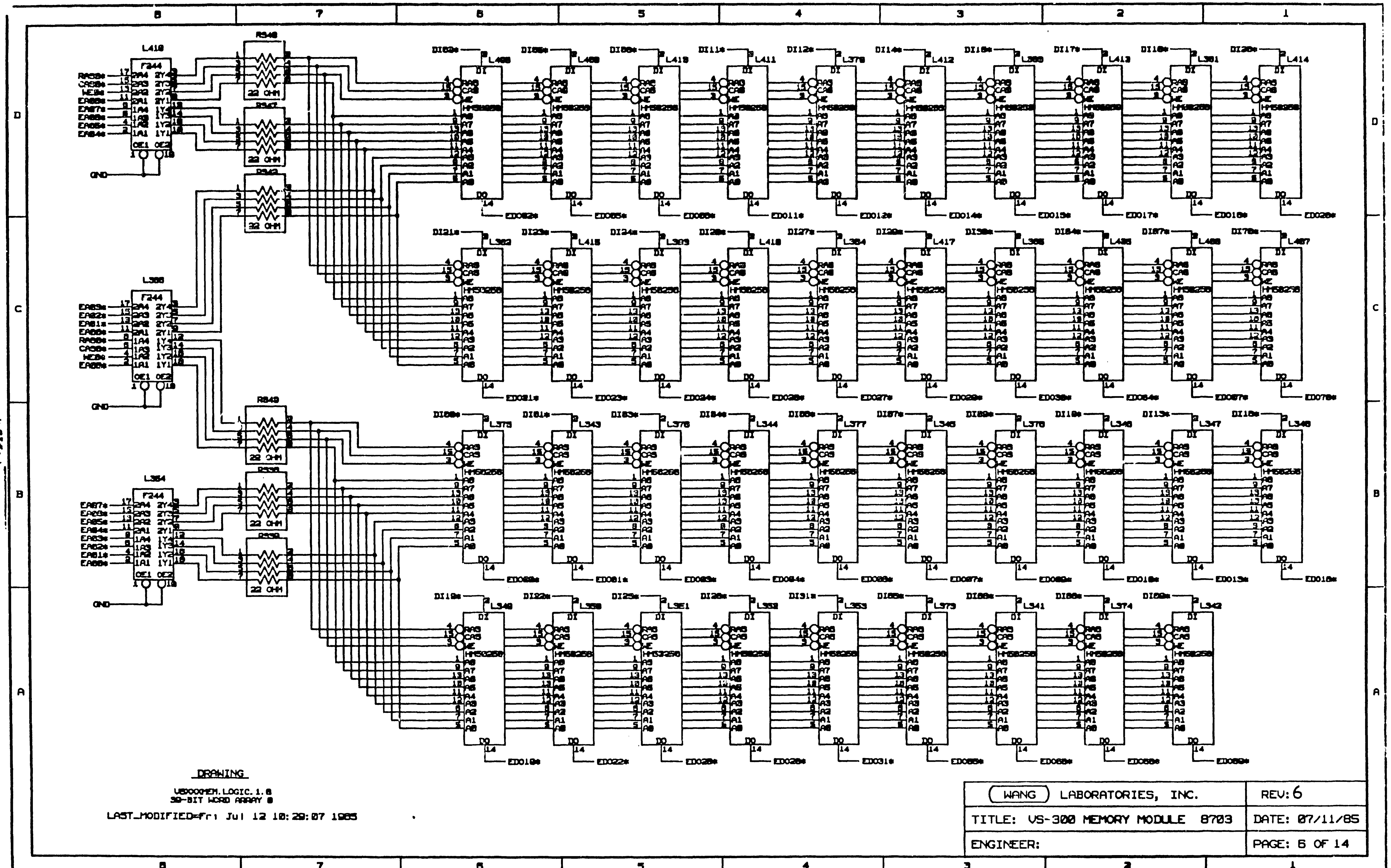


DRAWING

VS300MEM.LOGIC.1.5
DATA-OUT MEMBUS DRIVERS

LAST_MODIFIED=Fri Jul 12 10:08:35 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 5 OF 14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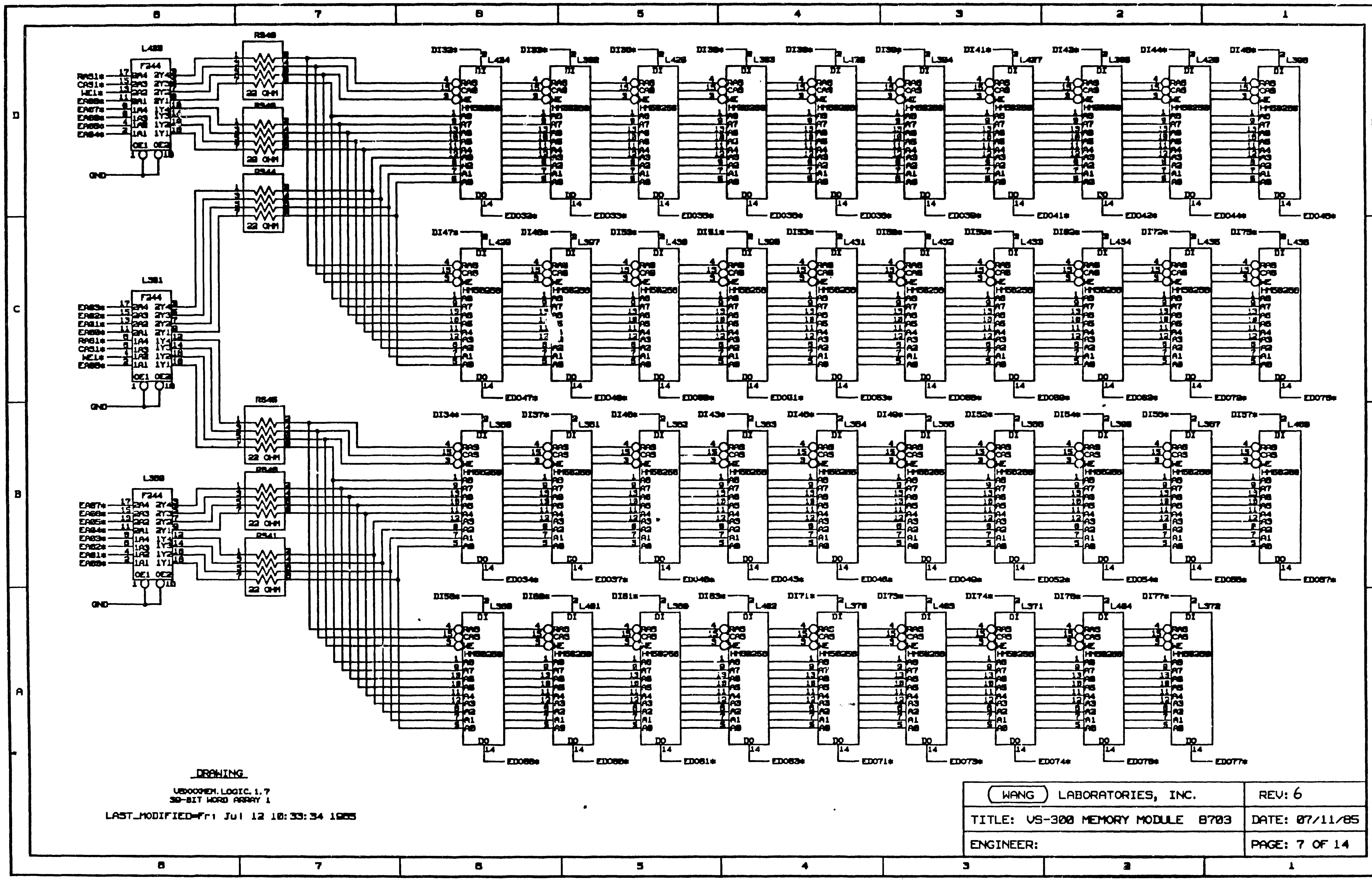
39-BIT WORD ARRAY 0
LAST_MODIFIED=Fri Jul 12 10:29:07 1985
WANG LABORATORIES, INC.
REV: 6
TITLE: VS-300 MEMORY MODULE 8703
DATE: 07/11/85
ENGINEER:
PAGE: 6 OF 14

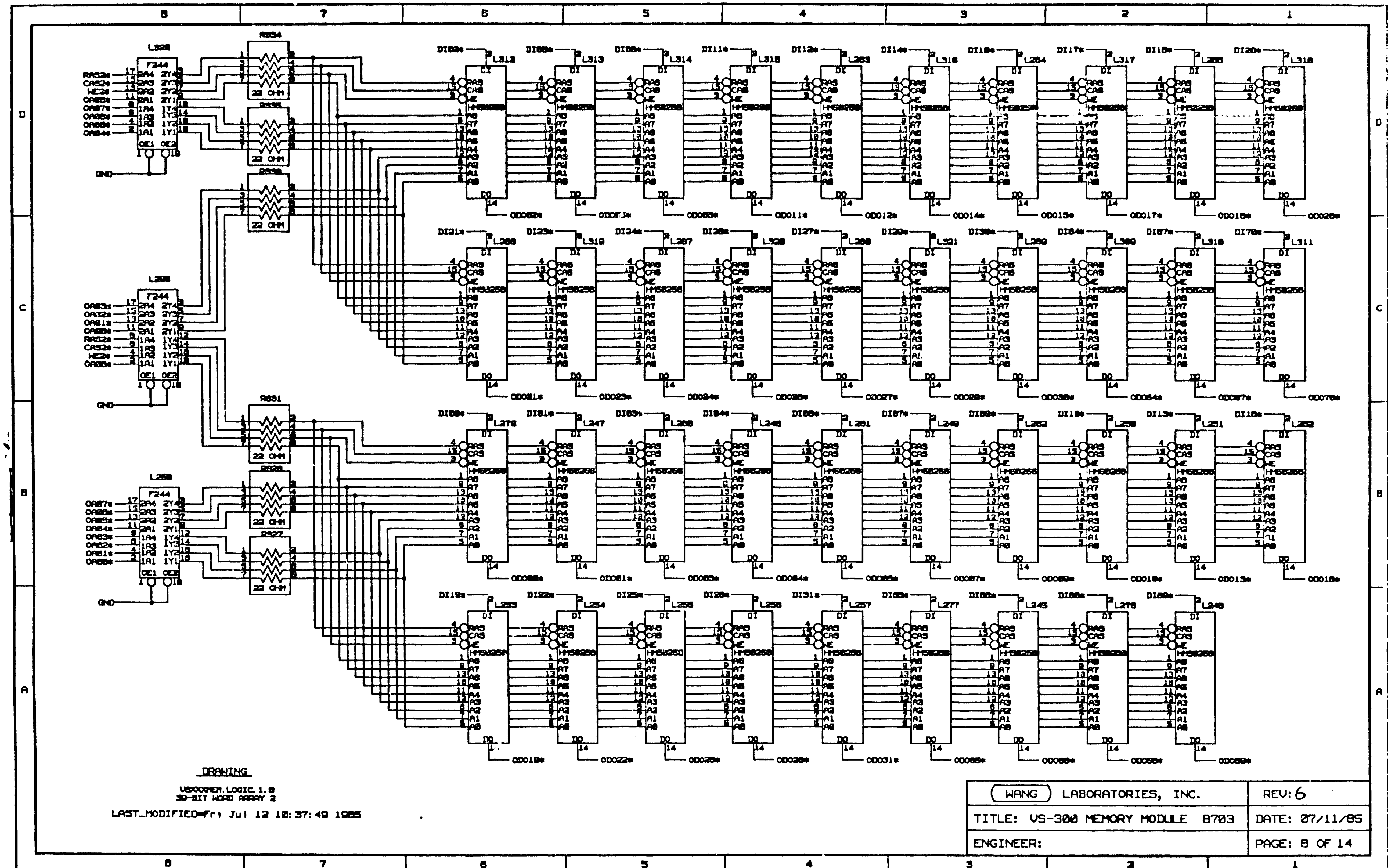


DRAWING

VSOOOMEM.LOGIC.1.7
39-BIT WORD ARRAY 1

LAST_MODIFIED=Fri Jul 12 10:33:34 1985

(WANG) LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 7 OF 14

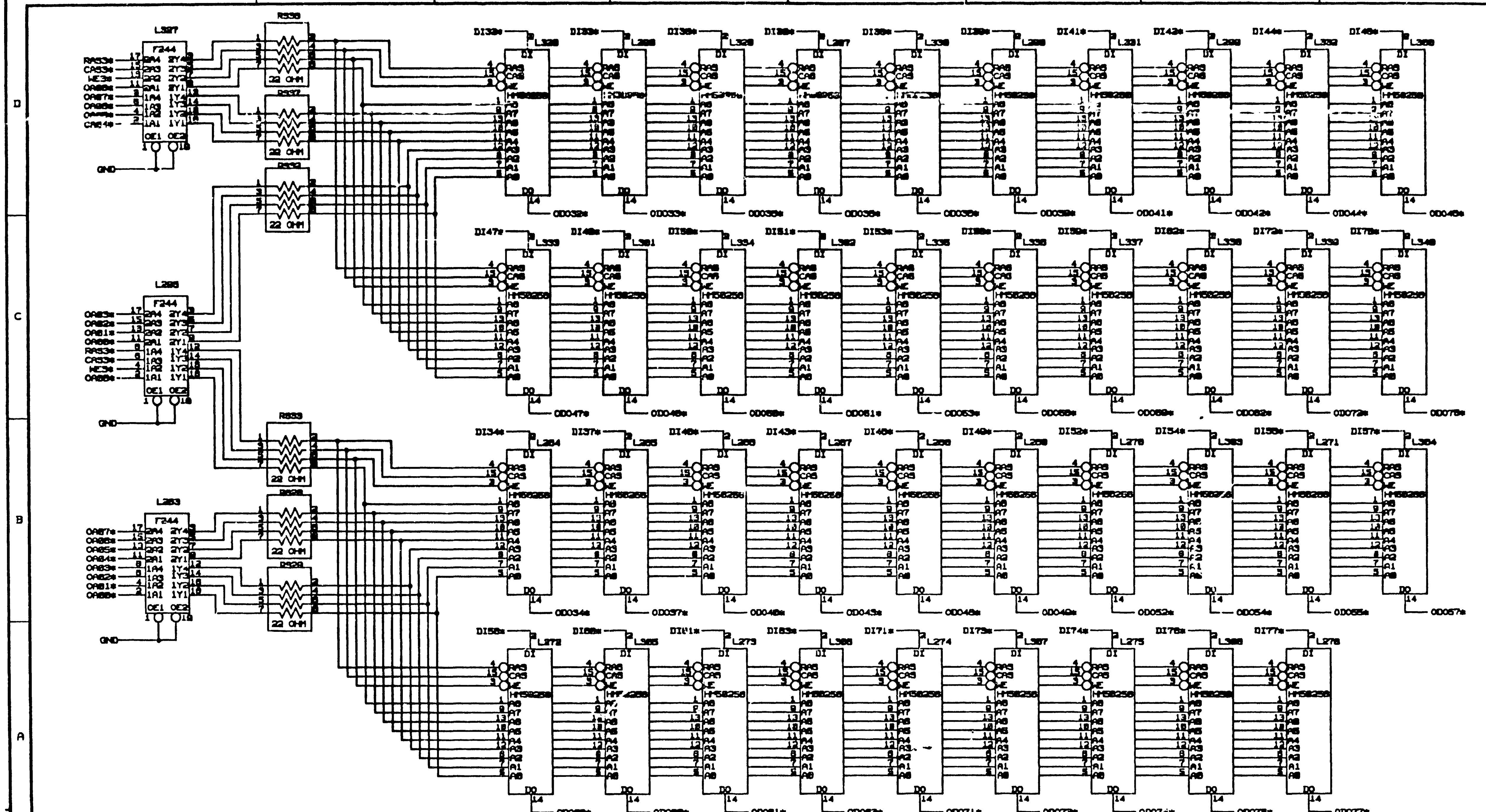


DRAWING

VS00MEM.LOGIC.1.8
39-BIT WORD ARRAY 2

LAST_MODIFIED=Fri Jul 12 10:37:49 1985

(WANG) LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 8 OF 14

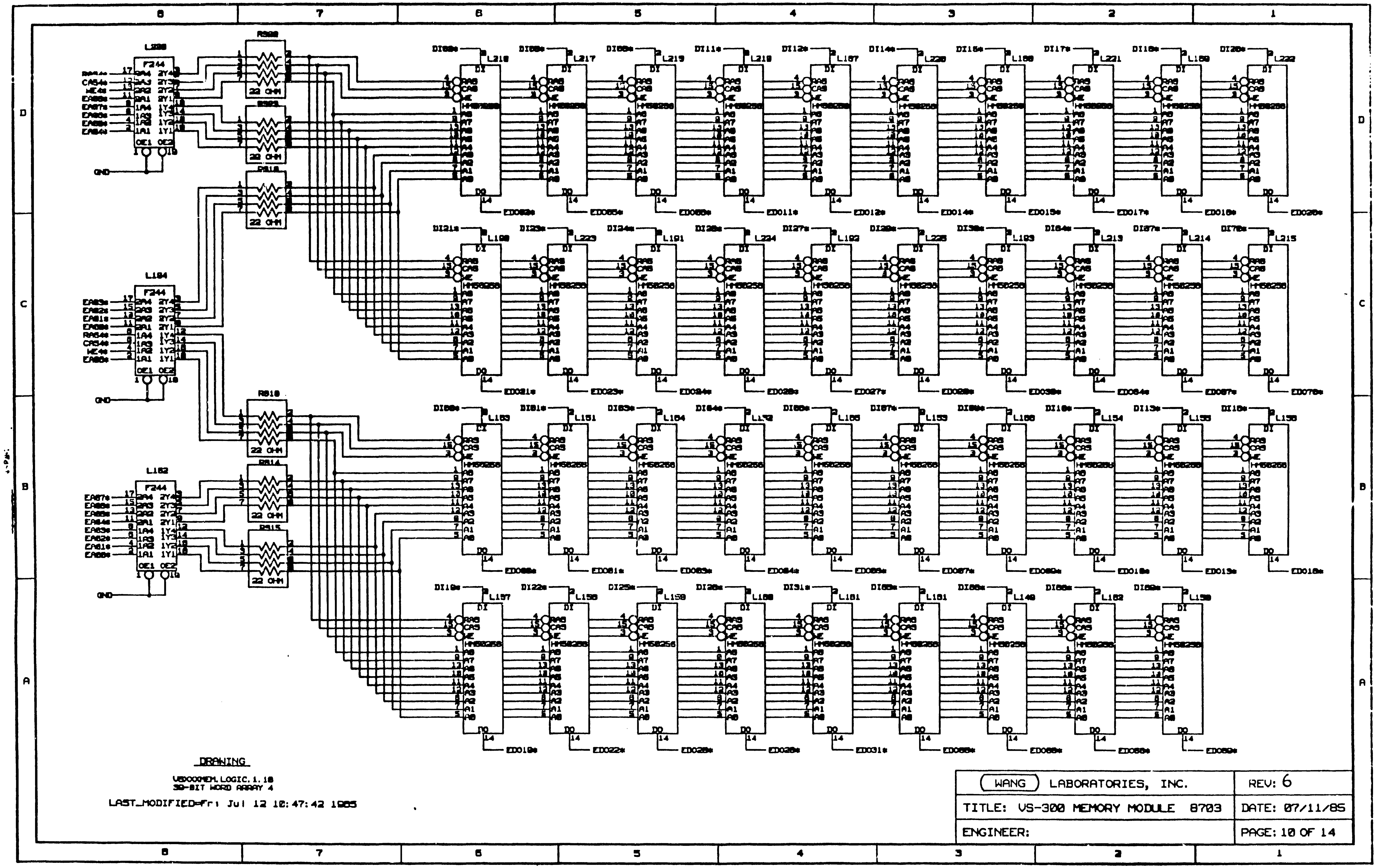


DRAWING

VS00OMEM.LOGIC.1.0
39-BIT WORD ARRAY 3

LAST_MODIFIED=Fri Jul 12 10:42:17 1985

(WANG) LABORATORIES, INC.	REV: 6.
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 9 OF 14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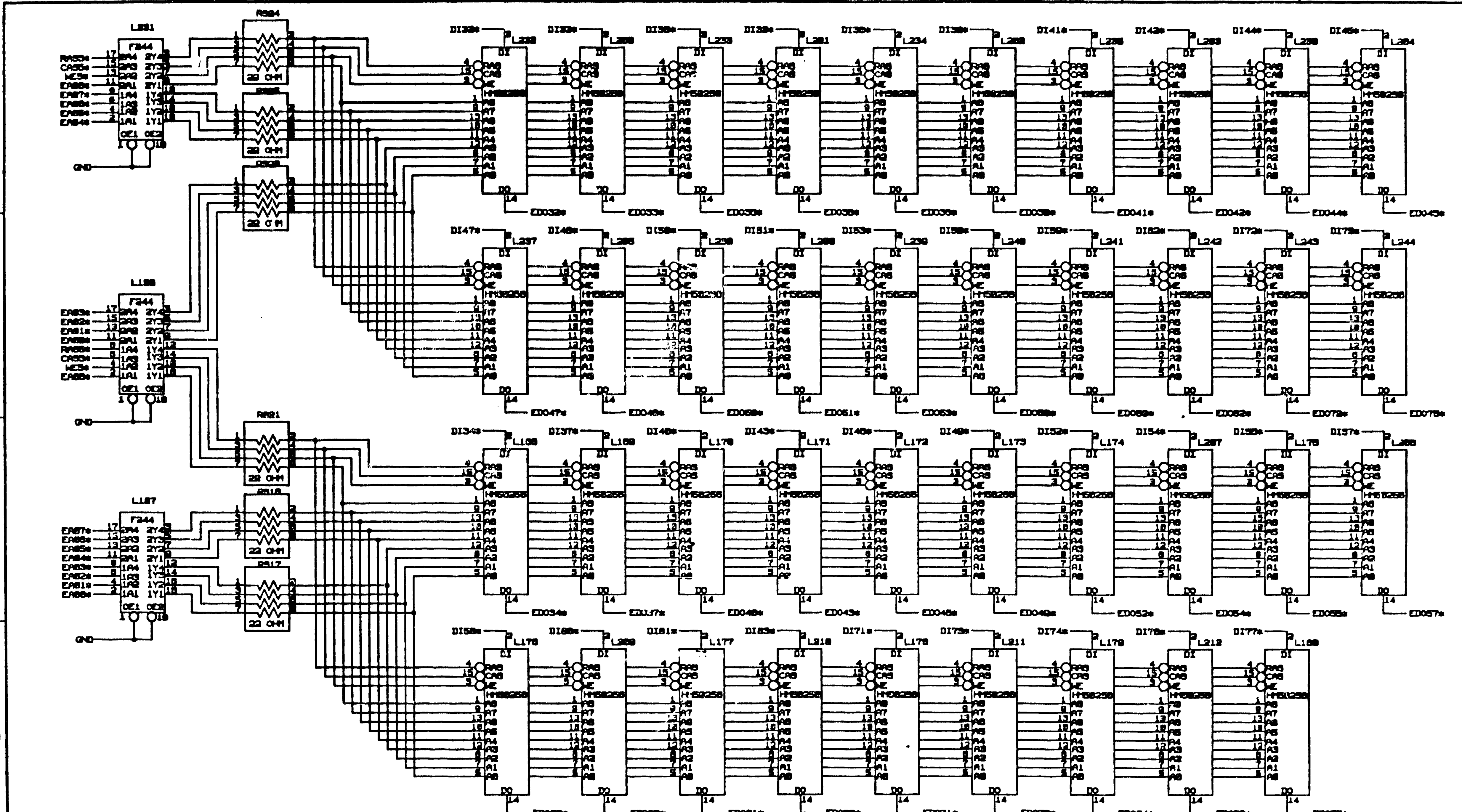
VS000MEM.LOGIC.1.10
36-BIT WORD ARRAY 4
LAST_MODIFIED=Fri Jul 12 10:47:42 1985
WANG LABORATORIES, INC.
REV: 6
TITLE: VS-300 MEMORY MODULE 8703
DATE: 07/11/85
ENGINEER:
PAGE: 10 OF 14

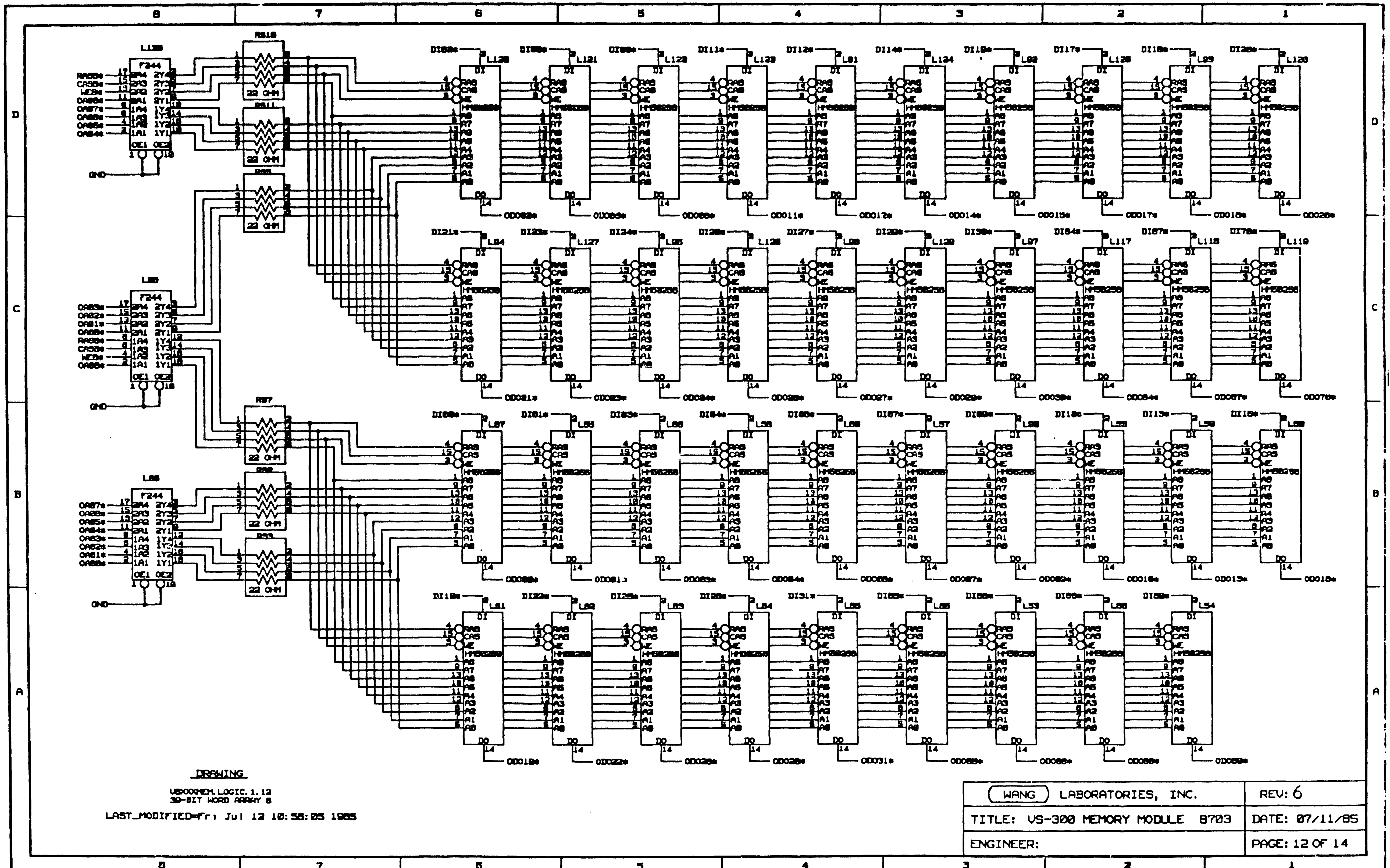


DRAWING

VS300MEM.LOGIC.1.11
39-BIT WORD ARRAY 5

LAST_MODIFIED=Fri Jul 12 10:51:54 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 11 OF 14

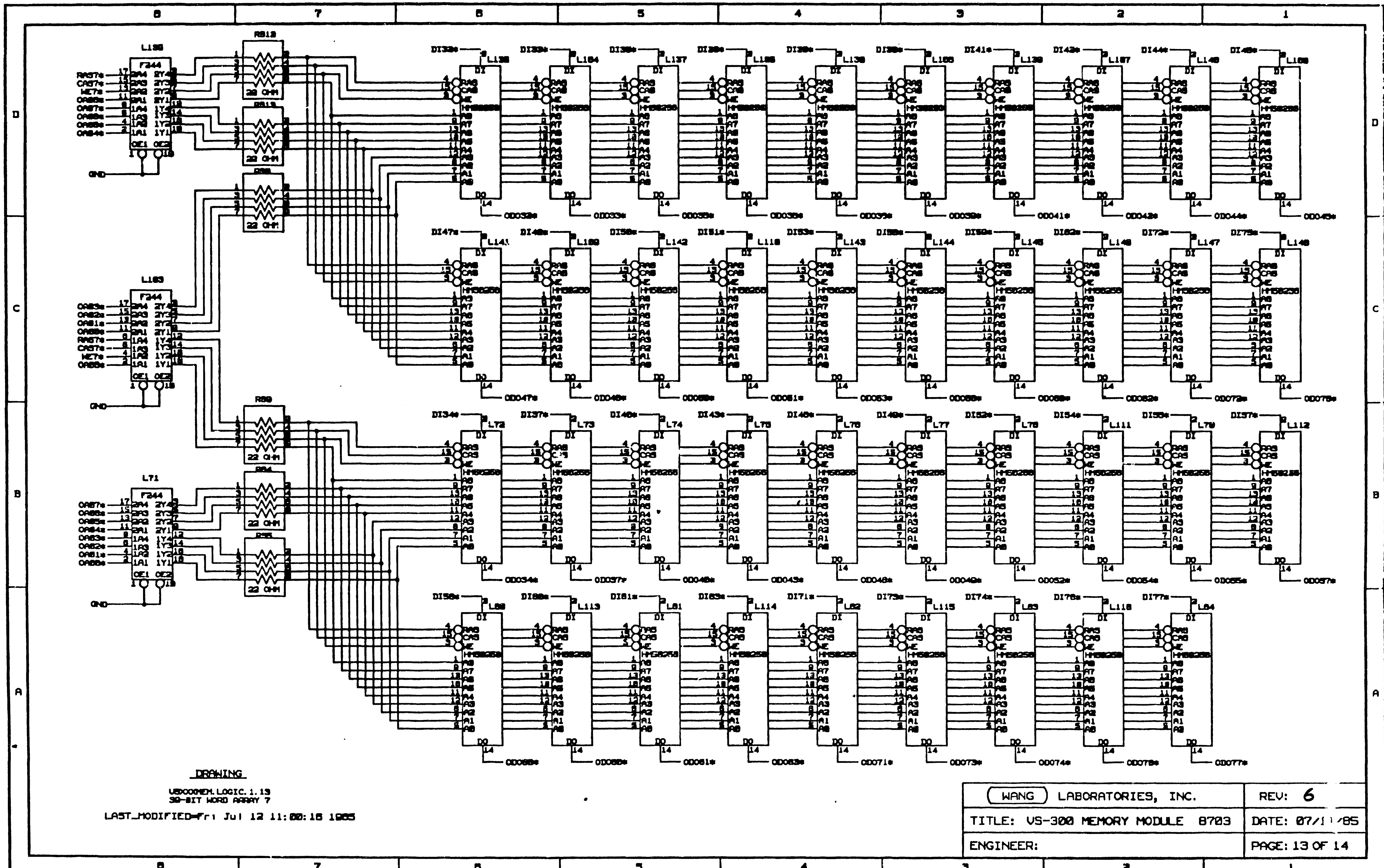


DRAWING

VS000MEM.LOGIC.1.12
38-BIT WORD ARRAY 8

LAST_MODIFIED=Fri Jul 12 10:58:05 1985

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 12 OF 14

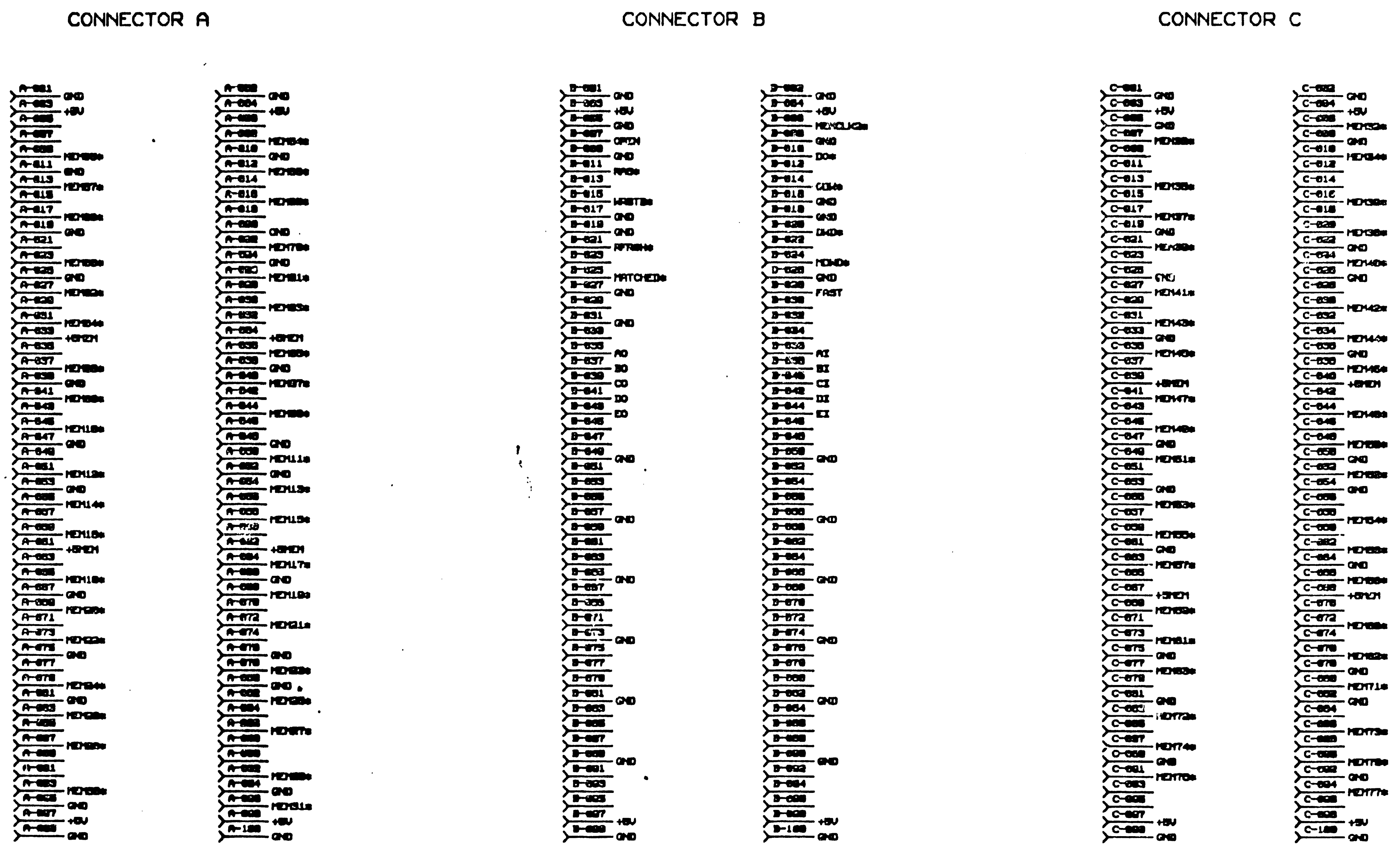


DRAWING

VSOOOMEM.LOGIC.1.13
39-BIT WORD ARRAY 7

LAST_MODIFIED=Fri Jul 12 11:00:16 1985

(WANG) LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/1?/85
ENGINEER:	PAGE: 13 OF 14

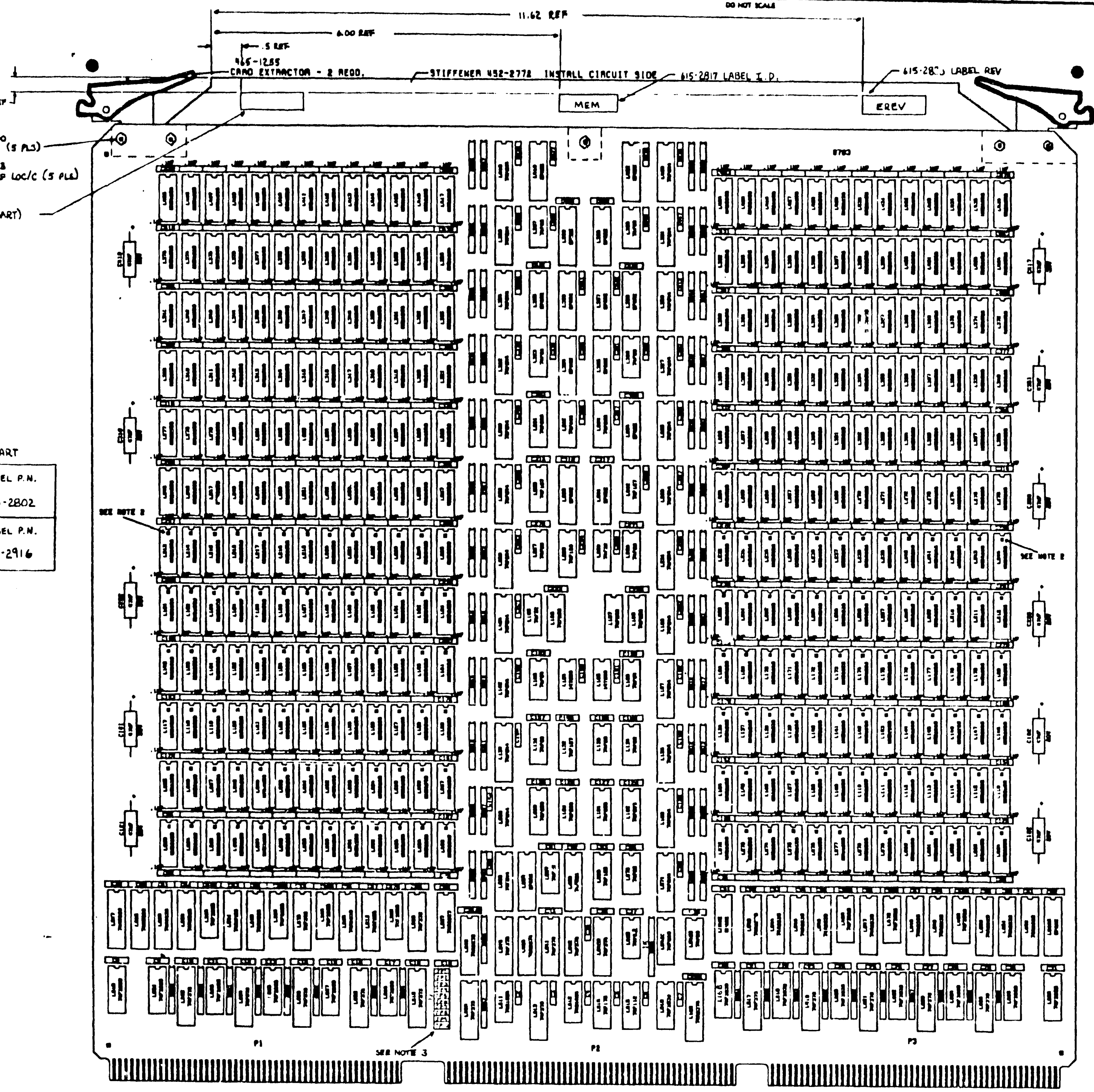


DRAWING

VS300MEM.LOGIC.1.14
FINGER CONNECTIONS

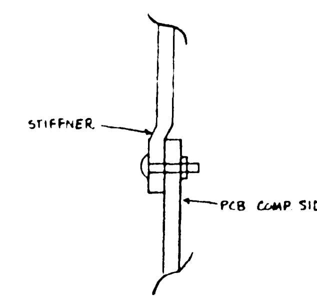
LAST_MODIFIED=Fri Jul 12 11:12:03 1985

(WANG) LABORATORIES, INC.	REV: 6
TITLE: VS-300 MEMORY MODULE 8703	DATE: 07/11/85
ENGINEER:	PAGE: 14 OF 14



LABEL # CHART

	LABEL P.N.
210-8703	615-2802
	LABEL P.N.
210-8703-1	615-2916



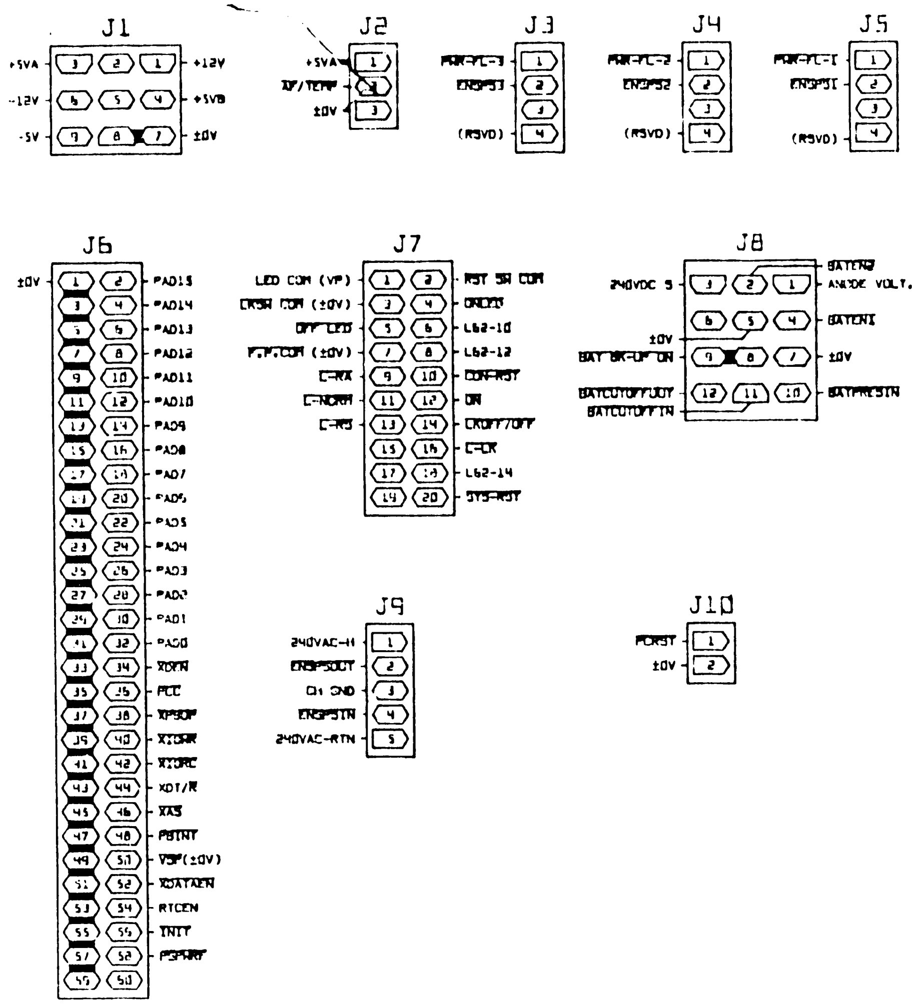
WANG VS-MEMORY MODULE
ASSEMBLY DRAWING 8703
REV. 6 PER ECO NO. 37331

NOTES
1. UNLESS OTHERWISE SPECIFIED
ALL CAPS ARE .047.300-1988.EXPRESSED IN MICROFARADS.
ALL RESISTOR NETWORKS ARE 22 OHM, 8 PIN.
2. * = DO NOT LOAD THESE DRAMS FOR 8703 (4MEG).
3. REFERENCE SCHEMATIC LOADING CHART OR PARTS LIST FOR JUMPER CONFIGURATION.

WANG LABORATORIES, INC.	BY	DATE	APPROVED BY	DATE
	DWN E. P. ELUS	7-2-85	E ENGR	
	CHK		M ENGR	
			MFG ENGR	
MATERIAL	MODEL NO. VS-300	TITLE ASSEMBLY, VS-MEMORY MODULE		
FINISH		210-8703	D	8703 / 6
	SCALE	WANG PART NUMBER	SIZE	DRAWING NUMBER / REV

NOTES

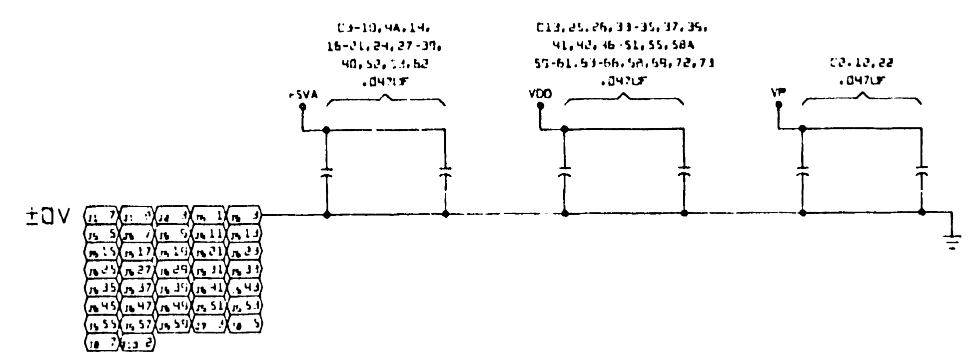
1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.



MNEMONICS	COORD.
XF/TEMP	8J14
ANODE VOLT.	2J1
BAT BK-UP ON	4H1
BAT CUT OFF IN	2K6
BAT CUT OFF OUT	4H2
BAT EN	2J1
BAT PRES IN	2C14
RTCEN	JA1
CON-RST	2F14
EN SPS1 - EN SPS3	2H1
INIT	2F1
C-CK	2F14
C-NORM	2F13
C-RX	2F14
C-RS	2F13
LED COM (VP)	2G1
CK OFF/OFF	2F13
L62-10	2D14
L62-12	2D13
L62-14	2D13
OFF LED	2G1
ON	2F14
ON LED	2H1
PAD0 - PAD15	JK1
PBINT	4G13
PCC	4F13
PC RST	2E1
PSPWRF	JC1
PWRFL1 - PWRFL3	2914
RST SR COM	2C1
SYS-RST	2D14
VSP	4D13
XAS	JJ13
XDATAEN	4D13
XDPIN	4J13
XDT/R	4F13
XTCRC	4J13
XTCRR	4F13
XPSOP	4F13
+5VA	JD14
+5VB	JD14
-5V	8B14
+12V	JC14
-12V	JA14
240VDC-S	4H13
240VAC-H	2J14
240VAC-RTN	2J14

LINEAR & TTL SPARES

IC TYPE	LOCATION	QTY
LM339	L74	3
7406	L13	3
4136	L55	3
74F02	L29	2
74F04	L3	2
	L28	2
74F74	L23	1



E REV 3 N

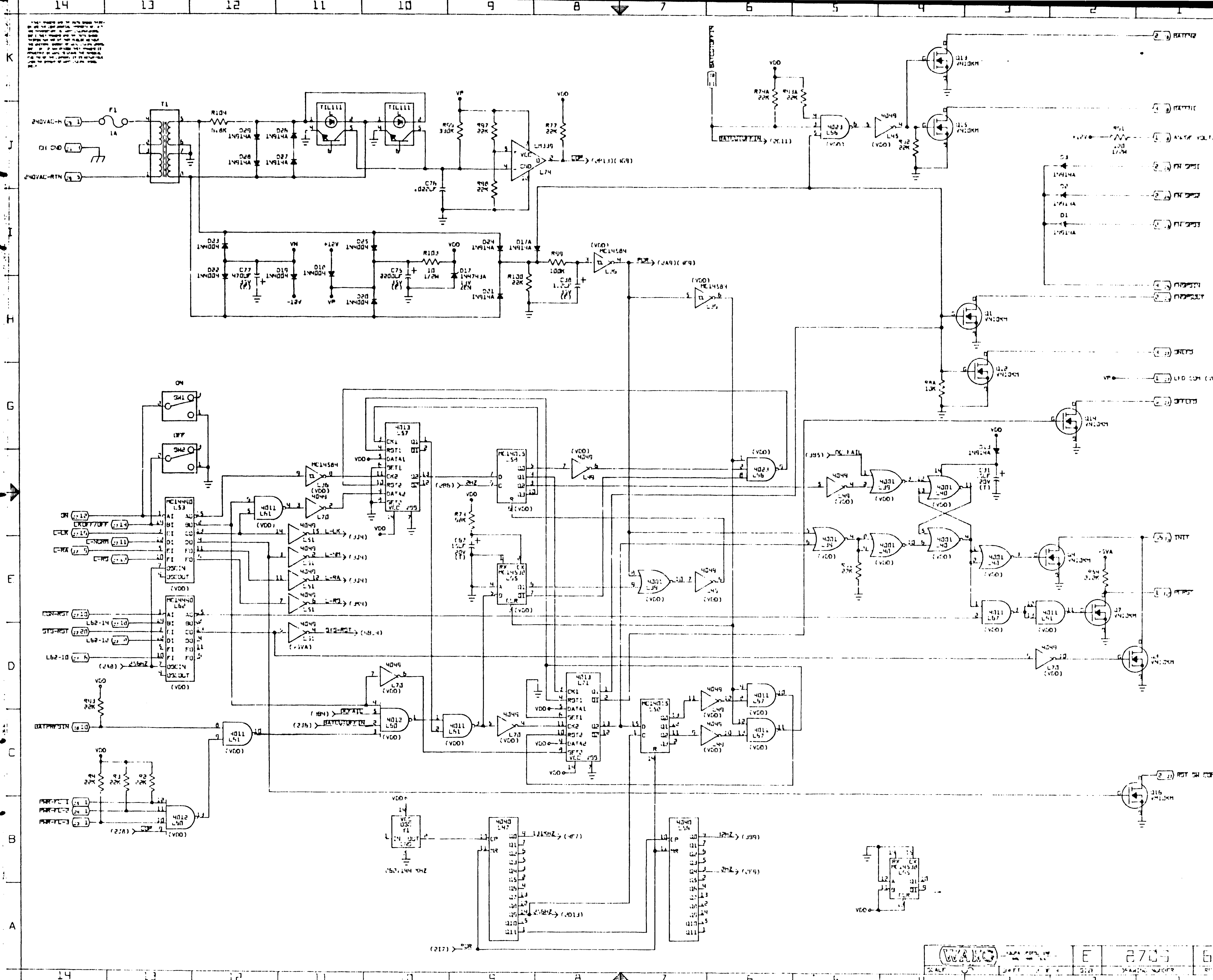
WANG

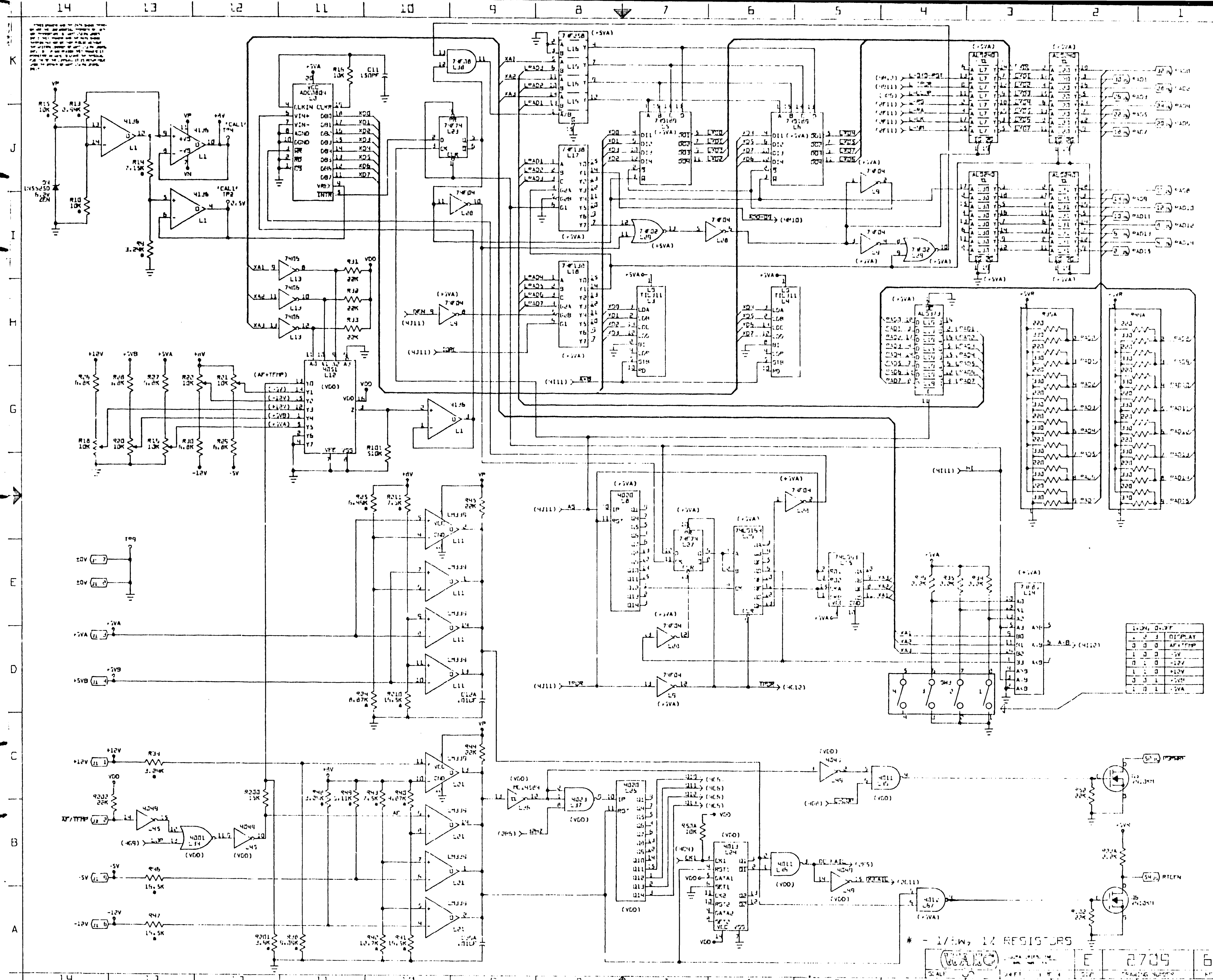
SCHEMATIC DIAGRAM

TITLE POWER SUPPLY CONTROLLER

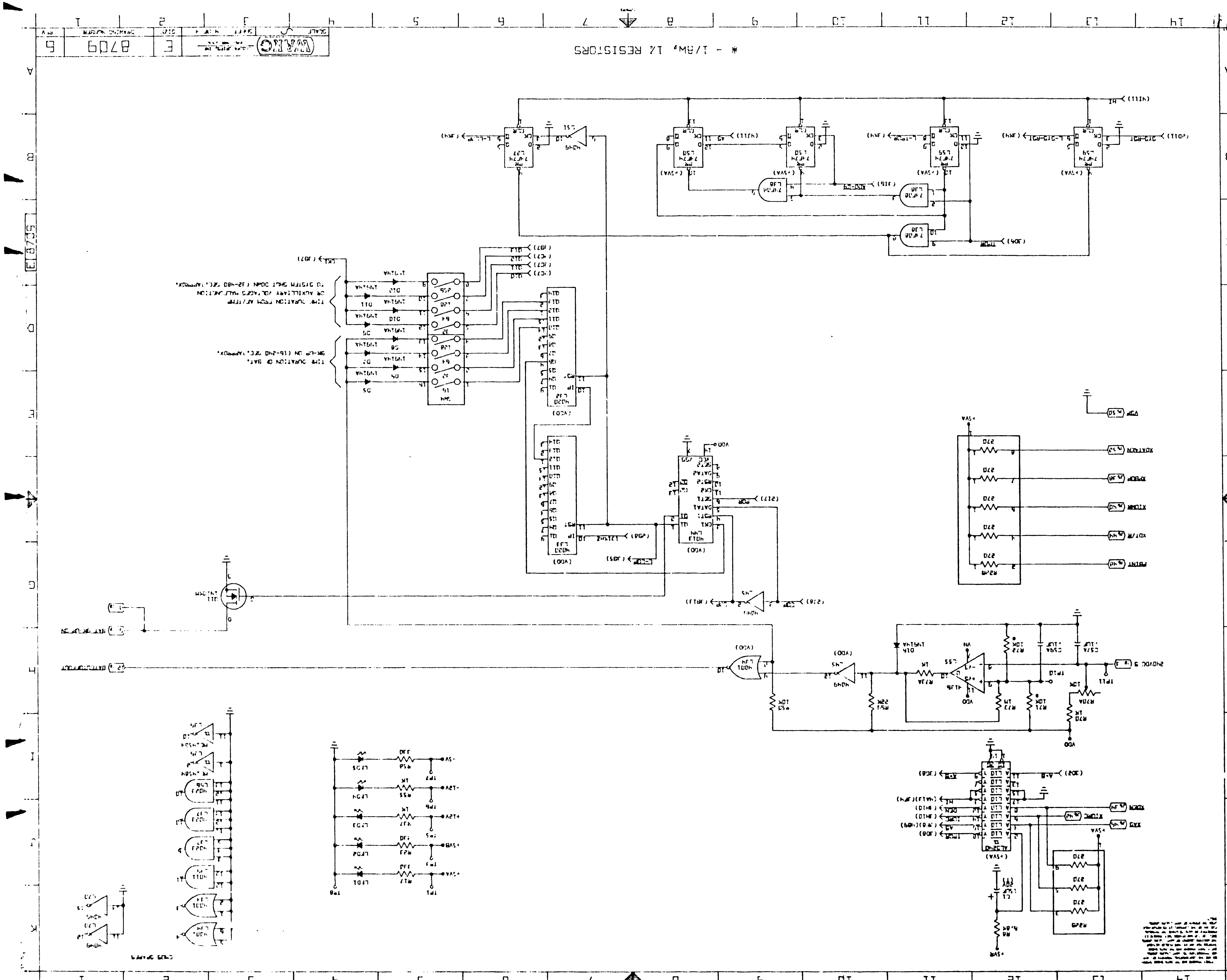
VS-300

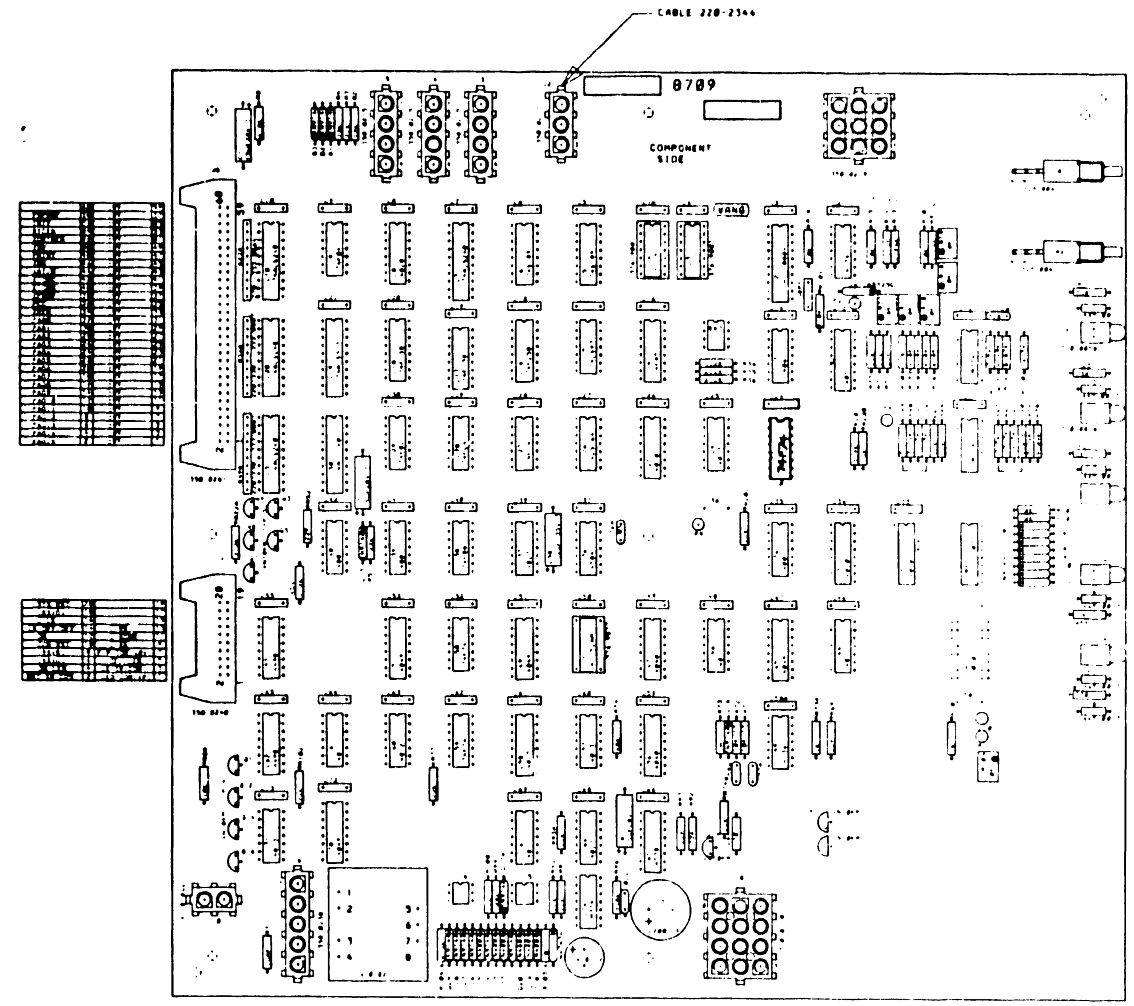
SIZE E DRAWING NUMBER 8709 RT. 5


240VAC-H
240VAC-RTN
TIL111
TIL111
LM339
MC14584
MC14490
4013
4049
4011
4023
4001
4040
4040
WAKO



1=ON, 0=OFF
1 2 3 DISPLAY
0 0 0 AF+TEMP
1 0 0 -5V
0 1 0 -12V
1 1 0 +12V
0 0 1 +5VB
1 0 1 +5VA
* - 1/4W, 1% RESISTORS
WANG
E
2705
6

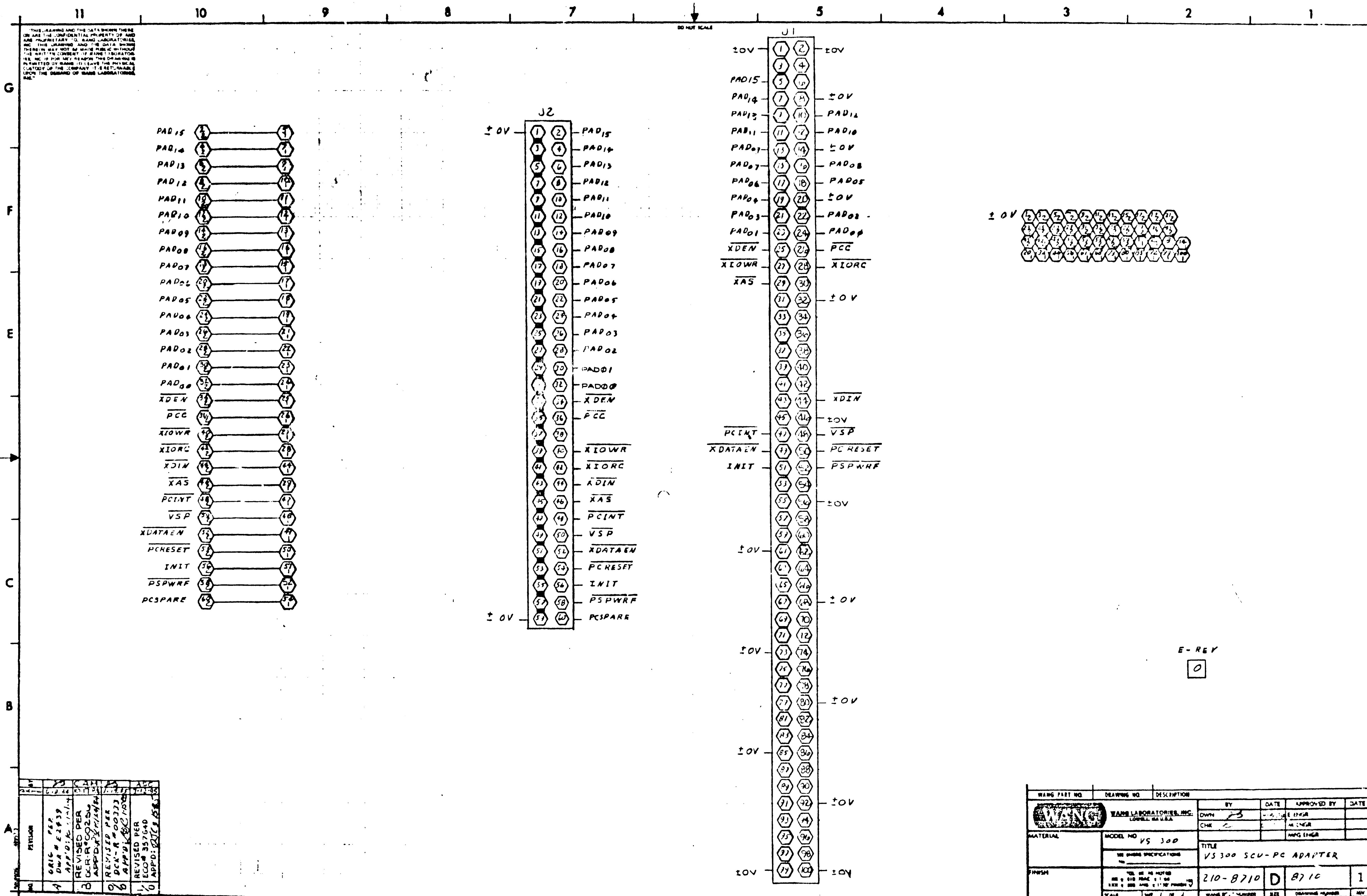




NOTES:

UNLESS OTHERWISE SPECIFIED
1. ALL CAPICITORS ARE .047UF CERAMIC EXPRESSED IN MICROFARADS
2. ALL RESISTORS ARE 1/4W, 5% EXPRESSED IN OHMS
3. ALL 1% RESISTORS ARE 1/8W
4. TP2, TP6, TP9-TP11 ARE WPN 654-1192.

WANG		BY	DATE	APPROVED BY	DATE
		DWN VS		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS300	E C CONTROL		MFG ENGR	
	10-203	TITLE VS300 POWER SUPPLY CONTROLLER ASSEMBLY DRAWING			
FINISH		210-8709	C	8709	5



J1
J2
PAD15
PAD14
PAD13
PAD12
PAD11
PAD10
PAD09
PAD08
PAD07
PAD06
PAD05
PAD04
PAD03
PAD02
PAD01
PAD00
XDEN
PCC
XIOWR
XIORC
XDIN
XAS
PCINT
VSP
XDATAEN
PCRESET
INIT
PSPWRF
PCSPARE
±0V
E-REV
0
D 8710
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
MODEL NO VS 300
TITLE
VS 300 SCU-PC ADAPTER
210-8710
D
8710
1
REVISION
ORIG REL DWR # E2939
REVISED PER DCR-R # C025
REVISED PER DCK-R # 00333
REVISED PER ECO# 35764D

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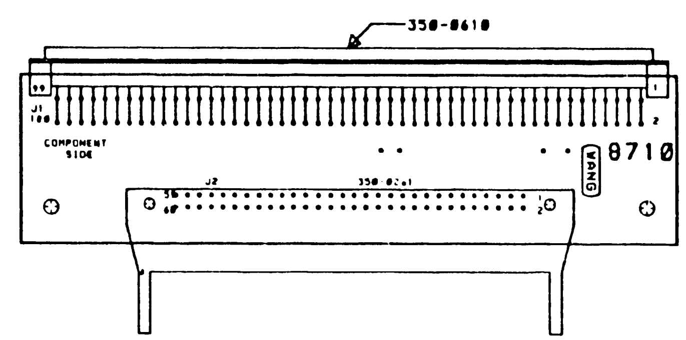


BY	DPW	HSL	GAR	DCT	
DATE	5/29/84	9/24/84	12/28/84	3/13/85	
CHECKER			JOL		
REVISION	DWR#E2439	DSR-R#00256	DSR-R#00333	ECO#35784D	
NO.	A\A	B\B		—	

WANG LABORATORIES INC.
LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN DPW	5/29/84	E ENGR	
CHK JOL		M ENGR	
E C CONTROL		MFG ENGR	

MATERIAL

FINISH

MODEL NO. VS300

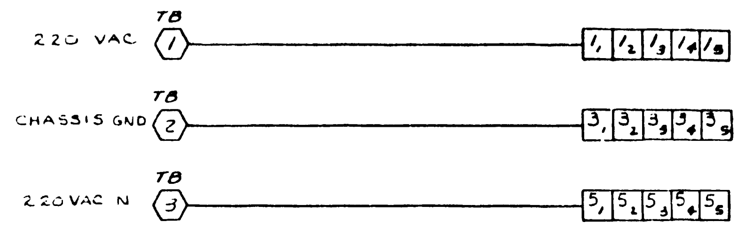
SEE ENGRG SPECIFICATIONS NO. 10-203

TOL. EX. AS NOTED
.XX+/- .010 FRAC.+/-1/64
.XXX+/-.005 ANG +/- 1 30'

SCALE 1/1 SHT 1 OF 1

TITLE VS 300 SCU-PC ADAPTER ASSEMBLY DRAWING

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-8710	C	8710	1



DO NOT SCALE

NO	REVISION	DATE	BY
A	ORIGINATED PER DWR#E2511 APP'D:		KM
C	REVISED PER DWR# 00579 APP'D: A		

WANG LABORATORIES, INC
LOWELL MASS U.S.A.

MODEL NO: VS 300

TITLE: AC DISTRIBUTION BOARD

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-8715	D	8715	C

DWN: KM
SHT 1 of 2

17" 17"

11" 11"

8.5" 8.5"

WANG LABORATORIES, INC. RUN DATE: 12/17/84 14:37 M

›››››› ELECTRICAL PARTS LIST ‹‹‹‹‹‹ SHEET 2 OF 2 PAGE 1

(FINAL PARTS LIST)

BOARD NO. & TITLE:	C8715	AC DISTRIBUTION BOARD	CREATED: 09/17/84 10:50
ASSEMBLY LEVEL & TITLE:	210	8715	LAST MODIFIED: 12/17/84 14:00 BY: NS
PARTS LIST REVISION (P):	1		EDITING REVISION: 7
ARTWORK REVISION (R):	00		
ASSEMBLY REVISION (A):	00		
SCHEMATIC REVISION (S):	00		
DWR OR MOST RECENT ECO:	E2511		

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
TB1	310-1315-	8PCV03	TERMINAL BLOCK, 3 SCREW		1
J1 - J5	350-0238-	5 CONT	CONN PC HEADER UNIVERSAL RED		5
01	510-8715-		PCB		1

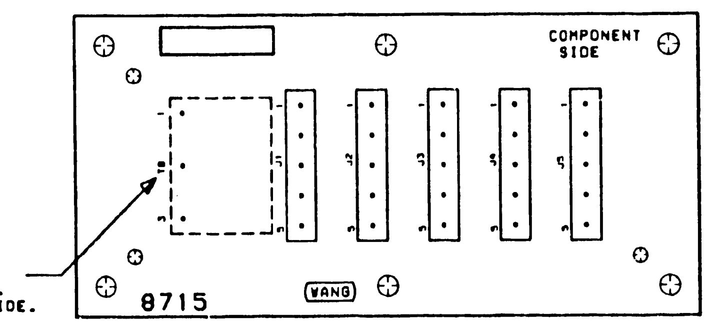
*** END-OF-REPORT ***

WANG — WANG LABORATORIES, INC. LOWELL, MA U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
				MFG ENGR	
MATERIAL	MODEL NO	TITLE AC DISTRIBUTION BOARD			
	SEE ENGRG SPECIFICATIONS No ______				
FINISH	TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH	210-8715	C	8715	0
	SCALE / SHT 2 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

8.5" 8.5"

11" 11"

17" 17"



8PCV TERMINAL BARRIER STRIP.
MOUNT COMPONENT FROM CIRCUIT SIDE.
(SEE NOTE 2.)

NOTE:
1. J1-J5 ARE W/P/N 350-0230.
2. TB1 IS W/P/N 310-1315.

BY	DPW	HRH	HRH
DATE	9/14/84	11/16/84	11/19/84
CHECKER			
REVISION	DWR#E2511	DCR-R#00291	DCR#00579
NO.	A/A	0/0	0

WANG LABORATORIES INC.
LOWELL, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN DPW	9/14/84	E ENGR	
CHK		M ENGR	
E C CONTROL		MFG ENGR	

MATERIAL

FINISH

MODEL NO. VS 300

SEE ENGRG SPECIFICATIONS NO. 10-203

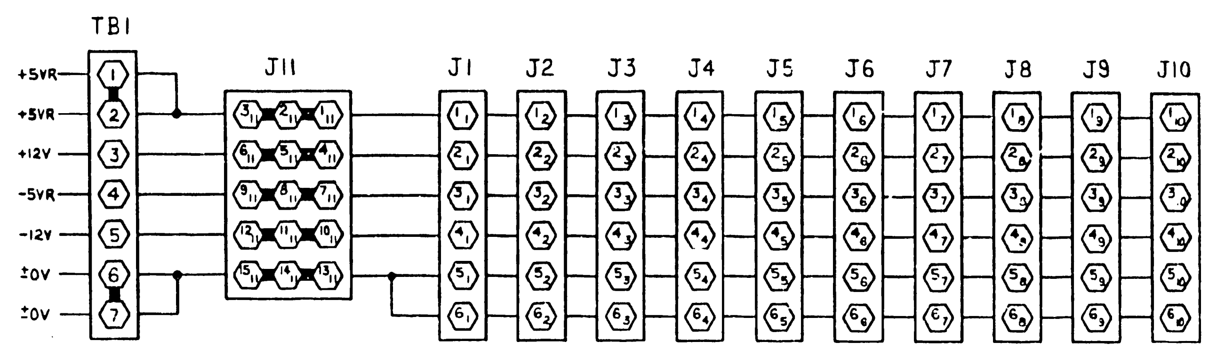
TOL. EX. AS NOTED
.XX+/- .010 FRAC.+/-1/64
.XXX+/-.005 ANG +/- 1 30'

SCALE 1/1 SHT 1 OF 1

TITLE AC DISTRIBUTION BOARD ASSEMBLY DRAWING

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-8715	C	8715	0

DO NOT SCALE



REV	REVISION	BY / DATE
0	ORIGINATED PER DWR #E2514 APP'D	BSR 11-20-84

E REV 0

WANG PART NO	DRAWING NO	DESCRIPTION

WANG LABORATORIES, INC.
LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	B.S. RICHARDS	11-20-84	E ENGR	
CHK			M ENGR	
			MFG ENGR	

MATERIAL —

MODEL NO VS 300

SEE ENG'G SPECIFICATIONS No

FINISH —

TOL EX AS NOTED
XX ± .010 FRAC ± 1/64
XXX ± .005 ANG ± 1°30' FINISH

SCALE — SHT 1 OF 2

TITLE DC DISTRIBUTION BOARD

WANG ART NUMBER	SIZE	DRAWING NUMBER	REV
210-8716	D	8716	0

D 8716

WANG LABORATORIES, INC. RUN DATE: 11/27/84 14:20

»»» ELECTRICAL PARTS LIST ««« M SHEET 2 OF 2 PAGE 1

(FINAL PARTS LIST)

BOARD NO. & TITLE: C8716 DC. DISTRIBUTION BOARD
ASSEMBLY LEVEL & TITLE: 210 8716
PARTS LIST REVISION (P): 1
ARTWORK REVISION (R): 00
ASSEMBLY REVISION (A): 00
SCHEMATIC REVISION (S): 00
DWR OR MOST RECENT ECO: E2514

CREATED: 09/14/84 13:42
LAST MODIFIED: 11/27/84 14:18 BY: LAB
EDITING REVISION: 6

REF. DES.	WANG PART NO.	VALUE/TYPE	DESCRIPTION	DRAWING NO.	QTY.
TB1	310-1122-	7 POS	7 POS ROI 8PCV-07 7 POS TERMINAL BLOCK		1
J11	350-0221-	15 CONT	CONN PC HEADER UNIVERSAL RED		1
J1 - J10	350-0306-	6 PIN	6 PIN MATE-N-LOK CONN.		10
@1	510-8716-		PCB		1

*** END-OF-REPORT ***

WANG — WANG LABORATORIES, INC. LOWELL, MA U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO			MFG ENGR	
	SEE ENGRG SPECIFICATIONS No. ______	TITLE DC DISTRIBUTION BD.			
FINISH	TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH 125 √	210-8716	C	8716	0
	SCALE / SHT 2 OF 2	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

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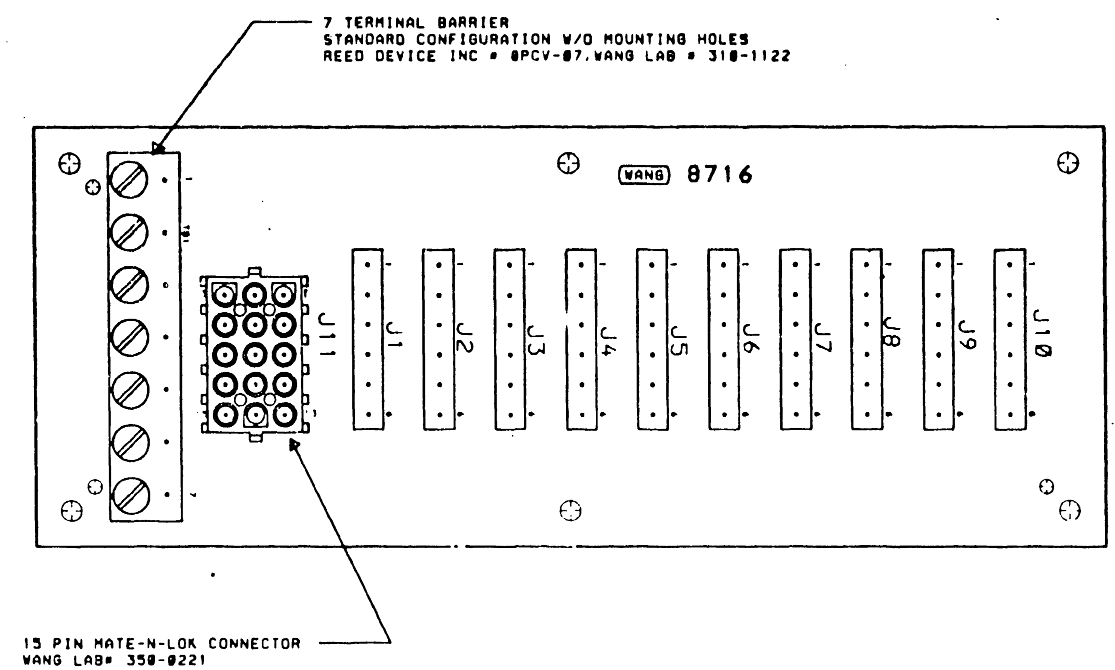


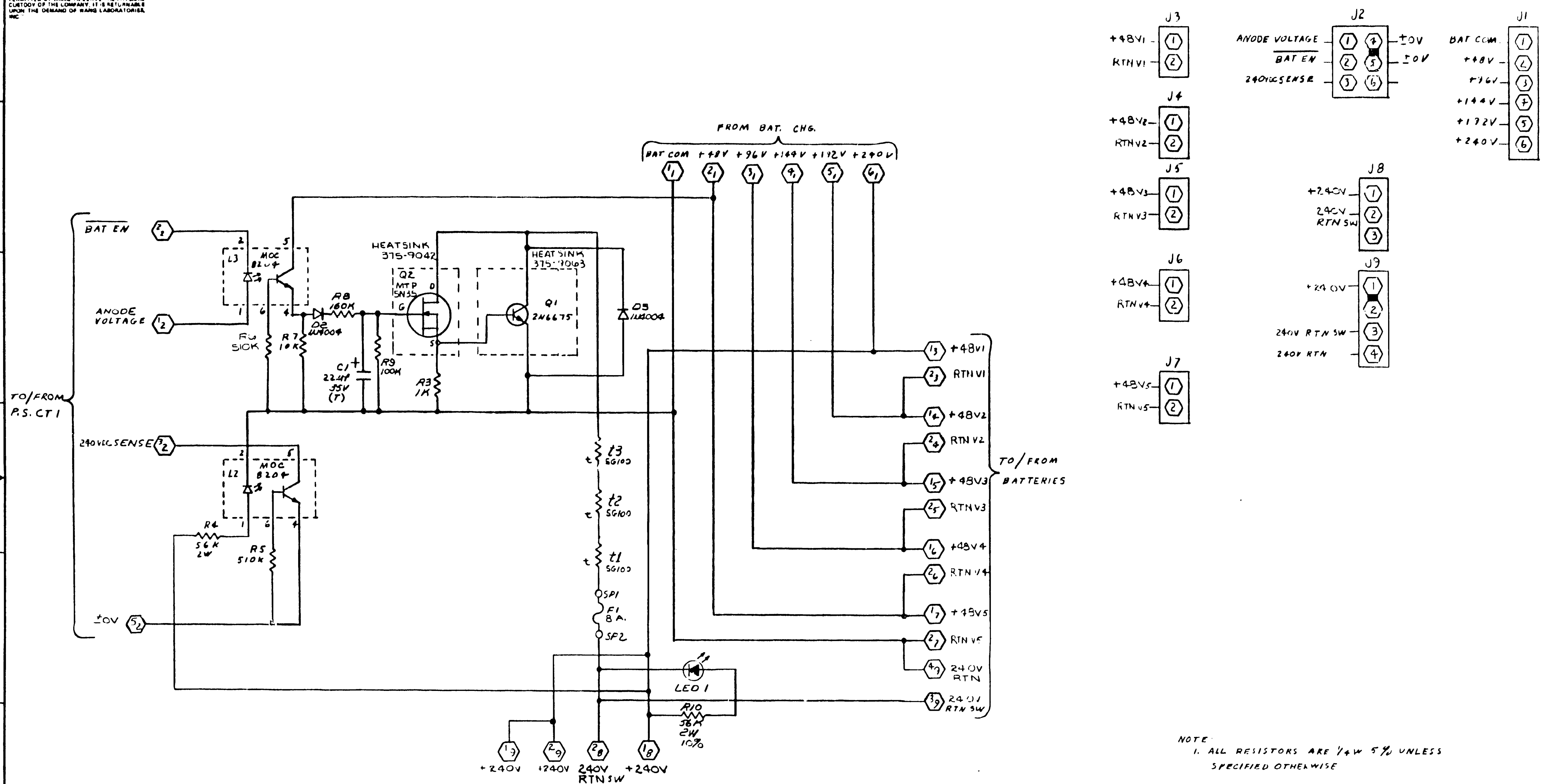
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL CONNECTORS ARE 6 PIN MATE-N-LOK,
WANG LAB # 350-0306

NO.	REVISION	DWR#E2514 DCR#00539	DWR-R0030
DRFT		DPW	GAR
DATE		9/14/84	11/14/84
CHECKER			

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN DPW	9/14/84	E ENGR	
				M ENGR	
MATERIAL	MODEL NO. VS 300	E C CONTROL			
	SEE ENGRG SPECIFICATIONS NO. 10-203	TITLE DC DISTRIBUTION BOARD ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC.+/-1/64	210-8716	C	8716	Ø
	SCALE 1/1 · SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC.

DO NOT SCALE



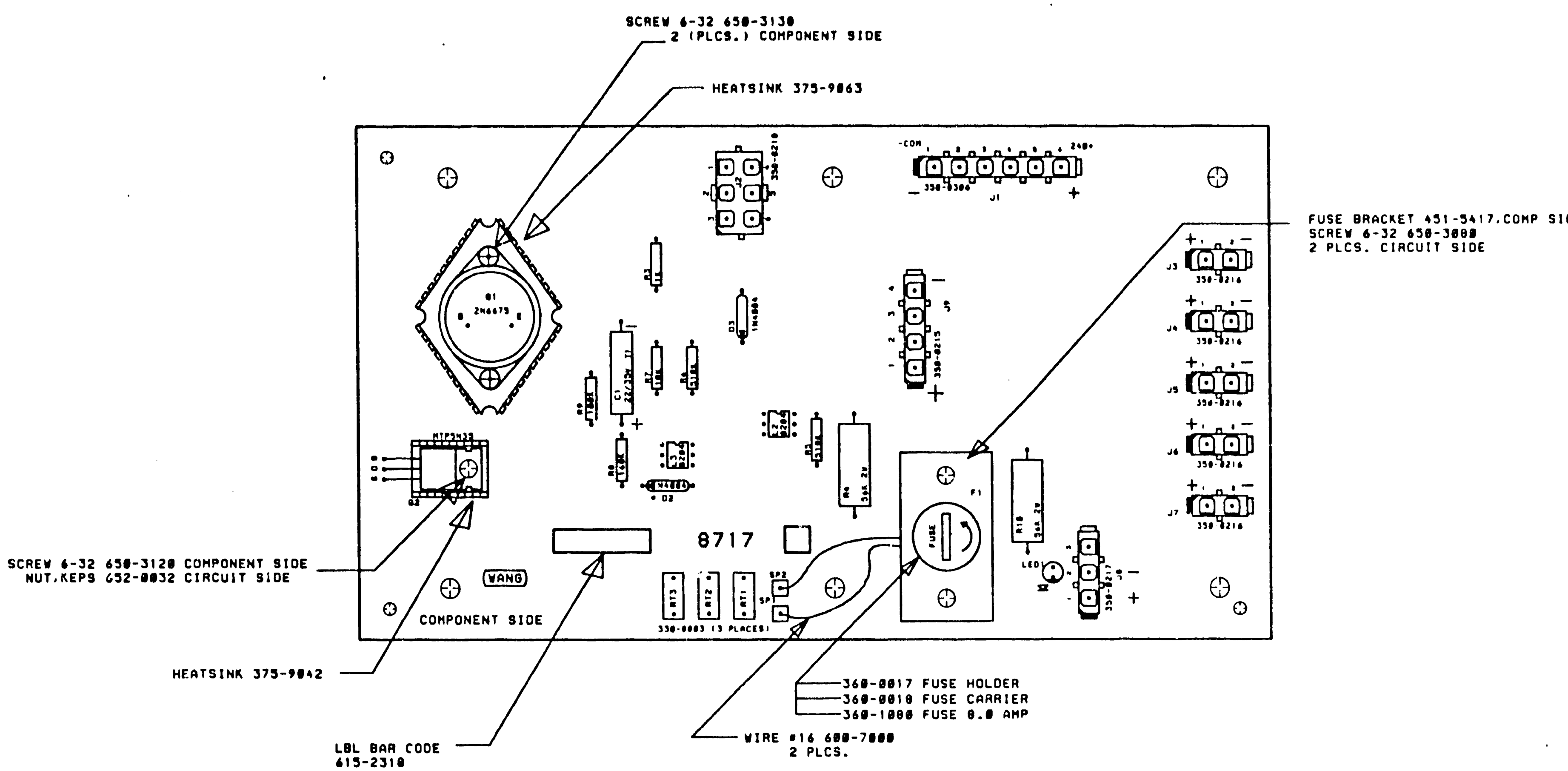
NOTE
1. ALL RESISTORS ARE 1/4W 5% UNLESS SPECIFIED OTHERWISE

E-REV
1

WANG PART NO	DRAWING NO	DESCRIPTION			
WANG LABORATORIES, INC. LOWELL, MA U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO VS 300			MFG ENGR	
	SEE ENG'G SPECIFICATIONS	TITLE BATTERY BACK UP			
FINISH		210-8717	D	8717	4
	SCALE / SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

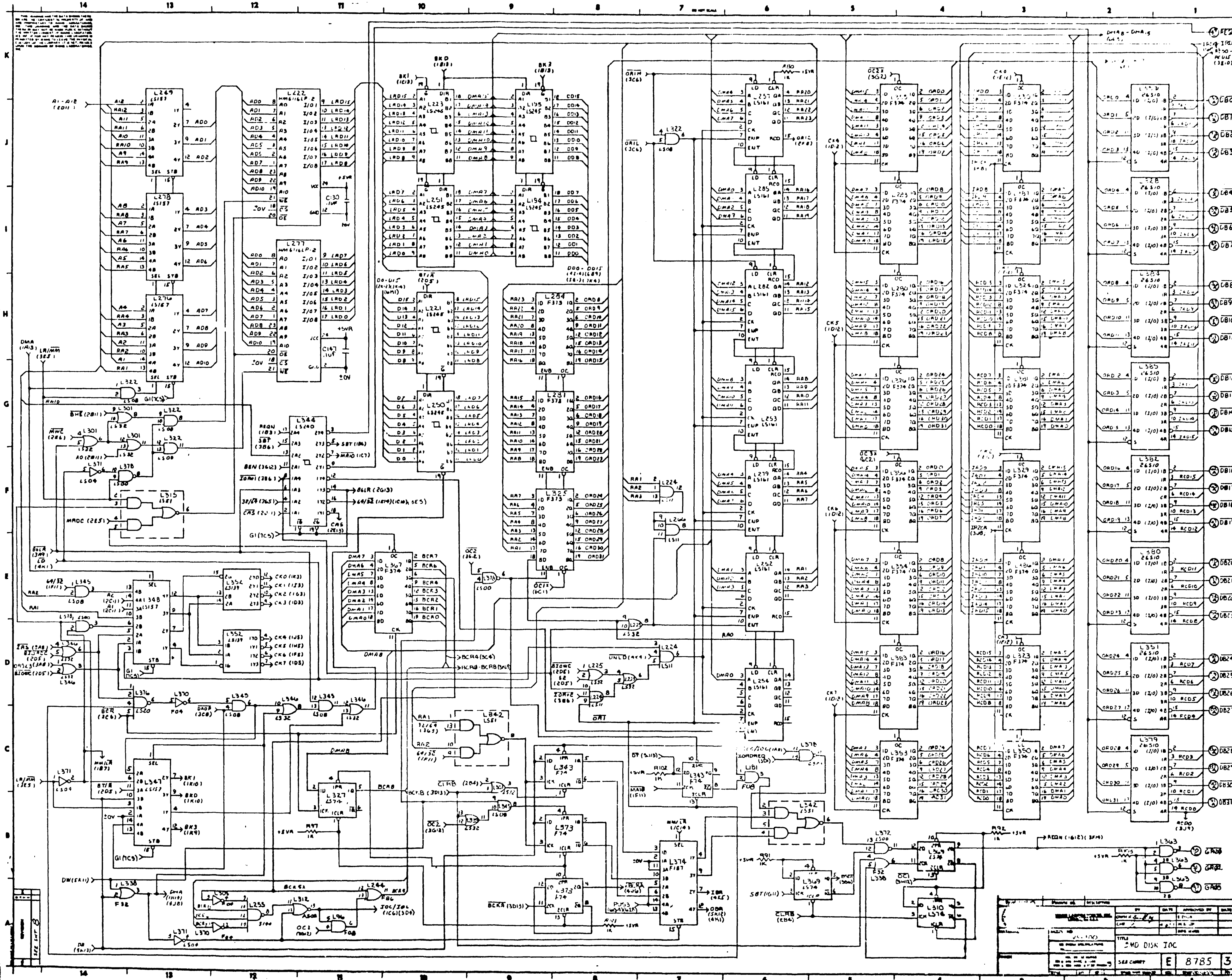
REVISION

D 8717

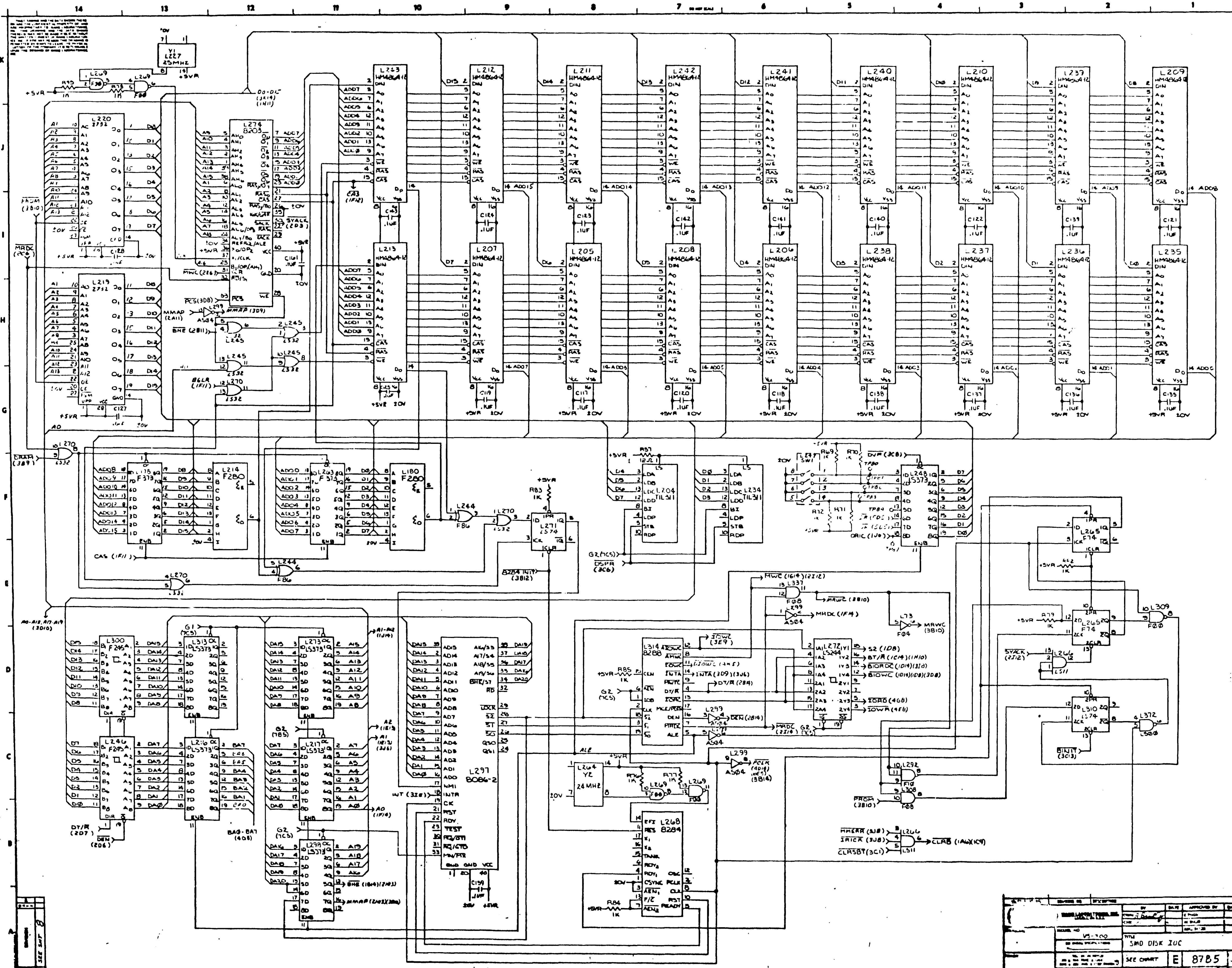


NOTES:
UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTORS ARE 1/4W 5% EXPRESSED IN OHMS
2. LOAD LED1 WITH A 370-0075.

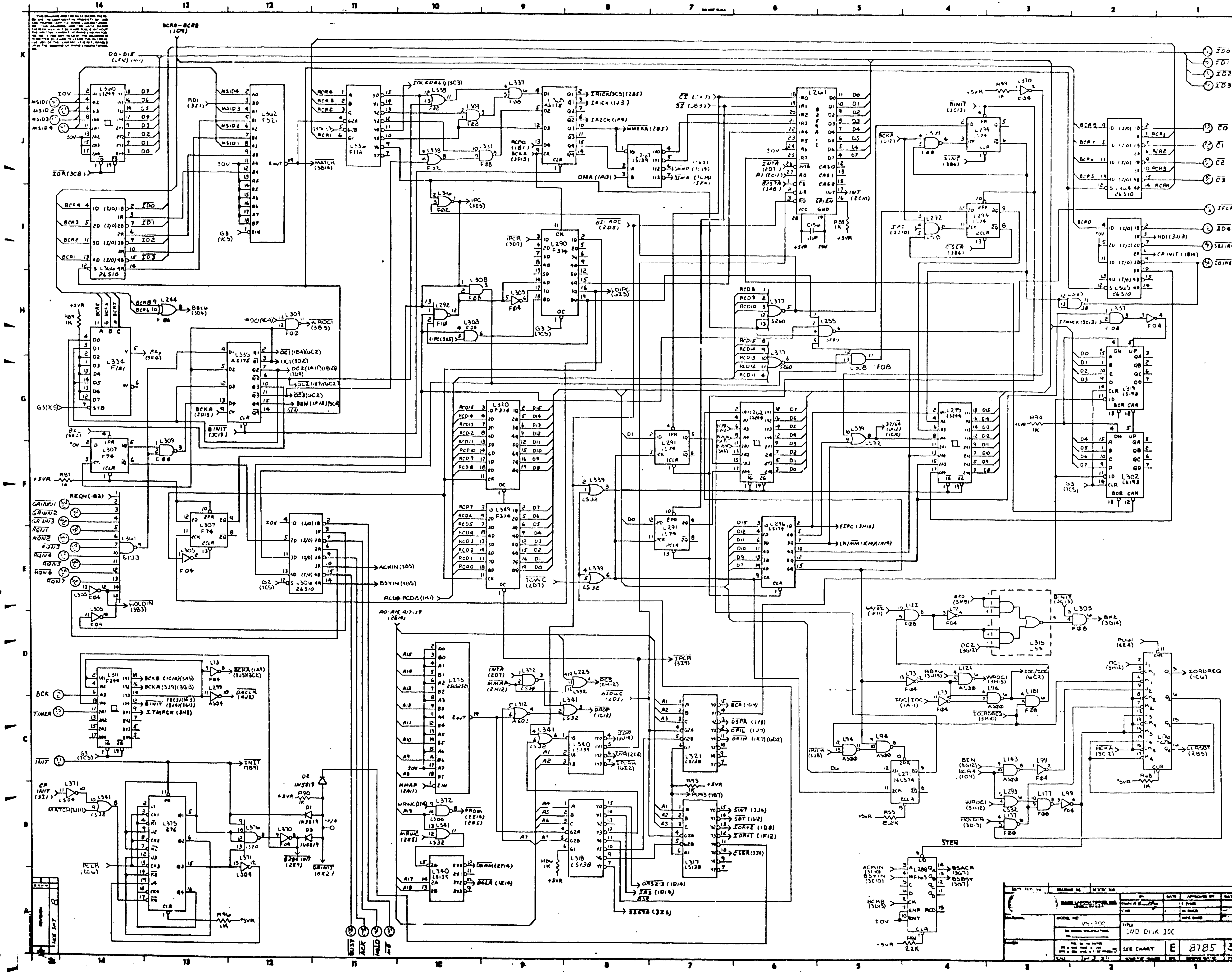
			BY	DATE	APPROVED BY	DATE
WANG	LABORATORIES INC. LOWELL, MASS. U.S.A.		DWN		E ENGR	
			CHK		M ENGR	
MATERIAL	MODEL NO. VS-300		E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-203		TITLE BATTERY BACK UP CTRL. BD. ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED		210-8717	C	8717	4
	SCALE 1/1	SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV



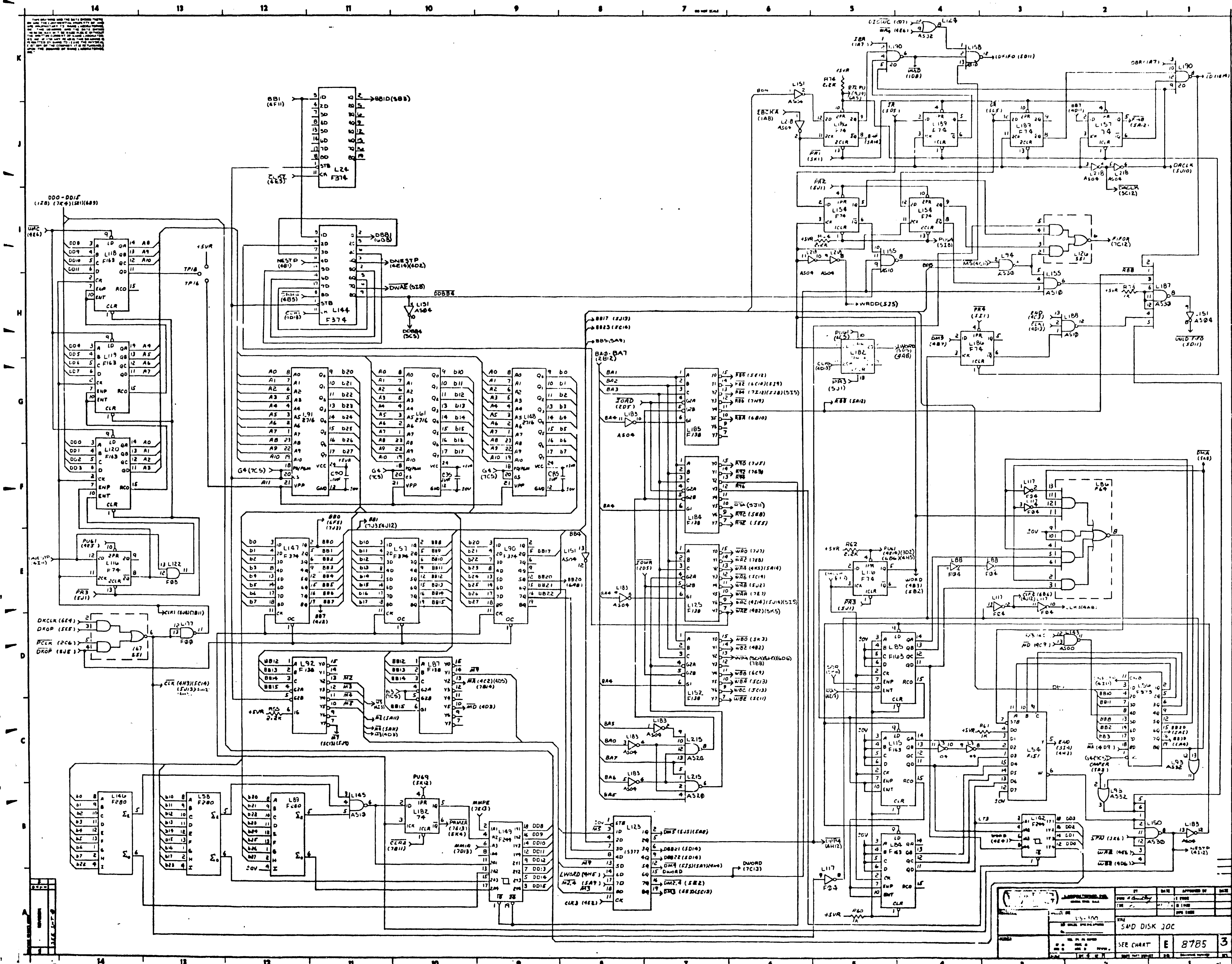
SMD DISK IOC
E
8785
3

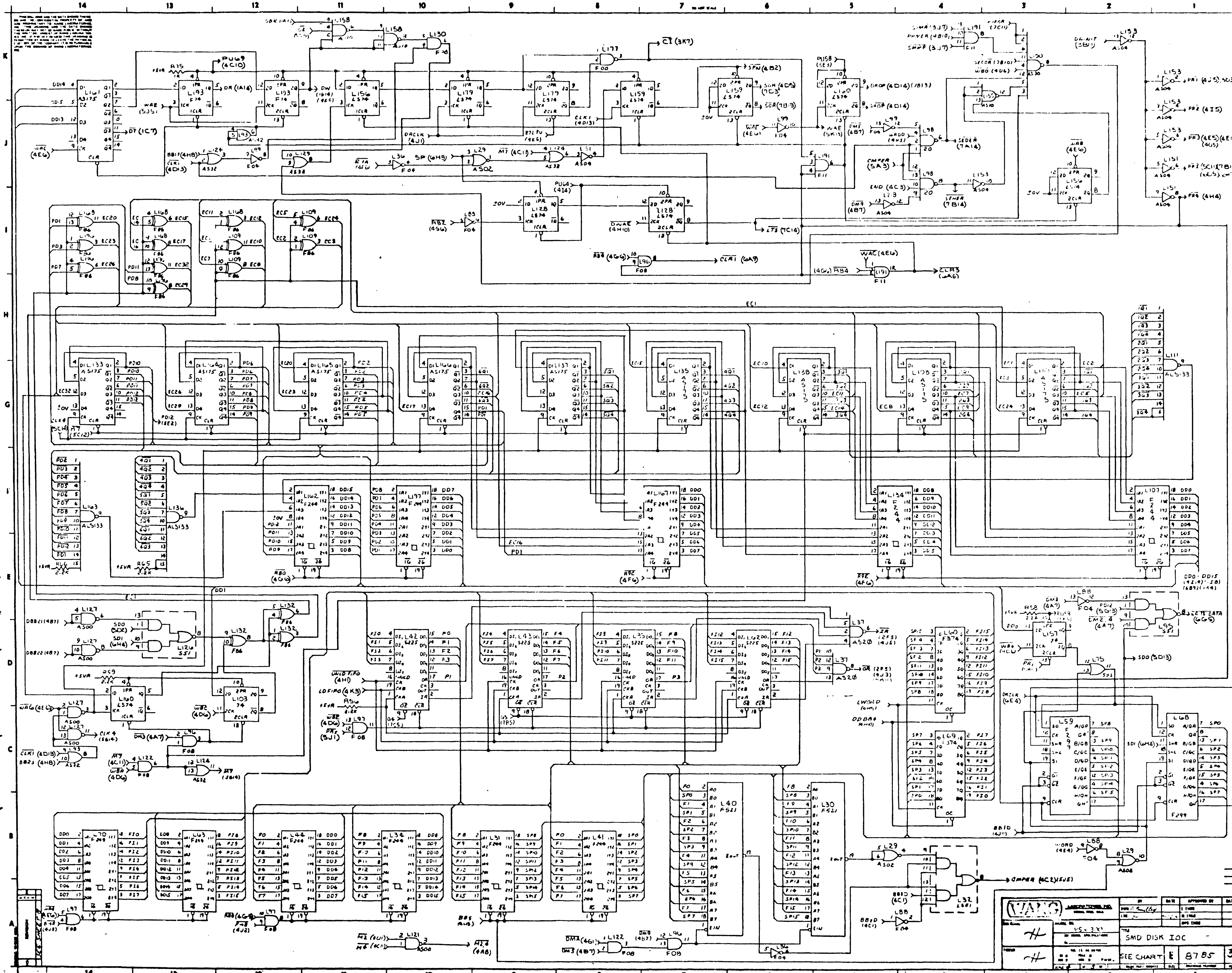


VS-300
SMD DISK IOC
E
8785
3

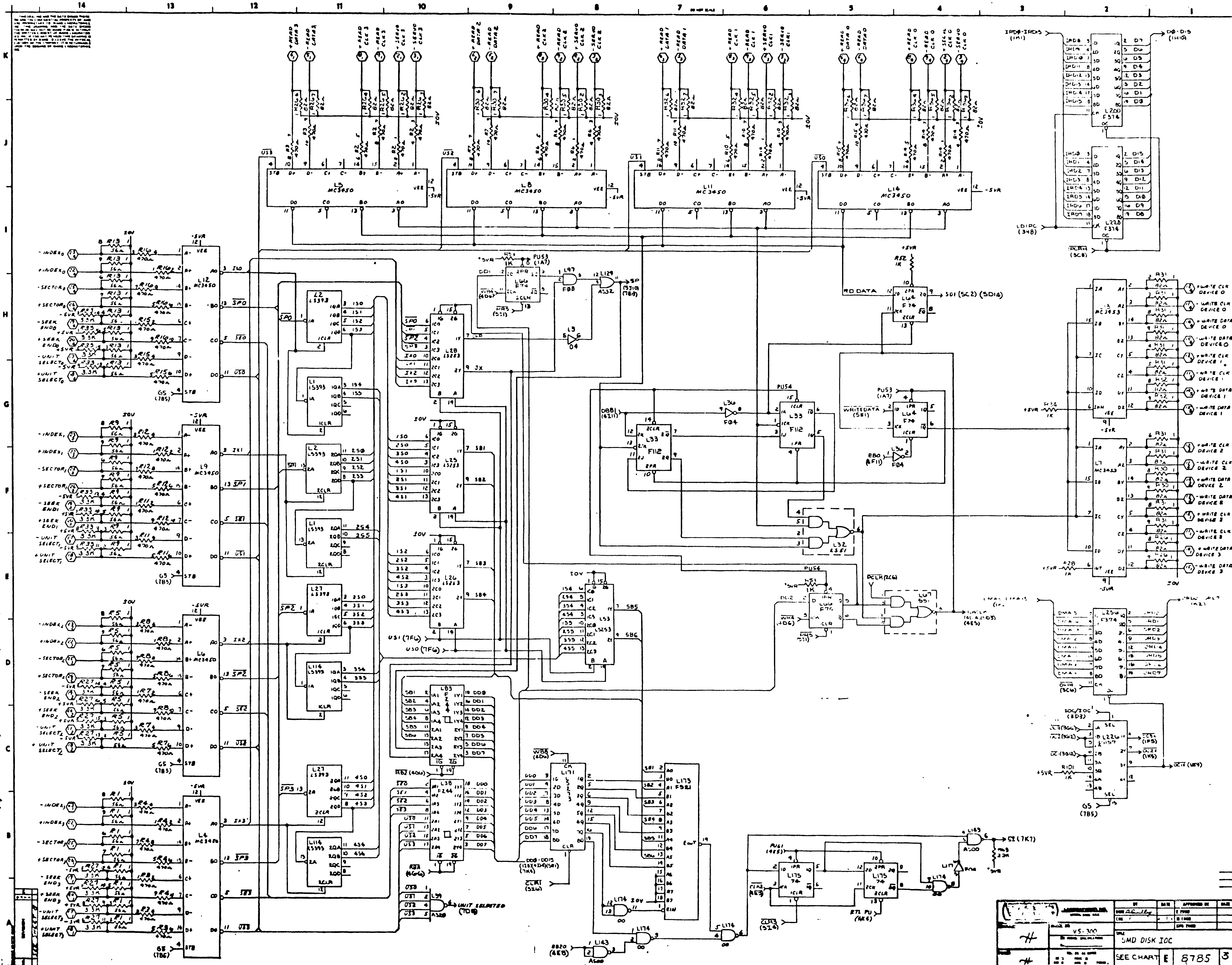


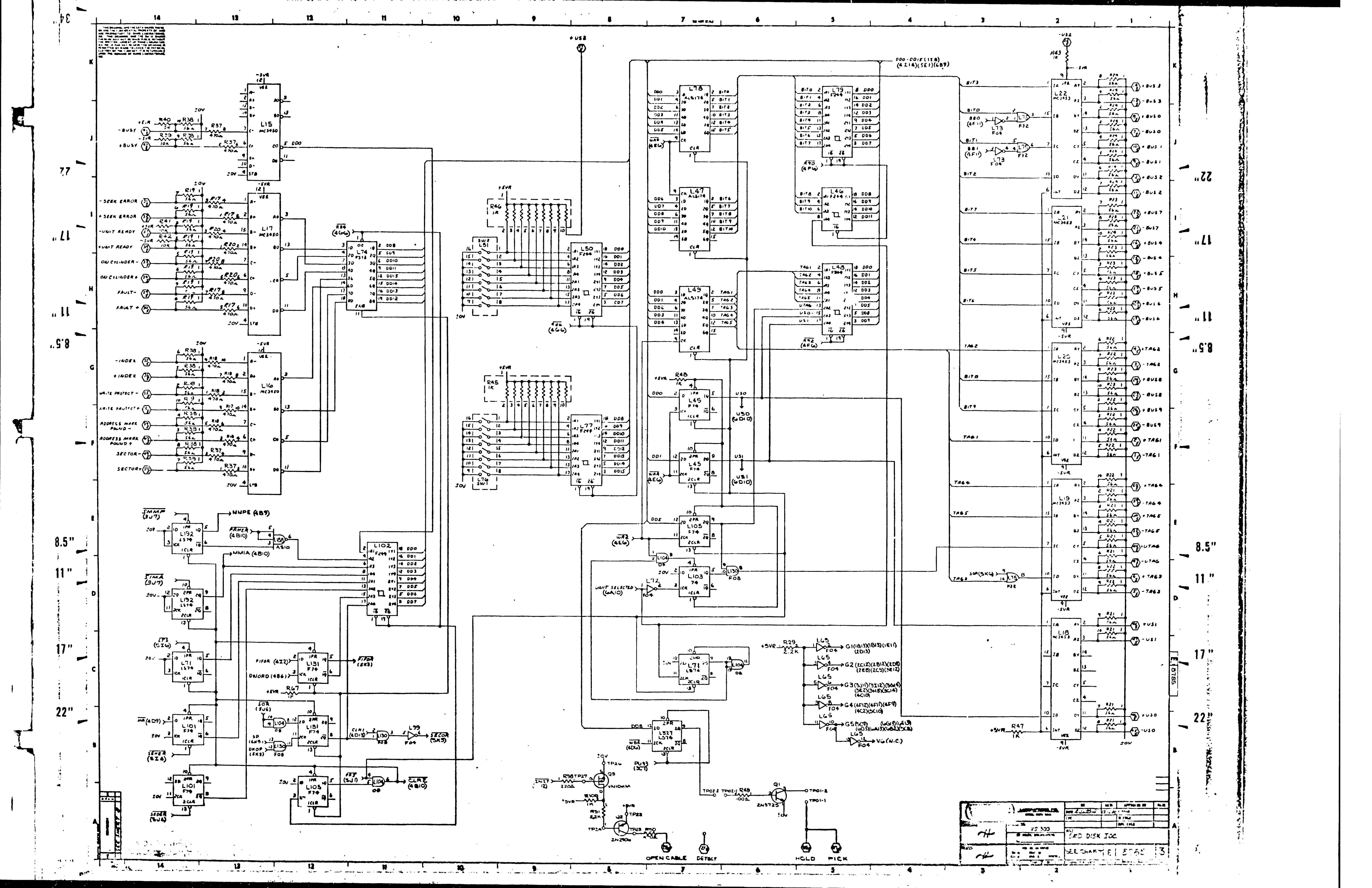
MODEL NO
VS-100
TITLE
IMD DISK IOC
SEE CHART
E
8785
3


SMD DISK IOC
SEE CHART
E
8785
3

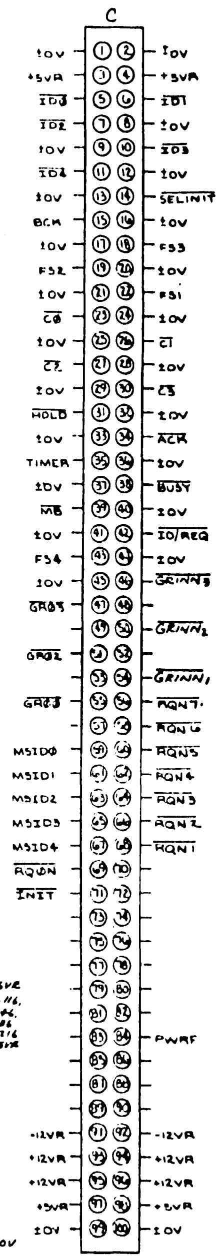


SMD DISK IOC
SEE CHART
8785
3

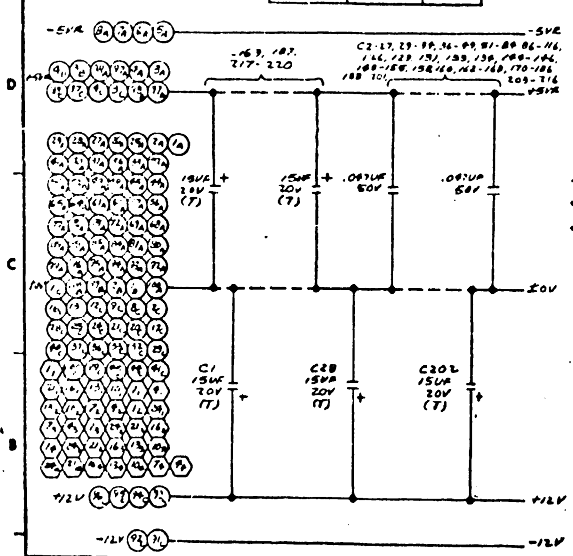

VS-300
SMD DISK IOC
SEE CHART
E
8785
3


OPEN CABLE
DETECT
HOLD
PICK
SMD DISK IOC

210 = 209 + 377 OR 378									
210	209	156.8... 7	L183 191 204 - 211	L197, 198	L200, 223	L232	L240	L246	L268
82RS A	82B5	377-2393	377-0417	377-0400	377-0428	377-0404	377-0437	377-0438	377-0338

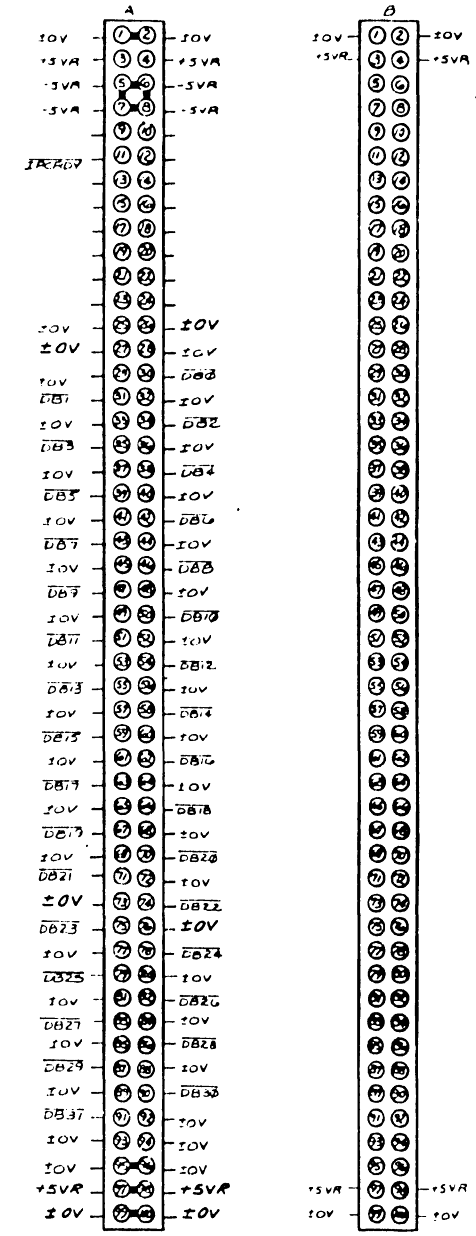


I C TYPE	LOCATION	SPARES
74LS00	L331	1
74S00	L85	3
	L109	1
	L118	3
	L157	2
74S02	L26	1
7404	L2	3
	L66	4
74LS04	L286	1
74S04	L33	2
	L67	4
	L[illegible]	3
	L123	1
74F08	L181	2
74S10	L113	2
	L168	1
74S11	L171	1
74LS20	L289	1
74S20	L36	1
74LS32	L203	1
	L236	3
74S32	L83	1
74S51	L86	1
74LS74	L281	1
74S86	L97	1
74LS139	L208	1
74S140	L206	1
74S244	L43	1
	L106	1



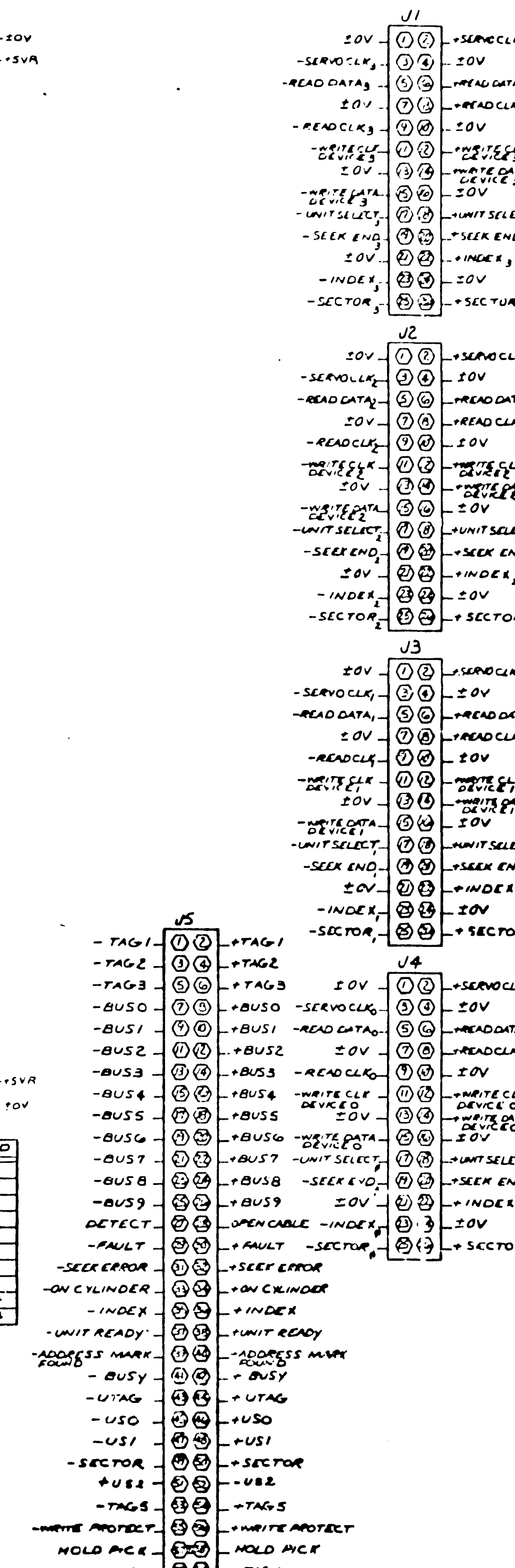
MNEMONICS	COOR'D
ACK	3A11
-ADDRESS MARK FOUND	7F14
+ADDRESS MARK FOUND	7F14
BCK	3D14
- BUS0	7J1
+ BUS0	7J1
- BUS1	7J1
+ BUS1	7J1
- BUS2	7I1
+ BUS2	7J1
- BUS3	7K1
+ BUS3	7K1
- BUS4	7H1
+ BUS4	7I1
- BUS5	7H1
+ BUS5	7H1
- BUS6	7H1
+ BUS6	7H1
- BUS7	7I1
+ BUS7	7I1
- BUS8	7G1
+ BUS8	7G1
- BUS9	7F1
+ BUS9	7F1
BUSY	3A11
- BUSY	7J14
+ BUSY	7J14
C0-C3	3J1
DB0-DB31	1J1
DETECT	7A7
- FAULT	7H14
+ FAULT	7H14
FPL	3A11
GRINN1-GRINN3	3F14
GRN	1B1

MNEMONICS	COOR'D
HOLD PICK	7A5
HOLD	3A11
IC0-IC3	3K1
IC4	3I1
- INDEX	7G14
+ INDEX	7G14
- INDEX0	6I14
+ INDEX0	6I14
- INDEX1	6G14
+ INDEX1	6F14
- INDEX2	6D14
+ INDEX2	6D14
- INDEX3	6B14
+ INDEX3	6B14
INIT	3C14
IO/REQ	3I1
[illegible]	3I1
MB	3A11
MSID0-MSID4	3J14
- ON CYLINDER	7H14
+ ON CYLINDER	7H14
OPEN CABLE	7A7
- READ CLK 0	6K4
+ READ CLK0	6K4
- READ CLK1	6K6
+ READ CLK1	6K6
- READ CLK2	6K8
+ READ CLK2	6K9
- READ CLK3	6K11
+ READ CLK3	6K11
- READ DATA0	6K5
+ READ DATA0	6K5
- READ DATA1	6K7
+ READ DATA1	6K7
- READ DATA2	6K9
+ READ DATA2	6K9
- READ DATA3	6K11
+ READ DATA3	6K12
RQON	1K1
RQN1-RQN7	3E14
SBC32/64	3K3
- SECTOR	7F14
+ SECTOR	7F14
- SECTOR0	6H14
+ SECTOR0	6H14
- SECTOR1	6F14
+ SECTOR1	6F14
- SECTOR2	6D14
+ SECTOR2	6D14
- SECTOR3	6B14
+ SECTOR3	6B14
- SEEK END0	6H14
+ SEEK END0	6H14
- SEEK END1	6F14
+ SEEK END1	6F14
- SEEK END2	6D14
+ SEEK END2	6C14
- SEEK END3	6A14
+ SEEK END3	6A14
- SEEK ERROR	7I14
+ SEEK ERROR	7I14
SELINIT	3I1
- SERVO CLK0	6K4
+ SERVO CLK0	6K4
- SERVO CLK1	6K6
+ SERVO CLK1	6K6
- SERVO CLK2	6K8
+ SERVO CLK2	6K8
- SERVO CLK3	6K10
+ SERVO CLK3	6K10
- TAG1	7F1
+ TAG1	7F1
- TAG2	7G1
+ TAG2	7G1
- TAG3	7D1
+ TAG3	7D1
- TAG4	7E1
+ TAG4	7E1
- TAG5	7E1
+ TAG5	7E1
TIMER	8C14



MNEMONICS	COOR'D
- UNIT READY	7I14
+ UNIT READY	7I14
- UNIT SELECT0	6H14
+ UNIT SELECT0	6G14
- UNIT SELECT1	6E14
+ UNIT SELECT1	6E14
- UNIT SELECT2	6C14
+ UNIT SELECT2	6C14
- UNIT SELECT3	6A14
+ UNIT SELECT3	6A14
- US0	7B1
+ US0	7B1
- US1	7C1
+ US1	7D1
- US2	7K2
+ US2	7K8
- UTAG	7D1
+ UTAG	7E1
- WRITE CLK DEVICE0	6H1
+ WRITE CLK DEVICE0	6H1
- WRITE CLK DEVICE1	6G1
+ WRITE CLK DEVICE1	6H1
- WRITE CLK DEVICE2	6F1
+ WRITE CLK DEVICE2	6G1
- WRITE CLK DEVICE3	6F1
+ WRITE CLK DEVICE3	6F1

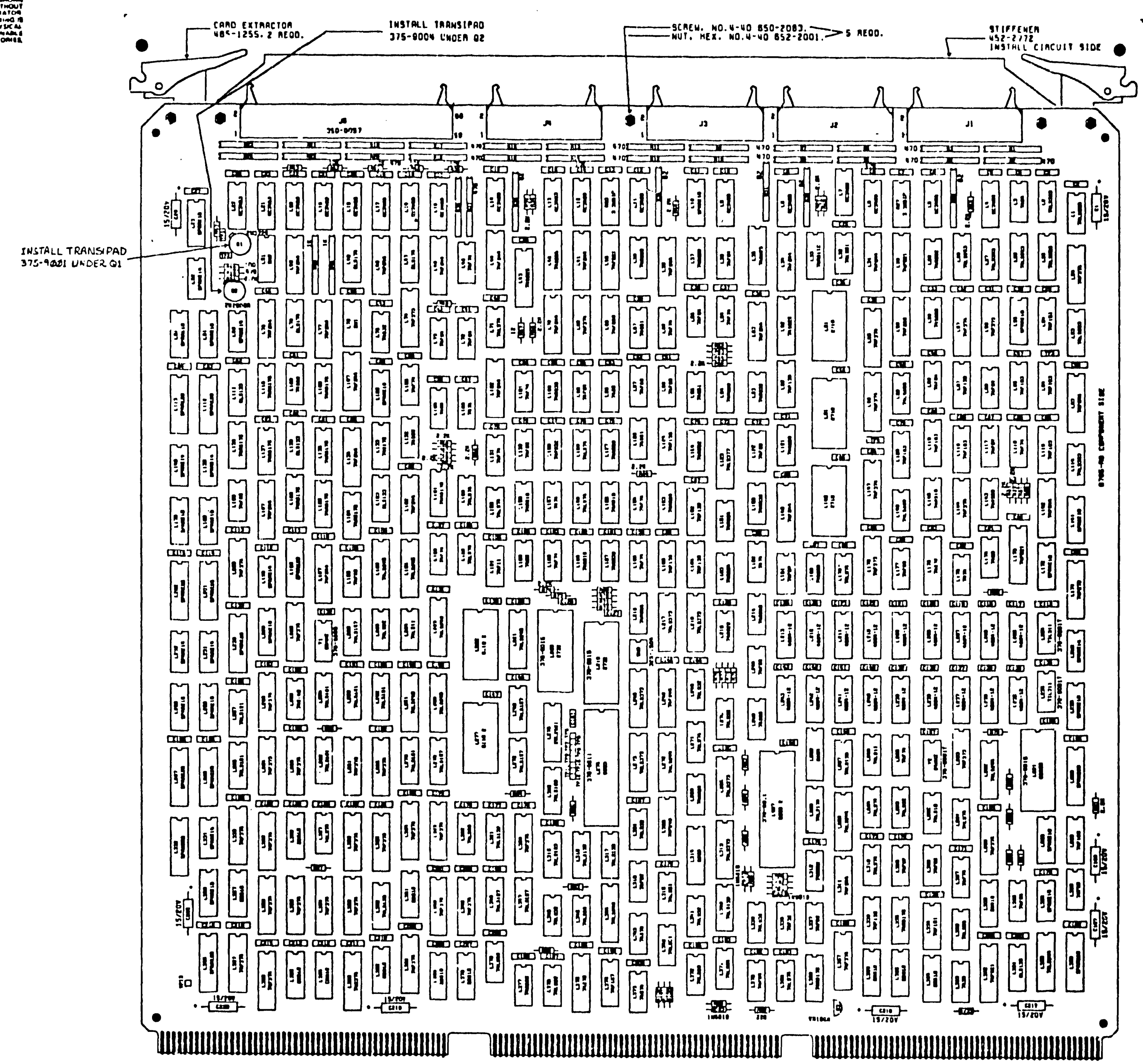
MNEMONICS	COOR'D
- WRITE DATA DEVICE0	6H1
+ WRITE DATA DEVICE0	6H1
- WRITE DATA DEVICE1	6G1
+ WRITE DATA DEVICE1	6G1
- WRITE DATA DEVICE2	6F1
+ WRITE DATA DEVICE2	6F1
- WRITE DATA DEVICE3	6E1
+ WRITE DATA DEVICE3	6E1
- WRITE PROTECT	7G14
+ WRITE PROTECT	7F14



E-REV
1

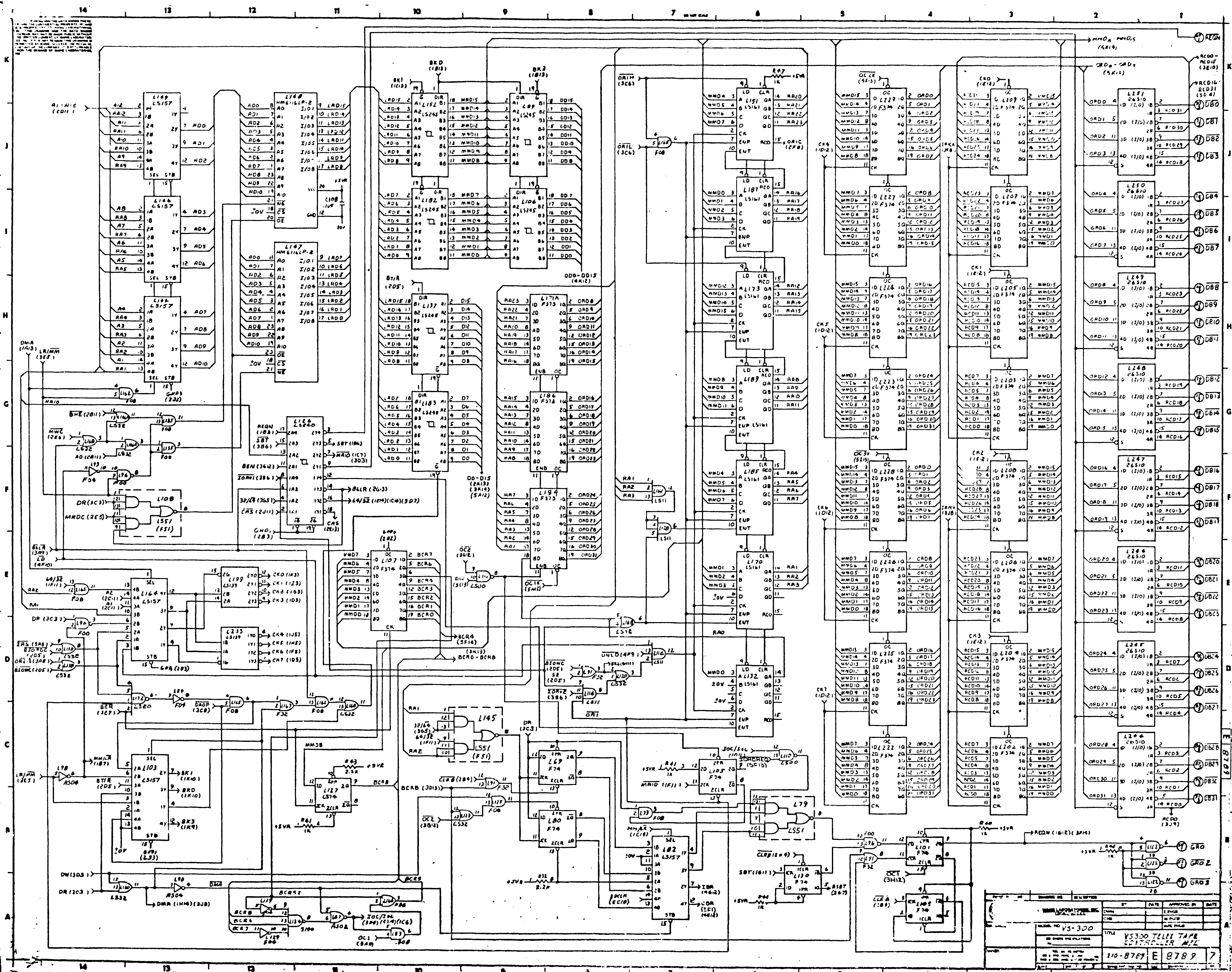
SMD DISK IOC

SEE CHART E 8785

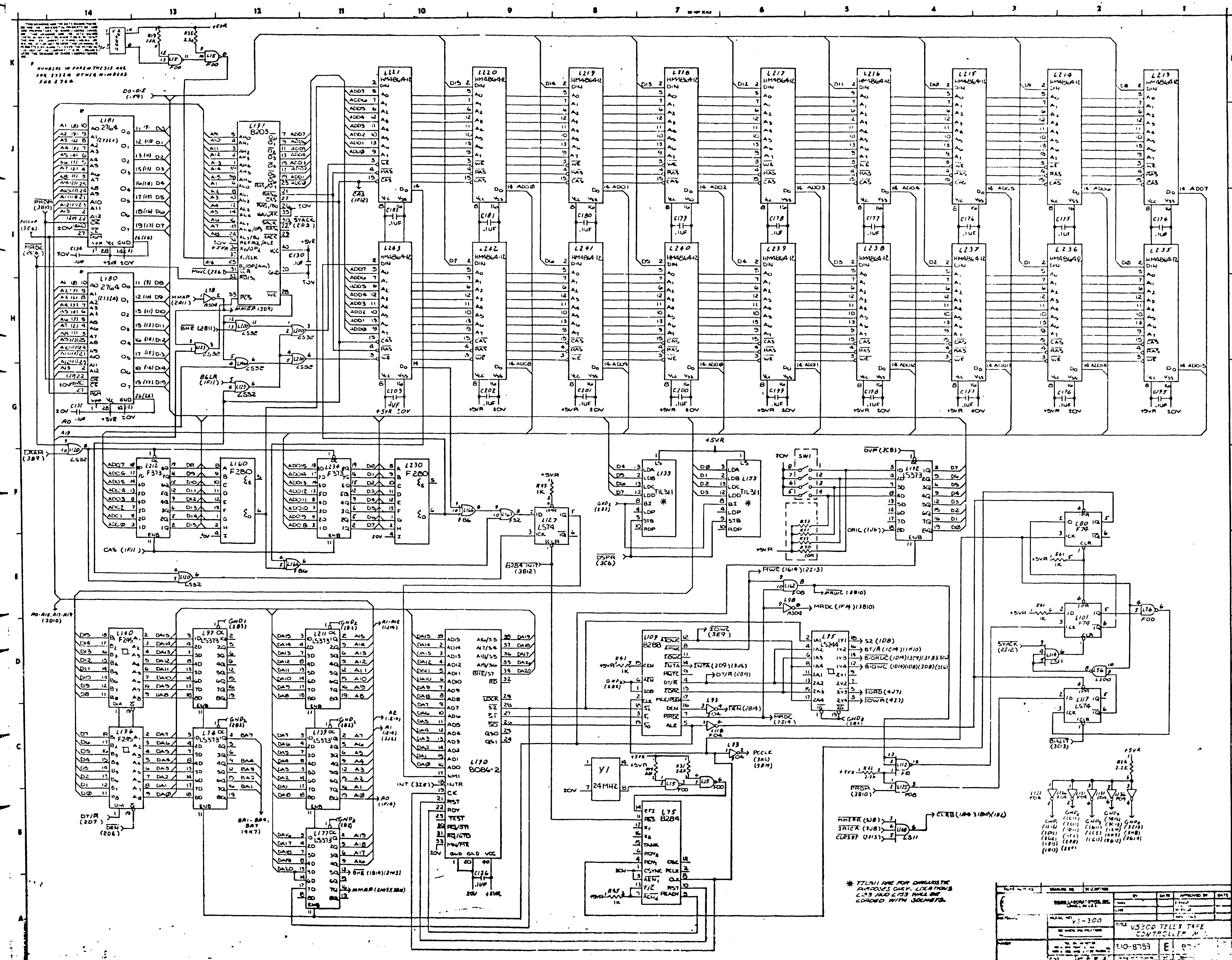


NOTES
1. UNLESS OTHERWISE SPECIFIED
ALL CAPACITORS ARE .047, EXPRESSED IN MICROFARADS.
ALL RESISTORS ARE 1K, 1/4W, 5%, EXPRESSED IN OHMS.
ALL CONNECTORS ARE 350-0058.
ALL RESISTOR NETWORKS ARE 333-0849 (58 OHMS).
2. C35,50,85,117-125,127,128,130,132,135-143,147,156,157,159,181 ARE .1 300-1930.
3. LOAD 24 PIN SKT.(378-8037) IN LOCATIONS L81,91,148,222,277.

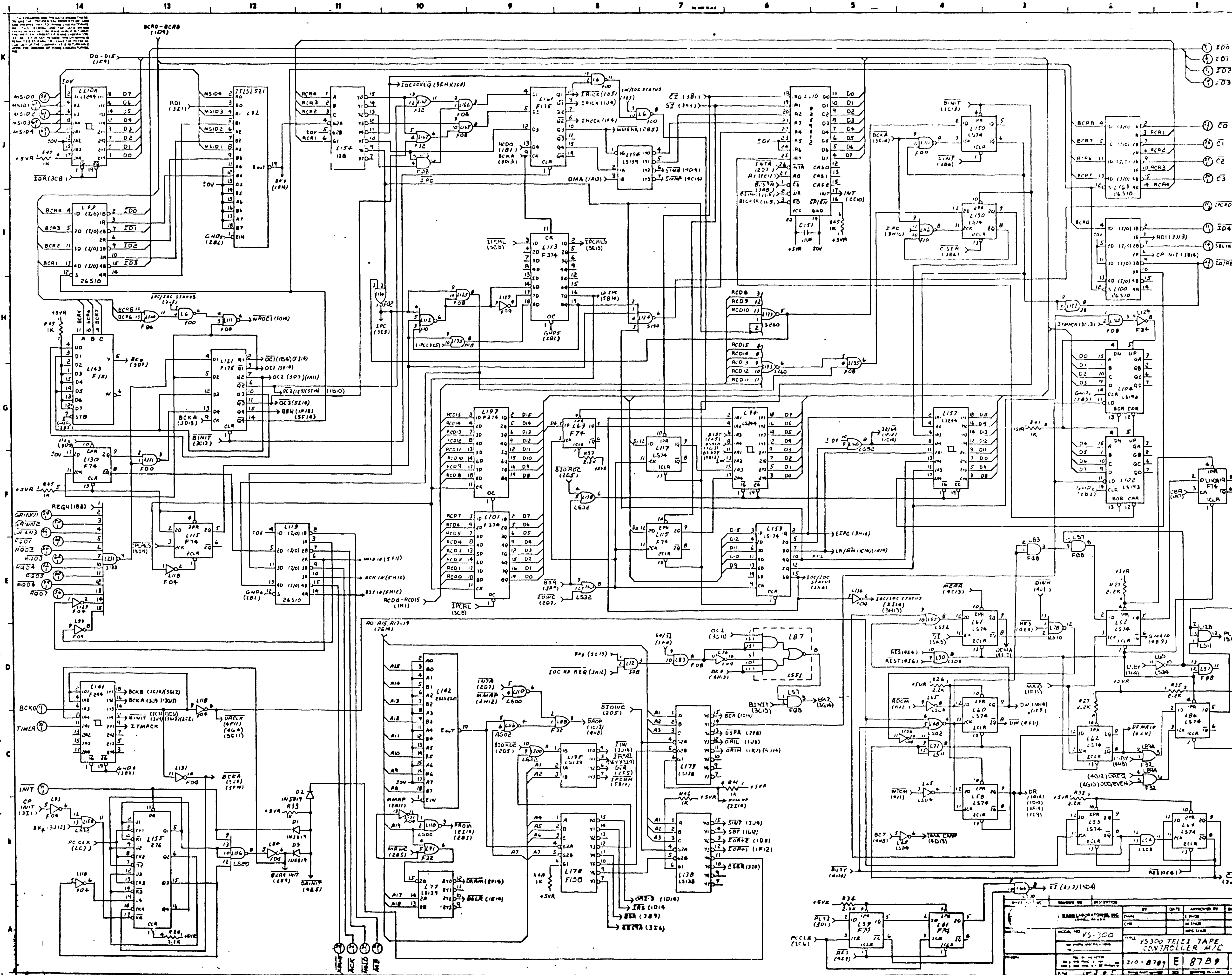
WANG LABORATORIES, INC.		BY	DATE	APPROVED BY	DATE
		DWN E PiEARS	4-21-05	E ENGR	
		CHK		M ENGR	
				MFG ENGR	
MATERIAL	MODEL NO. VS300	TITLE ASSEMBLY, VS300 SMD DISK CNTRL			
FINISH		210-8785	D	8785	4
	SCALE	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV



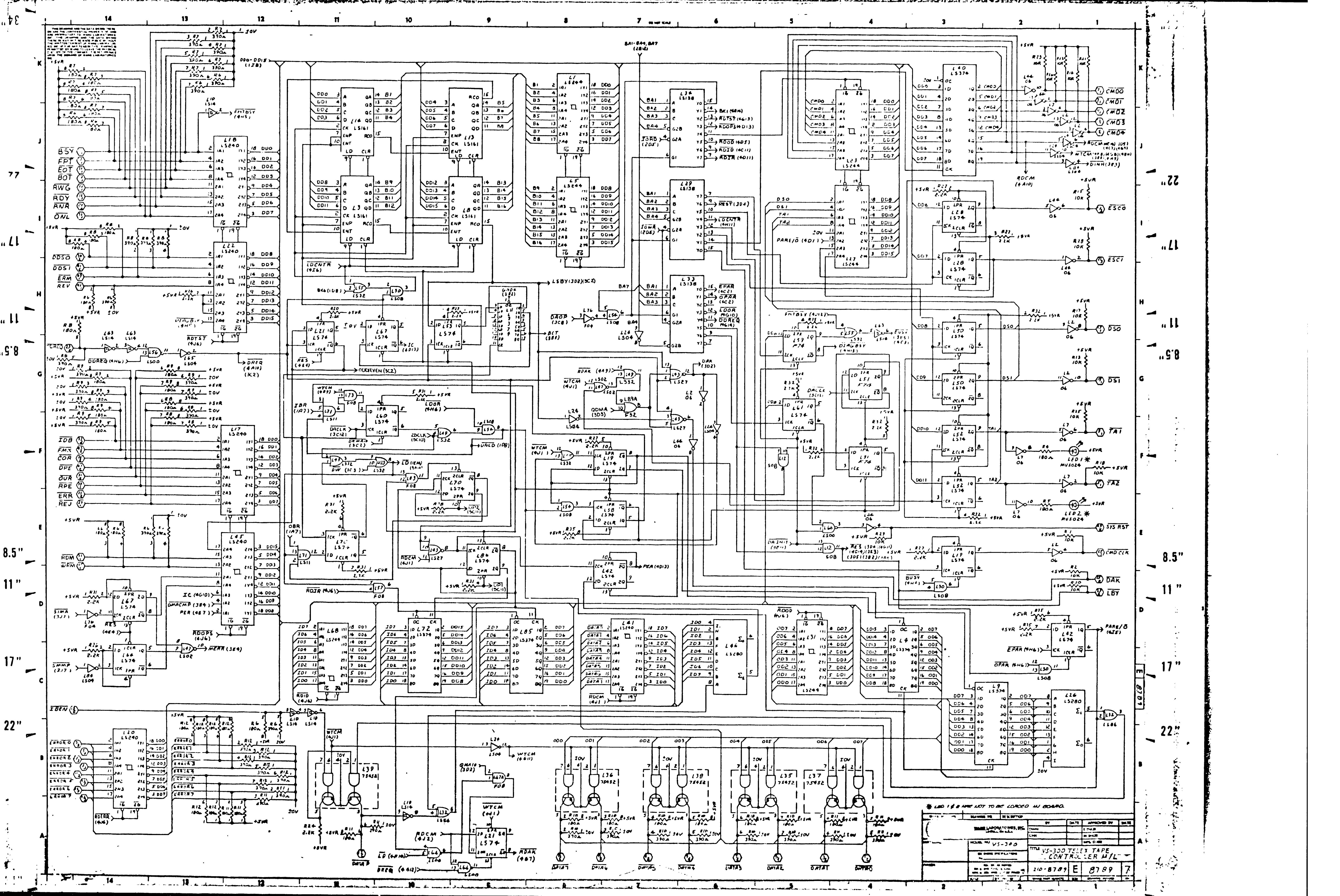
VS-300
VS300 TELEX TAPE CONTROLLER M/C
210-8789
E
8789
7



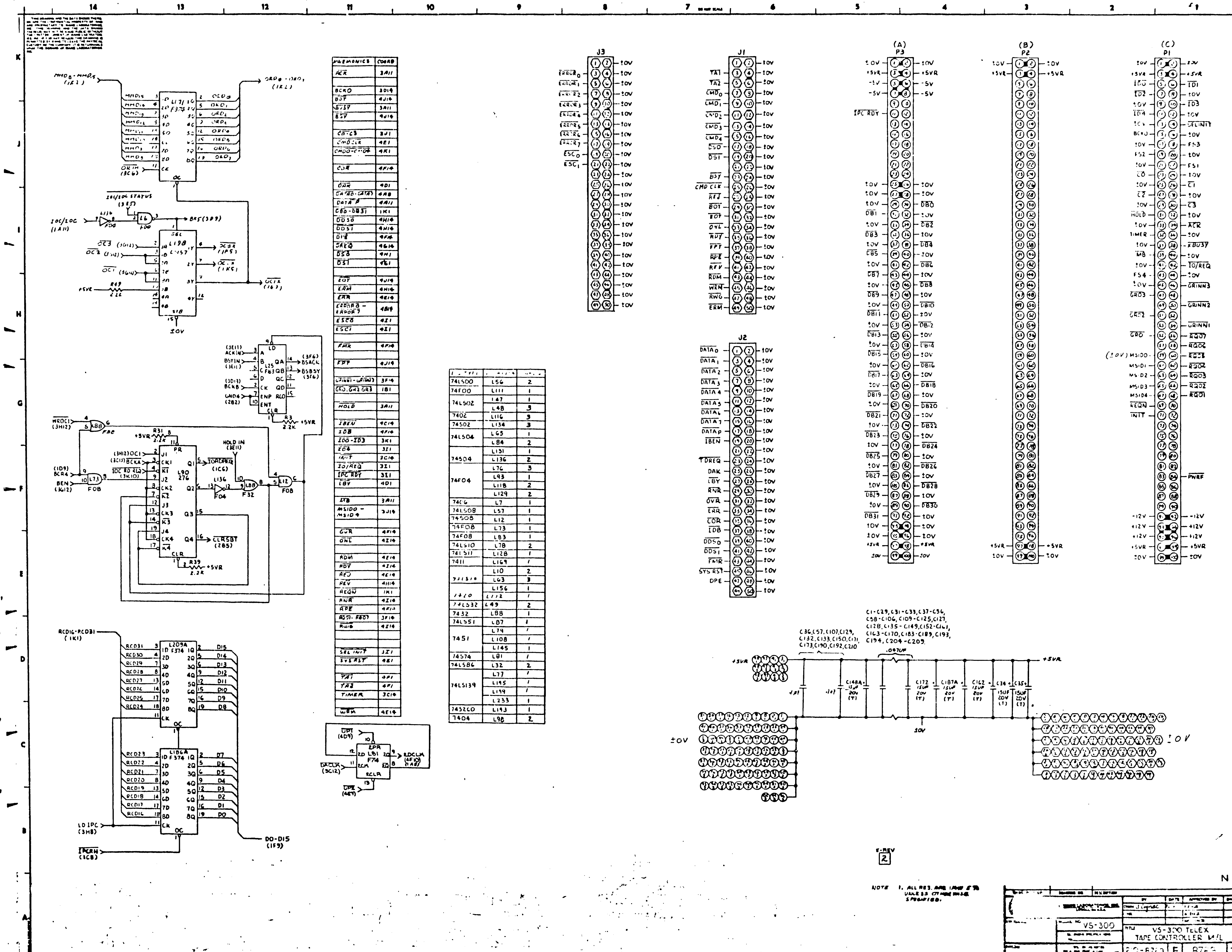
NUMBERS IN PARENTHESIS ARE FOR 27324 OTHER NUMBERS FOR 2764
L181 2764
L180 2764
L191 8203
HM4864-12
L170 8086-2
L109 8288
L75 8284
Y1 24MHZ
L133 TIL311
L153 TIL311
* TIL311 ARE FOR DIAGNOSTIC PURPOSES ONLY. LOCATIONS L133 AND L153 WILL BE LOADED WITH SOCKETS.
VS-300
VS300 TELEX TAPE CONTROLLER
310-8759



WANG LABORATORIES, INC.
MODEL NO VS-300
TITLE VS300 TELEX TAPE CONTROLLER M/L
210-8789
E
8789
7



* LED 1 & 2 ARE NOT TO BE LOADED ON BOARD.
VS-300 TELEX TAPE CONTROLLER M/L
210-8789
E
8789
7



MNEMONICS	COORD
ACR	3A11
BCKO	3D14
BOT	4J14
BUSY	3A11
BSY	4J14
C0-C3	3J1
CMD CLK	4E1
CMD0-CMD4	4K1
COR	4F14
DAK	4D1
DATA0-DATA7	4A8
DATA P	4A11
DB0-DB31	1K1
DDS0	4H14
DDS1	4H14
DPE	4F14
DREQ	4G14
DS0	4H1
DS1	4G1
EOT	4J14
ERM	4H14
ERR	4E14
ERROR0 - ERROR7	4B14
ESC0	4I1
ESC1	4I1
FMK	4F14
FPT	4J14
GRINN1-GRINN3	3F14
GR0, GR2 GR3	1B1
HOLD	3A11
IBEN	4C14
IDB	4F14
ID0-ID3	3K1
ID4	3I1
INIT	3C14
IO/REQ	3I1
IPC RDY	3I1
LBY	4D1
MB	3A11
MSID0 - MSID4	3J14
OVR	4F14
ONL	4I14
RDM	4E14
RDY	4I14
REJ	4E14
REV	4H14
REQN	1K1
RNR	4I14
RPE	4F14
RQ01- RQ07	3F14
RWG	4I14
SEL INIT	3I1
SYS RST	4E1
TA1	4F1
TA2	4F1
TIMER	3C14
WEM	4E14

74LS00	L56	2
74F00	L111	1
74LS02	L47	1
	L48	3
7402	L116	3
74S02	L134	3
74LS04	L65	1
	L84	2
74S04	L131	1
	L136	2
74F04	L76	3
	L93	1
	L118	2
	L129	2
7406	L7	1
74LS08	L57	1
74S08	L12	1
74F08	L73	1
74F08	L83	1
74LS10	L78	2
74LS11	L128	1
7411	L169	1
74LS14	L10	2
	L63	3
7420	L156	1
	L112	1
74LS32	L49	2
7432	L88	1
74LS51	L87	1
7451	L79	1
	L108	1
	L145	1
74S74	L81	1
74LS86	L32	2
74LS139	L77	1
	L195	1
	L199	1
	L233	1
74S260	L193	1
7404	L98	2

E-REV 2

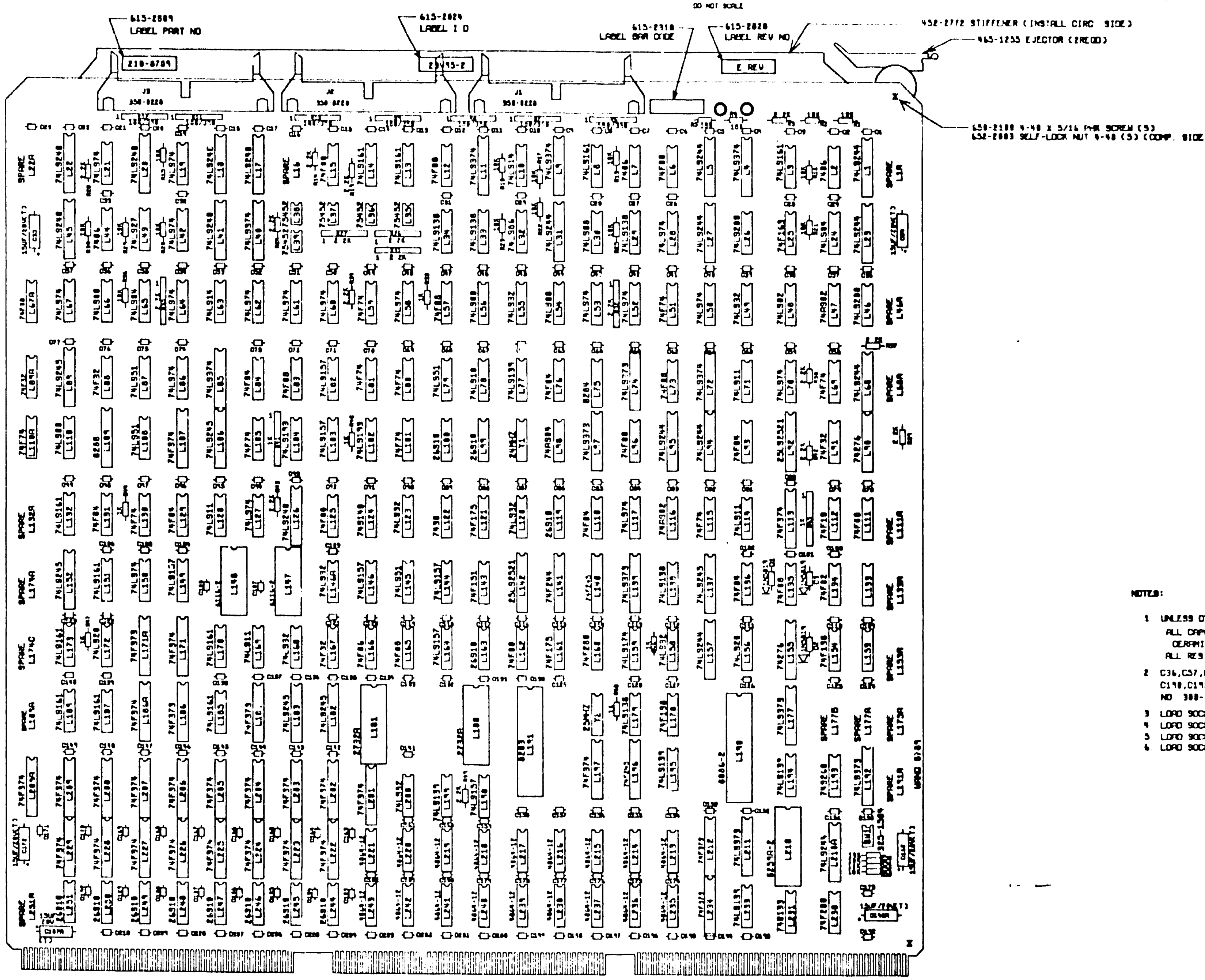
NOTE 1. ALL RES. ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

VS-300

TITLE VS-300 TELEX TAPE CONTROLLER M/L

210-8769 E 8769 7

DO NOT SCALE



NOTES:

1 UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE EXPRESSED IN MICROFARADS, 0 047, 50V, CERAMIC, WANG PART NO. 300-1966.
ALL RESISTORS ARE EXPRESSED IN OHMS, 1/4W, 5 PER CENT.

2 C36,C57,C107,C108,C126,C129-C134,C150,C151,C171,C173-C182, C190,C192,C195-C203,C210 ARE 0 1UF, 50V, H F., WANG PART NO 300-1033.

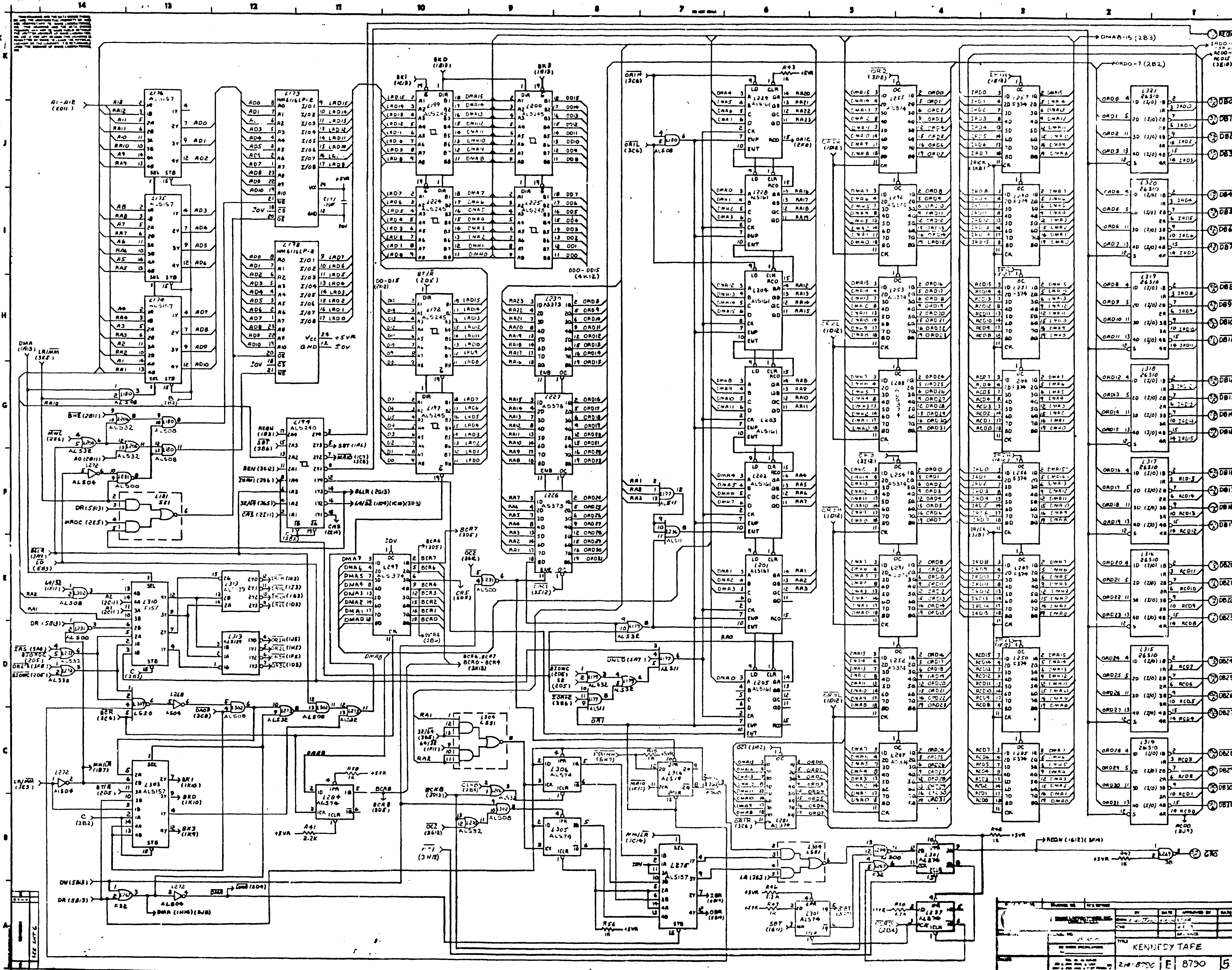
3 LOAD SOCKET 376-9001T (L133,L153).

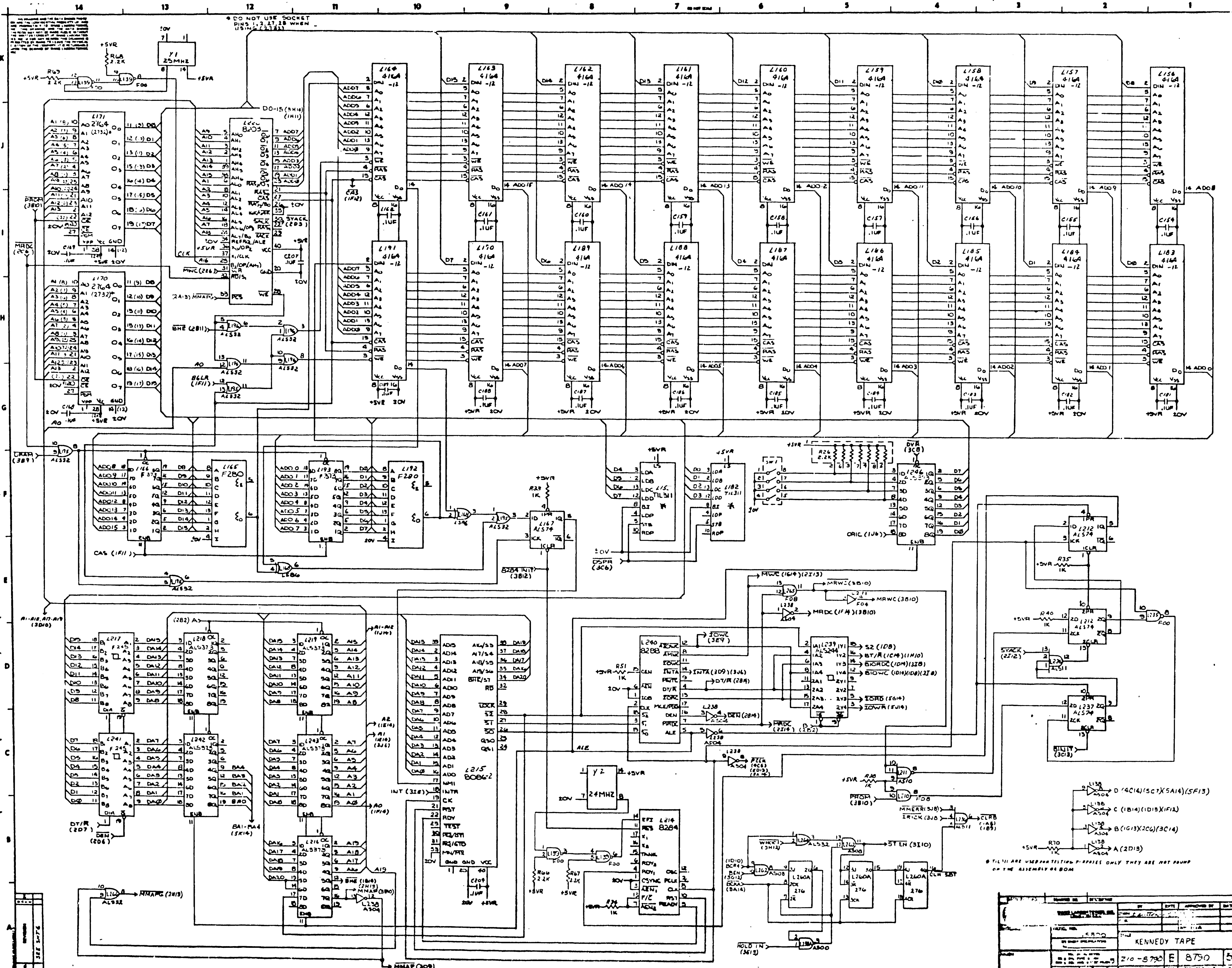
4 LOAD SOCKET 376-9008 (Y1,Y2).

5 LOAD SOCKET 376-9011 (L190).

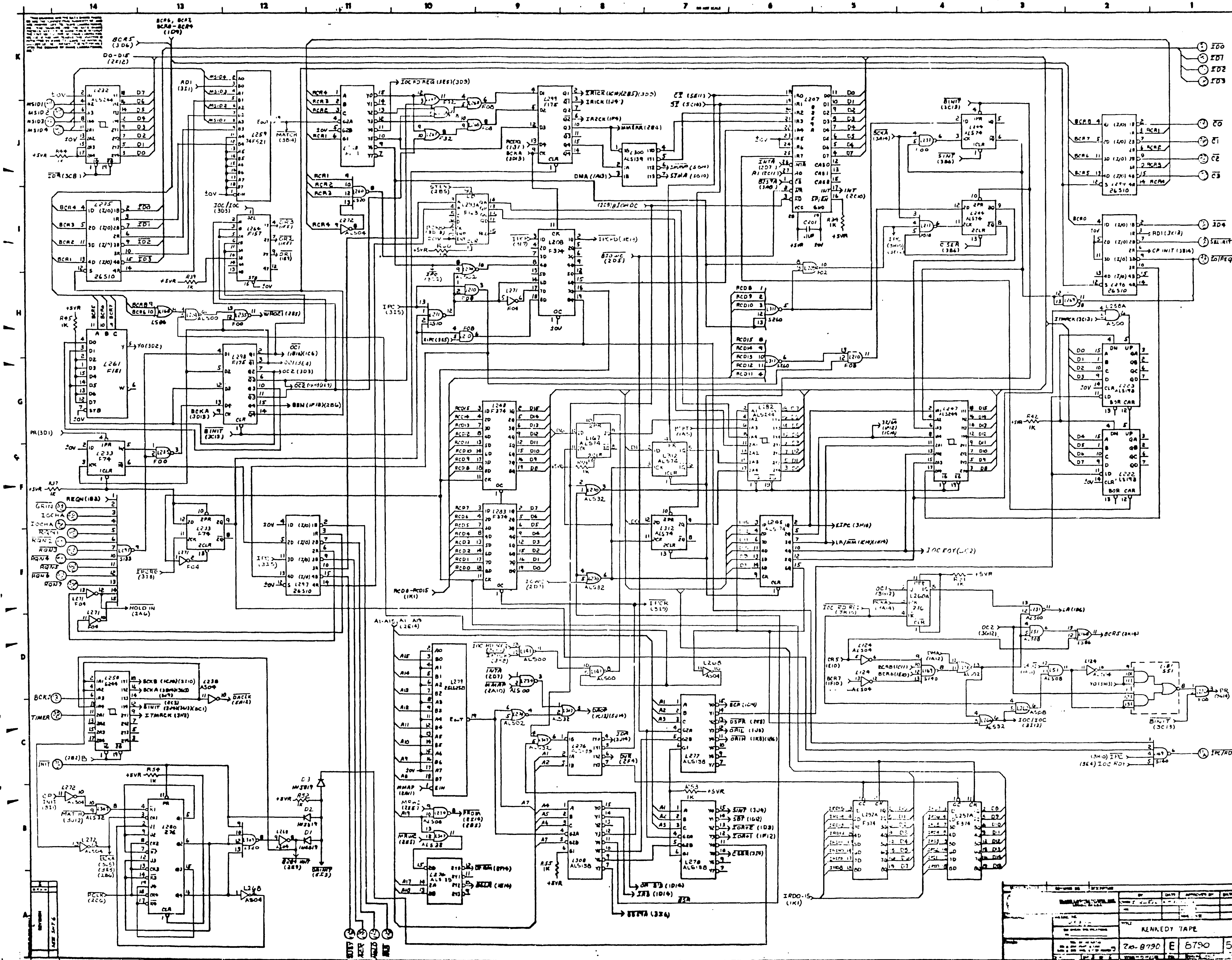
6. LOAD SOCKET 376-9015 (L180-L181).

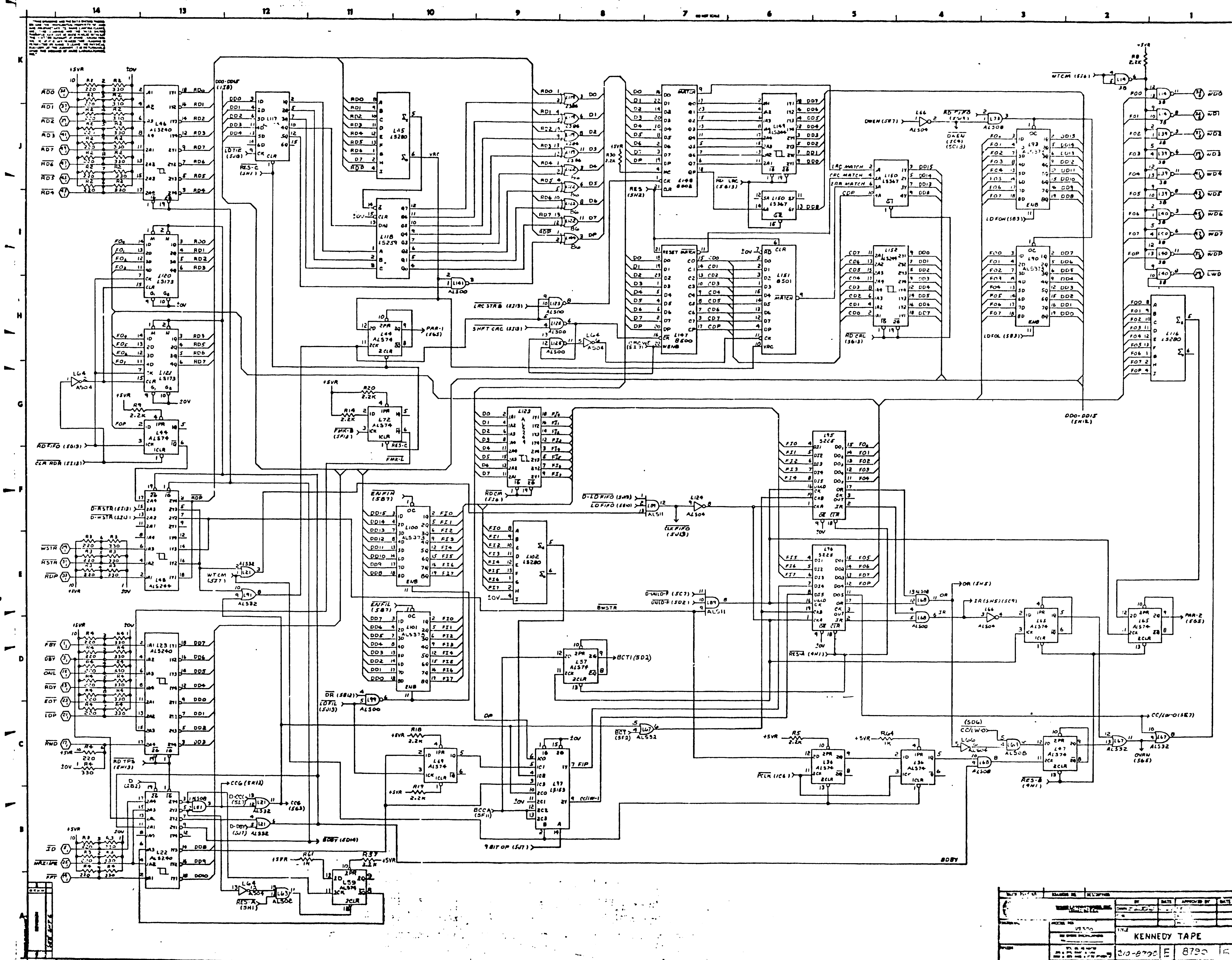
WANG LABORATORIES, INC.				
DWN P APREA				
CHK J LEARY				
MATERIAL —//—	MODEL NO VS-300	TITLE ASSEMBLY DRAWING TELEX TAPE CONTROLLER		
	NO 10-219			
FINISH —//—	SCALE 1/1	210-8789	D	8789 9


KENNEDY TAPE
E
8790
5

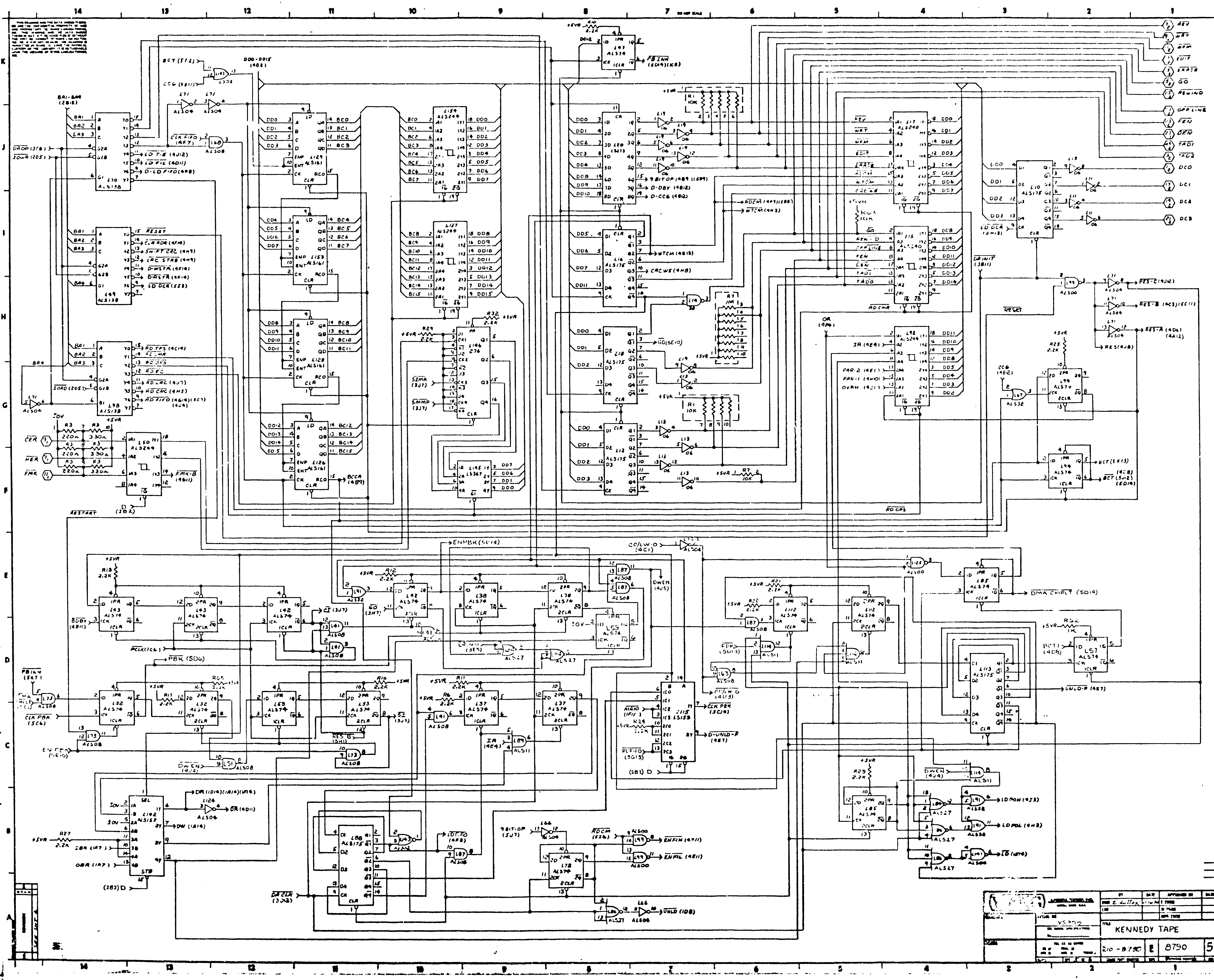


DO NOT USE SOCKET PINS 1,2,27,28 WHEN USING 2732
25MHZ
8085
416A
F280
8288
8086-2
8284
24MHZ
TIL311
KENNEDY TAPE
210-8790
E
8790
5


KENNEDY TAPE
210-8790
E
8790
5



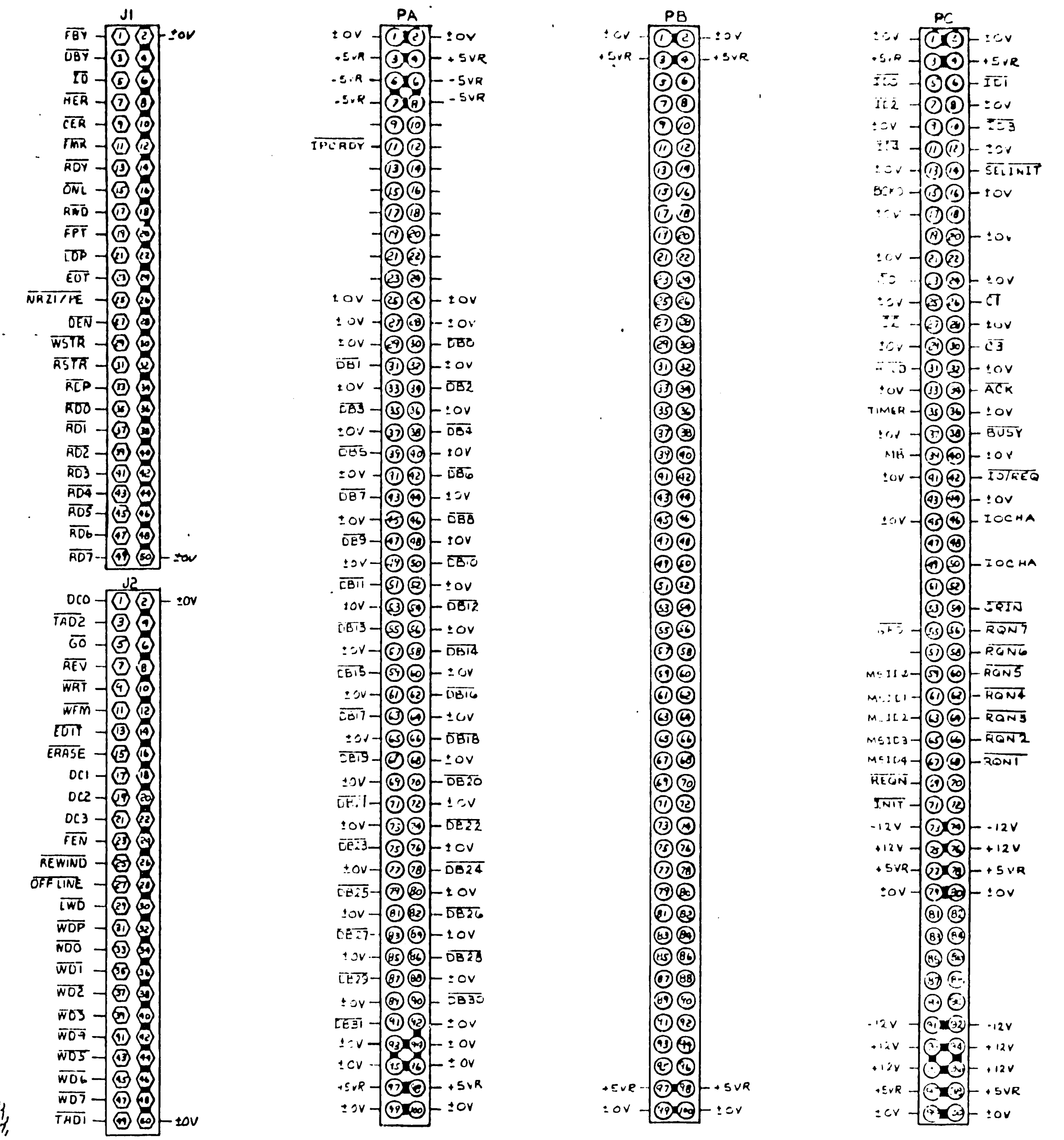
KENNEDY TAPE
210-8790
8790

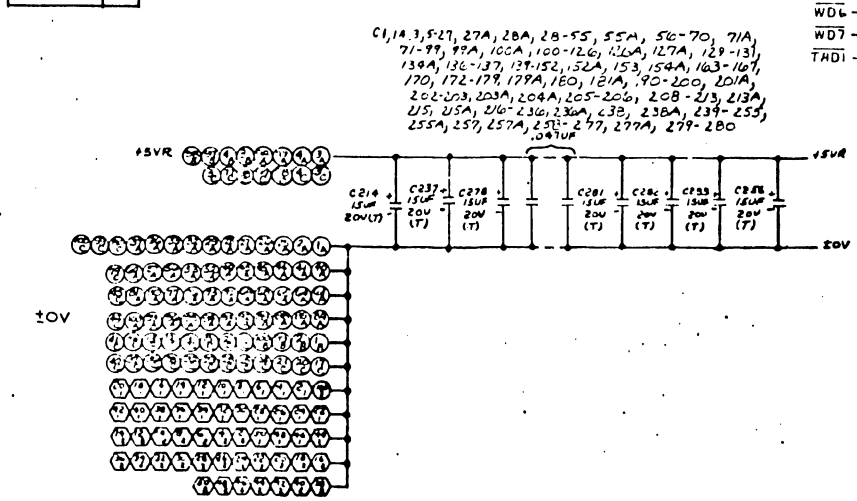


KENNEDY TAPE
210-8790
E
8790
5

TYPE	IC LOCATION	SPARES
74ALS02	L143	2
	L274	2
74ALS139	L300	1
74ALS32	L71	1
	L179	1
	L266	1
74ALS74	L69	1
	L284	1
	L305	1
74AS00	L258A	2
74AS04	L64	3
	L138	2
	L268	2
74F02	L209	3
74F04	L271	1
74F08	L265	1
	L232A	2
74LS20	L260	1
74LS367	L145	2
7406	L11	3
7486	L144	3
1438	L269	2
74ALS32	L270	1
SPARE	L1A, 1-9, 24-35, 25A, 26A, 53A, 54-56, 58, 60-62, 74A, 74-83, 102A, 103A, 105-111, 129A, 130A, 131-133, 154A, 156A, 178, 181A, 183A, 207A, 231A, 321A	

MNEMONICS	COORD
ACK	3A11
BCKD	3D14
BUSY	3A11
C0-C3	3J1
CER	5G14
DB0-DB31	1K1
DBY	4D14
DC0-DC3	5J1
DEN	5J1
EDIT	5K1
EOT	4D14
ERASE	5K1
FBY	4D14
FEN	5J1
FPT	4A14
FMK	5F14
GRIN	3F14
GRO	1B1
GO	5K1
HOLD	3A11
HER	5F14
ID	4B14
IDO-ID3	3K1
ID4	3I1
INIT	3C14
IO/REQ	3I1
IPC/RDY	3C1
LDP	4C14
LWD	4I1
MSID0-MSID4	3J14
MB	3A11
NRZI/PE	4B14
OFF LINE	5J1
ONL	4D14
RD0-RD7	4K14
RDP	4E14
RDY	4D14
REV	5K1
REQN	1K1
REWIND	5K1
RQN1-RQN7	3E14
RSTR	4E14
RWD	4C14
SEL INIT	3I1
TAD1	5J1
TAD2	5J1
TIMER	3C14
WDP	4I1
WD0-WD7	4K1
WRT	5K1
WSTR	4E14
WFM	5K1





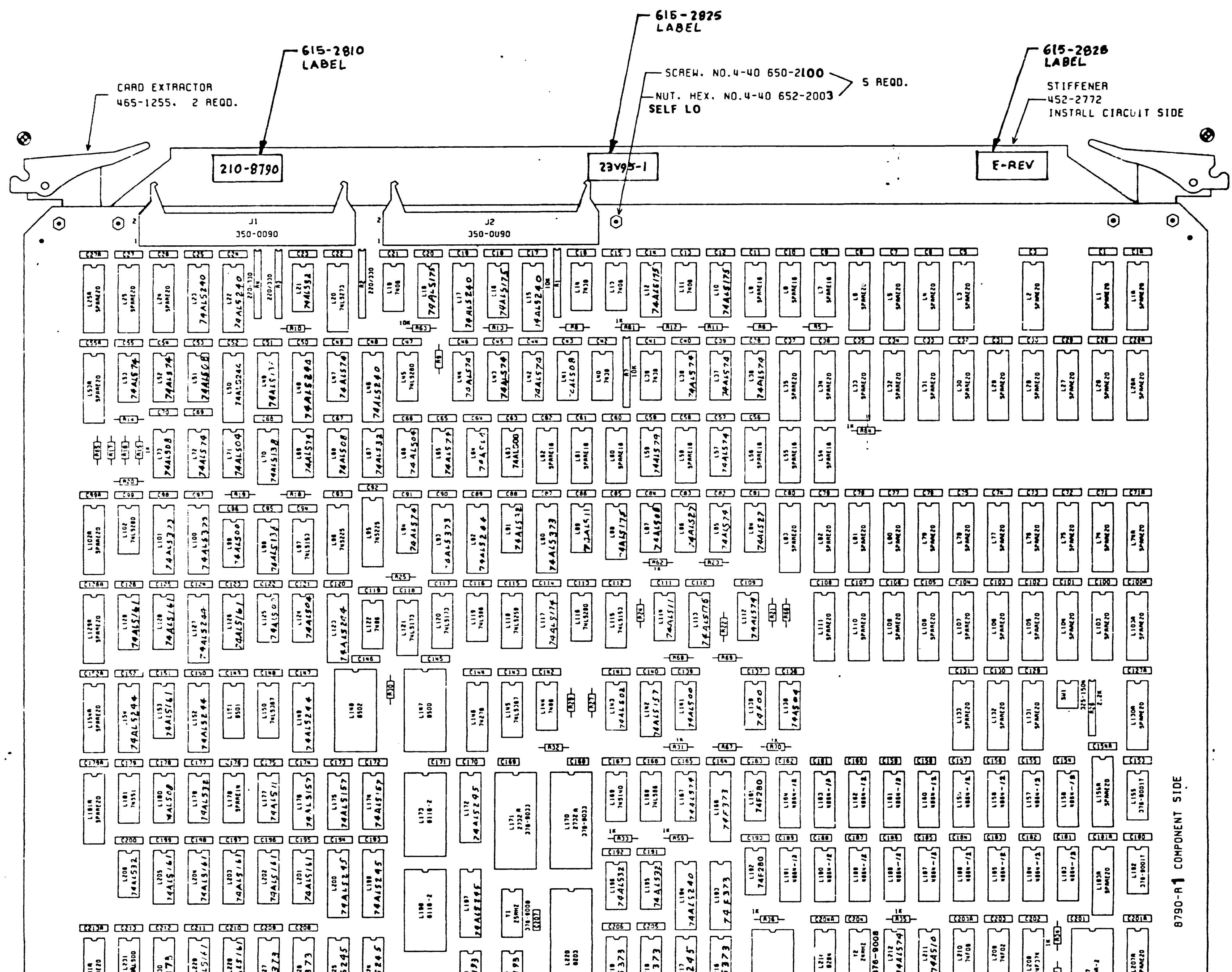
NOTE:
1. ALL RES. ARE 1/4W, 5% UNLESS OTHERWISE SPECIFIED.

E-REV
0

VS-300

KENNEDY TAPE

210-8790 | E | 8790 | 5



NOTES
1. UNLESS OTHERWISE SPECIFIED
ALL CAPACITORS ARE .047. EXPRESSED IN MICROFARADS.
ALL RESISTORS ARE 2.2K. 1/4W. 5% EXPRESSED IN OHMS.
2. C154-162.168.169.171.181-189.201.204.207 ARE .1.
3. R31,63,70 ARE 1K 5%

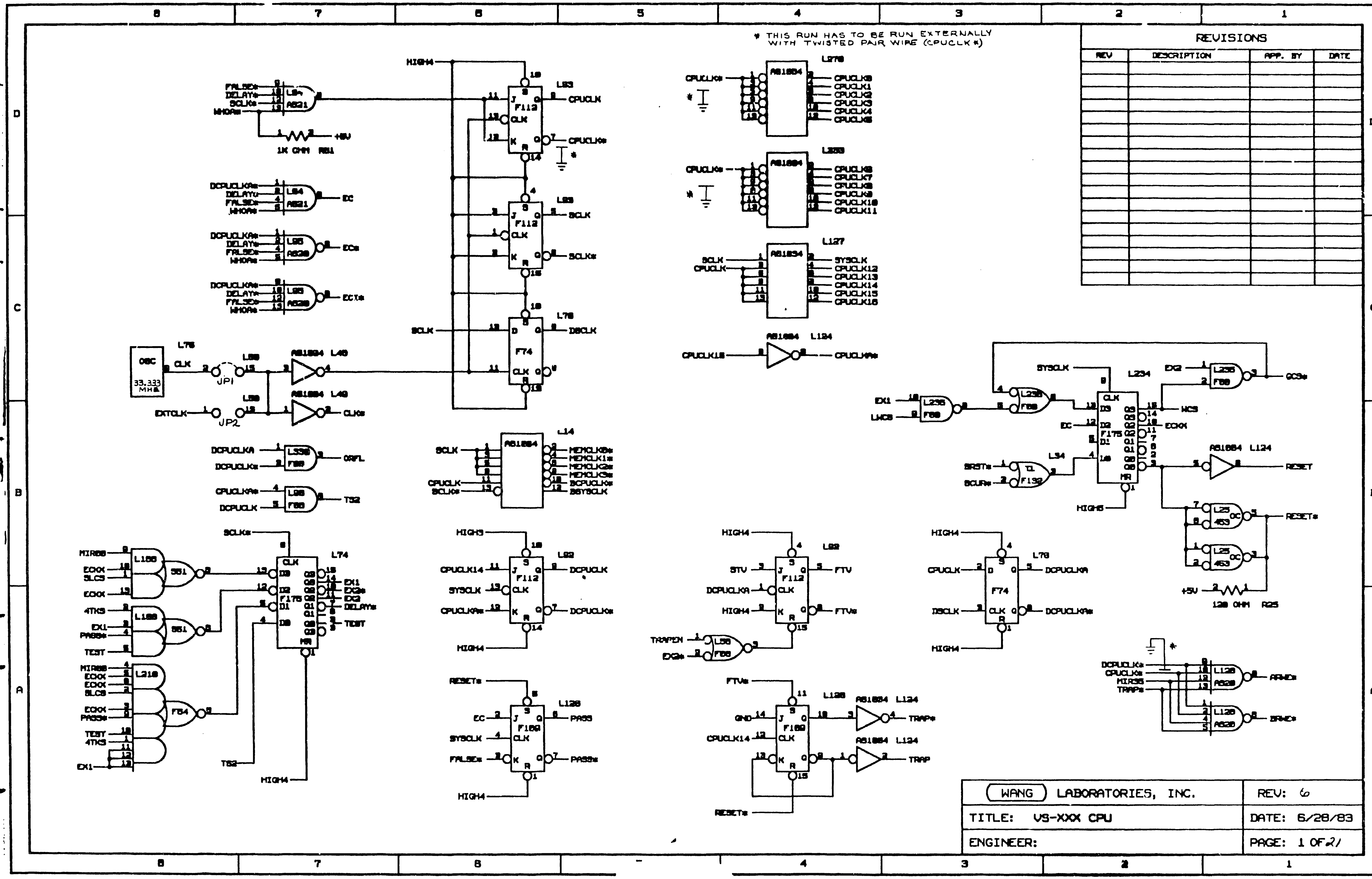
WANG LABS KENNEDY TAPE CONTROLLER
ASSEMBLY DRAWING
REV. 6 PER E.C.O. NO. 37821 9 OCT,85

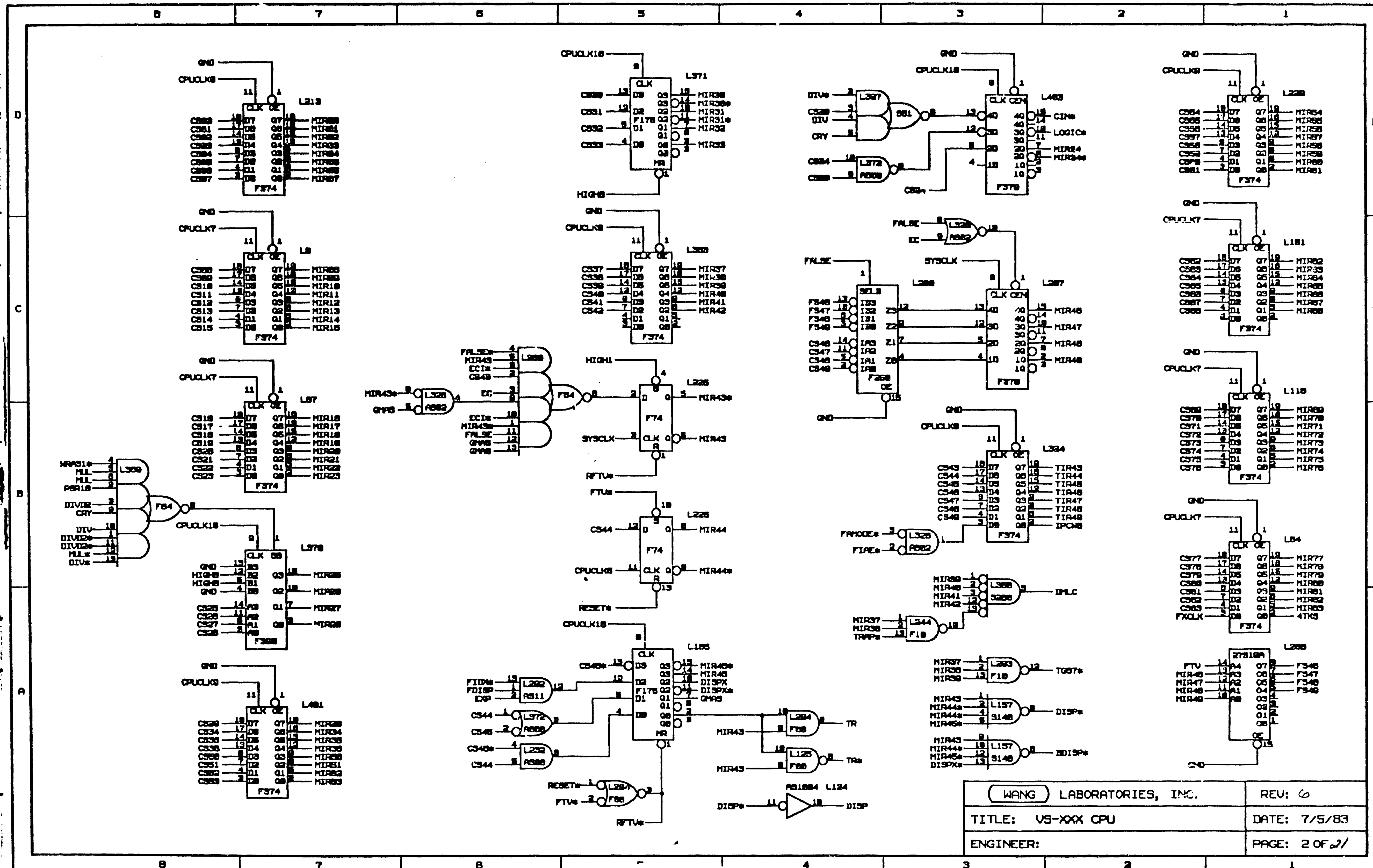
VS-XXX CPU INDEX

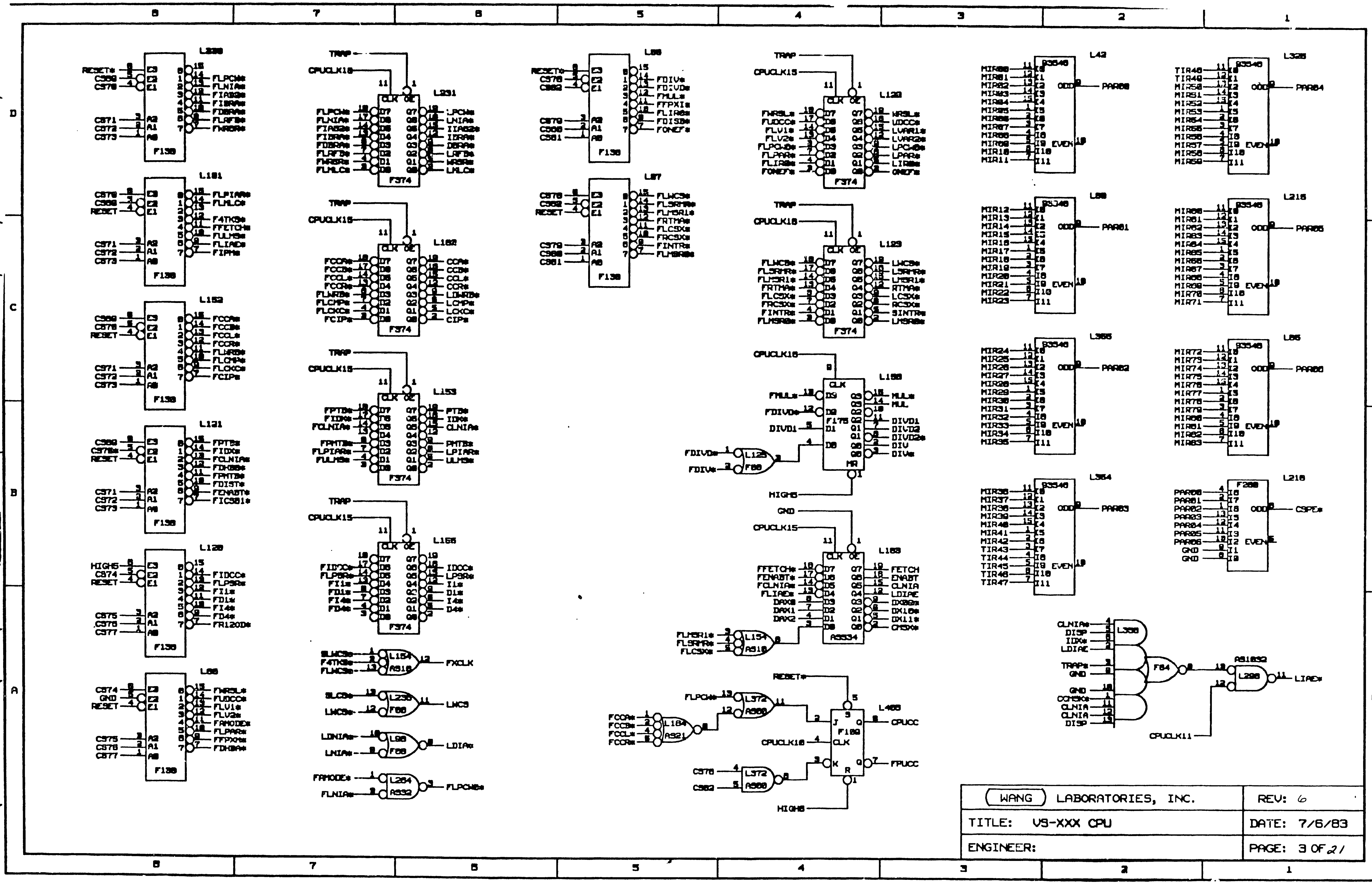
PAGE CONTENTS

E-REV 3

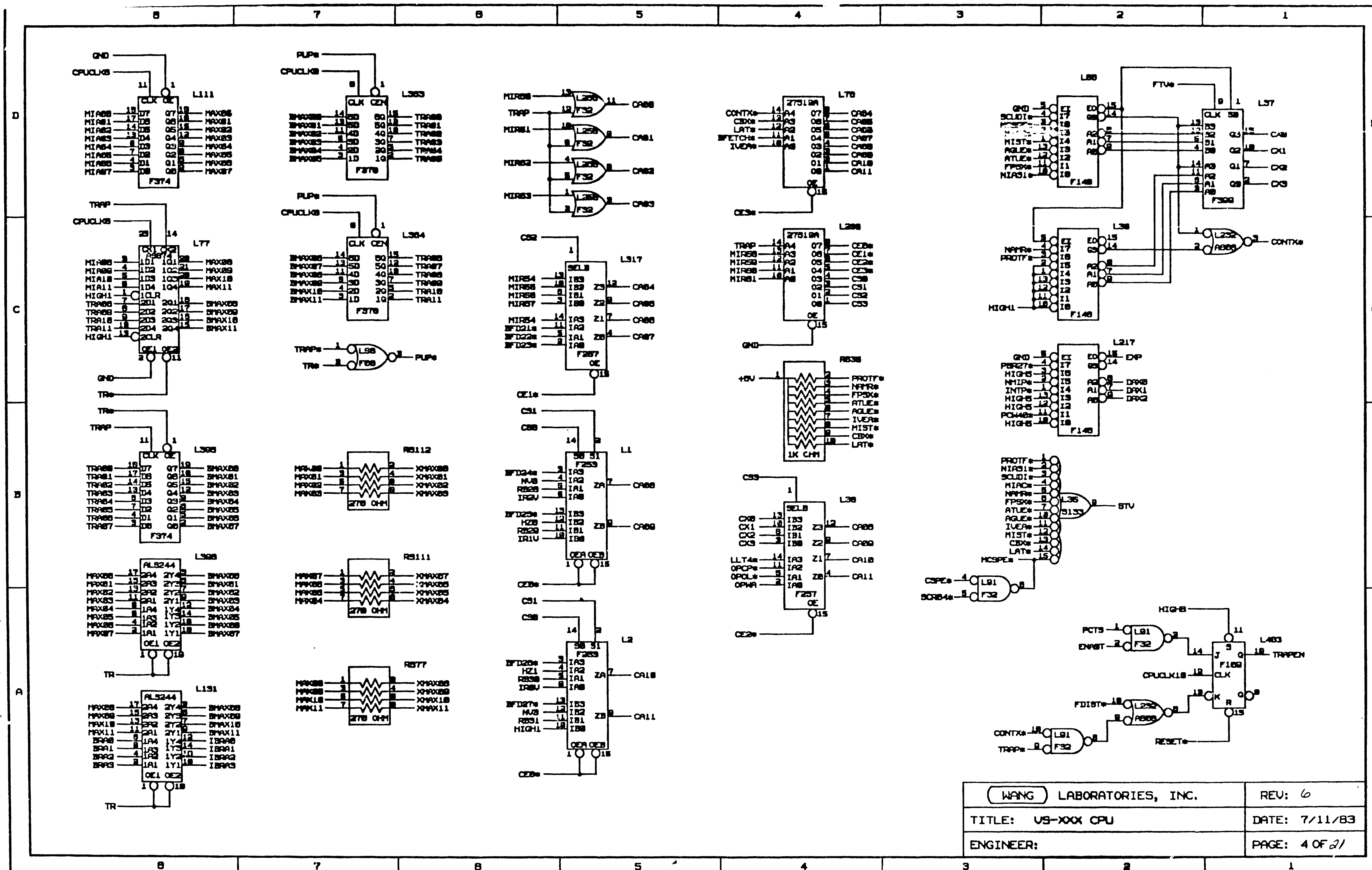
WANG LABORATORIES, INC.	REV: R6
TITLE: VS-XXX CPU	DATE: 02/13/84
ENGINEER:	PAGE: Ø OF 21


* THIS RUN HAS TO BE RUN EXTERNALLY WITH TWISTED PAIR WIRE (CPUCLK*)
REVISIONS
REV
DESCRIPTION
APP. BY
DATE
OSC 33.333 MHz
WANG LABORATORIES, INC.
REV: 6
TITLE: VS-XXX CPU
DATE: 6/28/83
ENGINEER:
PAGE: 1 OF 21


WANG LABORATORIES, INC.
REV: 6
TITLE: VS-XXX CPU
DATE: 7/5/83
ENGINEER:
PAGE: 2 OF 21



WANG LABORATORIES, INC.
REV: 6
TITLE: VS-XXX CPU
DATE: 7/6/83
ENGINEER:
PAGE: 3 OF 21



WANG LABORATORIES, INC.

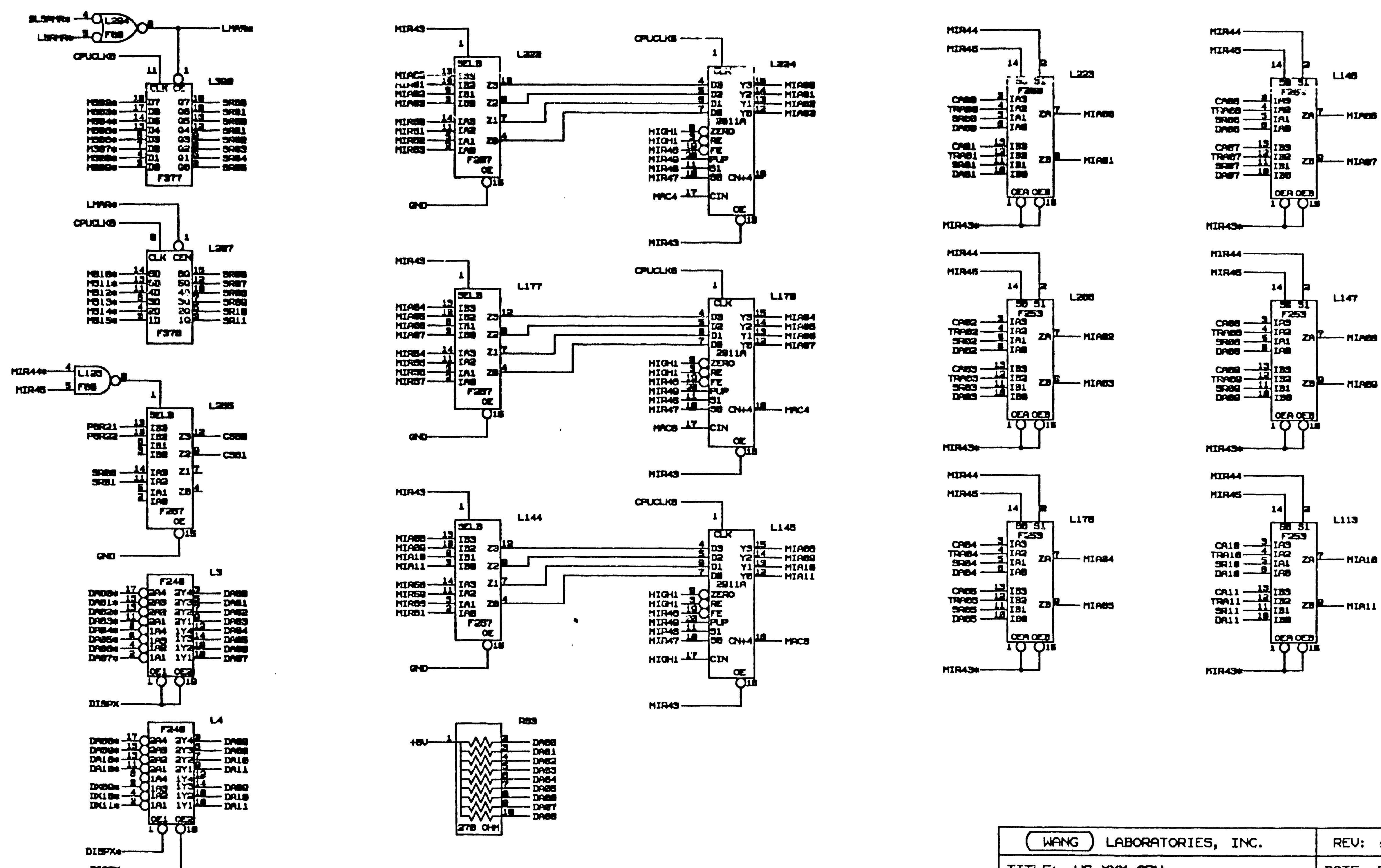
REV: 6

TITLE: VS-XXX CPU

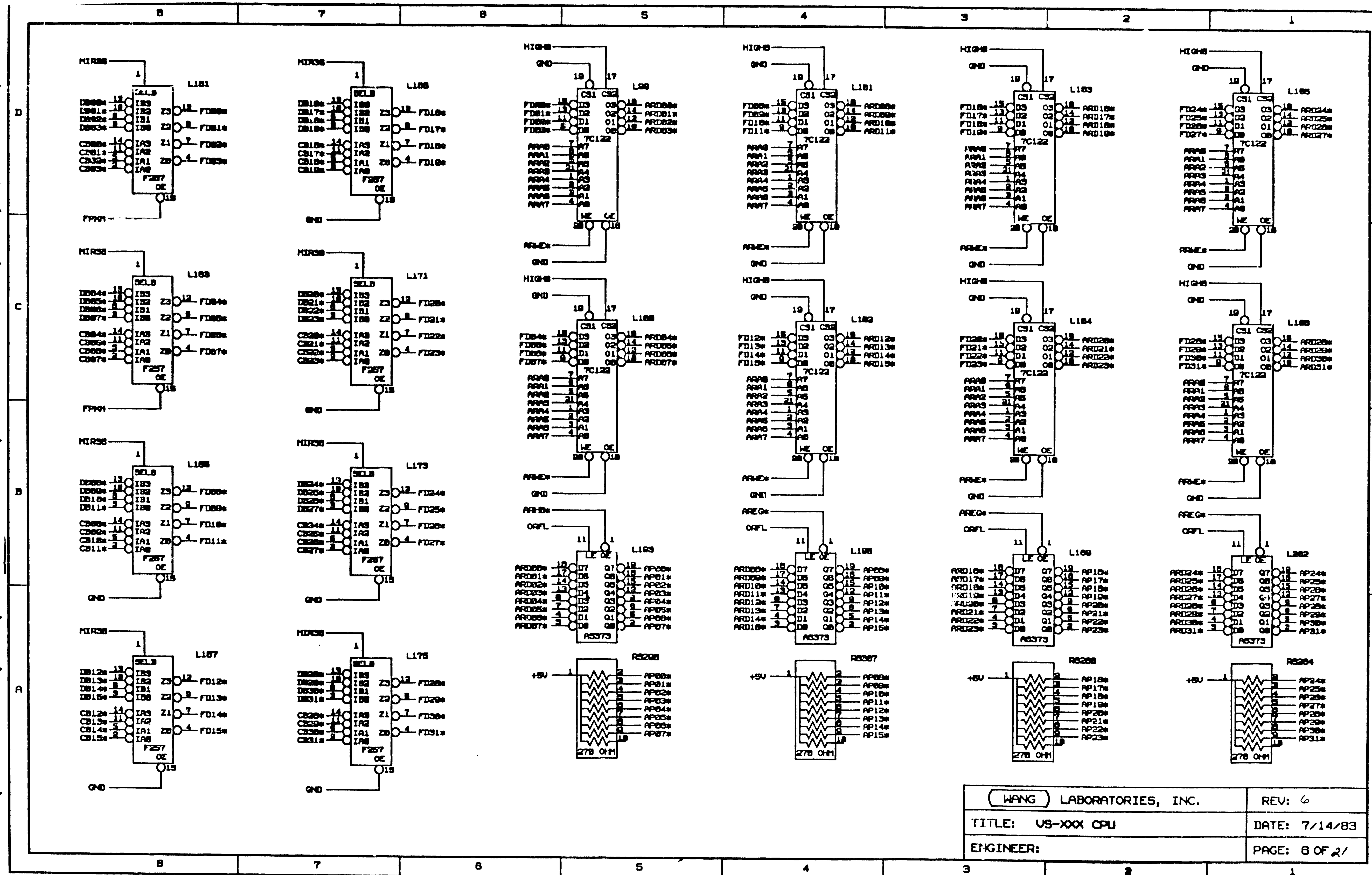
DATE: 7/11/83

ENGINEER:

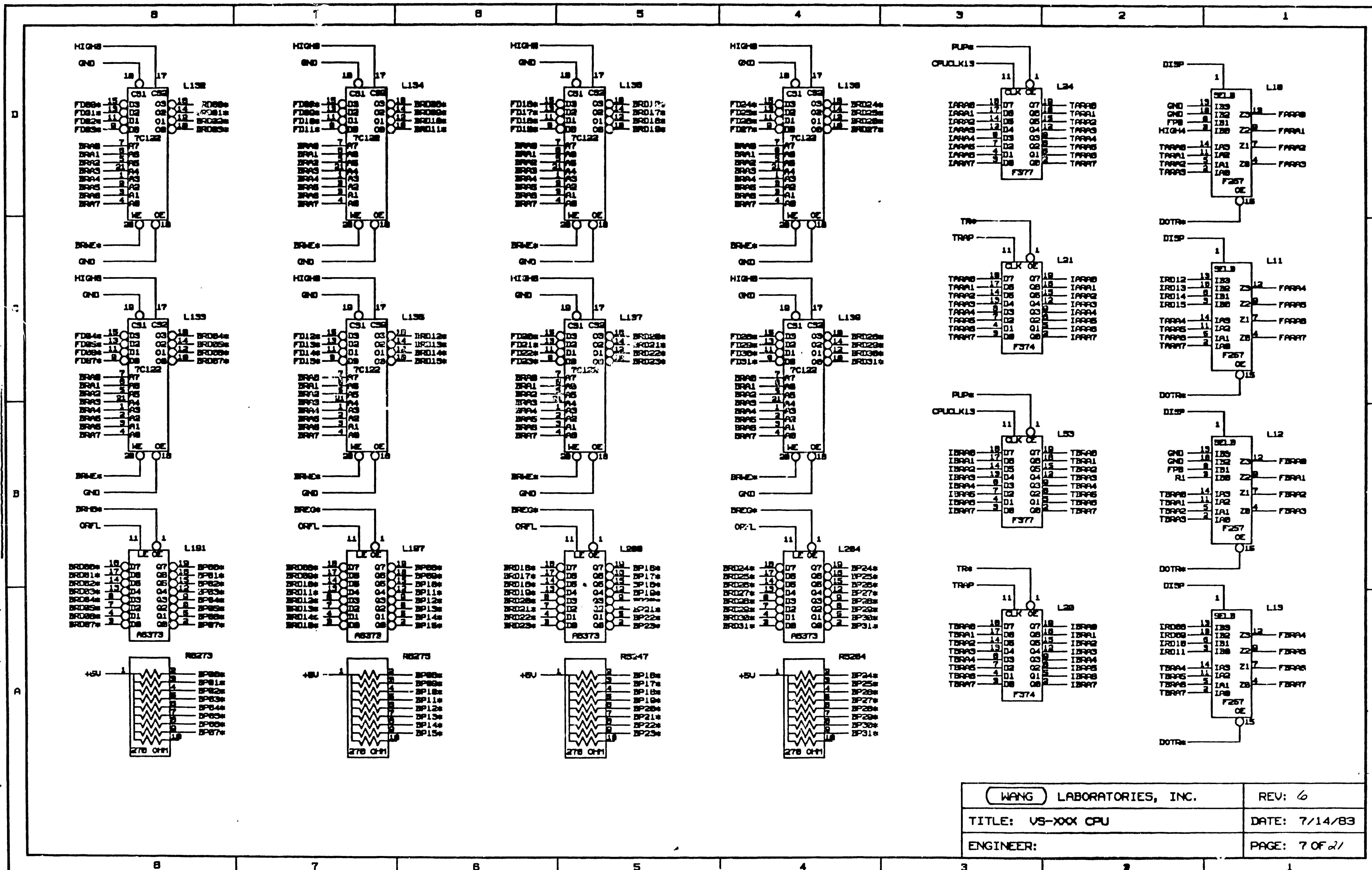
PAGE: 4 OF 21



WANG LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/12/83
ENGINEER:	PAGE: 5 OF 21



WANG LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/14/83
ENGINEER:	PAGE: 8 OF 21



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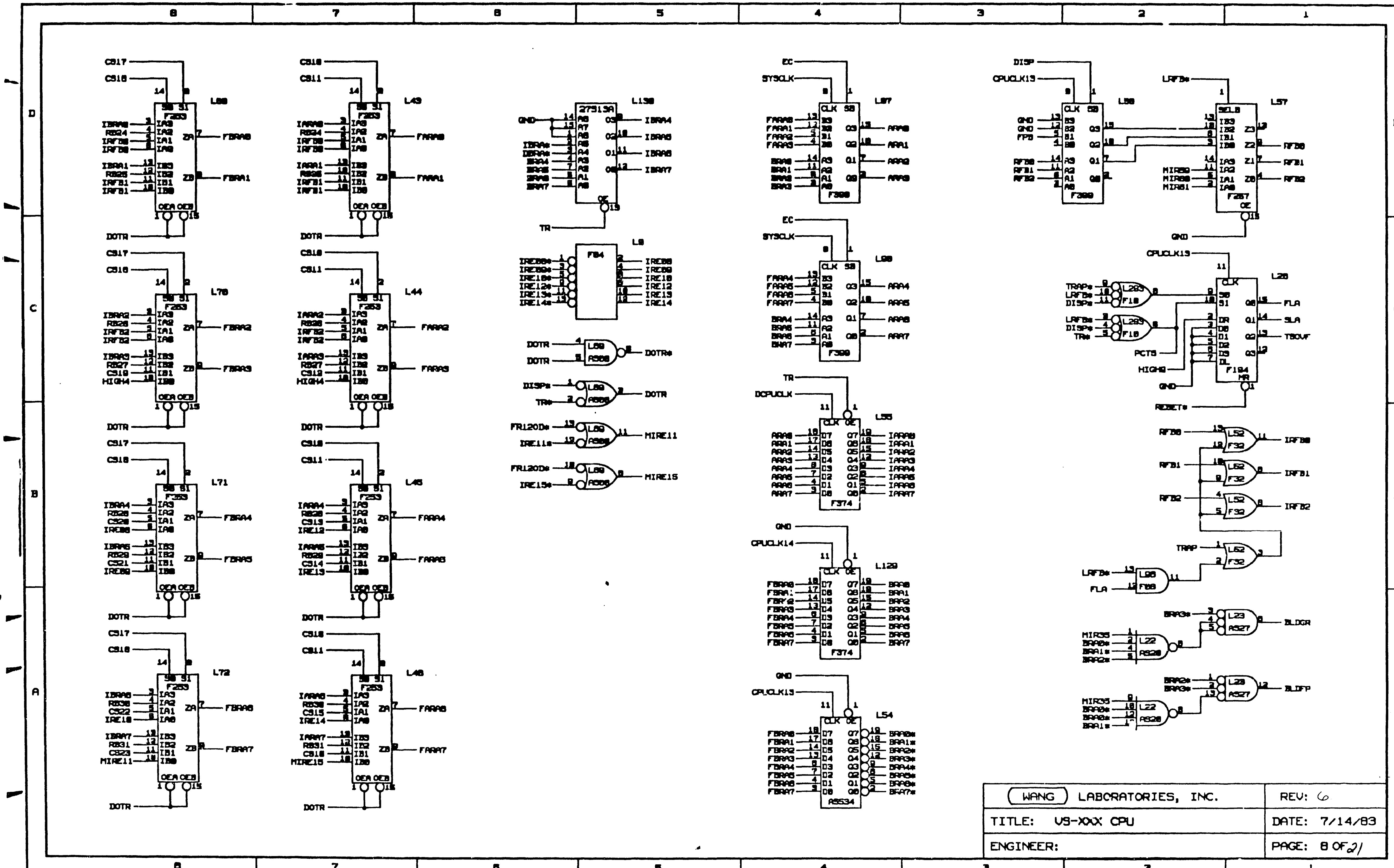
TITLE: VS-XXX CPU	DATE: 7/14/83
ENGINEER:	PAGE: 7 OF 21



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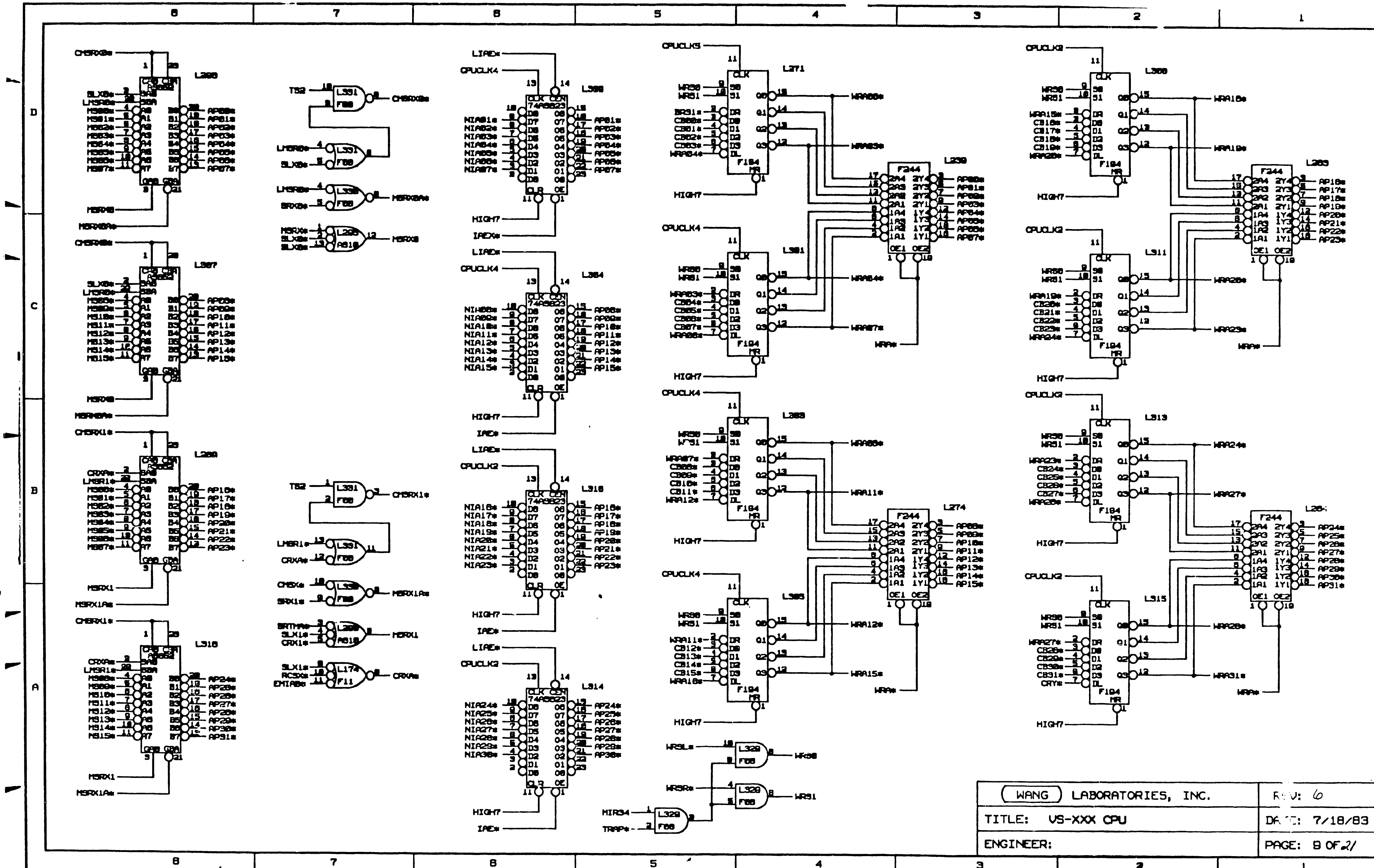
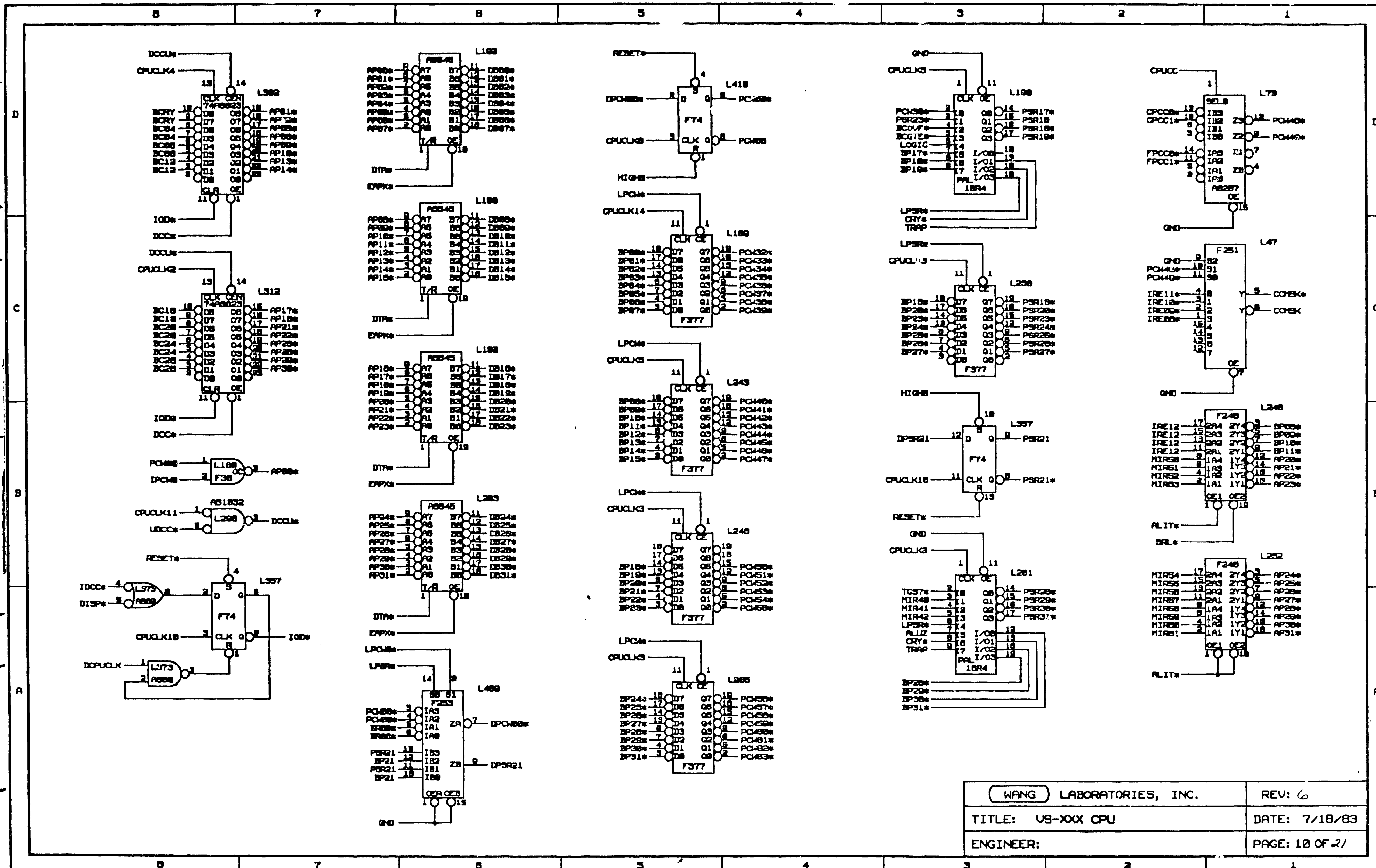
TITLE: VS-XXX CPU	DATE: 7/14/83
ENGINEER:	PAGE: 8 OF 21


WANG LABORATORIES, INC.
REV: 6
TITLE: VS-XXX CPU
DATE: 7/18/83
ENGINEER:
PAGE: 8 OF 21



WANG LABORATORIES, INC.

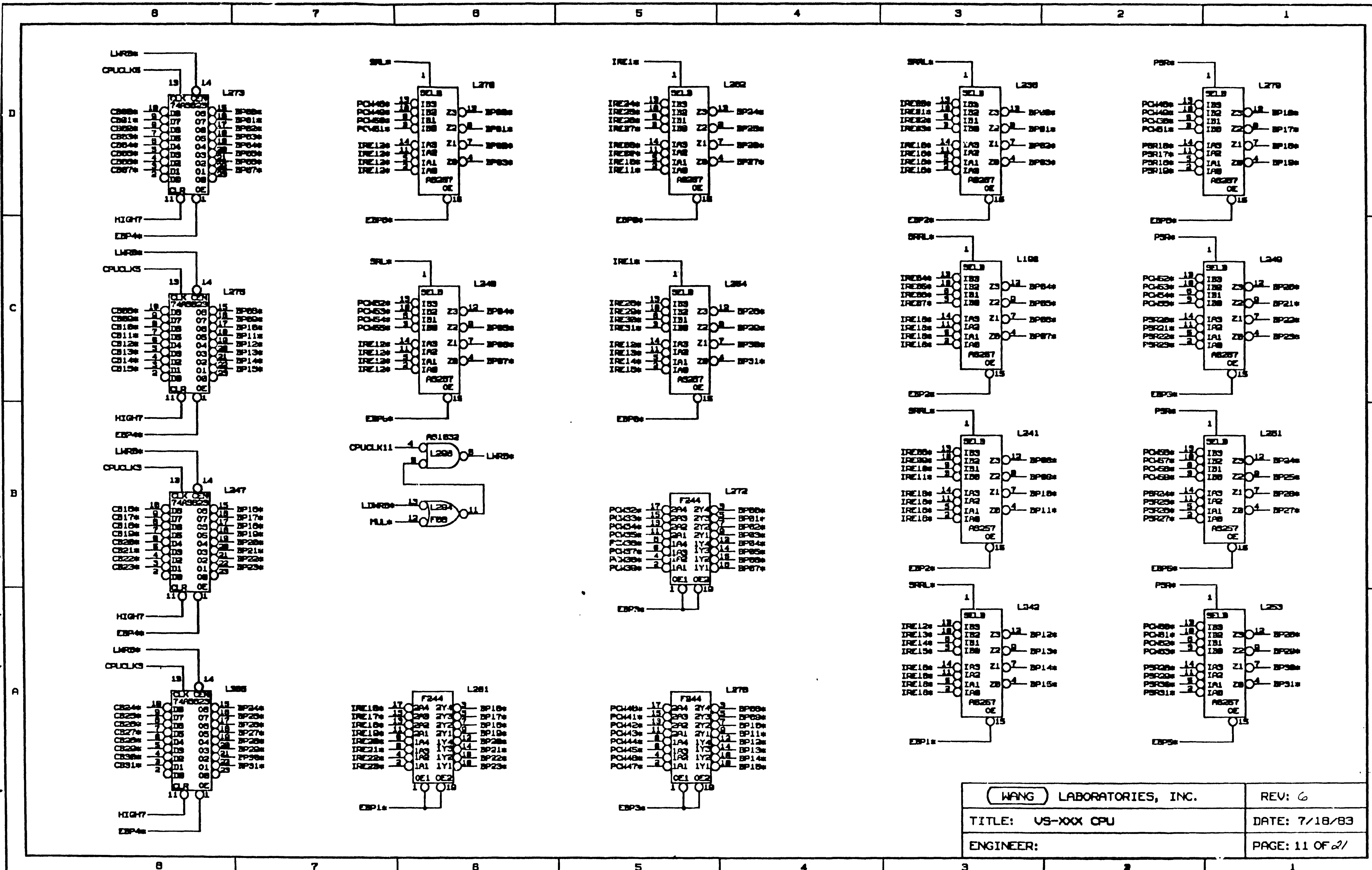
REV: 6

TITLE: VS-XXX CPU

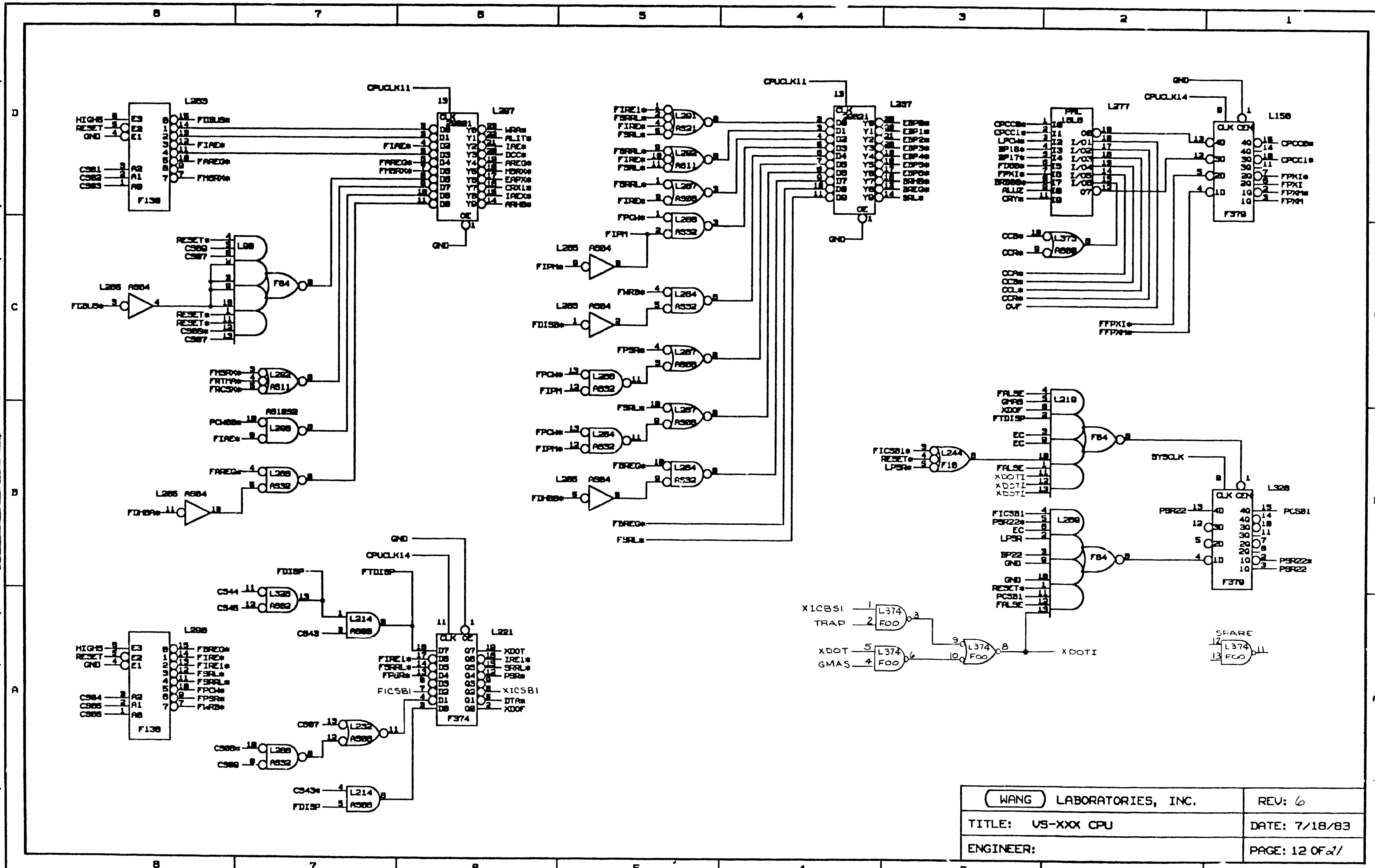
DATE: 7/18/83

ENGINEER:

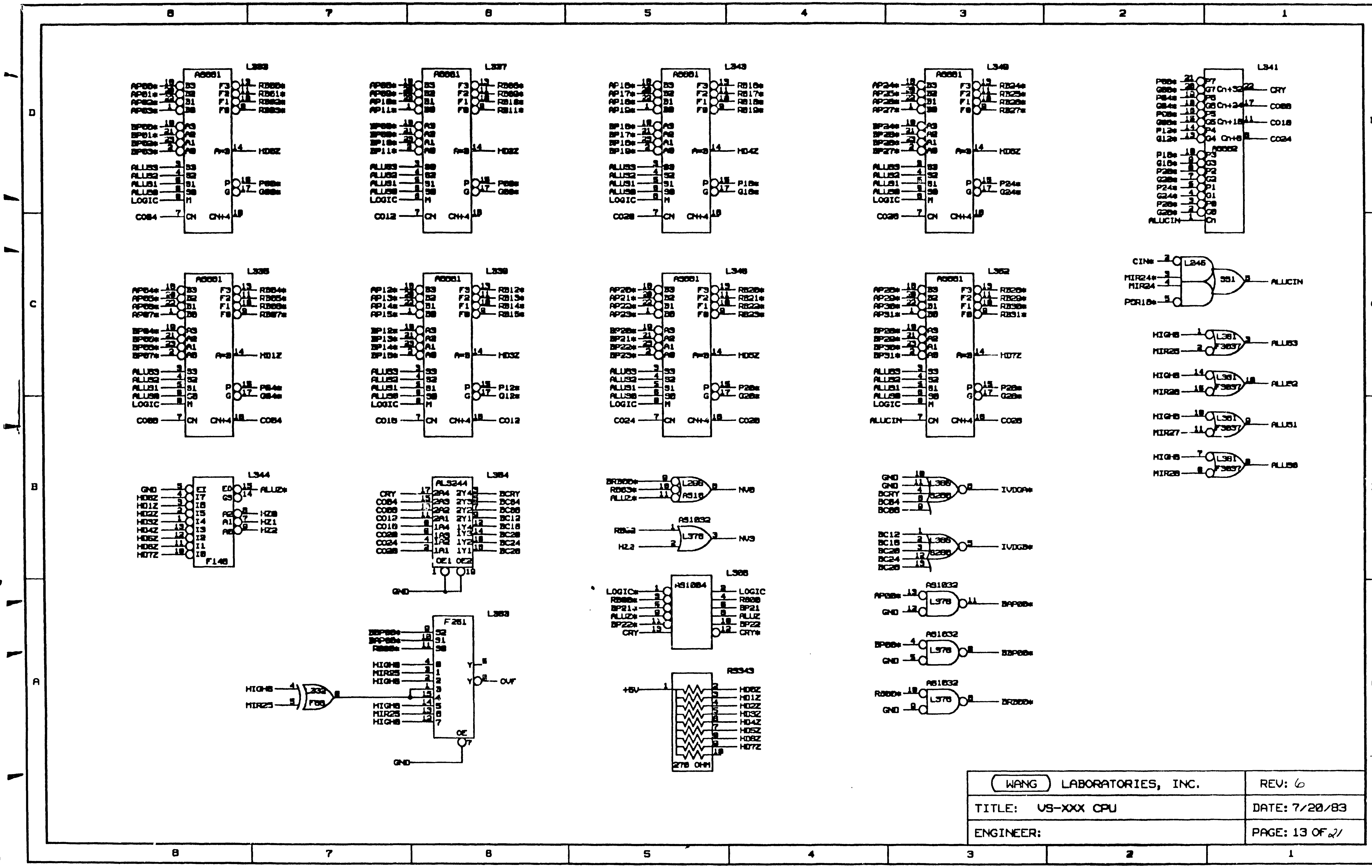
PAGE: 10 OF 21



(WANG) LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/18/83
ENGINEER:	PAGE: 11 OF 21



WANG LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/18/83
ENGINEER:	PAGE: 12 OF 21



WANG LABORATORIES, INC.

REV: 6

TITLE: VS-XXX CPU

DATE: 7/20/83

ENGINEER:

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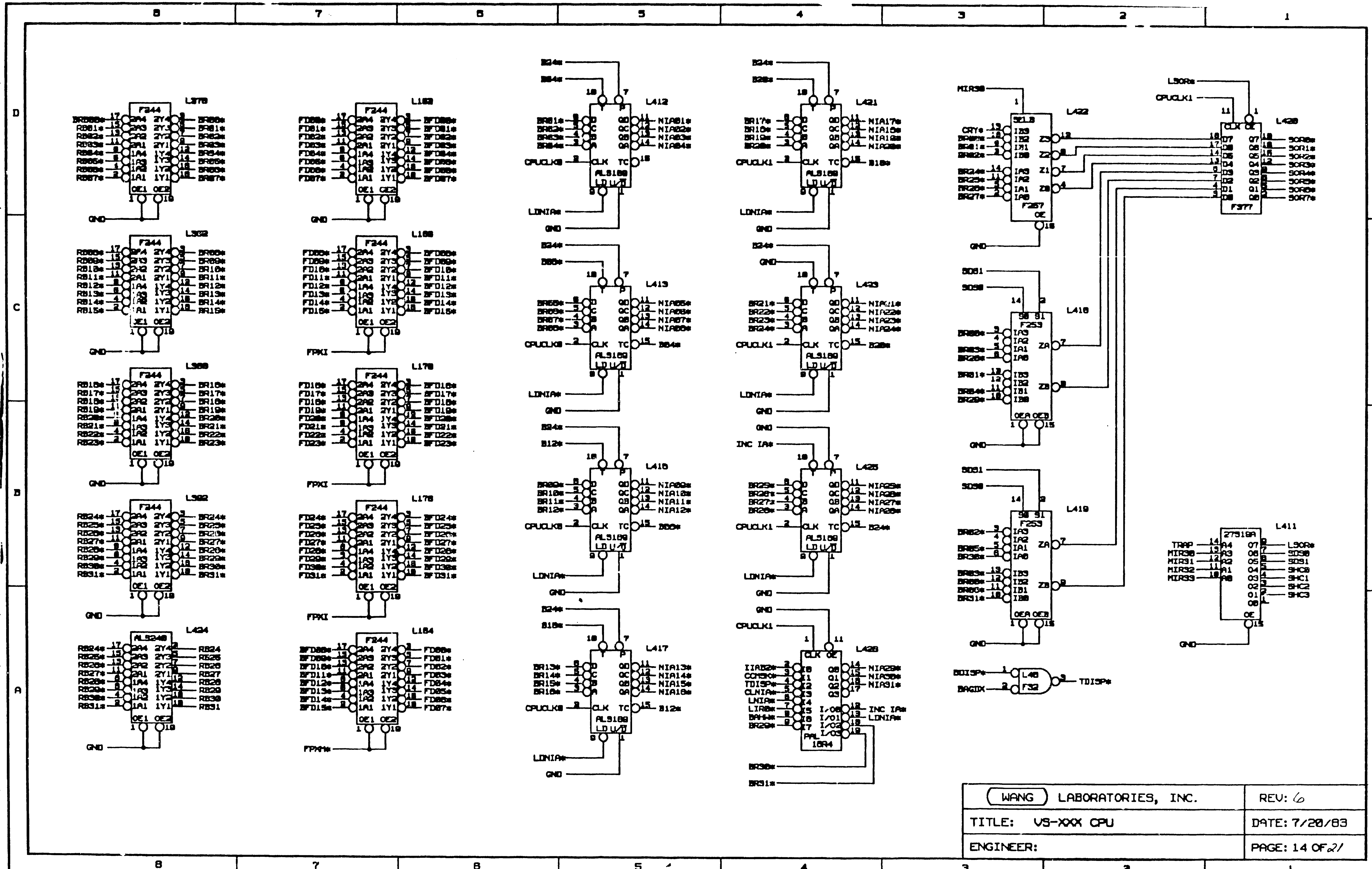
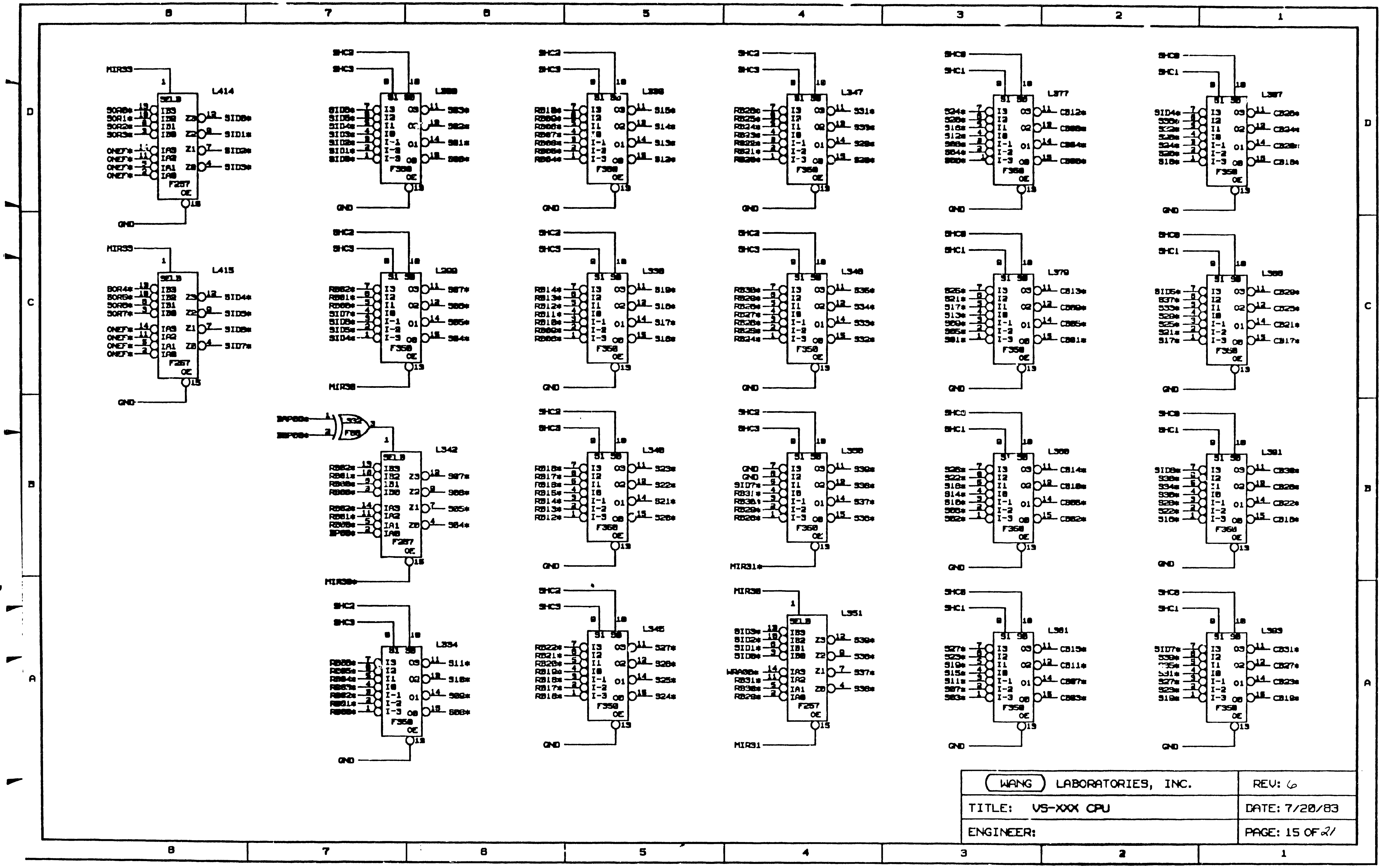
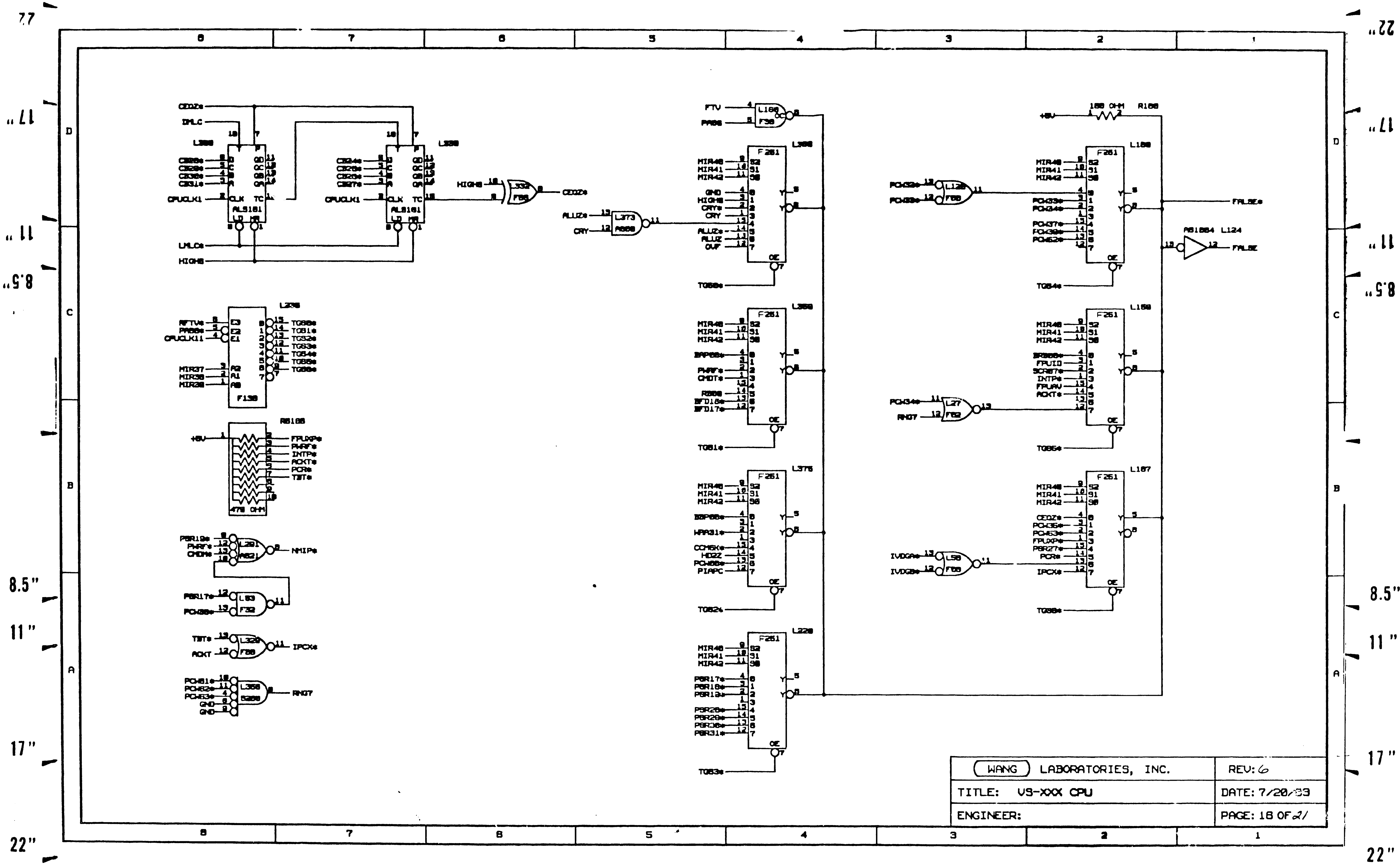
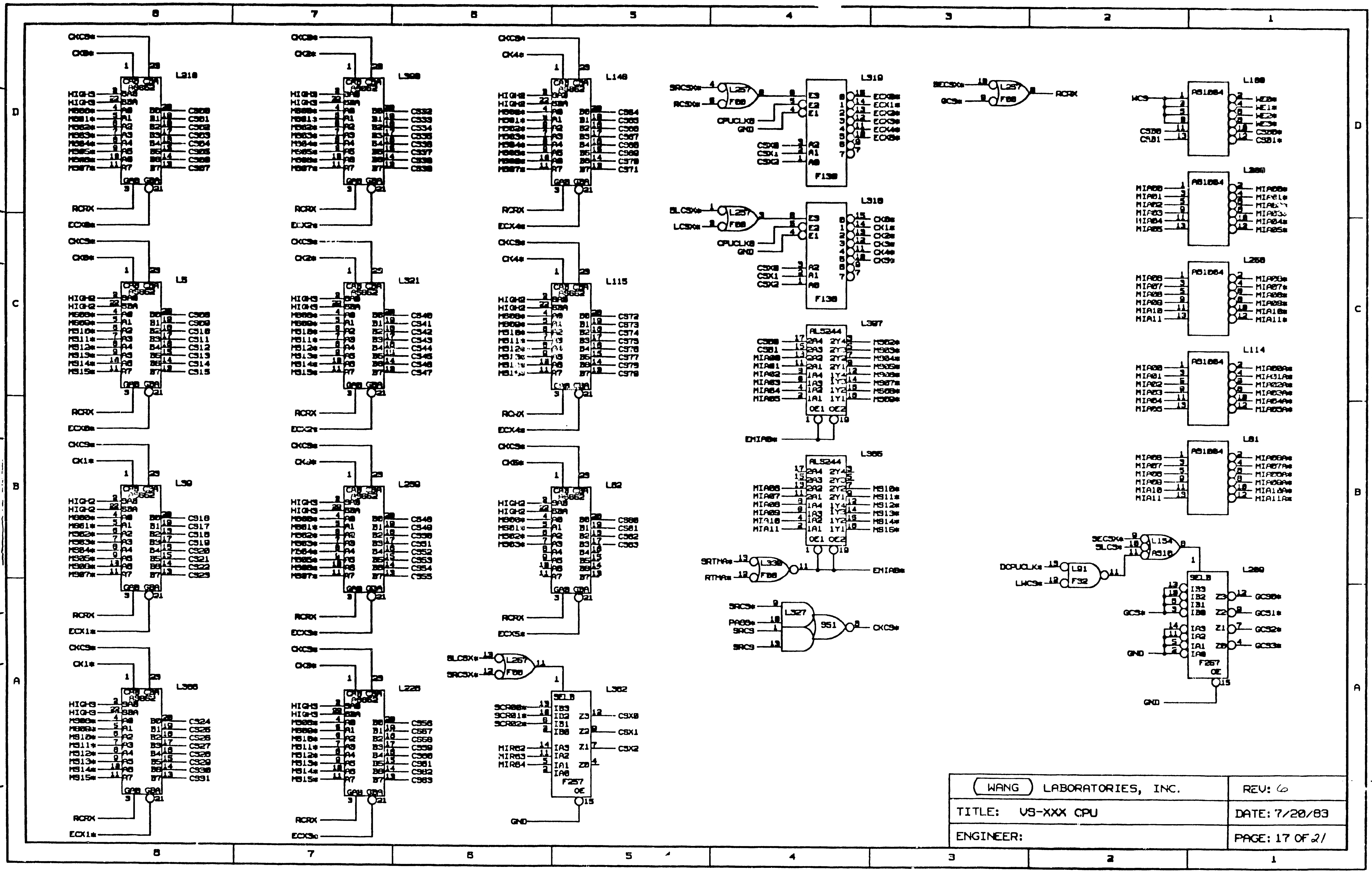


WANG LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/20/83
ENGINEER:	PAGE: 14 OF 21



WANG LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/20/83
ENGINEER:	PAGE: 15 OF 21


ALS161
F138
F261
F261
F261
F261
F261
F261
F261
TITLE: VS-XXX CPU
REV: 6
DATE: 7/20/83
ENGINEER:
PAGE: 18 OF 21
WANG LABORATORIES, INC.



WANG LABORATORIES, INC.

REV: 6

TITLE: VS-XXX CPU

DATE: 7/20/83

ENGINEER:

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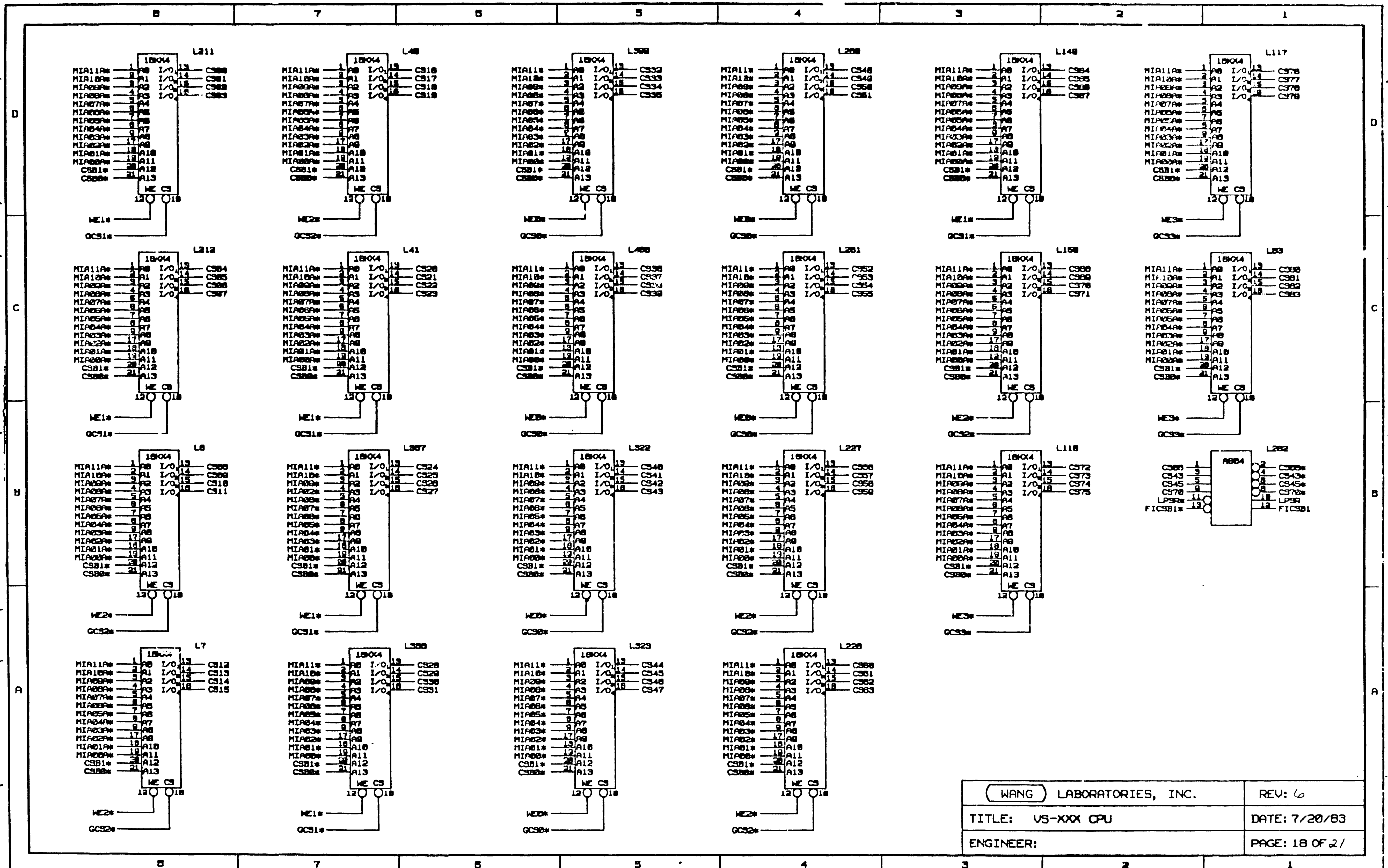
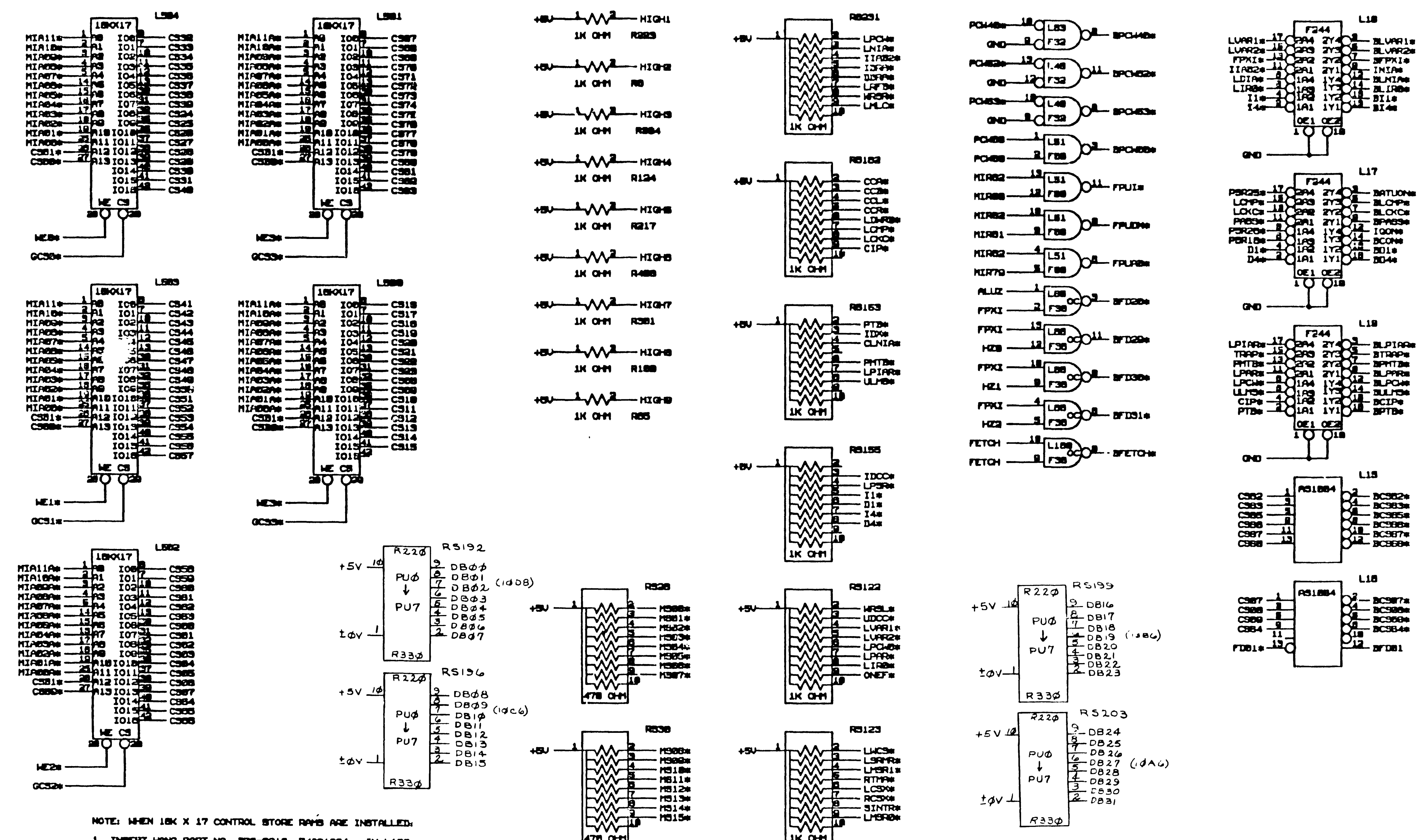


WANG LABORATORIES, INC. | REV: 6
TITLE: VS-XXX CPU | DATE: 7/20/83
ENGINEER: | PAGE: 18 OF 21

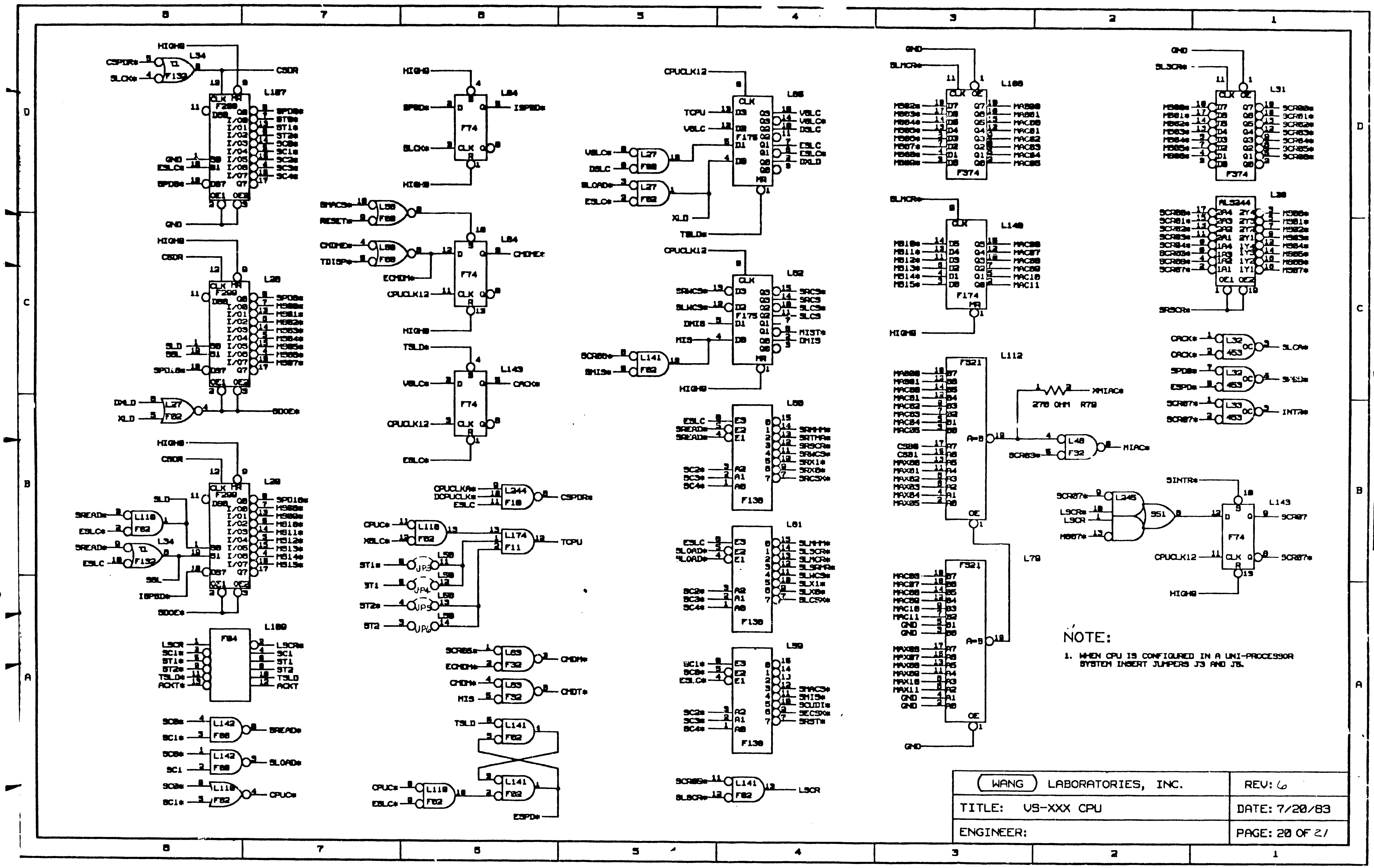


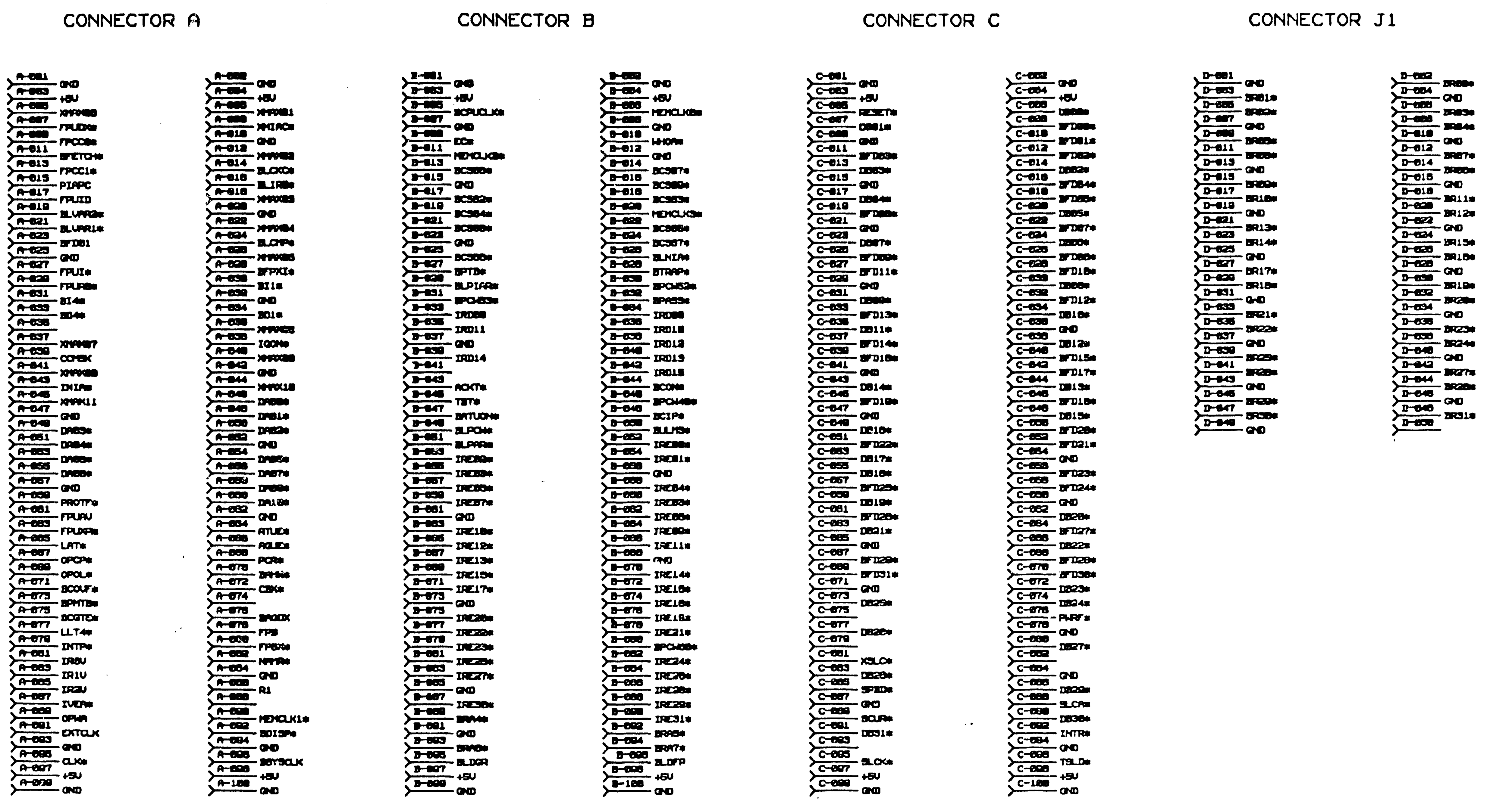
NOTE: WHEN 16K X 17 CONTROL STORE RAMS ARE INSTALLED:

1. INSERT WANG PART NO. 376-8918, 74AS1034, IN L100.

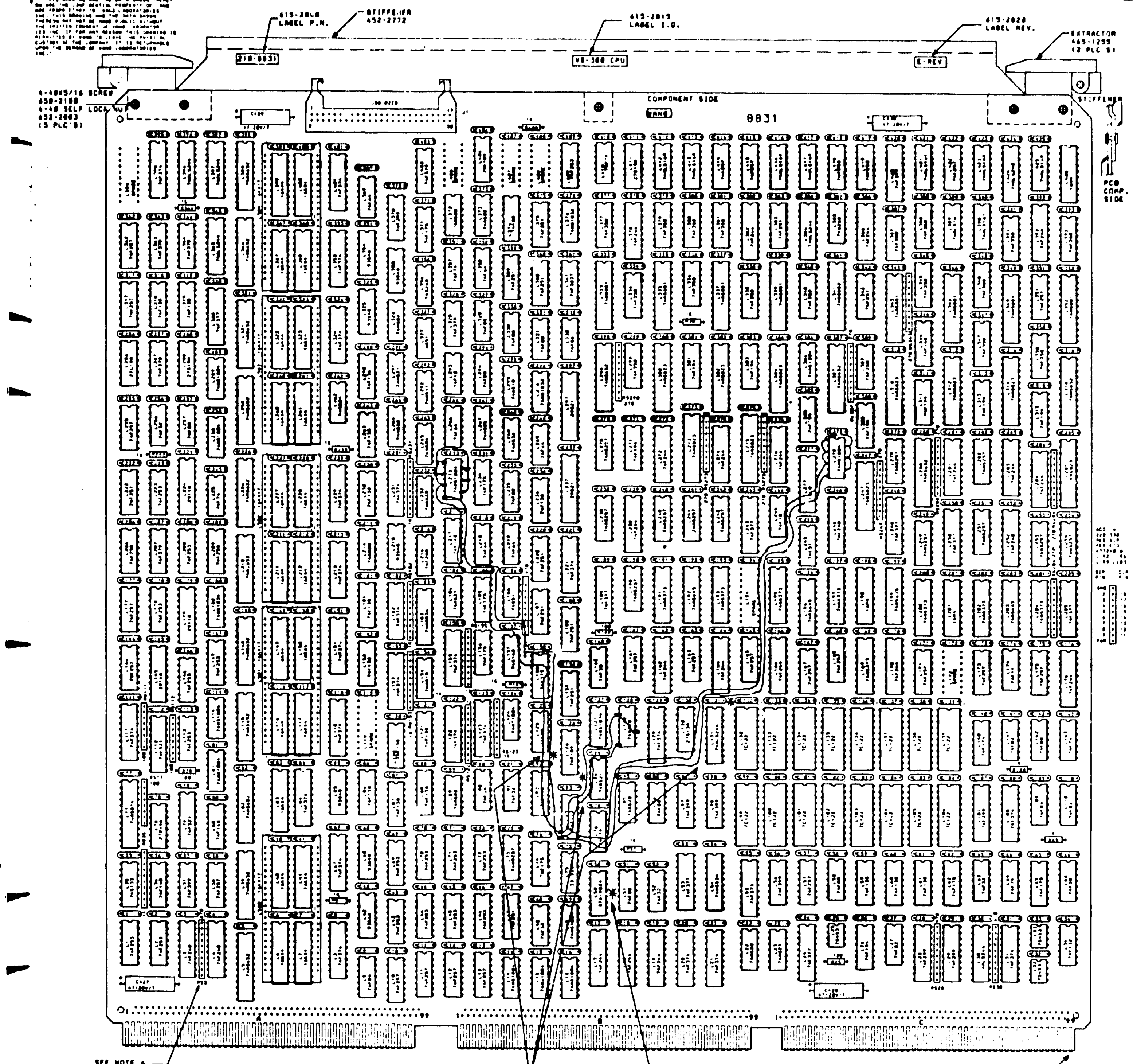
2. INSERT WANG PART NO. 376-8876, 74F258, IN L209.

WANG LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 7/20/83
ENGINEER:	PAGE: 19 OF 21


NOTE:
1. WHEN CPU IS CONFIGURED IN A UNI-PROCESSOR SYSTEM INSERT JUMPERS J3 AND J5.
WANG LABORATORIES, INC.
REV: 6
TITLE: VS-XXX CPU
DATE: 7/20/83
ENGINEER:
PAGE: 20 OF 21



(WANG) LABORATORIES, INC.	REV: 6
TITLE: VS-XXX CPU	DATE: 1/29/84
ENGINEER:	PAGE: 21 OF 21



#30 GAUGE SOLID TWISTED PAIR WIRE-
APPROX. 5 TURNS PER INCH
SHOWN AS SEPERATE WIRES
ONLY TO ILLUSTRATE CONNECTIONS!!!!

USE #28 GAUGE BUSS #(4S:600-9027)
FOR REMAINING CONNECTIONS.

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITORS ARE .047UF EXPRESSED IN MICROFARADS.
   ALL RESISTORS ARE 1/4W.5%. EXPRESSED IN OHMS.
2. INSTALL JMPR PLG ASSY(376-9129) 3 PLCS ON L50.
3. 16KX17 RAM CHIPS REPLACE 16KX4 RAM
   CHIPS AND ASSOCIATED .1 CAPACITORS.
4. PIN 1 OF ALL SIPS FACE TOWARDS THE STIFFENER.
5. REFERENCE SCHEMATIC LOADING CHART OR PARTS
   LIST FOR JUMPER CONFIGURATION.

WANG LABORATORIES INC. LOWELL MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN DCT		E ENGR	
		CHK		M ENGR	
		E C CONTROL		MFG ENGR	
MATERIAL	MODEL NO. VS-300	TITLE VS300 CPU			
	SEE ENGRG SPECIFICATIONS NO. 10-214				
FINISH		210-8831	C	8831	6
	SCALE 1/1 · SHT 1 OF 1		SIZE	DRAWING NUMBER	REV

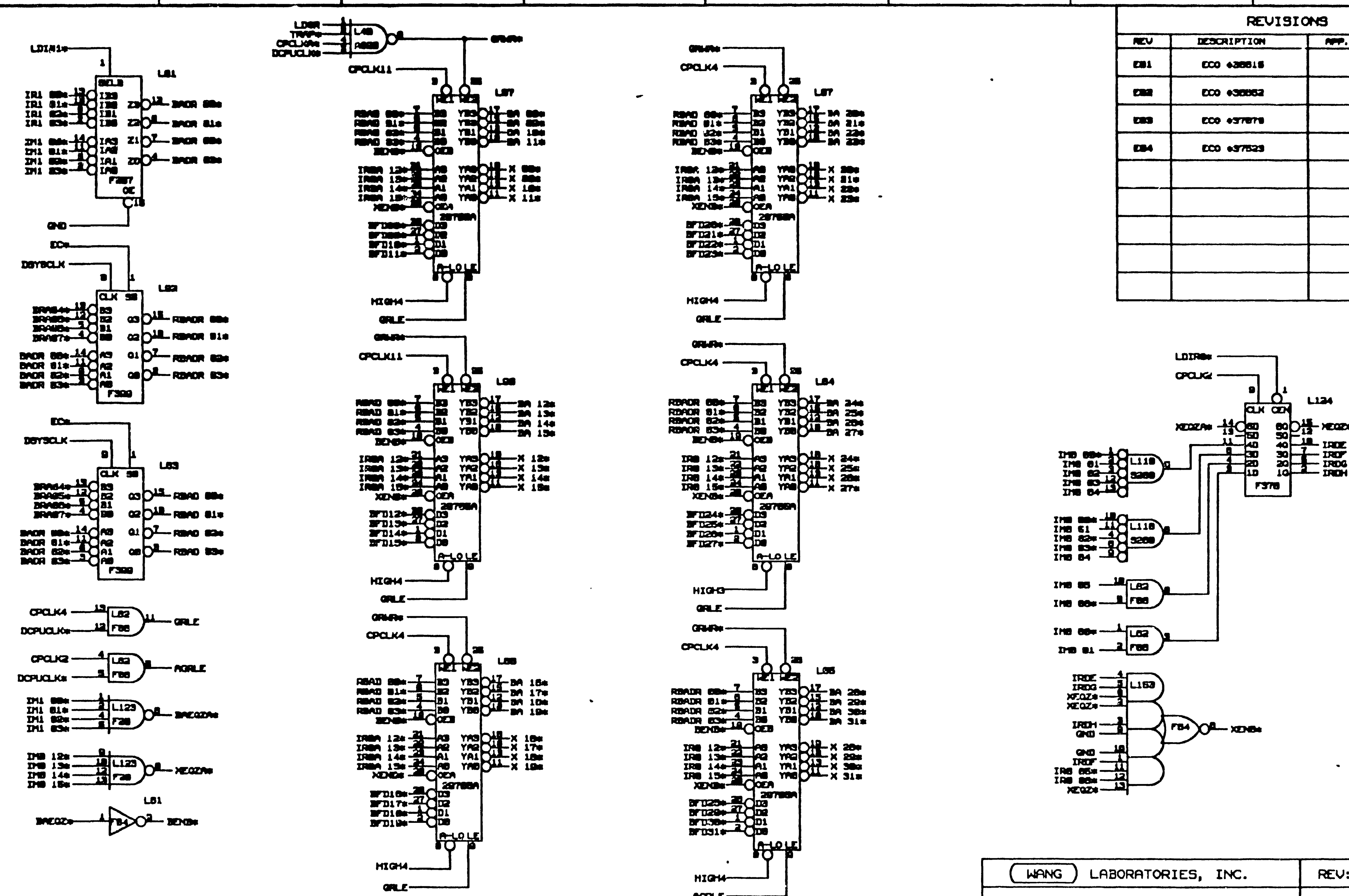
#8832 R 02 E-REV #04

ADDRESS GENERATION UNIT (AGU) INDEX

1. AGU REGISTER FILE
2. EA(08:31) CALCULATION
3. IR0, IR1 IQ INPUT MUX
4. IR2 IQ INPUT MUX
5. IQ REGISTERS, IRE
6. VAR1, VAR2
7. VA MUX
8. VAR, FP LONG EA, SS NWAY
9. IQ CONTROL, INSTRUCTION DECODING
10. ESU REGISTER FILE ADDRESSING
11. ESU REGISTER FILE, EALU
12. ESU CONTROL STORE, MIR
13. DISPATCH ADDRESS LOGIC
14. EA(01:07) CALCULATION
15. PULL-UP RESISTORS
16. AGU CLOCKS, INVERTERS, BUFFERS
17. BVA, DB, BUFFERS
18. REAL-TIME CLOCK
19. BACKPLANE AND CONNECTORS

DRAWING LAST_MODIFIED=Mon Aug 26 09:03:14 1985

WANG LABORATORIES, INC.	REV: 8832R02E04
TITLE: VS-300 AGU SCHEMATICS	DATE: 08/15/85
ENGINEER: W. S. ZUK X76272	PAGE: 0 OF 19

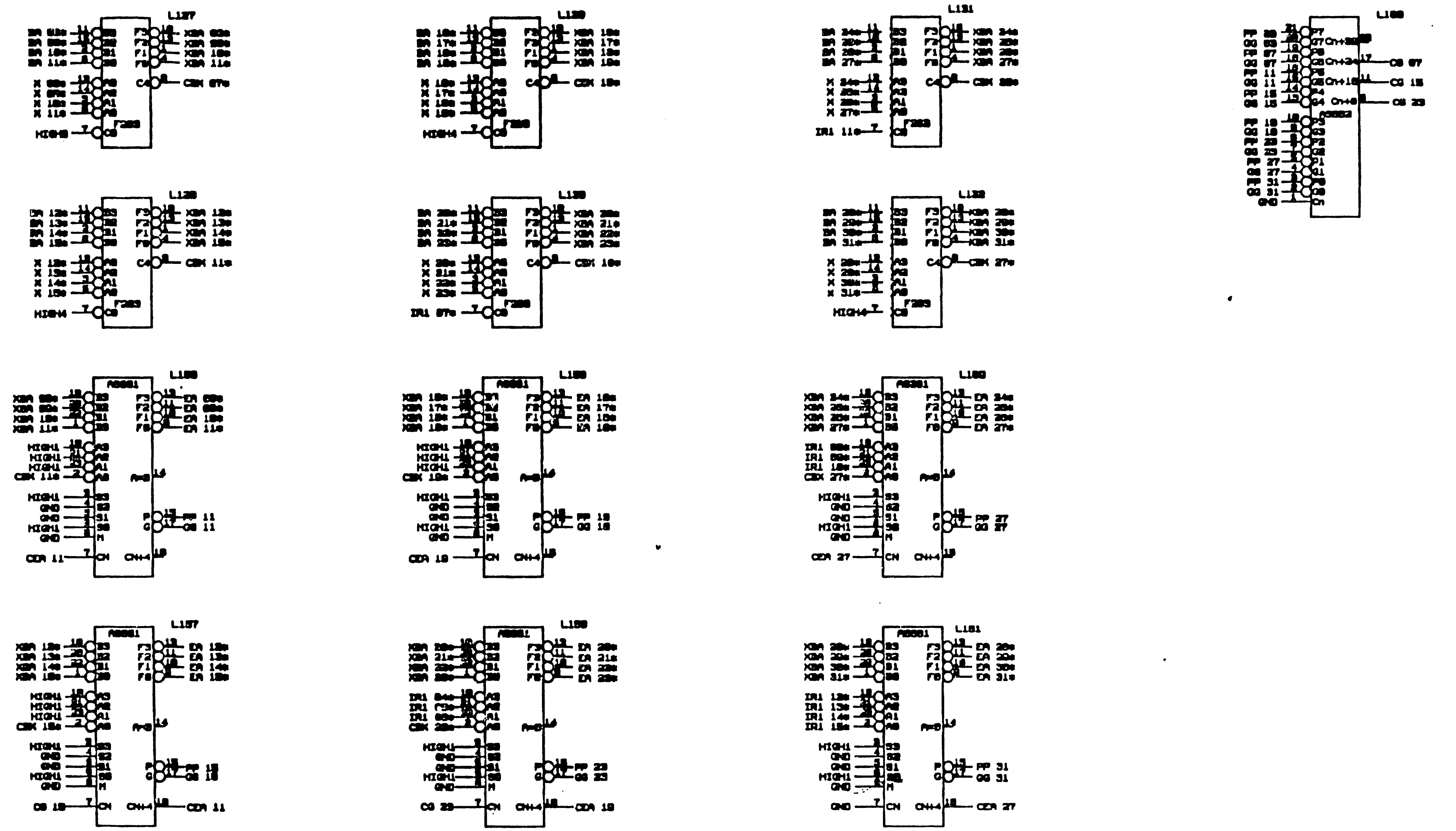


REVISIONS

REV	DESCRIPTION	APP. BY	DATE
E01	ECO #36615		04/30/85
E02	ECO #36662		05/02/85
E03	ECO #37878		05/21/85
E04	ECO #37523		06/14/85

DRAWING LAST_MODIFIED=Mon Aug 26 09:24:37 1985

WANG LABORATORIES, INC.	REV: 0832R02E04
TITLE: VS-300 AGU SCHEMATICS	DATE: 05/23/85
ENGINEER:	PAGE: 1 OF 19



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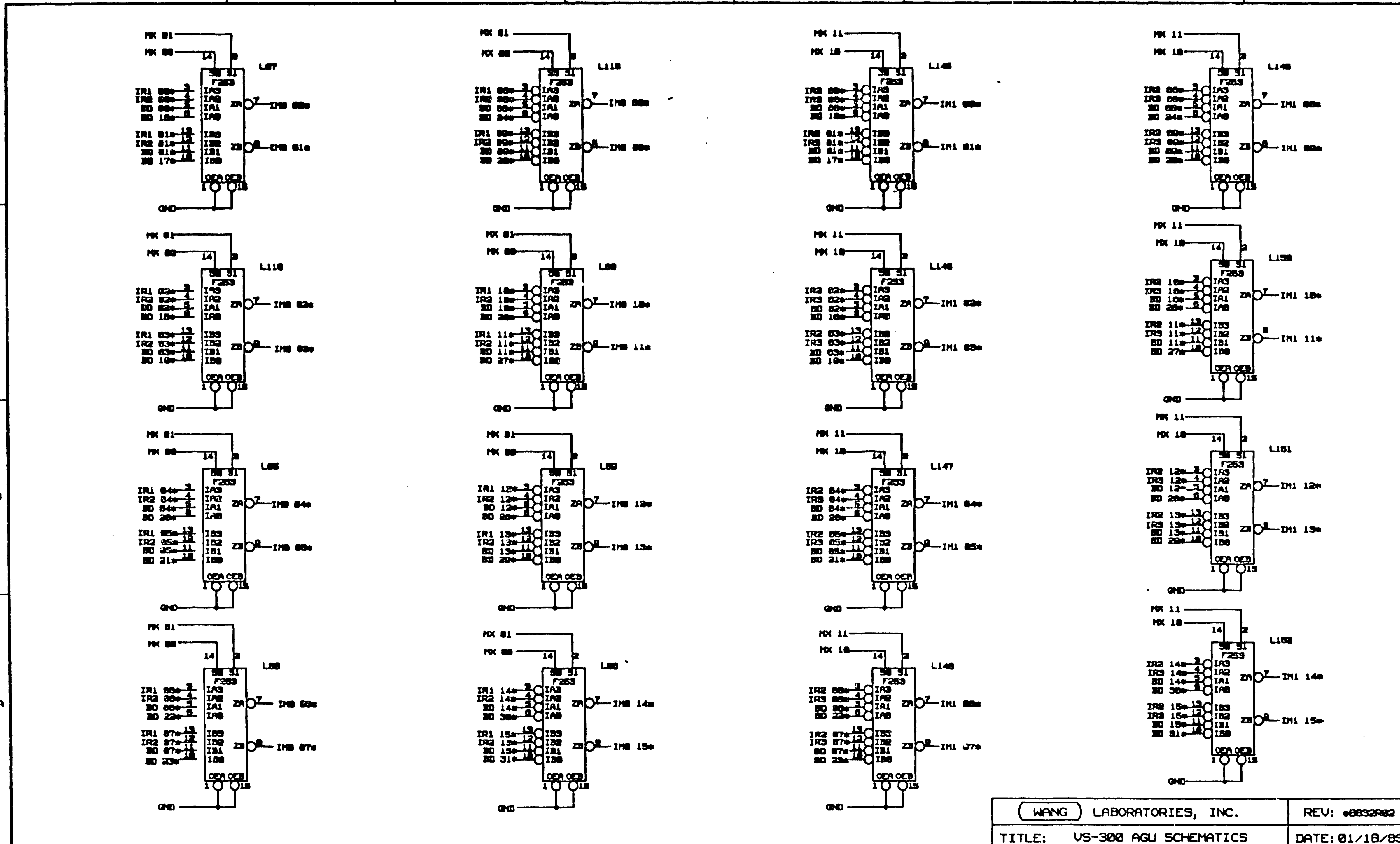
TITLE: VS-300 AGU SCHEMATICS	DATE: 03/06/85
ENGINEER:	PAGE: 2 OF 19



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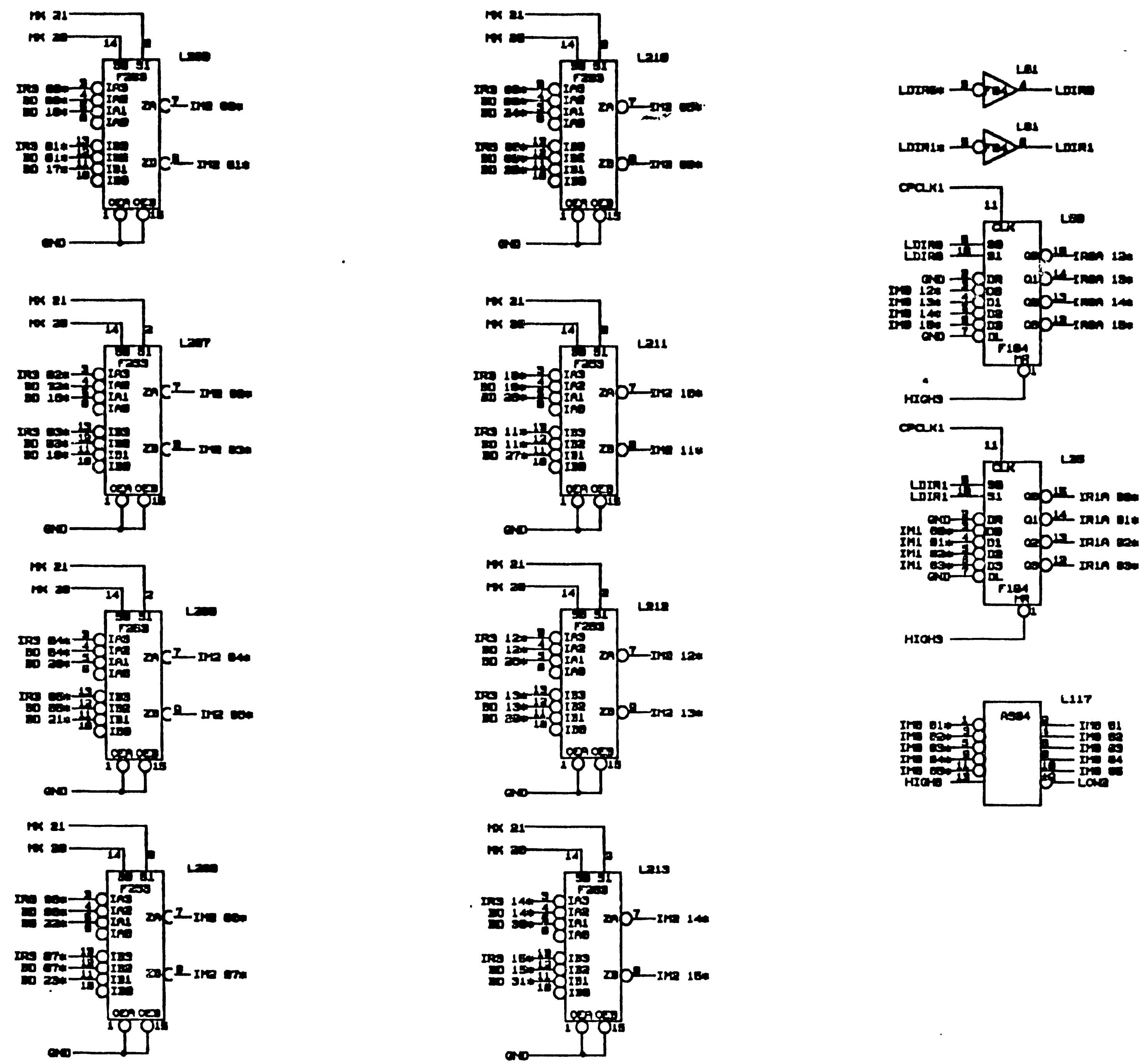
WANG LABORATORIES, INC.	REV: e0892R02
TITLE: VS-300 AGU SCHEMATICS	DATE: 01/18/85
ENGINEER:	PAGE: 3 OF 19



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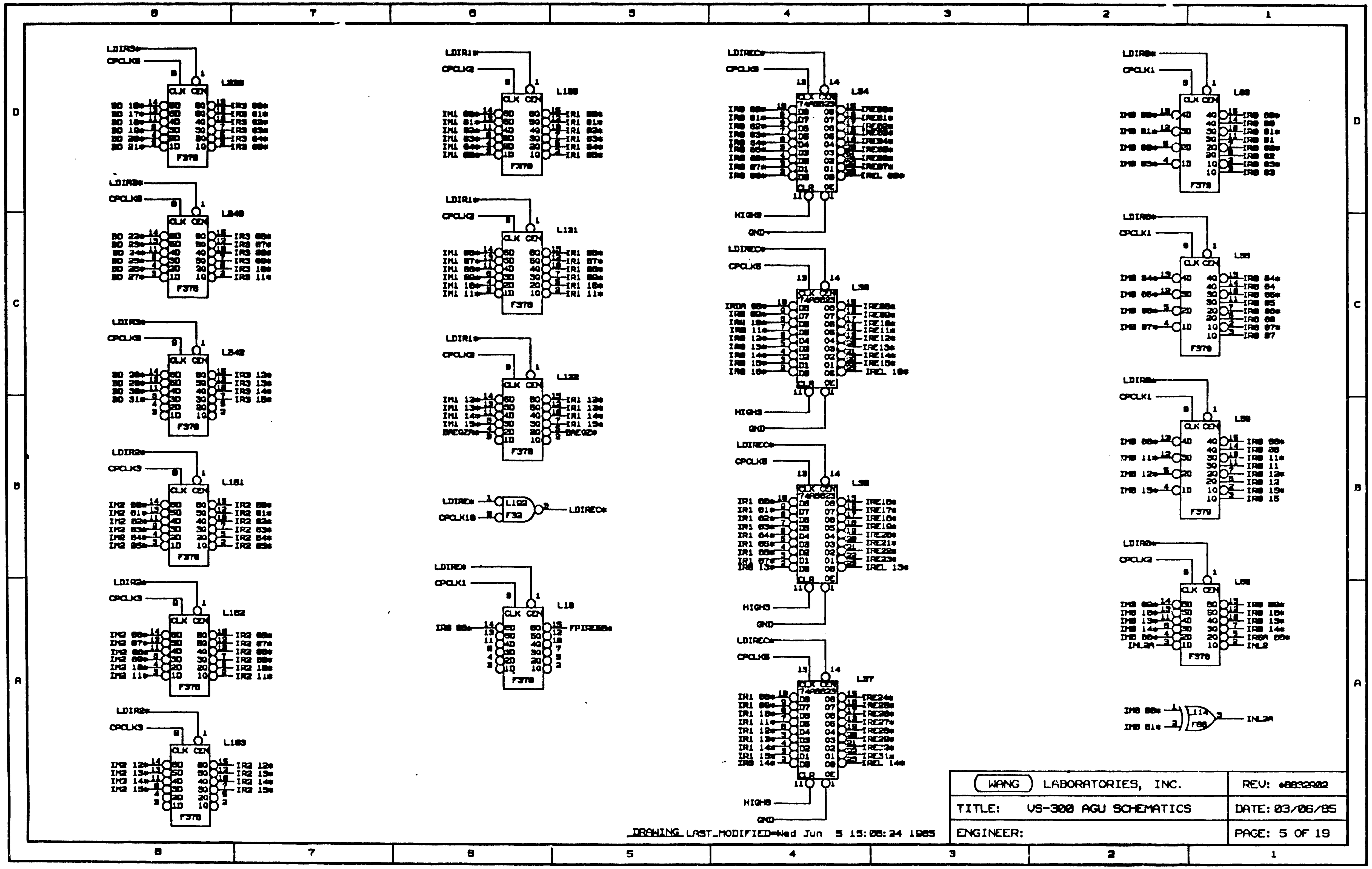
(WANG) LABORATORIES, INC.	REV: #8832R02
TITLE: VS-300 AGU SCHEMATICS	DATE: 01/18/85
ENGINEER:	PAGE: 4 OF 19



WANG LABORATORIES, INC.
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DATE: 03/06/85
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PAGE: 5 OF 19
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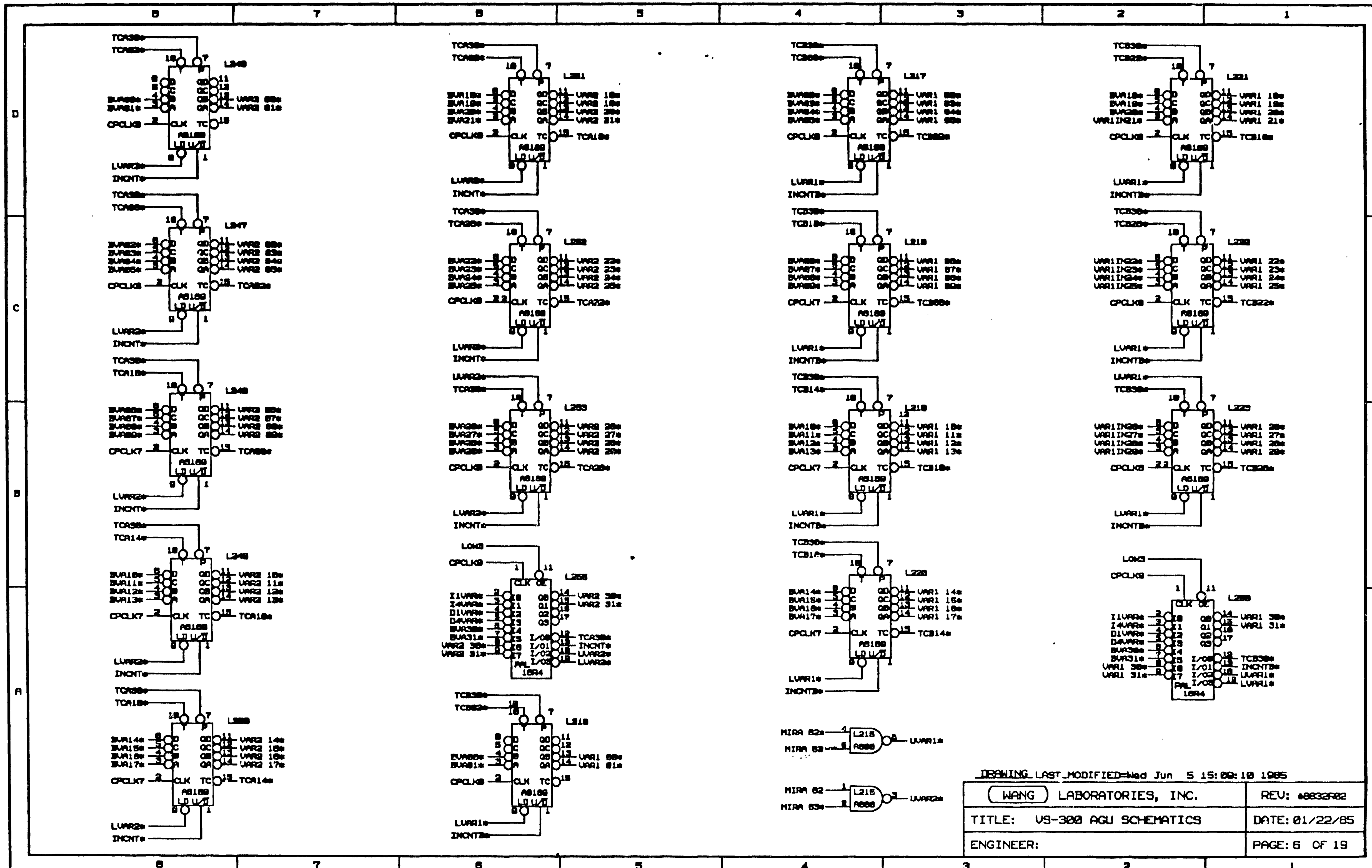
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DATE: 01/22/85
ENGINEER:
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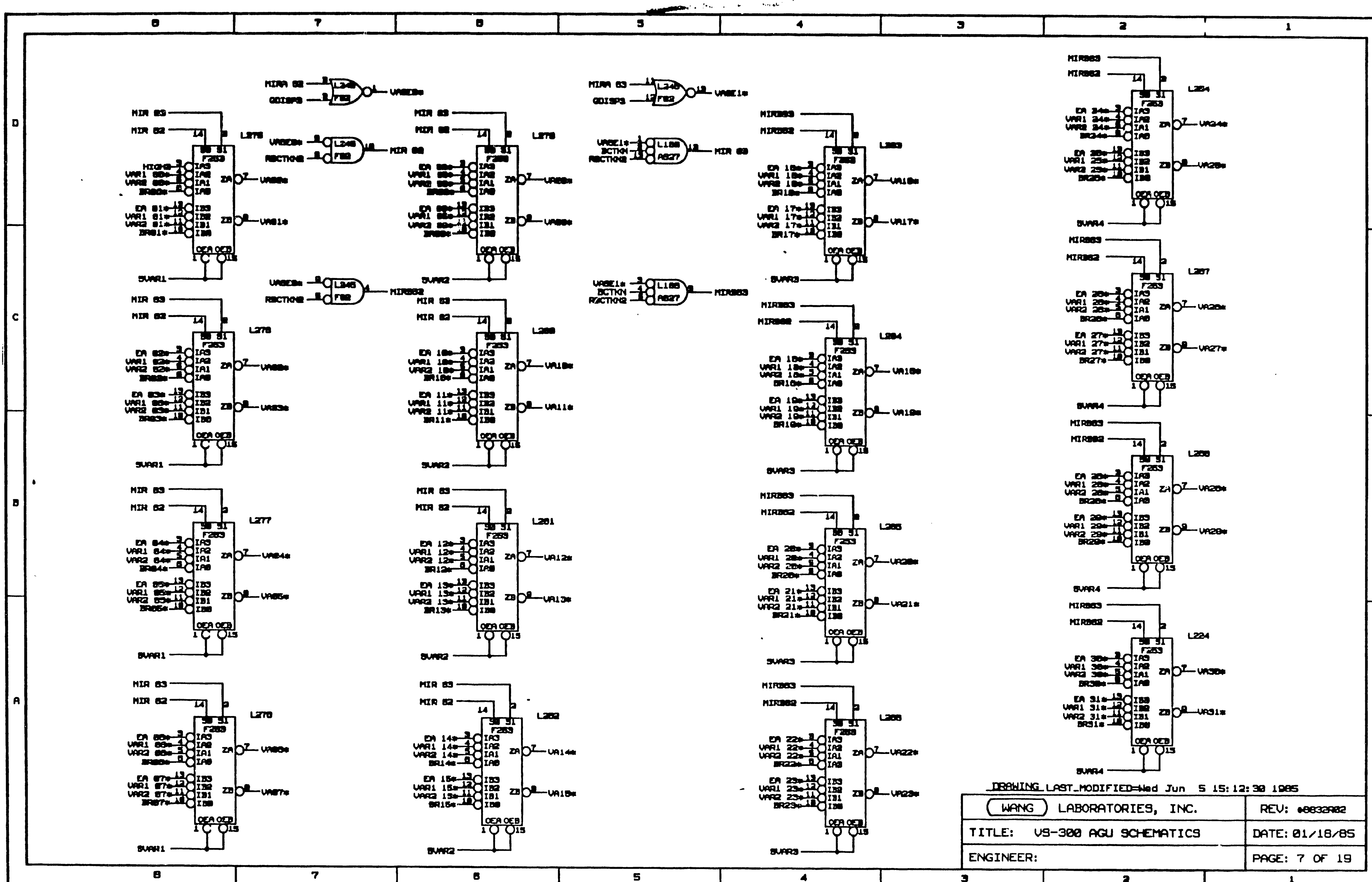

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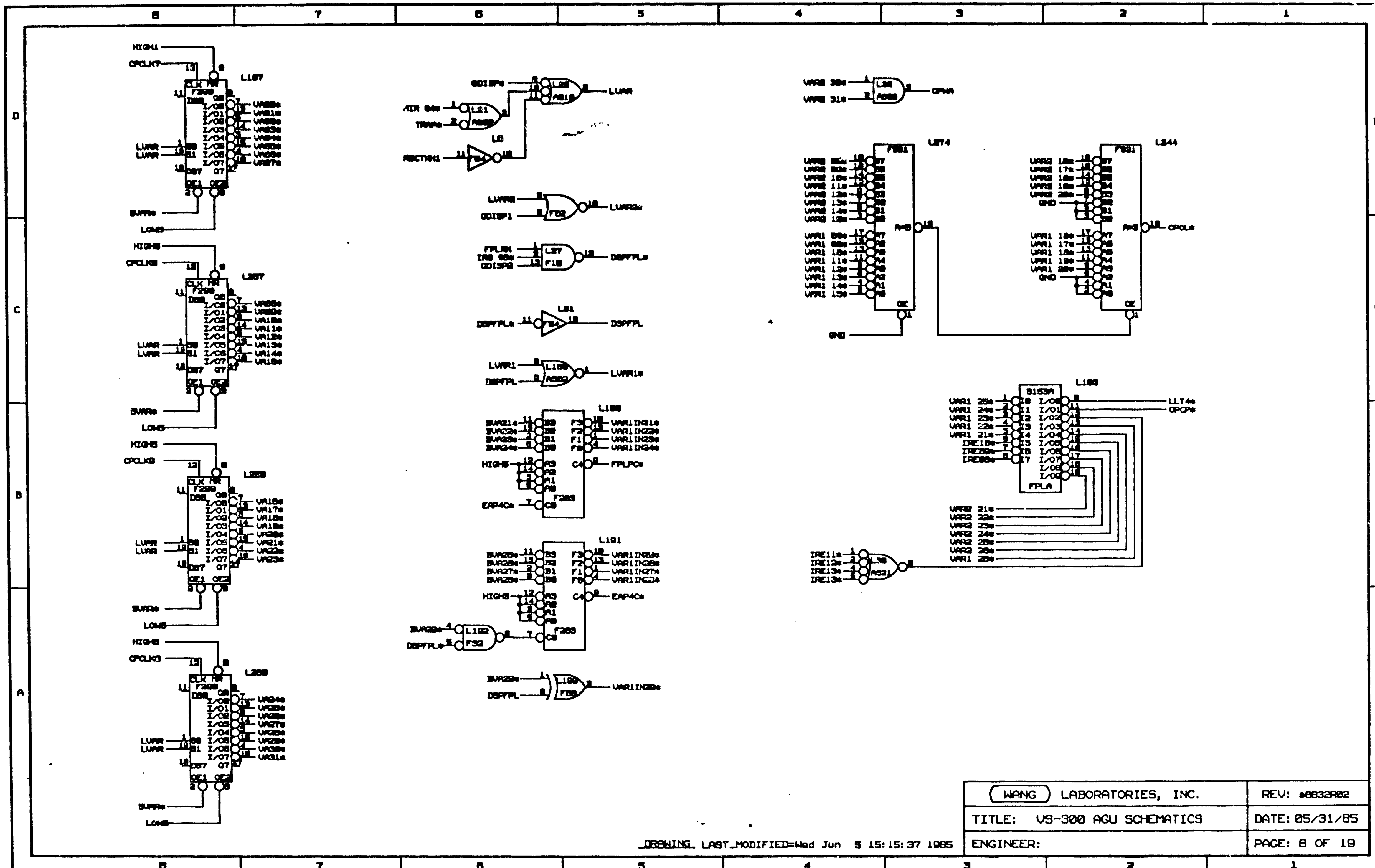
TITLE: VS-300 AGU SCHEMATICS	DATE: 01/18/85
ENGINEER:	PAGE: 7 OF 19



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WANG LABORATORIES, INC.

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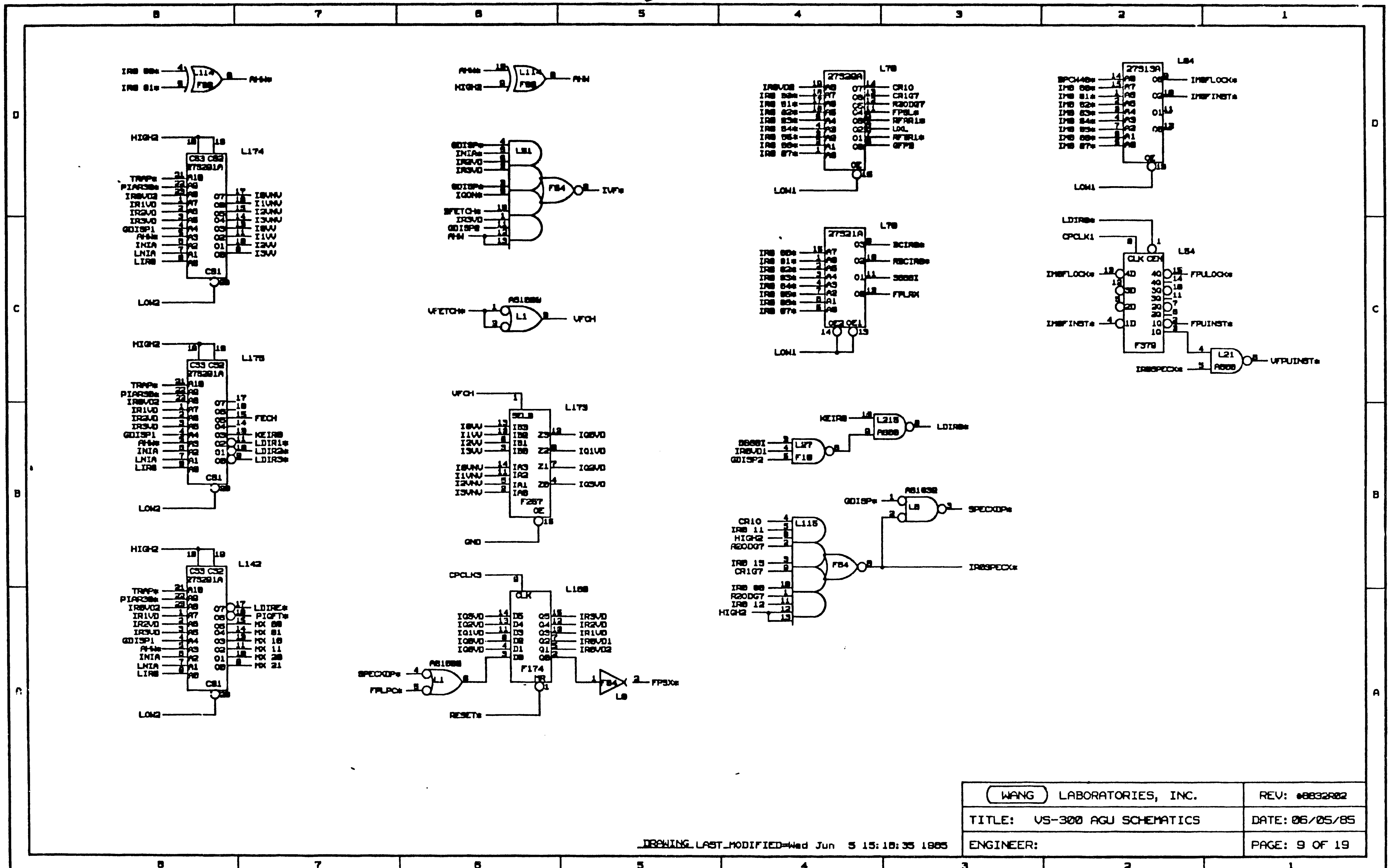
TITLE: VS-300 AGU SCHEMATICS

DATE: 05/31/85

ENGINEER:

PAGE: 8 OF 19



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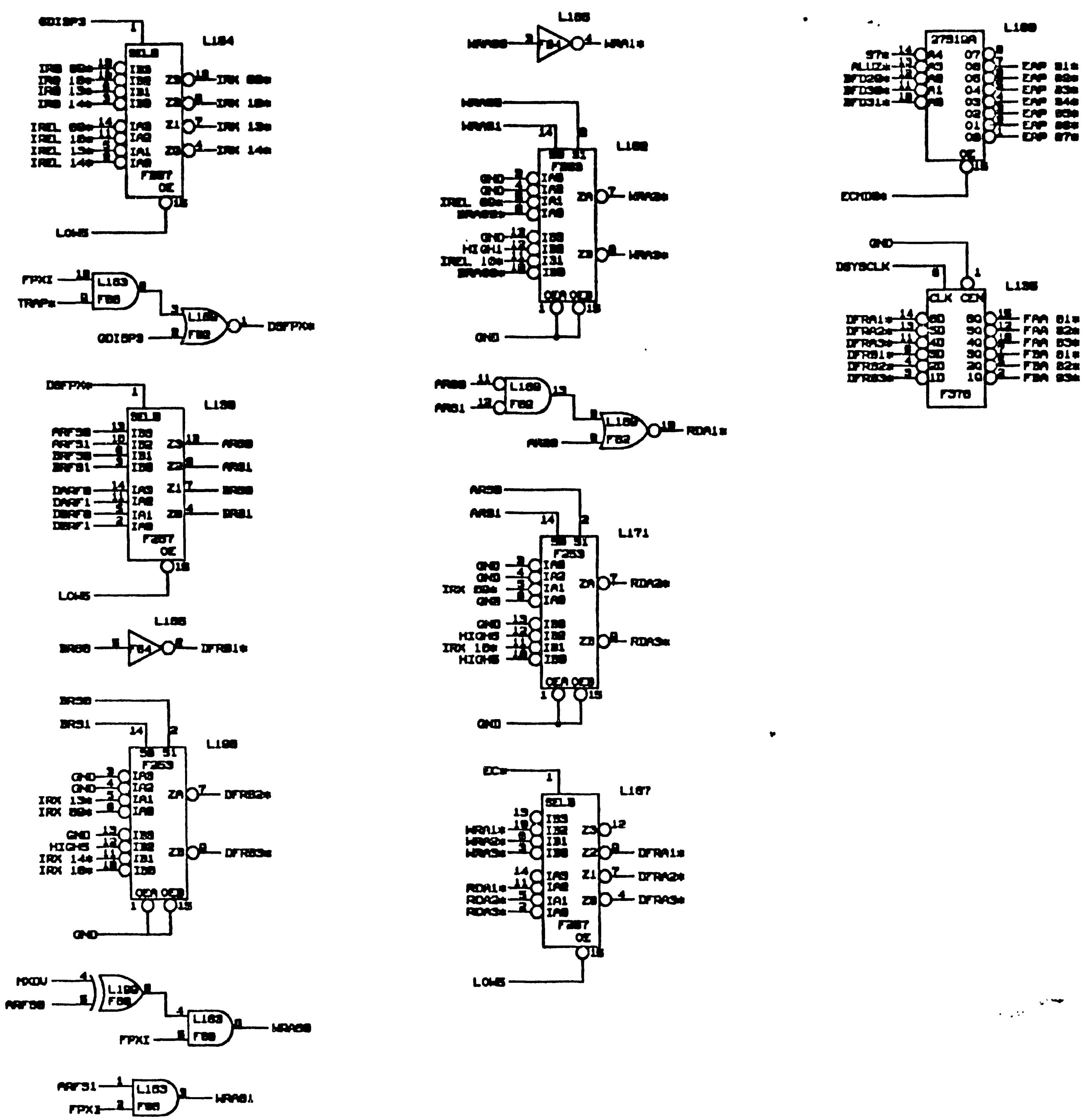
ENGINEER:	PAGE: 9 OF 19



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TITLE: VS-300 AGU SCHEMATICS	DATE: 08/15/85
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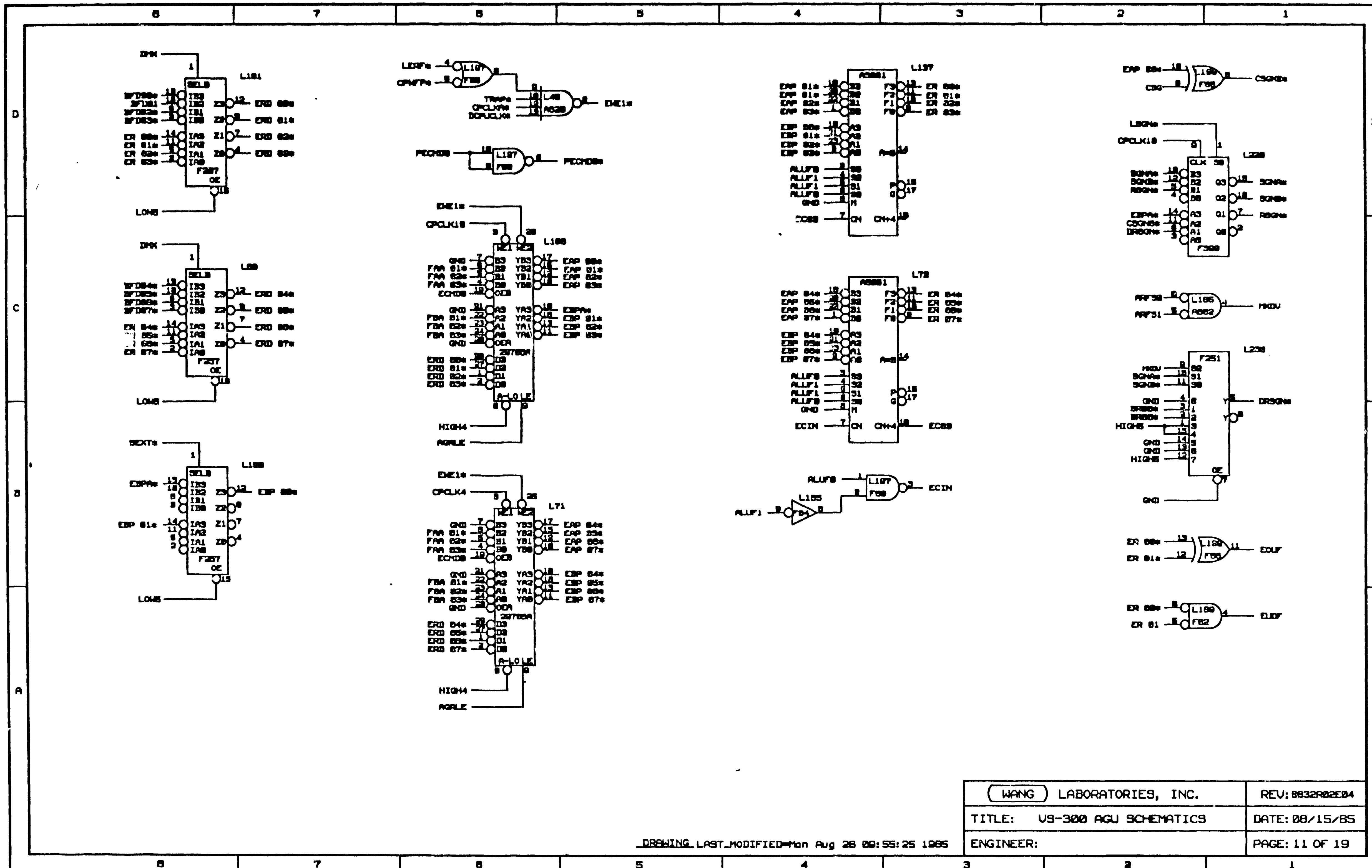

WANG LABORATORIES, INC.

REV: 8832R02E04

TITLE: VS-300 AGU SCHEMATICS

DATE: 08/15/85

ENGINEER:

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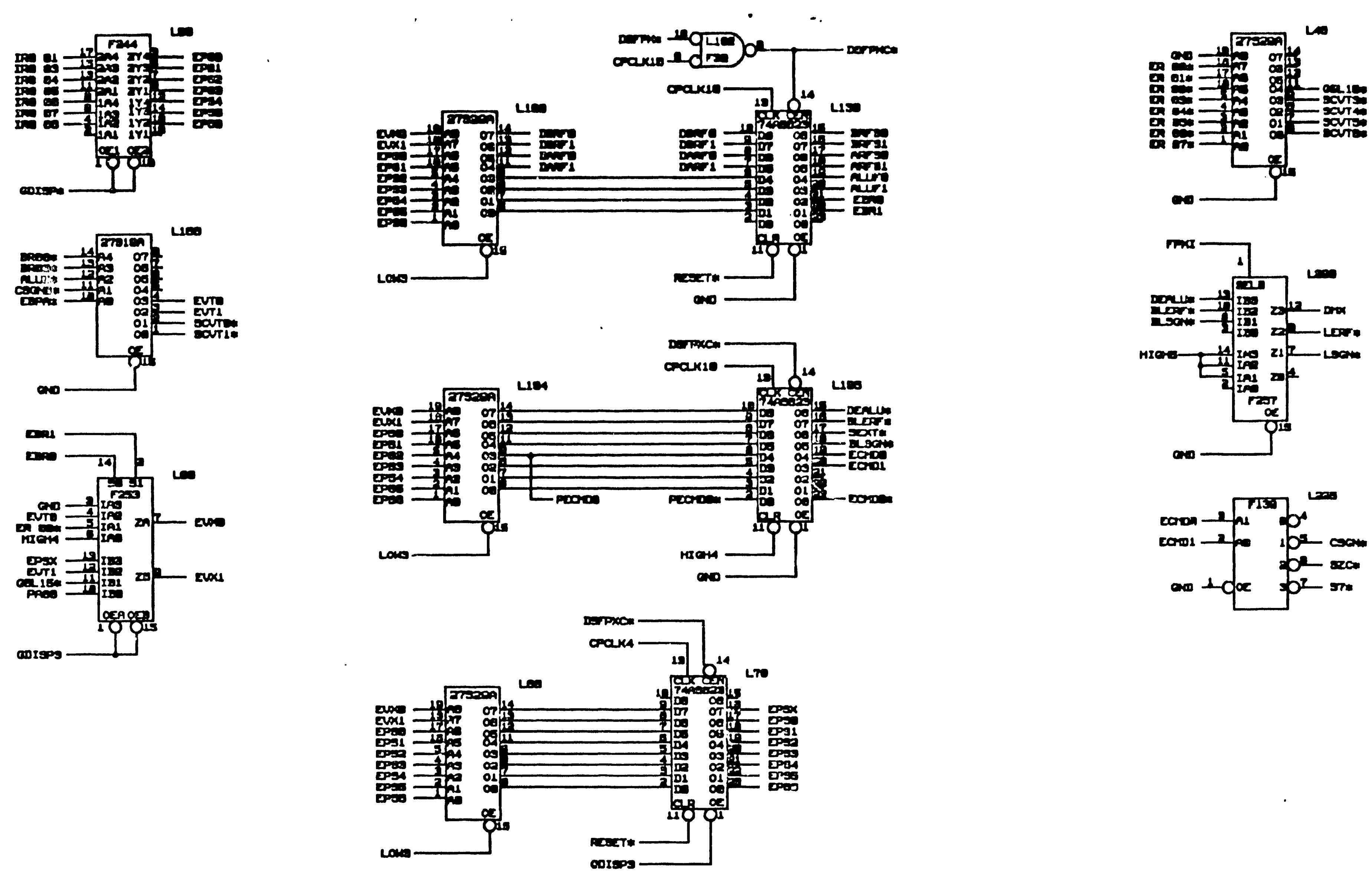

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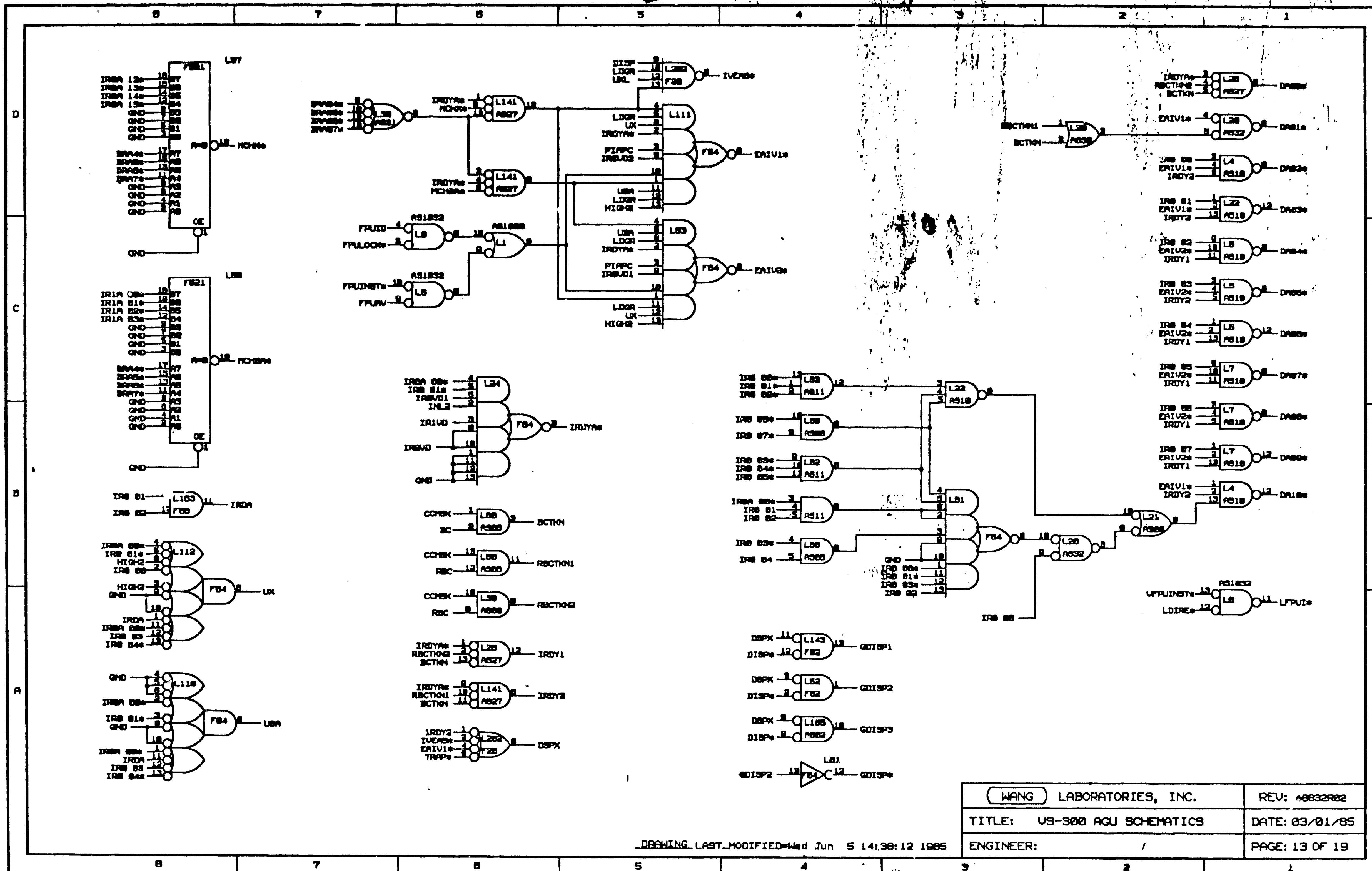

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TITLE: VS-300 AGU SCHEMATICS

DATE: 03/01/85

ENGINEER: /

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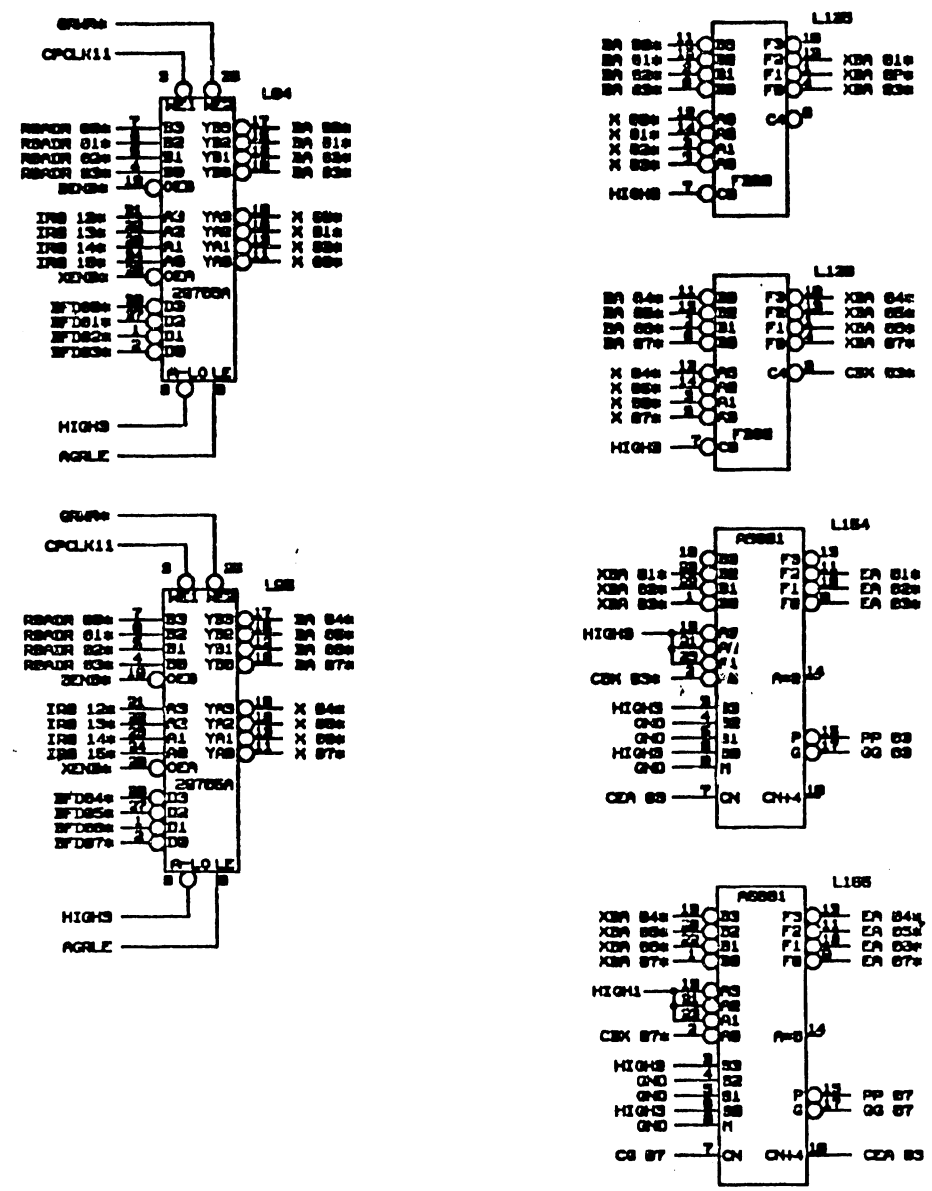

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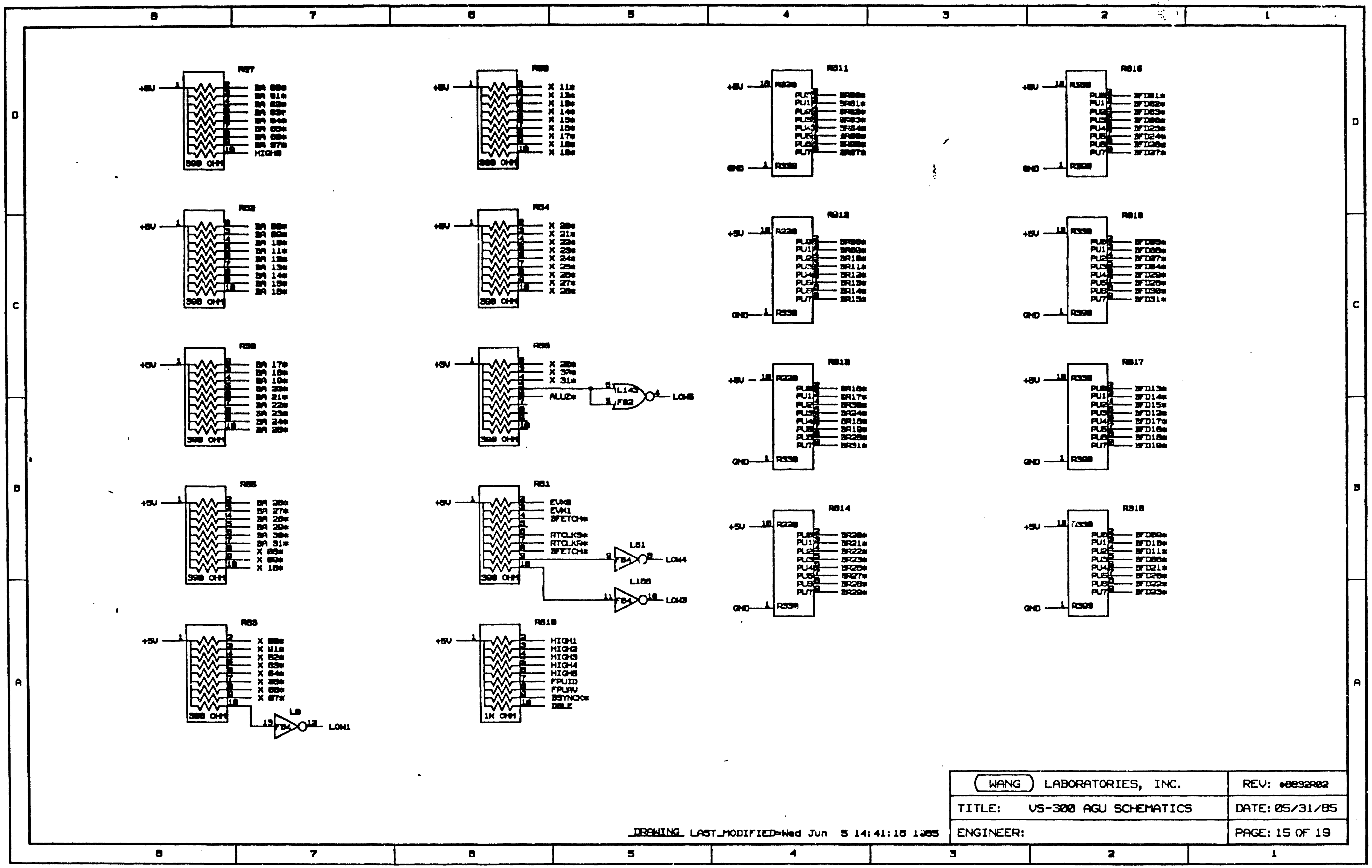
TITLE: VS-300 AGU SCHEMATICS	DATE: 11/21/83
ENGINEER:	PAGE: 14 OF 19



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TITLE: VS-300 AGU SCHEMATICS | DATE: 05/31/85

ENGINEER: | PAGE: 15 OF 19

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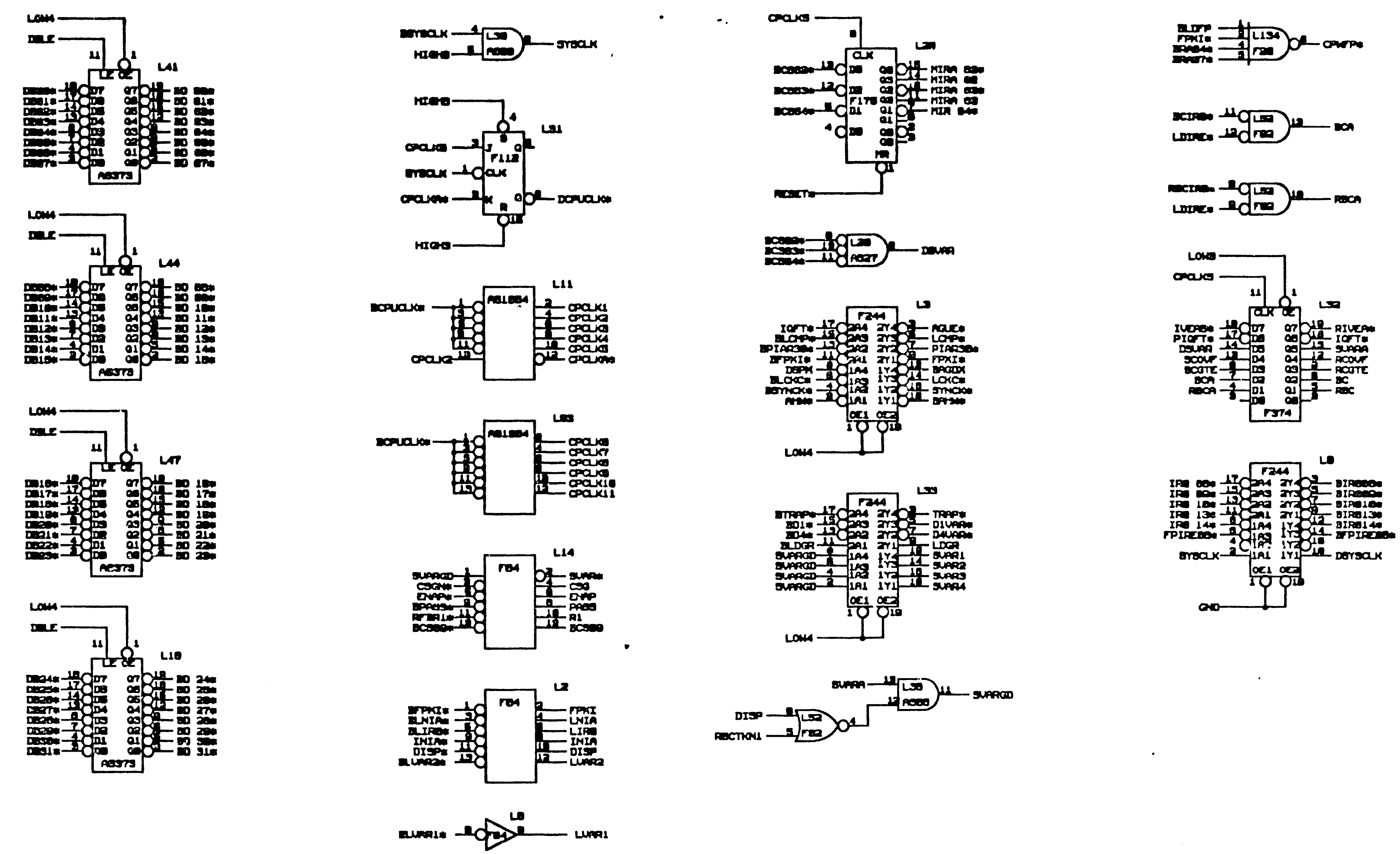

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TITLE: VS-300 AGU SCHEMATICS	DATE: 05/31/85
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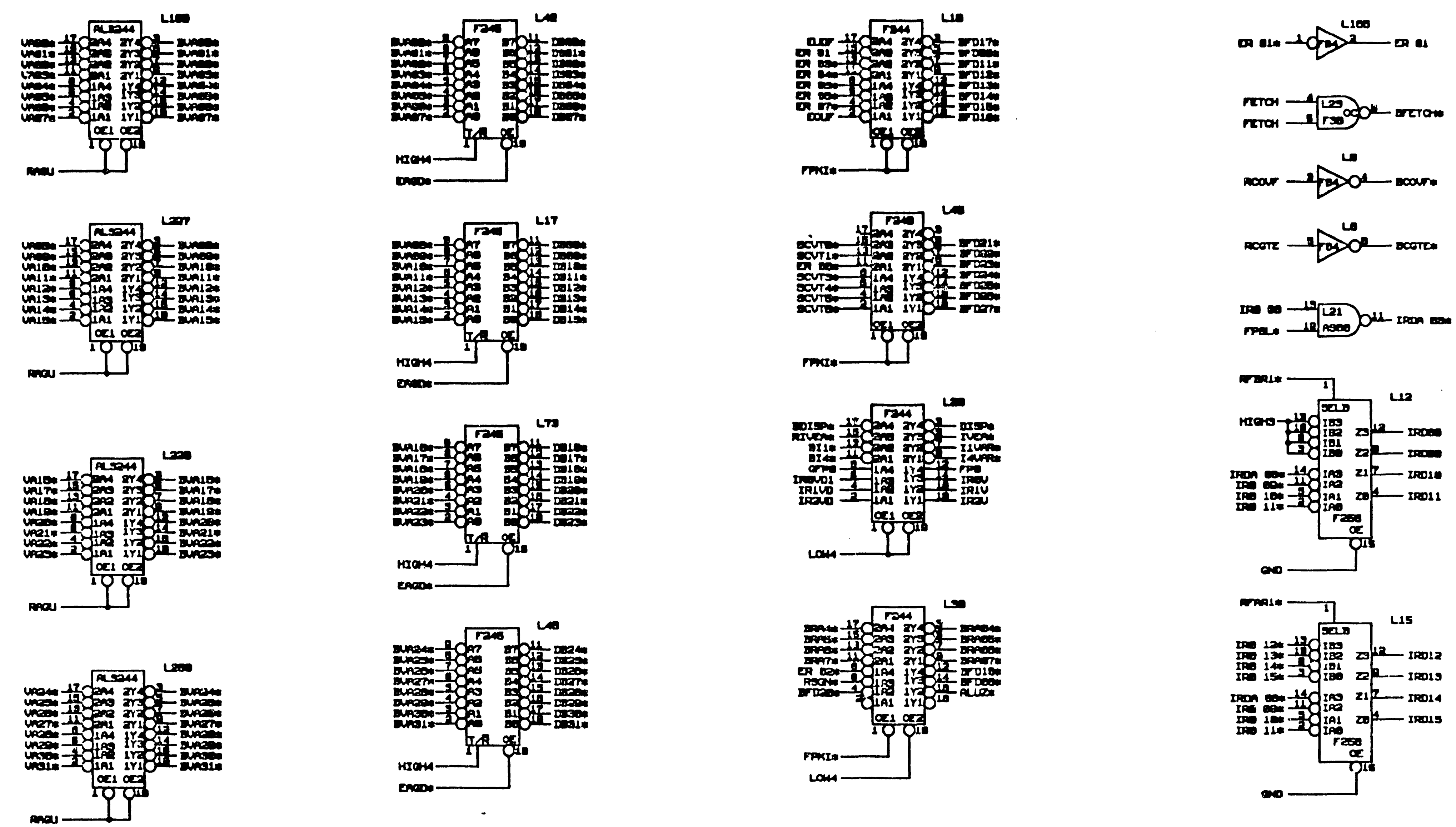

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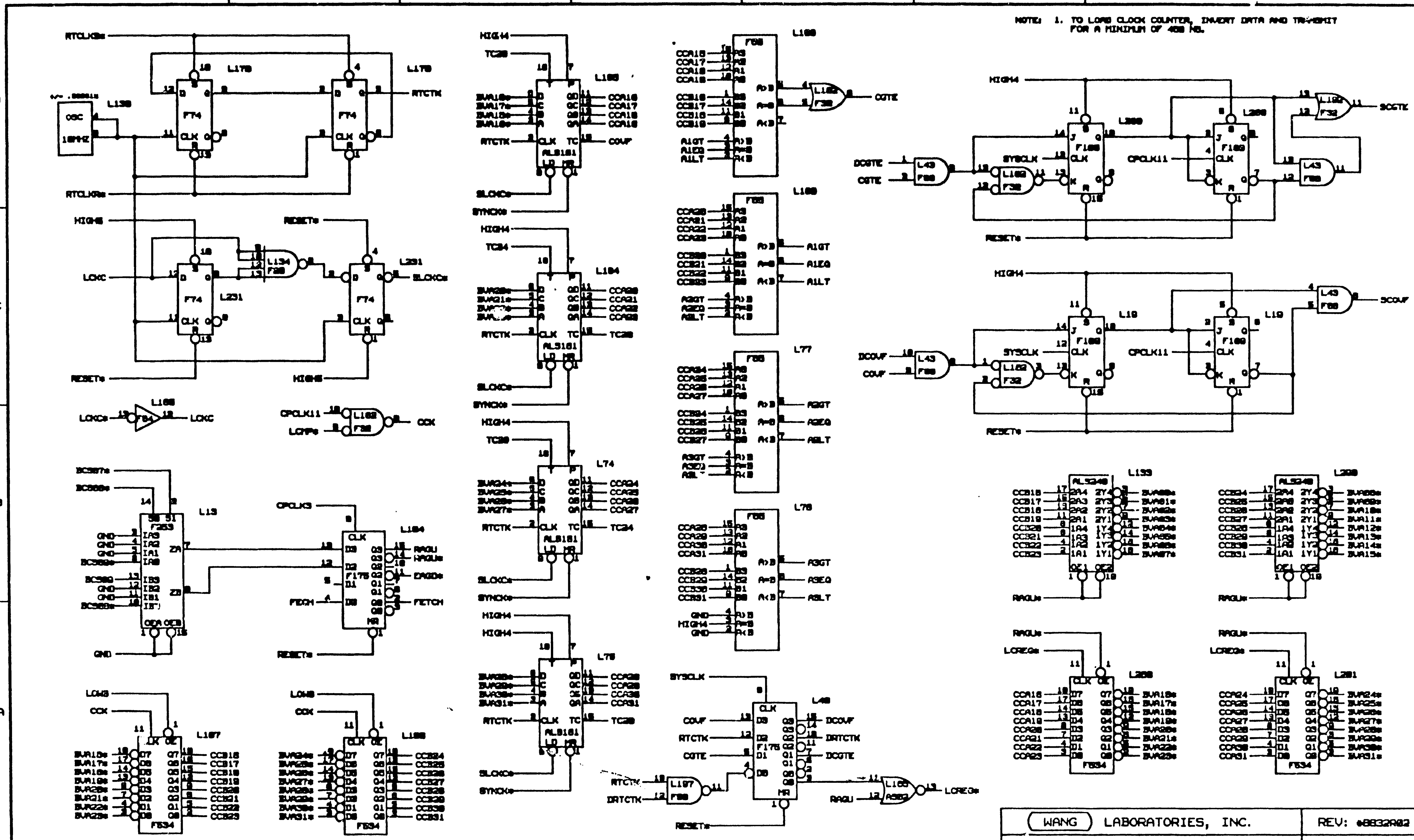
ENGINEER:	PAGE: 17 OF 19



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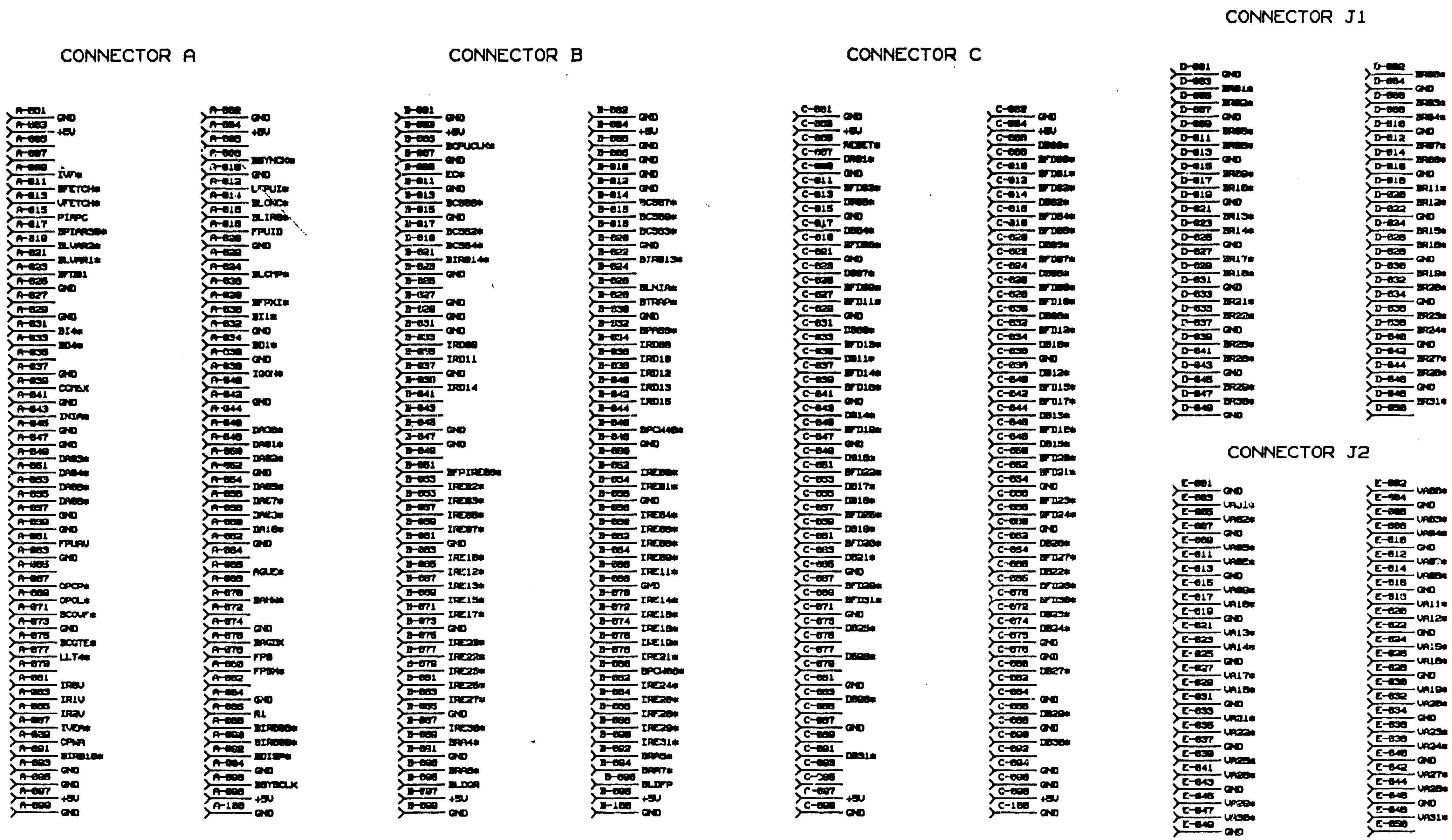

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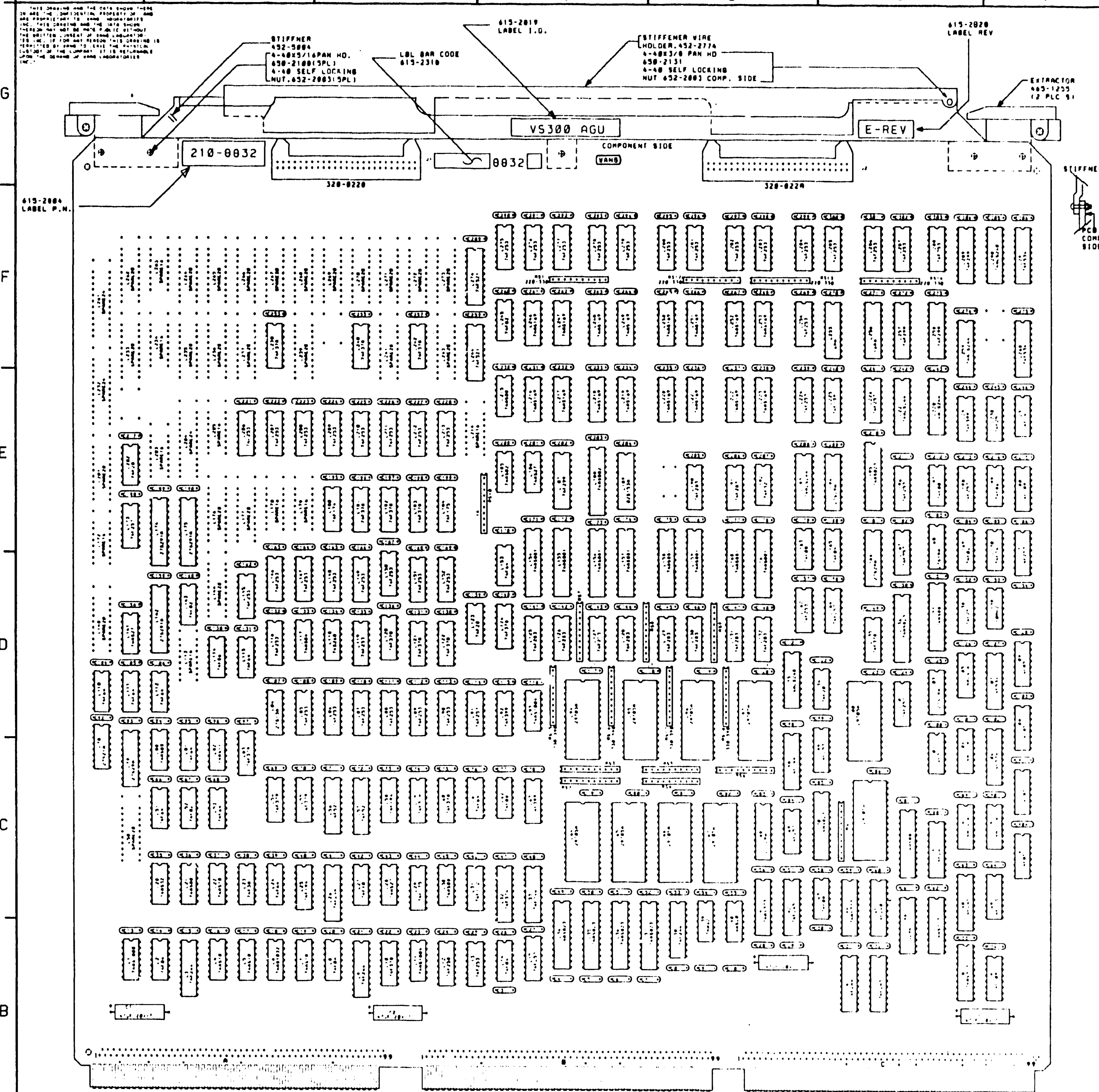
TITLE: VS-300 AGU SCHEMATICS	DATE: 05/23/85
ENGINEER:	PAGE: 19 OF 19



NOTES:
1. UNLESS OTHERWISE SPECIFIED,
ALL CAPACITORS ARE .047UF EXPRESSED IN MICROFARADS.
ALL SIPS ARE 390 EXPRESSED IN OHMS.

WANG		BY	DATE	APPROVED BY	DATE
		DWN OCT		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS300	E C CONTROL		MFG ENGR	
	10-214	TITLE VS300 AGU			
FINISH		214-8832	C	8832	6

VS-300 ATU INDEX

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1.	VIRTUAL ADDRESS BUFFERS, TRANSLATION BUFFER BYPASS, X-BUS TRANSCEIVER , X-BUS LATCH, TRANSLATION BUFFER PARITY GEN.
2.	TRANSLATION BUFFER STORE, TRANSLATION BUFFER PARITY CHECK, TRANSLATION BUFFER TAG COMPARE
3.	PHYSICAL ADDRESS REG.(PAR), PHYSICAL INSTUCTION ADDRESS REG.(PIAR), PHYSICAL ADDRESS MUX
4.	WRITE INSTRUCTION QUEUE DETECT, CURRENT RING OF EXECUTION, PROTECTION CHECKS, TRANSLATION BUFFER TAG BUFFER
5.	ADDRESS TRANSLATION BUFFER CONTROL, X-BUS CONTROL
6.	OCTAL FILL ADDR. REG, SYSTEM ADDR BUFFERS, INTER PROCESSOR COMMUNICATIONS REG, EXTERNAL MEMORY ADDR REG, CACHE ADDR DRIVERS, R/C ADDR DRIVERS
7.	CACHE TAG ADDR MUX, CACHE TAG DATA STORE, CACHE TAG PARITY LOGIC, CACHE TAG COMPARE LOGIC
8.	CACHE DATA STORE, CACHE PARITY DATA STORE, CACHE PARITY CHECK
9.	SYSTEM DATA BUS TRANSCEIVER, CACHE DATA STORE LATCH, CACHE PARITY DATA STORE LATCH
10.	WRITE REORDERING AND MERGE BUFFER
11.	READ REORDERING BUFFER
12.	D-BUS TRANSCEIVERS, SIGN EXTEND, ZERO FILL
13.	SYSTEM BUS INTERFACE CONTROL LOGIC
14.	CACHE CONTROLS
15.	MEMORY OP DECODING
16.	STATE MACHINES, EXTERNAL WRITE DETECTION
17.	IPC CONTROLS, RC TABLE ,ATU CONTROL REG.
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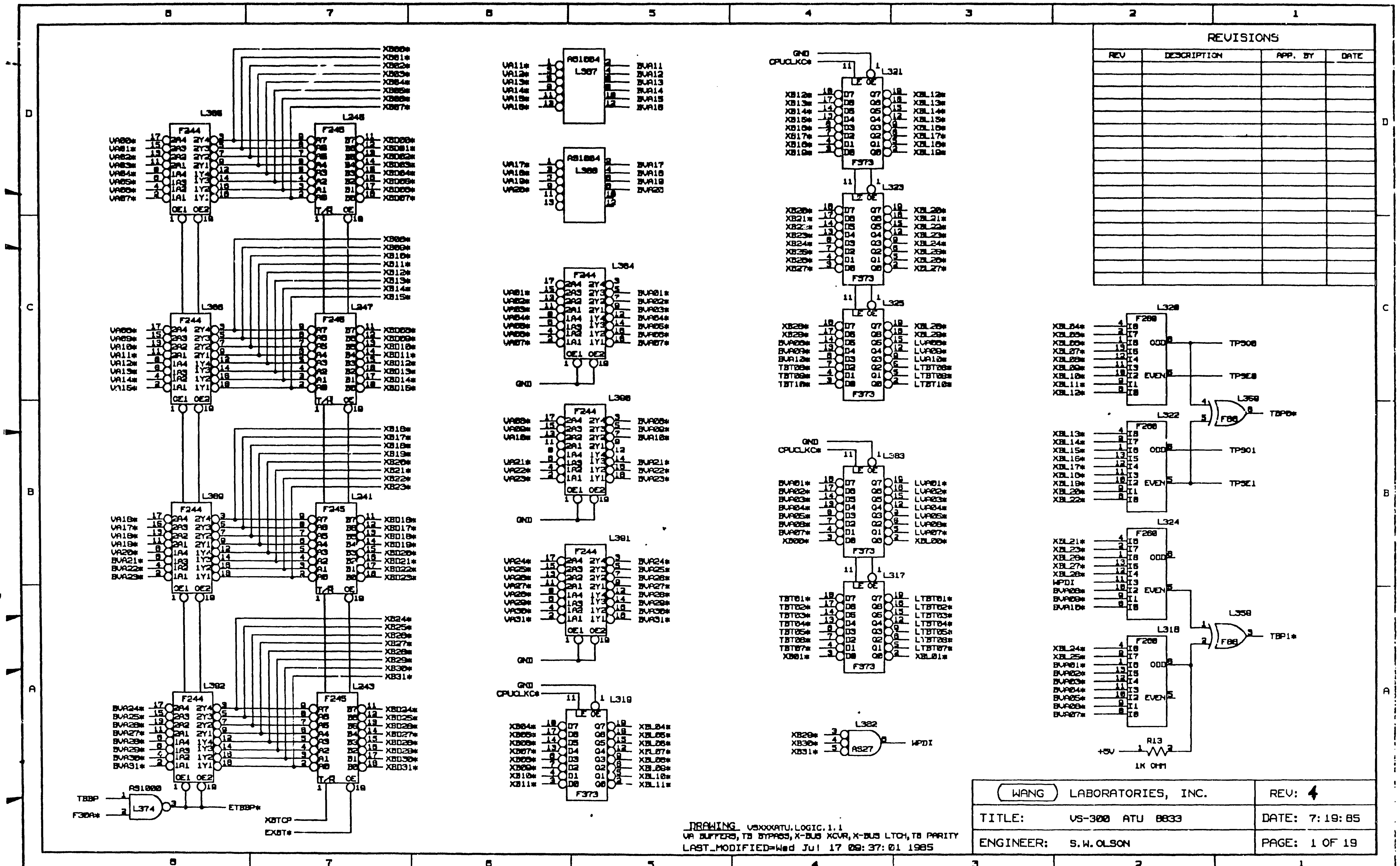
E-REV
2

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:19:85
ENGINEER: S.W.OLSON	PAGE: 0 OF 19



REVISIONS
REV
DESCRIPTION
APP. BY
DATE
F244
F245
F373
F280
F86
AS1004
AS1000
AS27
R13
1K OHM
+5V
GND
CPUCLKC*
TP500
TP5E0
TP501
TP5E1
TBP0*
TBP1*
WPDI
ETBBP*
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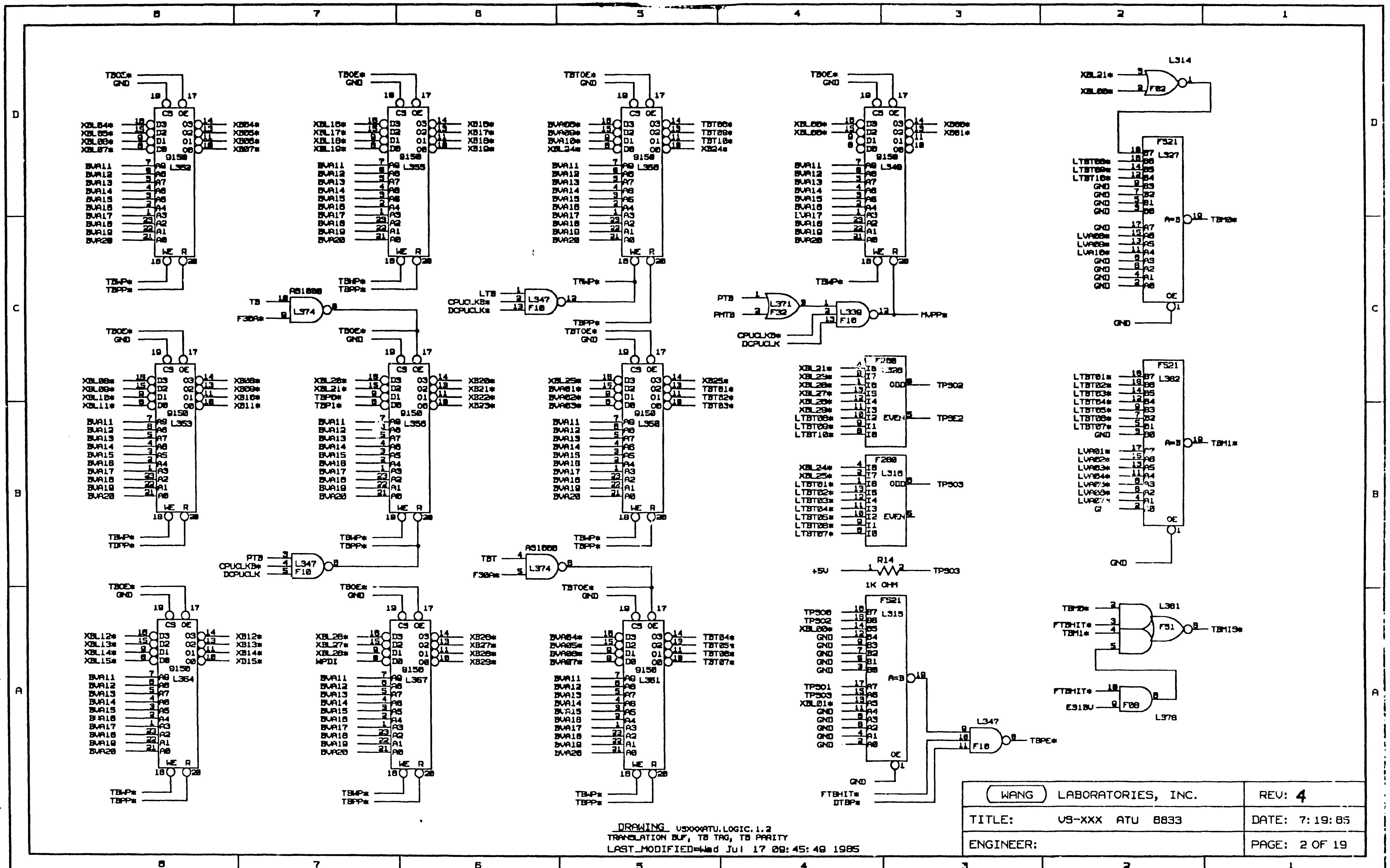
VA BUFFERS, TB BYPASS, X-BUS XCVR, X-BUS LTCH, TB PARITY
LAST_MODIFIED=Wed Jul 17 09:37:01 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 ATU 8833
DATE: 7:19:85
ENGINEER: S.W.OLSON
PAGE: 1 OF 19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TRANSLATION BUF, TB TAG, TB PARITY
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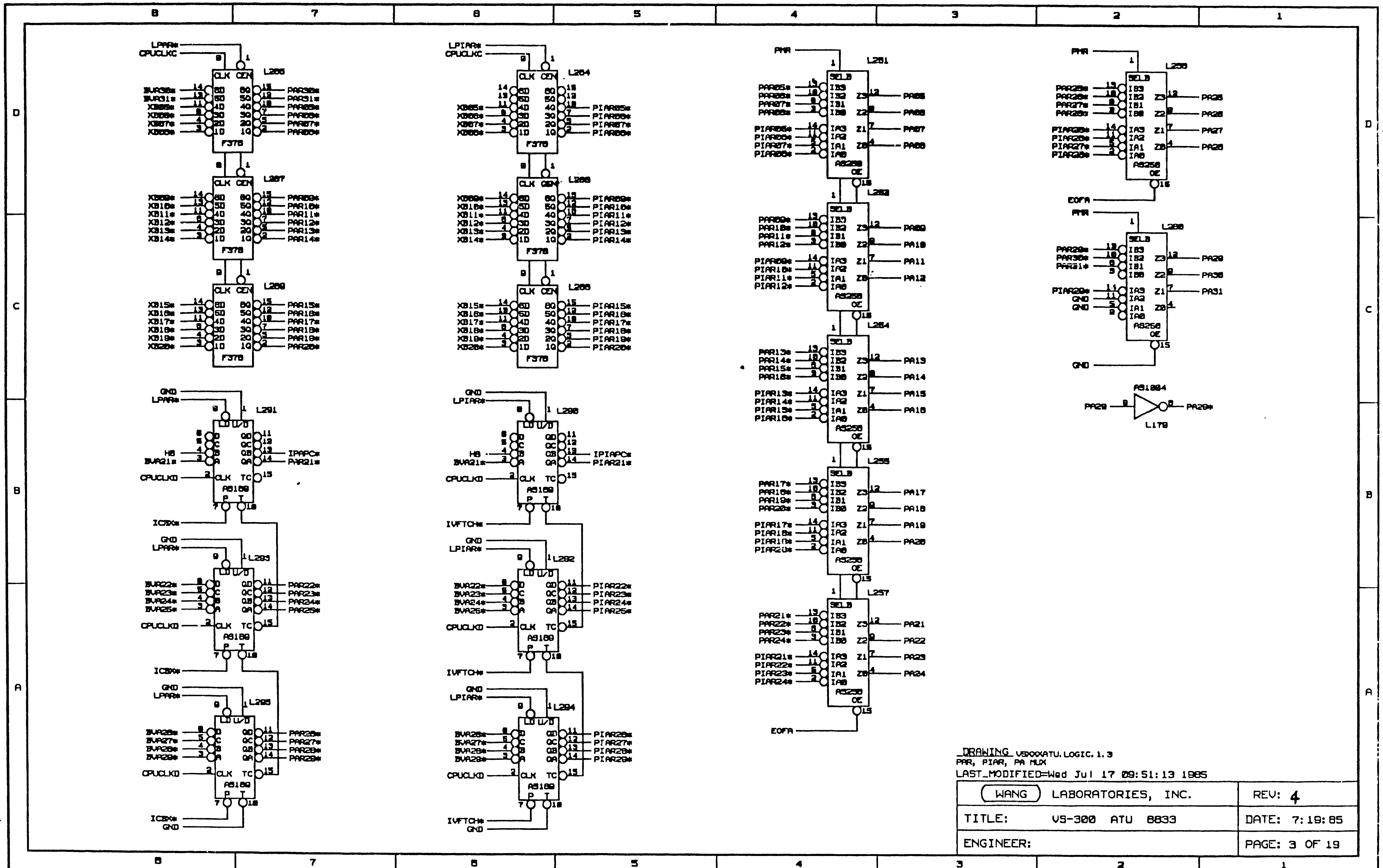
REV: 4
TITLE: VS-XXX ATU 8833
DATE: 7:19:85
ENGINEER:
PAGE: 2 OF 19



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PAR, PIAR, PA MUX
LAST_MODIFIED=Wed Jul 17 09:51:13 1985

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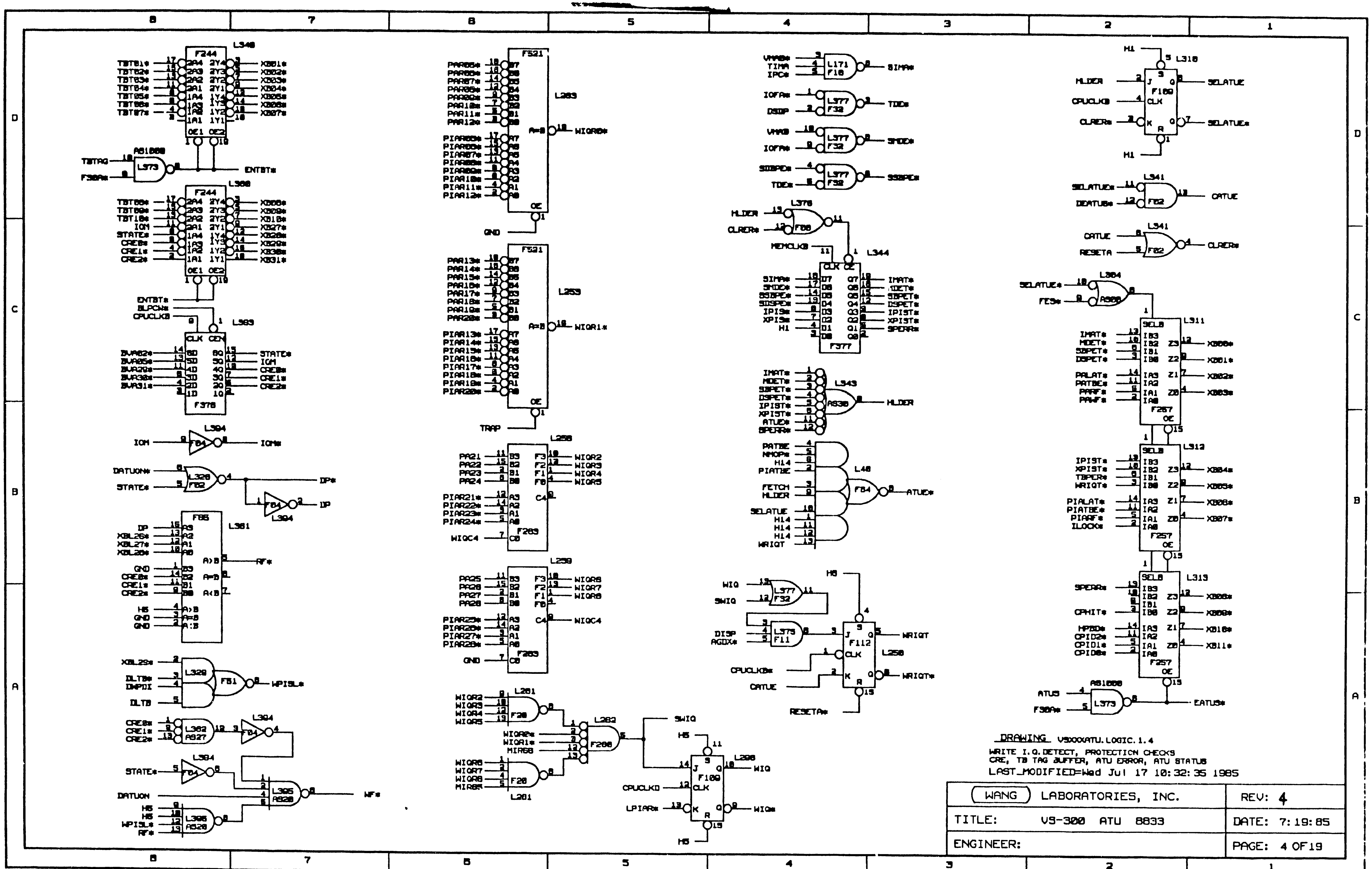
TITLE: VS-300 ATU 0833	DATE: 7:10:85
ENGINEER:	PAGE: 3 OF 19



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WRITE I.Q. DETECT, PROTECTION CHECKS
CRE, TB TAG BUFFER, ATU ERROR, ATU STATUS

LAST_MODIFIED=Wed Jul 17 10:32:35 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:19:85
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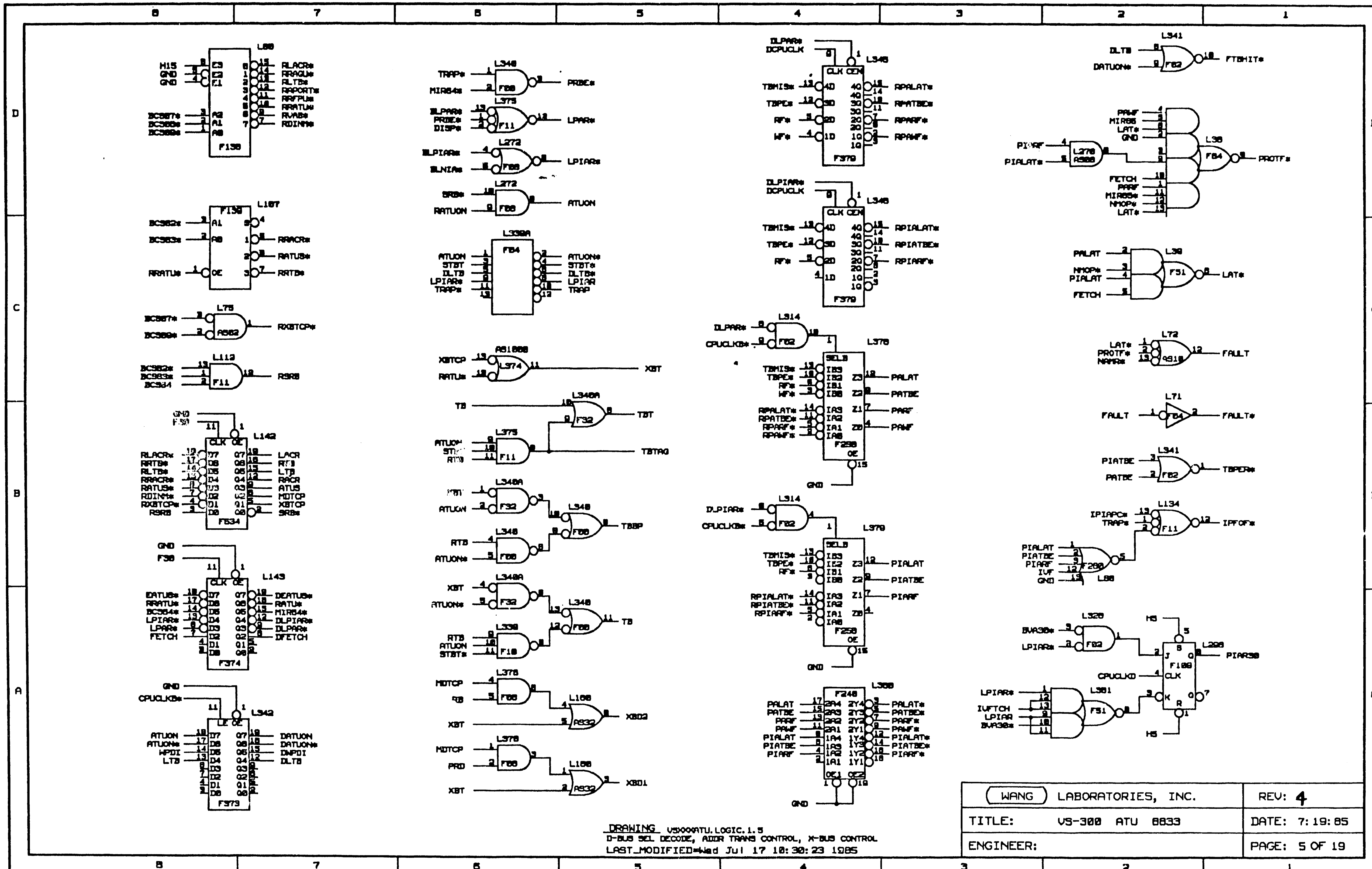

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D-BUS SEL DECODE, ADDR TRANS CONTROL, X-BUS CONTROL
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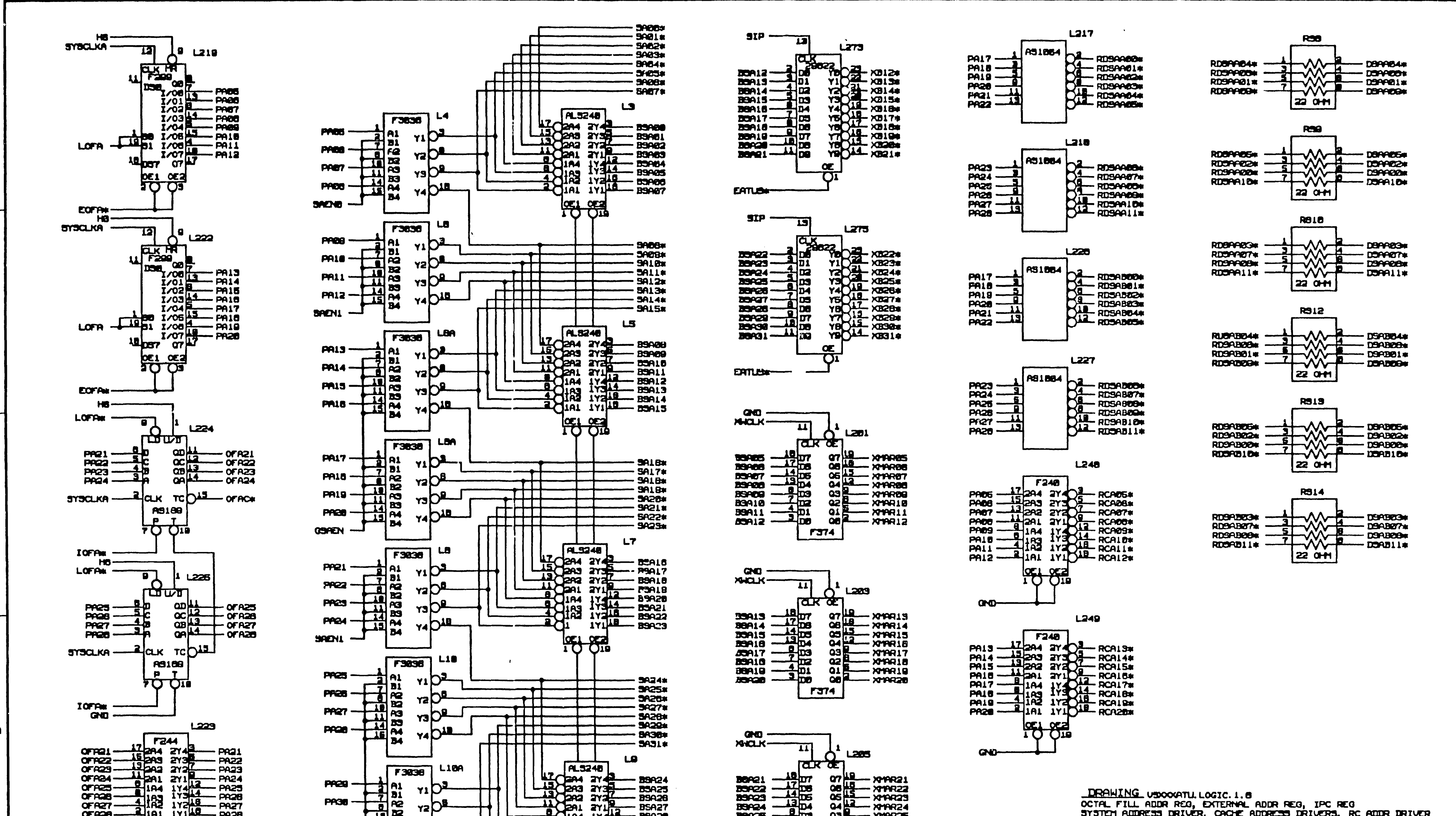
WANG LABORATORIES, INC. REV: 4
TITLE: VS-300 ATU 8833 DATE: 7:19:85
ENGINEER: PAGE: 5 OF 19



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OCTAL FILL ADDR REG, EXTERNAL ADDR REG, IPC REG
SYSTEM ADDRESS DRIVER, CACHE ADDRESS DRIVERS, RC ADDR DRIVER
LAST_MODIFIED=Wed Jul 17 10:38:42 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:18:85
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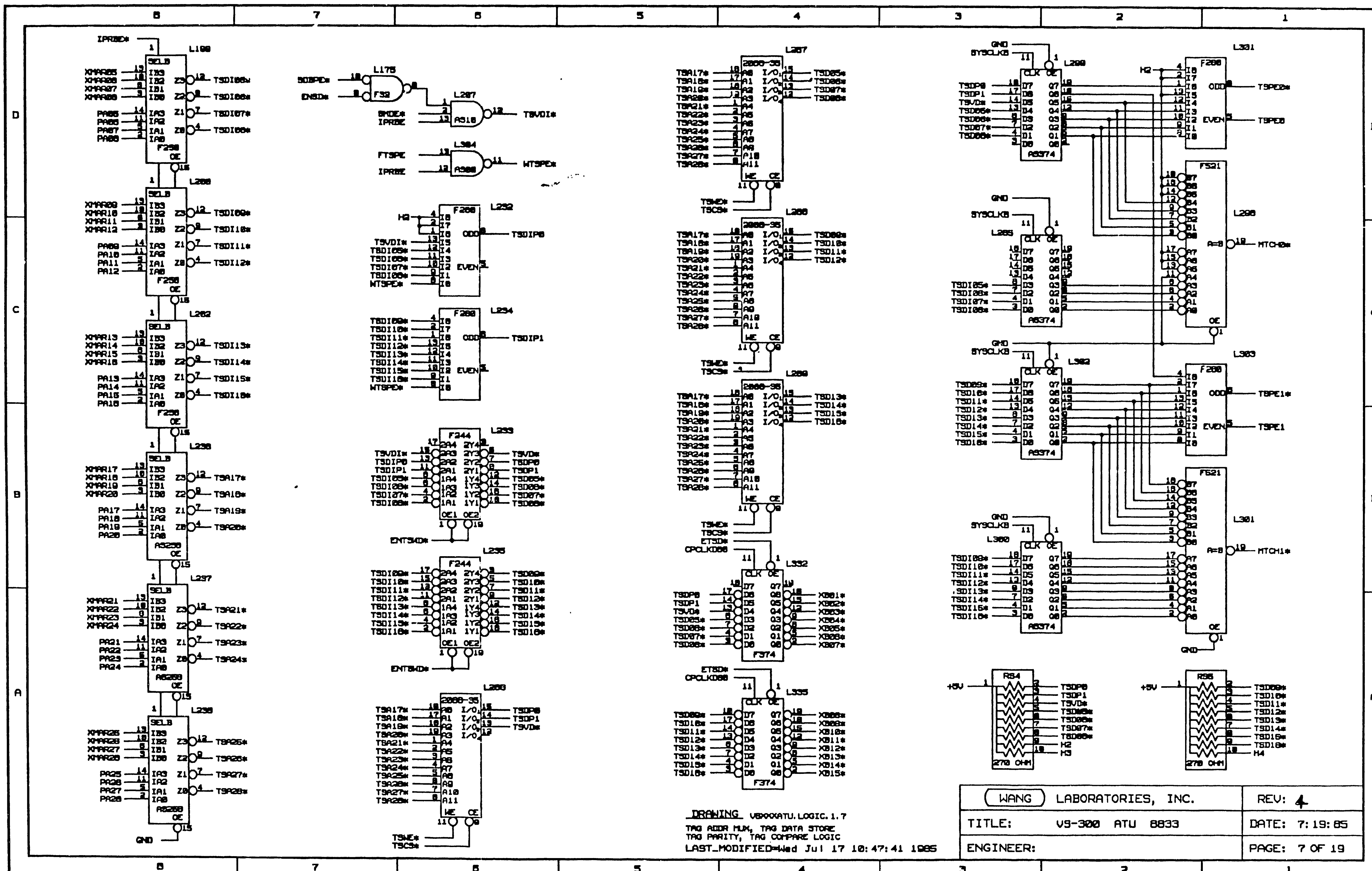

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TAG ADDR MUX, TAG DATA STORE
TAG PARITY, TAG COMPARE LOGIC
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WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 ATU 8833
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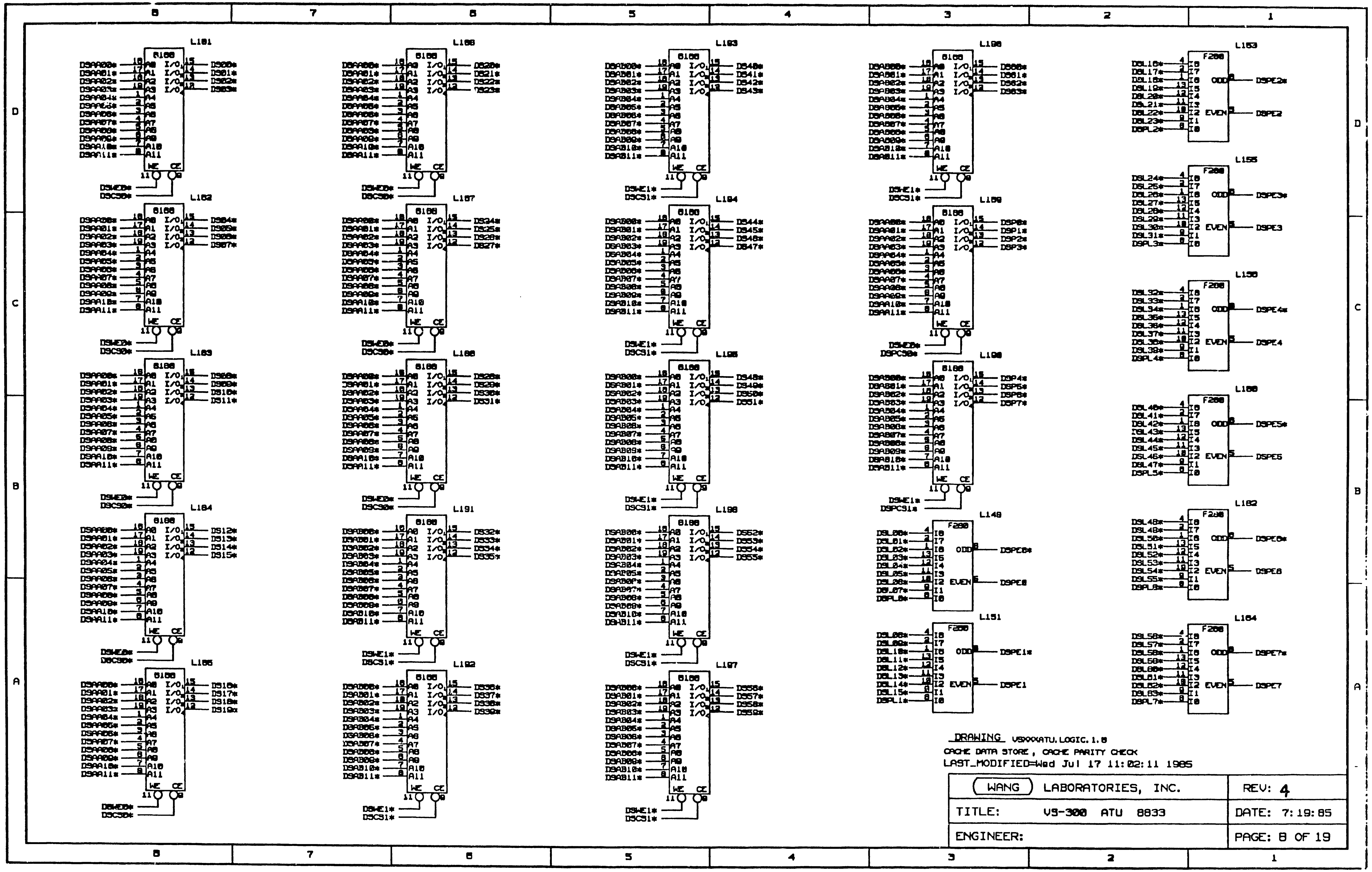

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CACHE DATA STORE, CACHE PARITY CHECK

LAST_MODIFIED=Wed Jul 17 11:02:11 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:19:85
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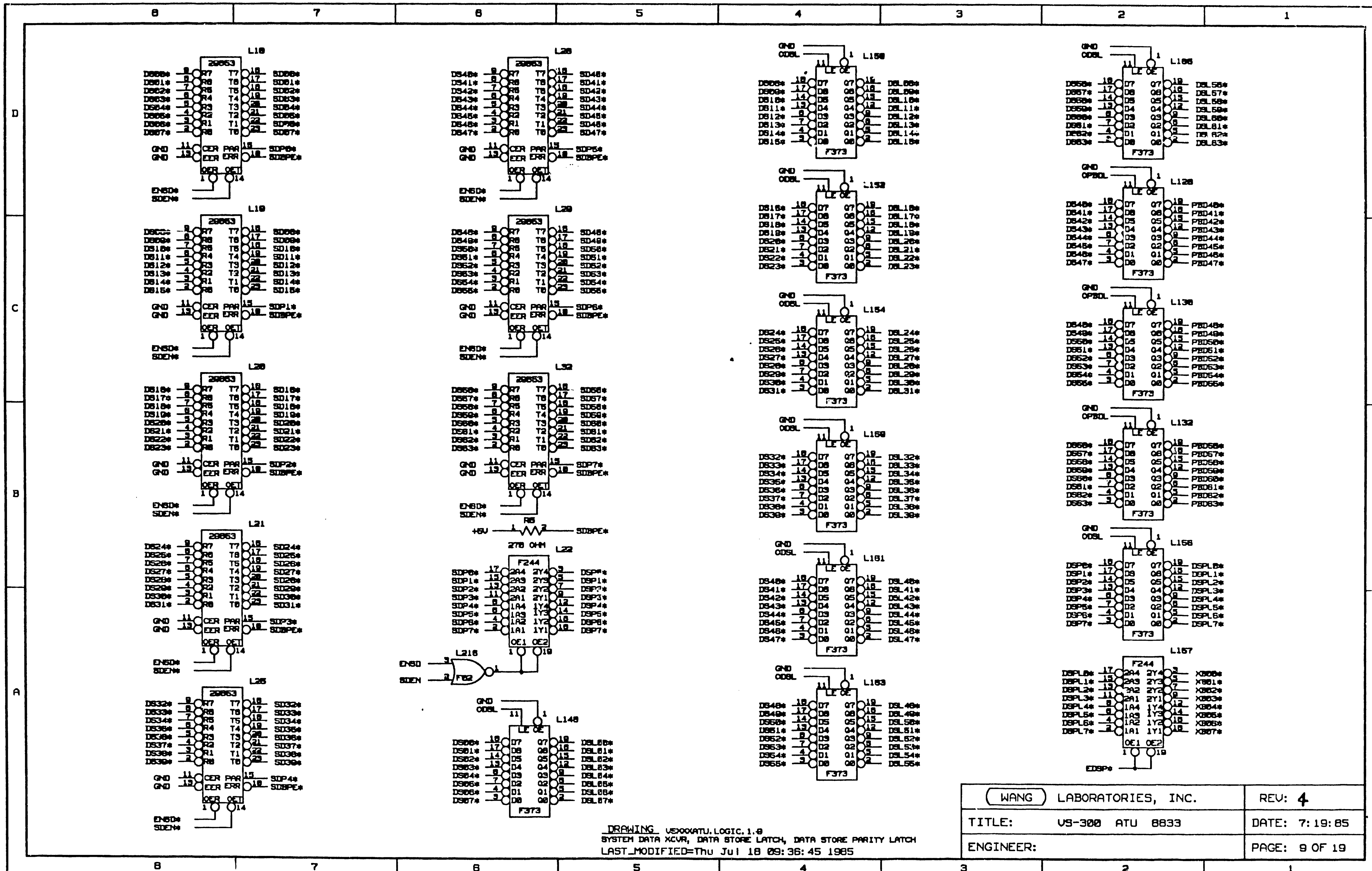
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REV: 4
TITLE: VS-300 ATU 8833
DATE: 7:19:85
ENGINEER:
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SYSTEM DATA XCVR, DATA STORE LATCH, DATA STORE PARITY LATCH
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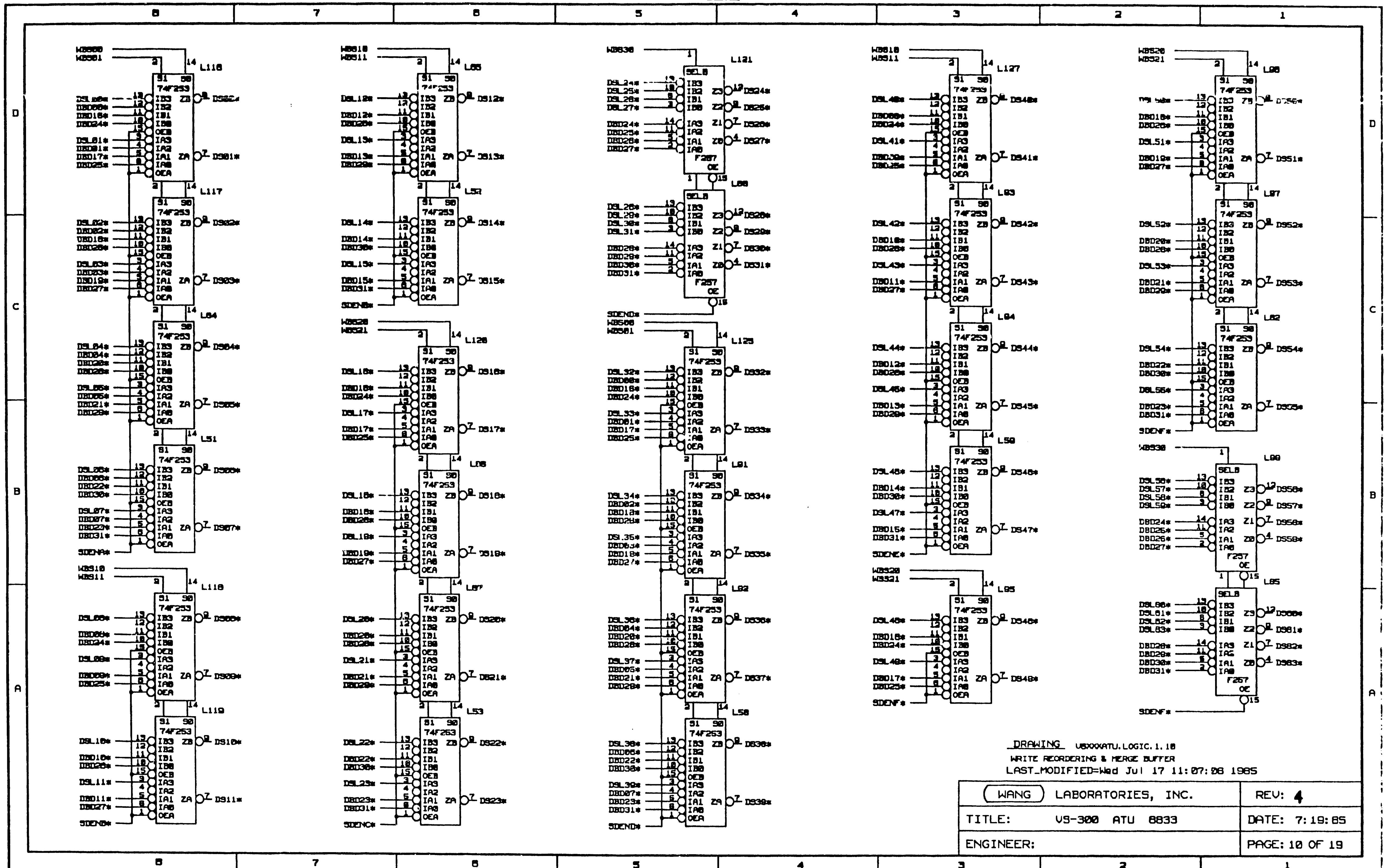

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WRITE REORDERING & MERGE BUFFER
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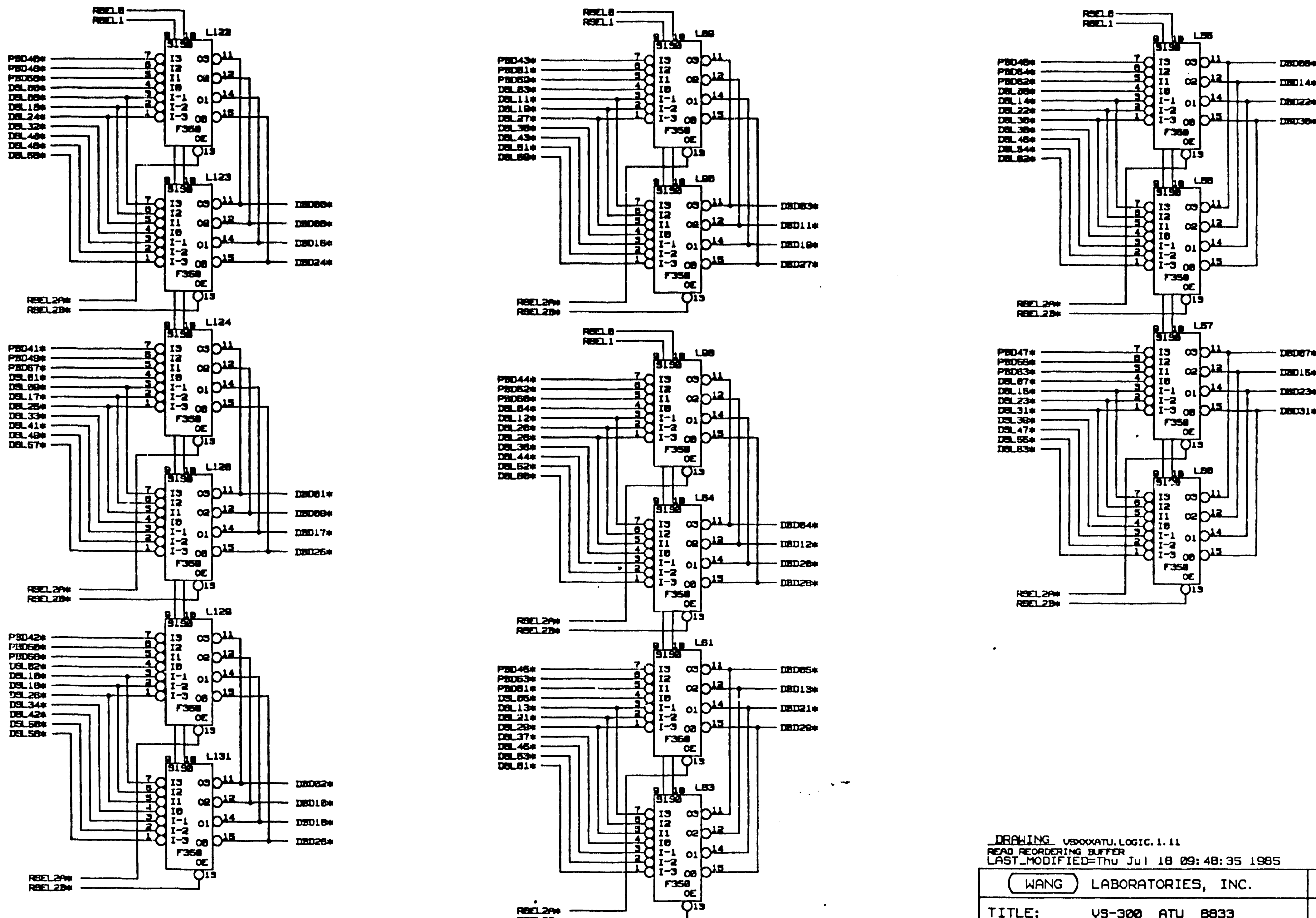
ENGINEER:	PAGE: 10 OF 19



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READ REORDERING BUFFER
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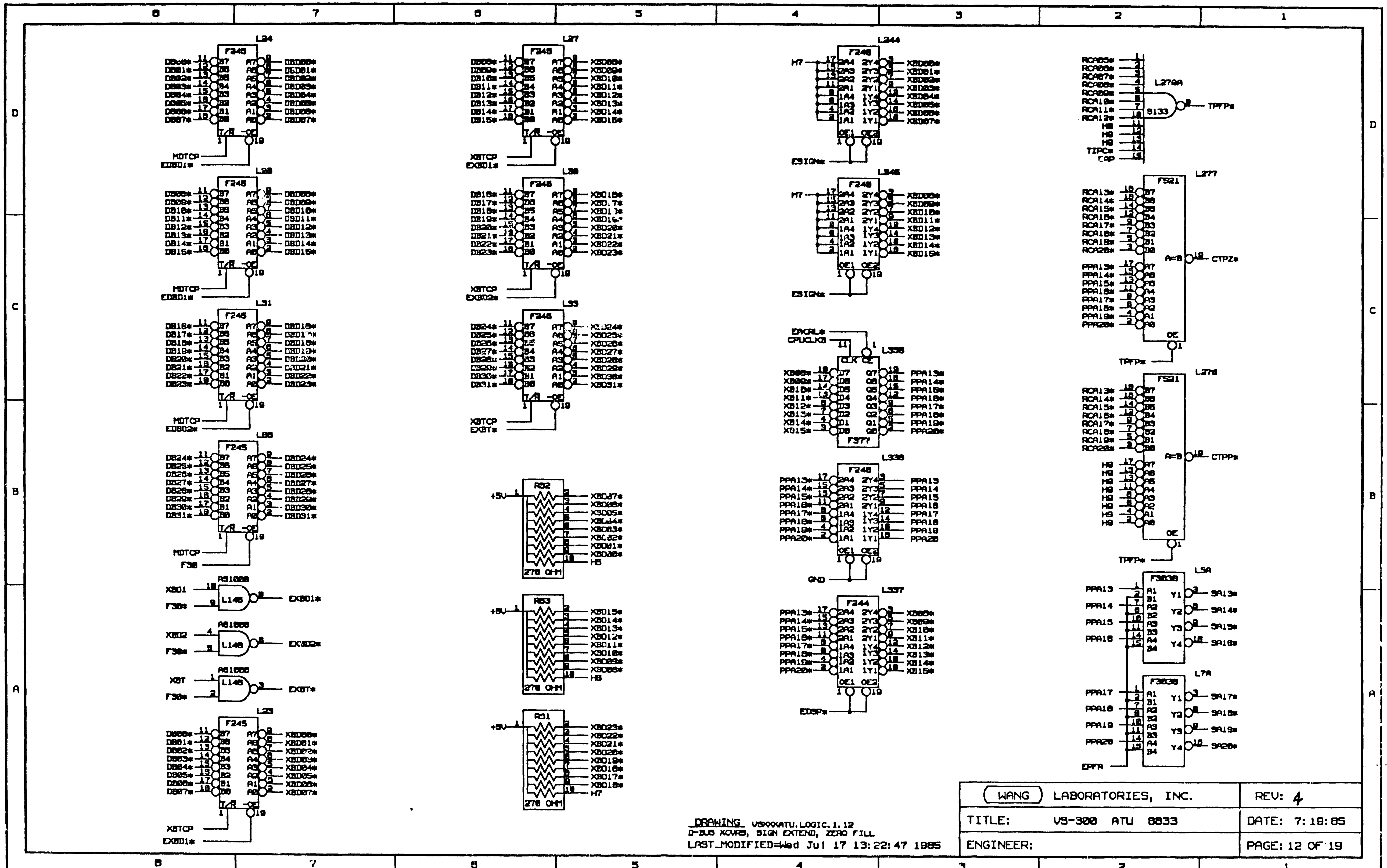

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D-BUS XCVRS, SIGN EXTEND, ZERO FILL
LAST_MODIFIED=Wed Jul 17 13:22:47 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:18:85
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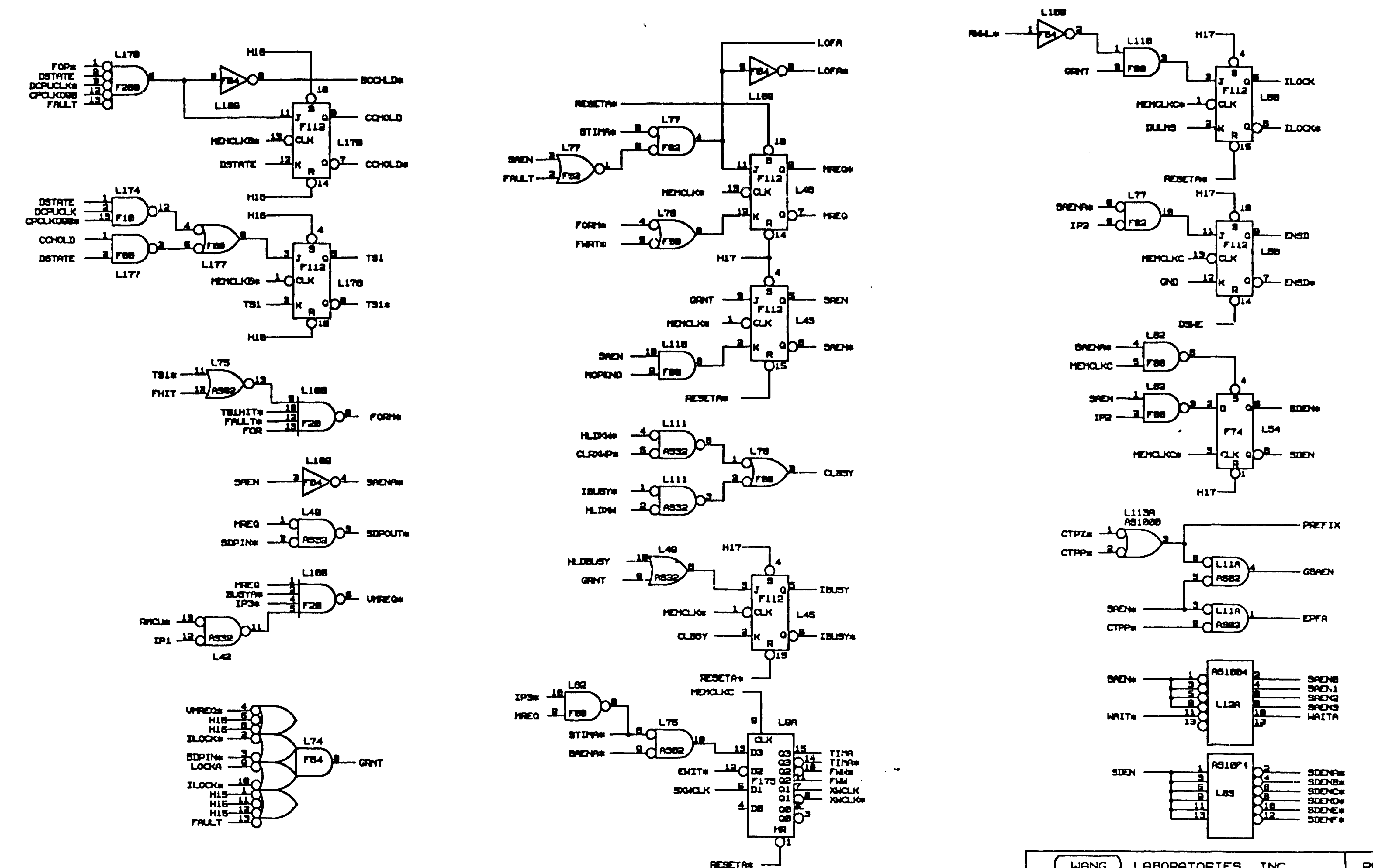

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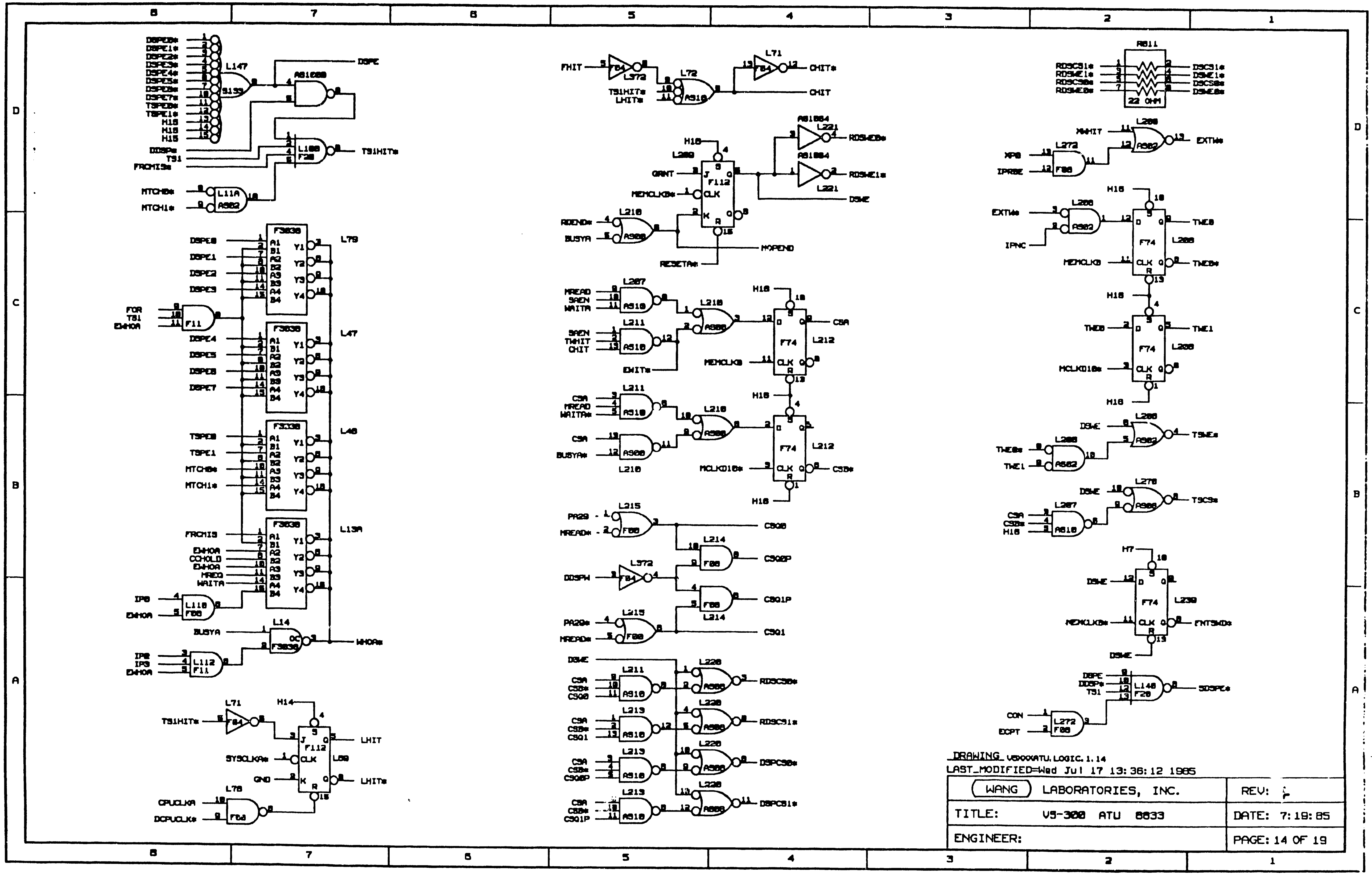
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TITLE: VS-300 ATU 8833
DATE: 7:18:85
ENGINEER:
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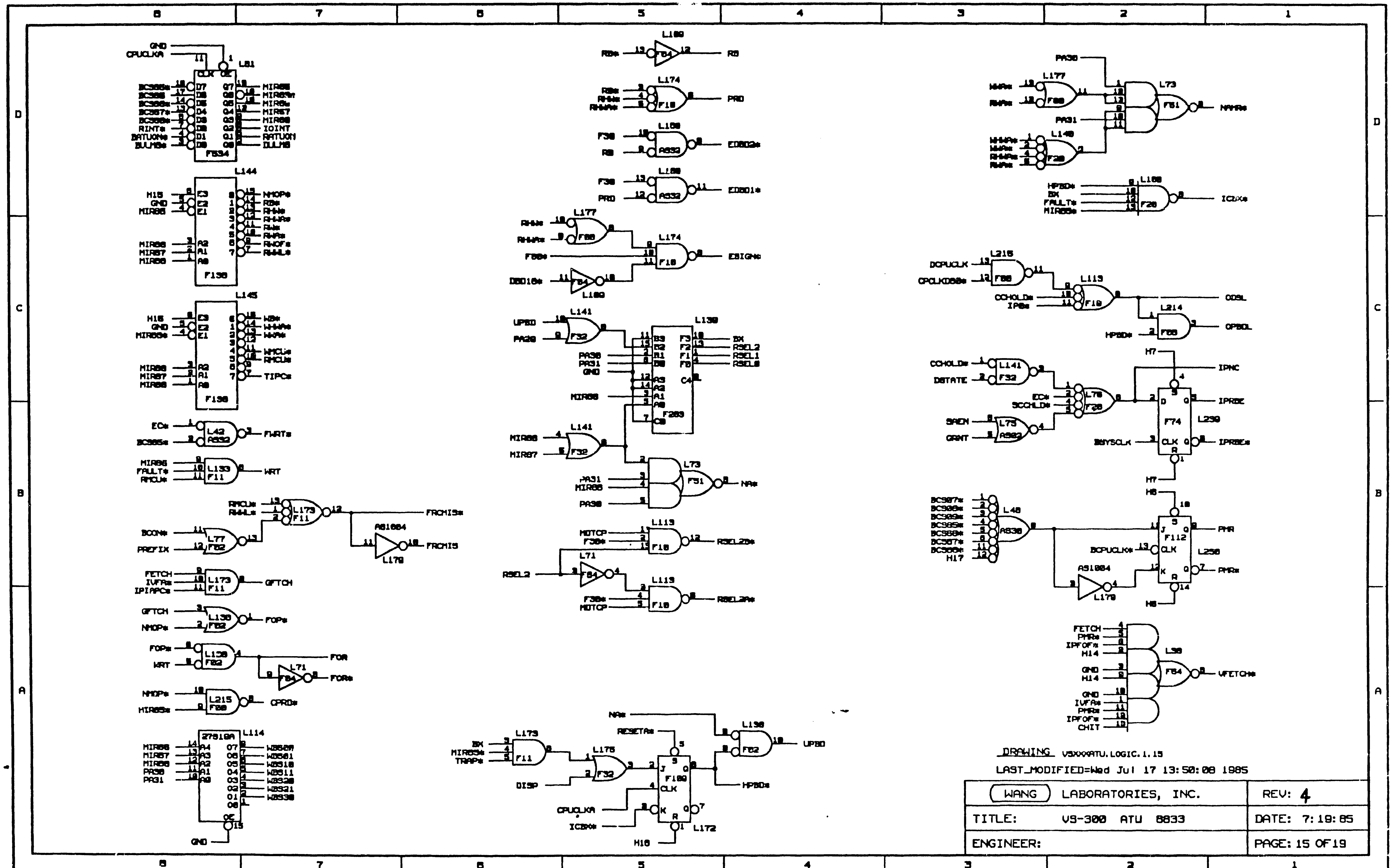

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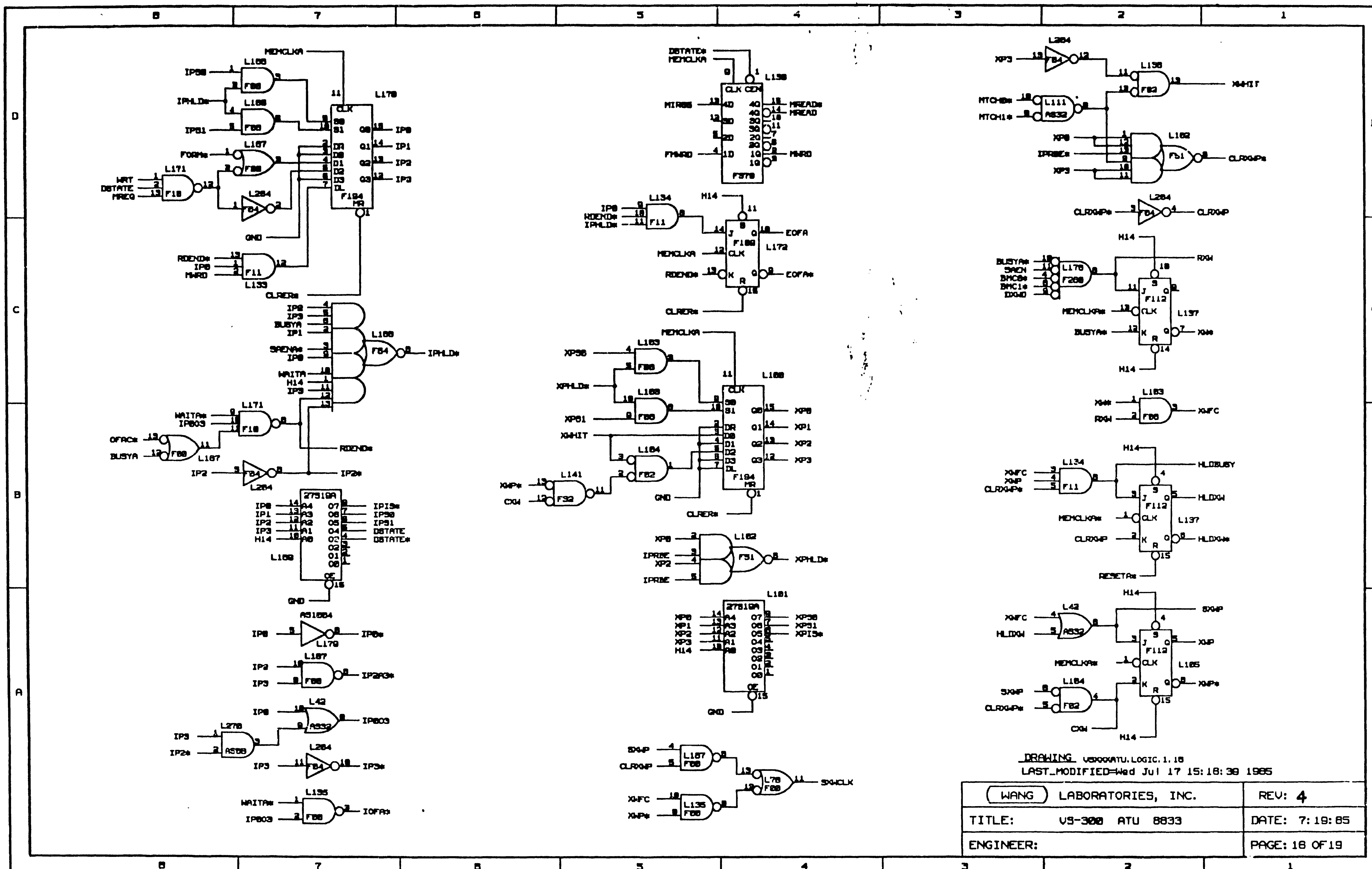
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TITLE: VS-300 ATU 8833
DATE: 7:19:85
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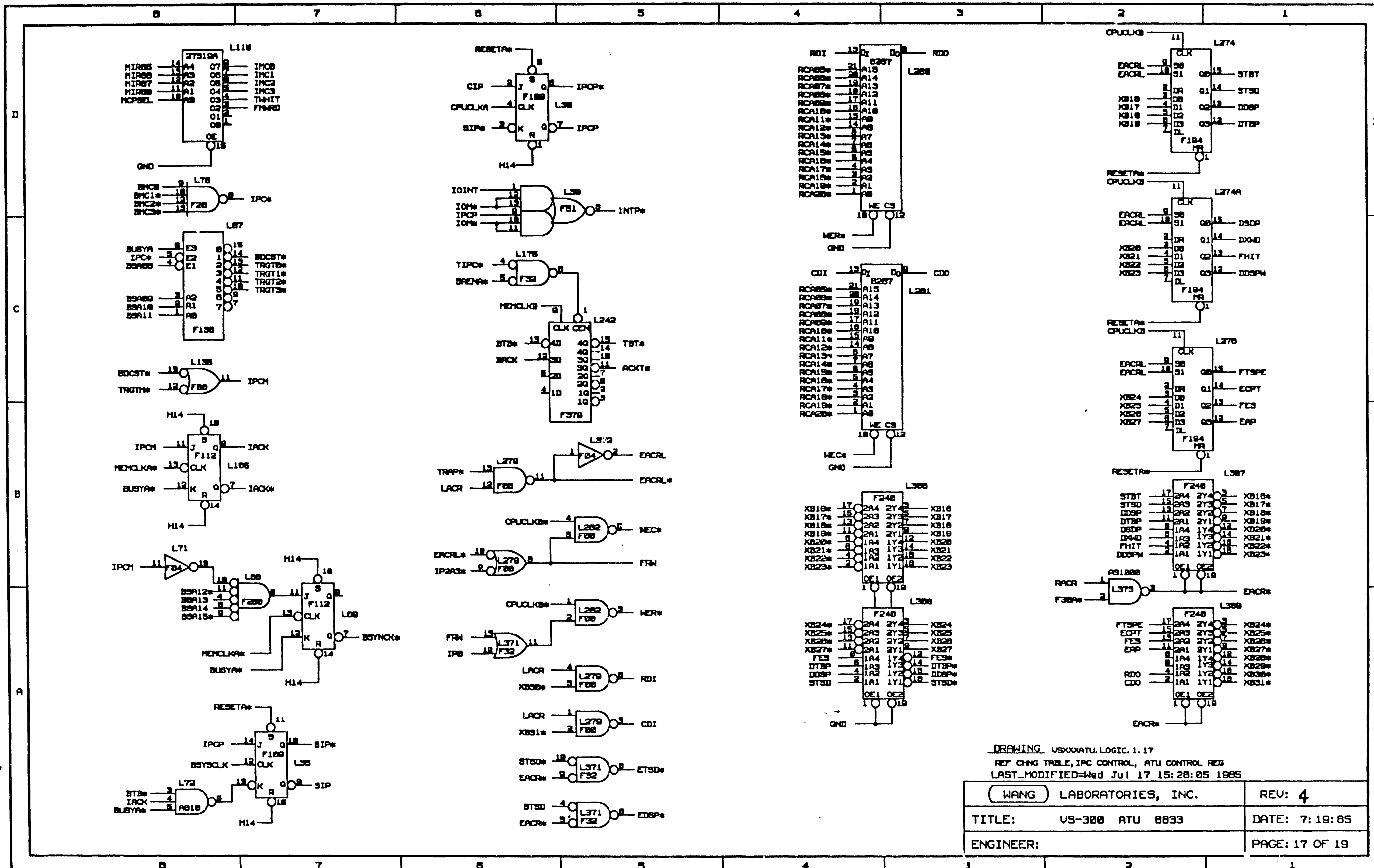

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REF CHNG TABLE, IPC CONTROL, ATU CONTROL REG
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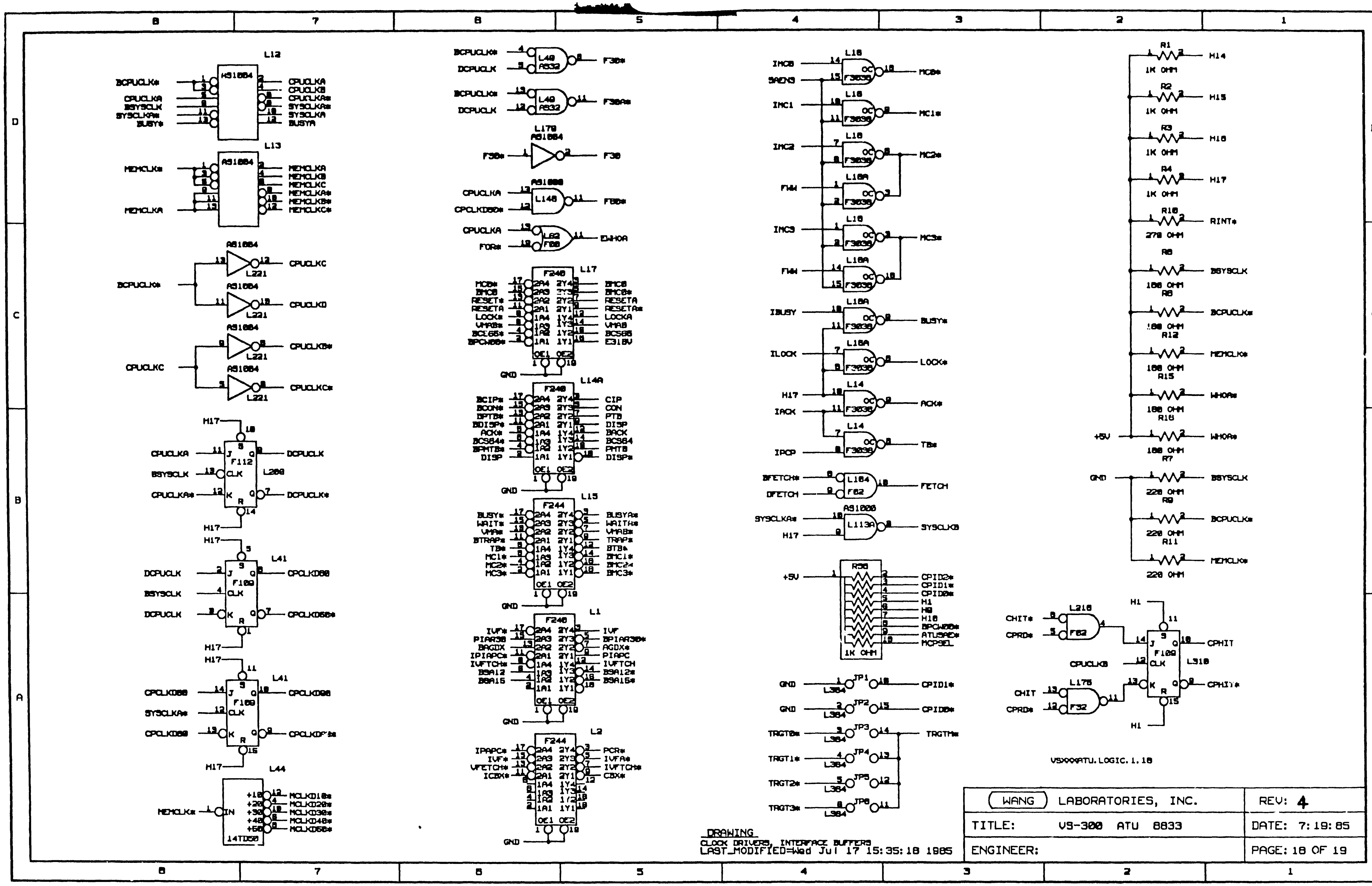
(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:19:85
ENGINEER:	PAGE: 17 OF 19



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CLOCK DRIVERS, INTERFACE BUFFERS
LAST_MODIFIED=Wed Jul 17 15:35:18 1985

VSXXXATU.LOGIC.1.18

WANG LABORATORIES, INC.		REV: 4
TITLE:	VS-300 ATU 8833	DATE: 7:19:85
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CONNECTOR A

Pin	Signal	Pin	Signal
A-001	GND	A-002	GND
A-003	+5V	A-004	+5V
A-005		A-006	
A-007		A-008	BSYNCK*
A-009	IVF*	A-010	GND
A-011	BFETCH*	A-012	RINT*
A-013	VFETCH*	A-014	SA00*
A-015	PIAPC	A-016	
A-017	BPIAR30*	A-018	SA01*
A-019	SA02*	A-020	GND
A-021	SA03*	A-022	
A-023		A-024	SA04*
A-025	GND	A-026	GND
A-027		A-028	SA05*
A-029	SA06*	A-030	
A-031	GND	A-032	GND
A-033	SA08*	A-034	SA07*
A-035		A-036	
A-037		A-038	SA09*
A-039	SA10*	A-040	
A-041	GND	A-042	GND
A-043	SA11*	A-044	
A-045		A-046	SA12*
A-047	GND	A-048	SA13*
A-049	SA14*	A-050	
A-051	GND	A-052	GND
A-053	SA15*	A-054	
A-055		A-056	SA16*
A-057	GND	A-058	GND
A-059	PROTF*	A-060	SA17*
A-061	SA18*	A-062	GND
A-063	SA19*	A-064	ATUE*
A-065	LAT*	A-066	SA20*
A-067	GND	A-068	PCR*
A-069		A-070	SA21*
A-071	SA22*	A-072	CBX*
A-073	BPMTB*	A-074	GND
A-075	SA24*	A-076	SA23*
A-077	GND	A-078	BACOK
A-079	INTP*	A-080	SA25*
A-081	SA26*	A-082	NAMR*
A-083		A-084	GND
A-085	SA27*	A-086	
A-087		A-088	SA28*
A-089	GND	A-090	SA29*
A-091	SA30*	A-092	BDISP*
A-093		A-094	GND
A-095	SA31*	A-096	BSYSCLK
A-097	+5V	A-098	+5V
A-099	GND	A-100	GND

CONNECTOR B

Pin	Signal	Pin	Signal
B-001	GND	B-002	GND
B-003	+5V	B-004	+5V
B-005	BCPUCLK*	B-006	MEMCLK*
B-007	GND	B-008	GND
B-009	EC*	B-010	WHOA*
B-011	GND	B-012	GND
B-013	BCS00*	B-014	BCS01*
B-015	GND	B-016	BCS09*
B-017	BCS02*	B-018	BCS03*
B-019	BCS04*	B-020	GND
B-021	BCS06*	B-022	BCS05*
B-023	GND	B-024	BCS07*
B-025	BCS08*	B-026	BLNIA*
B-027	BPTB*	B-028	BTRAP*
B-029	BLPIAR*	B-030	
B-031	GND	B-032	ATUSAE*
B-033	WAIT*	B-034	MC0*
B-035	BUSY*	B-036	MC1*
B-037	VMA*	B-038	MC2*
B-039	LOCK*	B-040	MC3*
B-041	SDPOUT*	B-042	SDPIN*
B-043	ACK*	B-044	BCON*
B-045	TB*	B-046	GND
B-047	BATUON*	B-048	BCIP*
B-049	BLPCW*	B-050	BULMS*
B-051	BLPAR*	B-052	ACKT*
B-053	SDP0*	B-054	TBT*
B-055	SD00*	B-056	GND
B-057	SD01*	B-058	SD02*
B-059	SD04*	B-060	SD03*
B-061	GND	B-062	SD05*
B-063	SD07*	B-064	SD06*
B-065	SDP1*	B-066	SD08*
B-067	SD09*	B-068	GND
B-069	SD11*	B-070	SD10*
B-071	SD12*	B-072	SD13*
B-073	GND	B-074	SD14*
B-075	SDP2*	B-076	SD15*
B-077	SD16*	B-078	SD17*
B-079	SD18*	B-080	BPCW00*
B-081	SD19*	B-082	SD20*
B-083	SD22*	B-084	SD21*
B-085	GND	B-086	SD23*
B-087	SD24*	B-088	SDP3*
B-089	SD25*	B-090	SD26*
B-091	SD27*	B-092	GND
B-093	SD28*	B-094	SD29*
B-095	SD31*	B-096	SD30*
B-097	+5V	B-098	+5V
B-099	GND	B-100	GND

CONNECTOR C

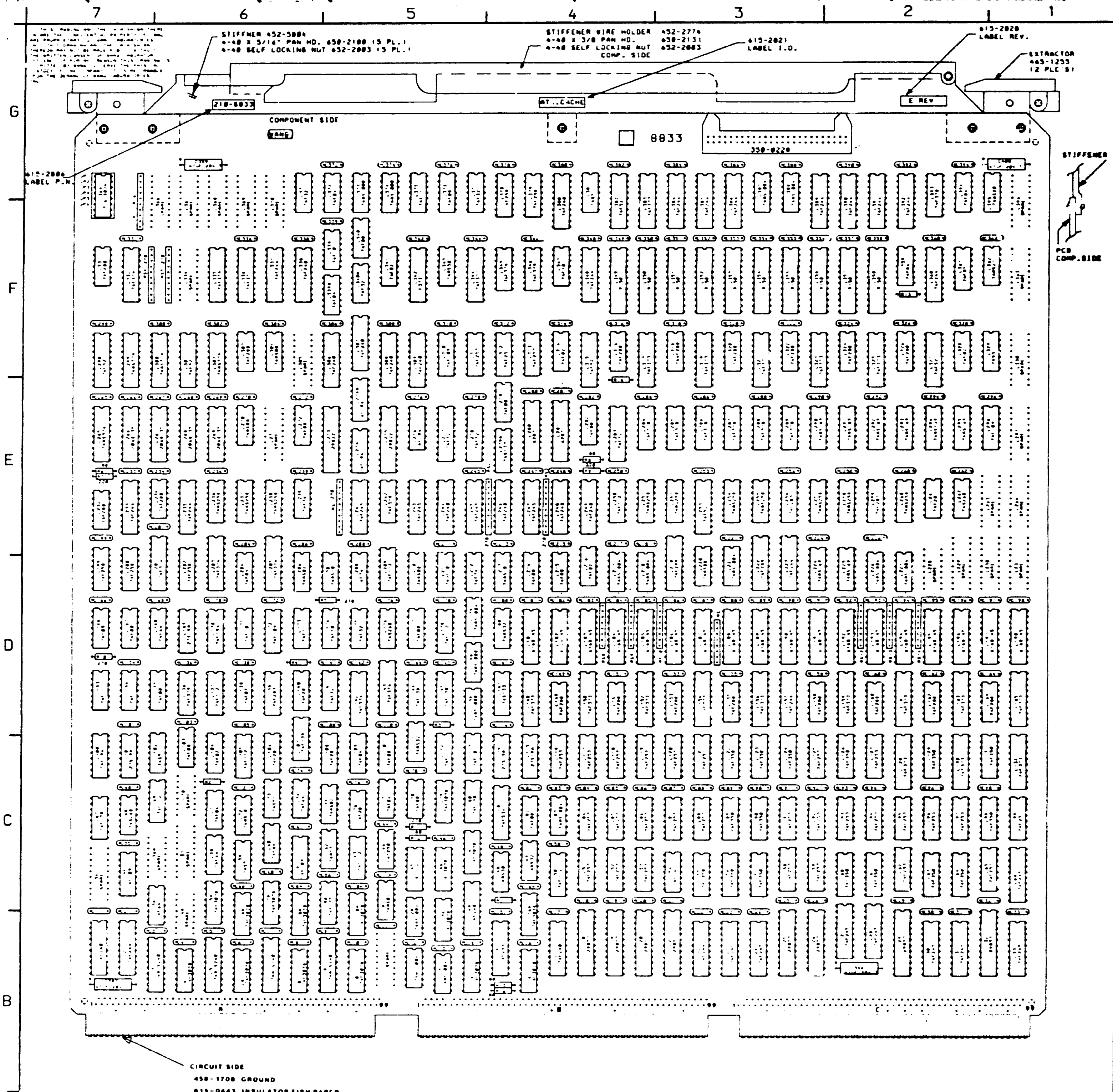
Pin	Signal	Pin	Signal
C-001	GND	C-002	GND
C-003	+5V	C-004	+5V
C-005	RESET*	C-006	DB00*
C-007	DB01*	C-008	SDP4*
C-009	SD32*	C-010	GND
C-011	SD34*	C-012	SD33*
C-013	DB03*	C-014	DB02*
C-015	SD35*	C-016	GND
C-017	DB04*	C-018	SD36*
C-019	SD37*	C-020	DB05*
C-021	GND	C-022	SD38*
C-023	DB07*	C-024	DB06*
C-025	SDP5*	C-026	SD39*
C-027	GND	C-028	SD40*
C-029	SD41*	C-030	DB08*
C-031	DB09*	C-032	SD42*
C-033	GND	C-034	DB10*
C-035	DB11*	C-036	SD43*
C-037	SD44*	C-038	DB12*
C-039	SD46*	C-040	SD45*
C-041	GND	C-042	SD47*
C-043	DB14*	C-044	DB13*
C-045	GND	C-046	SDP6*
C-047	SD48*	C-048	DB15*
C-049	DB16*	C-050	SD49*
C-051	SD50*	C-052	GND
C-053	DB17*	C-054	SD51*
C-055	DB18*	C-056	SD52*
C-057	SD53*	C-058	GND
C-059	DB19*	C-060	SD54*
C-061	SD55*	C-062	DB20*
C-063	DB21*	C-064	GND
C-065	SDP7*	C-066	DB22*
C-067	SD57*	C-068	SD56*
C-069	GND	C-070	SD58*
C-071	SD59*	C-072	DB23*
C-073	DB25*	C-074	DB24*
C-075	SD60*	C-076	GND
C-077	DB26*	C-078	SD61*
C-079	SD62*	C-080	DB27*
C-081	GND	C-082	SD63*
C-083	DB28*	C-084	GND
C-085		C-086	DB29*
C-087	GND	C-088	GND
C-089		C-090	DB30*
C-091	DB31*	C-092	
C-093		C-094	GND
C-095		C-096	
C-097	+5V	C-098	+5V
C-099	GND	C-100	GND

CONNECTOR J1

Pin	Signal	Pin	Signal
D-001	GND	D-002	VA00*
D-003	VA01*	D-004	GND
D-005	VA02*	D-006	VA03*
D-007	GND	D-008	VA04*
D-009	VA05*	D-010	GND
D-011	VA06*	D-012	VA07*
D-013	GND	D-014	VA08*
D-015	VA09*	D-016	GND
D-017	VA10*	D-018	VA11*
D-019	GND	D-020	VA12*
D-021	VA13*	D-022	GND
D-023	VA14*	D-024	VA15*
D-025	GND	D-026	VA16*
D-027	VA17*	D-028	GND
D-029	VA18*	D-030	VA19*
D-031	GND	D-032	VA20*
D-033	VA21*	D-034	GND
D-035	VA22*	D-036	VA23*
D-037	GND	D-038	VA24*
D-039	VA25*	D-040	GND
D-041	VA26*	D-042	VA27*
D-043	GND	D-044	VA28*
D-045	VA29*	D-046	GND
D-047	VA30*	D-048	VA31*
D-049	GND	D-050	

DRAWING VSXXXATU.LOGIC.1.19
I/O PIN LIST
LAST_MODIFIED=Wed Jul 17 15:48:30 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 ATU 8833	DATE: 7:19:85
ENGINEER: S.W.OLSON	PAGE: 19 OF 19



NOTES
1. UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE .047UF EXPRESSED IN MICROFARADS.
ALL RESISTORS ARE 1K 1/4W 5%. EXPRESSED IN OHMS.
ALL SIPS ARE 22 EXPRESSED IN OHMS.
2. PIN 1 OF ALL SIP PACKAGES FACE TOWARDS THE STIFFENER.

WANG		BY	DATE	APPROVED BY	DATE
		DWN DCT		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS300	E C CONTROL		MFG ENGR	
	10-214	TITLE VS300 ATU			
FINISH		210-8833	C	8833	4

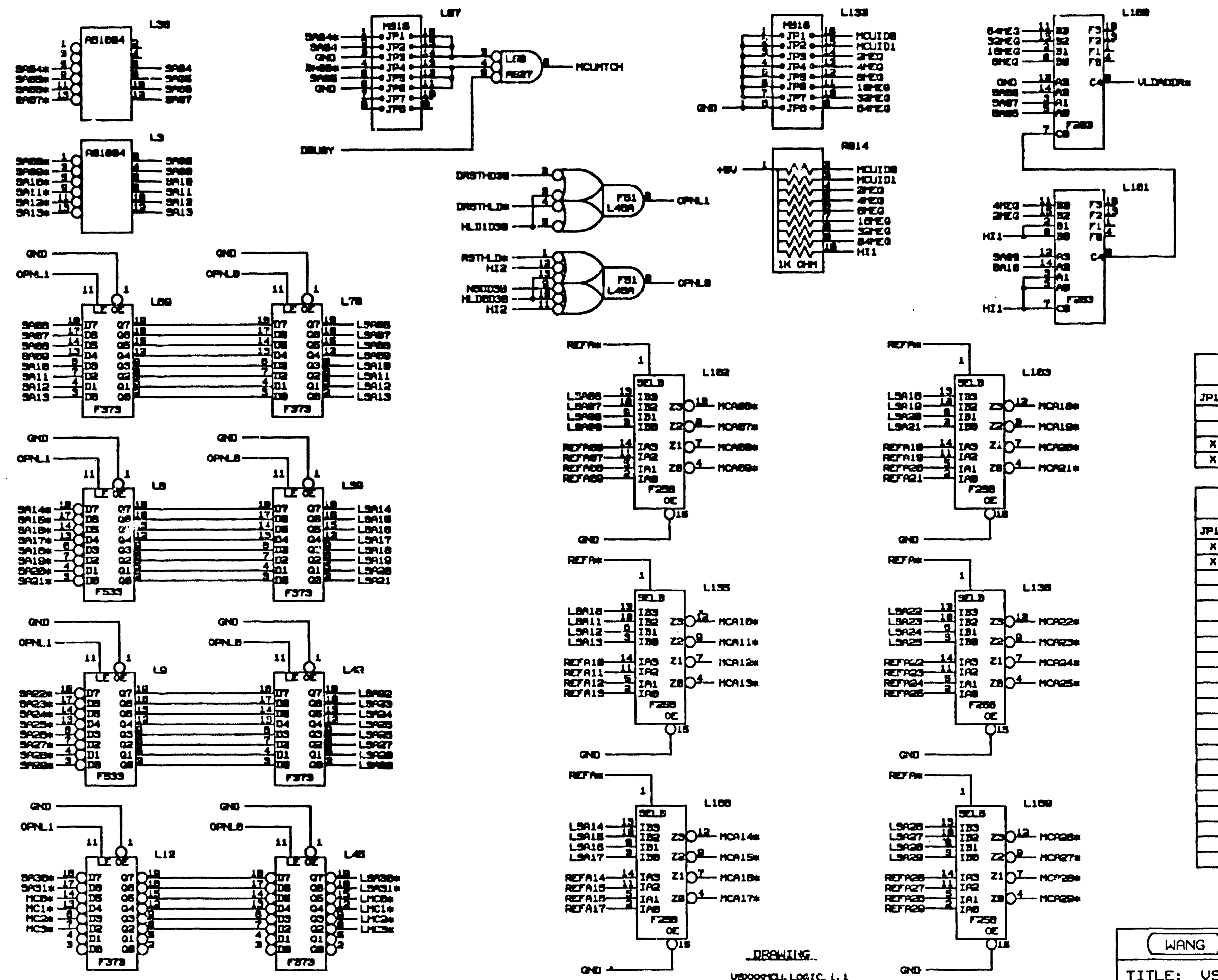
VS-300 MCU INDEX

DRAWING

VSXXXMCU.IDX.1.1
INDEX PAGE

LAST_MODIFIED=Thu Jul 11 11:16:31 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 0 OF 16



REVISIONS

REV	DESCRIPTION	APP. BY	DATE
1	ECO # 36620		7/3/85
2	ECO # 36950		7/8/85
3	ECO # 37074		7/18/85
4	ECO # 37493		8/2/85

L67 JUMPER CONFIGURATION

JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8	
	X			X				MCUID 00
	X		X					MCUID 01
X				X				MCUID 10
X			X					MCUID 11

L133 JUMPER CONFIGURATION

JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8	
X	X							MCUID 00
X								MCUID 01
	X							MCUID 10
								MCUID 11
			X					MAX MEMORY = 4 MEG
				X				MAX MEMORY = 8 MEG
			X	X				MAX MEMORY = 12 MEG
					X			MAX MEMORY = 16 MEG
			X		X			MAX MEMORY = 20 MEG
				X	X			MAX MEMORY = 24 MEG
			X	X	X			MAX MEMORY = 28 MEG
						X		MAX MEMORY = 32 MEG
			X			X		MAX MEMORY = 36 MEG
				X		X		MAX MEMORY = 40 MEG
			X	X		X		MAX MEMORY = 44 MEG
					X	X		MAX MEMORY = 48 MEG
			X		X	X		MAX MEMORY = 52 MEG
				X	X	X		MAX MEMORY = 56 MEG
			X	X	X	X		MAX MEMORY = 60 MEG
							X	MAX MEMORY = 64 MEG

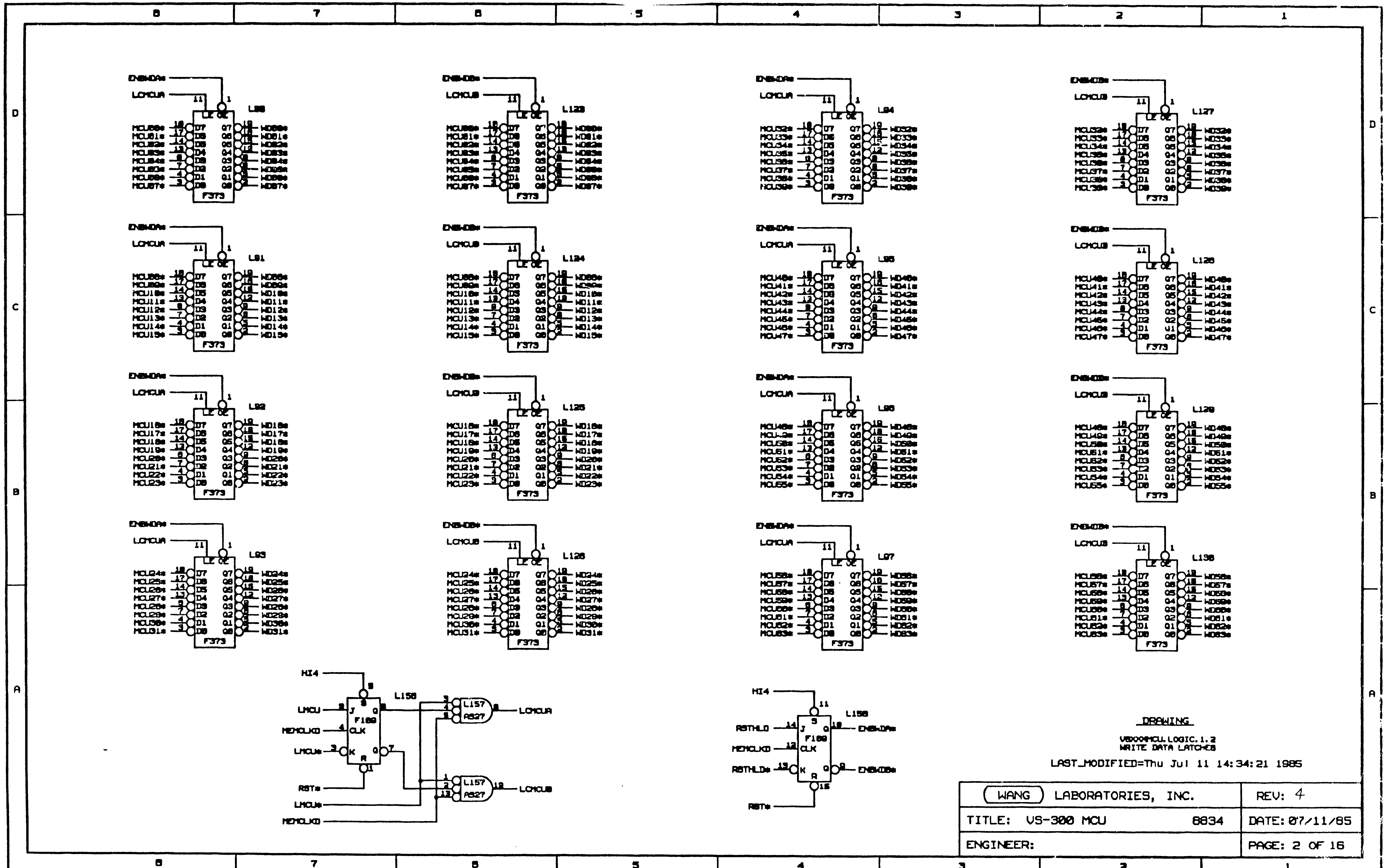
X = JUMPER WIRE IN

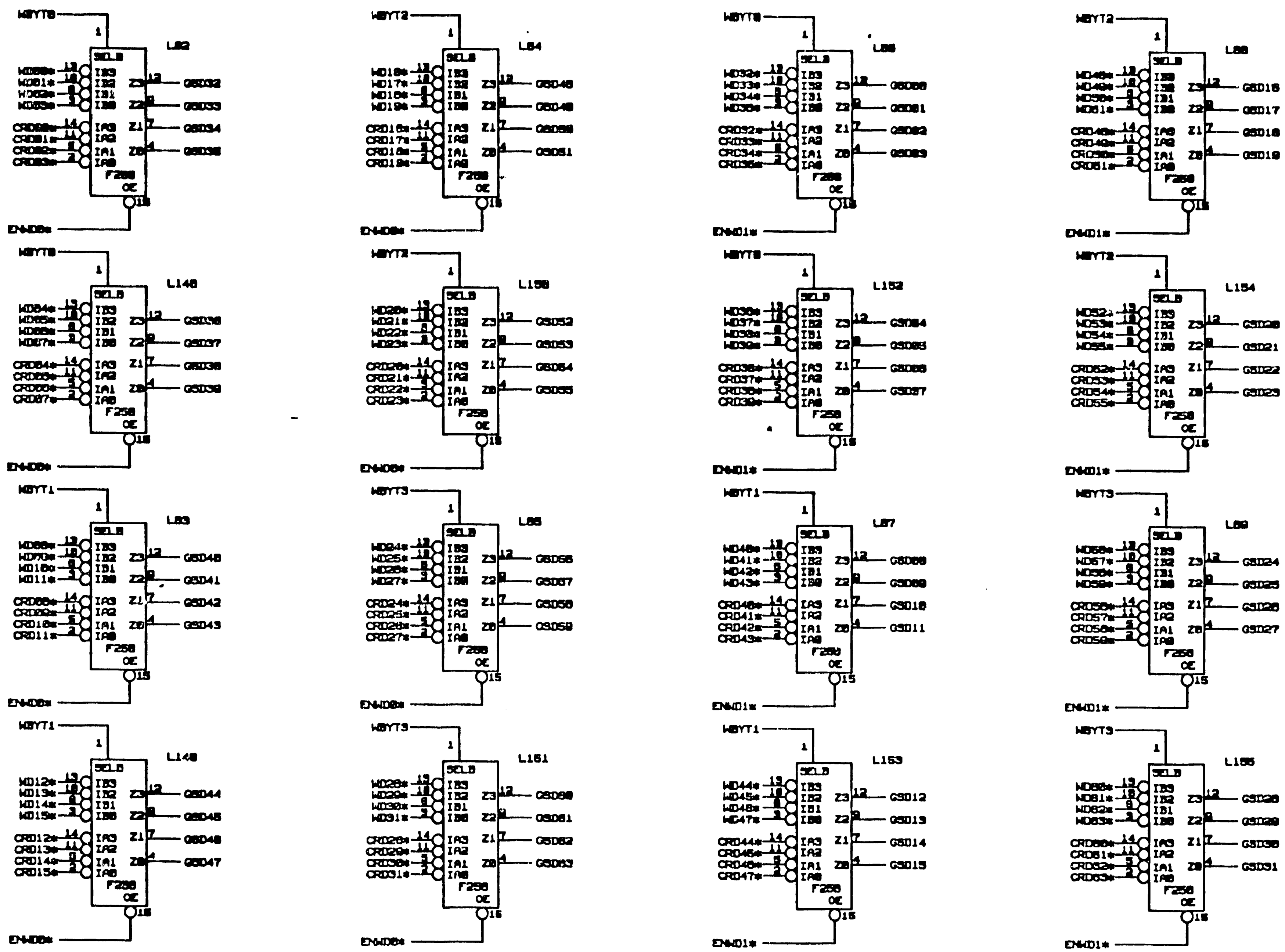
E-REV 4

DRAWING
VS300MCU.LOGIC.1.1
MEMORY CONTROLLER ADDRESS

LAST_MODIFIED=Thu Jul 11 14:31:25 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER: E. MANN	PAGE: 1 OF 16


DRAWING
VSXXXMCU.LOGIC.1.2
WRITE DATA LATCHES
LAST_MODIFIED=Thu Jul 11 14:34:21 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 MCU
8834
DATE: 07/11/85
ENGINEER:
PAGE: 2 OF 16

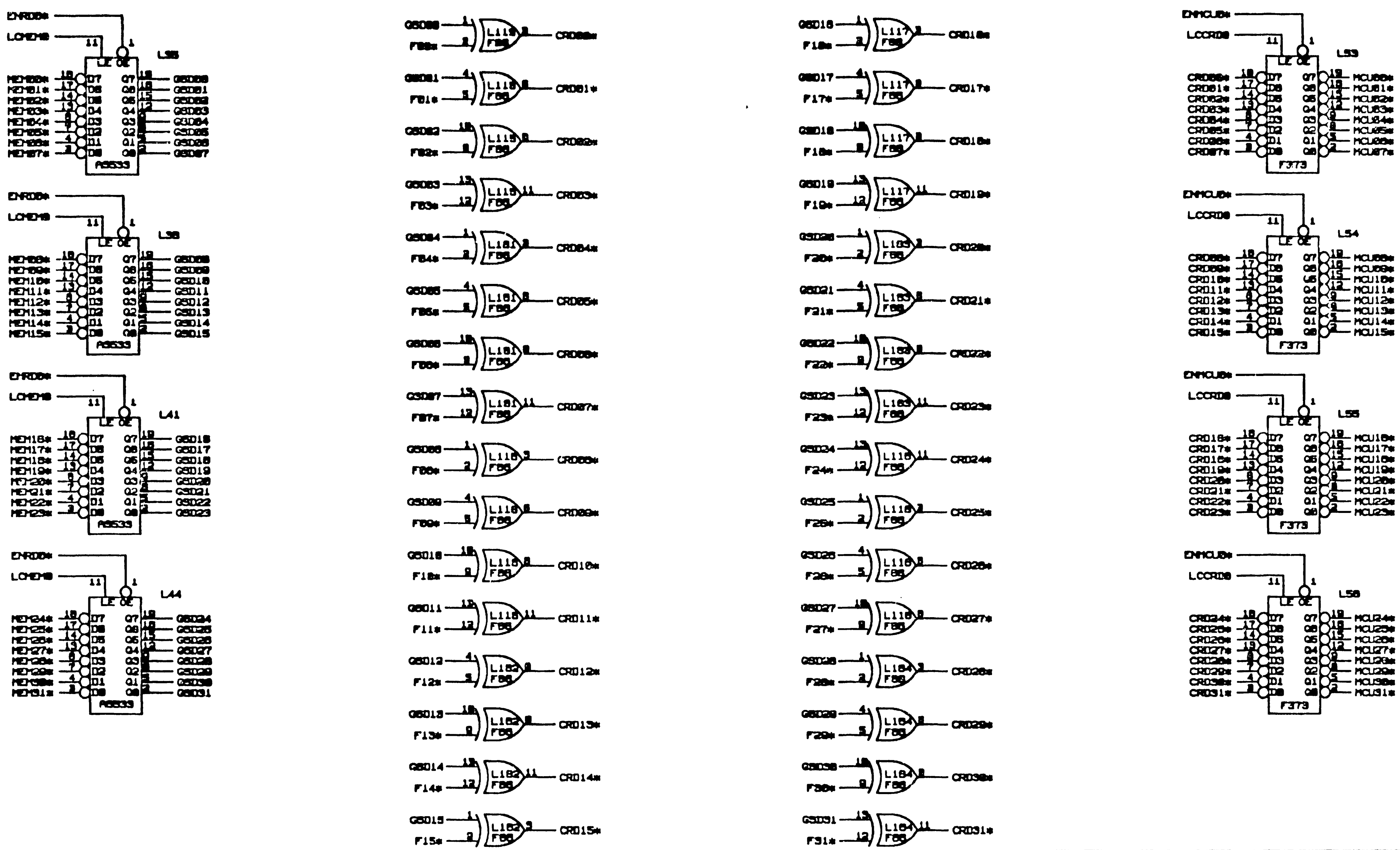


DRAWING

VSXXXMCU.LOGIC.1.3
WRITE DATA MULTIPLEXER

LAST_MODIFIED=Thu Jul 11 14:38:38 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 3 OF 16

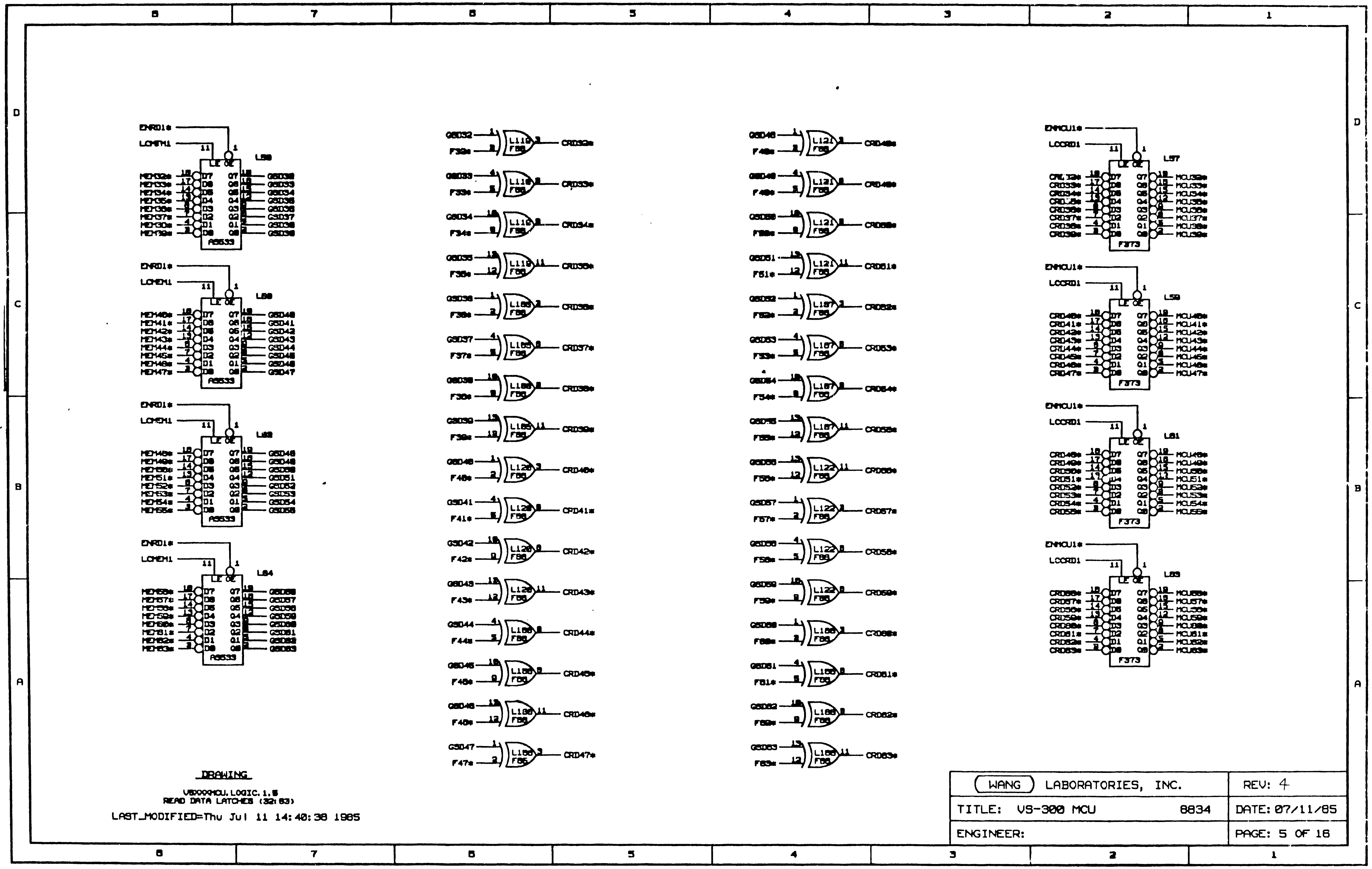


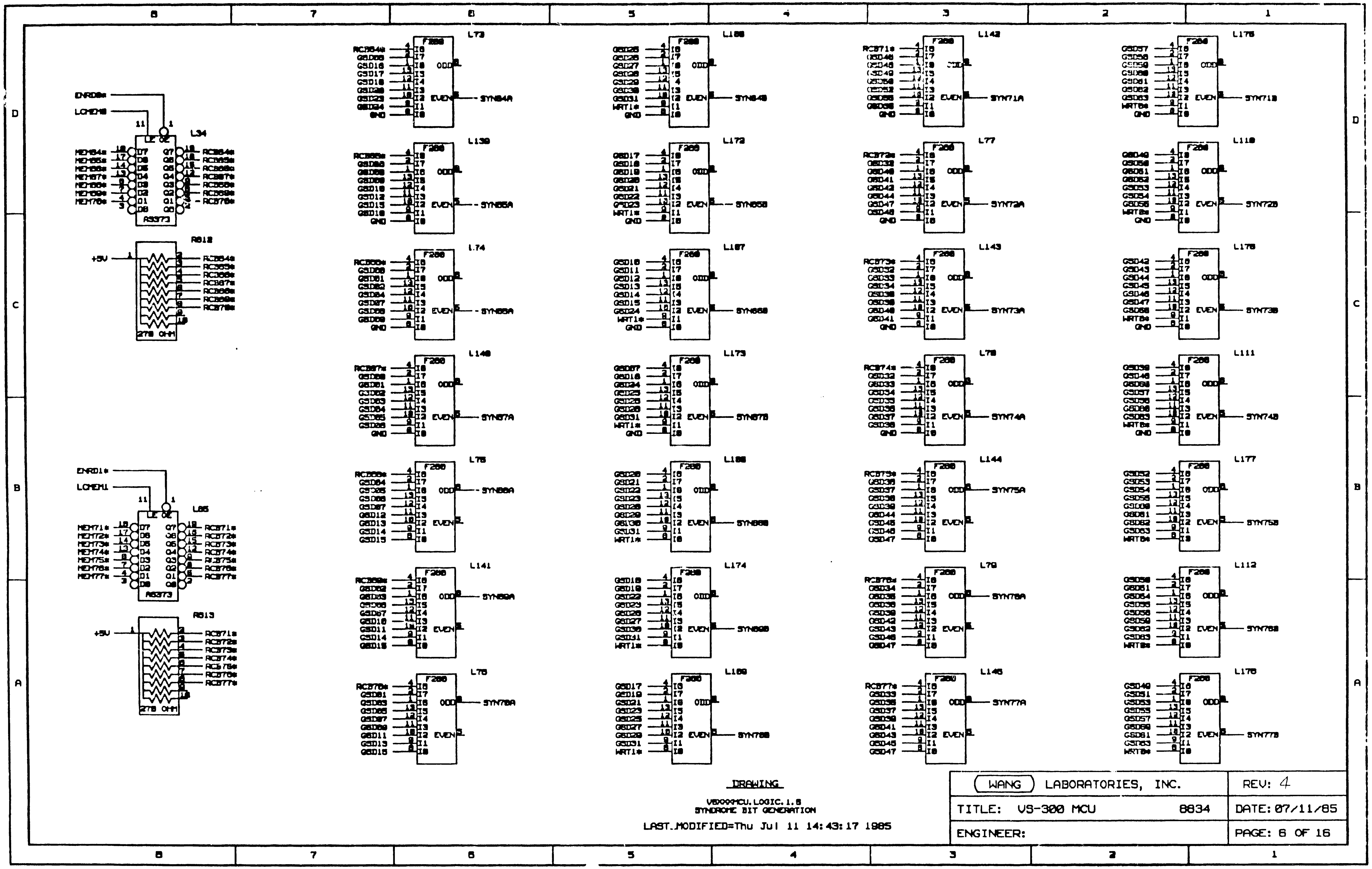
DRAWING

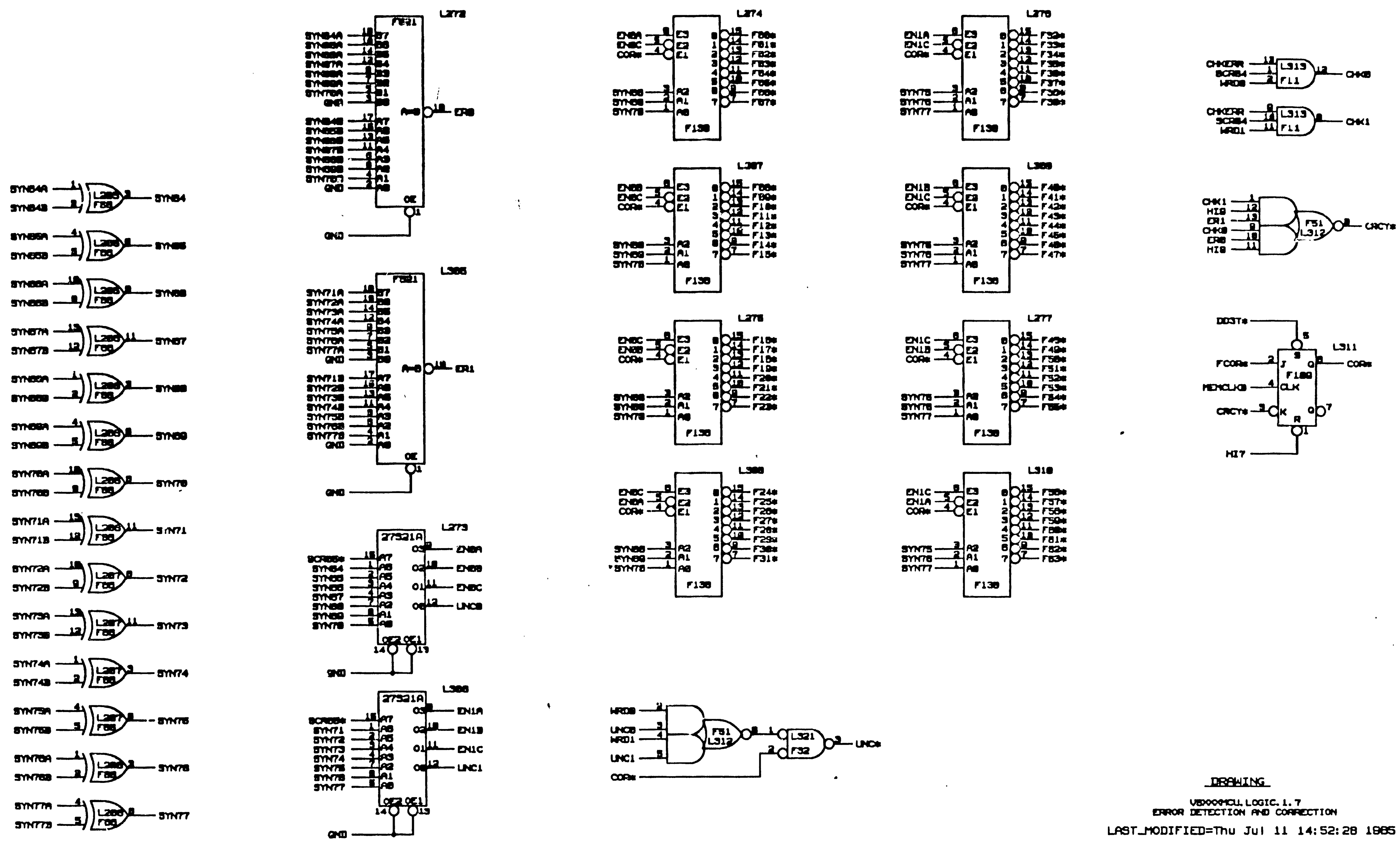
VSXXXMCU.LOGIC.1.4
READ DATA LATCHES (00:31)

LAST_MODIFIED=Thu Jul 11 14:38:34 1985

(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 4 OF 16


DRAWING
READ DATA LATCHES (32:63)
LAST_MODIFIED=Thu Jul 11 14:40:38 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 MCU
8834
DATE: 07/11/85
ENGINEER:
PAGE: 5 OF 16


DRAWING
VSXXXMCU.LOGIC.1.8
SYNDROME BIT GENERATION
LAST.MODIFIED=Thu Jul 11 14:43:17 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 MCU
8834
DATE: 07/11/85
ENGINEER:
PAGE: 6 OF 16

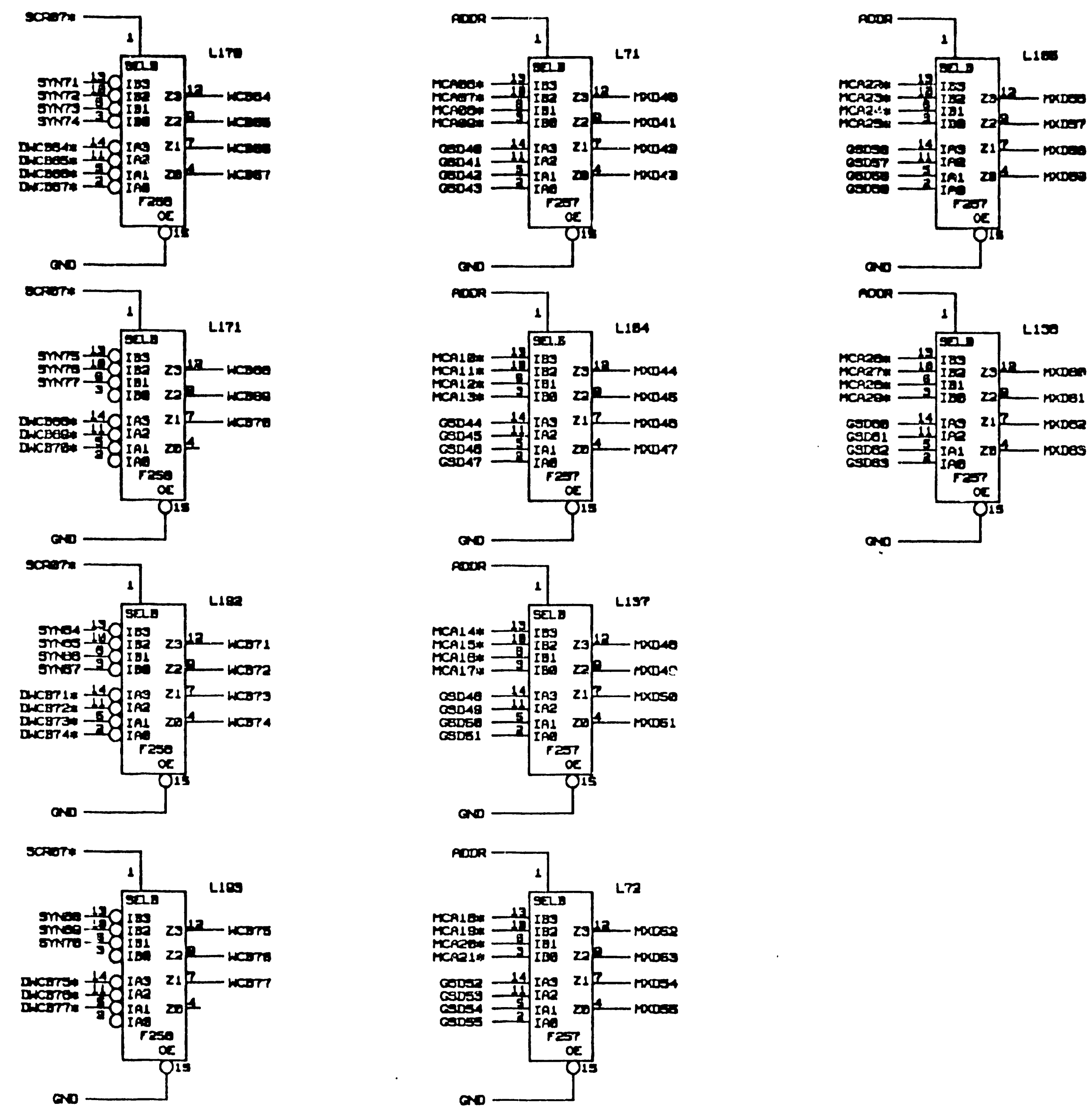


DRAWING

VS000MCU.LOGIC.1.7
ERROR DETECTION AND CORRECTION

LAST_MODIFIED=Thu Jul 11 14:52:28 1985

(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 7 OF 16

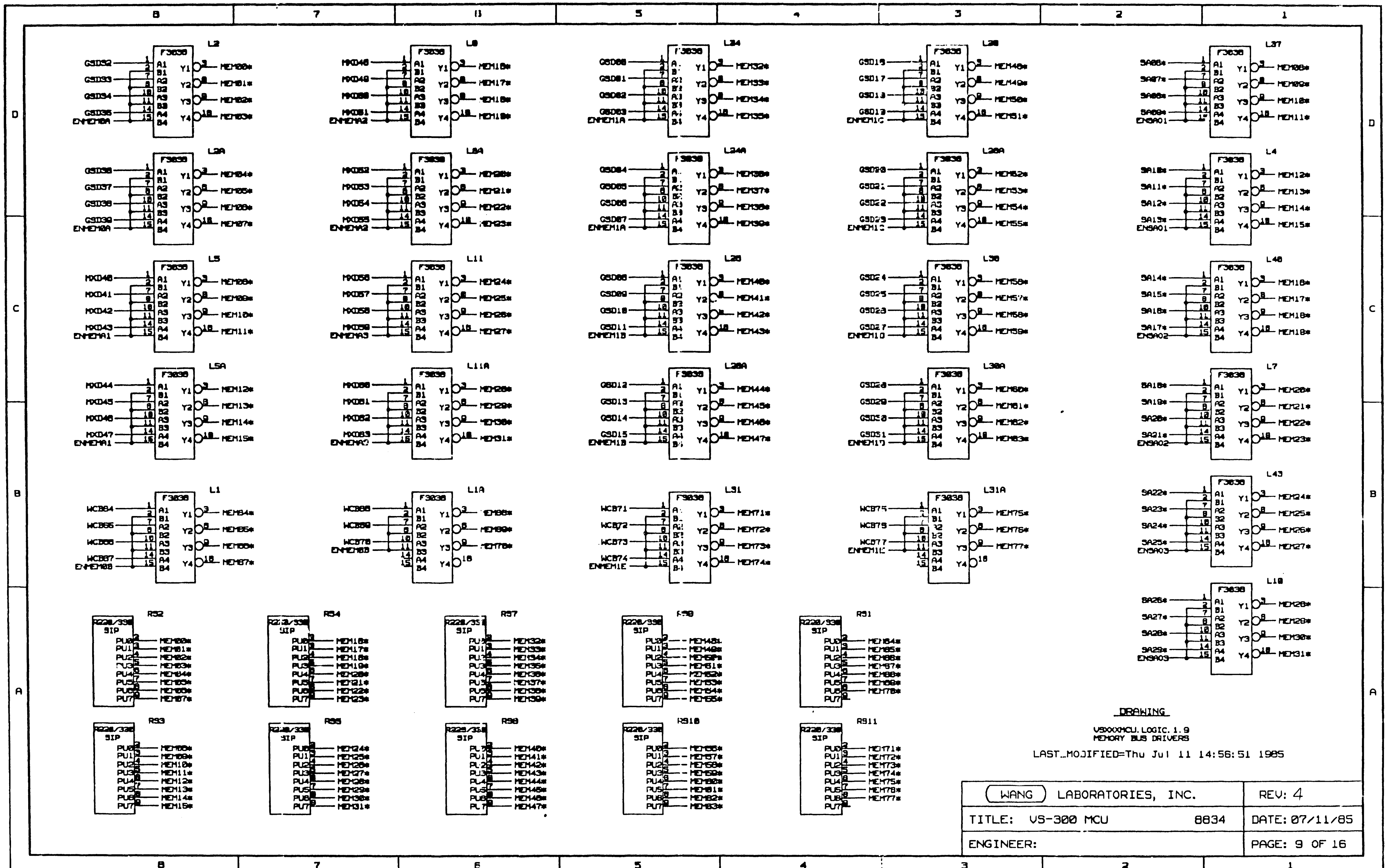


DRAWING

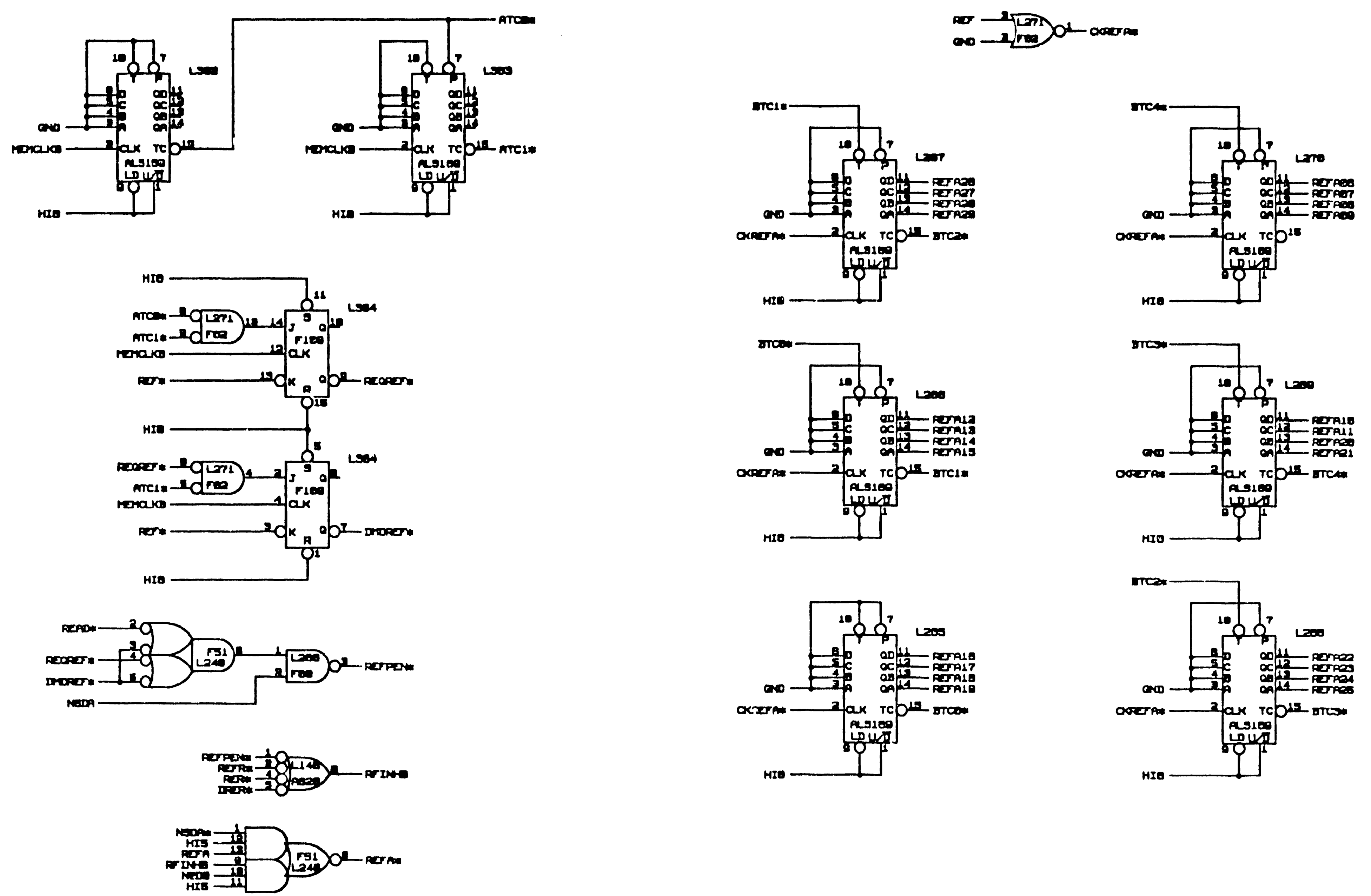
VSXXXMCU.LOGIC.1.8
HCB MUX
MXD MUX

LAST_MODIFIED=Thu Jul 11 14:54:31 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 8 OF 16



DRAWING
VSXXXMCU.LOGIC.1.9
MEMORY BUS DRIVERS
LAST_MODIFIED=Thu Jul 11 14:56:51 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 MCU
8834
DATE: 07/11/85
ENGINEER:
PAGE: 9 OF 16

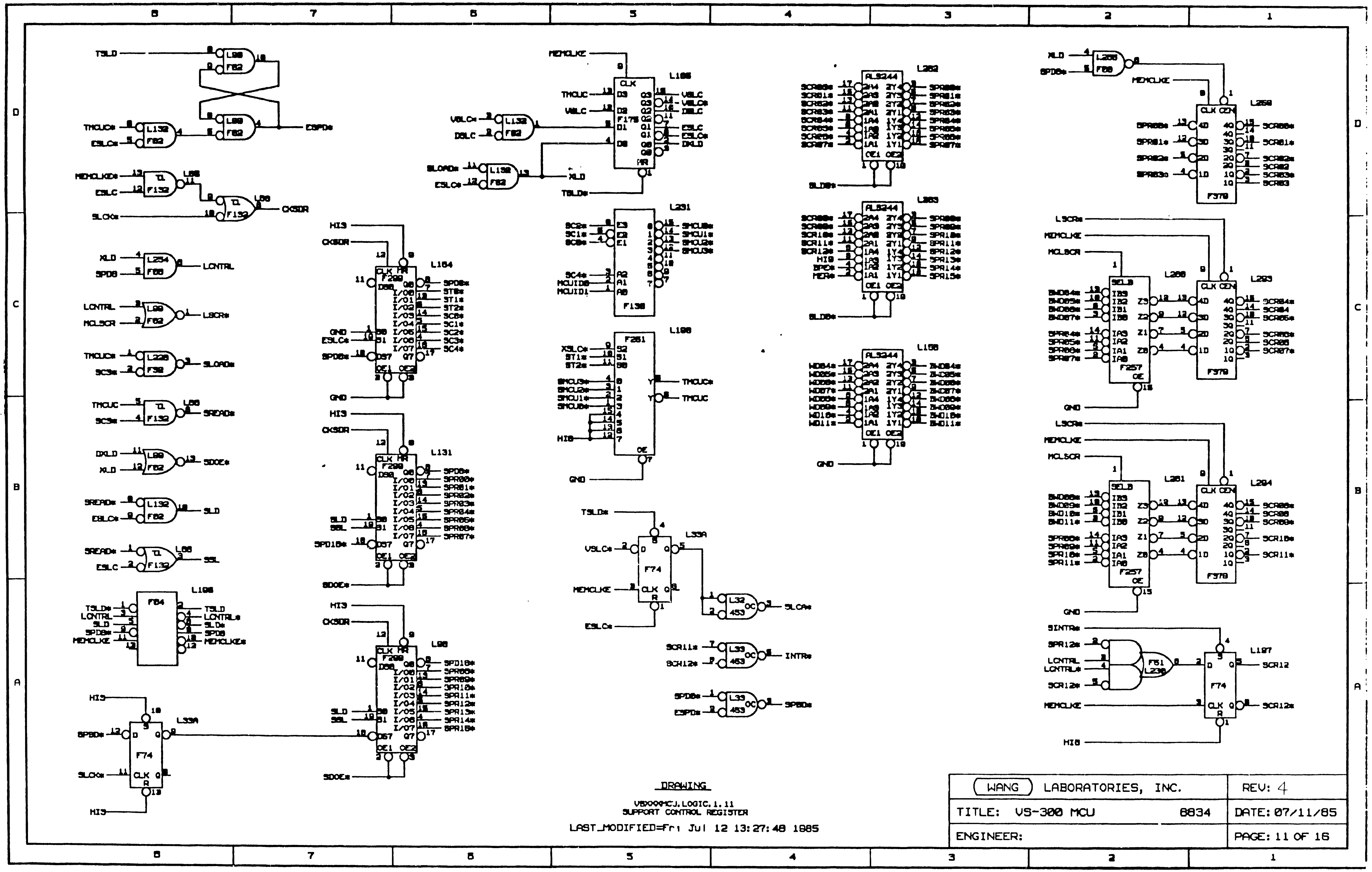


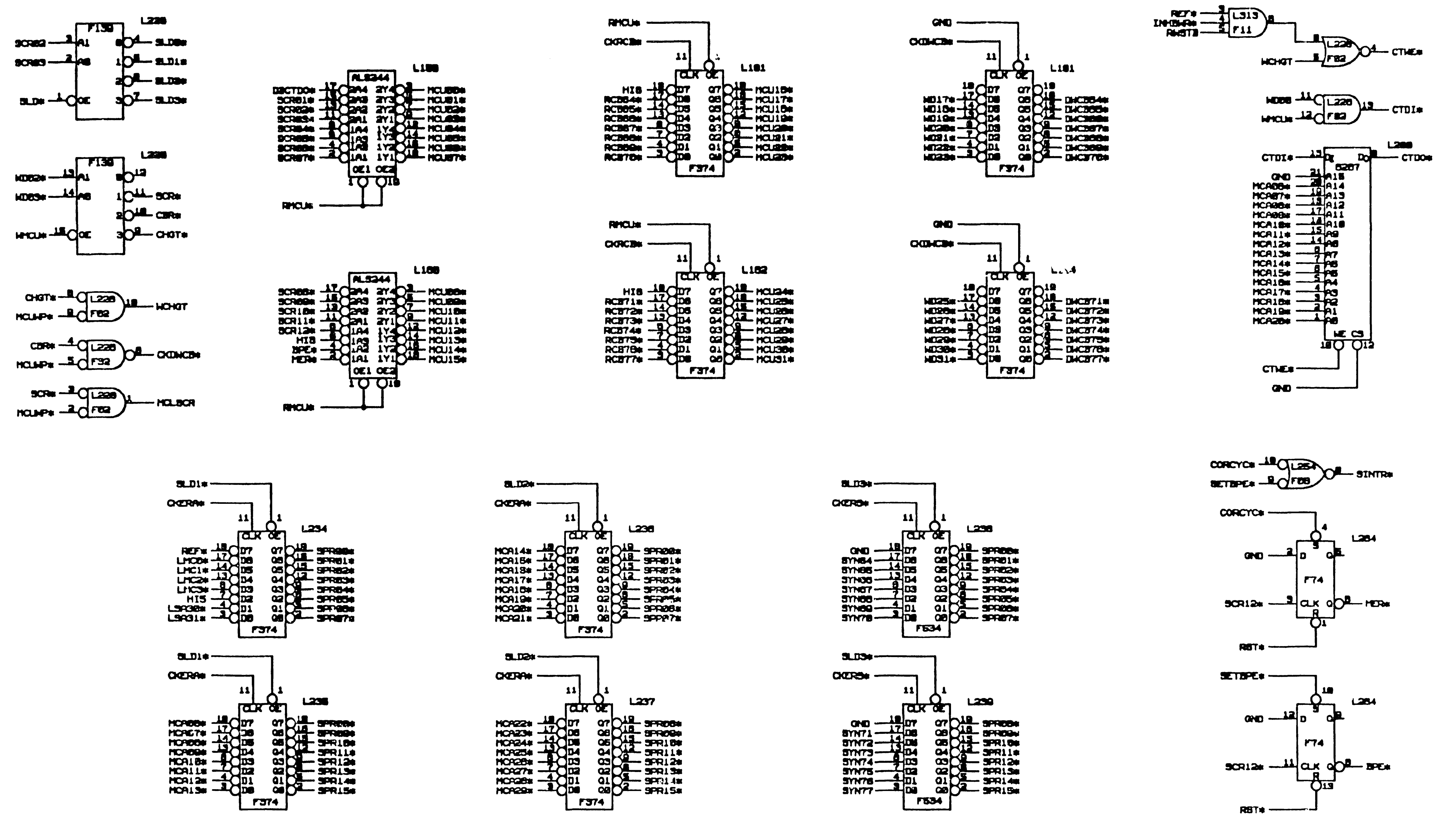
DRAWING

VSXXXMCU.LOGIC.1.10
REFRESH ADDRESS COUNTER

LAST_MODIFIED=Thu Jul 11 15:15:18 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 10 OF 18


DRAWING
VS300MCJ.LOGIC.1.11
SUPPORT CONTROL REGISTER
LAST_MODIFIED=Fri Jul 12 13:27:48 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 MCU
8834
DATE: 07/11/85
ENGINEER:
PAGE: 11 OF 16

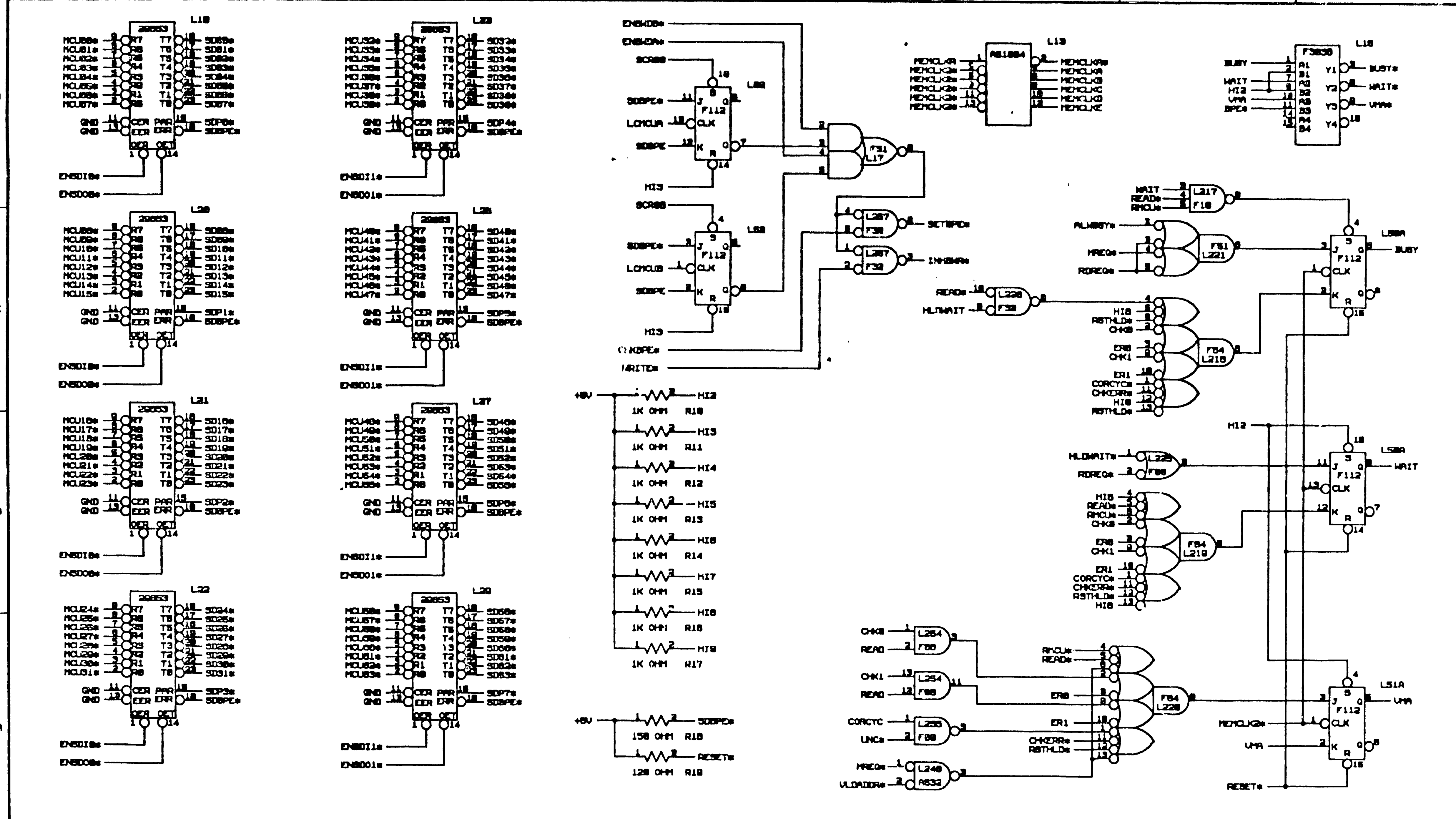


DRAWING

VSXXXMCU.LOGIC.1.12
CHANGE TABLE
ERROR LOG
WR/RD CHKBIT REGR

LAST_MODIFIED=Thu Jul 11 18:19:28 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 12 OF 16

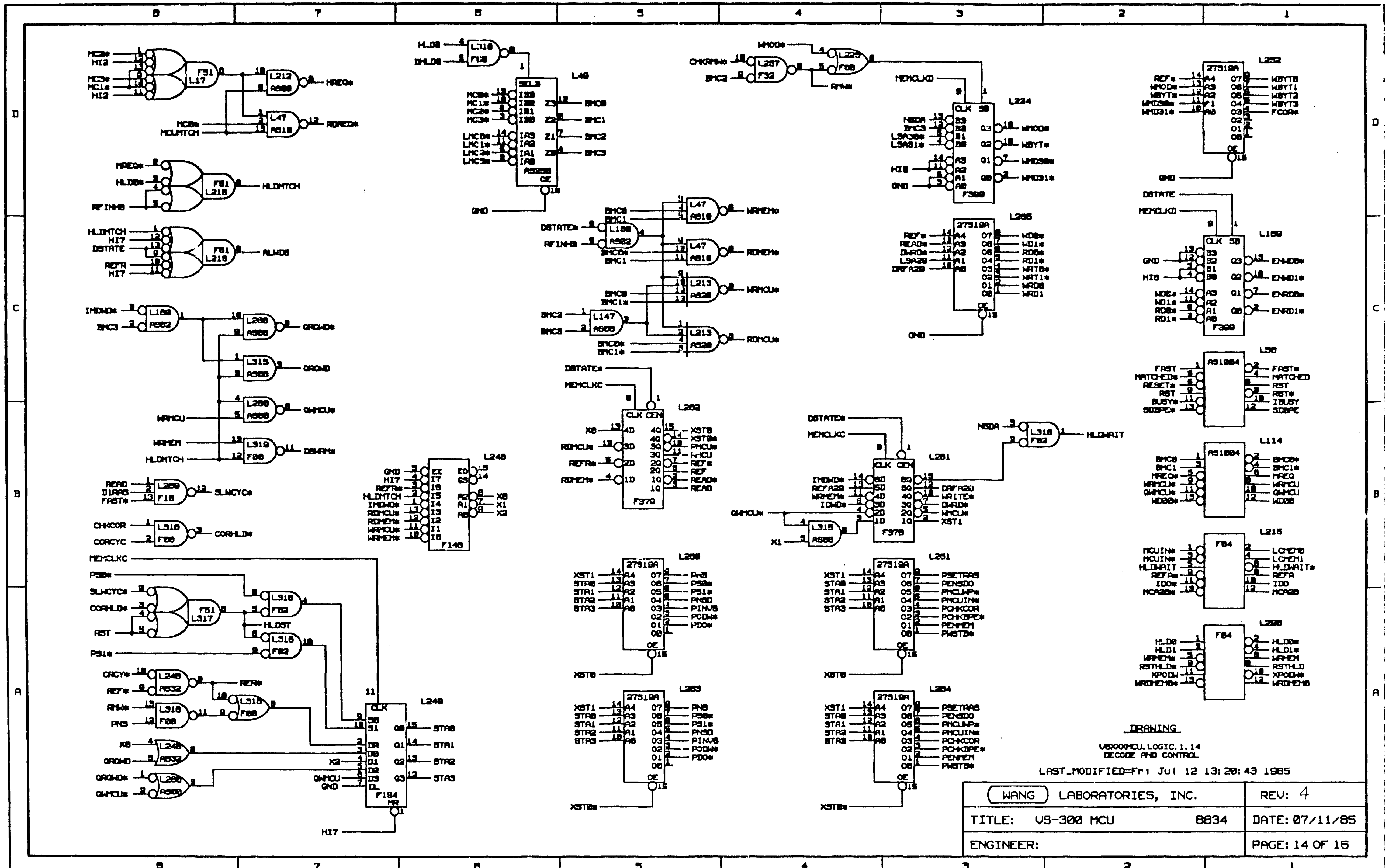


DRAWING

VS000MCU.LOGIC.1.13
SYSTEM DATA BUS TRANSCEIVERS

LAST_MODIFIED=Fri Jul 12 13:42:08 1985

(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 13 OF 16

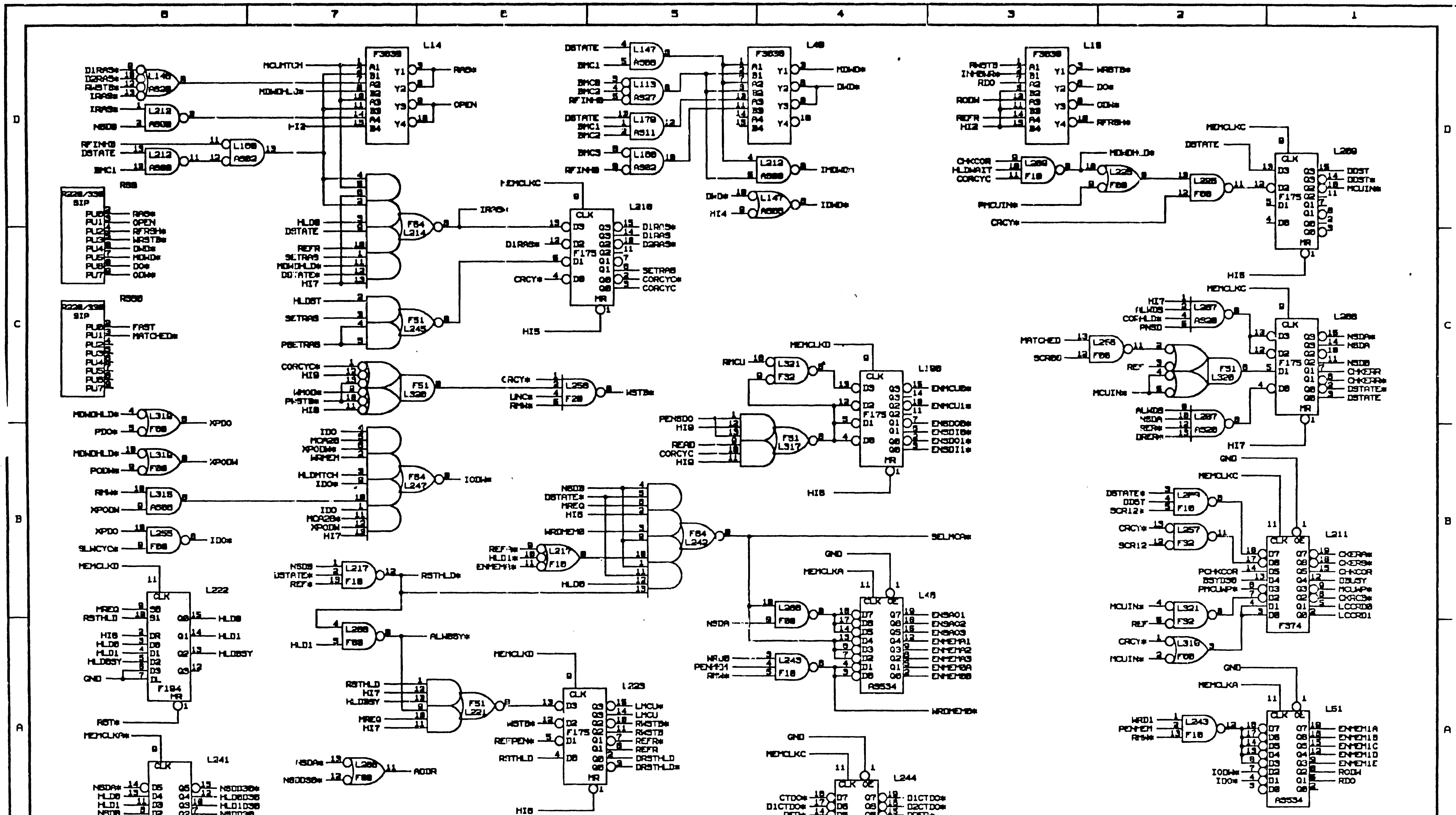


DRAWING

VS000MCU.LOGIC.1.14
DECODE AND CONTROL

LAST_MODIFIED=Fri Jul 12 13:20:43 1985

WANG LABORATORIES, INC.		REV: 4
TITLE: VS-300 MCU	8834	DATE: 07/11/85
ENGINEER:		PAGE: 14 OF 16

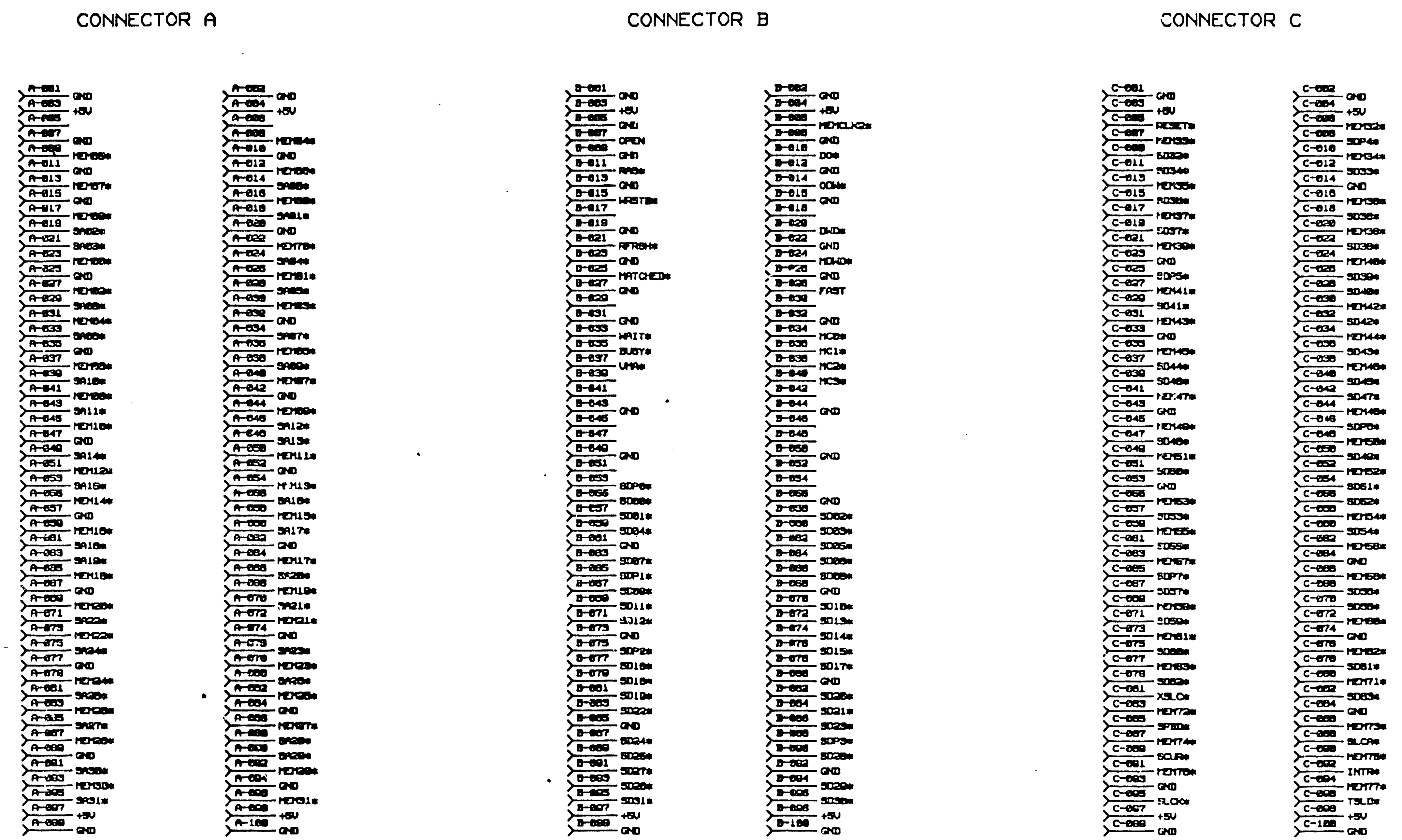


DRAWING

VSXXXMCU.LOGIC.1.16
MEMORY AND REGISTERED CONTROL

LAST_MODIFIED=Fri Jul 12 13:15:55 1985

(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 15 OF 16

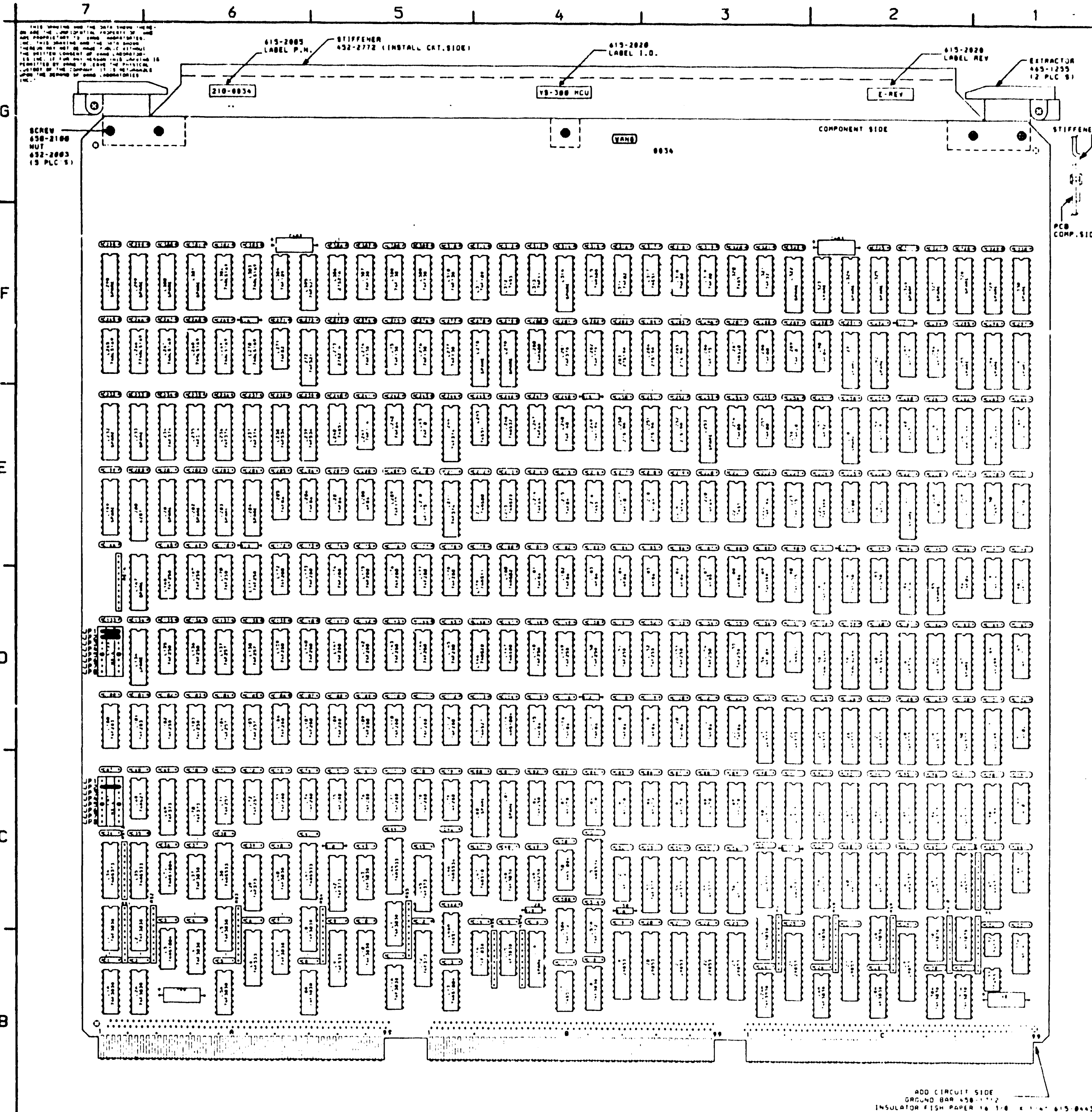


DRAWING

VS300MCU.LOGIC.1.16
FINGER CONNECTIONS

LAST_MODIFIED=Fri Jul 12 09:31:35 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 MCU 8834	DATE: 07/11/85
ENGINEER:	PAGE: 16 OF 16



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
CAPAITIORS C400-403 ARE 47UF/20V WPN.300-4034.
RESISTORS ARE EXPRESSED IN OHMS.
RESISTORS R10-17 ARE 1K WPN.330-3011.
RESISTORS RS1-11.50 ARE 220/330 WPN.333-0007 LOAD PIN 1 TOWARDS BOTTOM OF BOARD.
RESISTORS RS12.13 ARE 270 WPN.333-0064.
RESISTOR RS14 IS 1K WPN.333-0037.
INSTALL WPN.376-9024 AT LOCATION L67.133.
2. REFERENCE SCHEMATIC PARTS LIST FOR JUMPER
CONFIGURATIONS. JUMPERS ARE WPN 376-9129.

WANG		BY	DATE	APPROVED BY	DATE
		DWN DCT		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS300	E C CONTROL		MFG ENGR	
	10-214	TITLE VS300 MCU			
FINISH		210-8834	C	8834	4

VS-300 SCU

SUPPORT CONTROL UNIT

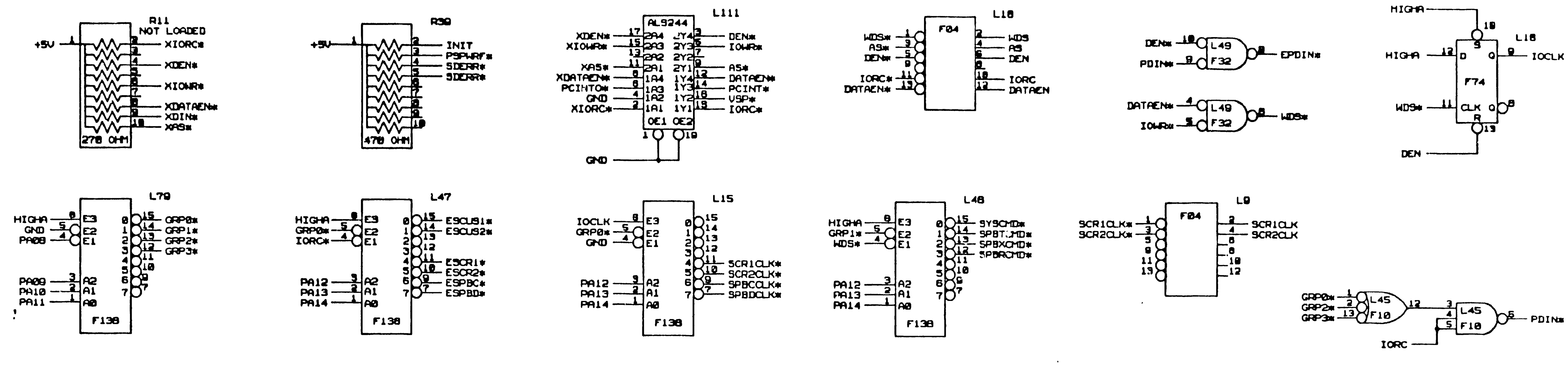
8835 Rev 02

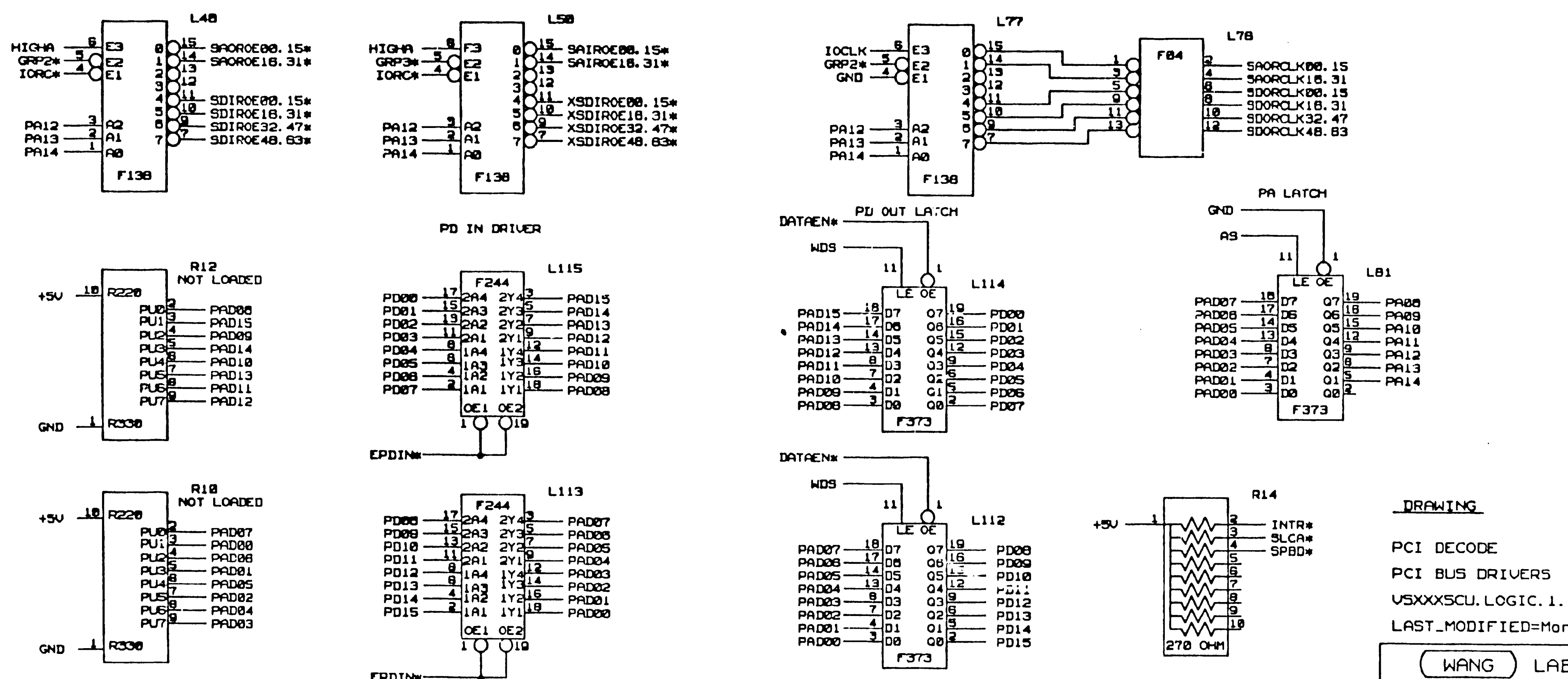
INDEX

DRAWING:
TITLE=VS-300 SCU 8835 R02
ABBREV=SCU
VSXXXSCU.LOGIC.1.1
LAST_MODIFIED=Mon Mar 18 12:07:27 1985

E-REV 1

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835R02	DATE: 2/8/85
ENGINEER:	PAGE: 1 OF 14





SCU ADDRESS DECODE		
HEX	READ	WRITE
00	STATUS 1	-
02	STATUS 2	-
04	-	-
06	-	-
08	CTRL 1	CTRL 1
0A	CTRL 2	CTRL 2
0C	SPB CTRL	SPB CTRL
0E	SPB DATA	SPB DATA
10		SYSCMD
12		SPBTCMD
14		SPBXCMD
16		SPBRCMD
18		-
1A		-
1C		-
1E		-
20	ADDRESS OUT 00.15	ADDRESS OUT 00.15
22	ADDRESS OUT 16.31	ADDRESS OUT 16.31
24	-	-
26	-	-
28	DATA OUT 00.15	DATA OUT 00.15
2A	DATA OUT 16.31	DATA OUT 16.31
2C	DATA OUT 32.47	DATA OUT 32.47
2E	DATA OUT 48.63	DATA OUT 48.63
30	ADDRESS IN 00.15	
32	ADDRESS IN 16.31	
34	-	
36	-	
38	DATA IN 00.15	
3A	DATA IN 16.31	
3C	DATA IN 32.47	
3E	DATA IN 48.63	

DRAWING

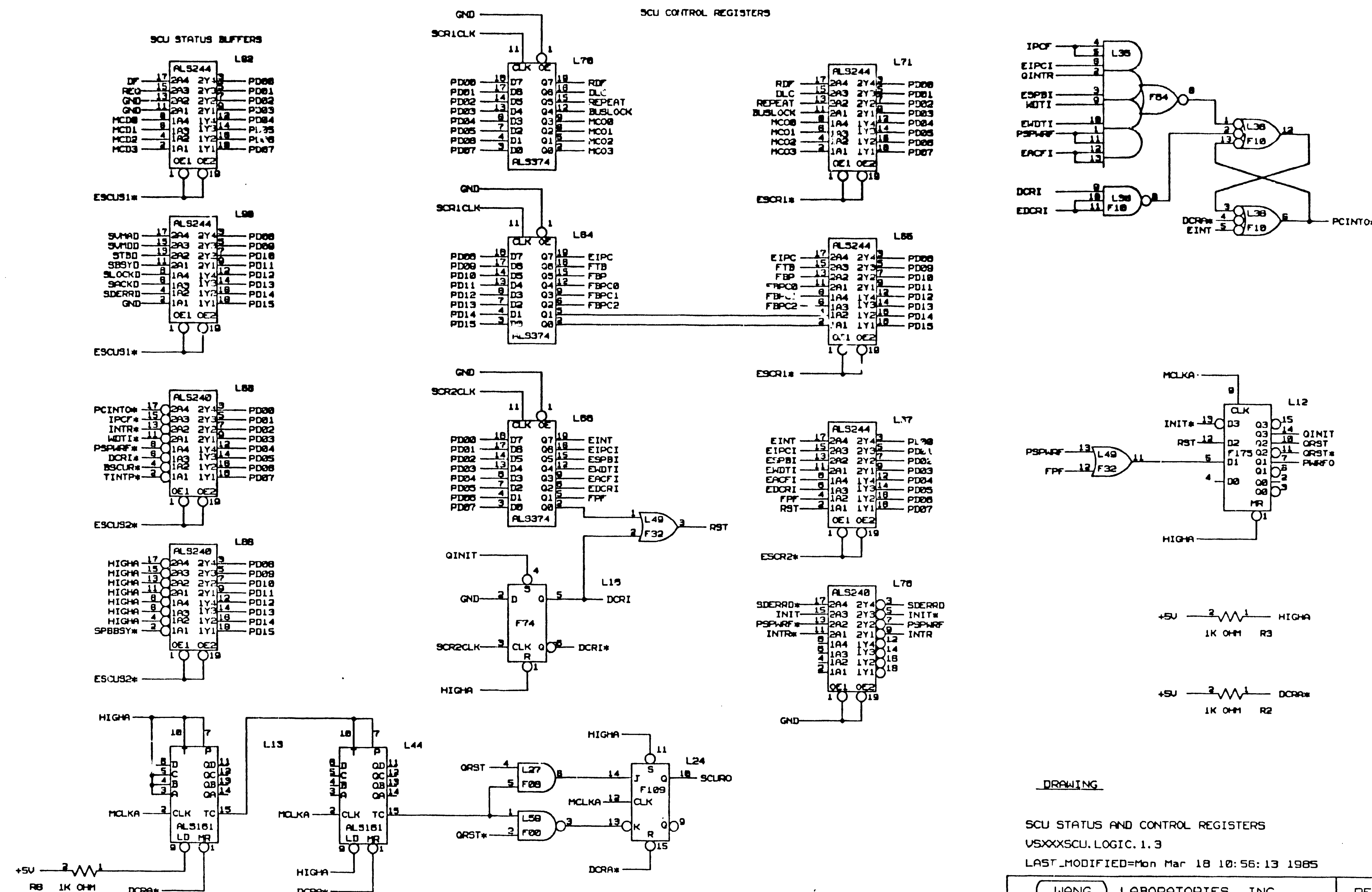
PCI DECODE

PCI BUS DRIVERS

VSXXXSCU.LOGIC.1.2

LAST_MODIFIED=Mon Mar 18 10:54:29 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 2 OF 14



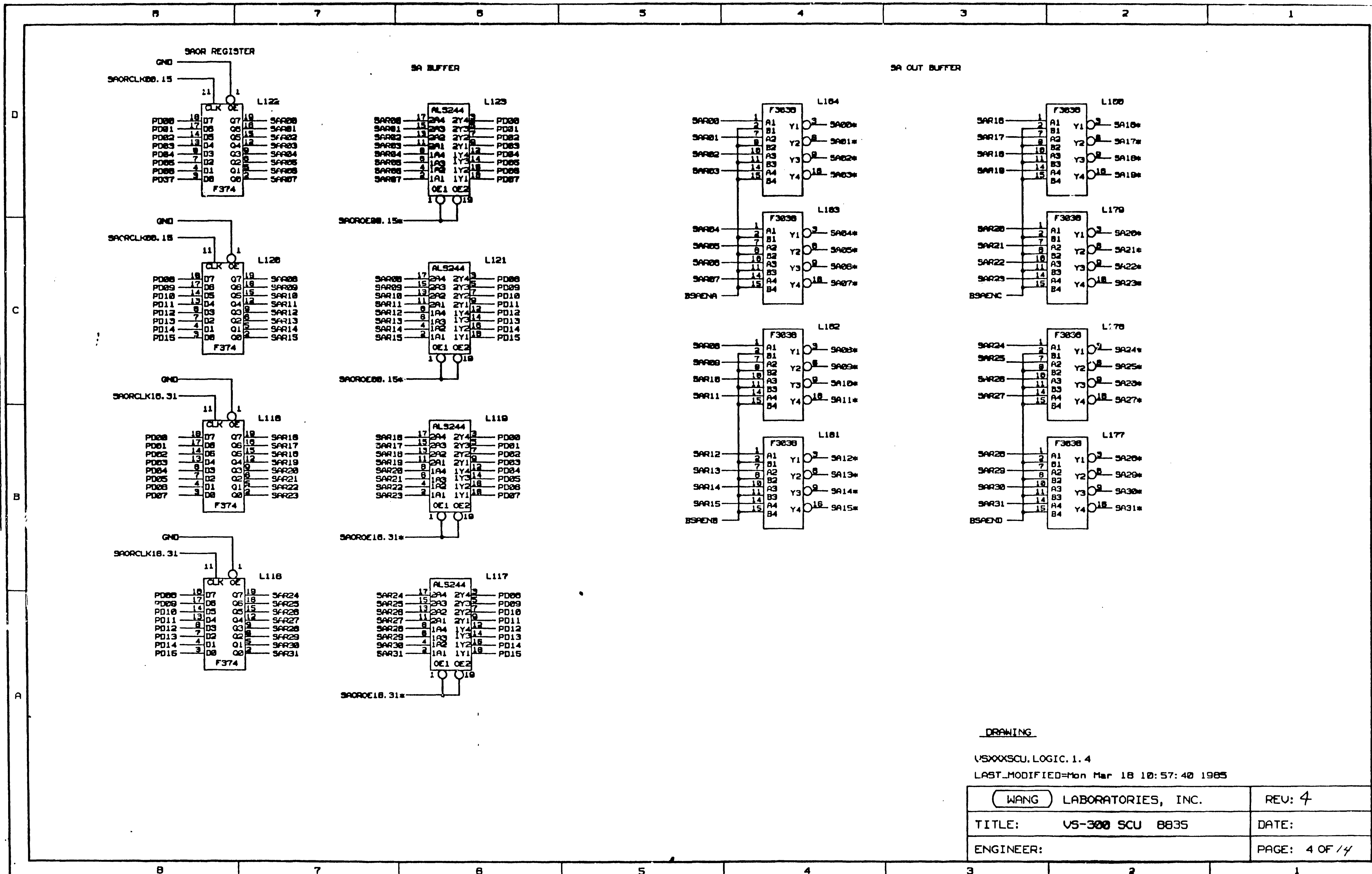
DRAWING

SCU STATUS AND CONTROL REGISTERS

VSXXXSCU.LOGIC.1.3

LAST_MODIFIED=Mon Mar 18 10:56:13 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 3 OF 14

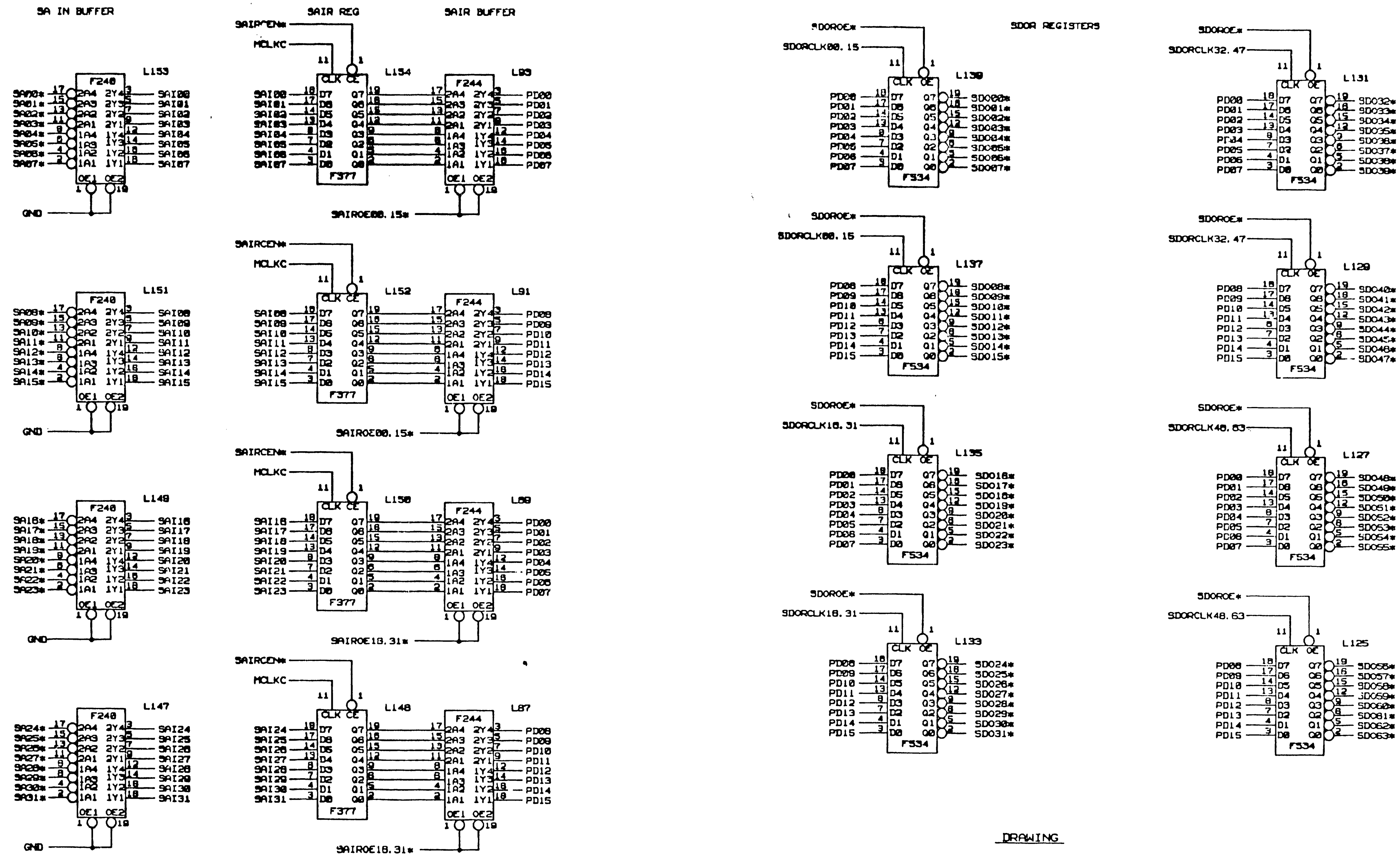


DRAWING

VSXXXSCU.LOGIC.1.4

LAST_MODIFIED=Mon Mar 18 10:57:40 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 4 OF 14



5VDC BYPASS CAPACITORS

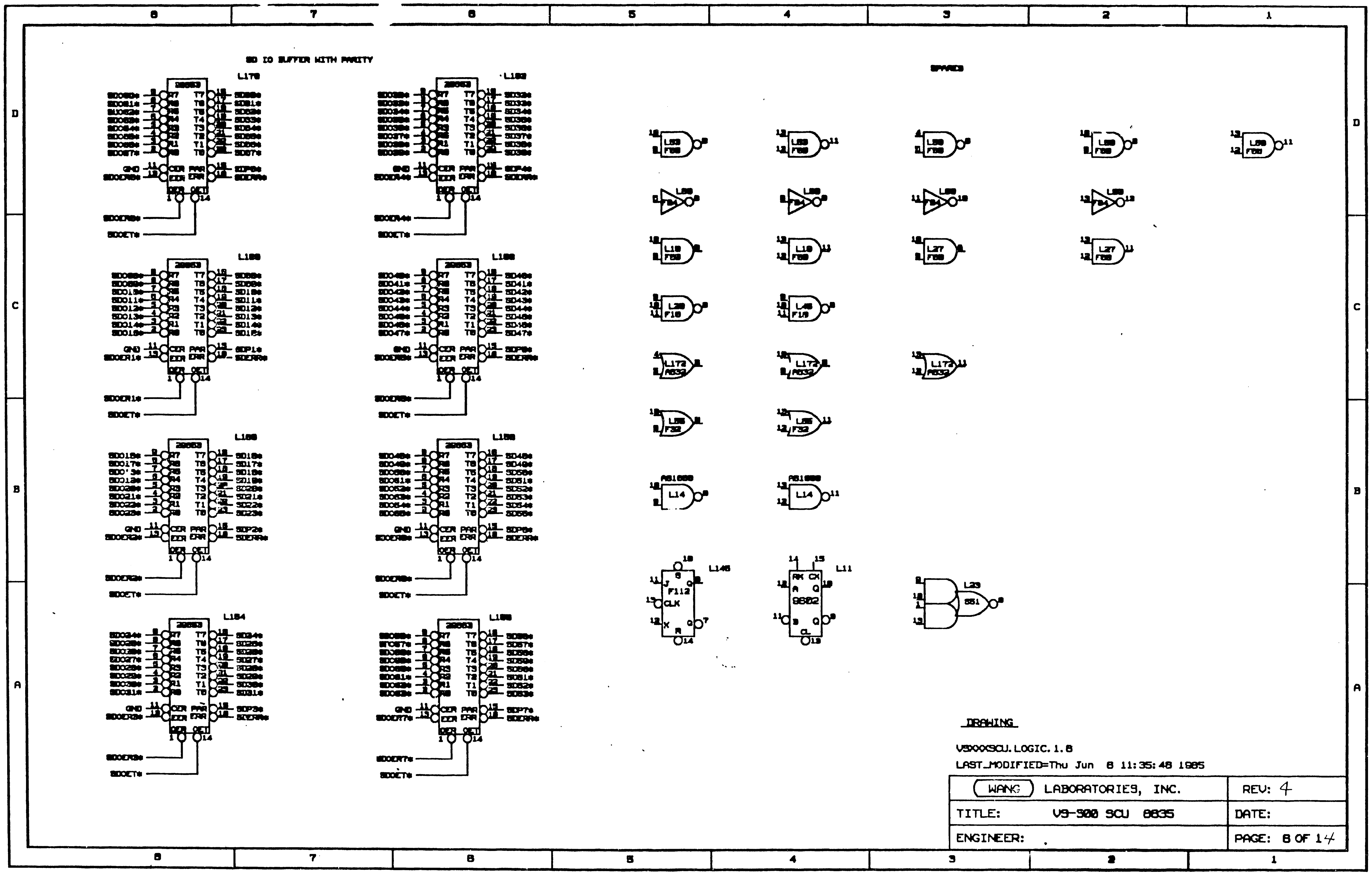
15 MFD, 20 VDC TANTALUM C1,C3,C177,C189
0.047 MFD CERAMIC C4 TO C176, C178 TO C188

DRAWING

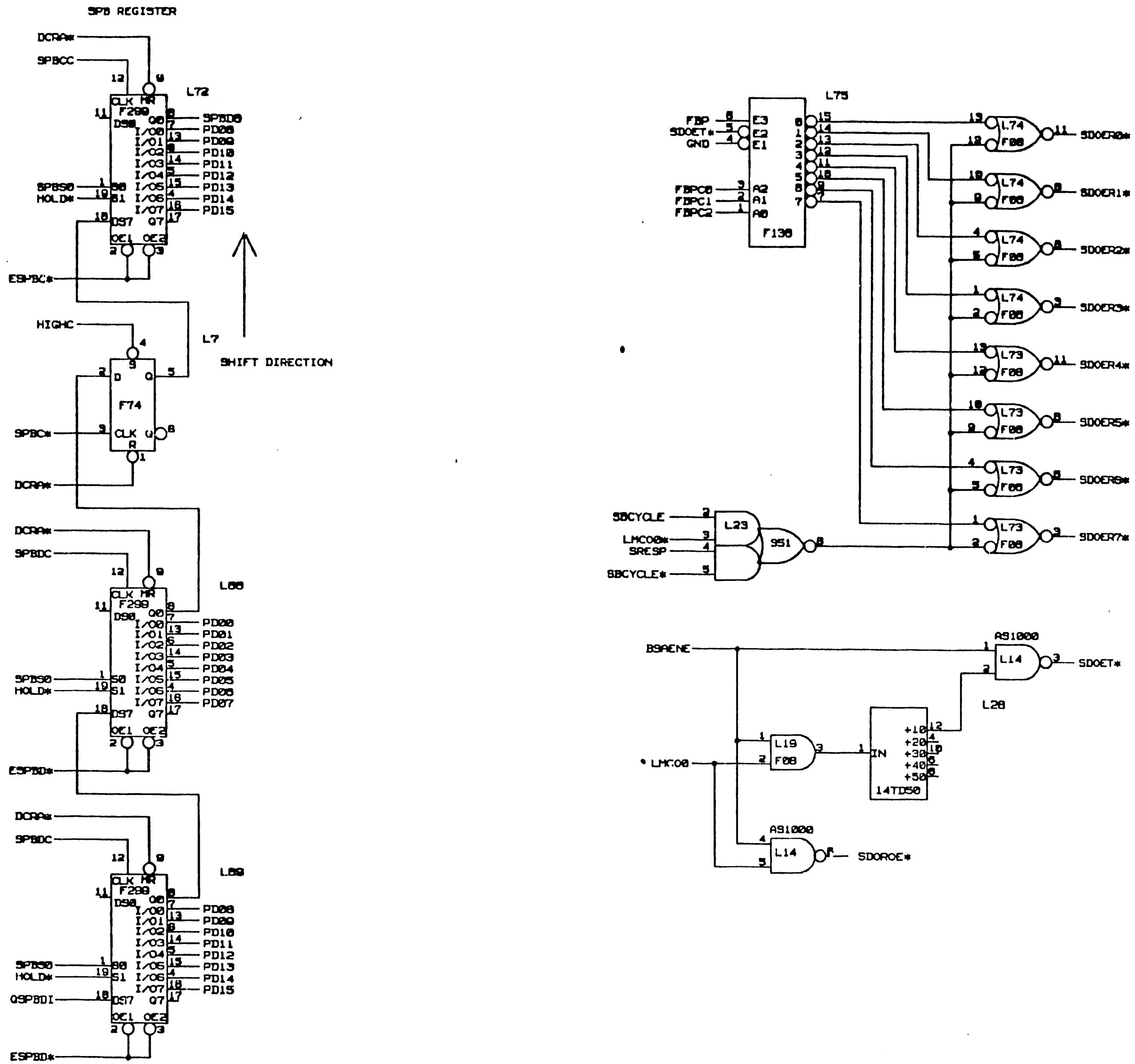
VSXXXSCU.LOGIC.1.5

LAST_MODIFIED=Mon Mar 18 10:59:28 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 5 OF 14

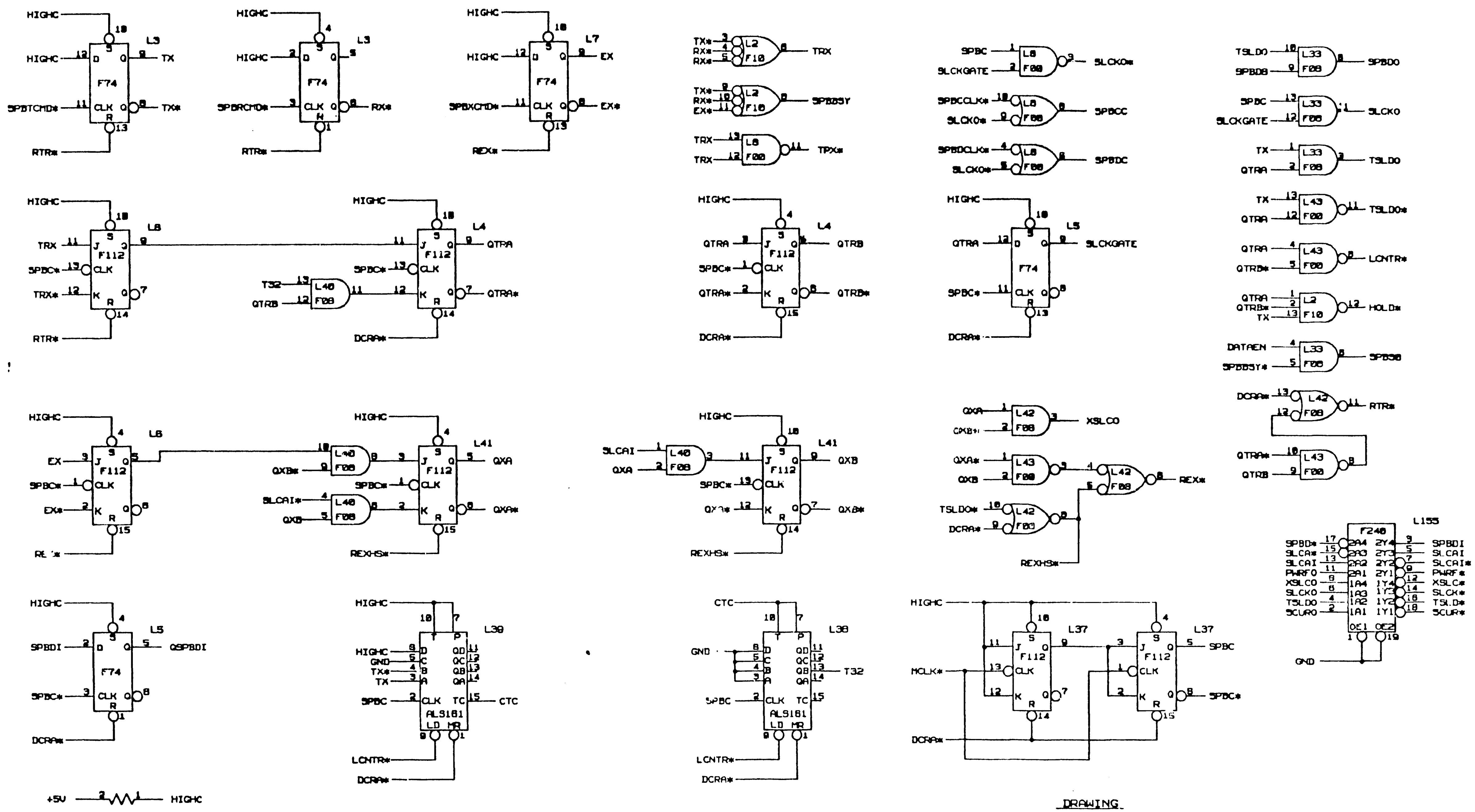


SD IO BUFFER WITH PARITY
SPARES
DRAWING
VSXXXSCU.LOGIC.1.8
LAST_MODIFIED=Thu Jun 6 11:35:48 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 SCU 8835
DATE:
ENGINEER:
PAGE: 8 OF 14



DRAWING
SDO BUS CONTROL
SPB INTERFACE
VSXXXSCU.LOGIC.1.7
LAST_MODIFIED=Mon Mar 18 11:03:00 1985

(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 7 OF 14



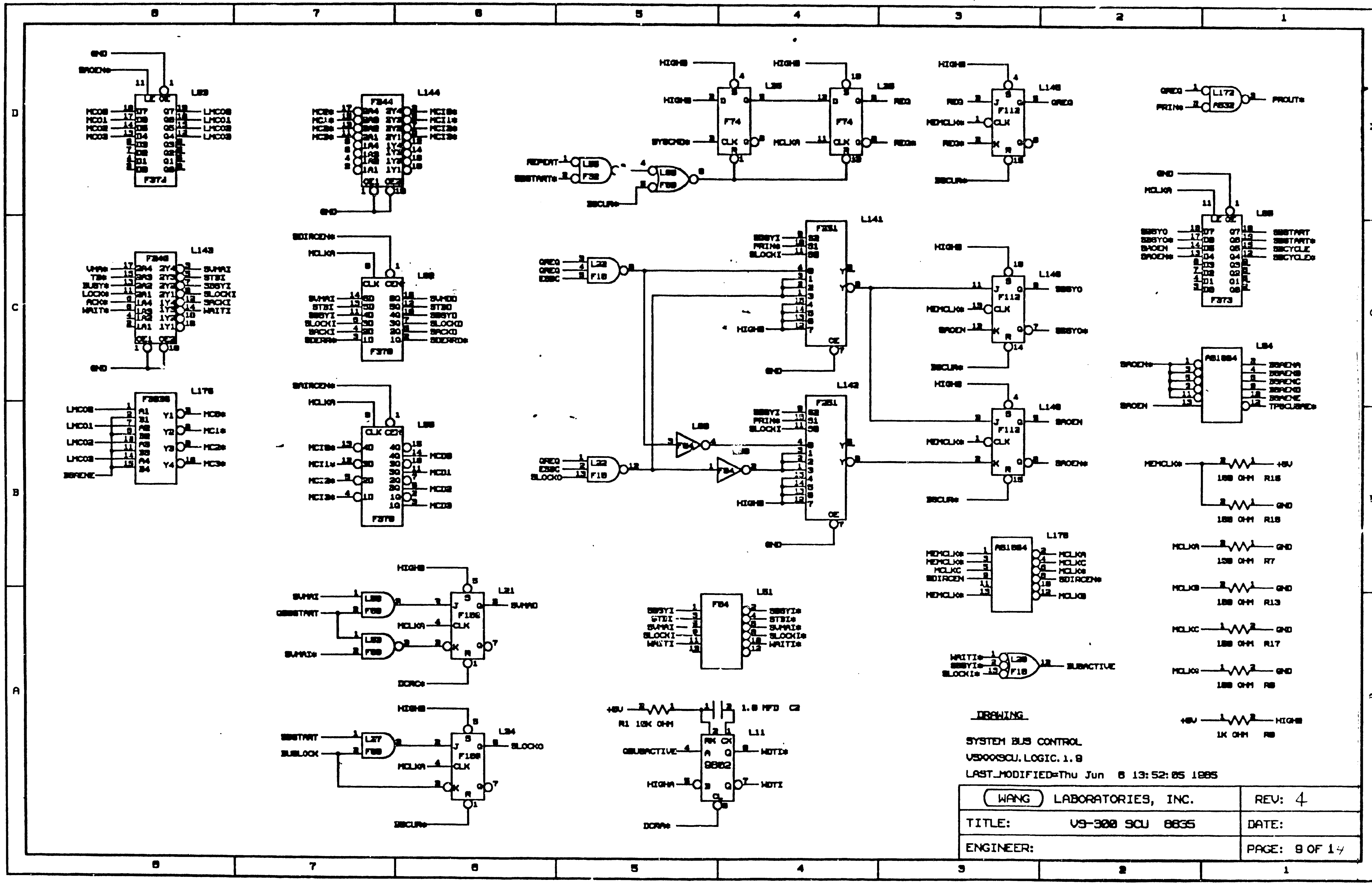
DRAWING

SPB CONTROL

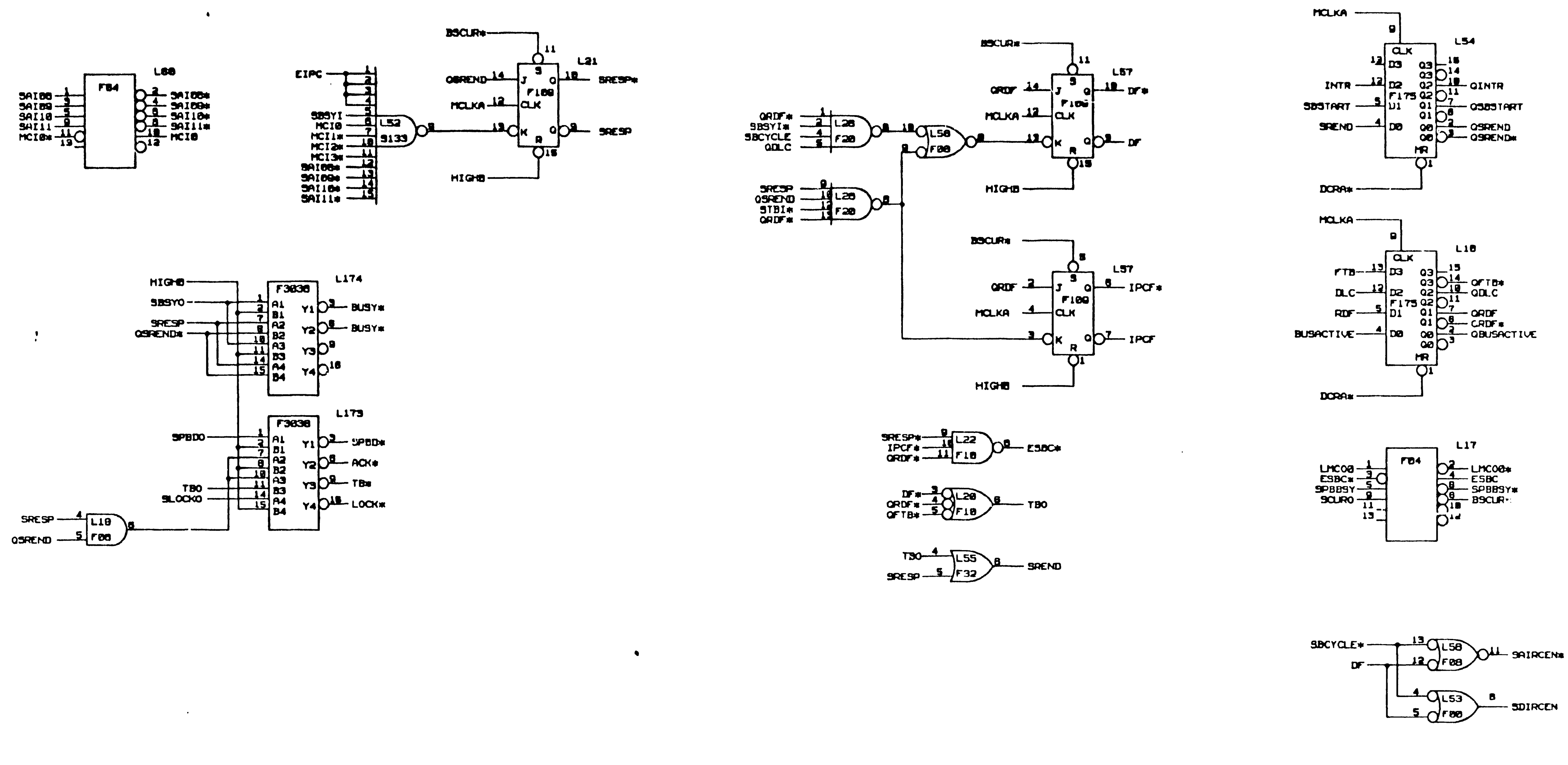
VSXXXSCU.LOGIC.1.8

LAST_MODIFIED=Mon Mar 18 11:04:13 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 8 OF 14



17" 11" 8.5" 11" 17" 22"



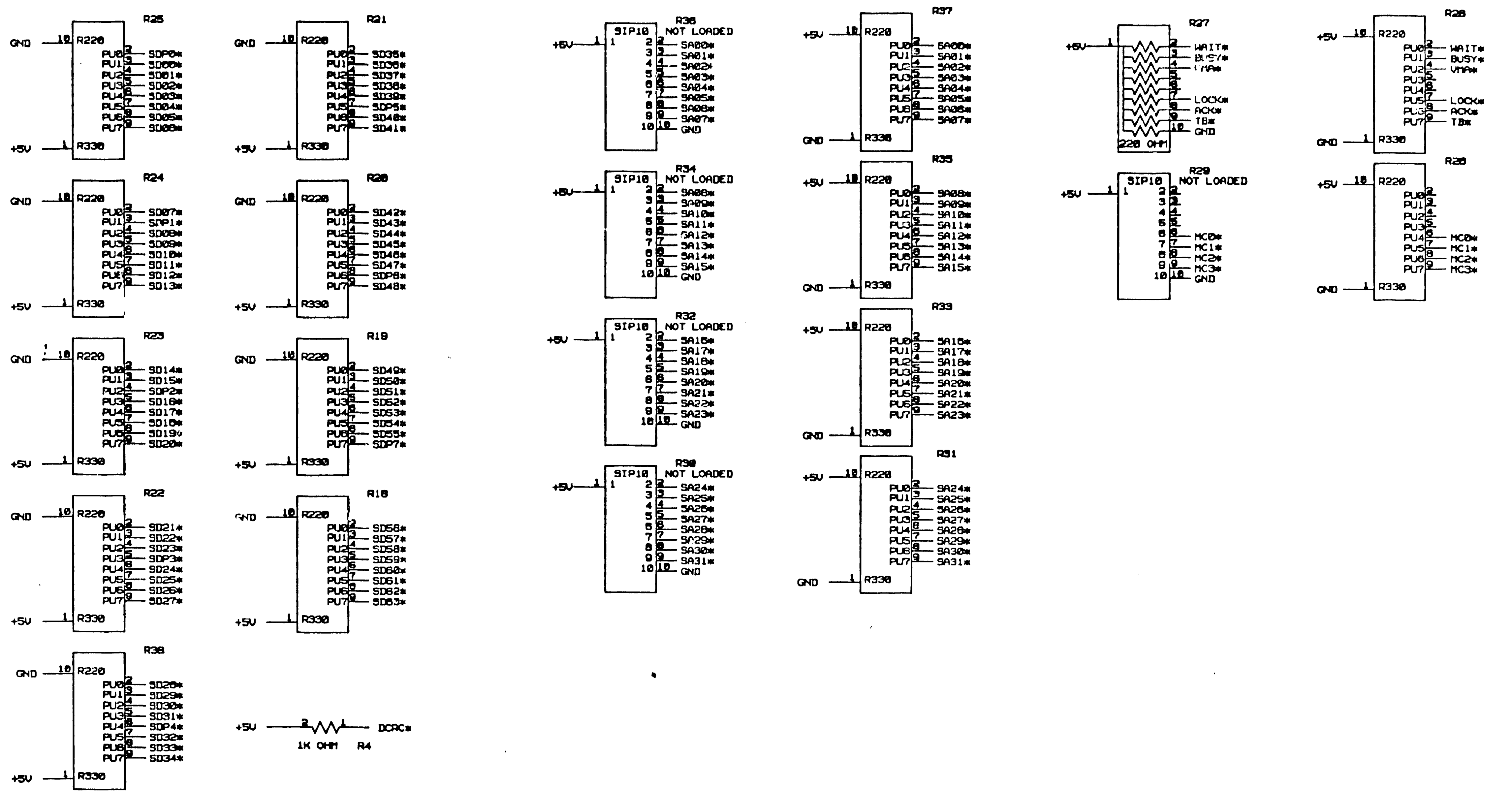
DRAWING

SYSTEM BUS IPC RESPONSE LOGIC

VSXXXSCU.LOGIC.1.10

LAST_MODIFIED=Mon Mar 18 10:45:59 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 10 OF 14

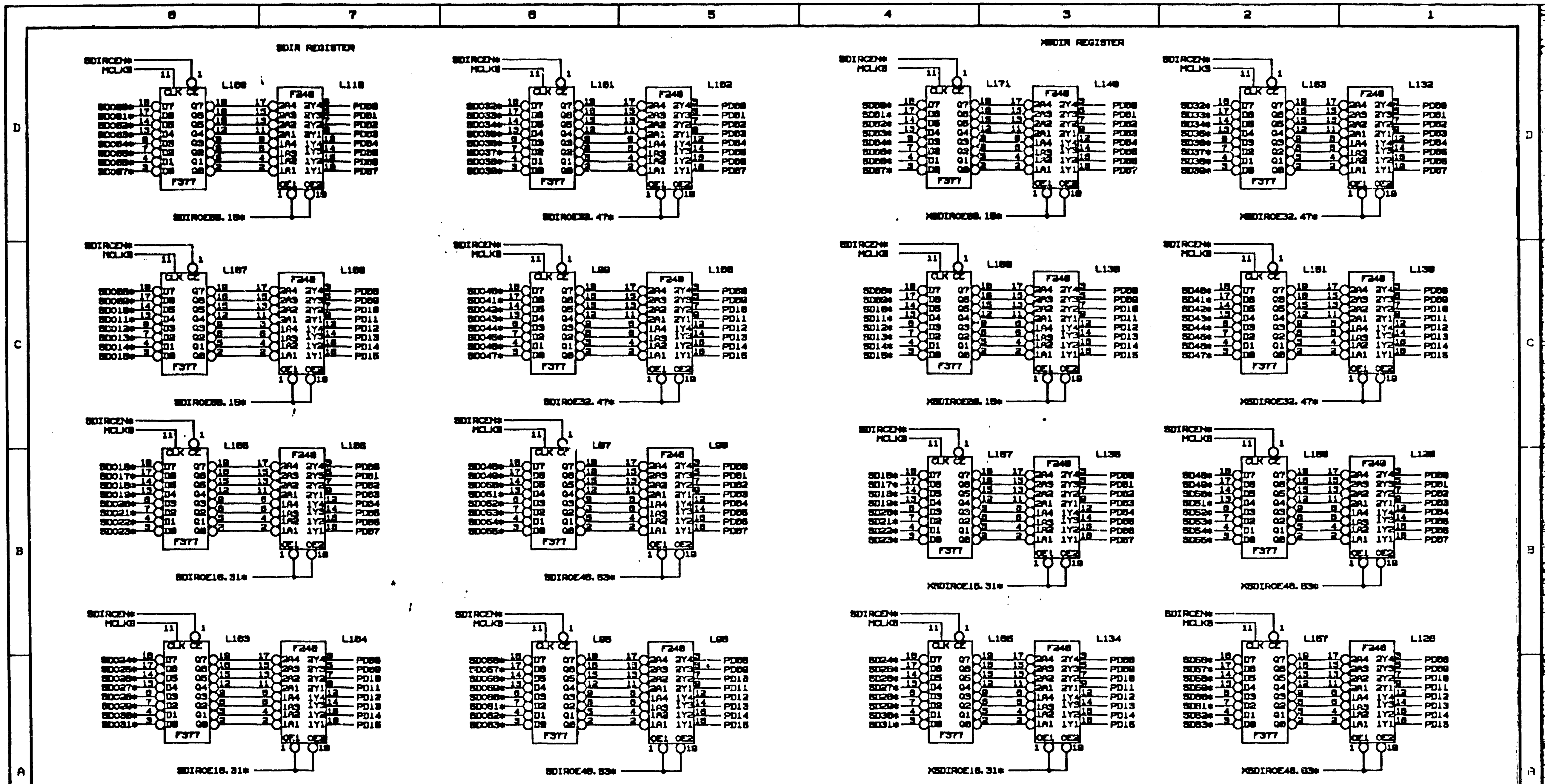


DRAWING

VSXXXSCU.LOGIC.1.11

LAST_MODIFIED=Mon Mar 18 10:47:02 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 11OF/4

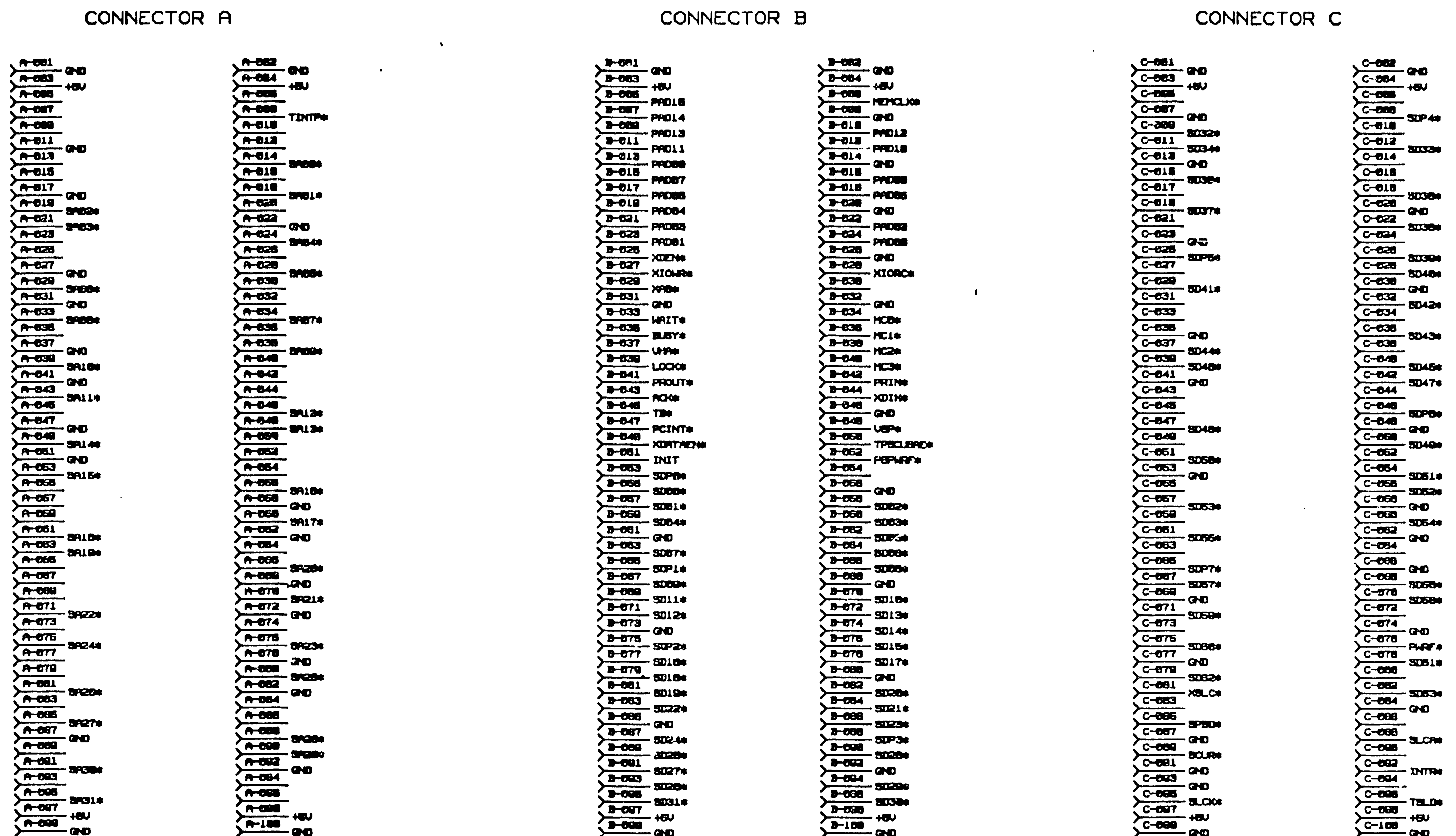


DRAWING

VSXXXSCU.LOGIC.1.12

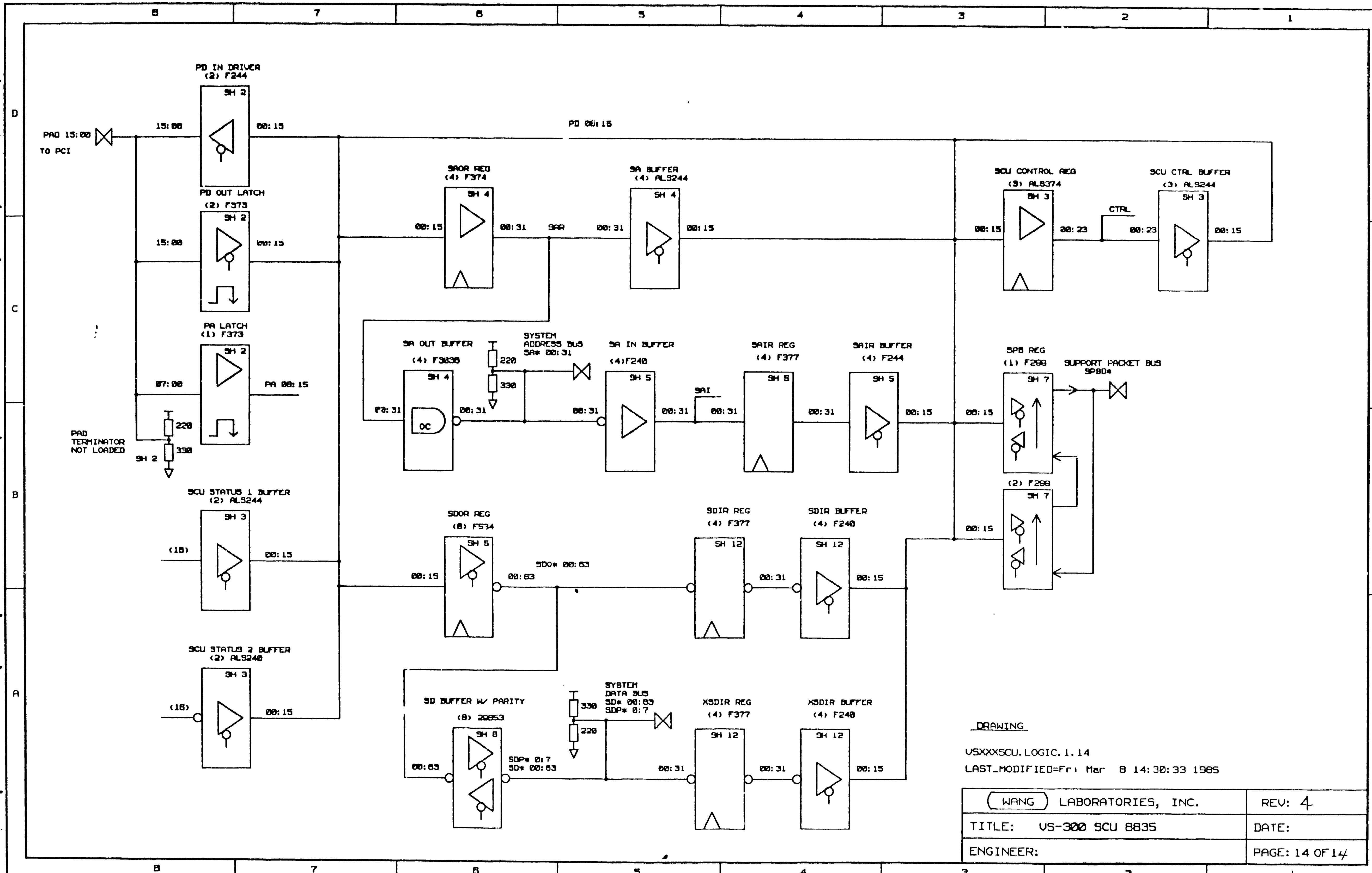
LAST_MODIFIED=Thu Jun 6 13:45:00 1985

WANG LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE:12 OF 14

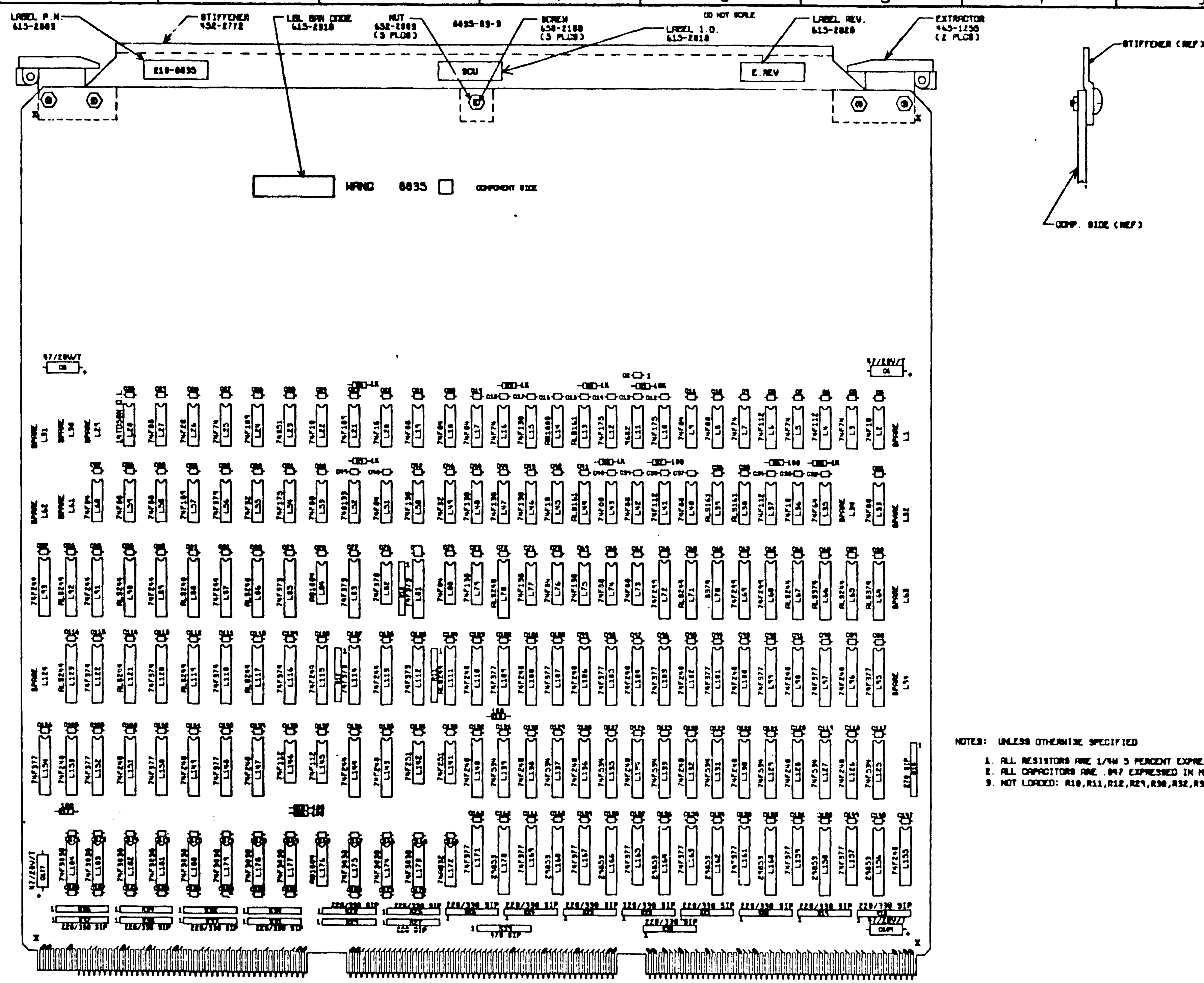


DRAWING
BACKPLANE CONNECTOR
VSXXXSCU.LOGIC.1.13
LAST_MODIFIED=Mon Jun 10 10:58:44 1985

(WANG) LABORATORIES, INC.	REV: 4
TITLE: VS-300 SCU 8835	DATE:
ENGINEER:	PAGE: 13 OF 14



PD IN DRIVER (2) F244
PD OUT LATCH (2) F373
PA LATCH (1) F373
PAD 15:00
TO PCI
PAD TERMINATOR NOT LOADED
PD 00:15
PA 00:15
SAOR REG (4) F374
SA BUFFER (4) ALS244
SCU CONTROL REG (3) ALS374
SCU CTRL BUFFER (3) ALS244
CTRL
SAR
SA OUT BUFFER (4) F3038
SYSTEM ADDRESS BUS SA* 00:31
SA IN BUFFER (4)F240
SAI
SAIR REG (4) F377
SAIR BUFFER (4) F244
SPB REG (1) F298
(2) F298
SUPPORT PACKET BUS SPBD*
SCU STATUS 1 BUFFER (2) ALS244
SCU STATUS 2 BUFFER (2) ALS240
SDOR REG (8) F534
SDO* 00:63
SDIR REG (4) F377
SDIR BUFFER (4) F240
SD BUFFER W/ PARITY (8) 29853
SYSTEM DATA BUS SD* 00:63 SDP* 0:7
SDP* 0:7 SD* 00:63
XSDIR REG (4) F377
XSDIR BUFFER (4) F240
DRAWING
VSXXXSCU.LOGIC.1.14
LAST_MODIFIED=Fri Mar 8 14:30:33 1985
WANG LABORATORIES, INC.
REV: 4
TITLE: VS-300 SCU 8835
DATE:
ENGINEER:
PAGE: 14 OF 14



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W 5 PERCENT EXPRESSED IN OHMS.
2. ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS.
3. NOT LOADED: R10,R11,R12,R29,R30,R32,R34,R36.

WANG LABORATORIES, INC.	BY	DATE	APPROVED BY	DATE
DWN	J. BOZZA	3/85		
MODEL NO. VS 300				
TITLE	ASSEMBLY DRAWING SCU M/L BOARD			
210-8835	D	8835	4	

VS-300 SBI 8836R1

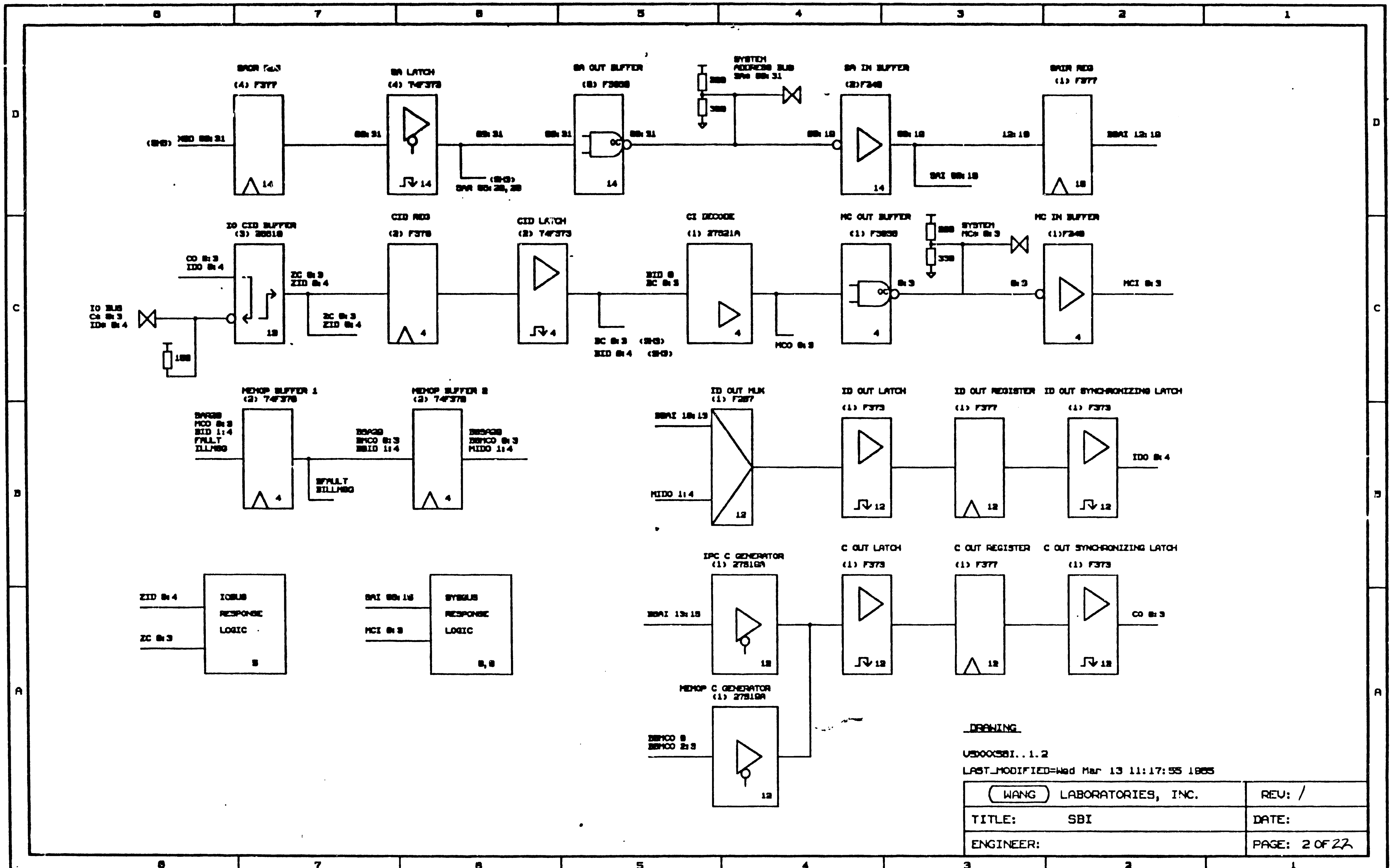
SYSTEM BUS INTERFACE

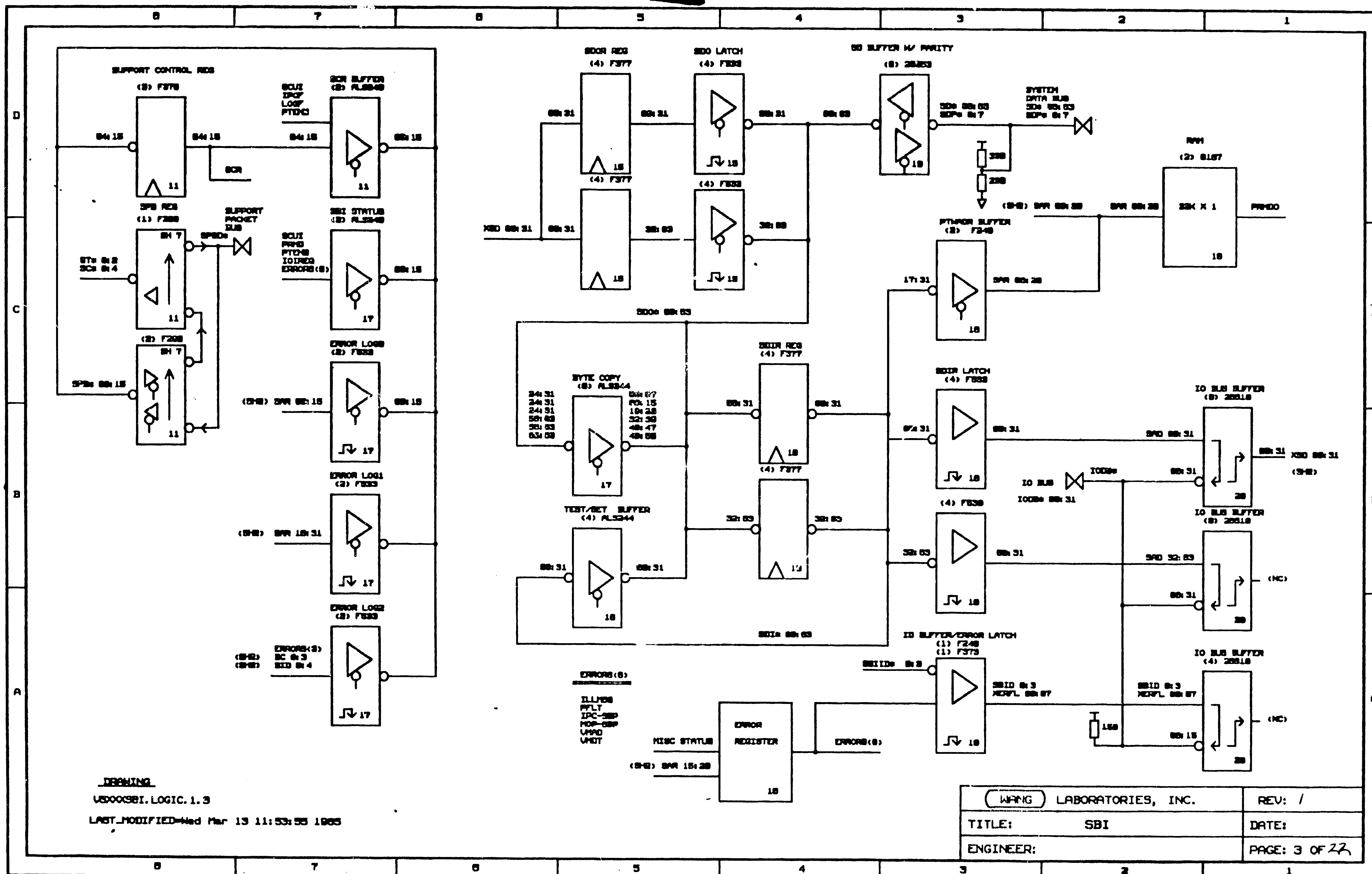
SHEET	DESCRIPTION
01	TITLE PAGE
02	BLOCK DIAGRAM
03	BLOCK DIAGRAM
04	IO ID AND COMMAND BUFFERS, SYSTEM BUS CONTROL DRIVERS AND RECEIVERS.
05	IO OPERATION-RECEIVE
06	SYSTEM BUS REQUEST AND GRANT LOGIC
07	TIMER, IO BUS GRANT, IO OUTPUT LATCH CONTROL
08	IOREQ, IPC RESPONSE SYSTEM BUS BUSY, IPC READY INPUT.
09	IPC RESPONSE LOGIC, IPC IOHOLD LOGIC.
10	SBI STATUS.
11	SBI SUPPORT PACKET BUS.
12	IO BUS COMMAND/ID OUTPUT, IO DATA OUTPUT CONTROL
13	IO COMMAND/ID TRANCEIVERS, IO BUS TERMINATORS.
14	SYSTEM BUS ADDRESS OUT REGISTER AND ADDRESS OUT LATCH, SYS ADDR OUT/IN BUFFERS.
15	SYSTEM BUS DATA OUT REGISTER AND DATA OUT LATCH.
16	IO PROTECTION, TEST/SET BUFFER.
17	SPB STATUS BUFFER, SPB ERROR LOG, WRITE BYTE COPY BUFFER.
18	SYSTEM BUS DATA IN REGISTER AND DATA IN LATCH.
19	SYSTEM BUS TERMINATION, SYSTEM DATA BUS TRANCEIVERS.
20	IO BUS DATA DRIVERS/RECEIVERS
21	BACK PLANE CONNECTOR.
22	SPARE GATES

E-REV 1

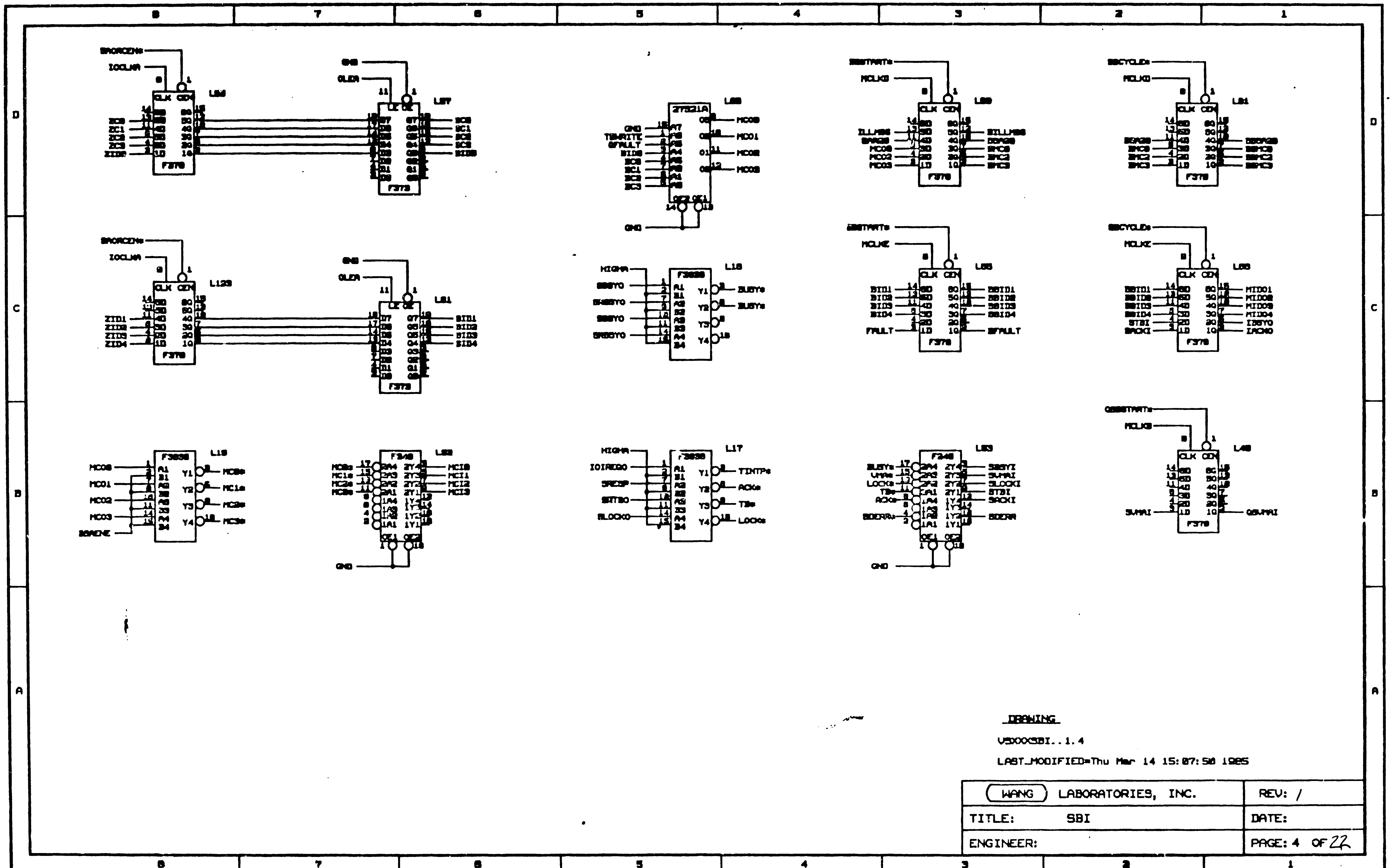
DRAWING
TITLE=VSXXXSBI
ABBREV=SBI
LAST_MODIFIED=Mon Aug 26 11:08:19 1985
VSXXXSBI.LOGIC.1.1

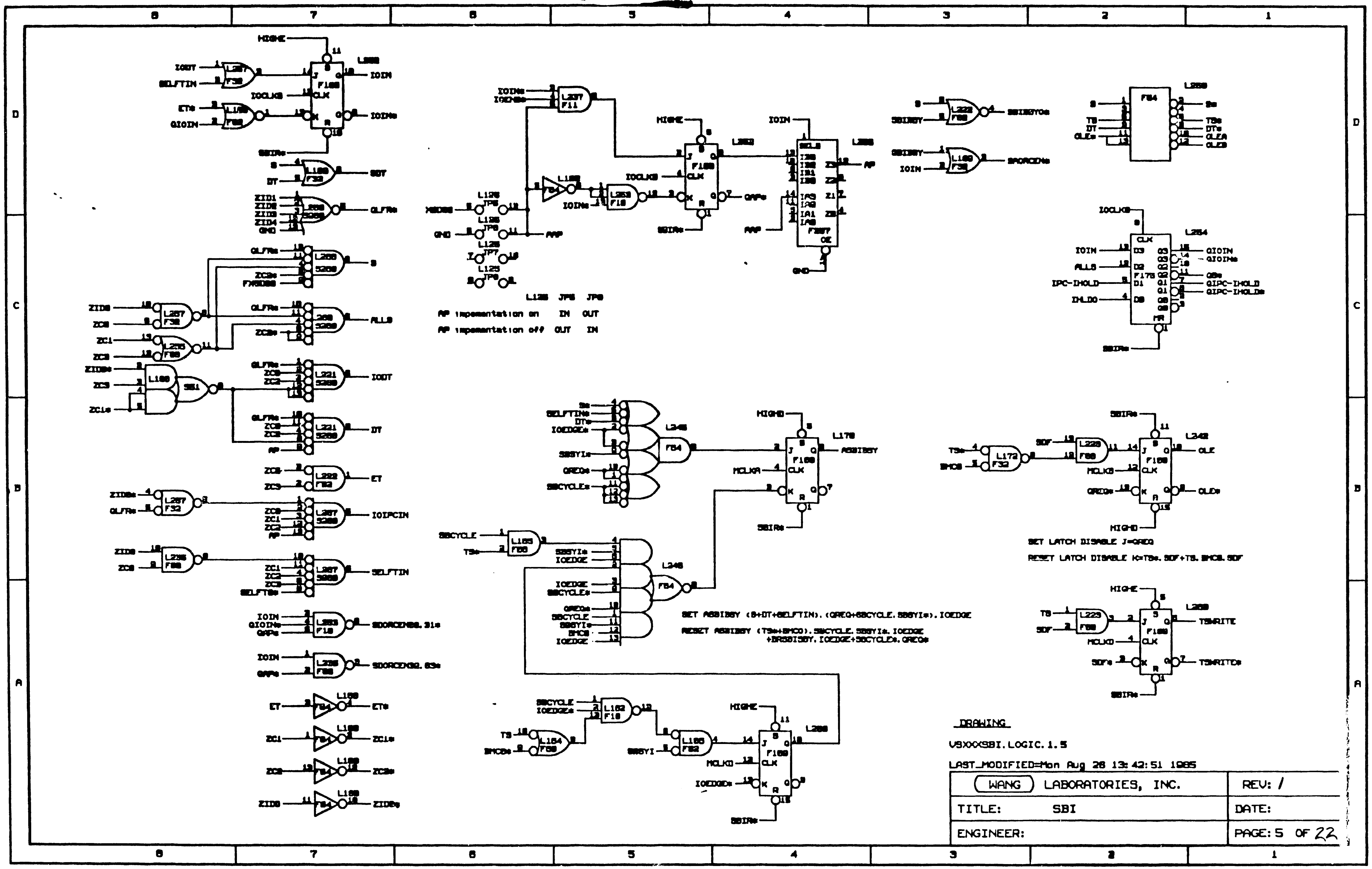
WANG LABORATORIES, INC.	REV: /
TITLE: VS-300 SBI 8836R1	DATE: 8/26/85
ENGINEER: B.J. PATEL , P.A. MORRISON	PAGE: 1 OF 22


SA LATCH
(4) 74F373
SA OUT BUFFER
(8) F3808
SYSTEM ADDRESS BUS
SA IN BUFFER
(2)F348
SAIR REG
(1) F377
ID CID BUFFER
CID REG
(2) F378
CID LATCH
(2) 74F373
CI DECODE
(1) 27621A
MC OUT BUFFER
SYSTEM
MC IN BUFFER
(1)F348
IO BUS
MEMOP BUFFER 1
(2) 74F378
MEMOP BUFFER 2
(2) 74F378
ID OUT MUX
(1) F287
ID OUT LATCH
(1) F373
ID OUT REGISTER
(1) F377
ID OUT SYNCHRONIZING LATCH
(1) F373
IDO 0:4
IOBUS
RESPONSE
LOGIC
SYSBUS
RESPONSE
LOGIC
IPC C GENERATOR
(1) 27819A
C OUT LATCH
(1) F373
C OUT REGISTER
(1) F377
C OUT SYNCHRONIZING LATCH
(1) F373
CO 0:3
MEMOP C GENERATOR
(1) 27819A
DRAWING
U5XXXSBI..1.2
LAST_MODIFIED=Wed Mar 13 11:17:55 1985
WANG LABORATORIES, INC.
REV: /
TITLE: SBI
DATE:
ENGINEER:
PAGE: 2 OF 22



SUPPORT CONTROL REG
SCR BUFFER
SPB REG
SUPPORT PACKET BUS
SBI STATUS
ERROR LOG0
ERROR LOG1
ERROR LOG2
SDOR REG
SDO LATCH
SD BUFFER W/ PARITY
SYSTEM DATA BUS
RAM
32K X 1
PTWRDR BUFFER
BYTE COPY
SDIR REG
SDIR LATCH
IO BUS BUFFER
TEST/SET BUFFER
IO BUFFER/ERROR LATCH
ERRORS(8)
ILLMSG
PFLT
IPC-SBP
MOP-SBP
VMRD
VMDT
MISC STATUS
ERROR REGISTER
DRAWING
VBXXXSBI.LOGIC.1.3
LAST_MODIFIED=Wed Mar 13 11:53:55 1985
WANG LABORATORIES, INC.
REV: /
TITLE: SBI
DATE:
ENGINEER:
PAGE: 3 OF 22


DRAWING
V5XXXSBI..1.4
LAST_MODIFIED=Thu Mar 14 15:07:50 1985
WANG LABORATORIES, INC.
REV: /
TITLE: SBI
DATE:
ENGINEER:
PAGE: 4 OF 22

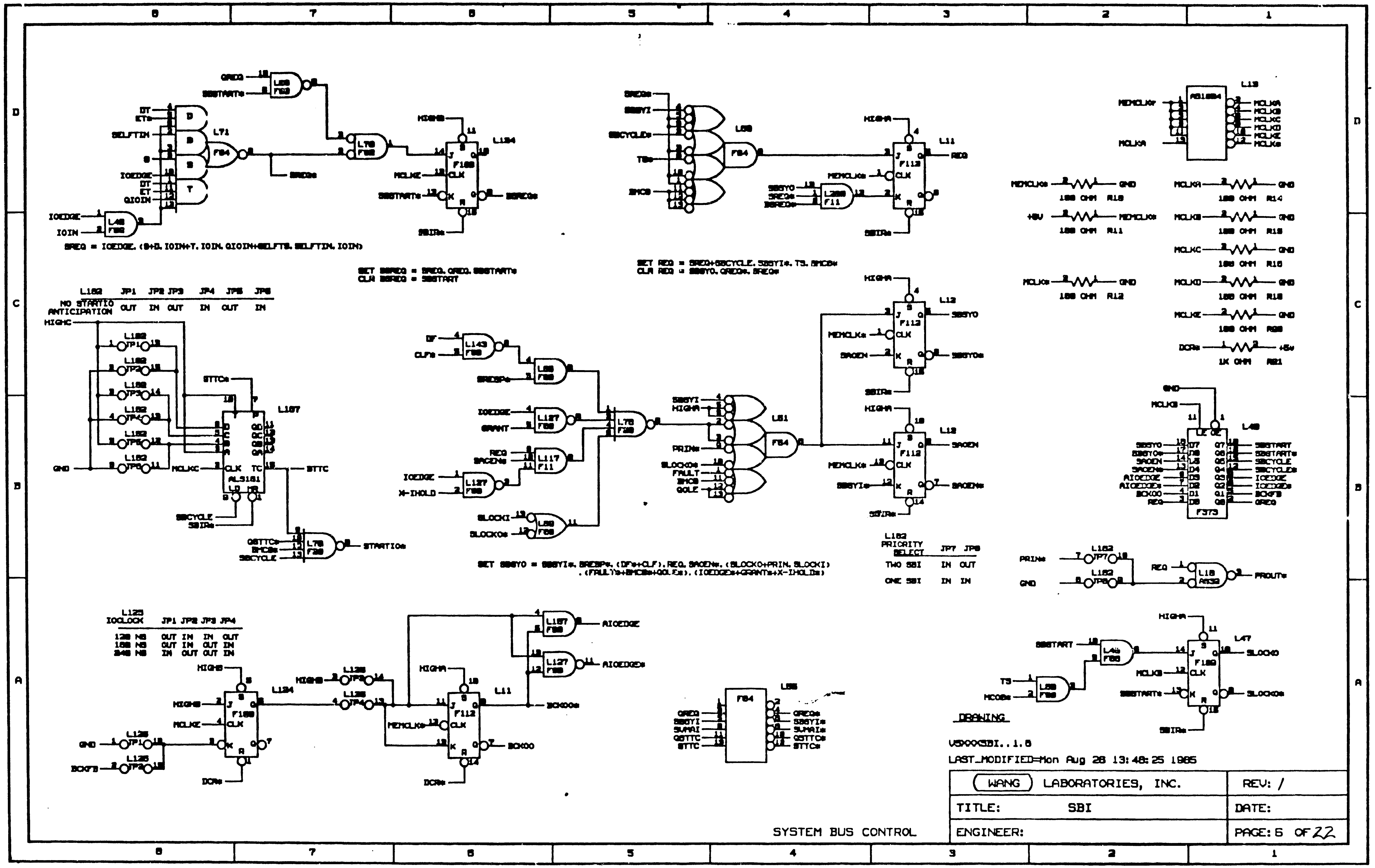


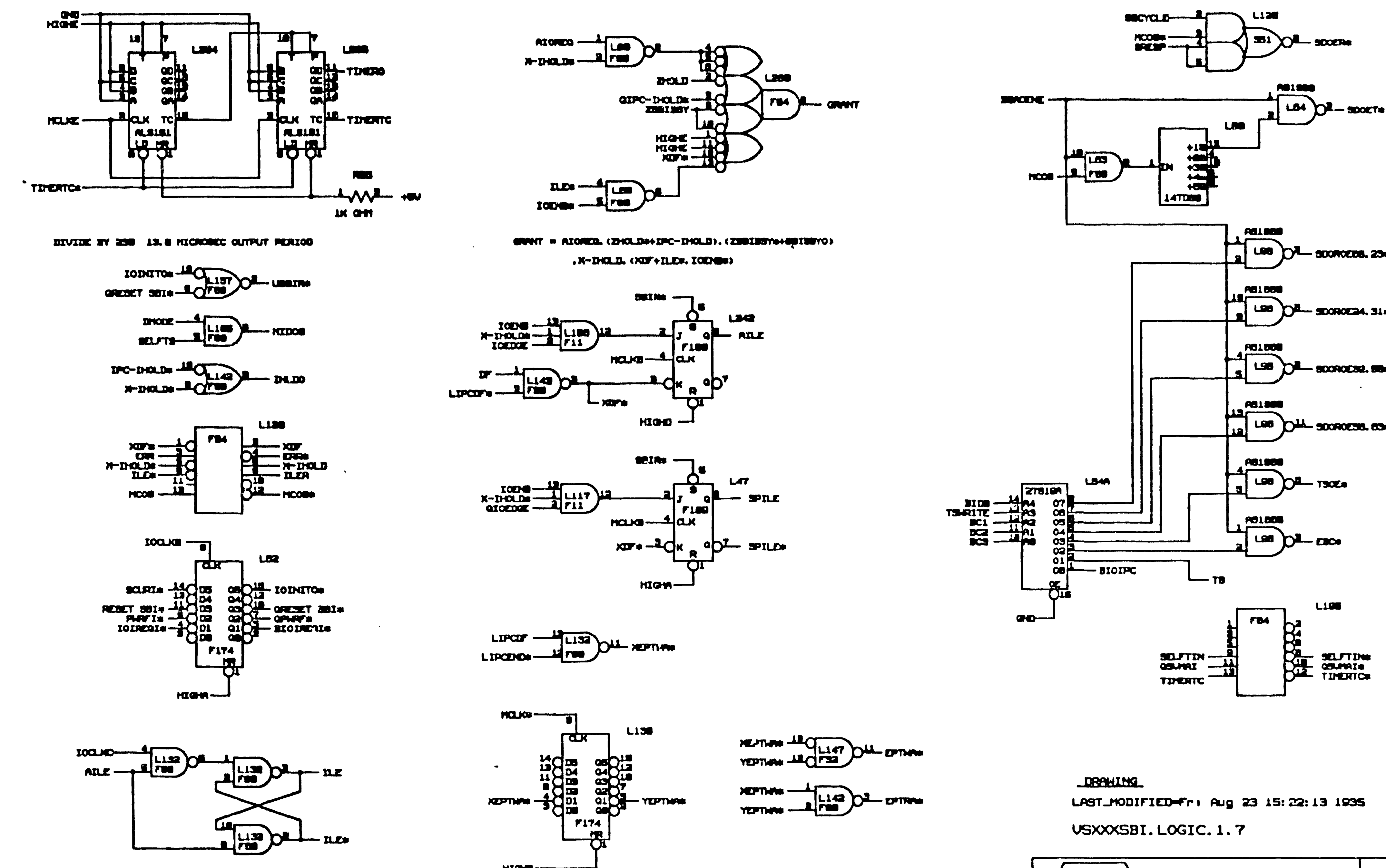
DRAWING

VSXXXSBI.LOGIC.1.5

LAST_MODIFIED=Mon Aug 26 13:42:51 1985

WANG LABORATORIES, INC.	REV: /
TITLE: SBI	DATE:
ENGINEER:	PAGE: 5 OF 22


SET SBREQ = SREQ. GREQ. SBSTARTs
CLR SBREQ = SBSTART
SYSTEM BUS CONTROL
DRAWING
V5XXXSBI..1.6
LAST_MODIFIED=Mon Aug 28 13:48:25 1985
WANG LABORATORIES, INC.
REV: /
TITLE: SBI
DATE:
ENGINEER:
PAGE: 6 OF 22

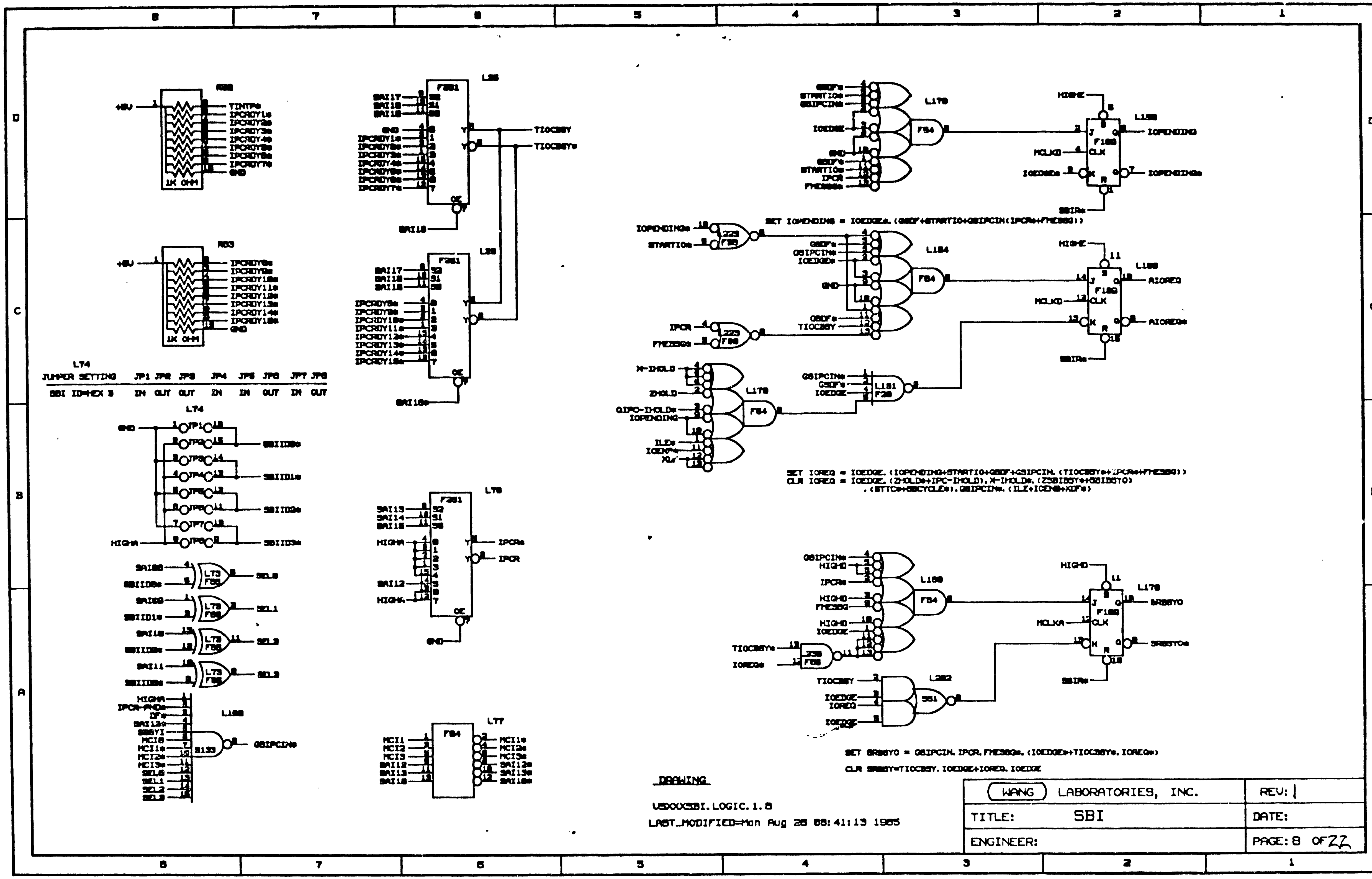


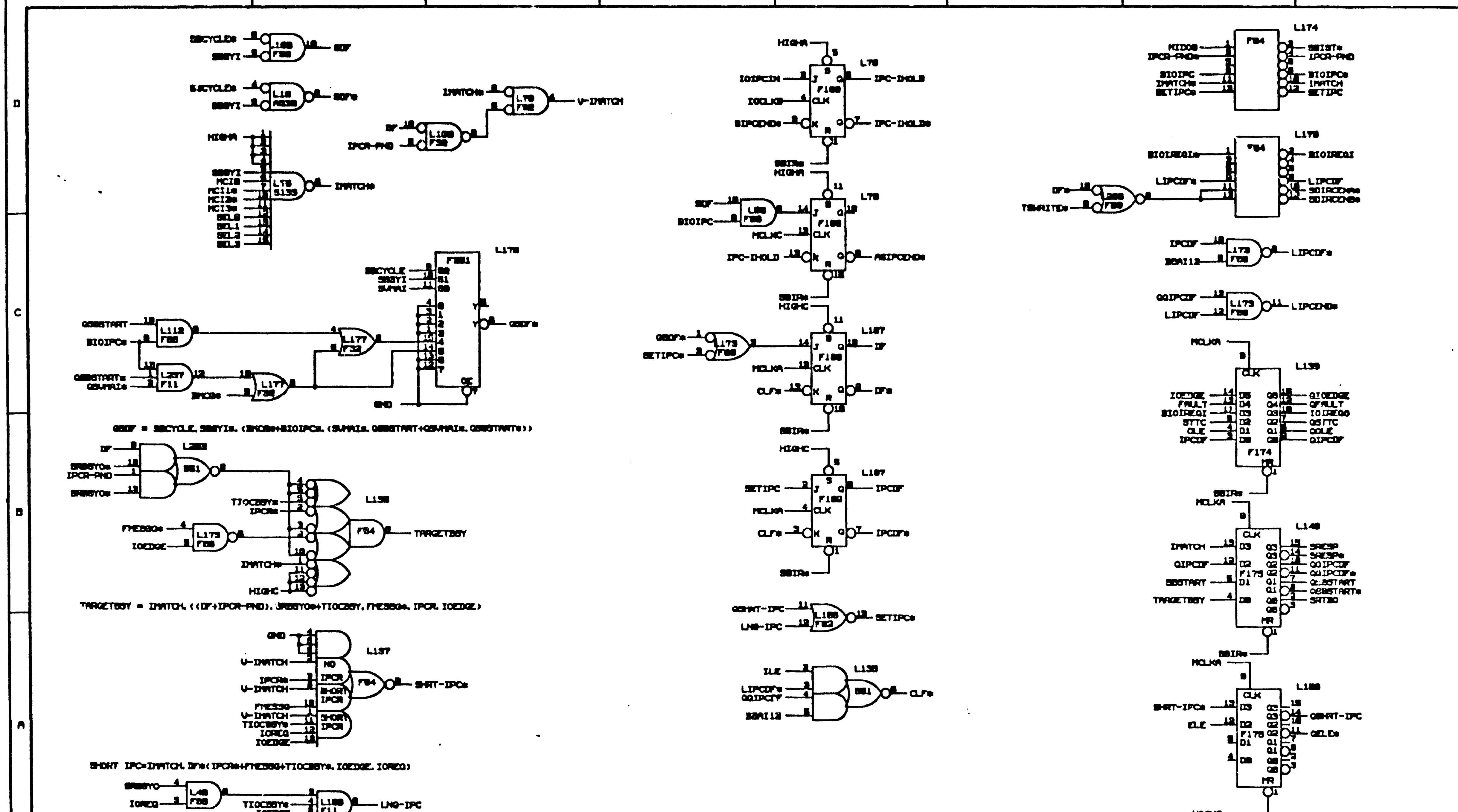
DRAWING

LAST_MODIFIED=Fri Aug 23 15:22:13 1935

VSXXXSBI.LOGIC.1.7

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 7 OF 22


DRAWING
V5XXXSBI.LOGIC.1.8
LAST_MODIFIED=Mon Aug 26 08:41:13 1985
WANG LABORATORIES, INC.
REV: |
TITLE: SBI
DATE:
ENGINEER:
PAGE: 8 OF 22

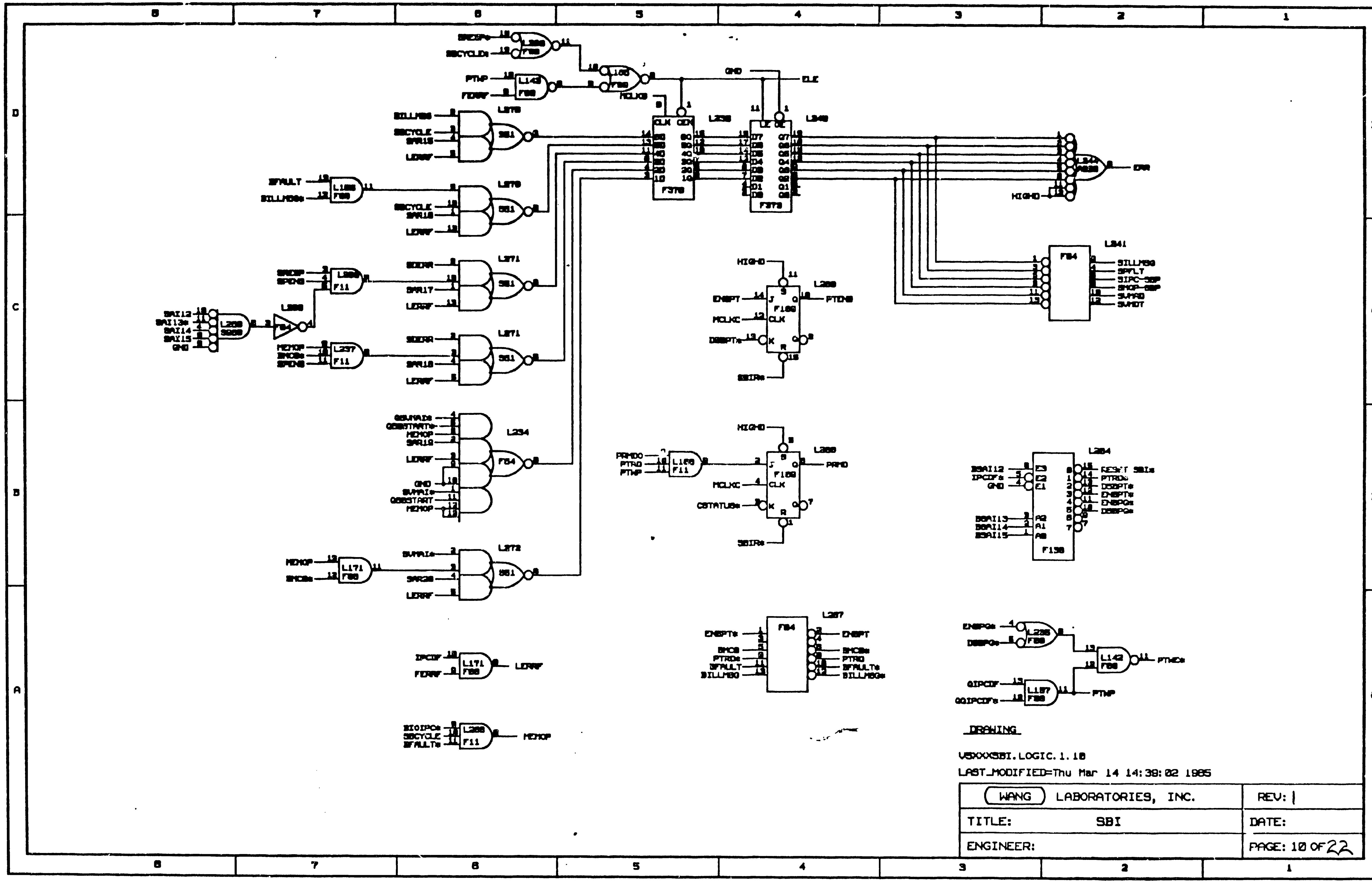


DRAWING

VS000SBI.LOGIC.1.9

LAST_MODIFIED=Thu Mar 14 15:21:19 1985

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 9 OF 22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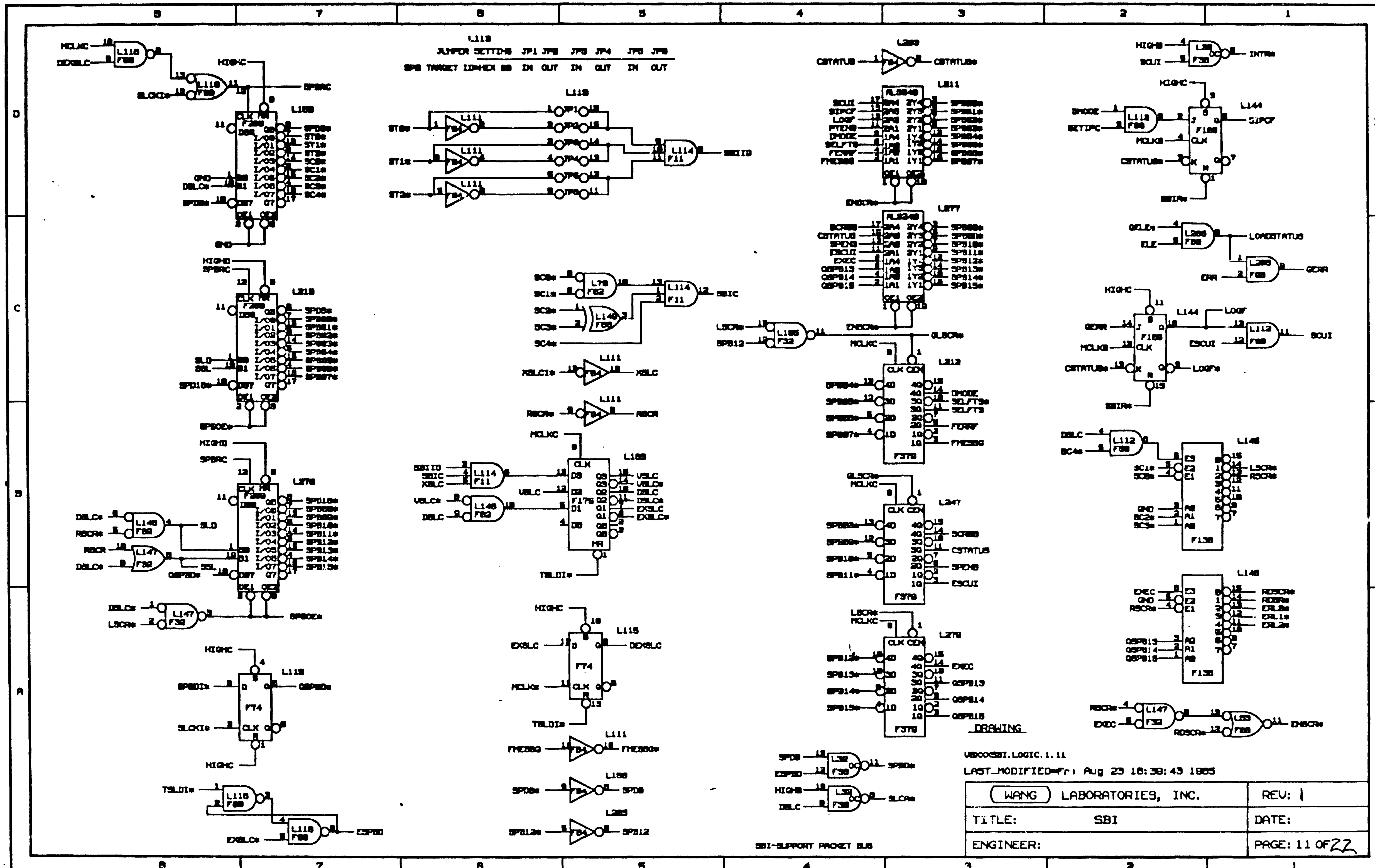
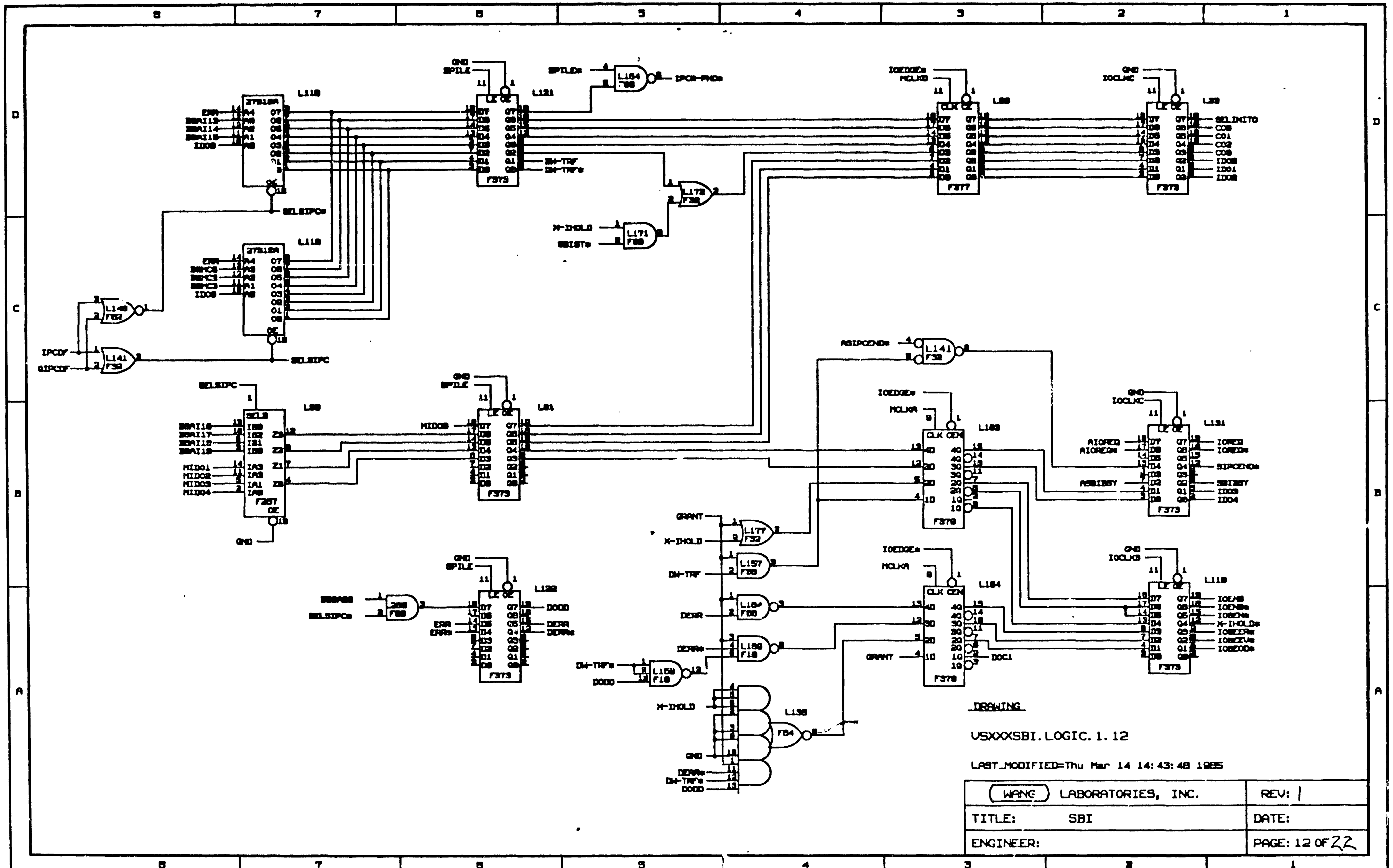
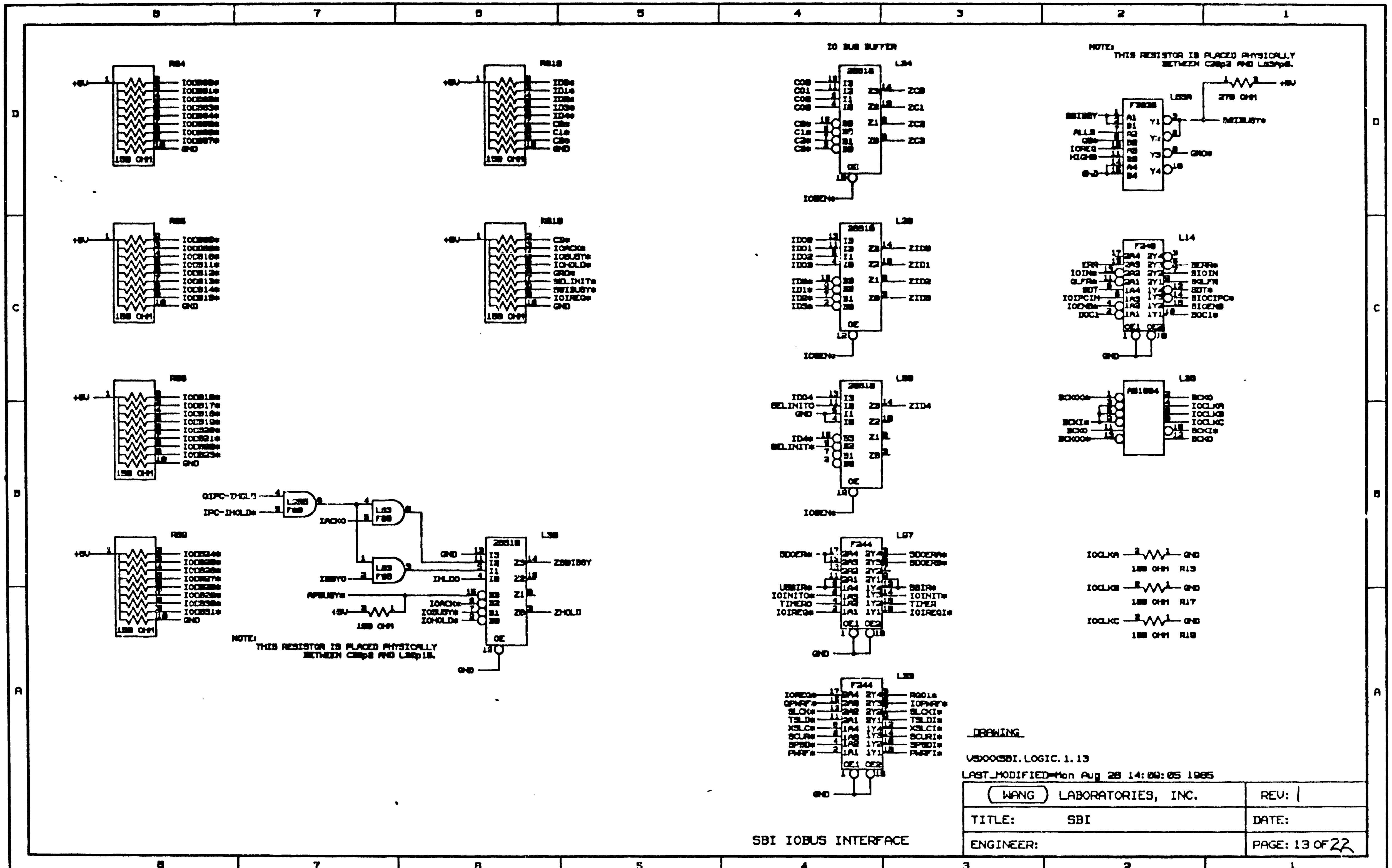
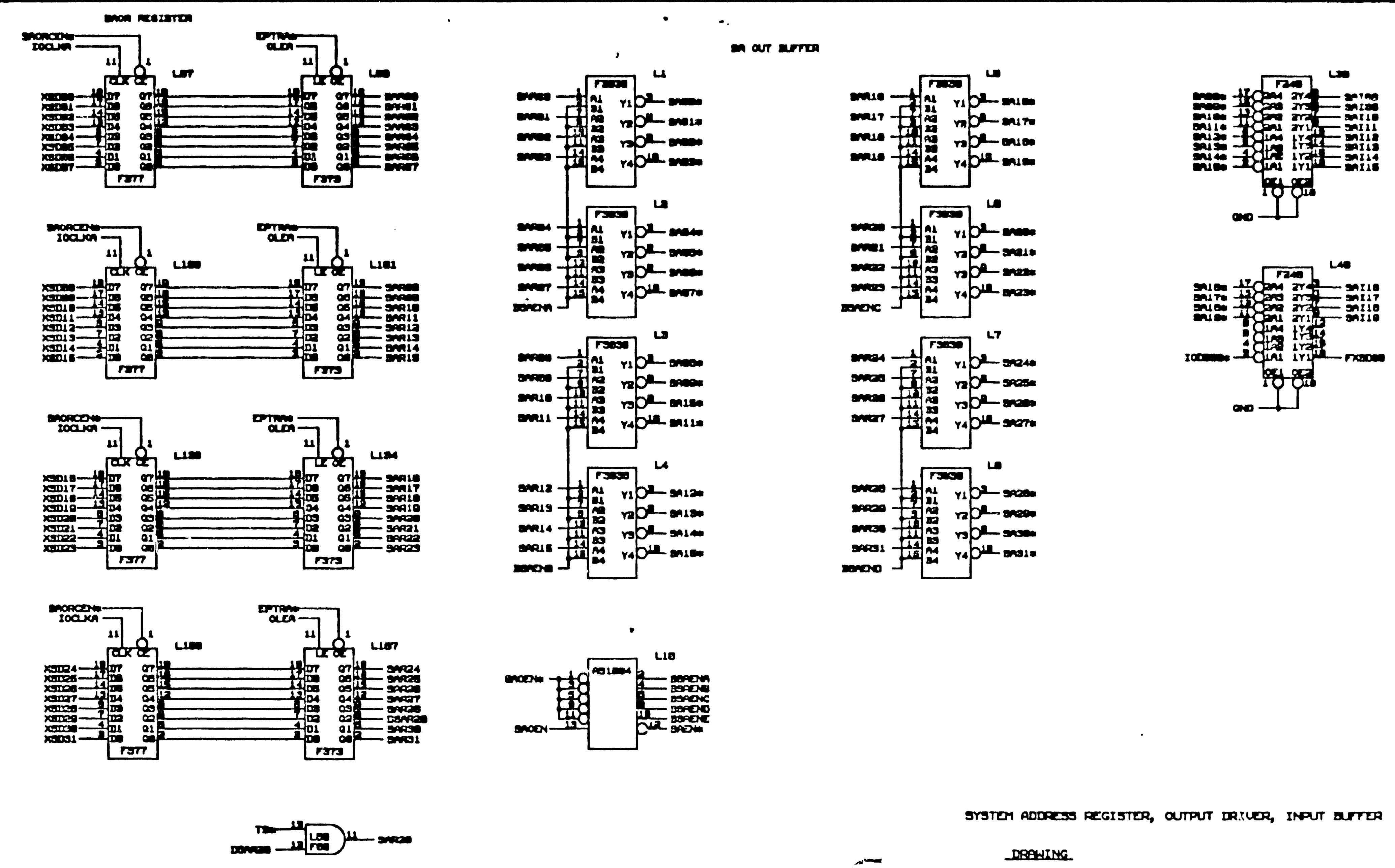
LAST_MODIFIED=Thu Mar 14 14:38:02 1985
WANG LABORATORIES, INC.
REV: 1
TITLE: SBI
DATE:
ENGINEER:
PAGE: 10 OF 22


L113
JUMPER SETTING JP1 JP2 JP3 JP4 JP5 JP6
SPB TARGET ID=HEX 88 IN OUT IN OUT IN OUT
DRAWING
VBXXSBI.LOGIC.1.11
LAST_MODIFIED=Fri Aug 23 16:38:43 1985
WANG LABORATORIES, INC.
REV: 1
TITLE: SBI
DATE:
ENGINEER:
PAGE: 11 OF 22
SBI-SUPPORT PACKET BUS


DRAWING
VSXXXSBI.LOGIC.1.12
LAST_MODIFIED=Thu Mar 14 14:43:48 1985
WANG LABORATORIES, INC.
REV: 1
TITLE: SBI
DATE:
ENGINEER:
PAGE: 12 OF 22


IO BUS BUFFER
NOTE:
THIS RESISTOR IS PLACED PHYSICALLY BETWEEN C38p2 AND L53Ap8.
NOTE:
THIS RESISTOR IS PLACED PHYSICALLY BETWEEN C38p2 AND L38p15.
DRAWING
VSXXXSBI.LOGIC.1.13
LAST_MODIFIED=Mon Aug 28 14:08:05 1985
WANG LABORATORIES, INC.
REV: 1
TITLE: SBI
DATE:
ENGINEER:
PAGE: 13 OF 22
SBI IOBUS INTERFACE



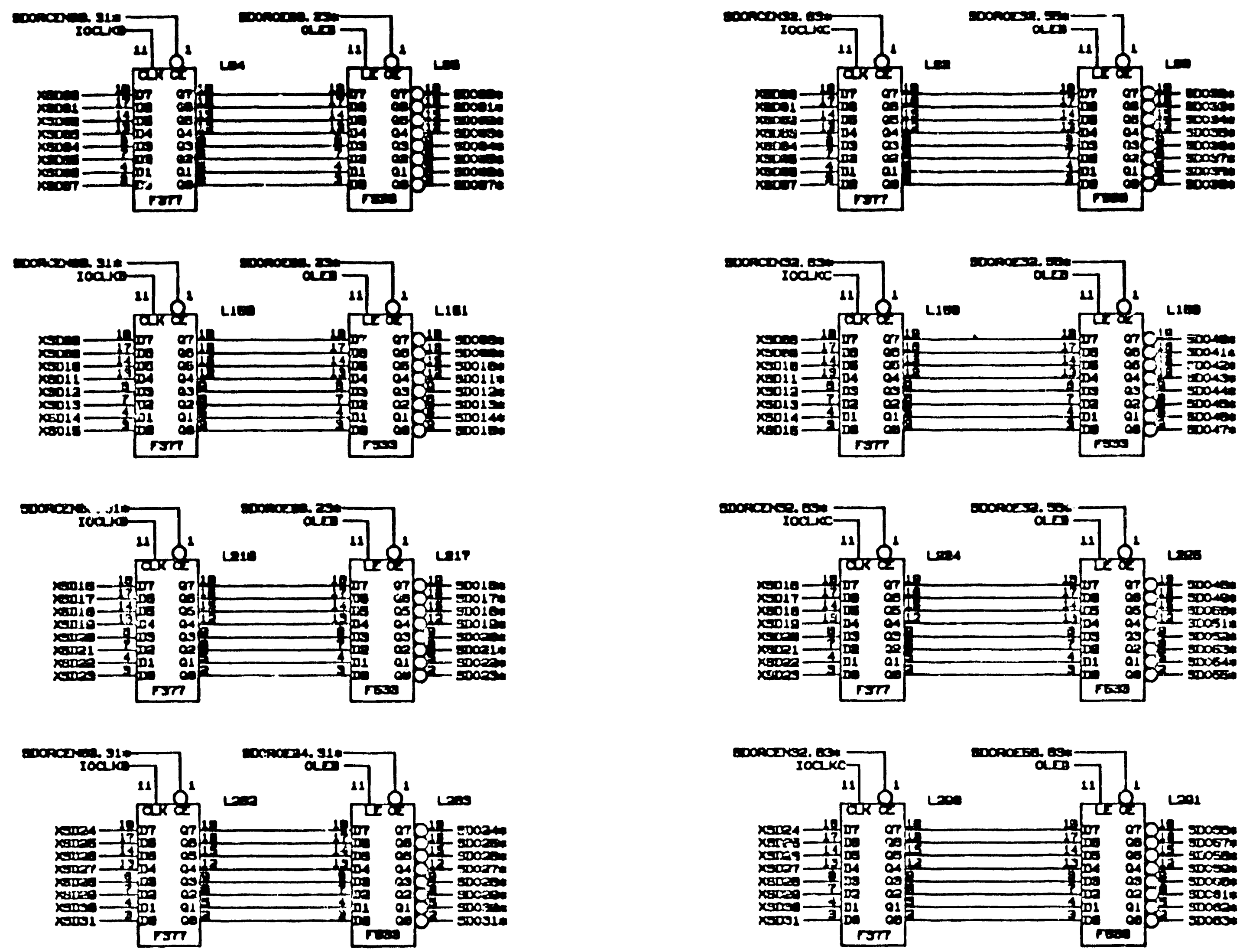
SYSTEM ADDRESS REGISTER, OUTPUT DRIVER, INPUT BUFFER

DRAWING

VSXXXSBI.LOGIC.1.14

LAST_MODIFIED=Mon Aug 28 18:01:48 1985

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 14 OF 22



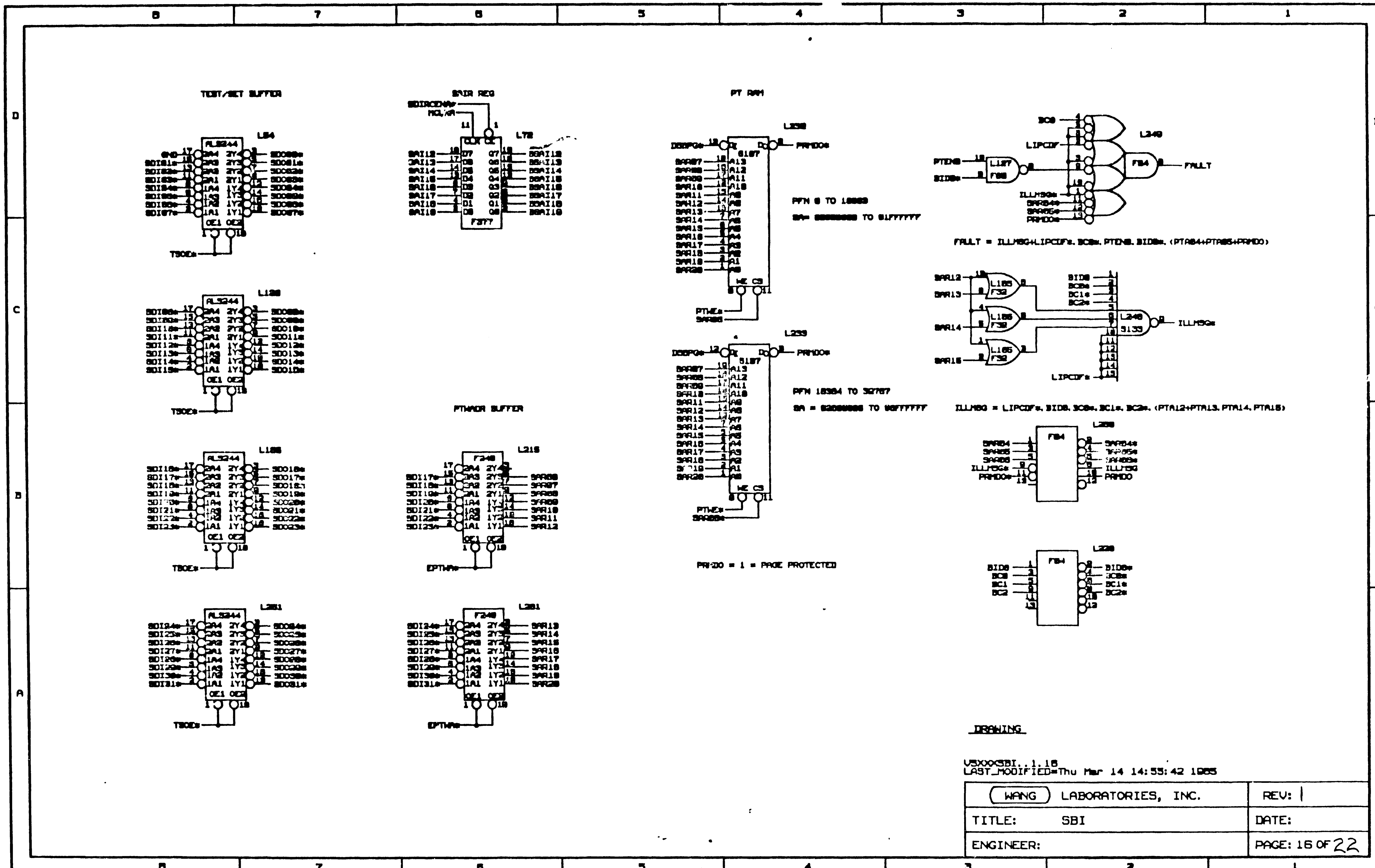
SYSTEM DATA OUTPUT REGISTER

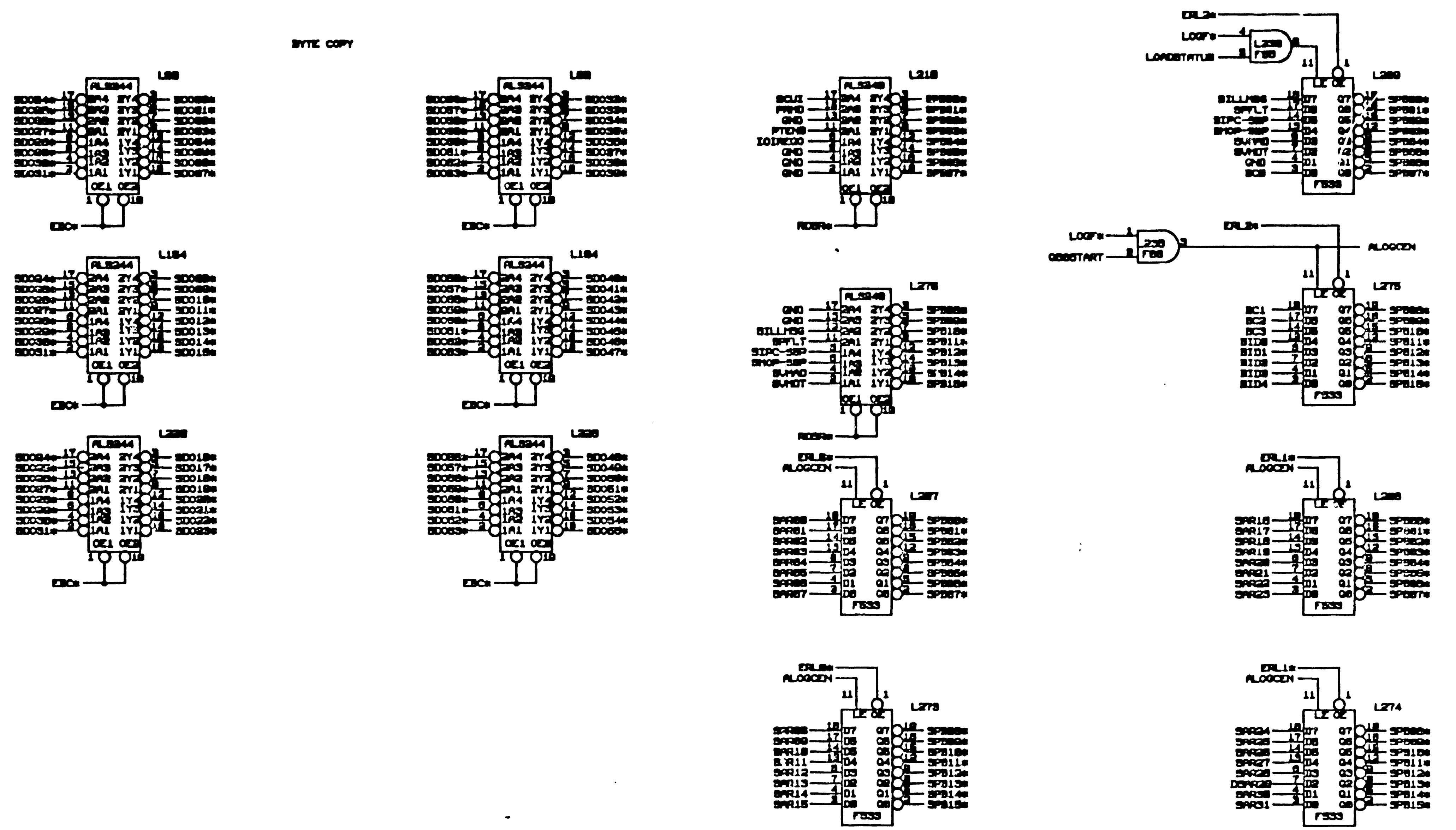
DRAWING

VSXXXSBI.LOGIC.1.15

LAST_MODIFIED=Thu Mar 14 14:53:08 1985

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 15 OF 22


TEST/SET BUFFER
SAIR REG
PT RAM
PTHADR BUFFER
PRMDO = 1 = PAGE PROTECTED
DRAWING
VSXXXSBI..1.16
LAST_MODIFIED=Thu Mar 14 14:55:42 1985
WANG LABORATORIES, INC.
REV: 1
TITLE: SBI
DATE:
ENGINEER:
PAGE: 16 OF 22

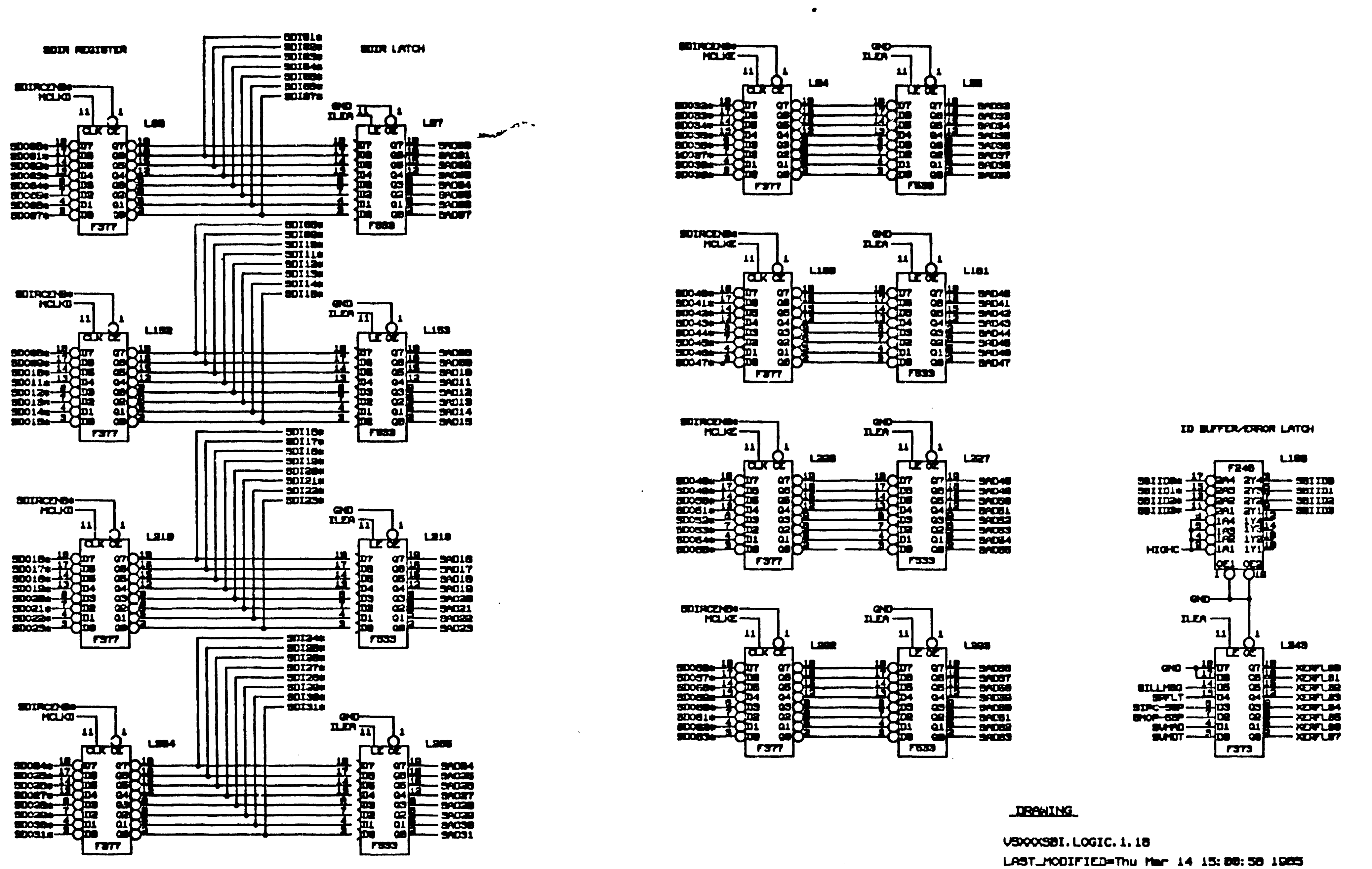


DRAWING

VSXXXSBI.LOGIC.1.17

LAST_MODIFIED=Thu Mar 14 14:57:28 1985

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 17 OF 22



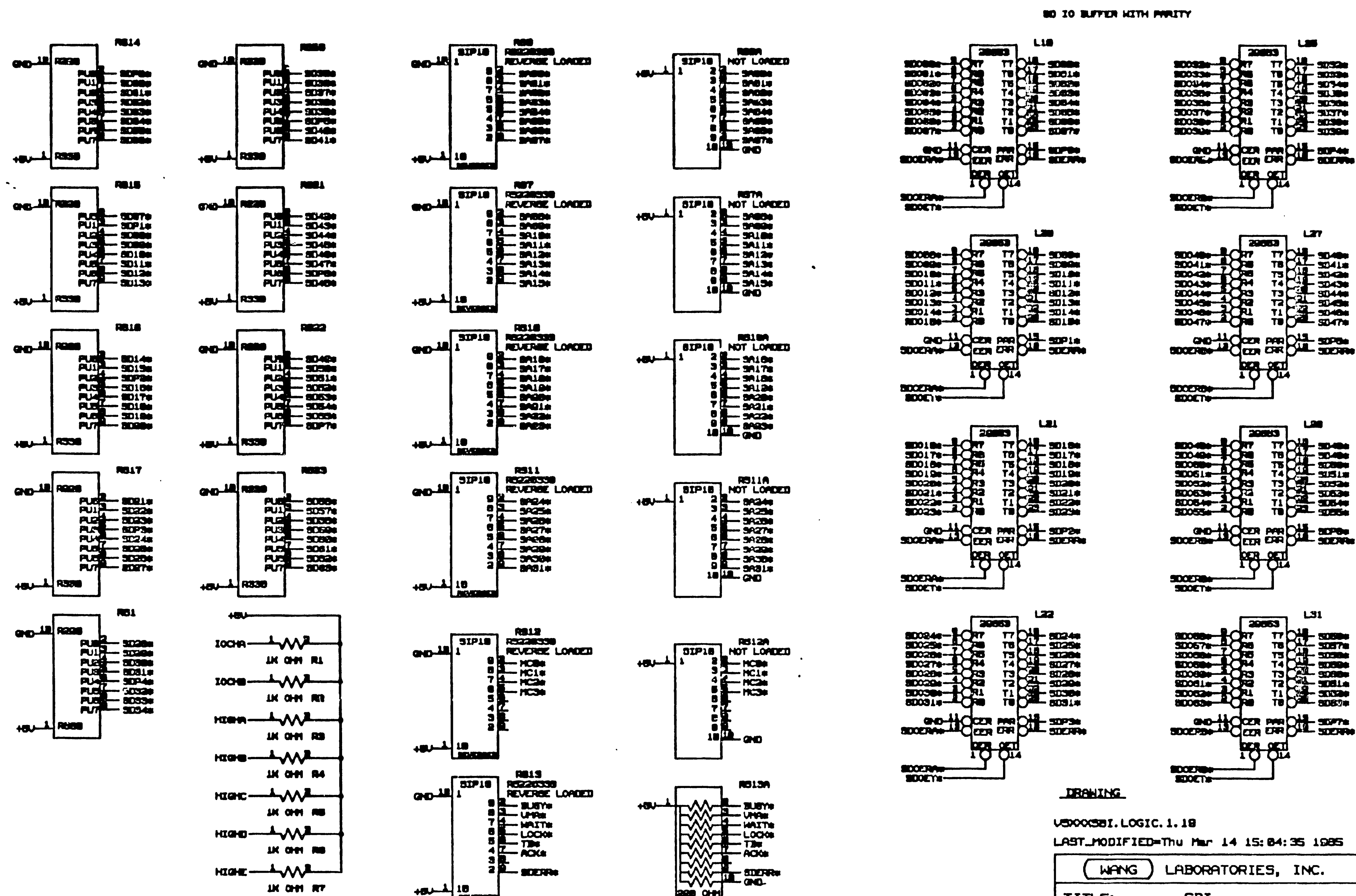
DRAWING

VSXXXSBI.LOGIC.1.18

LAST_MODIFIED=Thu Mar 14 15:08:58 1985

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 18 OF 22

SYSTEM DATA INPUT REGISTER, IO BUFFER

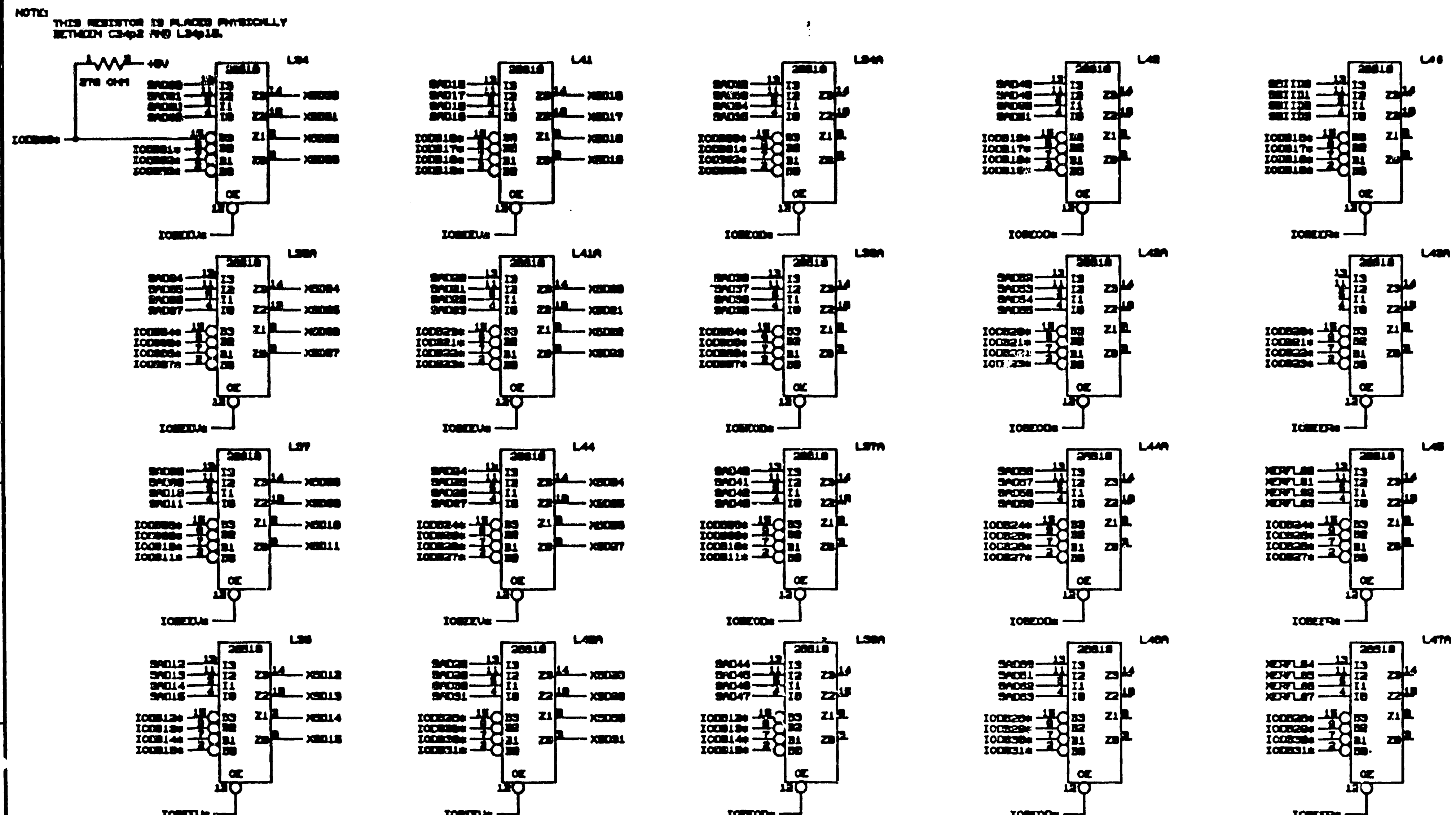


DRAWING

V5XXXSBI.LOGIC.1.19

LAST_MODIFIED=Thu Mar 14 15:04:35 1985

WANG LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE: 19 OF 22



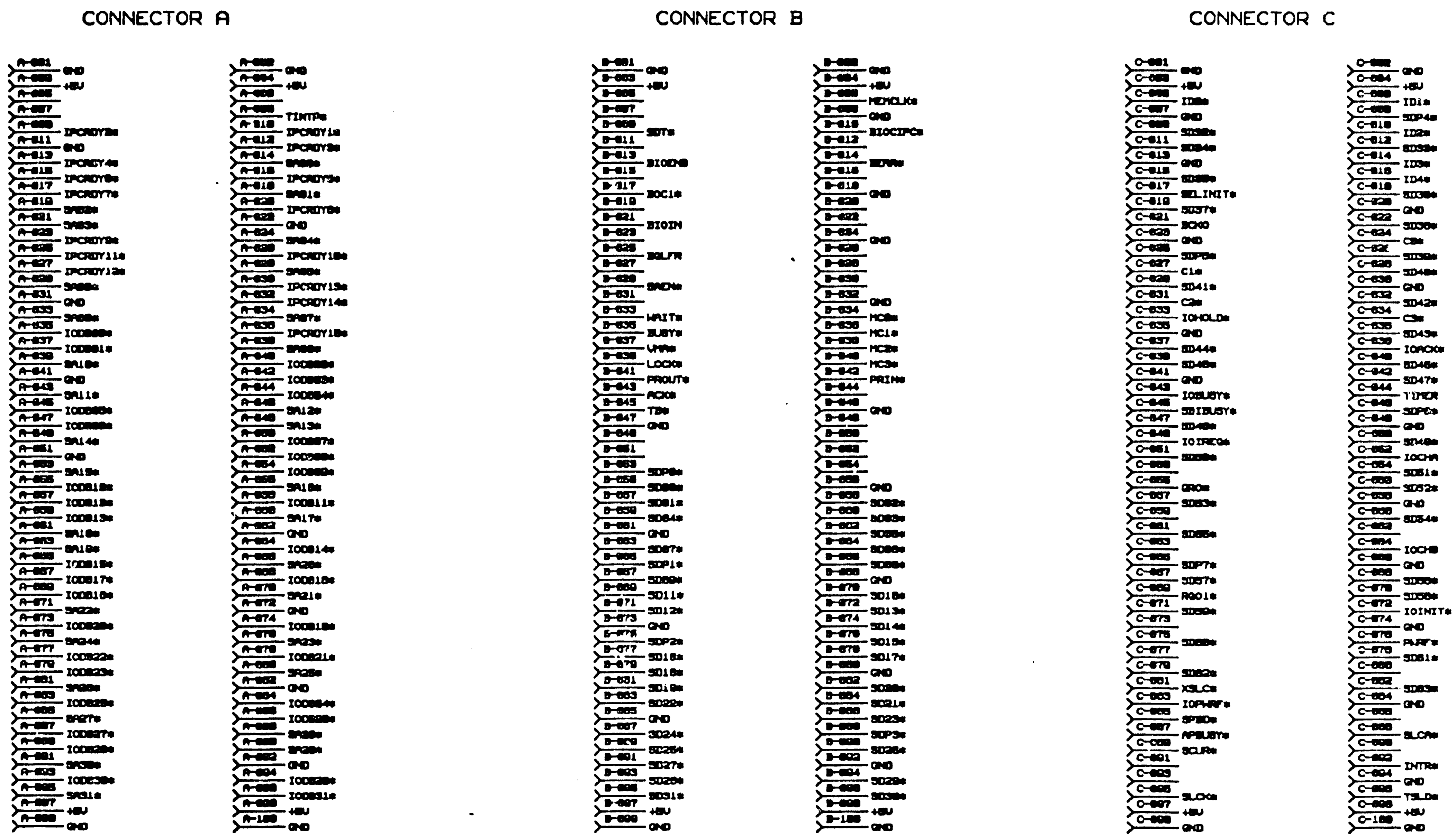
DRAWING

IO DATA BUS DRIVERS

VSXXXSBI..1.20

LAST_MODIFIED=Mon Aug 28 14:19:11 1985

WANG LABORATORIES, INC.	REV: /
TITLE: SBI	DATE:
ENGINEER:	PAGE: 20 OF 22



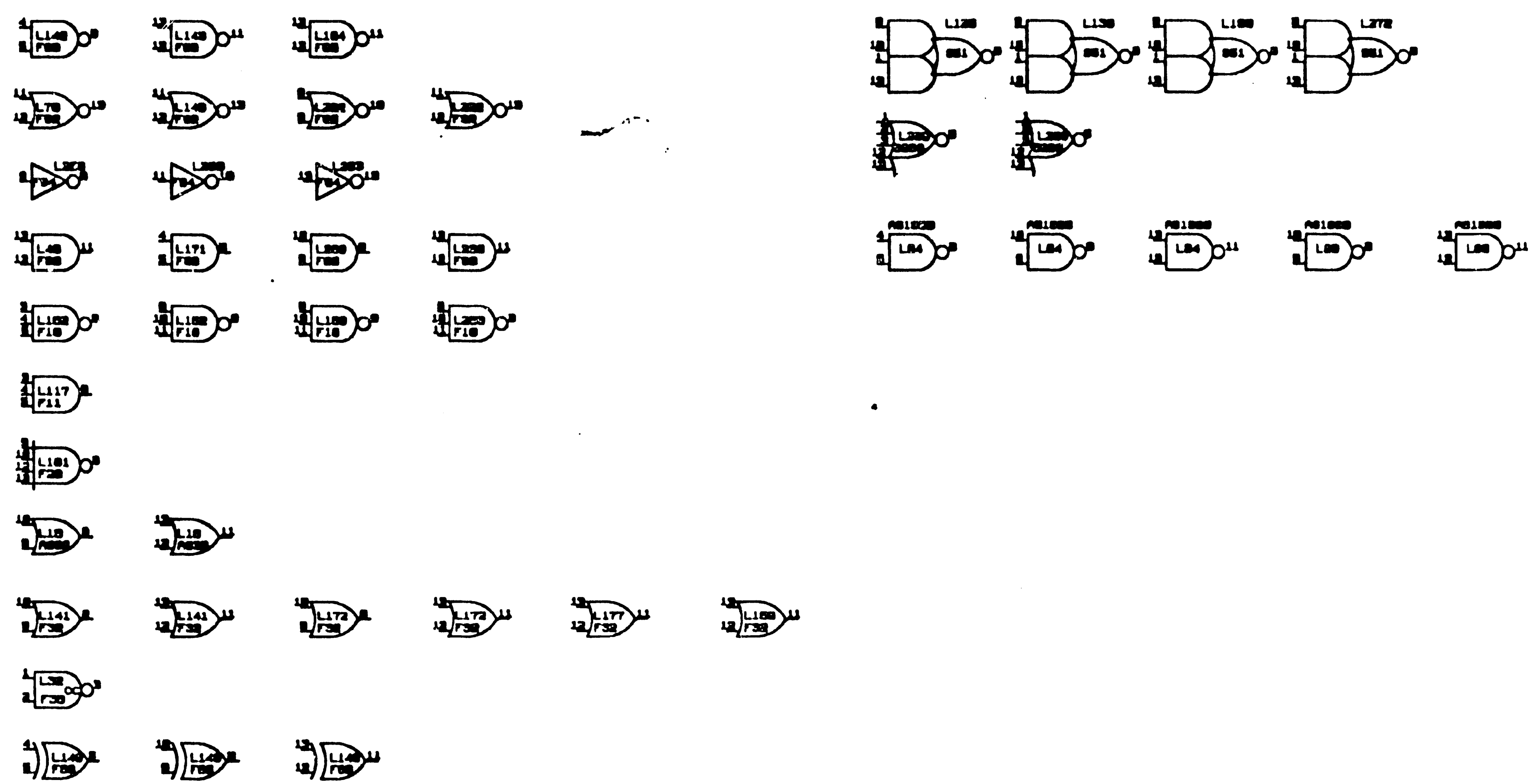
DRAWING

VSXXXSBI..1.21

LAST_MODIFIED=Mon Aug 2? 18:33:18 1985

BACKPLANE CONNECTOR

(WANG) LABORATORIES, INC.	REV: 1
TITLE: SBI	DATE:
ENGINEER:	PAGE:21 OF 22



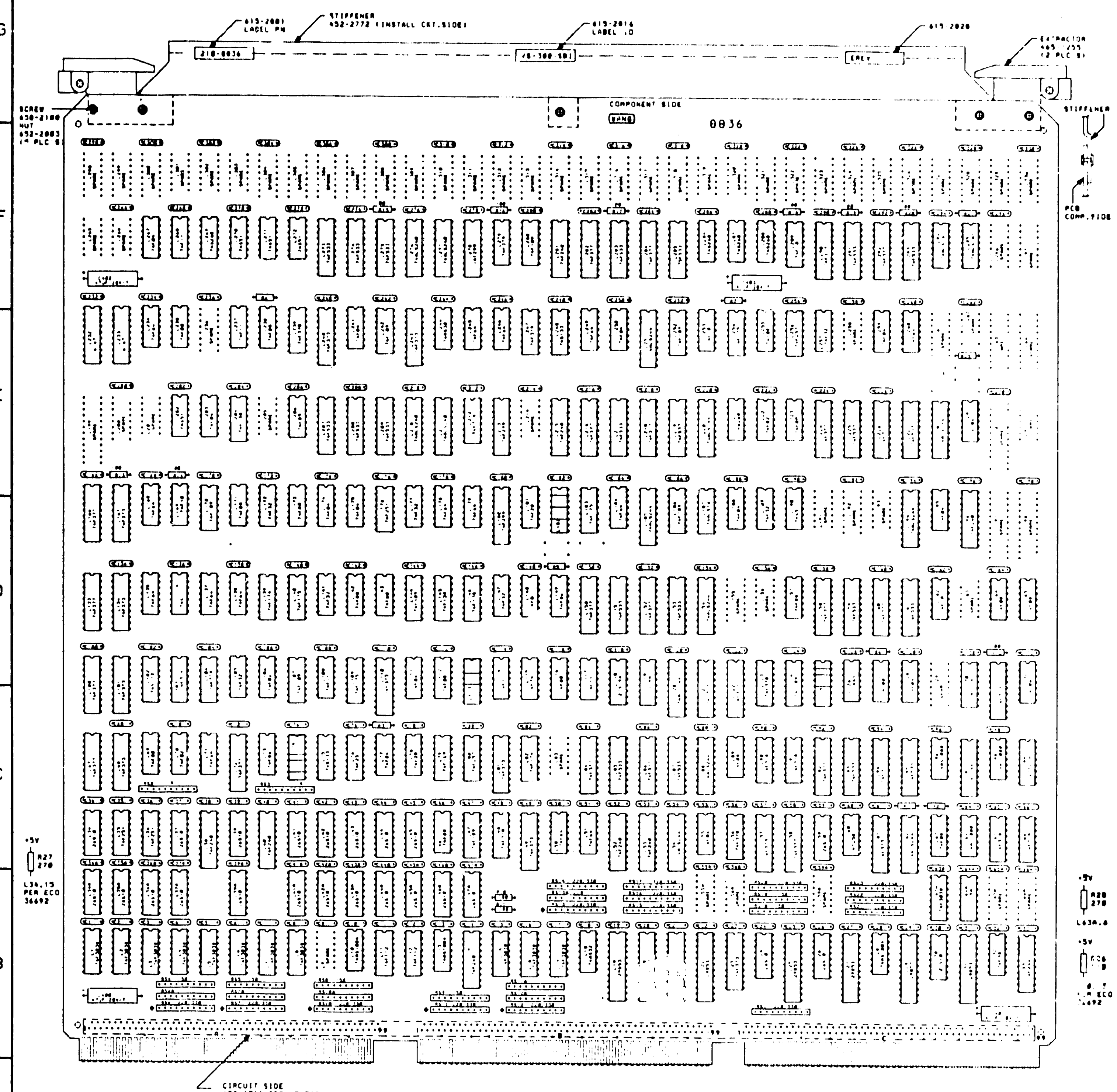
: SPARE GATES

DRAWING

VSXXXSBI.LOGIC.1.22

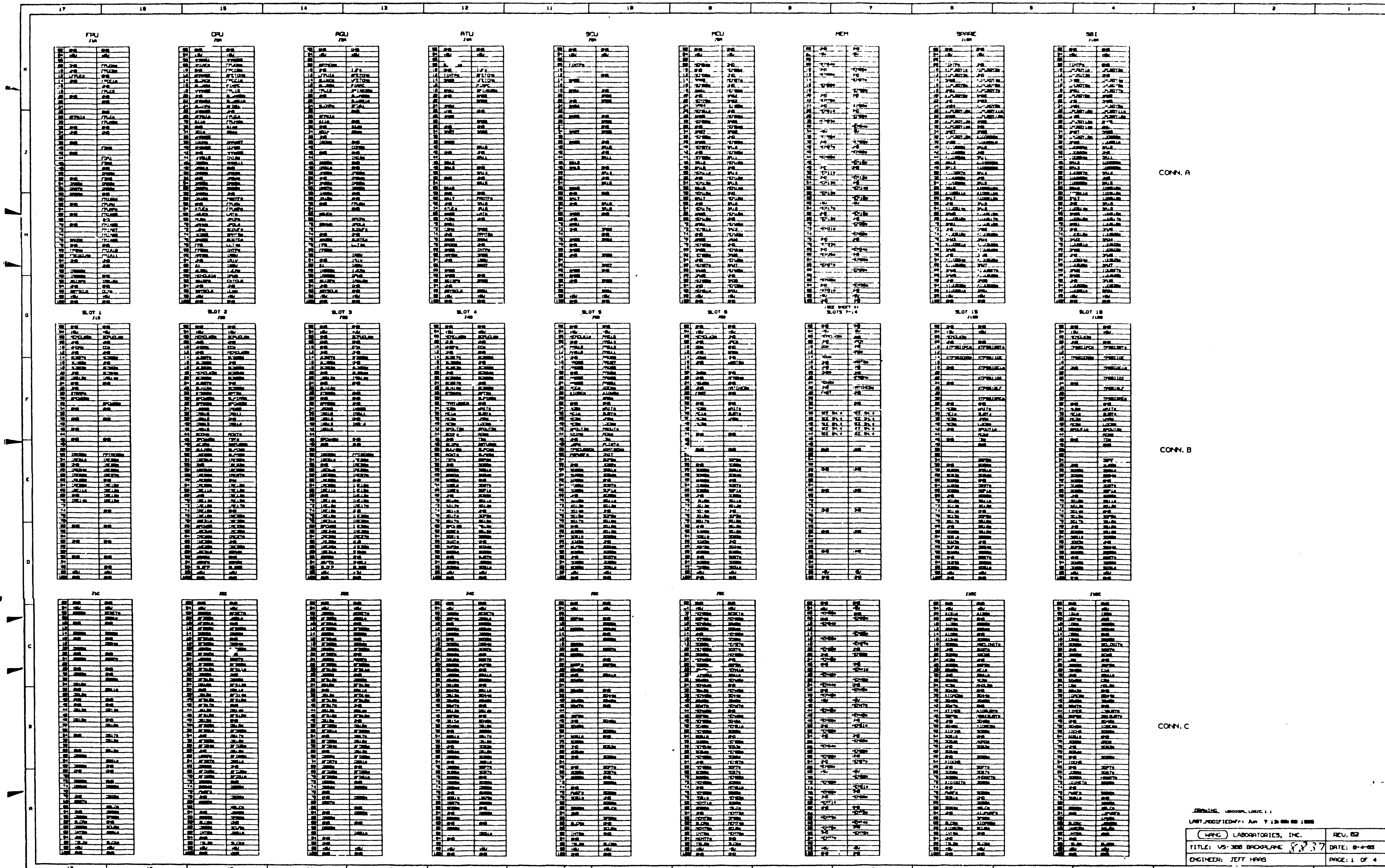
LAST_MODIFIED=Mon Aug 26 16:52:41 1985

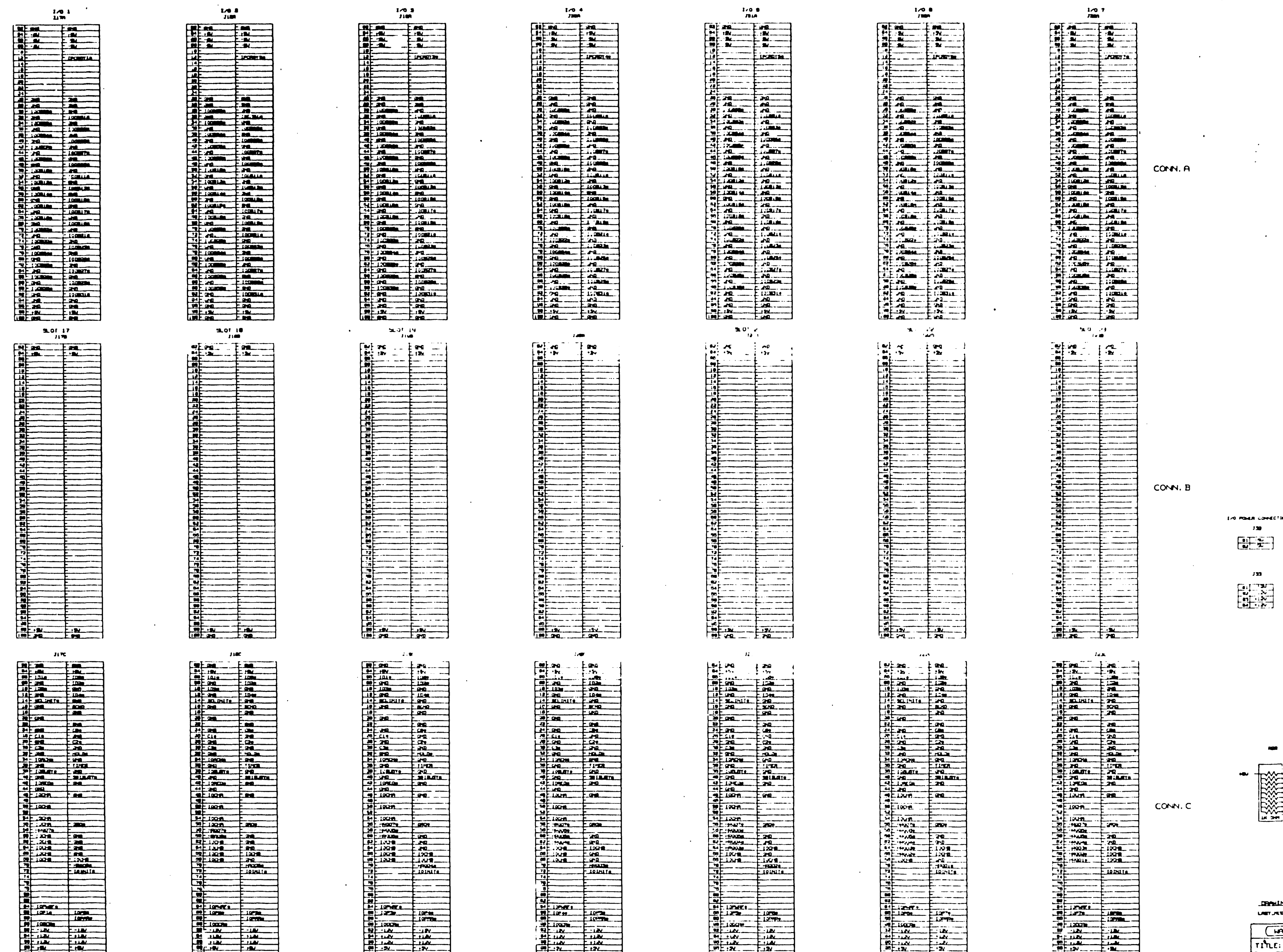
(WANG) LABORATORIES, INC.	REV: /
TITLE: SBI	DATE:
ENGINEER:	PAGE: 22 OF 22



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITORS ARE .047UF EXPRESSED IN MICROFARADS.
   ALL RESISTORS ARE 1K 1/4W.5% EXPRESSED IN OHMS.
   ALL SIPS WITH • SHOULD BE LOADED BACKWARDS
   PIN 1 OF SIP SHOULD BE IN PIN10 ON PCB.
2. RS6A,RS7A,RS10A,RS11A,AND RS12A ARE NOT LOADED.
3. REFERENCE ASSEMBLY PRINT AND/OR SCHEMATICS
   FOR JUMPER CONFIGURATIONS.
   JUMPERS ARE 374-9129.

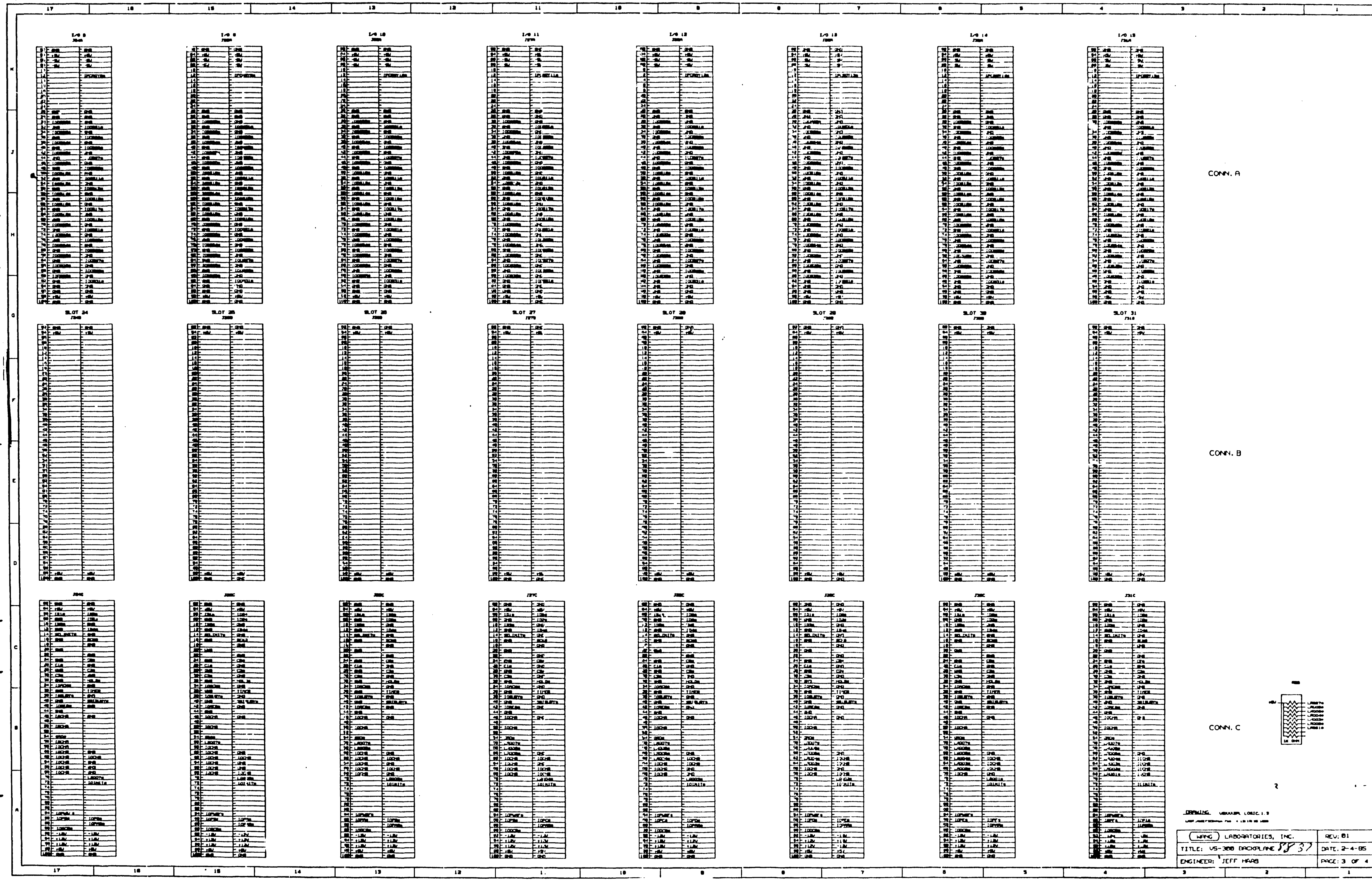
WANG		BY	APPROVED BY
		DWN OCT	E ENGR
		CHK	M ENGR
MATERIAL	MODEL NO. VS300	E C CONTROL	MFG ENGR
	10-214	TITLE VS300 SBI	
FINISH		210-0836	C 8836 3

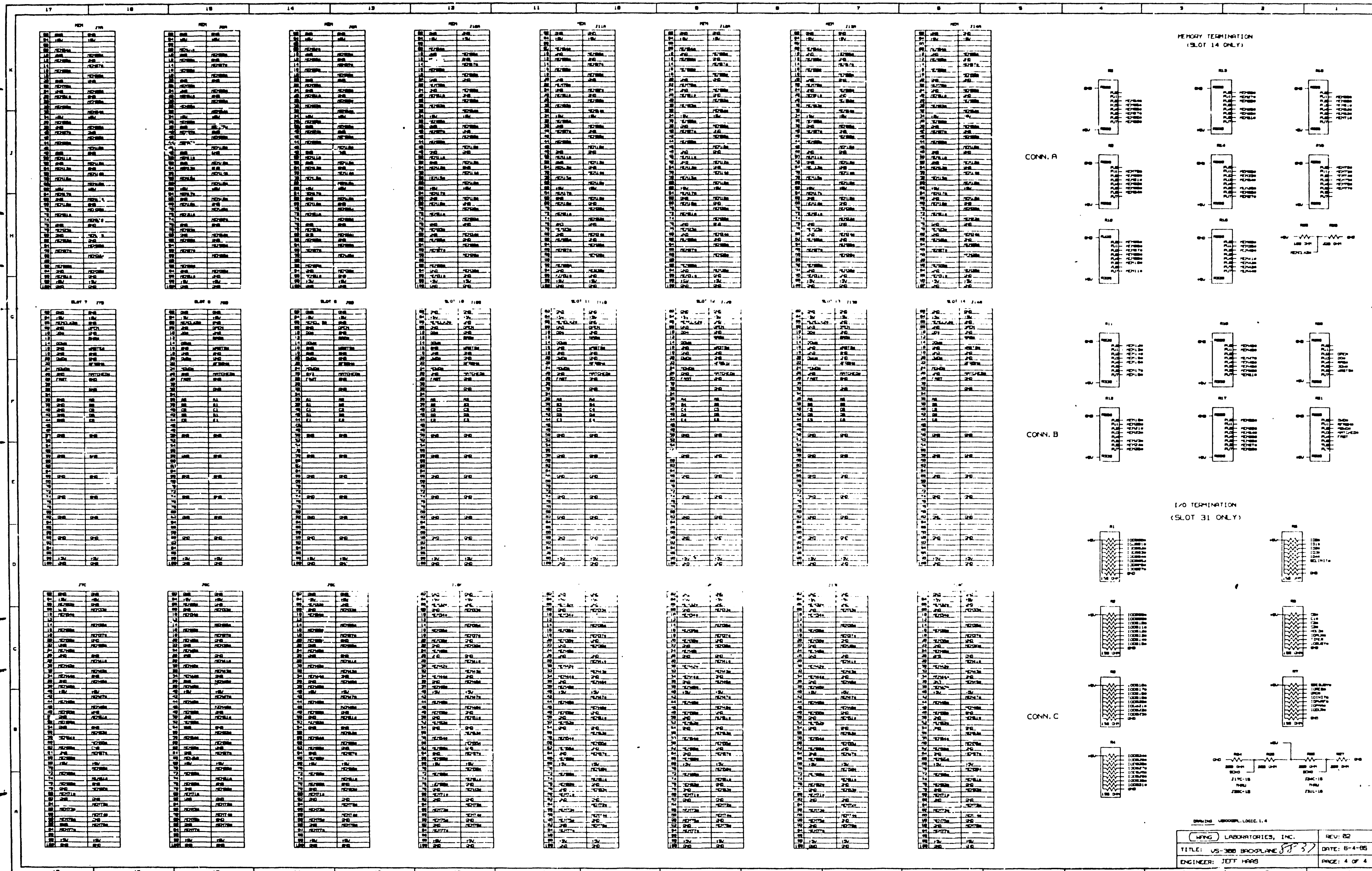

FPU
CPU
AGU
ATU
SCU
MCU
MEM
SPARE
SBI
CONN. A
SLOT 1
SLOT 2
SLOT 3
SLOT 4
SLOT 5
SLOT 6
SLOTS 7-14
SLOT 15
SLOT 16
CONN. B
CONN. C
WANG LABORATORIES, INC.
REV. 02
TITLE: VS-300 BACKPLANE 8837
DATE: 8-4-88
ENGINEER: JEFF HAAS
PAGE: 1 OF 4

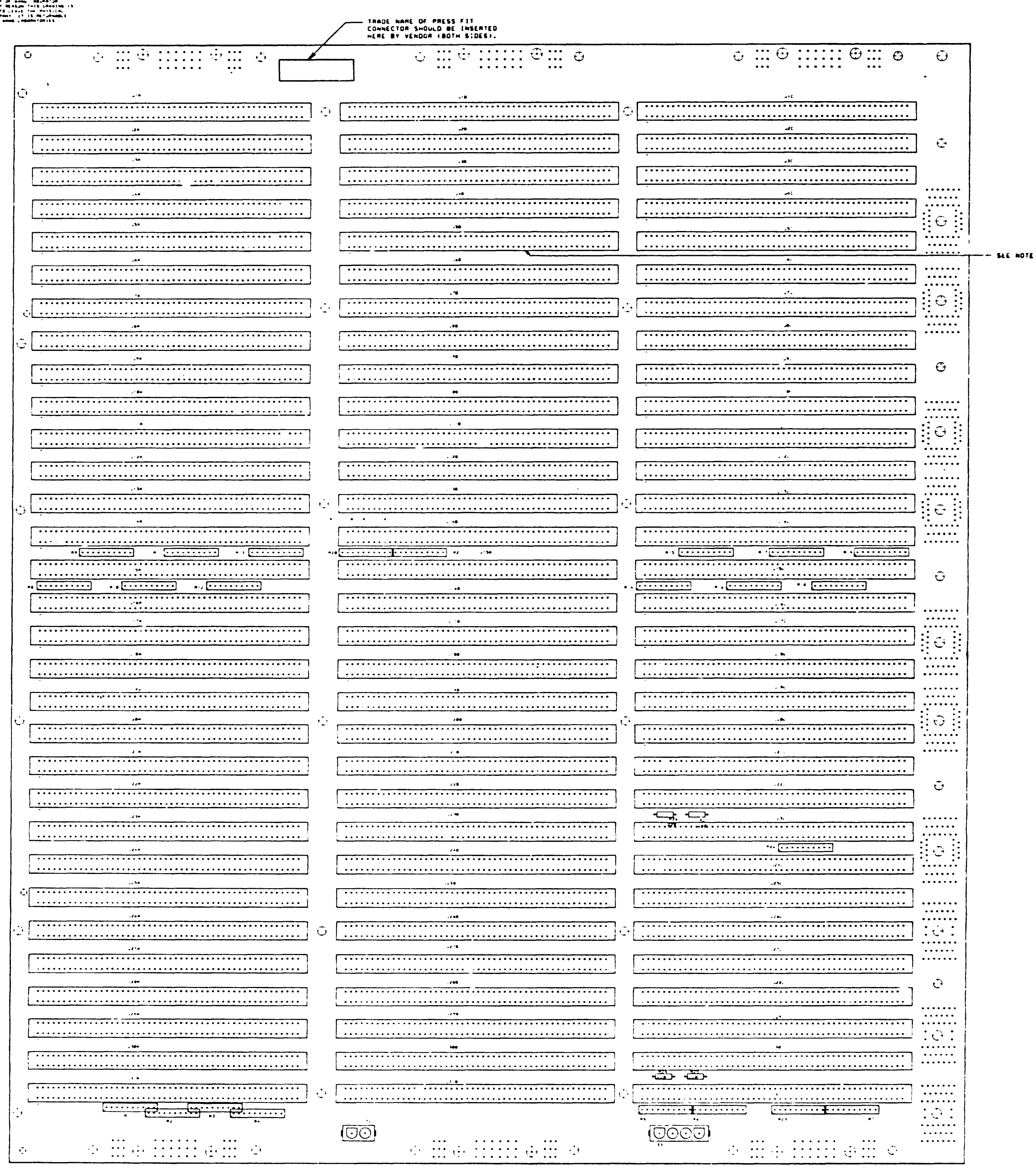


DRAWING VSXXXBPL.LOGIC.1.2

WANG LABORATORIES, INC.	REV: 02
TITLE: VS-300 BACKPLANE 58837	DATE: 6-4-85
ENGINEER: JEFF HAAS	PAGE: 2 OF 4


I/O 8
I/O 9
I/O 10
I/O 11
I/O 12
I/O 13
I/O 14
I/O 15
CONN. A
SLOT 24
SLOT 25
SLOT 26
SLOT 27
SLOT 28
SLOT 29
SLOT 30
SLOT 31
CONN. B
CONN. C
DRAWING
WANG LABORATORIES, INC.
REV: 01
TITLE: VS-300 BACKPLANE
DATE: 2-4-85
ENGINEER: JEFF HAAB
PAGE: 3 OF 4


MEMORY TERMINATION
(SLOT 14 ONLY)
CONN. A
CONN. B
I/O TERMINATION
(SLOT 31 ONLY)
CONN. C
J1YC-18
THRU
J1YC-18
THRU
DRAWING VS300BPL.LOGIC.1.4
WANG LABORATORIES, INC.
REV: 02
TITLE: VS-300 BACKPLANE 8837
DATE: 6-4-85
ENGINEER: JEFF HAAS
PAGE: 4 OF 4



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE EXPRESSED IN OHMS.
2. ALL CONN'S ARE WPN 350-0106 (92 PLCS.).
3. R1-R7 ARE 150 SIP WPN 333-0854.
   R8-R21 ARE 220/330 SIP WPN 333-0007. (SEE NOTE 6).
   R22-R23 ARE 1K SIP WPN 333-0037.
   R24-R27 ARE 220 WPN 330-2023.
4. U32 IS WPN 350-0216.
   U33 IS WPN 350-0215.
5. U50 IS WPN 350-0105 (1 PLACE)
6. ALL 220/330 SIPS (WPN 333-0007)
   MUST BE MOUNTED BACKWARDS.
   (PIN 10 OF RESISTORS INTO PIN 1 OF BOARD).

WANG

BY	DATE	APPROVED BY	DATE
DWN		E ENGR	
CHK		M ENGR	
E C CONTROL		MFG ENGR	

MATERIAL

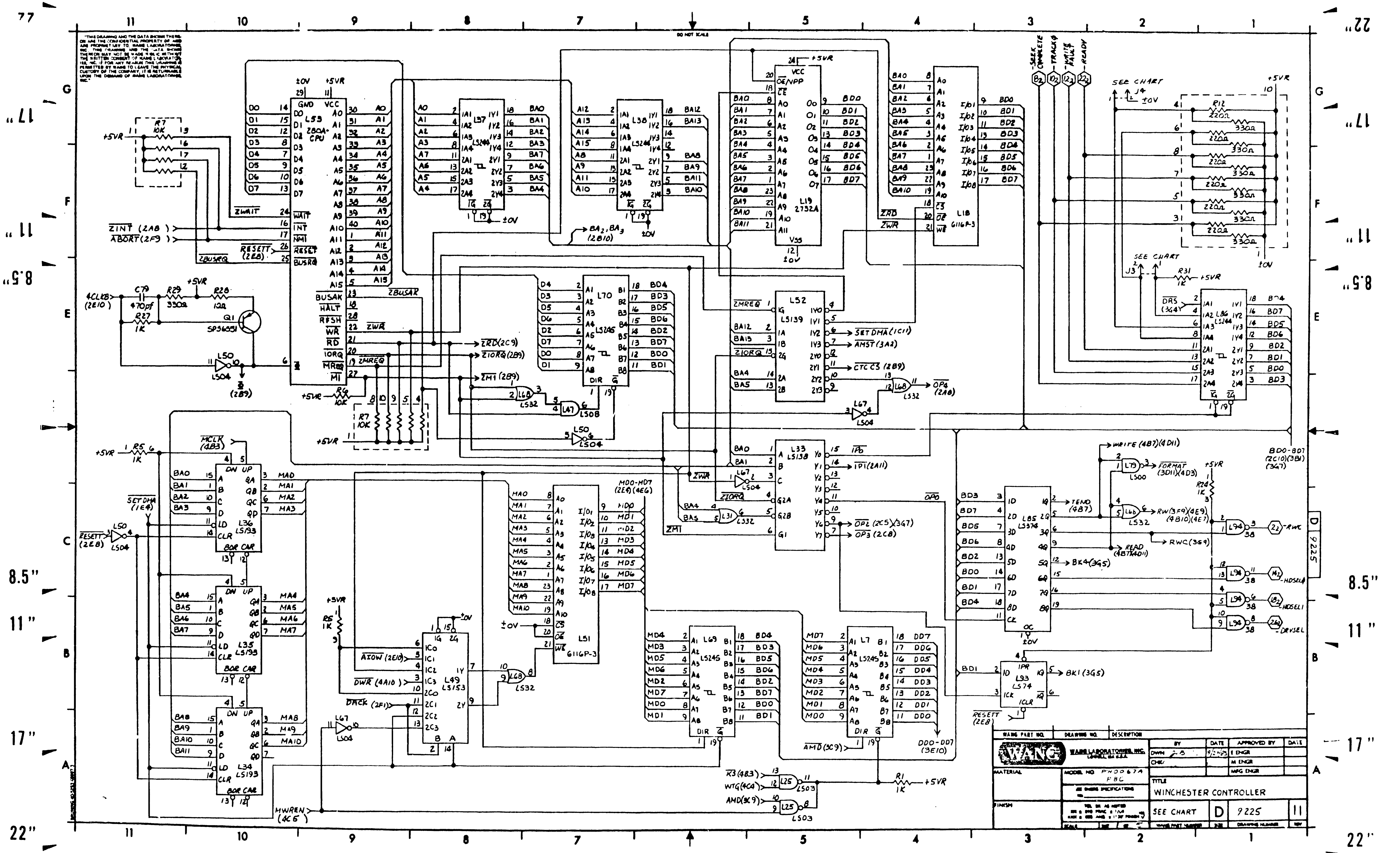
FINISH

MODEL NO. VS300

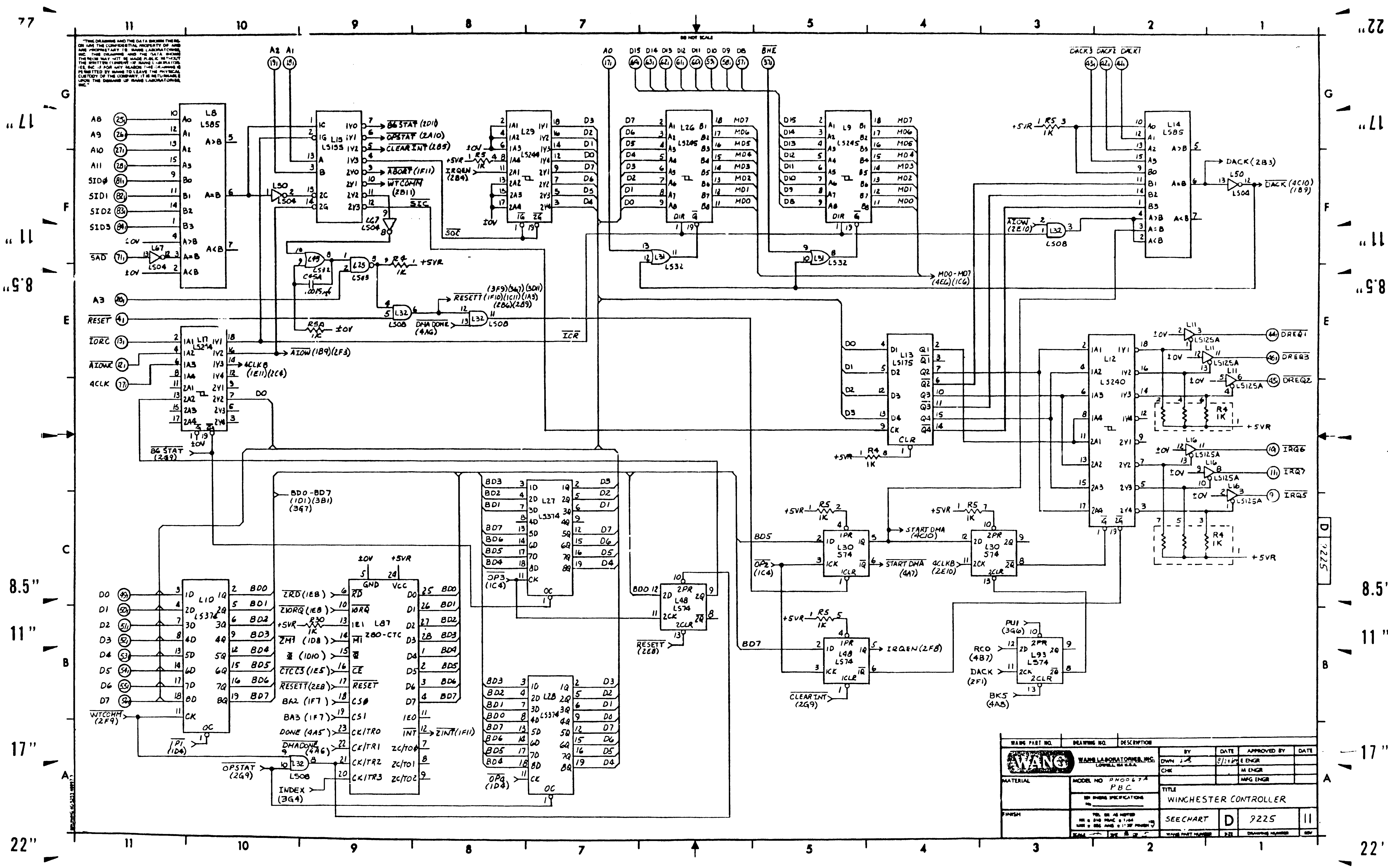
10-213

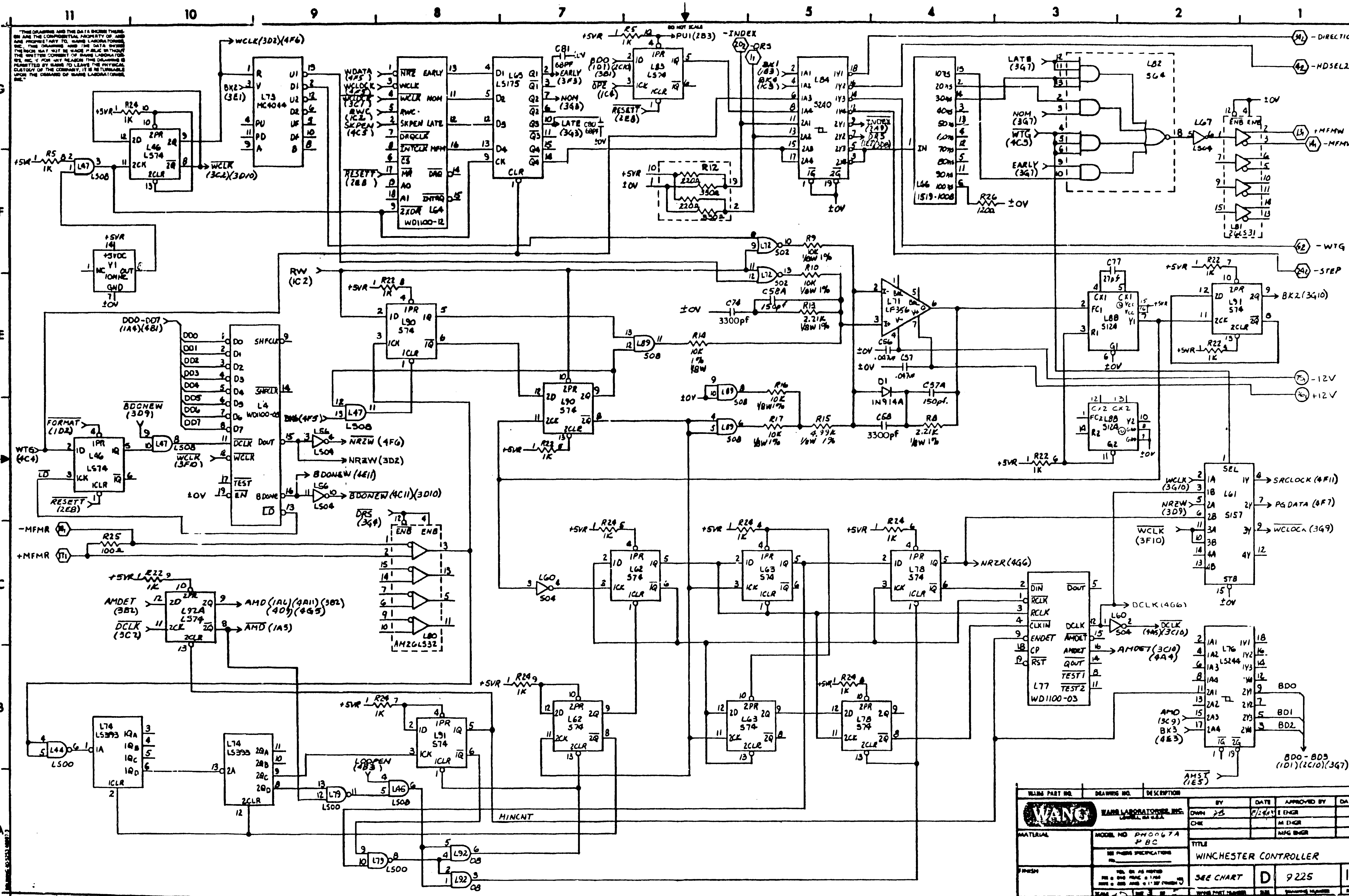
TITLE: BACKPLANE ML ASSEMBLY DRAWING

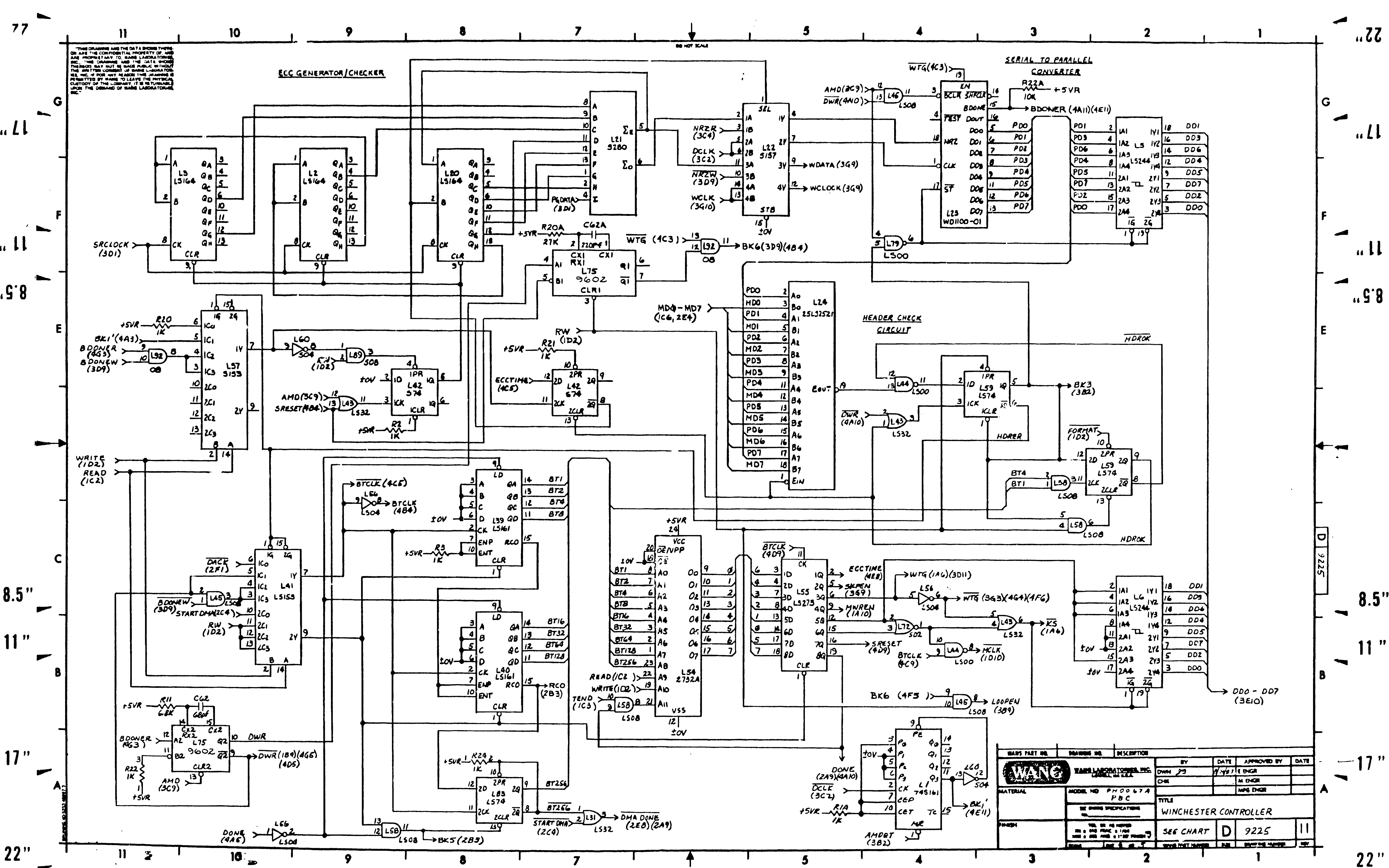
210-8037-R2 | C | 8837 | 4



WINCHESTER CONTROLLER
WANG LABORATORIES, INC.
SEE CHART
D
9225
11
DO NOT SCALE


WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
MODEL NO. PH00674
PBC
WINCHESTER CONTROLLER
SEE CHART
D
9225
11

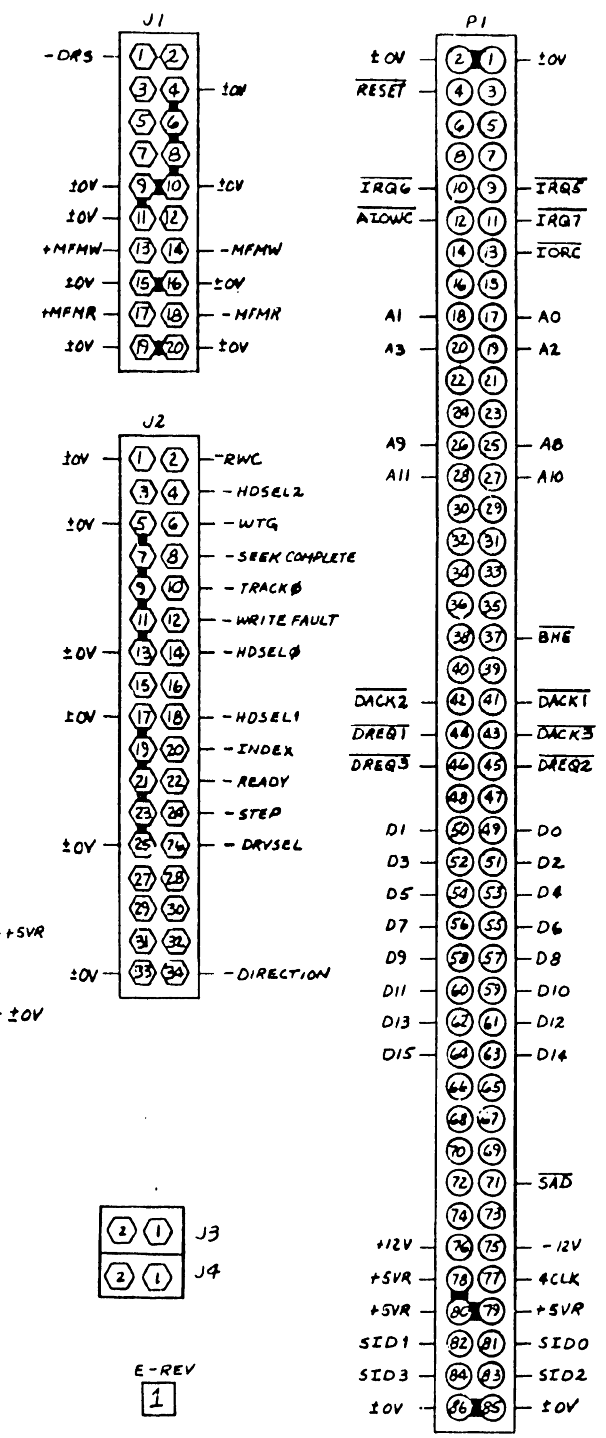

WANG LABORATORIES, INC.
LOWELL, MA U.S.A.
MODEL NO PM0067A PBC
TITLE WINCHESTER CONTROLLER
SEE CHART
D 9225
11
L73 MC4044
L64 WD1100-12
L65 LS175
L83 LS74
L84 S240
L66 1519-1008
L82 S64
L81 26LS31
L4 WD100-05
L71 LF356
L88 S124
L61 S157
L77 WD1100-03
L76 LS244
L80 AM26LS32
L74 LS393
L62 S74
L63 S74
L78 S74
L90 S74
L91 S74
L92A LS74
L46 LS74
L47 LS08
L44 LS00
L79 LS00
L75 LS00
L89 S08
L72 S02
L60 S04
L56 LS04
L67 LS04
WCLK (3D2)(4F6)
BK2 (3E1)
-INDEX
-DIRECTION
-HDSEL2
+MFMW
-MFMW
-WTG
-STEP
-12V
+12V
BK2 (3G10)
SRCLOCK (4F11)
PG DATA (4F7)
WCLOCK (3G9)
NRZR (4G6)
DCLK (4G6)
AMD (1A1)(2A11)(3B2)(4D9)(4G5)
AMD (1A5)
NRZW (4F6)
NRZW (3D2)
BDONEW (4E11)
BDONEW (4C11)(3D10)
BD0 - BD3 (1D1)(2C10)(3G7)
DD0-DD7 (1A4)(4B1)
-MFMR
+MFMR
HINCNT
WINCHESTER CONTROLLER

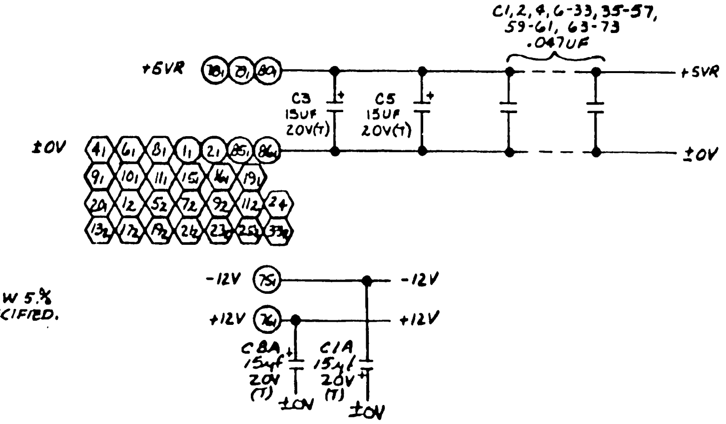

ECC GENERATOR/CHECKER
SERIAL TO PARALLEL CONVERTER
HEADER CHECK CIRCUIT
DO NOT SCALE
WANG
WANG LABORATORIES, INC.
WINCHESTER CONTROLLER
SEE CHART
D
9225
11
DDO - DD7 (3E10)

DO NOT SCALE

MNEMONICS	COORD
AIOWC	2E11
AØ	2G7
A1, A2	2G10
A8-A11	2G11
A3	2E11
BHE	2G5
DACK1 - DACK3	2G2
-DIRECTION	3G1
DREQ1 - DREQ3	2E1
-DRS	3G5
-DRVSEL	1B1
DØ-D7	2B11
D8-D15	2G6
-HDSELØ	1C1
-HDSEL1	1B1
-HDSEL 2	3G1
-INDEX	3G6
IORC	2E11
IRQ5-IRQ7	2D1
+MFMR	3C11
-MFMR	3C11
+MFMW	3G1
-MFMW	3G1

MNEMONICS	COORD.
-READY	1G3
RESET	2E11
-RWC	1C1
SAD	2F11
-SEEK COMPLETE	1G3
SIDØ - SID3	2F11
-STEP	3F1
-TRACKØ	1G3
-WRITE FAULT	1G3
-WTG	3F1
4CLK	2D11





NOTE:
1. ALL RESISTORS ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

WINCHESTER DRIVE JUMPER CONFIGURATION

DRIVE		JUMPER	
SIZE	VENDOR	PIN	PIN
10MEG.	ALL	NOT REQUIRED	
30MEG.	ATASI	J4-1	J4-2
30MEG.	QUANTUM	J3-2	J4-2

E-REV
1

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

BY	DATE	APPROVED BY	DATE
DWN [illegible]	3/[illegible]	E ENGR [illegible]	[illegible]
CHK. [illegible]	3/16	M ENGR	
		MFG ENGR	

MATERIAL

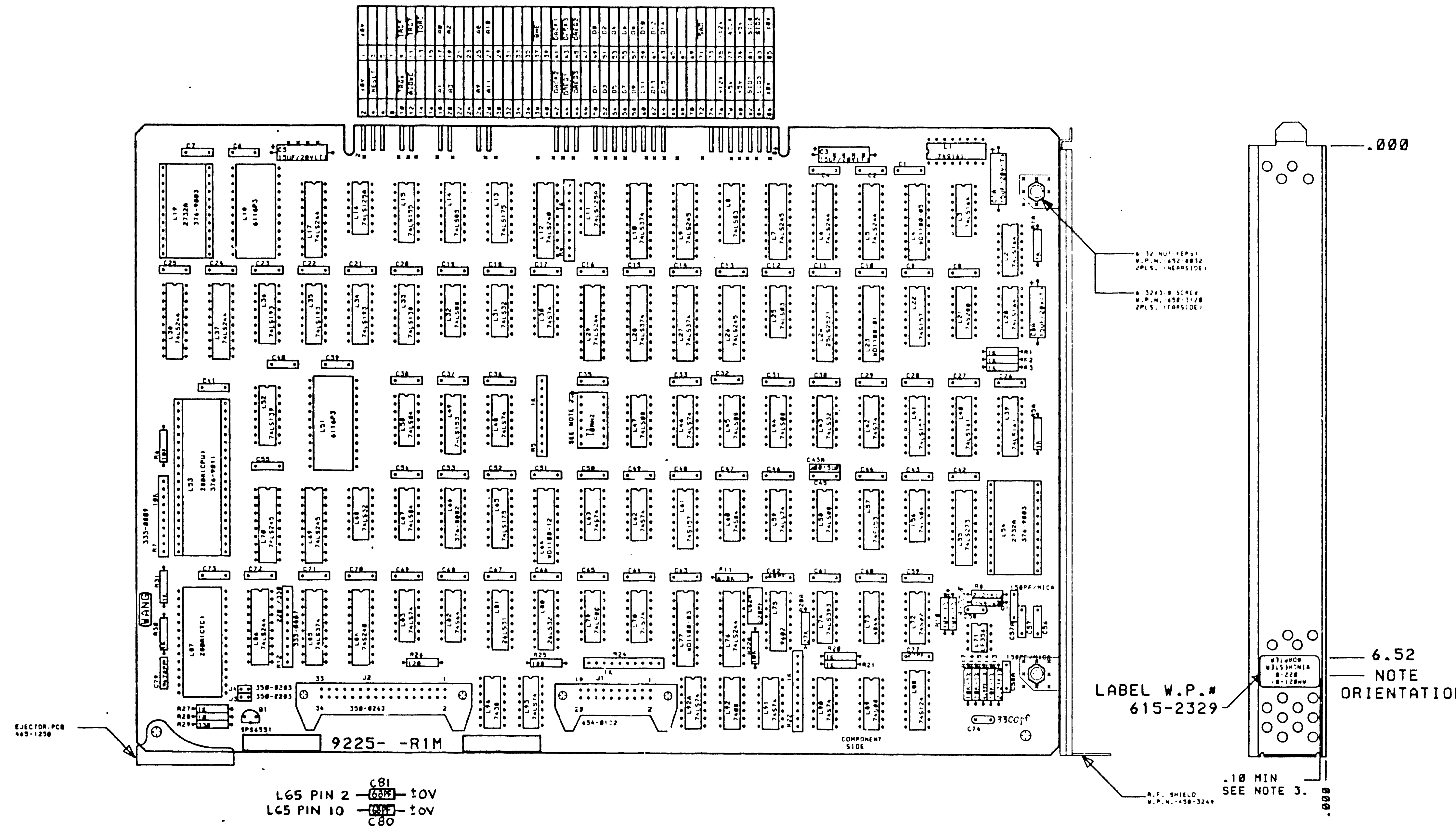
MODEL NO. PH0067A PBC

FINISH

TITLE: WINCHESTER CONTROLLER

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
SEE CHART	D	9225	11

D 9225

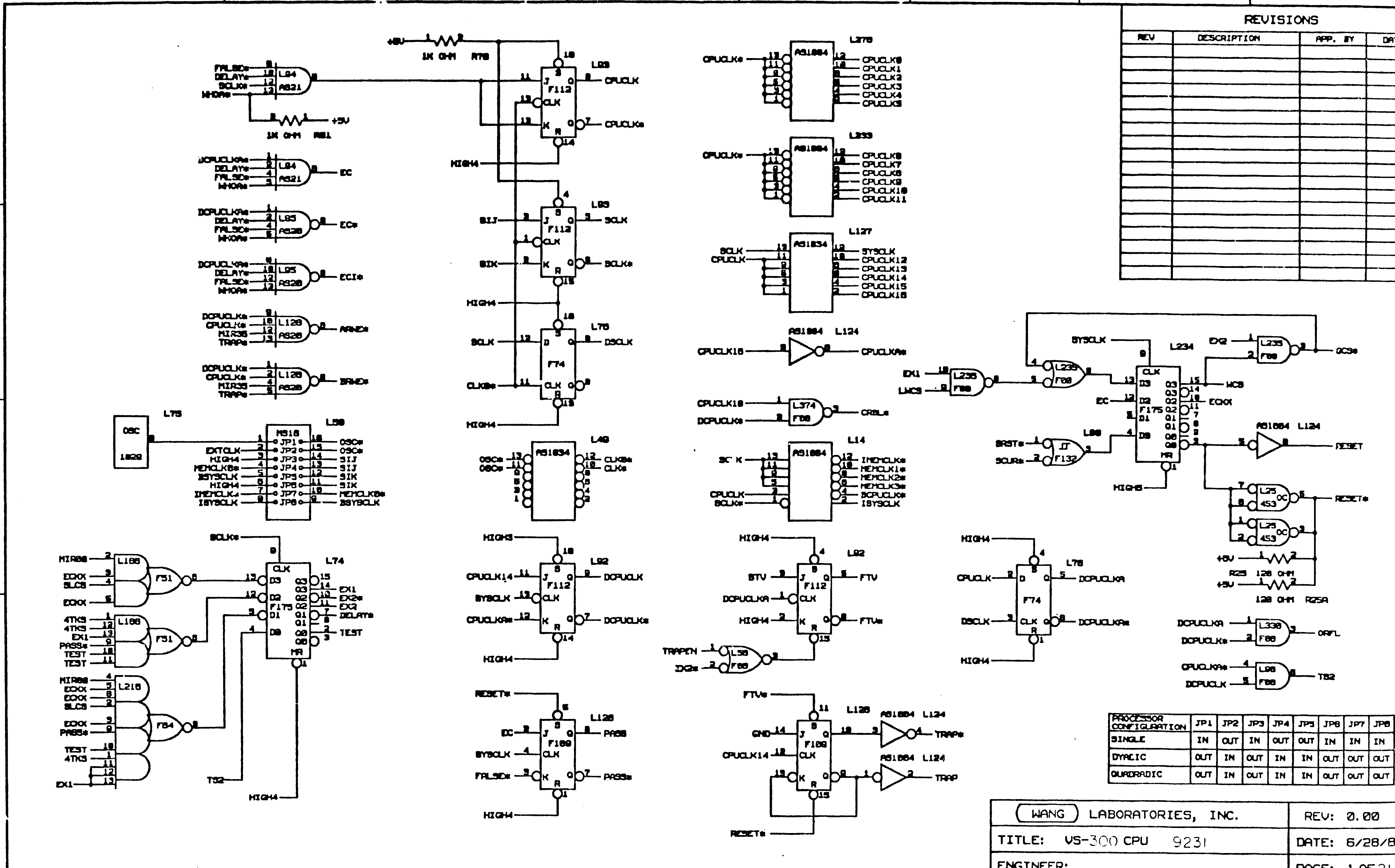


NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITORS ARE .047 P/N 300-1966, EXPRESSED IN MICROFARADS.
   ALL RESISTORS ARE 1/4W, 5%, EXPRESSED IN OHMS.
   ALL RESISTOR NETWORKS ARE 333-0037.
2. IC PAD (376-9000) MUST BE INSTALLED PRIOR TO Y1.
3. .10 MIN. DIMENSION HAS BEEN DESIGNATED TO AVIOD OVERLAP FROM ADJACENT SHIELD.

WANG LABORATORIES INC. LOWELL, MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN S.M.	12/82	E ENGR K.D.	12/82
		CHK A.W.	8/16/83	M ENGR	
MATERIAL	MODEL NO. PHOC67A PBC	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-213	TITLE WINCHESTER CONTROLLER BOARD ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED .XX+/- .010 FRAC. +/- 1/64 .XXX+/- .005 ANG +/- 1 30'	210-9225-R1 (WANG PART NUMBER)	C (SIZE)	9225 (DRAWING NUMBER)	5 (REV)
	SCALE 1/1 SHT 4 OF 9				

VS-XXX CPU INDEX

WANG LABORATORIES, INC.	REV: R0.0
TITLE: VS-300 CPU INDEX 9231	DATE: 02/13/84
ENGINEER:	PAGE: 1 OF 1

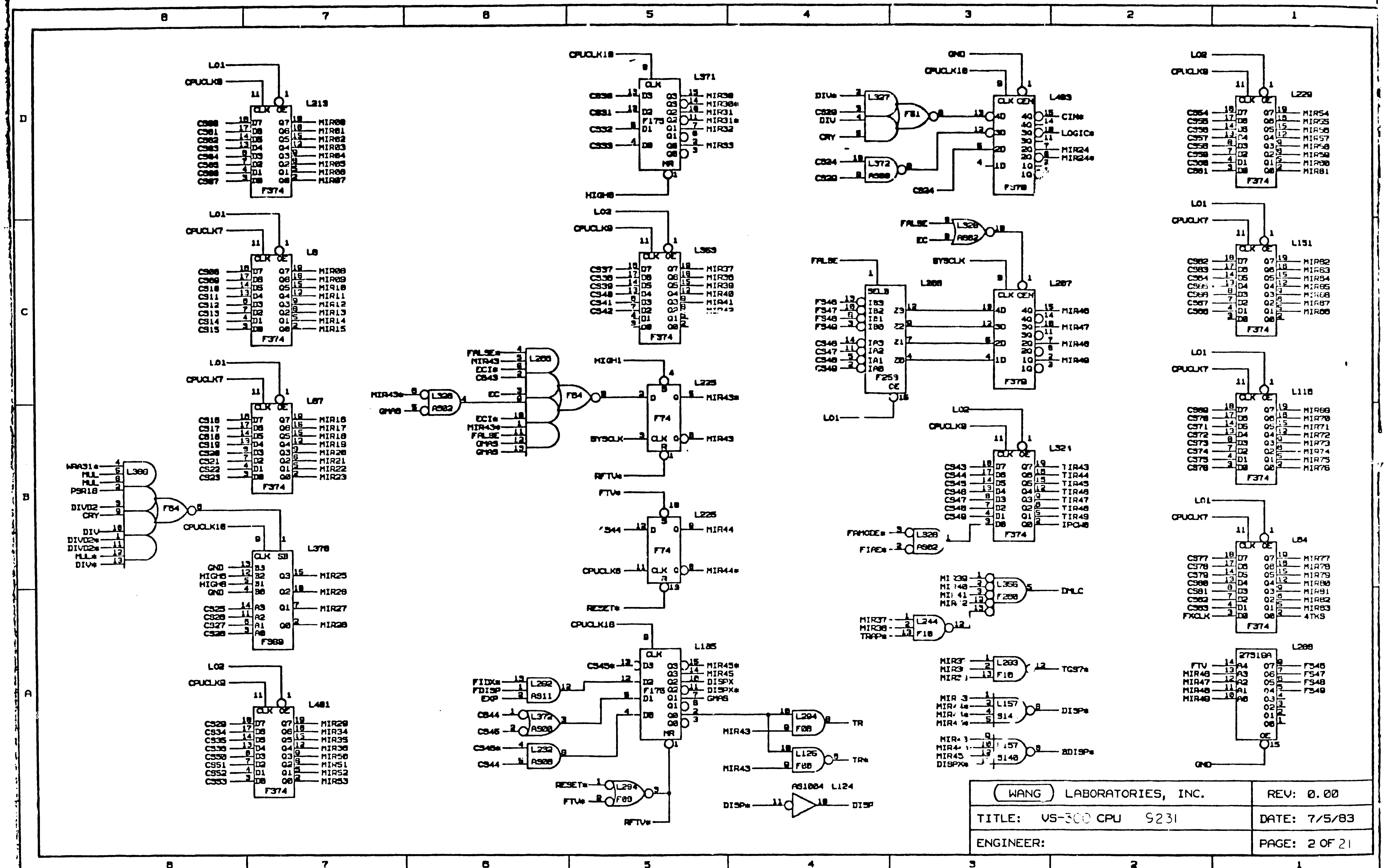


REVISIONS

REV	DESCRIPTION	APP. BY	DATE

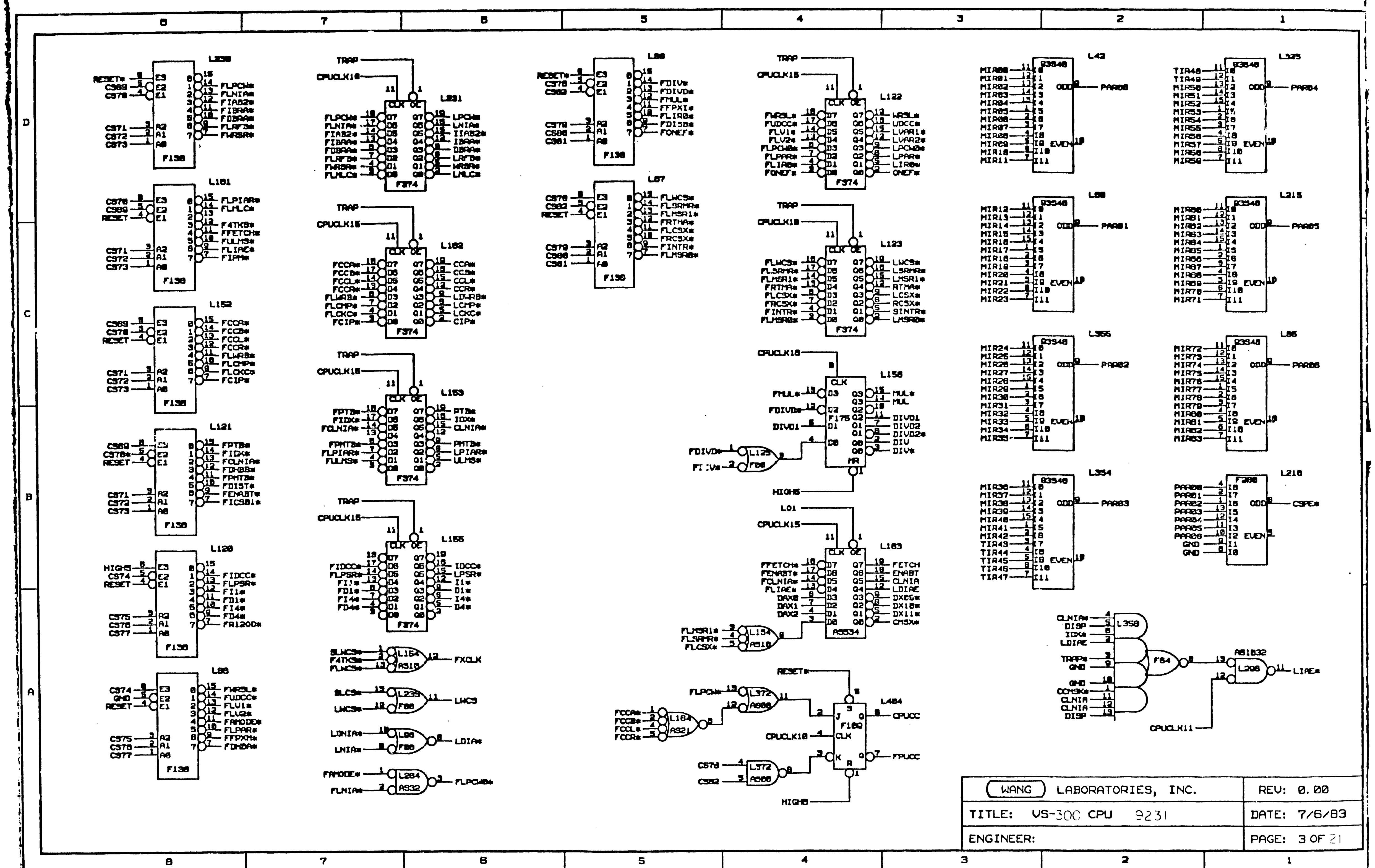
PROCESSOR CONFIGURATION	JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8
SINGLE	IN	OUT	IN	OUT	OUT	IN	IN	IN
DYADIC	OUT	IN	OUT	IN	IN	OUT	OUT	OUT
QUADRADIC	OUT	IN	OUT	IN	IN	OUT	OUT	OUT

WANG LABORATORIES, INC.	REV: 0.00
TITLE: VS-300 CPU 9231	DATE: 6/28/83
ENGINEER:	PAGE: 1 OF 21



WANG LABORATORIES, INC.	REV: 0.00
TITLE: VS-300 CPU 9231	DATE: 7/5/83
ENGINEER:	PAGE: 2 OF 21

8.5"
11"
17"
22"



WANG LABORATORIES, INC.

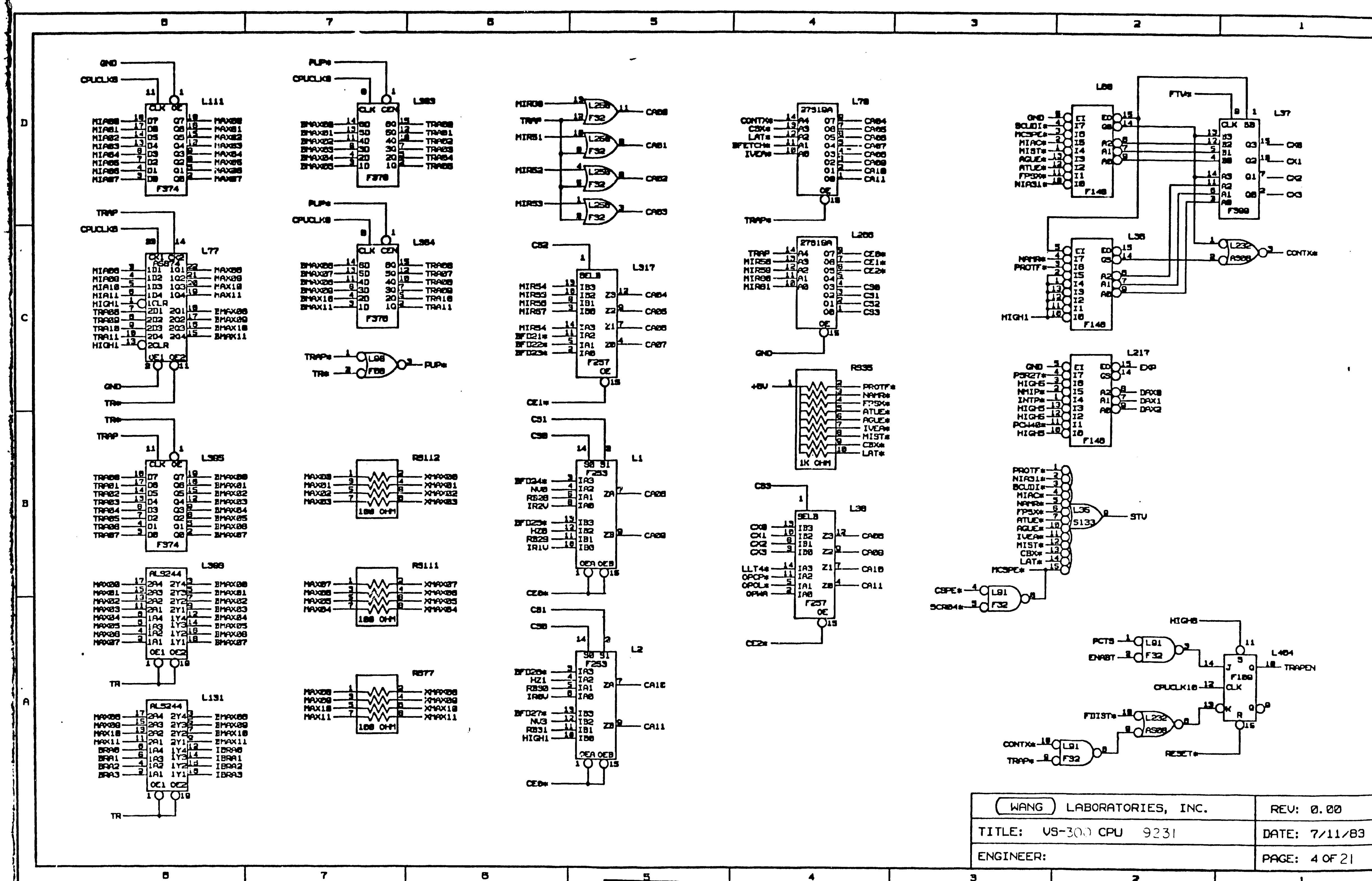
REV: 0.00

TITLE: VS-300 CPU 9231

DATE: 7/6/83

ENGINEER:

PAGE: 3 OF 21



WANG LABORATORIES, INC.

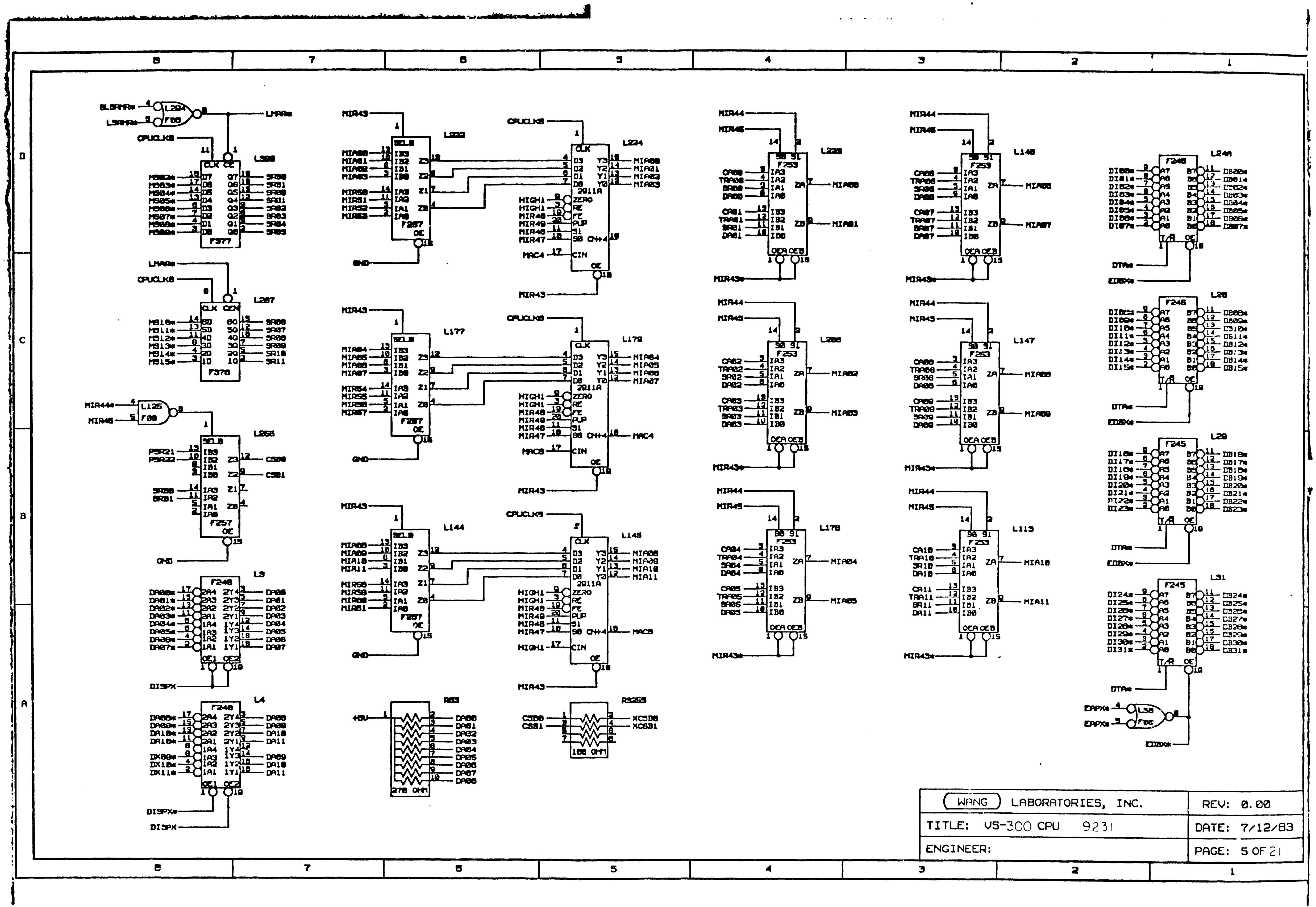
REV: 0.00

TITLE: VS-300 CPU 9231

DATE: 7/11/83

ENGINEER:

PAGE: 4 OF 21



WANG LABORATORIES, INC.

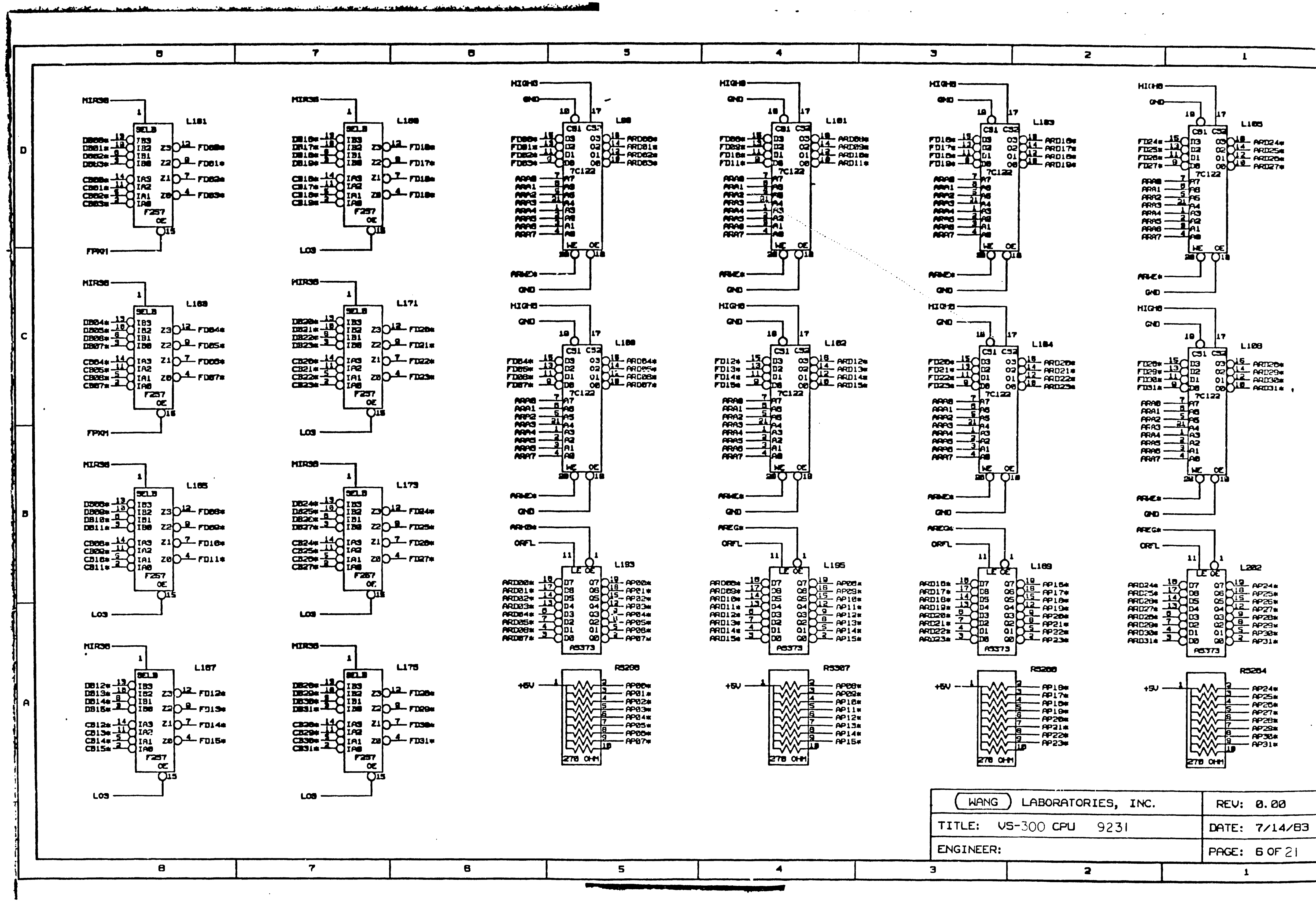
REV: 0.00

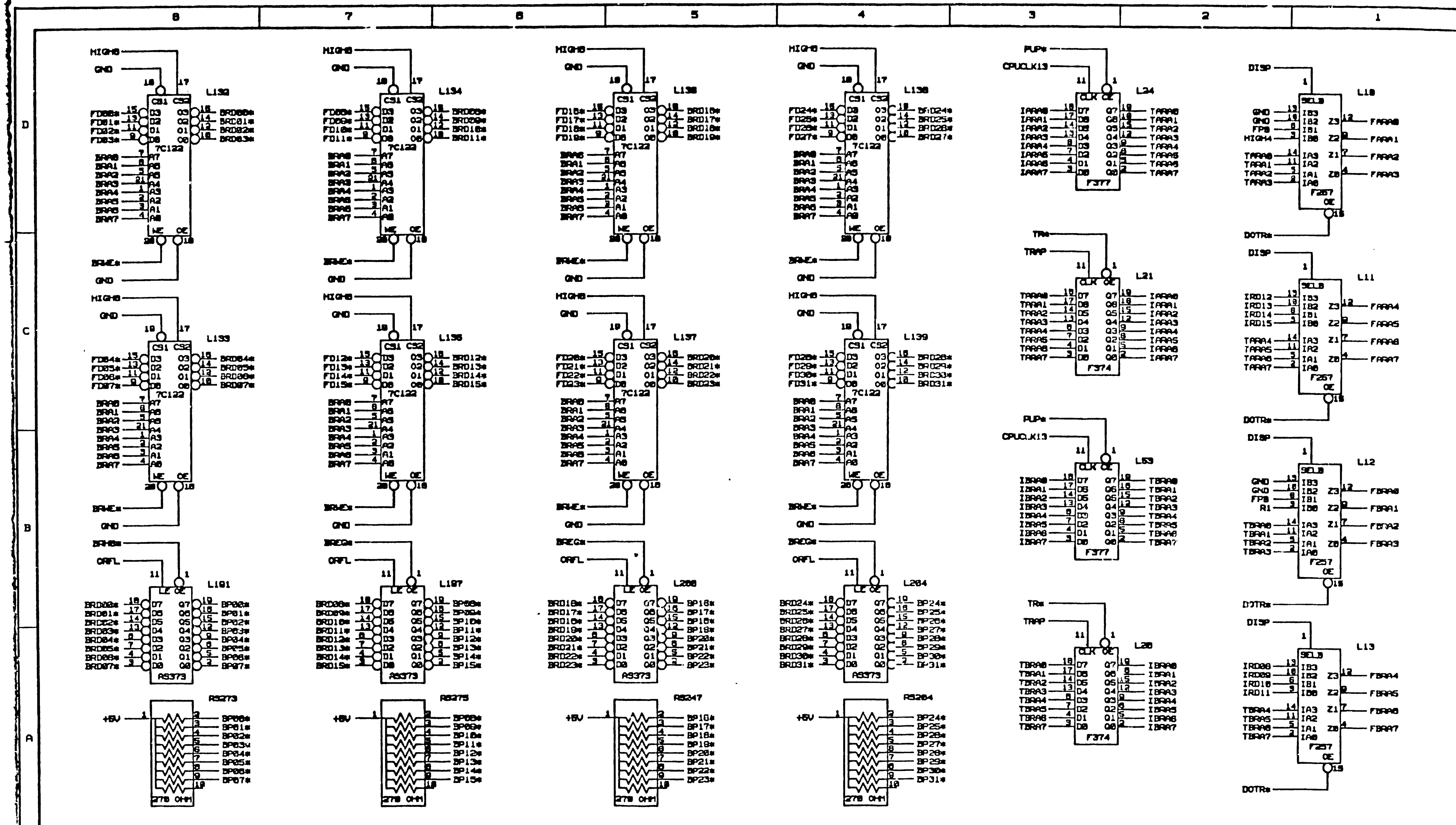
TITLE: VS-300 CPU 9231

DATE: 7/12/83

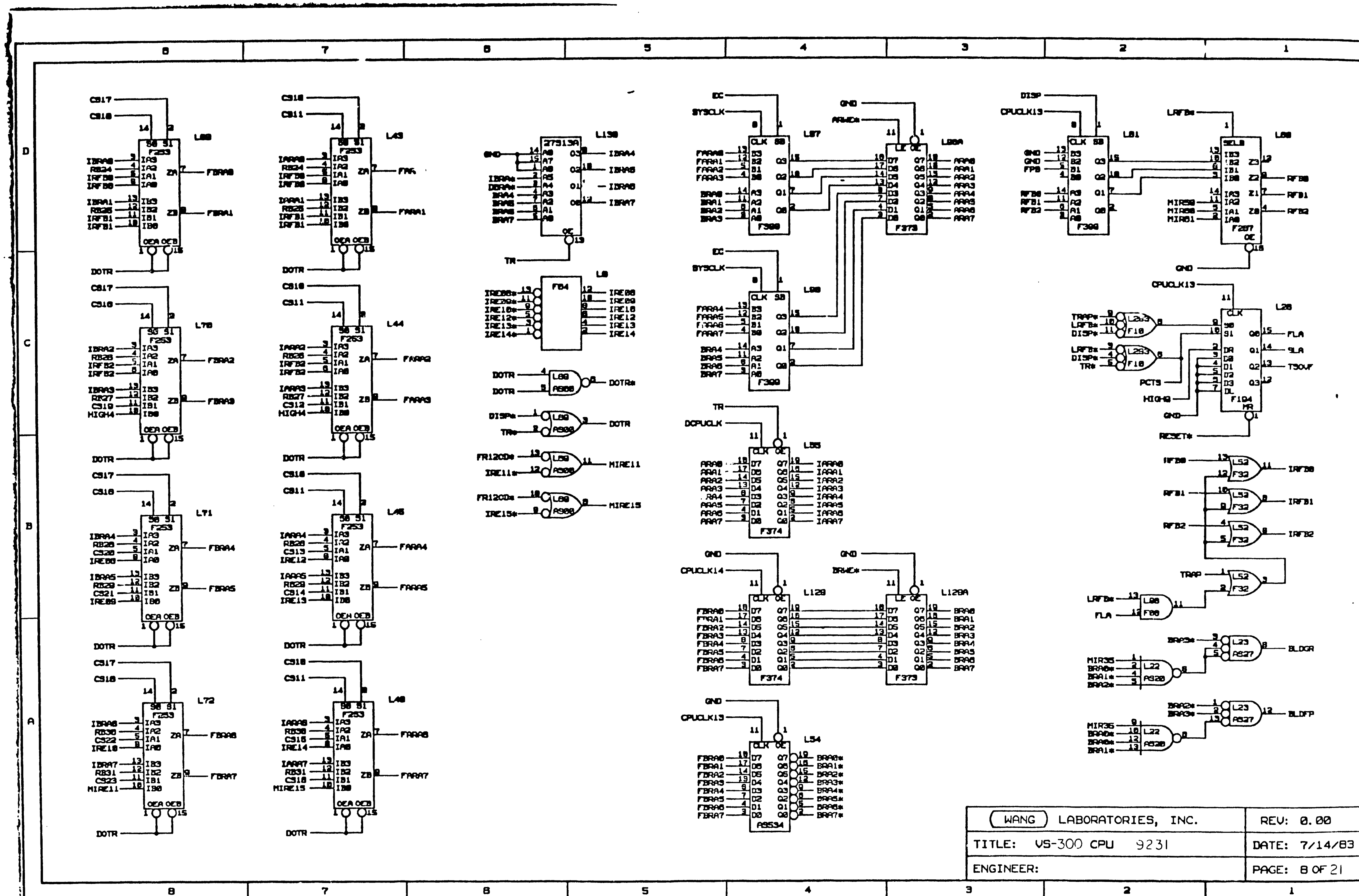
ENGINEER:

PAGE: 5 OF 21


WANG LABORATORIES, INC.
TITLE: VS-300 CPU 9231
ENGINEER:
REV: 0.00
DATE: 7/14/83
PAGE: 6 OF 21
8 7 6 5 4 3 2 1
D C B A
F257
7C122
AS373
L181
L169
L171
L173
L175
L183
L185
L187
L193
L195
L199
L202
270 OHM
MIR30
HIGH0
GND
ARWE*
ORFL
+5V
LO3



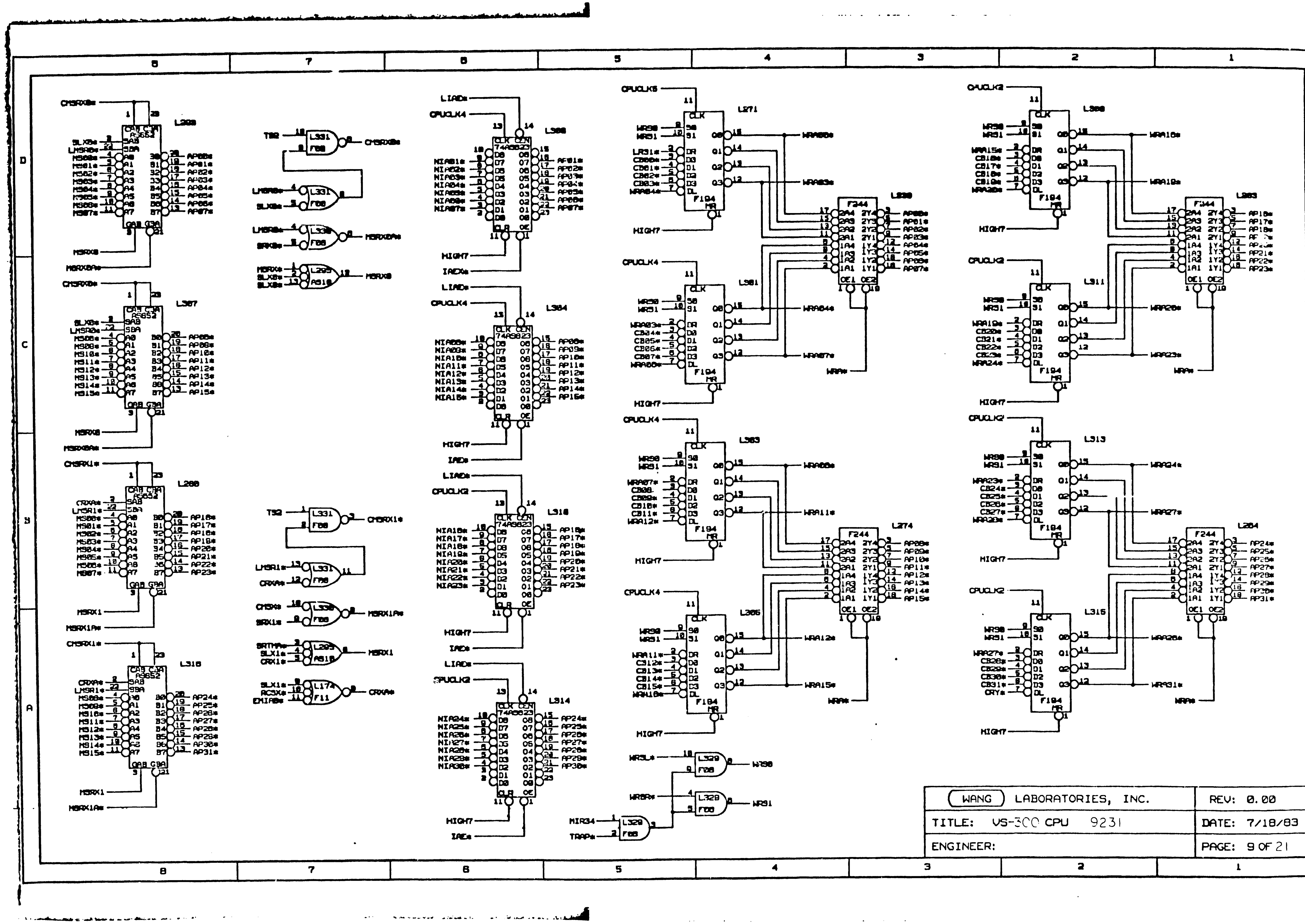
WANG LABORATORIES, INC.	REV: 0.00
TITLE: VS-300 CPU 9231	DATE: 7/14/83
ENGINEER:	PAGE: 7 OF 21



WANG LABORATORIES, INC. | REV: 0.00

TITLE: VS-300 CPU 9231 | DATE: 7/14/83

ENGINEER: | PAGE: 8 OF 21



WANG LABORATORIES, INC.

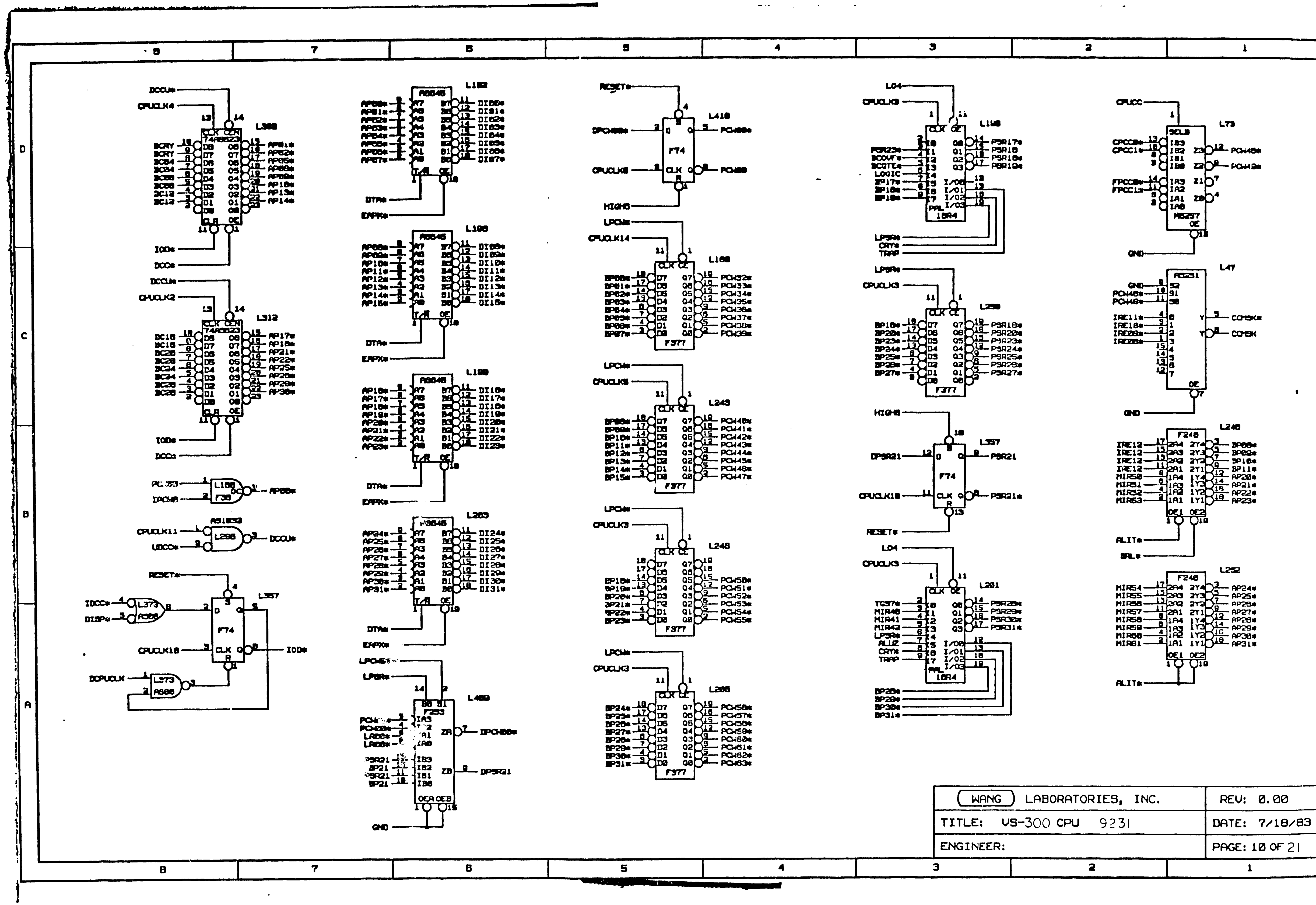
REV: 0.00

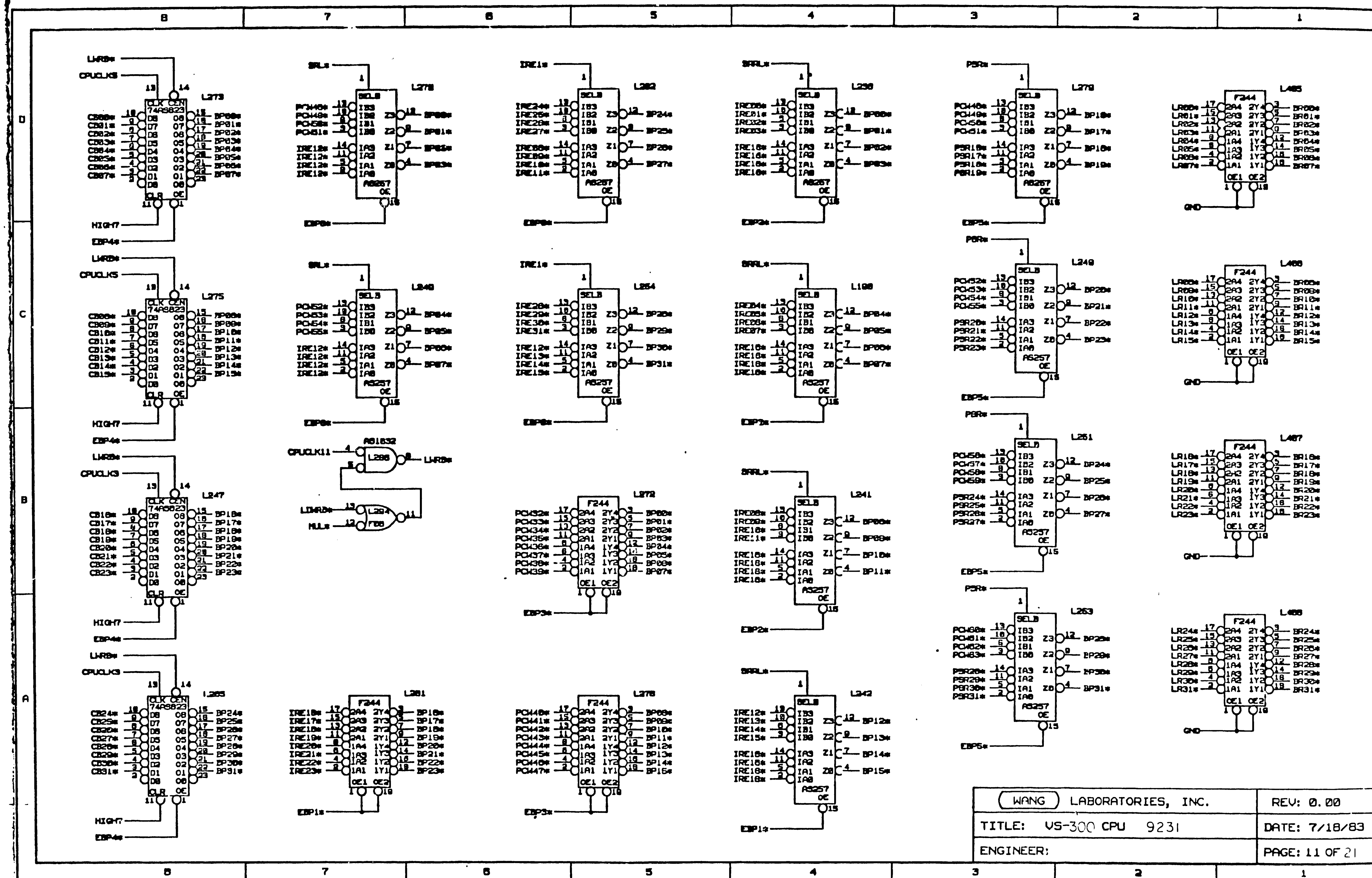
TITLE: VS-300 CPU 9231

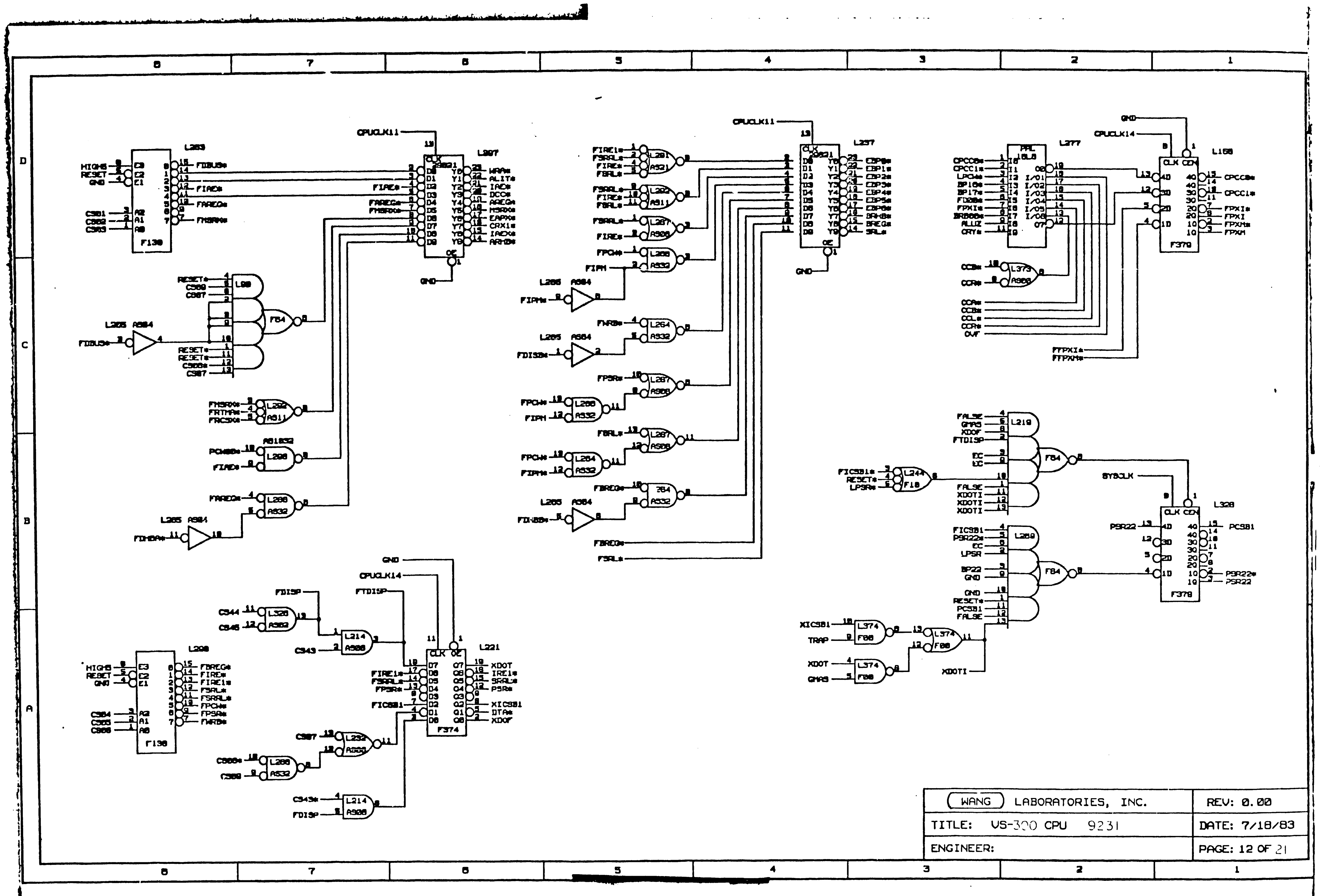
DATE: 7/18/83

ENGINEER:

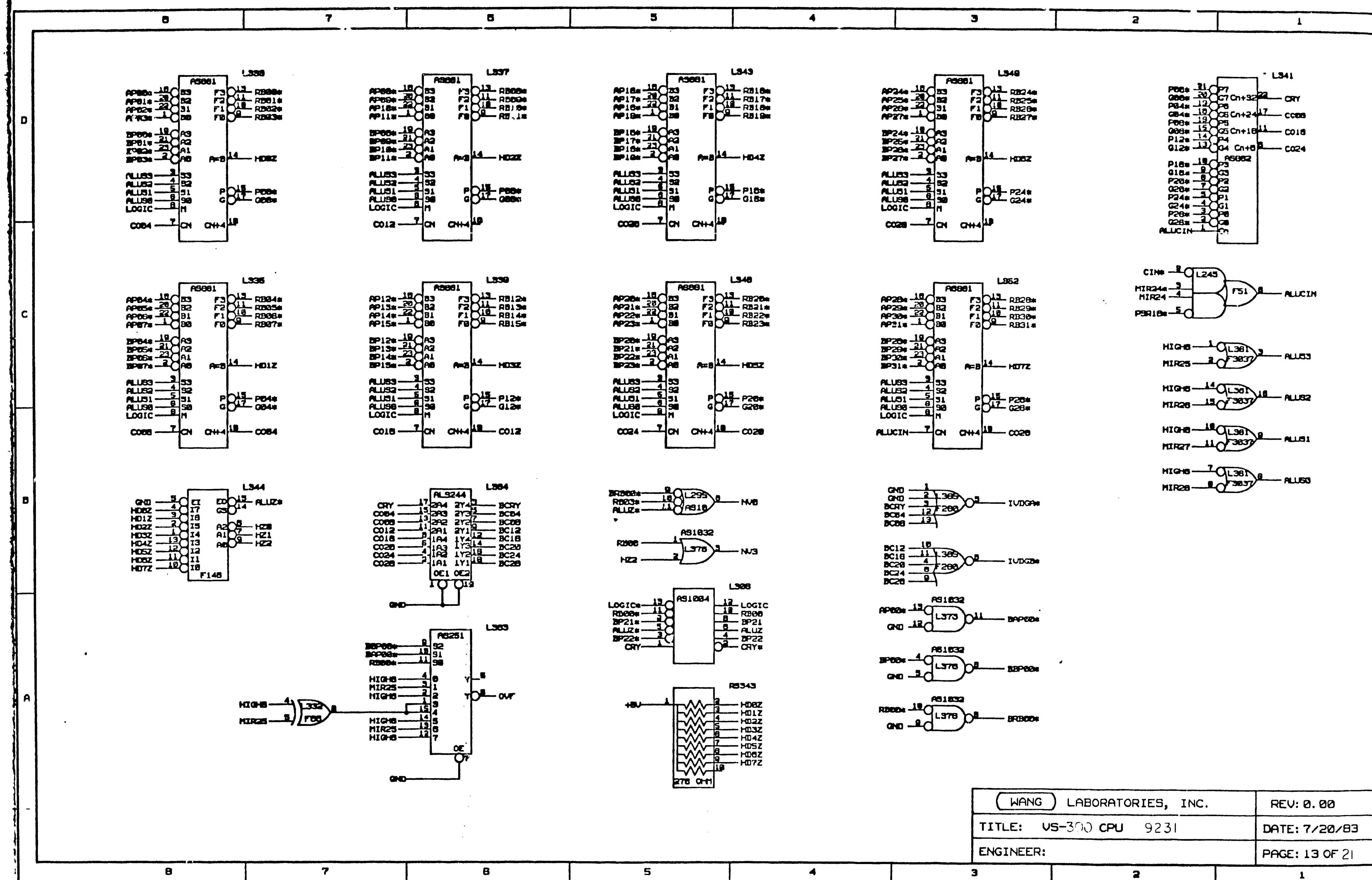
PAGE: 9 OF 21


WANG LABORATORIES, INC.
REV: 0.00
TITLE: VS-300 CPU 9231
DATE: 7/18/83
ENGINEER:
PAGE: 10 OF 21


WANG LABORATORIES, INC.
REV: 0.00
TITLE: VS-300 CPU 9231
DATE: 7/18/83
ENGINEER:
PAGE: 11 OF 21



WANG LABORATORIES, INC.
REV: 0.00
TITLE: VS-300 CPU 9231
DATE: 7/18/83
ENGINEER:
PAGE: 12 OF 21



WANG LABORATORIES, INC.

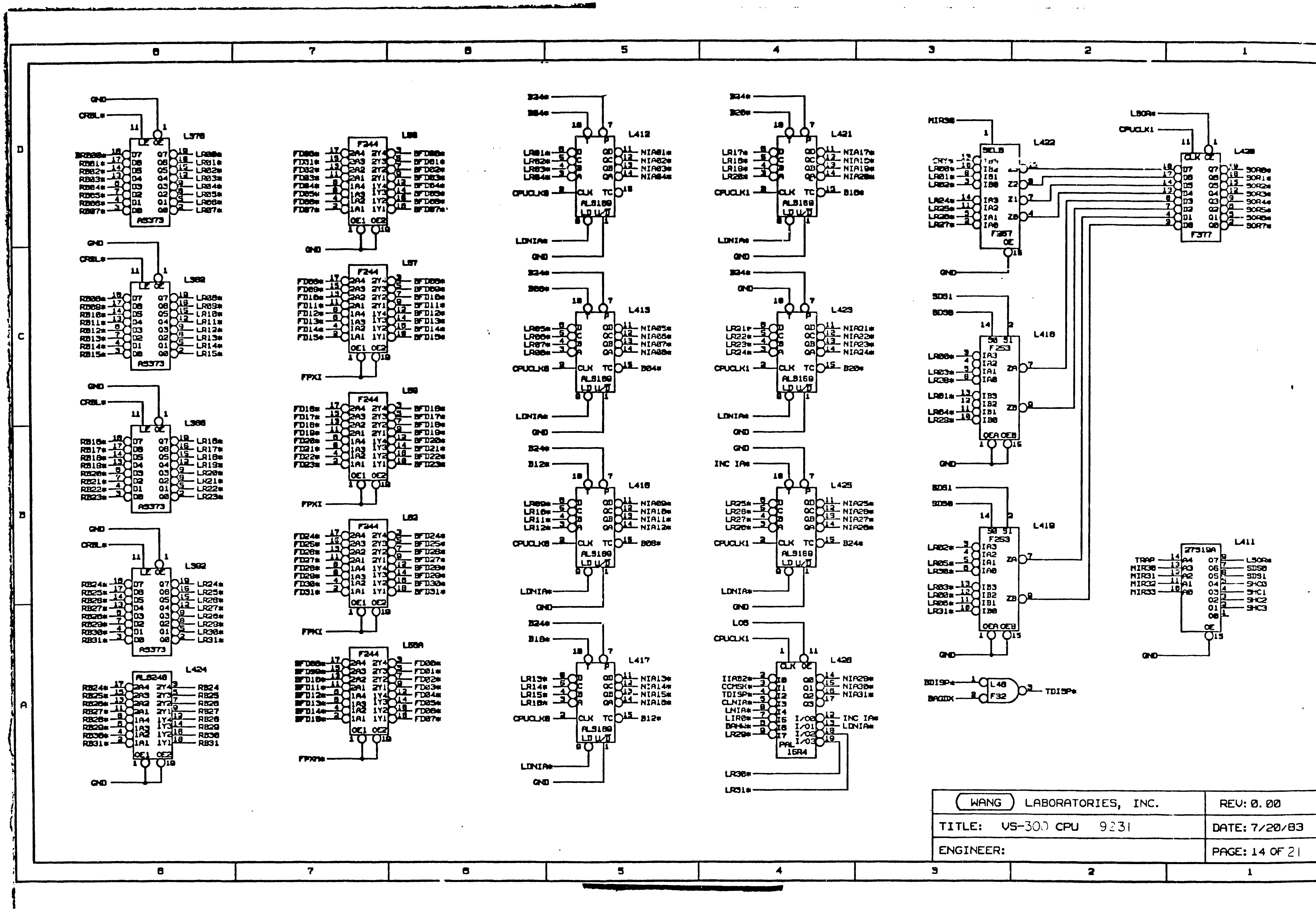
REV: 0.00

TITLE: VS-300 CPU 9231

DATE: 7/20/83

ENGINEER:

PAGE: 13 OF 21



WANG LABORATORIES, INC.

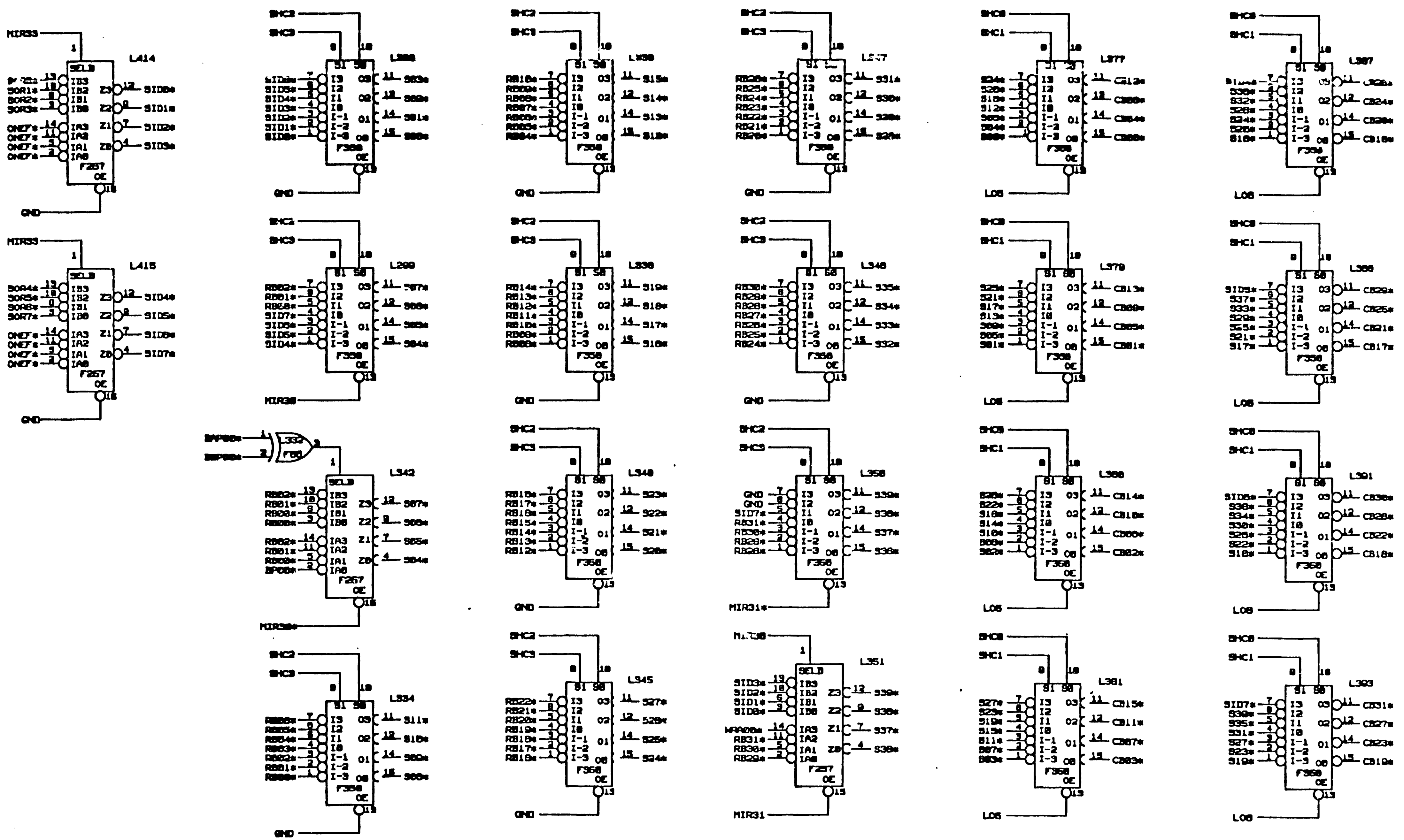
TITLE: VS-300 CPU 9231

ENGINEER:

REV: 0.00

DATE: 7/20/83

PAGE: 14 OF 21



WANG LABORATORIES, INC.

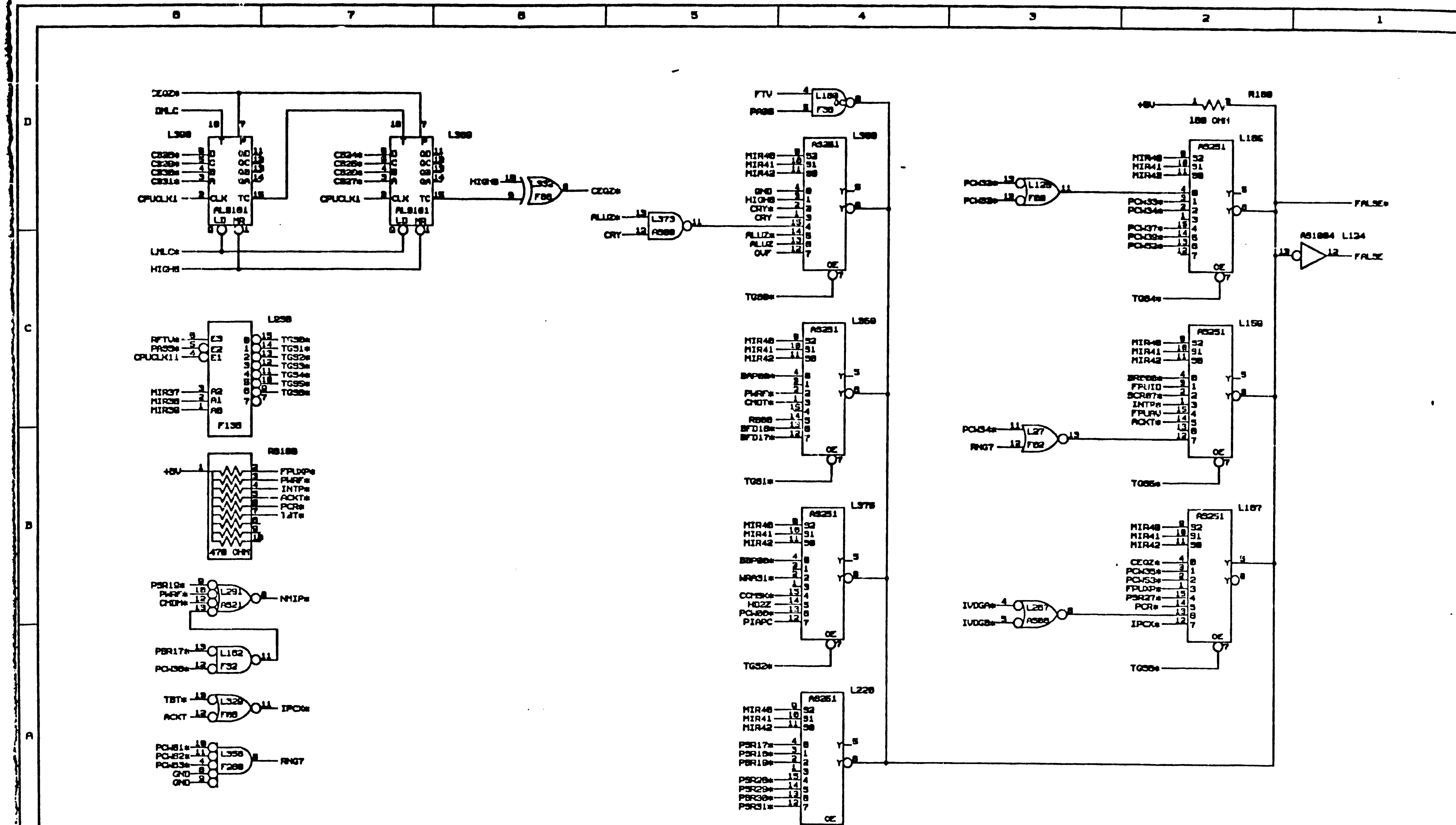
REV: 0.00

TITLE: VS-300 CPU 9231

DATE: 7/20/83

ENGINEER:

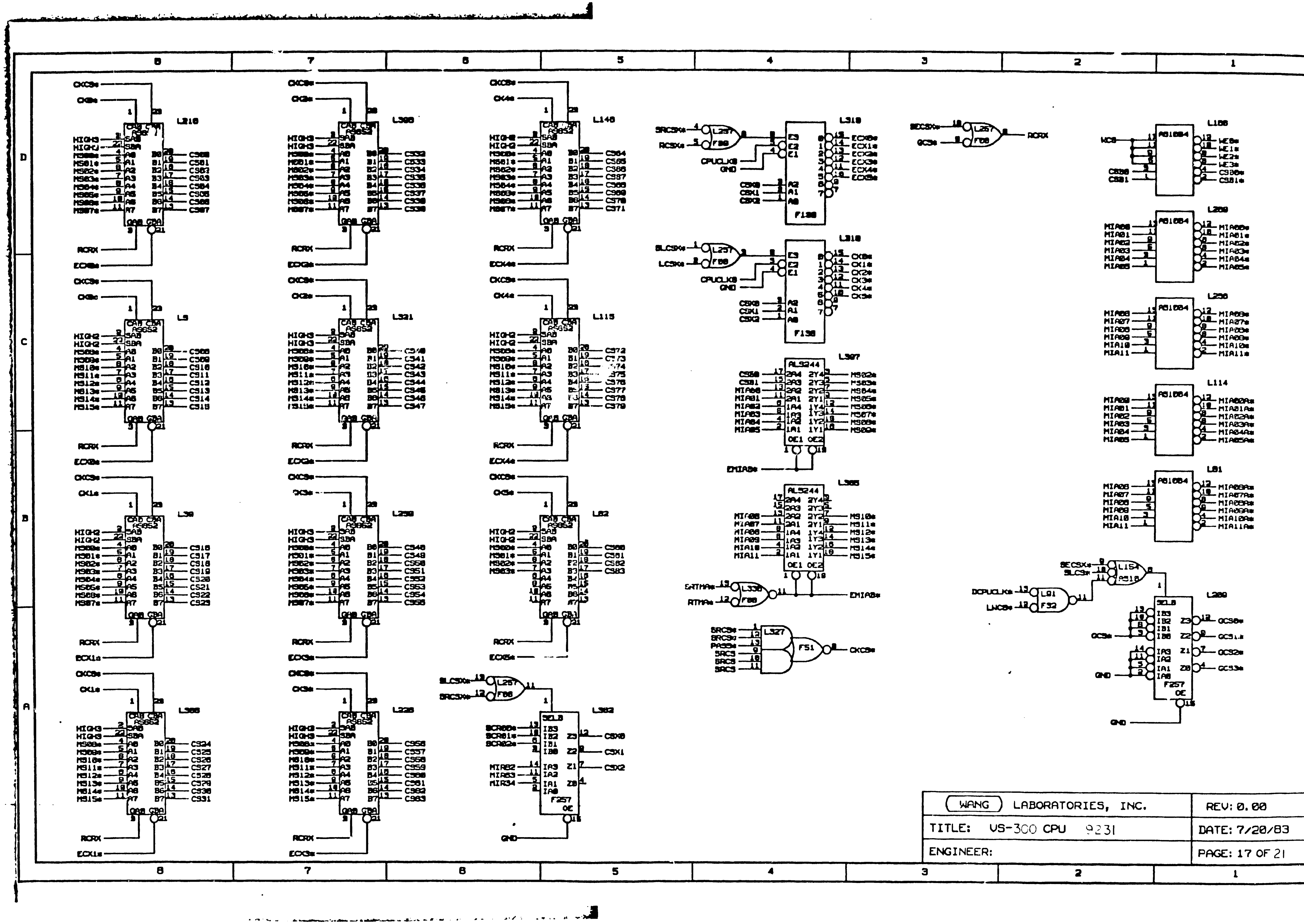
PAGE: 15 OF 21



(WANG) LABORATORIES, INC. | REV: 0.00

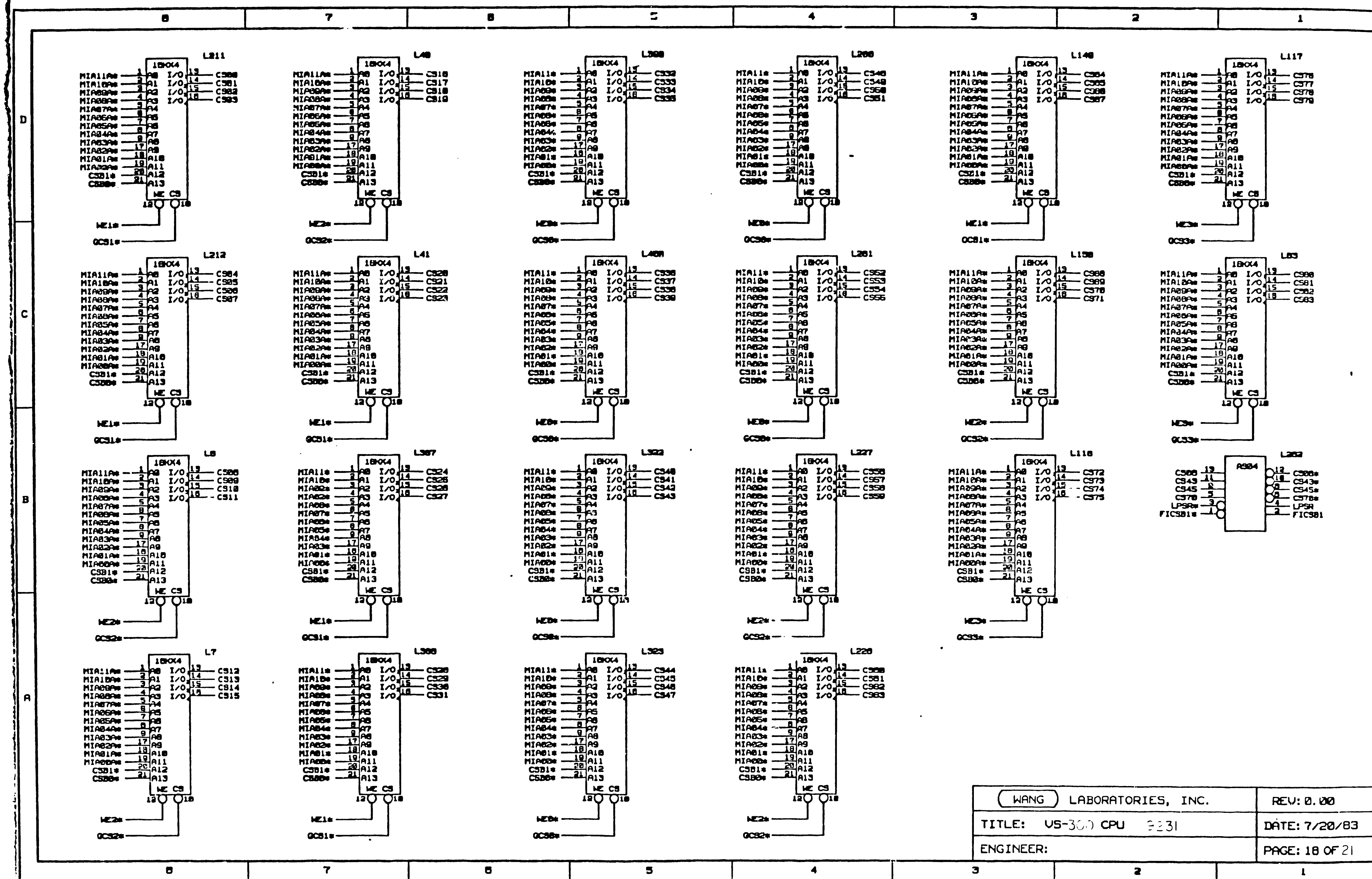
TITLE: VS-300 CPU 9231 | DATE: 7/20/83

ENGINEER: | PAGE: 18 OF 21

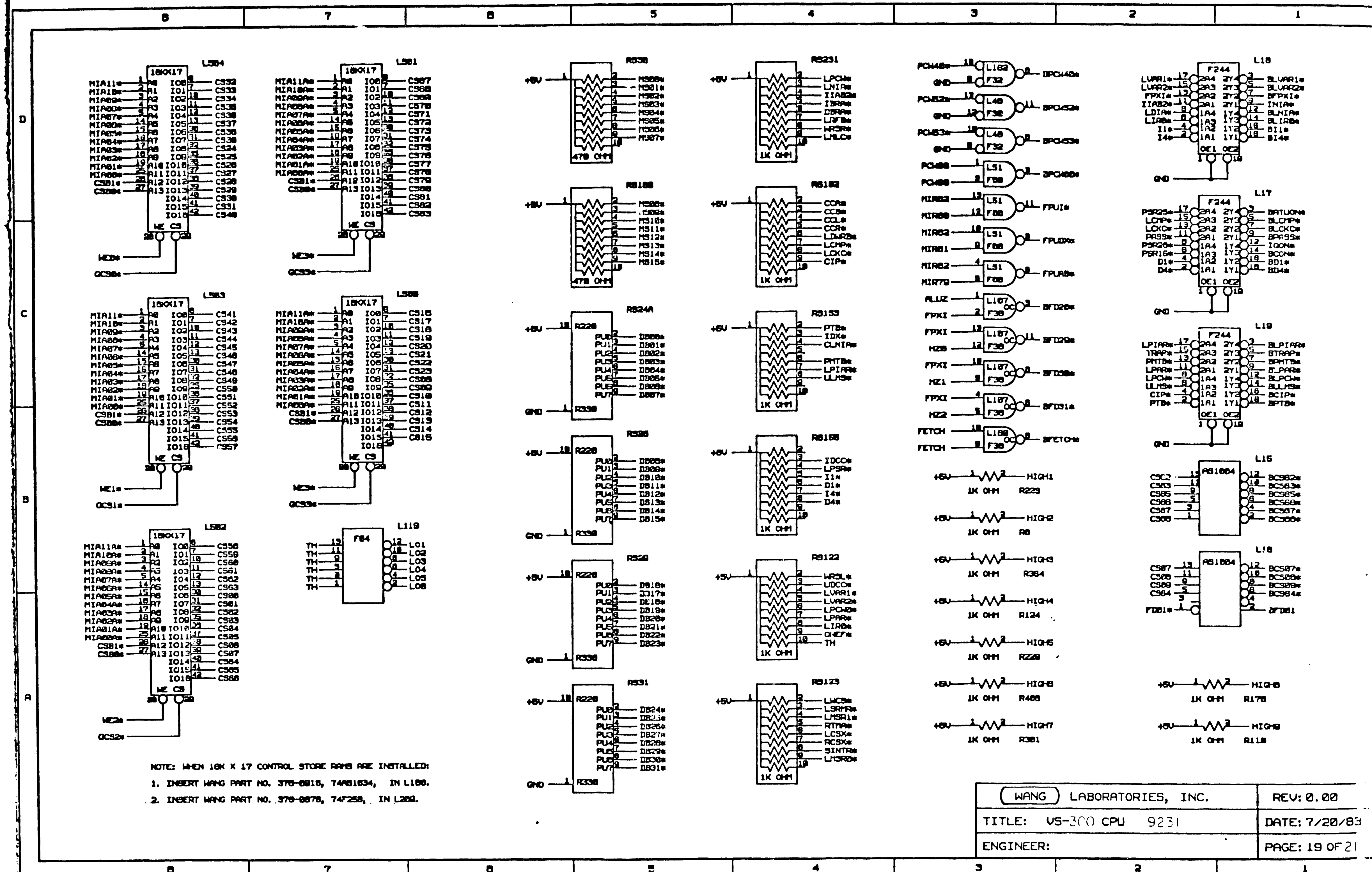


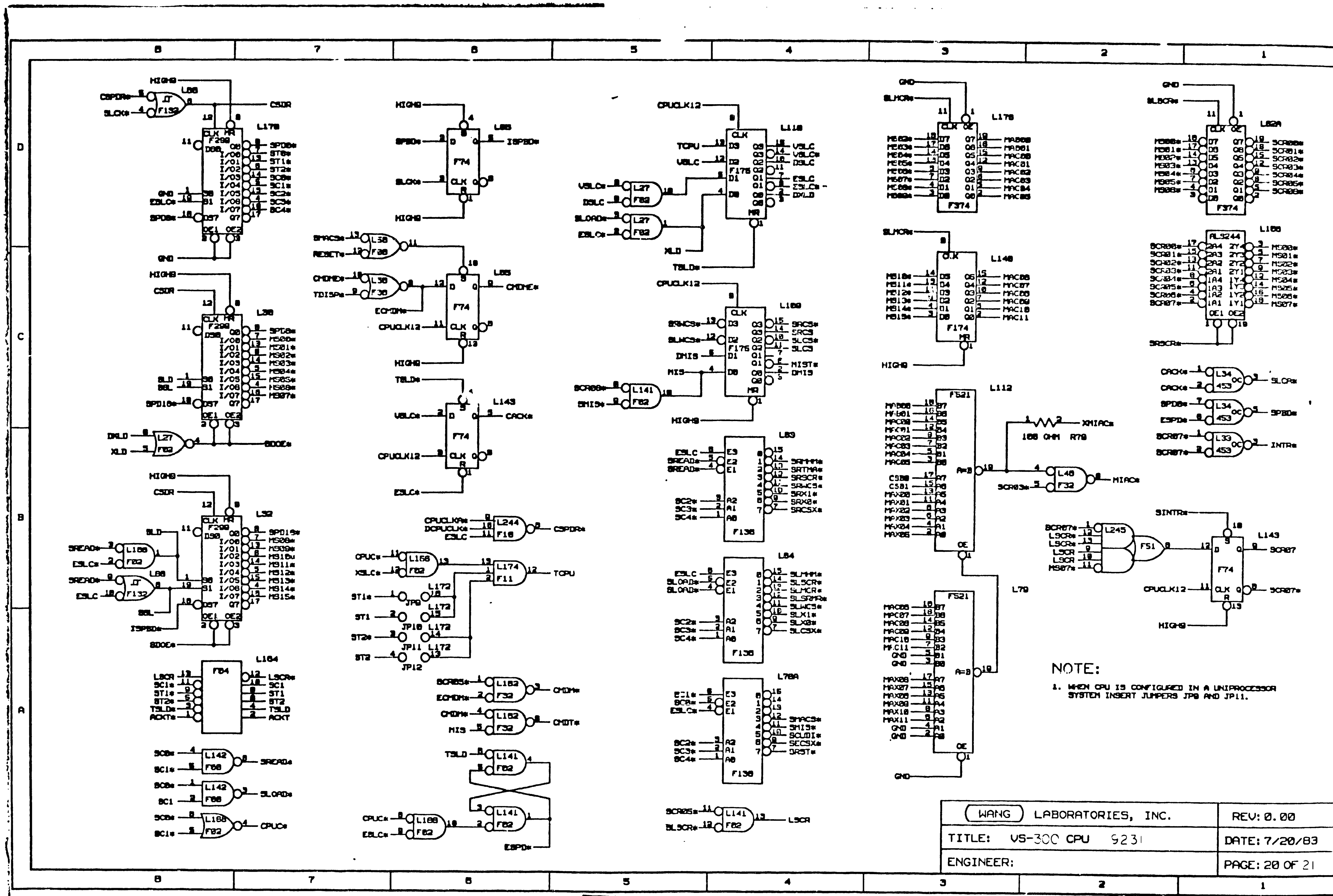
WANG LABORATORIES, INC.

TITLE: VS-300 CPU 9231	REV: 0.00
	DATE: 7/20/83
ENGINEER:	PAGE: 17 OF 21



WANG LABORATORIES, INC.
REV: 0.00
TITLE: VS-300 CPU 9231
DATE: 7/20/83
ENGINEER:
PAGE: 18 OF 21

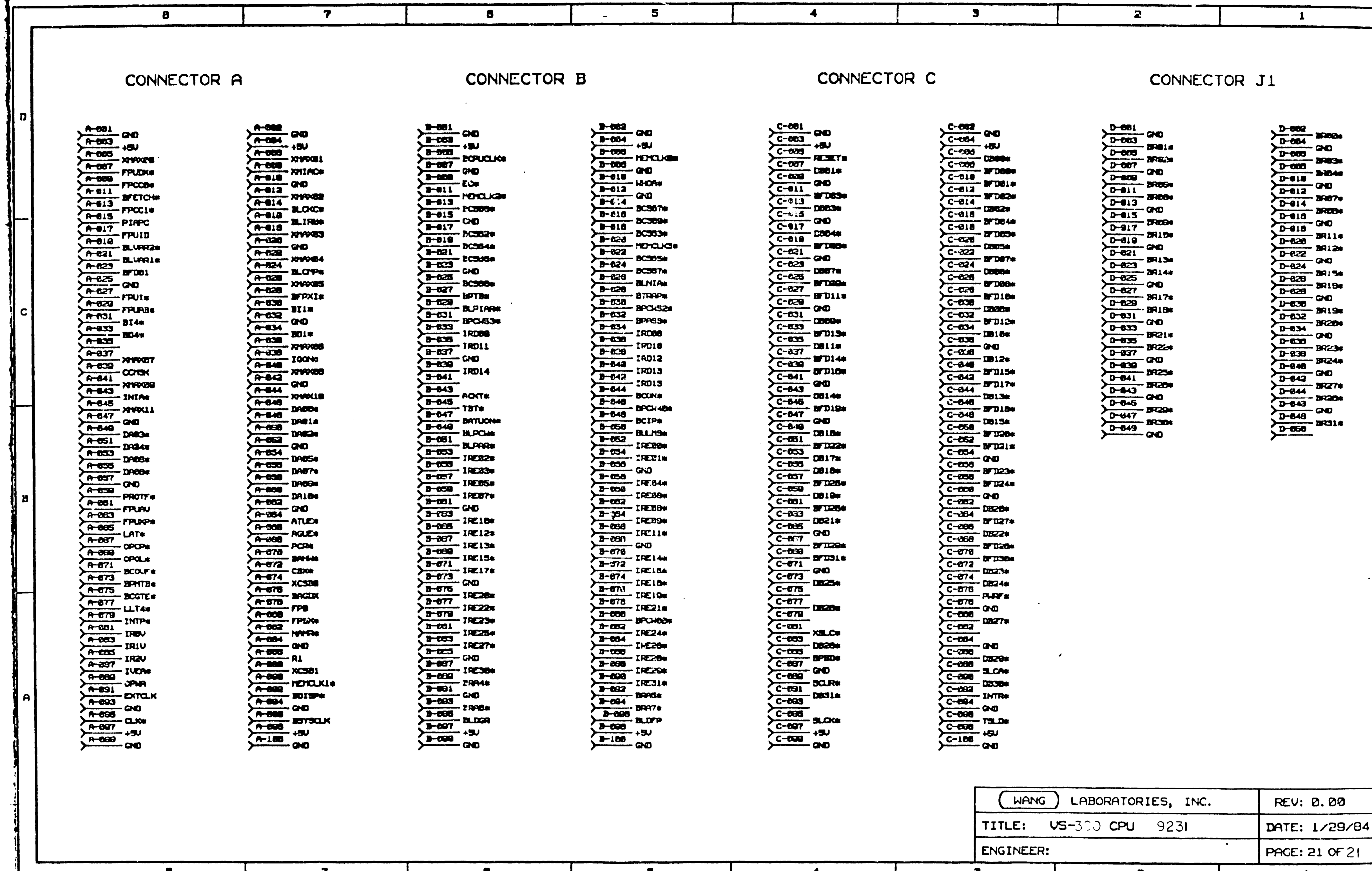

NOTE: WHEN 16K X 17 CONTROL STORE RAMS ARE INSTALLED:
1. INSERT WANG PART NO. 376-0018, 74AS1034, IN L100.
2. INSERT WANG PART NO. 376-0076, 74F258, IN L209.
WANG LABORATORIES, INC.
REV: 0.00
TITLE: VS-300 CPU 9231
DATE: 7/20/83
ENGINEER:
PAGE: 19 OF 21



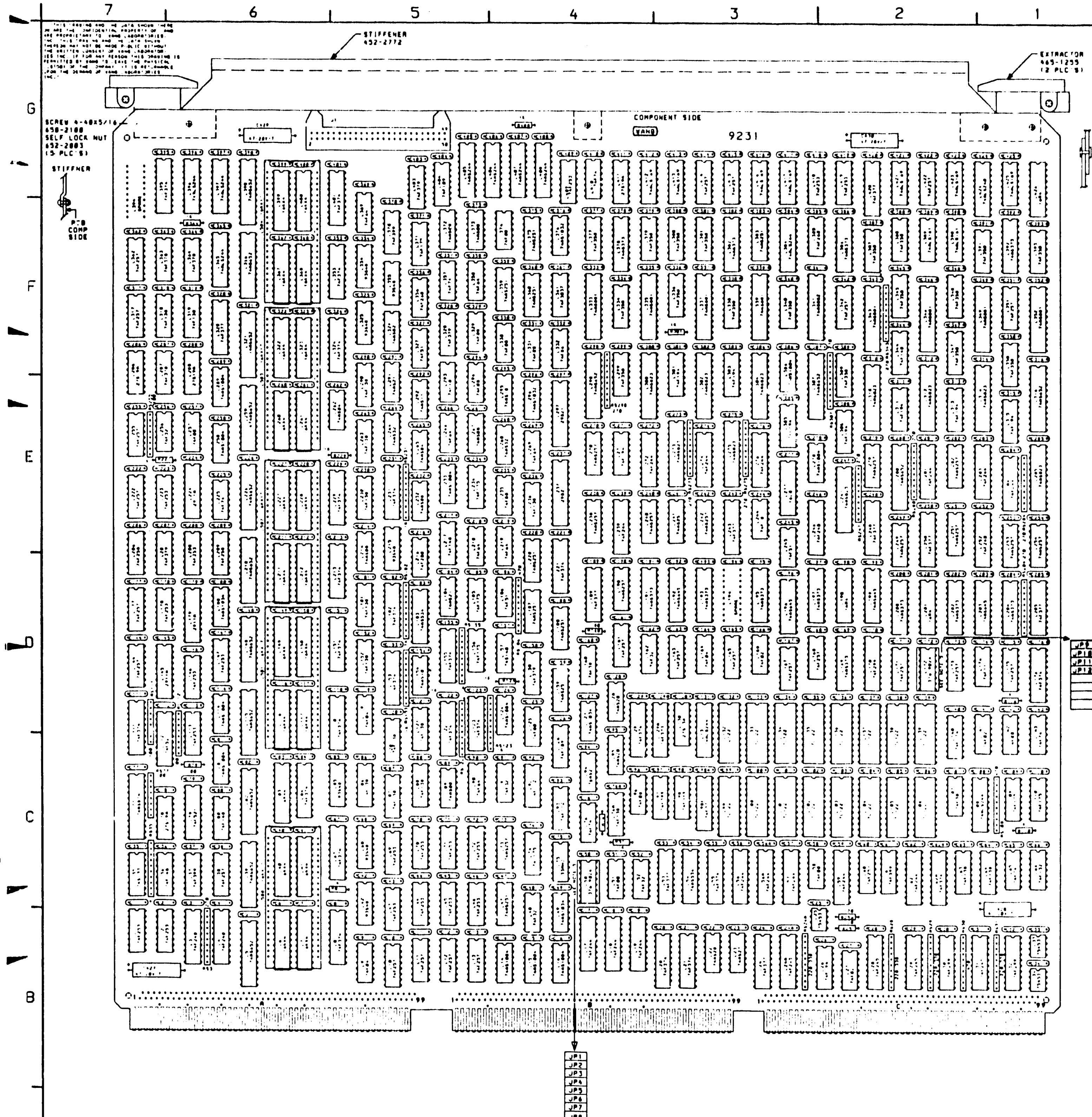
NOTE:

1. WHEN CPU IS CONFIGURED IN A UNIPROCESSOR SYSTEM INSERT JUMPERS JP9 AND JP11.

WANG LABORATORIES, INC.	REV: 0.00
TITLE: VS-300 CPU 9231	DATE: 7/20/83
ENGINEER:	PAGE: 20 OF 21



WANG LABORATORIES, INC.	REV: 0.00
TITLE: VS-300 CPU 9231	DATE: 1/29/84
ENGINEER:	PAGE: 21 OF 21



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITORS ARE .047UF EXPRESSED IN MICROFARADS.
   ALL RESISTORS ARE 1/4W.5%. EXPRESSED IN OHMS.
2. INSTALL JMPR PLG ASSY(376-9129) 3 PLCS ON L58.
3. 16KX17 RAM CHIPS REPLACE 16KX4 RAM CHIPS AND ASSOCIATED .1 CAPACITORS.
4. PIN 1 OF ALL SIPS FACE TOWARDS THE STIFFNER.
5. REF. SCHEMATIC LOADING CHART OR PARTS LIST FOR JUMPER CONFIGUPATION.
6. RESISTORS RS24A.F.J20-29.RS31 ARE 220/330 #PN 333-0007. LOAD PIN 1 TOWARDS BOTTOM OF BOARD.

WANG		BY	DATE	APPROVED BY	DATE
		DWN DPW		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS-300	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATION NO 10-214	TITLE VS300 CPU M/W			
FINISH		210-9231	C	9231	0
	SCALE 1/1 · SHT 1 OF 1	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV

VS-300 SBI 9236R0

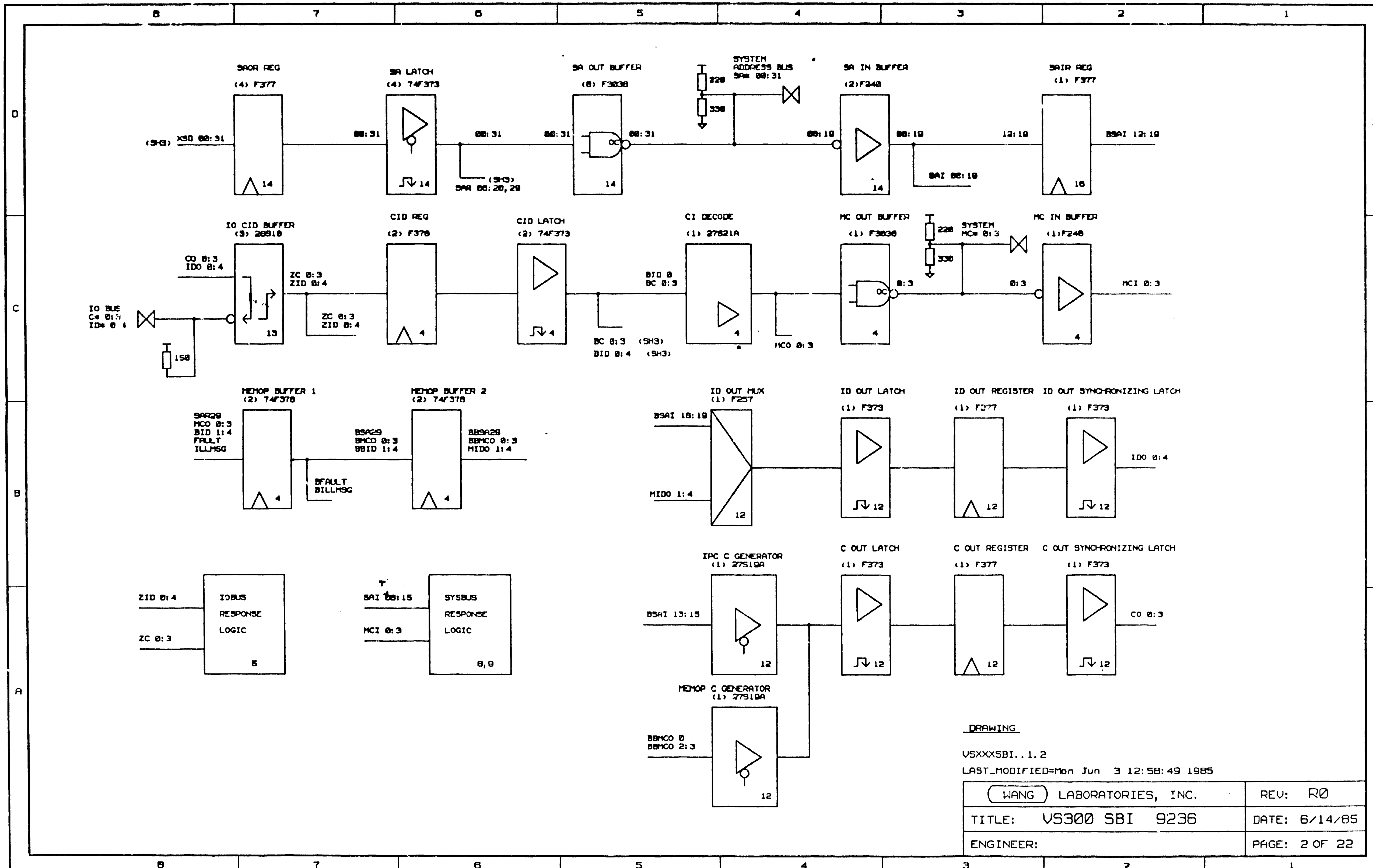
SYSTEM BUS INTERFACE

SHEET DESCRIPTION

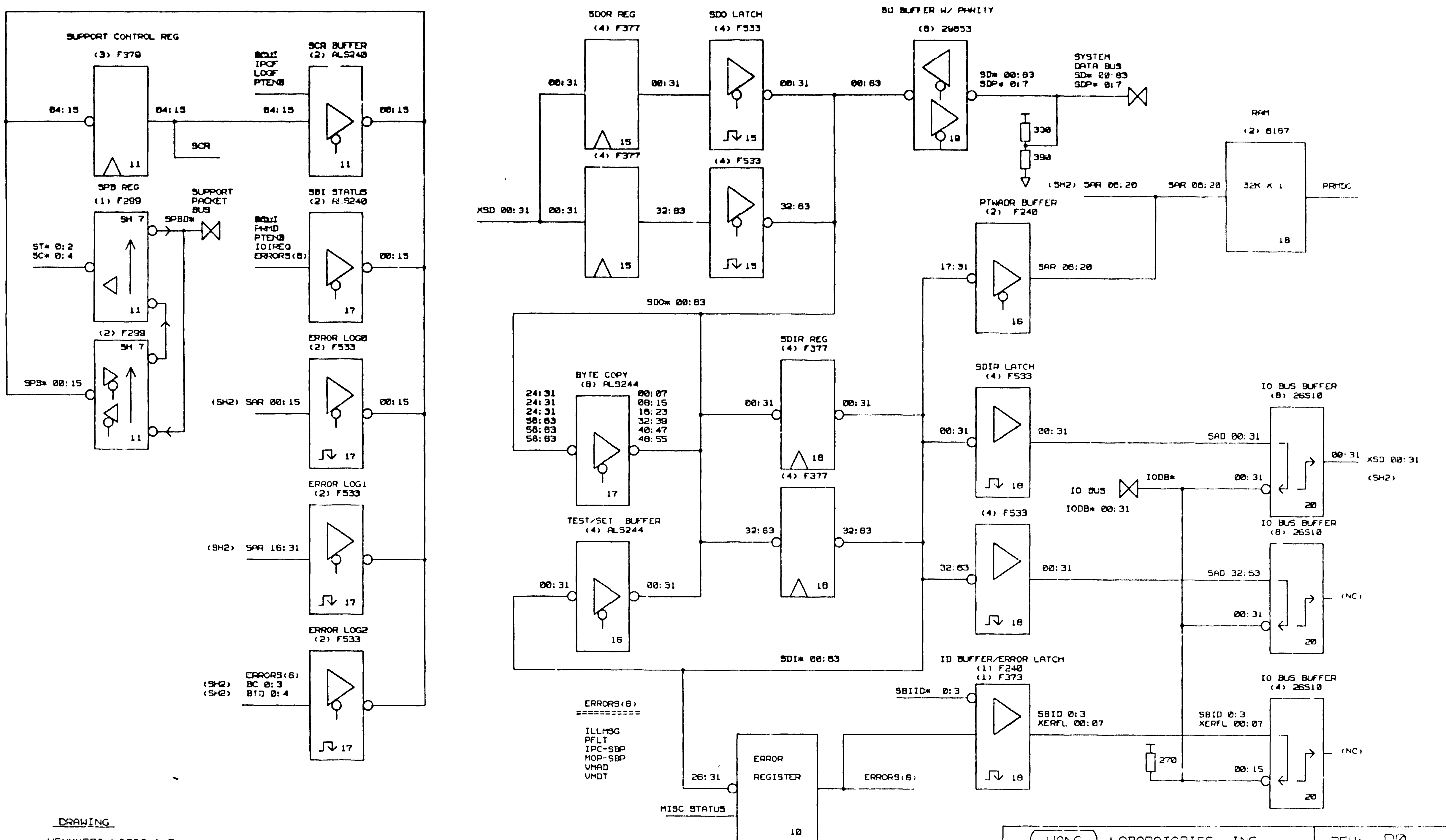
9236R0

DRAWING
TITLE=VSXXXSBI
ABBREV=SBI
LAST_MODIFIED=Fri Jun 14 13:37:08 1985
VSXXXSBI.LOGIC.1.1

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER: B.J. PATEL , P.A. MORRISON	PAGE: 1 OF 22



SAOR REG
(4) F377
SA LATCH
(4) 74F373
SA OUT BUFFER
(8) F3038
SYSTEM
ADDRESS BUS
SA* 00:31
SA IN BUFFER
(2)F240
SAIR REG
(1) F377
(SH3) XSO 00:31
00:31
(SH3)
SAR 06:20,28
BAI 00:19
12:19
BSAI 12:19
IO CID BUFFER
(3) 26S10
CID REG
(2) F378
CID LATCH
(2) 74F373
CI DECODE
(1) 27S21A
MC OUT BUFFER
(1) F3038
SYSTEM
MC* 0:3
MC IN BUFFER
(1)F240
CO 0:3
IDO 0:4
IO BUS
C* 0:3
ID* 0:4
ZC 0:3
ZID 0:4
BID 0
BC 0:3
BC 0:3 (SH3)
BID 0:4 (SH3)
MCO 0:3
MCI 0:3
MEMOP BUFFER 1
(2) 74F378
MEMOP BUFFER 2
(2) 74F378
SAR29
MCO 0:3
BID 1:4
FAULT
ILLMSG
BSA29
BMCO 0:3
BBID 1:4
BBSA29
BBMCO 0:3
MIDO 1:4
BFAULT
BILLMSG
IO OUT MUX
(1) F257
IO OUT LATCH
(1) F373
IO OUT REGISTER
(1) F377
IO OUT SYNCHRONIZING LATCH
(1) F373
BSAI 16:19
MIDO 1:4
IDO 0:4
ZID 0:4
ZC 0:3
IOBUS
RESPONSE
LOGIC
SAI 00:15
MCI 0:3
SYSBUS
RESPONSE
LOGIC
IPC C GENERATOR
(1) 27S19A
C OUT LATCH
(1) F373
C OUT REGISTER
(1) F377
C OUT SYNCHRONIZING LATCH
(1) F373
BSAI 13:15
CO 0:3
MEMOP C GENERATOR
(1) 27S19A
BBMCO 0
BBMCO 2:3
DRAWING
VSXXXSBI..1.2
LAST_MODIFIED=Mon Jun 3 12:58:49 1985
WANG LABORATORIES, INC.
REV: R0
TITLE: VS300 SBI 9236
DATE: 6/14/85
ENGINEER:
PAGE: 2 OF 22

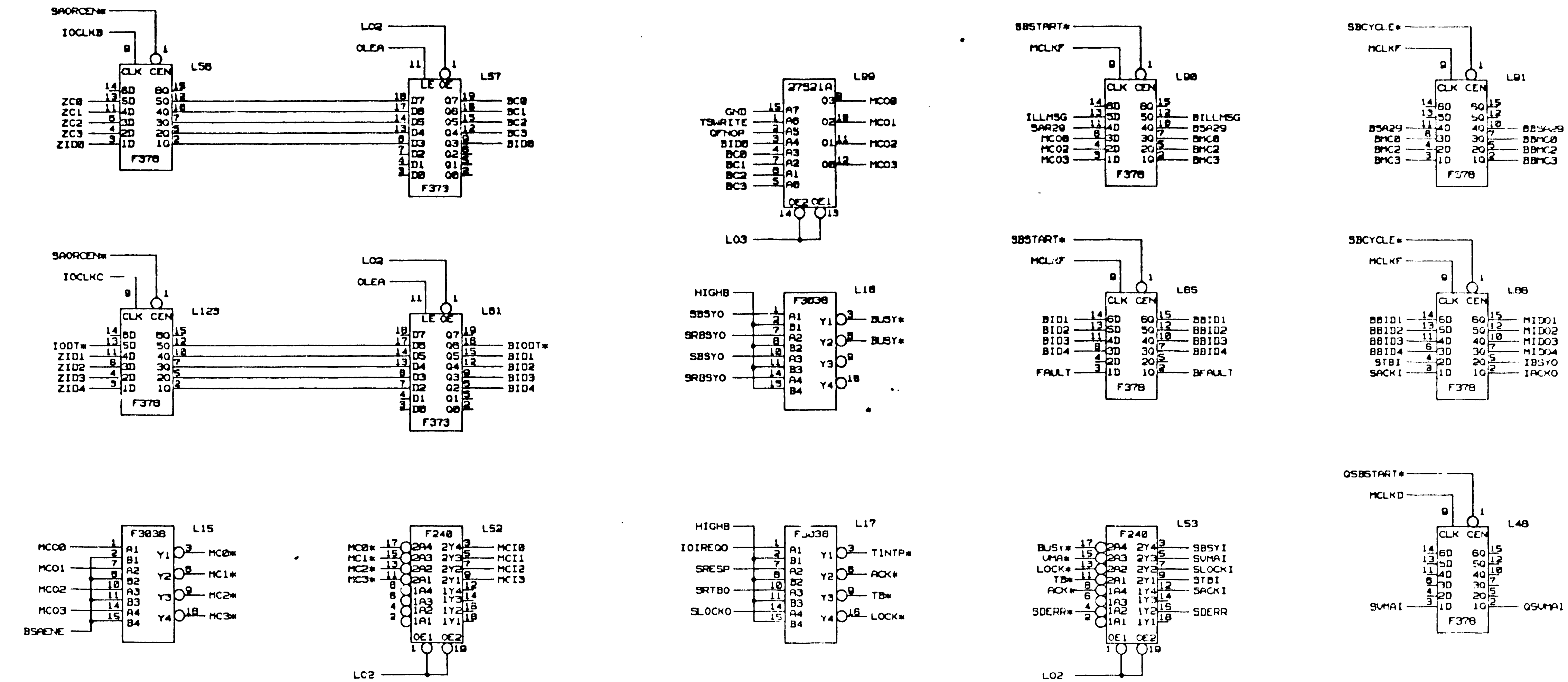


DRAWING

VSXXXSBI.LOGIC.1.3

LAST_MODIFIED=Tue Jun 4 14:02:27 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 3 OF 22

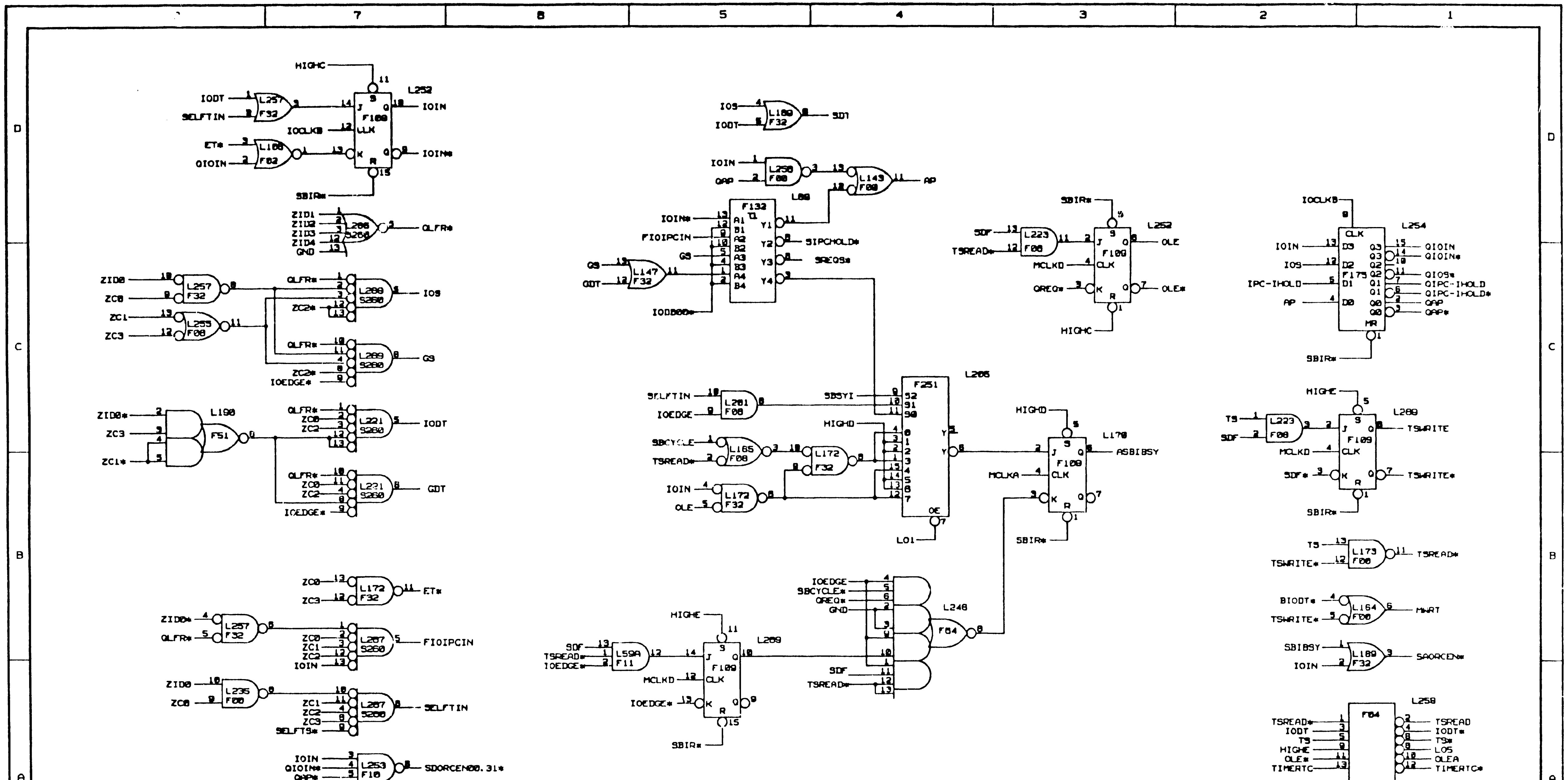


DRAWING

VSXXXSBI..1.4

LAST_MODIFIED=Mon Jun 17 12:22:10 1985

(WANG) LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 4 OF 22



SET ASBIBSY ((IOS+IODT).IODB00*+SELFTIN).IOIN*.IOEDGE.OLE*
.(SBCYCLE*+SBSYI+TSREAD)

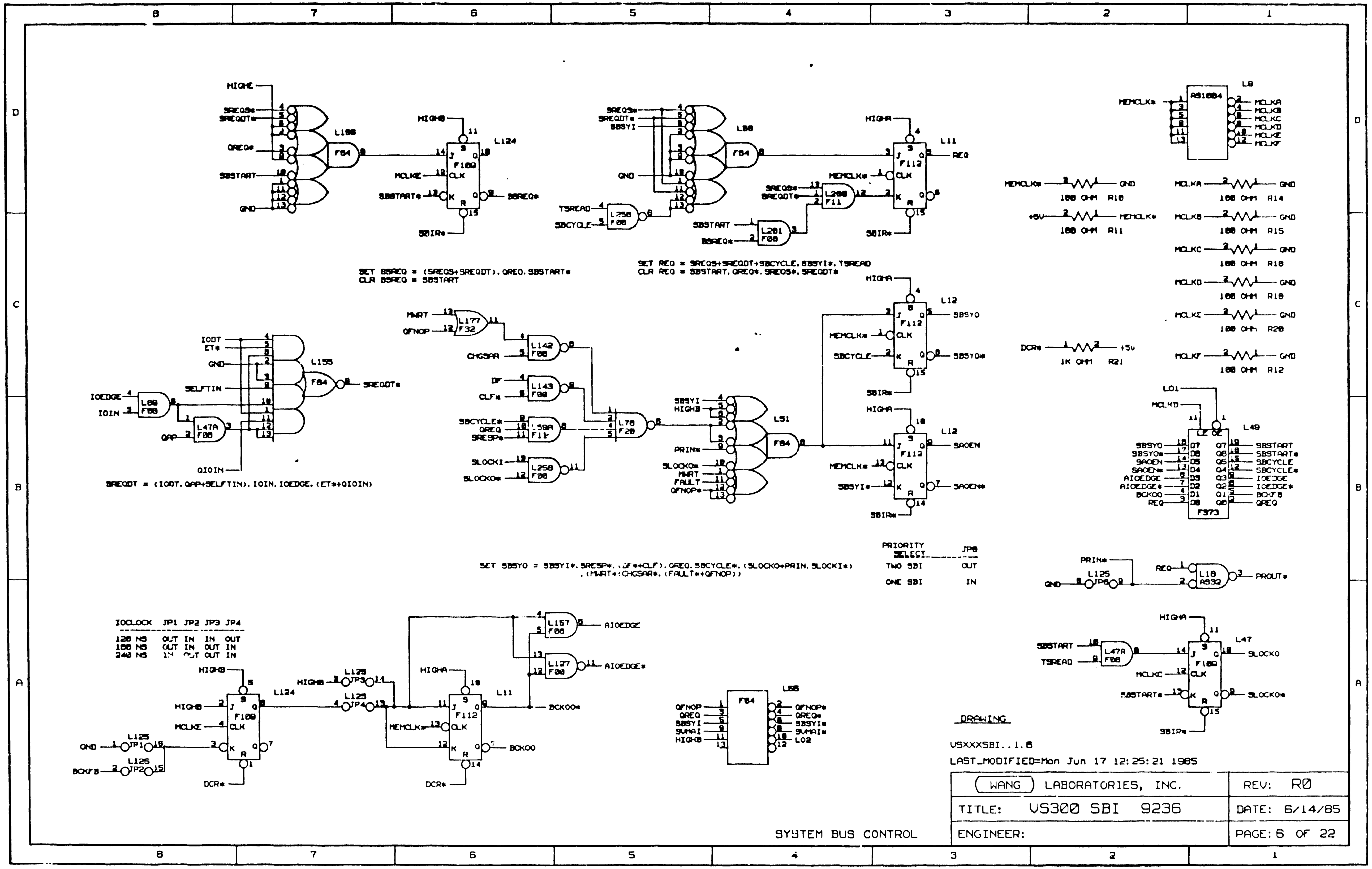
RESET ASBIBSY (BRSBIBSY+SBCYCLE*.QREQ*+SDF.TSREAD*).IOEDGE

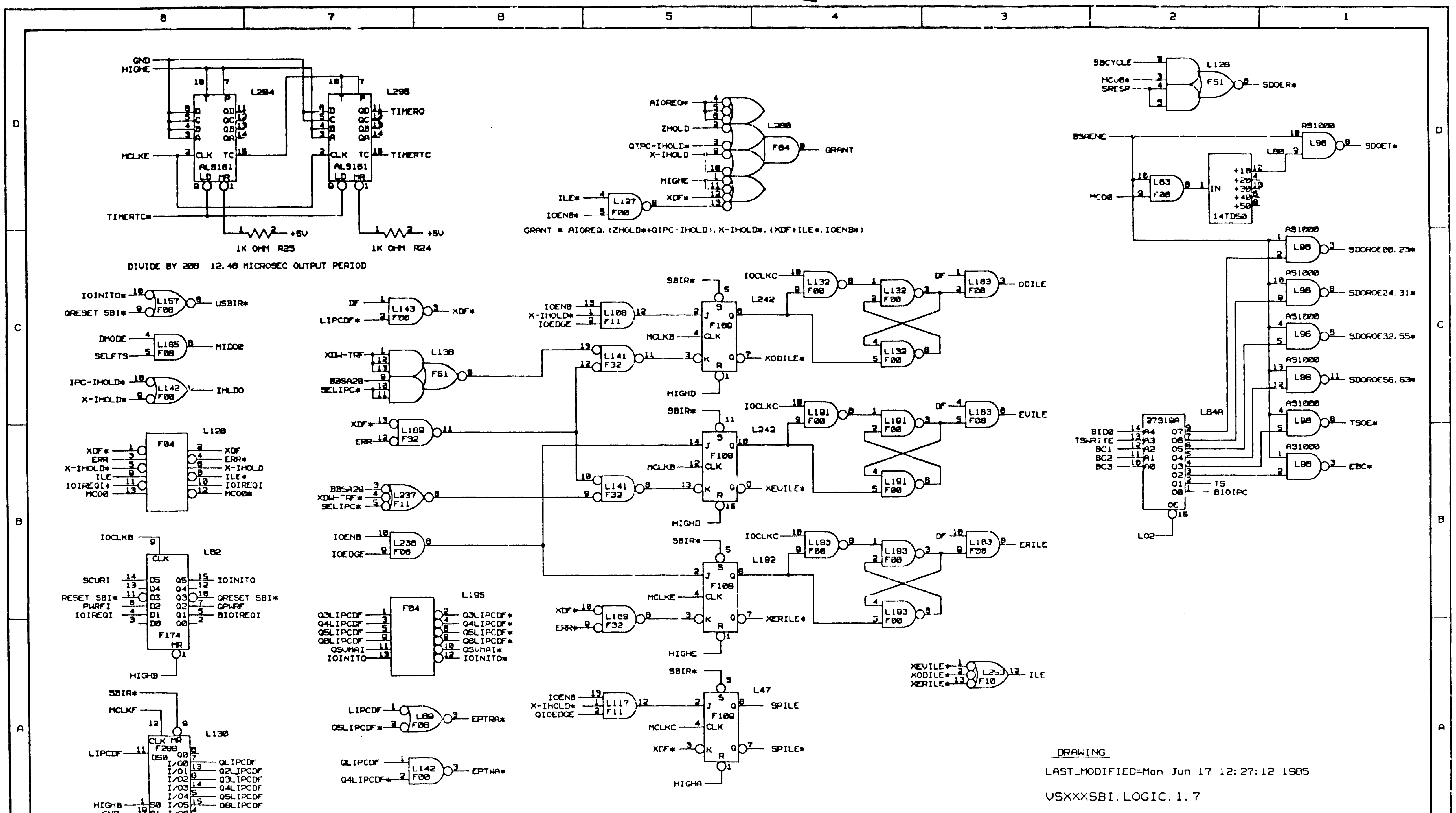
DRAWING

VSXXXSBI.LOGIC.1.5

LAST_MODIFIED=Mon Jun 17 12:23:51 1985

(WANG) LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 5 OF 22


SET SBREQ = (SREQS+SREQDT).QREQ.SBSTART*
CLR SBREQ = SBSTART
SET REQ = SREQS+SREQDT+SBCYCLE.SBSYI*.TSREAD
CLR REQ = SBSTART.QREQ*.SREQS*.SREQDT*
SREQDT = (IODT.QAP+SELFTIN).IOIN.IOEDGE.(ET*+QIOIN)
SET SBSYO = SBSYI*.SRESP*.(DF*+CLF).QREQ.SBCYCLE*.(SLOCKO+PRIN.SLOCKI*)
.(MWRT*+CHGSAR*.(FAULT*+QFNOP))
PRIORITY SELECT
JP8
TWO SBI
OUT
ONE SBI
IN
IOCLOCK JP1 JP2 JP3 JP4
120 NS OUT IN IN OUT
160 NS OUT IN OUT IN
240 NS IN OUT OUT IN
DRAWING
VSXXXSBI..1.8
LAST_MODIFIED=Mon Jun 17 12:25:21 1985
WANG LABORATORIES, INC.
REV: R0
TITLE: VS300 SBI 9236
DATE: 6/14/85
SYSTEM BUS CONTROL
ENGINEER:
PAGE: 6 OF 22

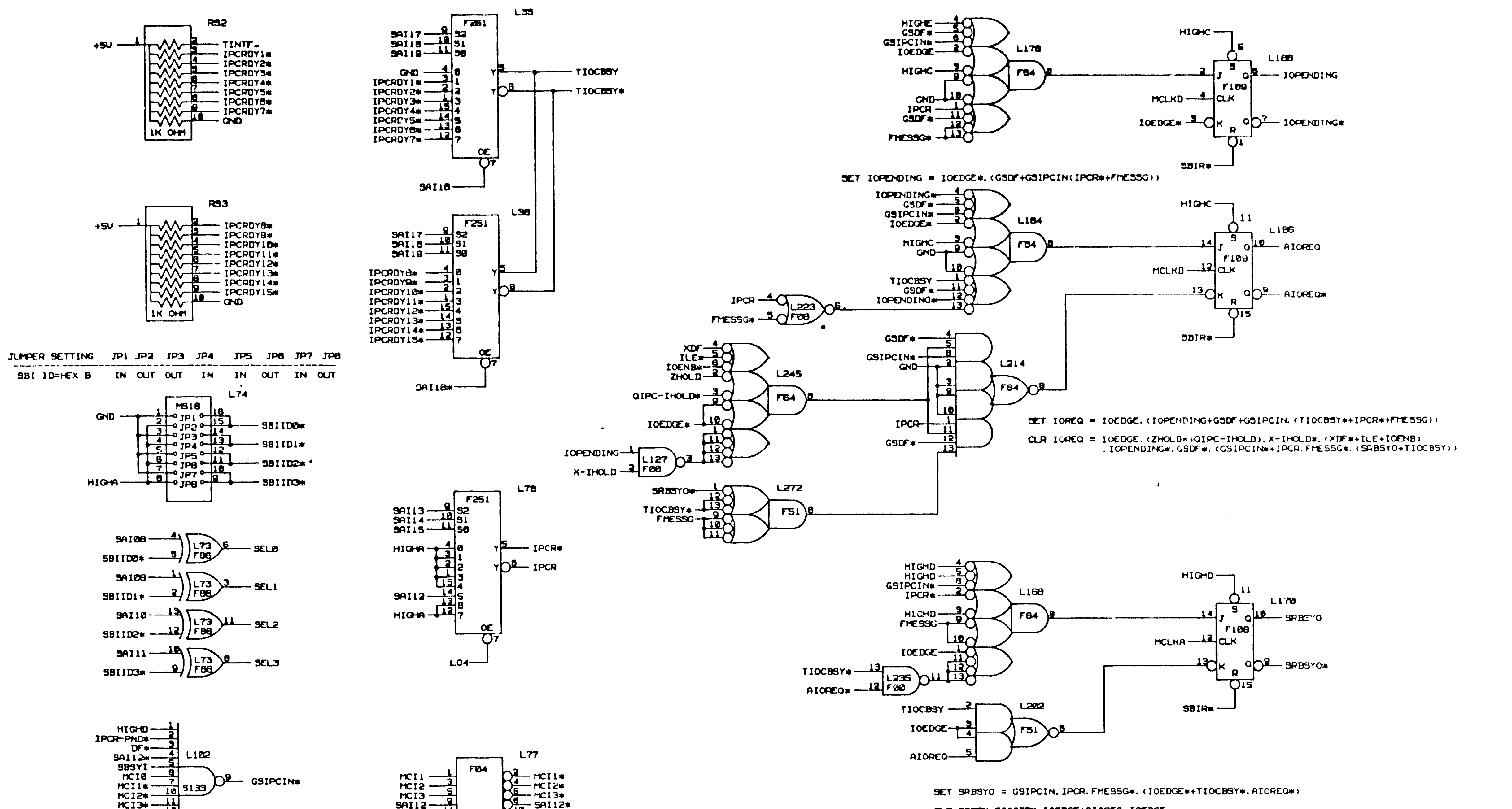


DRAWING

LAST_MODIFIED=Mon Jun 17 12:27:12 1985

VSXXXSBI.LOGIC.1.7

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 7 OF 22

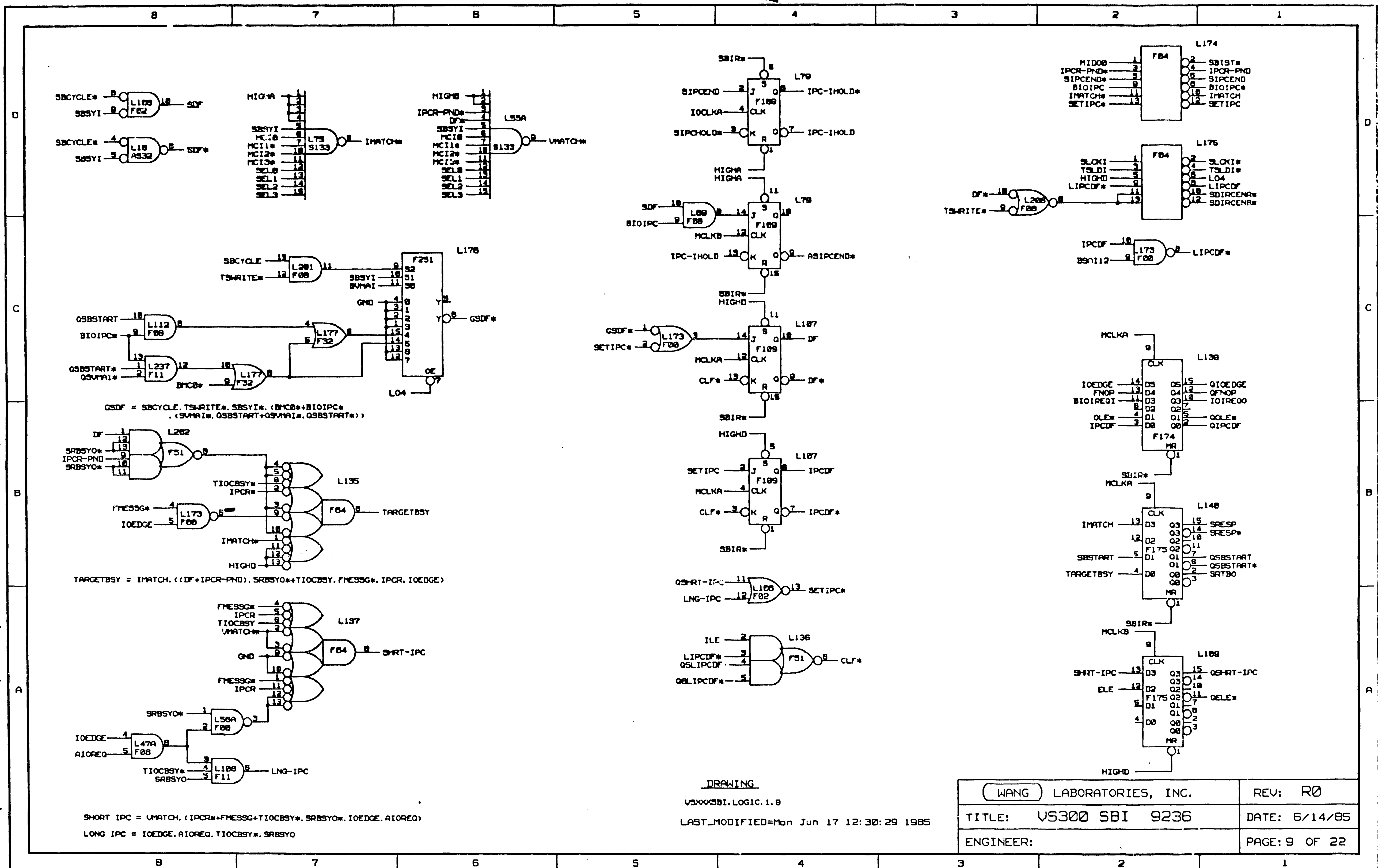


DRAWING

VSXXXSBI.LOGIC.1.8

LAST_MODIFIED=Mon Jun 17 12:28:57 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 8 OF 22



GSDF = SBCYCLE.TSWRITE*.SBSYI*.(BMC8*+BIOIPC* .(SVMAI*.QSBSTART+QSVMAI*.QSBSTART*))

TARGETBSY = IMATCH.((DF+IPCR-PND).SRBSYO*+TIOCBSY.FMESSG*.IPCR.IOEDGE)

SHORT IPC = VMATCH.(IPCR*+FMESSG+TIOCBSY*.SRBSYO*.IOEDGE.AIOREQ)

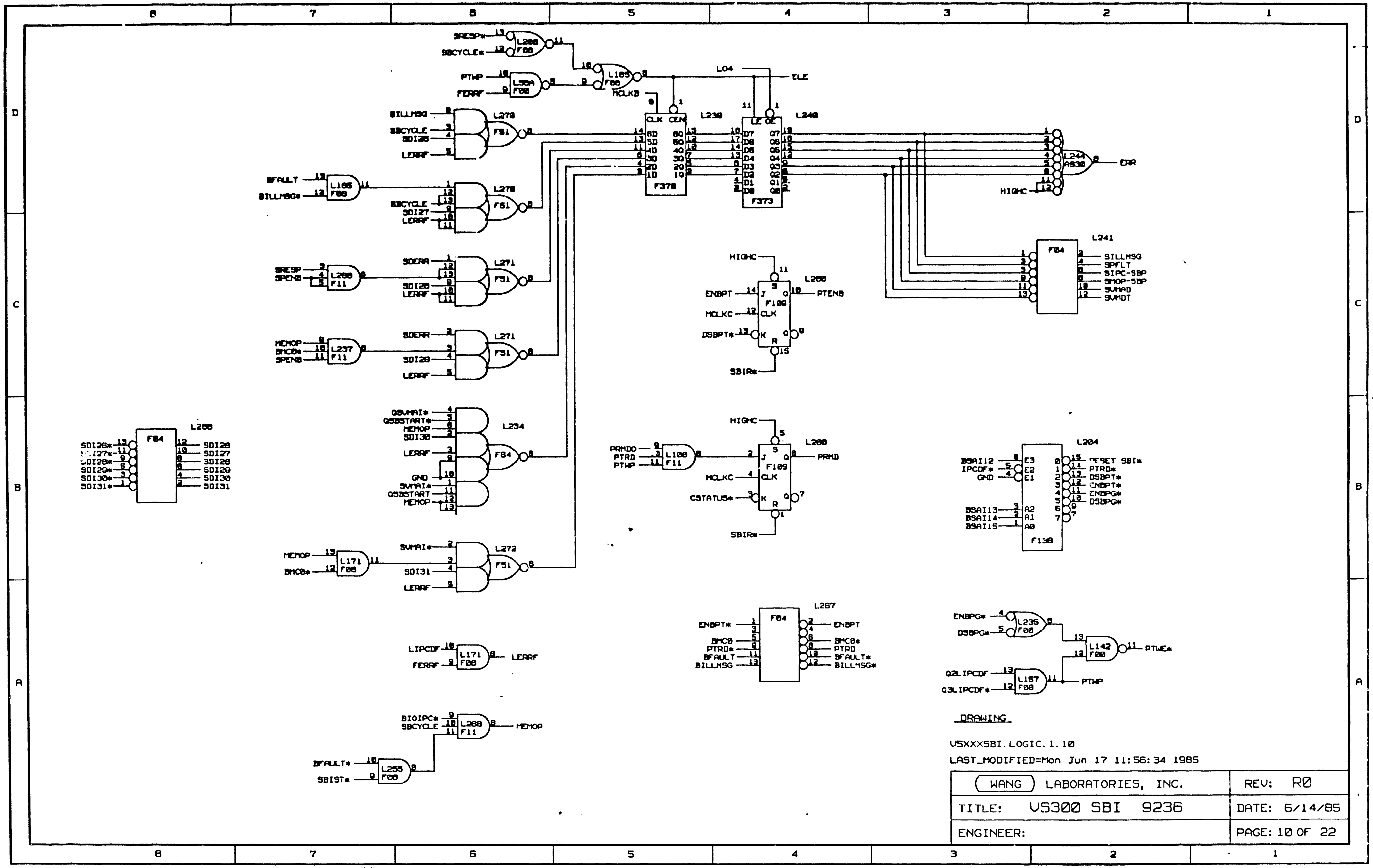
LONG IPC = IOEDGE.AIOREQ.TIOCBSY*.SRBSYO

DRAWING

VSXXXSBI.LOGIC.1.9

LAST_MODIFIED=Mon Jun 17 12:30:29 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 9 OF 22

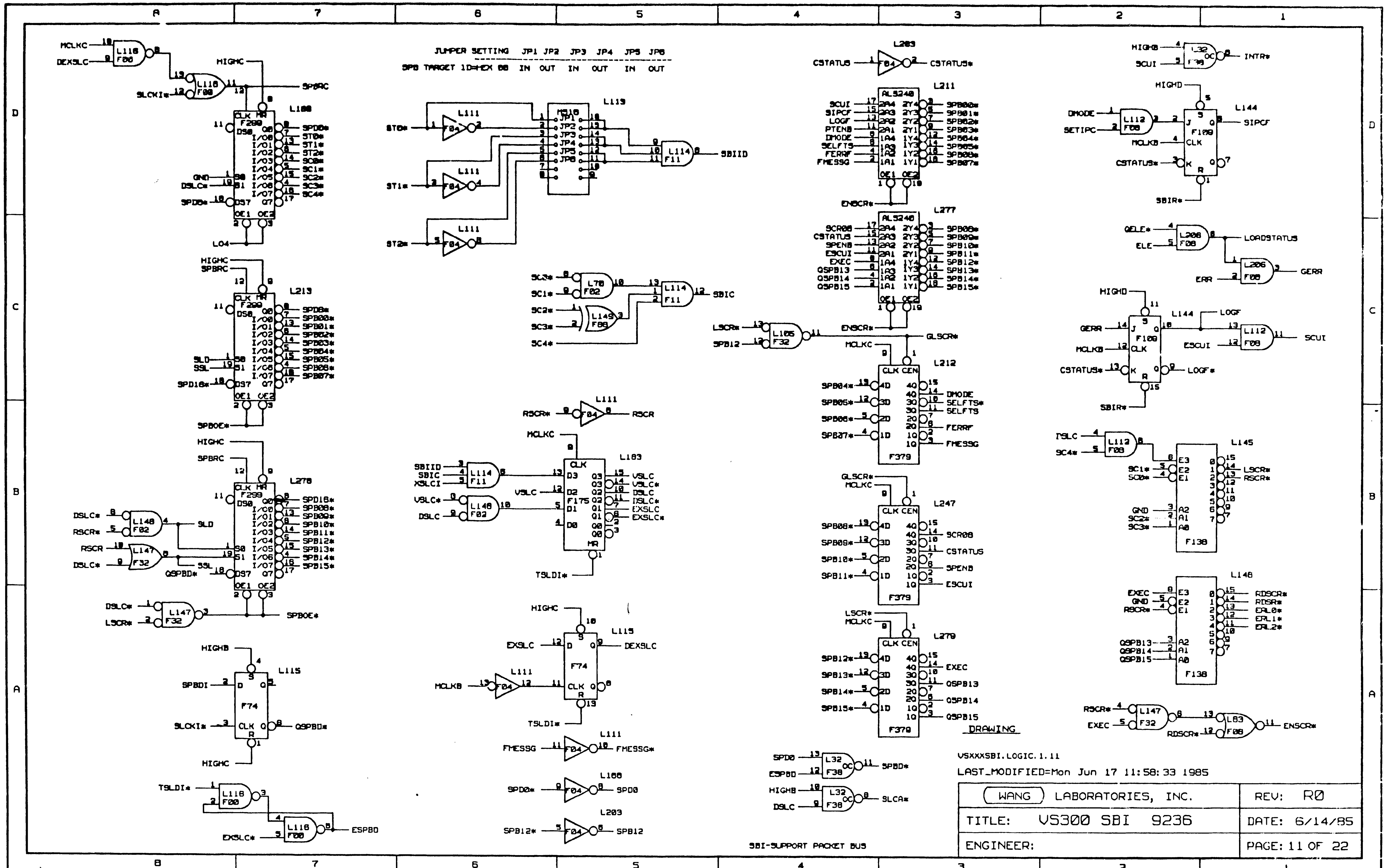


DRAWING

VSXXXSBI.LOGIC.1.10

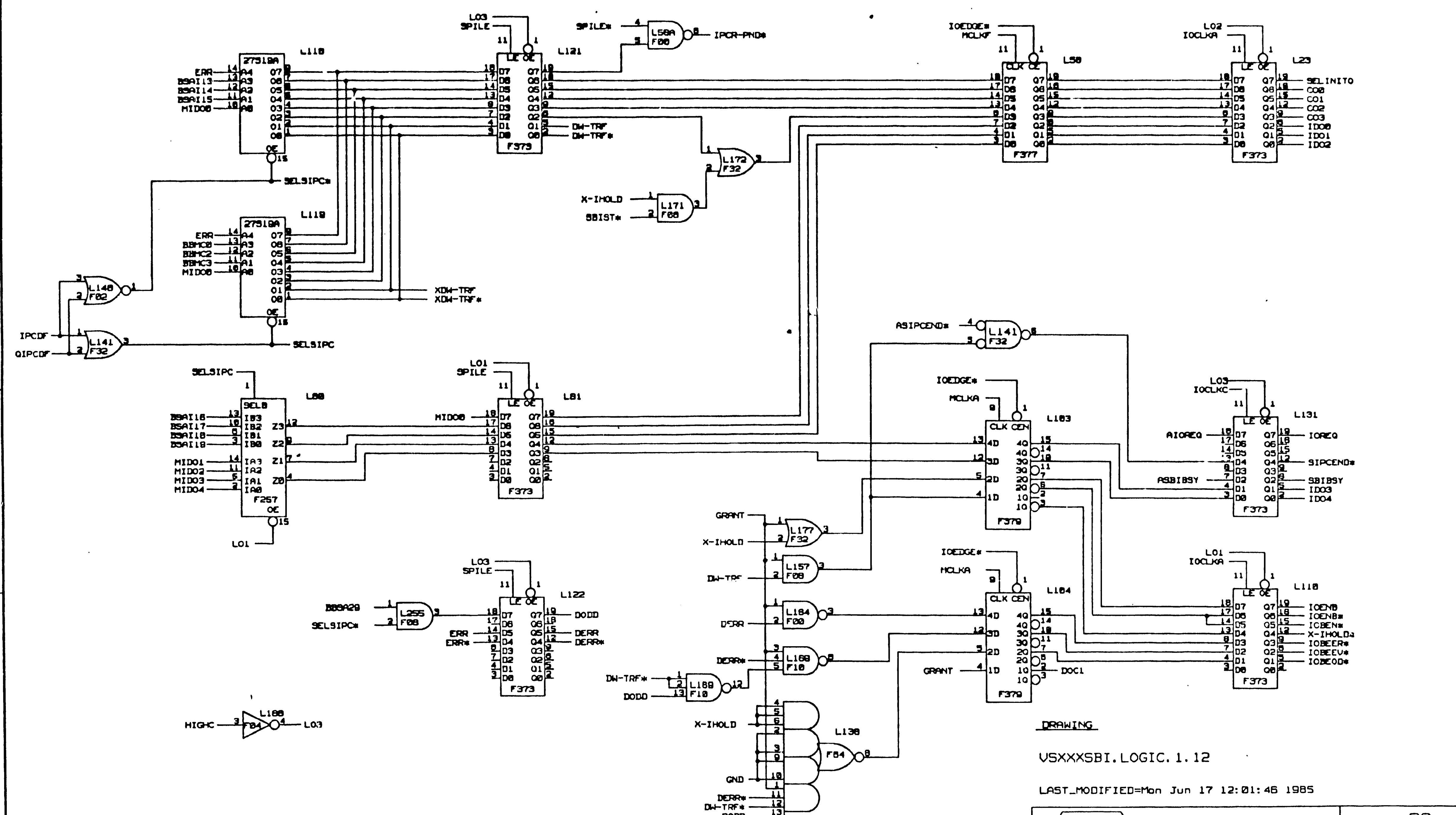
LAST_MODIFIED=Mon Jun 17 11:56:34 1985

(WANG) LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 10 OF 22



VSXXXSBI.LOGIC.1.11
LAST_MODIFIED=Mon Jun 17 11:58:33 1985

WANG LABORATORIES, INC.	REV: RØ
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 11 OF 22

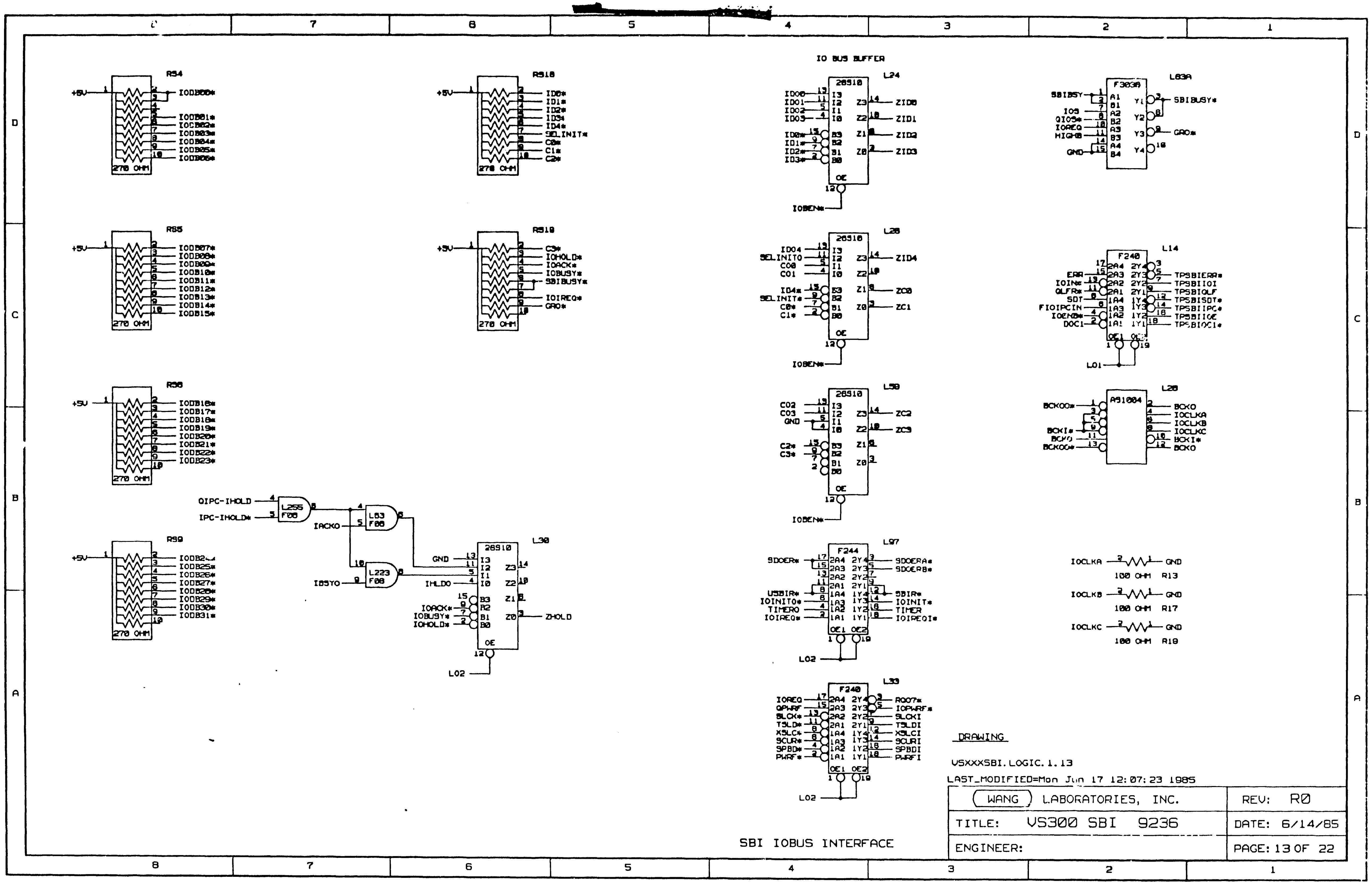


DRAWING

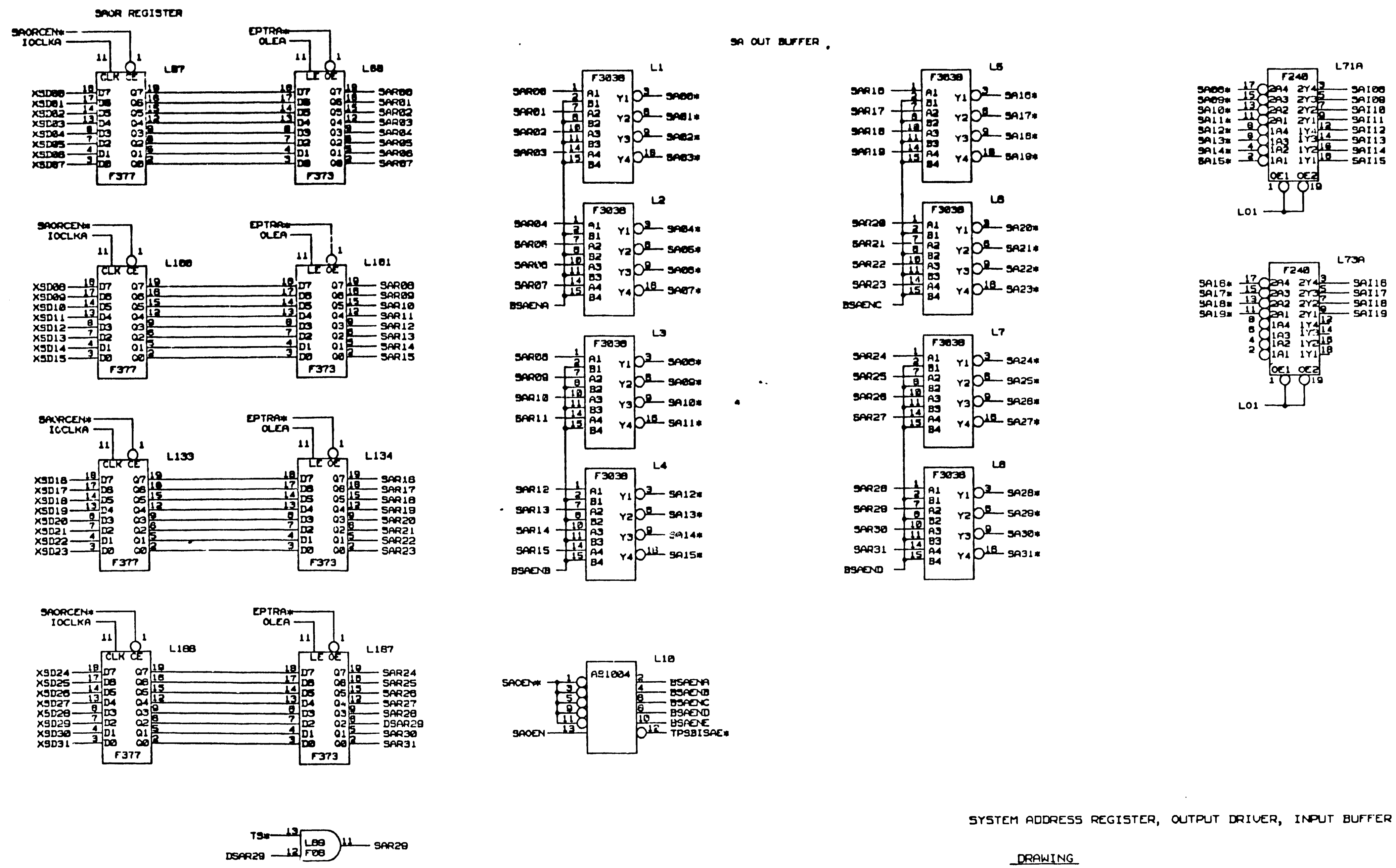
VSXXXSBI.LOGIC.1.12

LAST_MODIFIED=Mon Jun 17 12:01:46 1985

(WANG) LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 12 OF 22



IO BUS BUFFER
SBI IOBUS INTERFACE
DRAWING
VSXXXSBI.LOGIC.1.13
LAST_MODIFIED=Mon Jun 17 12:07:23 1985
WANG LABORATORIES, INC.
REV: R0
TITLE: VS300 SBI 9236
DATE: 6/14/85
ENGINEER:
PAGE: 13 OF 22

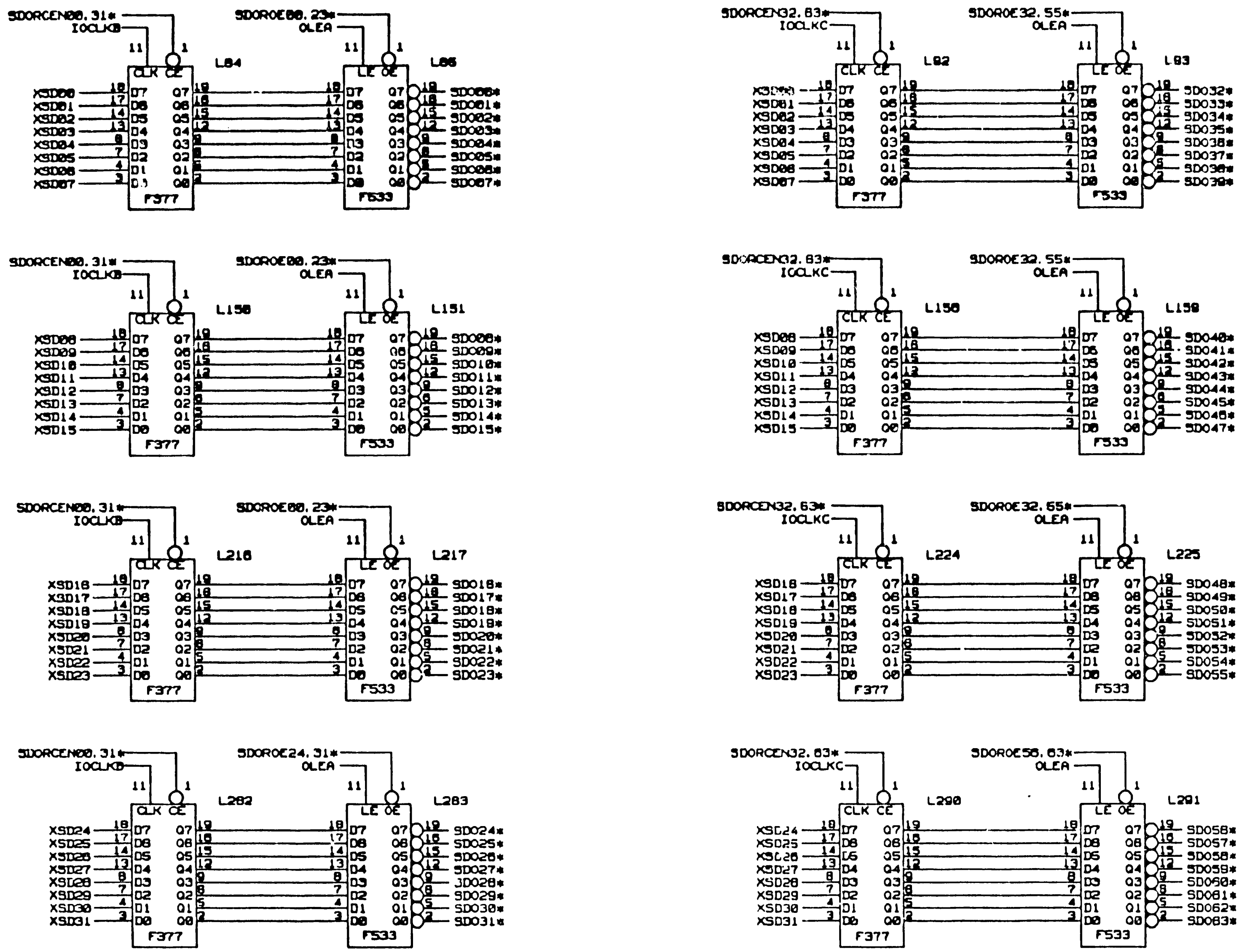


SYSTEM ADDRESS REGISTER, OUTPUT DRIVER, INPUT BUFFER

DRAWING

VSXXXSBI.LOGIC.1.14
LAST_MODIFIED=Mon Jun 17 12:09:19 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 14 OF 22



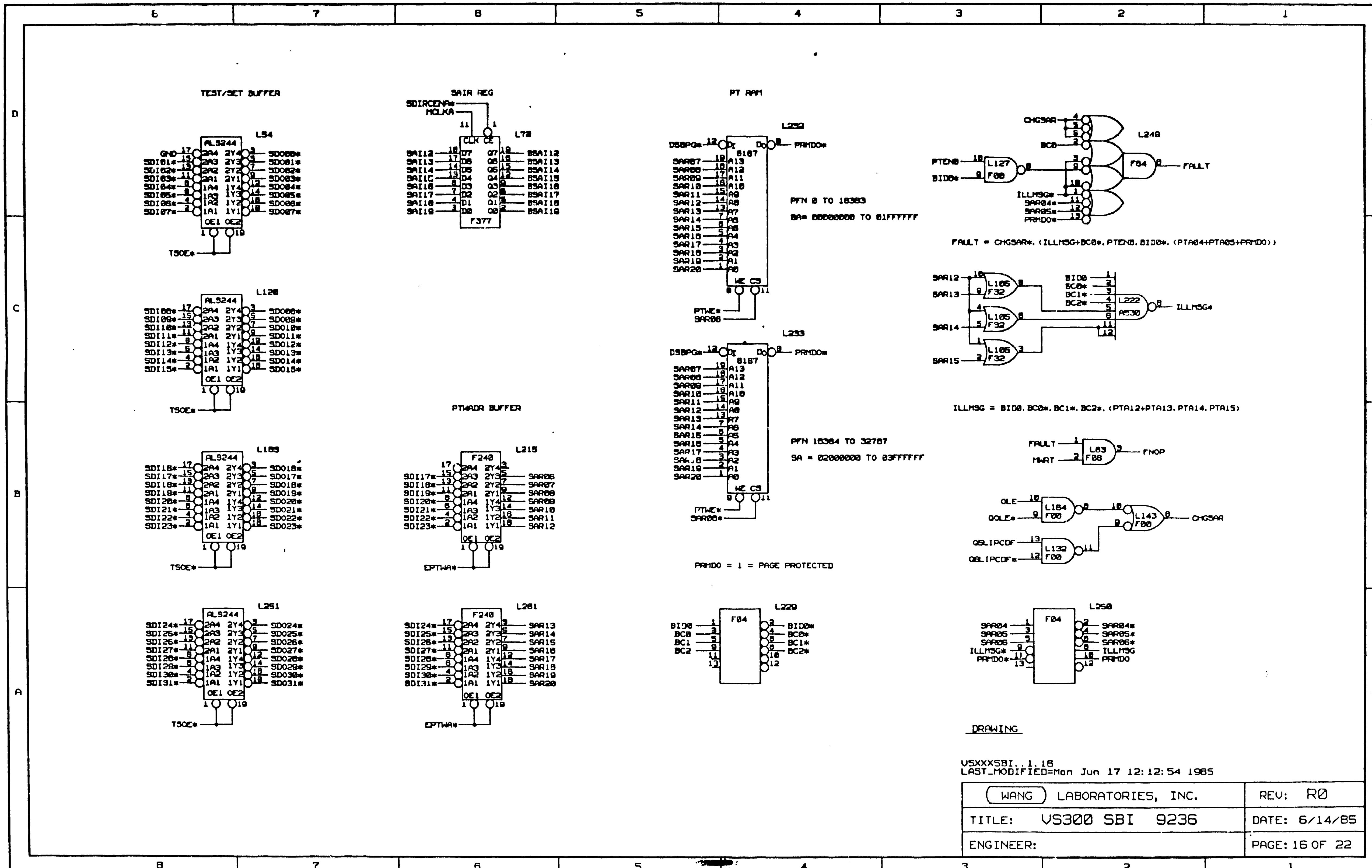
SYSTEM DATA OUTPUT REGISTER

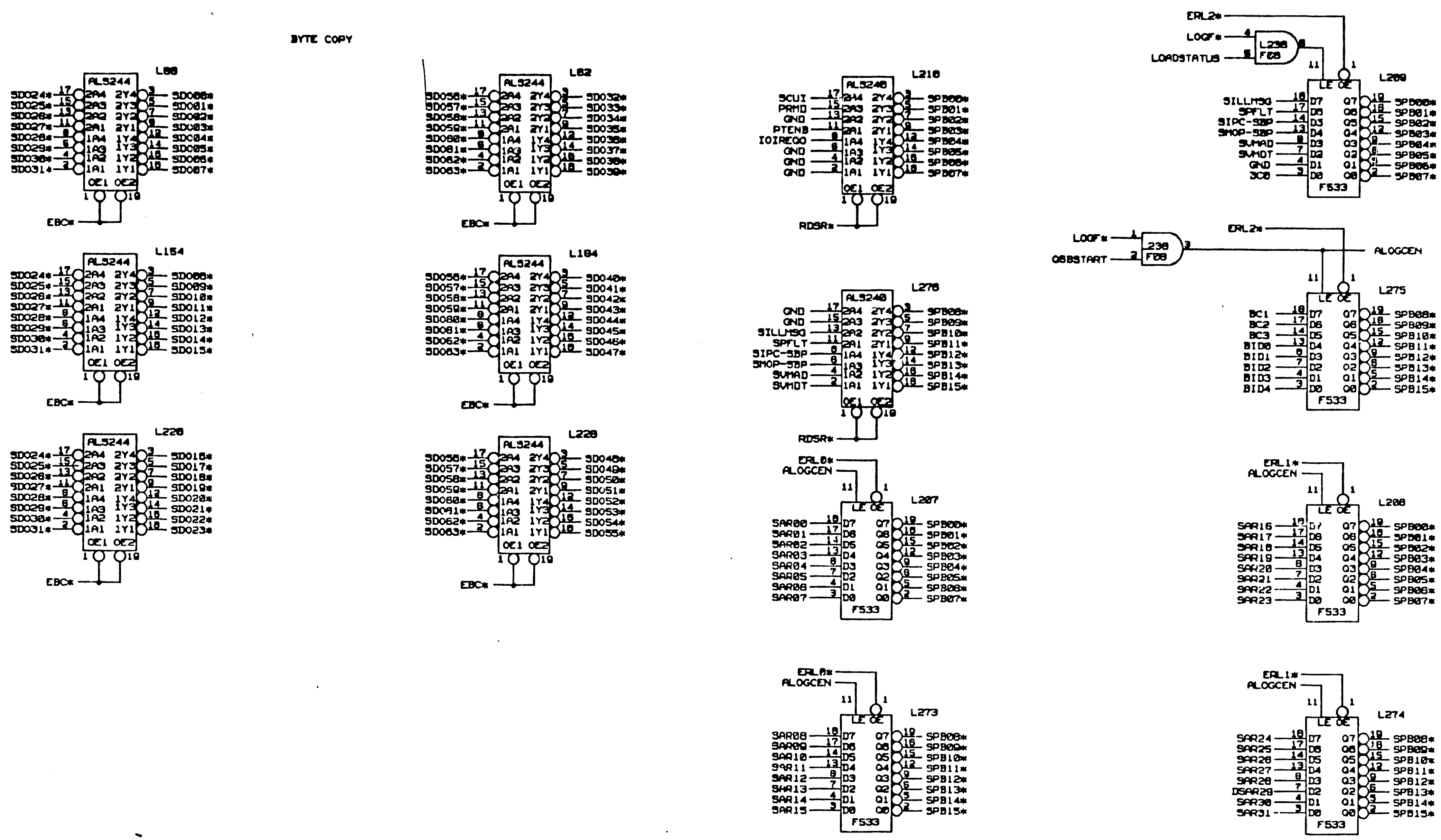
DRAWING

VSXXXSBI.LOGIC . 15

LAST_MODIFIED=Mon Jun 17 12:11:08 1985

(WANG) LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 15 OF 22


TEST/SET BUFFER
SAIR REG
PT RAM
PTWADR BUFFER
PFN 0 TO 16383
SA= 00000000 TO 01FFFFFF
PFN 16384 TO 32767
SA = 02000000 TO 03FFFFFF
PRMDO = 1 = PAGE PROTECTED
FAULT = CHGSAR*. (ILLMSG+BC0*. PTEN0. BID0*. (PTA04+PTA05+PRMDO))
ILLMSG = BID0. BC0*. BC1*. BC2*. (PTA12+PTA13. PTA14. PTA15)
DRAWING
VSXXXSBI..1.16
LAST_MODIFIED=Mon Jun 17 12:12:54 1985
WANG LABORATORIES, INC.
REV: R0
TITLE: VS300 SBI 9236
DATE: 6/14/85
ENGINEER:
PAGE: 16 OF 22

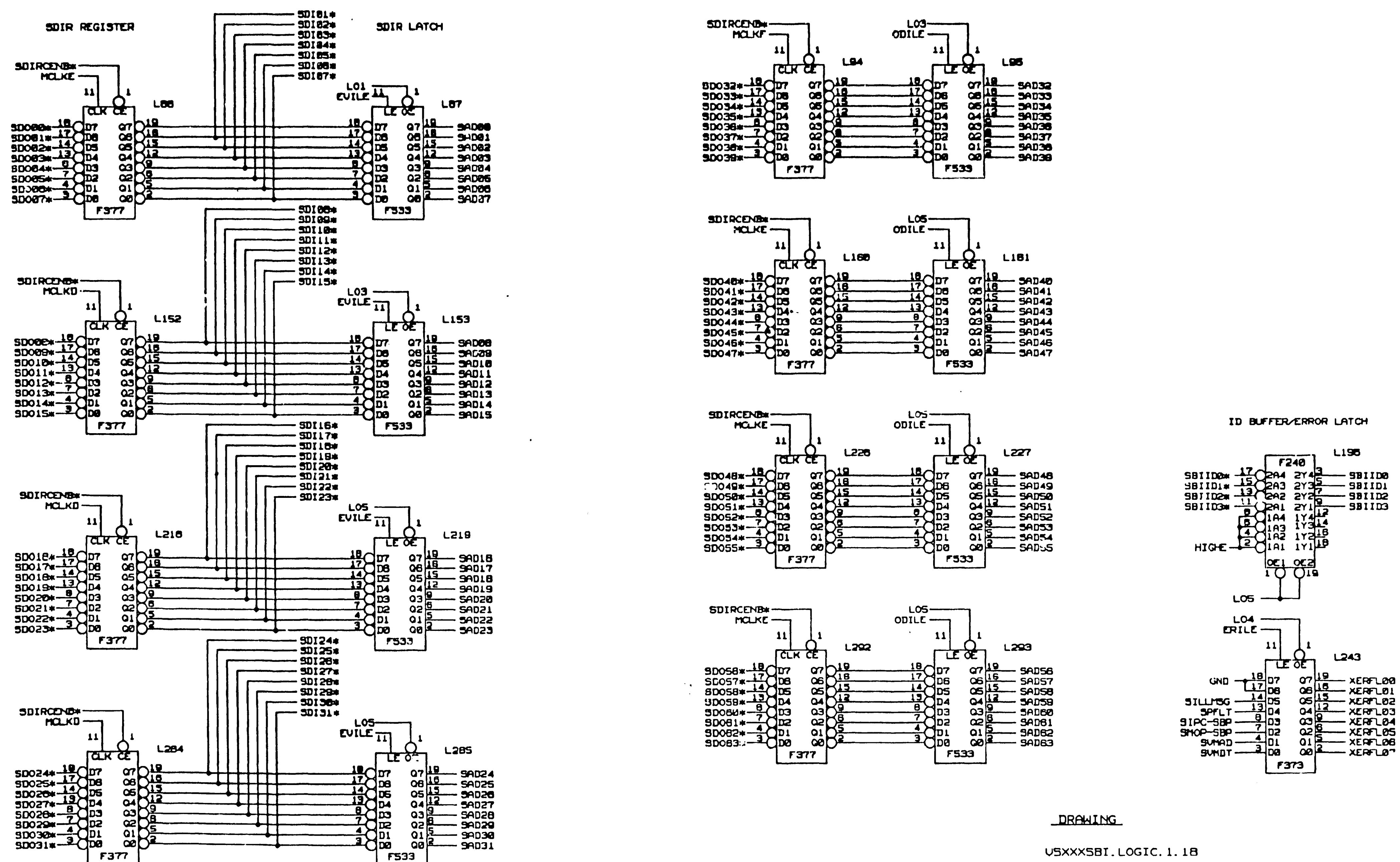


DRAWING

VSXXXSBI.LOGIC.1.17

LAST_MODIFIED=Mon Jun 17 12:14:37 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 17 OF 22



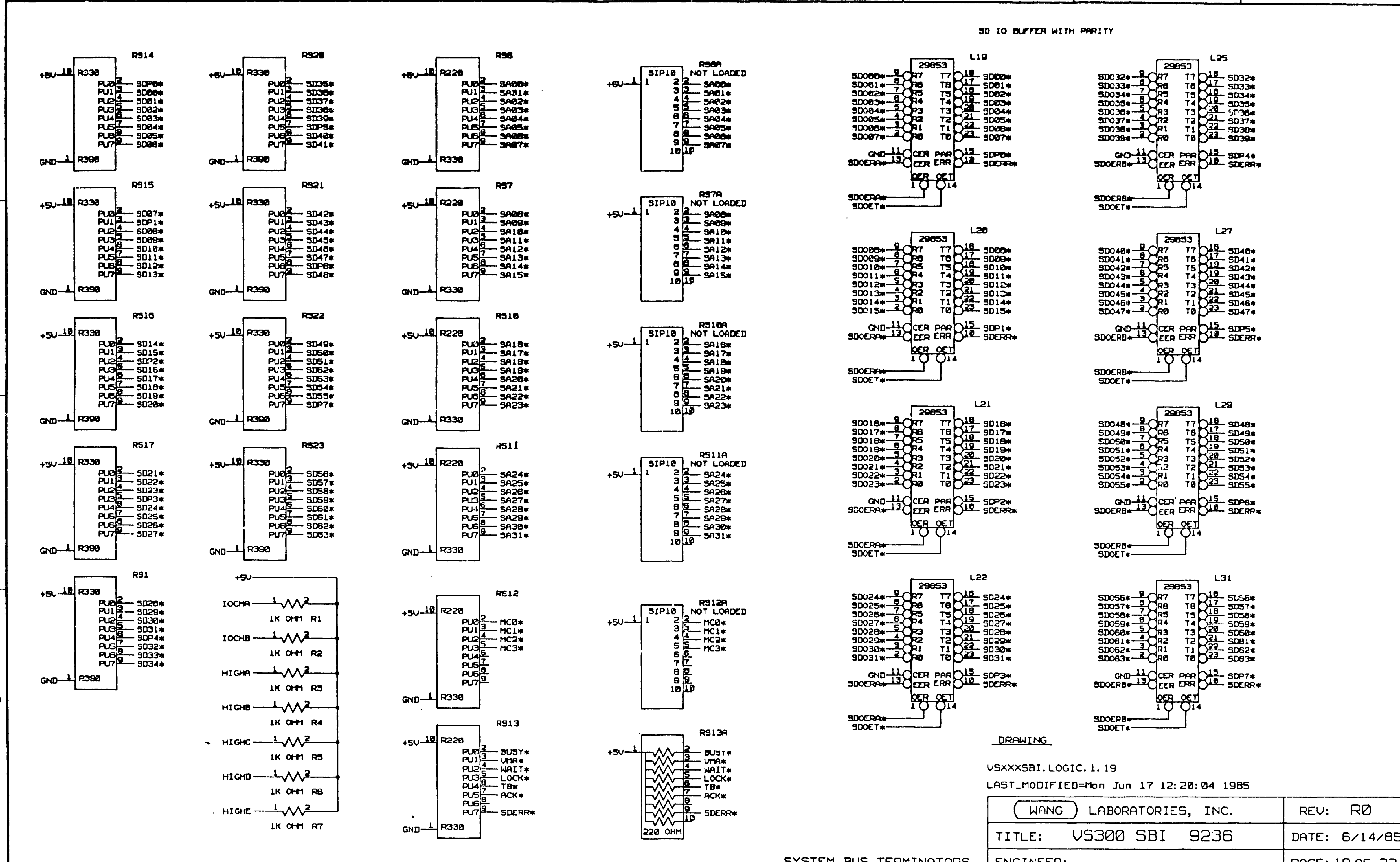
DRAWING

VSXXXSBI.LOGIC.1.18

LAST_MODIFIED=Mon Jun 17 12:17:06 1985

SYSTEM DATA INPUT REGISTER, IO BUFFER

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 18 OF 22

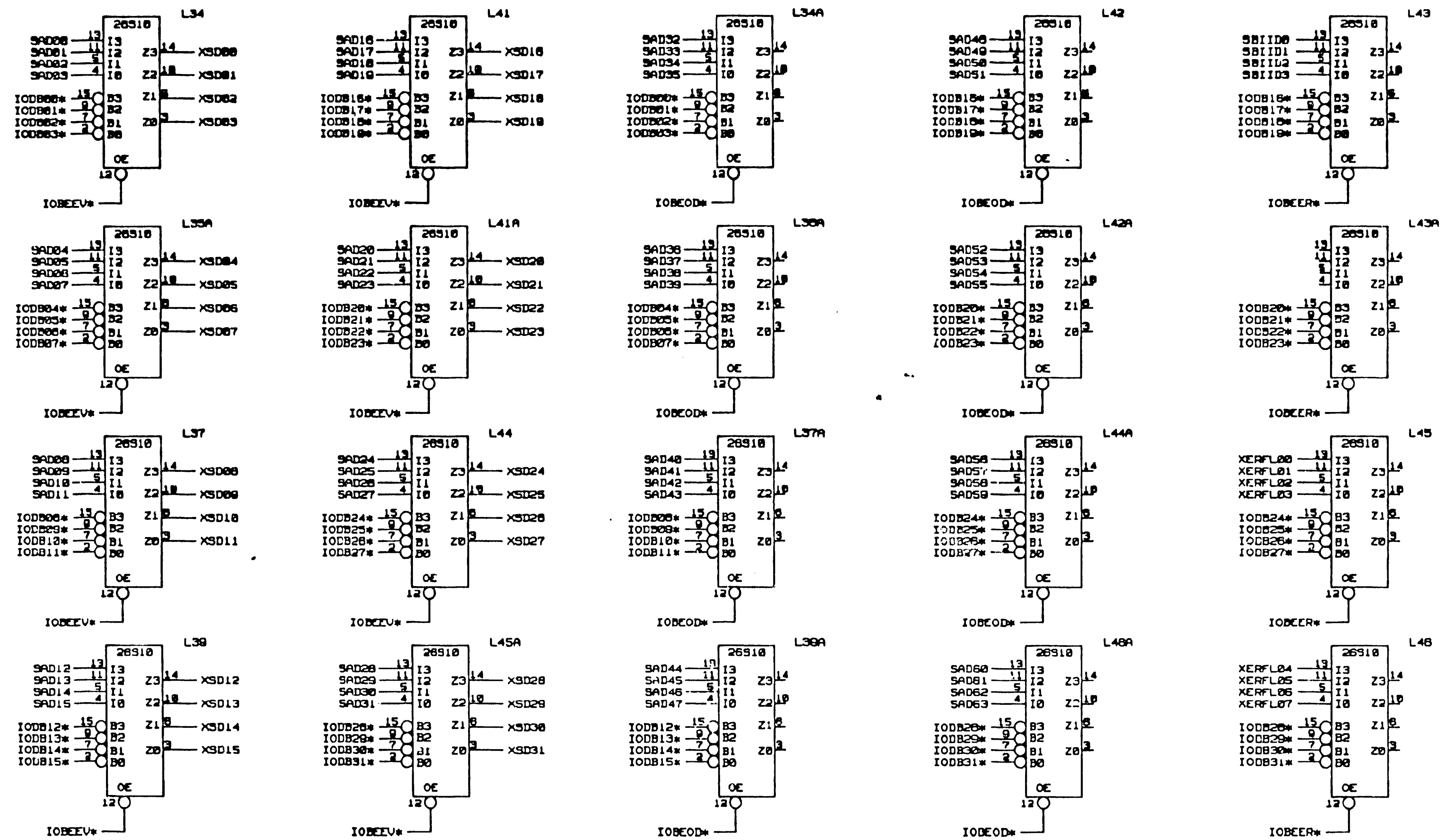


DRAWING

VSXXXSBI.LOGIC.1.19

LAST_MODIFIED=Mon Jun 17 12:20:04 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 19 OF 22



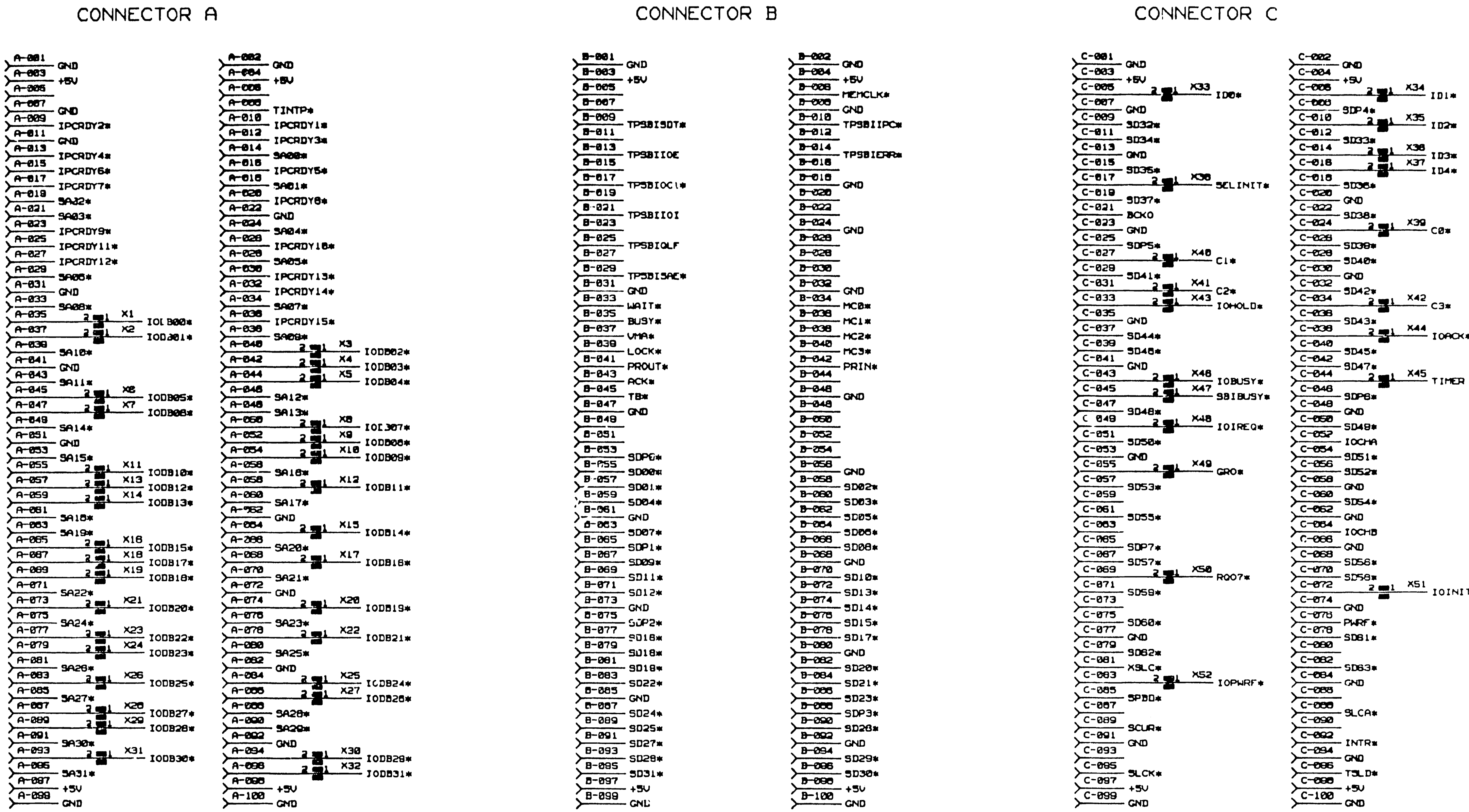
DRAWING

IO DATA BUS DRIVERS

VSXXXSBI..1.20

LAST_MODIFIED=Mon Jun 17 12:00:06 1985

WANG LABORATORIES, INC.		REV: R0
TITLE:	VS300 SBI 9236	DATE: 6/14/85
ENGINEER:		PAGE: 20 OF 22



DRAWING

VSXXXSBI..1.21

LAST_MODIFIED=Mon Jun 17 12:05:13 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE:21 OF 22

BACKPLANE CONNECTOR

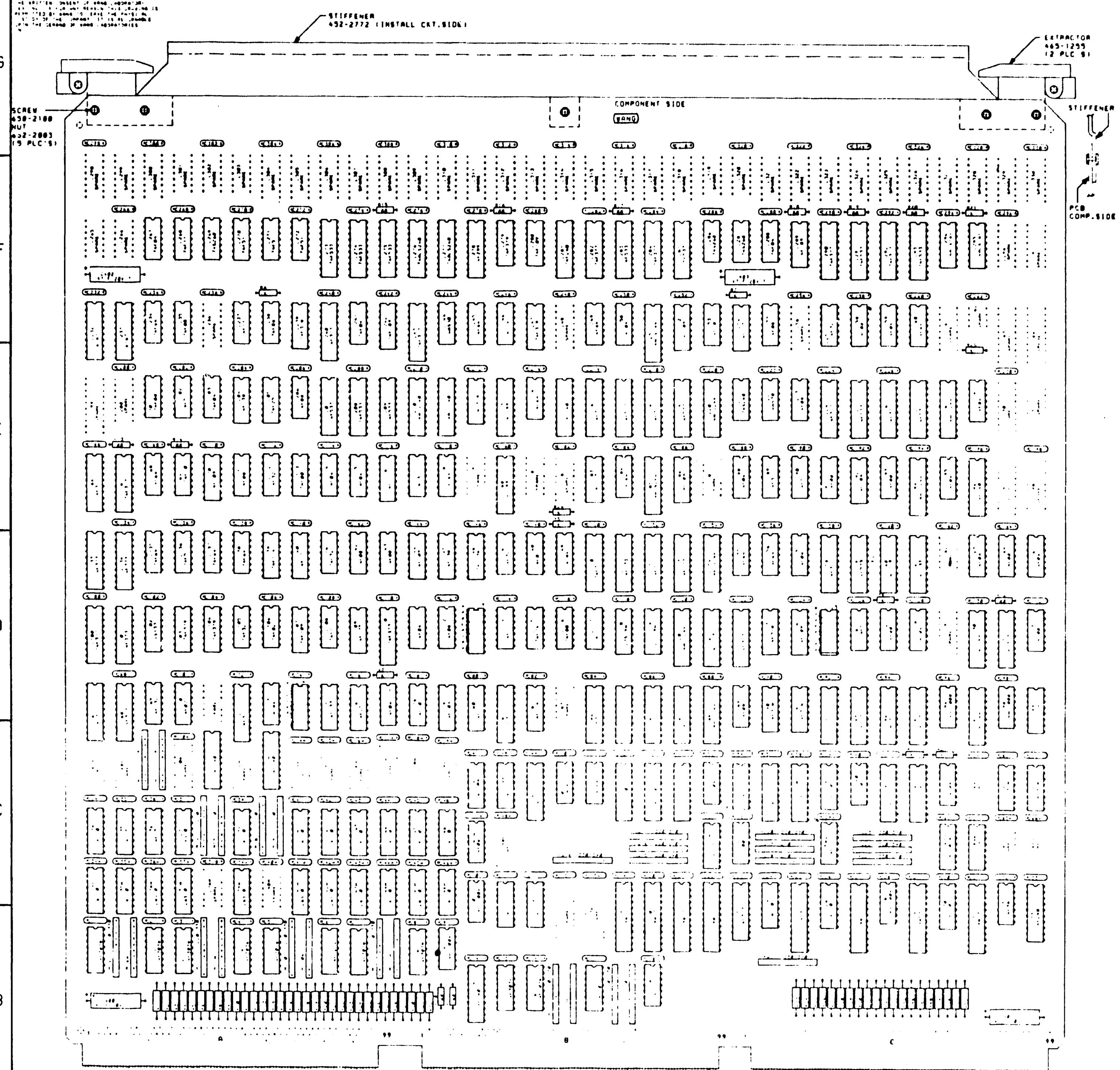
- SPARES LIST -

74F00 L191-11, L258-8, L164-11, L56A-11, L193-11
74F02 L106-4, L70-1, L70-4, L70-11, L148-11
74F04 L188-5, L203-3, L203-8, L203-10, L203-12
74F08 L47A-11, L238-11, L171-4, L183-11, L201-4
74F10 L253-8, L169-8
74F11 L117-8, L117-3, L59A-3
74F20 L78-8
74AS32 L18-8, L18-11
74F32 L257-11
74F38 L32-1
74F51 L126-1, L190-1
74F86 L149-4, L149-8, L149-11
74F109 L192-9
74S260 L286-4
74AS1000 L98-11
MACHINE SOCKET L125-5, L125-6, L125-7

DRAWING

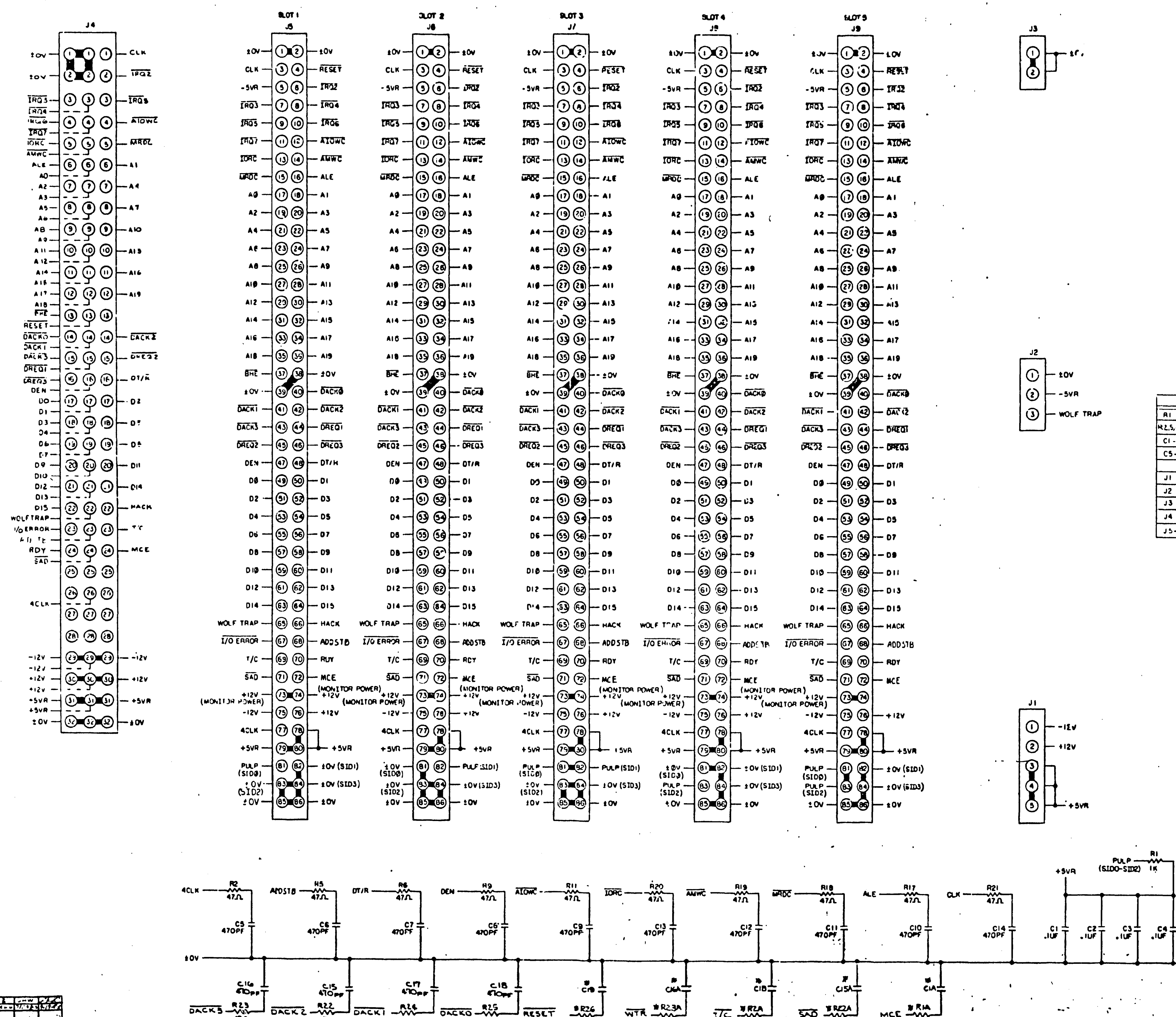
VSXXXSBI.LOGIC.1.22
LAST_MODIFIED=Fri Jun 14 15:05:47 1985

WANG LABORATORIES, INC.	REV: R0
TITLE: VS300 SBI 9236	DATE: 6/14/85
ENGINEER:	PAGE: 22 OF 22



NOTES
1. UNLESS OTHERWISE SPECIFIED,
ALL CAPACITORS ARE .047UF EXPRESSED IN MICROFARADS.
ALL RESISTORS ARE 1K 1/4W 5% EXPRESSED IN OHMS.
2. RS6A RS7A RS10A RS11A RS12A ARE NOT LOADED.
3. REFERENCE ASSEMBLY PRINT AND/OR SCHEMATICS FOR JUMPER CONFIGURATIONS.
JUMPERS ARE 376.9129.

WANG		BY	DATE	APPROVED BY	DATE
		DWN FVZ		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. VS300	E C CONTROL		MFG ENGR	
	10-214	TITLE VS300 SBI			
FINISH		214-9236	C	9236	0



COMPONENT	TYPE	WL PART NO
R1	1K 1/4W 5%	330-3011
R2,5,6,9,11,17-25	47Ω 1/4W 5%	330-1048
C1-4	.1UF 50V	300-1833
C5-19	470PF 50V	300-1083
J1	CONN,5PIN	350-0238
J2	CONN,3PIN	350-0217
J3	CONN,2PIN	350-0218
J4	CONN,96PIN	350-0492
J5-9	CONN,96PIN	350-0473

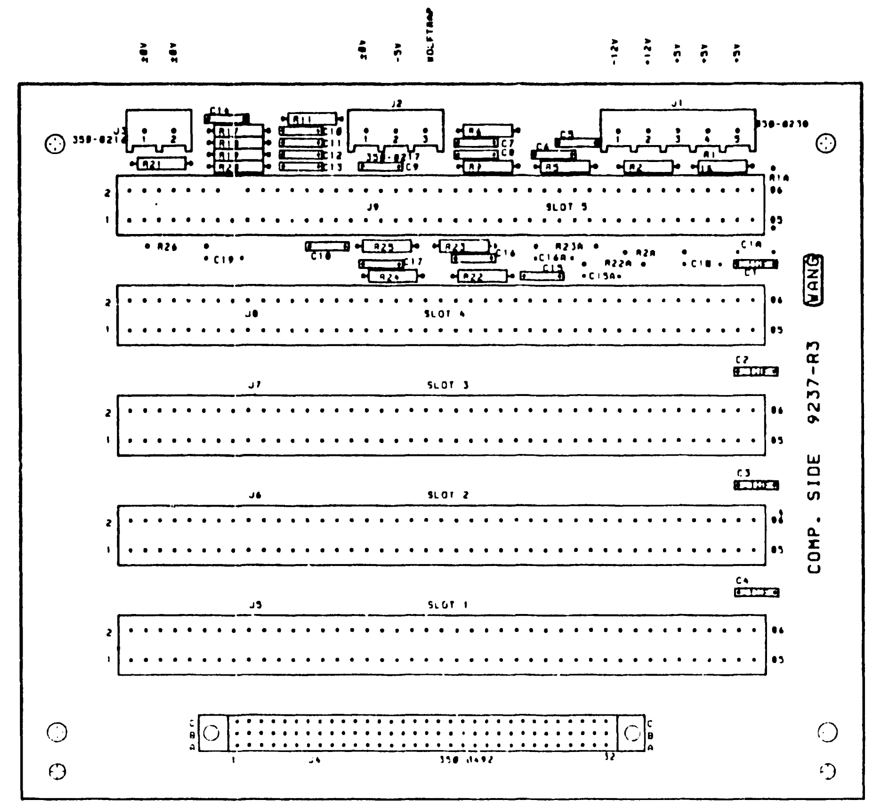
NOTE:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE IN OHMS 1/4W, 5%
* 2. C1A, C1B, C15A, C16A, C19, R1A, R2A, R22A, R23A, R26 ARE NOT LOADED AT THIS TIME FOR E.C.O. 29225.

E-REV 1

WANG

MOTHER BOARD

210-9237 E 9237



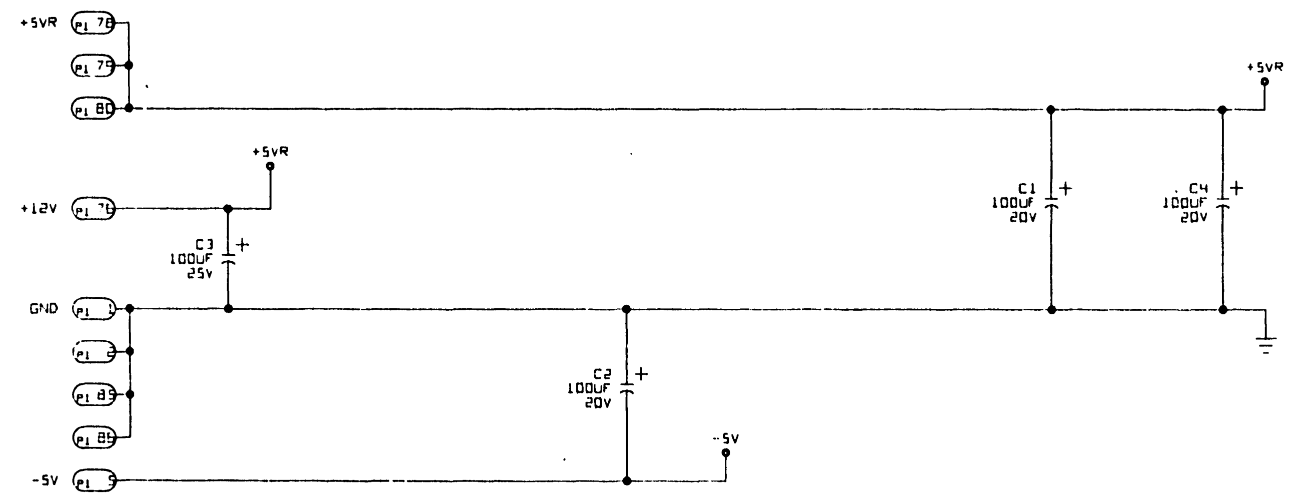
NOTES: 1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE 47 OHM 1/4W, 5%, EXPRESSED IN OHMS.
CONNECTORS J5-J9 ARE 350-0473.
CAPACITORS C5-C18 ARE 470 PF, P/N 300-1003.

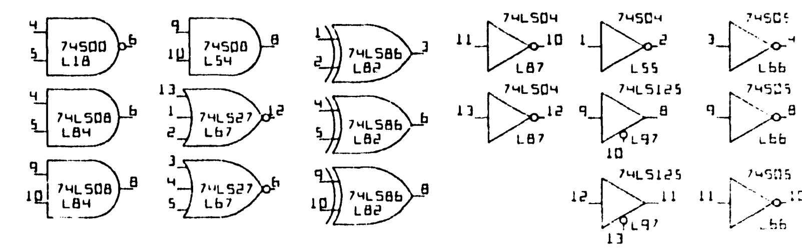
REV	NO.
EBA 7-20-83	DWR#E2125	1
SJM 9-22-83	ECO # 29229, 29096	2
GWC 11-4-83	ECO #30143	3

WANG LABORATORIES INC. LOWELL MASS. U.S.A.		BY	DATE	APPROVED BY	DATE
		DWN E.ACHESON	7-20-83	E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. PBC H0067A	E C CONTROL		MFG ENGR	
	SEE ENGRG SPECIFICATIONS NO. 10-213	TITLE MULTILAYER MOTHER BOARD ASSEMBLY DRAWING			
FINISH	TOL. EX. AS NOTED	210-9237-R3 (WANG PART NUMBER)	C (SIZE)	9237 (DRAWING NUMBER)	3 (REV)
	SCALE 1/1 SHT 4 OF 8				

NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.





MNEMONIC	COORD
ATCWC	5B11
AMWC	2C11
BHE	2C11
CLK	2A11
DACKD	2A11
DLRESTART	4A1
HACK	2B11
I/OADDRMATCH	5A7
I/OERROR	6B1
IORC	5D11
MRDC	2C11
PA0-PA7,PA16-PA19	3G11
PA8-PA15	6D11
PARITYERROR	6A1
PARITYCONTROL	6C11
PD0-PD15	6E1
PINT	5F11
RCYCLE	3C1
RDY	2B1

MNEMONIC	COORD
RESET	5A11
SAD	5D11
SID0-SID3	5C11
ZA0-ZA15	5E1
ZBUSAK	3E11
ZBUSRQ	4G1
ZCRTSEL	3E11
ZCRTWT	3E1
ZDLREQ	4F1
ZD0-ZD7	5G1
ZRD	4F1
ZRESET	6A11
ZWAIT	[illegible]
ZBCBCARDPRESENT	5E11
4CLK	3A11
+GA	5B1
+GB	5B1
-RA	5B1
-RB	5A1

E REV
1

BY	KTH	PGD	PGD	KTH	KTH	AB	JSW
DATE	7-29-83	11-14-83	12-29-83	05-09-84	05-09-84	07-05-84	8-14-84
REVISION	ORIGINATED PER DWP NO. [illegible] APPR:	REVISED PER ECO NO. 29895 APPR:	REVISED PER ECO NO. 29990 APPR:	REVISED PER ECO NO. 31448 CHKR:	REVISED PER ECO NO. 31799 CHKR:	REVISED PER ECO NO. 32222 CHKR:	REVISED PER ECO NO. 33195 CHKR:
NO	0	1	2	3	4	5	6

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

SCHEMATIC DIAGRAM

TITLE: PC LOCAL COMM BD

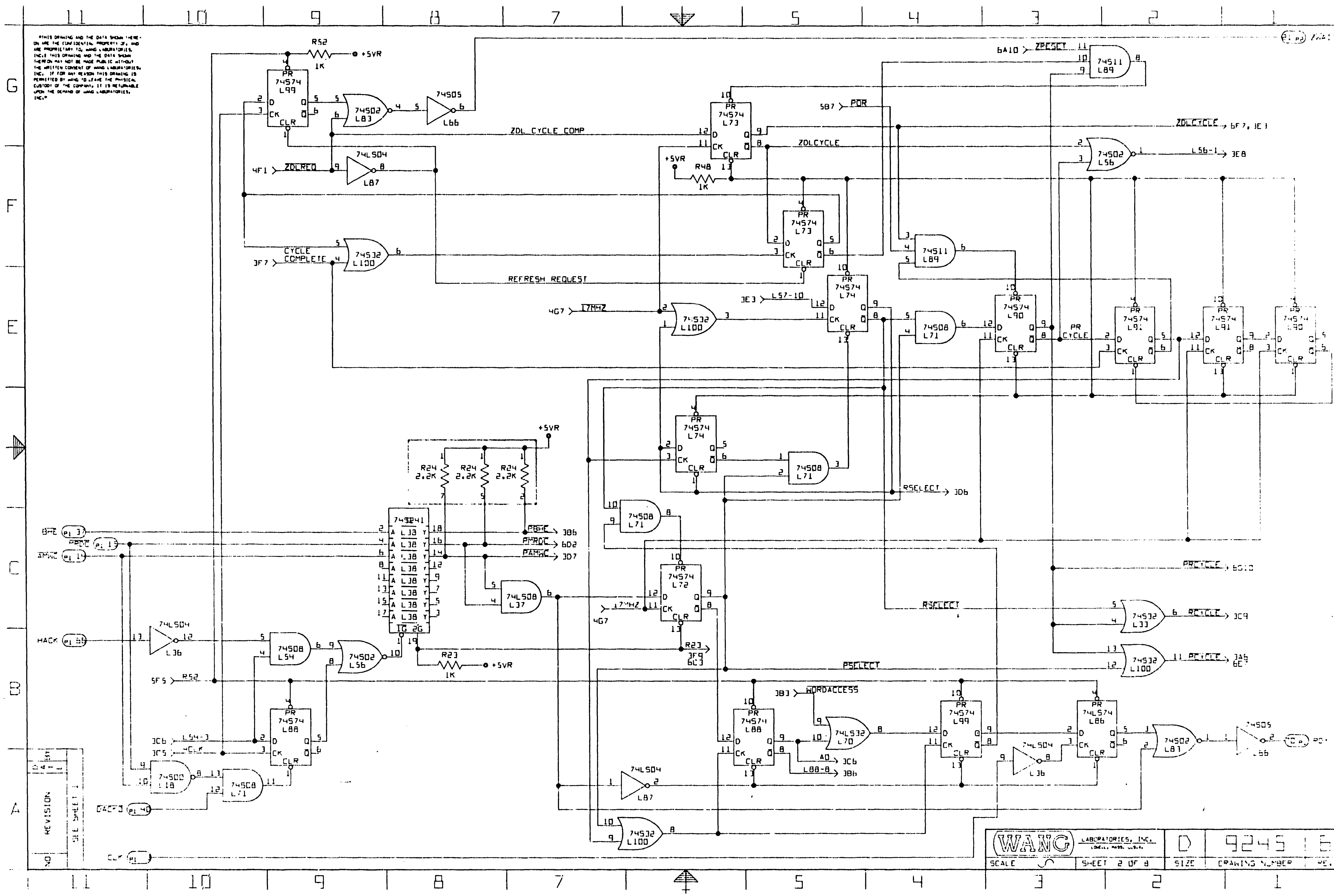
MODEL NUMBER: P67A PBC

WANG PART NUMBER: 210-9245

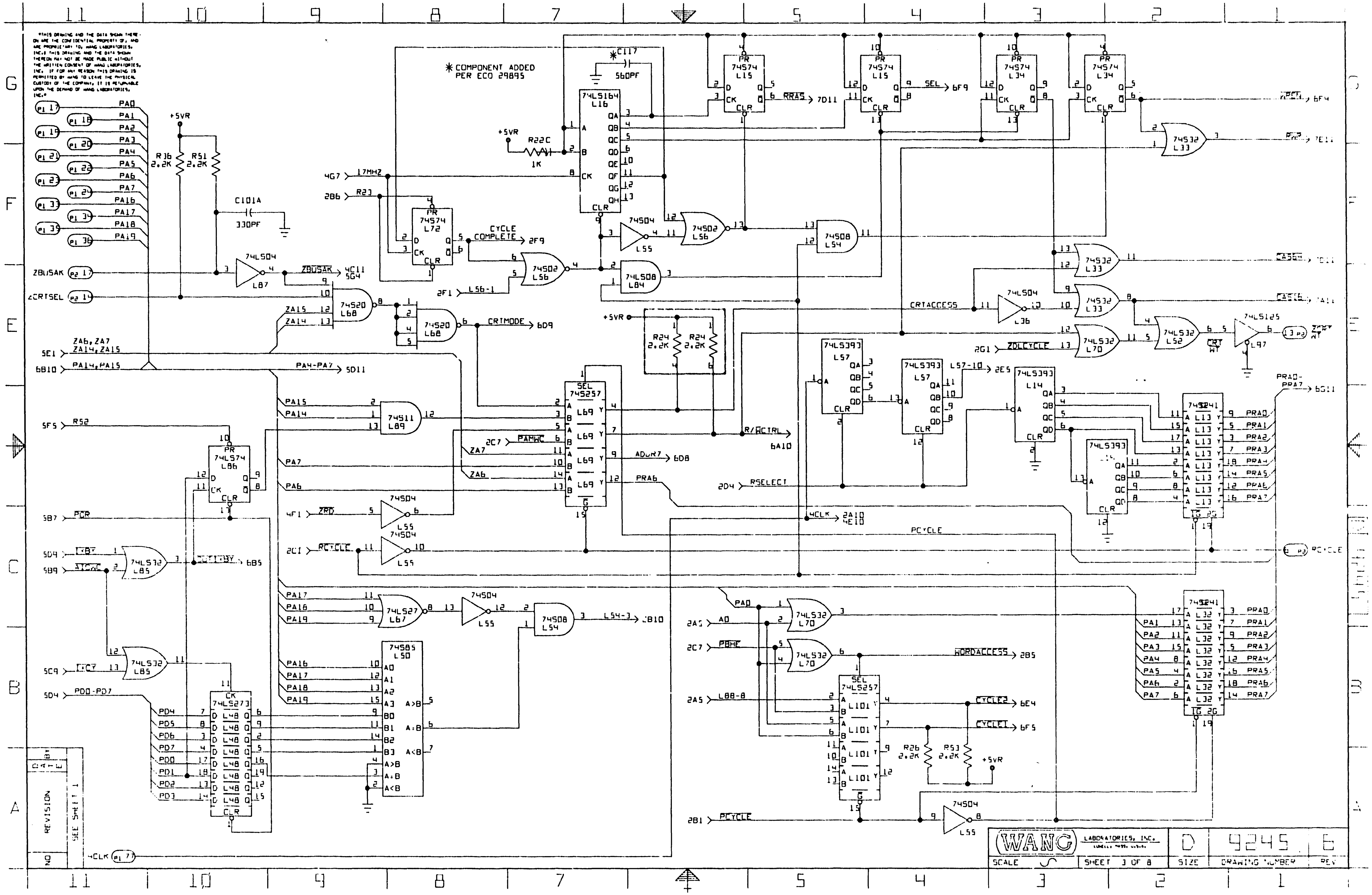
DWN KTH CHK ENG DIR

SIZE: D | DRAWING NUMBER: 9245 | REV: 6

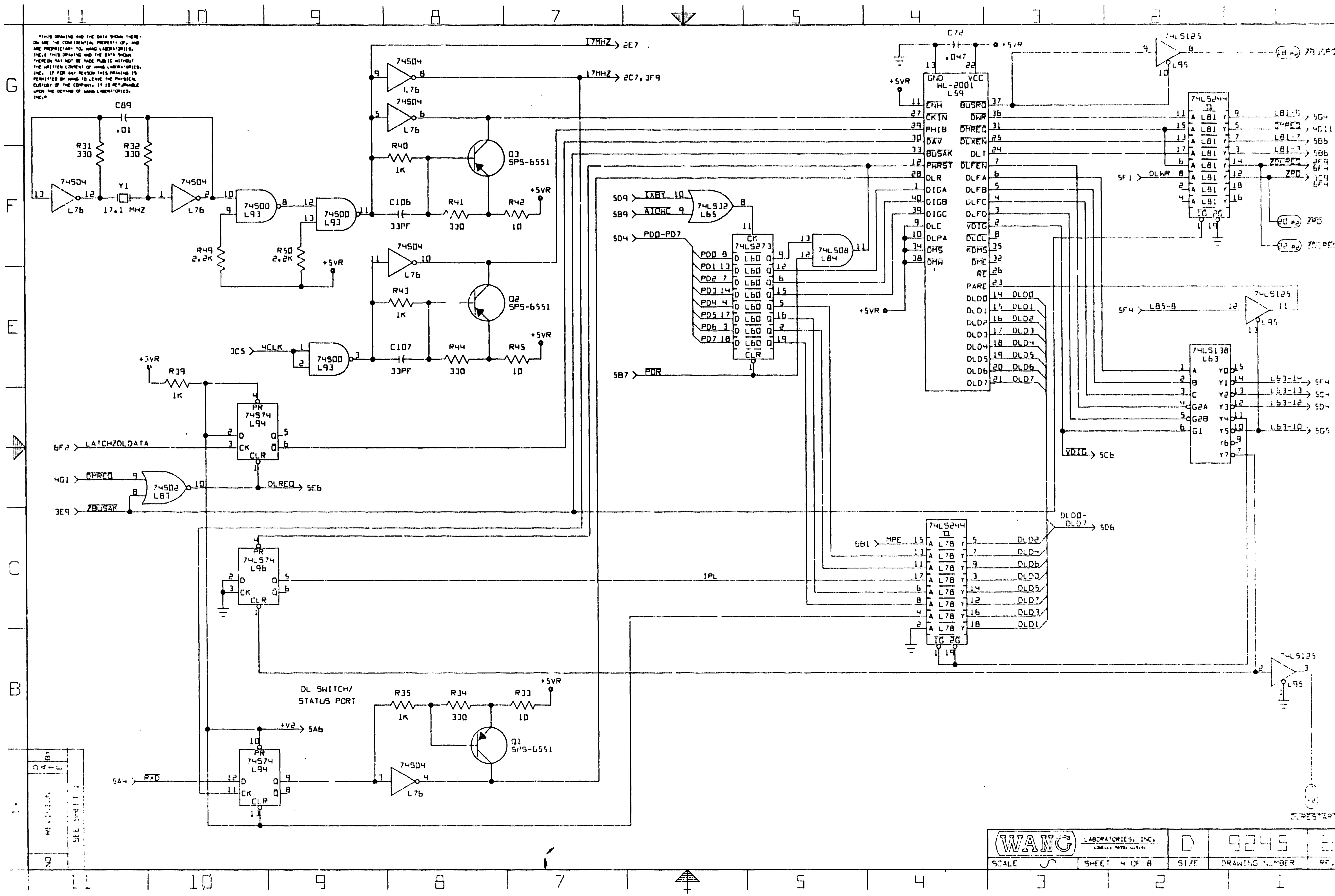
SCALE: — | SHEET 1 OF 8



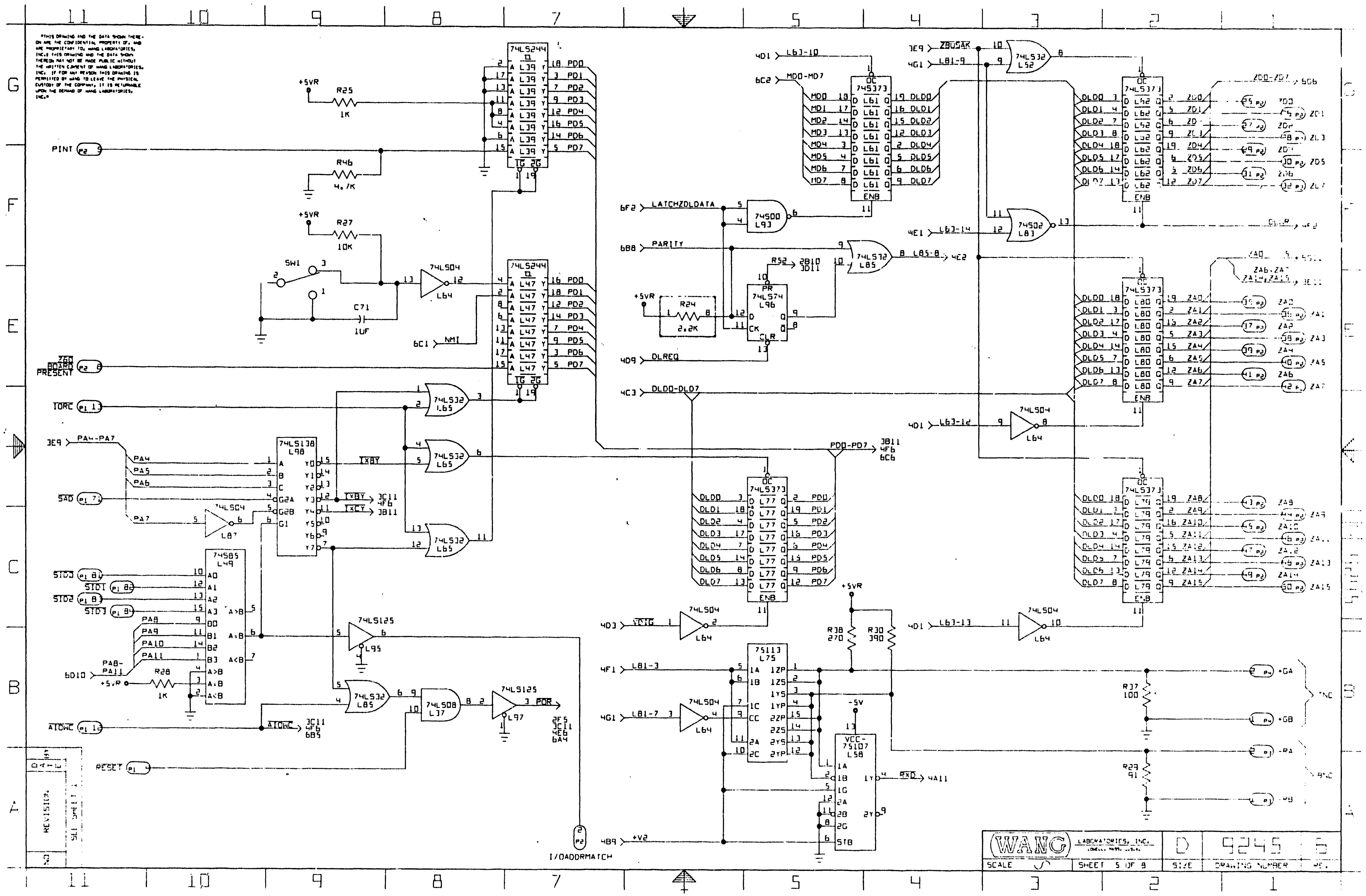
74S74 L99
74S02 L83
74S05 L66
74LS04 L87
ZDLREQ
ZDL CYCLE COMP
74S74 L73
ZDLCYCLE
74S11 L89
74S02 L56
CYCLE COMPLETE
74S32 L100
REFRESH REQUEST
17MHZ
74S74 L74
74S08 L71
74S74 L90
74S74 L91
RSELECT
74S241
74LS08 L37
PBME
PMRDC
PAMWC
HACK
74LS04 L36
74S08 L54
74S02 L56
74S74 L88
74S74 L72
74LS32 L70
WORDACCESS
74S74 L99
74LS74 L86
74S02 L87
74S05 L66
74S32 L33
PRECYCLE
74S32 L100
PSELECT
74LS04 L87
74S32 L100
R52 1K
R48 1K
R24 2.2K
R23 1K
+5VR
WANG LABORATORIES, INC.
D
9245
SHEET 2 OF 8
SCALE
SIZE
DRAWING NUMBER
REV.
REVISION



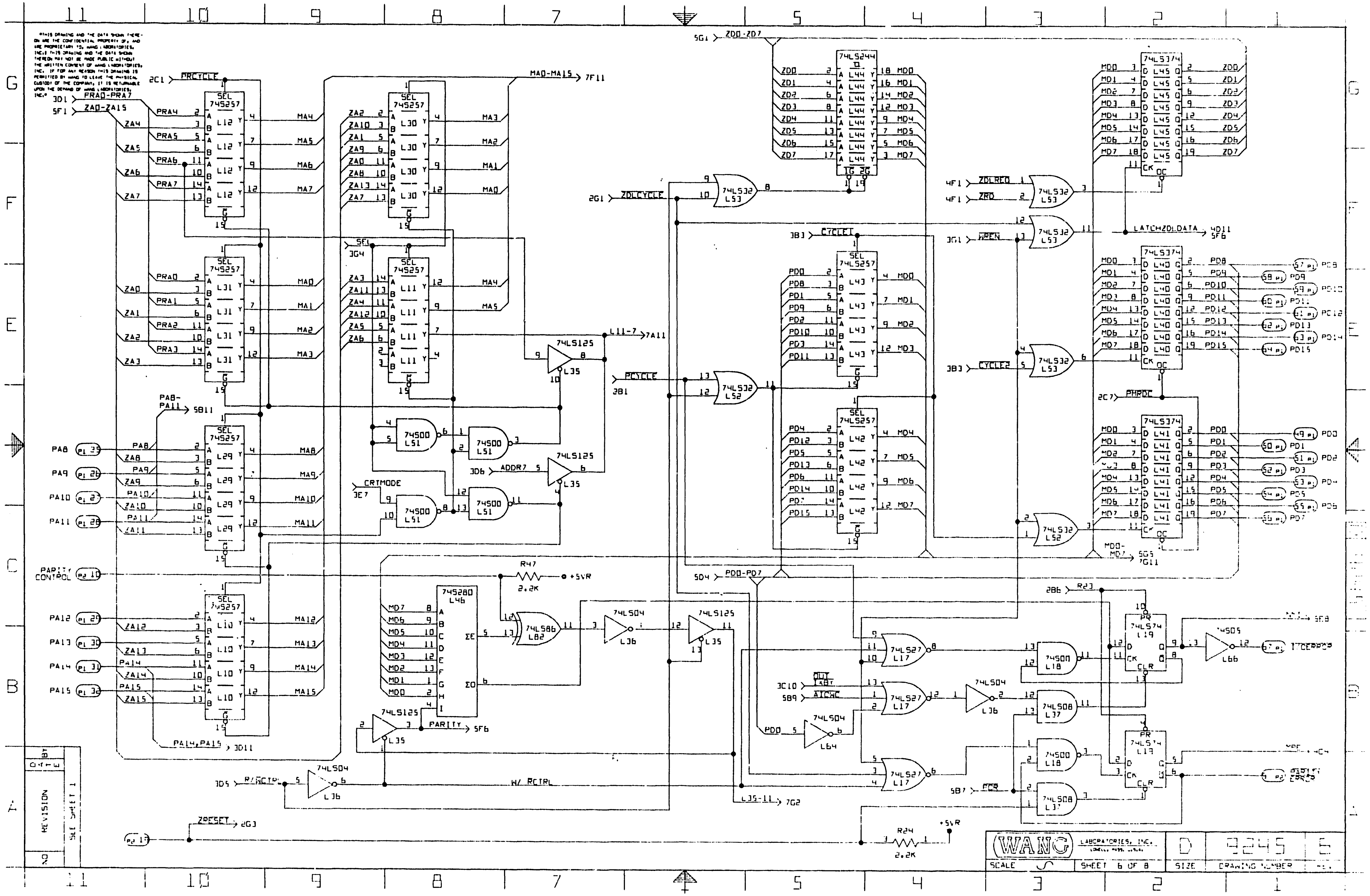
* COMPONENT ADDED PER ECO 29895
74LS164 L16
74S74 L15
74S74 L34
74S74 L72
74LS04 L87
74S20 L68
74S02 L56
74S08 L84
74S08 L54
74S32 L33
74LS32 L52
74LS32 L70
74LS125 L97
74LS393 L57
74LS393 L14
74S241 L13
74S241 L32
74S257 L69
74S11 L89
74LS74 L86
74LS32 L85
74LS27 L67
74S85 L50
74LS273 L48
74LS257 L101
CYCLE COMPLETE
CRTMODE
CRTACCESS
ZBUSAK
ZCRTSEL
RSELECT
WORDACCESS
CYCLE2
CYCLE1
PCYCLE
17MHZ
ADUR7
R/ACTRL
WANG LABORATORIES, INC.
SCALE
SHEET 3 OF 8
SIZE D
DRAWING NUMBER 9245
REV E



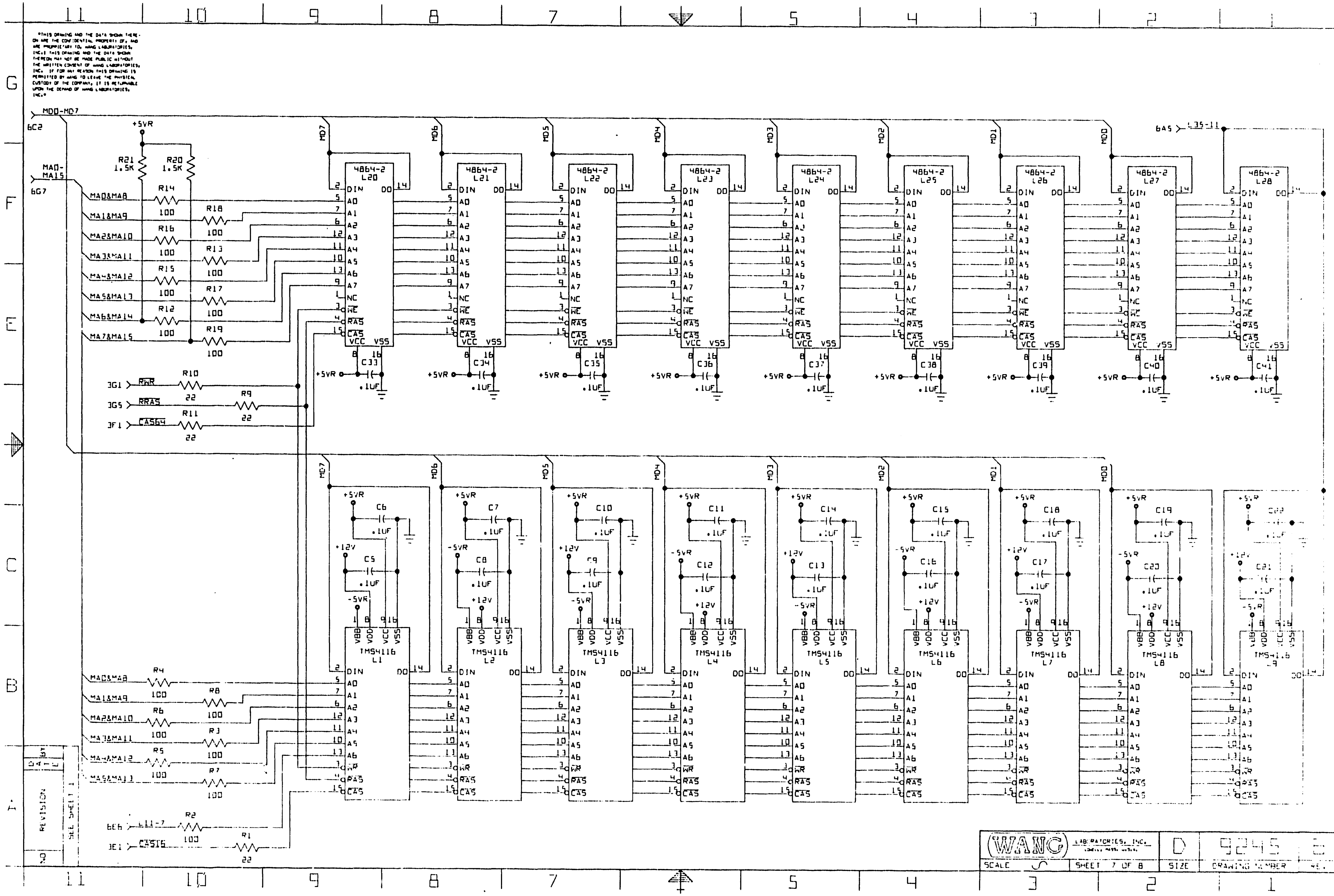
17MHZ 2E7
17MHZ 2C7, 3F9
C89 .01
R31 330
R32 330
74S04 L76
Y1 17.1 MHZ
74S00 L93
R49 2.2K
R50 2.2K
+5VR
R40 1K
Q3 SPS-6551
C106 33PF
R41 330
R42 10
R43 1K
Q2 SPS-6551
C107 33PF
R44 330
R45 10
3C5 4CLK
R39 1K
74S74 L94
6F2 LATCH2DLDATA
4G1 CMREQ
74S02 L83
DLREQ 5E6
3E9 ZBUSAK
74LS74 L96
IPL
DL SWITCH/
STATUS PORT
R35 1K
R34 330
R33 10
Q1 SPS-6551
+V2 5A6
5A4 PXD
C72 .047
+5VR
WL-2001 L59
GND VCC
ETH CKIN PHIB DAV BUSAK PWRST DLR DIGA DIGB DIGC DLE DLPA DHS DHW
BUSRQ DWR DHREQ DLXEN DLT DLFEN DLFA DLFB DLFC DLFD VDIG DLCL RDHS DHC RE PARE
DLD0 DLD1 DLD2 DLD3 DLD4 DLD5 DLD6 DLD7
5D9 IXBY
5B9 AIDHC
74LS32 L65
5D4 PD0-PD7
74LS273 L60
74LS08 L84
5B7 POR
74LS125 L95
74LS244 L81
5F1 DLWR
5F4 LB5-B
74LS138 L63
VDIG 5C6
DLD0-DLD7 5D6
6B1 MPE
74LS244 L78
WANG LABORATORIES, INC.
D 9245
SCALE
SHEET 4 OF 8
SIZE
DRAWING NUMBER
REV.



WANG LABORATORIES, INC.
D
9245
6
SCALE
SHEET 5 OF 8
SIZE
DRAWING NUMBER
REV.
74LS244
74LS373
74LS138
74S85
74LS32
74LS04
74LS125
74LS08
74S00
74S02
74LS74
75113
75107
PINT
IORC
PA4-PA7
SAD
RESET
I/OADDRMATCH
LATCHZDLDATA
PARITY
DLREQ
DLD0-DLD7
PD0-PD7
ZBUSAK
MD0-MD7



74S257
74LS244
74LS374
74LS257
74LS32
74LS125
74S00
74S280
74LS86
74LS04
74LS27
74LS74
74S08
74S05
PRA0-PRA7
ZA0-ZA15
MA0-MA15
ZD0-ZD7
PD0-PD7
MD0-MD7
LATCHZDLDATA
PARITY
PARITY CONTROL
CRTMODE
ADDR7
W/ RCTRL
ZRESET
R47
R23
R24
2.2K
+5VR
REVISION
SEE SHEET 1
WANG LABORATORIES, INC.
SCALE
SHEET 6 OF 8
SIZE
D
DRAWING NUMBER



MD0-MD7
MA0-MA15
+5VR
R21 1.5K
R20 1.5K
4864-2
TMS4116
RAS
CAS64
CAS16
WANG LABORATORIES, INC.
SCALE
SHEET 7 OF 8
SIZE D
DRAWING NUMBER
9245

IC LOCATION	TYPE	W.L. PART NO.
L1-L9	TMS4116-20JL	377-0345
L20-L28	4864-2	377-0417
L10-L12,L29-L31,L69	74S257	376-0131
L13,L32,L38	74S241	376-0506
L14,L57	74LS393	376-0307
L15,L34,L72-L74,L88, L90,L91,L94,L99	74S74	376-0202
L16	74LS164	376-0236
L17,L67	74LS27	376-0245
L18,L51,L93	74S00	376-0228
L19,L86,L96	74LS74	376-0155
L33,L100	74S32	376-0205
L35,L95,L97	74LS125	376-0486
L36,L64,L87	74LS04	376-0180
L37,L84	74LS08	376-0153
L39,L44,L47,L78,L81	74LS244	376-0288
L40,L41,L45	74LS374	376-0286
L42,L43,L101	74LS257	376-0204
L46	74S280	376-0246
L48,L60	74LS273	376-0302

IC LOCATION	TYPE	W.L. PART NO.
L49,L50	74S85	376-0259
L52,L53,L65,L70,L85	74LS32	376-0211
L54,L71	74S08	376-0200
L55,L76	74S04	376-0197
L56,L83	74S02	376-0199
L58	75107	376-0146
L59	2001	397-0508
L61	74S373	376-0306
L62,L77,L79,L80	74LS373	376-0310
L63,L98	74LS138	376-0294
L66	74S05	376-0555
L68	74S20	376-0230
L75	75113	376-0256
L82	74LS86	376-0231
L89	74S11	376-0237
L92,L102-L104	SPARE	

COMPONENT	TYPE	W.L. PART NO.	QTY
C1-C4	100UF 20V (T)	300-4067	4
C5-C22,C33-C41	.1UF 50V	300-1833	27
C23-C32,C42-C70,C72-C88,C90-C105,C108-C116	.047UF 50V	300-1966	81
C71	1UF 35V 10%	300-4110	1
C89	.01UF 25V	300-1903	1
C101A	330PF	300-1834	1
C106,C107	33PF 500V	300-1033	2
C117	560PF 10% 500V	300-1560	1
R1,R9-R11	22 1/4W 5%	330-1023	4
R2-R8,R12-R19,R37	100 1/4W 5%	330-2011	16
R20,R21	1.5K 1/4W 5%	330-3016	2
R22,R23,R25,R28,R35, R39,R40,R43,R48,R52	1K 1/4W 5%	330-3011	10
R24	2.2K SIP	333-0806	1
R26,R36,R47,R49 R50,R51,R53	2.2K 1/4W 5%	330-3023	7
R27	10K 1/4W 5%	330-4011	1
R29	91 1/4W 5%	330-1092	1
R30	390 1/4W 5%	330-2040	1
R31,R32,R34,R41,R44	330 1/4W 5%	330-2034	5
R33,R42,R45	10 1/4W 5%	330-1011	3
R38	270 1/4W 5%	330-2028	1
R46	4.7K 1/4W 5%	330-3042	1
[illegible]9	40 PIN SKT	376-9011	1
J3	CONN BNC	350-1036	1
J4	CONN TNC	350-2078	1
Q1-Q3	SPS 6551	375-1050	3
SW1		325-0040	1
Y1	17.1 MHZ	321 3018	1
	CONN TNC	350-2078	1
	CONN BNC	350-1036	1
	GND LUG	654-1011	2
	R. F. SHIELD	458-3086	1
	SCREW 3/8" 8-32	650-4120	2
	NUT 8-32	652-0029	2
	EJECTOR	465-1250	1
	LBL,REMOVE LCAL CONN	615-2201	1
	LBL,R.F.SHEILD 8245/9245	615-2204	1
	WIRE 22GA BLK	600-0300	A/R
	WIRE 22GA RED	600-0302	A/R

NOTES

1. ALL RESISTOR VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS UNLESS OTHERWISE INDICATED.
3. ALL RESISTORS 1/4W 5% UNLESS OTHERWISE INDICATED.

E REV 1

WANG LABORATORIES, INC. LOWELL, MASS. U.S.A.

SCHEMATIC DIAGRAM

TITLE PC LOCAL COMM [illegible] BD

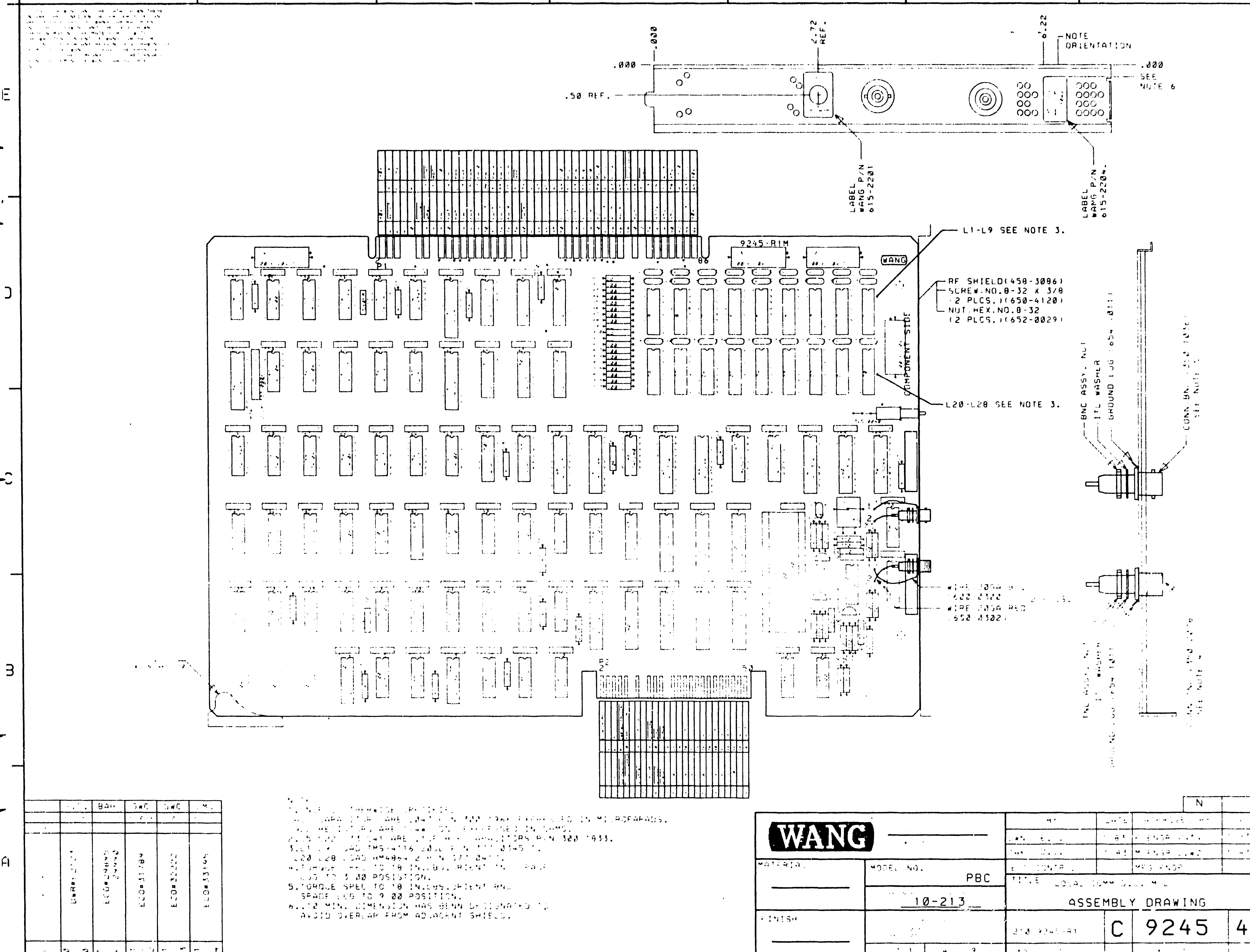
MODEL NUMBER P67A PBC

WANG PART NUMBER 210-9245

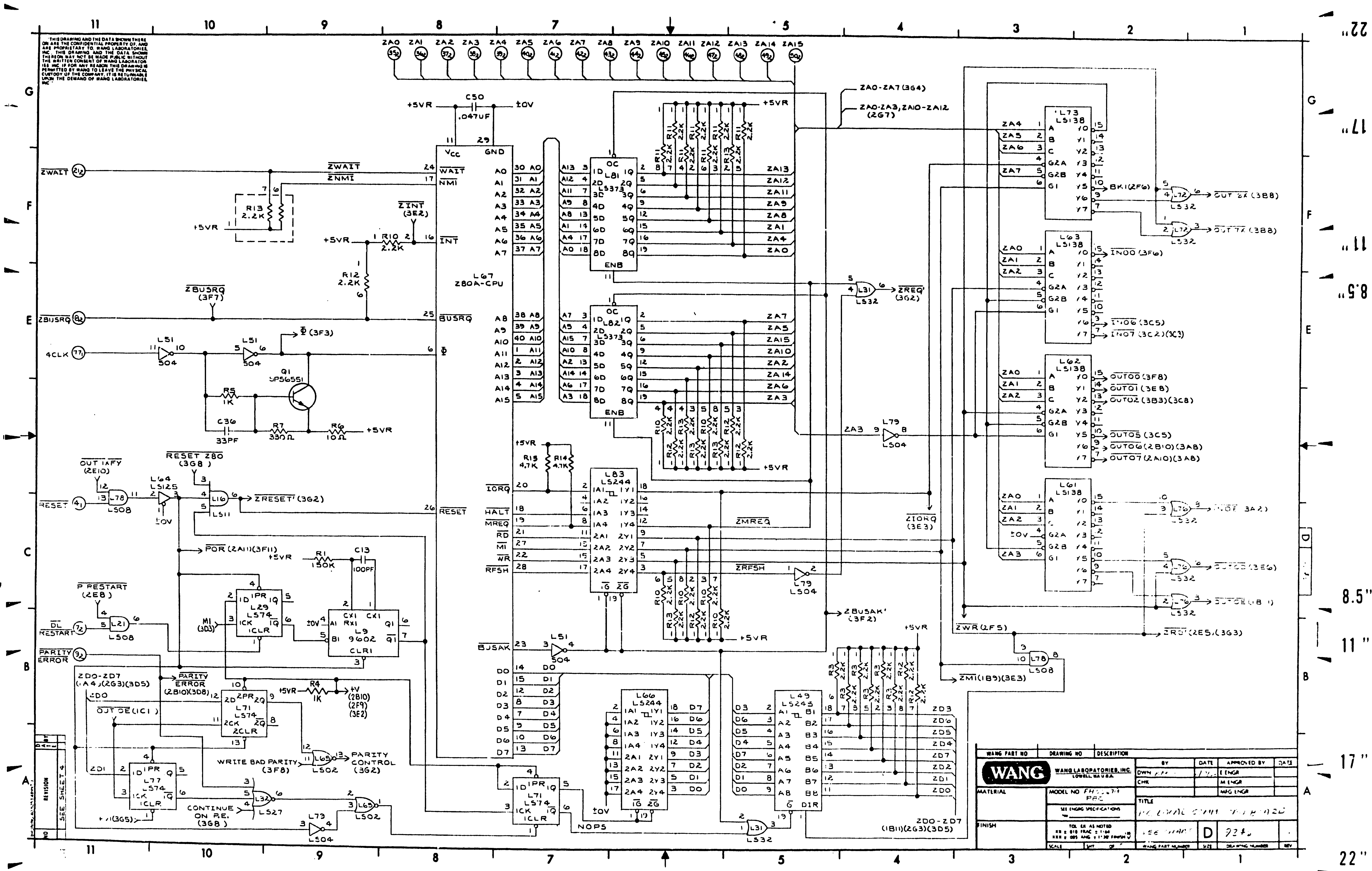
DWN KTH CHK ENG DIR

SIZE D DRAWING NUMBER 9245 REV E

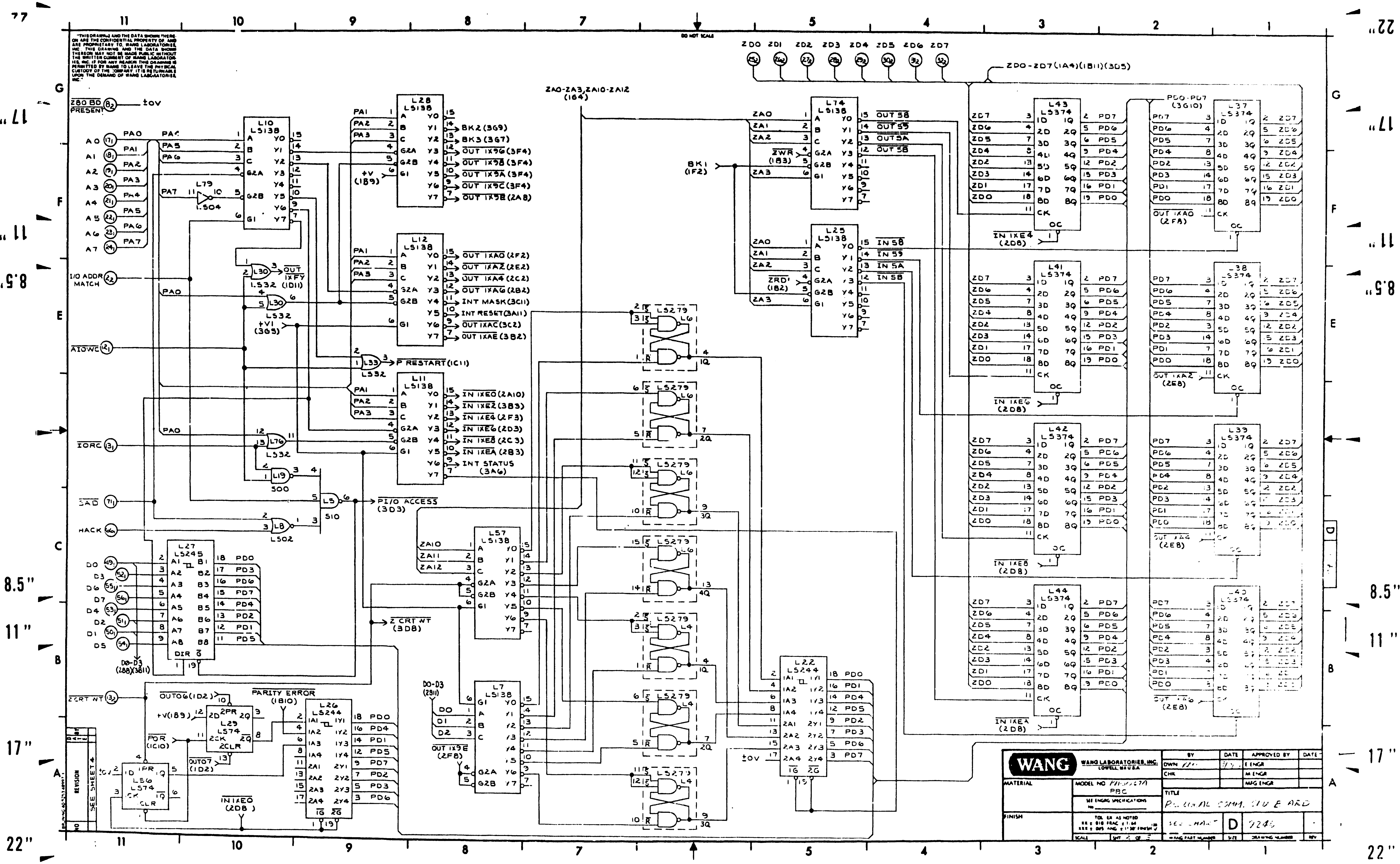
SCALE — SHEET 8 OF 8



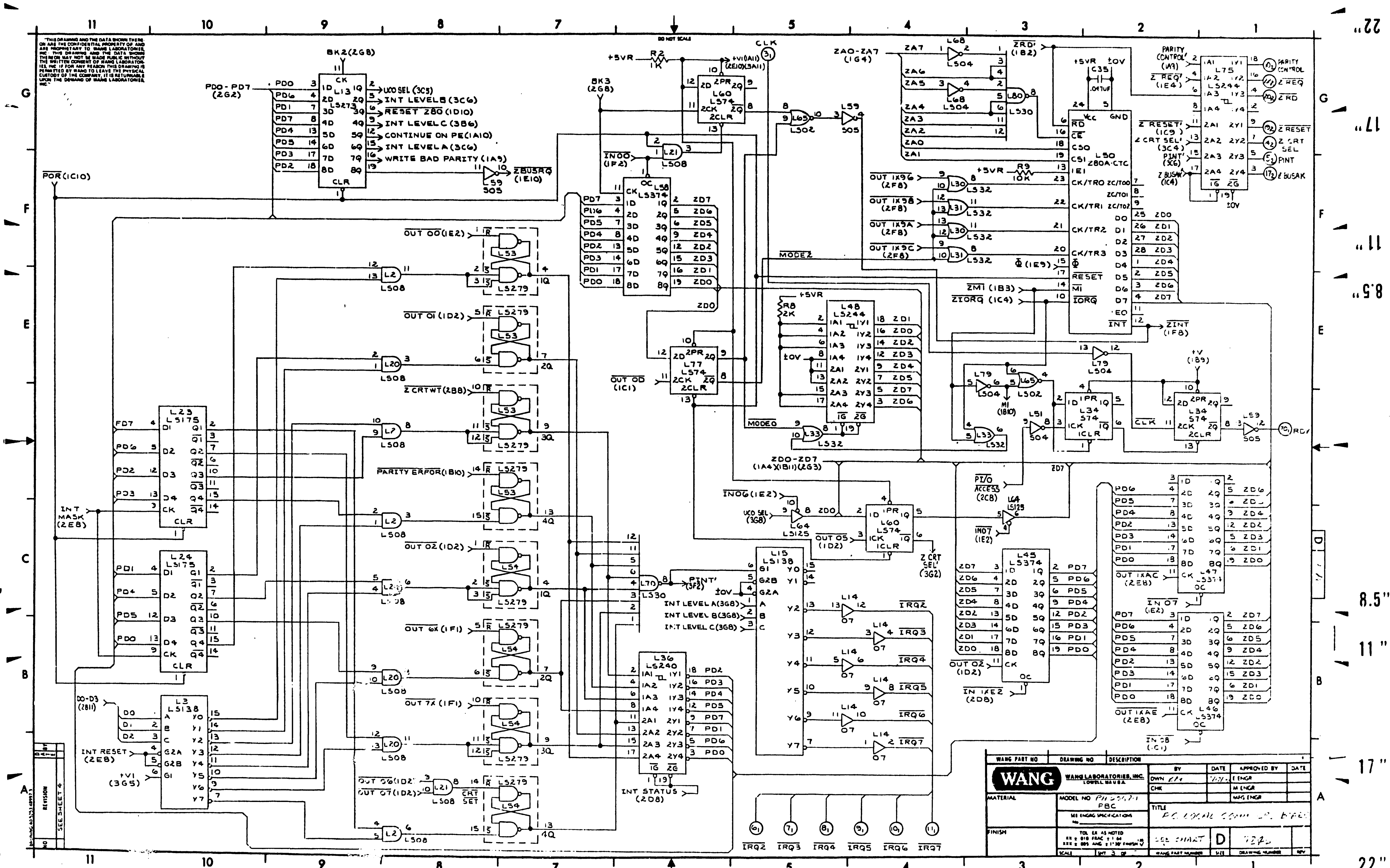
.000
2.72 REF.
6.22
NOTE ORIENTATION
.000
SEE NOTE 6
.50 REF.
LABEL WANG P/N 615-2201
LABEL WANG P/N 615-2204
9245-R1M
WANG
L1-L9 SEE NOTE 3.
RF SHIELD(458-3086)
SCREW.NO.8-32 X 3/8 (2 PLCS.)(650-4120)
NUT.HEX.NO.8-32 (2 PLCS.)(652-0029)
COMPONENT SIDE
L20-L28 SEE NOTE 3.
BNC ASSY. NUT
ITL WASHER
CONN BNC
5.TORQUE SPEC TO 18 IN.LBS.ORIENT AND SPADE LUG TO 9.00 POSITION.
AVOID OVERLAP FROM ADJACENT SHIELD.
WANG
MATERIAL
MODEL NO.
PBC
10-213
FINISH
TITLE
ASSEMBLY DRAWING
C
9245
4
N



L67
Z80A-CPU
L81 LS373
L82 LS373
L83 LS244
L66 LS244
L49 LS245
L73 LS138
L63 LS138
L62 LS138
L61 LS138
L9 9602
L29 LS74
L71 LS74
L77 LS74
Q1 SPS6551
WANG
WANG LABORATORIES, INC.
LOWELL, MA U.S.A.



WANG
WANG LABORATORIES, INC.
LOWELL, MASS.
DO NOT SCALE
L5138
L5374
L5279
L5245
L5244
L574
P RESTART (1C11)
PI/O ACCESS (3D3)
Z CRT WT (3D8)
PARITY ERROR (1B10)
I/O ADDR MATCH


WANG
WANG LABORATORIES, INC.
LOWELL, MASS.
MATERIAL
FINISH
MODEL NO
PBC
TITLE
REVISION
SEE SHEET 4

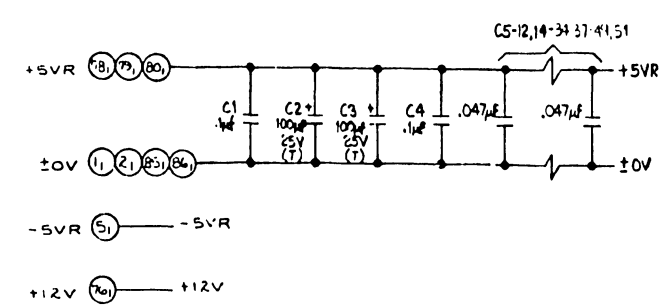
"THIS DRAWING AND THE DATA SHOWN THEREON ARE THE CONFIDENTIAL PROPERTY OF AND ARE PROPRIETARY TO WANG LABORATORIES, INC. THIS DRAWING AND THE DATA SHOWN THEREON MAY NOT BE MADE PUBLIC WITHOUT THE WRITTEN CONSENT OF WANG LABORATORIES, INC. IF FOR ANY REASON THIS DRAWING IS PERMITTED BY WANG TO LEAVE THE PHYSICAL CUSTODY OF THE COMPANY, IT IS RETURNABLE UPON THE DEMAND OF WANG LABORATORIES, INC."

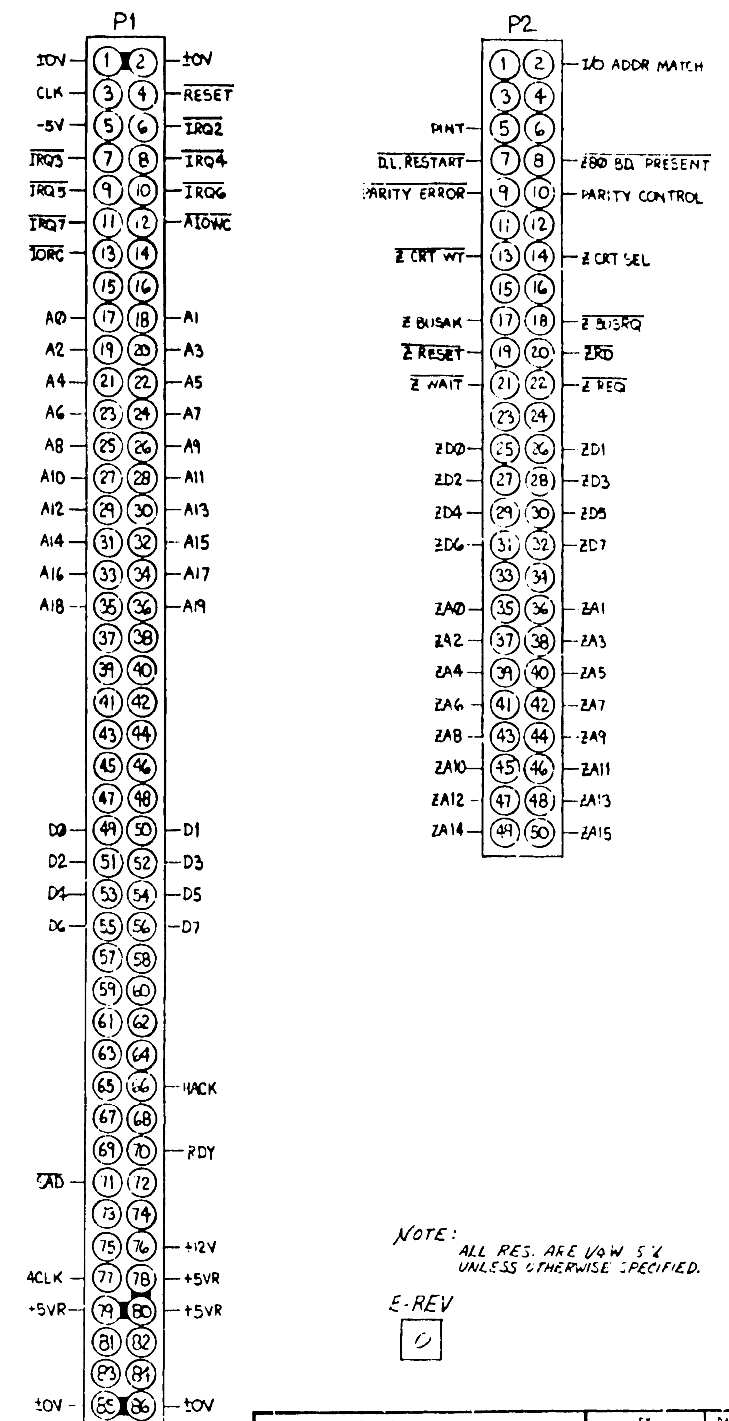
DO NOT SCALE

MNEMONICS	COORD
A0-A7	2F11
AIOWC	2E11
CLK	3G5
D0-D7	2C11
D.L. RESTART	1B11
DT/R	2B11
HACK	2C11
I/O ADDR MATCH	2E11
IORC	2C11
IRQ2-IRQ7	3A5
PARITY CONTROL	3F1
PARITY ERROR	B11
PINT	3G1
RDY	3D1
RESET	1C11
SAD	2C11
ZA0-ZA15	1G8
Z BUSAK	3G1
Z BUSRQ	1E11
Z CRT SEL	3G1
Z CRT WT	2B11
ZD0-ZD7	2G5
ZRD	3G1
Z RESET	3G1
Z REQ	3G1
Z WAIT	1F11
Z80 BD PRESENT	2G11
4CLK	1E11

I.C. TYPE	LOCATION	SPARES
74S00	L19	3
74LS02	L8	3
74LS04	L68	4
74S04	L51	2
74S05	L59	3
74LS08	L21	1
	L78	2
74S10	L5	2
74S11	L16	2
74LS27	L32	2
74LS32	L33	1
	L72	2
74LS74	L56	1
9602	L9	1
74LS125	L64	1
SPARE	L1,17,18,35, 52,55,69	

210 = 209 + 377 OR 378			
210	209	L50	L67
9246-A	9246	377-0371	377-0368





NOTE: ALL RES. ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

E-REV 0

REVISION	
0	ORIGINATED PER DWR #E2126 APP'D
1	REVISED PER ECO #30058 APP'D
2	REVISED PER ECO # APP'D
3	REVISED PER ECO #35585 APP'D
4	REVISED PER ECO # APP'D

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

MATERIAL | MODEL NO. | PBC | SEE ENGRG SPECIFICATIONS | FINISH | TITLE | D | DRAWING NUMBER

11 10 9 8 7 6 5 4 3 2 1

DO NOT SCALE

ITEM NO.	WANG PART NO.	DESCRIPTION	REFERENCE DESIGNATION(S)	QTY.
53				
52	376-0238	IC 74LS244	L22,26,48,66,75,83	6
51	376-0286	IC 74LS374	L37-47,58	12
50	376-0295	IC 74LS245	L27,49	2
49				
48	376-0249	IC 74LS30	L70,80	2
47	376-0245	IC 74LS27	L32	1
46	376-0238	IC 74S10	L5	1
45				
44	376-0229	IC 74S00	L19	1
43	376-0225	IC 74LS11	L16	1
42	376-0211	IC 74LS32	L30,31,33,72,76	5
41				
40	376-0209	IC 74LS02	L8,65	2
39	376-0202	IC 74S74	L34	1
38	376-0177	IC 74S04	L51	1
37				
36	376-0130	IC 74LS04	L69,79	2
35	376-0160	IC 74LS175	L23,24	2
34	376-0155	IC 74LS74	L13,56,60,71,77	5
33				
32	376-0153	IC 74LS08	L2,20,21,78	4
31	376-0104	IC 7602	L9	1
30	376-0056	IC 7407	L14	1
29				
28				
27	375-1050	TSTR SPS6551	[illegible]1	1
26				
25				
24	333-0906	RES. 2.2K SIP	R3,10-13	5
23				
22				
21				
20				
19	330-5616	RES. 150K 1/4W 5%	R1	1
18				
17	330-4011	RES 13K 1/4W 5%	R9	1
16	330-3048	RES. 4.7K 1/4W 5%	R14 15	2
15	330-3021	RES. 2K 1/4W 5%	R8	1
14				
13	330-3011	RES. 1K 1/4W 5%	R2,4,5	3
12	330-2034	RES. 330Ω 1/4W 5%	R7	1
11	330-1011	RES. 10Ω 1/4W 5%	R6	1
10				
9				
8				
7	300-3033	CAP 100UF 25V(T)	C2,3	2
6	300-1966	CAP .047UF 50V	C5-12,14-35 37-51	45
5				
4	300-1833	CAP .1UF 50V	C1,4	2
3	300-1100	CAP 100PF 500V	C13	1
2	300-1033	CAP 33PF 500V	C36	1
1				

ITEM NO.	WANG PART NO.	DESCRIPTION	REFERENCE DESIGNATION(S)	QTY
84	615-2213	LABEL R.F. SHIELD		1
83	652-0027	HEX NUT 6-32		2
82				
81				
80				
79				
78				
77	650-4120	SCREW #6-32x5/8"		2
76				
75				
74	451-5140	SHIELD (RF)		1
73				
72				
71	465 1.50	EXTRACTOR		1
70				
69				
68	SEE CHART	IC 2800-TC	L50	1
67	SEE CHART	IC 280A CPU	L57	1
66				
65				
64	376-7015	SKT 28PIN	L50	1
63	376-7011	SKT 40PIN	L57	1
62	376-0555	IC 74S15	L59	1
61				
60	376-0436	IC 74LS125	L64	1
59	376-0316	IC 74LS279	L4,6,53 54	4
58	376-0310	IC 74LS373	L81,82	2
57				
56	376-0302	IC 74LS173	L13	1
55	376-0277	IC 74LS240	L36	1
54	376-0214	IC 74LS138	L1,7,10-12,15,25,35,57,61,63,73,74	14

ITEM NO	WANG PART NO	DESCRIPTION	REFERENCE DESIGNATION(S)	QTY

BY	DATE	APPROVED BY	DATE
DWN		E ENGR	
CHK		M ENGR	
		MFG ENGR	

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

MATERIAL

FINISH

MODEL NO

UNLESS OTHERWISE SPECIFIED TOLERANCES AS NOTED

TITLE

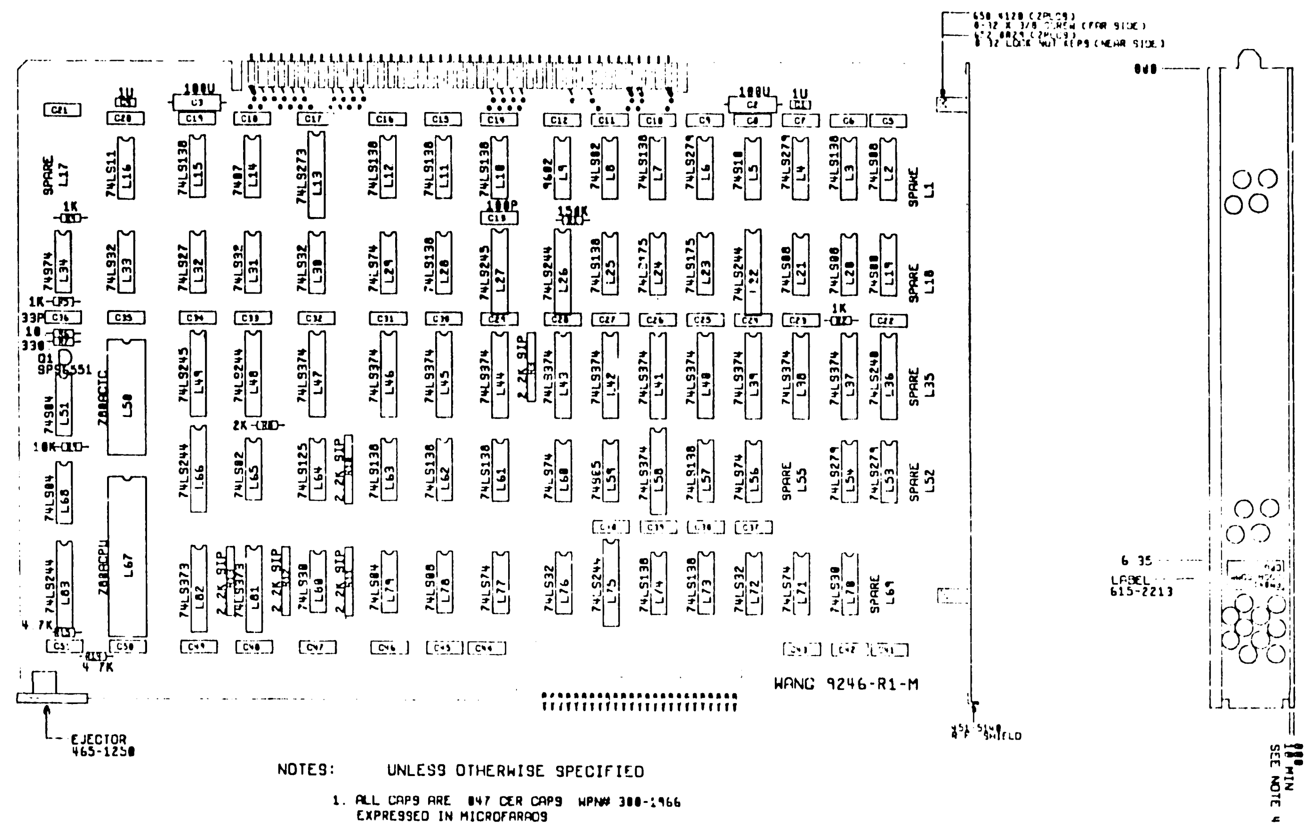
WANG PART NUMBER | SIZE D | DRAWING NUMBER | REV

REVISION

SHT. 4

11 10 9 8 7 6 5 4 3 2 1

DO NOT SCALE



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL CAPS ARE .047 CER CAPS WPN# 300-1966 EXPRESSED IN MICROFARADS
2. ALL RESISTORS ARE 1/4W 5 PERCENT EXPRESSED N OHMS
3. L67 LOAD 40 PIN SOCKET WPN# 376-9011
   L50 LOAD 28 PIN SOCKET WPN# 376-9015
4. 10 MIN. DESIGNATED TO PREVENT OVERLAP FROM ADJACENT SHIELD

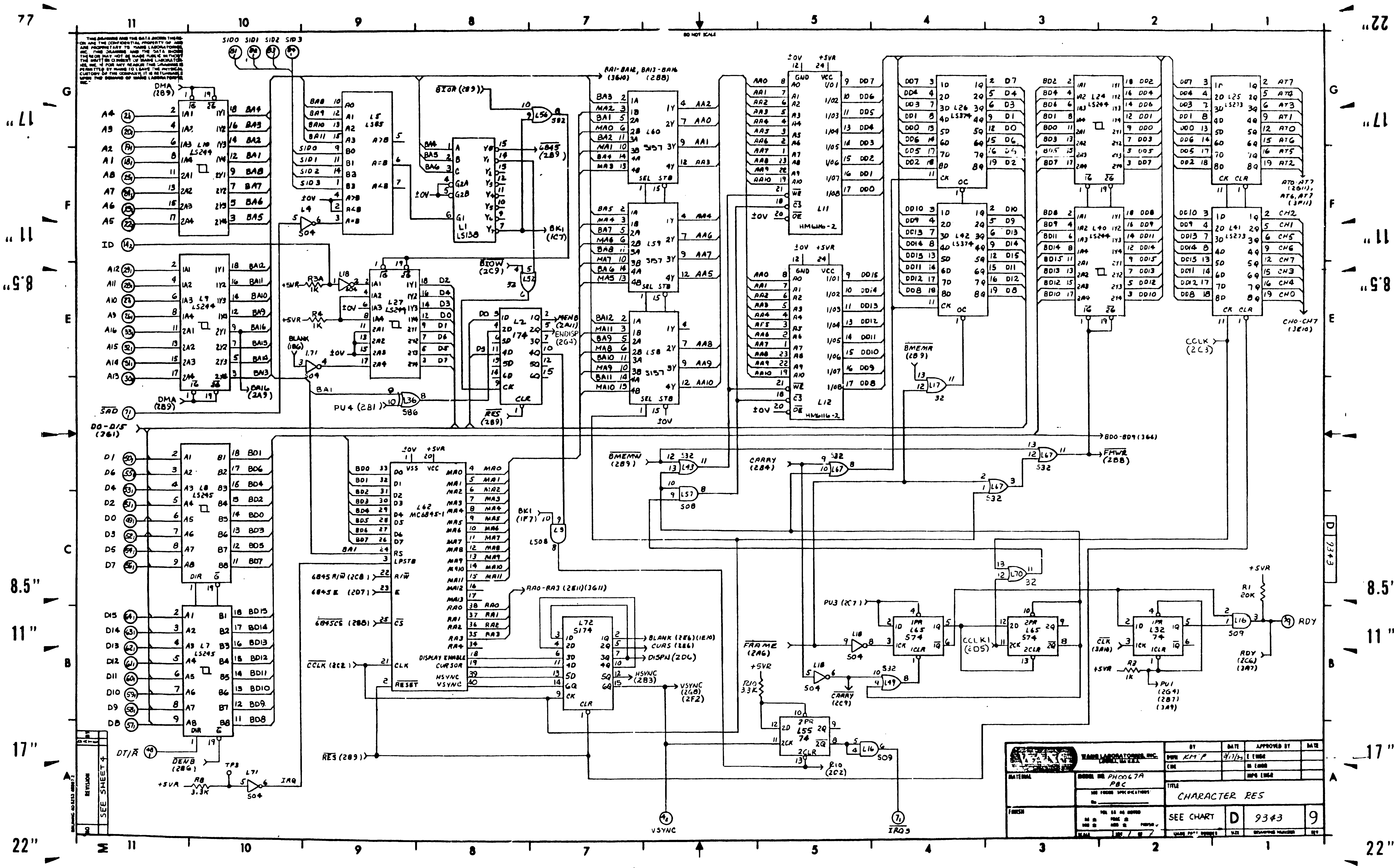
		JAR	JAR	JAR
	4/18/83	12/11/83	5/6/84	5/9/84
	DWR E2124	ECO 30858 ECO 32852	ECO 31585	ECO 31789
	R0/3	R1/1	R1/2	R1/3

WANG LABORATORIES INC

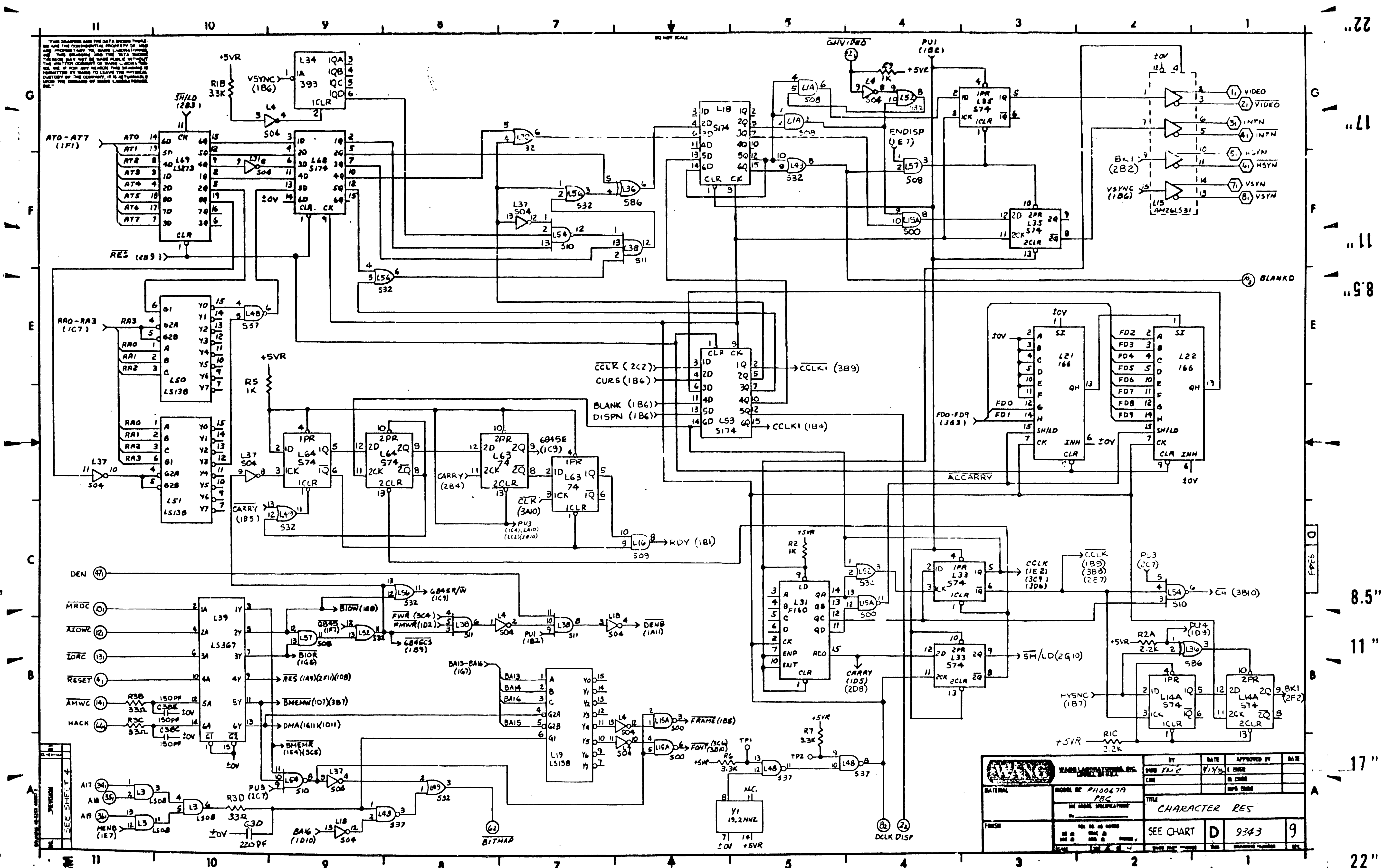
ASSEMBLY DRAWING

210-9246 R1

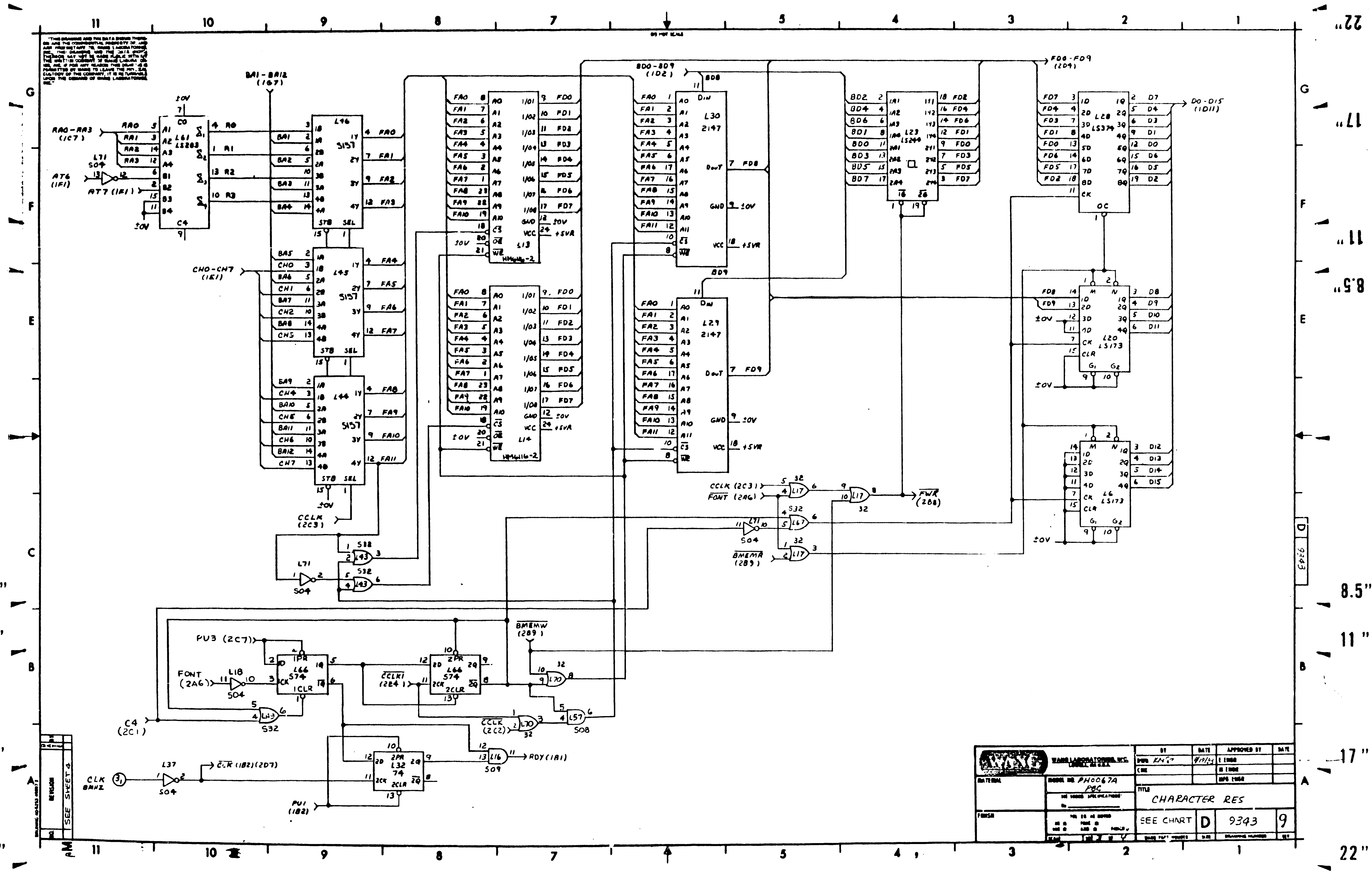
9246



CHARACTER RES
SEE CHART
D
9343
9
PHOO67A
PBC
L62 MC6845-1
L11 HM6116-2
L12 HM6116-2
VSYNC
IRQ3
RDY



CHARACTER RES
SEE CHART
D
9343
9
WANG LABORATORIES, INC. LOWELL, MA U.S.A.
P110067A
PBC
VIDEO
INTN
HSYN
VSYN
BLANKD
CCLK1 (3B9)
CCLK1 (1B4)
RDY (1B1)
DENB (1A11)
BITMAP
FRAME (1B6)
DCLK
DISP
SH/LD (2G10)
Y1 19.2MHZ

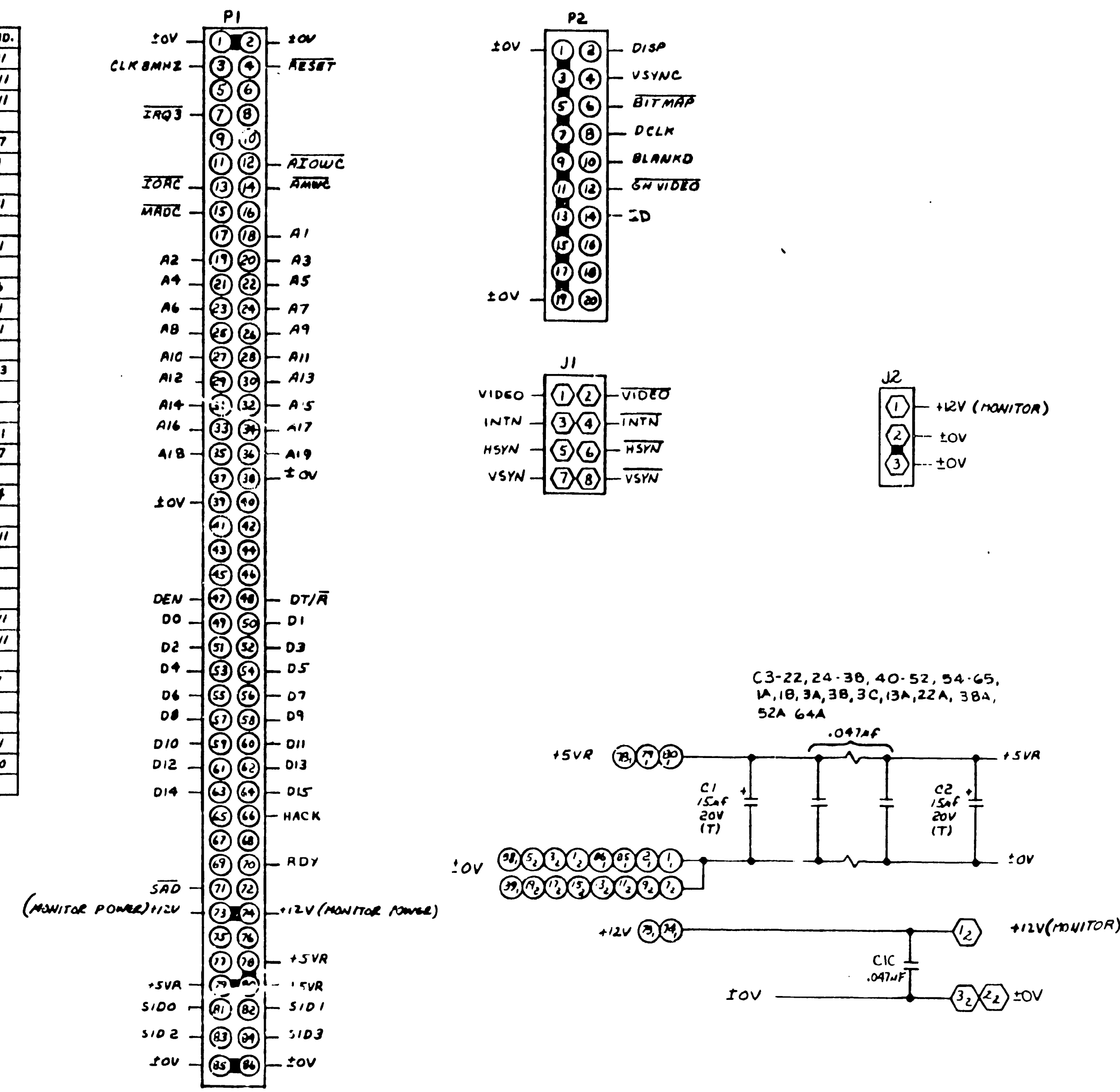


RA0 - RA3 (1C7)
AT6 (1F1)
AT7 (1F1)
L61 LS283
BA1 - BA12 (1G7)
CH0 - CH7 (1E1)
L46 S157
L45 S157
L44 S157
L13 HM6116-2
L14 HM6116-2
BD0 - BD9 (1D2)
L30 2147
L29 2147
L23 LS244
FD0 - FD9 (2D9)
L28 LS374
D0 - D15 (1D11)
L20 LS173
L6 LS173
CCLK (2C3)
FONT (2A6)
BMEMR (2B9)
FWR (2B8)
PU3 (2C7)
FONT (2A6)
CCLK1 (2E4)
BMEMW (2B9)
C4 (2C1)
CCLK (2C2)
RDY (1B1)
CLK 8MHZ
CLK (1B2)(2D7)
PU1 (1B2)
SEE SHEET 4
WANG LABORATORIES, INC. LOWELL, MA U.S.A.
PH0067A PBC
CHARACTER RES
SEE CHART
D
9343
9

MNEMONICS	COORD.
A1-A16	1G11
$\overline{AIOWC}$	2B11
$\overline{AMWC}$	2B11
$\overline{BITMAP}$	2A7
BLANKD	2B1
CLK 8MHZ	3A11
D0-D15	1D11
DCLK	2A6
DEN	2C11
DT/$\overline{R}$	1A11
$\overline{GHVIDEO}$	2G3
HACK	2B11
HSYNC	1A7
ID	1F11
$\overline{IRQ3}$	1A4
$\overline{IORC}$	2B11
M PAGE	2A11
$\overline{MRDC}$	2B11
$\overline{RESET}$	2B11
RDY	1B1
$\overline{SAD}$	1D11
SID0 - SID3	1G10

TYPE	LOCATION	SPARES
74S04	L37	1
74S08	L1A	3
74S32	L56	1
7474	L55	1
74S86	L36	1
74393	L34	1

210=209+377 OR 378			
210	209	L62	
9343A	9343	377-0473	



NOTE:
1. ALL RES. 1/4W 5% UNLESS OTHERWISE SPECIFIED.

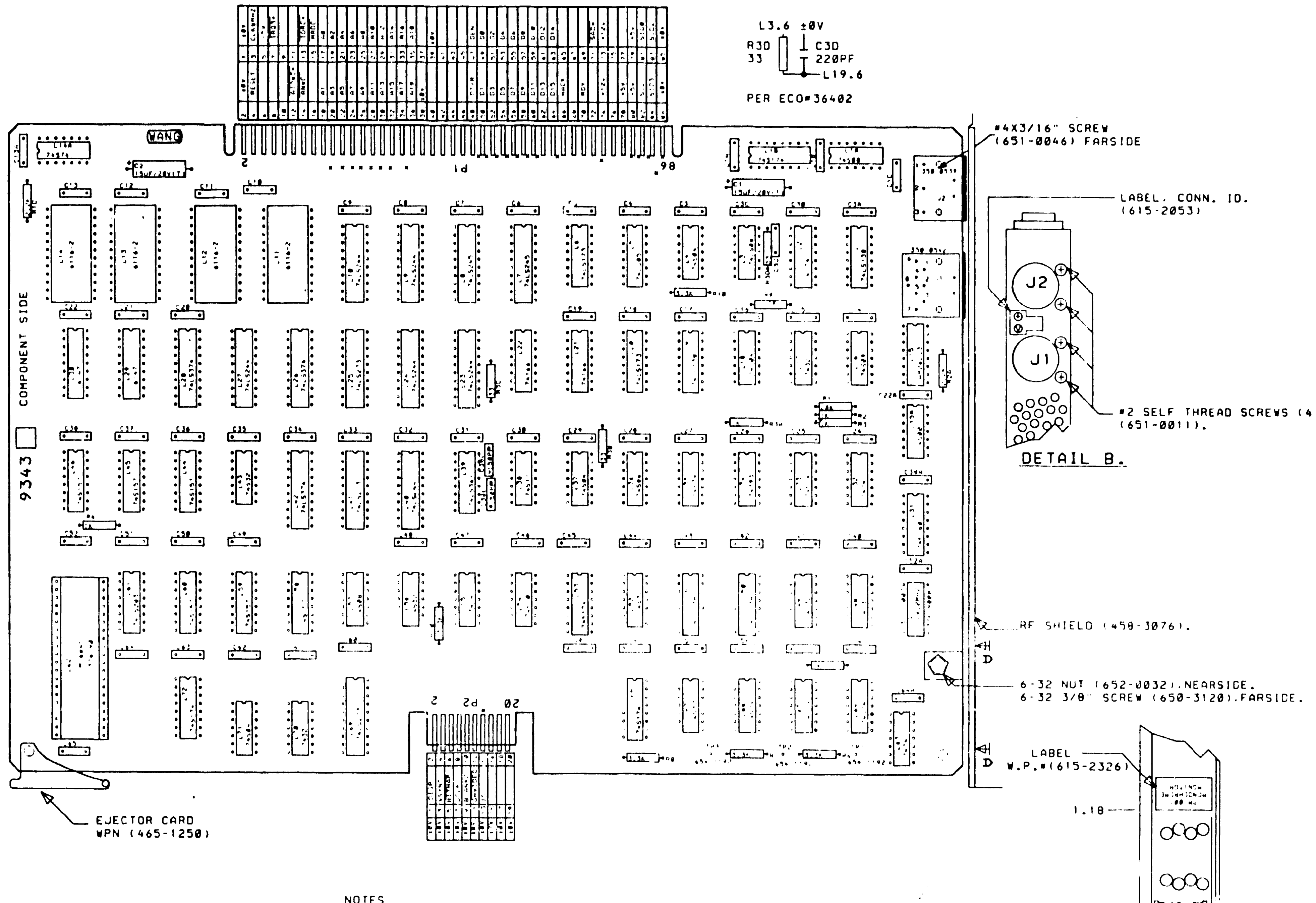
E-REV 2

WANG LABORATORIES, INC. LOWELL, MA U.S.A.

MODEL NO. PH0067A PBC

TITLE: CHARACTER RES

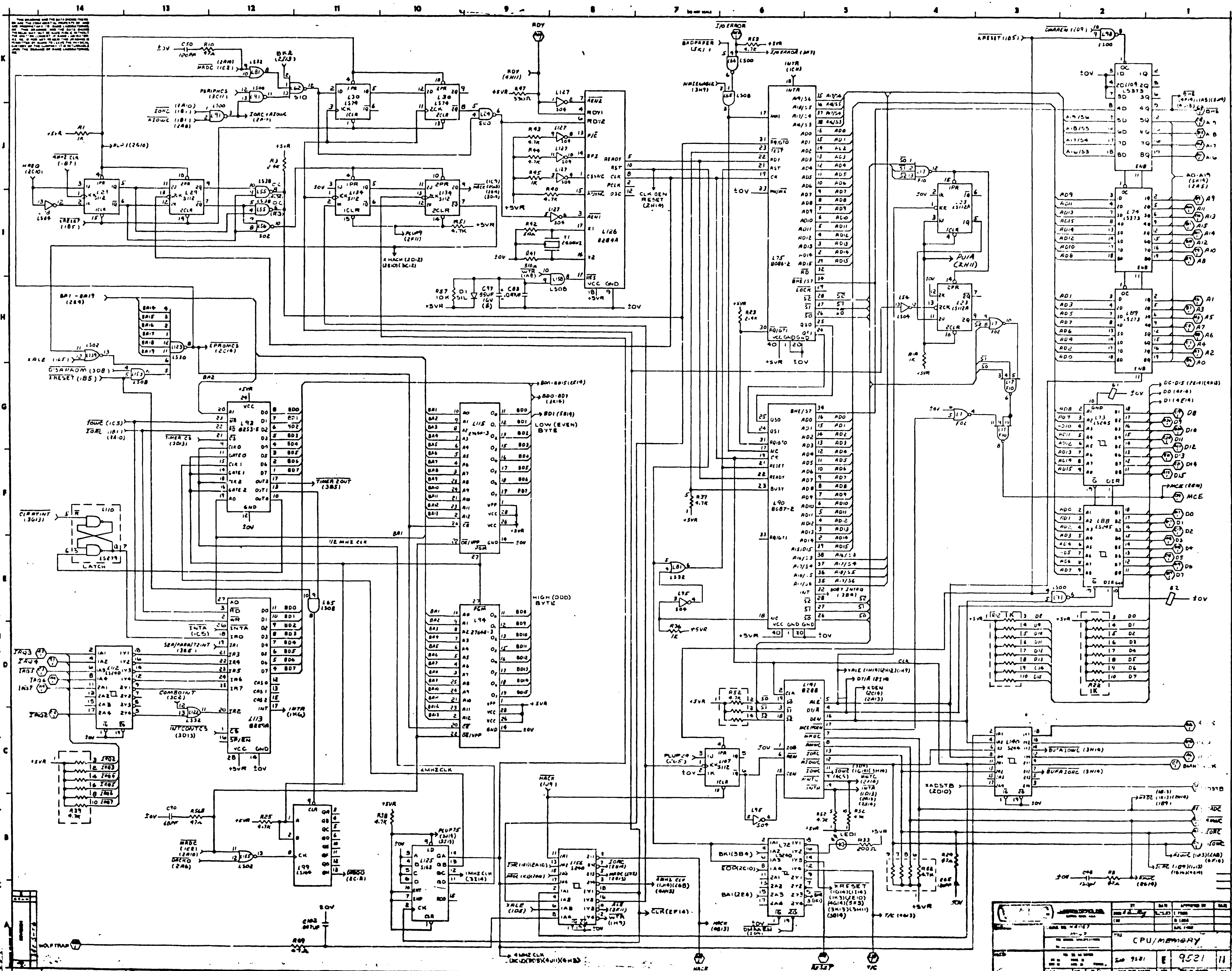
SEE CHART | D | 9343 | 9

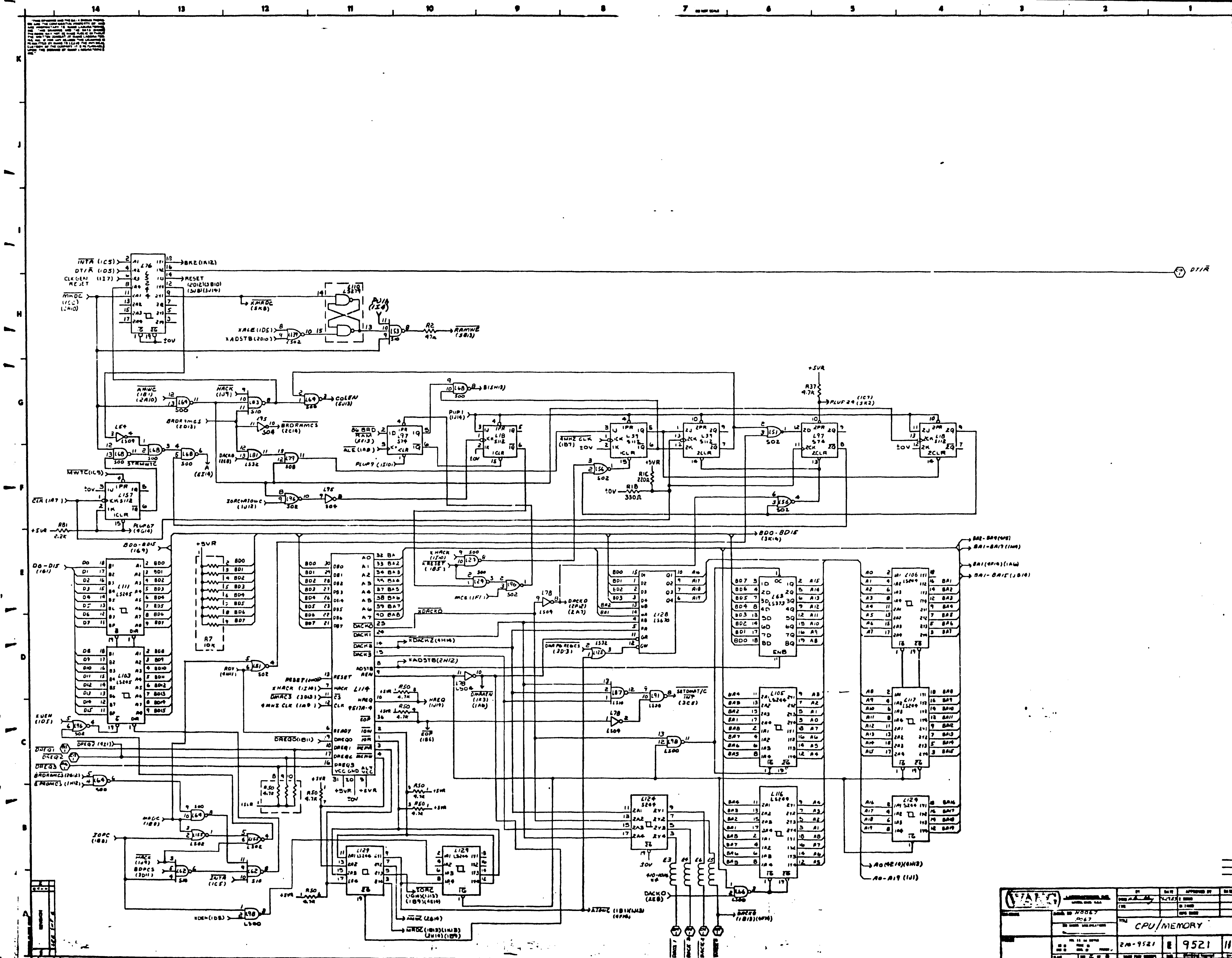


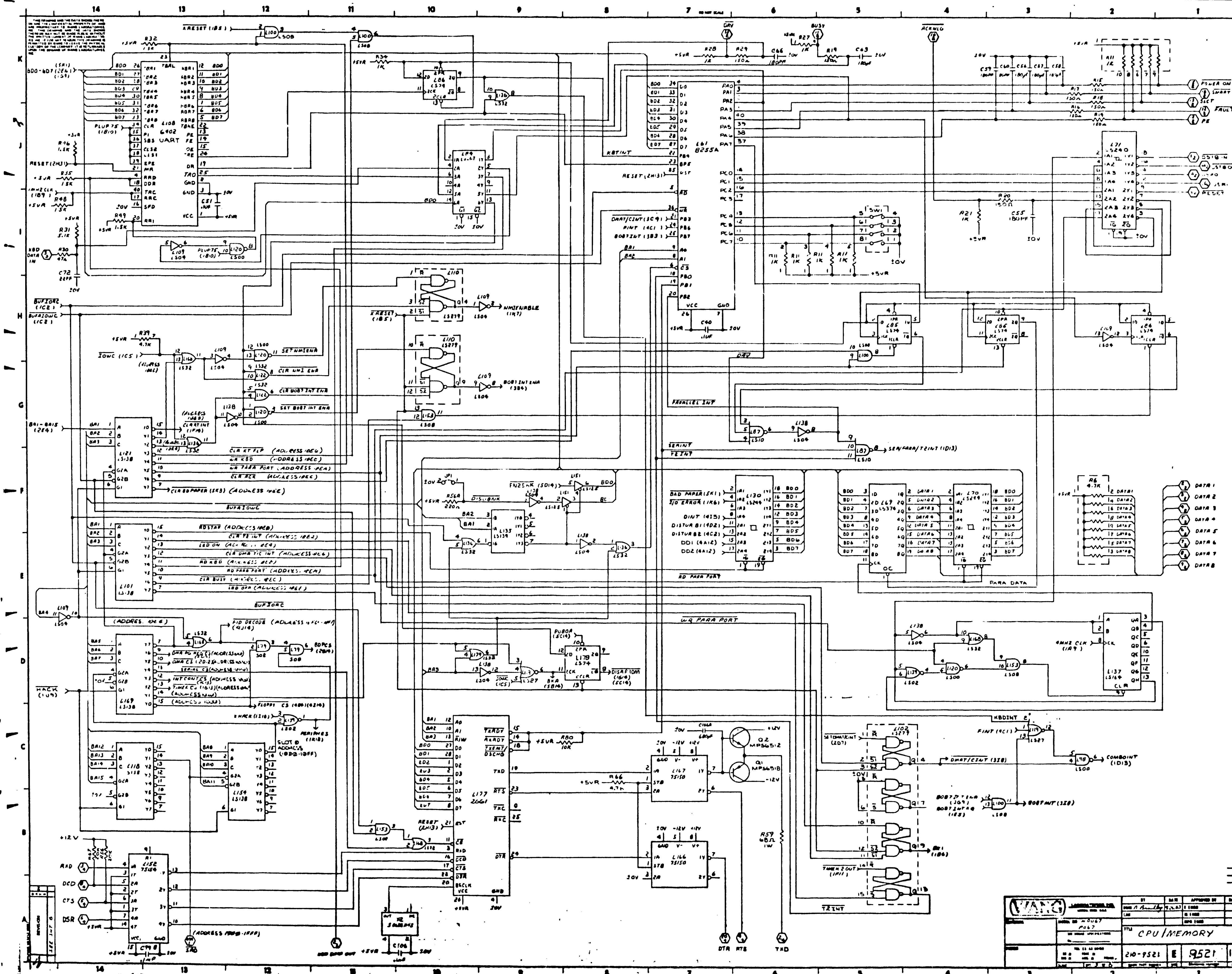
PARTIAL VIEW A-A

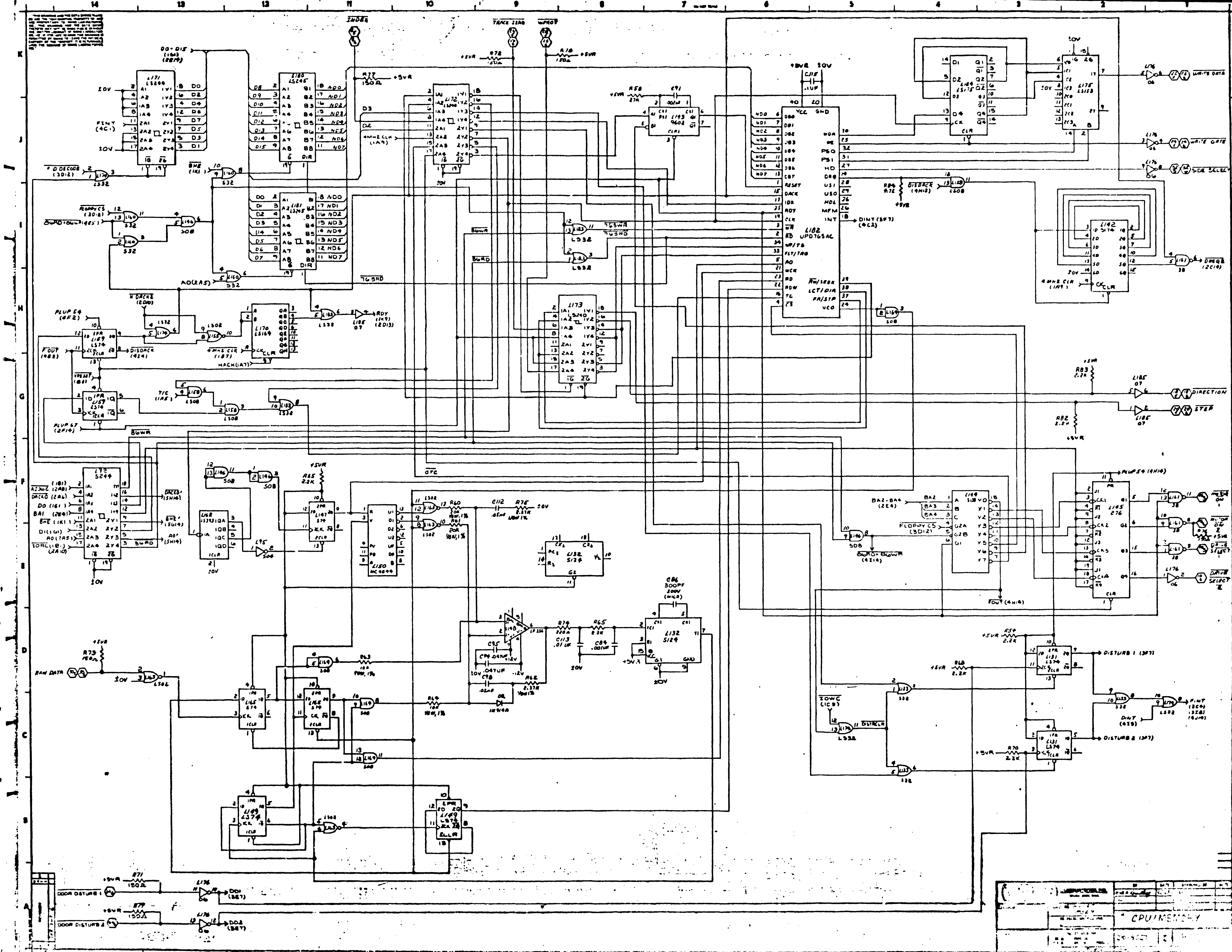
NOTES
1. UNLESS OTHERWISE SPECIFIED
   ALL CAPACITORS ARE .047UF. P/N 300 1966.
   ALL RESISTORS ARE 1/4W 5%. EXPRESSED IN OHMS.
2. .10 MIN. HAS BEEN DESIGNATED TO AVOID OVERLAP FROM ADJACENT SHIELD.

WANG		BY	DATE	APPROVED BY	DATE
		DWN		E ENGR	
		CHK		M ENGR	
MATERIAL	MODEL NO. PBC	E C CONTROL		MFG ENGR	
	10-213	TITLE CHARACTER RESOLUTION M/L ASSEMBLY DRAWING			
FINISH	SCALE 1/1 SH 1 OF 1	210 9343 R2	C	9343	10

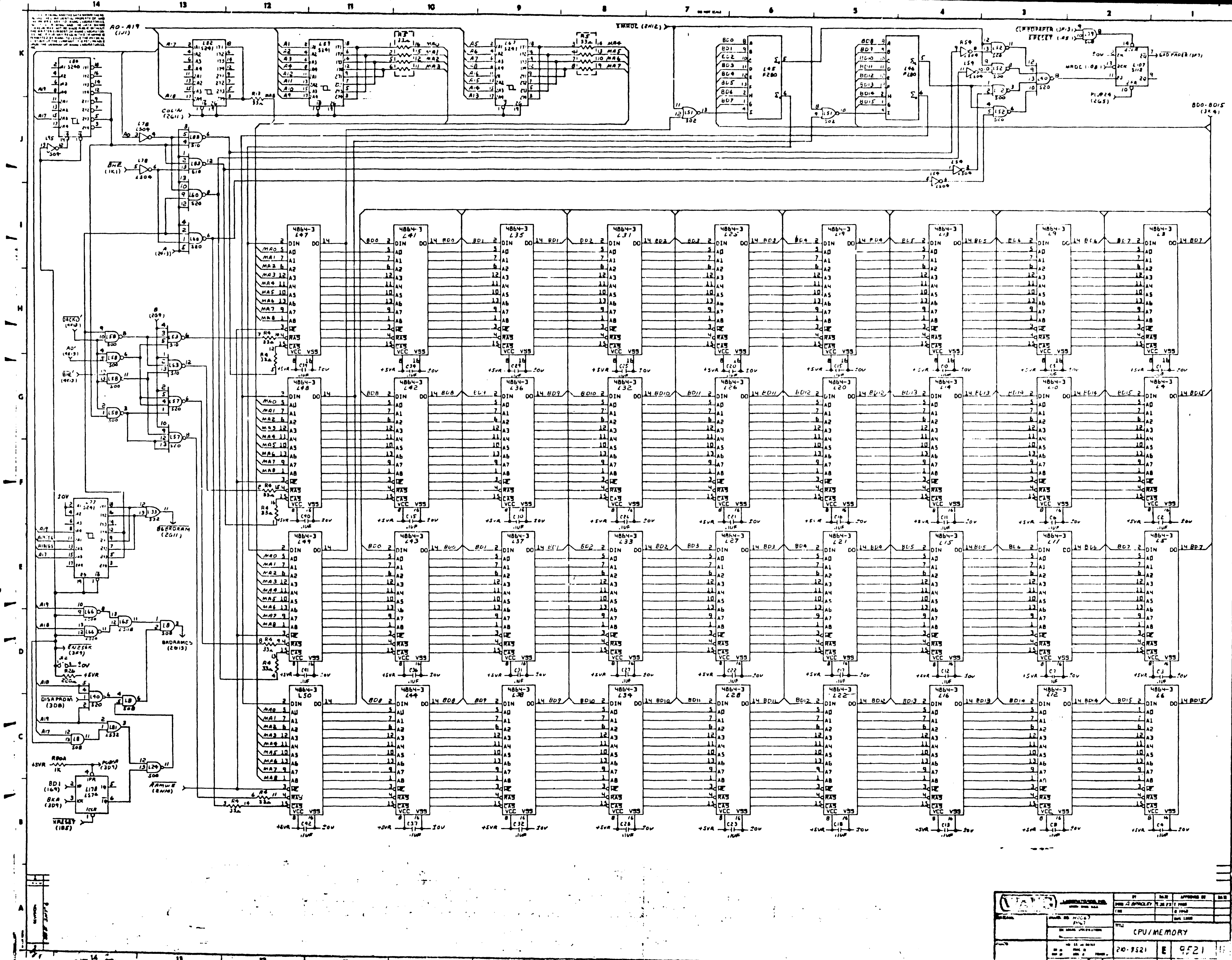

CPU/MEMORY
9521
11


CPU/MEMORY
210-9521
E
9521
11


CPU / MEMORY
210-9521
E
9521
6402 UART
8255A
2661
POWER ON
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
DATA 8
RXD
DCD
CTS
DSR
DTR
RTS
TXD
PARA DATA



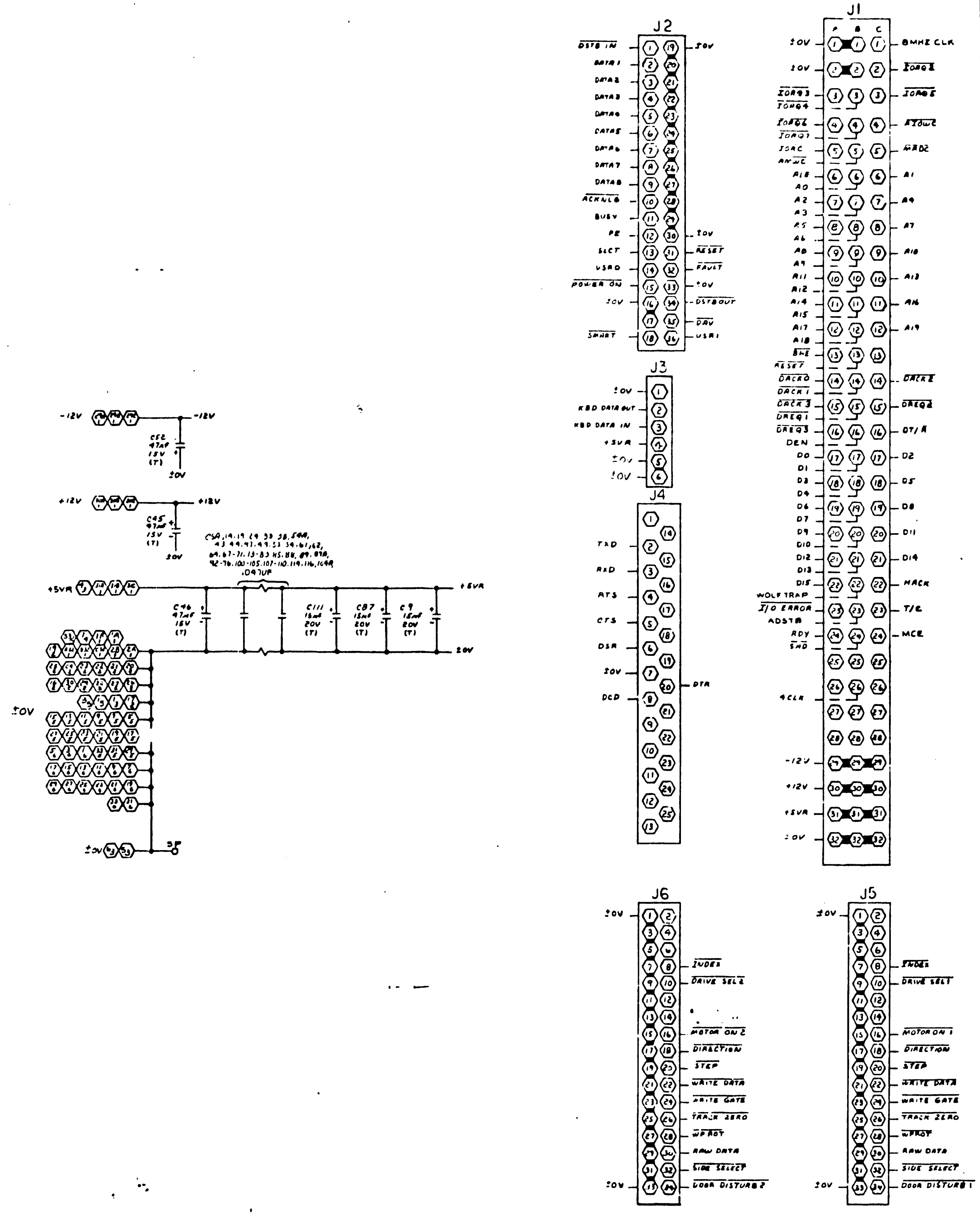
INDEX
TRACK ZERO
WPROT
L182
UPD765AC
WRITE DATA
WRITE GATE
SIDE SELECT
DIRECTION
STEP
DRIVE SELECT
DISTURB 1
DISTURB 2
RAW DATA
DOOR DISTURB 1
DOOR DISTURB 2
CPU/MEMORY



CPU/MEMORY
210-9521
E
9521
4864-3
BDRAMCS
RAMWE
DISAPROM
EN256K

I.C TYPE	LOCATION	SPARES
74S00	L24	1
74S02	L56	1
	L76	1
74S04	L138	5
	L127	1
74F02	L7	2
74LS04	L138	1
7407	L185	3
74LS08	L65	1
74S08	L8	1
74LS27	L119	1
74LS38	L55	2
74LS32	L179	3
7474	L147	1
74S112	L157	1
74LS125	L151	2
74LS279	L102	1
9602	L143	1

MNEMONICS	COORD.
A0 - A19	1H1
ACKNLG	3K4
AIOWC	1B1
ALE	1C1
AMWC	1B1
ADSTB	1C1
BHE	1J1
BUSY	3K5
CTS	3A14
D0 - D15	1E1
DACK0 - DACK3	2A7
DATA1 - DATA8	3F1
DAV	3H7
DCD	3A14
DEN	1C1
DIRECTION	4G1
DOOR DISTURB 1	4A14
DOOR DISTURB 2	4A14
DRIVE SELECT 1	4E1
DRIVE SELECT 2	4E1
DREQ1 - DREQ3	2C14
DSR	3A14
DSTB IN	3J1
DSTB OUT	3J1
DTR	3A7
DT/R	2I1
FAULT	3J1
HACK	[illegible]7
INDEX	4K11
I/O ERROR	1K6
IORC	1B1
IRQ2 - IRQ7	1D14
KBD DATA IN	3I14
KBD DATA OUT	3A11
MCE	1F1
MOTOR ON 1	4F1
MOTOR ON 2	4F1
MRDC	1B1
PE	3J1
POWER ON	3K1
RAW DATA	4D14
RESET	3J1
	1A5
RDY	1K9
RTS	3A6
RXD	3B14
SRD	3A13
SIDE SELECT	4J1
SLCT	3K1
SMART	3K1
STEP	4G1
T/C	1A5
TRACK ZERO	4K9
TXD	3A6
USR0	3J1
USR1	3J1
WOLFTRAP	1A14
WPROT	4K9
WRITE DATA	4K1
WRITE GATE	4J1
4 CLK	1C1
8MHZ CLK	1C1



E-REV
2

NOTE: ALL RES 1/4W 5% UNLESS OTHERWISE SPECIFIED.

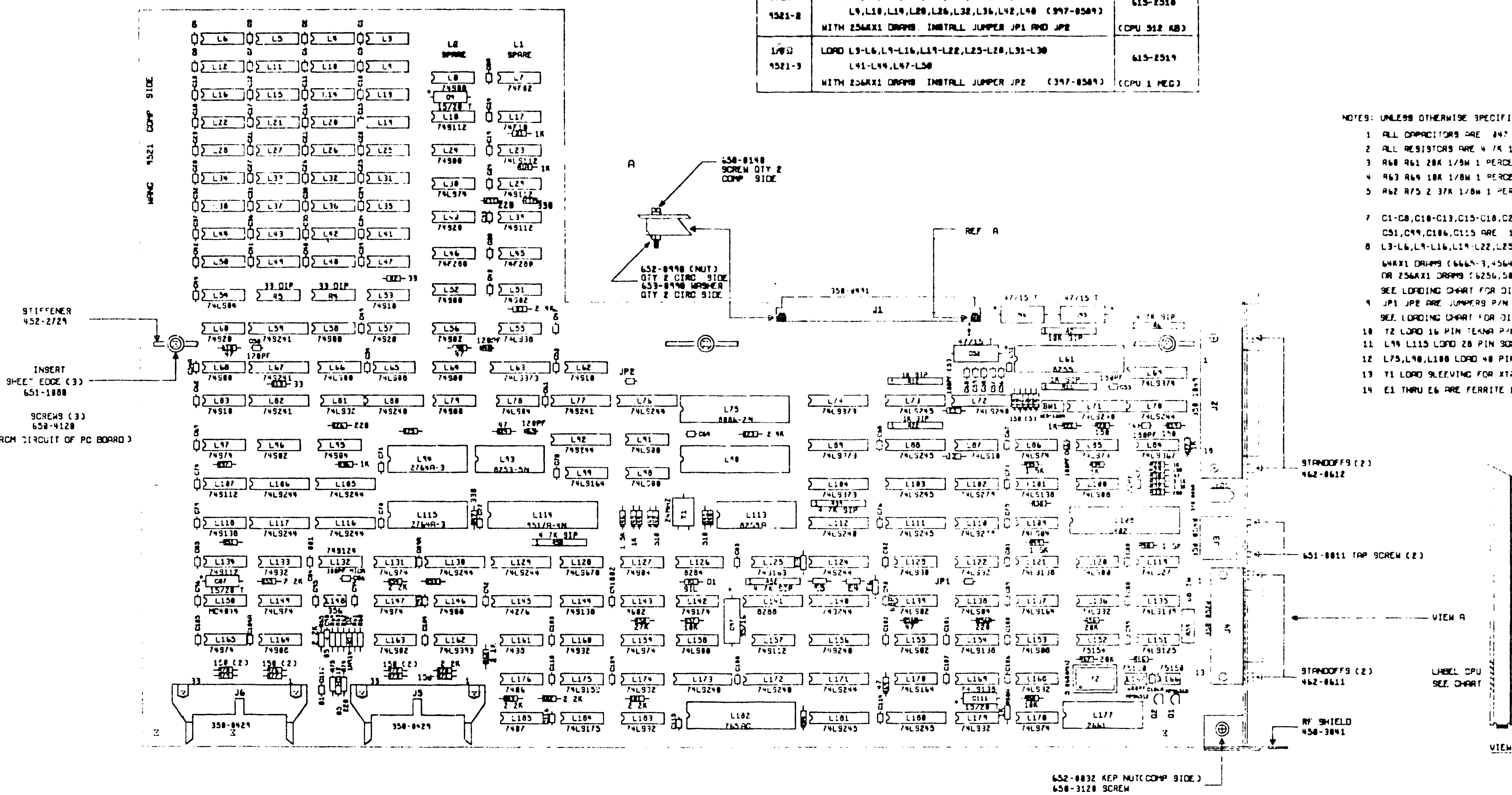
TITLE C.P.U./MEMORY

210-9521 E 9521 11

DO NOT SCALE

LOADING CHART

128K 9521	LOAD L3,L9,L13,L19,L25,L31,L35,L41,L47 L4,L10,L14,L20,L26,L32,L36,L42,L48 WITH 64KX1 DRAMS INSTALL JUMPER JP1 (397-0415)	615-2497 (CPU 128 KB)
256K 9521-1	LOAD L3-L6,L9-L16,L19-L22,L25-L28,L31-L38 L41-L44,L47-L50 WITH 64KX1 DRAMS NO JUMPERS INSTALLED. (397-0415)	615-2498 (CPU 256 KB)
512K 9521-2	LOAD L3,L9,L13,L19,L25,L31,L35,L41,L47 L4,L10,L14,L20,L26,L32,L36,L42,L48 (397-0509) WITH 256KX1 DRAMS. INSTALL JUMPER JP1 AND JP2	615-2518 (CPU 512 KB)
1MEG 9521-3	LOAD L3-L6,L9-L16,L19-L22,L25-L28,L31-L38 L41-L44,L47-L50 WITH 256KX1 DRAMS INSTALL JUMPER JP2 (397-0509)	615-2519 (CPU 1 MEG)



NOTES: UNLESS OTHERWISE SPECIFIED

1 ALL CAPACITORS ARE .047 EXPRESSED IN MICROFARADS
2 ALL RESISTORS ARE 4.7K 1/4W 5 PERCENT EXPRESSED IN OHMS
3 R60 R61 20K 1/8W 1 PERCENT
4 R63 R64 10K 1/8W 1 PERCENT
5 R62 R75 2.37K 1/8W 1 PERCENT

7 C1-C8,C10-C13,C15-C18,C20-C23,C25-C32,C34-C37,C39-C42 C51,C99,C106,C115 ARE 1UF 50V CER C P/N 300-1033
8 L3-L6,L9-L16,L19-L22,L25-L28,L31-L38,L41-L44,L47-L50 ARE 64KX1 DRAMS (6665-3,4564-3,2164-3,4164-3,-664-3,8264-3,3764-3) OR 256KX1 DRAMS (6256,50256)
SEE LOADING CHART FOR DIFFERENT LOADING VARIATIONS
9 JP1 JP2 ARE JUMPERS P/N 600-9027
SEE LOADING CHART FOR DIFFERENT LOADING VARIATIONS
10 Y2 LOAD 16 PIN TEKNA P/N 376-9008
11 L94 L115 LOAD 28 PIN SOCKET P/N 376-9015
12 L75,L90,L100 LOAD 40 PIN SOCKET P/N 376-9011
13 Y1 LOAD SLEEVING FOR XTAL 3/8 INCH P/N 605-0117
14 E1 THRU E6 ARE FERRITE BEADS, WP# 410-1016

WANG LABORATORIES, INC.	BY	DATE	APPROVED BY
	DWN P. MILEWSKI		E ENGR
	CHK		M ENGR
			MFG ENGR
MATERIAL	MODEL NO PBC	TITLE CPU/MEMORY ASSEMBLY DRAWING	
	10-213		
FINISH		210-9521-R3	D 9521 11

WANG LABORATORIES, INC

ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

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END