Western Automation Laboratories, Inc.
Acumen 301 / 301+ User's Manual

NOTE:

Western Automation suggests that you read this manual before attempting to install the Acumen 301 or 301+.

Acumen™ 301
User's Manual

CONTENTS

LIST OF FIGURES

LIST OF TABLES

To our valued Acumen customers,

Your Texas Instruments computer is a complex entity of controllers, memory, CPU, bus, interfaces, I/O devices, microcode, operating system, drivers, utilities, and application programs all attempting cooperation to present a working system. Due to the plethora of options supplied by a variety of hardware and software manufacturers there is always the potential for conflict between individual components. Therefore it is impossible to guarantee that the installation of any new piece of hardware (such as an Acumen board) or software (such as an operating system) will proceed completely trouble free.

However we at Western Automation believe in supporting our customers to our fullest extent and ability when conflicts occur between our products and the products of other manufacturers. If a problem should occur we will try to avoid pointing the fingers of blame at other manufacturers, but rather work with you the customer to resolve the problem regardless of source.

We believe that a good reputation, like a good name, is won by many acts . . . and lost by one.

Nathan Thompson
President

Acumen 301
User's Manual

1.0 Introduction

The Acumen design utilizes state-of-the-art high-speed low-power TTL integrated circuits on a CAD designed four layer glass-epoxy printed circuit board. Because the parts count has been reduced by availability of new devices, the board is relatively uncrowded allowing more leeway to design signal path lengths and geometry for better performance.

Maximum on-board primary memory capacity is 2 Mbytes with 256k RAM's installed (256k option), or 512 Kbytes with 64k RAM's (64k option). Smaller boards may be factory upgraded to larger sizes. On 1 Mbyte and 2 Mbyte boards, portions of high address space may be disabled to accomodate other peripherals which use this space. Additional memory on associated add-on memory expansion boards, up to the 2 Mbyte addressing limit, is fully supported. The cache memory has been expanded to 8 Kbytes of high-speed static RAM in one bank.

For installation instructions see section 2.

2.0 Installation

1. Unpack your Acumen board and inspect for damage. Note the Rev level of your board (silkscreened along the left edge as viewed with the word "**ACUMEN**" right side up) You will find with the board:

   - ☐ 2 spare memory devices (at locations 28R & 29R on Rev PA, PB, and PC; at 1J &32N on Rev PE and above).
   - ☐ This manual.

Save the original shipping container and packing as these will be required in the event you need to return the board.

2. Set the Base Address, TPCS Address, and Bank Select switches for your system as per the **Configuration Settings** of Section 3. Note the Rev level of your Acumen to determine which Section 3 diagrams to use.

3. **With power off,** plug the Acumen board into any available slot in your system and connect expansion memory board cables, if any.

4. Power on, boot and run as usual. If desired, run DOCS or other diagnostics to verify correct operation.

2.1 In Case of Trouble

If your Acumen operates, but shows memory errors, see section 4.7.

In the event your Acumen 301 fails to be recognized by the system, fails to boot, or crashes the system:

1. Verify correct switch settings. Note the direction of the "ON" arrow on switch bank housings and corresponding orientation in the Configuration Settings diagrams of Section 3. If running DOCS, be sure to tell DOCS that Acumen is a "16k Cache Controller" (fib) at the pertinent prompt.

2. Verify that Acumen memory space does not overlap any other memory space used by other memory or peripherals.

3. If 1 and 2 don't correct the problem, power off, pull the board and inspect the back-plane connector for debris, bent pins, etc. (you will need a flashlight). Try the board in a different slot.

4. **If all else fails, call your dealer or Western Automation Technical Support.**

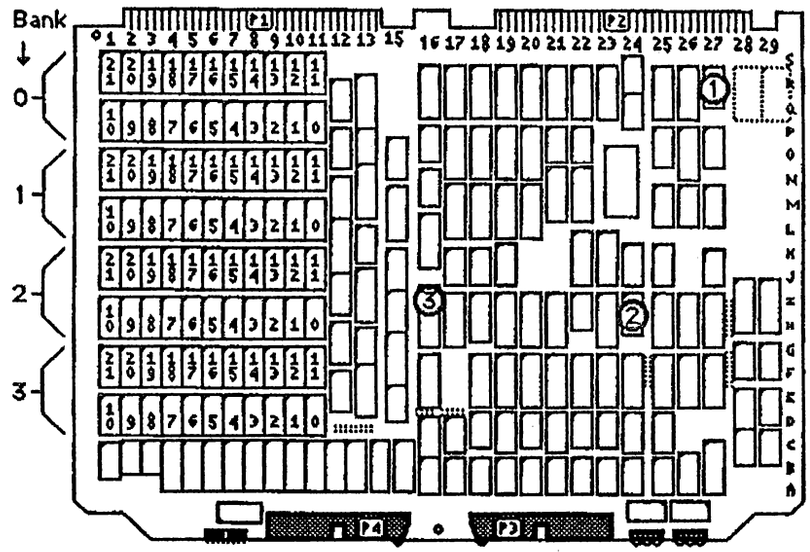
3.0 Configuration Settings

The following two figures apply to two different Acumen Rev levels. The Rev level of your Acumen is silkscreened along the right edge of the board as viewed with the word "Acumen" right side up. Figure 3.0–1 applies to Rev levels PA, PB, and PC. For Rev PE and higher, refer to Figure 3.0–2.

The Acumen 301 is normally shipped with the switches set to use all installed memory, starting at base address ØØØØØØ, and using TPCS address FB1Ø. The following figures indicate other settings you may need if you have other memory boards or other boards which require exclusive use of high address space in your system. For example, if you already have TPCS address FB1Ø assigned, the next recommended TPCS address, FB14, should be assigned to the Acumen 301. If you are running a 990/10A with 1 Mbyte of onboard memory, you will only be able to use 1024k on the Acumen 301 (Bank Enable switches 1 & 2 ON), and the Acumen addresses must start where the /10A address space leaves off, i.e., at $1ØØØØØ_{16}$ (Base Address switch 1 ON).

Take care not to overlap memory space or TPCS addresses with any other boards in your system. Use the List Device Configuration (LDC) command to determine TPCS addresses already in use.

If you have special devices which need exclusive use of high address space, such as Houston Computer Services Octacomm™ boards, special Bank Select switch options for 1920K (frees 1 64Kbyte block), 1792K (frees 3 64Kbyte blocks), and 1664K (frees 5 64Kbyte blocks) are provided as shown in Figures 3.0–1 and 3.0–2. For 990/10A sytems with 1024k on the system board and a 1024k Acumen, the 896k and 768k settings provide total memory space of 1920k and 1792k respectively.



ACUMEN 301 REV PA, PB, PC

TPCS Address Switches (2)

Settings for recommended TPCS addresses

	1	2	3	4	5	6	7	8
FB1Ø								
FB14								
FB18								

Base Address Switch (1)

On = Add Byte Weight to total

ZO	Byte Weight Hex	Decimal
1	+ 100000	+ 1024k
2	+ 80000	+ 512k
3	+ 40000	+ 256k
4	+ 20000	+ 128k
5	+ 10000	+ 64k
6	+ 8000	+ 32k
7	+ 4000	+ 16k
8	+ 2000	+ 8k

Example: For 90000 (Hex): switches 2 & 5 ON

Bank Enable Switches (3)

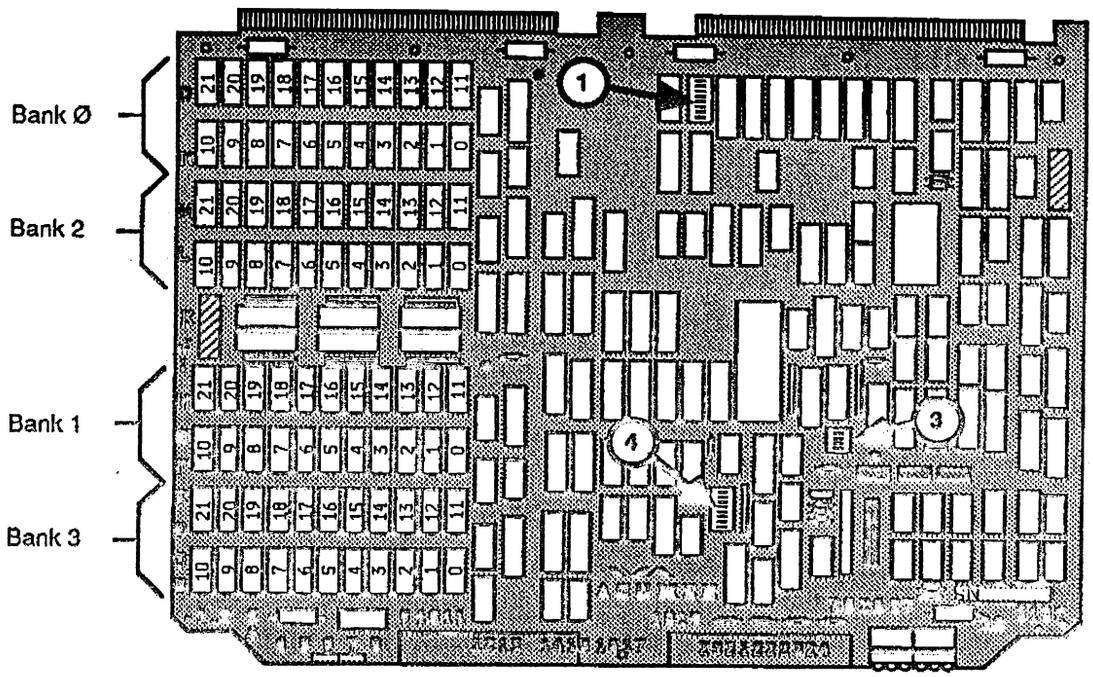
64k DRAM's	256k DRAM's	1	2	3	4	
512k	2048k					*
	1920k					
	1792k					
	1664k					
256k	1024k					*
	896k					
	768k					

Note: For switch settings marked with *, switches 1,2,3,4 correspond to primary memory banks Ø,1,2,3 respectively, and may be used accordingly to disable defective banks should need arise.

Other settings are special cases for disabling portions of high memory space (see text).

■ = ON ▯ = OFF

Figure 3.0-1 Acumen 301 Rev PA, PB, PC Configuration Settings



ACUMEN 301 REV PE & above

TPCS Address Switches (1)

Settings for recommended TPCS addresses

	1	2	3	4	5	6	7	8
FB1Ø								
FB14								
FB18								

Base Address Switch (4)

On = Add Byte Weight to total

►ZO	Byte Weight Hex	Decimal
1	+ 100000	+ 1024k
2	+ 80000	+ 512k
3	+ 40000	+ 256k
4	+ 20000	+ 128k
5	+ 10000	+ 64k
6	+ 8000	+ 32k
7	+ 4000	+ 16k
8	+ 2000	+ 8k

Example: For 90000 (Hex): switches 2 & 5 ON

Bank Enable Switches (3)

64k DRAM's	256k DRAM's	1	2	3	4	
512k	2048k					*
	1920k					
	1792k					
	1664k					
256k	1024k					*
	896k					
	768k					

Note: For switch settings marked with *, switches 1,2,3,4 correspond to primary memory banks Ø,1,2,3 respectively, and may be used accordingly to disable defective banks should need arise.

Other settings are special cases for disabling portions of high memory space (see text).

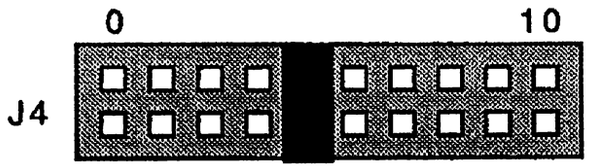
■ = ON ▯ = OFF

Figure 3.0-2 Acumen 301 Rev PE & above Configuration Settings

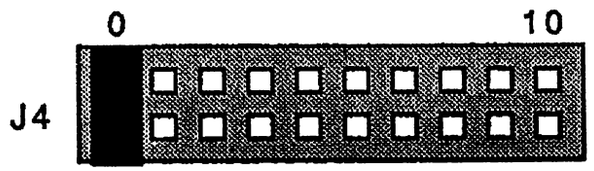
3.1 Timing Settings (301+ or 301 Rev PE and above only)

For Rev PE and above the 10 position J4 option block at location 26D is provided for fine tuning Acumen access time. The position of the shorting block determines the time delay allowed from the beginning of a TLGO signal (begins a memory Read or Write cycle) and the time the address bus is sampled. Systems with many boards tend to have noisier address busses, and may require a longer delay time here than lightly loaded systems. You may wish to experiment with different settings to tune up your system. Moving the shorting block towards "0" gives shorter delay times and thus faster operation, and vice versa. For each trial setting you must power down to reset the delay, and then reboot. The recommended procedure is to start at the fastest setting and work your way up until you have at least a week of stable operation. Each jumper position represents 5 nanoseconds of delay.

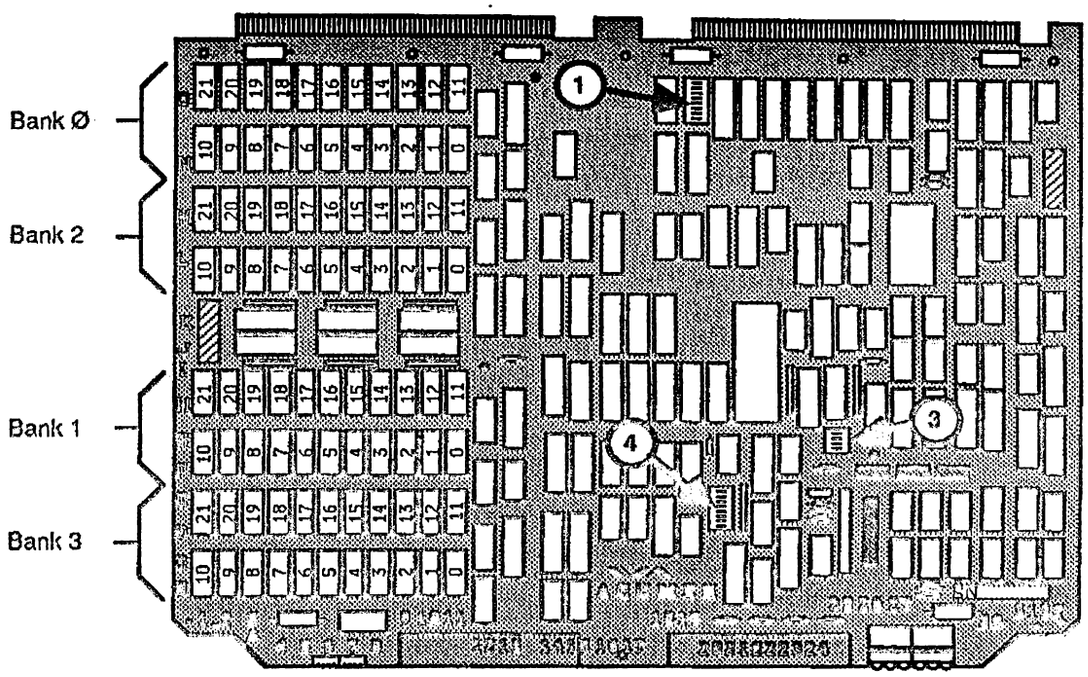
The Acumen 301 is shipped with this delay set at 0. The Acumen 301+ is shipped with this delay set at 4. (NOTE: tap 4 on the 301+ is the same relative time as tap 0 on the standard 301).



Acumen 301+ Initial Setting



Acumen 301 Initial Setting



ACUMEN 301 REV PE & above

TPCS Address Switches (1)

Settings for recommended TPCS addresses

	1	2	3	4	5	6	7	8
FB1Ø								
FB14								
FB18								

Base Address Switch (4)

On = Add Byte Weight to total

ON		Byte Weight Hex	Byte Weight Decimal
	1	+ 100000	+ 1024k
	2	+ 80000	+ 512k
	3	+ 40000	+ 256k
	4	+ 20000	+ 128k
	5	+ 10000	+ 64k
	6	+ 8000	+ 32k
	7	+ 4000	+ 16k
	8	+ 2000	+ 8k

Example: For 90000 (Hex): switches 2 & 5 ON

Bank Enable Switches (3)

64k DRAM's	256k DRAM's	1	2	3	4	
512k	2048k					*
	1920k					
	1792k					
	1664k					
256k	1024k					*
	896k					
	768k					

Note: For switch settings marked with *, switches 1,2,3,4 correspond to primary memory banks Ø,1,2,3 respectively, and may be used accordingly to disable defective banks should need arise.

Other settings are special cases for disabling portions of high memory space (see text).

■ = ON ▭ = OFF

Figure 3.0-2 Acumen 301 Rev PE & above Configuration Settings

3.1 Timing Settings (Rev PE and above only)

For Rev PE and above the 10 position J4 option block at location 26D is provided for fine tuning Acumen access time. The position of the shorting block determines the time delay allowed from the beginning of a TLGO signal (begins a memory Read or Write cycle) and the time the address bus is sampled. Systems with many boards tend to have noisier address busses, and may require a longer delay time here than lightly loaded systems. You may wish to experiment with different settings to tune up your system. Moving the shorting block towards "0" gives shorter delay times and thus faster operation, and vice versa. For each trial setting you must power down to reset the delay, and then reboot. The recommended procedure is to start at the fastest setting and work your way up until you have at least a week of stable operation. The Acumen 301 is shipped with this delay set at 0.

4.0 Principles of Operation

4.1 Overview

The Acumen 301 functions as a TILINE slave device and generates or accepts data only in response to a TILINE master device. Operation should be virtually identical to that of corresponding TI boards except for accelerated speed and increased memory capacity. All pertinent TILINE control and data signals are accommodated, as well as the expansion memory interface.

The Acumen contains four banks of dynamic RAM (DRAM) memory organized as two odd/even addressed pairs. Appropriate pairs of banks may be disabled (e.g. in case of malfunction) via four "Bank Select" pencil switches, in which case memory addressing will automatically be reorganized to make the best use of those banks remaining enabled. Other special settings of the Bank Select switches will disable portions of high memory (on a fully populated 2 Mbyte board) so the address space can be used by other peripherals. Each bank includes DRAM devices for 16 data bits plus 6 error checking bits for a total of 22 devices per bank. 64k x 1 devices yield 64k words (128k bytes) per bank; 256k x 1 devices yield 256k words (512k bytes) per bank. In Cache configuration, 8 4k x 4 high-speed static RAM devices are also installed to accommodate 8k bytes of Cache memory.

For error detection and correction, the controller generates a 6 bit modified Hamming code during a write operation which is checked during a read operation to see if single or multiple bit errors have occurred. Single bit errors are corrected automatically during a read operation. Double bit errors cannot be corrected, but are detected and reported. Three or more bits in error may or may not be detected.

The Acumen 301 board includes LED indicators (see section 4.7) to show which banks are being accessed at a given instant, whether a single (correctable) error has occurred, whether a multiple (uncorrectable) error has occurred, whether a cache hit has occurred, and whether a cache error has occurred. LED displays locate the memory chip that caused the first error. The same information is reported in the appropriate TPCS Read Words (see section 4.2).

The Base (starting) Address of the on-board memory is established by a row of 8 pencil switches corresponding to the 8 most significant bits (msb) of the corresponding 20-bit TILINE address, permitting base address selection in 8 Kbyte increments (see Section 3 for settings). A second set of 8 pencil switches selects the TPCS Control address.

4.2 TPCS Control Operations

As with similar TI controllers, the TILINE Peripheral Control Space (TPCS) CPU addresses, $F8ØØ_{16}$–$FBFE_{16}$, are mapped into $FFCØØ_{16}$-$FFDFF_{16}$ of the 2048 Kbyte TILINE address space, and the Acumen board is assigned an odd/even pair of such addresses via its TPCS Address switch bank (see Section 3 for settings). A master device, e.g. the CPU, gains access to Acumen control logic via this TPCS address pair for purposes of monitoring and controlling Acumen operation. This TPCS Control address pair can be used to enable cache and/or ECC operation, control error latches, and operate Acumen in diagnostic mode.

The data presented on the TILINE data bus during a write operation to either of Acumen's TPCS Control addresses (even or odd) controls Acumen operation. READ operations of the odd and even words of the TPCS Control address provide information about Acumen operation and status. The details of these TPCS Control operations are presented in the following figures and tables.

Bit Assignments for Acumen 301 TPCS Words:

TPCS Control Write Word

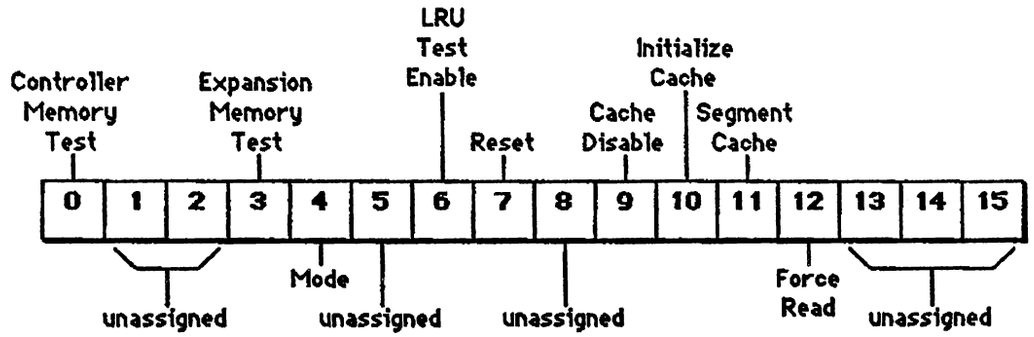


Figure 4.2-1

TPCS Control Write Word

Bit	Description
0	**Controller Memory Test** - When high, all read and write operations to onboard memory are modified as determined by bit 4.
1-2	Unassigned.
3	**Expansion Memory Test** - When high, all read and write operations to expansion memory are modified as determined by bit 4.
4	**Mode** - When low, error correction is disabled, when high data bits 0–5 are swapped with the ECC field for both read and write operations. Applies as specified by the settings of bits 0 and 3.
5	LRU Test Enable - echoed to bit 11 of Read Word 0. No other action. (1 bank cache)
6	Unassigned.
7	**Reset** - When high, primary and cache memory error logic and the associated error indicator LEDs are reset and held cleared. This bit must be reset to re-enable error logic.
8	Unassigned
9	**Cache Disable** - When low, the cache logic is enabled, that is, the cache controller will process primary memory references through the cache memory. When high, the cache logic is completely disabled, and all primary memory references are made directly to primary memory.
10	**Initialize Cache** - When toggled (set to 1, then 0), the cache memory is initialized; that is, all validity bits are set to false. All subsequent cache HITS will be disregarded unless the data was stored in the cache memory following the initialization.
11	**Segment Cache** - Not implemented.
12	**Force Read** - When high, this bit forces the cache to answer if an address match occurs. This bit is used to read cache addresses with parity errors.
13-15	**Unassigned**

TPCS Control Read Words

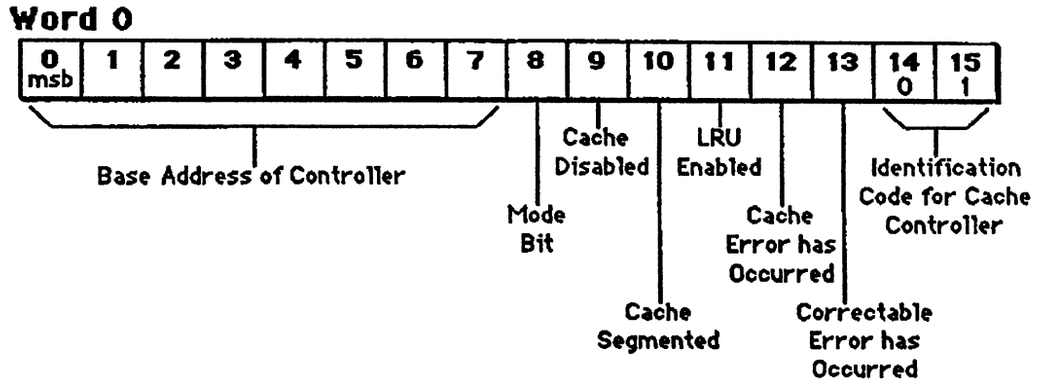


Figure 4.2-2

Bit Assignments for TPCS Control Read Word 0:

Bit	Description
0-7	**Base Address** - These eight bits indicate the setting found on the Acumen primary memory Base Address pencil switches.
8-11	These bits echo the diagnostic state of the controller as follows: bit 8 = mode, bit 9 = cache disabled, bit 10 = cache segmented, and bit 11 = LRU enabled (LRU is not implemented for Acumen which has only one bank of cache memory. Bit 11 thus only echoes bit 6 of the TPCS write word).
12	**Cache Error** - When high, a parity, validity, or bit error fault has occurred during a cache operation.
13	**Correctable Error** - When high, a single-bit error has been detected and corrected in a fetch from primary memory. Corresponds to the state of the "Single Error" LED.
14-15	**ID Code** - 01 to indicate Cache Controller.

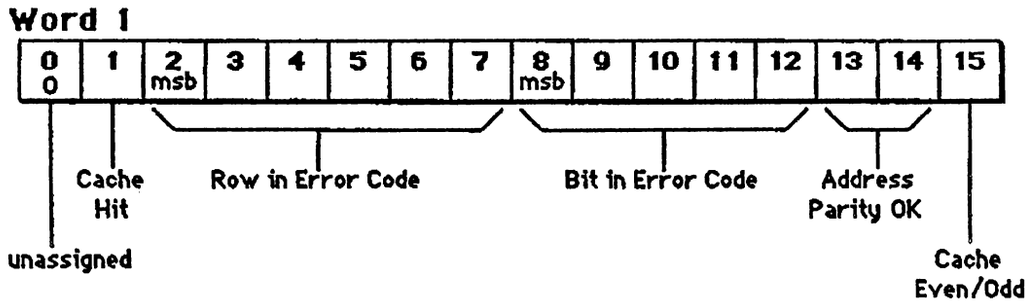


Figure 4.2-3

Bit Assignments for TPCS Control Read Word 1:

Bit	Description
0	Unassigned (always 0).
1	**Cache Hit** - This bit high indicates a cache hit.
2-7	**Row in Error** - These bits correspond to the Row-In-Error display. In accordance with TI convention, a "row" refers to a contiguous 16k segment of primary memory address space.
8-12	**Bit in Error** - These bits correspond to the Bit-In-Error display.
13-14	**Address Parity OK** - These bits high indicate the parity bits associated with the address fetch from cache memory were good. Should always be identical.
15	**Cache Even/Odd** - This bit high indicates an even word from cache memory has been selected. When low, an odd word has been selected.

4.3 Timing and Control

The Acumen 301 memory controller monitors the TILINE, decodes addresses on the TILINE address bus, and directs the performance of onboard and expansion memory Read and Write cycles under control of a TILINE MASTER device (e.g. the CPU).

The principle handshake signals between Acumen and the TILINE are:

From Master:

TLGO- Active low to initiate a TILINE request from a master device; inactive between TILINE requests.

TLREAD High indicates READ request, low indicates WRITE.

From Slave (Acumen):

TLMER- Active low to indicate a non-recoverable error has occurred during a memory READ operation.

TLTM- Active low to indicate that the requested operation has been completed, and either READ data may be strobed or WRITE data and control may be released.

Further information about TILINE signals is available in the TI Hardware Reference Manual for your TI model computer.

When Acumen senses TLGO- asserted, it waits for signals to settle, and determines if the address then present on the TILINE address lines falls within its on-board range. If so, the requested memory cycle is initiated.

A refresh cycle (required to maintain contents of dynamic RAM devices) is carried out approximately every 15 µsec. At this rate, all 256 row addresses of DRAM are refreshed within 4 msec.

4.4 ECC Operation

With error correction enabled, Acumen 301 generates a 6 bit modified Hamming Error Correction Code (ECC) for each data word written to primary memory, and stores it with the word. It also generates an ECC for each word read and compares it with the stored ECC. If the generated and stored ECC's are different an error has occurred. Single bit errors are corrected before presenting the data to the TILINE. Two bit errors will be detected, but not corrected. Three or more bit errors may or may not be detected. Detection of any error latches the Bank, Bit, and Row displays and the TPCS read word error reporting fields.

The heart of ECC operation is an LSI device, a 16 bit Parallel Error Detection and Correction Circuit, which, under Acumen control can a) generate a checkword, b) read data and checkword, c) latch and flag errors, or d) correct the data word and generate syndrome bits identifying the bit in error. The gross error conditions of all lows or all highs will be detected. Otherwise, reliable detection of errors in three or more bits of the 22 bit word are beyond the capabilities of the device.

4.5 Cache Operation

The objective of the cache memory system is to speed up operation by providing faster access to more frequently used memory words. This is accomplished by adding 8k bytes of high-speed static RAM cache memory, and keeping it loaded with the most recently read words from primary memory.

With the cache enabled, any READ operation referencing primary memory checks the cache first, and, if there is a "hit" (valid address match) the requested data word is provided immediately from cache. If there is not a "hit", the data word is read from primary memory and written (along with its associated odd or even partner) to the cache as well as returned to the requester on the TILINE. Since substantial speed improvement arises from caching contiguous segments of memory, both the odd and even addressed words are stored in cache whenever either is read. The primary memory is organized in Odd and Even banks, both addressed when either is read, thus facilitating rapid writing of both words to cache during a single READ cycle.

The cache memory is addressed by the 12 lsb (least significant bits) of the TILINE address, and stores the 8 msb (most significant bits) of the TILINE address, the associated 16 bit data word, 3 parity bits, and two validity bits which are reset upon cache initialization and set upon writing a word to cache. At the beginning of a READ or WRITE operation, the 8 address bits read from cache are compared to the incoming 8 msb. If cache mode is enabled, validity bits set, and there are no cache parity errors, a match on the 8 most significant address bits generates a cache "hit" signal, which conditions the remainder of the READ cycle as already described, or, for a WRITE cycle, updates the cache copy (as well as the primary memory location) of the word being written. This means a given cache word pair only gets overwritten when a READ occurs at an address with the same 12 lsb and a different 8 msb, which favors caching of contiguous segments.

Words in which errors have been detected are either not written to cache, or written with their validity bits reset, according to whether they are the first or second word respectively of an odd/even pair. Only onboard and expansion memory accesses are cached.

4.6 Expansion Memory

Expansion memory boards are supported in the normal way. Error correction is carried out by the Acumen controller as already described. The Base Address and Bank Enable switches must be set to configure all boards without overlapping addresses or exceeding the 2Mbyte address space limit of the 990.

4.7 LED Displays

Visible through cut-outs in the RFI Shield (front panel) are two clusters of LED readouts, as shown in Figure 4.7-1. On the left are 8 single LED's which indicate Active Bank, Cache Hit, and Error status. On the right are 6 digits of 7-segment LED displays, only 4 of which are used, which indicate the Bit and Row being accessed during normal operation, or the Bit and Row in error upon detection by the ECC circuits of a single or double bit error. All displays in both clusters, with the exception of the "Cache Hit" LED, are latched upon the first detection of an error, and reset by the next IORESET pulse (see bit 7 of the TPCS Control Write Word in section 4.2). **The Cache Hit LED is not an error indicator, just the reverse. It signals that cache memory is being used (see section 4.5).**

4.7.1 Locating Errors

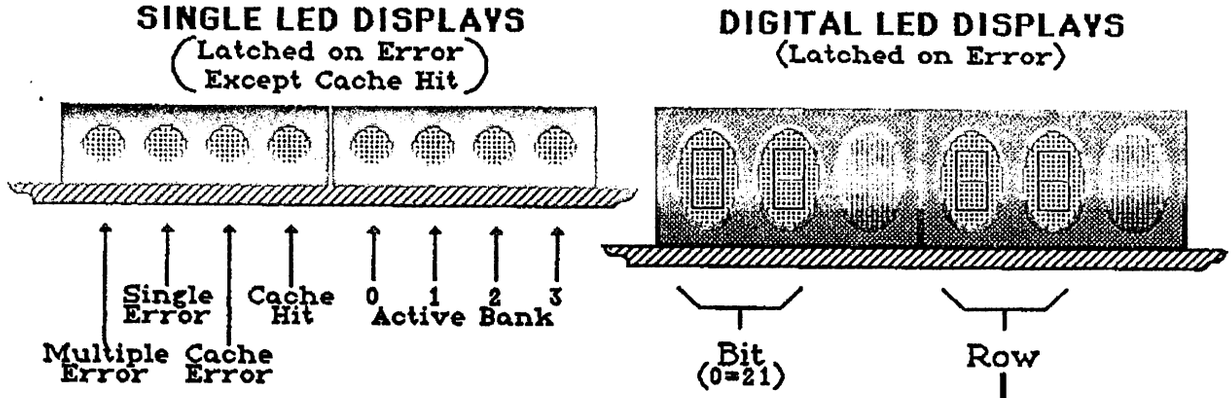
As illustrated by Figure 4.7-1, for ACUMENs with 64k memory devices (DRAM's) each of the 4 banks of memory comprises 128k bytes of memory configured as 64k 2 byte words for a maximum board capacity of 512k bytes. With 256k DRAM's each bank comprises 512k bytes (or 256k words) for a maximum board capacity of 2048k bytes. Either way the following methods for locating defective memory devices apply:

The Bit and Row indicators are normally illuminated with dashes or digits going by too fast to read during error free operation. Only when the "Single Error" LED is on do these digital displays stop (latch) and display the Bit and Row in error.

The memory device associated with a latched error display can be located by referencing the **Active Bank** and **Bit in Error** displays (as per the top drawings of Figure 4.7-1) directly to the map of Figure 3.0–1 or 3.0–2 (according to which Rev board you have), which shows the locations of each bank (0-3) of 22 devices (0-21) on the left side of the board. Bits 0-15 are data bits (2 bytes), and bits 16-21 are ECC check bits. Note that Banks 0 and 2 contain only even addresses, and Banks 1 and 3 contain only odd addresses (see lower drawings of Figure 4.7-1). Replacing the indicated memory device will usually correct the error condition. Spare memory devices are included on the Acumen 301 (at locations 28R and 29R on Rev PA, PB, and PC boards, locations 32N and 1J on Rev PE and above boards).

Correlating a memory Bank with the Row in Error display (far right pair of LED digits) is not as straightforward (see next section), nor should it normally be necessary as the method above is sufficient to locate an offending memory device. If you do find need to interpret the Row in Error display, for example in conjunction with DOCS diagnostics, see section 4.7.2.

Acumen 301
LED DISPLAYS



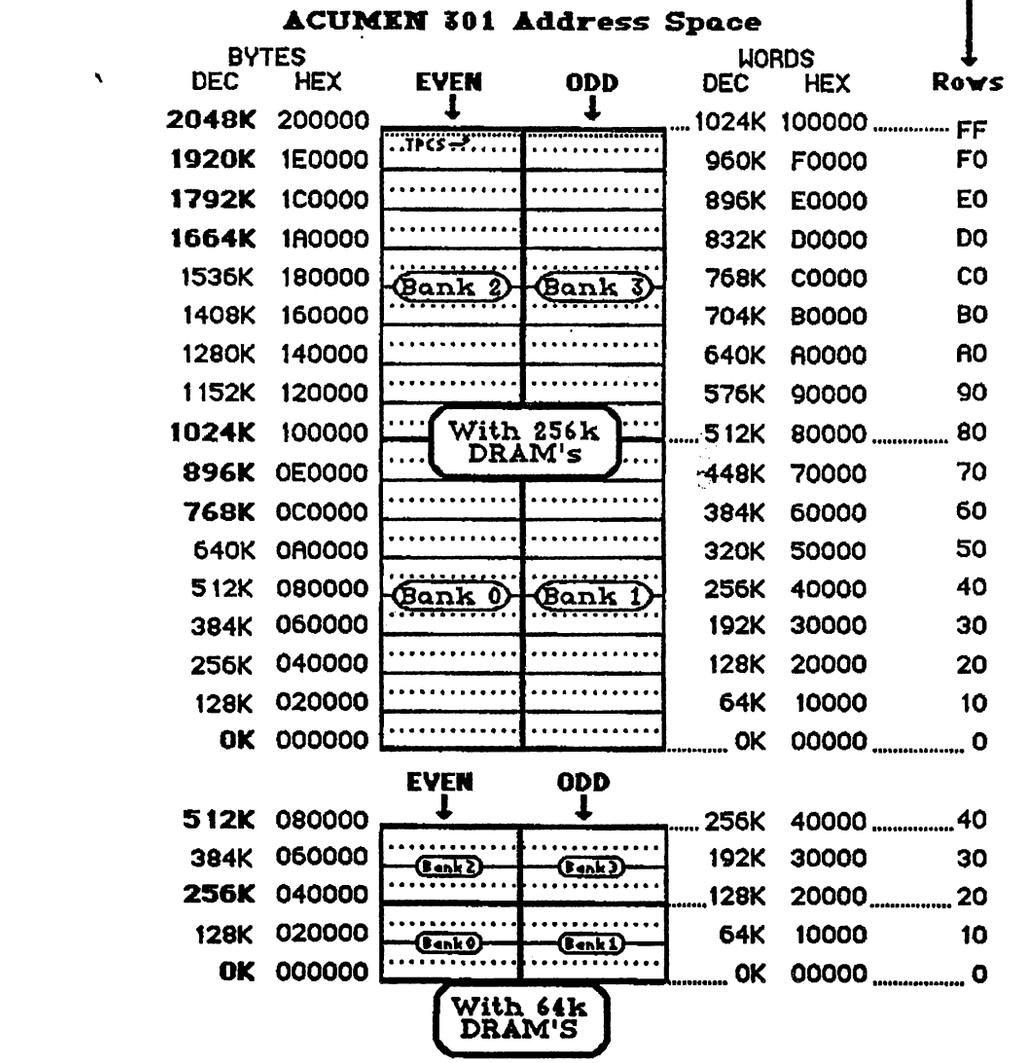


Figure 4.7-1

4.7.2 Row in Error Displays/Reports

The DOCS diagnostic program considers a "Row" to be a 32k byte (16k words) block of memory as per the use of 16k memory devices in the past. Thus there are 8 "Rows" per 64k DRAM Acumen Bank, and 32 "Rows" per 256k DRAM Acumen Bank.

Note also that DOCS considers Acumen 301 a "16k Cache Controller" when you respond to the pertinent DOCS prompt.

The Row in Error displayed on the digital LED displays is the hex word address of the row, but, for Rev PA, PB or PC boards the corresponding six most significant bits of the "Row in Error" reported via the TPCS Read Word 1 (bits 2-7) are reversed in terms of what DOCS expects. For example, if a DOCS diagnostic message on the CRT says the Row in Error is 3A (00111010) dropping the 2 left 0's (padding) and reversing the next 6 bits (111010)·(010111)gives an actual (ordinal) Row in Error of 17(with same padding), or a word address of 5C (without padding) which should agree with the digital display. The following table shows the pertinent translations for a 2 Mbyte Acumen 301. The entries pertaining to the above example are shown in bold face.

Acumen 301 ROW IN ERROR TRANSLATION TABLE

Bank 64K	Bank 256K	LED	CRT PA,PB,PC	CRT PE	DEC	Bank 256K	LED	CRT PA,PB,PC	CRT PE	DEC
0-1	0-1	00	00	00	00	2-3	80	01	20	32
		04	20	01	01		84	21	21	33
		08	10	02	02		88	11	22	34
		0C	30	03	03		8C	31	23	35
		10	08	04	04		90	09	24	36
		14	28	05	05		94	29	25	37
		18	18	06	06		98	19	26	38
		1C	38	07	07		9C	39	27	39
2-3		20	04	08	08		A0	05	28	40
		24	24	09	09		A4	25	29	41
		28	14	0A	10		A8	15	2A	42
		2C	34	0B	11		AC	35	2B	43
		30	0C	0C	12		B0	0D	2C	44
		34	2C	0D	13		B4	2D	2D	45
		38	1C	0E	14		B8	1D	2E	46
		3C	3C	0F	15		BC	3D	2F	47
		40	02	10	16		C0	03	30	48
		44	22	11	17		C4	23	31	49
		48	12	12	18		C8	13	32	50
		4C	32	13	19		CC	33	33	51
		50	0A	14	20		D0	0B	34	52
		54	2A	15	21		D4	2B	35	53
		58	1A	16	22		D8	1B	36	54
		5C	**3A**	**17**	**23**		DC	3B	37	55
		60	06	18	24		E0	07	38	56
		64	26	19	25		E4	27	39	57
		68	16	1A	26		E8	17	3A	58
		6C	36	1B	27		EC	37	3B	59
		70	0E	1C	28		F0	0F	3C	60
		74	2E	1D	29		F4	2F	3D	61
		78	1E	1E	30		F8	1F	3E	62
		7C	3E	1F	31		FC	3F	3F	63

TABLE 4.7-1

5.0 Specifications

Acumen 301 Technical Specifications

Operating Systems	Compatible with all software and operating systems including DNOS and DX10.
Compatibility	The Acumen 301 is compatible with all DS990/10, /10A, /12 systems and Business Systems 600 & 800. Acumen 301 will control Western Automation MB990™ and TI memory array boards.
Status LED's	Location of single bit error: 4 digit numerical LED's display bit and row in which an error is detected. Location of access Cache Hit Cache parity error Single bit error Multiple bit error
Board Sizes	256K, 512K,768K, 896K, 1024K, 1664K, 1792K, 1920K, 2048K (2MB) +8K cache memory
Operating Modes	ECC on/off Cache on/off Cache parity on/off
Memory Technology	Primary: 64K or 256K DRAMs Cache: 4Kx4 static RAMs
Power Consumption	2 Megabyte 301: 4 Amperes @ 5 volts
Weight	7 pounds maximum, including manual binder, in shipping container

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