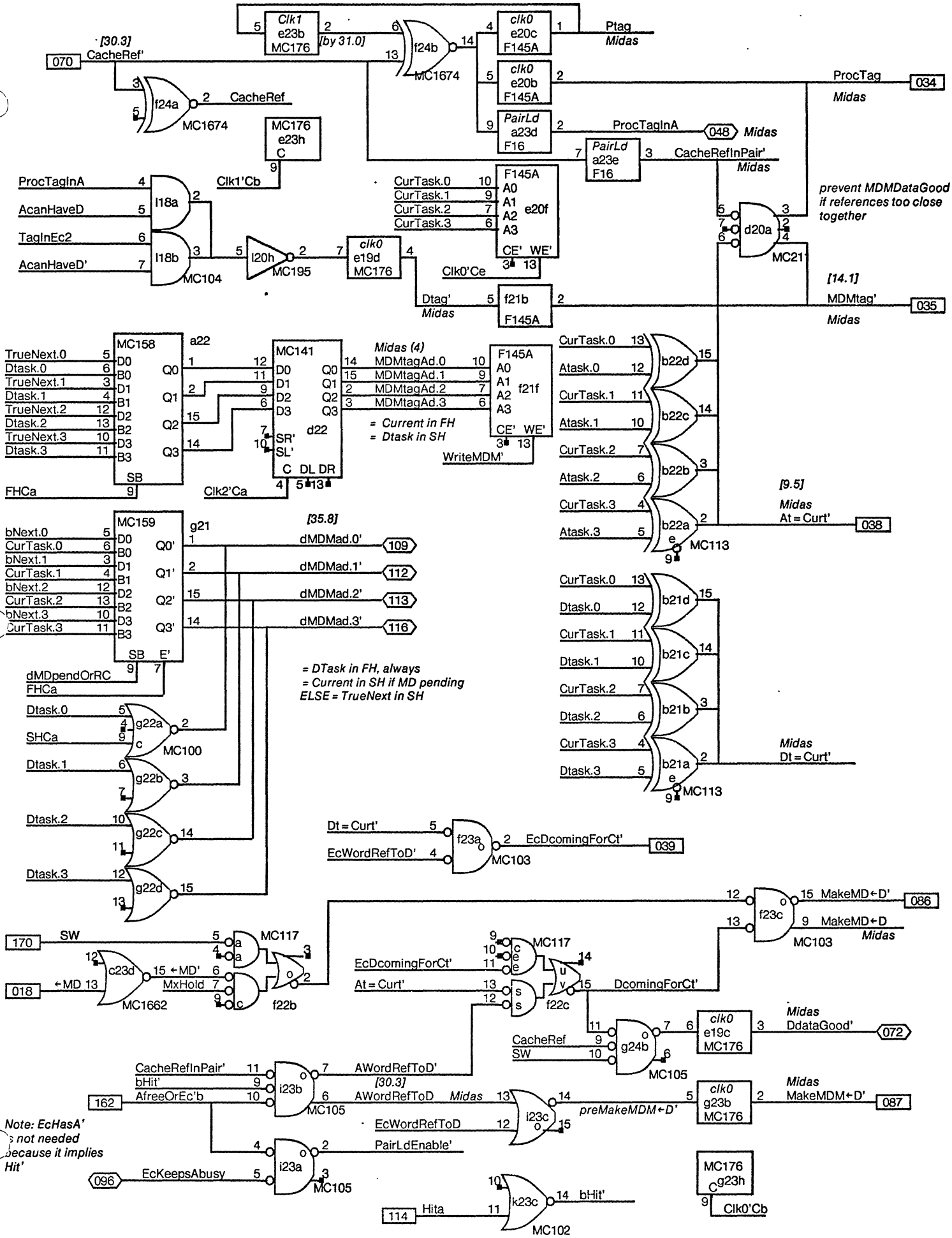
DORADO SCHEMATICS

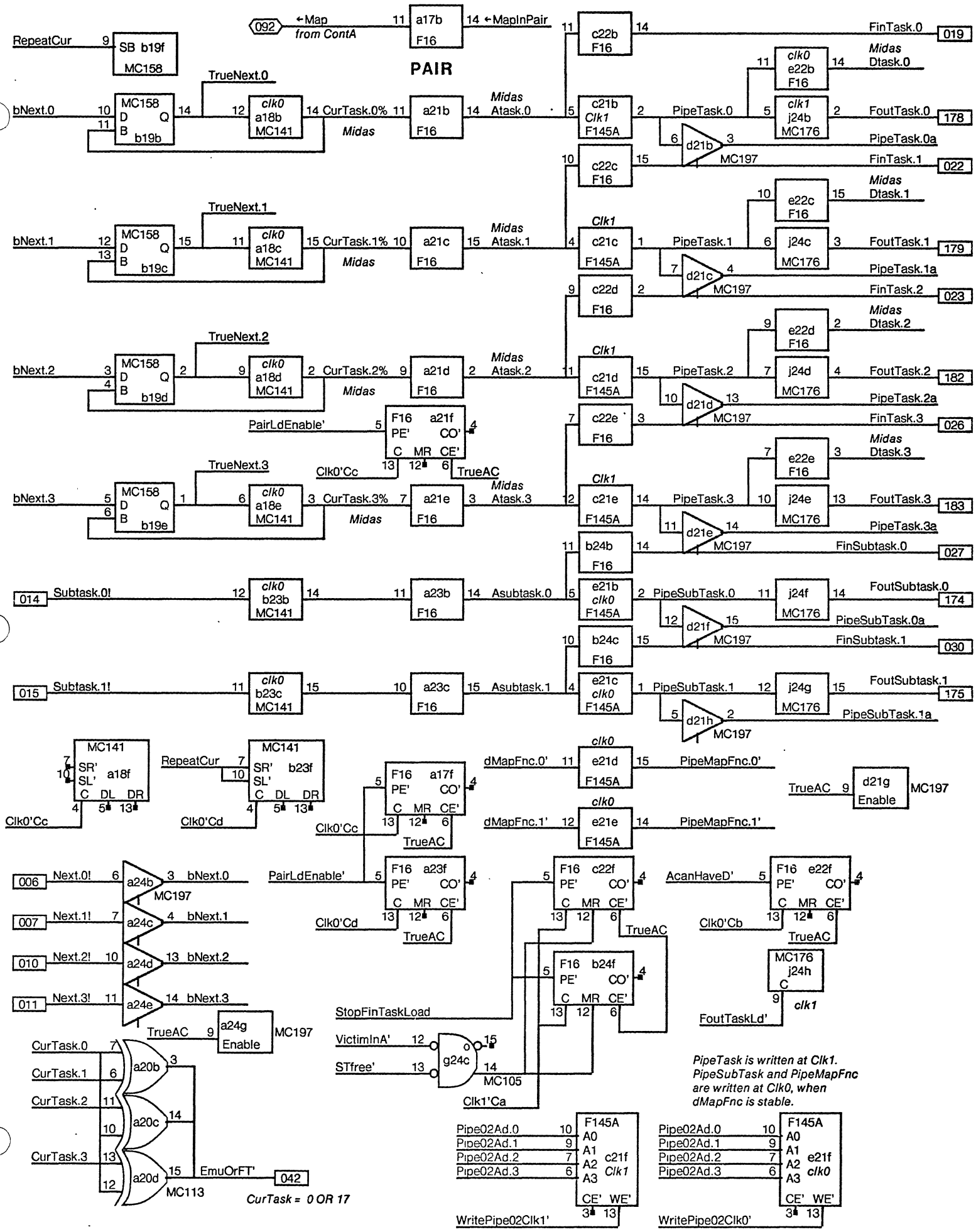
MemX

Table of contents

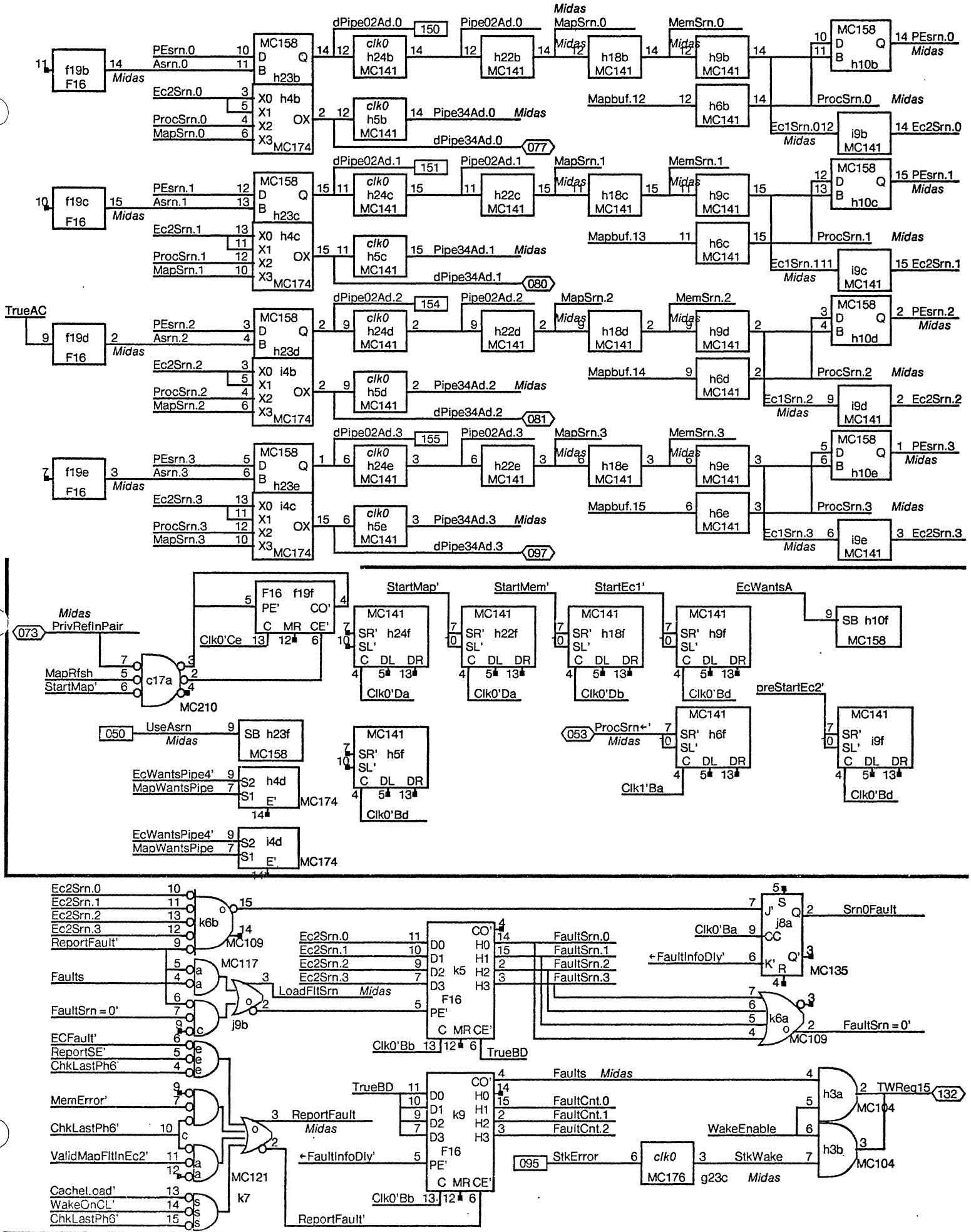
SIMTEST WILL SHOW MAPWAIT-MEMSTATE'(O.K. AND RBASGBYPASS/L



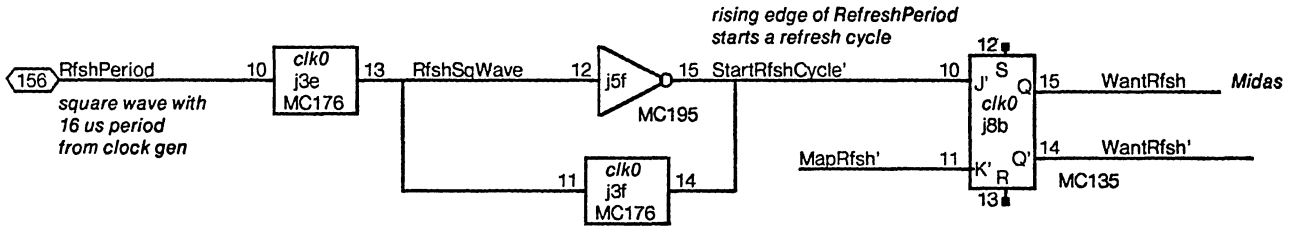
XEROX PARC	Project: Dorado	Memory Extension Board Tags, Tasks, MD Control	File: MemX01.sil	Designer: K. Pier	Rev: Cg	Date: 7/02/79	Page: 01



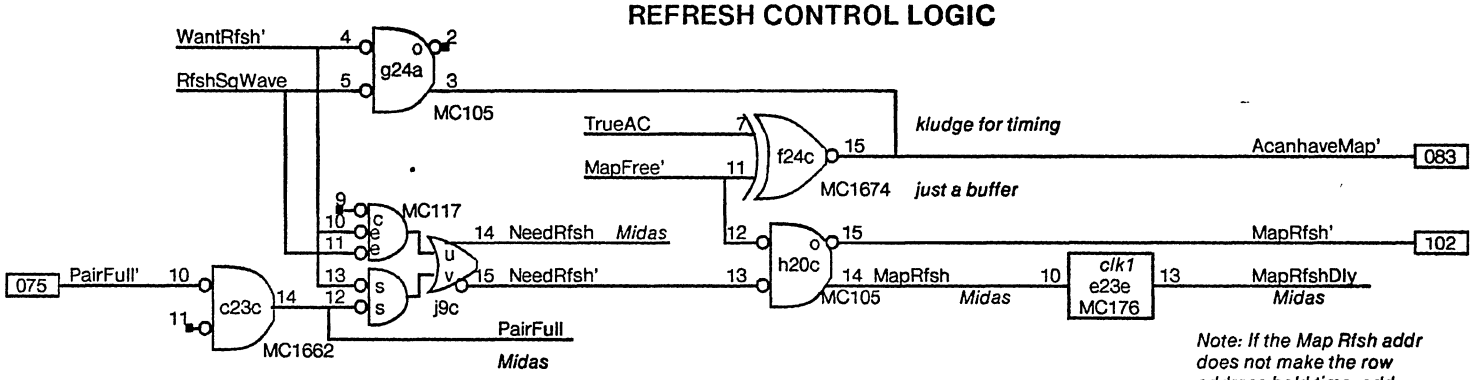
XEROX PARC	Project: Dorado	Memory Extension Board Next, *Task, Pipe 2	File: MemX02.sil	Designer: K. Pier	Rev: Cg	Date: 6/23/79	Page: 02



XEROX PARC	Project: Dorado	Memory Extension Board SRNs and Fault Info	File: MemX03.sil	Designer: K. Pier	Rev: Cg	Date: 9/08/79	Page: 03

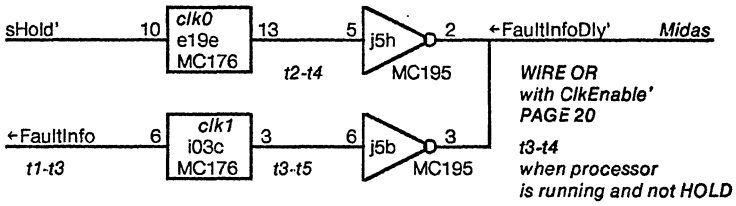


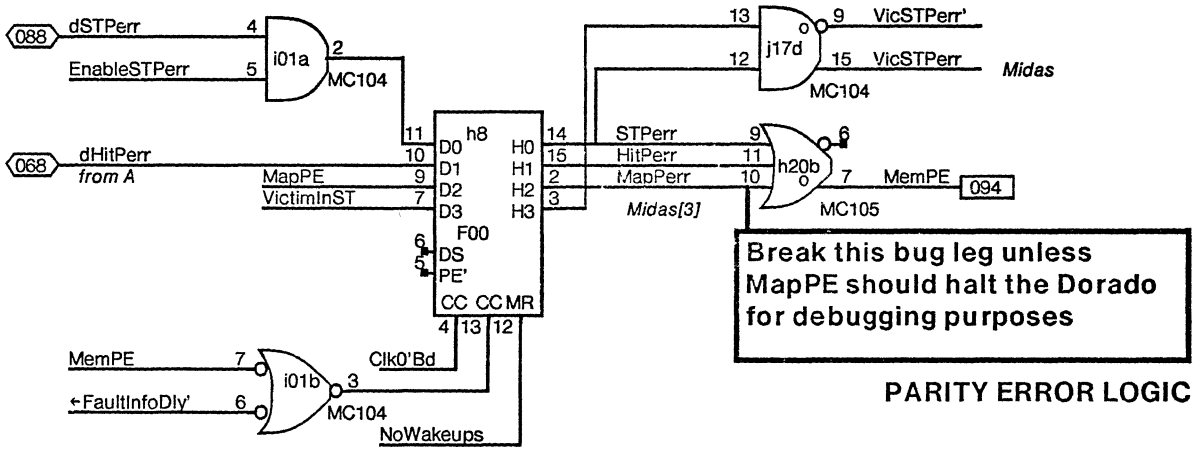
REFRESH CONTROL LOGIC



Note: If the Map Rfsh addr does not make the row address hold time, add a clk0 FF in series with this clk1 FF and OR the outputs with an OR gate.

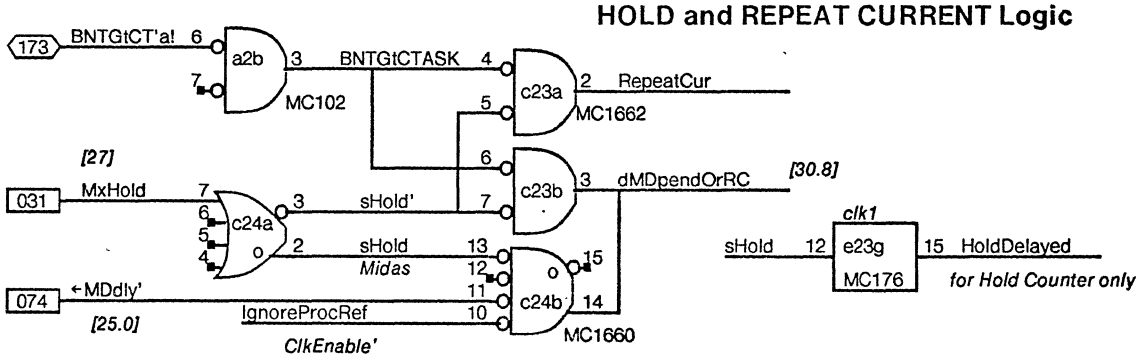
←FAULTINFO LOGIC



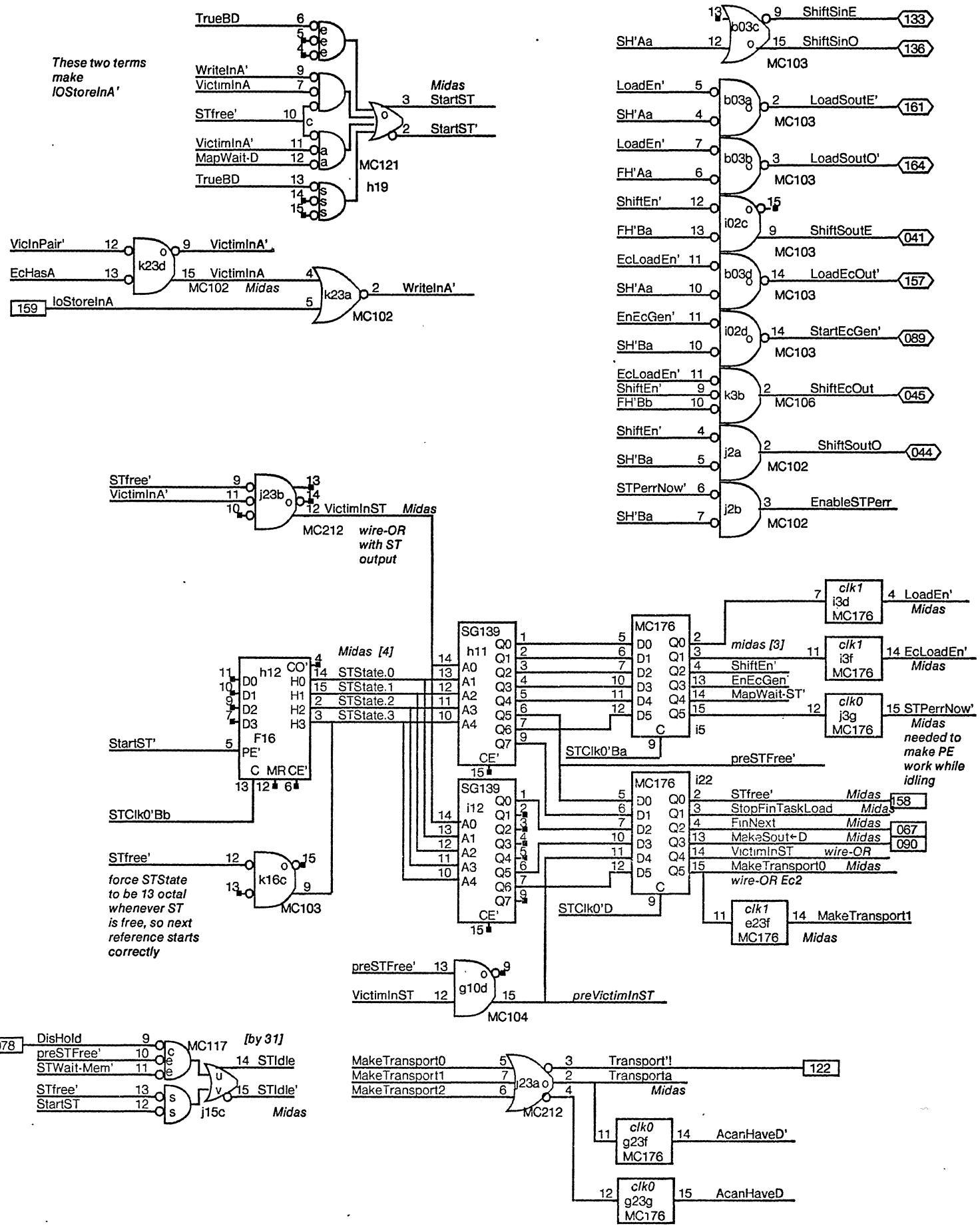


PARITY ERROR LOGIC

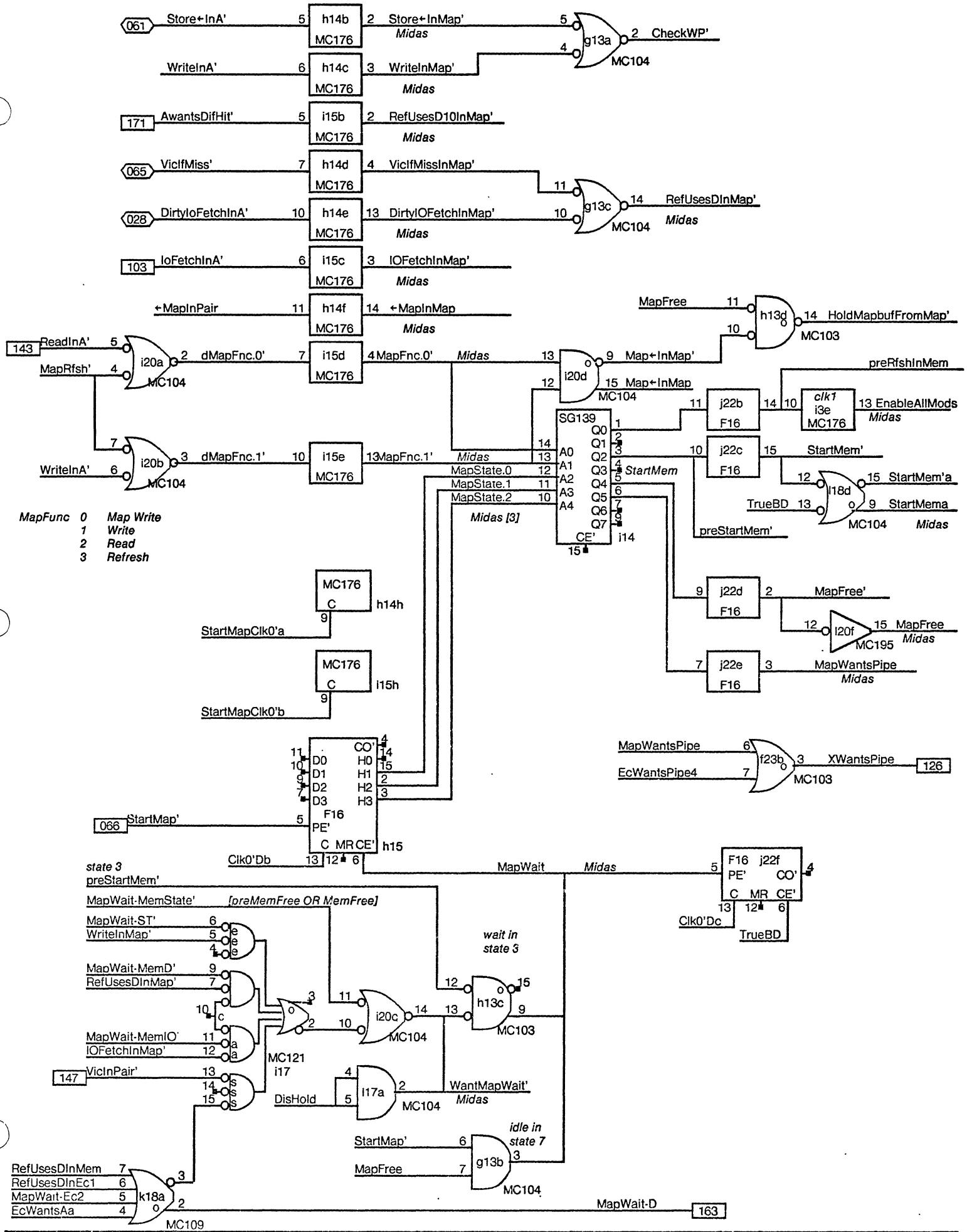
HOLD and REPEAT CURRENT Logic



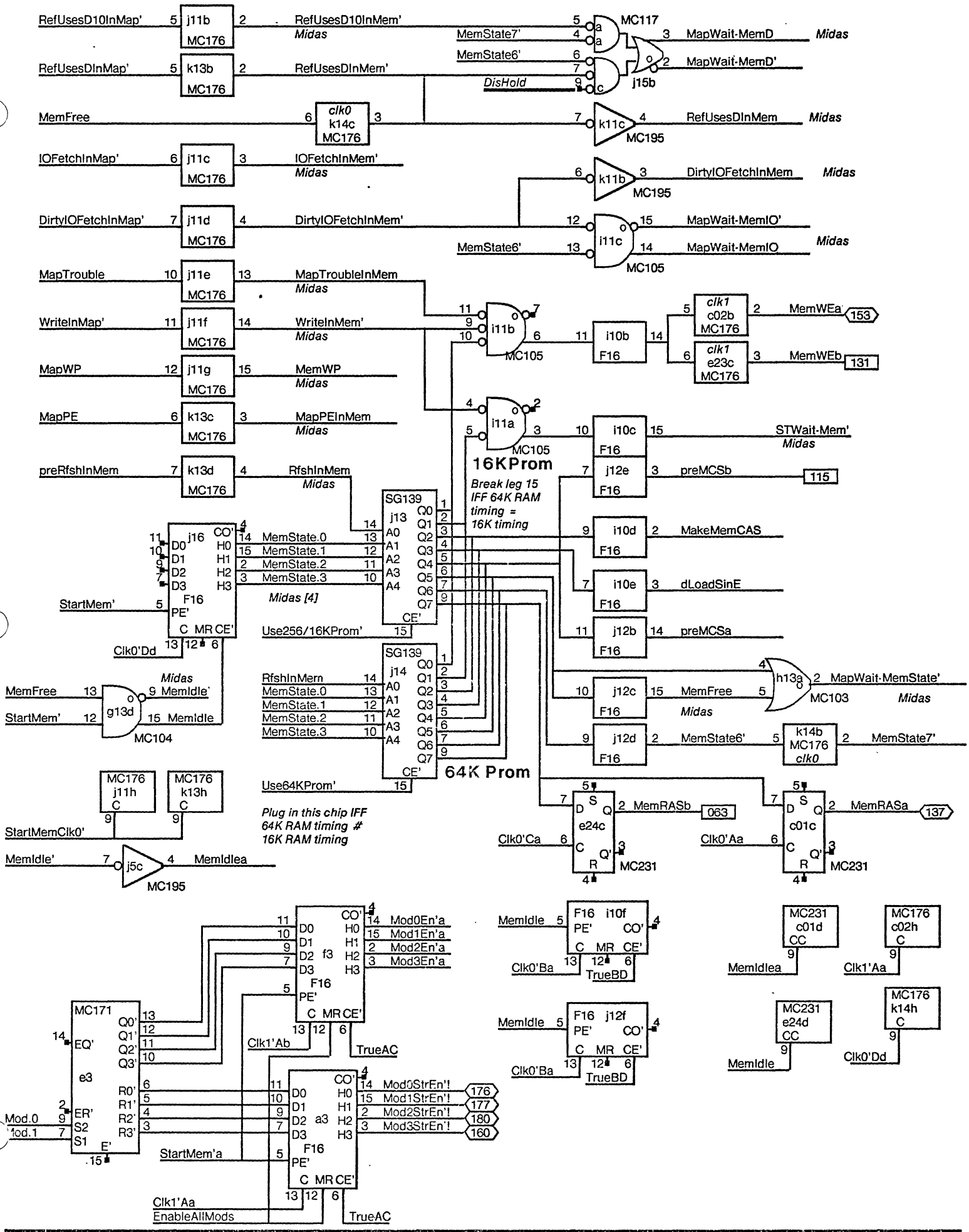
XEROX PARC	Project: Dorado	Memory Extension Board Refresh Control & PEs	File: MemX04.sil	Designer: K. Pier	Rev: Cg	Date: 7/11/79	Page: 04



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Store Transport Automaton	MemX05.sil	K. Pier	Cg	6/23/79	05



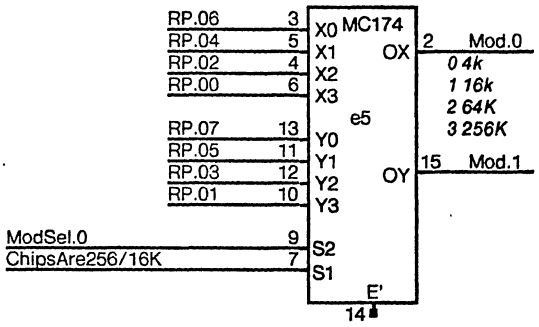
XEROX PARC	Project: Dorado	Memory Extension Board Map Automaton	File: MemX06.sil	Designer: K. Pier	Rev: Cg	Date: 6/23/79	Page: 06



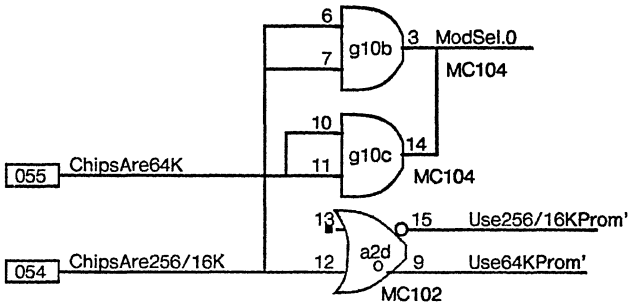
XEROX PARC	Project: Dorado	Memory Extension Board Memory Automaton	File: MemX07.sil	Designer: K. Pier	Rev: Cg	Date: 7/02/79	Page: 07

Note: Chip size options are available: 16K only, 16K or 64K, 64K only, 64K or 256K, 256K only.

Only one of the ChipsAreXXX signals should be true at any time.

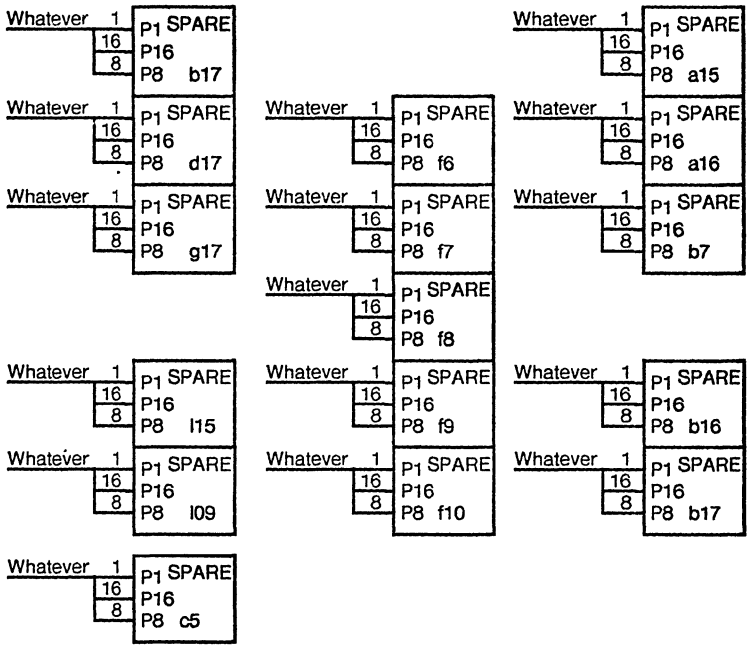


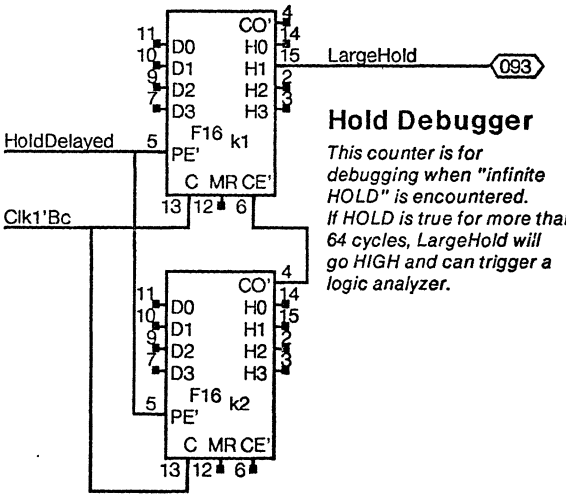
BREAK THIS BUG LEG UNTIL 256K CHIPS ARE USED



ChipsAre256k in the glorious future

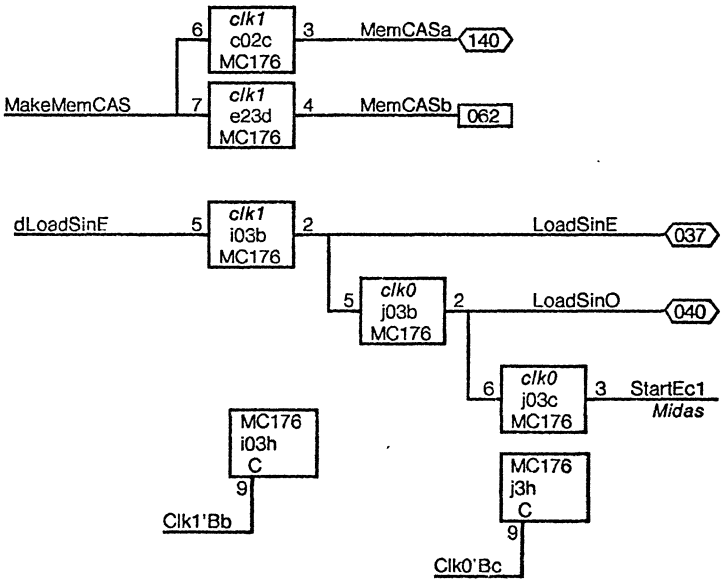
When the only two chip options for Dorado are 64K or 256K, then interpret this signal as ChipsAre256K and enable the upper gate of ModSel.0



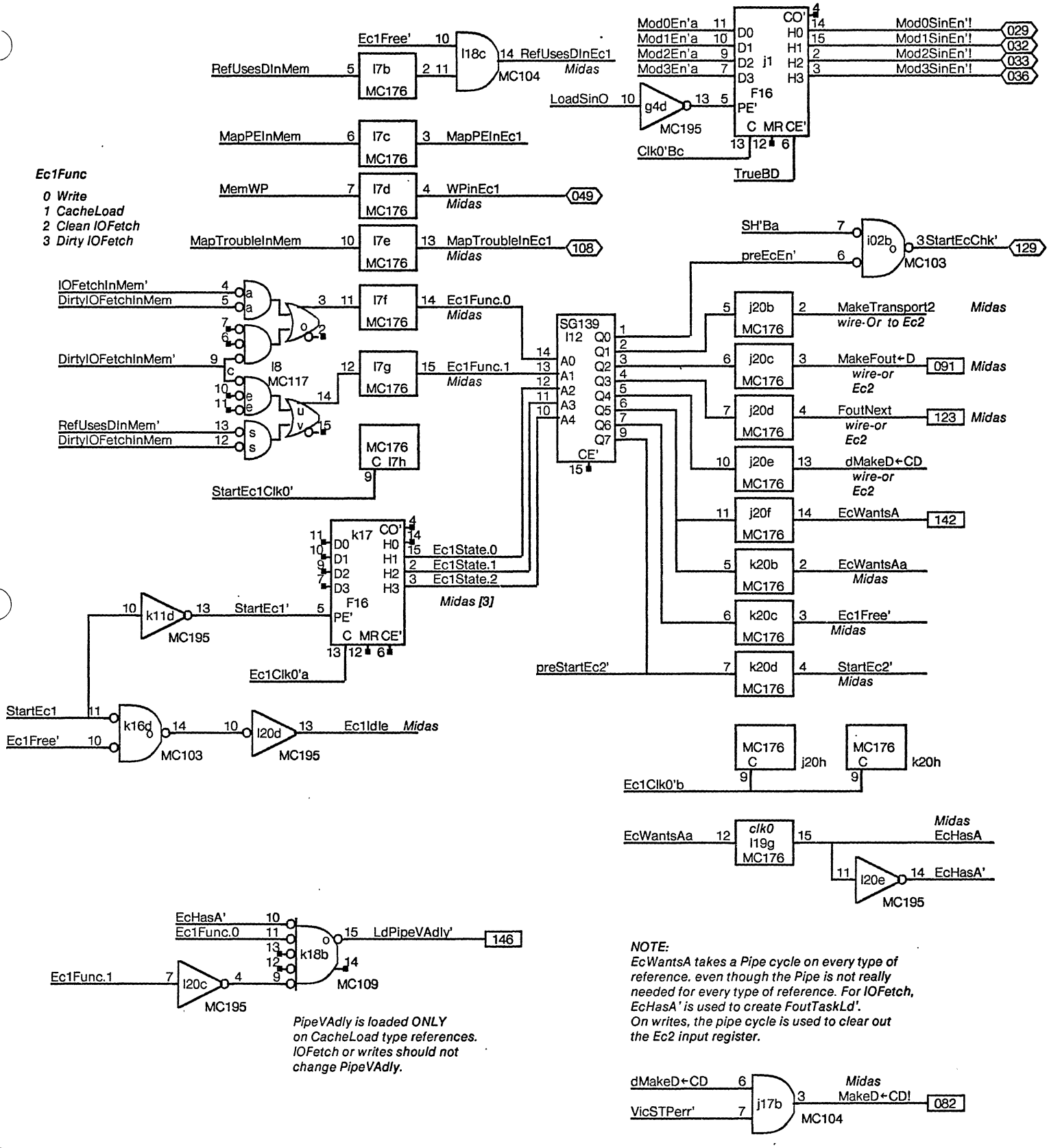


Hold Debugger

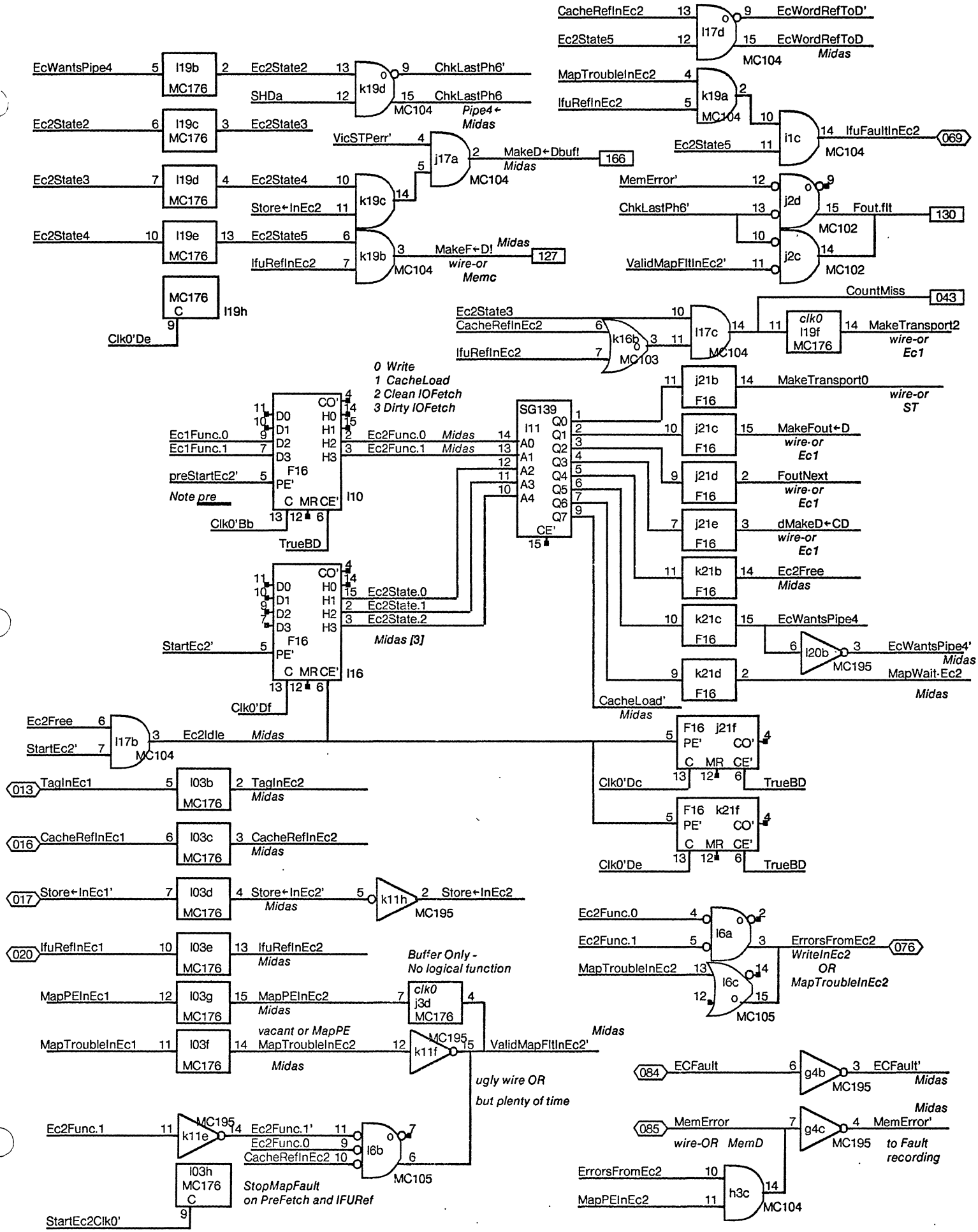
This counter is for debugging when "infinite HOLD" is encountered. If HOLD is true for more than 64 cycles, LargeHold will go HIGH and can trigger a logic analyzer.



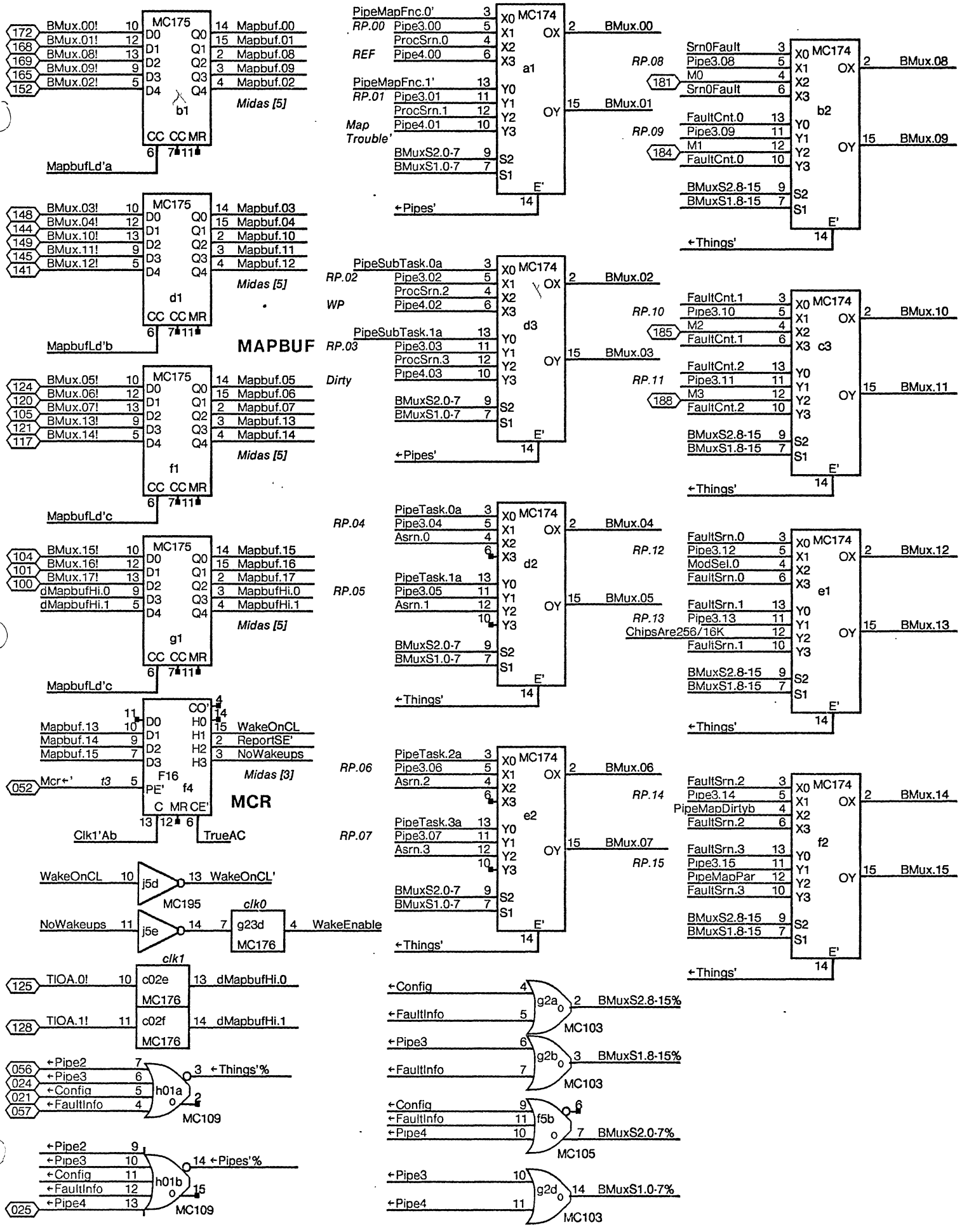
XEROX PARC	Project: Dorado	CAS Control RAM size control	File: MemX08.sil	Designer: K. Pier	Rev: Cg	Date: 10/29/79	Page: 08



XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Ec1 Automaton	MemX09.sil	K. Pier	Cg	7/11/79	09



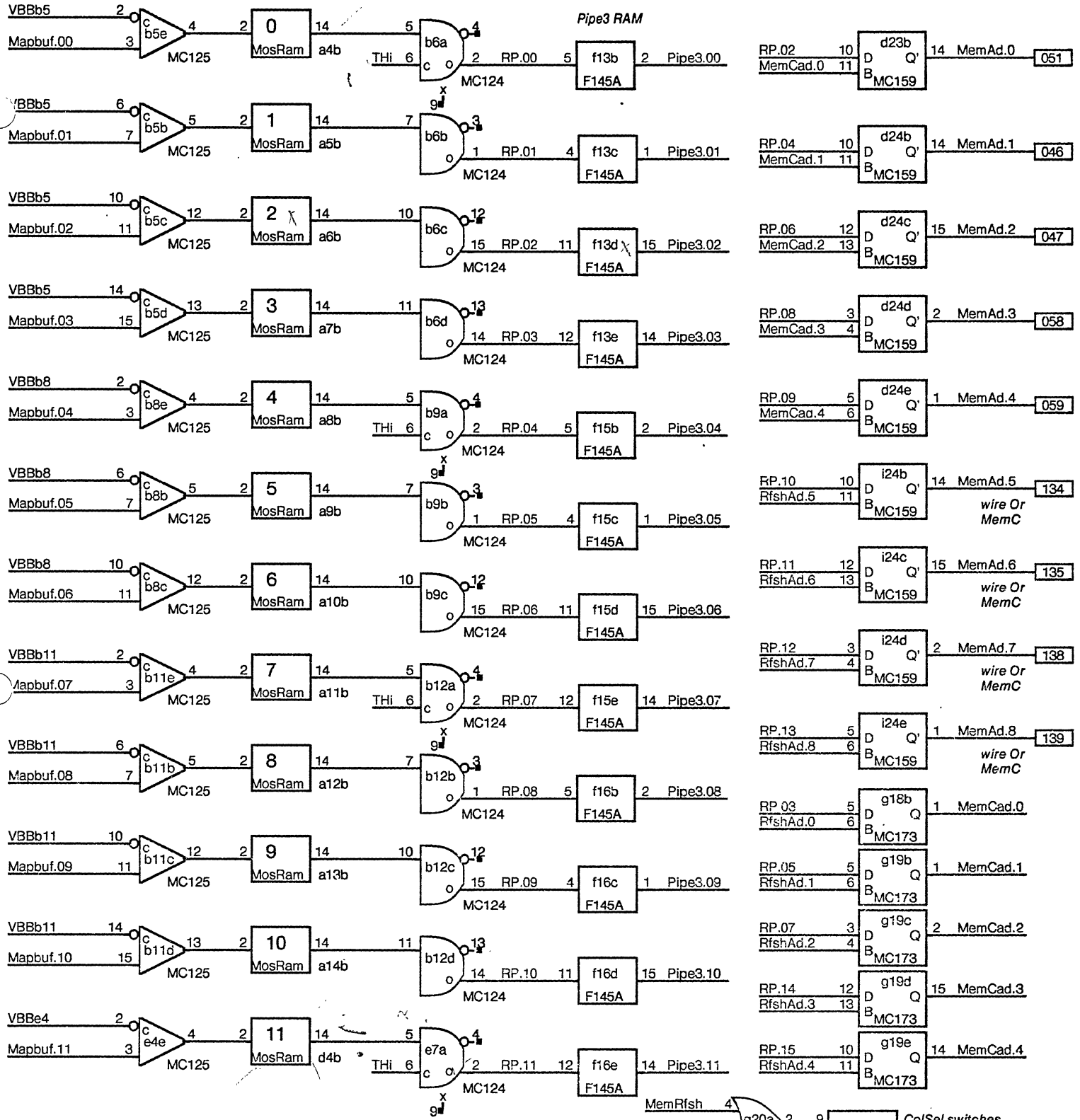
XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado Memory Extension Board Ec2 Automaton	MemX10.sil	K. Pier	Cg	9/08/79	10



XEROX PARC	Project: Dorado	Memory Extension Board BMux drivers and rcvrs	File: MemX11.sil	Designer: K. Pier	Rev: Cg	Date: 9/08/79	Page: 11

RP

PIPE 3



Chip	Mod 0	1	Row 0	1	2	3	4	5	6	7	8	Col 0	1	2	3	4	5	6	7	8
4k	6	7	-	-	-	8	9	10	11	12	13	-	-	-	14	15				
16k	4	5	-	-	6	8	9	10	11	12	13	-	-	7	14	15				
65k	2	3	-	4	6	8	9	10	11	12	13	-	5	7	14	15				
256	0	1	2	4	6	8	9	10	11	12	13	3	5	7	14	15				

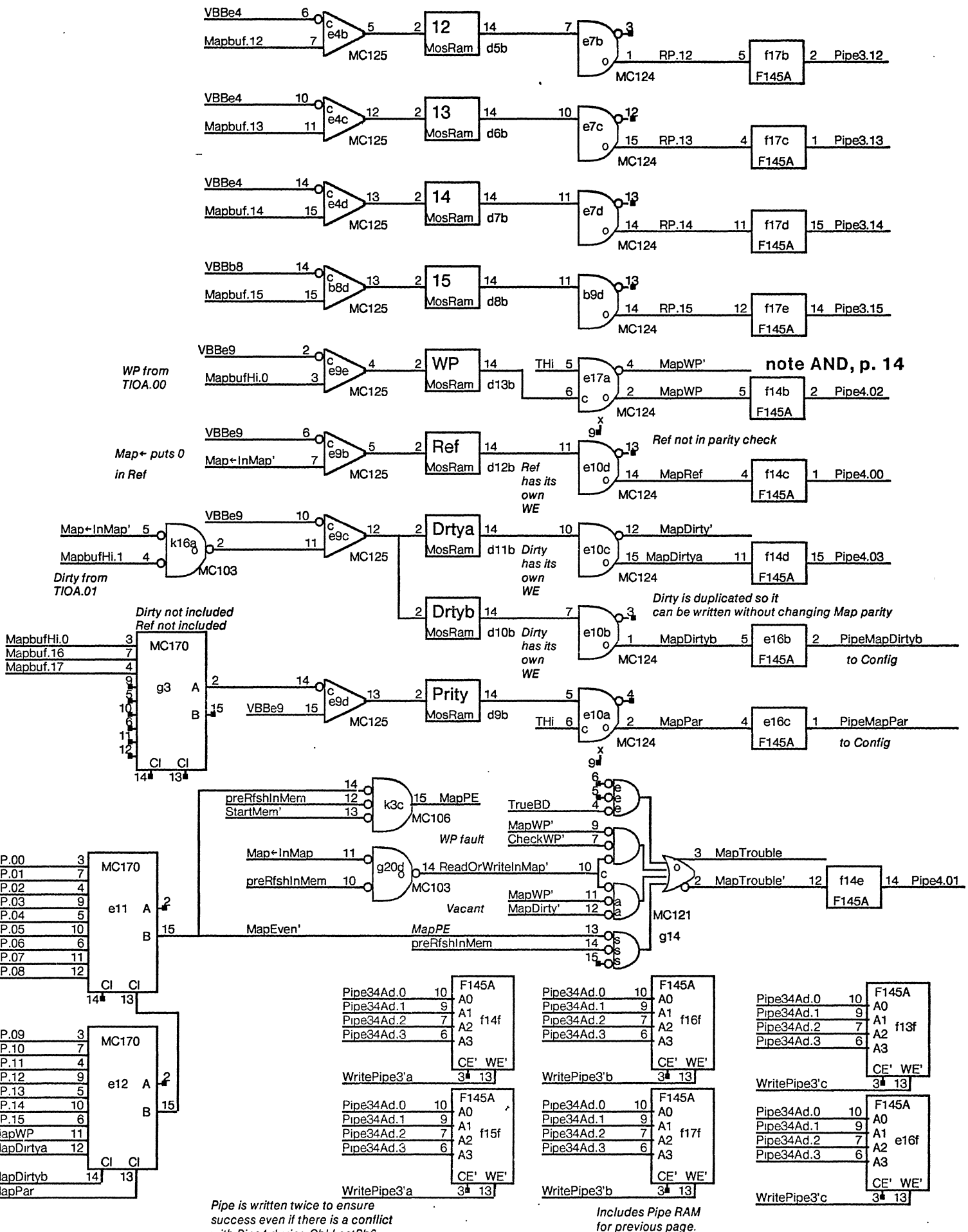
from C board

Real memory is always contiguous, and RP bits which select the module shift left as storage chips grow, thus:

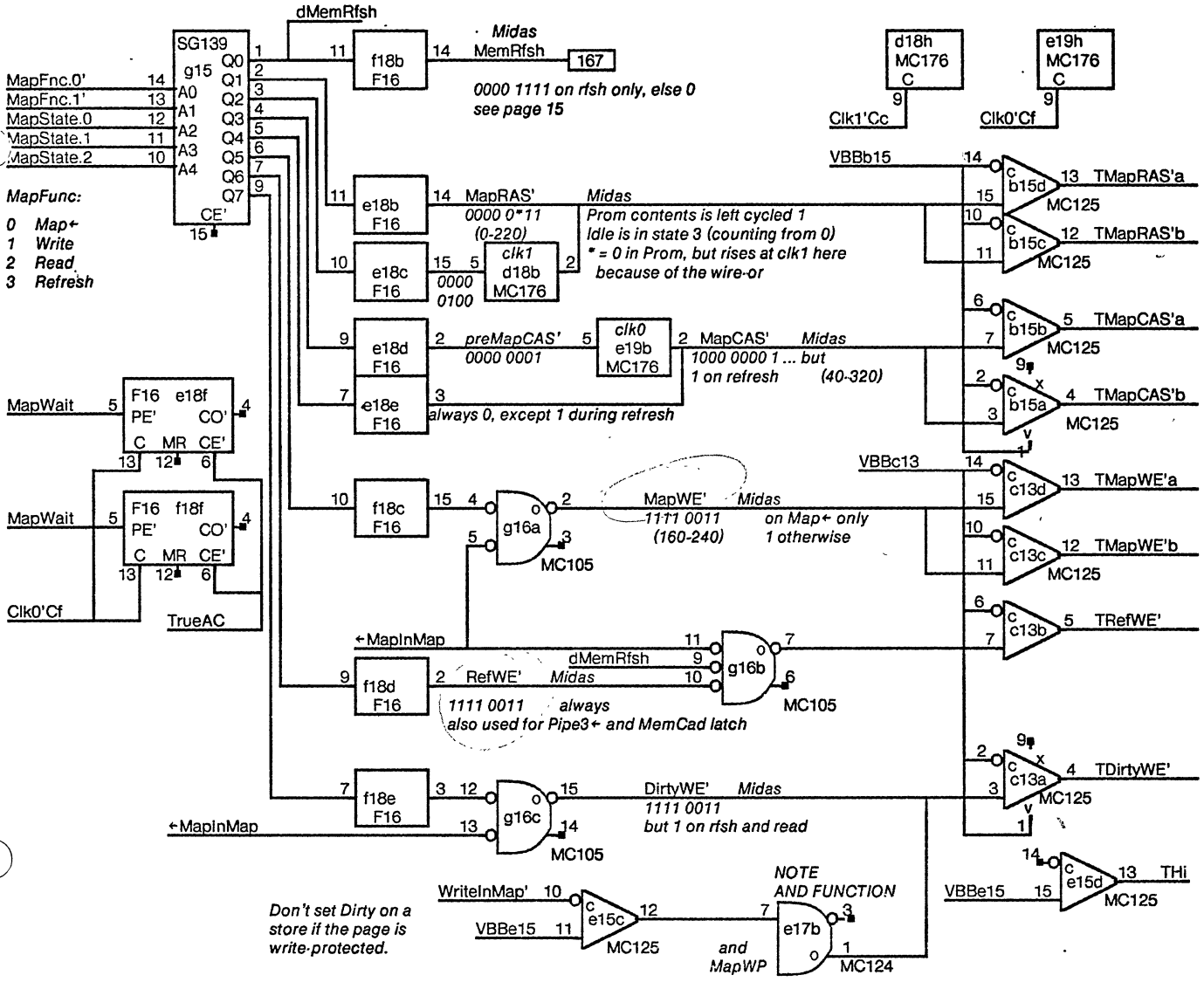
XEROX PARC	Project: Dorado	Memory Extension Board Map RP 00-11	File: MemX12.sil	Designer: K. Pier	Rev: Cg	Date: 7/03/79	Page: 12

RP

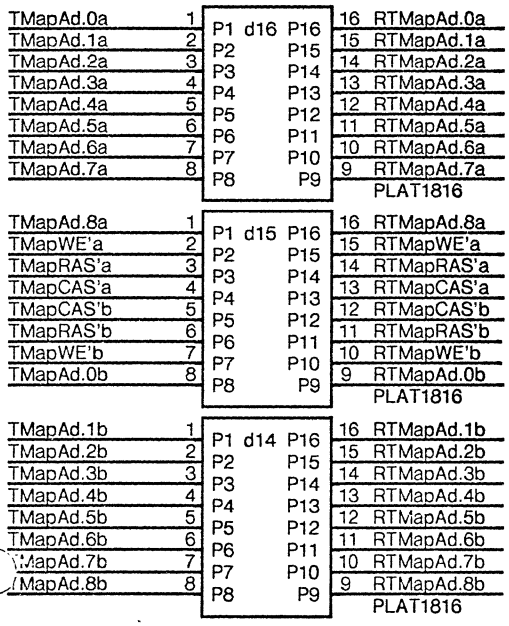
PIPE 3



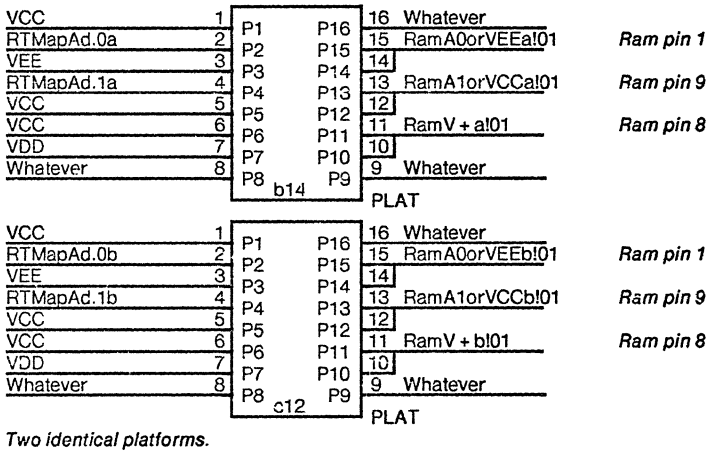
XEROX PARC	Project: Dorado	Memory Extension Board Map RP12-15 and Other	File: MemX13.sil	Designer: K. Pier	Rev: Cg	Date: 7/03/79	Page: 13

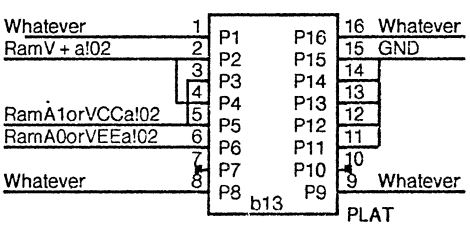


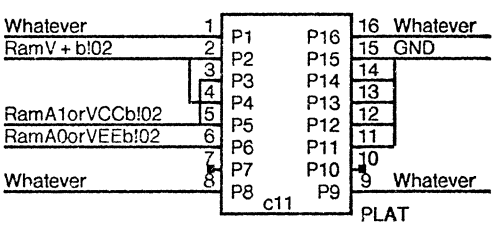
PLATS are BECKMAN 898-3-R027 series resistors 8 per chip



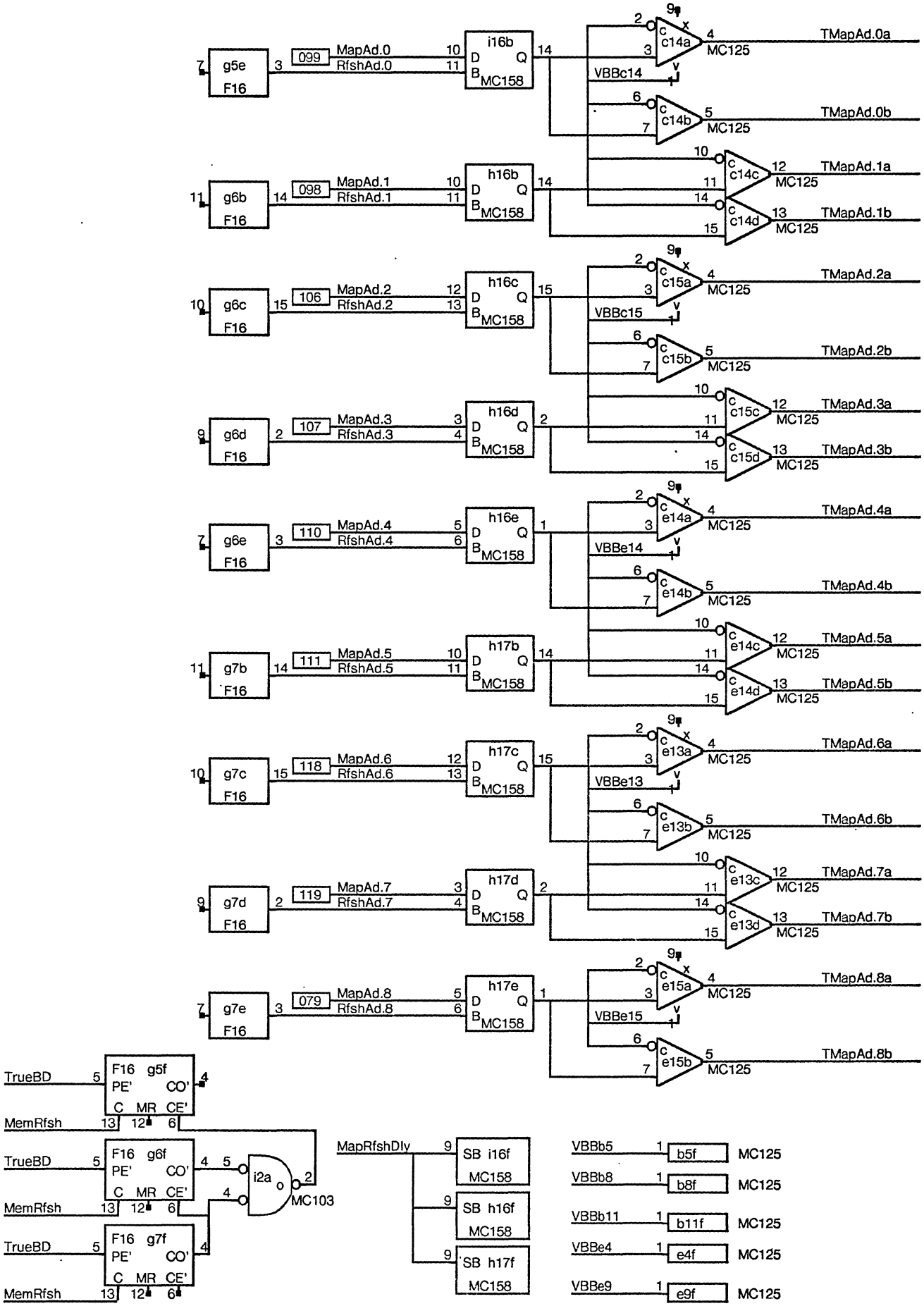
PLATS are Jumper wires for configuration





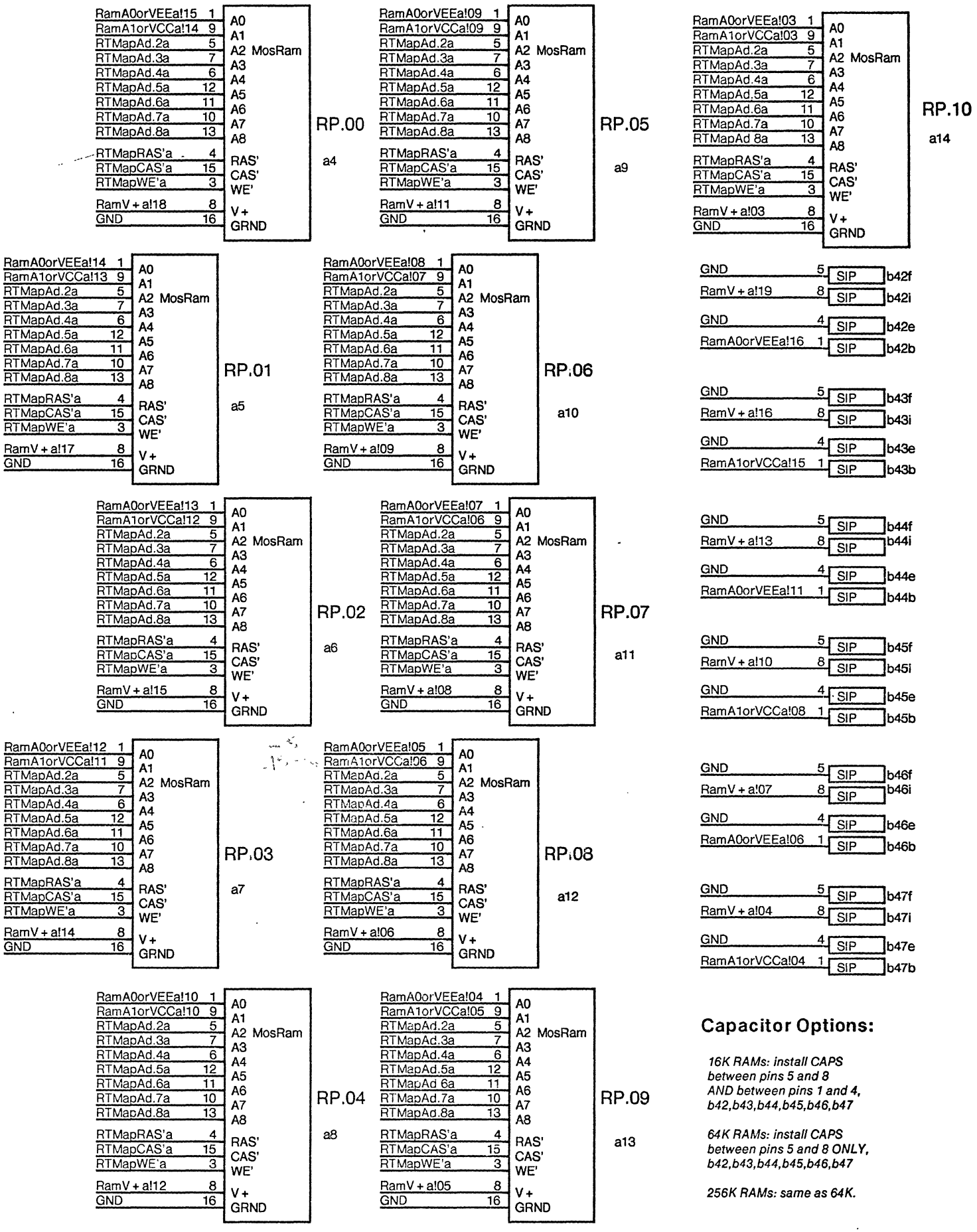


XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado	Memory Extension Board Map address and control	MemX14.sil	K. Pier	Cg	10/29/79	14



0000 1111 on rfsh only, else 0

XEROX PARC	Project: Dorado	Memory Extension Board Map address and control	File: MemX15.sil	Designer: K. Pier	Rev: Cg	Date: 7/03/79	Page: 15

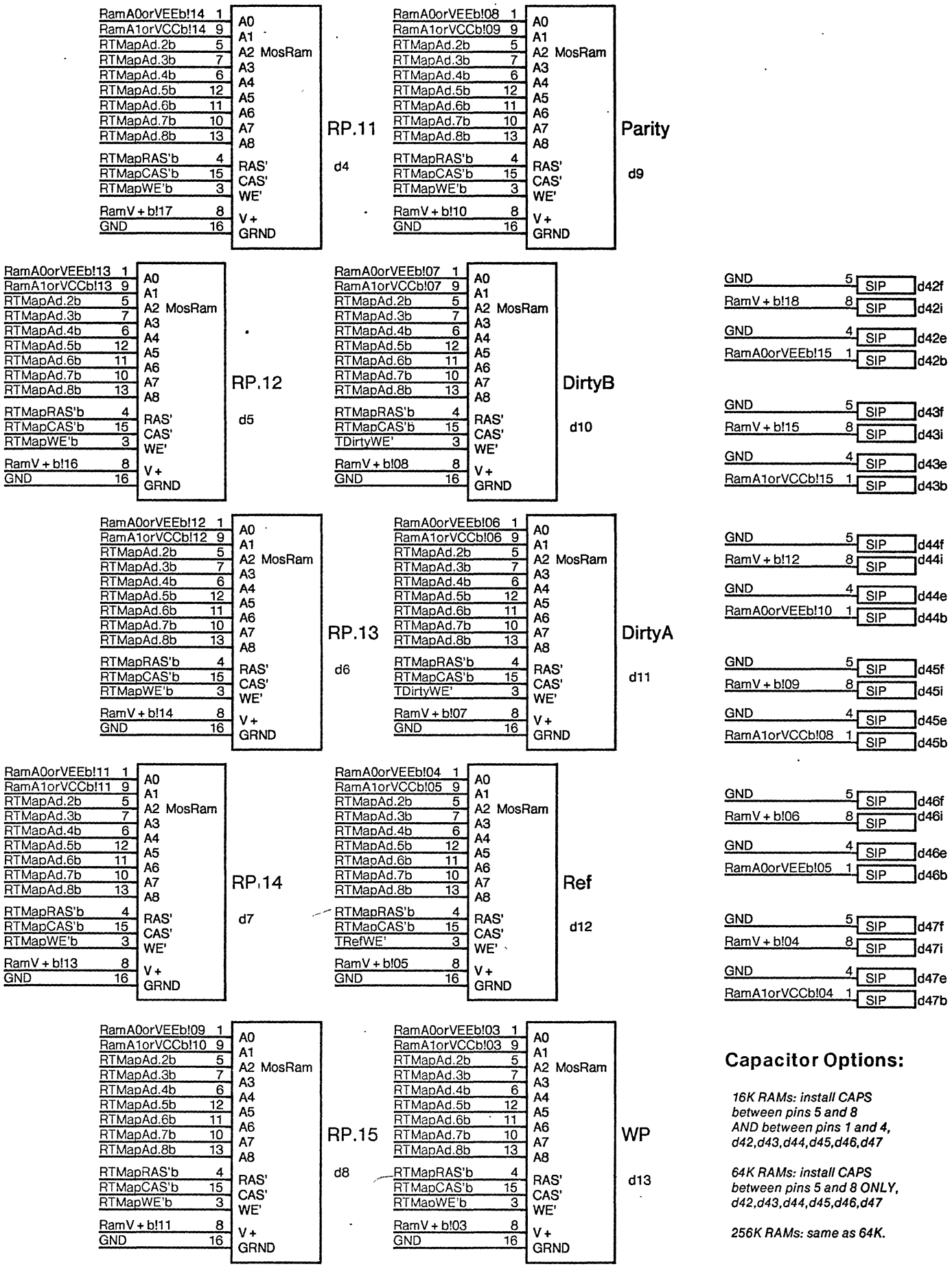


Capacitor Options:

16K RAMs: install CAPS between pins 5 and 8 AND between pins 1 and 4, b42,b43,b44,b45,b46,b47

64K RAMs: install CAPS between pins 5 and 8 ONLY, b42,b43,b44,b45,b46,b47

256K RAMs: same as 64K.



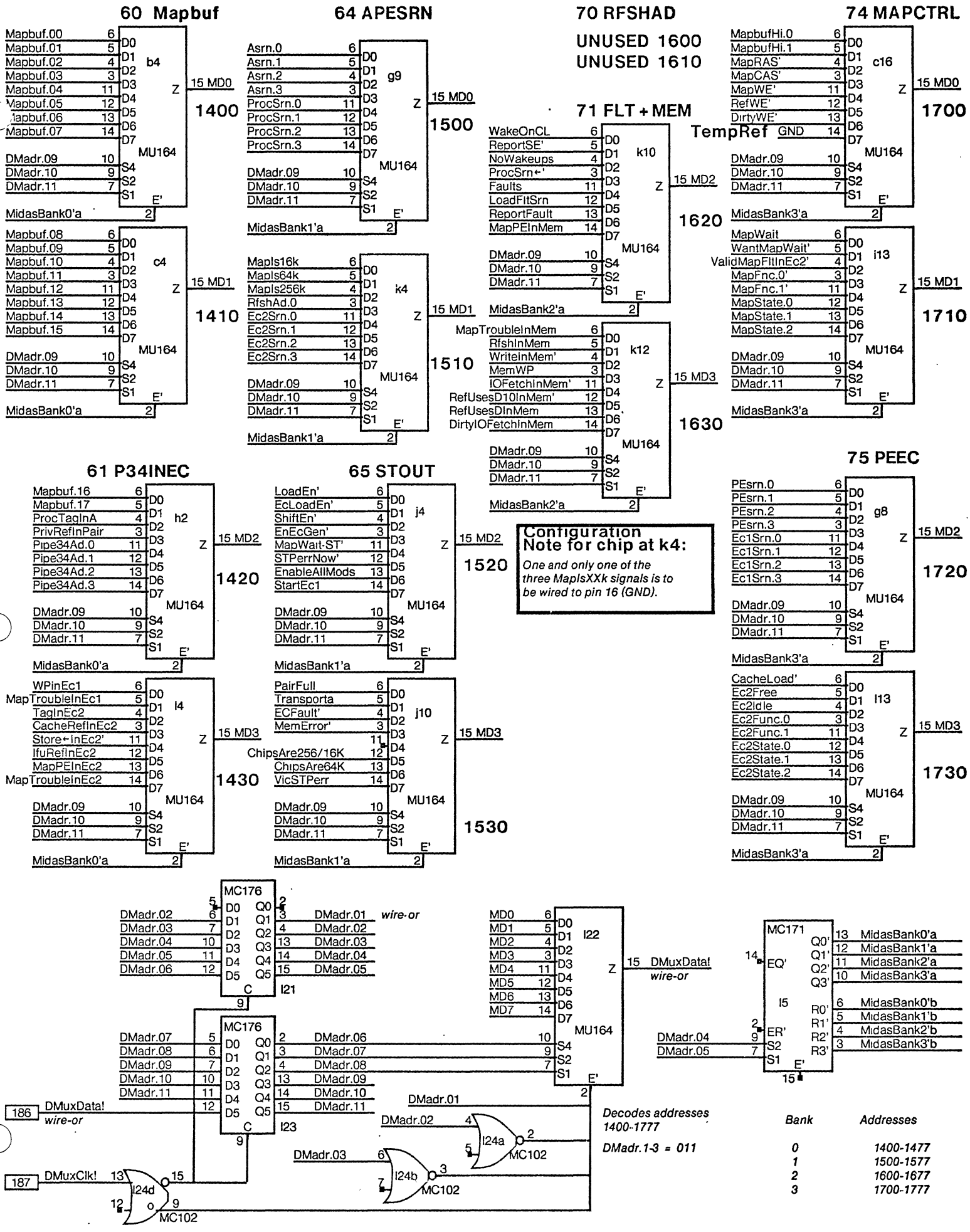
Capacitor Options:

16K RAMs: install CAPS between pins 5 and 8 AND between pins 1 and 4, d42,d43,d44,d45,d46,d47

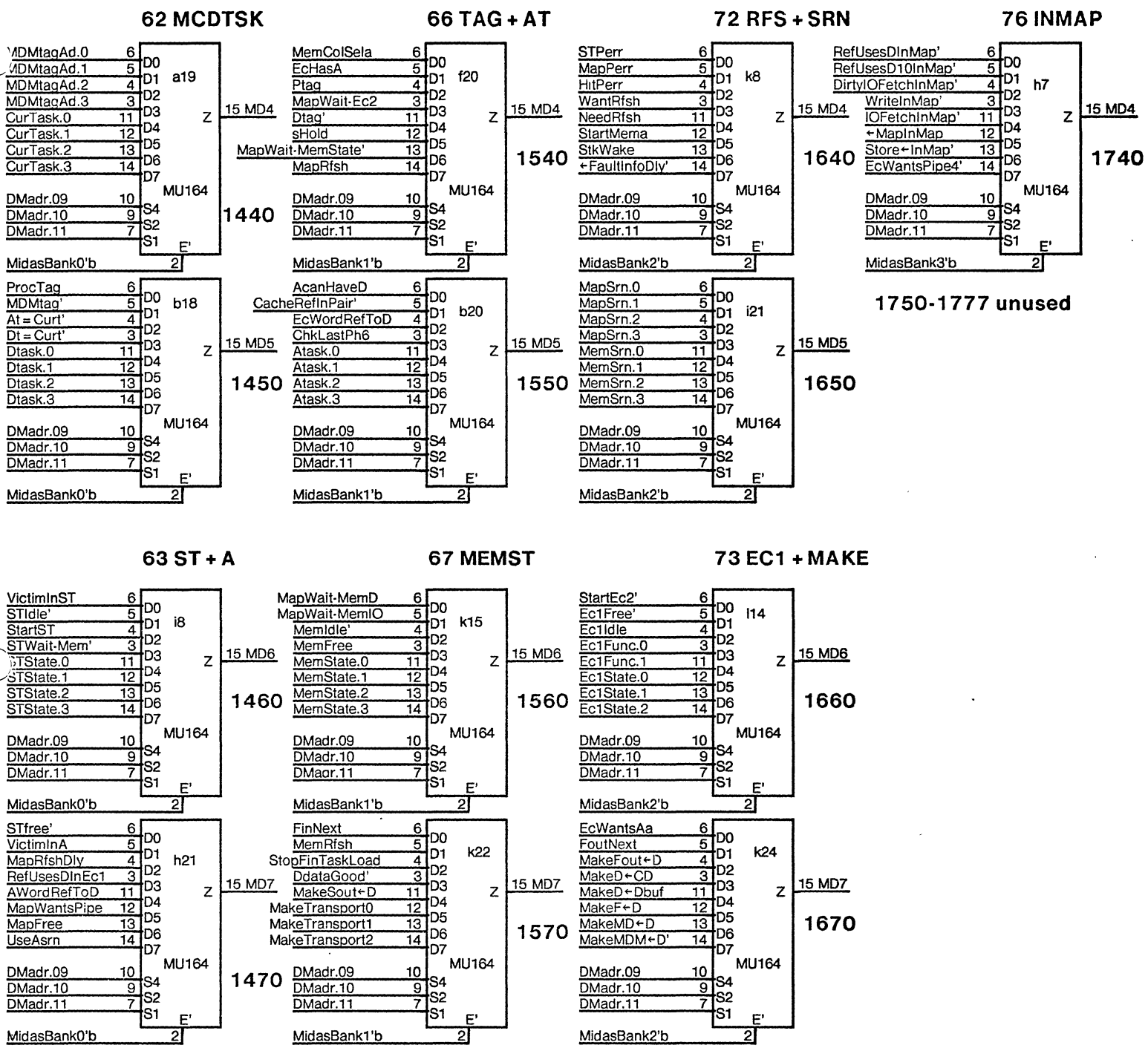
64K RAMs: install CAPS between pins 5 and 8 ONLY, d42,d43,d44,d45,d46,d47

256K RAMs: same as 64K.

XEROX PARC	Project: Dorado	Memory Extension Board Map RAM chips	File: MemX17.sil	Designer: K. Pier	Rev: Cg	Date: 10/29/79	Page: 17

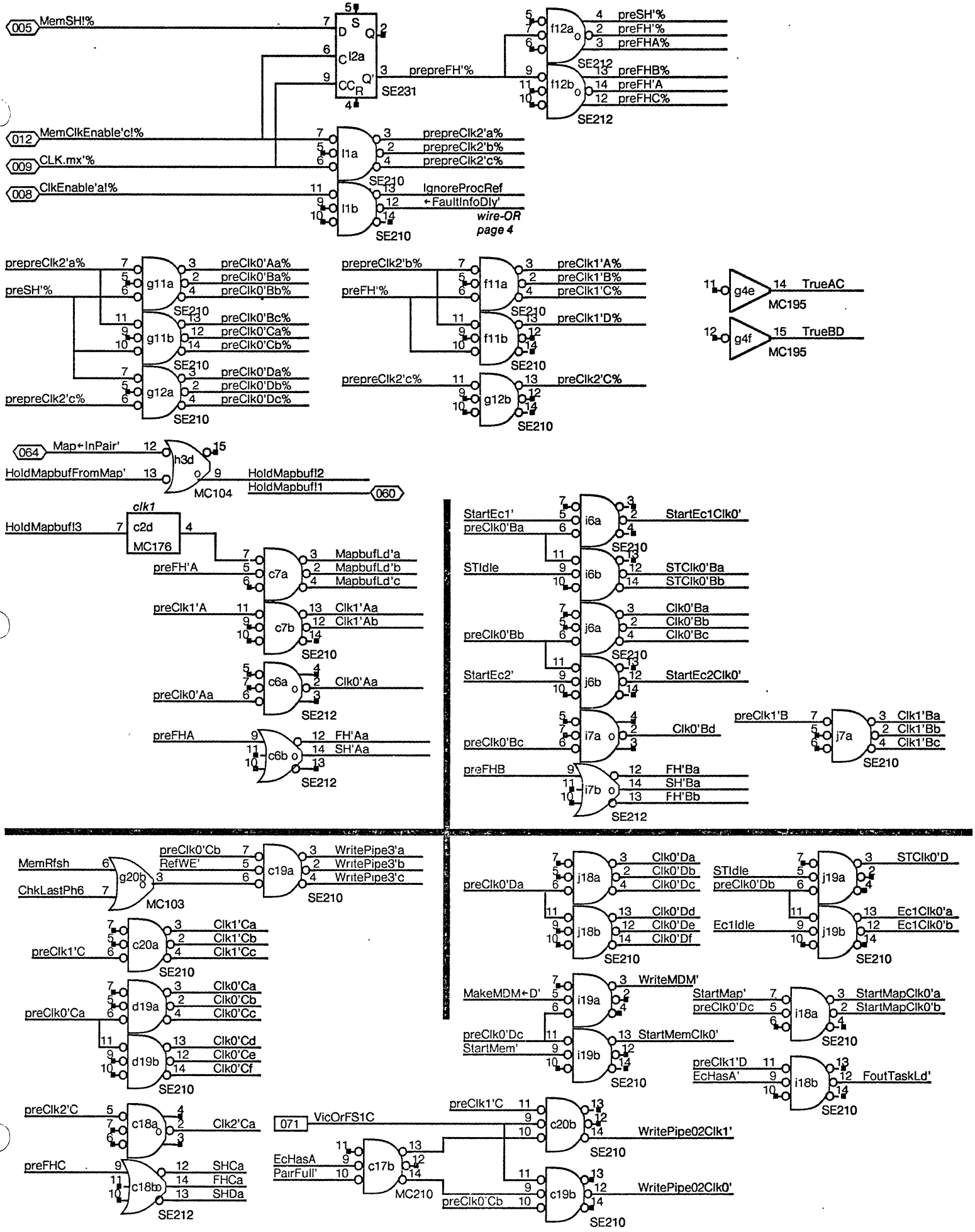


XEROX PARC	Project: Dorado	Memory Extension Board Midas Interface	File: MemX18.sil	Designer: K. Pier	Rev: Cg	Date: 7/19/79	Page: 18



Bank	Addresses
0	1400-1477
1	1500-1577
2	1600-1677
3	1700-1777

XEROX PARC	Project	File	Designer	Rev	Date	Page
	Dorado Memory Extension Board Midas Interface	MemX19.sil	K. Pier	Cg	7/03/79	19



XEROX PARC	Project: Dorado	Memory Extension Board Clock Logic	File: MemX20.sil	Designer: K. Pier	Rev: Cg	Date: 7/03/79	Page: 20

	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	
1	BmuxDrivr 0-1	Mapbuf 0-1-8-9	RAS-CAS A,7	Mapbuf 2-3-4-10 11-12	BmuxDrivr 12-13	Mapbuf 5-6-7-13 14-15	Mapbuf 16,17	BMuxEn 11,11	ErrorRcvr 4,4,10,D	ModSinEn	HOLDCntr	ppclk/IPR	1
41	174 11	175 11	231	175 11	174 11	175	175 11	109	104	F16 9	F16 8	210 20	
2	BNTGtCT a,4,c,8	BmuxDrivr 8-9	CAS-WE clk1 7,8,20 11,11,,	BmuxDrivr 4-5	BmuxDrivr 6-7	BmuxDrivr 14-15	BMxSel	MU	ShiftInEven 15,9,5.5	STOut 5,5,10,10	HOLDCntr	Clock	2
	102	174 11	176	174 11	174 11	174 11	103 11	P34INEC	103	102	F16 8	231 20	
3	ModEn	SHIFTS LOADS 5,5,5,5	BmuxDrivr 10-11	BmuxDrivr 2-3	ModDcode	ModEna	ParityIn	3,3,10,20	clk1 8,4,5,6,5,,	clk0 8,8,10, 4,4,5	A,5,13	Ec2AuIn	3
42	F16 7	103	174 11	174 11	171 7	F16 7	170 13	104	176	176	106	176 10	
4	0	MU Mapbuf	MU Mapbuf	11	IN 125 13	MCR F16 11	10,10,9, 20,20,4 195	dPipe34Ad 174 3	dPipe34Ad 174 3	MU STOUT	MU MAPEC2	MU P34INEC	4
5	1	IN		12	Mod 174 8	A,11,C 105	RfshCnt F16 15	Pipe34Ad 141 3	STOut 176 5	4,7,11 11,4,4 195	FaultSrn F16 3	MidasBank 171 16	5
43		125 12											
6	2	OUT 124 12	CLK 212 20	13			RfshCnt F16 15	ProcSrn 141 3	CLK 210 20	CLK 210 20	EcSrn = 0 Fsrn = 0 109 3,3	10,10,10 105	6
7	3		CLK 210 20	14	OUT 124 13		RfshCnt F16 15	MU INMAP	CLK 212 20	CLK 20,B 210	ReportFlt 121 3	Ec1AuIn 176 9	7
44													
8	4	IN 125 13		15			MU PEEC	MemPE F00 4	MU ST + A	srn0,Wrfsh 135 3,4	MU RFS + SRN	Ec1Func 117 9	8
9	5	OUT		PAR	IN 125 12		MU APESRN	Ec1Srn 141 3	Ec2Srn 141 3	LdFltCnt NeedRfsh 117 3,4	FaultCnt F16 3		9
45													
10	6			DTYb	OUT 124 12		A,8,8,5 104	PEsrn 158 3	MemAuOut F16 7	MU STOUT	MU FLT + MEM	Ec2Func F16 10	10
11	7	IN 125 12	PLAT BYPASS	DTYa	PARITY 170 13	CLK 210 20	CLK 210 20	STProm 139 4	7,7,7 105	MemAuIn 176 7	7,7,9 10,10,10 195	Ec2Prom 139 10	11
46													
12	8	OUT 124 12	PLAT SWITCH	REF	PARITY 170 13	CLK 212 20	CLK 210 20	STState F16 5	STProm 139 5	MemAuOut F16 7	MU FLT + MEM	Ec1Prom 139 9	12
13	9	PLAT BYPASS	WE 125 14	WP	ADDR 125 15	Pipe34 145 13	CheckWP 6,6,6,7 104	MapAu 7,B,6,6 103	MU MAPCTRL	MemProm 139 7	MemAuIn 176 7	MU PEEC	13
47													
14	10	PLAT SWITCH	ADDR 125 15	RESISTOR 14	ADDR 125 15	Pipe34 145 12	MapTrbl 121 13	MapAuIn 176 6	MapProm 139 6	MemProm 139 7	clk0 7,7,,,,, 176	MU EC1 + MAKE	14
15		RasCas 125 14	ADDR 125 15	RESISTOR 14	ADDR 15,15,14 125 14	Pipe34 145 12	MapProm 139 14	MapState F16 6	MapAuIn 176 6	STIdle MapWait 117 7,5	MU MEMST		15
48													
16			MU MAPCTRL	RESISTOR 14	Pipe34 145 13	Pipe34 145 12	←Map 105 14	MapAdMux 158 15	MapAdMux 158 15	MemState F16 7	13,10,5,9 103	Ec2State F16 10	16
17	Pair 2,,, F16		ASRNInc 3,20 210		OUT 124 13	Pipe34 145 13		MapAdMux 158 15	MapWait 121 6	VicSTPerr 10,9,C,4 104	Ec1State F16 9	6,10,10 104 10	17
49													
18	CurTask 141 2	MU MCDTSK	CLK 212 20	clk1 14,12,, 176 ,,,	MapRCW F16 14	MapRCW F16 14	MemCad 173 12	MemSrn 141 3	CLK 210 20	CLK 210 20	VicInSt MapWaitD 109 6,9	1,1,9,6 104	18
19	MU MCDTSK	TrueNext 158 2	CLK 210 20	CLK 210 20	clk0 14,1,1,4 176 f,g	ASRN F16 3	MemCad 173 12	StartST 121 5	CLK 210 20	CLK 210 20	104 10	clk0 5*10,9 176	19
50													
20	EMUorFT a,1,1,1 113	MU TAG + AT	CLK 210 20	Tag211 211 1,B	ProcTag F145	MU TAG + AT	12,20,C, 103 13	A,4,4 105	MapAu 104 6	Ec1AuOut 176 9	Ec1AuOut 176 9	10,9,9 9,6,1 195	20
21	Atask F16 2	Dt = Ct 113 1	PipeTask Pipe2 F145 2	PipeTaska 197 2	PipeSubT Pipe2 F145 2	MDMTag F145 1	dMDMad 159 1	MU ST + A	MU RFS + SRN	Ec2AuOut F16 10	Ec2AuOut F16 10	Midas 176 18	21
51													
22	dMDMtagAd 158 1	At = Ct 113 1	FinTask F16 2	MDMtagAd 141 1	DTask F16 2	MakeMD←D 117 1	dMDMad 100 1	MapSRN 141 3	STOut 176 5	MapAUOut F16 6	MU MEMST	Midas 164 18	22
23	ASubTask 2,2,1,1 F16	CurSubT 2,2,d,e 141	RptCur 4,4,4,1 1662	MemAd 0 159 12	CAS-WE 1,7,8,4,5,4 176 clk1	1,6,1,D 103	clk0 1,3,11,e 176 5,5	dPipe02Ad 158 3	Hit 1,1,1 105	Transport 212 5,5	5,B,1,5 102	Midas 176 18	23
52													
24	bNext 1,1,1,1,,, 197	FinSubT 2,2,d,e F16	HOLD 1660 4	MemAd 1-4 159 12	RAS-CAS A,7 231	CacheRef 1,1,4 1674	Page1 4.1,2 105	Pipe02Ad 141 3	MemAd 5-8 159 12	FoutTask 176 2	MU EC1 + MAKE	Midas 18,18, 102 C 18	24
C	a 11	b 26	c 39	d 55	e 70	f 86	99 g	114 h	129 i	143 j	159 k	174 l	D

XEROX PARC	Project Dorado	Reference MemX Board Layout	File MemX21.sil	Designer K. Pier	Rev Cg	Date 10/29/79	Page 21

Location h11

Q	ST ADDR / STATE	11 cycles IO Store 0-13 012345678910	14-17 11	12 cycles VictimStore 20-33 01234567891011	34-37
1	prepreLoadEn'	00000001110	0 1	00000000111 1	1
	preEcLoadEn'	10101010111	1 1	11010101011 1	1
2	preShiftEn'	00000001111	1 1	10000000111 1	1
3	preEnEcGen'	11111111110	0 1	01111111111 1	1
4	preMapWait-ST'	00001111110	0 1	00000111111 0	1
5	preSTfree'	11111111101	1 1	11111111110 1	1
6	prepreSTPerrNow'	00000000111	1 1	10000000011 1	1
7	preStopFinTaskLd	11111100001	1 0	11111111000 0	0

Location i12

0	preFinNext	11111110001	1 0	00000000000 0	0
5	preMakeSout←D	00000000000	0 0	11111111000 0	0
6	PreMakeTrnspt0	00000000000	0 0	11111110000 1	0

Location i14

Q	MAP ADDR / STATE	Refresh 0-7 01234567	Read 10-17 01234567	Write 20-27 01234567	Map write 30-37 01234567
0	prepreRfshInMem	00010000	00000000	00000000	00000000
1	UNUSED				
2	preStartMem'	11101111	11101111	11101111	11111111
3	preStartMem	00010000	00010000	00010000	00000000
4	preMapFree'	11111101	11111101	11111101	11111101
5	preMapWantsPipe	00000000	00110000	00110000	00110000

IDENTICAL

Location g15

Q	MAP ADDR / STATE	Refresh 0-7 01234567	Read 10-17 01234567	Write 20-27 01234567	Map Write 30-37 01234567
0	preMemRfsh	00011110	00000000	00000000	00000000
1	preRAS1'	00000110	00000110	00000110	00000110
2	preRAS2'	00001000	00001000	00001000	00001000
3	prepreCAS1'	11111110	00000010	00000010	00000010
4	prepreCAS2'	11111100	00000000	00000000	00000000
5	preMapWE'	11111111	11111111	11111111	11100111
6	preRefWE'	11100111	11100111	11100111	11100111
7	preDirtyWE'	11111111	11111111	11100111	11100111

Location j13

Q	MEM 16K chips ADDR / STATE	READ 0-7 01234567	WRITE 0-7 01234567	10-17	REFRESH 20-27 01234567	30-37
0	prepreMemWE'	10011111	10011111	1	11111111	1
1	preSTWait-Mem'	10111111	10111111	1	11111111	1
2	prepreMemCAS	11111100	11111100	0	00000000	0
3	prepreShiftLoadEven	00010000	00010000	0	00000000	0
4	prepreMCS	11111000	11111000	0	00000000	0
5	preMemFree	00000010	00000010	0	00000010	0
6	preMemState6'	11111011	11111011	1	11111011	1
7	preMemRAS	11110001	11110001	1	11110001	1

IDENTICAL

Location j14

Q	MEM 4K chips ADDR / STATE	READ 0-14 0123456789	10	11	12	15-17 13-15	WRITE 0123456789	10	11	12	13-15	REFRESH 20-34 0123456789	10	11	12	35-37 13-15
0	prepreMemWE'	1100000111	1	1	1	1	1100000111	1	1	1	1	1111111111	1	1	1	1
1	preSTWait-Mem'	1111101111	1	1	1	1	1111101111	1	1	1	1	1111111111	1	1	1	1
2	prepreMemCAS	0001111100	0	0	0	0	0001111100	0	0	0	0	0001111100	0	0	0	0
3	prepreShiftLoadEven	0000000100	0	0	0	0	0000000100	0	0	0	0	0000000000	0	0	0	0
4	prepreMCS	0111111000	0	0	0	0	0111111000	0	0	0	0	0000000000	0	0	0	0
5	preMemFree	0000000000	0	1	0	1	0000000000	0	1	0	1	0000000000	0	1	0	1
6	prepreState7'	1111111111	1	1	1	1	1111111111	1	1	1	1	1111111111	1	1	1	1
7	preMemRAS	1111111100	0	0	1	0	1111111100	0	0	1	0	1111111100	0	0	1	0

OBSOLETE

IDENTICAL

Location l12

Q	EC1 ADDR / STATE	Write 0-7 01234567	CacheLoad 10-17 01234567	Clean or Miss IOfetch 20-27 01234567	Dirty Hit IOfetch 30-37 01234567
0	preEcEn'	01111111	01111111	01111111	01111111
1	preMakeTrspt2	00000000	00111100	00000000	00111100
2	preMakeFcut←D	00000000	00000000	00000000	00011100
3	preFoutNext	00000000	00000000	00011100	00001100
4	preMakeD←CD	00000000	00111100	00000000	00000000
5	preEcWantsA	01000000	01000000	01000000	01000000
6	preEc1Free'	11111101	11111101	11111101	11111101
7	preStartEc2'	11111011	11111011	11111011	11111011

Location l11

Q	EC2 ADDR / STATE	Write 0-7 01234567	CacheLoad 10-17 01234567	CLEAN or Miss IOfetch 20-27 01234567	Dirty Hit IOfetch 30-37 01234567
0	prepreMakeTnspt1	00000000	11100001	00000000	11100001
1	preMakeFout←D	00000000	00000000	00000000	11110001
2	preFoutNext	00000000	00000000	11110001	11111001
3	preMakeD←CD	00000000	11100001	00000000	00000000
4	preEc2Free	00000010	00000010	00000010	00000010
5	preEcWantsPipe4	10000000	10000000	10000000	10000000
6	preMapWait-Ec2	00000000	11110001	00000000	11110001
7	CacheLoad'	11111111	00000010	11111111	11111111

XEROX PARC	Project: Dorado	Reference: Automata program tables	File: Memx22.sil	Designer: K. Pier	Rev: Cg	Date: 9/08/79	Page: 22

Dorado Memory Extension Board
Stuffing and Configuration Instructions

1. If 256 chips are NOT installed in the Memory Storage Arrays (MSA), then

a. Break g10.6 (MC104) before stuffing. Label this chip as MemX-g10.

2. Break h20.10 before stuffing. Label this chip as MemX-h20.
All SG10139 chips are PROMS which must be blown and labeled before stuffing.
Stuff all PLAT1816 with Beckman type 898-3-R27 resistor packs or equivalent.
↳ D14, 15, 16

3. Do all the actions in one of the following three columns:

Action	16K Map Chips	64K Map Chips	256K Map Chips
Blue Wire	k4.6 to k4.16	k4.5 to k4.16	k4.4 to k4.16
Stuff into MosRam sockets	MK4116-2 or equivalent	TMS4156 or equivalent	256K Ram or equivalent
Jumper wires in socket b14	3 to 14 5 to 12 7 to 10	6 to 11 4 to 13	6 to 11 4 to 13 2 to 15
Jumper wires in socket c12	3 to 14 5 to 12 7 to 10	6 to 11 4 to 13	6 to 11 4 to 13 2 to 15
capacitors in SIP sockets b42,b43,b44,b45,b46,b47 d42,d43,d44,d45,d46,d47	0.1 mmf pins 5 to 8 each socket AND 0.1 mmf pins 1 to 4 each socket	0.1 mmf pins 5 to 8 each socket	0.1 mmf pins 5 to 8 each socket
1 KOhm resistor in socket b14 and 1 KOhm resistor in socket c12	NO	1 to 15 IF Ram has self refresh feature-Motorola or equivalent	NO
22 uf Cap in PLAT c11 & b13	+ 2 to 15 +4 to 14 +11 to 6	+ 3 to 14 + 5 to 12	+ 3 to 14 + 5 to 12

Page Numbers: Yes First Page: 1
Columns: 2 Edge Margin: .8" Between Columns: .0"
Heading:
MemX-Rev-Cg.ps
COMPONENTS:

F00:	4					
F145A:	1	2	12	13		
F16:	1	2	3	5	6	7
	8	9	10	11	14	15
MC100:	1					
MC102:	1	4	5	8	10	18
MC103:	1	5	6	7	9	10
	11	12	13	15	20	
MC104:	1	3	4	5	6	7
	8	9	10	20		
MC105:	1	2	4	7	10	11
	14					
MC106:	5	13				
MC109:	3	6	9	11		
MC113:	1	2				
MC117:	1	3	4	5	7	9
MC121:	3	5	6	13		
MC124:	12	13	14			
MC125:	12	13	14	15		
MC135:	3	4				
MC141:	1	2	3			
MC158:	1	2	3	15		
MC159:	1	12				
MC1660:	4					
MC1662:	1	4				
MC1674:	1	4				
MC170:	13					
MC171:	7	18				
MC173:	12					
MC174:	3	8	11			
MC175:	11					
MC176:	1	2	3	4	5	6
	7	8	9	10	11	12
	14	18	20			
MC195:	1	4	6	7	9	10
	11	20				
MC197:	2					
MC210:	3	20				
MC211:	1					
MC212:	5					
MC231:	7					
MosRam:	12	13	16	17		
MU164:	18	19				
PLAT:	14					
PLAT1816:	14					
SE210:	20					
SE212:	20					
SE231:	20					
SG139:	5	6	7	9	10	14
SIP:	16	17				
SPARE:	8					

SIGNAL NAMES:

+:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)				
AcanHaveD:	1(1)	5(1)	19(1)			
AcanHaveD':	1(1)	2(1)	5(1)			
AcanhaveMap':	4(1)					
AfreeOrEc'b:	1(1)					
Asrn.0:	3(1)	11(1)	18(1)			
Asrn.1:	3(1)	11(1)	18(1)			
Asrn.2:	3(1)	11(1)	18(1)			
Asrn.3:	3(1)	11(1)	18(1)			
Asubtask.0:	2(1)					
Asubtask.1:	2(1)					
At=Curt':	1(2)	19(1)				

```
Atask.0:          1(1)    2(1)   19(1)
Atask.1:          1(1)    2(1)   19(1)
Atask.2:          1(1)    2(1)   19(1)
Atask.3:          1(1)    2(1)   19(1)
AwantsDifHit':    6(1)
AWordRefToD:      1(1)   19(1)
AWordRefToD':     1(1)
bHit':            1(2)
BMux.00:         11(1)
BMux.00!:        11(1)
BMux.01:         11(1)
BMux.01!:        11(1)
BMux.02:         11(1)
BMux.02!:        11(1)
BMux.03:         11(1)
BMux.03!:        11(1)
BMux.04:         11(1)
BMux.04!:        11(1)
BMux.05:         11(1)
BMux.05!:        11(1)
BMux.06:         11(1)
BMux.06!:        11(1)
BMux.07:         11(1)
BMux.07!:        11(1)
BMux.08:         11(1)
BMux.08!:        11(1)
BMux.09:         11(1)
BMux.09!:        11(1)
BMux.10:         11(1)
BMux.10!:        11(1)
BMux.11:         11(1)
BMux.11!:        11(1)
BMux.12:         11(1)
BMux.12!:        11(1)
BMux.13:         11(1)
BMux.13!:        11(1)
BMux.14:         11(1)
BMux.14!:        11(1)
BMux.15:         11(1)
BMux.15!:        11(1)
BMux.16!:        11(1)
BMux.17!:        11(1)
BMuxS1.0-7:      11(4)
BMuxS1.0-7%:     11(1)
BMuxS1.8-15:     11(4)
BMuxS1.8-15%:    11(1)
BMuxS2.0-7:      11(4)
BMuxS2.0-7%:     11(1)
BMuxS2.8-15:     11(4)
BMuxS2.8-15%:    11(1)
bNext.0:          1(1)    2(2)
bNext.1:          1(1)    2(2)
bNext.2:          1(1)    2(2)
bNext.3:          1(1)    2(2)
BNTGtCT'a!:       4(1)
BNTGtCTASK:       4(1)
CacheLoad':       3(1)   10(1)   18(1)
CacheRef:         1(2)
CacheRef':        1(1)
CacheRefInEc1:   10(1)
CacheRefInEc2:   10(4)   18(1)
CacheRefInPair':          1(2)   19(1)
CheckWP':         6(1)   13(1)
ChipsAre256/16K:          8(2)   11(1)   18(1)
ChipsAre64K:      8(1)   18(1)
ChkLastPh6:      10(1)   19(1)   20(1)
ChkLastPh6':      3(3)   10(2)
CLK.mx'%:        20(1)
Clk0'Aa:          7(1)   20(1)
Clk0'Ba:          3(1)    7(2)   20(1)
Clk0'Bb:          3(2)   10(1)   20(1)
Clk0'Bc:          8(1)    9(1)   20(1)
Clk0'Bd:          3(3)    4(1)   20(1)
Clk0'Ca:          7(1)   20(1)
Clk0'Cb:          1(1)    2(1)   20(1)
Clk0'Cc:          2(3)   20(1)
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```
Clk0'Cd:          2(2)   20(1)
Clk0'Ce:          1(1)    3(1)   20(1)
Clk0'Cf:         14(2)   20(1)
Clk0'Da:          3(2)   20(1)
Clk0'Db:          3(1)    6(1)   20(1)
Clk0'Dc:          6(1)   10(1)   20(1)
Clk0'Dd:          7(2)   20(1)
Clk0'De:         10(2)   20(1)
Clk0'Df:         10(1)   20(1)
Clk1'Aa:          7(2)   20(1)
Clk1'Ab:          7(1)   11(1)   20(1)
Clk1'Ba:          3(1)   20(1)
Clk1'Bb:          8(1)   20(1)
Clk1'Bc:          8(1)   20(1)
Clk1'Ca:          2(1)   20(1)
Clk1'Cb:          1(1)   20(1)
Clk1'Cc:         14(1)   20(1)
Clk2'Ca:          1(1)   20(1)
ClkEnable'a!%:   20(1)
CountMiss:       10(1)
CurTask.0:        1(4)    2(1)   19(1)
CurTask.0%:       2(1)
CurTask.1:        1(4)    2(1)   19(1)
CurTask.1%:       2(1)
CurTask.2:        1(4)    2(1)   19(1)
CurTask.2%:       2(1)
CurTask.3:        1(4)    2(1)   19(1)
CurTask.3%:       2(1)
DcomingForCt':    1(1)
DdataGood':       1(1)   19(1)
dHitPerr:         4(1)
DirtyIoFetchInA':          6(1)
DirtyIOFetchInMap':        6(1)    7(1)   19(1)
DirtyIOFetchInMem:         7(1)    9(2)   18(1)
DirtyIOFetchInMem':        7(1)    9(1)
DirtyWE':        14(1)   18(1)
DisHold:          5(1)    6(1)
dLoadSinE:        7(1)    8(1)
DMadr.01:        18(2)
DMadr.02:        18(3)
DMadr.03:        18(3)
DMadr.04:        18(3)
DMadr.05:        18(3)
DMadr.06:        18(2)
DMadr.07:        18(2)
DMadr.08:        18(2)
DMadr.09:        18(16)  19(13)
DMadr.10:        18(16)  19(13)
DMadr.11:        18(16)  19(13)
dMakeD←CD:        9(2)   10(1)
dMapbufHi.0:     11(2)
dMapbufHi.1:     11(2)
dMapFnc.0':       2(1)    6(1)
dMapFnc.1':       2(1)    6(1)
dMDMad.0':        1(1)
dMDMad.1':        1(1)
dMDMad.2':        1(1)
dMDMad.3':        1(1)
dMDpendOrRC:      1(1)    4(1)
dMemRfsh:        14(2)
DMuxClk!:        18(1)
DMuxData!:       18(2)
dPipe02Ad.0:      3(1)
dPipe02Ad.1:      3(1)
dPipe02Ad.2:      3(1)
dPipe02Ad.3:      3(1)
dPipe34Ad.0:      3(1)
dPipe34Ad.1:      3(1)
dPipe34Ad.2:      3(1)
dPipe34Ad.3:      3(1)
dSTPerr:          4(1)
Dt=Curt':         1(2)   19(1)
Dtag':            1(1)   19(1)
Dtask.0:          1(3)    2(1)   19(1)
Dtask.1:          1(3)    2(1)   19(1)
Dtask.2:          1(3)    2(1)   19(1)
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Dtask.3:          1(3)    2(1)   19(1)
Ec1Clk0'a:        9(1)   20(1)
Ec1Clk0'b:        9(1)   20(1)
Ec1Free':         9(3)   19(1)
Ec1Func.0:        9(2)   10(1)   19(1)
Ec1Func.1:        9(2)   10(1)   19(1)
Ec1Idle:          9(1)   19(1)   20(1)
Ec1Srn.0:         3(1)   18(1)
Ec1Srn.1:         3(1)   18(1)
Ec1Srn.2:         3(1)   18(1)
Ec1Srn.3:         3(1)   18(1)
Ec1State.0:       9(1)   19(1)
Ec1State.1:       9(1)   19(1)
Ec1State.2:       9(1)   19(1)
Ec2Free:         10(2)   18(1)
Ec2Func.0:       10(3)   18(1)
Ec2Func.1:       10(3)   18(1)
Ec2Func.1':      10(1)
Ec2Idle:         10(1)   18(1)
Ec2Srn.0:         3(4)   18(1)
Ec2Srn.1:         3(4)   18(1)
Ec2Srn.2:         3(4)   18(1)
Ec2Srn.3:         3(4)   18(1)
Ec2State.0:      10(1)   18(1)
Ec2State.1:      10(1)   18(1)
Ec2State.2:      10(1)   18(1)
Ec2State2:       10(2)
Ec2State3:       10(3)
Ec2State4:       10(2)
Ec2State5:       10(3)
EcDcomingForCt':          1(2)
ECFault:         10(1)
ECFault':         3(1)   10(1)   18(1)
EcHasA:           5(1)    9(1)   19(1)   20(1)
EcHasA':          9(2)   20(1)
EcKeepsAbusy:     1(1)
EcLoadEn':        5(3)   18(1)
EcWantsA:         3(1)    9(1)
EcWantsAa:        6(1)    9(2)   19(1)
EcWantsPipe4:     6(1)   10(2)
EcWantsPipe4':    3(2)   10(1)   19(1)
EcWordRefToD:     1(1)   10(1)   19(1)
EcWordRefToD':    1(1)   10(1)
EmuOrFT':         2(1)
EnableAllMods:    6(1)    7(1)   18(1)
EnableSTPerr:     4(1)    5(1)
EnEcGen':         5(2)   18(1)
ErrorsFromEc2:   10(2)
FaultCnt.0:       3(1)   11(2)
FaultCnt.1:       3(1)   11(2)
FaultCnt.2:       3(1)   11(2)
Faults:           3(2)   18(1)
FaultSrn.0:       3(1)   11(2)
FaultSrn.1:       3(1)   11(2)
FaultSrn.2:       3(1)   11(2)
FaultSrn.3:       3(1)   11(2)
FaultSrn=0':      3(2)
FH'Aa:            5(1)   20(1)
FH'Ba:            5(1)   20(1)
FH'Bb:            5(1)   20(1)
FHCa:             1(2)   20(1)
FinNext:          5(1)   19(1)
FinSubtask.0:     2(1)
FinSubtask.1:     2(1)
FinTask.0:        2(1)
FinTask.1:        2(1)
FinTask.2:        2(1)
FinTask.3:        2(1)
Fout.flt:        10(1)
FoutNext:         9(1)   10(1)   19(1)
FoutSubtask.0:    2(1)
FoutSubtask.1:    2(1)
FoutTask.0:       2(1)
FoutTask.1:       2(1)
FoutTask.2:       2(1)
FoutTask.3:       2(1)
```

```
FoutTaskLd':     2(1)   20(1)
GND:            14(2)   16(23)  17(22)  18(1)
Gnd:             1(1)    2(1)    3(1)    4(1)    5(1)    6(1)
                 7(1)    8(1)    9(1)   10(1)   11(1)   12(1)
                13(1)   14(1)   15(1)   16(1)   17(1)   18(1)
                19(1)   20(1)
Hita:            1(1)
HitPerr:         4(1)   19(1)
HoldDelayed:     4(1)    8(1)
HoldMapbuf!1:   20(1)
HoldMapbuf!2:   20(1)
HoldMapbuf!3:   20(1)
HoldMapbufFromMap':      6(1)   20(1)
IfuFaultInEc2:  10(1)
IfuRefInEc1:    10(1)
IfuRefInEc2:    10(4)   18(1)
IgnoreProcRef:   4(1)   20(1)
IoFetchInA':     6(1)
IOFetchInMap':   6(2)    7(1)   19(1)
IOFetchInMem':   7(1)    9(1)   18(1)
IoStoreInA:      5(1)
LargeHold:       8(1)
LdPipeVAdly':    9(1)
LoadEcOut':      5(1)
LoadEn':         5(3)   18(1)
LoadFltSrn:      3(1)   18(1)
LoadSinE:        8(1)
LoadSinO:        8(1)    9(1)
LoadSoutE':      5(1)
LoadSoutO':      5(1)
M0:             11(1)
M1:             11(1)
M2:             11(1)
M3:             11(1)
MakeD←CD:       19(1)
MakeD←CD!:       9(1)
MakeD←Dbuf:     19(1)
MakeD←Dbuf!:    10(1)
MakeFout←D:      9(1)   10(1)   19(1)
MakeF←D:        19(1)
MakeF←D!:       10(1)
MakeMDM←D':      1(1)   19(1)   20(1)
MakeMD←D:        1(1)   19(1)
MakeMD←D':       1(1)
MakeMemCAS:      7(1)    8(1)
MakeSout←D:      5(1)   19(1)
MakeTransport0:  5(2)   10(1)   19(1)
MakeTransport1:  5(2)   19(1)
MakeTransport2:  5(1)    9(1)   10(1)   19(1)
MapAd.0:        15(1)
MapAd.1:        15(1)
MapAd.2:        15(1)
MapAd.3:        15(1)
MapAd.4:        15(1)
MapAd.5:        15(1)
MapAd.6:        15(1)
MapAd.7:        15(1)
MapAd.8:        15(1)
Mapbuf.00:      11(1)   12(1)   18(1)
Mapbuf.01:      11(1)   12(1)   18(1)
Mapbuf.02:      11(1)   12(1)   18(1)
Mapbuf.03:      11(1)   12(1)   18(1)
Mapbuf.04:      11(1)   12(1)   18(1)
Mapbuf.05:      11(1)   12(1)   18(1)
Mapbuf.06:      11(1)   12(1)   18(1)
Mapbuf.07:      11(1)   12(1)   18(1)
Mapbuf.08:      11(1)   12(1)   18(1)
Mapbuf.09:      11(1)   12(1)   18(1)
Mapbuf.10:      11(1)   12(1)   18(1)
Mapbuf.11:      11(1)   12(1)   18(1)
Mapbuf.12:       3(1)   11(1)   13(1)   18(1)
Mapbuf.13:       3(1)   11(2)   13(1)   18(1)
Mapbuf.14:       3(1)   11(2)   13(1)   18(1)
Mapbuf.15:       3(1)   11(2)   13(1)   18(1)
Mapbuf.16:      11(1)   13(1)   18(1)
Mapbuf.17:      11(1)   13(1)   18(1)
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MapbufHi.0:      11(1)   13(2)   18(1)
MapbufHi.1:      11(1)   13(1)   18(1)
MapbufLd'a:      11(1)   20(1)
MapbufLd'b:      11(1)   20(1)
MapbufLd'c:      11(2)   20(1)
MapCAS':         14(1)   18(1)
MapDirty':       13(2)
MapDirtya:       13(2)
MapDirtyb:       13(2)
MapEven':        13(1)
MapFnc.0':        6(1)   14(1)   18(1)
MapFnc.1':        6(1)   14(1)   18(1)
MapFree:          6(3)   19(1)
MapFree':         4(1)    6(1)
MapIs16k:        18(1)
MapIs256k:       18(1)
MapIs64k:        18(1)
MapPar:          13(2)
MapPE:            4(1)    7(1)   13(1)
MapPEInEc1:       9(1)   10(1)
MapPEInEc2:      10(2)   18(1)
MapPEInMem:       7(1)    9(1)   18(1)
MapPerr:          4(1)   19(1)
MapRAS':         14(1)   18(1)
MapRef:          13(1)
MapRfsh:          3(1)    4(1)   19(1)
MapRfsh':         4(2)    6(1)
MapRfshDly:       4(1)   15(1)   19(1)
MapSrn.0:         3(2)   19(1)
MapSrn.1:         3(2)   19(1)
MapSrn.2:         3(2)   19(1)
MapSrn.3:         3(2)   19(1)
MapState.0:       6(1)   14(1)   18(1)
MapState.1:       6(1)   14(1)   18(1)
MapState.2:       6(1)   14(1)   18(1)
MapTrouble:       7(1)   13(1)
MapTrouble':     13(1)
MapTroubleInEc1:           9(1)   10(1)   18(1)
MapTroubleInEc2:          10(3)   18(1)
MapTroubleInMem:           7(1)    9(1)   18(1)
MapWait:          6(1)   14(2)   18(1)
MapWait-D:        5(1)    6(1)
MapWait-Ec2:      6(1)   10(1)   19(1)
MapWait-MemD:     7(1)   19(1)
MapWait-MemD':    6(1)    7(1)
MapWait-MemIO:    7(1)   19(1)
MapWait-MemIO':   6(1)    7(1)
MapWait-MemState':         6(1)    7(1)   19(1)
MapWait-ST':      5(1)    6(1)   18(1)
MapWantsPipe:     3(2)    6(2)   19(1)
MapWE':          14(1)   18(1)
MapWP:            7(1)   13(2)
MapWP':          13(3)
Map←InMap:        6(1)   13(1)
Map←InMap':       6(1)   13(2)
Map←InPair':     20(1)
Mcr←':           11(1)
MD0:             18(4)
MD1:             18(4)
MD2:             18(5)
MD3:             18(5)
MD4:             18(1)   19(4)
MD5:             18(1)   19(3)
MD6:             18(1)   19(3)
MD7:             18(1)   19(3)
MDMtag':          1(1)   19(1)
MDMtagAd.0:       1(1)   19(1)
MDMtagAd.1:       1(1)   19(1)
MDMtagAd.2:       1(1)   19(1)
MDMtagAd.3:       1(1)   19(1)
MemAd.0:         12(1)
MemAd.1:         12(1)
MemAd.2:         12(1)
MemAd.3:         12(1)
MemAd.4:         12(1)
MemAd.5:         12(1)
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MemAd.6:          12(1)
MemAd.7:          12(1)
MemAd.8:          12(1)
MemCad.0:         12(2)
MemCad.1:         12(2)
MemCad.2:         12(2)
MemCad.3:         12(2)
MemCad.4:         12(2)
MemCASa:           8(1)
MemCASb:           8(1)
MemClkEnable'c!%:         20(1)
MemColSela:       12(1)   19(1)
MemError:         10(1)
MemError':         3(1)   10(2)   18(1)
MemFree:           7(3)   19(1)
MemIdle:           7(4)
MemIdle':          7(2)   19(1)
MemIdlea:          7(2)
MemPE:             4(2)
MemRASa:           7(1)
MemRASb:           7(1)
MemRfsh:          12(3)   14(1)   15(3)   19(1)   20(1)
MemSH!%:          20(1)
MemSrn.0:          3(1)   19(1)
MemSrn.1:          3(1)   19(1)
MemSrn.2:          3(1)   19(1)
MemSrn.3:          3(1)   19(1)
MemState.0:        7(2)   19(1)
MemState.1:        7(2)   19(1)
MemState.2:        7(2)   19(1)
MemState.3:        7(2)   19(1)
MemState6':        7(3)
MemState7':        7(2)
MemWEa:            7(1)
MemWEb:            7(1)
MemWP:             7(1)    9(1)   18(1)
MidasBank0'a:     18(5)
MidasBank0'b:     18(1)   19(4)
MidasBank1'a:     18(5)
MidasBank1'b:     18(1)   19(4)
MidasBank2'a:     18(3)
MidasBank2'b:     18(1)   19(4)
MidasBank3'a:     18(5)
MidasBank3'b:     18(1)   19(1)
Mod.0:             7(1)    8(1)
Mod.1:             7(1)    8(1)
ModOEn'a:          7(1)    9(1)
ModOSinEn'!:       9(1)
ModOStrEn'!:       7(1)
Mod1En'a:          7(1)    9(1)
Mod1SinEn'!:       9(1)
Mod1StrEn'!:       7(1)
Mod2En'a:          7(1)    9(1)
Mod2SinEn'!:       9(1)
Mod2StrEn'!:       7(1)
Mod3En'a:          7(1)    9(1)
Mod3SinEn'!:       9(1)
Mod3StrEn'!:       7(1)
ModSel.0:          8(2)   11(1)
MxHold:            1(1)    4(1)
NeedRfsh:          4(1)   19(1)
NeedRfsh':         4(1)
Next.0!:           2(1)
Next.1!:           2(1)
Next.2!:           2(1)
Next.3!:           2(1)
NoWakeups:         4(1)   11(2)   18(1)
PairFull:          4(1)   18(1)
PairFull':         4(1)   20(1)
PairLdEnable':     1(1)    2(2)
PEsrn.0:           3(2)   18(1)
PEsrn.1:           3(2)   18(1)
PEsrn.2:           3(2)   18(1)
PEsrn.3:           3(2)   18(1)
Pipe02Ad.0:        2(2)    3(1)
Pipe02Ad.1:        2(2)    3(1)
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Pipe02Ad.2:      2(2)    3(1)
Pipe02Ad.3:      2(2)    3(1)
Pipe3.00:       11(1)   12(1)
Pipe3.01:       11(1)   12(1)
Pipe3.02:       11(1)   12(1)
Pipe3.03:       11(1)   12(1)
Pipe3.04:       11(1)   12(1)
Pipe3.05:       11(1)   12(1)
Pipe3.06:       11(1)   12(1)
Pipe3.07:       11(1)   12(1)
Pipe3.08:       11(1)   12(1)
Pipe3.09:       11(1)   12(1)
Pipe3.10:       11(1)   12(1)
Pipe3.11:       11(1)   12(1)
Pipe3.12:       11(1)   13(1)
Pipe3.13:       11(1)   13(1)
Pipe3.14:       11(1)   13(1)
Pipe3.15:       11(1)   13(1)
Pipe34Ad.0:      3(1)   13(6)   18(1)
Pipe34Ad.1:      3(1)   13(6)   18(1)
Pipe34Ad.2:      3(1)   13(6)   18(1)
Pipe34Ad.3:      3(1)   13(6)   18(1)
Pipe4.00:       11(1)   13(1)
Pipe4.01:       11(1)   13(1)
Pipe4.02:       11(1)   13(1)
Pipe4.03:       11(1)   13(1)
PipeMapDirtyb:  11(1)   13(1)
PipeMapFnc.0':   2(1)   11(1)
PipeMapFnc.1':   2(1)   11(1)
PipeMapPar:     11(1)   13(1)
PipeSubTask.0:   2(1)
PipeSubTask.0a:  2(1)   11(1)
PipeSubTask.1:   2(1)
PipeSubTask.1a:  2(1)   11(1)
PipeTask.0:      2(1)
PipeTask.0a:     2(1)   11(1)
PipeTask.1:      2(1)
PipeTask.1a:     2(1)   11(1)
PipeTask.2:      2(1)
PipeTask.2a:     2(1)   11(1)
PipeTask.3:      2(1)
PipeTask.3a:     2(1)   11(1)
preClk0'Aa:     20(1)
preClk0'Aa%:    20(1)
preClk0'Ba:     20(1)
preClk0'Ba%:    20(1)
preClk0'Bb:     20(1)
preClk0'Bb%:    20(1)
preClk0'Bc:     20(1)
preClk0'Bc%:    20(1)
preClk0'Ca:     20(1)
preClk0'Ca%:    20(1)
preClk0'Cb:     20(2)
preClk0'Cb%:    20(1)
preClk0'Da:     20(1)
preClk0'Da%:    20(1)
preClk0'Db:     20(1)
preClk0'Db%:    20(1)
preClk0'Dc:     20(2)
preClk0'Dc%:    20(1)
preClk1'A:      20(1)
preClk1'A%:     20(1)
preClk1'B:      20(1)
preClk1'B%:     20(1)
preClk1'C:      20(2)
preClk1'C%:     20(1)
preClk1'D:      20(1)
preClk1'D%:     20(1)
preClk2'C:      20(1)
preClk2'C%:     20(1)
preEcEn':        9(1)
preFH'%:        20(2)
preFH'A:        20(2)
preFHA:         20(1)
preFHA%:        20(1)
preFHB:         20(1)
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preFHB%:         20(1)
preFHC:          20(1)
preFHC%:         20(1)
preMCSa:          7(1)   12(1)
preMCSb:          7(1)
prepreClk2'a%:   20(2)
prepreClk2'b%:   20(2)
prepreClk2'c%:   20(3)
prepreFH'%:      20(1)
preRfshInMem:     6(1)    7(1)   13(3)
preSH'%:         20(2)
preStartEc2':     3(1)    9(1)   10(1)
preStartMem':     6(2)
preSTFree':       5(3)
PrivRefInPair:    3(1)   18(1)
ProcSrn.0:        3(2)   11(1)   18(1)
ProcSrn.1:        3(2)   11(1)   18(1)
ProcSrn.2:        3(2)   11(1)   18(1)
ProcSrn.3:        3(2)   11(1)   18(1)
ProcSrn←':        3(1)   18(1)
ProcTag:          1(1)   19(1)
ProcTagInA:       1(2)   18(1)
Ptag:             1(1)   19(1)
RamA0orVEEa!01:  14(1)
RamA0orVEEa!02:  14(1)
RamA0orVEEa!03:  16(1)
RamA0orVEEa!04:  16(1)
RamA0orVEEa!05:  16(1)
RamA0orVEEa!06:  16(1)
RamA0orVEEa!07:  16(1)
RamA0orVEEa!08:  16(1)
RamA0orVEEa!09:  16(1)
RamA0orVEEa!10:  16(1)
RamA0orVEEa!11:  16(1)
RamA0orVEEa!12:  16(1)
RamA0orVEEa!13:  16(1)
RamA0orVEEa!14:  16(1)
RamA0orVEEa!15:  16(1)
RamA0orVEEa!16:  16(1)
RamA0orVEEb!01:  14(1)
RamA0orVEEb!02:  14(1)
RamA0orVEEb!03:  17(1)
RamA0orVEEb!04:  17(1)
RamA0orVEEb!05:  17(1)
RamA0orVEEb!06:  17(1)
RamA0orVEEb!07:  17(1)
RamA0orVEEb!08:  17(1)
RamA0orVEEb!09:  17(1)
RamA0orVEEb!10:  17(1)
RamA0orVEEb!11:  17(1)
RamA0orVEEb!12:  17(1)
RamA0orVEEb!13:  17(1)
RamA0orVEEb!14:  17(1)
RamA0orVEEb!15:  17(1)
RamA1orVCCa!01:  14(1)
RamA1orVCCa!02:  14(1)
RamA1orVCCa!03:  16(1)
RamA1orVCCa!04:  16(1)
RamA1orVCCa!05:  16(1)
RamA1orVCCa!06:  16(2)
RamA1orVCCa!07:  16(1)
RamA1orVCCa!08:  16(1)
RamA1orVCCa!09:  16(1)
RamA1orVCCa!10:  16(1)
RamA1orVCCa!11:  16(1)
RamA1orVCCa!12:  16(1)
RamA1orVCCa!13:  16(1)
RamA1orVCCa!14:  16(1)
RamA1orVCCa!15:  16(1)
RamA1orVCCb!01:  14(1)
RamA1orVCCb!02:  14(1)
RamA1orVCCb!03:  17(1)
RamA1orVCCb!04:  17(1)
RamA1orVCCb!05:  17(1)
RamA1orVCCb!06:  17(1)
RamA1orVCCb!07:  17(1)
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RamA1orVCCb!08: 17(1)
RamA1orVCCb!09: 17(1)
RamA1orVCCb!10: 17(1)
RamA1orVCCb!11: 17(1)
RamA1orVCCb!12: 17(1)
RamA1orVCCb!13: 17(1)
RamA1orVCCb!14: 17(1)
RamA1orVCCb!15: 17(1)
RamV+a!01:      14(1)
RamV+a!02:      14(1)
RamV+a!03:      16(1)
RamV+a!04:      16(1)
RamV+a!05:      16(1)
RamV+a!06:      16(1)
RamV+a!07:      16(1)
RamV+a!08:      16(1)
RamV+a!09:      16(1)
RamV+a!10:      16(1)
RamV+a!11:      16(1)
RamV+a!12:      16(1)
RamV+a!13:      16(1)
RamV+a!14:      16(1)
RamV+a!15:      16(1)
RamV+a!16:      16(1)
RamV+a!17:      16(1)
RamV+a!18:      16(1)
RamV+a!19:      16(1)
RamV+b!01:      14(1)
RamV+b!02:      14(1)
RamV+b!03:      17(1)
RamV+b!04:      17(1)
RamV+b!05:      17(1)
RamV+b!06:      17(1)
RamV+b!07:      17(1)
RamV+b!08:      17(1)
RamV+b!09:      17(1)
RamV+b!10:      17(1)
RamV+b!11:      17(1)
RamV+b!12:      17(1)
RamV+b!13:      17(1)
RamV+b!14:      17(1)
RamV+b!15:      17(1)
RamV+b!16:      17(1)
RamV+b!17:      17(1)
RamV+b!18:      17(1)
ReadInA':        6(1)
ReadOrWriteInMap':      13(1)
RefUsesD10InMap':        6(1)    7(1)    19(1)
RefUsesD10InMem':        7(1)   18(1)
RefUsesDInEc1:   6(1)    9(1)   19(1)
RefUsesDInMap':  6(2)    7(1)   19(1)
RefUsesDInMem:   6(1)    7(1)    9(1)   18(1)
RefUsesDInMem':  7(1)    9(1)
RefWE':         12(2)   14(1)   18(1)   20(1)
RepeatCur:       2(2)    4(1)
ReportFault:     3(1)   18(1)
ReportFault':    3(2)
ReportSE':       3(1)   11(1)   18(1)
RfshAd.0:       12(1)   15(1)   18(1)
RfshAd.1:       12(1)   15(1)
RfshAd.2:       12(1)   15(1)
RfshAd.3:       12(1)   15(1)
RfshAd.4:       12(1)   15(1)
RfshAd.5:       12(1)   15(1)
RfshAd.6:       12(1)   15(1)
RfshAd.7:       12(1)   15(1)
RfshAd.8:       12(1)   15(1)
RfshInMem:       7(2)   18(1)
RfshPeriod:      4(1)
RfshSqWave:      4(2)
RP.00:           8(1)   12(1)   13(1)
RP.01:           8(1)   12(1)   13(1)
RP.02:           8(1)   12(2)   13(1)
RP.03:           8(1)   12(2)   13(1)
RP.04:           8(1)   12(2)   13(1)
RP.05:           8(1)   12(2)   13(1)
```

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RP.06:            8(1)   12(2)   13(1)
RP.07:            8(1)   12(2)   13(1)
RP.08:           12(2)   13(1)
RP.09:           12(2)   13(1)
RP.10:           12(2)   13(1)
RP.11:           12(2)   13(1)
RP.12:           12(1)   13(2)
RP.13:           12(1)   13(2)
RP.14:           12(1)   13(2)
RP.15:           12(1)   13(2)
RTMapAd.0a:      14(2)
RTMapAd.0b:      14(2)
RTMapAd.1a:      14(2)
RTMapAd.1b:      14(2)
RTMapAd.2a:      14(1)   16(11)
RTMapAd.2b:      14(1)   17(10)
RTMapAd.3a:      14(1)   16(11)
RTMapAd.3b:      14(1)   17(10)
RTMapAd.4a:      14(1)   16(11)
RTMapAd.4b:      14(1)   17(10)
RTMapAd.5a:      14(1)   16(11)
RTMapAd.5b:      14(1)   17(10)
RTMapAd.6a:      14(1)   16(11)
RTMapAd.6b:      14(1)   17(10)
RTMapAd.7a:      14(1)   16(11)
RTMapAd.7b:      14(1)   17(10)
RTMapAd.8a:      14(1)   16(11)
RTMapAd.8b:      14(1)   17(10)
RTMapCAS'a:      14(1)   16(11)
RTMapCAS'b:      14(1)   17(10)
RTMapRAS'a:      14(1)   16(11)
RTMapRAS'b:      14(1)   17(10)
RTMapWE'a:       14(1)   16(11)
RTMapWE'b:       14(1)   17(7)
SH'Aa:            5(3)   20(1)
SH'Ba:            5(3)    9(1)   20(1)
SHCa:             1(1)   20(1)
SHDa:            10(1)   20(1)
ShiftEcOut:       5(1)
ShiftEn':         5(4)   18(1)
ShiftSinE:        5(1)
ShiftSinO:        5(1)
ShiftSoutE:       5(1)
ShiftSoutO:       5(1)
sHold:            4(2)   19(1)
sHold':           4(2)
SrnOFault:        3(1)   11(2)
StartEc1:         8(1)    9(1)   18(1)
StartEc1':        3(1)    9(1)   20(1)
StartEc1Clk0':    9(1)   20(1)
StartEc2':        9(1)   10(2)   19(1)   20(1)
StartEc2Clk0':   10(1)   20(1)
StartEcChk':      9(1)
StartEcGen':      5(1)
StartMap':        3(2)    6(2)   20(1)
StartMapClk0'a:   6(1)   20(1)
StartMapClk0'b:   6(1)   20(1)
StartMem':        3(1)    6(1)    7(2)   13(1)   20(1)
StartMem'a:       6(1)    7(1)
StartMema:        6(1)   19(1)
StartMemClk0':    7(1)   20(1)
StartRfshCycle':          4(1)
StartST:          5(2)   19(1)
StartST':         5(2)
STClk0'Ba:        5(1)   20(1)
STClk0'Bb:        5(1)   20(1)
STClk0'D:         5(1)   20(1)
STfree':          2(1)    5(5)   19(1)
STIdle:           5(1)   20(2)
STIdle':          5(1)   19(1)
StkError:         3(1)
StkWake:          3(1)   19(1)
StopFinTaskLoad:          2(1)    5(1)   19(1)
Store←InA':       6(1)
Store←InEc1':    10(1)
Store←InEc2:     10(2)
```

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Store←InEc2':   10(1)   18(1)
Store←InMap':    6(1)   19(1)
STPerr:          4(1)   19(1)
STPerrNow':      5(2)   18(1)
STState.0:       5(1)   19(1)
STState.1:       5(1)   19(1)
STState.2:       5(1)   19(1)
STState.3:       5(1)   19(1)
STWait-Mem':     5(1)    7(1)   19(1)
Subtask.0!:      2(1)
Subtask.1!:      2(1)
SW:              1(2)
TagInEc1:       10(1)
TagInEc2:        1(1)   10(1)   18(1)
TDirtyWE':      14(1)   17(2)
THi:            12(4)   13(2)   14(1)
TIOA.0!:        11(1)
TIOA.1!:        11(1)
TMapAd.0a:      14(1)   15(1)
TMapAd.0b:      14(1)   15(1)
TMapAd.1a:      14(1)   15(1)
TMapAd.1b:      14(1)   15(1)
TMapAd.2a:      14(1)   15(1)
TMapAd.2b:      14(1)   15(1)
TMapAd.3a:      14(1)   15(1)
TMapAd.3b:      14(1)   15(1)
TMapAd.4a:      14(1)   15(1)
TMapAd.4b:      14(1)   15(1)
TMapAd.5a:      14(1)   15(1)
TMapAd.5b:      14(1)   15(1)
TMapAd.6a:      14(1)   15(1)
TMapAd.6b:      14(1)   15(1)
TMapAd.7a:      14(1)   15(1)
TMapAd.7b:      14(1)   15(1)
TMapAd.8a:      14(1)   15(1)
TMapAd.8b:      14(1)   15(1)
TMapCAS'a:      14(2)
TMapCAS'b:      14(2)
TMapRAS'a:      14(2)
TMapRAS'b:      14(2)
TMapWE'a:       14(2)
TMapWE'b:       14(2)
Transport'!:     5(1)
Transporta:      5(1)   18(1)
TRefWE':        14(1)   17(1)
TrueAC:          2(7)    3(1)    4(1)    7(2)   11(1)   14(1)
                20(1)
TrueBD:          3(2)    5(2)    6(2)    7(2)    9(1)   10(3)
                13(1)   15(3)   20(1)
TrueNext.0:      1(1)    2(1)
TrueNext.1:      1(1)    2(1)
TrueNext.2:      1(1)    2(1)
TrueNext.3:      1(1)    2(1)
TWReq15:         3(1)
Use256/16KProm':         7(1)    8(1)
Use64KProm':     7(1)    8(1)
UseAsrn:         3(1)   19(1)
ValidMapFltInEc2':       3(1)   10(2)   18(1)
VBBb11:         12(4)   15(1)
VBBb15:         14(1)
VBBb5:          12(4)   15(1)
VBBb8:          12(3)   13(1)   15(1)
VBBc13:         14(1)
VBBc14:         15(1)
VBBc15:         15(1)
VBBe13:         15(1)
VBBe14:         15(1)
VBBe15:         14(2)   15(1)
VBBe4:          12(1)   13(3)   15(1)
VBBe9:          13(4)   15(1)
VCC:            14(6)
VDD:            14(2)
VEE:            14(2)
VicIfMiss':      6(1)
VicIfMissInMap':         6(1)
VicInPair':      5(1)    6(1)
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VicOrFS1C:       20(1)
VicSTPerr:        4(1)    18(1)
VicSTPerr':       4(1)     9(1)    10(1)
VictimInA:        5(2)    19(1)
VictimInA':       2(1)     5(3)
VictimInST:       4(1)     5(3)    19(1)
WakeEnable:       3(1)    11(1)
WakeOnCL:        11(2)    18(1)
WakeOnCL':        3(1)    11(1)
WantMapWait':     6(1)    18(1)
WantRfsh:         4(1)    19(1)
WantRfsh':        4(2)
Whatever:         8(16)   14(14)
WPinEc1:          9(1)    18(1)
WriteInA':        5(2)     6(2)
WriteInMap':      6(2)     7(1)    14(1)    19(1)
WriteInMem':      7(1)    18(1)
WriteMDM':        1(1)    20(1)
WritePipe02Clk0':          2(1)    20(1)
WritePipe02Clk1':          2(1)    20(1)
WritePipe3'a:    13(2)    20(1)
WritePipe3'b:    13(2)    20(1)
WritePipe3'c:    13(2)    20(1)
XWantsPipe:       6(1)
←Config:         11(4)
←FaultInfo:       4(1)    11(5)
←FaultInfoDly':   3(2)     4(2)    19(1)    20(1)
←Map:             2(1)
←MapInMap:        6(1)    14(2)    19(1)
←MapInPair:       2(1)     6(1)
←MD:              1(1)
←MD':             1(1)
←MDdly':          4(1)
←Pipe2:          11(2)
←Pipe3:          11(4)
←Pipe4:          11(3)
←Pipes':         11(2)
←Pipes'%:        11(1)
←Things':        11(6)
←Things'%:       11(1)
```