K20

LOGIC ANALYZER

USER'S MANUAL

GOULD

Electronics

K20 USER'S MANUAL
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1.1 USING THE MANUAL

It is recommended that this manual, which should be read prior to using the Gould K20 Logic Analyzer, be used while learning to operate the instrument. It should be kept for reference after the user has become familiar with the operation of the K20. Because the Gould K20 Analyzers include menu-driven Help Messages, use this manual only when more detail is required.

If you requier any assistance with this product, please call Gould Instruments Division Customer Service on the toll free, hot line numbers listed below.

National (800) 538-9320/9321

California (800) 662-9231

1.2 INSTRUMENTS DESCRIBED IN THE MANUAL

This manual covers the basic use of the Gould K20 Logic Analyzer, the 24 Channel State Probe, and the 8 Channel Timing Probe.

1.3 GOULD K20 SERIES, GENERAL DESCRIPTION

The K20 Logic Analyzer System consists of the K20 Logic Analyzer unit, the Timing Analysis Data Probe and the general purpose State Mode Data Probe.

The general purpose State Mode Probe offers 24 bits of data input with an advanced clocking capability and a substantial triggering capability for most microprocessor and bus configurations (both 8 and 16 bits). The Timing Mode Probe offers complex triggering, sampling rates to 100 MHz, glitch detection, extremely deep sample memory and sufficient channels for most jobs, all as standard features.

Because of its considerable sample memory depth, the K20 has a new feature not previously found in logic analyzers: Accelerating Rate Scrolling (ARS). ARS allows scrolling through memory to be slow and precise, or fast, to move to another point quickly. The rate accelerates as the scrolling switch continues to be pressed. Releasing the switch momentarily causes a return to the slower rate. None of the data are missed during scrolling.

The K20 also offers "Help" messages to lessen reliance on the User's Manual. The K20 has virtually no limit in terms of expansion and the addition of software. The base analyzer unit contains the software required to run the standard data probes and help messages. Other probes come with software and expanded hardware capabilities within the Probe. There is never a need to open the main unit to add an option.

The K20 Series analyzers which are small and lightweight, offer a high performance/price ratio. There are only a few, simple menus. Specific Menus for specialized probes are included with the software within the Probe.

2.0 PREPARATION FOR USE

This section covers unpacking, inspection and preparation of the equipment prior to use.

2.1 INCOMING INSPECTION

Look for obvious shipping damage such as dents or punctures. Also, check for loose components.

Note:

If shipping damage has occurred, SAVE THE ORIGINAL CONTAINER and notify the shipper immediately.

2.2 RETURN OF EQUIPMENT

If the unit must be sent back to the factory for any reason, contact Gould, Inc. Design & Test Systems Division, Cupertino California or your local sales office for instructions and a RETURN AUTHORIZATION NUMBER.

Note:

EQUIPMENT RETURNED TO THE FACTORY WITHOUT PRIOR AUTHORIZATION CANNOT BE ACCEPTED.

2.3 CARE AND USE OF THE INSTRUMENTS

The Gould K20 Series Logic Analyzers are lightweight, portable units and if used properly and not abused will provide years of service. The buttons, handles, tilt feet, cables and connectors, CRT, and data probes should be treated with care. Because the units are equipped with a convection cooling system (no fan), air flow around the instruments must not be inhibited. To allow maximum ventilation, it is recommended that the instruments be tilted above the flat horizontal position when being used for extended periods of time. Air flow near the instruments should not be retarded by nearby objects.

Never place flat objects, such as books and papers, on top of the instruments. Normal ventilation of the instruments is facilitated by vents in the bottom and top case panels. The metal back panel, the inner metal chassis and the power supply chassis function as heat radiators. To control air movement through the case, the internal ventilation holes were carefully placed with respect to the case openings. When in a horizontal position, and unobstructed above and for two inches from the sides and back, the K20 will ventilate properly at room temperatures to 80 degrees F.

The K20 is also designed to ventilate properly when used in a vertical position. If the instrument must be used in a hot or obstructed position, the tilt feet or handle can be used to allow better ventilation from beneath. In extreme cases the instrument should only be powered up when in actual use.

Typically, the Data probes are designed to be used with normal logic level voltages. Unless the data probe (such as an analog probe) is specially designed to handle higher voltages, areas where higher voltages exist should be handled very carefully.

CAUTION

Extra care should always be used when connecting the probe inputs to the circuits under test. Making connections to the circuits under test while power is applied to the circuits should be avoided if possible.

The analyzer and data probe must be powered up before connections are made to a system under test. The best way to do this when changing the connections is to disconnect momentarily the test clip cables from the input to the Timing or State probe. This is not possible when connecting a single clip of a microprocessor probe to a microprocessor under test. Here, first turn off the power to the system under test as well as to the analyzer. After the connection is made, turn the power on to the analyzer. Then turn the power on to the circuit under test.

Active signals coming into a probe (not already powered up) can sometimes damage the probe. At all times when a probe is being connected to the analyzer, there should be no input connection to the probe and the analyzer should have its power turned off.

The K20 is designed to be expandable using optional add-on data probes and devices. There should never be an attempt to connect any device or cable to the unit unless it is specifically designed to be compatible with the K20 Analyzer. This is also true for any of the data probes and accessories.

Note:

The protective power fuse should not be substituted with one of a higher current value. If the recommended fuse is failing, the unit should be returned to an authorized service center. The covers should not be removed because there are no user-serviceable components within the units. All service should be performed by an authorized service center.

2.4 SPECIFICATIONS

Specifications cover the Gould Models K20 Logic Analyzers, the State Mode probe and the Timing Mode probe.

The K20 analyzer contains an integral five-inch CRT and is supplied with an 8-channel timing probe and a 24-channel state probe. The analyzer has a composite video output for use with any standard video monitor.

2.5 TIMING MODE, 8 - CHANNEL TIMING PROBE

2.5.1 MEMORY

Formats	8 Bits up to 27 MHz 4 Bits at 50 MHz 2 Bits at 100 MHz 4 Bits up to 27 MHz with glitch capture
Depth	24,576 Words at 100 MHz 12,288 words at 50 MHz 6,144 words at 25 MHz and below 6,144 words in glitch capture mode

2.5.2 CLOCKS

Internal	25 Hz TO 100 MHz in 2.5, 5, 10 sequence
External	DC TO 27 MHz (Pulse Width > 10 ns, Active High or Active Low)
Ext Times 2	DC TO 13.5 MHz. This mode uses the external input and the internal frequency double for two samples per clock period (must be symmetrical). It adds additional sampling resolution and allows the clock itself to be viewed when also connected to one of the data inputs.

2.5.3 TRIGGERING

Qualification	Three independent qualifiers, each 8-bits wide
Sequencing	Three sequence levels (first, then, then) using any qualifier and the external input or their inverses (any can be repeated).
Delay	Samples Before Trigger Zero counts to 100 percent of sample Memory depth

2.5.4 GLITCH DETECTION

Captures glitches down to ten nanosecond duration

2.5.5 Probe INPUTS

High Speed CMOS, TTL Level

Skew	< 5ns, < 3ns at 100 MHz

2.6 STATE MODE, 24 - CHANNEL STATE PROBE

2.6.1 **MEMORY** 24 bits by 2048 words

2.6.2 **CLOCKS** Frequency DC to 9 MHz, pulse width > 40ns.

Data Setup Time: > 20ns, Hold time: 0.

The 24 data inputs are divided into three independently clocked 8-bit bytes that can be clocked in parallel, or separately in any order. The three clocks can be defined as virtually any logical combination of the NAND, OR, NOR.

2.6.3 **FEATURES**

Bus Demultiplexing

Capture read data only, write only, I/O write only, etc.

Sufficient for virtually any processor system, 8-bit or 16-bit.

2.6.4 **TRIGGERING**

Qualification — Three independent 8-bit qualifiers which can also be defined as one 16-bit and one 8-bit qualifier, or as a single 24-bit qualifier.

Sequencing — Three sequence levels (first, then, then) using any qualifier or any 8-bit portion of a qualifier and the external input or their inverses (any can be repeated).

2.6.5 **PROBE INPUTS** High Speed CMOS, TTL Level

24 bits by 2048 words with typical 8-bit microprocessors such as 6502, Z80, and 8080A.

2.7 PHYSICAL CHARACTERISTICS

Dimensions

K20 - 5.3" X 10" X 10"
(13cm X 25cm X 25cm)

Weight

K20 - 9 lb (4.1 kg)

Environment

Operating temperature: 0 to 40 C

Operating altitude: 10,000 ft.

Power Requirements

120 Vac 60 Hz

K20 - 20 watts

08/85 Specifications subject to change

3.1 MENUS AND INPUT

The Gould K20 Series Logic Analyzers are controlled by menu prompting through the use of the four cursor control keys and four command keys. Upon power up, the K20 Series Logic Analyzer presents the Gould initial display, warns the user to connect the probes only when power is off and requests the user to press any key. The analyzer then interrogates the probe for proper setup and proceeds to the next menu (see figure 3-1. initialization menu).

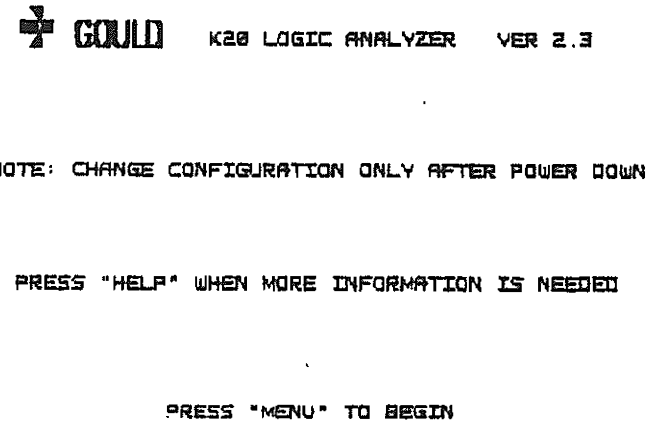


Figure 3-1. Initialization Menu

In each menu, setup data are outlined in a box and the active data are typically video inverted. This is true in the Timing mode and the Clock Source menu in which there are two fields, each having more than one possible selection. The selected fields are highlighted with inverse video, and following initial power up, one selection in each field remains highlighted after initially being set. To make a selection, move DOWN to the appropriate line and press the ENTER switch. An old selection in any given field will change back to normal video. In the Triggering menu, to set up, press ENTER when you are in the trigger sequence fields. When in the Qualifier fields, ENTER has a slighty different function (see below).

The required control switches are listed in each menu. UP, DOWN, LEFT, and RIGHT cursor keys indicate direction of flashing cursor movement, and ENTER locks in a new selection. Pressing DOWN at the bottom of a menu causes a wrap back to the top of the menu. UP at the top causes a wrap back to the bottom. RIGHT at the right end of a line causes a wrap back to the left end. ENTER is used to step through values in fields that have various selections at the flashing cursor position. In a Binary field the possible selections for each bit are X, 0, and 1. In a Hex field the selections would be 0, 1, 2, ..., E, F, and X. Each key will autorepeat if held in position.

To reset the internal processor, press **ENTER** and **ARM-RUN** at the same time, hold for several seconds, then release. Setups in memory will remain as they were. This procedure will not be necessary unless the internal processor gets lost (owing to power line transients or other factors). Turning the analyzer off for several seconds will also force a reset; however, setups in memory will be affected.

3.2 TIMING MODE, CLOCK SOURCE MENU

The CLOCK SOURCE fields identify the source of the clock that the system will use to take samples.

INTERNAL: Formats the system to use the analyzer's internal clock at a sample frequency set by the user in the following menu.

EXTERNAL: Formats the system to use an external clock supplied by the user (DC to 27 MHz).

EXT TIMES 2: When this field is selected, the user-supplied clock (2.5 Hz to 13.5 MHz, which must be symmetrical) is doubled for two samples per clock period. This allows the actual clock to be examined.

Glitch detection which can be set ON or OFF, functions when the analyzer is in Timing mode (clock source: INTERNAL, EXTERNAL, or EXT TIMES 2) and the sample rate is 27 MHz or below; glitches are displayed as single bit width positive pulses on normally low-level lines beneath the bit lines (B0 through B3). The glitch lines (G0 through G3) "point" to the data above and indicate where glitches were detected.

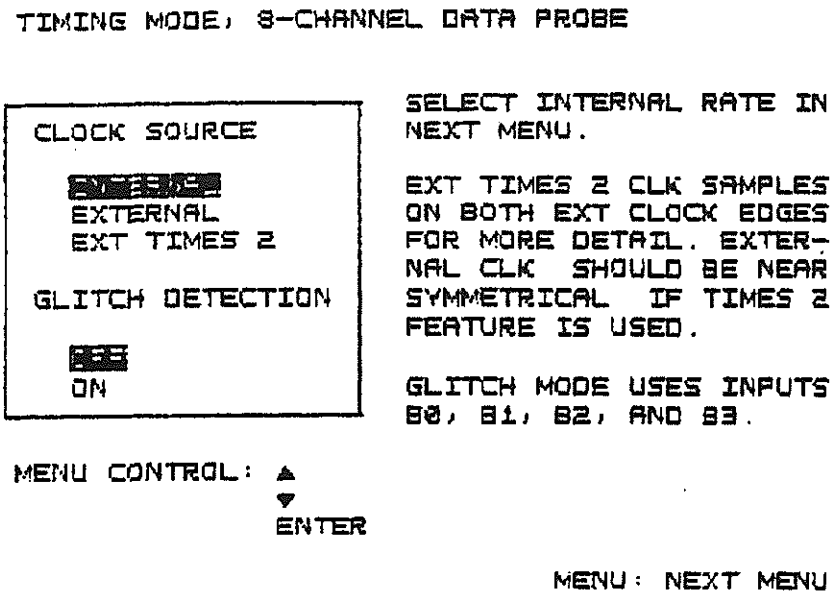


Figure 3-2. Timing Mode, Clocking Source Menu

3.3 INTERNAL SAMPLE CLOCK MENU (TIMING MODE)

Simply step to the desired sample frequency and press **ENTER,** continue to the next screen. When the system is set for glitch detection, the cursor will skip 50 and 100 MHz sample rates. The default setting is 10 MHz.

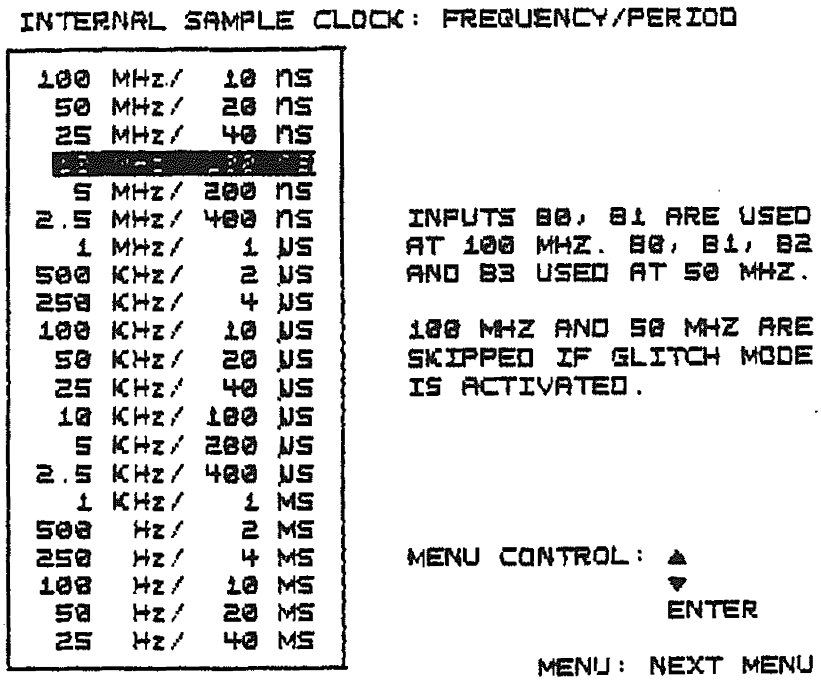


Figure 3-3. Internal Sample Clock Menu (Timing Mode)

3.4 TRIGGER MENU (TIMING AND STATE)

The Trigger menu contains three basic fields:

1. Qualifiers - used to compare with sample data for pattern match,

2. Trigger Sequence - used to set the sequence or combination of qualifiers, and

3. Trigger Delay - the number of samples taken before the trigger point.

To enter qualifiers, move to the desired position using the cursor key. After the cursor reaches the right-most position, it returns to the left-most field. At the desired bit, press the switch labelled **ENTER** to change from X (don't care), 0, or 1. Then move to the next position.

The trigger sequence fields are changed by moving to the desired condition and pressing **ENTER**. The NOT fields switch state each time **ENTER** is pressed.

To set the trigger delay, move down to the field; the cursor will flash on the number of delay samples. To increase the number of delay samples, press >. To decrease the delay samples, press <. The delay samples increment or decrement at an increasing rate the longer the switch is held. Once the desired delay sample count is displayed, press MENU to continue to the next screen.

To display the Help Message, press HELP. The screen will clear and display the message. Pressing any key causes a return to the Trigger menu.

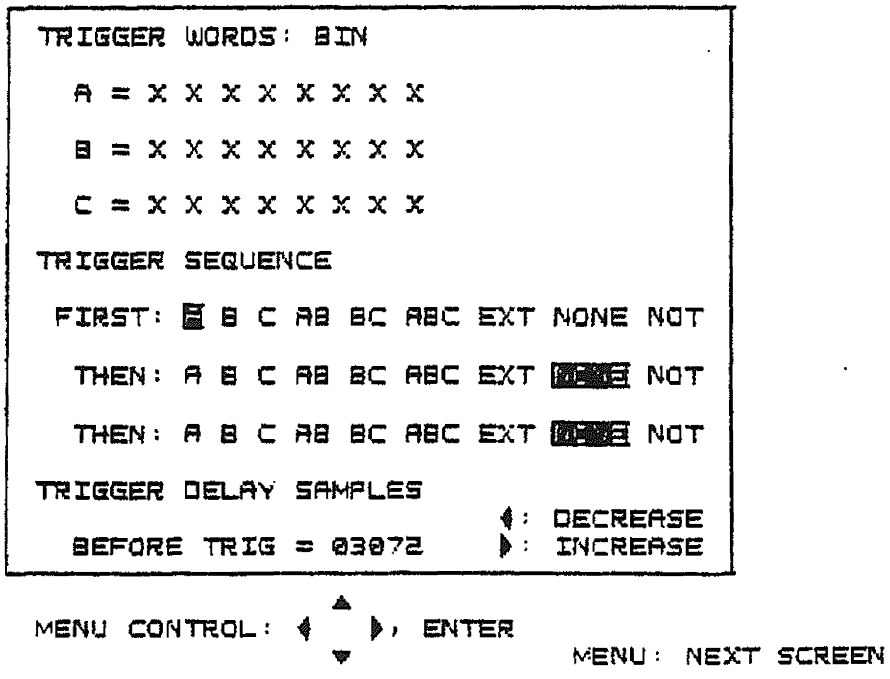


Figure 3-4. Trigger Menu

3.5 TIMING DISPLAY

The Timing display is formated to show eight timing waveforms when sampling at 25 MHz (or below): four waveforms at 50 Mhz, four waveforms with four glitch display lines, and 2 waveforms at 100 MHz. The sample rate is shown in the upper left corner and displays in cycles per second and sample clocks in seconds. Total samples for the setup are displayed in the upper right corner. The trigger position is shown next to the "T" in the lower left corner. The screen position is shown on the opposite or right side. To scroll through memory, press the UP cursor key to move up through memory,or DOWN cursor key to move down through memory. To move rapidly through memory, hold the key down; the display will accelerate. When the trigger condition or end of memory appears on the screen, the scroll rate will automatically slow down. The help screen can be displayed by pressing the HELP switch (see 3-5 for timing and help displays).

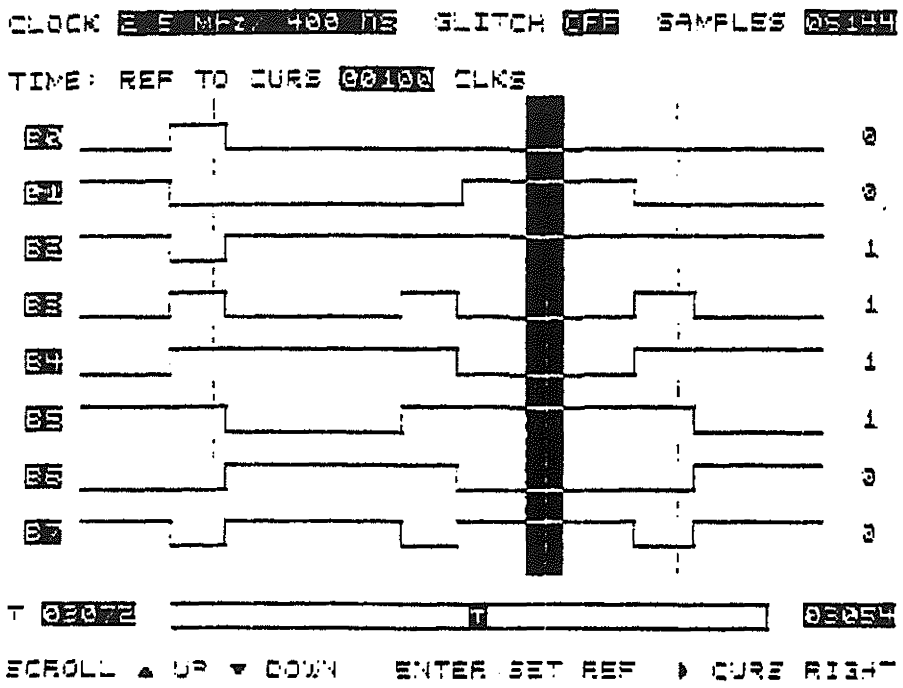


Figure 3-5. Timing Display

3.6 STATE MODE CLOCKING MENU

The 24 data inputs are divided into three independently clocked, 8-bit bytes that can be clocked in parallel or separately in any order. The three clocks can be defined as virtually any logical combination of the three external clock inputs (see figure 3-6 for State mode Clocking Menu and HELP message).

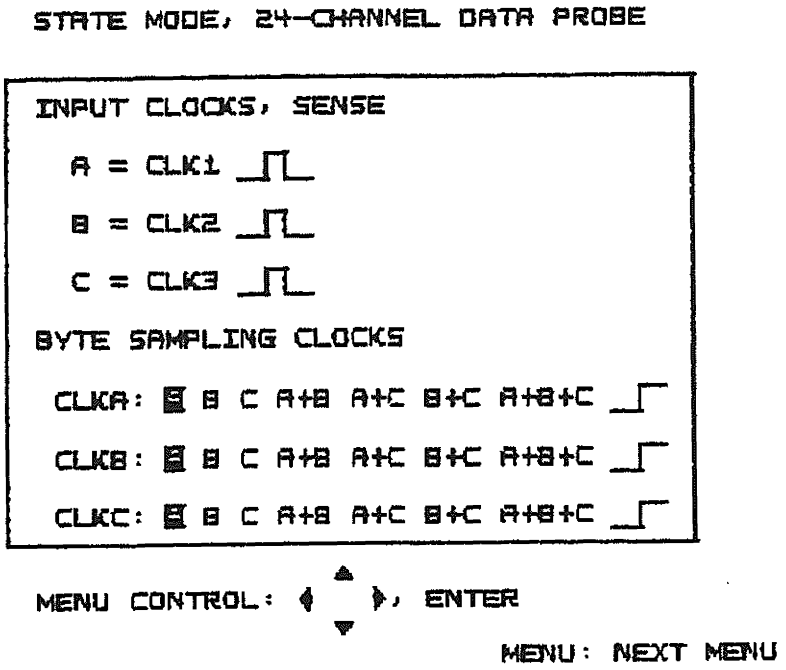


Figure 3-6. State Clocking Menu

3.7 STATE DISPLAY

In State mode, 24 channels are displayed as BYTE A, BYTE B, and BYTE C, in Hex and Binary. The location of sample data is displayed on the left in decimal and hex. The trigger is displayed as an inverted memory location with the actual position shown in decimal and hex. The total number of channels sampled is displayed in the left corner (see figure 3-7 for State Display).

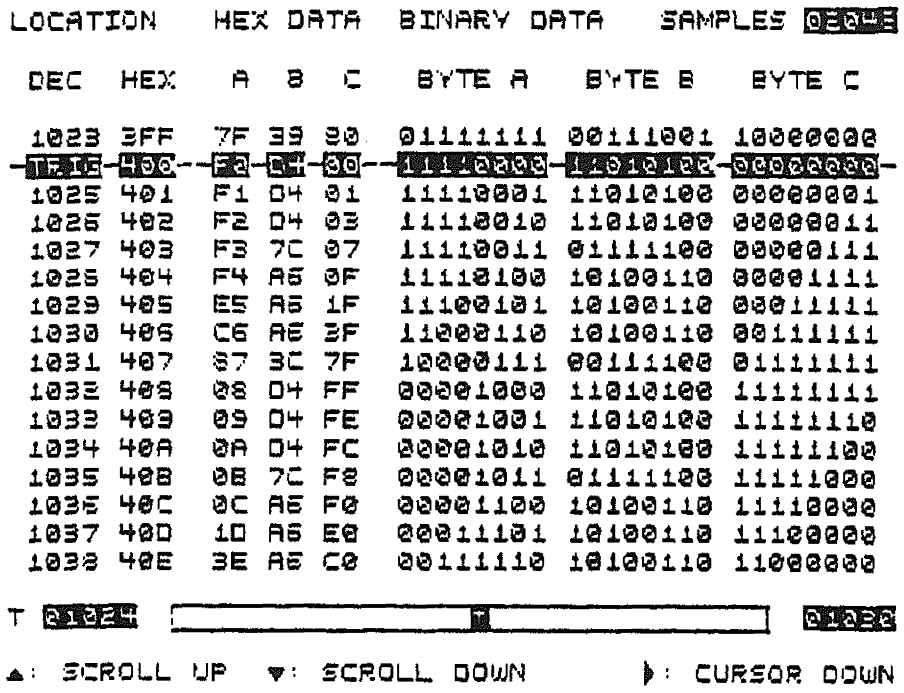


Figure 3-7 State Display

4.1 PROCEDURES TO SET UP THE ANALYZER FOR TIMING MODE

With power off, connect the Gould Timing Probe to the connector on the front of the instrument. Make sure the clips are locked.

1. Connect the GROUND lead to a point on the signal ground,
2. connect the EXT CLK lead to an external clock signal (if used),
3. connect the EXT TRIG lead to an external trigger signal (if used),
4. connect the remaining leads to the appropriate points on the equipment under test (Bit 0 - Bit 7), and
5. to avoid misleading random pickup, connect all unused input leads to Ground.

These are the three menus to set up the Timing :

1. TIMING , CLOCK SOURCE MENU,
2. INTERNAL SAMPLE CLOCK MENU (if Internal used), and
3. TRIGGER MENU.

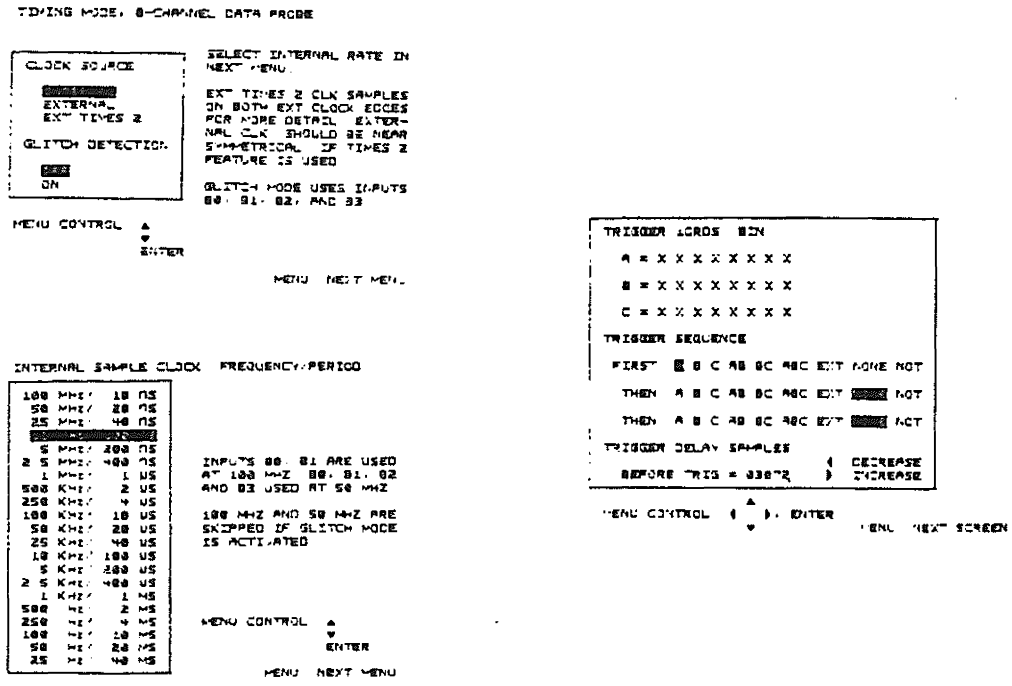


Figure 4-1. Timing Menus

4.2 TIMING, CLOCK SOURCE MENU

Using the Clock Source menu to set up the clock source and the glitch detection, select the desired clock source by moving to the appropriate field. Then press **ENTER**.

INTERNAL
EXTERNAL
EXT TIMES 2

If Glitch Detection is desired, move to:

GLITCH DETECTION

OFF
"ON"

and press **ENTER**. Remember, when glitch detection is ON, maximum sample frequency is 27 MHz.

To proceed to the next screen, press MENU.

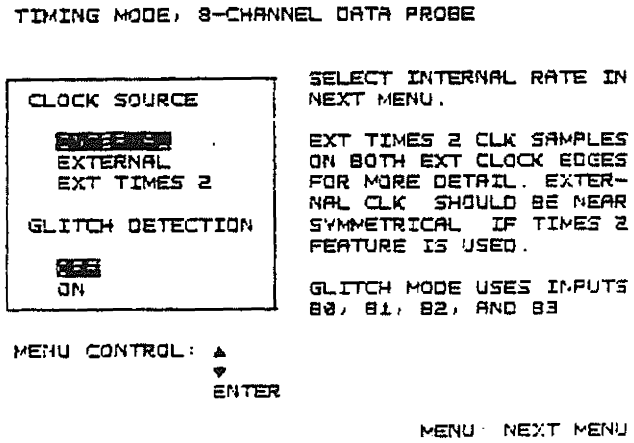


Figure 4-2. Clock Source Menu

4.3 INTERNAL SAMPLE CLOCK MENU

Using the Internal Sample Clock menu to choose the internal sampling rate, move to the desired frequency. Then proceed to the next screen by pressing **MENU.**

When GLITCH DETECTION is ON, 50 and 100 MHz sample rates cannot be selected.

4.4 TRIGGER MENU, TIMING

The Trigger Menu is used to set up qualifiers, to set up the trigger sequence, and to set up the trigger delay for the Timing .

The Trigger Menu contains three basic fields:

1. Trigger Words - used to compare with sample data for pattern match,

2. Trigger Sequence - used to set the sequence and combination of words, and

3. Trigger Delay - the number of samples taken before the trigger point.

WORDS: The least significant bits is on the right. **ENTER** steps through the values 0, 1, and X in the Trigger Words fields. X is the symbol for Don't Care. The three words are set to X (Don't Care) on power up.

TRIGGER SEQUENCE: Move right to the desired qualifier, combination of qualifiers, or **NONE** and press **ENTER**. The NOT field simply alters state when **ENTER** is pressed. The power on default for the trigger sequence is set to: FIRST A, THEN NONE, THEN NONE.

TRIGGER DELAY: Once the cursor is on the Trigger Delay Field, press right cursor key to increase the delay or left cursor key to decrease the delay. By keeping the switch pressed, the value will change increasingly faster. The power on default for TRIGGER DELAY is set to 3072.

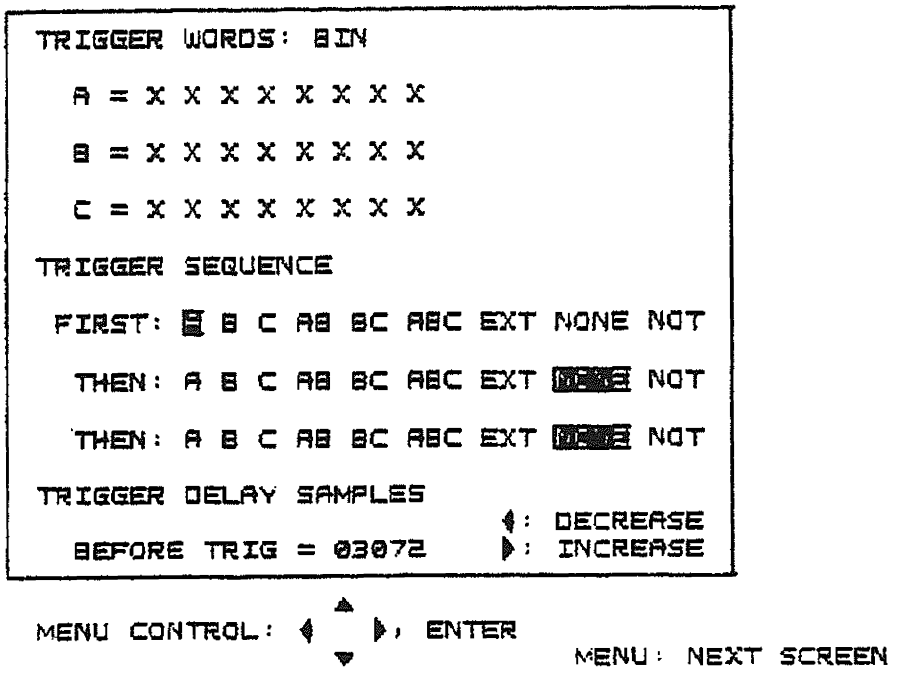


Figure 4-3. Trigger Menu

4.5 TIMING DISPLAY

In Timing, channels are displayed B0-B7, with the label on the left side of screen. Clock source is displayed in the upper left corner, with the sample rate displayed (if **INTERNAL** was chosen in the Clock Source Menu). Glitch detection **ON/OFF** is displayed midscreen at the top, and total samples taken is shown in the upper right corner.

4.5.1 WAVEFORM, TRIGGER, MEMORY MAP

Below the waveform display is a display of the system memory map. The "T" indicates the position of the trigger in memory. The sample position of the trigger is displayed to the left of the memory map and is set to 3072 samples on power on default. To the right of the memory map is the current position of the screen within memory; this is also shown as an inverted block within the memory map. As the display is scrolled through memory (Press the up cursor key to move up through memory, and the down cursor key to move down) the inverted screen block moves through the memory map. The trigger is indicated as a large inverted bar. Scrolling automatically slows down when the trigger is on screen.

4.5.2 NUMBER OF CHANNELS VS SAMPLE RATES

When the sample rate is set at 25 MHz or below, eight channels can be sampled and displayed (see figure 4-4) with a total of 6,144 samples. If Glitch detection is on, the total samples remains the same but only four channels can be samples (B0-B3). The display for Glitch detection is a sample channel followed by a glitch channel. Glitches appear as spikes directly below the area where the glitch occurred in the sample channel. When the sample rate is set at 50 MHz, data is taken on the first four channels, and at 100 MHz on the first two channels (see figure 4.4).

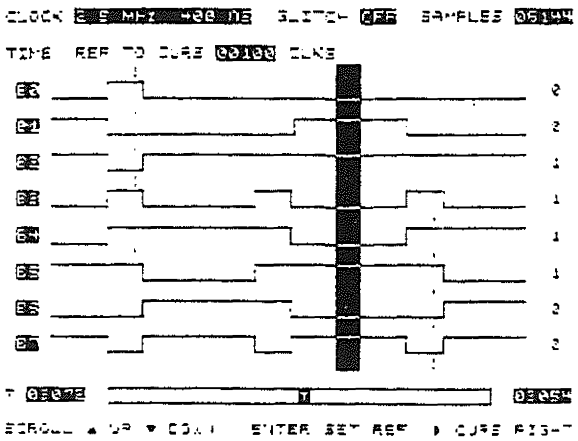


Figure 4-4. Timing Display

4.5.3 CURSOR, TIME MEASUREMENT, VALUE AT CURSOR

To position the cursor, press the right cursor key and the cursor will move to the right. When the cursor reaches the end of display, it will wrap around to the left portion and continue to move. The numeric value at cursor is displayed, on the right side of the screen. For a time measurement, place the cursor at the desired location and press **ENTER** to set the reference, then press the right cursor key to move the cursor to the desired position. The display for reference to cursor is shown above the timing display in number of clocks. This reference is in absolute clocks. The power on default is set at 100 clocks.

4.5.4 ARM-RUN

To perform data collection press the ARM-RUN switch once to "ARM" (start taking pre-data) then press again to collect data and trigger. To abort an invalid trigger condition, press HELP and the analyzer will abort data collection.

5.1 GOULD K20 LOGIC ANALYZER , STATE MODE

The following describes the procedures required to set up the analyzer in the State mode.

With the power turned off, connect the State probe to the connector on the front of the instrument. Make sure the clips are locked.

1. Connect the GROUND leads to points on the signal ground,

2. connect the CLOCK leads to external clock or qualifier signals,

3. connect the remaining leads (bit 0 - bit 23) to the appropriate points on the equipment under test, and

4. to avoid misleading random pickup, connect all unused input leads to Ground.

These are the two menus to set up State Mode:

1. State Mode Clocking Menu

2. Trigger Menu

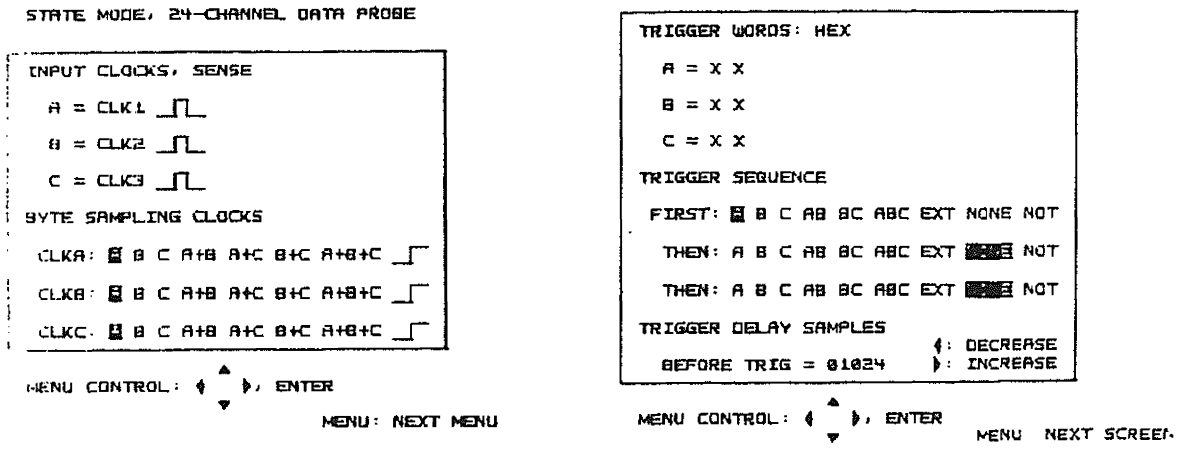


Figure 5-1. State Mode Menus

5.2 STATE MODE CLOCKING MENU AND OVERVIEW

State mode clocking allows a logical expression to be defined for the input clocks. There are three clock inputs to the state probe. These three clocks relate to the three defined sample clocks. CLK1 becomes CLKA, CLK2: CLKB, CLK3: CLKC. CLKA clocks in Byte A, CLKB clocks in Byte B, and so on. The displayed order is always Byte A, Byte B, then Byte C.

The three input clocks can be true or inverted. If the clock is to be active Low, select inverted for an input clock. Then an "OR" expression of the three input clocks is defined; it can also be true or inverted. A logical "AND" is created by inverting the input terms, choosing an "OR" expression, then inverting the result (Demorgan's Theorem). So any OR, NOR, AND, NAND expression of the three inputs can be defined.

Any input clock that is not used as an actual clock can function as an External Qualifier for another clock. CLK3 (CLKC) is the clock that actually causes memory transfer and must occur last in any phased sequence. For instance, in a multiplexed bus system that has an Address Strobe followed by a Data Strobe, the data strobe clock (in this example) must be connected to the CLK3 input. In a 6502 system, there is only one sampling clock, Phase 2. The trailing edge (falling) is used for all data transfers. The menu setup would be as follows:

- The three input cloks can be Active High ⎍⎍⎎ , indictated in text by TRUE and Active Low ⎏⎍⎍ indicated in text by INVERTED.

A = CLK1 ⎏⎍⎍ A = CLK1 ⎍⎍⎎

CLKA = A ⎍⎍⎎ or CLKA = A ⎏⎍⎍

CLKA = A ⎍⎍⎎ CLKA = A ⎏⎍⎍

CLKA = A ⎍⎍⎎ CLKA = A ⎏⎍⎍

CLK1 and CLK2 are not used and should be connected to Ground.

Because only one clock is used, the low-order address byte, the high-order address byte, and the data byte can be used as Byte A, B, and C in any order, but typically would be as follows:

Bits 0-7 ADDR HIGH, Bits 8-15 ADDR LOW, Bits 16-23 DATA.

Multiplexed buses will typically require more than one input probe on a given bus line.

ENTER toggles Active High or Active Low in the Clocking menu.

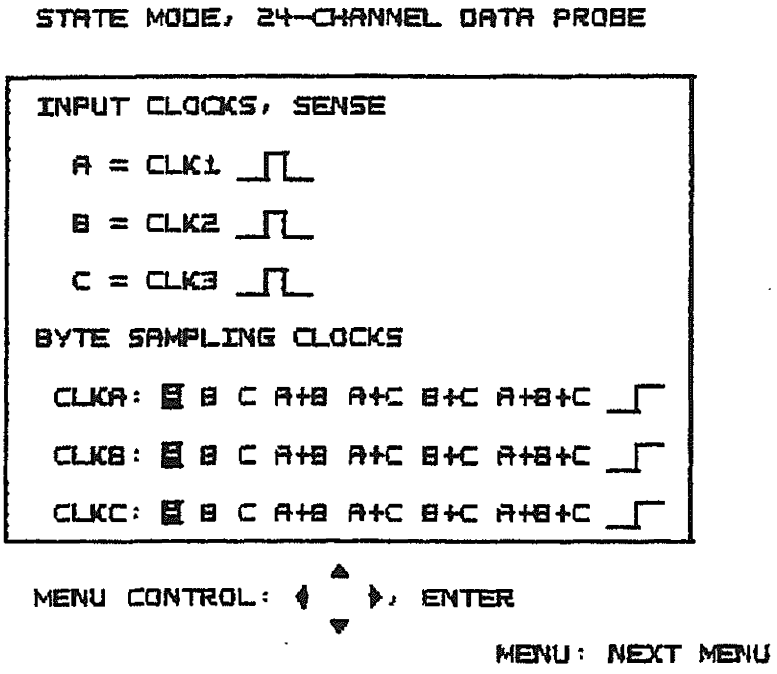


Figure 5-2. State Mode Clocking Menu

5.3 Trigger Menu, State Mode

The following describes how to use the Trigger menu to set up qualifiers, trigger sequence and trigger delay for State Mode.

The Trigger menu contains three basic fields:

1. Qualifiers used to compare with sample data for pattern match,

2. trigger sequence used to set the sequence and combination of qualifiers, and

3. trigger delay, the number of samples taken before the trigger point.

QUALIFIERS: The least significant bit is on the right. **ENTER** steps through the values 0, 1, and X in the qualifier fields. X is the symbol for Don't Care.

TRIGGER SEQUENCE: Move right to the desired qualifier, combination of qualifiers, or NONE and press **ENTER**. The **NOT** field simply alters state when ENTER is pressed.

TRIGGER DELAY: Once the cursor is on the Trigger Delay Field, press the right cursor key to increase the delay or the left cursor key to decrease the delay. By keeping the switch pressed, the value will change increasingly faster.

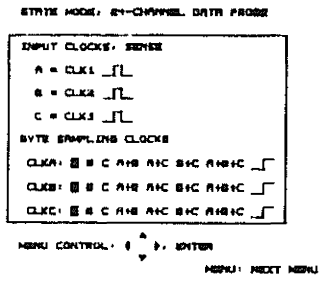


Figure 5-3. Trigger Menu

5.4 STATE DISPLAY

The total number of channels sampled with State probe is 2048 (see figure 5-4 for State Display).

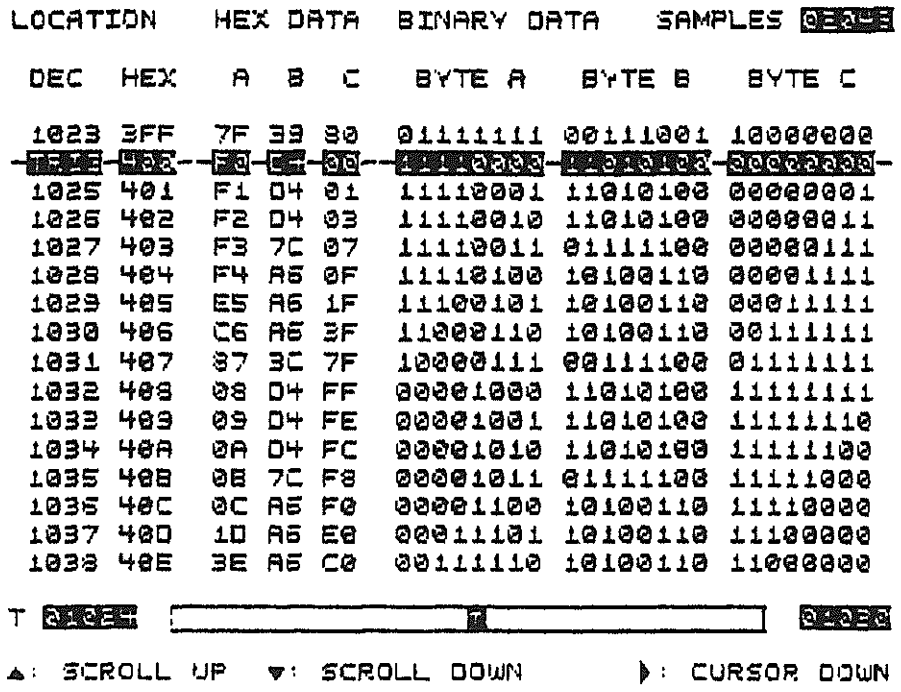


Figure 5-4. State Display

5.4.1 MEMORY MAP

As with the Timing mode display there is a display of the system memory map with "T" indicating the position of the trigger in memory and, the sample position of the trigger displayed to the left of the memory map and set to 3072 samples on power on default. To the right of the memory map is the current position of the screen within memory, this is also shown as an inverted block within the memory map. As the display is scrolled through memory (Press the up cursor key to move up through memory, and the down cursor key to move down) the inverted screen block moves through the memory map. The trigger is indicated as a large inverted bar. Scrolling automatically slows down when the trigger is on screen.

5.4.2 CURSOR

In State mode the cursor is for reference only. To position the cursor, press F6,and the cursor will move down. When the cursor reaches the bottom of the display it will wrap around to the top portion and continue to move.

5.4.3 ARM-RUN STATE MODE

To perform data collection, press the **ARM-RUN** switch once to "ARM" (start taking pre-data). Press again to collect data and trigger. To abort an invalid trigger condition, press **HELP,** and the analyzer will abort data collection.

6.1 GLITCH DETECTION, TIMING MODE

Glitch detection is available when the system is being used as a timing analyzer. When **GLITCH MODE** is **ON**, the unit takes sample data up to 25 MHz (27 MHz with External Clock) on four channels. It is a four Channel mode that is displayed as eight lines; the actual bit values (B), and separate lines (G) show glitch activity for a given bit line. A glitch is indicated as a single bit-width, positive-going pulse on a normally low-level line below a given bit line. The glitch lines "point" to the data lines above and indicate where glitches were detected.

6.2 STATE MODE CLOCKING, DETAILED

Operation of the analyzer in State mode, when using the standard State Mode probe, requires clock setup. The general-purpose State probe offers advanced clocking features that allow a logical expression of the three external clock inputs or qualifiers. This arrangement offers extreme versatility and is sufficient for most clocking requirements. The clocking setup for microprocessor or other circuitry under test must be studied and understood thoroughly. Data lines that are sampled typically are only valid during either the rising clock edge or the falling edge. Data may only be valid during a combination of the clock edge and some other combination of clocks and qualifiers that create the same result. Sometimes the right combination is very simple. Other times it can be very complex. Timing diagrams for the circuitry under test should be studied carefully. It is also necessary to understand the characteristics and features of the Gould general purpose State Mode probe. Clock setup for State mode is a hardware requirement when the user is actually more interested in analyzing software. However, it generally only needs to be done once for any given collection of hardware.

Below is a representation of the menu for State Mode Clocking as it appears on the Gould K20 screen. An explanation of the format and clocking characteristics will be given, followed by practical examples that should make clear how to use the Gould clocking features. When actually using the analyzer for general purpose State mode analysis, the menu Help message should be sufficient to set up clocking.

INPUT CLOCK, SENSE

A = CLK1
B = CLK2
C = CLK3

BYTE SAMPLING CLOCKS

CLKA: A B C A+B A+C B+C A+B+C
CLKB: A B C A+B A+C B+C A+B+C
CLKC: A B C A+B A+C B+C A+B+C

CLK1, CLK2, and CLK3 are the hardware clock and/or qualifier input lines on the Gould State Mode probe. These lines are also designated CLK1, CLK2, CLK3. In the menu, each of these inputs can be defined with a Sense, which means that the input can be active when it is logic level 0, as indicated by A = CLK1 INVERTED, or as logic level 1, as indicated by A = CLK1 TRUE, where the INVERTED version is not selected. In the Gould K20 Series, a logical 1 is a high-logic voltage level, and a logical 0 is a low-logic voltage level. Data latching (clocking) in the Gould K20 is done on the rising edge transition from a logical 0 (or low) to logical 1 (or high). The following three new intermediate logic variables are created as the Sense of each input is chosen: A, B, and C. These variables are either the TRUE (actual) version of the input, or the INVERTED version. These variables get further defined as logical expressions when the BYTE SAMPLING CLOCKS are defined next in the menu. These expressions, which can also be TRUE or INVERTED, can have up to three variables. Variables can be actual or inverse. The "+" sign in the expression represents a logical OR, not an arithmetic plus. The expressions of more than one term are OR expressions. Because, each input variable can be INVERTted, and the final result can be INVERTed (by Demorgan's Theorem), AND funtions can also be defined, because:

(CLK1) (CLK2) IS THE SAME AS [(CLK1¬⌐) + (CLK2 ¬⌐)]¬⌐

By using the OR expressions and by INVERTing the inputs and final results (as necessary, any OR, NOR, AND, or NAND expressions of up to three variables) can be defined.

With the Gould K20 in the 24-Channel State mode, three bytes are displayed in the state display; BYTE A, BYTE B, and BYTE C. These are clocked in by the three byte sampling clocks, CLKA, CLKB, and CLKC respectively. The order cannot be changed. However, the byte sampling clocks are defined by an expression based on input definitions, which allow the sampling order to vary. The display order still cannot vary. In the Gould K20 the CLKC must be the last to occur in any clocking sequence in which the three byte sampling clocks do not occur at the same time. The three clock inputs to the probe can be either in the form of actual clocks or as any form of qualifier. CLKA, CLKB, and CLKC, defined by the expressions, are the actual internal hardware clocks.

6.3 STATE MODE CLOCKING EXAMPLE, 6502 MICROPROCESSOR

The 6502 microprocessor uses a simple clocking arrangement. All data transfers, both Reads and Writes, are valid at the trailing (falling) edge of Phase 2. To capture all data transfers to and from the processor, only one clock input to the Data probe is necessary. All address lines are also valid at this same falling edge (at the end of Phase 2). The Read/Write (R/W) line is active High during Reads and active Low during Writes. The SYNC line is active High during OP CODE Reads.

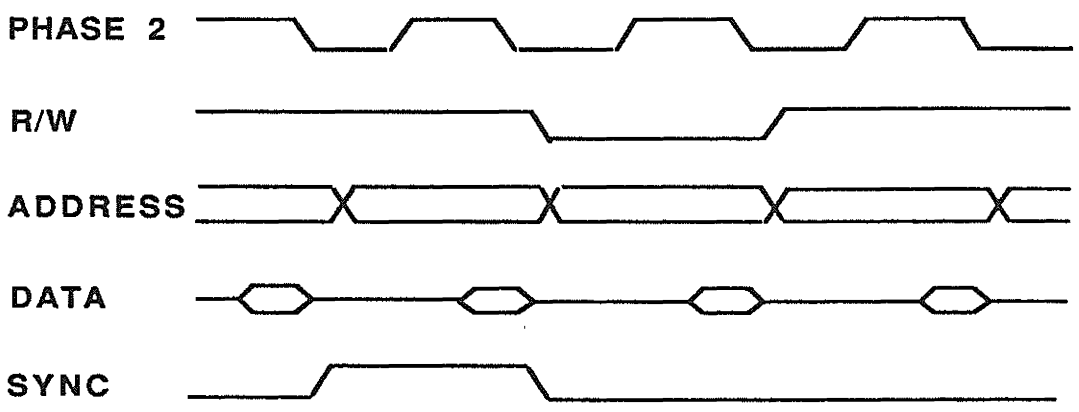


Figure 6-1. 6502 Timing Diagram, Simplified

To capture all data bus activity (all Reads and all Writes), refer to two of the several possible clocking menu setups:

A = CLK1 ⌐⌊⌐ A = CLK1 ⌐⌊⌐

CLKA = A ⌐⌊⌐ or CLKA = A ⌐⌊⌐

CLKA = A ⌐⌊⌐ CLKA = A ⌐⌊⌐

CLKA = A ⌐⌊⌐ CLKA = A ⌐⌊⌐

The setup on the right is preferred. The Phase 2 clock on the 6502 is an active High signal. NOTing of the final expressions is performed to allow the trailing edge of Phase 2 to be rising. This is compatible with the probe hardware. In the setups above, B for CLK2, or C for CLK3 could have been used.

A for CLK1 was used as the only necessary clock/qualifier input, and CLK2 and CLK3 were not used. Phase 2 of the 6502 (pin 39) must be connected to the CLK1 input of the Data probe. To display the 6502's Address Bus followed by the Data Bus, the following connections are required:

Model K20 Connections	**6502 Connections**
Bit 0 to Bit 7	AB8 TO AB15, pins 17, 18, 19, 20, 22, 23, 24, 25
Bit 8 to Bit 15	AB0 to AB7, pins 9, 10, 11, 12, 13, 14, 15, 16
Bit 16 to Bit 23	DB0 to DB7, pins 33, 32, 31, 30, 29, 28, 27, 26
GROUND	VSS, pin 21

In the state display, with these connections, the Address High Order byte is displayed as BYTE A, the Address Low Order byte as BYTE B, and the Data byte as BYTE C. This uses all 24 data input bits to the probe. If desired the display order could be changed by the pin connections on the 6502.

The 6502 example, shown above leaves two spare clock/qualifier inputs available on the data probe. One can be connected to the READ/WRITE line to capture only Read data, or only Write data. Or, one could be connected to the SYNC line, allowing only OP CODEs to be captured. For each, valid addresses will be captured. Additional clock qualifications as mentioned here, require the use of AND expressions.

Example

Using the Gould State probe with Data and Address connections listed above, capture all Read data activity of the 6502 and ignore all Writes.

This example requires a simple AND function of the Phase 2 clock and the Read/Write line. The Phase 2 clock is an active High line. Even though the falling edge of Phase 2 is the active edge, the clock itself is active High. Also, during Reads, the R/W line is active High. The required logical expression is as follows:

Clock = (Phase 2) AND (R/W)

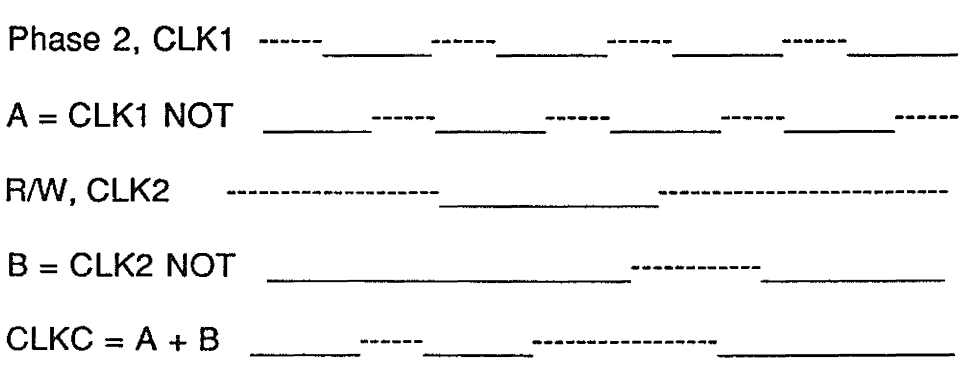
By Demorgan's Theorem:

(Phase 2) AND (R/W) = [(Phase 2 ⌝⌟) OR (R/W ⌝⌟)] ⌝⌟

With this result we have an active High clock that will only be true during data Reads. The trailing (falling) edge of the clock is the active edge, just as it is with the unqualified Phase 2. Because the State probe requires a rising clock edge, the final INVERTed term should be removed from the expression, leaving the following:

CLOCK = (Phase 2 ⌝⌟) + (R/W ⌝⌟)

This can be further illustrated with timing diagrams of the data probe clock inputs and the menu-selectable variables:



The rising edges of the bottom line are the points at which data are sampled. In this example CLKA and CLKB will be the same as CLKC since BYTES A, B, and C are all clocked at the same time. These are the menu setups for this example and the SYNC qualification example.

For 6502 Read Data Only:

Connect CLK1 on probe to Pin 39 (Phase 2) located on the 6502, and connect CLK2 on probe to Pin 34 (R/W) on 6502, then set menu:

A = CLK1 ⌐⌊⌐ , B = CLK2 ⌐⌊⌐ , C (not used)

CLKA: A+B, CLKB: A+B, CLKC: A+B

For 6502 Write Data Only:

Same as above, but change B = CLK2 ⌐⌊⌐ to B = CLK2 _⌐⌊_ in menu.

For 6502 OP CODE READ Data Only:

Connect CLK1 on probe, to Pin 39 (Phase 2) located on the 6502, and CLK2 on probe to Pin 39 (SYNC) located on the 6502, then set Menu:

A = CLK1 ⌐⌊⌐ , B = CLK2 ⌐⌊⌐ , C (not used)

CLKA: A+B, CLKB: A+B, CLKC: A+B

6.4 STATE MODE CLOCKING EXAMPLE, 8085 MICROPROCESSOR

The 8085 microprocessor, which has a more complex clocking arrangement than the 6502, uses clocking that is in some ways similar to the 8080 and Z80. There are separate READ and WRITE lines. Generally it is desired that all Read and all Write data are captured. This requires a logical OR term clocking expression. An understanding of the Read/Write data sampling for the 8085 applies directly to sampling in the 8080 and Z80.

The 8085 has a multiplexed data/address bus. This adds more complexity to the clocking requirements, as well as to the data connections.

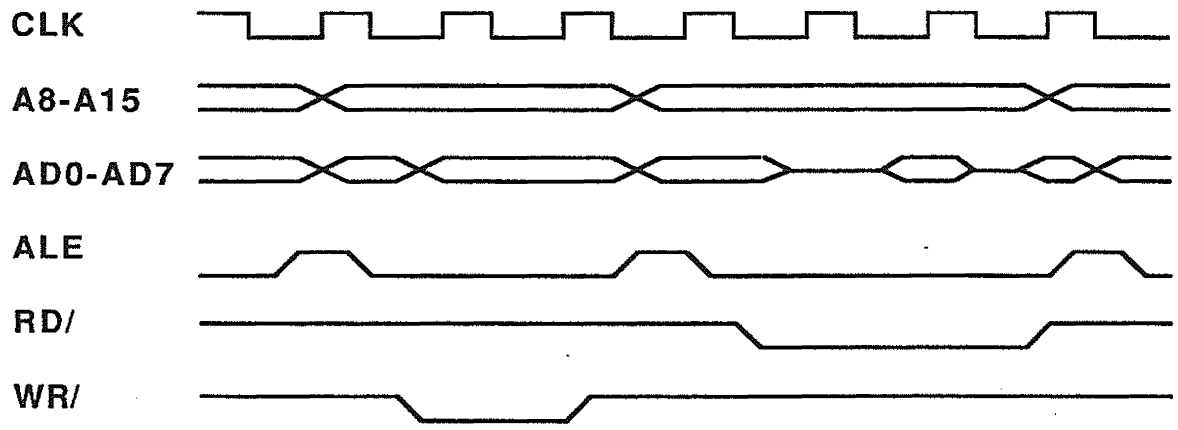


Figure 6-2. Simplified 8085 Timing Diagram

The State Data probe can easily handle the clocking requirements of the 8085 microprocessor. To capture all data Reads and Writes, the three clock/qualifier inputs to the data probe are used. The 8-bit multiplexed data/address bus has two probe input connections on each pin. Recommended data and address connections to the 8085 are as follows:

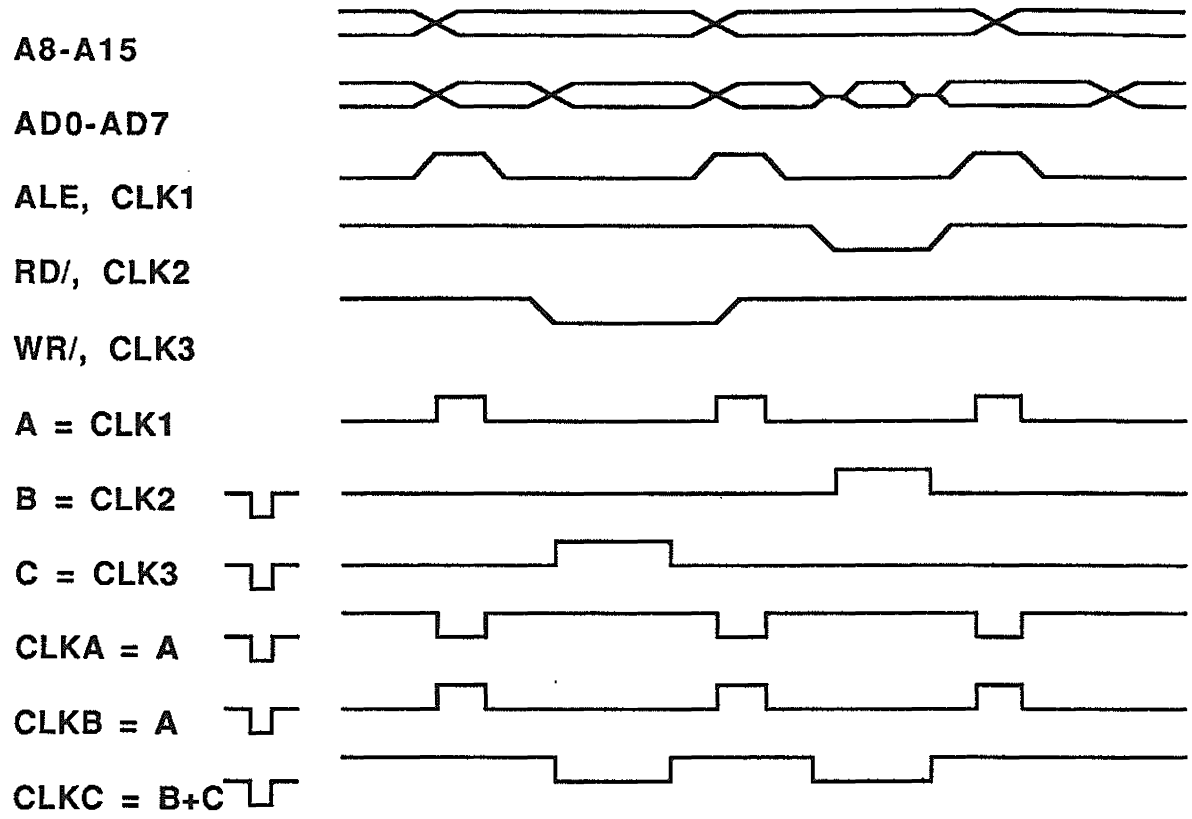
Model K20 Connections	8085 Connections
Bit 0 to Bit 7	A8 to A15, pins 21, 22, 23, 24, 25, 26, 27, 28
Bit 8 to Bit 15	AD0 to AD7, pins 12, 13, 14, 15, 16, 17, 18, 19
Bit 16 to Bit 24	AD0 to AD7, pins 12, 13, 14, 15, 16, 17, 18, 19
GROUND	VSS, pin 20

With these connections and the clocking recommended below, the address high-order byte is displayed as BYTE A, the address low-order byte as BYTE B, and the data byte as BYTE C in the State display.

In the 8085 clocking, the Address Latch Enable (ALE) line is used to demultiplex the address from the data of the common address/data lines. The low-order eight bits of address are valid at the trailing (falling) edge of the active High ALE signal. This line in its INVERTed form is the clock that is required to sample the low order address byte, BYTE B. This clock can also be used to sample the high-order eight bits of address, BYTE A, because they are also valid at the trailing edge of the ALE.

The data are valid on the common address/data bus at the trailing (rising) edge of either the RD/ line or the WR/ line. To capture all Reads and Writes, it is necessary to use a logical OR combination of these two lines. RD/ and WR/ are active Low signals; their senses should be defined as INVERTED versions of the clock inputs to the probe. An OR expression of active low variables creates an active Low result. To create an active High result (rising edge clock) for the data probe, the final OR expression should also be INVERTed. This is also true for CLKA and CLKB.

This is illustrated below with timing diagrams of the data probe clock inputs and menu selectable variables, with data and address included for reference.



The rising edges of CLKA, CLKB, and CLKC are the actual hardware sampling points for address and data. CLKC will be the last clock to occur in each machine cycle of the 8085. As required by the probe, CLKC must always be last to occur in any clocking sequence.

For 8085 READ and WRITE data sampling:

Connect CLK1 on probe, to pin 30 (ALE) on 8085, CLK2 on probe to pin 32 (RD/) on 8085, and CLK3 on probe to pin 31 (WR/) on 8085, then set menu:

A = CLK1, B = CLK2 ⌐⌐, C = CLK3 ⌐⌐

CLKA: A ⌐⌐, CLKB: A ⌐⌐, CLKC: B+C ⌐⌐

6.5 TRIGGERING

The Gould K20 Series Logic Analyzer offers sophisticated triggering capabilities as standard features: Three independent qualifiers, an external trigger qualifier and three independent eight-bit pattern recognizer/qualifiers for use with the State mode. There are three levels of sequence recognition that use the three qualifiers. Trigger can be delayed to any point within sample memory. This allows the user to choose the amount of pre-trigger data (occurring before the trigger point) or the amount of post-trigger data (occurring after the trigger point). Either amount can vary from zero to 100 percent of the sample memory.

6.5.1 TRIGGER QUALIFIERS

There are three pattern recognizer/qualifiers. Each qualifier is eight-bits wide; any combination of the eight bits of a qualifier can be selected. Each bit may be defined as a logical 0, logical 1, or logical X (don't care). The bit order for the qualifiers 76543210, corresponds to the bit order of the eight bits of data input to the Timing probe. Bit 0 of the probe corresponds to bit 0 to each trigger qualifier. The other bits correspond in the same manner. The three qualifiers are labeled A, B, and C. In Timing mode they are totally independent of each other. In State mode each qualifier relates to one of the three input data bytes to the state probe. Qualifier A relates to BYTE A of both the state probe and the state display. Qualifier B relates to BYTE B, and qualifier C to BYTE C. Each qualifier relates to only one input data byte. The significance of this should be apparent in the description of the trigger sequence (see below). Bits 0 to 7 of qualifier A relate to bits 0 to 7 of BYTE A of the data probe and in the state display. Bits 0 to 7 of qualifier B relate to bits 8 to 15 of BYTE B. Bits 0 to 7 of qualifier C relate to bits 16 to 23 of BYTE C. It is generally not necessary in state mode for each bit of a qualifier to be settable to a logical Don't Care; however, this feature is available just as in Timing mode.

6.5.2 TRIGGER SEQUENCE

The K20 can be triggered only after a particular sequence of events that are made up of occurrences of the trigger qualifiers A, B, or C, or the external qualifier, or any of their inverses. The number of sequences is set in the menu. Any sequence that has been selected as NONE (or None Not) will be ignored. Any two NONE's selected in the sequence fields will create a one-level sequence requirement for triggering. If any one NOT is active, a two-level sequence is necessary for triggering. If there are no NOT's active, a three-level sequence of events is required. When all sequence fields are disabled by setting NONE active in all lines, a zero-level sequence is created; this is how a manual trigger condition is specified. Triggering occurs immediately after the trigger delay times out after the ARM-RUN switch is pressed the second time. If all the bits of a trigger qualifier are set to Don't Care, they act the same as a NONE in a sequence field. If all the bits have been specified as Don't Cares, they are ignored if selected.

6.5.3 TRIGGER, TIMING MODE

In Timing mode, all of the qualifiers, A, B, and C relate, to the same eight bits of data from the timing probe. Choosing a sequence of these qualifiers is straightforward. A, B, and C can be in any order. The trigger sequence AND functions of the three qualifiers, AB, BC, and ABC, are not normally used in the Timing mode. Some examples of Timing mode trigger sequence selection follows. A two-line compact form of the trigger menu is used for the examples.

Example 1

A = XXXXXXX1 B = XXXXXXX0 C = XXXXXXX1

FIRST: A THEN: B THEN: C

In this example, a 1 must first be detected on bit 0 of the input data. Then bit 0 must change to a 0, and back to a 1. Equivalent sequences would be: A then B then A, or C then B then C, or C then B then A, or A then A NOT then A, or B NOT then B then B NOT. The Don't Care bits have no affect on the result whether the result is True or if it gets NOTed. This is true whenever the qualifier has at least a one 0 or a 1 in it. The special case where all eight bits are X, is valid when the NOT is not active in the sequence fields. However, if the NOT is active, an impossible condition will be specified that will cause the sequence to be hung up, since:

XXXXXXX0 NOT = 1, XXXXXXX1 NOT = 0, XXXXXXXX NOT is undefined

Example 2

A = 00110011 B = 00110000 C = 11110000

FIRST: A THEN: A THEN: B

This sequence appears to be the same as: A then NONE then B, or NONE then A then B. It looks as if the two identical and consecutive sequences, A then A, will instantly fall through and act as a single sequence. However, the two A sequences will not be sampled at the same time, but will be separated in time by one clock cycle. This can be used to advantage in asynchronous (Timing mode) sampling as a digital pattern duration filter.

Example 3

A = XXXXXXX0 B = XXXX1111 C = 00000000

FIRST: A THEN: C THEN: C NOT

The first sequence occurs when a 0 is detected on bit 0 of qualifier A. Because of the Don't Cares, there are 128 possible patterns of 8 bits that will satisfy this condition. The second sequence is completely specific. There is only one pattern out of 256 possible patterns that will satisfy the condition. The third sequence, because of the NOT term, is very unspecific. There is only one pattern that will not satisfy the condition, and 255 patterns that will. When more than just a few of the bits are active (0 or 1), use of the NOT's in the Sequence fields must be done with care.

Example 4

A = 00110011 B = 00110000 C = 11110000

FIRST: EXT NOT THEN: A THEN: NONE

An active low external trigger is used here, possibly the hardware RESET line of a microprocessor. The external trigger must first go Low. Then the pattern specified by qualifier A must occur.

Example 5

A = XXXXXXX1 B = XXXXXXXX C = XXXXXXXX

FIRST: A THEN: NONE THEN: NONE

The sequence is complete once bit 0 goes High one time. This is similar to the limited single-channel triggering capability of a common oscilloscope.

Example 6

A = 00110011 B = 00110000 C = XXXXXXXX

FIRST: NONE THEN: NONE THEN: NONE NOT

Example 7

A = 00110011 B = 00110000 C = XXXXXXXX

FIRST: C THEN C: THEN: C

Either of the two setups above will specify a manual trigger. Triggering occurs immediately after the trigger delay times out (after the ARM-RUN switch is pressed the second time).

6.5.4 STATE MODE TRIGGERING

In State mode, the three qualifiers A, B, and C relate to BYTE A, BYTE B, and BYTE C of the State probe and the state display. The displayed order of the three bytes is BYTE A, BYTE B, then BYTE C. In the sequence fields of the trigger menu, the AND combinations of the A, B, and C qualifiers (AB, BC, and ABC) are used to form wider (16- bit and 24-bit) qualifiers. When eight-bit qualifiers are ANDed to form wider qualifiers, the available number of sequence levels is affected. This is demonstrated in the examples shown below. Again, as was done for Timing mode, a two-line compact form of the trigger menu is used, but in a form that is slightly different from that used for the Timing mode. In State mode, it is common to consider data in hexadecimal format. For reference the hex representations for each of the three qualifier bytes have been added to the left of each binary byte.

Example 1

A = 0F 00001111 B = 59 01011010 C = 4C 01001100

FIRST: A THEN: B THEN: C

The sequence is complete when pattern A occurs on BYTE A, then pattern B on BYTE B, then pattern C on BYTE C. There are three sequence levels, and each level has a distinct eight-bit qualifier associated with it.

Example 2

A = FF 11111111 B = 3E 00111110 C = 40 01000000

FIRST: ABC THEN: NONE THEN: NONE

In this example, the three, 8-bit qualifiers have been ANDed into one 24-bit qualifier (ABC in the sequence line). The one-level sequence will be complete the first time the three byte pattern below occurs across all 24 bits, simultaneously.

Hex FF 3E 40, Binary: 11111111 00111110 01000000

In example 1, three sequence levels were defined. There were three distinct qualifiers that could be used in defining the sequence, even though each one was only eight-bits wide. In example 2, there was only one distinct 24-bit qualifier defined, the AND combination ABC. Since all three of the 8-bit qualifiers were used up in forming ABC; there can be only one distinct 24-bit qualifier in any given sequence. If two 8-bit qualifiers are ANDed (AB or BC in a sequence line) to form one 16-bit qualifier, then two distinct qualifiers will be available for use in the trigger sequence, one 16-bit and the remaining 8-bit qualifier. Combining the 8-bit qualifiers to form wider qualifiers affects their specific use in a sequence. However, there are always three sequence levels available that may include distinct 8-, 16-, or 24-bit qualifiers, their Boolean inverses, any of the three 8-bit qualifiers (even though they may already be defined as part of a wider qualifier), or the True or NOT version of the external trigger input; any may be repeated.

When BYTEs A, B, and C are discussed in the examples below, it is assumed that a typical eight-bit microprocessor system is being analyzed in State mode, and that the three bytes of data coming into the state probe, and displayed in the state display, relate to BYTEs A, B, and C in the following manner. BYTE A is the high-order-byte of the 16-bit address of the microprocessor, with bit 15 on the left. Byte B is the low-order address byte, and Byte C is the data byte. The displayed order in the state display will be address high-byte, address low byte, then data byte. The order of the 24 bits is shown below, the same order that is typically used with optional microprocessor probes. However, when using the general purpose state probe, the bit order may be set as desired by simply changing the input connections to the probe.

A15, A14, A13, ..., A0, D7, D6, D5, ..., D0

Example 3

A = 08 00001000 B = 30 00110000 C = 8D 10001101

FIRST: AB THEN: C THEN: NONE

The sequence is complete the first time the hex value 8D appears on the data bus, after the hex value 0830 appears at least once on the address bus.

Example 4

A = 08 00001000 B = 30 00110000 C = 10001101

FIRST: ABC THEN: ABC THEN: ABC

A 24-bit qualifier has been specified. This could be the address and data at the entry point of a subroutine. The sequence will be complete the third time the subroutine is entered. The data byte would be redundant in this example, because the 16-bit address totally defines the entry point of the subroutine. This address could have been the hardware location of an input device, If this is true, the sequence would be complete once the same data value (hex 8D) occurred at the input port three times.

Example 5

A = F0 11110000 B = 30 00110000 C = 8D 10001101

FIRST: A THEN: C THEN: A NOT

The software that is executing must first enter Page F0 of the address space. The sequence will be complete as Page F0 is exited after hex 8D has appeared on the data bus.

Example 6

A = 37 00110111 B = DB 11011011 C = C4 11000100

FIRST: EXT NOT THEN: ABC THEN: C

In this example the external trigger line is used and is connected to the IRQ line on the microprocessor. The trigger sequence is complete once the IRQ (Interrupt Request) is pulled Low, data hex C4 occurs at address Hex 37DB, and the same data byte occurs at any other address.

6.5.5 TRIGGER DELAY

A complete trigger definition requires one more element in addition to those previously discussed. The qualifiers are first defined in the trigger menu. Then a sequence of events based on the internal qualifiers and the external trigger qualifier is selected. The final condition for triggering is the amount of delay, measured in clock cycles, that precedes (and follows) the point where the sequence was complete and triggering actually occurred. The delay in the trigger menu is specified as the number of samples before trigger. Because the total number of samples is a fixed amount, this also sets the numbers samples that will follow the trigger point. In eight-bit Timing mode, the total number of samples is 6144. If the trigger delay samples before Trig is set to 2000, then the number of samples after the trigger point will be what remains, 4144. The trigger point will always exist somewhere within the sample memory. If the number of samples before Trig is set to 0000, then the trigger point will be at the very beginning of the sample memory. The value 6134 puts the trigger point at the end of memory. The value 3072 puts the trigger at the center of memory. The total number of samples varies with the modes of the K20 Analyzers. This information is listed below, and also appears in the Timing and State displays.

Model K20	Total Number of Samples
Timing, 100 MHz	24,576
Timing, 50 MHz	12,288
Timing, to 25 MHz	6,144
Timing, Glitch Detection	6,144
State, 24-bit, Standard probe	2,048

6.6 TRIGGER DELAY

Trigger delay, which allows the user to position the trigger anywhere within the sample memory, is simply the number of samples the analyzer will take before the trigger point. By using the trigger delay, the trigger can be placed anywhere within the sample memory. To set the delay, (in the Trigger Setup menu for both Timing and State modes), move DOWN to trigger delay. The cursor will begin to flash. To increase the delay, press the righ cursor key and the delay counter will begin to increase. Pressing the left cursor key causes the delay counter to decrease. Once the proper delay is set, press MENU to proceed to the next screen.

6.7 ARM-RUN

To start sampling data, press the switch labelled ARM-RUN. This key requires two closures to complete a sample. When ARM-RUN is pressed, the memory pretrigger data starts filling. There is a 1/2 second delay allowed for the pre-data to complete. This is typically long enough at most sample rates. When very slow clocks are used externally or from the Timing probe, more time may be required. At 25 Hz it can take up to 80 seconds. Press HELP to abort a long sample or one that cannot find a valid trigger condition.

When ARM-RUN is pressed the second time, the sample completes by filling the remainder of the sample memory with data that occurred after the trigger condition.

6.8 RESET

If for some reason the system fails to respond, press **ENTER** and **ARM-RUN** simultaneoulsy. This will cause a hardware reset. Setups in memory remain as they were, and the Reset Entry Screen is displayed. This procedure will not be necessary unless the internal processor gets lost because power line transients or other factors.

If the system is in Timing or State display and cannot find a trigger condition, press the HELP switch to abort the sample and to return to the Timing or State display.

7.1 ANALYSIS EXAMPLES

The training/test card is intended as a training aid to help guide the user through the operation of the K20 logic analyzer.

7.1.1 TRAINING/TEST CARD DESCRIPTION

The logic analyzer training/test card is an option that allows you and your coworkers to rapidly familiarize yourselves with the basic and advanced features of the Gould K20 Logic Analyzer series. The training/test card consists of 5 ICs that generate sample signals for use in state and timing demonstrations. The card uses a 3 volt 150 MAH battery and has 24 signal pins, 3 clock pins, a ground, and one glitch pin. The oscillator on the card runs at approximately 220 KHz (see figure 7-1).

7.1.2 CONNECTING TEST LEADS TO THE TRAINING/TEST CARD

With the test lead set disconnected from the probe, connect the Black test lead set to the first 6 bits, the Red test lead set to the second 8 bits (bits 7-16), and the White test lead set to third 8 bits (bits 17-23). Now connect the clocks, Black set gray lead to CLK1 on the training/test card, Red set gray lead to CLK2, and White set gray lead to CLK3.

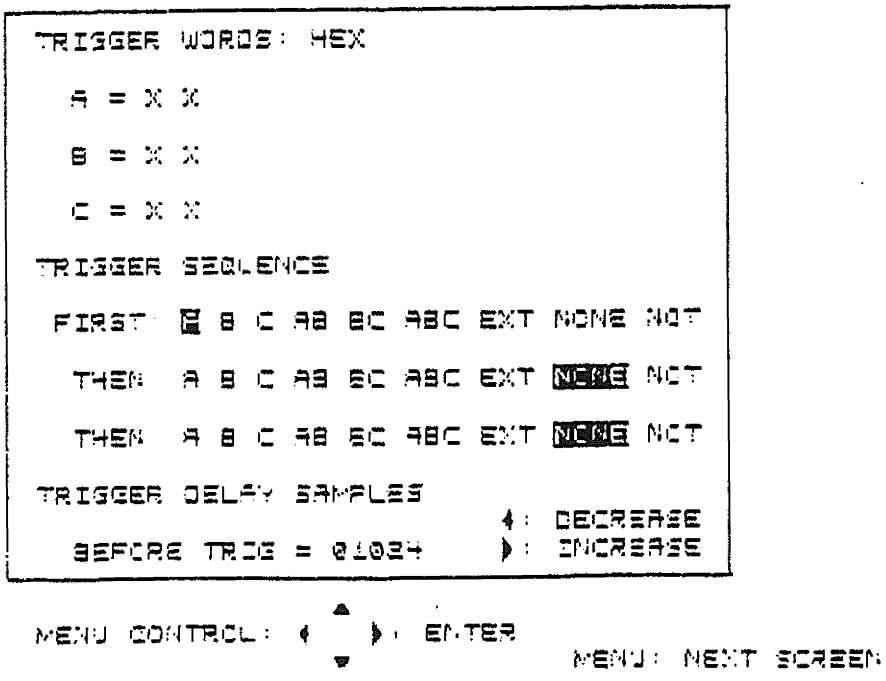


Figure 7-1. Training/Test Card

7.2.1 BASIC TIMING ANALYSIS

With power off, plug in the Timing Probe, connect the ground lead to the card and turn on the analyzer. Then, plug in the Black test lead set to the probe. The first screen is the clock source menu. Set the clock source to **INTERNAL** and Glitch detection OFF. Next press **MENU** to proceed to the internal sample clock menu. Step to a sample rate of 2.5 MHz, then proceed to the trigger menu. Step to the first trigger sequence field, (the default sequence will be set to "FIRST A, THEN NONE, THEN NONE") change the first sequence to "NONE" (this is a manual trigger). The samples before trigger is set to 3072, to change samples before trigger press the right cursor key to increase, the left cursor key to decrease (see figure 7-2 for trigger menu). Press **MENU** to move to the Timing display.

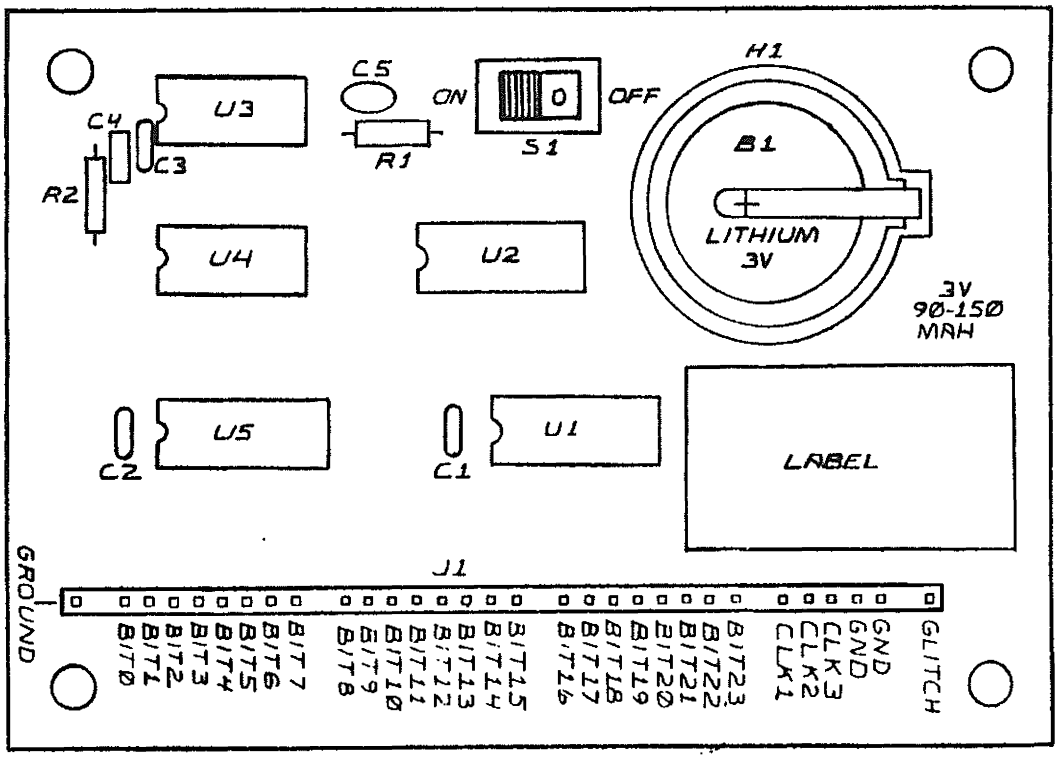


Figure 7-2 Trigger Menu

7.2.2 CAPTURING SAMPLE DATA

Once in the Timing display, sample data is captured by Pressing the **ARM-RUN** key. A flashing "ARMED" will appear just above the numeric screen position indicator. Then press **ARM-RUN** again to take a capture sample data (see figure 7-3)

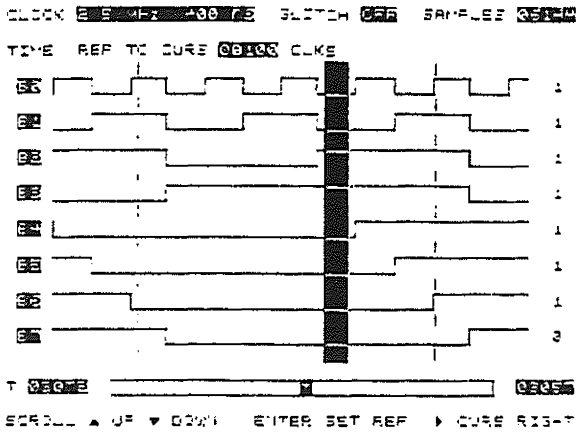


Figure 7-3 Timing Display

7.2.3 CURSOR AND TIME MEASUREMENT

To move the cursor, press the right cursor key. The cursor will move to the right and wrap around the display. In this example move the cursor to a rising edge of B1 (see figure 7-4). Notice the bit display on down the right side of the screen.

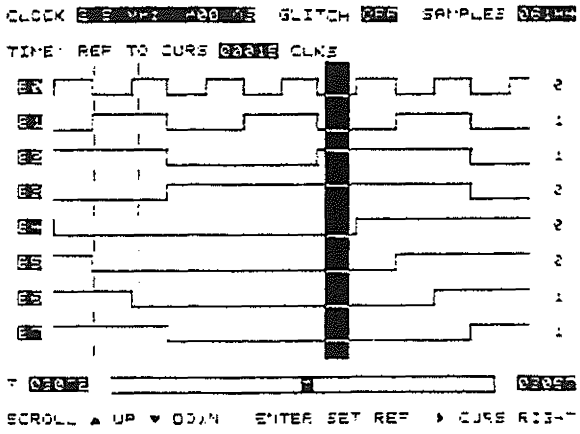


Figure 7-4. Setting the Cursor

To make a time measurement, press **ENTER** to set the reference at the point where the cursor is displayed. Once the right cursor key is pressed, the reference cursor will move to the cursor position. Pressing the right cursor key will move the cursor to the right, and the time reference in clocks is displayed above the timing display (see figure 7-5).

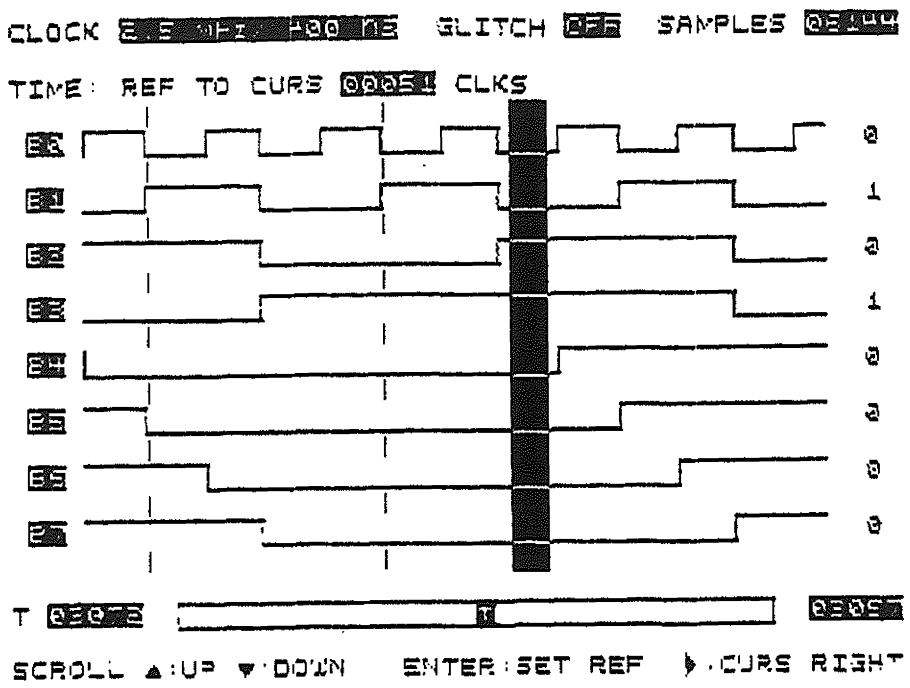


Figure 7-5. Time Measurement

7.2.4 **TRIGGER**

Step to the trigger menu, and set trigger word A to XXXX1111 (XF in hex) and B word to XXXX0000 (X0 in hex). Now, set the sequence to FIRST A, THEN B, THEN NONE. Sampling data in this mode will trigger at the reload point for the synchronous counter (see figure 7-6).

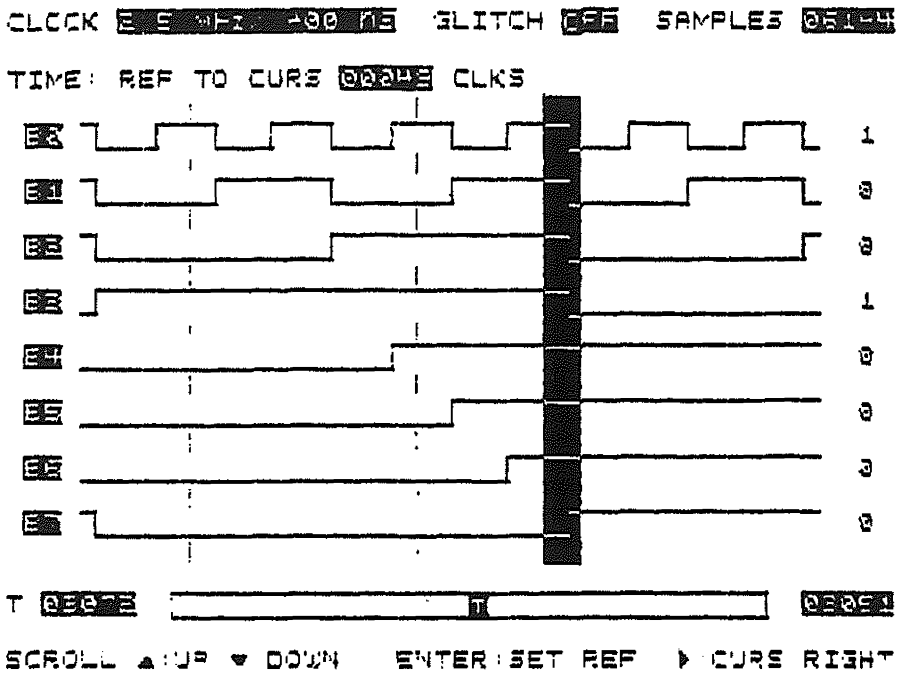


Figure 7-7. Timing Display, Edge Trigger

In the example above we have set the analyzer to edge trigger on the first four bits. An alternative approach is to set up trigger word and then set the trigger sequence to be: FIRST A, THEN A NOT THEN NONE.

7.2.5 GLITCH DETECTION

For the a demonstration of glitch detection first turn off the card. Then, disconnect the black test lead set and connect the Red set to the Timing probe. Turn on the card, and move to the Clock Source menu (the first menu), step to **GLITCH DETECTION** and press enter when the cursor is at the ON field. Move to the timing display (by pressing Menu) and press **ARM-RUN** to collect sample data. Glitches will appear on the screen as spikes going high just below the location where the glitch occurs, note the glitch on bit 1 (see figure 7-7).

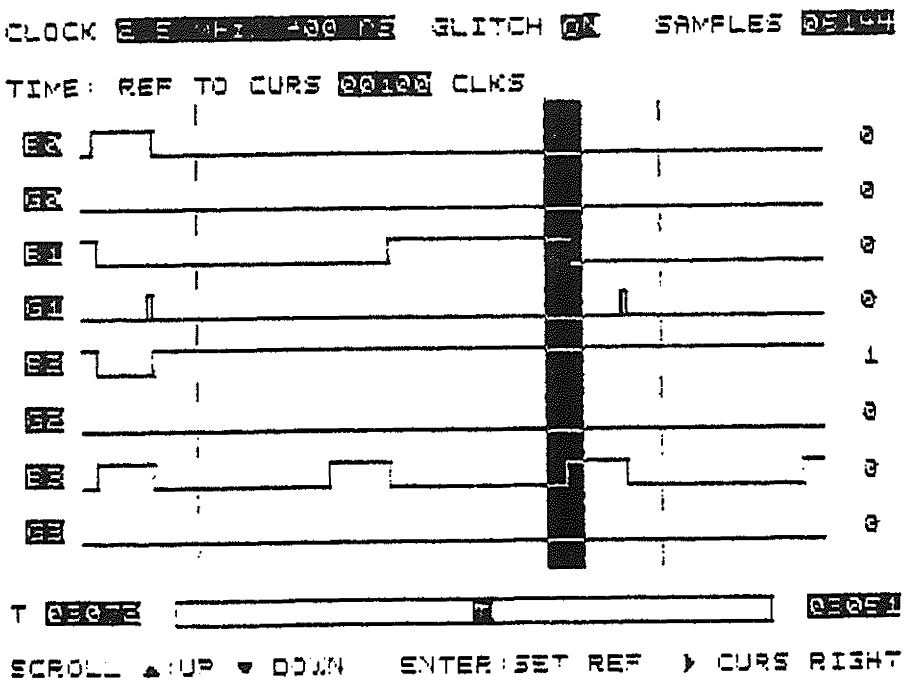


Figure 7-7 Timing Display in Glitch Detect Mode

7.3.1 BASIC STATE ANALYSIS

Turn off the training/test card and then the analyzer. Disconnect the Timing probe and connect the State Probe. Now, connect the Black test lead set to byte A, the Red test lead set to byte B, and the White test lead set to byte C.

The first menu for state mode is the Clocking menu. The clocks can be set to active high or active low (indicated by the inverted NOT next to CLK1, CLK2, and CLK3). Set all the clocks active, then proceed to the the fields labeled BYTE SAMPLING CLOCKS, and set each to A.

7.3.2 TRIGGER MENU, STATE

Press the menu key to move to the trigger menu, the three trigger words will be displayed in HEX. Set the A trigger word to F0 and step to trigger sequence. Set the trigger sequence to FIRST A THEN NONE THEN NONE. Press the menu key to move to the State display and press ARM-RUN to collect sample data. The state pattern will repeat every 16 clocks or one screen (see figure 7-8).

```
LOCATION    HEX DATA   BINARY DATA     SAMPLES
 DEC  HEX    A  B  C    BYTE A    BYTE B    BYTE C

 1025 401   F1 D4 01   11110001  11010100  00000001
 1026 402   F2 D4 03   11110010  11010100  00000011
 1027 403   F3 7C 07   11110011  01111100  00000111
 1028 404   F4 A6 0F   11110100  10100110  00001111
 1029 405   E5 A6 1F   11100101  10100110  00011111
 1030 406   C6 A6 3F   11000110  10100110  00111111
 1031 407   87 3C 7F   10000111  00111100  01111111
 1032 408   08 D4 FF   00001000  11010100  11111111
 1033 409   09 D4 FE   00001001  11010100  11111110
 1034 40A   0A D4 FC   00001010  11010100  11111100
 1035 40B   0B 7C F8   00001011  01111100  11111000
-1036-40C--0C-A6-F0--00001100-10100110-11110000-
 1037 40D   1D A6 E0   00011101  10100110  11100000
 1038 40E   3E A6 C0   00111110  10100110  11000000
 1039 40F   7F 39 80   01111111  00111001  10000000

T

▲: SCROLL UP   ▼: SCROLL DOWN   ▶: CURSOR DOWN
```

Figure 7-8. State Display

APPENDIX

Acquisition — The process by which input logic signals are compared at a discrete instant to a threshold level and recorded.

Active Clock Edge — The clock transition on which all receivers (listeners) interpret the data on the bus. A logic analyzer must monitor the system using the same active edge as the clock.

Address Bus — That bus in the system used to address or define the memory or device location enabled.

Aliasing — The misleading display of sampled analog waveform when the sample rate is less than twice the input frequency.

Arm — An input or condition that must occur prior to the analyzer trigger conditions being recognized.

ASCII — American Standard Code for Information interchange; a standard alphanumeric code defining a character set.

Assemble — To combine routines to form a program; to translate a source program into a machine language, usually producing one or more machine language instructions for each source language instruction.

Assembly Language — Asynchronous Clocking Data are clocked into the logic analyzer at a rate unrelated to the system under test.

Asynchronous Data — Data that are not referenced to time. The completion of one operation signals the next operation.

Asynchronous Trigger — Triggering of timing analyzer by signals independent of the analyzer clock.

Automatic Test — A capability of some analyzers that allows the storage of a partial or complete test procedure, plus the expected results, in an auxiliary memory. Tests are then executed with minimal user intervention.

Auxiliary Memory — Space in memory in addition to the active recording memory. It may include RAM and PROM and is used in comparing data, halting on difference, automatic testing and other functions.

Baud Rate — The number of symbols per second that are transmitted (a symbol normally consists of one bit).

Block Transfer — The movement of a group of fields from one group of addresses to another group of addresses.

Breakpoint — A point in a program in which a process(or) may be made to stop automatically for a check on the progress of the data handling (see Emulator).

Bus System — A network of paths or set of lines that facilitate data flow in a digital system. The common buses are the Address, Data, and Control.

Clock — The pulses that control the timing of operations in a digital system; some systems having more than one clock. Both the system and any monitoring instrument must interpret the data on an active clock edge when all data are valid.

Clock Delay — The number of clock occurrences before an event.

Combinational Trigger — The pattern of 0s, 1s and "Don't Cares" set on all channels that, when matched by the sampled data, causes a trace to commence.

Comparator — A circuit that compares two or more signals and supplies an indication of their agreement or disagreement to initiate some other action.

Compare Data — Any form of display in which a captured data record is manipulated with the data set in auxiliary memory in such a way as to make differences conspicuous. Two examples: the "exclusive-OR" display and rapid alteration of the display between recording and auxiliary memories.

Compiler — A routine by which a computer can translate a source program into an object program by assembling and copying from other programs stored in a library of routines.

Composite Video — An analog signal containing not only display information but also horizontal and vertical synchronizing pulses, all of standard polarity and size.

Contents — The word or field stored at a given address or in a given register.

Controls Character — A character embedded in operand data that specifies an operation to be performed, such as skip to a new page while printing output data.

Correlation — A comparison function; a figure of merit, indicating the number of similarities relative to the number of differences between two elements.

Cross-Domain Linkage — Linkage between the state and timing domains.

Data Compression — Any display technique intended to reduce the time or effort required to examine an entire data record. The simplest form converts binary words into hexadecimal words.

Data Domain — A domain concerned with the total amount of data that must be collected every event/time to characterize synchronous systems behavior. A logic analyzer is a data domain monitoring instrument.

Data Qualified Clocking — Specifying a data pattern that is logically ANDed with the clock to exclude "non- qualified" clock occurrences.

Data Rate — The clock rate for synchronous systems; it must not exceed the specified maximum clock rate of the analyzer.

Debugger — A program used to facilitate testing of a microprocessor system.

Dedicated Pod — A pod used to examine a particular microprocessor chip. It is by clipping over the processor and passively monitors its state transactions.

Delay — User-set for an N-count of selected events. Delay is used to offset in time the position of final data record with respect to the trigger event (see Trigger Delay).

Demultiplexing — The sorting of multiple signals that time-share a signal path into dedicated lines (channels).

Disassembly — The reverse of assembly; to convert machine language code into user recognizable mnemonics, usually performed with the help of a dedicated pod.

Don't Care — A channel that may be in either State "0" or State "1", symbolized "X", thereby not restricting data qualification if used in a qualifier word.

Edge Sensitive — Response of a system to rising (positive) or falling (negative or trailing) transitions as opposed to levels of the clock (see Active Clock Edge).

Emulator — Hardware containing a microprocessor that replaces the target system's microprocessor and permits execution and interaction with the user's program.

External Trigger — An active signal or an external logic analyzer input that will start (trigger) the analyzer (see Trigger).

Field — One or more adjoining characters treated as group.

File — A set of records on a common subject and usually organized or ordered on the basis of some combination of items of data uniformly found in all the records of the file, such as a date.

Filter — A circuit that ensures trigger conditions (i.e, Boolean combinations) are satisfied for a minimum time before actually triggering the analyzer.

Glitch Memory — An auxiliary memory that stores the presence of any glitches between sample periods.

Glitch Triggering — Triggering on a glitch on any specified channel. Usually combined with other logic level requirements on all lines.

Hold-time — The time following the active clock edge where the analyzer may sample data. Since many systems do not hold the data past the active clock edge, a logic analyzer should ideally, have a zero hold time.

Independent CLK/TRIG Qualification — The concept of forced acceptance of an otherwise not qualified trigger word; occuring before or after (i.e., displaced from) the clock qualifications (see Clock Qualifier, Trigger Qualifier).

Interrupt — An external controls system used to suspend normal operations and possibly cause new sequences of instructions to be followed.

Latch — A glitch latch detects narrow pulses and stretches them such that they are traced by the clock.

Parallel Trigger — The event caused by the occurrence of a selected word (or simultaneous occurrence of two words, like address and data) at the inputs. One of the obvious advantages of logic analyzers over conventional analog oscilloscopes.

Parity Check — A type of redundant check in which the evenness or oddness of the number of 1 bits is verified.

Pass Count — (See Trigger Delay).

Positive True Logic — Refers to a logic "1" being true.

Post Processing — Processing of data after the collection is complete. For example, determining the number of occurrences of a specific data pattern.

Post-trigger — Positive triggering. Post-trigger means the captured record consists of data, all or most of which occurred after the trigger.

Pretrigger — Negative triggering. Pretrigger means that the captured record consists of data, all or part of which occurred before the trigger. It can never be greater than the memory capacity.

Sample Clock — The signal that when enabled clocks data to the sample memory in the analyzer.

Sample Event — A start or stop of the sample clock.

Sample Processor — The system in the probe that determines the time and length of all sampling periods.

Sequential Trigger — A trigger condition that must be satisfied by a series of states in the specified sequence.

Serial Data Bus — A bus on which data are transferred bit-by-bit in a serial manner.

Set-Up Time — The time prior to the active clock edge during which data may be sampled by the analyzer. Therefore, the data must be valid for at least this interval.

Skew — The difference in the delays across channels as measured between the probe time and the point when the data are interpreted by the analyzer.

Source — Unit under test.

State Analyzer — State-sequences of a digital system are recorded for analysis with a logic state analyzer.

Strobe — A signal whose predefined edge latches data which is considered valid on that edge.

Synchronous Analyzer — Traces data which are synchronized with the clock of the system under observation (see State Analyzer).

Synchronous Data — Data that coincide or are valid with a defined clock or controls signal.

System Clock — Clock signal provided by the system under test.

Threshold — A signal amplitude level that divides one state from a second. A facility that allows the threshold on a logic analyzer to be varied either for different logic families or to check marginal data transitions.

Time Measurements — Time measured with logic analyzers that ma be relative (between samples), absolute (from trigger word), or between states and trigger stack levels, or between edges of specific traces.

Timing Analyzer — A Timing Analzyer monitors the activity of a digital system and presents its observations as a state-time display or a pseudowaveform of logic waveform.

Trigger — A word, or sequence of words or events, that defines the point where a logic analyzer references its tract to the system activity, the start of a data collection process. Used initiate the capture of a data record. Loosely, it may refer to the triggering event (see Parallel, Sequential, Non-occurence, Pre and Post-trigger).

Trigger Delay — Delay added so that the Nth word past the trigger is recorded by the logic analyzer.

Trigger Qualifier — A combinatorial signal (word) that places constraints on satisfying trigger conditions; i.e., the analyzer is triggerd only when the specified trigger state and the trigger qualifier conditions occur.