LOGICPAK

COMPREHENSIVE LOGIC DEVICE SUPPORT

The LogicPak™ with a Data I/O® mainframe, is a complete programming and testing system for logic devices. The LogicPak programs virtually all programmable logic devices (PLDs) on the market today, using manufacturer-approved algorithms. And, with either generic or manufacturer-specific adapters, the LogicPak has the built-in flexibility to program the latest device types and hard-to-handle packages.

CONTINUITY TESTING

Continuity testing has been incorporated into the new generic program and test adapters, the 303A-011A and 303A-011B, to eliminate improper programming due to poor socket connections. When using these adapters, the Logic-Pak performs a continuity check on each device pin prior to programming the part. If there is an improper connection, programming halts and the user is notified on the display. This feature is especially important for PLCC devices, because the operator cannot see if the device is seated once the lid on the socket is closed.

FUNCTIONAL TESTING

The LogicPak uses two methods to functionally test programmed devices: the Structured Vectors Method and the Logic Fingerprint™ Method.

Structured Vectors

This test applies a series of designer-specific stimulus vectors sequentially to the inputs of a programmed device, while monitoring the outputs for the expected response vectors. An important feature of the LogicPak and P/T adapters is the ability to support "preload" vectors, which set internal device registers to specific states. The LogicPak supports up to 9,999 structured test vectors. Test vector capacity is determined by the available RAM (see table on reverse). The LogicPak also accepts test vectors generated by Data I/O's PLDtest.®

Logic Fingerprint Test

The Logic Fingerprint test utilizes a signature analysis-based process in which cycles of 128,000 pseudorandom stimulus vectors are applied to a programmed device. The resulting output of a properly programmed device is a unique pattern called its Logic Fingerprint.

DATA I/O
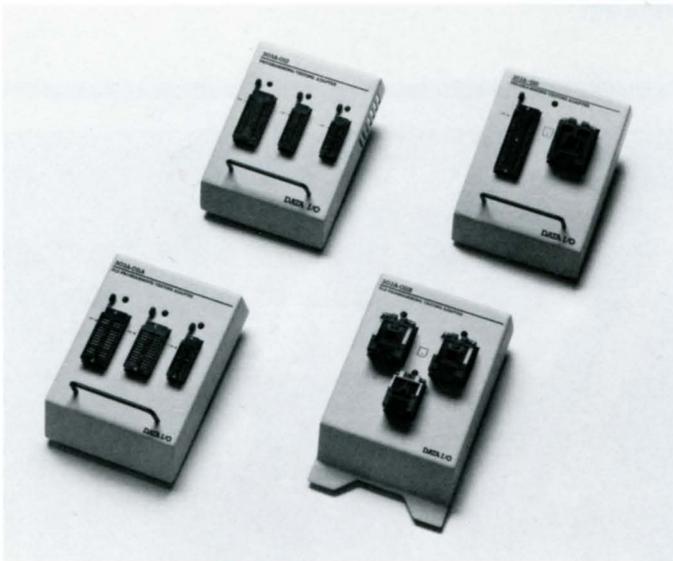
GENERIC P/T ADAPTERS

Adapter	Device Support
303A-010	40-pin (DIP) and 44-pin (PLCC); CMOS
303A-011A	20/24/28-pin (DIP); Bipolar and CMOS
303A-011B	20/28-pin (PLCC); Bipolar and CMOS
303A-012	20/24/28-pin (DIP); Vertical Cell (AIM)

MANUFACTURER-SPECIFIC P/T ADAPTERS

Adapter	Device Support
303A-001	20/24/28-pin (DIP); Signetics/TI IFL
303A-007	Harris 16XCX Family CMOS
303A-008A	MMI 32R16 (DIP/LCC)
303A-008B	MMI 32R16 (DIP/PLCC)

P/T ADAPTER COMPATIBILITY

P/T Adapter	Mainframe Programmer	Minimum Prog. RAM	Minimum LogicPak Revision*
303A-001	19, 29A, 29B, 100A	8K	V04 & 950-1942-006 H/W
303A-007	19, 29A, 29B, 100A	8K	"
303A-008A	29A, 29B	64K	"
303A-008B	29A, 29B	64K	"
303A-010	29A, 29B	64K	"
303A-011A	19, 29A, 29B	16K	"
303A-011B	19, 29A, 29B	16K	"
303A-012	19, 29A, 29B	16K	"

* Additional programmer compatibility requirements may be indicated in the LogicPak operator's manual and P/T adapter user note.

TEST VECTOR RAM CAPACITIES FOR FUNCTIONAL VERIFICATION

RAM Size	Vector Capacity
16K x 8 (Minimum)	256
64K x 8	1792
128K x 8	3840
256K x 8	7936
1MByte x 8	9999

PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

Altitude:	Sea level to 3 km (10,000 ft.)
Operating Humidity:	90% maximum (noncondensing)
Operating Temperature:	5° to 45°C (41° to 113°F)
Storage Temperature:	−40° to 70°C (−40° to 158°F)
Dimensions:	17.9 x 17.3 x 21.7 cm (7.05 x 6.81 x 8.54 in.)
Weight:	1.6 kg (3 lb. 8 oz.)

DATA I/O