Service Guide

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Agilent Technologies 1670G-Series Logic Analyzers

Agilent Technologies 1670G-Series Logic Analyzers

The Agilent 1670G-Series are 150-MHz State/500-MHz Timing Logic Analyzers. There are two options available. One option is to add a 2 GSa/s digitizing oscilloscope. Another option is to add a 32 channel pattern generator.

Features

Some of the main features of the Agilent 1670G-Series Logic Analyzers are as follows:

- 132 data channels and 4 clock/data channels in the Agilent 1670G
- 98 data channels and 4 clock/data channels in the Agilent 1671G
- 64 data channels and 4 clock/data channels in the Agilent 1672G
- 32 data channels and 2 clock/data channels in the Agilent 1673G
- 3.5-inch flexible disk drive
- 2-GB hard disk drive
- GPIB, RS-232-C, Centronics, and LAN interfaces
- Thinlan and Ethertwist LAN ports
- Variable setup/hold time
- 64K memory on all channels with 256K and 2M options
- Marker measurements
- 12 levels of trigger sequencing for state and 10 levels of sequential triggering for timing
- Full programmability
- DIN mouse
- DIN keyboard support

The pattern generator option includes the following features:

- 15 output channels at 200 MHz
- 32 output channels at 100 MHz
- Memory depth of 258,048 vectors
- Support for TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL terminated, ECL unterminated, and differential ECL (without pod).

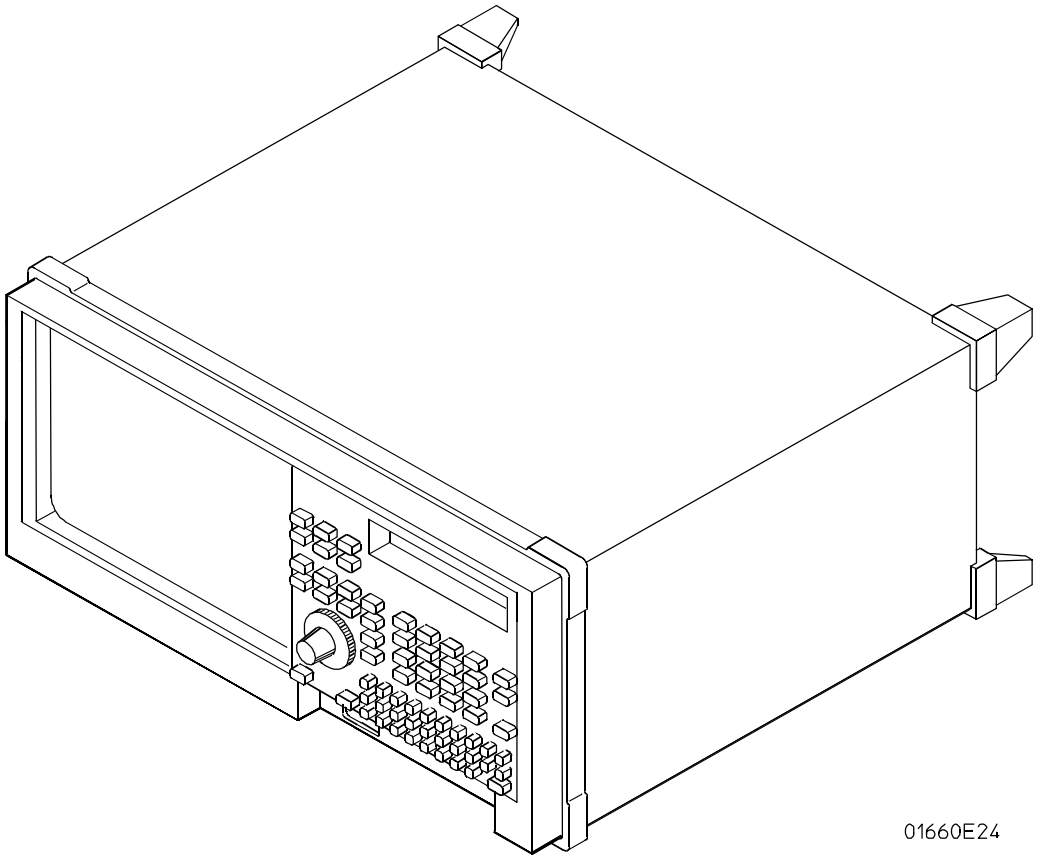
The oscilloscope option includes the following features:

- 2 GSa/s digitizing for 500 MHz bandwidth single shot oscilloscope
- >32000 samples per channel
- Automatic pulse parameters displays time between markers, acquires until specified time between markers is captured, performs statistical analysis on time between markers
- Lightweight mini probes

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the Agilent 1670G-series logic analyzers.

This logic analyzer can be returned to Agilent for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for details.



Agilent Technologies 1670G-Series Logic Analyzer

In This Book

This book is the service guide for the Agilent 1670G-Series Logic Analyzers and is divided into eight chapters.

Chapter 1 contains information about the logic analyzer and includes accessories, specifications and characteristics, and equipment required for servicing.

Chapter 2 tells how to prepare the logic analyzer for use.

Chapter 3 gives instructions on how to test the performance of the logic analyzer.

Chapter 4 contains calibration instructions for the logic analyzer.

Chapter 5 contains self-tests and flowcharts for troubleshooting the logic analyzer.

Chapter 6 tells how to replace assemblies of the logic analyzer and how to return them to Agilent Technologies.

Chapter 7 lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8 explains how the logic analyzer works and what the self-tests are checking.

Table of Contents

Service Strategy 1–iii

1 General Information

Accessories 1–2
Specifications (logic analyzer) 1–3
Specifications (oscilloscope) 1–4
Specifications (pattern generator) 1–4
Characteristics (logic analyzer) 1–5
Characteristics (oscilloscope) 1–5
Characteristics (pattern generator) 1–6
Recommended Test Equipment (logic analyzer) 1–9
Recommended test equipment (oscilloscope) 1–10
Recommended test equipment (pattern generator) 1–11

2 Preparing for Use

To inspect the logic analyzer 2–2
To apply power 2–3
To operate the user interface 2–3
To clean the logic analyzer 2–3
To test the logic analyzer 2–4

3 Testing Performance

To perform the self-tests 3–3

To make the test connectors (logic analyzer) 3–7

To test the threshold accuracy (logic analyzer) 3–9
Set up the equipment 3–9
Set up the logic analyzer 3–10
Connect the logic analyzer 3–12
Test the ECL Threshold 3–13
Test the 0 V User threshold 3–15
Test the next pod 3–16

To test the single-clock, single-edge, state acquisition (logic analyzer) 3–17
Set up the equipment 3–17
Set up the logic analyzer 3–18
Connect the logic analyzer 3–20
Verify the test signal 3–23
Check the setup/hold combination 3–24
Test the next channels 3–28

To test the multiple-clock, multiple-edge, state acquisition (logic analyzer) 3–29
Set up the equipment 3–29
Set up the logic analyzer 3–30
Connect the logic analyzer 3–32
Verify the test signal 3–35

Check the setup/hold with single clock edges, multiple clocks 3–36
Test the next channels 3–40

To test the single-clock, multiple-edge, state acquisition (logic analyzer) 3–41
Set up the equipment 3–41
Set up the logic analyzer 3–42
Connect the logic analyzer 3–44
Verify the test signal 3–47
Check the setup/hold with single clock, multiple clock edges 3–49
Test the next channels 3–52

To test the time interval accuracy (logic analyzer) 3–53
Set up the equipment 3–53
Connect the logic analyzer 3–54
Set up the logic analyzer 3–55
Acquire the data 3–58

To test the input resistance (oscilloscope) 3–59
Set up the equipment 3–59
Set up the logic analyzer 3–60
Connect the logic analyzer 3–61
Acquire the data 3–62

Perform an operational accuracy calibration 3–62

To test the voltage measurement accuracy (oscilloscope) 3–63
Set up the equipment 3–63
Set up the logic analyzer 3–64
Connect the logic analyzer 3–65
Acquire the data 3–66

To test the offset accuracy (oscilloscope) 3–67
Set up the equipment 3–67
Set up the logic analyzer 3–68
Connect the logic analyzer 3–69
Acquire the zero input data 3–70
Acquire the DC input data 3–71

To test the bandwidth (oscilloscope) 3–72
Set up the equipment 3–72
Set up the logic analyzer 3–73
Connect the logic analyzer 3–75
Acquire the data 3–76

To test the time measurement accuracy (oscilloscope) 3–77
Set up the equipment 3–77
Set up the logic analyzer 3–78
Connect the logic analyzer 3–80

Acquire the data 3–80

To test the trigger sensitivity (oscilloscope) 3–81
Set up the equipment 3–81
Set up the logic analyzer 3–82
Connect the logic analyzer 3–84
Acquire the data 3–84

Performance Test Record (logic analyzer) 3–85

Performance Test Record (oscilloscope) 3–88

Performance Test Record (pattern generator) 3–91

4 Calibrating and Adjusting

Logic analyzer calibration 4–2

To calibrate the oscilloscope 4–3
Set up the equipment 4–3
Load the Default Calibration Factors 4–4
Self Cal menu calibrations 4–5

To test the CAL OUTPUT ports 4–6
Set up the equipment 4–6
Set up the logic analyzer 4–7
Verify the DC CAL OUTPUT port 4–8
Set up the logic analyzer 4–9
Verify the AC CAL OUTPUT port 4–9

5 Troubleshooting

To use the flowcharts 5–2
To check the power-up tests 5–11
To run the self-tests 5–12
To test the power supply voltages 5–20
To test the LCD display signals 5–21
To test the keyboard signals 5–22
To test the flexible disk drive voltages 5–24
To test the hard disk drive voltages 5–26
To perform the BNC test 5–28
To test the logic analyzer probe cables 5–29
To verify pattern output (pattern generator option only) 5–33
The Ether address 5–35
To test the auxiliary power 5–36

6 Replacing Assemblies

To remove and replace the handle 6–5
To remove and replace the feet and tilt stand 6–5
To remove and replace the cover 6–5

To remove and replace the disk drive assembly 6–6
To remove and replace the acquisition board 6–7
To remove and replace the CPU board 6–9
To remove and replace SIMM memory 6–10
To remove and replace the rear panel 6–11
To remove and replace the power supply 6–12
To remove and replace the oscilloscope board (oscilloscope option only) 6–13
To remove and replace pattern generator board (pattern generator option only) 6–14
To remove and replace the front panel and keyboard 6–15
To remove and replace the LCD display and Inverter board 6–16
To remove and replace the handle plate 6–17
To remove and replace the fan 6–18
To remove and replace the pattern generator cables (pattern generator option only) 6–18
To remove and replace the GPIB and RS-232-C cables 6–19
To remove and replace the I/O board 6–19
To return assemblies 6–20

7 Replaceable Parts

Replaceable Parts Ordering 7–2
Replaceable Parts List 7–3
Exploded View 7–4
Power Cables and Plug Configurations 7–8

8 Theory of Operation

Block-Level Theory 8–3
The Agilent 1670G-Series Logic Analyzer 8–3
The Logic Acquisition Board 8–7
The Oscilloscope Board 8–10
The Pattern Generator Board 8–15

Self-Tests Descriptions 8–17
Power-up Self-Tests 8–17
System Tests (SysPV) 8–18
Analyzer Tests (Analy PV) 8–22
Oscilloscope tests (Scope PV) 8–25
Pattern Generator tests (Patt Gen) 8–26
GPIB 8–30
RS-232-C 8–32

1

Accessories 1–2
Specifications (logic analyzer) 1–3
Specifications (oscilloscope) 1–4
Specifications (pattern generator) 1–4
Characteristics (logic analyzer) 1–5
Characteristics (oscilloscope) 1–5
Characteristics (pattern generator) 1–6
Recommended Test Equipment (logic analyzer) 1–9
Recommended Test Equipment (oscilloscope) 1–10
Recommended Test Equipment (pattern generator) 1–11

General Information

General Information

This chapter lists the accessories, the specifications and characteristics, and the recommended test equipment.

Accessories

The following accessories are supplied with the Agilent 1670G-series logic analyzers. The part numbers are current as of the print date of this edition of the Service Guide, but further upgrades may change the part numbers. Do not be concerned if the accessories you receive have different part numbers.

Accessories Supplied	Part Number	Qty
Probe tip assemblies	01650-61608	Note 1
Probe cables	01660-61605	Note 2
Grabbers (20 per pack)	5090-4356	Note 1
Probe ground (5 per pack)	5959-9334	Note 1
Double Probe Adapter	16542-61607	1
PS2 Mouse	C3751-60201	1

Note 1 Quantities:
8 - 1670G
6 - 1671G
4 - 1672G
2 - 1673G

Note 2 Quantities:
4 - 1670G
3 - 1671G
2 - 1672G
1 - 1673G

Pattern Generator Option-Series Additional Accessories

Accessories Supplied	Part Number	Qty
Data Output Cable	16522-61601	4
Clock Output Cable	16522-61602	1

Oscilloscope Option-Series Additional Accessories

Accessories Supplied	Part Number	Qty
10:1 probes	1160A	2
BNC miniprobe adapter	1250-1454	1

Accessories Available

Other accessories available for the Agilent 1670G-series logic analyzer are listed in the *Accessories for Agilent Logic Analyzers* brochure.

Specifications (logic analyzer)

The specifications are the performance standards against which the product is tested.

Maximum State Speed (selectable)	150 MHz
Minimum Master to Master Clock Time*	6.666 ns
Threshold Accuracy	± (100 mV + 3% of threshold setting)

Setup/Hold Time:*

Single Clock, Single Edge	3.0/0.0 ns through -0.5/3.5 ns, adjustable in 500-ps increments
Single Clock, Multiple Edges	3.5/0.0 ns through -0.5/4.0 ns, adjustable in 500-ps increments
Multiple Clocks, Multiple Edges	4.0/0.0 ns through -0.5/4.5 ns, adjustable in 500-ps increments

* Specified for an input signal VH = –0.9 V, VL = –1.7 V, slew rate = 1 V/ns, and threshold = –1.3 V.

Specifications (oscilloscope)

The Agilent 1670G Logic Analyzers with an oscilloscope also include the following specifications:

Bandwidth (*,1)	DC to 500 MHz (real time, dc-coupled)
Time Interval Measurement Accuracy(*, 2)	±[(0.005% X Δt)+ (2 x 10^{-6} x delay setting)+150 ps]
DC Offset Accuracy(*)	±(1.0% of channel offset + 2.0% of full scale)
Voltage Measurement Accuracy(*, 3)	± [(1.25% of full scale + offset accuracy) + (0.016 x V/div)]
Trigger Sensitivity(*)	DC to 50 MHz: 0.063 x full scale, 50 to 500 MHz: 0.125 x full scale
Input R (selectable) (*)	1 MΩ: ±1%, 50 Ω: ±1%

* Specifications (valid within ± 10° C of auto-calibration temperature, excluding bandwidth–see note 1 for bandwidth specification.)

1. Upper bandwidth reduces by 2.5 MHz for every degree C above 35° C.

2. Specification applies to the maximum sampling rate. At lower rates, the specification is:± [(0.005% x Δt)+(2 x 10^{-6} x delay setting) + (0.15 x sample interval)] for bandwidth limited signals (t_r = 1.4 x sample interval). Sample interval is defined as $\frac{1}{sample\ rate}$

3. Digitizing level = (#vertical divisions)$(\frac{1}{2})(\frac{1}{LSB})$, where LSB=$2^{\#\ bits\ in\ ADC}$

Specifications (pattern generator)

There are no specifications for the pattern generator option of the Agilent 1670G-Series Logic Analyzers.

Characteristics (logic analyzer)

These characteristics are not specifications, but are included as additional information.

		Full Channel	**Half Channel**
Maximum State Clock Rate		150 MHz	not applicable
Maximum Conventional Timing Rate		250 MHz	500 MHz
Memory Depth		64K	128K
Memory Depth (option #001)		256K	512K
Memory Depth (option #002)		2048K	4196K
Channel Count:			
	1670G	136	68
	1671G	102	51
	1672G	68	34
	1673G	34	17

Characteristics (oscilloscope)

The Agilent 1670G Logic Analyzers with an oscilloscope also include the following characteristics:

Maximum Sample Rate	2 Gigasample per second
Number of Channels	2
Rise Time(1)	700 ps
ADC	8-bit real time
Vertical Resolution	8 bits over 4 vertical divisions (± 0.4%)
Waveform Record Length	>32000 points
Vertical (DC) Gain Accuracy(2)	±1.25% of full scale
Input Coupling	1 MΩ: ac and DC, 50 Ω: DC only
Input C	Approximately 7 pF

1. Rise time is calculated from the formula: $t_r = \frac{0.35}{bandwidth}$
2. Vertical gain accuracy decreases 0.08% per degree C from software calibration temperature.

Characteristics (pattern generator)

The Agilent 1670G Logic Analyzers with a pattern generator also include the following characteristics:

Output channels	16 channels at 200 MHz clock; 32 channels at 100 MHz clock
Memory depth	258,048 vectors
Logic levels (data pods)	TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL terminated, ECL unterminated, and differential ECL (without pod)
Data inputs	3-bit pattern - level sensing (clock pod)
Clock outputs	Synchronized to output data, delay of 11 ns in 9 steps (clock pod)
Clock input	DC to 200 MHz (clock pod)
Internal clock period	Programmable from 5 ns to 250 μs in a 1, 2, 2.5, 4, 5, 8 sequence
External clock period (user supplied)	DC to 200 MHz
External clock duty cycle	2 ns minimum high time
Maximum number of "IF condition" blocks at 50 MHz clock	1
Maximum number of different macros	100
Maximum number of lines in a macro	1024
Maximum number of macro invocations	1,000
Maximum number of Repeat loop invocations	1,000
Maximum number of Wait event patterns	4

Probes

Maximum Input Voltage	± 40V, CAT 1

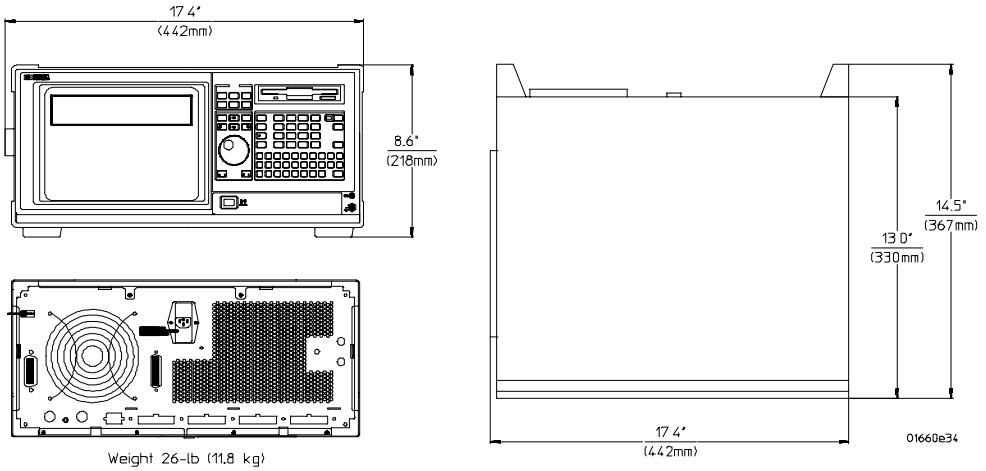
Auxiliary Power

Power Through Cables	1/3 amp at 5 V maximum per cable, CAT 1

Operating Environment (for indoor use only)

Temperature	Instrument, 0 °C to 55 °C (+32 °F to 131 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F). Disk media, 10 °C to 40 °C (+50 °F to 104 °F).
Humidity	Instrument, probe lead sets, and cables, up to 80% relative humidity at +40 °C (+122 °F).
Altitude	To 3067 m (10,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.3 g (rms). Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈ 2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Dimensions



Product Regulations

Safety	IEC 1010-1:1990+A1 / EN 61010-1:1993 UL3111 CSA-C22.2 No. 1010.1:1993		
EMC	This product meets the requirement of the European Communities (EC) EMC Directive 89/336/EEC.		
Emissions	EN55011/CSIPR 11 (ISM, Group1,Class A equipment) IEC 555-2 and IEC 555-3		
Immunity	EN50082-1	Code[1]	Notes[2]
	IEC 801-2 (ESD)4kV CD, 8kV AD	1	
	IEC 801-3 (Rad.) 3V/m	1	
	IEC 801-4 (EFT) 1kV	1	

[1]Performance Codes:
1 PASS - Normal operations, no effect.
2 PASS - Temporary degradation, self recoverable.
3 PASS - Temporary degradation, operator intervention required.
4 FAIL - Not recoverable, component damage.

Recommended Test Equipment (logic analyzer)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Pulse Generator	150 MHz, 3.0 ns pulse width, < 600 ps rise time	8133A Option 003	P,T
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A mainframe with 54751A plugin module	P
Function Generator	Accuracy ≤ (5)(10^{-6}) × frequency, DC offset voltage ±6.3 V	3325B Option 002	P
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A	P
BNC-Banana Cable		11001-60001	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P
Cable	BNC (m)(m) 48 inch	8120-1840	P,T
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948	P
Adapter (Qty 4)	SMA(m)-BNC(f)	1250-1200	P, T
Adapter	SMA(f)-BNC(m)	1250-2015	P
Coupler (Qty 4)	BNC (m)(m)	1250-0216	P, T
20:1 Probes (Qty 2)		54006A	P
BNC Coax Cable	BNC(m)(m), >2 GHz bandwidth, >1 meter length	10503A	T
BNC Test Connector, 17x2 (Qty 1)**			P
BNC Test Connector, 6x2 (Qty 4)**			P,T
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B	T
BNC Shorting Cap		1250-0774	T
BNC-Banana Adapter		1251-2277	T

*A = Adjustment P = Performance Tests T = Troubleshooting
**Instructions for making these test connectors are in chapter 3, "Testing Performance."

Recommended test equipment (oscilloscope)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Signal Generator	Frequency: 1 - 500 MHz at approx. 170 mV RMS Output Accuracy: ± 1 dB 1 MHz time base accuracy 0.25 ppm	8656B Option 001	P
DC Power Supply	Range: –35.000 to +35.000 Vdc, ±1 mV	3245A Option 002	P
Digital Multimeter	0.1 mV resolution Accuracy: better than 0.005% Resistance measurement: better than 0.25% accuracy	3458A	P
Power Meter/Sensor	1 - 250 MHz ±3% accuracy	436/8482A	P
Power Splitter	Outputs differ by <0.15 dB	11667B	P
Blocking Capacitor	BNC (m)(f), 0.18 µF, ±200 V	10240B	P
BNC Shorting Cap		1250-0074	P
Adapter	BNC (f)(f) (UG-914/U)	1250-0080	C
Adapter	BNC(f)-to-Dual Banana Plug	1251-2277	P
Adapter	Type N(m)-to-BNC(f)	1250-0780	P
BNC Tee	BNC (m)(f)(f)	1250-0781	P,C
Cable	Type N(m-to-m) 24-inch	11500B	P
Cable	50 Ω BNC (m-to-m) 48-inch	10503A	P, C
Cable (2)	50 Ω BNC (m-to-m) 9 inch	10502A	C

*P = Performance Tests C = Calibration

Recommended test equipment (pattern generator)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part	Use*
Oscilloscope	≥ 500 MHz Bandwidth	54820A	T
Probe	500 MHz Bandwidth	1160A	T
Output Data Pod	no substitute	10460A - series	T

* T = Troubleshooting

2

To inspect the logic analyzer 2–2
To apply power 2–3
To operate the user interface 2–3
To clean the logic analyzer 2–3
To test the logic analyzer 2–4

Preparing for Use

Preparing For Use

This chapter gives you instructions for preparing the logic analyzer for use.

Power Requirements

The logic analyzer requires a power source of either 115 Vac or 230 Vac, –22 % to +10 %, single phase, 48 to 66 Hz, CAT II pollution degree 2, 200 Watts maximum power.

Operating Environment

The operating environment is listed in chapter 1. The logic analyzer will operate at all specifications within the temperature and humidity range given in chapter 1. However, reliability is enhanced when operating the logic analyzer within the following ranges:

- Temperature: +20 °C to +35 °C (+68 °F to +95 °F)
- Humidity: 20% to 80% noncondensing

Note the recommended noncondensing humidity. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40 °C to +75 °C
- Humidity: Up to 90% at 65 °C
- Altitude: Up to 15,300 meters (50,000 feet)

Protect the logic analyzer from temperature extremes which cause condensation on the instrument.

To inspect the logic analyzer

1. Inspect the shipping container for damage.

   If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2. Check the supplied accessories.

   Accessories supplied with the logic analyzer are listed in "Accessories" in chapter 1.

3. Inspect the product for physical damage.

   Check the logic analyzer and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To apply power

1. Check that the line voltage selector, located on the rear panel, is on the correct setting and the correct fuse is installed.

   See also, "To set the line voltage" on this page.

2. Connect the power cord to the instrument and to the power source.

   This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. Refer to chapter 7, "Replaceable Parts," for option numbers of available power cables and plug configurations.

3. Turn on the instrument power switch located on the front panel.

To operate the user interface

To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. For more information about the logic analyzer interface, refer to the *Agilent 1670G-Series Logic Analyzers User's Guide*.

To set the GPIB address or to configure for RS-232-C, refer to the *Agilent 1670G-Series Logic Analyzer User's Guide*.

To clean the logic analyzer

With the instrument turned off and unplugged, use mild soap and water to clean the front and cabinet of the logic analyzer. Harsh soap might damage the water-base paint.

To test the logic analyzer

- If you require a test to verify the specifications, start at the beginning of chapter 3, "Testing Performance."
- If you require a test to initially accept the operation, perform the self-tests in chapter 3.
- If the logic analyzer does not operate correctly, go to the beginning of chapter 5, "Troubleshooting."

3

To perform the self-tests 3-3
To make the test connectors (logic analyzer) 3-7
To test the threshold accuracy (logic analyzer) 3-9
To test the single-clock, single-edge, state acquisition (logic analyzer) 3-17
To test the multiple-clock, multiple-edge, state acquisition (logic analyzer) 3-29
To test the single-clock, multiple-edge, state acquisition (logic analyzer) 3-41
To test the time interval accuracy (logic analyzer) 3-53
To test the CAL OUTPUT ports (oscilloscope) 3-59
To test the input resistance (oscilloscope) 3-63
To test the voltage measurement accuracy (oscilloscope) 3-67
To test the offset accuracy (oscilloscope) 3-71
To test the bandwidth (oscilloscope) 3-76
To test the time measurement accuracy (oscilloscope) 3-81
To test the trigger sensitivity (oscilloscope) 3-85
Performance Test Record (logic analyzer) 3-89
Performance Test Record (oscilloscope) 3-92
Performance Test Record (pattern generator) 3-95

Testing Performance

Testing Performance

This chapter tells you how to test the performance of the logic analyzer against the specifications listed in chapter 1. To ensure the logic analyzer is operating as specified, you perform software tests (self-tests) and manual performance tests on the analyzer. The logic analyzer is considered performance-verified if all of the software tests and manual performance tests have passed. The procedures in this chapter indicate what constitutes a "Pass" status for each of the tests.

The Logic Analyzer Interface

To select a field on the logic analyzer screen, use the arrow keys to highlight the field, then press the Select key. For more information about the logic analyzer interface, refer to the *Agilent 1670G-Series Logic Analyzers User's Guide*.

Test Strategy

For a complete test, start at the beginning with the software tests and continue through to the end of the chapter. For an individual test, follow the procedure in the test. The examples in this chapter were performed using an Agilent 1670G. Other analyzers in the series will have appropriate pods showing on the screen.

With the oscilloscope option, ensure that the operational accuracy calibration has been done before doing the performance verification tests (see chapter 4).

The performance verification procedures starting on page 3–8 are each shown from power-up. To exactly duplicate the setups in the tests, save the power-up configuration to a file on a disk, then load that file at the start of each test.

If a test fails, check the test equipment setup, check the connections, and verify adequate grounding. If a test still fails, the most probable cause of failure would be the acquisition board.

Test Interval

Test the performance of the logic analyzer against specifications at two-year intervals.

Performance Test Record

A performance test record for recording the results of each procedure is located at the end of this chapter. Use the performance test record to gauge the performance of the logic analyzer over time.

Test Equipment

Each procedure lists the recommended test equipment. You can use equipment that satisfies the specifications given. However, the procedures are based on using the recommended model or part number. Before testing the performance of the logic analyzer, warm-up the instrument and the test equipment for 30 minutes.

To perform the self-tests

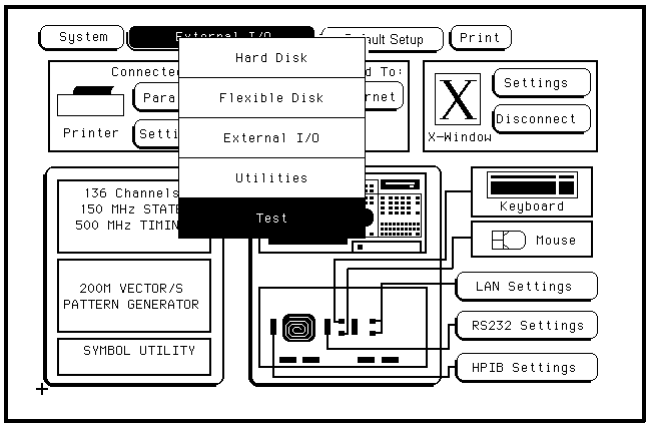
The self-tests verify the correct operation of the logic analyzer. Self-tests can be performed all at once or one at a time. While testing the performance of the logic analyzer, run the self-tests all at once.

The performance verification (PV) self-tests consist of system PV tests and analyzer PV tests. For the oscilloscope option there are oscilloscope PV tests, and for the pattern generator option there is a pattern generator test.

These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

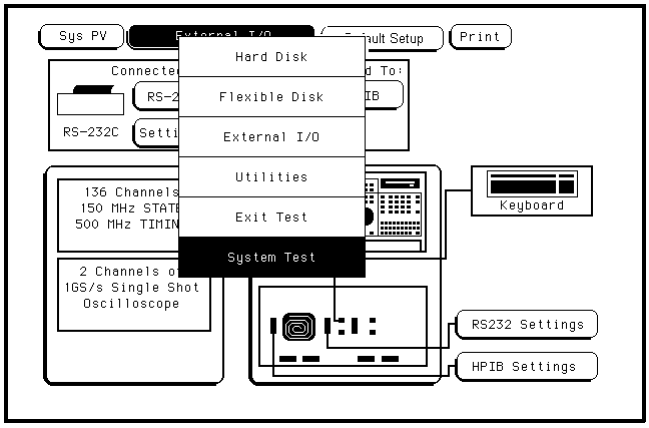
1 Disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.

2 Press the System key. Select External I/O, then select Test in the pop-up menu.



3 Select the box labeled Load Test System.

4 Select the Analy PV field. then select SysPV in the pop-up menu. Select the field next to Sys PV, then select System Test in the pop-up menu.

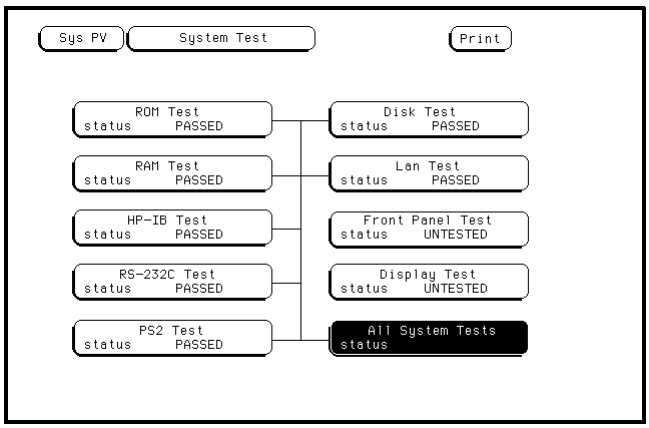


5 Install a formatted disk that is not write protected into the disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port.

6 Select All System Tests.

You can run all tests at one time, except for the Front Panel Test and Display Test, by running All System Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All System Tests changes from UNTESTED to TESTED. Note that the Front Panel Test and Display Test remain UNTESTED.



7 Select the Front Panel Test.

A screen duplicating the front panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color. Test the knob by turning it in both directions.

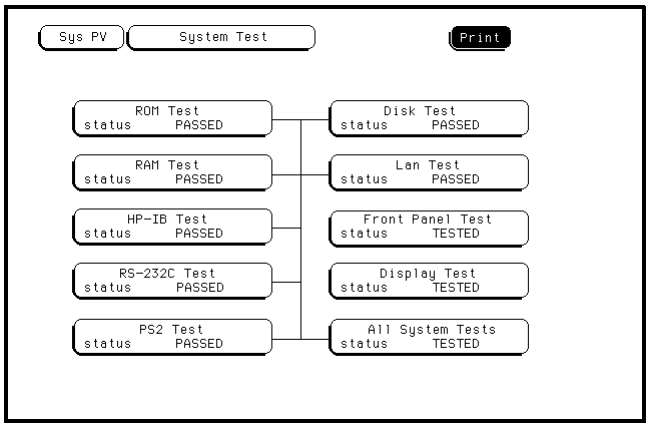
b Note any failures, then press the Done key a second time to exit the Front Panel Test. The status of the test changes from UNTESTED to TESTED.

8 Select the Display Test.

A white grid pattern is displayed. Continuously press the Select key to step through the other display screens. When completed, the test screen will again appear, and the Display Test status will indicate Tested.

The six display screens are:

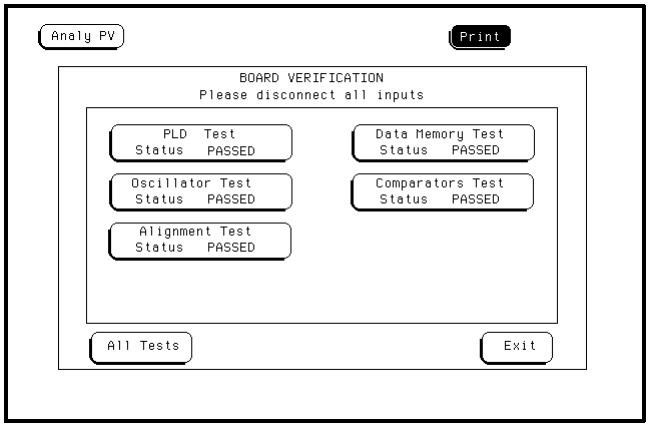
1. white pattern on black background
2. white
3. red
4. yellow
5. green
6. black



9 Select Sys PV, then select Analy PV in the pop-up menu. In the Analy PV menu, select Board Verification. In the Board Verification menu, select All Tests.

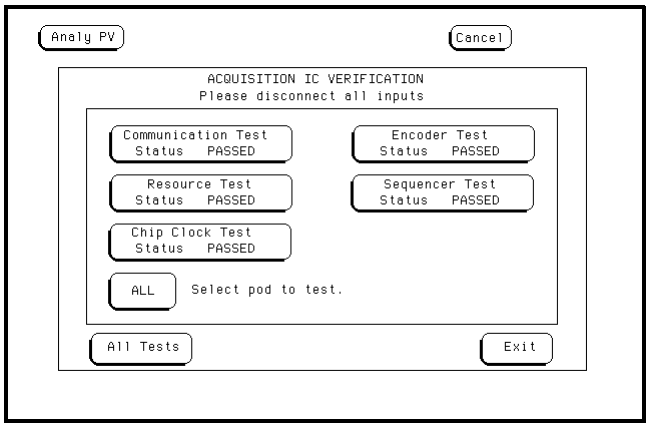
You can run all tests at one time by selecting All Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All Tests changes from UNTESTED to TESTED.



10 Select Exit to exit the Board Verification. In the Analy PV menu, select Acquisition IC Verification. In the Acquisition IC Verification menu, select All Tests.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All Tests changes from UNTESTED to TESTED.



11 Record the results of the tests on the performance test record at the end of this chapter.

12 If you have an oscilloscope, go to step 14. If you have a pattern generator, go to step 17. Otherwise, go to step 18.

13 If you do not have an Agilent 1670G-series logic analyzer with the oscilloscope option or pattern generator option, exit the tests by pressing the System key. Select the field to the right of the Sys PV field. Select the Exit Test System.

14 If you have the oscilloscope, Select Analy PV, then select Scope PV in the pop-up menu. In the Scope PV menu, select Functional Tests then select ALL Tests.

You can run all tests at one time, except for the Data Input Inspection, by running All Tests. To see more details about each test when troubleshooting failures, you can run each test individually.

15 Record the results of the tests on the performance test record at the end of this chapter.

16 To exit the test system, press the System key, then press the Select key. Select Exit Test, then select Exit Test System.

17 If you have the pattern generator option, Select Analy PV, then select PattGen in the pop-up menu. In the PattGen menu select All Tests.

You can run all tests at one time (except the Output Patterns routine) by selecting All Tests. To see more details about each test, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows Passed or Failed.

18 Exit the test system.

a. Select Analy PV, Scope PV, or PattGen depending on what was last tested.

b. Select Sys PV.

c. Select System Test, then select Exit Test.

d. Select Exit Test System to reload the operating system.

To make the test connectors (logic analyzer)

The test connectors connect the logic analyzer to the test equipment.

Materials Required

Description	Recommended Part	Qty
BNC (f) Connector	1250-1032	5
100 Ω 1% resistor	0698-7212	8
Berg Strip, 17-by-2		1
Berg Strip, 6-by-2		4
20:1 Probe	54006A	2
Jumper wire		

1 Build four test connectors using BNC connectors and 6-by-2 sections of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

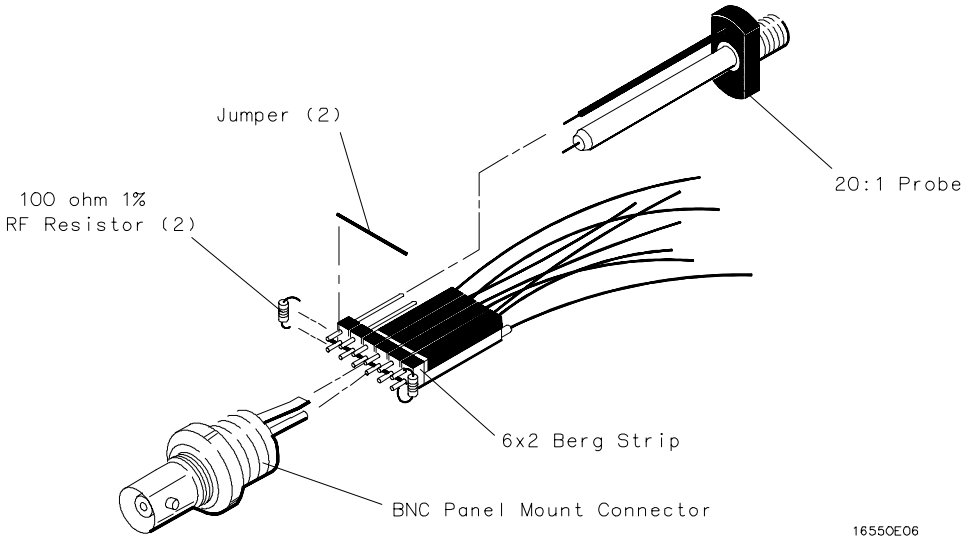
b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder two resistors to the Berg strip, one at each end between the end pins.

d Solder the center of the BNC connector to the center pin of one row on the Berg strip.

e Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.

f On two of the test connectors, solder a 20:1 probe. The probe ground goes to the same row of pins on the test connector as the BNC ground tab.



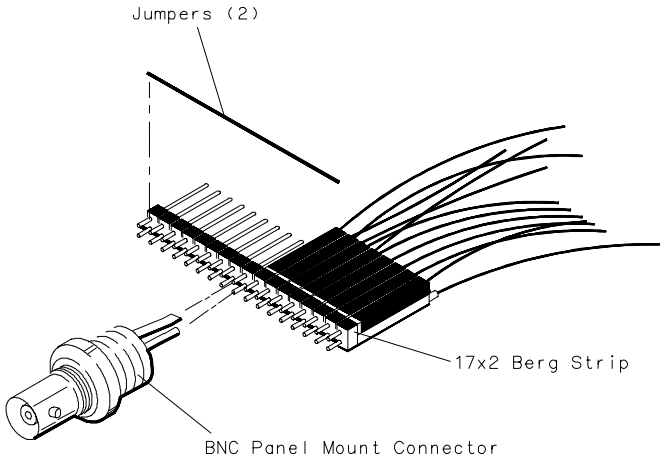
2 Build one test connector using a BNC connector and a 17-by-2 section of Berg strip.

a Solder a jumper wire to all pins on one side of the Berg strip.

b Solder a jumper wire to all pins on the other side of the Berg strip.

c Solder the center of the BNC connector to the center pin of one row on the Berg strip.

d Solder the ground tab of the BNC connector to the center pin of the other row on the Berg strip.



1655OEO5

To test the threshold accuracy (logic analyzer)

Testing the threshold accuracy verifies the performance of the following specification:

- Clock and data channel threshold accuracy.

These instructions include detailed steps for testing the threshold settings of pod 1. After testing pod 1, connect and test the rest of the pods one at a time. To test the next pod, follow the detailed steps for pod 1, substituting the next pod for pod 1 in the instructions.

Each threshold test tells you to record a pass/fail reading in the performance test record located at the end of this chapter.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, 0.005% accuracy	3458A
Function Generator	Accuracy $\leq (5)(10^{-6})\times$ frequency, DC offset voltage ± 6.3 V	3325B Option 002
BNC-Banana Cable		11001-60001
BNC Tee		1250-0781
BNC Cable		8120-1840
BNC Test Connector, 17x2		

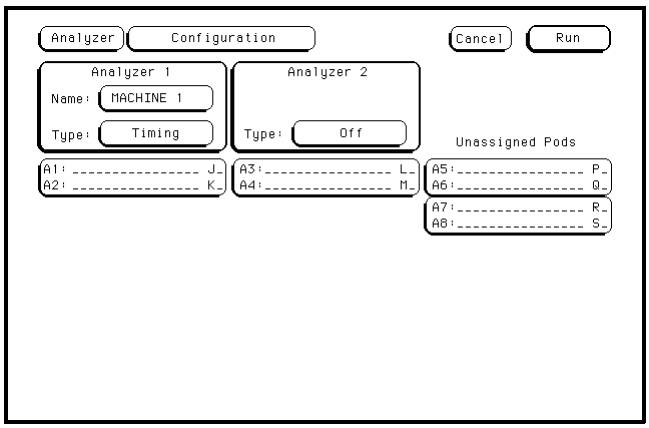
Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test.
2. Set up the function generator.
   a. Set up the function generator to provide a DC offset voltage at the Main Signal output.
   b. Disable any AC voltage to the function generator output, and enable the high voltage output.
   c. Monitor the function generator DC output voltage with the multimeter.

Set up the logic analyzer

1 Press the Config key.

2 Unassign Pods 3 and 4, Pods 5 and 6, and Pods 7 and 8. To unassign the pods, select the pod field. In the pop-up menu, select Unassigned.



3 Set up the Format menu.

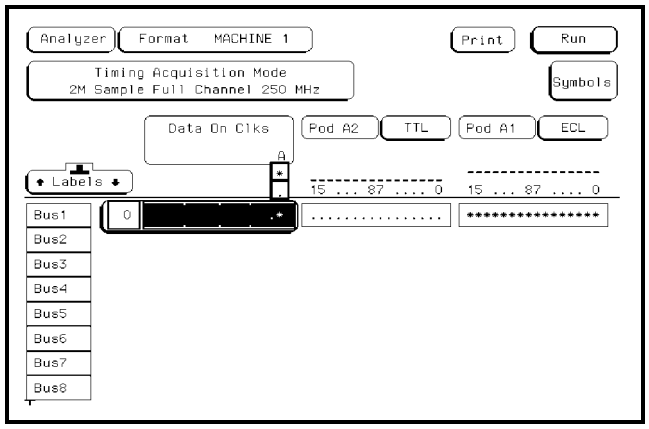
a Press the Format key.

b Select the field to the right of Pod A1, then select ECL in the pop-up menu.

c Move the cursor over the Pod A1 channel selection field. Press the Clear Entry button until all channels are assigned (all '*'), then press Done.

d Move the cursor over the Data on Clocks channel selection field, then press Select. Rotate the RPG knob to move the channel selector to the channel indicated in the following table, then press Select. Press Done.

Pod	Channel
A1, A3, A5, A7	0
A2, A4, A6, A8	1

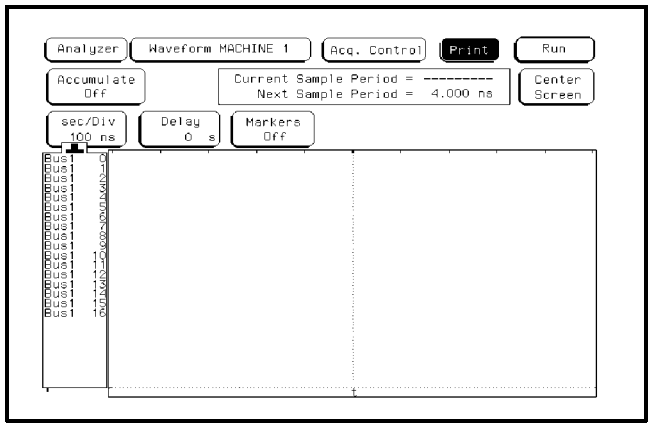


4 Set up the Waveform menu.

a Press the Waveform key.

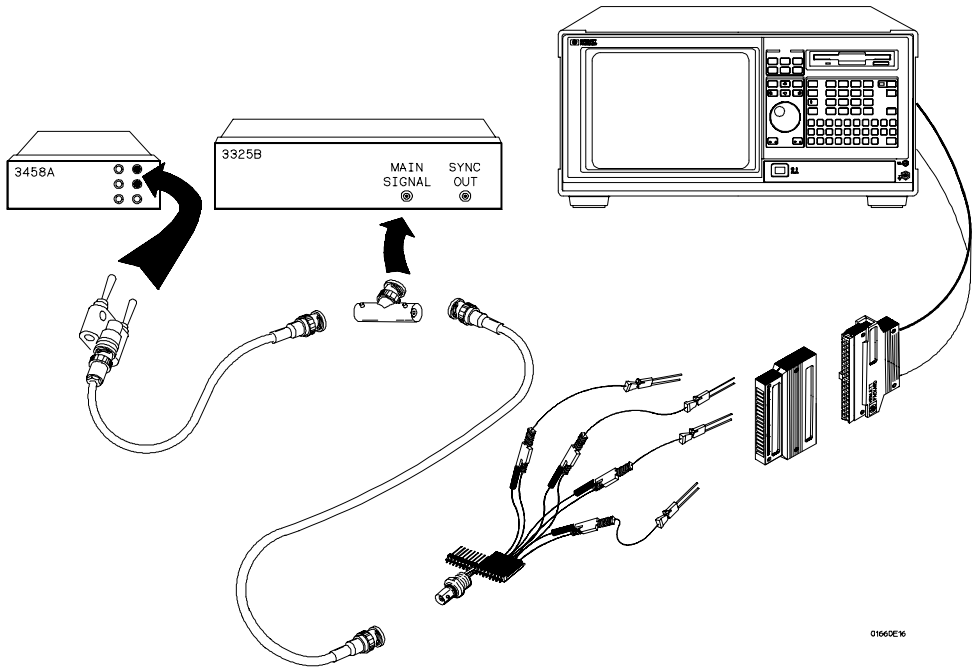
b In the Waveform menu, move the cursor to the pod/channel selection field, then press Select. In the pop-up menu, select Delete All, then select Continue.

c Again press Select. At the pop-up menu, select Insert, then select Bus1, then select Sequential.



Connect the logic analyzer

1. Using the 17-by-2 test connector, BNC cable, and probe tip assembly, connect the data and clock channels of pod 1 to one side of the BNC Tee.
2. Using a BNC-banana cable, connect the voltmeter to the other side of the BNC Tee.
3. Connect the BNC Tee to the Main Signal output of the function generator.

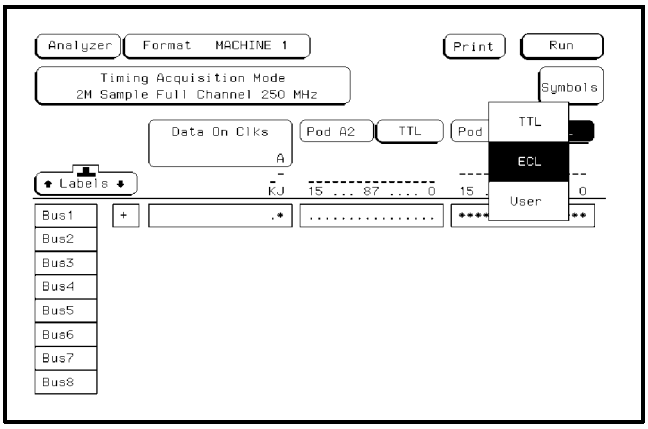


Test the ECL Threshold

1 Set up the Format menu.

a Press the Format key.

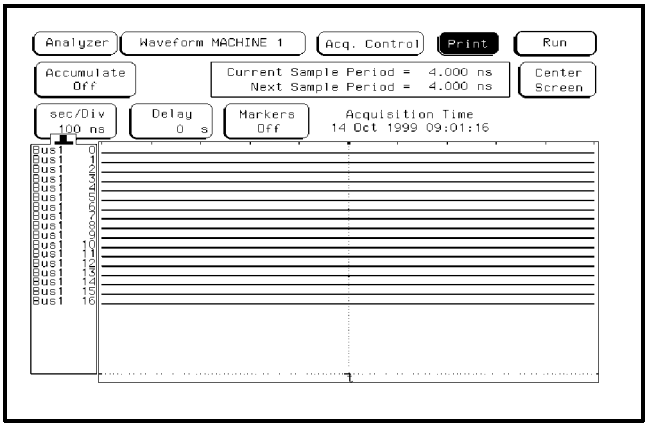
b Select the field to the right of Pod A1, then select ECL in the pop-up menu.



2 Test the high-to-low transition.

a On the DC power source, enter -1.438 V.

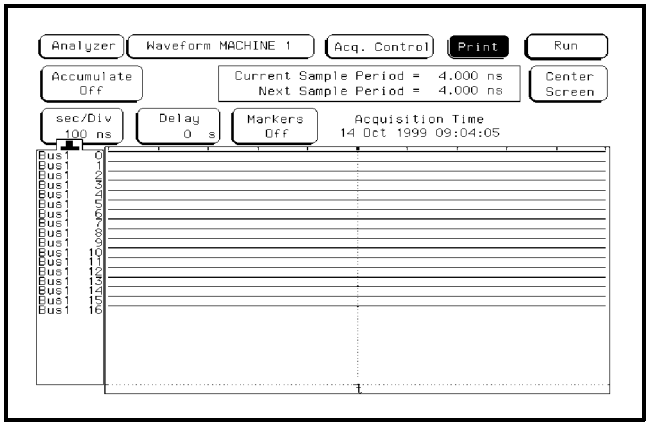
b On the logic analyzer, press Run. The display should show all channels at a logic "0"



3. Test the low-to-high transition

a On the DC source, enter -1.162 V

b On the logic analyzer, press Run. The display should show all channels at a logic "1".



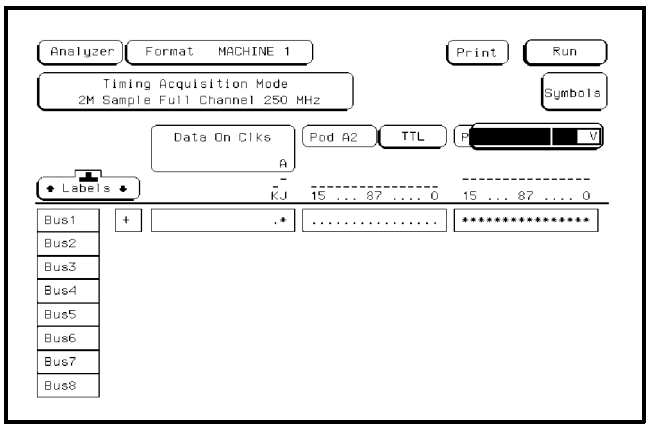
4 Record a PASS/FAIL in the performance test record for Threshold Accuracy Pod 1 - ECL.

Test the 0 V User threshold

1 Set up the Format menu.

a Press the Format key.

b Select the field to the right of Pod A1, then select User in the pop-up menu, then enter 0 V.



2 Test the high-to-low transition.

a On the DC power source, enter -0.099 V.

b On the logic analyzer, press Run. The display should show all channels at a logic "0".

3 Test the low-to-high transition

a On the DC source, enter 0.099 V

b On the logic analyzer, press Run. The display should show all channels at a logic "1".

4 Record a PASS/FAIL in the performance test record for Threshold Accuracy Pod 1 - 0 V.

Test the next pod

1. Using the 17-by-2 test connector and probe tip assembly, connect the data and clock channels of the next pod to the output of the function generator until all pods have been tested.
2. Unassign the channels just tested.
   a. Press the Format key.
   b. Move the cursor over the channel assignment field for the pod tested. Press Clear Entry until all channels show unassigned (all '.').
   c. Move the cursor over the Data on Clocks channel assignment field. Press Clear Entry until all channels show unassigned (all '.').
3. Start with "Set up the logic analyzer" on page 3–10, substituting the next pod to be tested for pod 1.

To test the single-clock, single-edge, state acquisition (logic analyzer)

Testing the single-clock, single-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for single-clock, single-edge, state acquisition

This test checks two combinations of data channels using a single-edge clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	150 MHz 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 2	Mode: Square
Period: 6.666 ns	Divide: PULSE ÷ 2	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 3.000 ns	Offs: 0.00 V	
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V

b Disable the pulse generator channel 1 COMP (with the LED off).

3 Set up the oscilloscope.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

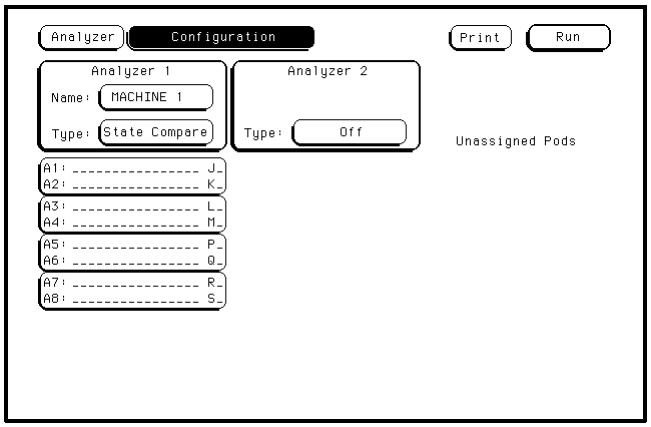
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign the pods, select the pod fields, then select Machine 1 in the pop-up menu.

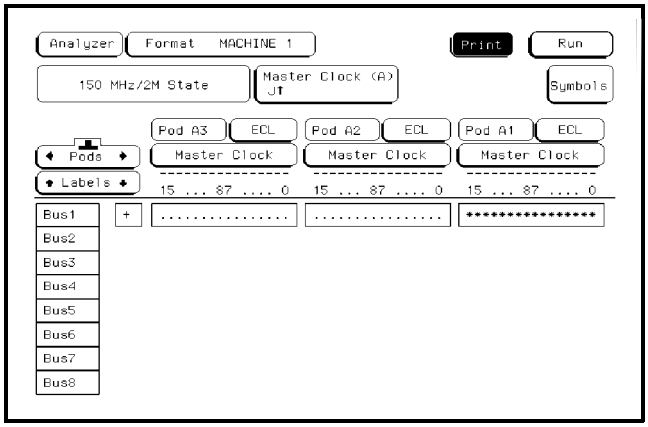
c Select the Type field in the Analyzer 1 box, then select State Compare.



2 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each pod, then select ECL in the pop-up menu. Use the knob to access pods not shown on the screen.



3 Set up the Trigger menu.

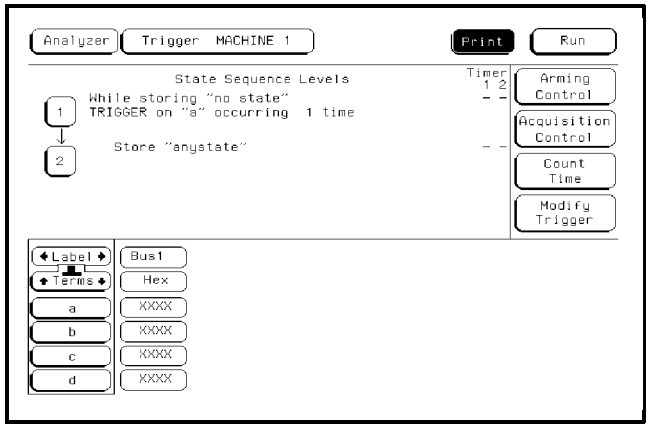
a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All in the pop-up menu.

b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

c Select Acquisition Control. If the Acquisition Control is "Manual," use the cursor keys to move the cursor to the Acquisition Mode field. Press the "Select" key to toggle this field to "Automatic."

d In the Acquisition Control menu, use the knob to set the Memory Length to 4096. Press the Done key.

e Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate," then select "no state." Select Done to exit the State Sequence Levels menu.



Connect the logic analyzer

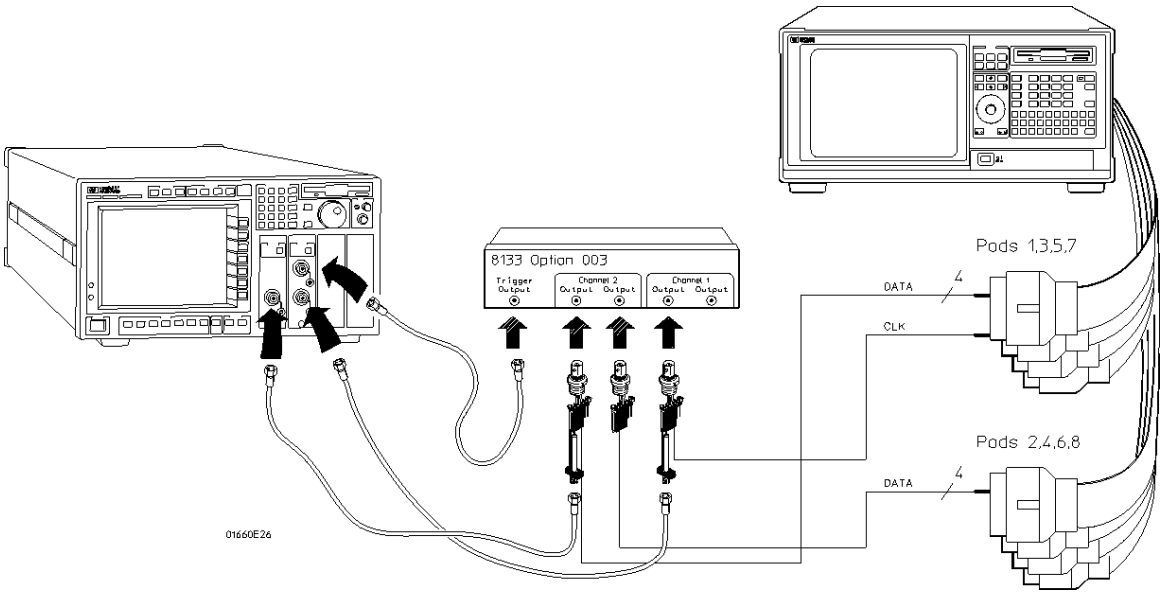
1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an Agilent 1670G or Agilent 1671G, you will repeat this test for the second combination.

2 Using SMA cables, connect the oscilloscope to the pulse generator channel 1 Output, channel 2 Output, and Trigger Output.

Connect the Agilent 1670G or Agilent 1671G Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3 *	J-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11*	J-clock

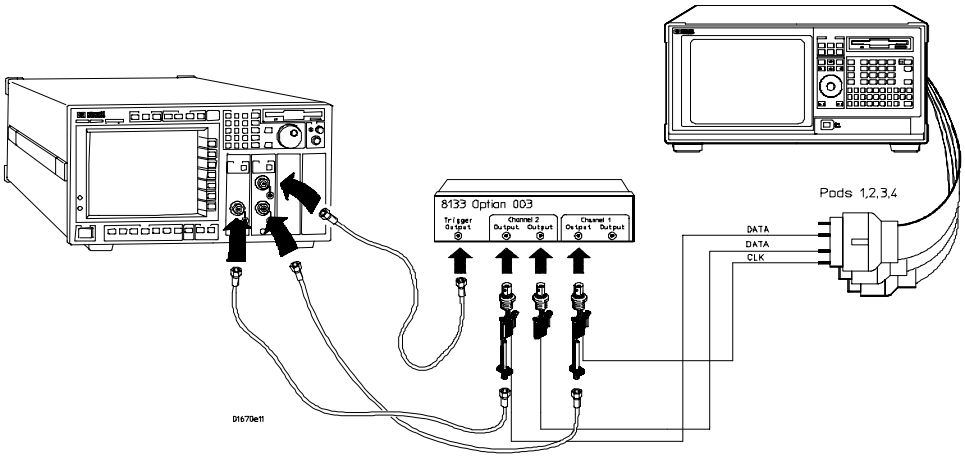
*Agilent 1670G only



Connect the Agilent 1672G or Agilent 1673G Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 11 Pod 2, channel 11 Pod 3, channel 11* Pod 4, channel 11*	J-clock

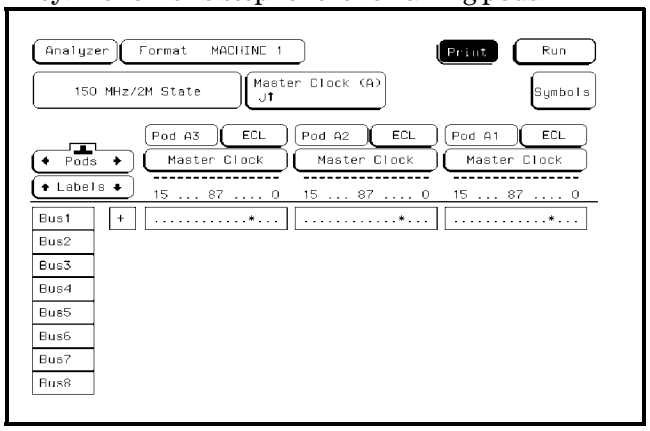
*Agilent 1672G only



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested, then press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.



4 Configure the trigger according to the connected channels.

a Press the Trigger key.

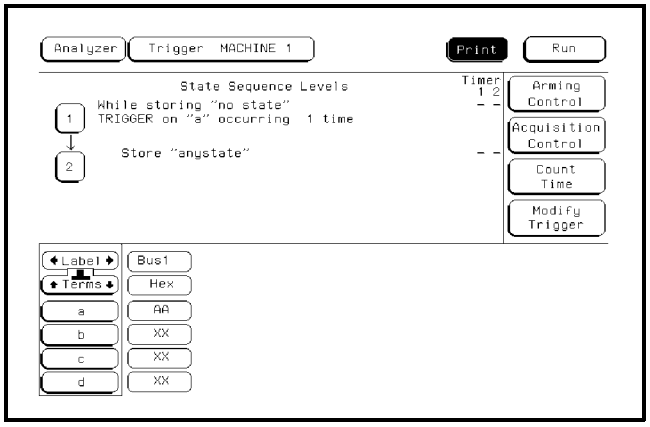
b Select the field next to "a" under the label Bus1. Type the following for your logic analyzer, then press the Select key.

Agilent 1670G – "AA"

Agilent 1672G – "AA"

Agilent 1671G – "2A"

Agilent 1673G – "0A"



5 Enable the pulse generator channel 1, channel 2, and trigger outputs (with the LEDs off).

Verify the test signal

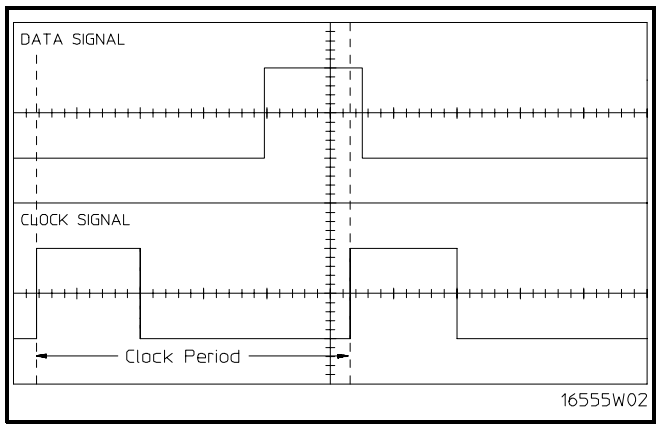
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 6.666 ns, +0 ps or −100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 6.666 ns, go to step d. If the period is less than 6.666 ns, go to step 3.

d In the oscilloscope Timebase menu, increase Position 6.666 ns. If the period is not less than 6.666 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 6.666 ns.

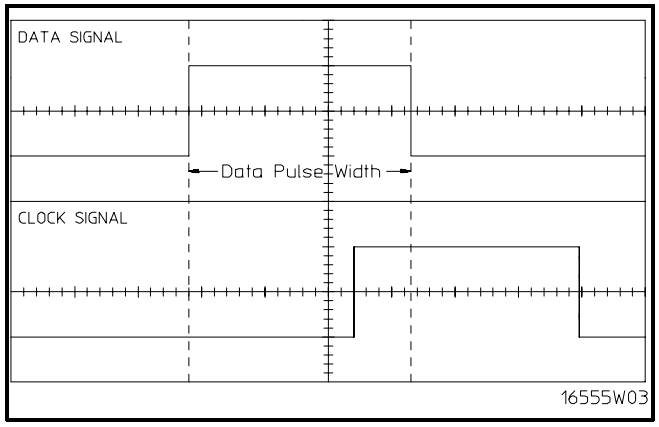


2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.000 ns, +0 ps or −100 ps.

a In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

b On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

c If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold combination

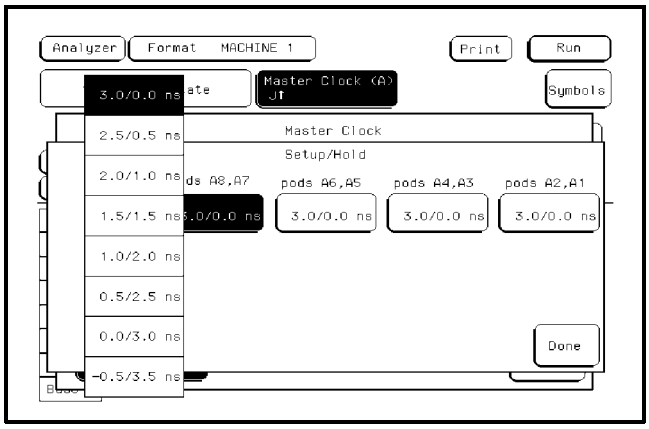
1 Select the logic analyzer setup/hold time.

a In the logic analyzer Format menu, select Master Clock.

b Select the Setup/Hold field, then select the setup/hold combination to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
3.0/0.0 ns
-0.5/3.5 ns

c Select Done to exit the setup/hold combinations.



2 Disable the pulse generator channel 1 COMP (with the LED off).

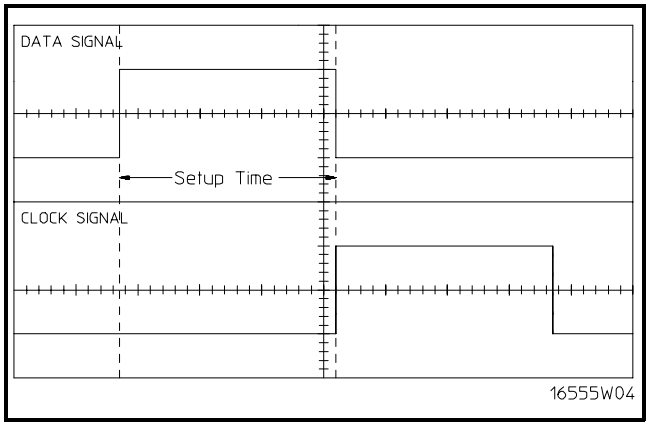
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



Disregard the oscilloscope Period(2) value. The settings provided in this procedure measure the period from falling edge to falling edge, which is not a valid measurement.

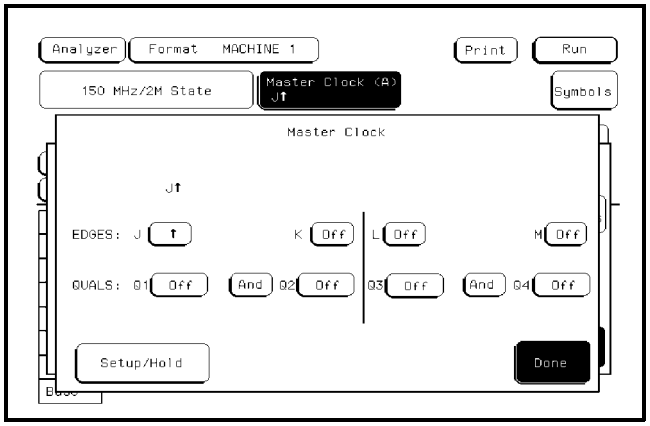
4 Select the clock to be tested.

a In the Master Clock menu, select the clock field to be tested, then select the clock edge as indicated in the table. The first time through this test, use the top clock and edge in the following table.

Clocks
J↑
K↑
L↑
M↑

b Connect the clock to be tested to the pulse generator channel 1 output.

c Select Done to exit the Master Clock menu.



5 Note: Do this step only the first time through the test, to create a Compare file. For subsequent runs, go to step 6.

Use the following to create a Compare file:

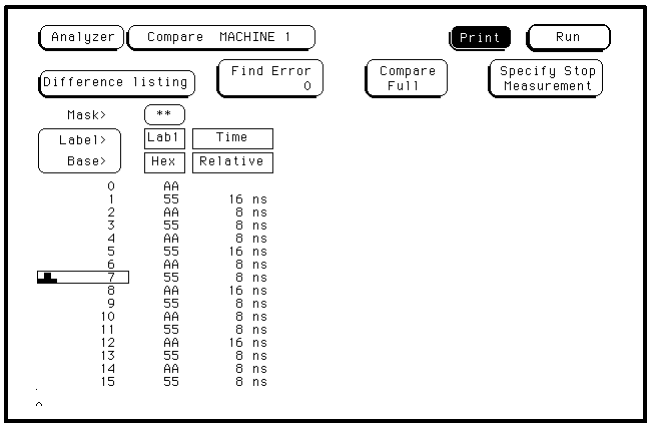
a Press Run. The display should show an alternating pattern of "AA" and "55." Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key. Select Execute.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop-up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop-up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



6 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

7 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 4, 6, and 7 for the next clock edge listed in the table in step 4, until all listed clock edges have been tested.

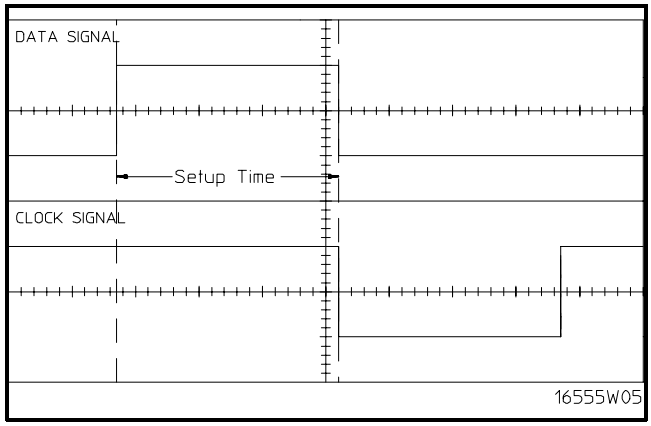
8 Enable the pulse generator channel 1 COMP (with the LED on).

9 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



Disregard the oscilloscope Period(2) value. The settings provided in this procedure measure the period from rising edge to rising edge, which is not a valid measurement.

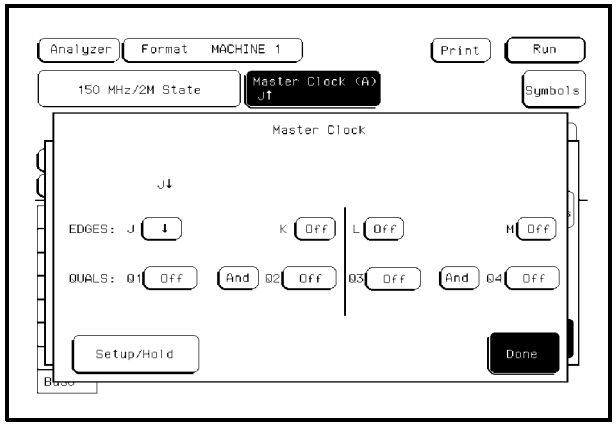
10 Select the clock to be tested.

a In the Master Clock menu, select the clock field to be tested, then select the clock edge as indicated in the table. The first time through this test, use the top clock and edge.

Clocks
J↓
K↓
L↓
M↓

b Connect the clock to be tested to the pulse generator channel 1 output.

c Select Done to exit the Master Clock menu.



11 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

12 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 10, 11, and 12 for the next clock edge listed in the table in step 11, until all listed clock edges have been tested.

13 Test the next setup/hold combination.

a In the logic analyzer Format menu, press Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 1 through 13 for the next setup/hold combination listed in step 1 on page 3–24, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

Connect the next combination of data channels and clock channels, then test them.

Start on page 3–20, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the multiple-clock, multiple-edge, state acquisition (logic analyzer)

Testing the multiple-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for multiple-clock, multiple-edge, state acquisition

This test checks two combinations of data using multiple clocks at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	150 MHz 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 2	Mode: Square
Period: 6.666 ns	Divide: PULSE ÷ 2	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 4.000 ns	Offs: 0.00 V	
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V

b Disable the pulse generator channel 1 COMP (with the LED off).

3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

Set up the logic analyzer

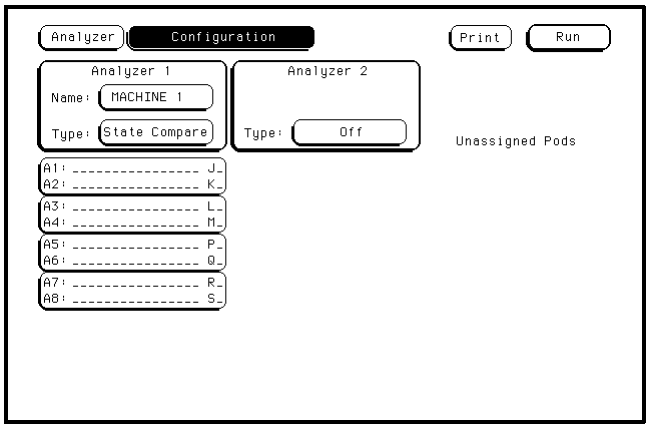
Do the following steps if you have not already done them for a previous test.

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign pods, select the pod fields, then select Machine 1.

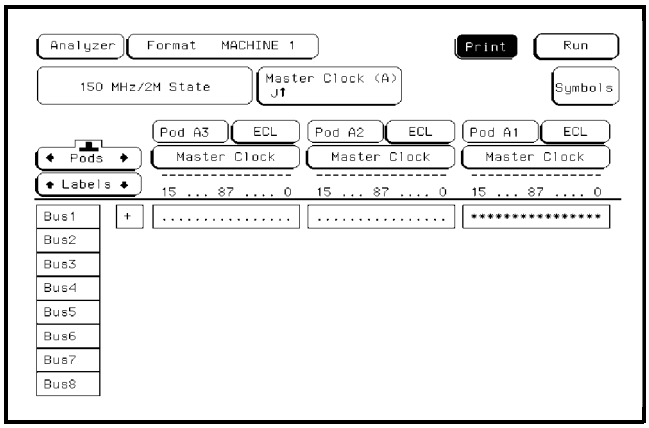
c In the Analyzer 1 box, select the Type field, then select State Compare.



2 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each Pod field, then select ECL. The screen does not show all Pod fields at one time. Use the knob to access more Pod fields.



3 Set up the Trigger menu.

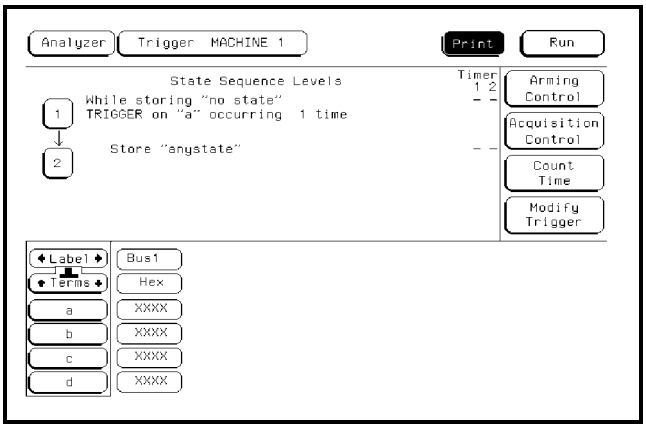
a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All in the pop-up menu.

b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

c Select Acquisition Control. If the Acquisition Control is "Manual," use the cursor keys to move the cursor to the Acquisition Mode field. Press the "Select" key to toggle this field to "Automatic."

d In the Acquisition Control menu, use the knob to set the Memory Length to 4096. Press the Done key.

e Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate", then select "no state." Select Done to exit the State Sequence Levels menu.



Connect the logic analyzer

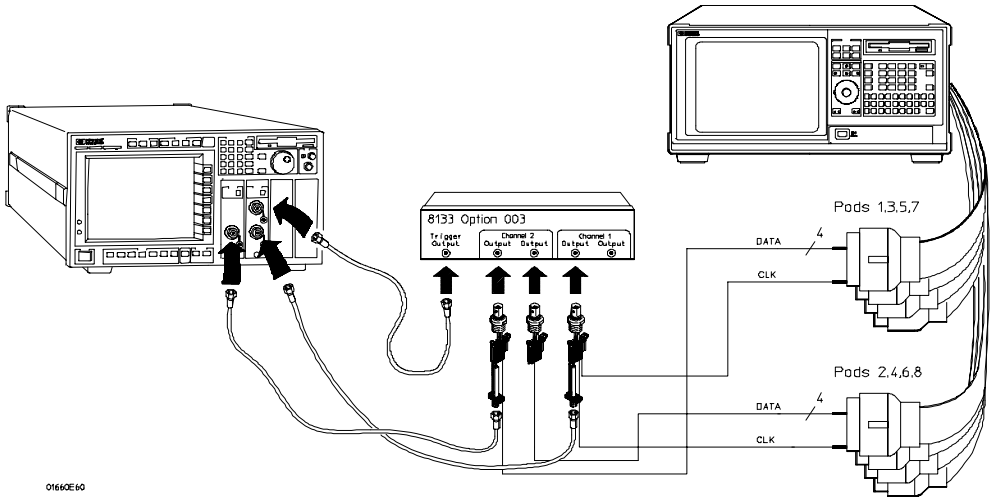
1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an Agilent 1670G or Agilent 1671G, you will repeat this test for the second combination.

2 Using SMA cables, connect channel 1, channel 2, and trigger of the oscilloscope to the pulse generator.

Connect the Agilent 1670G or Agilent 1671G Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 $\overline{\text{Output}}$	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3 *	J-clock K-clock L-clock M-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11 *	J-clock K-clock L-clock M-clock

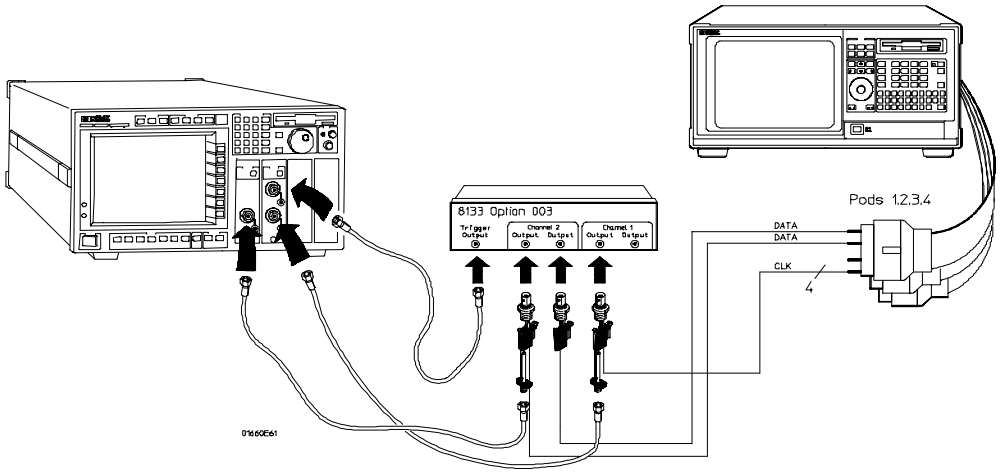
*Agilent 1670G only.



Connect the Agilent 1672G or Agilent 1673G Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3	Pod 1, channel 11	J-clock
	Pod 2, channel 3	Pod 2, channel 11	K-clock
	Pod 3, channel 3	Pod 3, channel 11 *	L-clock
	Pod 4, channel 3	Pod 4, channel 11 *	M-clock

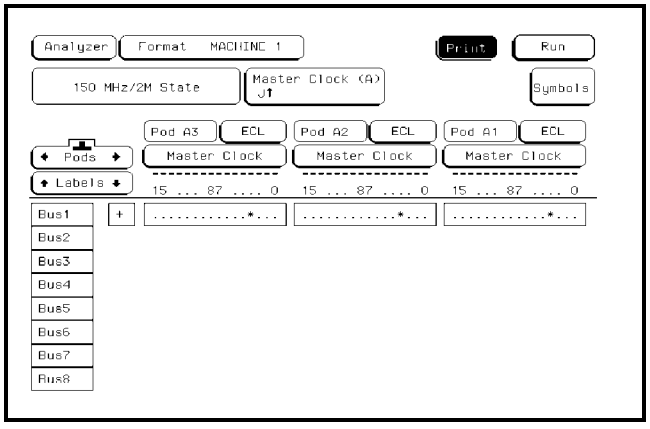
*Agilent 1672G only.



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested. Press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.



4 Configure the trigger according to the connected channels.

a. Press the Trigger key.

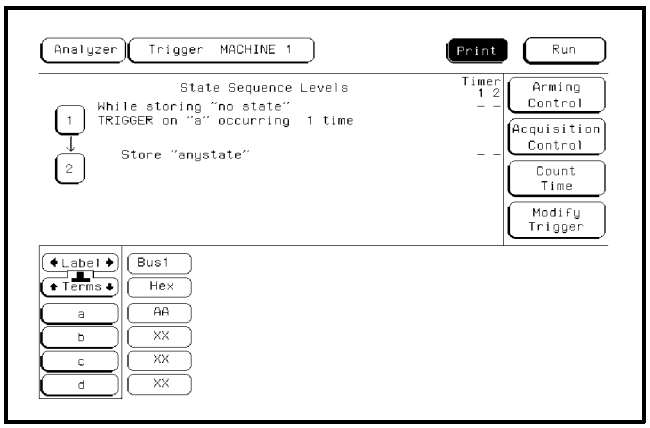
b. Select the field next to the pattern recognizer "a" under the label Bus1. Type the following for your logic analyzer, then press Select.

Agilent 1670G – "AA"

Agilent 1672G – "AA"

Agilent 1671G – "2A"

Agilent 1673G – "A"



5 Enable the pulse generator channel 1, channel 2, and trigger ouputs (with the LEDs off).

Verify the test signal

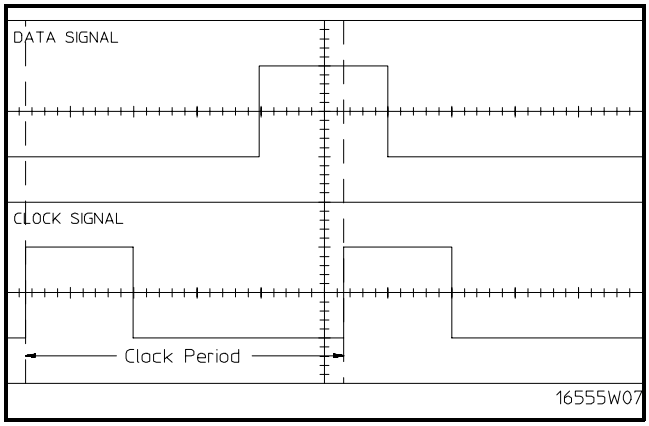
1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 6.666 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

c On the oscilloscope, select [Shift] Period: channel 2, then select [Enter] to display the clock period (Period(2)). If the period is not less than 6.666 ns, go to step d. If the period is less than 6.666 ns, go to step 2.

d In the oscilloscope Timebase menu, increase Position 6.666 ns. If the period is not less than 6.666 ns, decrease the pulse generator Period in 10 ps increments until one of the two periods measured is less than 6.666 ns.

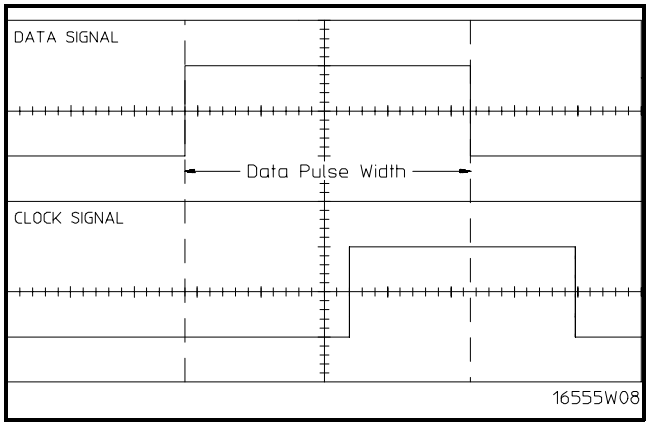


2 Check the data pulse width. Using the oscilloscope verify that the data pulse width is 4.000 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

b On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width (1)).

c If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock edges, multiple clocks

1 Select the logic analyzer setup/hold time.

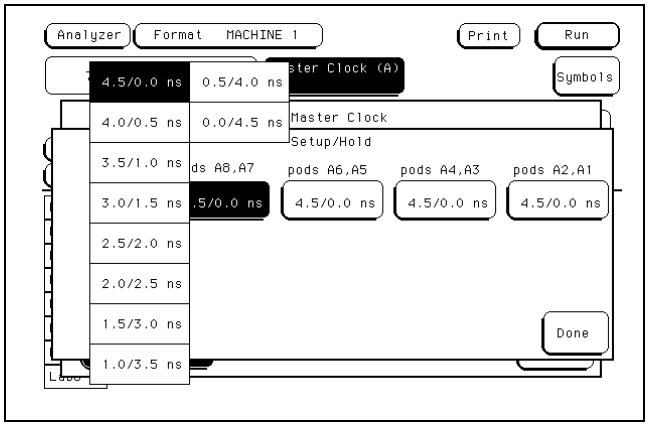
a In the logic analyzer Format menu, select Master Clock.

b Select and activate any two clock edges.

c Select the Setup/Hold field and select the setup/hold to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
4.0/0.0 ns
-0.5/4.5 ns

d Select Done to exit the setup/hold combinations.



2 Disable the pulse generator channel 1 COMP (with the LED off).

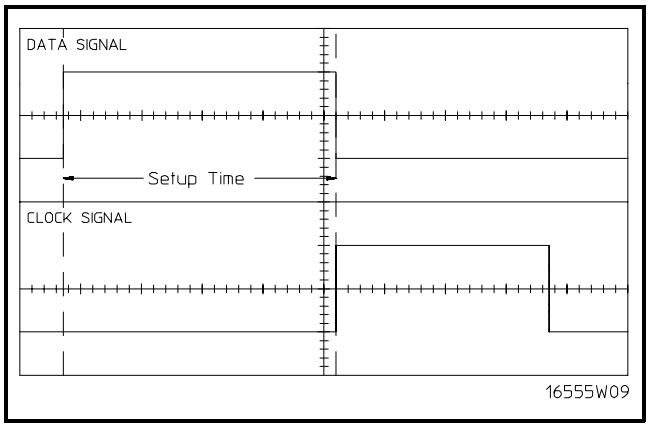
3 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the rising edge of the clock waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



Disregard the oscilloscope Period(2) value. The settings provided in this procedure measure the period from falling edge to falling edge, which is not a valid measurement.

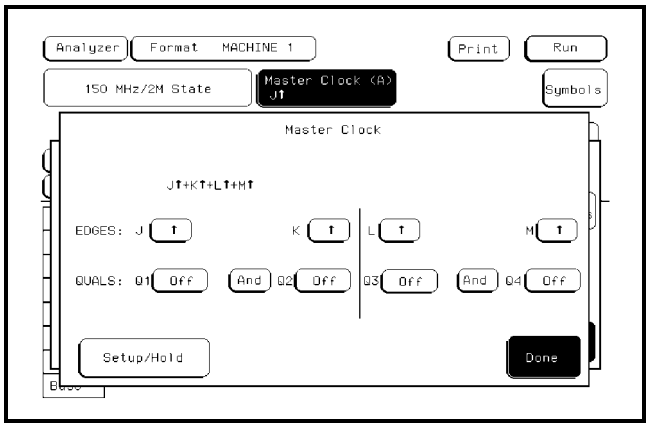
4 Select the clocks to be tested.

a Select the clock field to be tested and then select the clock edges as indicated in the table.

Clocks
J↑ + K↑ + L↑ + M↑

b Connect the rising edge clocks to the pulse generator channel 1 output.

c Select Done to exit the Master Clock menu.



5 Note: Do this step if you have not already created a Compare file for the previous test (single-clock, single-edge state acquisition), use the following steps to create one. For subsequent passes through this test, skip this step and go to step 6.

Use the following to create a Compare file:

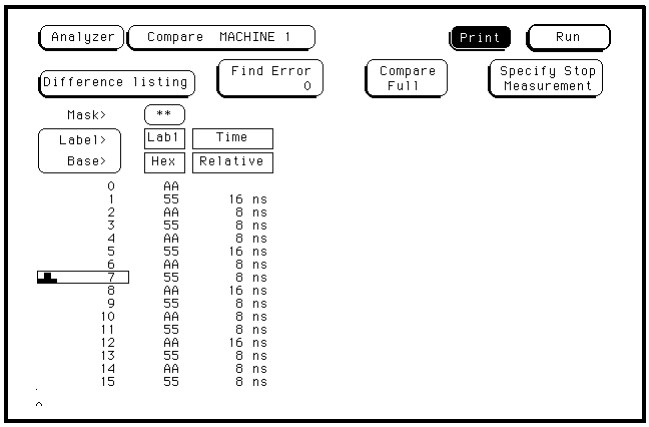
a Press Run. The display should show an alternating pattern of "AA" and "55." Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key. Select Execute.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop-up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop-up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



6 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

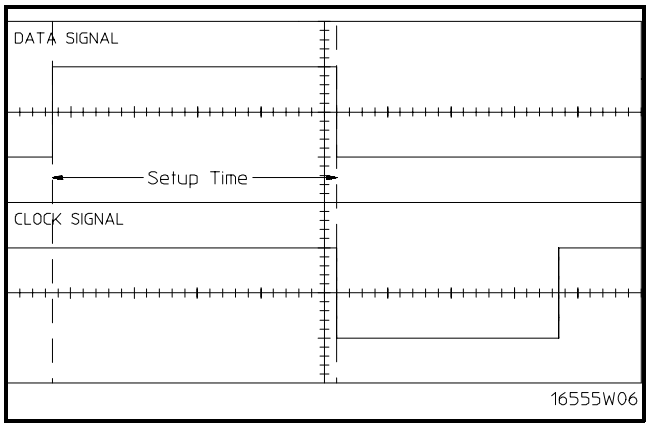
7 Enable the pulse generator channel 1 COMP (with the LED on).

8 Using the Delay mode of the pulse generator channel 1, position the pulses according to the setup/hold combination selected, +0.0 ps or -100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: falling.

b On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

c Adjust the pulse generator channel 1 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



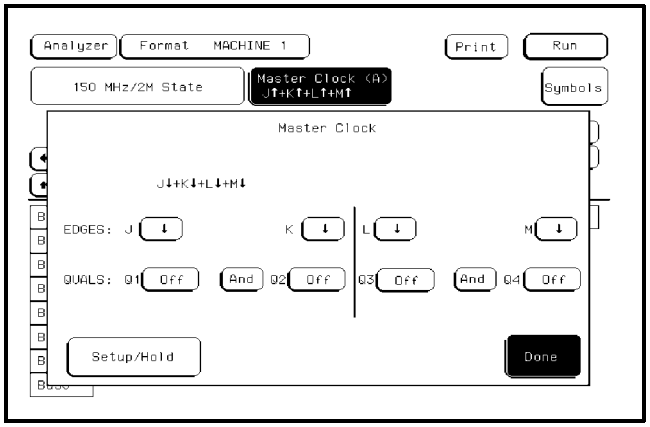
Disregard the oscilloscope Period(2) value. The settings provided in this procedure measure the period from rising edge to rising edge, which is not a valid measurement.

9 Select the clocks to be tested.

a Select the clock field to be tested, then select the clock edges as indicated in the table.

Clocks
J↓ + K↓ + L↓ + M↓

b Select Done to exit the Master Clock menu.



10 Press the blue shift key, then press the Run key. If two to four acquisitions are obtained without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

11 Test the next clocks.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clocks just tested.

c Repeat steps 2 through 11 for the next clock edges listed in the table in step 4, until all listed clock edges have been tested.

12 Test the next setup/hold combination.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clocks just tested.

c Repeat steps 1 through 12 for the next setup/hold combination listed in step 1 on page 3-36, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

Connect the next combination of data channels and clock channels, then test them.

Start on page 3–32 "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the single-clock, multiple-edge, state acquisition (logic analyzer)

Testing the single-clock, multiple-edge, state acquisition verifies the performance of the following specifications:

- Minimum master-to-master clock time
- Maximum state acquisition speed
- Setup/Hold time for single-clock, multiple-edge, state acquisition

This test checks two combinations of data using a multiple-edge single clock at two selected setup/hold times.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	150 MHz 3.0 ns pulse width, < 600 ps rise time	8133A option 003
Digitizing Oscilloscope	≥ 6 GHz bandwidth, < 58 ps rise time	54750A w/ 54751A
Adapter	SMA(m)-BNC(f)	1250-1200
SMA Coax Cable (Qty 3)	18 GHz bandwidth	8120-4948
Coupler	BNC(m)(m)	1250-0216
BNC Test Connector, 6x2 (Qty 4)		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes before beginning the test if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 1	Mode: Square
Period: 13.333 ns	Divide: PULSE ÷ 1	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 3.500 ns	Offs: 0.00 V	

3 Set up the oscilloscope. If the oscilloscope was not configured for the previous test, then do the following steps.

a Select Setup, then select Default Setup.

b Configure the oscilloscope according to the following table.

Oscilloscope Setup

Acquisition	**Display**	**Trigger**	**[Shift] Δ Time**
Averaging: On # of averages: 16	Graticule Graphs: 2	Level: -250 mV	Stop src: channel 2 [Enter]

Channel 1	**Channel 2**	**Define meas**
Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: –1.300 V	Alternate Scale Attenuation: 20.00:1 Scale: 200 mV/div Offset: -1.300 V	Thresholds: user-defined Units: Volts Upper: -980 mV Middle: -1.30 V Lower: -1.62 V

Set up the logic analyzer

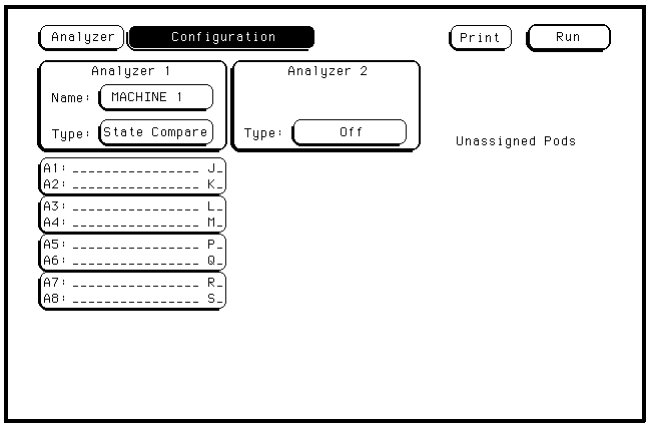
Do the following steps if you have not already done them for a previous test.

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign all pods to Machine 1. To assign all pods, select the pod fields, then select Machine 1 in the pop-up menu.

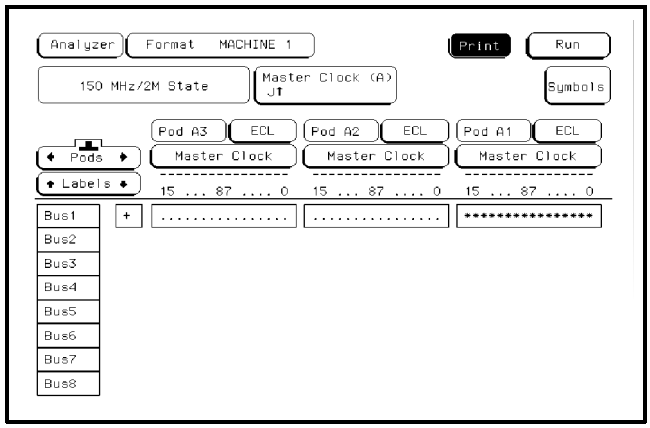
c Select the Type field in the Analyzer 1 box, then select State Compare.



2 Set up the Format menu.

a Press the Format key.

b Select the field to the right of each pod field, then select ECL. The screen does not show all pod fields at one time. Use the knob to access pod fields not shown on the screen.



3 Set up the Trigger menu.

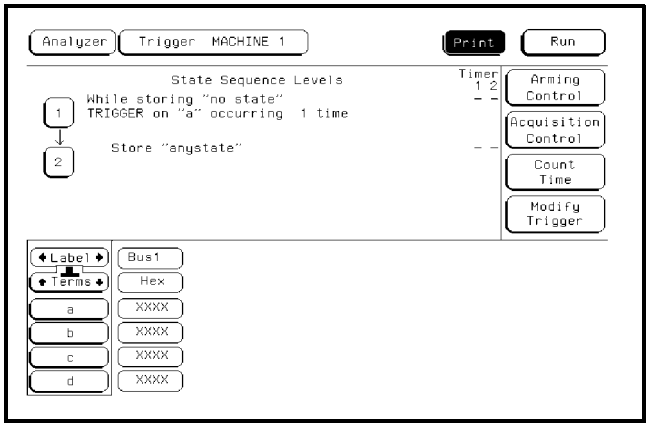
a Press the Trigger key. Select Modify Trigger, then select Clear Trigger, then select All in the pop-up menu.

b Select Count Off. Press Select again, then select Time in the pop-up menu. Select Done to exit the menu.

c Select Acquisition Control. If the Acquisition Control is "Manual," use the cursor keys to move the cursor to the Acquisition Mode field. Press the "Select" key to toggle this field to "Automatic."

d In the Acquisition Mode menu, use the knob to set the Memory Length to 4096.

e Select the field labeled 1 under the State Sequence Levels. Select the field labeled "anystate," then select "no state." Select Done to exit the State Sequence Levels menu.



Connect the logic analyzer

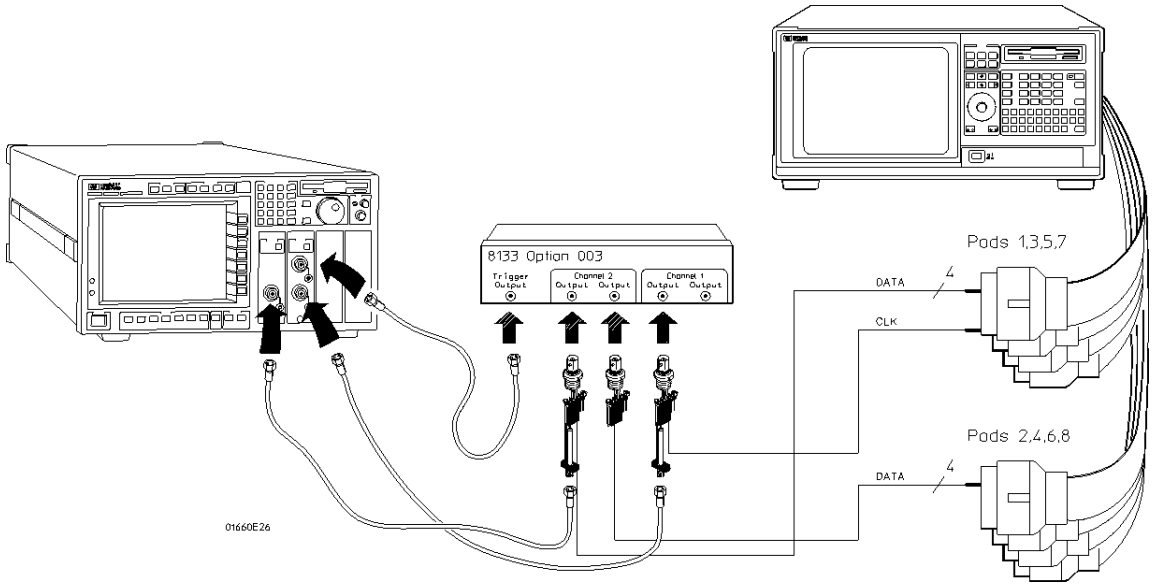
1 Using the 6-by-2 test connectors, connect the first combination of logic analyzer clock and data channels listed in one of the following tables to the pulse generator.
If you are testing an Agilent 1670G or Agilent 1671G, you will repeat this test for the second combination.

2 Using the SMA cables, connect channel 1, channel 2, and trigger from the oscilloscope to the pulse generator.

Connect the Agilent 1670G or Agilent 1671G Logic Analyzer to the Pulse Generator

Testing Combinations	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 3, channel 3 Pod 5, channel 3 Pod 7, channel 3	Pod 2, channel 3 Pod 4, channel 3 Pod 6, channel 3 Pod 8, channel 3 *	J-clock
2	Pod 1, channel 11 Pod 3, channel 11 Pod 5, channel 11 Pod 7, channel 11	Pod 2, channel 11 Pod 4, channel 11 Pod 6, channel 11 Pod 8, channel 11 *	J-clock

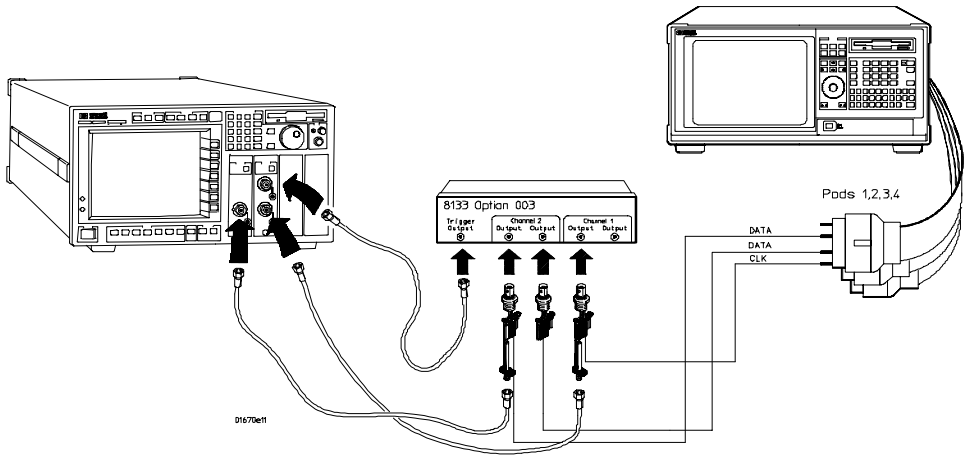
*Agilent 1670G only



Connect the Agilent 1672G or 1673G Logic Analyzer to the Pulse Generator

Testing Combination	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 2 Output	Connect to 8133A Channel 1 Output
1	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 Pod 4, channel 3	Pod 1, channel 3 Pod 2, channel 3 Pod 3, channel 3 * Pod 4, channel 3 *	J-clock

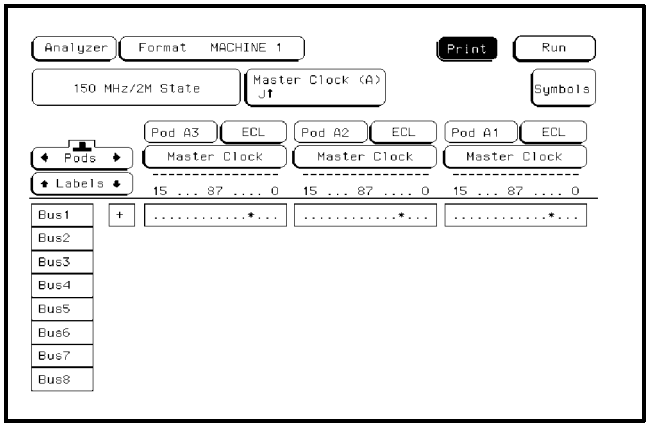
*Agilent 1672G only



3 Activate the data channels that are connected according to one of the previous tables.

a Press the Format key.

b Select the field showing the channel assignments for one of the pods being tested. Press the Clear entry key. Using the arrow keys, move the selector to the data channels to be tested, then press the Select key. An asterisk means that a channel is turned on. When all the correct channels of the pod are turned on, press the Done key. Follow this step for the remaining pods.



4 Configure the trigger according to the connected channels.

a Press the Trigger key.

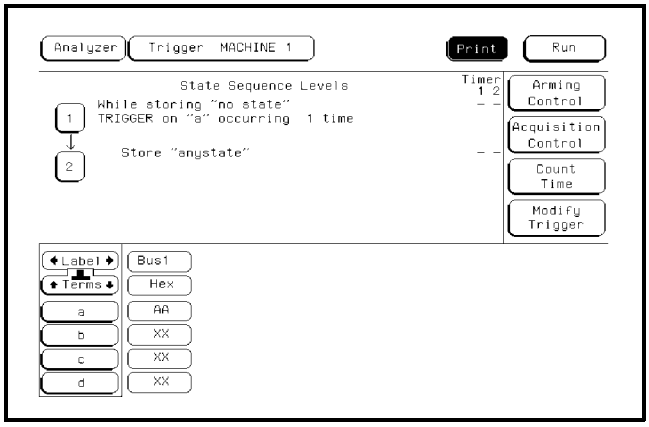
b Select the field next to "a" under the label Bus1. Type the following for your logic analyzer, then press the Select key.

Agilent 1670G – "AA"

Agilent 1672G – "AA"

Agilent 1671G – "2A"

Agilent 1673G – "A"



5 Enable the pulse generator channel 1, channel 2, and trigger outputs (with the LEDs off).

Verify the test signal

1 Check the clock period. Using the oscilloscope, verify that the master-to-master clock time is 6.666 ns, +0 ps or – 100 ps.

a Enable the pulse generator channel 1, channel 2, and trigger outputs (LED off).

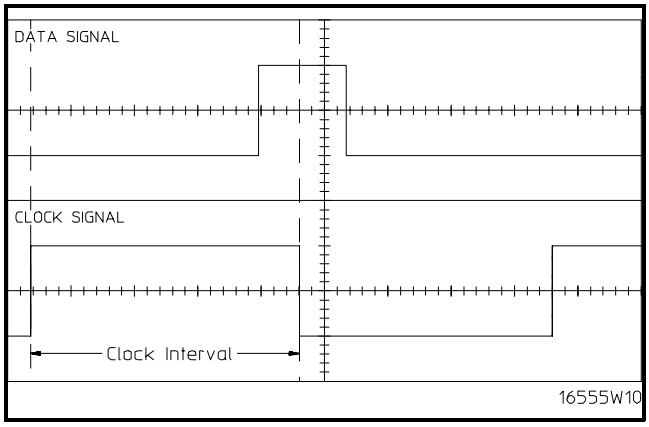
b In the oscilloscope Timebase menu, select Scale: 2.000 ns/div.

c In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the clock waveform so that a rising edge appears at the left of the display.

d On the oscilloscope, select [Shift] + width: channel 2, then select [Enter] to display the master-to-master clock time (+ width(2)). If the positive-going pulse width is more than 6.666 ns, go to step d. If the positive-going pulse width is less than or equal to 6.666 ns but greater than 6.566 ns, go to step 2.

e On the oscilloscope, select [Shift] - width: channel 2, then select [Enter] (- width(2)). If the negative pulse width is less than or equal to 6.666 ns but greater than 6.566 ns, go to step 2.

f Decrease the pulse generator Period in 100 ps increments until the oscilloscope + width (2) or - width (2) read less than or equal to 6.666 ns, but greater than 6.566 ns.



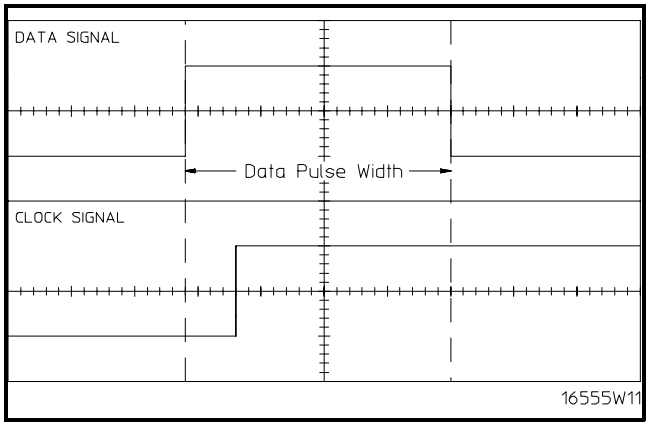
2 Check the data pulse width. Using the oscilloscope, verify that the data pulse width is 3.500 ns, +0 ps or –100 ps.

a In the oscilloscope Timebase menu, select Scale: 1.000 ns/div.

b In the oscilloscope Timebase menu, select Position. Using the oscilloscope knob, position the data waveform so that the waveform is centered on the screen.

c On the oscilloscope, select [Shift] + width: channel 1, then select [Enter] to display the data signal pulse width (+ width(1)).

d If the pulse width is outside the limits, adjust the pulse generator channel 2 width until the pulse width is within limits.



Check the setup/hold with single clock, multiple clock edges

1 Select the logic analyzer setup/hold time.

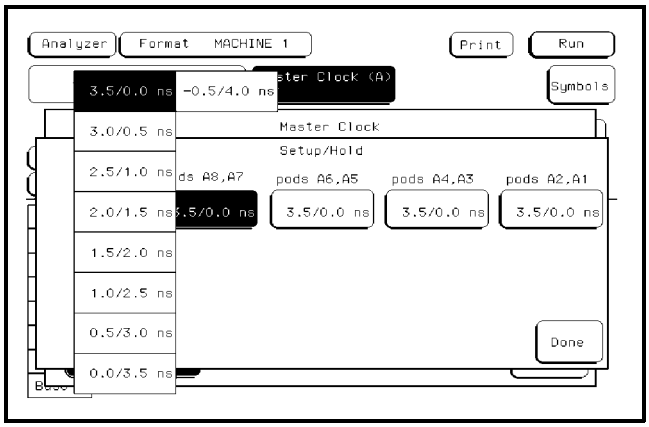
a In the logic analyzer Format menu, select Master Clock.

b Select and activate any multiple clock edge.

c Select the Setup/Hold field, then select the setup/hold to be tested for all pods. The first time through this test, use the top combination in the following table.

Setup/Hold Combinations
3.5/0.0 ns
-0.5/4.0 ns

d Select Done to exit the setup/hold combinations.



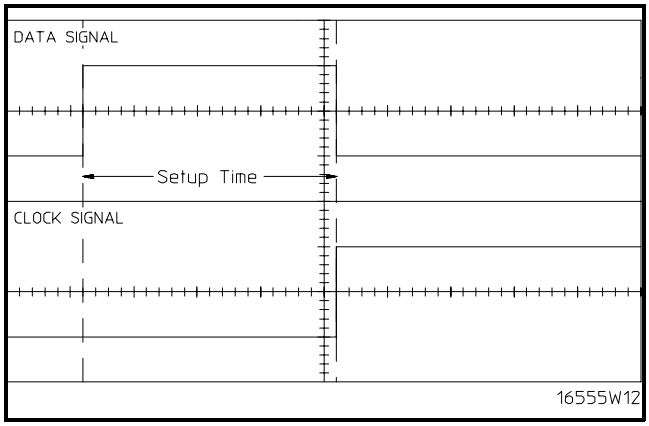
2 Using the Delay mode of the pulse generator channel 2, position the pulses according to the setup time of the setup/hold combination selected, +0.0 ps or –100 ps.

a On the Oscilloscope, select [Define meas] Define Δ Time - Stop edge: rising.

b In the oscilloscope timebase menu, select Position. Using the oscilloscope knob, position the falling edge of the data waveform so that it is centered on the display.

c On the oscilloscope, select [Shift] Δ Time. Select Start src: channel 1, then select [Enter] to display the setup time (Δ Time(1)-(2)).

d Adjust the pulse generator channel 2 Delay until the pulses are aligned according the the setup time of the setup/hold combination selected, +0.0 ps or -100 ps.



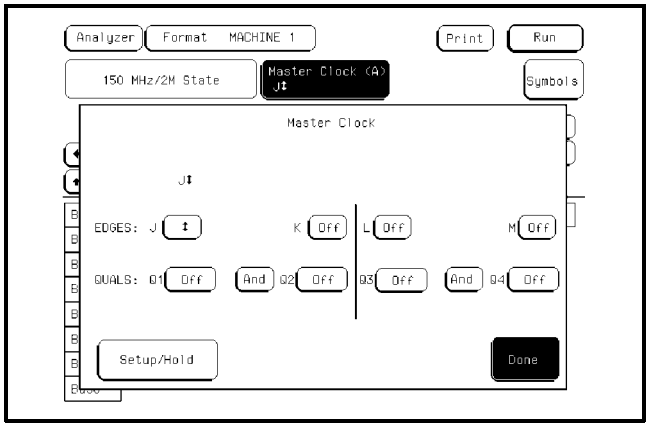
3 Select the clock to be tested.

a Select the clock field to be tested, then select the clock as indicated in the table. The first time through this test, use the top multiple-edge clock in the following table.

Clocks
J↕
K↕
L↕
M↕

b Connect the clock to be tested to the pulse generator channel 1 output.

c Select Done to exit the Master Clock menu.



4 Note: Do this step if you have not already created a Compare file for one of the previous tests, use the following steps to create one. For subsequent passes through this test, skip this step and go to step 5.

Use the following to create a Compare file:

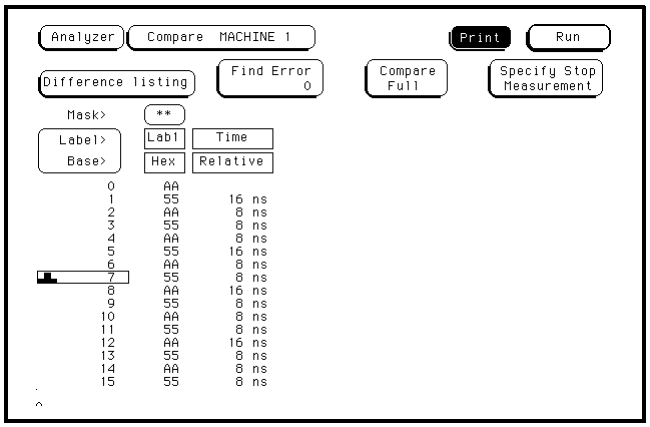
a Press Run. The display should show an alternating pattern of "AA" and "55." Verify the pattern by scrolling through the display.

b Press the List key. In the pop-up menu, use the knob to move the cursor to Compare. Press Select.

c In the Compare menu, move the cursor to Copy Listing to Reference, then press the Select key. Select Execute.

d Move the cursor to Specify Stop Measurement and press the Select key. Press Select again to turn on Compare. At the pop-up menu, select Compare. Move the cursor to the Equal field and press the Select key. At the pop-up menu, select Not Equal. Press Done.

e Move the cursor to the Reference Listing field and select. The field should toggle to Difference Listing.



5 Press the blue shift key, then press the Run key. If the analyzer obtains two to four acquisitions without the "Stop Condition Satisfied" message appearing, then the test passes. Press Stop to halt the acquisition. Record the Pass or Fail results in the performance test record.

6 Test the next clock.

a Press the Format key, then select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 4, 6 and 7 for the next clock listed in the table in step 4, until all clocks have been tested.

7 Test the next setup/hold combination.

a In the logic analyzer Format menu, select Master Clock.

b Turn off and disconnect the clock just tested.

c Repeat steps 1 through 10 for the next setup/hold combination listed in step 1 on page 3–48, until all listed setup/hold combinations have been tested.

When aligning the data and clock waveforms using the oscilloscope, align the waveforms according to the setup time of the setup/hold combination being tested, +0.0 ps or –100 ps.

Test the next channels

- Connect the next combination of data channels and clock channels, then test them.

  Start on page 3–44, "Connect the logic analyzer," connect the next combination, then continue through the complete test.

To test the time interval accuracy (logic analyzer)

Testing the time interval accuracy does not check a specification, but does check the following:

- 125-MHz oscillator

This test verifies that the 125-MHz timing acquisition synchronizing oscillator is operating within limits.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Pulse Generator	150 MHz, 3.0 ns pulse width, < 600 ps rise time	8133A Option 003
Function Generator	Accuracy $\leq (5)(10^{-6}) \times$ frequency	3325B Option 002
SMA Cable		8120-4948
Adapter	BNC(m)-SMA(f)	1250-2015
BNC Test Connector, 6x2		

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

2 Set up the pulse generator according to the following table.

Pulse Generator Setup

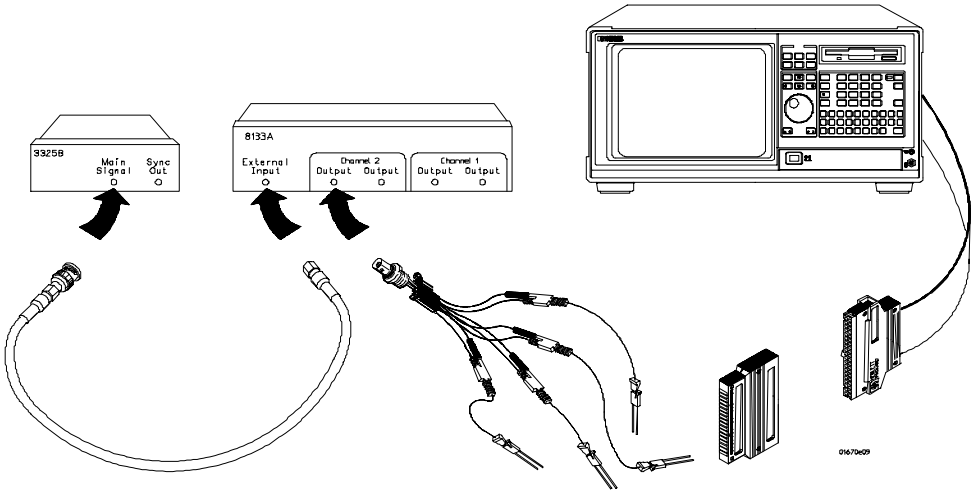
Timebase	Channel 1	Trigger
Mode: Ext	Mode: Square	Divide: Divide ÷ 1
Period: 25.000 ns	Delay: 0.000 ns	Ampl: 0.50 V
	High: –0.90 V	Offs: 0.00 V
	Low: –1.70 V	
	COMP: Disabled (LED off)	

3 Set up the function generator according to the following table.

Function Generator Setup
Freq: 40.000 00 MHz
Amptd: 1.00 V
Modulation: Off

Connect the logic analyzer

1 Using a 6-by-2 test connector, connect channel 0 of Pod A1 to the pulse generator channel 1 output.
2 Using the SMA cable and the BNC adapter, connect the External Input of the pulse generator to the Main Signal of the function generator.



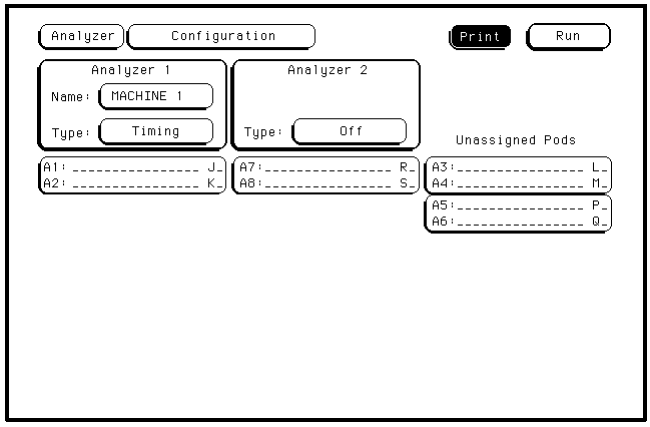
Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key.

b In the Configuration menu, assign Pod 1 to Machine 1. To assign Pod 1, select the Pod 1 field, then select Machine 1.

c In the Analyzer 1 box, select the Type field, then select Timing.

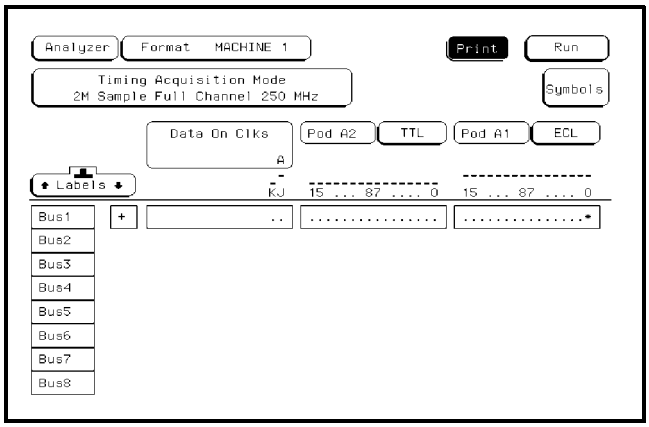


2 Set up the Format menu.

a Press the Format key. Select Timing Acquisition Mode, then select Full Channel 250 MHz.

b Select the field to the right of the Pod A1 field, then select ECL.

c Select the field showing the channel assignments for Pod A1. Deactivate all channels by pressing the Clear entry key. Using the arrow keys, move the selector to Channel 0. Press the Select key to put an asterisk in the channel position, activating the channel, then press the Done key.



3 Set up the Trigger menu.

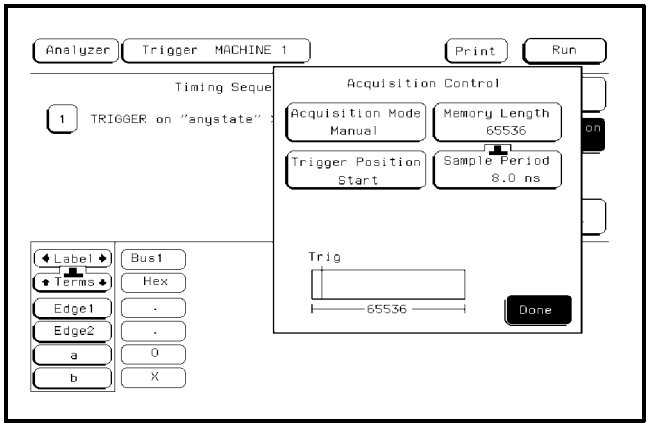
a Select Acquisition Control. Select the Acquisition Mode field, and the acquisition mode should toggle to Manual.

b Select Trigger Position. In the Pop-up menu, select Start.

c Select the Sample Period field. In the numeric pop-up menu, select 8 ns.

d Select the Memory Length field, and then use the RPG to select 65536.

e Press the Done key to exit the Acquisition Control menu.



4 Enable the pulse generator channel 1 output (with the LED off).

5 Set up the Waveform menu.

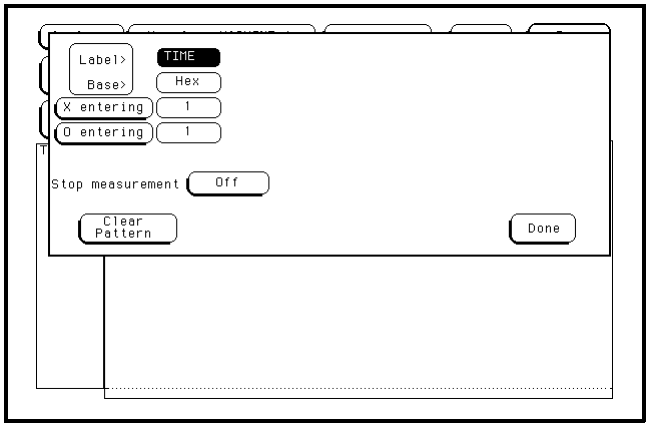
a Press Run to fill the acquisition memory so the markers can be configured.

b Press the Waveform key.

c Move the cursor to the sec/Div field, then use the knob to dial in 100 ns.

d Select the Markers Off field, then select Pattern.

e Select the Specify Patterns field. Select X entering 1 and O entering 1.

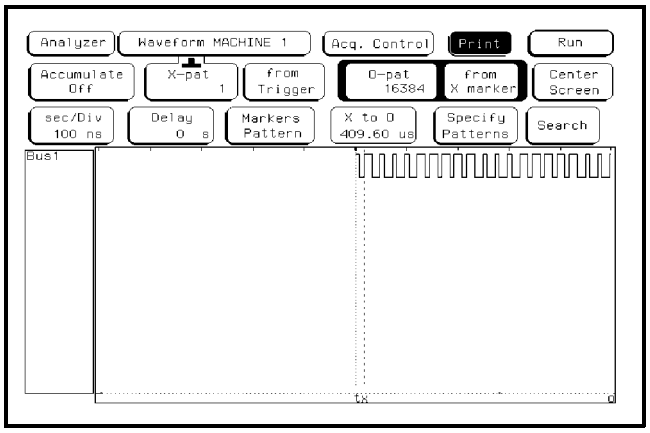


f Select Done to exit the Specify Patterns menu.

g Move the cursor to the X-pat field. Type 1, then press Done.

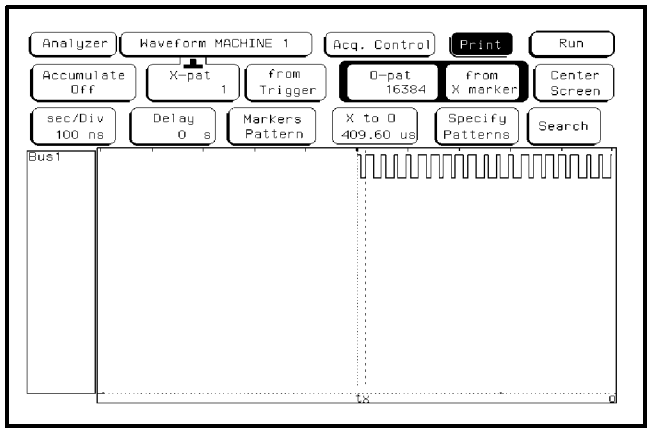
h Move the cursor to the O-pat field. Type 16384, then press Done.

i Select O-pat from Trigger field, and then select from X marker.



Acquire the data

1 Press the blue key, then press the Run key to select Run-Repetitive. Allow the logic analyzer to acquire data for at least 1 minute. Observe the X to O time field and ensure the X marker to O marker time is between 409.56 and 409.64 µs during the test.



Record the results in the performance test record.

To test the input resistance (oscilloscope)

Testing the input resistance verifies the performance of the following specification:

- Input resistance

This test checks the input resistance at the 50 Ω and 1 MΩ settings in the Coupling field.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	Measure resistance (4-wire) better than 0.25% accuracy	3458A
Cables (2)	BNC (m)(m) 48-inch	8120-1840
Adapter	BNC Tee (m)(f)(f)	1250-0781
Adapters (2)	BNC (f) to Dual Banana Plug	1251-2277

Set up the equipment

1. Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.
2. Set up the multimeter to make a 4-wire resistance measurement.

Set up the logic analyzer

1 Set up the Channel menu.

a Press the Config key.

b At the pop up menu, select Scope Channel.

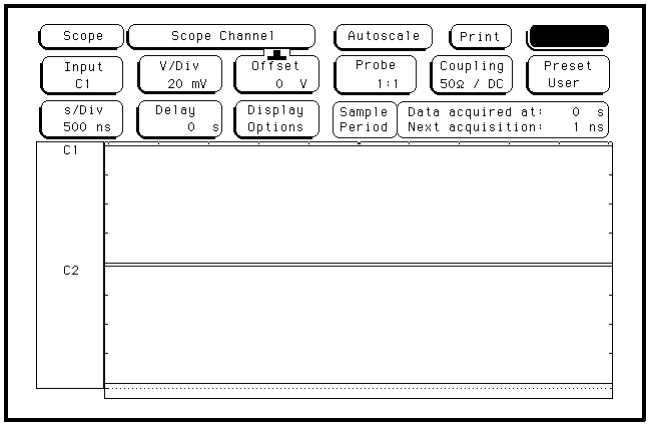
c Select the Input field, then select C1.

d Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

e Move the cursor to the V/Div field, then use the RPG knob to dial in 20 mV.

f Move the cursor to the Offset field. Set the Offset to 0 V by typing 0, then pressing the Select key.

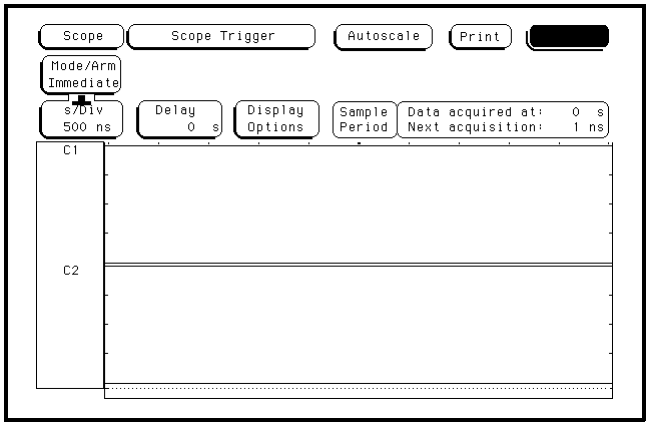
g Select the Coupling field, then select 50Ω / DC.



2 Set up the Trigger menu.

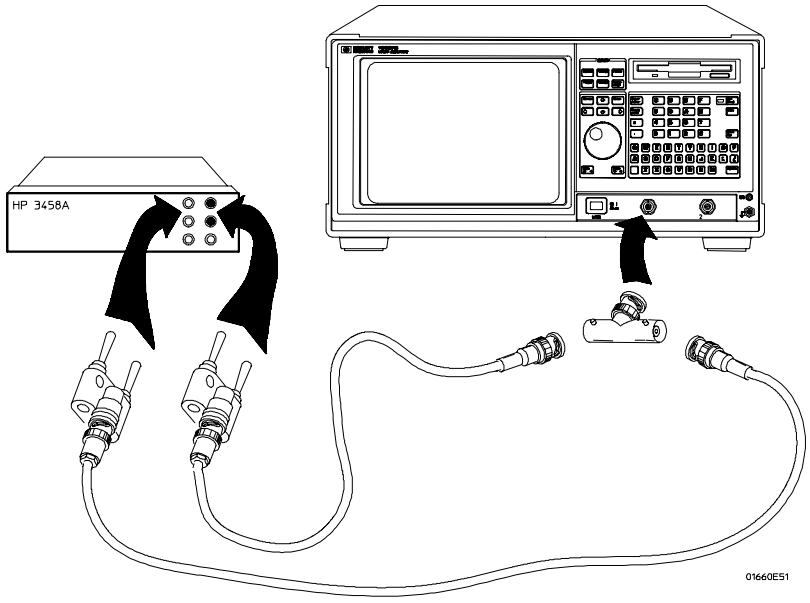
a Press the Trigger key.

b Select the Mode/Arm field, then select Immediate.



Connect the logic analyzer

Using the BNC-to-banana adapters, connect one end of each BNC cable to the 4-wire resistance connections on the multimeter, and connect the free ends of the cables to the BNC Tee. Connect the male end of the BNC tee to the channel 1 input of the oscilloscope module.



Acquire the data

1. Press the RUN key. The clicking of attenuator relays should be audible. Verify resistance readings on the digital multimeter of 50 Ω ± 0.5 Ω (49.5 to 50.5 Ω). Record the reading in the performance test record.
2. In the Channel menu change the Coupling field to 1MΩ / DC. The clicking of attenuator relays should be audible.
3. Press the RUN key. Verify resistance readings on the digital multimeter of 1 MΩ ± 10 kΩ (0.990 to 1.010 MΩ). Record the reading in the performance test record.
4. In the Channel menu change the Coupling field to 50 Ω/DC and V/Div to 200 mV/Div. Repeat steps 1 through 3.
5. In the Channel menu change the Coupling field to 50 Ω /DC and V/Div to 1 V/Div. Repeat steps 1 through 3.
6. In the Channel menu change the Coupling field to 50 Ω /DC and V/Div to 4 V/Div. Repeat steps 1 through 3.
7. Connect the male end of the BNC tee to the channel 2 input of the oscilloscope module.
8. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

See Also

If a reading is not within limits, then the attenuator for the out-of-bounds channel should be replaced (see chapter 6).

Perform an operational accuracy calibration

At this point, an operational accuracy calibration should be performed. Complete the following procedures in chapter 4, "Calibrating and Adjusting."

- "To test the CAL OUTPUT ports"
- "To calibrate the oscilloscope"
- "Self Cal menu calibrations"

To test the voltage measurement accuracy (oscilloscope)

Testing the voltage measurement accuracy verifies the performance of the following specification:

- Voltage measurement accuracy

This test verifies the DC voltage measurement accuracy of the instrument, using a dual cursor measurement that nullifies offset error.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
DC Power Supply	–14 Vdc to +14 Vdc, 0.1 mV resolution	3245A option 002
Digital Multimeter	Better than 0.1% accuracy	3458A
Cable	BNC (m)(m) 48-inch	8120-1840
Adapter (cable to power supply)	BNC (f) to Dual Banana Plug	1251-2277
Adapter	BNC tee (m)(f)(f)	1250-0781
Blocking Capacitor	BNC (m)(f) 0.18 µF, ±200 V	10240B
BNC Shorting Cap		1250-0074

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

Set up the logic analyzer

1 Set up the Channel menu.

a Press the Config key. In the pop up menu, select Scope Channel.

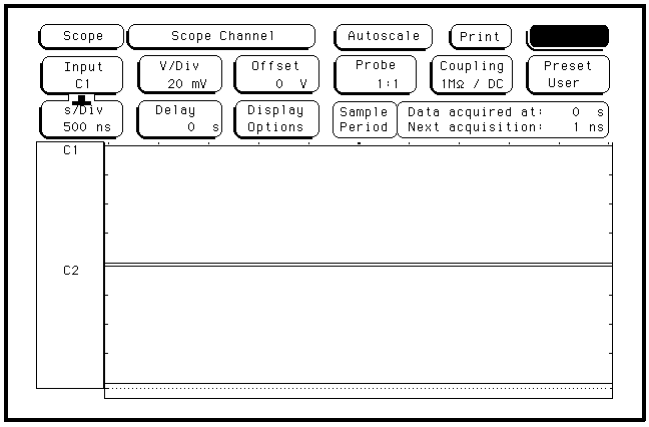
b Select the Input field, then select C1.

c Move the cursor to the Probe field, then use the RPG knob to dial in 1:1.

d Select the Coupling field, then select 1MΩ / DC.

CAUTION Set the Channel Coupling field to 1MΩ / DC or damage to the equipment will result.

e Move the cursor to the s/Div field, then use the RPG knob to dial in 500 ns.



2 Set up the Display menu.

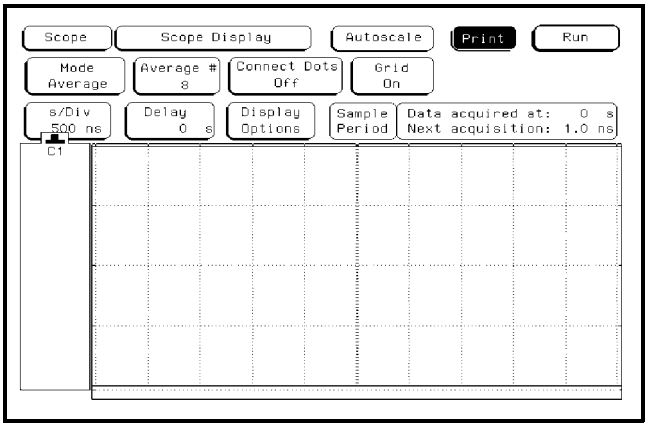
a Press the Display key.

b Select the Mode field, then select Average.

c Move the cursor to the Average # field. Type 8 on the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



3 Set up the Trigger menu.

a Press the Trigger key.

b Select the Mode/Arm field, then select Immediate.

4 Set up the Marker menu.

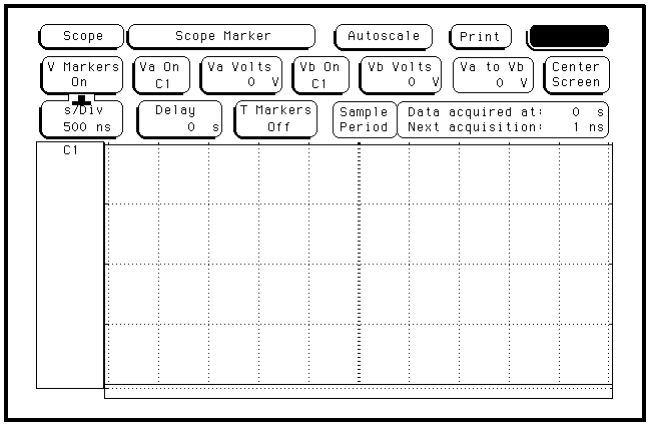
a Press the Marker key.

b Move the cursor to the V Markers field and press Select. The voltage markers should now be On.

c Select Va on C1.

d Select Vb on C1.

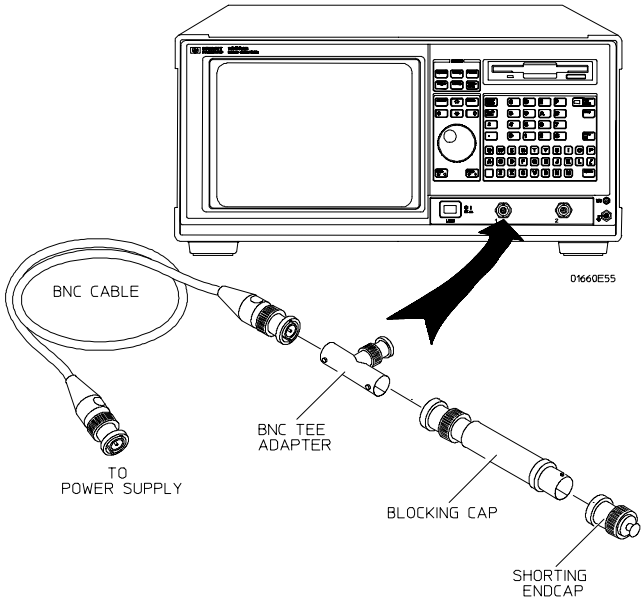
e If the T markers are On, turn the T markers Off by moving the cursor to the T markers field and pressing Select. Select Off.



Connect the logic analyzer

1 Using a BNC-to-banana adapter, connect one end of the cable to the power supply. Connect the BNC tee, the blocking capacitor, and the shorting endcap to the other end of the cable.

2 Monitor the power supply output with the Digital Multimeter.



Acquire the data

Use the following table for steps 1 through 5.

Oscilloscope Settings		Voltage Readings		
V/Div	**Offset**	**Supply**	**Upper Limit**	**Lower Limit**
4 V/Div	-7.0 V	-14.0 V	-13.7 V	-14.3 V
1 V/Div	-1.75 V	-3.50 V	-3.43 V	-3.57 V
400 mV/Div	-700.0 mV	-1.40 V	-1.37 V	-1.43 V
40 mV/Div	-70.0 mV	-140.0 mV	-137.0 mV	-143.0 mV
40 mV/Div	70.0 mV	140.0 mV	143.0 mV	137.0 mV
400 mV/Div	700.0 mV	1.40 V	1.43 V	1.37 V
1 V/Div	1.75 V	3.50 V	3.57 V	3.43 V
4 V/Div	7.0 V	14.0 V	14.3 V	13.7 V

1. Set up the oscilloscope according to the table above.
   - **a** Press the Chan key.
   - **b** Move the cursor to the V/Div field, then use the RPG knob to dial in the V/Div values shown on the first line of the table.
   - **c** Move the cursor to the Offset field. Use the front-panel keyboard to enter the offset value shown on the first line of the table. Use the left and right cursor-control keys to select either mV or V.
2. Acquire the zero input voltage.
   - **a** Disconnect the power supply from the channel input.
   - **b** Press the blue shift key, then press the Run key. Wait for approximately five seconds (averaging complete), then press Stop.
   - **c** Press the Markers key. Move the cursor to the Va Volts field. Using the RPG knob, move the Va marker over the oscilloscope trace on the display.
3. Acquire the measured voltage.
   - **a** Connect the power supply to the channel input. Set the power supply voltage according to the first line of the table above.
   - **b** Press the blue shift key, then press the Run key. Wait for approximately five seconds (averaging complete), then press Stop.
   - **c** Press the Markers key. Move the cursor to the Vb Volts field. Using the RPG knob, move the Vb marker over the oscilloscope trace on the display.
   - **d** Record the voltage in the Va to Vb field in the performance test record.
4. Repeat steps 1 through 3 for the second line of the table, then for the rest of the lines of the table for channel 1.
5. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

To test the offset accuracy (oscilloscope)

Testing the offset accuracy verifies the performance of the following specification:

- Offset accuracy

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
DC Power Supply	–35.000 to +35.000 Vdc, ± 1 mV resolution	3245A option 002
Digital Multimeter	Better than 0.1% accuracy	3458A
Cable	BNC (m)(m) 48-inch	8120-1840
Adapter (cable to power supply)	BNC (f) to Dual Banana Plug	1251-2277
Adapter	BNC tee (m)(f)(f)	1250-0781
Blocking Capacitor	BNC (m)(f) 0.18 μF, ±200 V	10240B
BNC Shorting Cap		1250-0074

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

c Move the cursor to the Probe field, press Select, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field, press Select, then use the PRG knob to dial in 4.00 V.

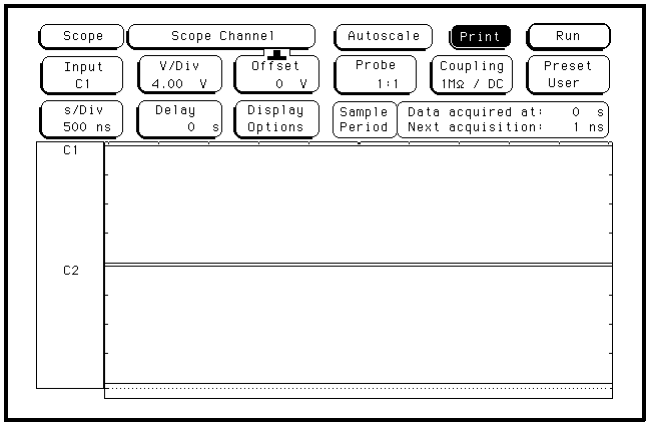
e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Select the Coupling field, then select 1MΩ / DC.

CAUTION

Set the Channel Coupling field to 1MΩ / DC or damage to the equipment will result.

g Move the cursor to the s/Div field, then use the RPG knob to dial in 500 ns.



2 Set up the Display menu.

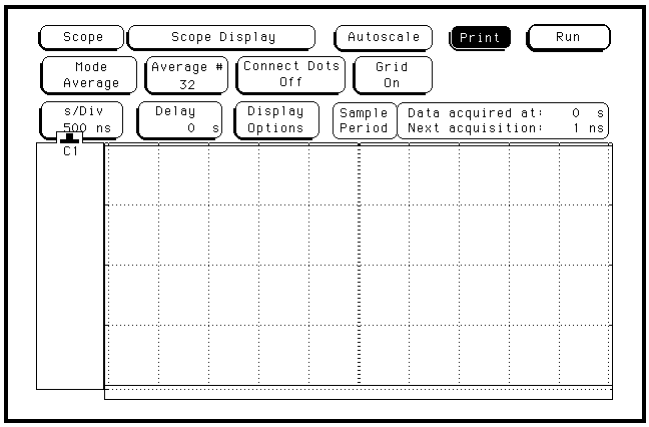
a Press the Display key.

b Select the Mode field, then select Average.

c Move the cursor to the Average # field. Type 32 on the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



3 Set up the Trigger menu.

a Press the Trigger key.

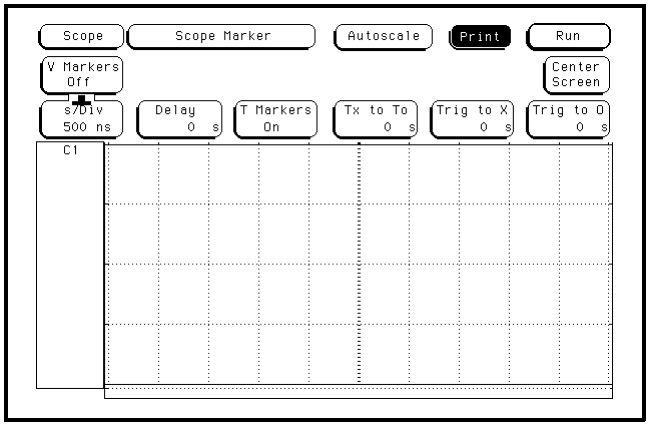
b Select the Mode/Arm field, then select Immediate.

4 Set up the Marker menu.

a Press the Marker key.

b Move the cursor to the T Markers field. Press Select, and then press On.

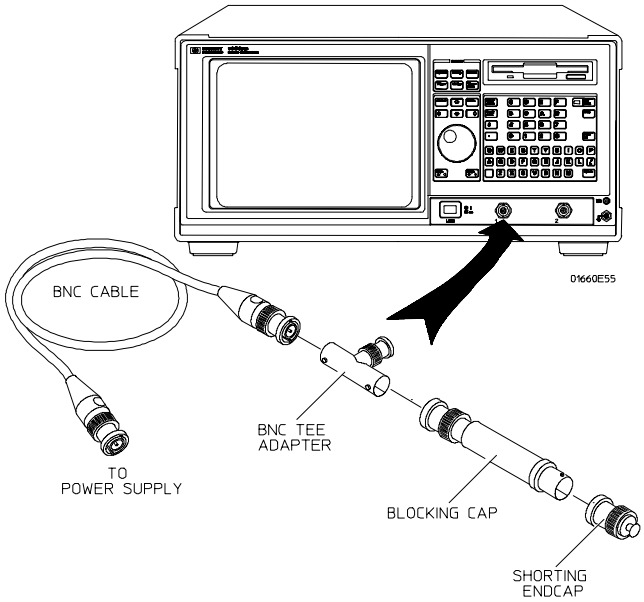
c If the V markers are On, turn the V markers Off by moving the cursor to the V markers field and pressing Select.



Connect the logic analyzer

1 Using a BNC-to-banana adapter, connect one end of the cable to the power supply. Connect the BNC tee, the blocking capacitor, and the shorting endcap to the other end of the cable.

2 Monitor the power supply output with the Digital Multimeter.



Acquire the zero input data

1. Disconnect the power supply from the channel input.
2. Press the Chan key. Move the cursor to the V/Div field and press the Select key.
3. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 320 mV) and enter the value in the performance test record.
4. Use the RPG knob to dial in 1 V/Div. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 80 mV) and enter the value in the performance test record.
5. Use the RPG knob to dial in 100 mV/Div. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 8 mV) and enter the value in the performance test record.
6. Use the RPG knob to dial in 10 mV/Div. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key. Read the voltage from the Markers voltage field (0.00 V ± 800 µV) and enter the value in the performance test record.

Acquire the DC input data

Use the following table for steps 1 through 5.

Multimeter Settings

Scope Settings		Power Supply Settings	Scope Readings	
V/Div	**Offset**	**Supply**	**Minimum**	**Maximum**
1 V/Div	–35.00 V	–35.00 V	–35.4 V	–34.6 V
200 mV/Div	–10.00 V	–10.00 V	–10.1 V	–9.90 V
20 mV/Div	–2.00 V	–2.00 V	–2.02 V	–1.98 V
20 mV/Div	+2.00 V	+2.00 V	+1.98 V	+2.02 V
200 mV/Div	+10.00 V	+10.00 V	+9.90 V	+10.1 V
1 V/Div	+35.00 V	+35.00 V	+34.6 V	+35.4 V

1. Connect the power supply to the oscilloscope channel 1 input. Set the power supply according to the first line of the table above.
2. Set up the oscilloscope according to the table above.
   a. Move the cursor to the V/Div field, then use the RPG knob to dial in the V/Div value shown on the first line of the table.
   b. Move the cursor to the Offset field. Use the front-panel keyboard to type in the offset value shown in the first line of the table. Use the left and right cursor-control keys to select either mV or V. Press the Select key.
3. Acquire the measured voltage.
   a. Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key.
   b. Read the voltage from the Markers voltage field. The value should be between the minimum and maximum values listed in the table. Record the value in the performance test record.
4. Repeat steps 1 through 3 for the second line of the table, then for the rest of the lines of the table for channel 1.
5. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

To test the bandwidth (oscilloscope)

Testing the bandwidth verifies the performance of the following specification:

- Bandwidth

This test verifies the bandwidth (dc coupled) of the instrument from dc to 500 MHz.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Signal Generator	1 - 250 MHz at approximately 170 mV rms	8656B
Power Meter/Sensor	1 - 250 MHz ± 3% accuracy	436/8482A
Power Splitter	Outputs differ by <0.15 dB	11667B
Cable	Type N (m)(m) 24-inch	11500B
Adapter	Type N (m) to BNC (f)	1250-0780

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

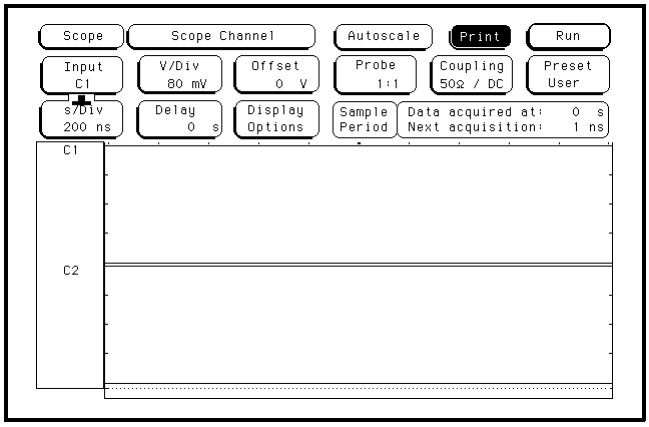
c Move the cursor to the Probe field, press Select, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field and press Select. Type 80 on the front-panel keyboard, then use the left and right control keys to select mV. Press the Select key.

e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Select the Coupling field, then select 50Ω / DC.

g Move the cursor to the s/Div field, press Select, then use the RPG knob to dial in 200 ns.



2 Set up the Display menu.

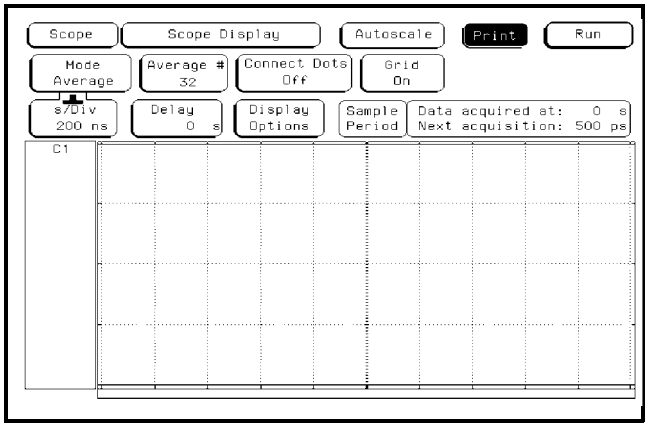
a Press the Display key.

b Select the Mode field, then select Average.

c Move the cursor to the Average # field. Type 32 on the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



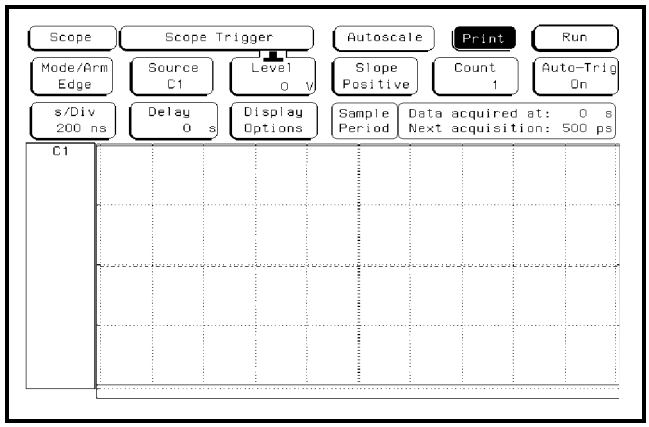
3 Set up the Trigger menu.

a Press the Trigger key.

b Select the Mode/Arm field, then select Edge.

c Select the Source field, then select C1.

d Move the cursor to the Level field. Set the trigger level to 0 by typing 0 in the front-panel keyboard, then pressing Select.

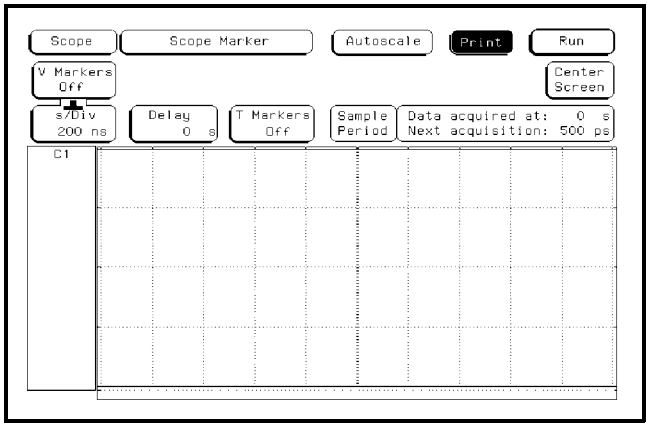


4 Turn off the voltage and time markers.

a Press the Marker key.

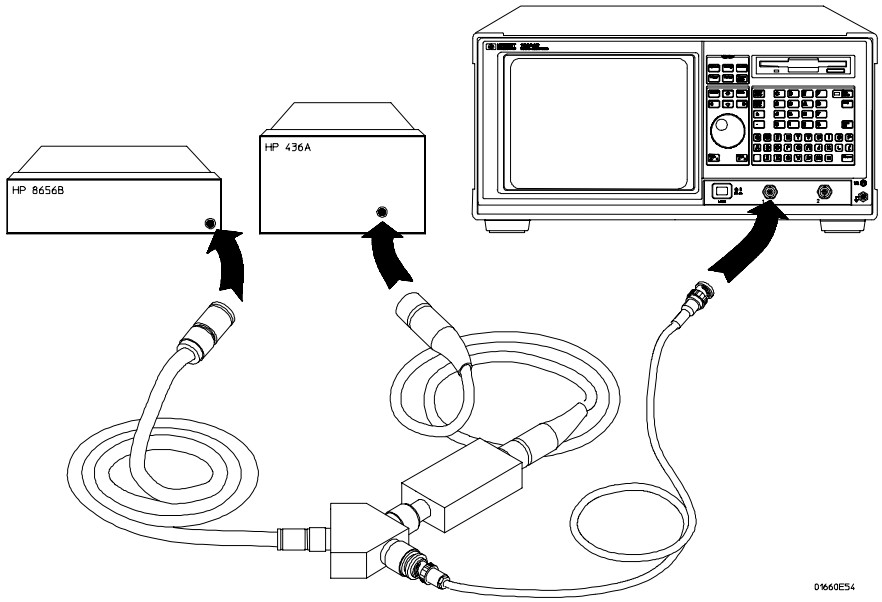
b Move the cursor to the V Markers field and press Select. The Select key should toggle the marker to Off.

c Move the cursor to the T Markers field and press Select. At the pop up menu, select Off.



Connect the logic analyzer

1. Using the N cable, connect the signal generator to the power splitter input. Connect the power sensor to one output of the power splitter.
2. Using the N-to-BNC adapter and the BNC cable, connect the other power splitter output to the channel 1 input of the oscilloscope.



Acquire the data

1. Obtain the 1 MHz response.
   - **a** Set the signal generator for 1 MHz at –2.4 dBm.
   - **b** Press the blue shift key, then press the Run key. The signal on the screen should be two cycles at three divisions amplitude. After approximately 15 seconds (averaging complete), press the Stop key.
   - **c** Press the Meas key. Note the voltage reading in the $V_{p\text{-}p}$ field.
     $V_{1\ MHz}$ = _____ mV.
2. Set the signal generator for 500 MHz frequency.
   - **a** Set the power meter Cal Factor % to the 1 MHz value from the calibration chart on the power splitter. Press dB[REF] to set a 0 dB reference.
   - **b** Change the signal generator frequency to 500 MHz. Set the power meter Cal Factor % to the 500 MHz value from the chart.
   - **c** Adjust the signal generator amplitude for a power reading as close as possible to 0.0 dB[REL] and note the power reading. Reading = _____ dB.
3. Obtain the 500 MHz response.
   - **a** Use the RPG knob to dial in a s/Div value of 1 ns/Div.
   - **b** Press the blue shift key, then press the Run key. After approximately 15 seconds (averaging complete), press the Stop key.
   - **c** Note the voltage reading in the $V_{p\text{-}p}$ field V_{500MHz} = _____mV.
4. Determine the oscilloscope response.
   - **a** Calculate the response using the formula:

     $$response\ (dB) = 20\log_{10}\frac{V_{500Mhz}}{V_{1MHz}} = 20\log_{10}(_____) = _____dB$$

   - **b** Correct the result from step 4a above with any differences in the power meter from step 2c. Observe signs. For example:

     Result from step 4a = –2.3 dB
     Power meter reading = –0.2 dB[REL]
     then true response = (–2.3) – (–0.2) = –2.1dB

     (_____) – (_____) = _____ dB
   - **c** The result from step 4b should be ≤ –3.0 dB. Record the result in the performance test record.
5. Remove the power splitter from the oscilloscope channel 1 input and connect it to the channel 2 input.
6. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where applicable.

See Also

Failure of the bandwidth test can be caused by a faulty attenuator or main assembly (see chapter 6).

To test the time measurement accuracy (oscilloscope)

Testing the time measurement accuracy verifies the performance of the following specification:

- Time Measurement accuracy

This test uses a precise frequency source to check the accuracy of time measurement functions.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Signal Generator	200 MHz, timebase accuracy 0.25 ppm	8656B Opt. 001
Cable	BNC (m)(m) 48-inch	8120-1840
Adapter	Type N (m) to BNC (f)	1250-0780

Set up the equipment

1 Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.
2 Set the signal generator to 181.81818 MHz (5.5 ns period) and approximately 600 mV rms.

Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

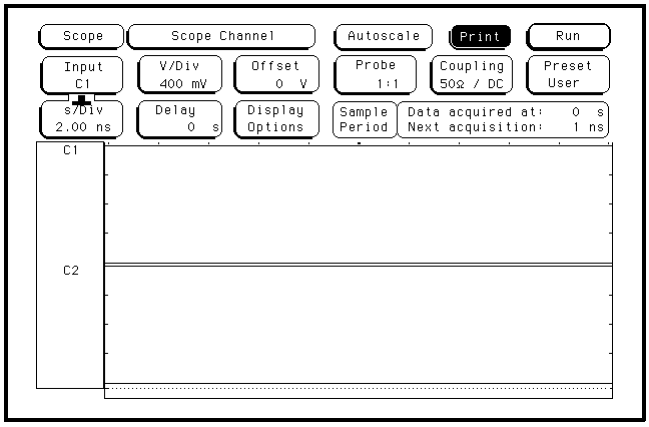
c Move the cursor to the Probe field, press Select, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field, press Select, then use the PRG knob to dial in 400 mV.

e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Select the Coupling field, then select 50Ω / DC.

g Move the cursor to the s/Div field, press Select, then use the RPG knob to dial in 2.00 ns.



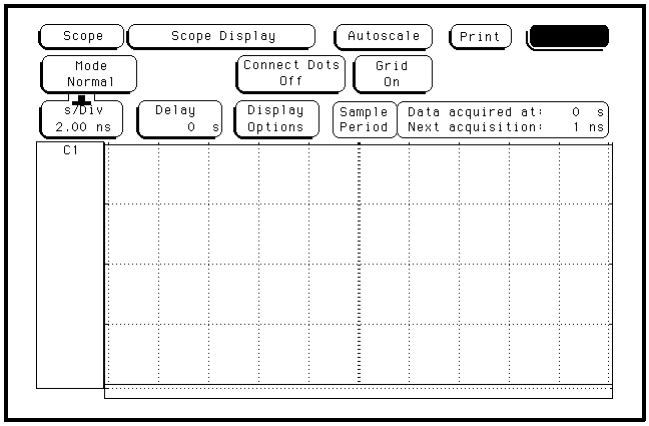
2 Set up the Display menu.

a Press the Display key.

b Select the Mode field, then select Normal.

c Select the Grid field and set it to On.

d In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



3 Set up the Trigger menu.

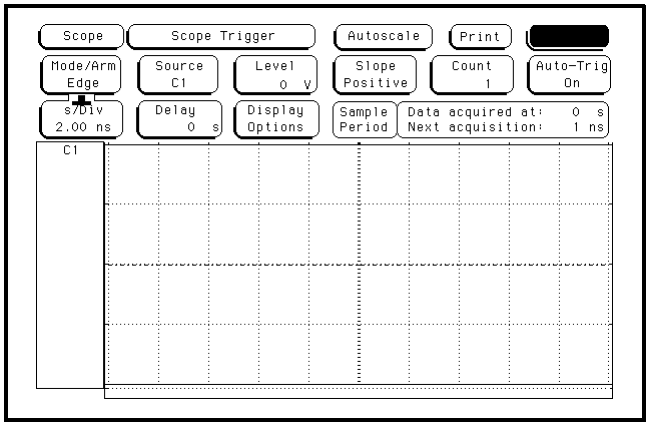
a Press the Trigger key.

b Select the Mode/Arm field, then select Edge.

c Select the Source field and set it to C1.

d Move the cursor to the Level field. Set the trigger level to 0 by typing 0 in the front-panel keyboard, then pressing Select.

e Select the Slope field and set it to Positive.



4 Set up the Markers menu.

a Press the Marker key.

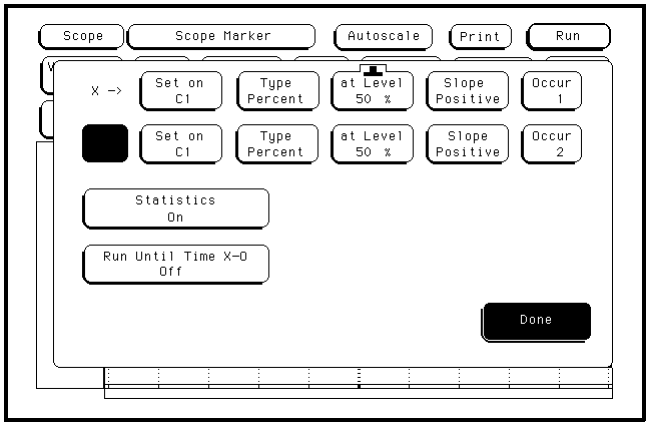
b Move the cursor to the T Markers field and press Select. At the pop up menu, select Auto.

c Select the X marker, and set it on C1 at Level 50%, Slope Positive, Occur 1 (use the RPG knob for Occur).

d Select the O marker, and set it on C1 at Level 50%, Slope Positive, Occur 2 (use the RPG knob for Occur).

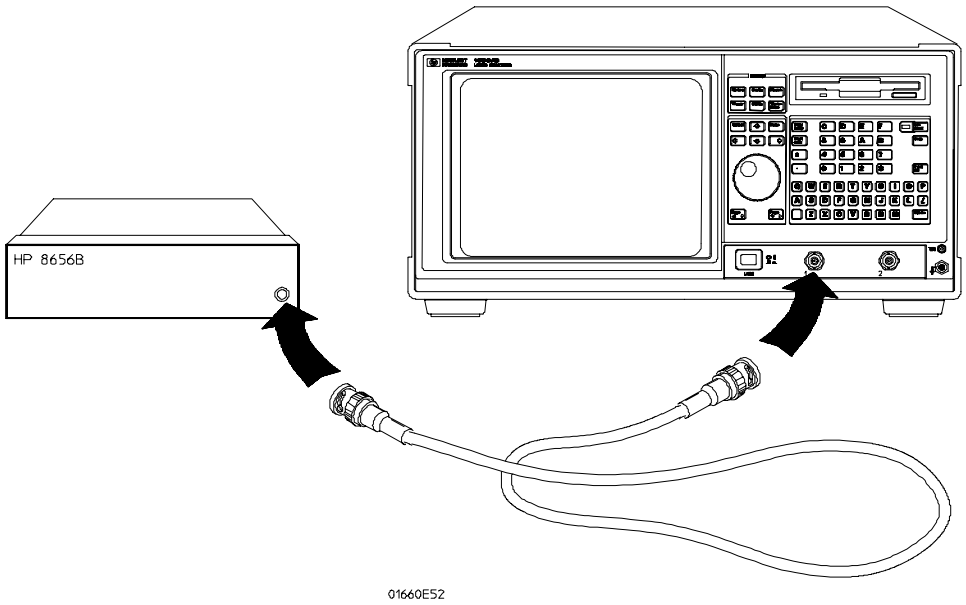
e Select the Statistics field and set it to On.

f Select Done.



Connect the logic analyzer

Using the N-to-BNC adapter and the BNC cable, connect the signal generator output to the channel 1 input of the oscilloscope.



Acquire the data

1 Determine short time period accuracy.

- **a** Press the blue shift key, then press Run. If the waveform is clipping, reduce the signal generator output voltage level until the waveform no longer clips. After approximately two minutes, press the Stop key.
- **b** In the Statistics field, check to see that the Mean X - O field is approximately 5.500 ns. Check that both the Min X - O and the Max X - O are within 150 ps of the Mean X - O. Record the results in the performance test record.

2 Determine longer time period accuracy.

- **a** Press Select twice to call up the T Markers Auto menu.
- **b** Select the X marker Set On field. At the pop up menu, select Manual.
- **c** Move the cursor to the O marker Occur field. Press the 1 key, then press Select.
- **d** Press Done.
- **e** Press the Display key. Select the Mode field, then select Average. Move the cursor to the Average # field. Type 8 on the front-panel keyboard, then press Done.
- **f** Move the cursor to the Delay field. Type 99 on the front-panel keyboard, and use the left and right cursor-control keys to select "ns." Press done.
- **g** Press the Marker key. Press the blue shift key, then press the Run key. After approximately two minutes, press the Stop key.
- **h** In the Statistics field, check to see that the Mean X - O field is approximately 99 ns. Check that both the Min X - O and the Max X - O are within 155 ps of the Mean X - O. Record the results in the performance test record.

To test the trigger sensitivity (oscilloscope)

Testing the trigger sensitivity verifies the performance of the following specifications:

- DC to 50 MHz: 0.063 x full scale (0.25 division)
- 50 MHz to 500 MHz: 0.125 x full scale (0.5 division)

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Signal Generator	50 MHz and 225 MHz, 30 - 80 mV RMS output	8656B Opt. 001
Cable	BNC 48-inch	8120-1840
Adapter	Type N (m) to BNC (f)	1250-0780

Set up the equipment

Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

Set up the logic analyzer

1 Set up the Configuration menu.

a Press the Config key. At the pop up menu, select Scope Channel.

b Select the Input field, then select C1.

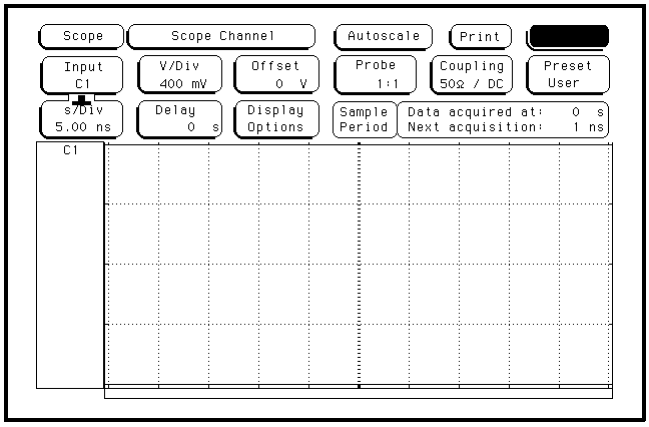
c Move the cursor to the Probe field, press Select, then use the RPG knob to dial in 1:1.

d Move the cursor to the V/Div field, press Select, then use the PRG knob to dial in 400 mV.

e Move the cursor to the Offset field. Set the offset to 0 by typing 0, then pressing the Select key.

f Move the cursor to the Coupling field, then press Select. Select 50Ω / DC.

g Move the cursor to the s/Div field, press Select, then use the RPG knob to dial in 5.00 ns.



2 Set up the Display menu.

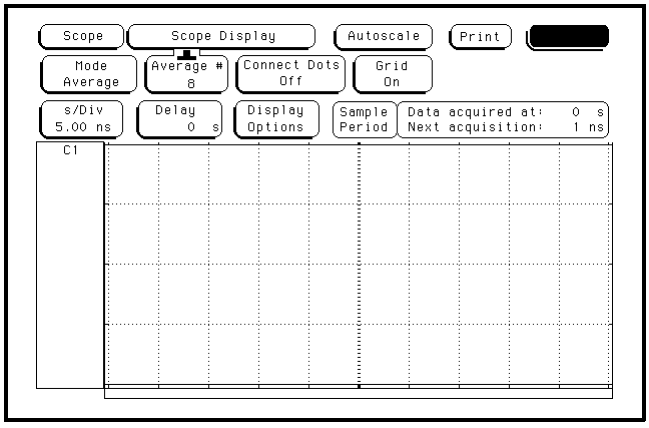
a Press the Display key.

b Select the Mode field, then select Average.

c Move the cursor to the Average # field. Enter "8" in the front-panel keyboard, then press Done.

d Select the Grid field and set it to On.

e In the Waveform selection menu, delete channel 2. If channel 1 is not inserted, insert channel 1.



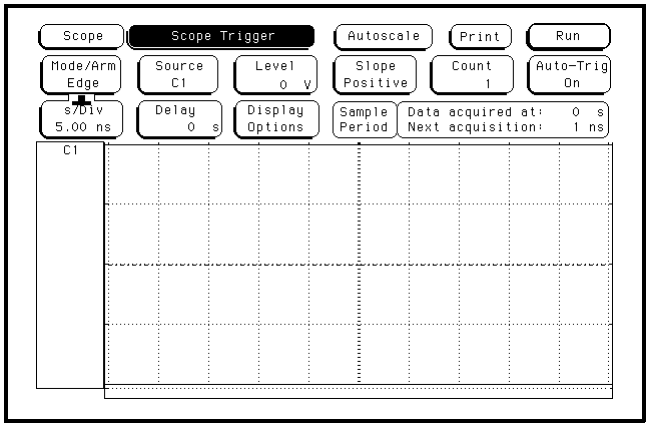
3 Set up the Trigger menu.

a Press the Trigger key.

b Select the Mode/Arm field, then select Edge.

c Select the Source field and set it to C1.

d Move the cursor to the Level field. Set the trigger level to 0 by typing 0 in the front-panel keyboard, then pressing Select.

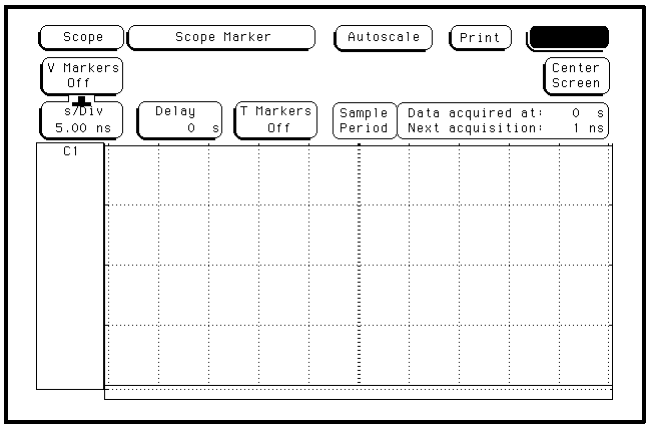


4 Turn off the voltage and time markers.

a Press the Marker key.

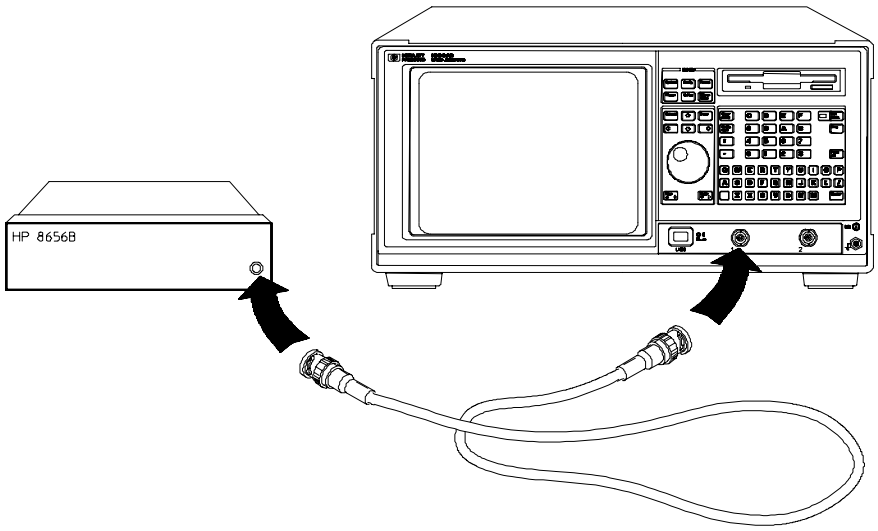
b Move the cursor to the V Markers field and press Select. The Select key should toggle the marker to Off.

c Move the cursor to the T Markers field and press Select. At the pop up menu, select Off.



Connect the logic analyzer

Using the N-to-BNC adapter and the BNC cable, connect the signal generator output to the channel 1 input of the oscilloscope.



Acquire the data

1. Test the upper bandwidth trigger sensitivity.
   - **a** Set the signal generator to provide a 225 MHz signal with 70 mV rms amplitude.
   - **b** Press the blue shift key, then press the Run key. Press the Trigger key.
   - **c** If the Auto triggered message appears (oscilloscope doesn't trigger), move the cursor to the Level field and use the RPG knob to adjust the trigger level until the oscilloscope triggers (Auto triggered message goes away).
   - **d** If the oscilloscope triggers, record a pass in the performance test record.
   - **e** Press Stop to halt the acquisition. Read the Vp-p field and record the voltage in the performance test record.
2. Test the lower bandwidth trigger sensitivity.
   - **a** Use the RPG knob to dial in s/Div of 20 ns.
   - **b** Set the signal generator to provide a 50 MHz signal with 35 mV rms amplitude.
   - **c** Press the blue shift key, then press the Run key.
   - **d** If the oscilloscope doesn't trigger, move the cursor to the Level field and use the RPG knob to adjust the trigger level until the oscilloscope triggers (Auto triggered message goes away).
   - **e** If the oscilloscope triggers, record a pass in the performance test record.
   - **f** Press Stop to halt the acquisition.
3. Remove the signal generator output from channel 1 and connect the BNC cable to channel 2. Repeat from "Set up the logic analyzer" for channel 2, replacing channel 1 with channel 2 where appropriate.

Performance Test Record (logic analyzer)

Agilent 1670G Series Logic Analyzer_____

Serial No._____ Work Order No._____

Recommended Test Interval - 2 Years/4000 hours Date_____

Recommended next testing_____ Temperature_____

Test	Settings	Results
Self-Tests		Pass/Fail _____
Threshold Accuracy	± (100 mV + 3% of threshold setting)	
Pod 1	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 2	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 3	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 4	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 5	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 6	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 7	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____
Pod 8	ECL, ±139 mV 0 V, ±100 mV	Pass/Fail _____ Pass/Fail _____

Performance Test Record (continued)

Test	Settings		Results			
Single-Clock, Single-Edge Acquisition				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	3.0/0.0 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
	Setup/Hold Time	-0.5/3.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	3.0/0.0 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
	Setup/Hold Time	-0.5/3.5 ns	J↑ K↑ L↑ M↑	_____ _____ _____ _____	J↓ K↓ L↓ M↓	_____ _____ _____ _____
Multiple-Clock, Multiple-Edge Acquisition				Pass/Fail		Pass/Fail
All Pods, Channel 3	Setup/Hold Time	4.0/0.0 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
	Setup/Hold Time	-0.5/4.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
All Pods, Channel 11	Setup/Hold Time	4.0/0.0 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____
	Setup/Hold Time	-0.5/4.5 ns	J↑ + K↑ + L↑ + M↑	_____	J↓ + K↓ + L↓ + M↓	_____

Performance Test Record (continued)

Test	Settings		Results	
Single-Clock, Multiple-Edge Acquisition			Disable pulse generator, channel 1 COMP (LED off)	
				Pass/Fail
All Pods, Channel 3	Setup/Hold Time	3.5/0.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
	Setup/Hold Time	-0.5/4.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
All Pods, Channel 11	Setup/Hold Time	3.5/0.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
	Setup/Hold Time	-0.5/4.0 ns	J↕ K↕ L↕ M↕	_____ _____ _____ _____
Time Interval Accuracy		Expected	Limits	Measured
		409.60 µs	409.56 µs to 409.64 µs	_____

Performance Test Record (oscilloscope)

Performance Test Record (oscilloscope)

Test	Settings	Results
Self-Tests		Pass/Fail _____
Input Resistance	50 Ω± 0.5 Ω (49.5 to 50.5 Ω) 1MΩ± 10 KΩ (0.990 to 1.010 MΩ)	
Channel 1		
		50 Ω @ 20 mV/Div _____
		1 MΩ @ 20 mV/Div _____
		50 Ω @ 200 mV/Div _____
		1 MΩ @ 200 mV/Div _____
		50 Ω @ 1 V/Div _____
		1 MΩ @ 1 V/Div _____
		50 Ω @ 4 V/Div _____
		1 MΩ @ 4 V/Div _____
Channel 2		
		50 Ω @ 20 mV/Div _____
		1 MΩ @ 20 mV/Div _____
		50 Ω @ 200 mV/Div _____
		1 MΩ @ 200 mV/Div _____
		50 Ω @ 1 V/Div _____
		1 MΩ @ 1 V/Div _____
		50 Ω @ 4 V/Div _____
		1 MΩ @ 4 V/Div _____

Performance Test Record (oscilloscope)

Test	Settings	Results	
Voltage Measurement Accuracy		Limits	Measured
Channel 1	Zero Input	-13.7 V to -14.3 V	_____
		-3.43 V to -3.57 V	_____
		-1.37 V to -1.43 V	_____
		-137.0 mV to -143.0 mV	_____
		143.0 mV to 137.0 mV	_____
		1.43 V to 1.37 V	_____
		3.57 V to 3.43 V	_____
		14.3 V to 13.7 V	_____
Channel 2	Zero Input	-13.7 V to -14.3 V	_____
		-3.43 V to -3.57 V	_____
		-1.37 V to -1.43 V	_____
		-137.0 mV to -143.0 mV	_____
		143.0 mV to 137.0 mV	_____
		1.43 V to 1.37 V	_____
		3.57 V to 3.43 V	_____
		14.3 V to 13.7 V	_____
Offset Accuracy	**Zero-input offset**		
Channel 1	4 V/Div	0.00 V±320.0 mV	_____
	1 V/Div	0.00 V±80.0 mV	_____
	100 mV/Div	0.00 V±8.0 mV	_____
	10 mV/Div	0.00 V±800.0 µV	_____
Channel 2	4 V/Div	0.00 V±320.0 mV	_____
	1 V/Div	0.00 V±80.0 mV	_____
	100 mV/Div	0.00 V±8.0 mV	_____
	10 mV/Div	0.00 V±800.0 µV	_____
	DC-input offset		
Channel 1	-35.00 V	-35.4 V to -34.6 V	_____
	-10.00 V	-10.1 V to -9.90 V	_____
	-2.00 V	-2.02 V to -1.98 V	_____
	+2.00 V	+1.98 V to +2.02 V	_____
	+10.00 V	+9.90 V to +10.1 V	_____
	+35.00 V	+34.6 V to +35.4 V	_____
Channel 2	-35.00 V	-35.4 V to -34.6 V	_____
	-10.00 V	-10.1 V to -9.90 V	_____
	-2.00 V	-2.02 V to -1.98 V	_____
	+2.00 V	+1.98 V to +2.02 V	_____
	+10.00 V	+9.90 V to +10.1 V	_____
	+35.00 V	+34.6 V to +35.4 V	_____

Performance Test Record (oscilloscope)

Test	Settings	Results
Bandwidth		Limit Measured
Channel 1		≤–3.0 dB _____
Channel 2		≤–3.0 dB _____
Time Measurement Accuracy	5.500 ns ± 150 ps	MEAN X-0 _____ MIN X-0 _____ MEAN X-0 - MIN X-0 _____ MAX X-0 _____ MAX X-0 - MEAN X-0 _____
	99.000 ns ± 155 ps	MEAN X-0 _____ MIN X-0 _____ MEAN X-0 - MIN X-0 _____ MAX X-0 _____ MAX X-0 - MEAN X-0 _____
Trigger Sensitivity		
Channel 1	Trigger Stable dc to 50 MHz Trigger Stable 50 MHz to 500 MHz	Pass/Fail _____ Pass/Fail _____
Channel 2	Trigger Stable dc to 50 MHz Trigger Stable 50 MHz to 500 MHz	Pass/Fail _____ Pass/Fail _____

Performance Test Record (pattern generator)

Performance Test Record (pattern generator)

Test	Settings	Results
Self-Tests		Pass/Fail _____

4

Logic analyzer calibration 4-2
To calibrate the oscilloscope 4–3
Set up the equipment 4–3
Load the Default Calibration Factors 4–4
Self Cal menu calibrations 4–5

Calibrating and Adjusting

Calibrating and Adjusting

This chapter gives you instructions for calibrating and adjusting the logic analyzer.

To periodically verify the performance of the analyzer, refer to "Testing Performance," chapter 3.

Logic analyzer calibration

The logic analyzer circuitry of the Agilent 1670G-series Logic Analyzers does not require an operational accuracy calibration. To test the logic analyzer circuitry against specifications (full calibration), refer to chapter 3, "Testing Performance."

The oscilloscope circuitry in the Agilent 1670G-series Logic Analyzers with the oscilloscope option requires an operational accuracy calibration by the user or service department under any of the following conditions:

- at six months intervals or every 1,000 hours
- if the ambient temperature changes more than 10° C from the temperature at full calibration
- to optimize measurement accuracy

To test the oscilloscope circuitry against specifications (full calibration), refer to chapter 3, Testing Performance.

The pattern generator circuitry in the Agilent 1670G-series Logic Analyzers with the pattern generator option does not require an operational accuracy calibration.

To calibrate the oscilloscope

Equipment Required

Equipment	Critical Specification	Recommended Model/Part	Qty
Cable (2)	BNC, 9-inch (equal length)	10502A	1
Cable	BNC	10503A	
Adapter	BNC tee (m)(f)(f)	1250-0781	1
Adapter	BNC (f)(f) (ug-914/u)	1250-0080	

Set up the equipment

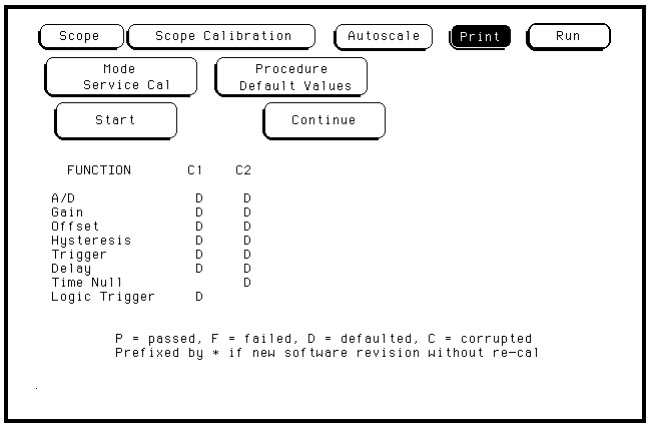
Turn on the logic analyzer. Let it warm up for 30 minutes if you have not already done so.

Load the Default Calibration Factors

Note that once the default calibration factors are loaded, all calibrations must be done. This includes all of the calibrations in the Self Cal menu. The calibration must be performed in the exact sequence listed below.

NOTE The calibration PROTECT/UNPROTECT switch on the back panel of the Agilent 1670G series logic analyzer with the oscilloscope must be set to UNPROTECT.

1. Press the System key. Select System, then select Scope.
2. Select the menu field (top row, second from the left), then select Scope Calibration from the pop-up menu.
3. Select the Mode field, then select Service Cal from the pop-up menu.
4. Select the Procedure field, then select Default Values from the pop-up menu.



5. Select the Start field and follow the instructions on the display.

After you select the Start field, you can abort the calibration procedure by selecting either the Mode or Procedure fields if the Continue field is still displayed on the screen.

Self Cal menu calibrations

Messages will be displayed as each calibration routine is completed to indicate calibration has passed or failed. The resulting calibration factors are automatically stored to nonvolatile RAM at the conclusion of each calibration routine.

The Self Cal menu lets you optimize vertical sensitivity (Vert Cal) for channels 1 and 2 individually or both channels on a board simultaneously. Also, the Self Cal menu lets you optimize delay (Delay) for channel 1 and 2 separately, then Time Null for channel 2 and the Logic Trigger.

1 Optimize Vert Cal of the Self Cal.

- **a** Connect two BNC 50-Ω, 9-inch cables to the BNC tee adapter. Connect the BNC 50Ω (f)(f) adapter to the BNC tee adapter, and connect the 48-inch BNC cable to the BNC 50Ω (f)(f) adapter. Once you select Start, the instrument will prompt you to connect the cables to the appropriate locations on the rear panel of the instrument.
- **b** Select the Mode field, then select Self Cal from the pop-up menu.
- **c** Select the Procedure field, then select Vert Cal from the pop-up menu.
- **d** Select the Channel field, then select a channel choice from the pop-up menu.
- **e** Select the Start field and follow the instructions on the display.
- **f** After completion of Vertical Calibration, remove the cables from the instrument.

2 Optimize Delay of the Self Cal.

- **a** Obtain a BNC 50-Ω, 48-inch cable. Once you select Start, the instrument will prompt you to connect the cable to the appropriate location on the rear panel of the instrument.
- **b** Select the Procedure field, then select Delay from the pop-up menu.
- **c** Select the Channel field, then select C1.
- **d** Select the Start field and follow the instructions on the display.
- **e** Repeat steps c and d for channel 2.
- **f** After completing all of the channel delay calibrations, remove the cable from the oscilloscope.

3 Optimize the Time Null of the Self Cal.

- **a** Connect two BNC 50-Ω, 9-inch cables to the BNC tee adapter. Connect the BNC 50Ω (f)(f) adapter to the BNC tee adapter, and connect the 48-inch BNC cable to the BNC 50Ω (f)(f) adapter. Once you select Start, the instrument will prompt you to connect the cables to the appropriate locations on the rear panel of the instrument.
- **b** Select the Procedure field, then select Time Null from the pop-up menu.
- **c** Select the Start field and follow the instructions on the display.
- **d** After completion of the Time Null calibration, remove the cables from the instrument.

4 Calibrate the Logic Trigger of the Self Cal.

- **a** Obtain a BNC 50-Ω, 48-inch cable.
- **b** Select Start. The instrument will prompt you to connect the cable to the appropriate location on the rear panel of the instrument.
- **c** Select the Procedure field, then select Logic Trigger from the pop-up menu.
- **d** Select the Start field and follow the instructions on the display.
- **e** After completion of the Logic Trigger calibration, remove the cable from the instrument.

To test the CAL OUTPUT ports

This test does not need to be performed every time an operational accuracy calibration is done. Testing the oscilloscope CAL OUTPUT ports checks the following:

- DC CAL OUTPUT voltage
- AC CAL OUTPUT voltage

This test verifies that the CAL OUTPUT voltages are operating within limits, so that they can provide accurate calibration for the oscilloscope operational accuracy calibration and probe calibration.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	3458A
Cable	BNC (m)(m) 48-inch	8120-1840
Adapter	BNC (f) to Dual Banana Plug	1251-2277

Set up the equipment

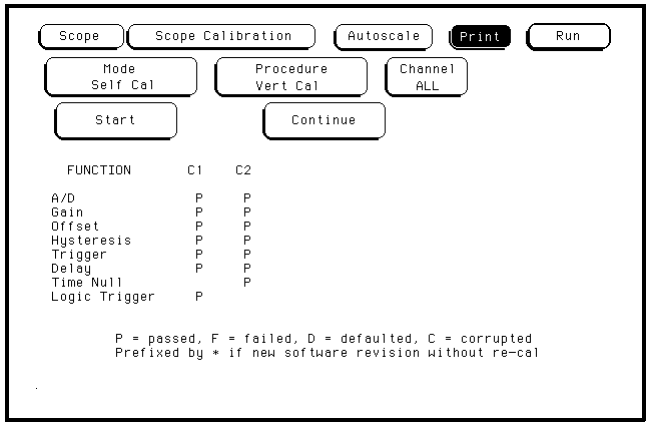
Turn on the equipment required and the logic analyzer. Let them warm up for 30 minutes if you have not already done so.

Set up the logic analyzer

1 Set up the Calibration menu.

a Press the Waveform key.

b Press the Waveform key again. At the pop up, select Scope Calibration.

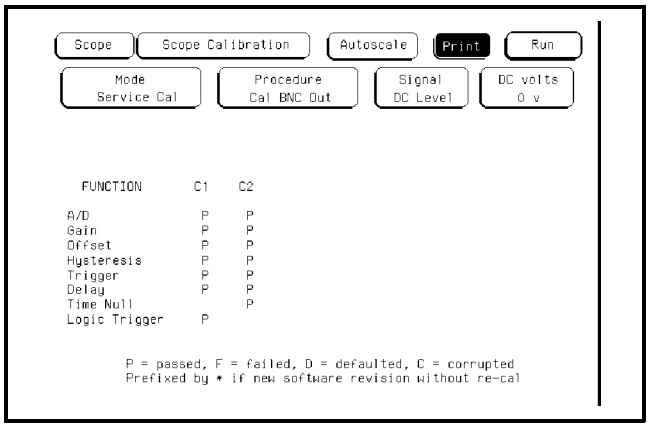


c Select the Mode field, then select Service Cal.

d Select the Procedure field, then select Cal BNC Out.

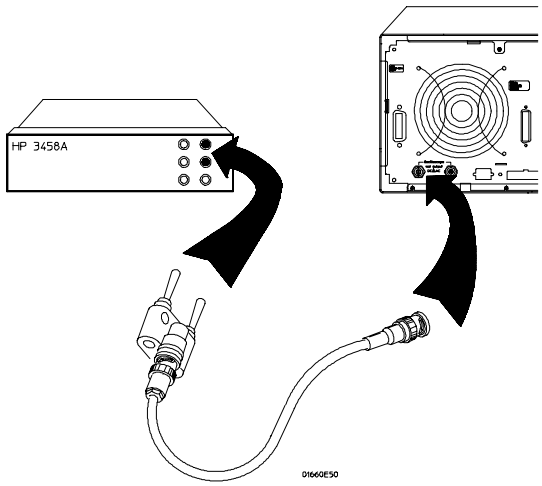
e Select Signal Probe Comp, then select DC Level.

f Select the DC volts field, and set it to 0 V.



Verify the DC CAL OUTPUT port

1 Using the BNC-to-banana adapter, connect the BNC cable between the multimeter and the oscilloscope DC CAL OUTPUT connector.



2 The digital voltmeter should read close to 0.0000 V. Record the reading to four decimal places. V_1 = _____.

3 In the Calibration menu set the DC Volts to 5 V.

4 The digital voltmeter should read close to 5.0000 V. Record the reading to four decimal places. V_2 = _____.

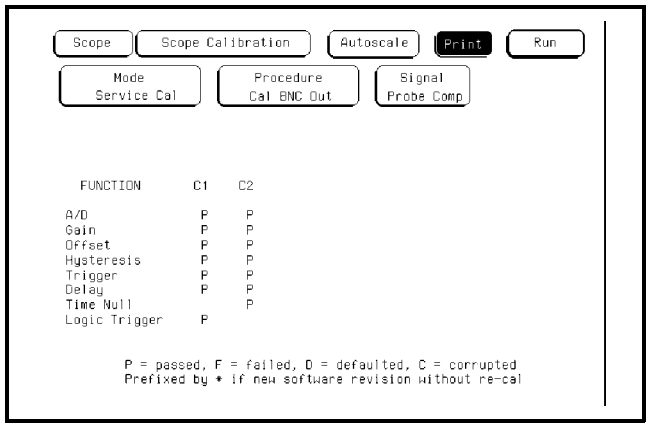
5 In the Calibration menu set the DC Volts to 0 V.

6 Subtract V_1 from V_2. The difference should be between 4.990 and 5.010 V. Record the reading in the performance test record.

Set up the logic analyzer

1 Set up the Calibration menu.

a Select the Signal field, then select Probe Comp.

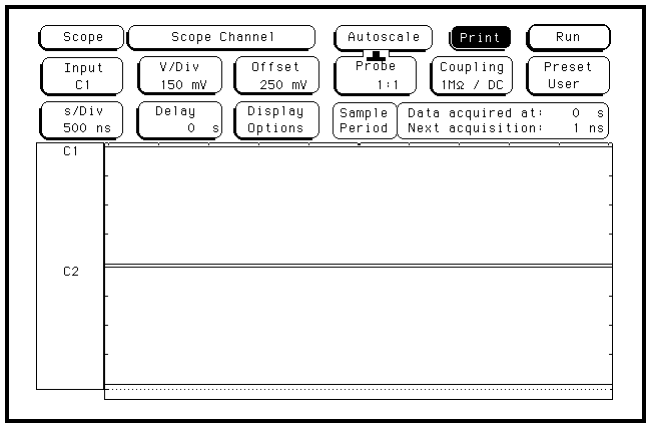


2 Set up the Channel menu.

a Press the Chan key.

b Select the Coupling field, then select 1MΩ / DC.

c Move the cursor to the Probe field, press Select, then use the RPG knob to dial in 1:1.



Verify the AC CAL OUTPUT port

1 Using the BNC cable, connect channel 1 of the oscilloscope to the AC CAL OUTPUT connector.

2 In the Calibration menu select Autoscale.

3 Press the Meas key. Verify that the waveform is approximately 0.8 Vp_p at approximately 1.0000 KHz. Record the reading in the performance test record.

5

To use the flowcharts 5–2
To check the power-up tests 5–17
To run the self-tests 5–18
To test the power supply voltages 5–26
To test the LCD display signals 5–27
To test the keyboard signals 5–28
To test the flexible disk drive voltages 5–30
To test the hard disk drive voltages 5–32
To perform the BNC test 5–34
To test the logic analyzer probe cables 5–35
To verify pattern output (pattern generator) 5–39
The ether address 5–41
To test the auxiliary power 5–42

Troubleshooting

Troubleshooting

This chapter helps you troubleshoot the logic analyzer to find defective assemblies. The troubleshooting consists of flowcharts, self-test instructions, and tests. This information is not intended for component-level repair.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform other tests.

The service strategy for this instrument is the replacement of defective assemblies. This instrument can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

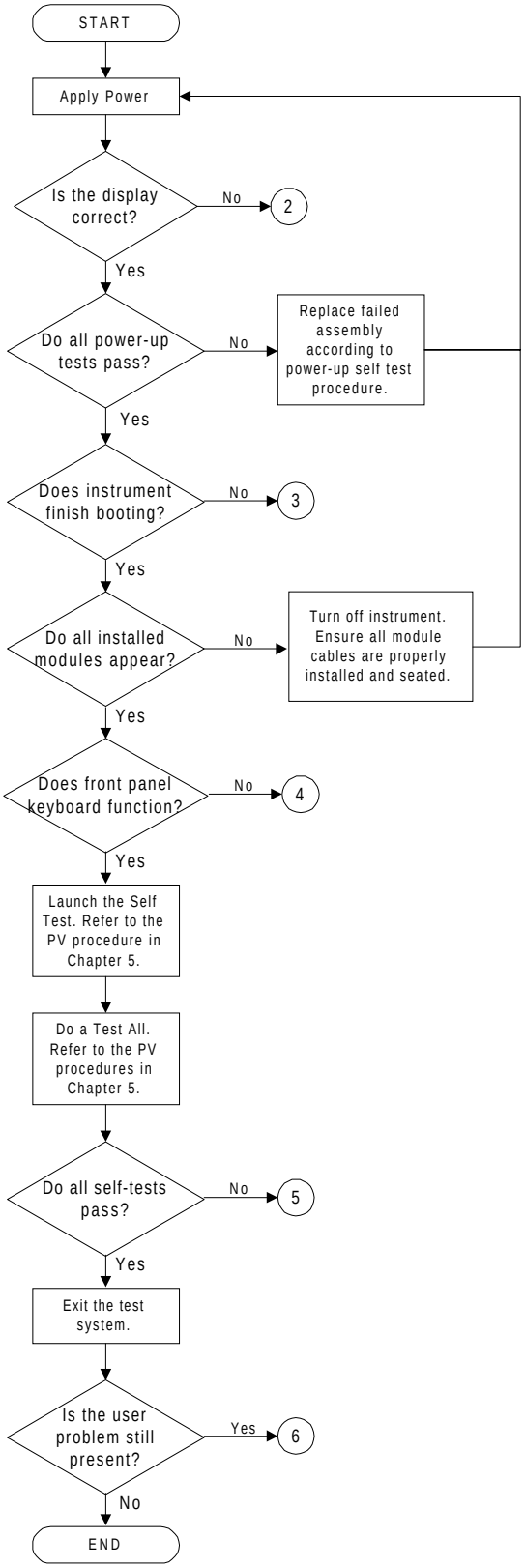
CAUTION

Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when you perform any service to this instrument or to the cards in it.

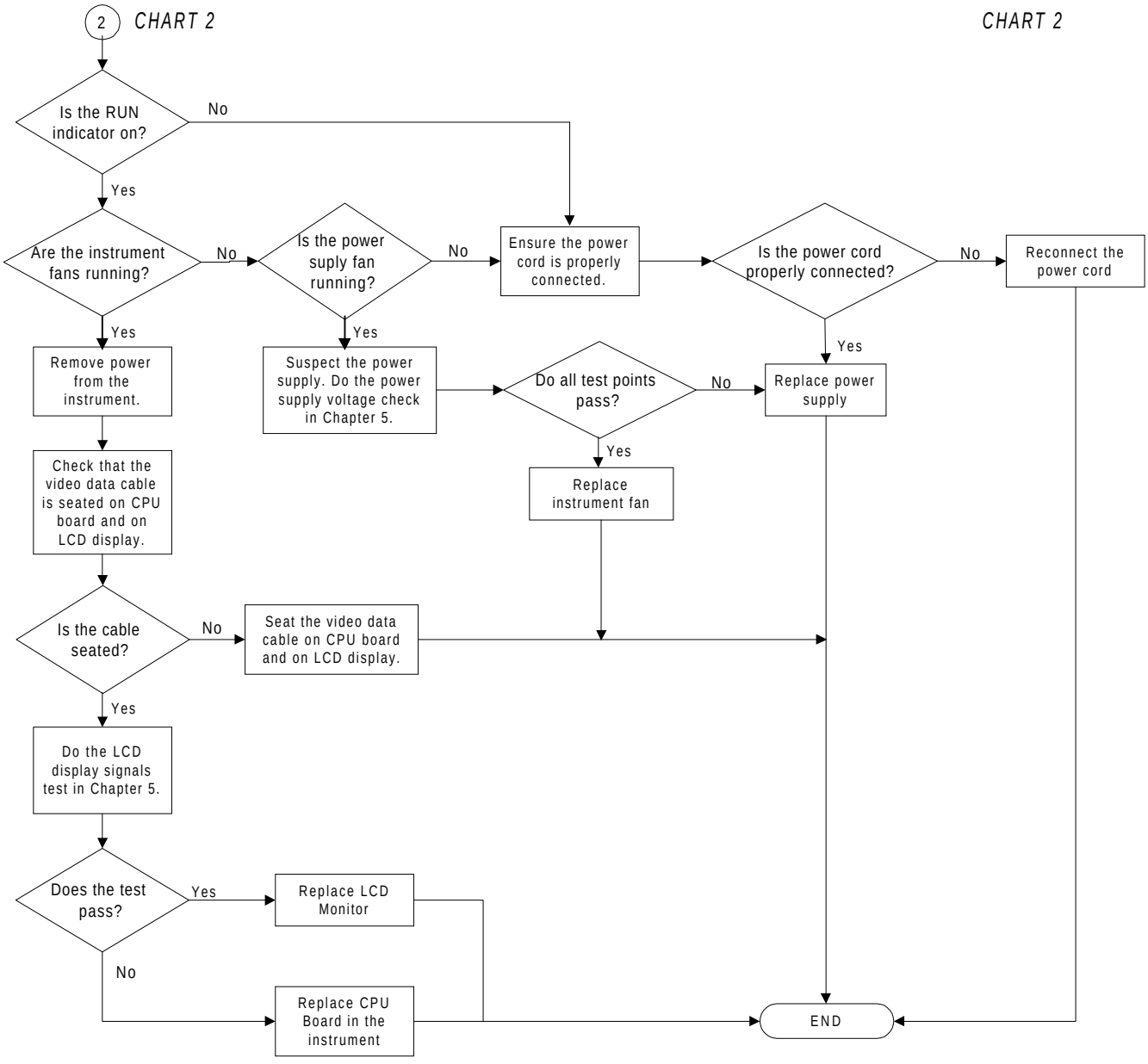
To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled letters on the charts indicate connections with the other flowcharts. Start your troubleshooting at the top of the first flowchart.

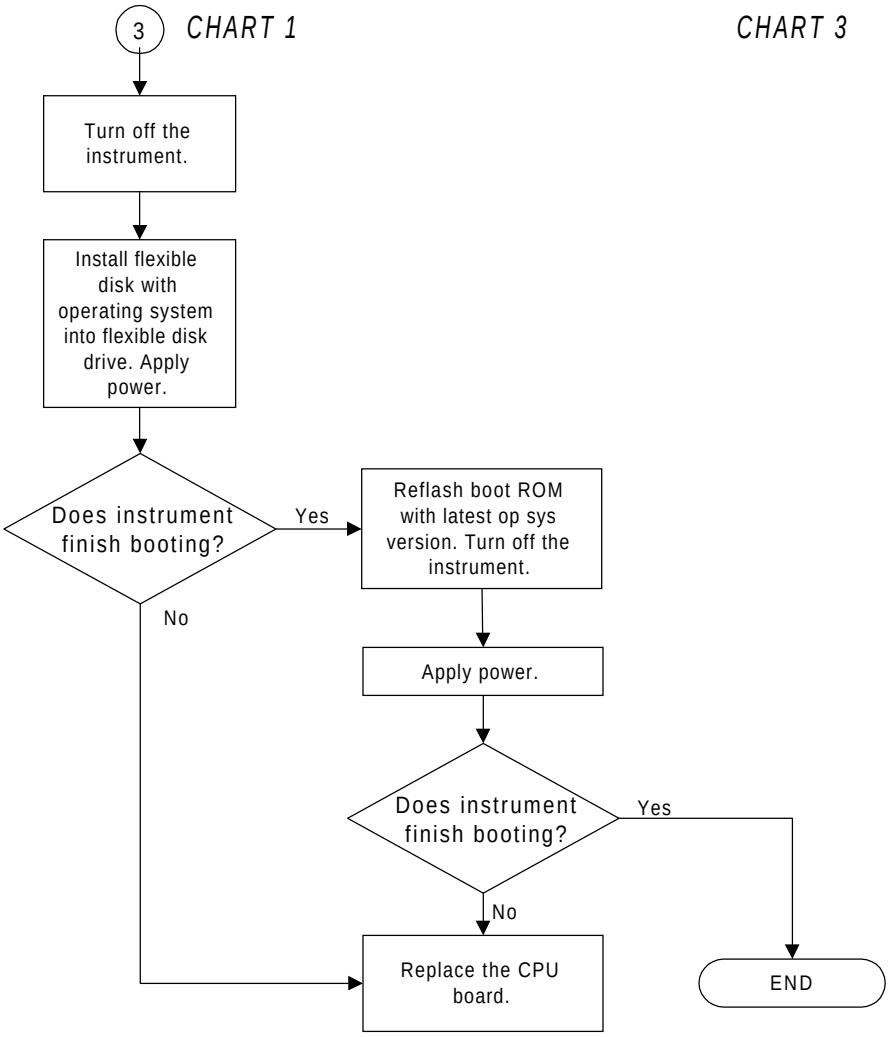
Troubleshooting Flowchart 1



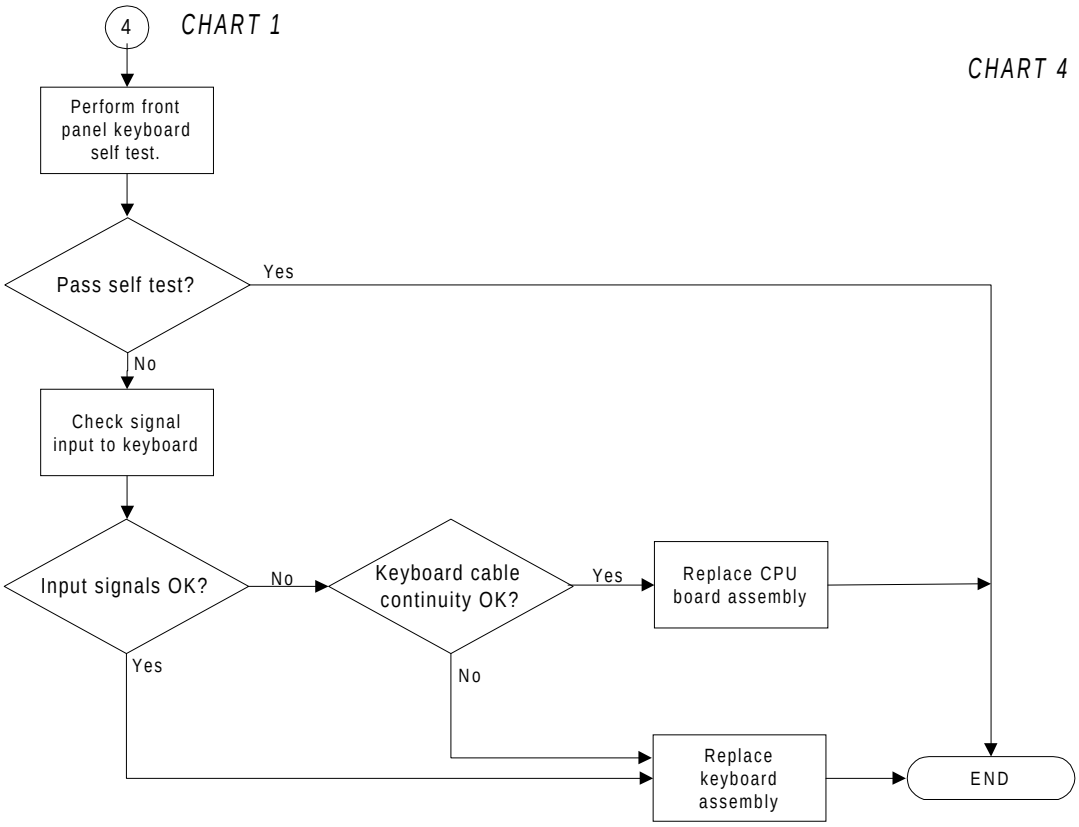
Troubleshooting Flowchart 2



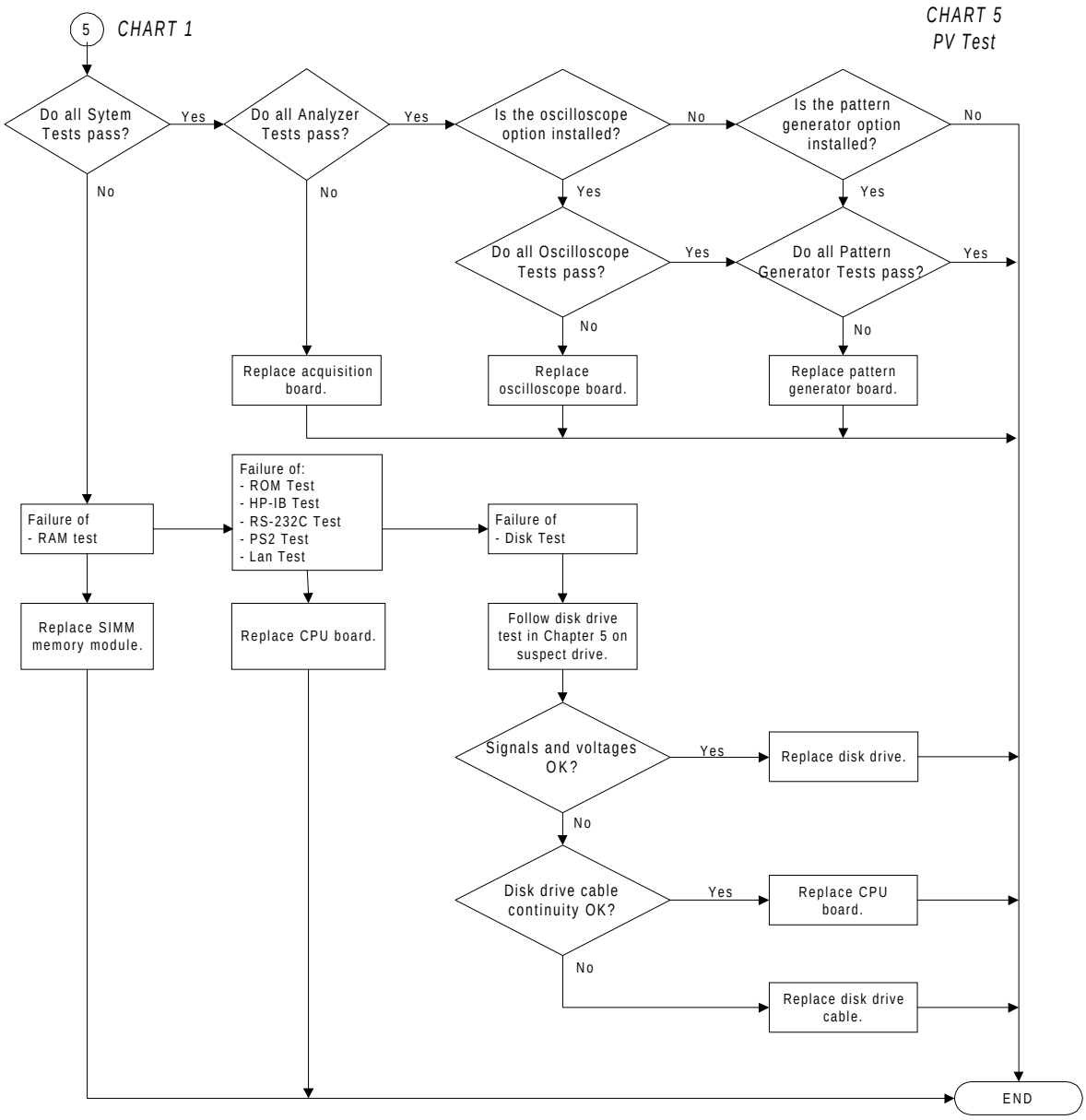
Troubleshooting Flowchart 3



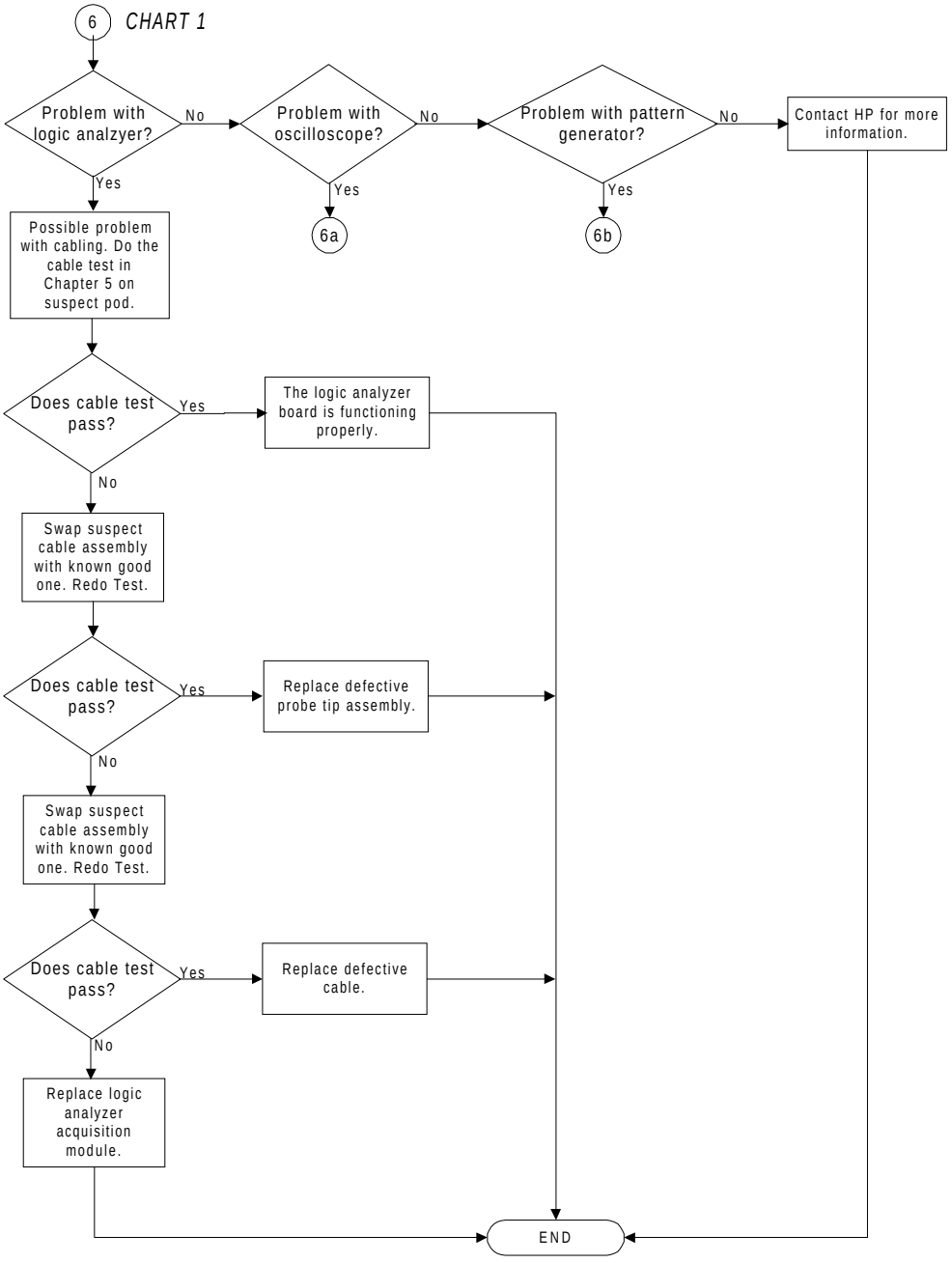
Troubleshooting Flowchart 4



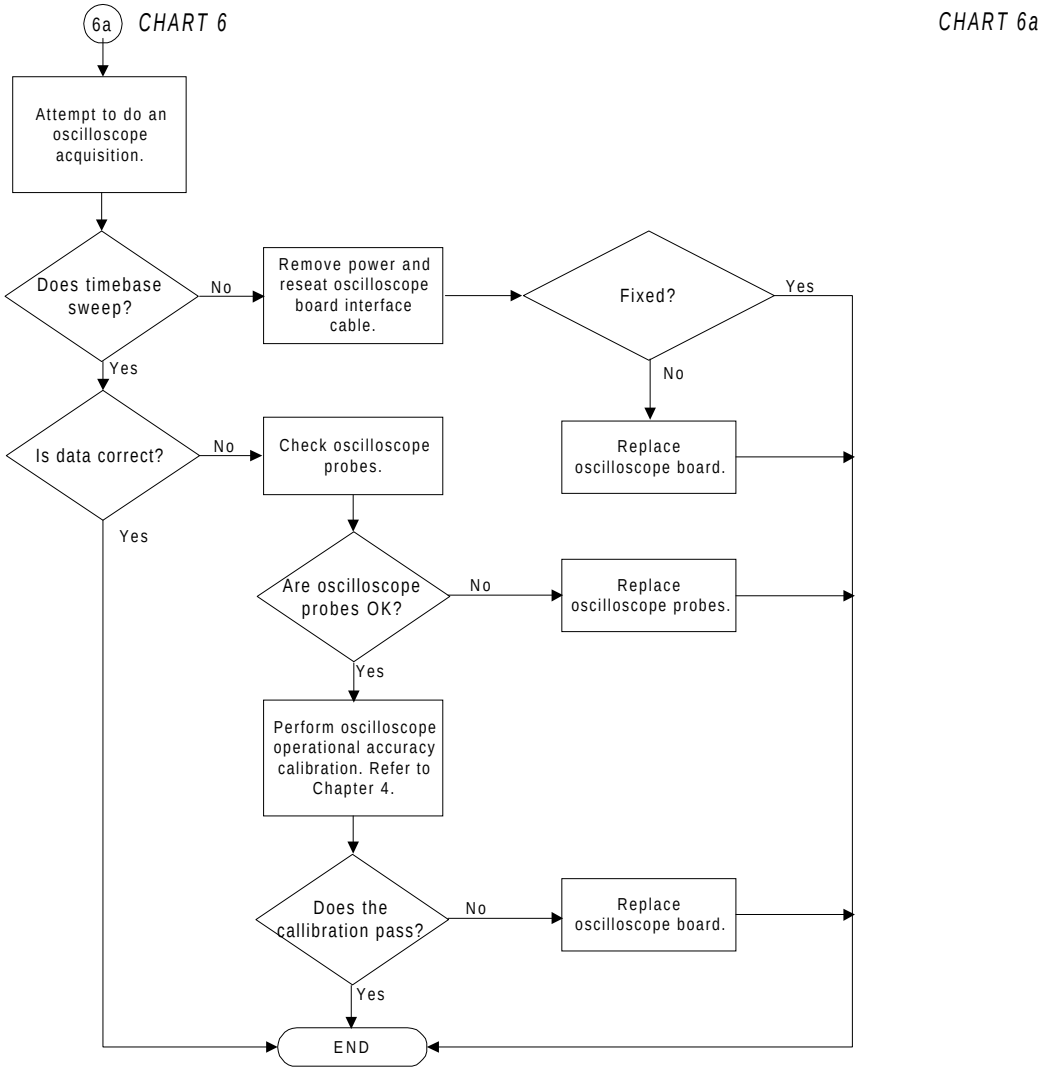
Troubleshooting Flowchart 5



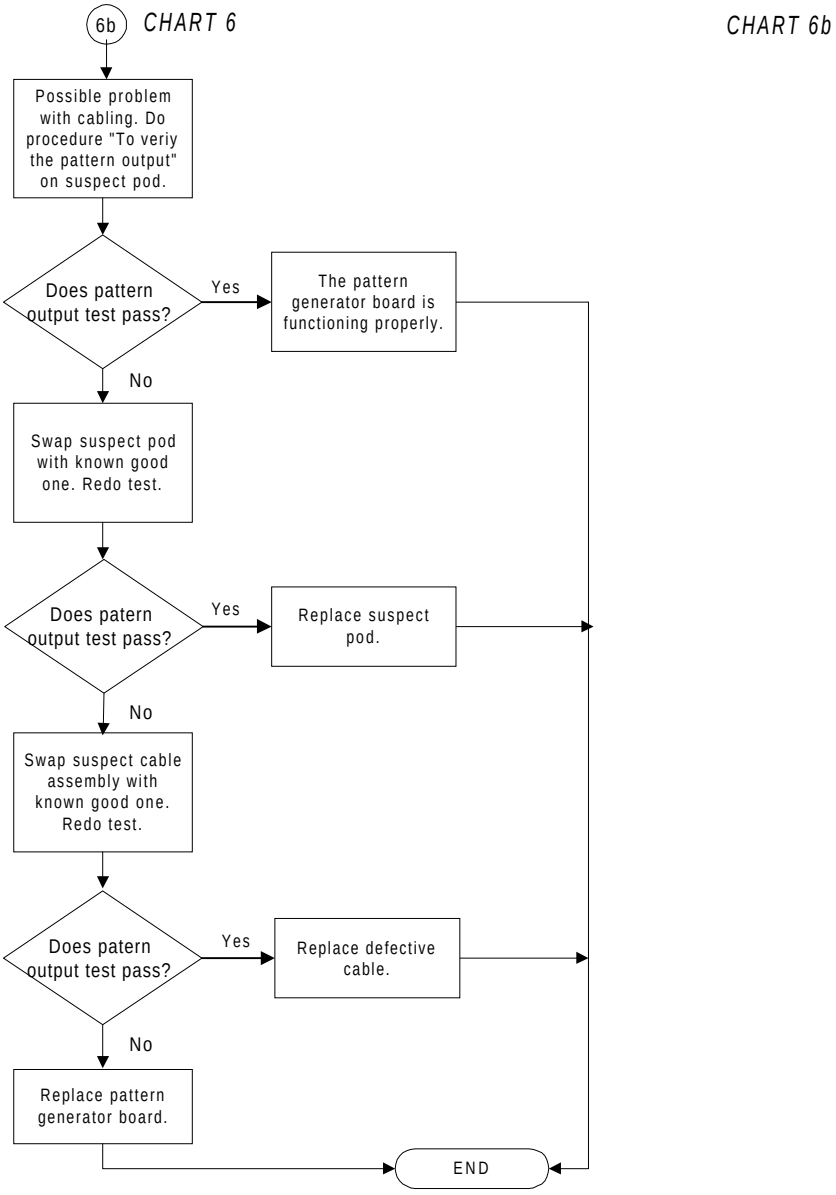
Troubleshooting Flowchart 6



Troubleshooting Flowchart 6a



Troubleshooting Flowchart 6b



To check the power-up tests

The logic analyzer automatically performs power-up tests when you apply power to the instrument. The revision number of the operating system shows in the upper-right corner of the screen during these power-up tests. As each test completes, either "PASSED" or "FAILED" prints on the screen in front of the name of each test.

1. Disconnect all inputs, then insert a formatted disk into the disk drive.
2. Let the instrument warm up for a few minutes, then cycle power by turning off then turning on the power switch.

   If the instrument is not warmed up, the power-up test screen will complete before you can view the screen.
3. As the tests complete, check if they pass or fail.

   The Flexible Disk Test reports No Disk if a disk is not in the disk drive.

Performing Power-Up Self-Tests

passed	ROM text
passed	RAM test
passed	Interrupt test
passed	Display test
passed	PS2 Controller Test
passed	Hard Disk Test
No Disk	Flexible Disk Test

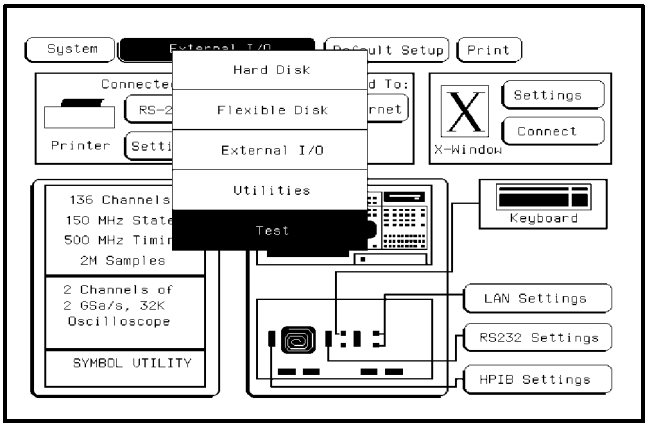
To run the self-tests

Self-tests identify the correct operation of major functional areas of the instrument. You can run all self-tests without accessing the interior of the instrument. If a self-test fails, the troubleshooting flowcharts instruct you to change a part of the instrument.

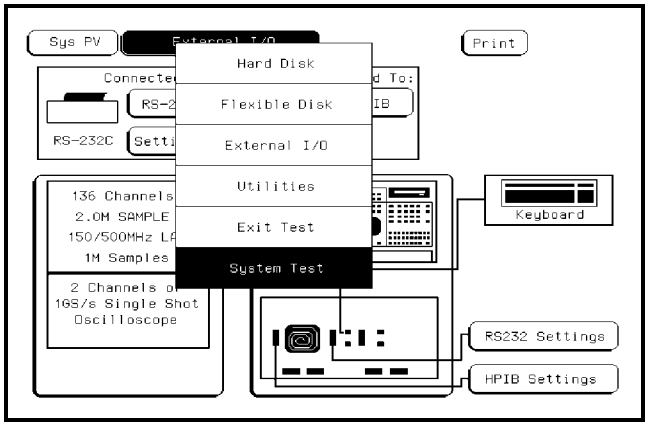
These procedures assume the files on the PV disk have been copied to the /SYSTEM subdirectory on the hard disk drive. If they have not already been copied, insert the PV disk in the flexible disk drive before starting this procedure.

1. If you just did the power-up self-tests, go to step 2.

   If you did not just do the power-up self-tests, disconnect all inputs, then turn on the power switch. Wait until the power-up tests are complete.
2. Press the System key, then select the field next to System. Select Test in the pop-up menu.

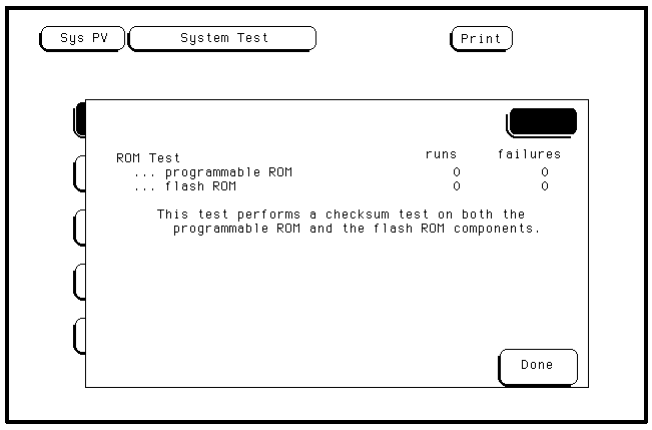


3. Select the box labeled Load Test System.
4. Press the System key, then select the field next to Sys PV. Select System Test to access the system tests.



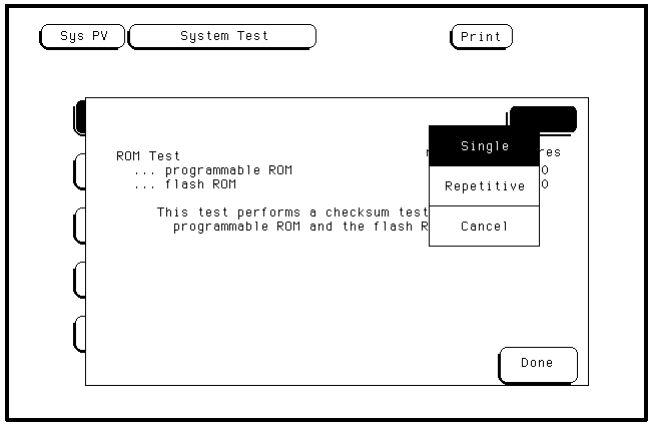
5 Select ROM Test. The ROM Test screen is displayed.

You can run all tests at one time by running All System Tests. To see more details about each test, you can run each test individually. This example shows how to run an individual test.

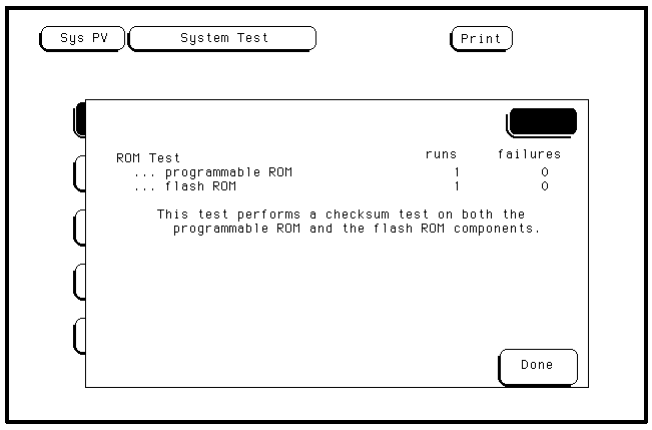


6 Select Run, then select Single.

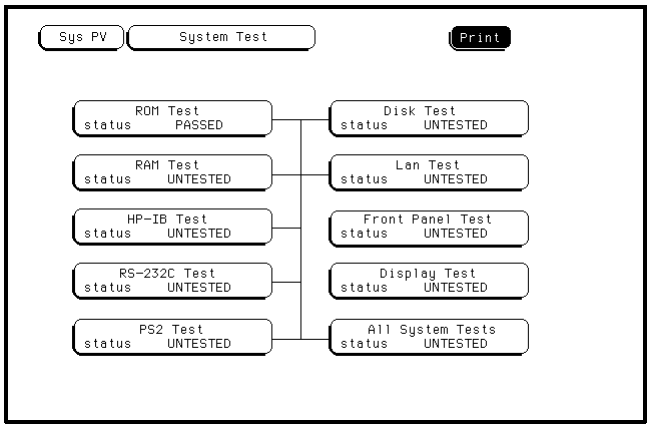
To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.



For a Single run, the test runs one time and the screen shows the results.



7 To exit the ROM Test, select Done. Note that the status changes to PASSED or FAILED.



8 Install a formatted disk that is not write protected into the flexible disk drive. Connect an RS-232-C loopback connector onto the RS-232-C port. Run the remaining System Tests in the same manner.

9 Select the Front Panel Test.

A screen duplicating the front-panel appears on the screen.

a Press each key on the front panel. The corresponding key on the screen will change from a light to a dark color.

b Test the knob by turning it in both directions.

c Note any failures, then press the Done key a second time to exit the Front Panel Test. The test screen shows the Front Panel Test status changed to TESTED.

10 Select the Display Test.

A white grid pattern is displayed. These display screens can be used to adjust the display.

a Select Continue and the screen changes to full bright.

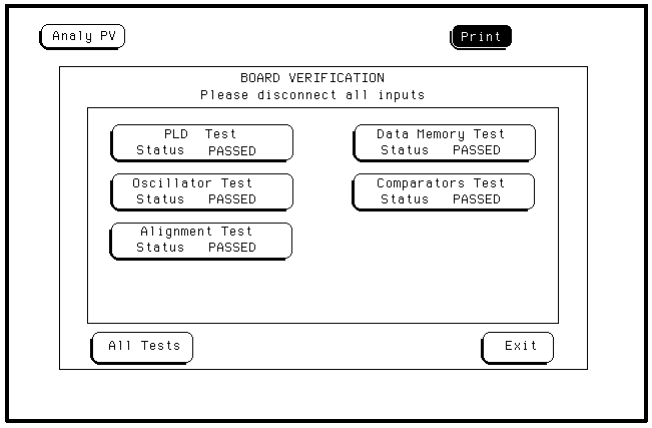
b Select Continue and the screen changes to half bright.

c Select Continue and the test screen shows the Display Test status changed to TESTED.

11 Select Sys PV, then select Analy PV in the pop-up menu. In the Analy PV menu, select Board Verification Tests. In the Board Verification menu, select All Tests.

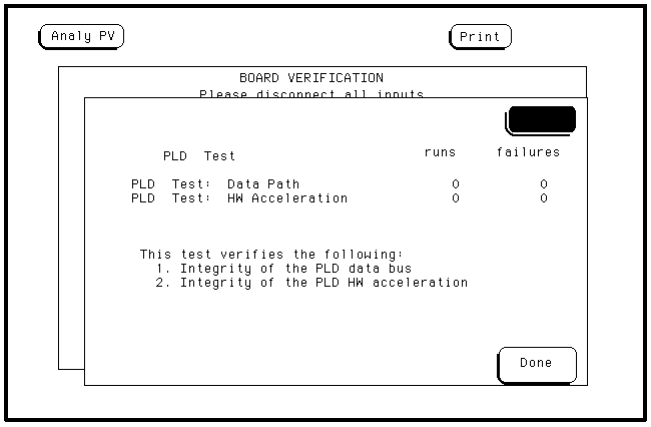
You can run all tests at one time by selecting All Tests. To see more details about each test when troubleshooting failures, you can run each test individually. This example shows how to run all tests at once.

When the tests finish, the status for each test shows PASSED or FAILED, and the status for the All Tests changes from UNTESTED to TESTED.



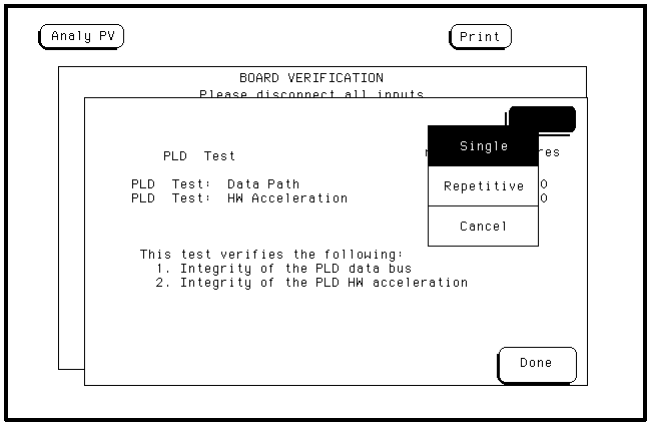
12 Select PLD Test. The PLD Test screen is displayed.

You can run all tests at one time by running All System Tests. To see more details about each test, you can run each test individually. This example shows how to run an individual test.

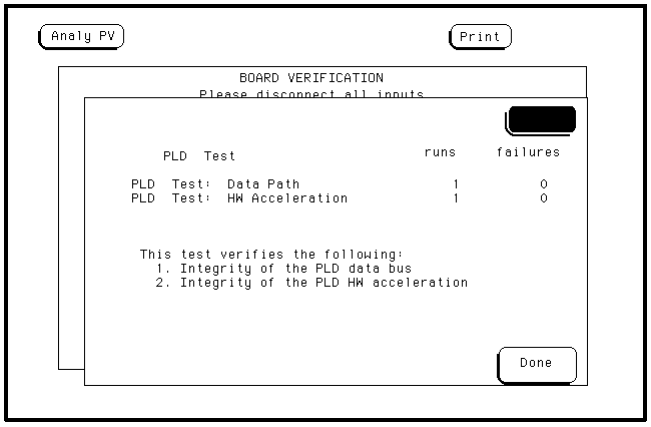


13 Select Run, then select Single.

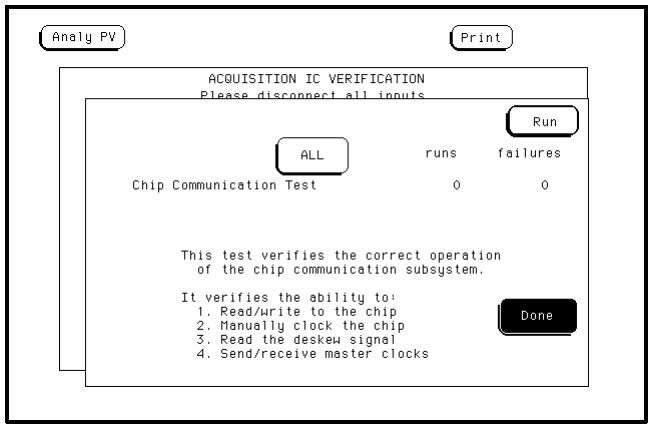
To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.



For a Single run, the test runs one time, and the screen shows the results.



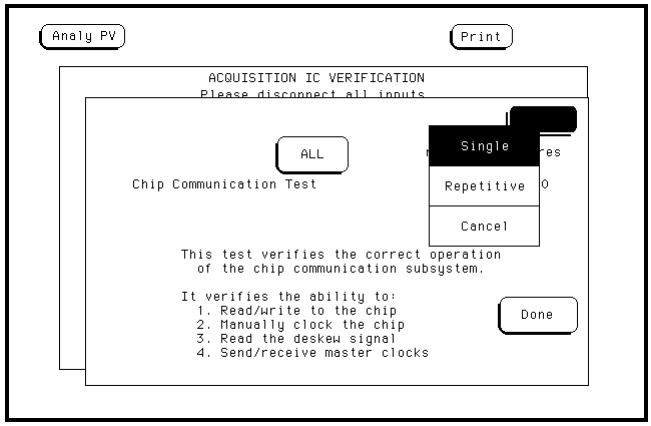
14 Select Exit to exit the Board Verification Test. In the Analy PV menu, select Acquisition IC Verification, then select Communication Test.



15 Select Run, then select Single.

To run a test continuously, select Repetitive. Select Stop to halt a repetitive test.

For a Single run, the test runs one time and the screen shows the results.

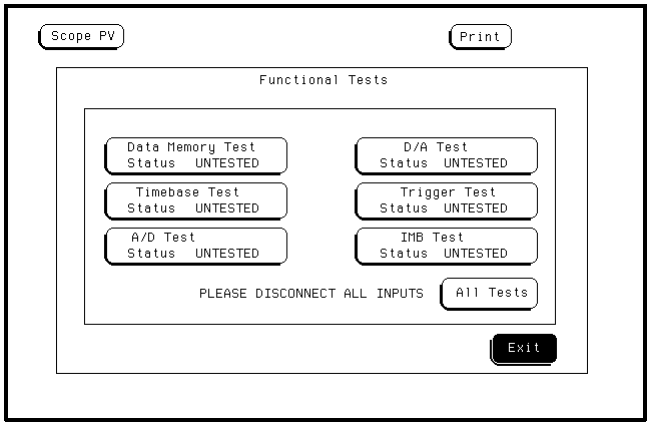


If you have an Agilent 1670G-series Logic Analyzer without an oscilloscope or pattern generator, go to step 19. If you have an Agilent 1670G-series Logic Analyzer with a pattern generator, go to step 18. If you have an Agilent 1670G-series Logic Analyzer with an oscilloscope, continue with step 15.

16 Select Analy PV, then select Scope PV in the pop up menu. Select Functional Tests.

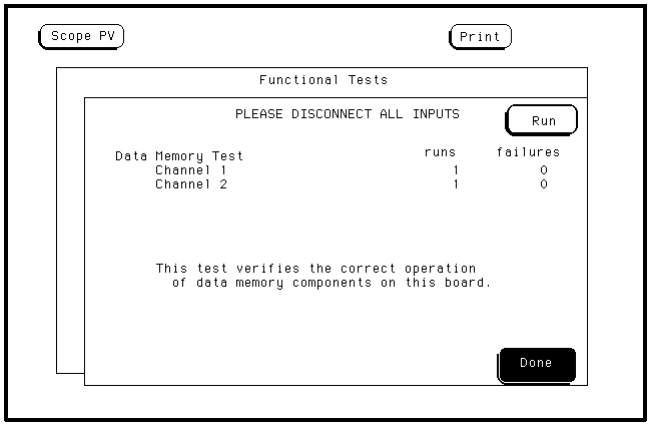
17 Select one of the Scope PV tests.

You can run all of the tests at one time by selecting All Tests, or you can run each test individually. For this example, select Data Memory Test.



18 In the Data Memory Test menu, select Run, then select Single. The test runs one time, then the screen shows the results. When the test is finished, select Done.

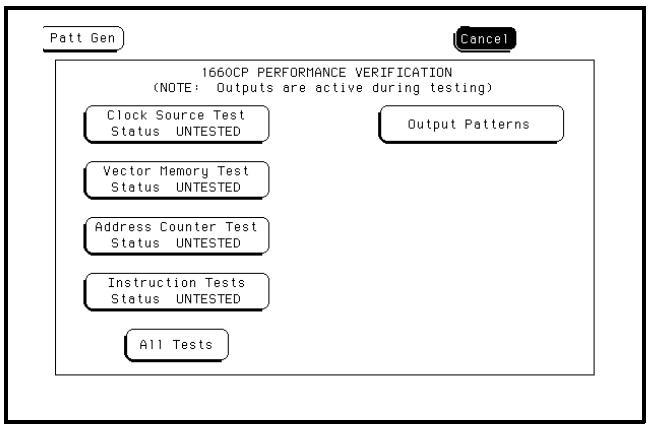
To run a test continuously, select Repetitive. Select Stop to halt a Repetitive Run.
Go to step 19 to exit the test system.



19 For the pattern generator, Select Analy PV, then select Patt Gen in the pop-up menu. In the Patt Gen menu select Clock Source Test.

You can run all tests at one time (except the Output Patterns routine) by selecting All Tests. To see more details about each test, you can run each test individually. This example shows how to run the Clock Source Test. The Vector Memory Test, Address Counter Test, and Instruction Tests are run in a similar manner.

When the tests finish, the status for each test shows Passed or Failed. Select Done.



20 To exit the tests, press the System key. Select the field to the right of the Sys PV field.

21 Select the Exit Test System.

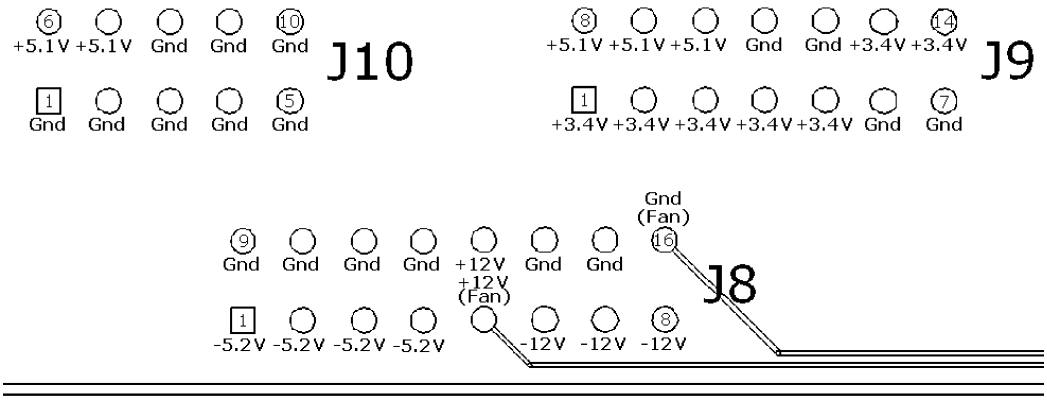
If you are performing the self-tests as part of the troubleshooting flowchart, return to the flowchart.

To test the power supply voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

WARNING Hazardous voltages exist on the power supply and the LCD display. Only service-trained personnel who are aware of the hazards involved, such as fire and electrical shock, should perform this procedure.

1. Turn off the instrument, then remove the power cable. Remove the cover of the instrument and the disk drive assembly (including the support plate).
2. Reconnect both the hard disk drive and flexible disk drive to the CPU board
3. Connect the power plug, then turn on the instrument.
4. Check for voltages on the acquisition board power input connectors according to the following diagram.



5. Turn off the instrument. Allow time for the capacitors in the power supply to discharge. Remove and replace the power supply if needed.
6. Reassemble the instrument.

To test the LCD display signals

Before attempting to do this procedure, ensure that the video signal cable connected to the LCD display and to the CPU board is properly seated in both connectors. Attempt to reseat the cable two or three times. If other repairs were done to the instrument, and the video is now no longer operating, it is very likely that the video cable is not properly seated at either the LCD display or the CPU board.

Refer to chapter 6, "Replacing Assemblies", for instructions to remove or replace covers and assemblies.

WARNING Warning Hazardous voltages exist on the power supply and the LCD display, and the LCD inverter. This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electric shock.

1. Remove the following assemblies. Refer to chapter 6 for more information on how to remove the assemblies.
   - Cover
   - Disk Drives
   - Acquisition Board
2. Reconnect the power supply.

   a. Position the power supply so that it does not obstruct the CPU board, yet provides access to probe J4 on the CPU board.

   b. Connect both the line filter and the power output cable to the power supply.

   c. Ensure the power supply does not contact any other subassembly in the instrument.
3. Using an oscilloscope, probe the following pins of J4 for digital signals.

   12,13,14

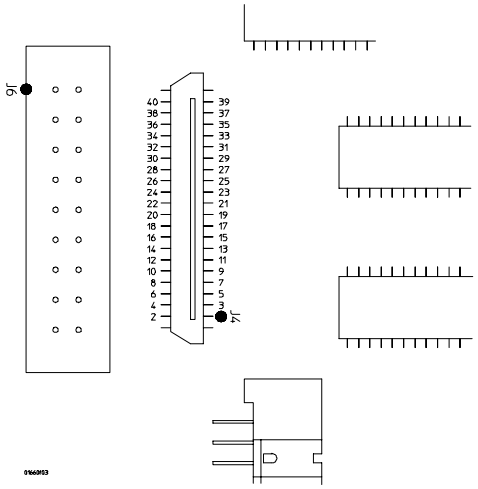
   16,17,18

   20,21,22

   24,25,26

   28,29,30

   23,33,34



4 Using an oscilloscope, probe pins 1 and 2 of J4 for +3.3Vdc

If +3.3Vdc is present on J4 of pins 1 and 2, and digital signals are present on the video data pins indicated above, then the CPU board video circuit is operating properly.

5 Remove power. Allow time for the capacitors in the power supply to discharge before disconnecting the power supply, doing the repair, and reassembling the instrument.

To test the keyboard signals

Refer to chapter 6, "Replacing Assemblies," for instructions to remove covers and assemblies.

WARNING

Hazardous voltages exist on the power supply and the LCD display. Only service-trained personnel who are aware of the hazards involved, such as fire and electrical shock, should perform this procedure.

1 Turn off the instrument and remove the power cable.

2 Without disconnecting the keyboard cable, follow the keyboard removal procedure to loosen the keyboard. Leave the keyboard in place in front of the instrument.

3 Reconnect the power cable, then turn on the instrument.

4 Run the PV Front Panel Test, pressing all of the keys.

5 If a random key is not operating, go to the next step.

If a group of keys do not work, then check the keyboard voltages and signals.

Keyboard Connector Signals

Pin	Signal	Pin	Signal
1	Keyboard Return	13	Keyboard Scan
2	"	14	"
3	"	15	"
4	"	16	"
5	"	17	"
6	"	18	"
7	"	19	LED
8	"	20	+5 V
9	Keyboard Scan	21	Ground
10	"	22	Knob
11	"	23	Ground
12	"	24	Knob

6 Allow the keyboard assembly to fall forward from the front panel. Separate the elastomeric keypad and keyboard panel from the PC board.

7 Using a paper clip or screwdriver, short the PC board trace of the non-operating key and look for an appropriate response on the display.

8 If the display responds as though the key was pressed, replace the elastomeric keypad.

If the display does not respond as though the key was pressed, replace the keyboard.

9 Check the RPG connector.

The RPG connector has a TTL pulse on pins 22 and 24 when you turn the knob. Pin 20 of the connector is +5 V.

To test the flexible disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

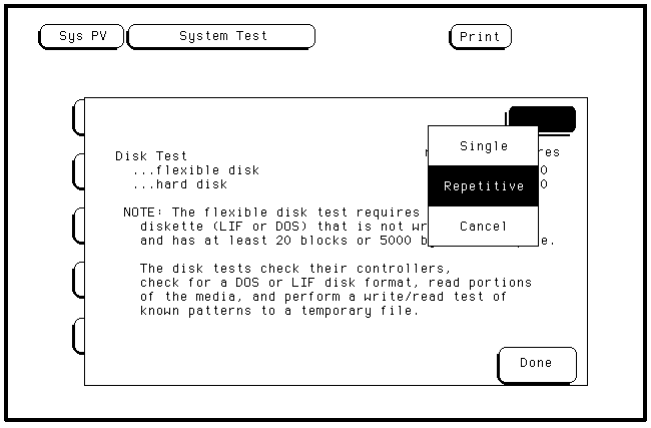
WARNING

This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B

1. Turn off the instrument, then remove the power cable. Remove the instrument cover and the disk drive.
2. Reconnect the disk drive cable to the rear of the disk drive. Turn the disk drive over so that the solder connections of the cable socket are accessible.
3. Connect the power cable, then turn on the instrument.
4. Insert the disk that contains the functional performance verification software and enter the test operating system.
5. In the Sys PV menu select the Disk test. Insert a disk that has enough available bytes to run the test in the disk drive, then select Run-Repetitive.



6 Check for the following voltages and signals using an oscilloscope.

Disk Drive Voltages

Pin	Signals	Pin No.	Signal
1	+5V	2	INDEX
3	+5V	4	DRIVE SELECT
5	+5V	6	DISK CHANGE
7	NC	8	READY
9	HD OUT (HD at HIGH level)	10	MOTOR ON
11	NC	12	DIRECTION SELECT
13	NC	14	STEP
15	0V	16	WRITE DATA
17	0V	18	WRITE GATE
19	0V	20	TRACK 00
21	NC	22	WRITE PROTECT
23	0V	24	READ DATA
25	0V	26	SIDE ONE SELECT

7 Select Stop, and turn off the logic analyzer. Remove the power cable.

The test will not immediately stop when Stop is selected; it will continue until the current iteration of the disk test is completed and then stop.

8 Disconnect the disk drive cable and re-install the disk drive in the logic analyzer.

9 Reconnect the disk drive cable and install the cover on the logic analyzer.

To test the hard disk drive voltages

Refer to chapter 6, "Replacing Assemblies," for instructions to remove or replace covers and assemblies.

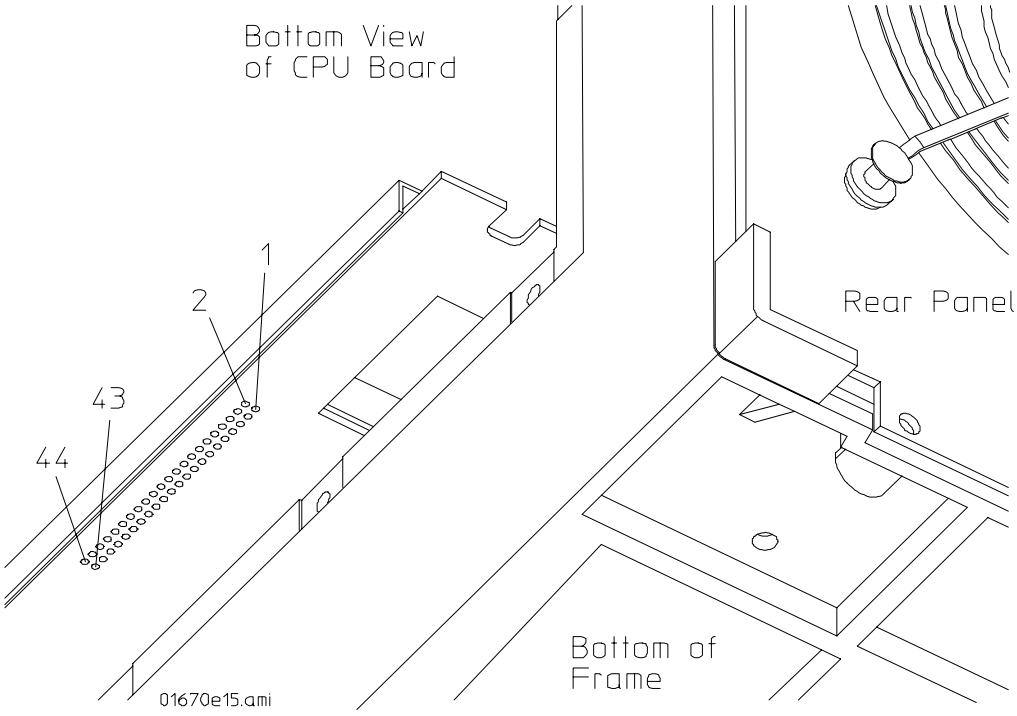
WARNING

This procedure is to be performed by service-trained personnel aware of the hazards involved, such as fire and electrical shock.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	> 100 MHz Bandwidth	54600B

1. Turn off the instrument, then remove the power cable. Remove the instrument cover and the disk drive assembly.
2. Remove the two locking pins from the top of the power supply. Slide the CPU board out of the instrument enough to access J12 on the outer edge of the CPU board.
3. Reconnect the disk drive cables.
4. Connect the power cable, then turn on the instrument.
5. In the Sys PV menu select the Disk test. Select Run-Repetitive.



6 Check for the following voltages and signals at J12 on the CPU board using an oscilloscope.

Disk Drive Voltages

Pin No.	Signal	Voltage	Pin No.	Signal	Voltage	Pin No.	Signal	Voltage
1	RESET		27	IORDY		34	PDIAG	
3 - 18	DATA		28	CSEL		35	DA00	
20	KEY		29	DMACK		36	DA02	
21	DMARQ		31	INTRQ		37	CS0	
23	DIOW		32	IOCS16		38	CS1	
25	DIOR		33	DA01		39	DASP	
						41	+5V Logic	PWR
						42	+5V Motor	PWR
Pins 2, 19, 22, 24, 26, 30, 40, 43 are GROUND						44	(Resv)	

7 Select Stop, and turn off the logic analyzer. Remove the power cable.

The test will not immediately stop when Stop is selected; it will continue until the current iteration of the disk test is completed and then stop.

8 Disconnect the disk drive cables. Re-install the hard disk drive onto the disk drive assembly, and then re-install the disk drive assembly in the logic analyzer.

9 Reconnect the disk drive cables and install the cover on the logic analyzer.

Connect the hard disk drive cable to the data pins as shown in the illustration. Do not connect the cable to the address pins.

To perform the BNC test

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Digitizing Oscilloscope	100 MHz Bandwidth	54820A
BNC Shorting Cap		1250-0774
BNC Cable		8120-1840
BNC-Banana Adapter		1251-2277

1. Press the Config key.
2. Assign pods 1 and 2 to Machine 1.

   To assign the pod field, select the pods 1 and 2 field, then select Machine 1 in the pop-up menu.
3. In the Analyzer 1 box, select the Type field. Select Timing in the pop-up menu.
4. Set up the trigger menu.
   a. Press the Trig key. Select Clear Trigger All.
   b. Select Arming Control. In the Arming Control pop-up menu, select the field labeled Run, then select Port In. Press the Done key.
5. Attach a BNC shorting cap to the External Trigger Input on the rear panel of the logic analyzer.
6. Using a BNC cable, connect the External Trigger output to the oscilloscope channel 1 input. Set the oscilloscope to Trigger On and measure TTL voltage levels.
7. Press the RUN front-panel key.

   The warning "MACHINE 1 Waiting on level 1" will appear.
8. Remove the shorting cap from the rear-panel External Trigger input BNC.
9. The warning will go away and the oscilloscope will display a positive-going TTL pulse.

To test the logic analyzer probe cables

This test allows you to functionally verify the probe cable and probe tip assembly of any of the logic analyzer pods. Only one probe cable can be tested at a time. Repeat this test for each probe cable to be tested.

Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	100 MHz, 3.5 ns pulse width, < 600 ps rise time	8133A Option 003
Adapter (Qty 4)	SMA (m) - BNC (f)	1250-1200
Coupler (Qty 4)	BNC (m)(m)	1250-0216
6x2 Test Connectors (Qty 4)		

1 Turn on the equipment and the logic analyzer.

2 Set up the pulse generator.

a Set up the pulse generator according to the following table.

Pulse Generator Setup

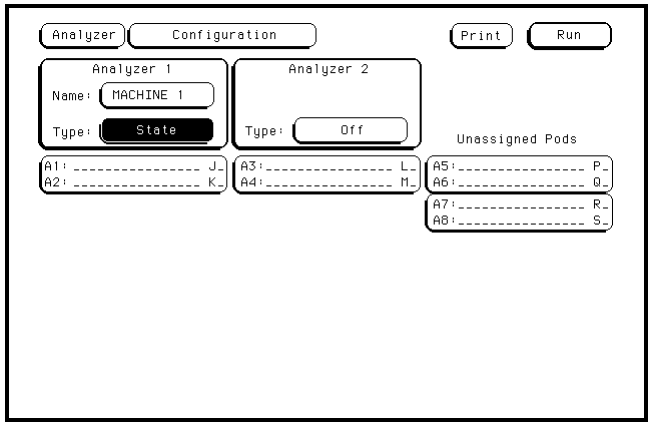
Timebase	Channel 2	Period	Channel 1
Mode: Int	Mode: Pulse	Divide: Divide ÷ 1	Mode: Pulse
Period: 20.000 ns	Divide: PULSE ÷ 1	Ampl: 0.50 V	Delay: 0.000 ns
	Width: 3.500 ns	Offs: 0.00 V	Width: 3.500 ns
	High: –0.90 V		High: –0.90 V
	Low: –1.70 V		Low: –1.70 V
	COMP: Disabled (LED Off)		COMP: Disabled (LED Off)

b Enable the pulse generator channel 1 and channel 2 outputs (with the LEDs off).

3 Set up the logic analyzer Configuration menu.

a Press the Config key.

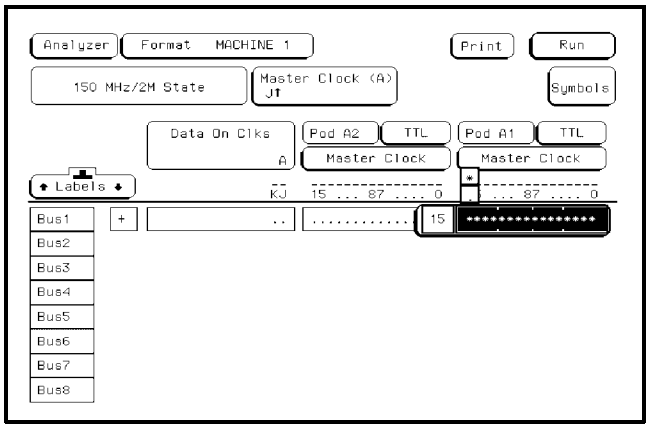
b In the Analyzer 1 box, select the field to the right of Type, then select State.



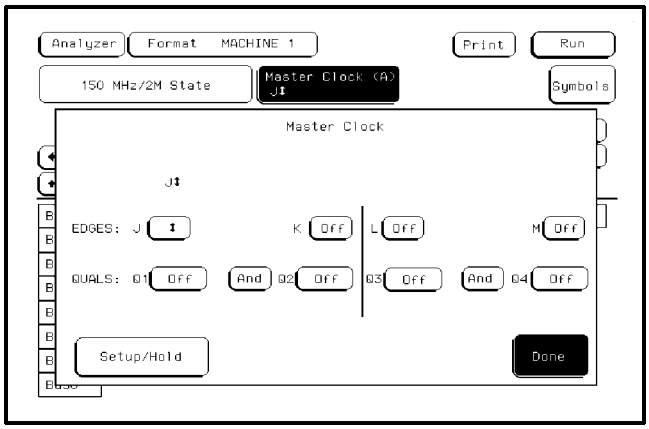
4 Set up the Format menu.

a Press the Format key.

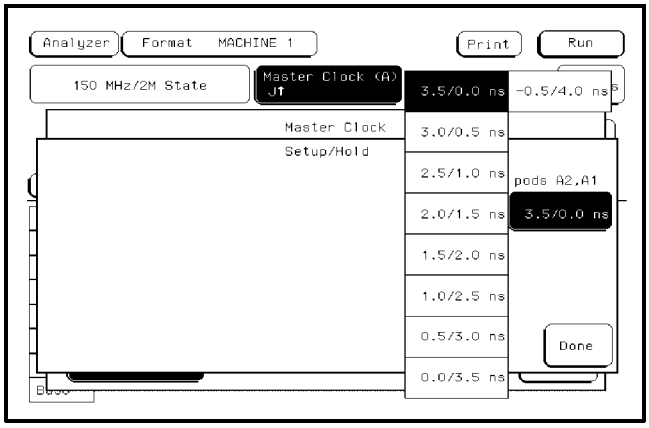
b Move the cursor to the field showing the channel assignments for the pod under test. Press the Clear Entry key until the pod channels are all assigned (all asterisks (*)). Press the Done key.



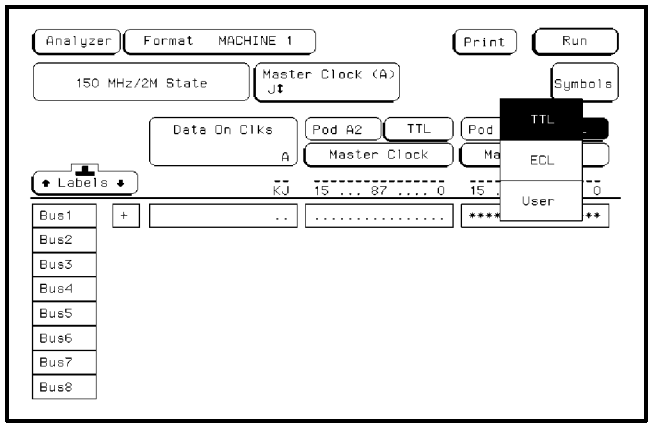
c Select Master Clock, then select a double edge for the clock of the pod under test. Turn off the other clocks.



d In the Master Clock menu, select Setup/Hold, then select 4.0/0.0 ns for the pod being tested. Select Done. Select Done again to exit the Master Clock menu.



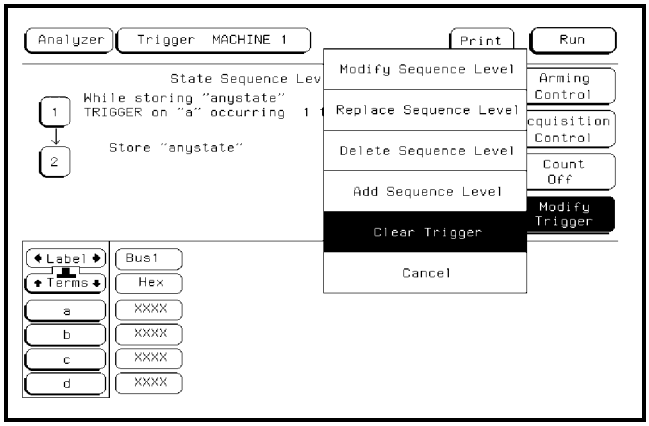
e Select the field to the right of the pod being tested, then select TTL.



5 Set up the Trigger menu.

a Press the Trigger key.

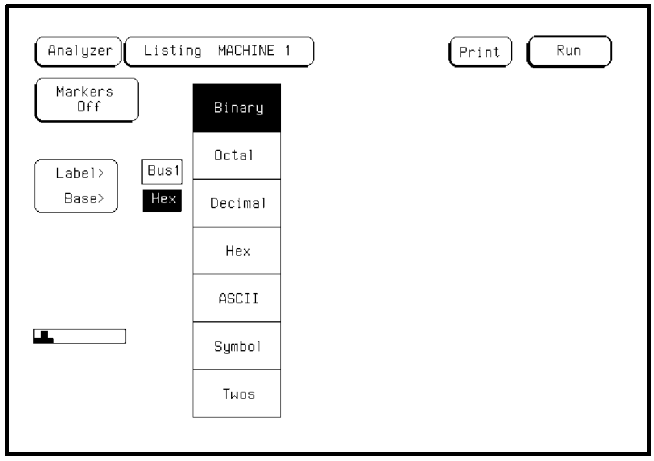
b Select Modify Trigger, then select Clear Trigger, then select All.



6 Set up the Listing menu.

a Press the List key.

b Select the field to the right of Base, then select Binary.



7 Using four 6-by-2 test connectors, four BNC Couplers, and four SMA (m) - BNC (f) Adapters, connect the logic analyzer to the pulse generator channel outputs. To make the test connectors, see chapter 3, "Testing Performance."

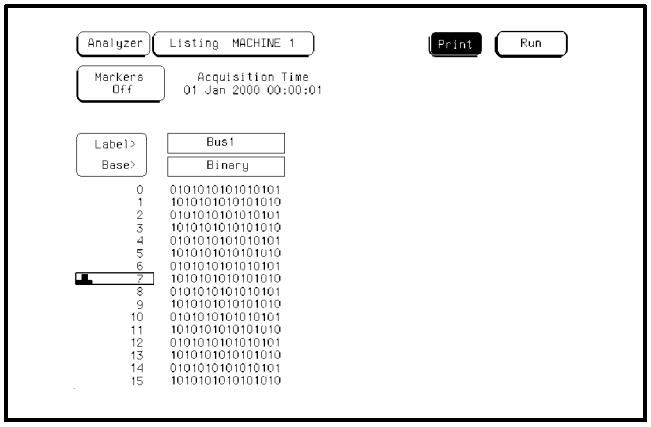
a Connect the even-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 Output and J-clock.

b Connect the odd-numbered channels of the lower byte of the pod under test to the pulse generator channel 1 $\overline{\text{Output}}$.

c Connect the even-numbered channels of the upper byte of the pod under test and the clock channel to the pulse generator channel 2 Output.

d Connect the odd-numbered channels of the upper byte of the pod under test to the pulse generator channel 2 $\overline{\text{Output}}$.

8 On the logic analyzer, press Run. The display should look similar to the figure below.



9 If the display looks like the figure, then the cable passed the test.

If the display does not look similar to the figure, then there is a possible problem with the cable or probe tip assembly. Causes for cable test failures include the following:

- open channel
- channel shorted to a neighboring channel
- channel shorted to either ground or a supply voltage

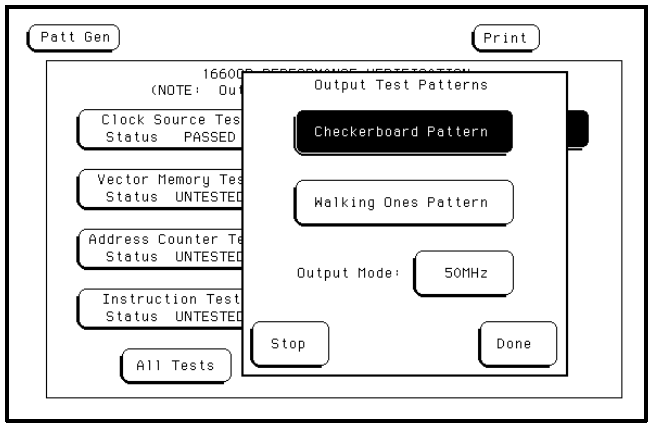
Return to Troubleshooting Flowchart 7.

To verify pattern output (pattern generator option only)

Equipment Required

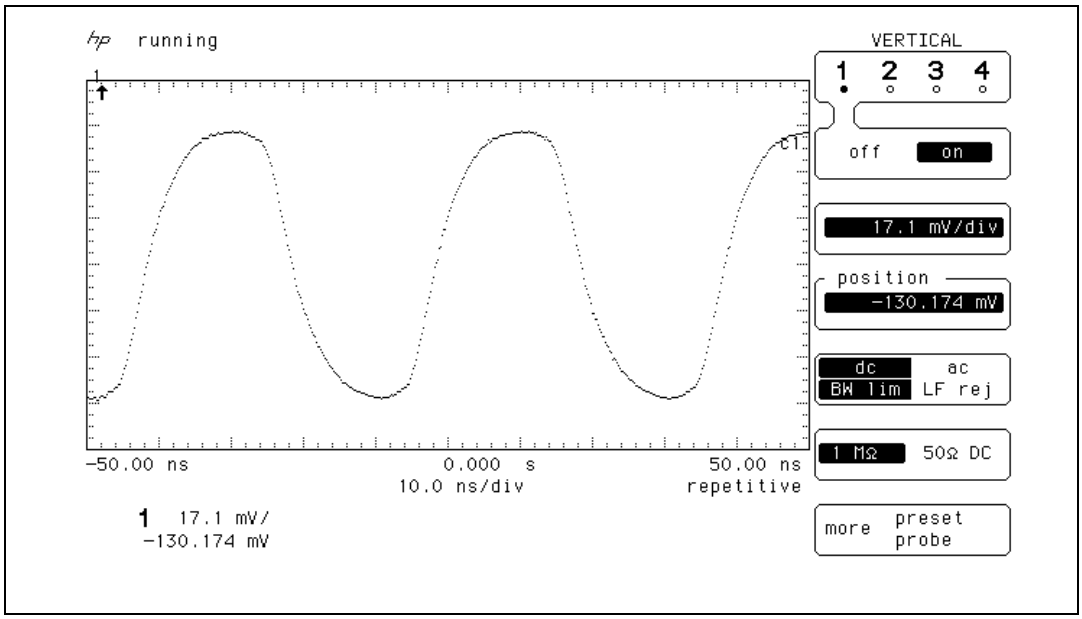
Equipment	Critical Specification	Recommended Model/Part
Oscilloscope	≥ 500 MHz Bandwidth	54522A
Probe	500 MHz Bandwidth	10441A
Output Data Pod	no substitute	10460A - series

1 Connect one of the 10460-series data pods to the end of the pattern generator Pod 1 cable.



2 Touch Output Patterns. In the pop-up menu, touch Checkerboard Pattern.

3 Using an oscilloscope, verify the existence of logic-level transitions by touching the oscilloscope probe to each channel of Data Pod 1 and doing an Autoscale. The signal levels that appear on the oscilloscope display should correspond with the logic levels represented by the 10460-series pod being used.



4 Repeat step 3 for each of the remaining four data pods.

5 Connect one of the 10460-series clock pods to the end of the pattern generator clock cable.

6 Using the oscilloscope as in step 3, verify the existence of logic-level transitions by touching the oscilloscope probe to each clock output of the clock pod.

7 In the pattern generator Output Patterns menu, touch Stop, then touch Done to exit the menu.

The Ether address

If for some reason the CPU board NV-RAM (non-volitile memory) becomes corrupted, the Ether (LANIC) address will reinitialize itself. The instrument polls the NV-RAM as part of the boot routine. If the instrument senses a reinitialized Ether address, the following red error message appears after the instrument finished booting:

```
Corrupted Ether Address! LAN not functional!
```

To store the instrument Ether Address

When the CPU board is replaced, the Ether address must be re-entered into the CPU board NV-RAM. Normally a prompt will appear to re-enter the Ether address as part of the boot routine. In case a prompt does not appear, use the following procedure to re-enter the original Ether address after replacing the CPU board. The Ether address is on a sticker on the rear panel of the instrument.

1. Look on the rear panel for the Ether Address sticker. On the sticker is the 12-digit Ether address. If desired, write down the number.
2. After the instrument finishes booting, push the [System] key. The instrument should be in the External I/O menu.
3. Move the cursor to the LAN Settings field, and push the [Select] key.
4. In the LAN Setting menu, move the cursor to the Factory Settings field and push the [Select] key.
5. In the Factory Settings menu, enter the 12-digit Ether address in the Ether Address field. Then move the cursor to the Enter field and push the [Select] key.
6. Push the [Done] key to exit the Factory Settings menu. Push the [Done] key again to exit the LAN Settings field.

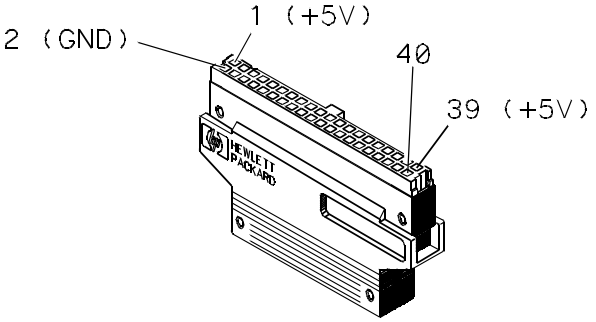
To test the auxiliary power

The +5 V auxiliary power is protected by a current overload protection device. If the current on pins 1 and 39 exceed 0.33 amps, the circuit will open. When the short is removed, the circuit will reset in approximately 1 minute. There should be +5 V after the 1 minute reset time.

Equipment Required

Equipment	Critical Specifications	Recommended Model/Part
Digital Multimeter	0.1 mV resolution, better than 0.005% accuracy	E2373A

- Use the multimeter to verify the +5 V on pins 1 and 39 of the probe cables.



MISC/EX50

6

To remove and replace the
- Handle 6-5
- Feet and tilt stand 6-5
- Cover 6-5
- Disk drive assembly 6-6
- Acquisition board 6-7
- CPU board 6-9
- SIMM memory 6-10
- Rear panel assembly 6-11
- Power supply 6-12
- Oscilloscope board 6-13
- Pattern generator board 6-14
- Front panel and keyboard 6-15
- To remove and replace the LCD display 6-16
- Handle plate 6-17
- Fan 6-18
- Pattern generator cables 6-18
- GPIB and RS-232-C cables 6-19
- I/O board 6-19

To return assemblies 6-20

Replacing Assemblies

Replacing Assemblies

This chapter contains the instructions for removing and replacing the assemblies of the logic analyzer. Also in this chapter are instructions for returning assemblies.

WARNING

Hazardous voltages exist on the power supply, the CRT, and the CRT driver board. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors on the power supply board and the CRT driver board to discharge before servicing the instrument. Refer servicing to qualified personnel.

CAUTION

Damage can occur to electronic components if you remove or replace assemblies when the instrument is on or when the power cable is connected. Never attempt to remove or install any assembly with the instrument on or with the power cable connected.

Replacement Strategy

These replacement procedures are organized as if disassembling the complete instrument, from the first assembly to be removed to the last. Some procedures say to remove other assemblies of the instrument, but do not give complete instructions. Refer to the procedure for that specific assembly for the instructions. Use the exploded view of the instrument on the next page as a reference during the replacement procedures.

CAUTION

Electrostatic discharge can damage electronic components. Use grounded wrist straps and mats when performing any service to this logic analyzer.

Tools Required

#10 TORX screwdriver
#15 TORX screwdriver
#20 TORX screwdriver
#1 Posidrive screwdriver
3/16-inch (5-mm) nut driver
9/32-inch (7-mm) nut driver

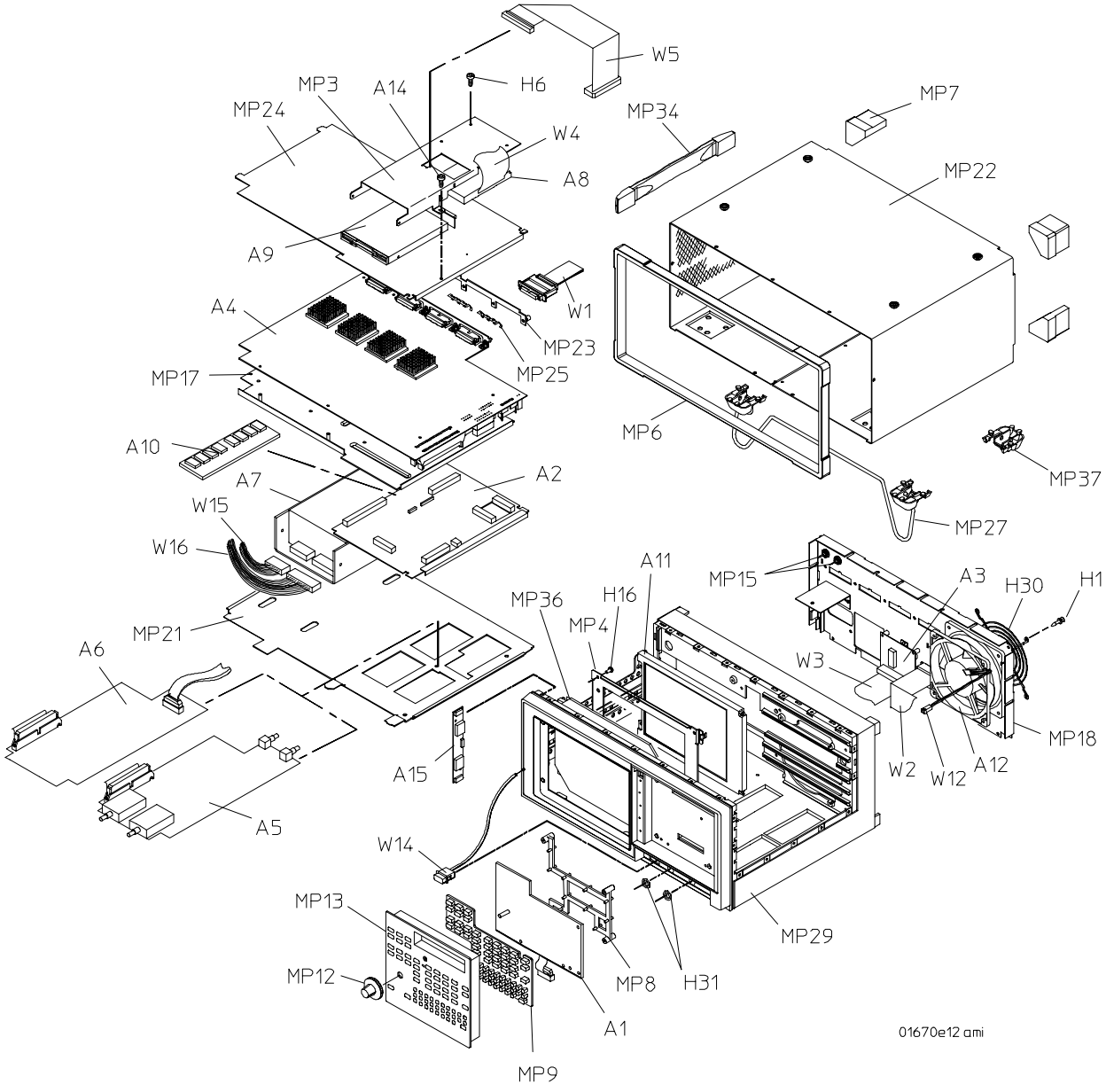
Exploded View

Listing

A1	Keyboard	MP1	Locking pin	W2	RS-232-C cable
A2	CPU board	MP3	Disk drive bracket	W3	I/O cable
A3	I/O Board	MP8	Front panel spacer	W4	Hard disk drive cable
A4	Acquisition board	MP9	Elastomeric keypad	W5	Flexible disk drive cable
A5	Oscilloscope board *	MP11	Keyboard spacer	W7	Display cable
A5	Attenuator assembly	MP12	RPG knob	W8	Inverter cable
A6	Pattern Generator board*	MP13	Keyboard panel	W9	CPU Cable
A7	Power supply	MP15	BNC connector	W10	Cable - 60-conductor *
A8	Hard disk drive	MP18	Rear panel	W12	Fan cable
A9	Flexible disk drive	MP19	Handle brace	W13	GPIB cable
A10	SIMM	MP21	Mounting plate	W15	Power supply cable-24
A11	LCD display	MP28	Insulator	W16	Power supply cable -16
A12	Fan	MP29	Chassis assembly	W17	Jumper cable-orange
				W18	Jumper cable-white
H30	Fan guard				
H31	Hex nut **				

* The Agilent 1670G series with the pattern generator option has a pattern generator board, and the Agilent 1670G series with the oscilloscope option has an oscilloscope board.

** Agilent 1670G series with the oscilloscope option only



Exploded View of the Agilent 1670G-series logic analyzer

To remove and replace the handle

- Remove the two screws in the endcaps, then lift off the handle.
- Replace the handle and tighten the screws to 2.4 Nm (21 in-lb.).

To remove and replace the feet and tilt stand

1. Remove the screws connecting the four rear feet to the instrument.
2. Separate the rear feet from the instrument to remove them.
3. Press the locking tab on the bottom feet, then remove them.
4. Remove the tilt stand from the bottom front feet by sliding each foot off of the stand.
5. Reverse this procedure to install the feet and tilt stand.

To remove and replace the cover

1. Turn the power off and remove the power cord.
2. Remove the probe plate and disconnect the logic analyzer cables from the rear panel.
3. Using the previous procedures, remove the handle and the four rear feet.
4. Remove the seven screws from the front molding, then slide the molding forward to remove it.
5. Remove the cover.

   To remove the cover, set the instrument upright and facing toward you. Slide the chassis toward the front, out of the cover, and set it on a static-safe work area.
6. Reverse this procedure to install the cover.

   Check that all assemblies are properly installed before installing the cover.

   When installing the chassis in the cover, check that the tabs located at the bottom, rear of the cover align with the holes in the rear panel.

To remove and replace the disk drive assembly

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover

2 Disconnect the two disk-drive ribbon cables from the CPU board. Peel the cables away from the double-sided tape used to secure the cables to the disk drive bracket.

3 Remove the two screws that attach the disk drive bracket to the support tray.

4 Slide the disk drive assembly toward the front of the instrument about 1/2 inch (1.25 cm). Angle the rear of the bracket up and out of the chassis. Then remove the disk drive assembly completely out of the chassis by sliding the assembly toward the rear of the instrument.

5 If needed, remove the support tray from the chassis.

a. Lift the PCB locking pins out of the chassis.

b. Slide the support tray out of the second slot of the chassis.

When installing the support tray, ensure that the tabs on the support tray are inserted into the slots in the handle plate.

6 Remove the flexible disk drive from the bracket.

a. Disconnect the flexible disk drive from the bracket.

b. Remove the four screws that attach the flexible disk drive to the bracket. There are two on each side.

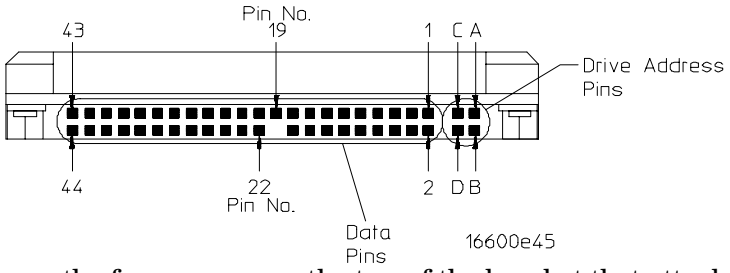
c. Lift the flexible disk drive out of the bracket.

d. To remove the interface board, remove one screw that attaches the interface board to the bracket and lift the board out of the bracket.

7 Remove the hard disk drive from the bracket.

a. Disconnect the hard disk drive cable from the hard disk drive.

When connecting the cable, ensure the cable is connected to the Data pins, not the Address pins.



b. Remove the four screws on the top of the bracket that attach the hard drive to the bracket.

c. Lift the hard disk drive out of the bracket.

8 Reverse this procedure to install the disk drive assembly.

Check that the following assemblies are properly installed before installing the disk drive:

- Power Supply
- LCD Display
- Front Panel
- CPU Board
- Acquisition Board
- Oscilloscope/Pattern Generator Board (if installed)

To remove and replace the acquisition board

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly

2 Disconnect the following cables from the acquisition board:

CAUTION

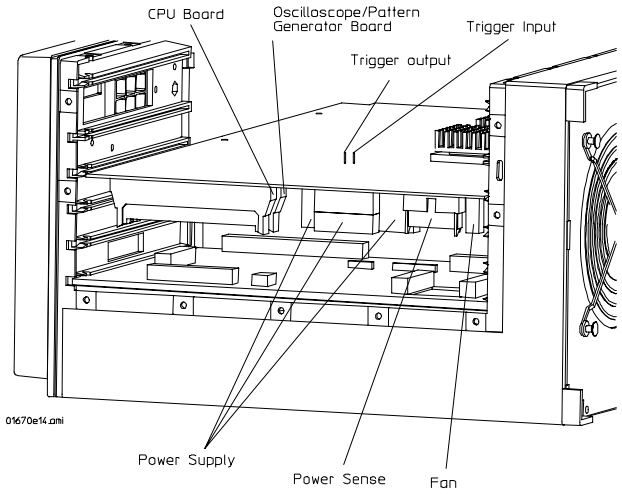
When reconnecting the cables, the ribbon cable from the CPU Board to the Acquisition Board must not be connected to J12. This cable goes from the CPU Board to J13 (at the edge of the Acquisition Board). If the cable is connected to J12 on the Acquisition Board equipment damage will occur.

Bottom of the acquisition board

- Power Sense
- Fan
- Power Supply
- CPU Board
- Oscilloscope or Pattern Generator Board (if installed)

Top of the acquisition board

- Trigger input (white wire to J6)
- Trigger output (orange wire to J5)



3 Remove the acquisition board.

a Remove six screws that secure the acquisition board to the deck.

b Angle the front edge of the acquisition board up out of the chassis.

When installing the acquisition board, ensure the two vertical tabs (one on each side of the probe cable connectors) are inserted into the slots of the rear panel. These tabs act as a pivot point when angling the acquisition board onto the deck.

c Remove the acquisition board up and out of the chassis.

4 If needed, remove the deck from the chassis.

a Remove two screws that secure the deck to the handle brace.

b Remove one screw that secures the deck to the rear panel.

c Slide the deck out of the fourth slot of the chassis.

5 Reverse this procedure to install the acquisition board.

CAUTION

When reconnecting the cables, the ribbon cable from the CPU Board to the Acquisition Board must not be connected to J12. This cable goes from the CPU Board to J13 (at the edge of the Acquisition Board). If the cable is connected to J12 on the Acquisition Board equipment damage will occur.

Check that the following assemblies are properly installed before installing the acquisition board.

- LCD Display
- Front Panel
- Power Supply
- Oscilloscope or Pattern Generator Board (if installed)
- Rear Panel

To remove and replace the CPU board

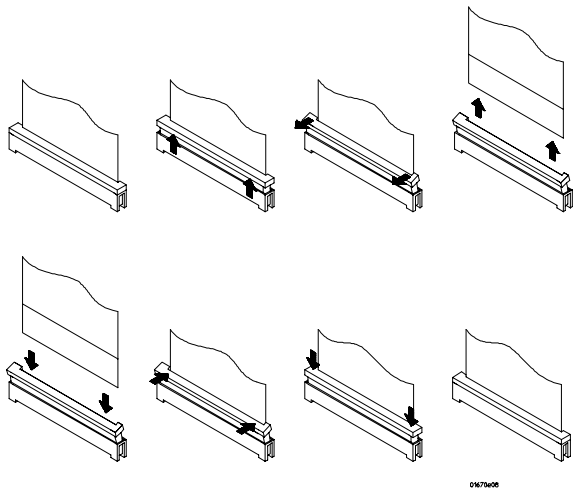
1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Acquisition Board

2 Disconnect the following cables from the CPU board:

CAUTION When reconnecting the cables, the ribbon cable from the CPU Board to the Acquisition Board must not be connected to J12. This cable goes from the CPU Board to J13 (at the edge of the Acquisition Board). If the cable is connected to J12 on the Acquisition Board equipment damage will occur.

- Rear Panel (J5)
- LCD Data (J4)



Removing the LCD data cable from the CPU board

- LCD Inverter (J3)
- GPIB (J13)
- RS-232 (J8)
- Front Panel (J7)

3 Slide the board out the side of the instrument.

4 Reverse this procedure to install the CPU board.

When connecting the LCD data cable to the CPU board, ensure the blue side of the cable faces away from the SIMM memory.

CAUTION When reconnecting the cables, the ribbon cable from the CPU Board to the Acquisition Board must not be connected to J12. This cable goes from the CPU Board to J13 (at the edge of the Acquisition Board). If the cable is connected to J12 on the Acquisition Board equipment damage will occur.

Check that the following assemblies are properly installed before installing the CPU board:

- LCD Display
- Front Panel
- Power Supply
- Oscilloscope/Pattern Generator Board (if installed)

After replacing the CPU board, you will have to restore the ether address in the CPU board. Follow the procedure "The Ether Address" in chapter 5.

To remove and replace SIMM memory

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Acquisition Board
- CPU Board

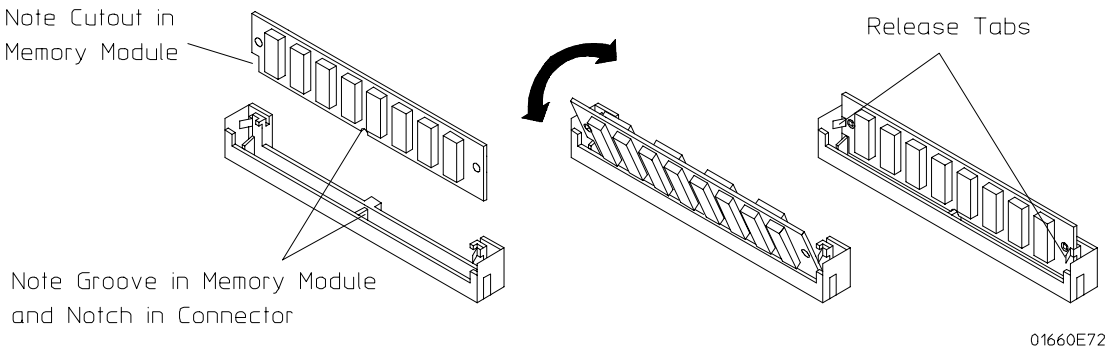
WARNING

Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before servicing the instrument.

2 Hold the release tabs away from the SIMM (single inline memory module), then pull the module out.

3 Reverse this procedure to install a replacement SIMM.

Slide the SIMM module into the connector at an angle, then push it down parallel to the CPU board.



To remove and replace the rear panel

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Acquisition Board
2. Disconnect the RS-232-C and GPIB cables from the CPU board.
3. Disconnect the I/O cable from the CPU board.
   a. For the Agilent 1670G-series Logic Analyzers with the oscilloscope option, remove the hex nut and lock washer from the BNC Cal port.
   b. For the Agilent 1670G-series Logic Analyzers with the pattern generator option, disconnect the pattern generator cable from the pattern generator board.
4. Remove the seven rear panel screws.
5. Lift the rear panel away from the chassis.
6. Reverse this procedure to install the rear panel.

   Check that the following assemblies are properly installed before installing the rear panel:
   - Power Supply
   - Oscilloscope Board (oscilloscope option only)
   - Pattern Generator Board (pattern generator option only)

   When installing the rear panel, check that the alignment tabs on the acquisition board are lined up with the corresponding holes in the rear panel. Also, for the Agilent 1670G-series Logic Analyzers with the pattern generator option, ensure the ground springs are installed on the acquisition board and on the pattern generator board before installing the rear panel.

To remove and replace the power supply

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Acquisition Board
- CPU Board
- Rear Panel

WARNING

Hazardous voltages exist on the power supply. To avoid electrical shock, disconnect the power from the instrument before performing the following procedures. After disconnecting the power, wait at least three minutes for the capacitors to discharge before continuing.

2 Disconnect the power switch cable from the power supply power on/off connector.

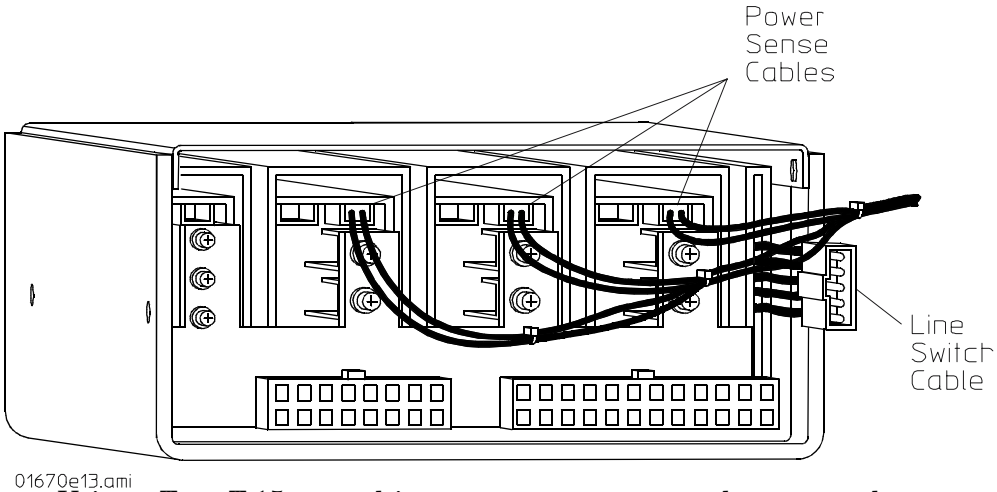
3 Using a Torx T-15 screwdriver, remove two screws on the bottom toward the front of the instrument that secure the power supply to the bottom of the chassis..

4 Loosen the remaining two T-15 screws on the bottom toward the rear of the instrument.

5 Slide the power supply toward the rear of the instrument approx. 12 mm (1/2) inch), then lift the power supply out of the chassis

6 Unplug the power supply output cables and power sense cables from the power supply.

When installing the power sense cable, ensure each cable is plugged onto the correct connectors of the power supply.



7 Using a Torx T-15 screwdriver, remove two screws that secure the power supply bracket to the power supply.

Reverse this procedure to install the power supply.

Check that the LCD Display is properly installed before installing the power supply.

To remove and replace the oscilloscope board (oscilloscope option only)

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Rear Panel
   - Disk Drive Assembly
   - Acquisition Board
   - Power Supply
2. Remove the hex nut from the oscilloscope input attenuators on the lower front panel.
3. Slide the mounting plate out the rear of the instrument.

   Verify that the cable release tabs are down to slide the mounting plate out, then slide the mounting plate toward the rear out of the chassis.
4. Remove the oscilloscope board.
   a. Disconnect the acquisition board-oscilloscope board interface cable from the oscilloscope board. To do this press down on the cable release tabs on the cable socket located on the board.
   b. Remove the screw at the center of the oscilloscope board that secures the board to the mounting plate.
   c. Slide the board approximately 0.5 cm and lift the board off the mounting plate.
5. Remove the attenuators from the oscilloscope board by removing the mounting screws (two per attenuator) from the underside of the board. Then carefully lift the attenuator straight off of the board.
6. Reverse this procedure to install the oscilloscope board.

   When installing the mounting plate, check that the alignment tabs on the mounting plate are installed in the alignment holes in the inside bottom, front of the chassis.

To remove and replace pattern generator board (pattern generator option only)

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Rear Panel
   - Disk Drive Assembly
   - Acquisition Board
   - Power Supply
2. Slide the mounting plate out the rear of the instrument.

   Verify that the cable release tabs are down to slide the mounting plate out, then slide the mounting plate toward the rear out of the chassis.
3. Separate the pattern generator board from the mounting plate by removing the screw at the center of the board. Remove the pattern generator-to-acquisition board cable.
   a. Disconnect the acquisition board-pattern generator board interface cable from the pattern generator board. To do this press down on the cable release tabs on the cable socket located on the board.
   b. Remove the screw at the center of the pattern generator board that secures the board to the mounting plate.
   c. Slide the board approximately 0.5 cm and lift the board off the mounting plate.
4. Reverse this procedure to install the pattern generator board.

   When installing the mounting plate, check that the alignment tabs on the mounting plate are installed in the alignment holes in the inside bottom, front of the chassis.

To remove and replace the front panel and keyboard

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Acquisition Board
   - CPU Board
2. Remove the four screws connecting the front panel.
3. Slide the front panel assembly out the front of the instrument.
4. Slide the spacer out the front of the instrument to remove it.

   Older units have copper ground strips on the spacer. Be careful not to lose the strips.

   When installing the spacer, insert the pins of the spacer in the appropriate holes in the chassis. You can hold the spacer in place while installing the front panel by holding it with your finger through the disk drive mounting slot in the chassis.
5. Remove the RPG knob by pulling the knob off the RPG shaft.
6. Disassemble the front panel assembly by lifting the keyboard circuit board away from the front panel.
7. Lift the elastomeric keypad out of the front panel.
8. Reverse this procedure to assemble and install the front panel assembly.

   When assembling the front panel, check that the holes in the elastomeric keypad and the keyboard circuit board align with the pins on the front panel.

To remove and replace the LCD display and Inverter board

1 Using previous procedures, remove the following assemblies:

- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Acquisition Board
- CPU Board
- Rear Panel
- Power Supply

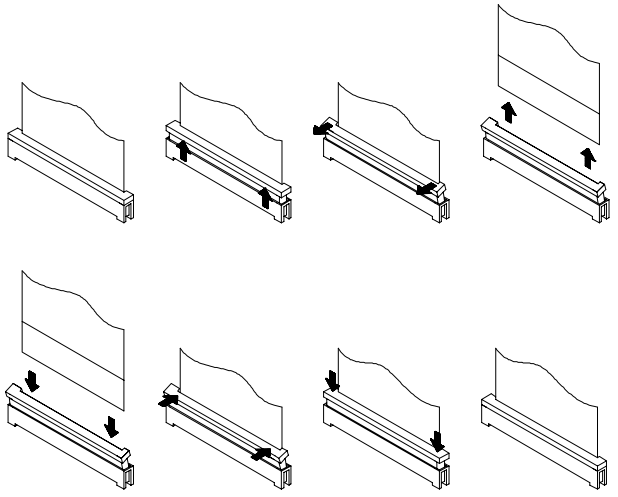
WARNING

Hazardous voltages exist on the LCD Inverter. To avoid electrical shock, disconnect power from the instrument before performing the following procedure. After disconnecting the power, wait at least three minutes for the capacitors in the power supply to discharge before servicing the instrument.

2 Remove the LCD display

a. Disconnect the LCD data cable from the connector on back of the LCD display.

Removing/replacing the LCD data cable at the CPU board



b On the LCD display, disconnect the two cables from the LCD Inverter.

c Remove the two screws from the side of the LCD display. As you face the back of the LCD display, the screws are on the right side.

d Slide the LCD display slightly to the right and remove it.

When connecting the LCD data cable to the LCD display, ensure the blue side of the cable faces toward the LCD display.

3 Remove the Inverter Board
   a Disconnect the CPU Inverter Cable from the Inverter Board.
   b Remove two screws that secure the LCD Inverter to the bezel.
   c Remove the inverter board from the bezel.

   The LCD display and inverter are replaced as one unit.

4 If the lens needs to be removed, remove the four screws that secure the bezel to the chassis. Remove the bezel from the chassis.

   The lens is attached to the bezel with a foam gasket. If the lens must be replaced, remove it from the bezel.

To remove and replace the handle plate

1 Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Acquisition Board

2 Remove the four screws that attach the handle plate to the chassis.

3 Remove the handle plate.

   To remove the handle plate, align the plate toward the front of the instrument, then move it up and out of the instrument.

4 Reverse this procedure to install the handle plate.

To remove and replace the fan

1 Using previous procedures, remove the following assemblies:
- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Acquisition Board
- Rear Panel

2 Note the orientation of the fan cable and the air flow arrow on the fan.

3 Remove the four fan screws from their plastic push fasteners.

4 Remove four plastic push fasteners.

5 Lift the fan away from the rear panel.

6 Lift the fan guard away from the rear panel.

7 Reverse this procedure to install the fan.

When installing the fan, position it with its cable nearest the fan connector feedthrough hole. The airflow arrow on the fan must point in. If you mount the fan backwards, the instrument will overheat.

To remove and replace the pattern generator cables (pattern generator option only)

1 Using the previous procedures, remove the following assemblies:
- Handle
- Rear Feet
- Cover
- Disk Drive Assembly
- Acquisition Board
- CPU Board

2 Remove the two screws securing the pattern generator cable clamp to the rear panel and remove the cable clamp.

3 Disconnect the faulty cable from the pattern generator board and feed the cable through the rear panel.

4 Reverse this procedure to install the replacement cable.

To remove and replace the GPIB and RS-232-C cables

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Acquisition Board
   - Rear Panel
2. Remove the two hex standoffs connecting the GPIB cable, then slide the GPIB cable forward and out of the rear panel.
3. Remove the two hex standoffs connecting the RS-232-C cable, then slide the RS-232-C cable forward and out of the rear panel.
4. Reverse this procedure to install the GPIB and RS-232-C cables.

To remove and replace the I/O board

1. Using previous procedures, remove the following assemblies:
   - Handle
   - Rear Feet
   - Cover
   - Disk Drive Assembly
   - Acquisition Board
   - Rear Panel
2. Remove two jackscrews that attach the parallel printer (Centronics) port to the rear panel.
3. Remove four screws that secure the I/O board to the rear panel.
4. Reverse this procedure to install the I/O board onto the rear panel.

To return assemblies

Before shipping the logic analyzer or assemblies to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details.

1. Write the following information on a tag and attach it to the part to be returned.
   - Name and address of owner
   - Model number
   - Serial number
   - Description of service required or failure indications
2. Remove accessories from the logic analyzer.

   Only return accessories to Agilent Technologies if they are associated with the failure symptoms.
3. Package the logic analyzer.

   You can use either the original shipping containers, or order materials from an Agilent Technologies Sales Office.

CAUTION For protection against electrostatic discharge, package the logic analyzer in electrostatic material.

4. Seal the shipping container securely, and mark it FRAGILE.

7

Replaceable Parts Ordering 7–2
Replaceable Parts List 7–3
Exploded View 7–4
Power Cables and Plug Configurations 7–8

Replaceable Parts

Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your logic analyzer.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and there are no invoices.

For Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. Addresses and telephone numbers are located in a separate document at the back of the service guide.

Exchange Assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also "To return assemblies," in chapter 6.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

The exploded view does not show all of the parts in the replaceable parts list.

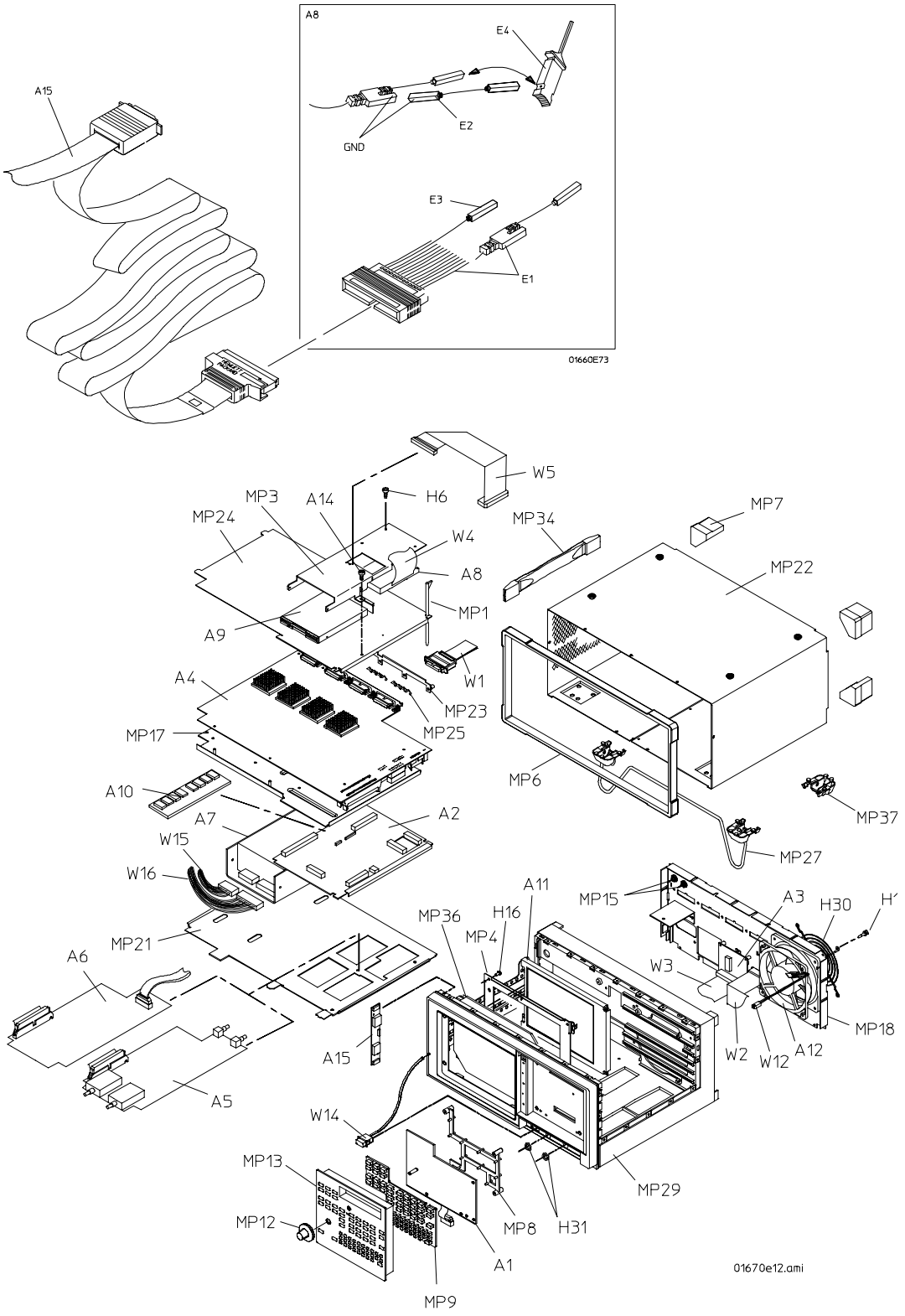
Information included for each part on the list consists of the following:

- Reference designator
- Agilent Technologies part number
- Total quantity included with the instrument (Qty)
- Description of the part

Reference designators used in the parts list are as follows:

- A Assembly
- E Miscellaneous Electrical Part
- F Fuse
- H Hardware
- MP Mechanical Part
- W Cable

Exploded View



Exploded view of the Agilent 1670G-series logic analyzer.

Agilent 1670-Series Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
			Exchange Assemblies
	01660-69529		Exchange Board Assembly-CPU
	01670-695130		Exchange Board Assembly-ACQ 136 CH X 64K (Agilent 1670G)
	01670-695131		Exchange Board Assembly-ACQ 96 CH x 1024K (Agilent 1671G)
	01670-695132		Exchange Board Assembly-ACQ 64 CH x 1024K (Agilent 1672G)
	01670-695140		Exchange Board Assembly-ACQ 102 CH X 64K (Agilent 1671G)
	01670-695141		Exchange Board Assembly-ACQ 102 CH X 256K (Agilent 1671G #001)
	01670-695142		Exchange Board Assembly-ACQ 102 CH X 2M (Agilent 1671G #002)
	01670-695150		Exchange Board Assembly-ACQ 68 CH X 64K (Agilent 1672G)
	01670-695151		Exchange Board Assembly-ACQ 68 CH X 256K (Agilent 1672G #001)
	01670-695152		Exchange Board Assembly-ACQ 68 CH X 2M (Agilent 1672G #002)
	01670-695160		Exchange Board Assembly-ACQ 34 CH X 64K (Agilent 1672G)
	01670-695161		Exchange Board Assembly-ACQ 34 CH X 256K (Agilent 1672G #001)
	01670-695162		Exchange Board Assembly-ACQ 34 CH X 2M (Agilent 1672G #002)
	01660-69527		Exchange Board Assembly-2 Gsa/s Oscilloscope (Option #003)
	54512-69402		Exchange Assembly-Attenuator (Option #003)
			Replacement Parts
A1	01660-66502	1	Board Assembly-Keyboard
A2	01660-66529	1	Board Assembly - CPU
A3	01660-66516	1	Board Assembly-I/O
A4	01670-665130	1	Board Assembly-ACQ 136 CH X 64K (Agilent 1670G)
A4	01670-665131	1	Board Assembly-ACQ 136 CH X 256K (Agilent 1670G #001)
A4	01670-665132	1	Board Assembly-ACQ 136 CH X 2M (Agilent 1670G #002)
A4	01670-665140	1	Board Assembly-ACQ 102 CH X 64K (Agilent 1671G)
A4	01670-665141	1	Board Assembly-ACQ 102 CH X 256K (Agilent 1671G #001)
A4	01670-665142	1	Board Assembly-ACQ 102 CH X 2M (Agilent 1671G #002)
A4	01670-665150	1	Board Assembly-ACQ 68 CH X 64K (Agilent 1672G)
A4	01670-665151	1	Board Assembly-ACQ 68 CH X 256K (Agilent 1672G #001)
A4	01670-665152	1	Board Assembly-ACQ 68 CH X 2M (Agilent 1672G #002)
A4	01670-665160	1	Board Assembly-ACQ 34 CH X 64K (Agilent 1672G)
A4	01670-665161	1	Board Assembly-ACQ 34 CH X 256K (Agilent 1672G #001)
A4	01670-665162	1	Board Assembly-ACQ 34 CH X 2M (Agilent 1672G #002)
A5	01660-69527	1	Board Assembly-2 Gsa/s Oscilloscope (Option #003, includes attenuators)
A5	54512-63402	2	Attenuator Assembly (Option #003)
A6	01660-66526	1	Board Assembly-Pattern Generator (Option #004)
A7	0950-3403	1	Power Supply
A8	0950-3933	1	Hard Disk Drive
A9	0950-2782	1	Flexible Disk Drive
A10	1818-5623	1	2048K X 32 SIMM
A11	2090-0396	1	LCD Display Assembly
A12	3160-1013	1	Fan-tubeaxial
A13	1150-7846	1	Mouse
A14	01660-66522	1	PC Board Assembly Adapter (Hard Disk Drive)
A15	0950-2888	1	Inverter Board
A16	01650-61608	8	Probe Tip Assembly (1670G)
A16	01650-61608	6	Probe Tip Assembly (1671G)
A16	01650-61608	4	Probe Tip Assembly (1672G)
A16	01650-61608	2	Probe Tip Assembly (1673G)
A17	1160A	2	10:1 Passive Probe (Option #003)
A18	16542-61607	1	Double Probe Adapter
E1	5959-9333		Replacement Probe Leads (5 per package)
E2	5959-9334		Replacement Probe Grounds (5 per package)
E3	5959-9335		Replacement Pod Grounds (2 per package)
E4	5090-4833		Grabber Kit Assembly (20 grabbers per package)
H1	0361-1272	4	Plastic Push Fastener (fan to rear panel)
H2	0380-1482	2	STDF-HEX .34-IN (GPIB Cable)
H3	0380-1927	4	Jackscrew with lock (RS-232, Centronics port to rear panel)
H4	0515-0372	2	M 3.0 x 0.50 8mm (LCD display to display plate)
H5	0515-0390	2	M 4.0 x 0.70 6mm (power supply bracket to power supply)

Agilent 1670-Series Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
H6	0515-0430	24	MSPH M 3.0 x 0.5 6mm (acquisition board to deck, deck to chassis, rear panel to cabinet, PC board adapter to drive bracket, hard disk drive to drive bracket, I/O Board to rear panel
H7	0515-0430	1	MSPH M 3.0 x 0.5 6mm (Option #003, oscilloscope board to PC mounting plate)
H8	0515-0430	3	MSPH M 3.0 x 0.5 6mm (Option #004, pattern generator board to PC mounting plate, cable bracket to rear panel)
H9	0515-0664	4	MSPH M 3.0 x 12.0 SMS10 (rear feet to rear panel)
H10	0515-1031	4	MSFH M 3.0 x 6 T10 (accessory pouch to cover)
H11	0515-1103	2	MSFH M 3.0 x 10 T10 (trim strip, cover to cabinet bottom)
H12	0515-1246	2	MSPH M 3.0 x 0.5 6mm (inverter board to display plate)
H13	0515-1349	4	SM M 3.0 x 0.5 30mm-LG (keyboard assembly to cabinet)
H14	0515-1363	7	MSTH M 3.0 x 5 T10 (BNC shorting cap to rear panel, handle plate to cabinet, disk drive bracket to support tray)
H15	0515-1974	4	MSPH M 2.5 x 0.45 4mm (flexible disk drive to disk drive bracket)
H16	0515-2113	8	M 4.0 x 0.7 8mm (display assembly to cabinet, power supply to cabinet)
H17	0515-2349	5	MS M 3.0 X 0.50 14mm (trim strip cover to cabinet top and sides)
H18	1250-0774	1	BNC Shorting Cap (LAN BNC)
H19	1252-5894	5	Socket Retainer Clip (Option #004, pattern generator cables)
H20	1252-7017	1	Socket Retainer Clip (I/O cable to I/O board)
H21	1400-0611	1	Cable Clamp (Inverter cable secure to power supply)
H22	1400-1779	1	Cable Clamp (power supply cables secure to power supply bracket)
H23	1400-2209	0.04	Cable Tie (Option #003, pattern generator cables)
H24	2190-0009	2	WIL.168 .340 .02 (GPIB cable to rear panel)
H25	2190-0016	2	WIL.377 .507 .02 (Trigger In and Out BNC to rear panel)
H26	2950-0001	2	NUTH 3/8-32 .093 (Trigger In and Out BNC to rear panel)
H27	2190-0068	1	WIL.505 .630 .02 (Option #003, oscilloscope trigger BNC to rear panel)
H28	2950-0054	1	NUTH 1/2-28 .125 (Option #003, oscilloscope trigger BNC to rear panel)
H29	3050-0010	4	WFL.147 .312 .03 (rear feet to rear panel)
H30	3160-0092	1	Fan Guard
H31	54503-25701	2	Hex Nut (Option #003, attenuator to front panel)
MP1	01650-46101	2	Locking Pin PCB
MP2	01650-94309	1	Probe Label (Option #004)
MP3	01660-01213	1	Disk Drive Bracket
MP4	01660-04107	1	Display Plate
MP5	01660-09101	2	Ground Spring (Option #004)
MP6	01660-40503	1	Trim Strip
MP7	01660-40504	4	Rear Foot
MP8	01660-40505	1	Front Panel Spacer
MP9	01660-41903	1	Keypad (all except Option #003)
MP10	01660-41904	1	Keypad (Option #003)
MP11	01660-44703	1	Keyboard Spacer
MP12	01660-47402	1	RPG Knob
MP13	01660-60006	1 0 0	Assembled Keyboard Panel and Label
MP14	01660-61203	1	Cable Clamp (Option #004)
MP15	01660-67601	2	BNC Connector Assembly
MP16	01660-94315	1	Pod and Cable Label
MP17	01670-00101	1	Deck
MP18	01670-00202	1	Rear Panel (all except Option #003, #004)
MP18	01670-00203	1	Rear Panel (Option #003)
MP18	01670-00204	1	Rear Panel (Option #004)
MP19	01670-01204	1	Handle Brace
MP20	01670-01206	1	Cable Bracket
MP21	01670-04104	1	PC Mounting Plate
MP22	01670-60003	1	Cover Assembly with Feet
MP23	01670-04109	1	Probe Mounting Plate (Agilent 1670G)
MP23	01670-04108	1	Probe Mounting Plate (Agilent 1671G)
MP23	01670-04107	1	Probe Mounting Plate (Agilent 1672G)
MP23	01663-04101	1	Probe Mounting Plate (Agilent 1673G)
MP24	01670-04701	1	Support Tray
MP25	01670-09101	4	Ground Spring (Agilent 1670G)
MP25	01670-09101	3	Ground Spring (Agilent 1671G)

Agilent 1670-Series Replaceable Parts

Ref. Des.	Agilent Part Number	QTY	Description
MP25	01670-09101	2	Ground Spring (Agilent 1672G)
MP25	01670-09101	1	Ground Spring (Agilent 1673G)
MP26	01670-01206	1	Power Supply Bracket
MP27	01670-23701	1	Tilt Stand
MP28	01670-45401	1	Insulator-PC Board (Option #003, #004)
MP29	01670-60101	1	Chassis Assembly
MP30	01670-94304	1	Line Switch Label (all except Option #003)
MP30	01670-94305	1	Line Switch Label (Option #003)
MP31	01670-94306	1	ID Label (Agilent 1670G)
MP31	01671-94304	1	ID Label (Agilent 1671G)
MP31	01672-94304	1	ID Label (Agilent 1672G)
MP31	01673-94304	1	ID Label (Agilent 1673G)
MP32	1250-1454	1	Adapter, BNC to Probe (Option #003)
MP33	16500-41201	5	Ribbon Cable ID Clip (Option #004)
MP34	16600-68707	1	Handle Assembly
MP34	54801-24702	0	Spacer
MP34	54810-44901	0	Handle
MP34	54810-45001	0	End Cap
MP34	5021-4309	0	Machine Screw
MP35	16700-84501	1	Accessory Pouch
MP36	54542-48001	1	Glass Lens (Protects LCD Display)
MP37	54810-61001	4	Bottom Foot
W1	16710-61603	4	Probe Cable (Agilent 1670G)
W1	16710-61603	3	Probe Cable (Agilent 1671G)
W1	16710-61603	2	Probe Cable (Agilent 1672G)
W1	16710-61603	1	Probe Cable (Agilent 1673G)
W2	01660-61601	1	RS-232-C Cable
W3	01660-61611	1	I/O Board Cable
W4	01660-61615	1	Hard Disk Drive Cable
W5	01660-61616	1	Flexible Disk Drive Cable
		1	
W7	01660-61618	1	Display Cable
W8	01660-61619	1	Inverter Cable
W9	01670-61601	1	CPU Cable
W10	01670-61602	1	Cable-60 Conductor (Option #003, #004)
W11	01670-61603	1	Power Supply Sense Cable
W12	01670-61604	1	Fan Cable
W13	01670-61605	1	GPIB CABLE
W14	01670-61606	1	Power Switch Cable
W15	01670-61607	1	Power Supply Cable-24 Conductor
W16	01670-61608	1	Power Supply Cable-16 Conductor
W17	01670-61609	1	Jumper Cable - orange
W18	01670-61610	1	Jumper Cable - white
W19	16522-61601	4	Output Cable (Option #004)
W20	16522-61602	1	Clock Cable (Option #004)
W21	8120-1521		Power Cord-United States (7.5 ft)
W21	8120-1703		Power Cord (Option #900-UK)
W21	8120-0696		Power Cord (Option #901-Austl)
W21	8120-1692		Power Cord (Option #902-Europe)
W21	8120-2296		Power Cord (Option #906-Swit)
W21	8120-2957		Power Cord (Option #912-Den)
W21	8120-4600		Power Cord (Option #917-Africa)
W21	8120-4754		Power Cord (Option #918-Japan)
W21	8120-6799		Power Cord (Option #919-Israel)
W21	8120-6871		Power Cord (Option #920-Argentina)
W21	8120-6979		Power Cord (Option #921-Chile)
W21	8120-8377		Power Cord (Option #922-China)

Power Cables and Plug Configurations

This instrument is equipped with a three-wire power cable. The type of power cable plug shipped with the instrument depends on the country of destination. The W 21 reference designators (table, previous page) show option numbers of available power cables and plug configurations.

8

Block-Level Theory 8-3
The Agilent 1670G-Series Logic Analyzer 8-3
The Logic Acquisition Board 8-7
The Oscilloscope Board 8-10
The Pattern Generator Board 8-13
Self-Tests Description 8-15
Power-up Self-Tests 8-15
System Tests (SysPV) 8-16
Analyzer Tests (Analy PV) 8-19
Oscilloscope tests (Scope PV) 8-22
Pattern Generator tests (Patt Gen) 8-23
GPIB 8-27
RS-232-C 8-29

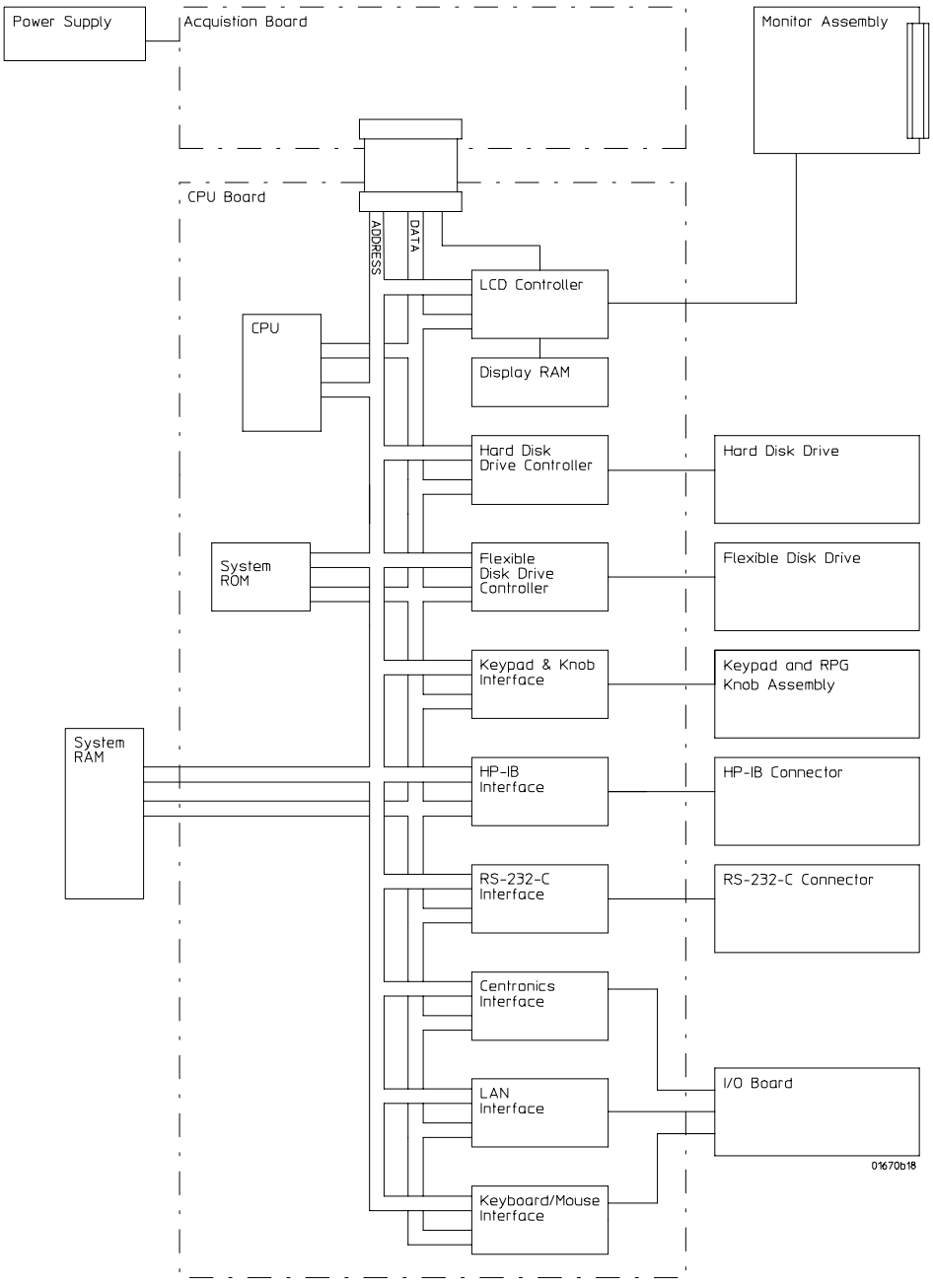
Theory of Operation

Theory of Operation

This chapter tells the theory of operation for the logic analyzer and describes the self-tests. The information in this chapter will help you understand how the logic analyzer operates and what the self-tests are testing. This information is not intended for component-level repair.

The block-level theory is divided into two parts: theory for the logic analyzer and theory for the acquisition boards. A block diagram is shown with each theory.

The Agilent 1670G-Series Logic Analyzer



Agilent 1670G Logic Analyzer Block Diagram

Agilent 1670G-Series Logic Analyzer Theory

CPU Board

The microprocessor is a Motorola 68EC020 running at 25 MHz. The microprocessor controls all of the functions of the logic analyzer including processing and storing data, displaying data, and configuring the acquisition ICs to obtain and store data.

System Memory

The system memory is made up of both read-only memory (ROM) and random access memory (RAM). Two types of ROM are used. A single 128Kx8 EPROM is used as a boot ROM, and four 512Kx8 flash ROMS are configured to provide a 256Kx32 flash ROM space. One 1Mx4byte SIMM provides 8MB RAM space.

On power-up, instructions in the boot ROM command the instrument to execute its boot routine. The boot routine includes power-up operation verification of the instrument subsystems and entering the operating system. The CPU searches for the operating system on flash ROM. Then, if the operating system is in flash ROM, the instrument will be initialized with the default configuration and await front panel instructions from you. If the operating system is not in flash ROM, the CPU accesses the disk drive to see if the operating system is on the disk.

The DRAM stores the instrument configuration, acquired data to be processed, and any inverse assembler loaded in the instrument by the user.

LCD Display Controller and Display RAM

Two RAMDAC ICs store the video information, then supply the data to a proprietary color palette. A video frame generator IC provides the sync signal to the display to create new frames.

Disk Drive Controller

The disk drive controller consists of a single floppy drive controller IC. The floppy drive controller provides all signals to the disk drive including read and write data, read and write signals, write gate, and step signal. The floppy drive controller also reads status signals from the disk drive, including a track 00 signal, disk ready, and disk change signal.

Keypad and Knob Interface

The front panel keypad is scanned directly from the microprocessor address bus during the video blanking cycle of the CRT. When a front panel key is pressed the associated address bits are fed to the data bus through the pressed key and read by the microprocessor.

The rotary pulse generator (RPG) knob has its own interface circuit. Pulses and direction of rotation information are directed to the RPG interface. The microprocessor then reads and interprets the RPG signals and performs the desired tasks.

GPIB Interface

The instrument interfaces to GPIB as defined by IEEE Standard 488.2. The interface consists of an GPIB controller and two octal drivers/receivers. The microprocessor routes GPIB data to the controller. The controller then buffers the 8-bit GPIB data bits and generates the bus handshaking signals. The data and handshaking signals are then routed to the GPIB bus through the octal line drivers/receivers. The drivers/receivers provide data and control signal transfer between the bus and controller.

RS-232-C Interface

The instrument RS-232-C interface is compatible with standard RS-232-C protocol. The interface consists of a controller, and drivers/receivers. The controller serializes parallel data from the microprocessor for transmission. At the same time the controller also receives serial data and converts the data to parallel data characters for the microprocessor.

The controller contains a baud rate generator that can be programmed from the logic analyzer front panel for one of eight baud rates. Other RS-232-C communications parameters can also be programmed from the logic analyzer front panel.

The drivers/receivers interface the instrument with data communications equipment. Slew rate control is provided on the ICs eliminating the need for external capacitors.

LCD Display Assembly

The LCD display is a Mitsubishi 8.4-inch industrial-quality TFT active display. 6 bits of display data from the CPU board result in a 640x480 VGA resolution at the display.

Flexible Disk Drive

The disk drive assembly is a high density disk drive that formats double-sided, double-density or high-density disks in LIF or DOS format. A disk drive controller on the CPU board controls the disk drive. Signals are routed directly to the disk drive through the disk drive cable.

Power Supply

A low voltage power supply provides all dc voltages needed to operate the logic analyzer. The power supply also provides the +5 Vdc voltage to the probe cables to power logic analyzer accessories and analysis probes.

Unfiltered voltages of +12 V, -12 V, +5 V, -5.2 V, and +3.5 V are supplied to the acquisition board where they are filtered and distributed to the CPU board, CRT Monitor Assembly, and probe cables.

Centronics Interface

The interface to the Centronics port includes latches and buffers. The latches and buffers convert the logic analyzer backplane signals into parallel Centronics signals.

LAN Interface

The LAN Interface is primarily a single LAN integrated circuit with supporting components. Isolation circuitry for the LAN port is included on the I/O board.

Keyboard/Mouse Interface

An 82C42PC PS2 controller makes up the PS2 Keyboard/Mouse interface. The PS2 controller interfaces the logic analyzer backplane with the keyboard and/or mouse devices.

I/O Board

The Input/Output (I/O) Board primarily includes a Centronics port and two mini-DIN (PS2) ports for the base 1670G-series products. The I/O board also includes isolation circuitry for the LAN.

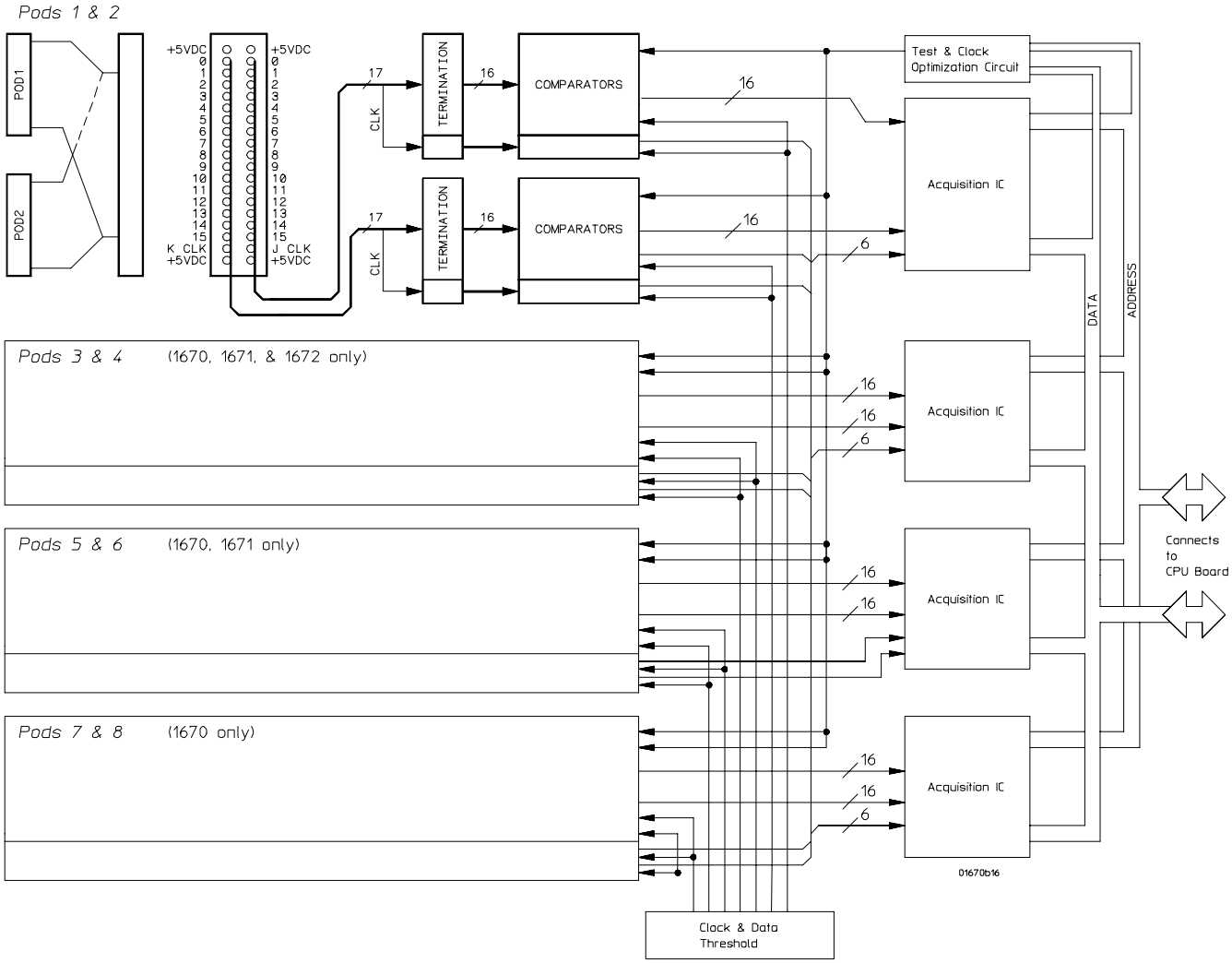
Hard Disk Drive Interface

Buffers interface the hard disk drive with the logic analyzer backplane.

Hard Disk Drive

The Hard Disk Drive is an IDE-compatible disk drive. A 40-pin IDE connector allows the disk drive to interface with the logic analyzer backplane through the hard disk drive interface.

The Logic Acquisition Board



Logic Acquisition Board Block Diagram

Logic Acquisition Board Theory

Probing

The probing circuit includes the probe cable and terminations. The probe cable consists of two 17-channel pods which are connected to the circuit board using a high-density connector. Sixteen single-ended data channels and one single-ended clock/data channel are passed to the circuit board per pod.

If the clock/data channel is not used as a state clock in state acquisition mode, it is available as a data channel. The clock/data channel is also available as a data channel in timing acquisition mode. Eight (Agilent 1670G), six (Agilent 1671G), or four (Agilent 1672G) clock/data channels are available as data channels, however there is a maximum of four clock/data channels available as clock channels.

The cables use nichrome wire woven in polyarmid yarn for reliability and durability. The pods also include one ground path per channel in addition to a pod ground. The channel grounds are configured such that their electrical distance is the same as the electrical distance of the channel.

The probe tip assemblies and termination modules connected at the end of the probe cables have a divide-by-10 RC network that reduces the amplitude of the data signals as seen by the circuit board. This adds flexibility to the types of signals the circuit board can read in addition to improving signal integrity.

The terminations on the circuit board are resistive terminations that reduce transmission line effects on the cable. The terminations also improve signal integrity to the comparators by matching the impedance of the probe cable channels with the impedance of the signal paths of the circuit board. All 17 channels of each pod are terminated in the same way. The signals are reduced by a factor of 10.

Comparators

Two proprietary 9-channel comparators per pod interpret the incoming data and clock signals as either high or low depending on where the user-programmable threshold is set. The threshold voltage of each pod is individually programmed, and the voltage selected applies to the clock channel as well as the data channels of each pod.

Each of the comparator ICs has a serial test input port used for testing purposes. A test bit pattern is sent from the Test and Clock Synchronization Circuit to the comparator. The comparators then propagate the test signal on each of the nine channels of the comparator. Consequently, all data and clock channel pipelines on the circuit board can be tested by the operating system software from the comparator.

Acquisition

The acquisition circuit is made up of a single Agilent proprietary ASIC. Each ASIC is a 34-channel state/timing analyzer, and one such ASIC is included for every two logic analyzer pods. All of the sequencing, pattern/range recognition, and event counting functions are performed on board the IC.

In addition to the storage qualification and counting functions, the acquisition ASICs also perform master clocking functions. All four state acquisition clocks are fed to each IC, and the ICs generate their own sample clocks. Every time you select RUN, the ICs individually perform a clock optimization before data is stored.

Clock optimization involves using programmable delays on board the IC to position the master clock transition where valid data is captured. This procedure greatly reduces the effects of channel-to-channel skew and other propagation delays.

In the timing acquisition mode, an oscillator-driven clock circuit provides a four-phase, 125-MHz clock signal to each of the acquisition ICs. For high speed timing acquisition (125 MHz and faster), the sample period is determined by the four-phase, 125-MHz clock signal.

For slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The sample clock is then fed to all acquisition ICs.

Threshold

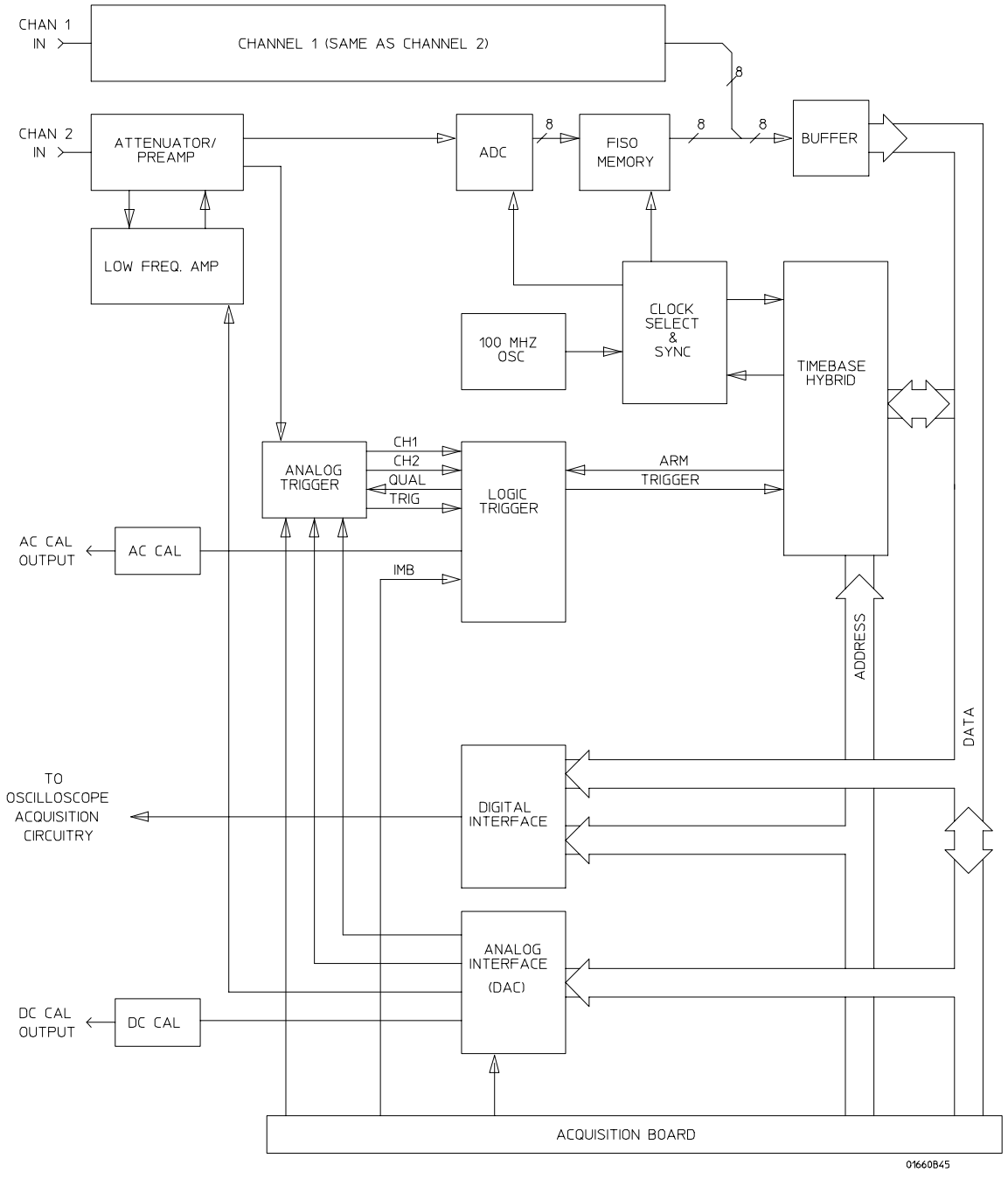
A precision octal DAC and precision op amp drivers make up the threshold circuit. Each of the eight channels of the DAC is individually programmable which allows you to set the thresholds of the individual pods. The 16 data channels and the clock channel of each pod are all set to the same threshold voltage.

Test and Clock Synchronization Circuit

ECLinPS ICs are used in the Test and Clock Synchronization Circuit for reliability and low channel-to-channel skew. Test patterns are generated and sent to the comparators during software operation verification. The test patterns are propagated across all data and clock channels and read by the acquisition ASIC to ensure both the data and clock pipelines are operating correctly.

The Test and Clock Synchronization Circuit also generates a four-phase, 125-MHz sample/synchronization signal for the acquisition ICs operating in the timing acquisition mode. The synchronizing signal keeps the internal clocking of the individual acquisition ASICs locked in step with the other ASICs at fast sample rates. At slower sample rates, one of the acquisition ICs divides the 125-MHz clock signal to the appropriate sample rate. The slow speed sample clock is then used by all acquisition ICs.

The Oscilloscope Board



Oscilloscope Board Block Diagram

Oscilloscope Board Theory (oscilloscope option only)

Attenuator/Preamp Theory of Operation

The channel signals are conditioned by the attenuator/preamps, thick film hybrids containing passive attenuators, impedance converters, and a programmable amplifier. The channel sensitivity defaults to the standard 1-2-4 sequence (other sensitivities can be set also). However, the firmware uses passive attenuation of 1, 5, 25, and 125, with the programmable preamp, to cover the entire sensitivity range.

The input has a selectable 1 MΩ input impedance with ac or dc coupling or a 50Ω input impedance with dc coupling. Compensation for the passive attenuators is laser trimmed and is not adjustable. After the passive attenuators, the signal is split into high-frequency and low-frequency components. Low frequency components are amplified on the main assembly, where they are combined with the offset voltage. The ac coupling is implemented in the low frequency amplifier.

The high- and low-frequency components of the signal are recombined and applied to the input FET of the preamp. The FET provides a high input impedance for the preamp. The programmable preamp adjusts the gain to suit the required sensitivity and provides the output signal to the main assembly. The output signal is then sent to both the trigger circuitry and ADC.

Oscilloscope Acquisition

The acquisition circuitry provides the sampling, digitizing, and storing of the signals from the channel attenuators. The channels are identical. Trigger signals from each channel and the external triggers synchronize acquisition through the time base circuitry. A 100 MHz oscillator and a time base provide system timing and sample clocking. A voltage-controlled oscillator (VCO), frequency divider, and digital phase detector provide the sample clock for higher sample rates. After conditioning and sampling, the signals are digitized, then stored in a hybrid IC containing a FISO (fast in, slow out) memory.

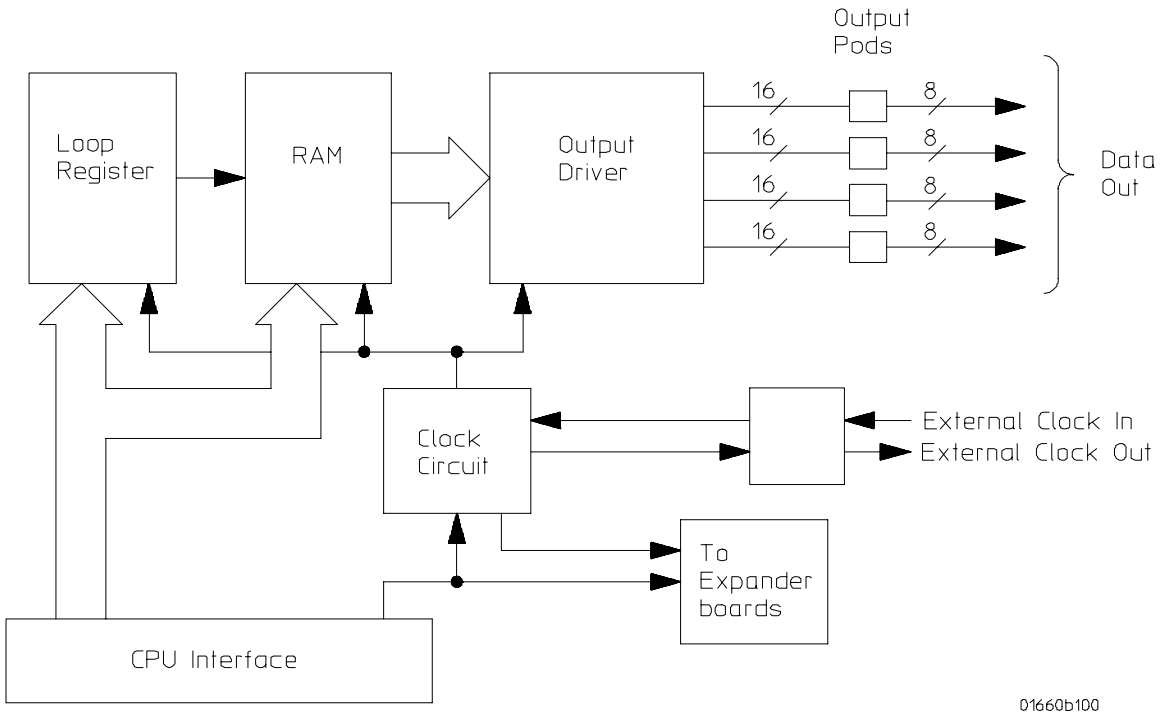
ADC The eight-bit ADC digitizes the channel signal. Digitization is done by comparators in a flash converter. The sample clock latches the digitized value of the input to save it so that it can be sent to memory.

FISO Memory 8000 samples of the FISO (fast in, slow out) memory are used per measurement per channel. Memory positions are not addressed directly. The configuration is a ring which loops continuously as it is clocked. Memory position is tracked by counting clocks. The clocking rate is the same as the ADC, however the clock frequency is half that of the ADC since the FISO clocks on both transitions of the clock period. Data is buffered onto the CPU data bus for processing.

Triggering There are two main trigger circuits that control four trigger sources. The two trigger circuits are the analog trigger and the logic trigger. The analog trigger IC operates as a multichannel Schmidt trigger/comparator. A trigger signal (a copy of the analog input signal) from each of the inputs is directed to the analog trigger IC inputs. The trigger signal is continuously compared with the trigger reference level selected by the user. Once the trigger condition is met, the trigger TRUE signal is fed to the logic trigger, which begins the acquisition and store functions by way of the time base.

The four trigger sources are Channel 1, Channel 2, Intermodule Bus (IMB), and external BNC. The operation of the input channels was discussed previously. The IMB trigger signal is sent directly to the logic trigger. External triggering is provided by the BNC input of the Agilent 1670G-series Logic Analyzer.

Time Base The time base provides the sample clocks and timing necessary for data acquisition. It consists of the 100 MHz reference oscillator and time base hybrid.



The 100 MHz reference oscillator provides the base sample frequency.

The time base hybrid has programmable dividers to provide the rest of the sample frequencies appropriate for the time range selected. The time base uses the time-stretched output of the fine interpolator to time-reference the sampling to the trigger point. The time base has counters to control how much data is taken before (pre-trigger data) and after (post-trigger data) the trigger event. After the desired number of pre-trigger samples has occurred, the Time base hybrid sends a signal to the Logic Trigger (trigger arm) indicating it is ready for the trigger event. When the trigger condition is satisfied, the Logic Trigger sends a signal back to the time base hybrid. The time base hybrid then starts the post-trigger delay counter.

When the countdown reaches zero, the sample clocks are stopped and the CPU is signaled that the acquisition is complete. The Fine Interpolator is a dual-slope integrator that acts as a time-interval stretcher. When the logic trigger receives a signal that meets the programmed triggering requirements, it signals the time base. The time base then sends a pulse to the fine interpolator. The pulse is equal in width to the time between the trigger and the next sample clock. The fine interpolator stretches this time by a factor of approximately 500. Meanwhile, the time base hybrid runs a counter with a clock derived from the sample rate oscillator. When the interpolator indicates the stretch is complete, the counter is stopped. The count represents, with much higher accuracy, the time between the trigger and the first sample clock. The count is stored and used to place the recently acquired data in relationship with previous data.

AC Cal The AC Cal is a multiplexer circuit that can provide several signals to the Probe Compensation/AC Calibrator output on the rear panel. The signal provided depends on the mode of the instrument. It can be either a probe compensation signal, a pulse representing the trigger event, signals used for self-calibration, or the 100 MHz reference oscillator when sample period is 1 ns.

DC Cal The DC Cal output, a rear panel signal, is used for self-calibration. It is one output from the 16-channel DAC.

Digital Interface The Digital Interface provides control and interface between the system control and digital functions in the acquisition circuitry.

Analog Interface The Analog Interface provides control of analog functions in the acquisition circuitry. It is primarily a 16-channel DAC with an accurate reference and filters on the outputs. It controls channel offsets and trigger levels, and provides the DC Cal output.

The Pattern Generator Board

The Pattern Generator Board Block Diagram

Pattern Generator Board Theory (pattern generator option only)

Loop Register

The loop register holds the programmable vector flow information. When the pattern generator reaches the end of the vector listing, the loop register is queried for the RAM address location of the next user-programmed vector. In many cases, the next vector address location would be the start of the vector listing. Consequently the vectors would continue to loop from the end of the listing back to the beginning until the user instructs the module to stop.

RAM

Consisting of six 256Kx16 VRAM ICs and RAM addressing circuitry, the RAM stores the desired patterns that appear at the output. The RAM addressing circuitry is merely a counter which addresses the pattern locations in RAM. When the end of the vector listing is reached, the addressing circuitry is loaded from the loop register with the address of the first vector of the listing to provide an uninterrupted vector loop. The RAM output is sent to the Output Driver circuit where the patterns are presented into a logic configuration usable by the output pods.

Output Driver

The output driver circuit is made up of a series of latch/logic translators and multiplexers. The latch/translators convert the working-level TTL signals to output-level ECL signals for each channel. The ECL-level signals are then directed to the multiplexers.

The multiplexers, one per channel, direct the programmed data patterns to the output channels. The single-ended ECL-level signals are converted to differential signals which are routed to the output cables and to the pods. Note that the differential ECL output signal of the pattern generator module is not suitable to directly drive ECL circuitry.

Clock Circuit

The clock circuit paces the loop register, the RAM address circuitry, and the multiplexers in the output driver according to the desired data rate. A 200 MHz clock source is directed through a divider circuit which provides a 100MHz and 50MHz clock in addition to 200MHz. The 200MHz, 100MHz, 50MHz and external clock signals are routed to a clock select multiplexer. The output of the multiplexer, which represents the user-selected clocking rate, is distributed to the above listed subcircuits on both the master board and all expander boards that are configured with the master board.

The output of the clock select multiplexer is also distributed to an external clock out circuit. The clock signal is routed to a bank of external clock delays, and then to an external clock delay select multiplexer. The output of this multiplexer, which represents the desired clock delay, is directed to the external clock out pin on the clock pod. Consequently, either the internal clock or external clock is redirected to the clock out pin on the clock pod with a user-selected clock delay.

CPU Interface

The CPU interface is a single programmable-logic device which interprets the 1670G-series (with the pattern generator) CPU logic and translates the logic into signals to drive and program the pattern generator module.

Pod

The Clock or Data Pod converts the differential output ECL signal to the logic levels of interest. Because the output of the pattern generator module cannot directly drive ECL circuitry, the Clock and Data Pod is required to interface the pattern generator with the target system.

Self-Tests Descriptions

The self-tests identify the correct operation of major functional areas in the logic analyzer. The self-tests are not intended for component-level diagnostics.

Three types of tests are performed on the Agilent 1670G-series logic analyzers: the power-up self-tests, the functional performance verification self-tests, and the parametric performance verification tests.

The power-up self-tests are performed when power is applied to the instrument.

The functional performance verification self-tests are run using a separate operating system, the performance verification (PV) operating system. The PV operating system resides on a separate disk that must be inserted in the disk drive when running the functional performance verification self-tests. The system and analyzer tests are functional performance verification tests.

Parametric performance verification requires the use of external test equipment that generates and monitors test data for the logic analyzer to read. The performance verification procedures in chapter 3 of this service guide make up the parametric performance verification for the logic analyzer. Refer to chapter 3, "Testing Performance," for further information about parametric performance verification.

Power-up Self-Tests

The power-up self-tests are divided into two parts. The first part is the system memory tests and the second part is the microprocessor interrupt test. The system memory tests are performed before the logic analyzer actually displays the power-up self-test screen. Both the system ROM and RAM are tested during power-up. The interrupt test is performed after the power-up self-test screen is displayed.

The following describes the power-up self-tests:

ROM Test

The ROM test performs several checksum tests on various read only memory elements, including the system ROM as well as the various software modules present in flash ROM.

Passing the ROM test implies that the microprocessor can access each ROM memory address and that each ROM segment provides checksums that match previously calculated values.

RAM Test

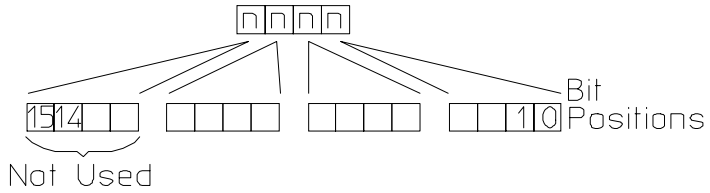
The RAM test checks the video RAM (VRAM), system dynamic RAM (DRAM), and static RAM memory within the real time clock IC. The microprocessor first performs a write/read in each memory location of the VRAM. At each VRAM memory location a test pattern is written, read, and compared. An inverse test pattern is then written, read, and compared. After verifying correct operation of the VRAM, the System RAM and real time clock RAM are tested in a similar fashion.

Passing the RAM test implies that the microprocessor can access each VRAM memory location and that each VRAM memory location can store a logical "1" or a logical "0." If the VRAM is functioning properly, the logic analyzer can construct a correct, undistorted display. Passing the RAM test also implies that the memory locations of system RAM can be accessed by the microprocessor and the data in RAM is intact, and that the memory locations inside the real time clock IC can store a logical "1" or a logical "0."

Interrupt Test

The Interrupt Test checks the microprocessor interrupt circuitry. With all interrupts disabled from their source, the microprocessor waits for a short period of time to see if any of the interrupt lines are asserted. An asserted interrupt line during the wait period signifies incorrect functioning of the device generating the interrupt or the interrupt circuitry itself. Those interrupts that can be asserted under software control are exercised to verify functionality.

Passing the Interrupt Test implies that the interrupt circuitry is functioning properly. Passing the Interrupt Test also implies that the interrupt generating devices are also functioning properly and not generating false interrupts. This means that the microprocessor can execute the operating system code and properly service interrupts generated by pressing a front panel key or receiving an GPIB or RS-232-C command.



16500m05

System Tests (SysPV)

The system tests are functional performance verification tests. The following describes the system tests:

ROM Test

The ROM test performs several checksum tests on various read only memory elements, including the system ROM as well as the various software modules present in flash ROM.

Passing the ROM test implies that the microprocessor can access each ROM memory address and that each ROM segment provides checksums that match previously calculated values.

RAM Test

The RAM test performs a write/read operation in each memory location in system dynamic RAM (DRAM). The video RAM in the display subsystem and the acquisition RAM in the data acquisition subsystem are not tested as part of the RAM test and are tested elsewhere. At each DRAM memory location, the code that resides at that location is stored in a microprocessor register. A test pattern is then stored at the memory location, read, and compared. An inverse test pattern is then stored, read, and compared. The original code is then restored to the memory location. This continues until all DRAM memory locations have been tested. The static RAM in the real time clock chip is also tested in a similar fashion.

Passing the RAM test implies that all RAM memory locations can be accessed by the microprocessor and that each memory location can store a logical "1" or a logical "0."

GPIB Test

The GPIB test performs a write/read operation to each of the registers of the GPIB IC. A test pattern is written to each register in the GPIB IC. The pattern is then read and compared with a known value.

Passing the GPIB test implies that the read/write registers in the GPIB IC can store a logical "1" or a logical "0," and that the GPIB IC is functioning properly. Incoming and outgoing GPIB information will not be corrupted by the GPIB IC.

RS-232-C Test

This test checks the basic interface functions of the RS-232-C port. Both internal and external portions of the port circuitry are tested. In order for the RS-232-C test to pass, the RS-232-C loopback connector must be installed on the RS-232-C connector.

PS2 Test

The PS2 test exercises the PS2 interface between the logic analyzer and external keyboard, if an external keyboard is connected. First, a read/write operation is performed to each of the registers of the PS2 IC. A test pattern is written to each memory location, read, and compared with a known value. Second, if an external keyboard is connected to the PS2 port, the keyboard controller that resides in the keyboard is polled by the microprocessor. A test pattern is sent to the keyboard controller and returned to the microprocessor by the keyboard controller. The test pattern is then compared with a known value.

Passing the PS2 test implies that the read/write registers in the PS2 IC can store a logical "1" or a logical "0," and that the PS2 IC is functioning properly. Also, passing the PS2 test implies that the PS2 pathway to the external keyboard is functioning and that the keyboard controller can communicate with the microprocessor in the logic analyzer. Incoming PS2 information from the external keyboard will not be corrupted by the pathway between the keyboard controller and microprocessor.

Disk Test

The disk test verifies the operation of both the flexible disk drive and hard disk drive.

For the flexible disk drive, the disk test exercises the disk controller circuitry by performing a write/read on a disk. Either a LIF-formatted disk with 20 sectors available space or DOS-formatted disk with 5K available space is required and should be inserted in the disk drive. When the disk test is executed the disk is first checked sector by sector to find any bad

sectors. If no bad sectors are found a test file will be created on the disk and test data will be written to the file. The file is then read and the test data compared with known values. The test file is then erased at the conclusion of the test.

For the hard disk drive, the disk test exercises the disk controller that is on the hard disk drive assembly. In addition, the buffers that make up the hard disk drive interface are tested. When the test is executed, the sectors of the hard disk are checked, and then write/read tested like the flexible disk drive.

Passing the disk test implies that the flexible disk controller circuitry in the logic analyzer and the disk read/write circuitry in the flexible disk drive are functioning properly. The flexible disk drive can read and write to a LIF- or DOS-formatted disk, and the data will not be corrupted by the flexible disk drive circuitry. Passing the disk test also implies that the hard disk drive controller circuitry, interface, and read/write circuitry are functioning properly, and that the data will not be corrupted by the hard disk drive circuitry.

Perform Test All

Selecting Perform Test All will initiate all of the previous functional verification tests in the order they are listed. The failure of any or all of the tests will be reported in the test menu field of each of the tests. The Perform All Test will not initiate the Front Panel Test or the Display Test.

Front Panel Test

A mock-up of the logic analyzer front panel is displayed on the CRT when the Front Panel Test is initiated. The operator then pushes each front panel button and turns the RPG (rotary pulse generator) knob to toggle the corresponding fields from light to dark on the front panel mock-up. Successively pushing any front panel key will cause the corresponding field to toggle back and forth between light and dark. An exception is the Done key. Pressing the Done key a second time will cause an exit of this test.

The Front Panel Test passes when all of the key fields in the front panel mock-up on the CRT can be toggled by pressing the corresponding front panel key, and the two RPG fields can be toggled by turning the knob. The Front Panel Test is not called when Perform Test All is selected.

Display Test

When initiated, the display test will cause three test screens to be displayed sequentially. The first test screen is a test pattern used to align the CRT. The other two screens verify correct operation of the greyscale palette by displaying first a full-bright screen and then a half-bright screen.

The pass or fail status of the display test is determined by the operator. The Display Test passes when all three test screens are displayed according to chapter 4, "Calibrating and Adjusting." The display test is not used when Perform Test All is selected.

LAN Test

The LAN test verifies the functionality of the LAN circuitry on the logic analyzer CPU board. A status code is returned for each of the LAN tests when each test is completed. The following figure shows the bit positions of the hexidecimal status reporting word.

A "1" in a bit position signifies that the bit is set and the test failed.

A "0" in a bit position signifies that the bit is not set and the test passed.

Status Reporting Message

Status Bits

Bit 0	The internal registers of the LAN IC are loaded with known test values and then are read. If this bit is not set, it implies that the LAN IC is operating properly and that the microprocessor can communicate with the LAN IC. If this bit is set, then the LAN module is not operational and must be replaced.
Bit 1	The CAM (Content Addressable Memory) bit reports whether the LAN address can be written from the LAN module Static RAM (SRAM) to the internal memory of the LAN IC. Also, the CAM bit reports whether the LAN address can be written to SRAM from the LAN IC. If this bit is not set, it implies that both the SRAM and the LAN IC internal memory are able to recognize and store the LAN address. If this bit is set, then the LAN module is not operational and must be replaced.
Bit 2	If this bit is not set, then the self-test has detected that the LAN cable is properly connected to the logic analyzer. If this bit is set, then the physical connection of the LAN cable must be checked.
Bit 3	If the Termination bit is set, then the self-test has detected an excessive number of collisions. The most probable cause of excessive collisions is an improperly terminated LAN cable. Provide a proper termination of the LAN cable according to the LAN topology being used.
Bit 4	The MAC (Media Access Control) bit indicates whether the Media Access Control unit on the LAN IC is functioning. If this bit is not set, it implies that both the transmit functions and receive functions of the LAN IC are operating properly. If this bit is set, then the LAN module is not able to properly transmit and receive packets and must be replaced.
Bit 5	The ENDEC (Encoder/Decoder) bit indicates whether the encoder/decoder internal to the LAN IC is functioning. The encoder/decoder is the interface between the MAC and the Ethernet transceiver. If this bit is set, then the ENDEC is not operating properly and the LAN module must be replaced.
Bit 6	The TRANS (Transceiver, such as Ethernet transceiver) bit indicates whether the circuitry between the LAN IC and the LAN cable is functioning. If this bit is not set, then the path between the LAN cable and the LAN IC is operating properly. If this bit is set, then either the CPU board or the I/O board must be replaced.
Bit 7	Timeout bit. If this bit is set, then bits 4, 5, or 6 will also be set. Refer to the appropriate bit for a suggested course of action.
Bit 8	The Tx bit indicates whether the transmission portion of the MAC, ENDEC, or TRANS test failed. Therefore, the Tx bit is used in conjunction with bits 4, 5, and 6. Refer to the appropriate bit for the suggested course of action.
Bit 9	The Rx bit indicates whether the receive portion of the MAC, ENDEC, or TRANS test failed. The Rx bit is used in conjunction with bits 4, 5, and 6. Refer to the appropriate bit for the suggested course of action.
Bit 10	The Parameters bit indicates the integrity of the LAN module self-test parameters. If this bit is not set, then the parameters sent to the self-test routine are correct. If this bit is set, then contact your nearest Agilent Sales and Service Office.
Bit 11	The EPROM that is used to hold the Ethernet address, IP address, and gateway address has been corrupted. If this bit is set, the LAN module must be replaced.
Bits 12–15	Not Used

Analyzer Tests (Analy PV)

The analyzer tests are functional performance verification tests. The self-tests identify the correct operation of major functional areas in the module. There are two sets of self-tests: the Board Verification Tests and the Acquisition IC Verification Tests. The self-tests are not intended for component-level diagnostics.

Board Verification Tests

The Board Verification Tests functionally verify the main subsystems of the module other than the acquisition ICs. Five tests are performed on the module subsystems. The tests are the PLD, Oscillator, Data Memory, Comparators, and Alignment Tests

PLD Test Programmable Logic Devices (PLD) are utilized as an interface between the acquisition board and the CPU board. The PLD Test verifies the operation of the data bus through the PLD. Test patterns are sent to the module and are written to a block of module memory. The patterns are then read and compared with known values. Also, a HW acceleration test verifies the PLD's high speed pattern search operation.

Passing the PLD Test implies that the PLD is not corrupted and that data can be passed between the acquisition board and the CPU board.

Oscillator Test The Oscillator Test functionally verifies the two oscillators and the oscillator internal pathways on the logic analyzer module. The oscillators are checked using the event counter on one of the acquisition ICs. The event counter will count the number of oscillator periods within a pre-determined time window. The count of oscillator periods is then compared with a known value.

Passing the Oscillator Test implies that both oscillators on the logic analyzer module are operating properly.

Data Memory Test After verifying the integrity of the memory address bus, the acquisition RAM is checked by filling the RAM with a checkerboard pattern of "1"s and "0"s then reading each memory location and comparing the test pattern with known values. Then the RAM is filled with an inverse checkerboard pattern, read, and compared with known values. The acquisition ICs are then used to generate a walking "1"s pattern, which is stored in RAM. The patterns are then read and compared with known values.

Passing the memory test implies that the acquisition RAM is functioning and that each memory location bit can hold either a logic "1" or logic "0." Passing this test also implies that the RAM is addressable by both the acquisition ICs and the mainframe CPU system through the CPU interface.

Alignment Test The alignment test exercises the clock optimization circuit on-board the acquisition IC. A test signal is generated by the comparators and sent to the acquisition IC. A test run is then done to see if the clock optimization circuit aligns the data signal with the master clock signal.

Passing the alignment test implies the clock optimization circuit that resides on the acquisition IC operates properly. Consequently the acquisition IC can properly sample data with minimal channel-to-channel skew.

Comparators Test The comparators in the logic analyzer front end are checked by varying the threshold voltage and reading the state of the activity indicators. The output of the comparator DAC is set to the upper voltage limit and the activity indicators for all the pod channels are read to see if they are all in a low state.

The DAC output is then set to the lower voltage limit, and the activity indicators are read to see if they are in a high state. The DAC output is then set to 0.0 V, allowing the comparators to recognize the test signal being routed to the test input pin of all of the comparators. Consequently, the activity indicators are read to see if they show activity on all channels of all the pods.

If the Comparators Test reveals that a logic analyzer channel is not recognizing the test data, a message will appear alerting the user that the channel is not operating as expected. If the module cannot be immediately serviced, then the user is alerted so that the failed channel is not used until the module can be serviced.

Passing the Comparators Test implies that the logic analyzer front end is operating properly and all channels are capable of passing data to the acquisition ICs.

Acquisition IC Verification Tests

During the Acquisition IC Verification Tests, five tests are performed on the acquisition ICs. The tests are the Communications, Encoder, Resource, Sequencer, and Clock Tests.

Communication Test The communication test verifies that communications pipeline between the various subsystems of the IC are operating. Checkerboard patterns of "1"s

and "0"s are routed to the address and data buses and to the read/write registers of each chip. After verifying the communications pipelines, the acquisition clock synchronization signals that are routed from IC to IC are checked. Finally, the IC master clock optimization path is checked and verified.

Passing the communication test implies that the communications pipelines running from subsystem to subsystem on the acquisition IC are functioning and that the clock optimization circuit on the IC is functioning. Also, passing this test implies that the acquisition clock synchronization signals are functioning and appear at the synchronization signal output pins of the acquisition IC.

Encoder Test The encoder is tested and verified using a walking "1" and walking "0" pattern. The walking "1" and "0" is used to stimulate all of the encoder output pins which connect directly to the memory ICs. Additionally, the post-store counter in each of the acquisition ICs is tested.

Passing the encoder test implies that the encoder is functioning and can properly route the acquired data to the acquisition memory. Also, passing this test implies that the post-store counter on the acquisition ICs is functioning.

Resource Test The pattern, range, edge, and glitch recognizers are tested and verified. First, an on-chip test register is verified for correct operation. Next, the pattern comparators are tested to ensure that each bit in the recognizer as well as the logic driver/receiver are operating. The edge and glitch pattern detectors are then verified in a similar manner. The range detectors are verified with their combinational logic to ensure that the in- and out-of-range conditions are recognized.

Passing the resource test implies that all of the pattern, range, edge, and glitch resources are operating and that an occurrence of the pattern, edge, or glitch of interest is recognized. Also, passing this test implies that the range recognizers will detect and report in- and out-of-range acquisition data to the sequencer or storage qualifier. The drivers and receivers at the recognizer input and output pins of the acquisition IC are also checked to be sure they are functioning.

Sequencer Test The sequencer, the state machine that controls acquisition storage, is tested by first verifying that all of the sequencer registers are operating. After the registers are checked, the combinational logic of the storage qualification is verified. Then, both the occurrence counter and the sequencer level counter is checked.

Passing the sequencer test implies that all 12 available sequence levels are functioning and that all possible sequence level jumps can occur. Also, passing this test implies that user-defined ANDing and ORing of storage qualified data patterns will occur, and that the occurrence counter that appears at each sequence level is functioning.

Chip Clock Test The sample clock generator on the acquisition ICs are tested by first checking the operation of the clock optimization circuit. The state acquisition clock paths are then checked to ensure that each state clock and clock qualifier are operating by themselves and in all possible clock and qualifier combinations. The timing acquisition optimization circuit is then operationally verified. Finally, the timing acquisition frequency divider (for slower timing sample rates) is checked.

Passing the chip clock test implies that each acquisition IC can generate its own master clock whether the clock is generated using a combination of external clocking signals (state mode) or internal sample clock signals (timing mode).

Oscilloscope tests (Scope PV)

The following self-tests check the major components of the Agilent 1670G-series oscilloscope board as well as all associated circuitry (you must have the oscilloscope option). When the self-tests have all been completed with a "PASS" status, the major data and control pipelines in the Agilent 1670G-series oscilloscope board are functioning properly.

Data Memory Test This test verifies the correct operation of the FISO (fast-in/slow-out) data memory on the board. Test patterns are written into the memory and then read and compared with known values.

Timebase Test The pre-trigger and post-trigger delay modes are first tested by programming a predetermined time interval in the trigger counters. At the end of the time intervals, the arm, trigger, and run status bits are read and compared with known values. The coarse and fine interpolators are then checked by reading the values of the interpolator counters after a simulated acquisition. The counter values are then compared with a known value. Finally, the sample clock is checked by programming a sample clock frequency and then reading the status of the clock to detect when one clock period has elapsed. The clock period time interval is then compared with a known value.

A/D Test This test verifies the correct operation of the A/D converter on the board. A check of the trigger in Trigger Immediate mode is first made. The A/D converters are then exercised by setting the reference voltage and channel offset such that a simulated acquisition obtains data in the extremes and middle of the quantization range of the A/D converter. After each simulated acquisition, the data is compared with known values.

D/A Test This test verifies the correct operation of the D/A converter on the board. Both the offset and trigger level D/A converters for each channel are set to a reference level and then changed. The logic trigger IC is programmed to detect the changes. The detection of a correct trigger indicates that the D/A converter is operating normally.

Trigger Test This test verifies the correct operation of the trigger components on the board. First, the logic trigger memory is checked by writing and then reading known patterns. The logic qualifiers, logic trigger output, and trigger holdoff are then checked.

IMB Test This test verifies the correct operation of the oscilloscope board interface to the intermodule bus.

All Tests This will automatically execute each test, one at a time, until all tests are done.

Pattern Generator tests (Patt Gen)

The following section contains a description of each of the the pattern generator self tests.

Clock Source Test

The Clock Source Test checks that the internal clock sources are functioning by verifying the presence of a given clock source. The test toggles each clock source in the following fashion. First the board is stopped and outputs are disabled. Module RAM is loaded with zeros, then the module is placed in the respective mode for the given clock and the clock source is selected. The module is then started and the main status checked to see that the pipeline is running. The board will then be stopped and the status checked to see that the pipeline did stop.

Passing the Clock Source Test implies that the internal clock sources are functioning properly, and that the other dependent subcircuits respond to the clock signal.

Diagnostic Integer Value: The integer returned will have the following bit format:

BIT #:	15, 14,13, 12	11, 10, 9, 8	7, 6, 5, 4	3, 2, 1, 0
	200M clk	100M clk	50M clk	PLD clk

Each nibble of the output corresponds to one of the clock sources. The bit pattern of each nibble has the following definition:

0 — passed
1 — failed to run
2 — failed to stop
3 — failed to both run and stop

Vector Memory Test

The Vector Memory Test does a first order check of the functionality of RAM. The first pass of the test will load the entire RAM with 0x0000. The software will step the clock enough times to output one page worth of data. At each clock a test read port for each RAM IC will be checked and verified for all 0s.

The second pass of the test will load all the RAMS with 0xFFFF and then check using the same technique as in the first pass, verifying for all Fs.

The third pass loads memory with an alternating 0x5555 and 0xAAAA checkerboard pattern. Again the test checks the data in the same fashion as in the first pass.

Passing the Vector Memory Test implies that each memory location in RAM can store a logic 1 or 0. Passing the test also implies that the CPU interface is functioning and can properly affect control over the memory and memory addressing.

Diagnostic Integer Value: This test checks the RAM of the entire board. The returned integer for a particular card has the following format:

BIT #:	15, 14	13, 12, 11, 10, 9, 8, 7, 6	5, 4, 3, 2, 1, 0
	Test 1	Fail row	Failed test

Bits 14,15 contain the test that failed where the value is the following:

1— failed all zeros test
2— failed all ones test
3— failed alternating test

Bits 6-13 contain the row of the page that failed.
Bits 0-5 contain the failure code for the six RAM ICs on the board. Bits 0-4 contain the failure code for the RAMs for pod 1-5, and bit 5 contains the failure code for the RAM used for instructions. A one in the bit position indicates that that RAM provided incorrect information.

Address Counter Test

The Address Counter Test contains four subtests that check the functionality of the column and row address counters for board RAM. The four subtests use each of the four loop registers to perform the test.

The first step of the test is to load memory using the current loop register with a specific pattern for the address counter. Memory is loaded with 0x0000 except at predetermined RAM row and column positions, which are loaded with 0xFFFF.

The current loop register is used to set the address for the 0xFFFF loading. The loop register is also used to reset the addresses back to zero for starting the stepping process.

After memory has been loaded the clock is stepped through all possible RAM addresses checking for the correct data at each address.

Passing the Address Counter Test implies that each RAM memory location can be accessed by the RAM addressing circuitry while under control of the clocking circuit. Passing the test also implies that the loop registers are operating correctly.

Diagnostic Integer Value: This test checks the counters of the entire board. The returned integer has the following format:

BIT #:	15	14, 13, 12, 11, 10, 9, 8, 7, 6	5, 4, 3, 2, 1, 0
	Row/Col	Fail row	Failed RAM

Bit 15 is used to flag where the value of the fail row bits (6-14) came from. If the failing row value was less than 511 bit 15 is set to zero. If the failing row was greater than 511 bit 15 is set to one. The failed row bits (6-14) contain a value from 0 to 255.

Bits 0-5 contain the failure code for the six RAMs on the board. Bits 0-4 contain the failure code for the RAM for pods 1-5, and bit 5 contains the failure code for the RAM used for instructions. A one in the bit position indicates that that ram provided incorrect information.

Instruction Tests

This test contains three subtests that have unique descriptions. Each subtest is described below.

Passing the Instruction Tests implies that CPU addressing, RAM addressing, and the instruction decoder of the board responds properly to user commands.

Subtest #1 — Instruction Interface Test This test checks the functionality of the break command in the instruction memory and the status register that reads the break.

On the first pass of this test, instruction memory is loaded with zeros (NOP). The board is run and the main status register polled to see that the hardware is running. If the hardware is stopped the test fails.

The second pass of the test places the break instruction on the next to last vector in memory. Again the hardware is started and the status is read. This time the board should stop or the test fails.

Diagnostic Integer Value: This test is only valid for signals on the master board of the configuration. The values returned from any expansion cards will be zero. The integer returned will have the following bit format:

BIT #:	15 ,14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4	3, 2, 1, 0
	unused	Test Mode

The Test Mode bit positions have the following meaning:

0 — passed
1 — stopped without break
2 — failed to stop from software
4 — failed to stop with break
8 — stopped by something other than break

Subtest #2 — Wait Instruction Test This test checks the functionality of the wait command in the instruction memory and the status register that reads the wait. The test is performed on each of the four event registers. The current wait event being tested is loaded on the first page of memory and a break instruction is loaded on the third page of memory.

The first pass of the test places a wait on no event in the event register. The hardware is started and a wait is begun for the vectors to hit the break instruction on the third page. The main status is checked to see that the hardware is stopped by the break instruction.

The second pass of the test places a wait on any condition in the event register. Again the hardware is started wait is begun. On this pass the hardware should be stopped by the wait condition and not by the break condition.

The final pass clears the current wait condition using the hardware wait clear command. The board should run from the current wait to the break condition and once again stop.

Diagnostic Integer Value: The integer returned will have the following bit format:

BIT #:	15, 14,13, 12	11, 10, 9, 8	7, 6, 5, 4	3, 2, 1, 0
	Event D	Event C	Event B	Event A

Each nibble corresponds to the event register being tested. The value of the nibble for the event register has the following definition:

0 — passed
1 — failed to stop on break with no event wait
2 — stopped on wait with setting of no event
3 — failed to stop on break or wait with wait any event
4 — failed to stop on wait with wait any event
5 — failed to clear wait
6 — stopped on false break condition

It should be noted that the value returned will be the last error encountered.

Subtest #3 — If Instruction Test This test checks the functionality of the if branching. Instruction memory is loaded with a wait on event 'a' instruction in the non-if branch of memory and a break instruction in the if branch.

The first pass of the test sets the branch pattern to a never branch condition. The board is started and a wait is begun for the vectors to get to the wait instruction. The hardware should stop on the wait instruction, not the break. The main status is checked to verify this stop condition.

The second pass of the test sets the branch pattern to always branch. Again the board is started and a wait is begun. In this case the break instruction should be the stop condition.

Diagnostic Integer Value: The integer returned will have the following bit format:

BIT #:	15 ,14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4	3, 2, 1, 0
	unused	Test Mode

The Test Mode bit positions have the following meaning:

0 — passed
1 — failed to stop on wait in non-if branch
2 — took if branch on no branch event
4 — failed to stop on break in if branch
8 — took non-if branch on any branch event

Output Patterns for testing with an external logic analyzer or oscilloscope

The performance test will set up two predefined patterns for examining the board from an external analyzer or scope. This allows the user to check the output pipeline for functionality and also helps to perform a quick check of all bit locations in the data VRAMS.

The data is output based on the frequency mode chosen by the user:

50MHz Mode — 20 ns period

100MHz Mode — 10 ns period

200MHz Mode — 5 ns period

Either a checkerboard pattern (alternating 1s and 0s across the output channels) or a walking ones pattern are available.

GPIB

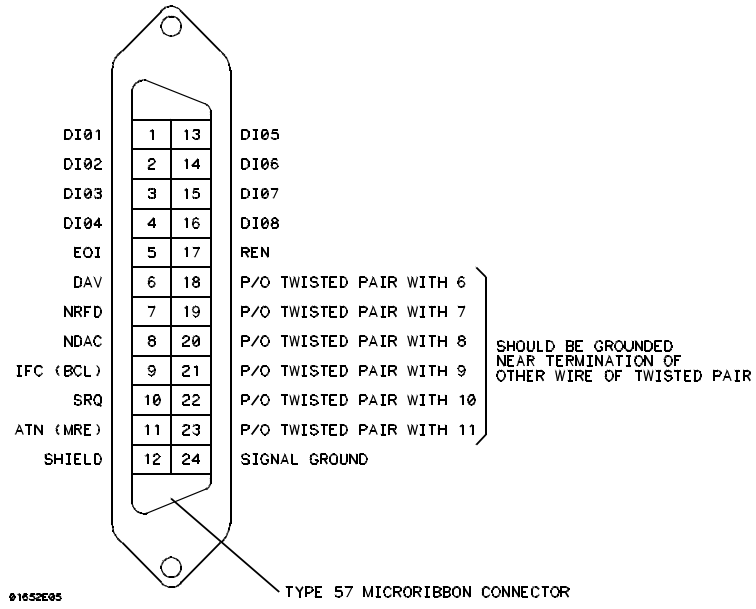
The Agilent Technologies Interface bus (GPIB) is Agilent Technologies' implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programming Instrumentation." GPIB is a carefully defined interface that simplifies the integration of various instruments and computers into systems. The interface makes it possible to transfer messages between two or more GPIB compatible devices. GPIB is a parallel bus of 16 active signal lines divided into three functional groups according to function.

Eight signal lines, called data lines, are in the first functional group. The data lines are used to transmit data in coded messages. These messages are used to program the instrument function, transfer measurement data, and coordinate instrument operation. Input and output of all messages, in bit parallel-byte serial form, are also transferred on the data lines. A 7-bit ASCII code normally represents each piece of data.

Data is transferred by means of an interlocking "Handshake" technique which permits data transfer (asynchronously) at the rate of the slowest active device used in that transfer. The data byte control lines coordinate the handshaking and form the second functional group.

The remaining five general interface management lines (third functional group) are used to manage the devices connected to the GPIB. This includes activating all connected devices at once, clearing the interface, and other operations.

The following figure shows the connections to the GPIB connector located on the rear panel.



GPIB Interface Connector

RS-232-C

The logic analyzer interfaces with RS-232-C communication lines through a standard 25-pin D connector. The logic analyzer is compatible with RS-232-C protocol. When a hardwire handshake method is used, the Data Terminal Ready (DTR) line, pin 20 on the connector, is used to signal if space is available for more data in the logical I/O buffer. Pin outs of the RS-232-C connectors are listed in the following table.

RS-232-C Signal Definitions

Pin Number	Function	RS-232-C Standard	Signal Direction and Level
1	Protective Ground	AA	Not applicable
2	Transmitted Data (TD)	BA	Data from Mainframe High = Space = "0" = +12 V Low = Mark = "1" = –12 V
3	Received Data (RD)	BB	Data to Mainframe High = Space = "0" = +3 V to +25 V Low = Mark = "1" = –3 V to –25 V
4	Request to Send (RTS)	CA	Signal from Mainframe High = ON = +12 V Low = OFF = –12 V
5	Clear to Send (CTS)	CB	Signal to Mainframe High = ON = +3 V to +12 V Low = OFF = –3 V to –25 V
6	Data Set Ready (DSR)	CC	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = –3 V to –25 V
7	Signal Ground	AB	Not applicable
8	Data Carrier Detect (DCD)	CF	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = –3 V to –25 V
20	Data Terminal Ready (DTR)	CD	Signal from Mainframe High = ON = +12 V Low = OFF = –12 V
23	Data Signal Rate Selector	CH/CI	Signal from Mainframe Always High = ON = +12 V

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Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
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- Use caution when exposing or handling the CRT. Handling or replacing the CRT shall be done only by qualified maintenance personnel.

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Hazardous voltage symbol.

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