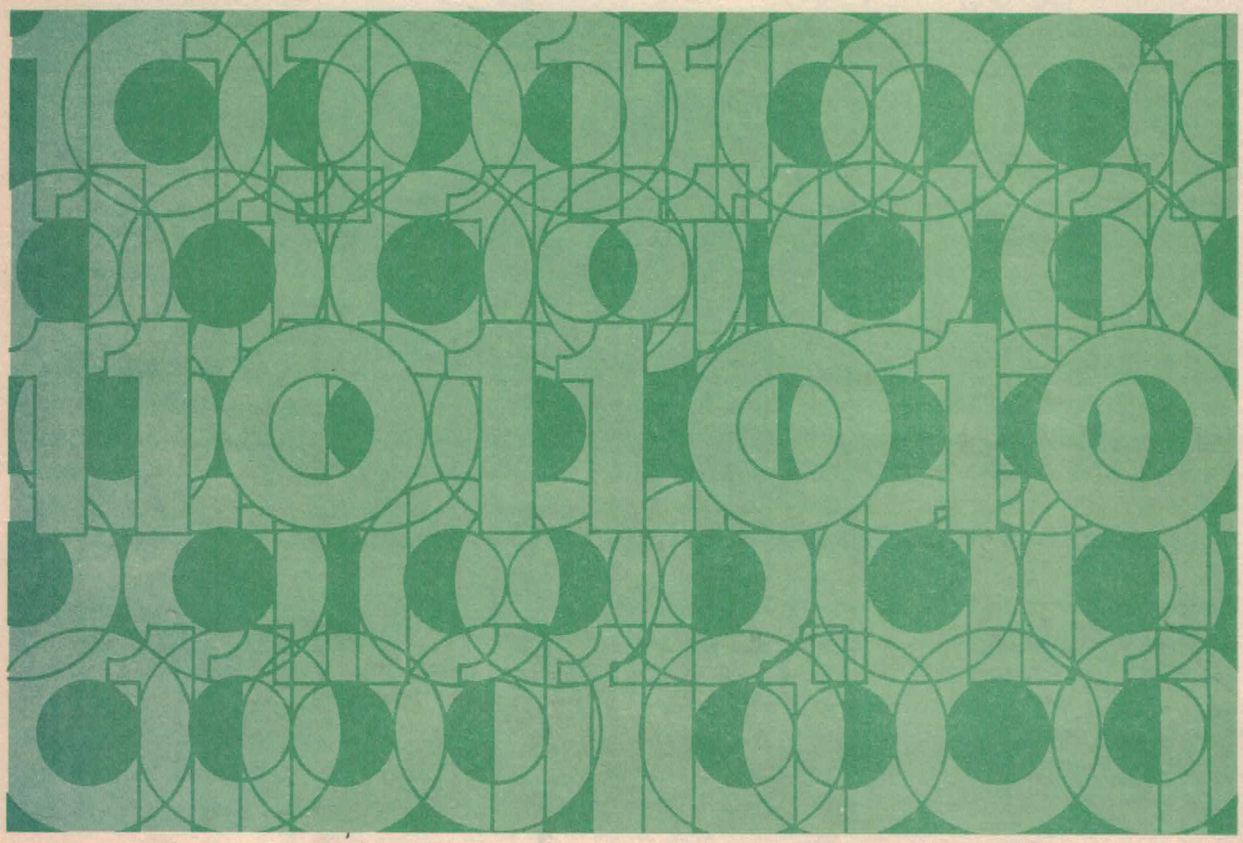
PRICE $4.95
(May be applied towards the purchase of the Model 10)

THE MODEL 10 TRIGGER EXPANDER

(For Use With the Model 100A Logic Analyzer)

INCLUDES:

- Using the Model 10 to Expand the Model 100A
- How to use the Controls
- Understanding Circuit Operation
- Assembly & Test of the Model 10 Kit
- Troubleshooting
- Applications of the Model 100A/Model 10



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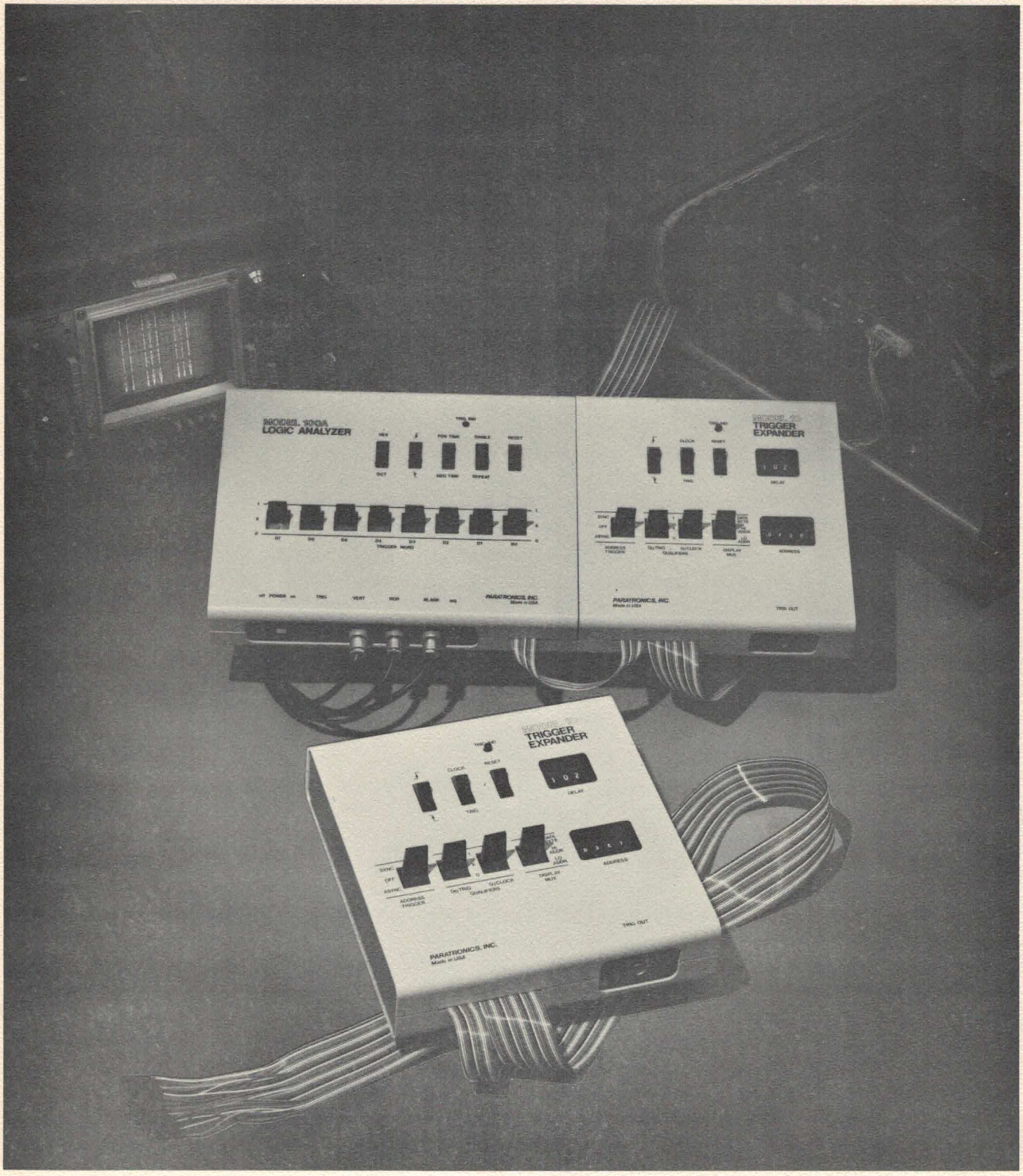
CAUTION

REFER TO THE MODEL 100A MANUAL BEFORE CONNECTING THE BLANKING OUTPUT OF THE ANALYZER TO YOUR SCOPE. OTHERWISE THE SCOPE's Z-AXIS INPUT CIRCUIT MAY BE DAMAGED.


LOGIC ANALYZER
TRIGGER EXPANDER
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1.0 INTRODUCTION

There is no doubt that the introduction of the microprocessor several years ago has revolutionized the electronics industry. More and more companies, educational institutions and individuals are using microprocessor-based systems.

When the first low-cost logic state analyzer (the Model 100A) was introduced through a cover article in the February 1977 issue of Popular Electronics, the resulting large response from a wide variety of customers provided us with a great deal of insight about how deeply the microprocessor had penetrated into both industrial and nonindustrial areas. Customers who acquired the Model 100A Logic Analyzer for use with their microprocessor systems included large and small computer corporations, power and tire companies, the inmates of a state penitentiary, wineries, amusement parks, all manner of schools and hobbyists, and even a chewing gum manufacturer!

Why has the Model 100A been so popular? The answer is related to the low cost of today's basic microprocessor systems. For example, a "starter" system consisting of a CPU board, a small amount of memory, a chassis and a power supply can be purchased for just a few hundred dollars. But the related supporting test equipment--such as logic analyzers-- has historically required an investment of several thousand dollars or approximately ten times the cost of the simple microprocessor system. For many companies, schools and individuals just getting into the design and use of microcomputers, this type of investment for supporting equipment was difficult, if not impossible, to justify. Yet the inherent complexity of a microprocessor system requires sophisticated logic analysis techniques for development, maintenance, and training: the old scope-and-ohmmeter method are just not enough. Thus, the introduction of the Model 100A came at a time when the microcomputer user needed a logic analyzer at a price compatible with the cost of his system. And since the Model 100A has many of the features of units costing much more, it is enjoying widespread use.

The Model 100A's low price was made possible through the use of efficient design and packaging techniques as well as by eliminating some of the more complicated and less frequently used "bells and whistles" of more expensive analyzers.

However, as microcomputing systems increase in complexity, the user may find that the basic analysis capabilities of the Model 100A are not adequate. For example, with the Model 100A you can trigger from and view the activity on the 8-bit data bus. But let's say as you view this bus, you find that it's necessary to capture and display only STORE instructions occurring after a particular 16-bit address. The Model 100A alone can't satisfy this requirement. And that's where the Model 10 Trigger Expander comes in. Without affecting any of the basic features of the Model 100A, the Model 10 adds the following capabilities: 16-bit address bus triggering, qualifiers for monitoring selected data, digital delay for paging through long programs, and the viewing of the events on the address bus as well as the data bus without having to move the input probes.

All Model 100A Logic Analyzers in the field can readily be upgraded with the Model 10. As shown in the photo at the front of the manual, the two units mechanically interlock to form a single, integrated package.

By way of summary, Table 1-1 compares the features of the Model 100A alone, the Model 100A and the Model 10, and the Hewlett-Packard HP-1607 Logic Analyzer.

The Model 10 is another member of P.I.'s growing family of high-quality, cost-effective instruments and systems. P.I. will continue to develop these affordable products, each providing the high performance and advanced features demanded by the microprocessor user.

If you have any questions or comments about our products, we'd like to hear from you. Address all correspondence to:

Paratronics, Inc.
800 Charcot Avenue
San Jose, CA 95131

Table 1-1

COMPARISON OF MODEL 100A LOGIC ANALYZER WITH HP-1607

FEATURE	HP-1607 LOGIC ANALYZER	MODEL 100A LOGIC ANALYZER	WITH MODEL 10 TRIGGER EXPANDER
DISPLAY TYPE	TRUTH TABLE	TRUTH TABLE	SAME
DISPLAY FORMAT	HEX/OCTAL	HEX/OCTAL	SAME
DATA COLLECTION	PRE-TRIGGER & POST-TRIGGER	PRE-TRIGGER & POST-TRIGGER	SAME
DISPLAY MODES	SINGLE/REPEAT	SINGLE/REPEAT	SAME
INTENSIFIED TRIGGER	YES	YES	SAME
CLOCK EDGE SELECT	RISING/FALLING	RISING/FALLING	SAME
EXTERNAL TRIG. PULSE	YES	YES	SAME
TRIGGER WORD	16 BITS	8 BITS	24 BITS
QUALIFIERS	TRIGGER OR CLOCK	-	TRIGGER & CLOCK
DELAY	0 - 99,999 CLOCKS	-	0 - 999 CLOCKS OR TRIGGER WORDS
DISPLAY SIZE	2 BYTES BY 16 DEEP	1 BYTE BY 16 DEEP	3 BYTES BY 16 DEEP (1 BYTE AT A TIME)
LOGIC FAMILY COMPATIBILITY	TTL, DTL, RTL, MOS, CMOS, ECL	TTL, DTL, RTL, MOS, CMOS	SAME AS MODEL 100A
DATA COLLECTION RATE	20MHz	8MHz	SAME AS MODEL 100A
MAP MODE	YES	NO	-
AUXILIARY MEMORY	YES	NO	-
BLANKING OUTPUT	10 VOLTS MAX	30 VOLTS MAX	SAME AS MODEL 100A
EXT. SCOPE REQ'D	YES	YES	SAME AS MODEL 100A
SCOPE COUPLING	DC RECOMMENDED	AC OR DC	SAME AS MODEL 100A
WEIGHT	14 POUNDS	5 POUNDS	3 POUNDS
POWER	120 WATTS	7.5 WATTS	2 WATTS

2.0 MODEL 10 SPECIFICATIONS

The Model 10 Trigger Expander is designed to interface with the Model 100A Logic Analyzer to enhance the Model 100A's data domain analysis capabilities. When used with the Model 100A, the Model 10 provides a 24-bit input trigger word, trigger and input clock qualifiers, a user-programmable digital delay of events related to input clock or trigger occurrences, and a multiplexed 8 x 16 display of the microprocessor's upper address byte, the lower address byte, and the data byte.

The controls for all of the above functions, with the exception of the trigger word switches for the data byte, are located on the Model 10. (The data byte is controlled by the 8 trigger word switches on the Model 100A.)

The Model 10 is powered through a flat ribbon cable which plugs into the input probe socket of the Model 100A. The necessary "handshaking" signals for the above data domain analysis capabilities are also provided through this interconnecting cable. Figure 2-1 shows the connections for a typical microprocessor application. The Model 100A and the Model 10 are both readily attached to an optional mounting baseplate with plastic fasteners, so that the two units become a single, integrated instrument. See Figure 2-2.

The Model 10 can also be used in a stand-alone mode as a low-cost 16-bit "word recognizer." In this capacity, it will provide an oscilloscope with a sync pulse for troubleshooting a system where a problem is occurring at (or delayed from) a particular logic state. For stand-alone applications, the user must provide a +5.0V at 300 milliamps from an external source. Refer to Section 8.0 for additional information.

The detailed specifications associated with the Model 10 are shown in Table 2-1.

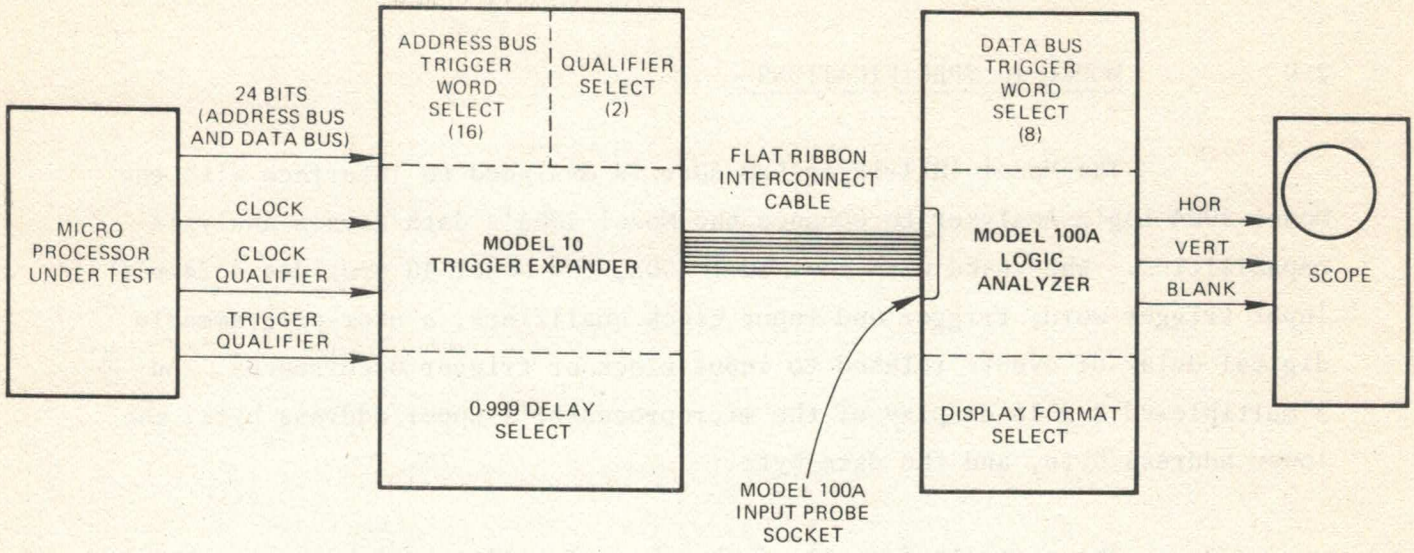


Fig. 2-1. Model 10 and Model 100A electrical connections for a typical microprocessor application.

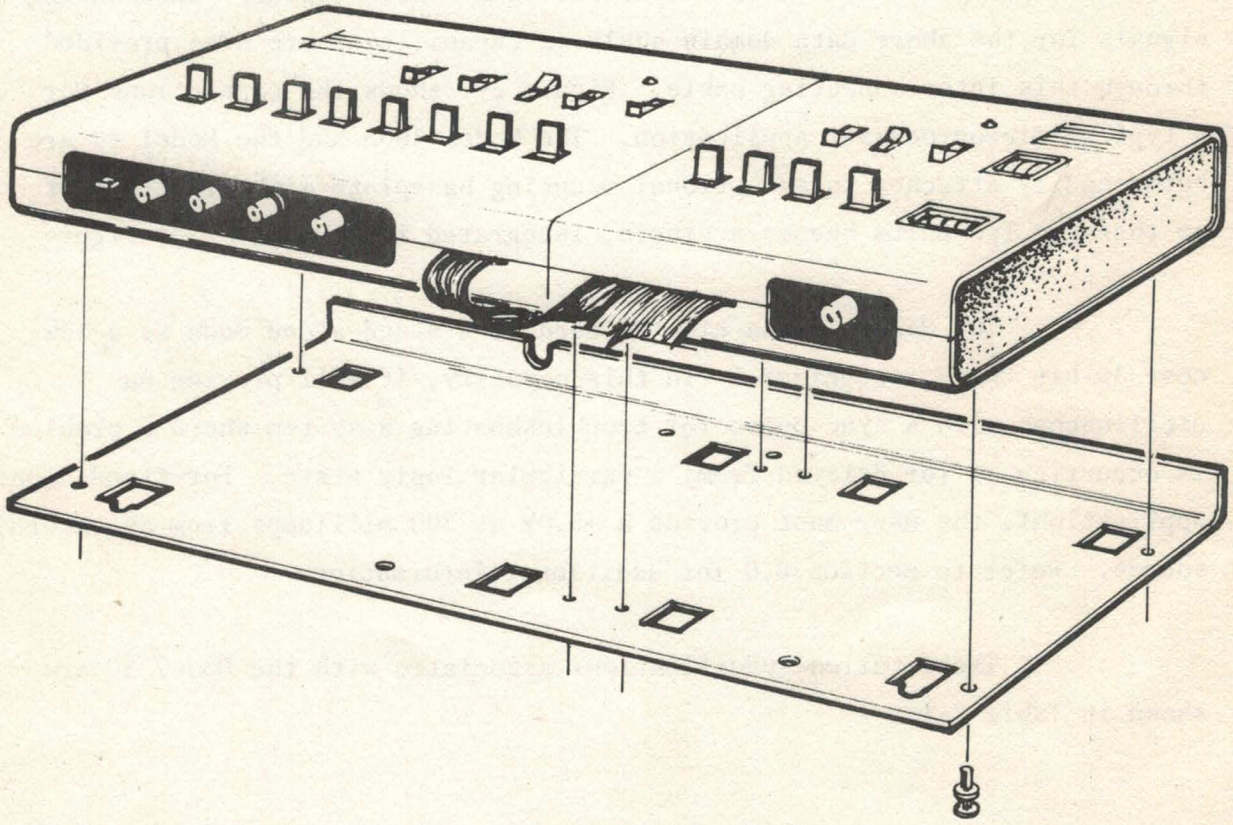


Fig. 2-2. The optional mounting baseplate interconnects the two units so that they becon a single, integrated instrument.

Table 2-1

SPECIFICATIONS

Scope Requirements:	Any laboratory or field oscilloscope with 100 KHz bandwidth and an external Horizontal (X) input. A blanking input is useful but not mandatory.
Address Triggering:	16 buffered address inputs. Address selectable with 4-digit HEX thumbwheel switches.
Address Input Load:	Logic 0: -0.5V to +1.6V; -720 microamps max. Logic 1: +1.6V to +15V; +100 microamps max.
Data Word Triggering:	8 buffered data inputs. Data word is selectable from eight 3-position trigger word switches on Model 100A ("1," "0," or "X").
Data Word Load:	Logic 0: -0.5V to +1.6V; -360 microamps max. Logic 1: +1.6V to +15V; +100 microamps max.
Display Multiplexing:	Provided by 3-position switch which multiplexes the upper address byte, the lower address byte, or the data byte into the Model 100A's data memory. This feature permits the viewing of 3 individual 8 x 16 truth tables without moving the Model 10 input probes.
Input Clock:	Positive or negative edge triggering.
Input Clock Load:	(Same as address input load.)
Maximum Clock Frequency:	8 MHz
Minimum Clock Pulse Width:	50 ns (active edge to inactive edge)
Address or Data Hold Time:	0 ns after active clock edge
Address or Data Set-up Time:	25 ns before active clock edge.
Clock Qualifier:	Permits READ, STORE, I/O and other selected operations which are associated with a particular clock to be collected for display. Controlled by a 3-position switch ("1," "0," or "X").
Address Qualifier:	Permits machine states associated with a particular address to be collected for display. Controlled by a 3-position switch ("1," "0," or "X").
Address Qualifier Set-Up Time:	25 ns before active clock edge.
Address Qualifier Hold Time:	0 ns after active clock edge.
Qualifier Load:	(Same as data word load.)
Digital Delay:	Selectable by a 3-digit thumbwheel switch (0-999 events).
Delay Modes:	CLOCK (for paging through 1000 program steps); and TRIGGER (for permitting the machine to loop up to 1000 times before display).
Address Trigger Modes:	SYNCHRONOUS, OFF, or ASYNCHRONOUS.
Trigger Output:	Auxiliary TTL pulse which occurs when valid trigger word is detected. (This is main output for stand-alone operation.)
Trigger Indicator:	LED on Model 10 indicates that unit is waiting for valid trigger to occur.
Input Probes:	Multi-wire, color-coded flat ribbon cable terminated in gold-plated "universal" pin connectors.
Model 100A Connection:	16-pin flat ribbon cable from Model 10 plugs into Model 100A input probe socket (field installable).
Power:	Model 100A provides power through above cable. (+5V @ 300 milliamps when used in stand-alone mode.)
Mounting:	Optional baseplate permits Model 10 to be mechanically mated to Model 100A so that the two units become a single, integrated instrument.
Weight:	3 pounds.

3.0 WHAT THE CONTROLS DO

The controls of the Model 10 are shown in the photo of Figure 3-1. In most cases, the description of these controls pertains to the use of the Model 10 connected to the Model 100A.

RISING (↱)/FALLING (↳) CLOCK EDGE SELECT - This control determines the active edge of the input clock of the system-under-test. In some circuits, data are valid on the rising edge of the system clock, while in others, the negative clock edge determines the validity of the data. IN ORDER TO OBTAIN A MEANINGFUL DISPLAY, THE CLOCK EDGE SELECT CONTROL ON THE MODEL 10 MUST BE SET TO THE CORRECT POSITION. ALSO, THE CORRESPONDING CONTROL ON THE MODEL 100A MUST ALWAYS BE SET TO THE FALLING (↳) EDGE POSITION. Figure 3-2 summarizes the above statement. Also, be sure and observe the timing relationships shown in the figure. (Note: With the Model 10 in the stand-alone mode, the hold time for data after the active clock edge is 0 ns. When the Model 10 is used with the Model 100A, the hold time for the two units together is approximately 20 ns.)

CLOCK/TRIG - This mode switch selects whether the digital delay control on the Model 10 refers to clock pulses or trigger occurrences. For example, the CLOCK mode is useful for paging through long programs; while the TRIG mode can be used to display the state of the machine after it has looped "n" times. (These concepts are explained further below.)

RESET - This switch functions in parallel with the one on the Model 100A. It is used when the Model 100A is in the SINGLE mode to clear the display and "arm" the analyzer for the capturing of the next truth table. EITHER RESET SWITCH CAN BE USED TO PERFORM THIS FUNCTION. (The Model 10 has the duplicate RESET switch for stand-alone operation. Refer to Section 8.0 for additional details.)

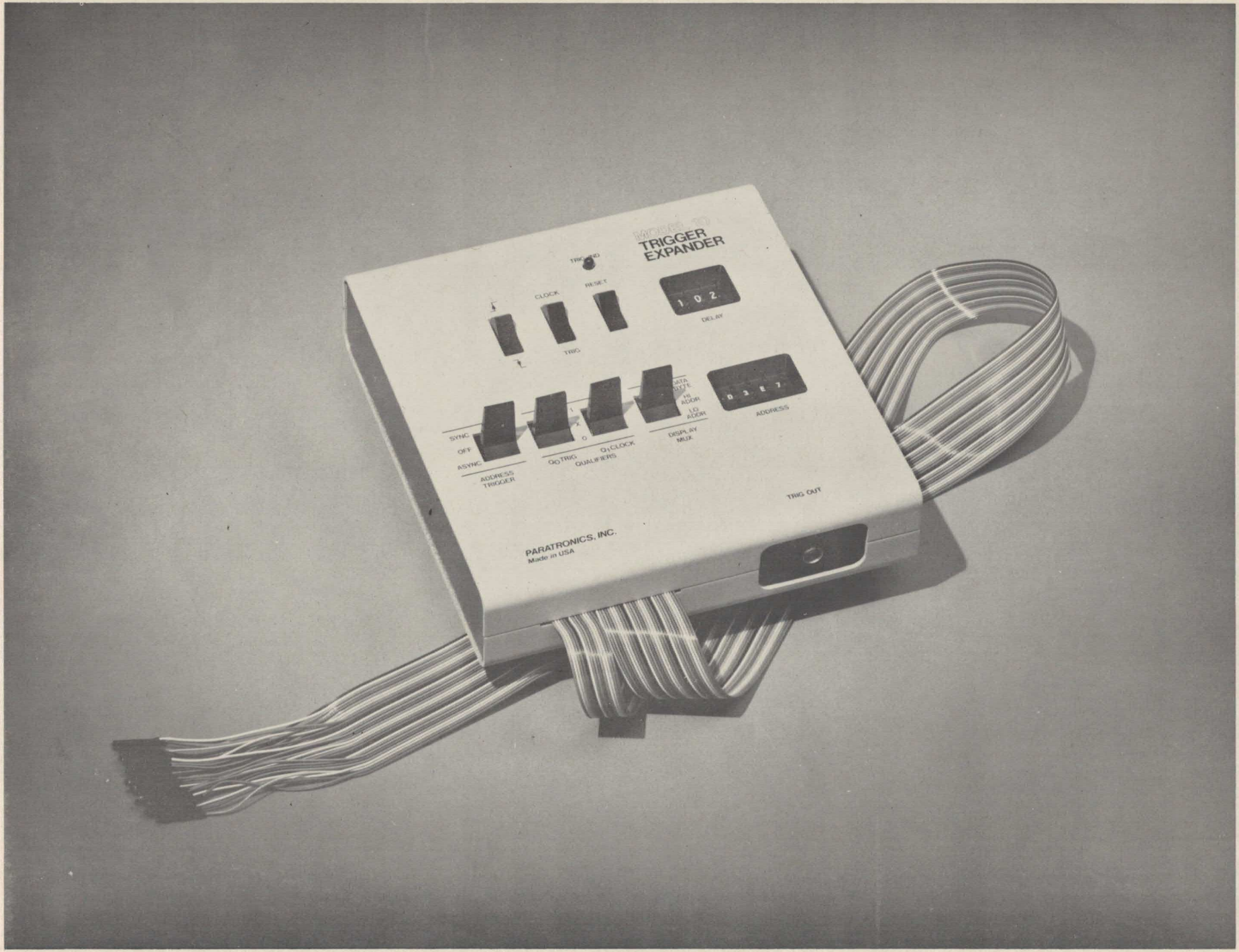
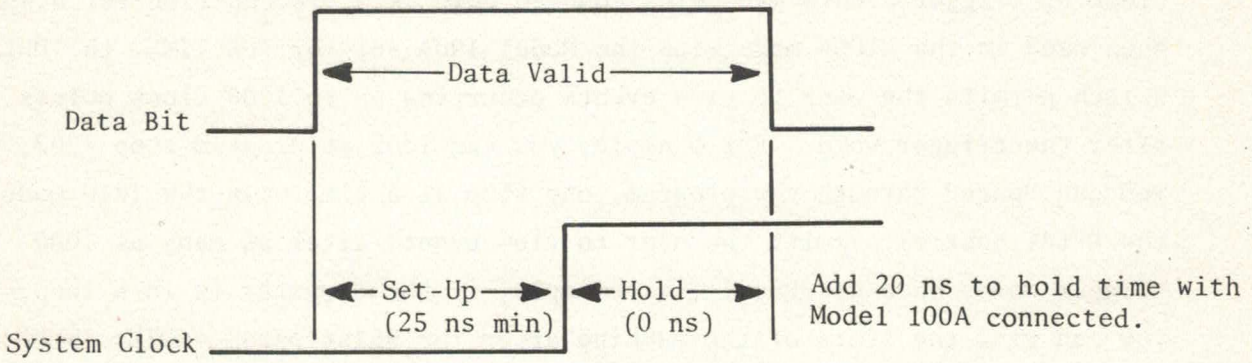


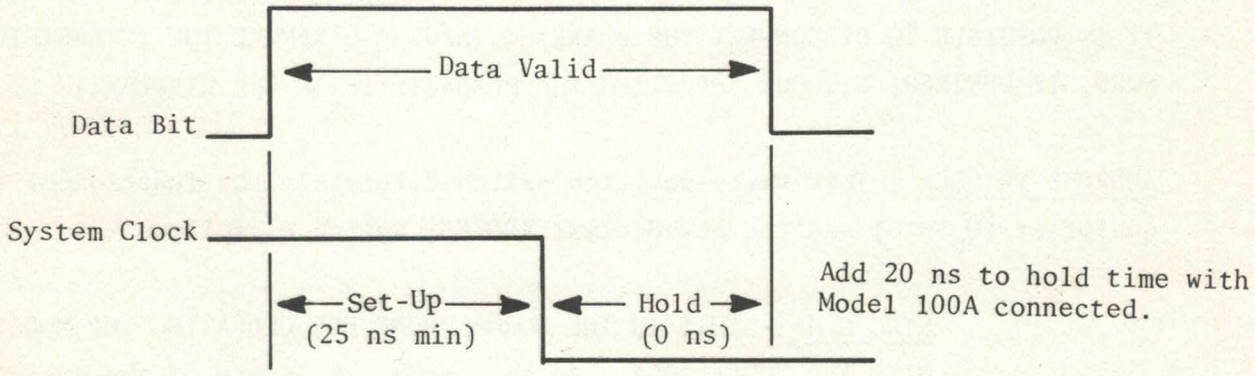
Fig. 3-1. The controls of the Model 10 Trigger Expander.



POSITIVE CLOCK EDGE SYSTEMS

Note:

Model 100A Clock Edge Select Control must always be in falling (↘) edge position.



NEGATIVE CLOCK EDGE SYSTEMS

Fig. 3-2. In order to collect meaningful data, the proper input clock edge must be chosen on the Model 10.

DELAY - This three station thumbwheel switch selects the number of clock pulses or trigger words (0-999) that must occur before the data will be displayed by the Model 100A. (The CLOCK/TRIG mode switch determines whether clock or trigger events are being counted down as a precondition for display.) When used in the CLOCK mode with the Model 100A set for POS TIME, the DELAY switch permits the user to view events occurring up to 1000 clock pulses after the trigger word. For example, you can look at program step #702, or you can "page" through the program, one step at a time. In the TRIG mode, the DELAY control permits the user to view events after as many as 1000 trigger words have occurred. For example, if the computer is in a loop, you can view the state of the machine after the 951st pass. NOTE: WHEN THE DELAY CONTROL IS SET AT "000," NO DELAY TAKES PLACE. THE CLOCK/TRIG SWITCH MAY BE SET TO EITHER THE CLOCK OR TRIGGER POSITIONS. When the Model 100A is set for NEG TIME and the Model 10 in the CLOCK mode, you can "move" the trigger word up from the bottom of the screen towards the top so that events before and after the trigger can be observed. (Refer to Section 4.0 for a discussion concerning the function of the delay control when the setting exceeds 016.) NOTE: WHEN USING THE DELAY FEATURE OF THE MODEL 10, THE INTENSIFIED FIRST OR LAST WORDS IN THE TRUTH TABLE HAVE NO MEANING EXCEPT TO INDICATE WHETHER THE MODEL 100A IS IN THE POS OR NEG TIME MODE. THE TRIGGER WORD ITSELF WILL NO LONGER BE INTENSIFIED. (HINT: FOR MANY SCOPES, IT IS POSSIBLE TO DISCONNECT THE BLANKING INPUT AND REMOVE THE INTENSIFIED WORD, IF DESIRED, WITHOUT AFFECTING THE READABILITY OF THE DISPLAY.)

ADDRESS TRIGGER - This three-position switch determines the function of trigger qualifier (Q_0TRIG) and the hexadecimal ADDRESS switch as follows:

> SYNC Mode - THIS IS THE NORMAL MODE FOR OPERATING THE MODEL 10 WITH THE MODEL 100A. In this mode, the state of the system's address bus and the Q_0 qualifying signal are sampled synchronously using the input clock. (The resulting TRIG OUT pulse, described below, is also synchronous with the input clock.)

OFF Mode - This switch position places the input address lines and the Q_0 qualifier into the "don't care" state so that they have no affect on triggering. Thus, in this mode, triggering is solely a function of the Model 100A's eight trigger switches.

ASYNC Mode - This switch position should be used only when the Model 10 is used in the stand-alone mode as a 16-bit word recognizer. The signal at TRIG OUT is then a TTL level which occurs anytime the 16 bits of the input trigger word plus the trigger qualifier (Q_0) are satisfied. Note, in this mode, the input clock line has no effect.

Q_0TRIG - This switch controls the operation of a 1-bit input line used to qualify the input address bus. The switch has three positions as follows: "1," "0," and "X." In the "X" position, the qualifying line is turned off. In either of the other two positions, it determines the active level that must be provided by the microprocessor-under-test before address triggering can occur. For example, by connecting the Q_0 input to a microprocessor control line, such as the write signal, triggering of the analyzer will occur only when a STORE operation is performed at the selected input address. Note that the Q_0 qualifier functions as an enable signal and is not displayed.

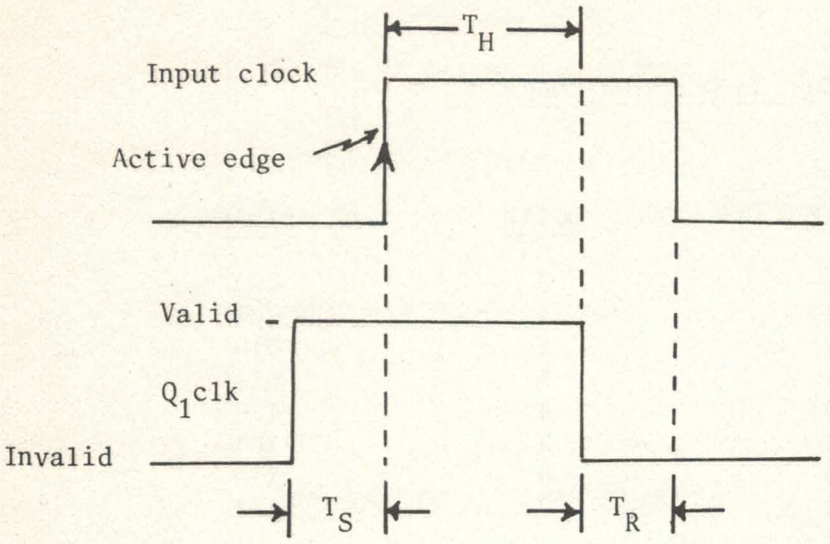
Q_1CLOCK - This switch controls a 1-bit input line used to qualify the input clock. Like the Q_0TRIG switch, it also has three positions: "1," "0," and "X." In the "X" position, Q_1 is disabled and the clock is not qualified. In either of the other two positions, it determines the active level that must be provided by the microprocessor-under-test before an input clock pulse can be received by the Model 10. By connecting the associated Q_1 input line to the appropriate control signal, only data or addresses occurring when the Q_1 line is enabled will be clocked into the Model 10. For example, in Motorola 6800 applications, the Q_1 line can be connected to the signal "VMA" (Valid Memory Address), and the Q_1CLOCK switch can be set to the "1" state. With

this set-up, only 6800-directed bus activity will be monitored. Note that the Q_1 qualifier, like the Q_0 qualifier, functions as an enable signal and is not displayed. See Figure 3-3 for Q_1 timing requirements.

DISPLAY MUX - This three-position switch multiplexes the microprocessor's data byte, lower address byte, and upper address byte into the Model 100A's 8-bit data memory. With the Model 100A in the REPEAT mode, changing this switch position on the Model 10 will automatically cause three 16-word truth tables associated with the lower and upper address bytes and the data byte to be displayed. IN MOST APPLICATIONS, THE MODEL 100A'S TRIGGER SWITCHES SHOULD BE IN THE "X" (DON'T CARE) POSITION WHEN USING THIS FUNCTION. REFER TO SECTIONS 4.0 AND 6.0 FOR ADDITIONAL INFORMATION CONCERNING TRIGGERING.

ADDRESS - This is a four-digit thumbwheel switch which determines the value of the 16-bit address trigger word. This switch is coded in hexadecimal. (Refer to the chart in Table 3-1 to convert other address codes.) NOTE: UNUSED ADDRESS INPUT LINES WILL ASSUME THE "1" STATE. HOWEVER, IF NOISE ON THESE LINES IS A PROBLEM WITH SOME SYSTEMS, IT IS RECOMMENDED THAT THESE UNUSED INPUTS BE GROUNDED AND TREATED AS "0's" WHEN USING THE HEX THUMBWHEEL SWITCH.

TRIG OUT - This is a BNC-type connector which provides a TTL output whenever the conditions described below are met. When the ADDRESS TRIGGER switch is in the SYNC mode, an active high pulse will appear at this output at the instant all input triggering conditions are met. When the ADDRESS TRIGGER switch is in the OFF mode, the BNC connector gives the user direct access to the internal trigger bus of the Model 100A. And finally, when the ADDRESS TRIGGER switch is in the ASYNC mode, an active high TTL level will appear at this output whenever the 16-bit address and Q_0 qualifier inputs are satisfied. This mode of operation is primarily intended for applications requiring the stand-alone word recognizing capabilities of the Model 10. (Refer to Section 8.0 for additional details.)



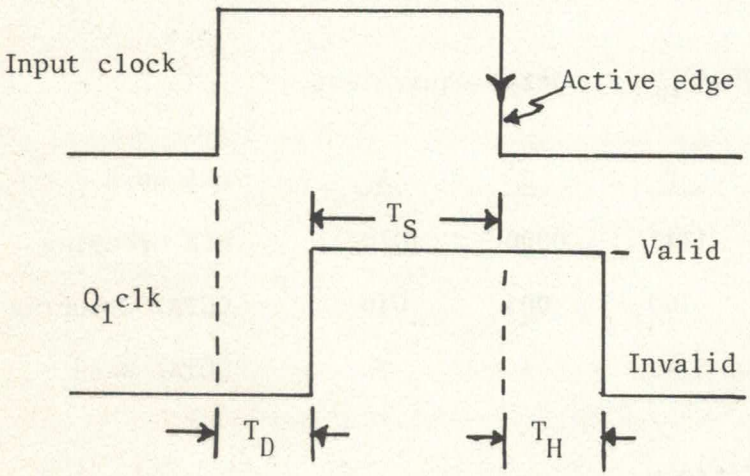
T_S = Q_1 set-up prior to positive edge of clock = 50ns min.

T_H = Q_1 hold time after positive edge of clock = 50ns min.

T_R = Release of Q_1 before negative edge of clock = 25ns min.

POSITIVE CLOCK EDGE SYSTEMS:

Q_1 MUST "BRACKET" RISING CLOCK EDGE



T_S = Q_1 set-up prior to negative edge of clock = 50ns min.

T_H = Q_1 hold time after negative edge of clock = 50ns min.

T_D = Delay of Q_1 after positive edge of clock = 25ns min.

NEGATIVE CLOCK EDGE SYSTEMS:

Q_1 MUST "BRACKET" FALLING CLOCK EDGE

Fig. 3-3. Clock qualifier (Q_1) timing requirements. Q_1 can be selected as "1," "0," or "X."

Table 3-1

CODE CONVERSION CHART

HEX	BINARY	OCTAL	BINARY
0	0000	0	000
1	0001	1	001
2	0010	2	010
3	0011	3	011
4	0100	4	100
5	0101	5	101
6	0110	6	110
7	0111	7	111
8	1000		
9	1001		
A	1010		
B	1011		
C	1100		
D	1101		
E	1110		
F	1111		

Example: Convert $(0F0A)_{HEX}$ to octal equivalent.

Procedure:		0	F	0	A	HEX Word
		0000	1111	0000	1010	HEX Grouping
0	000	111	100	001	010	OCTAL Grouping
0	0	7	4	1	2	OCTAL Word

Thus $(0F0A)_{HEX} = (7412)_{OCT}$

TRIG IND - This is a LED indicator on the front panel of the Model 10 which operates in parallel with the indicator on the Model 100A. In the OFF and SYNC modes, an illuminated LED signifies that the Model 100A/Model 10 integrated package is waiting for all trigger, qualifier, and delay requirements to be satisfied. When these conditions are met, both LEDs will turn off. In the ASYNC mode, the LEDs have no functions and will always remain on. The LED on the Model 10 is particularly useful when operating the unit in the stand-alone mode. In this mode, it provides information about the occurrence of a particular logic state.

INPUT DATA PROBES - The input probes are constructed out of multi-colored flat ribbon cable separated in groups as shown in Figure 3-4a. Each wire is terminated in a gold-plated "universal" pin connector which will readily interface with standard wirewrap pins, IC clips, and E-Z hooks (ball clips). See Figure 3-4b.

NOTE: WHENEVER CONNECTING THE MODEL 10 TO THE SYSTEM-UNDER-TEST, IT IS RECOMMENDED THAT THE BLACK (GROUND) PROBES BE CONNECTED FIRST. THIS WILL PREVENT DAMAGE TO THE INPUT BUFFERS IN THE EVENT THAT THE SYSTEM-UNDER-TEST AND THE MODEL 10 DO NOT HAVE A COMMON GROUND.

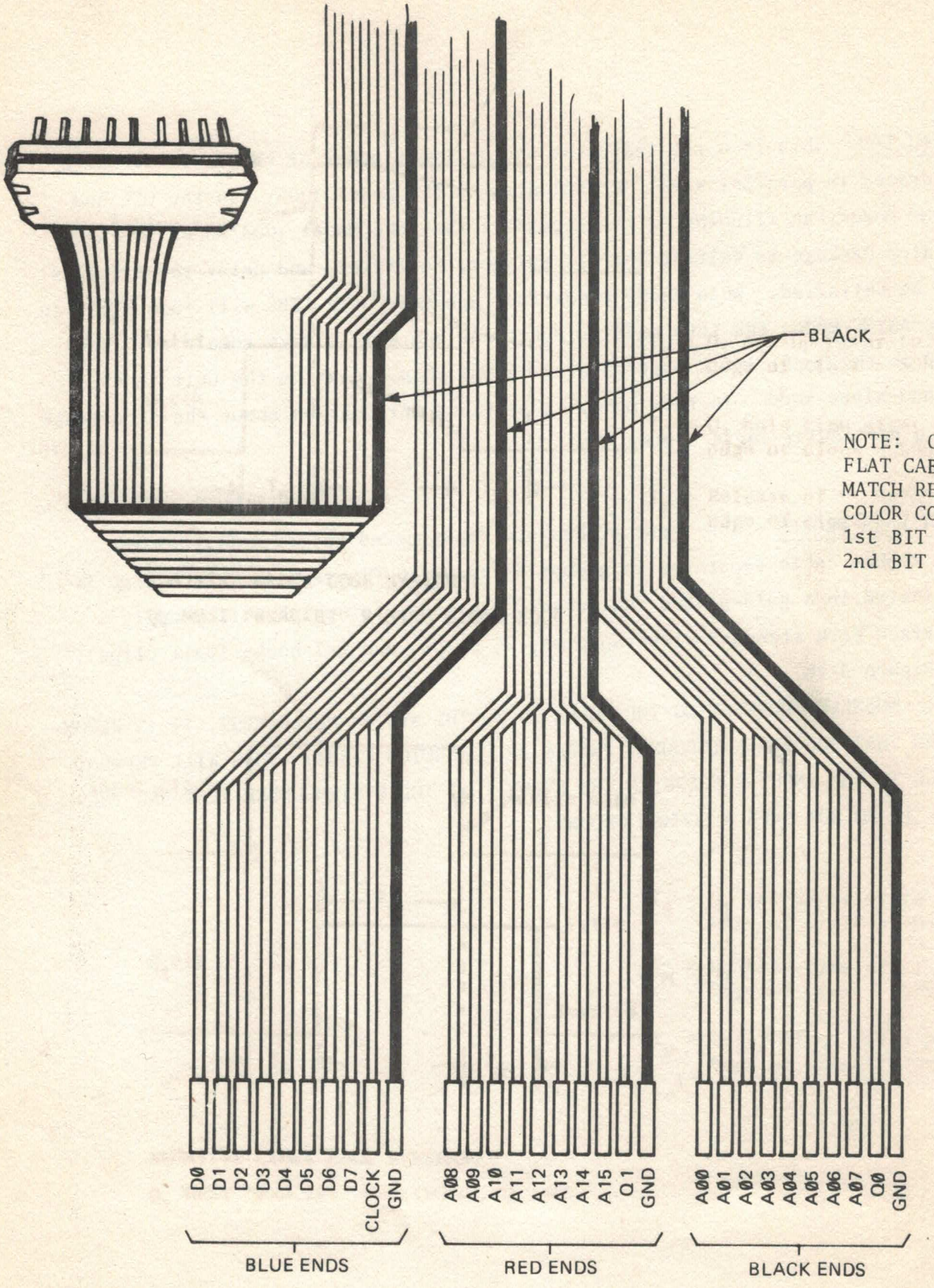


Fig. 3-4a. Model 10 input probe assembly signal definitions.

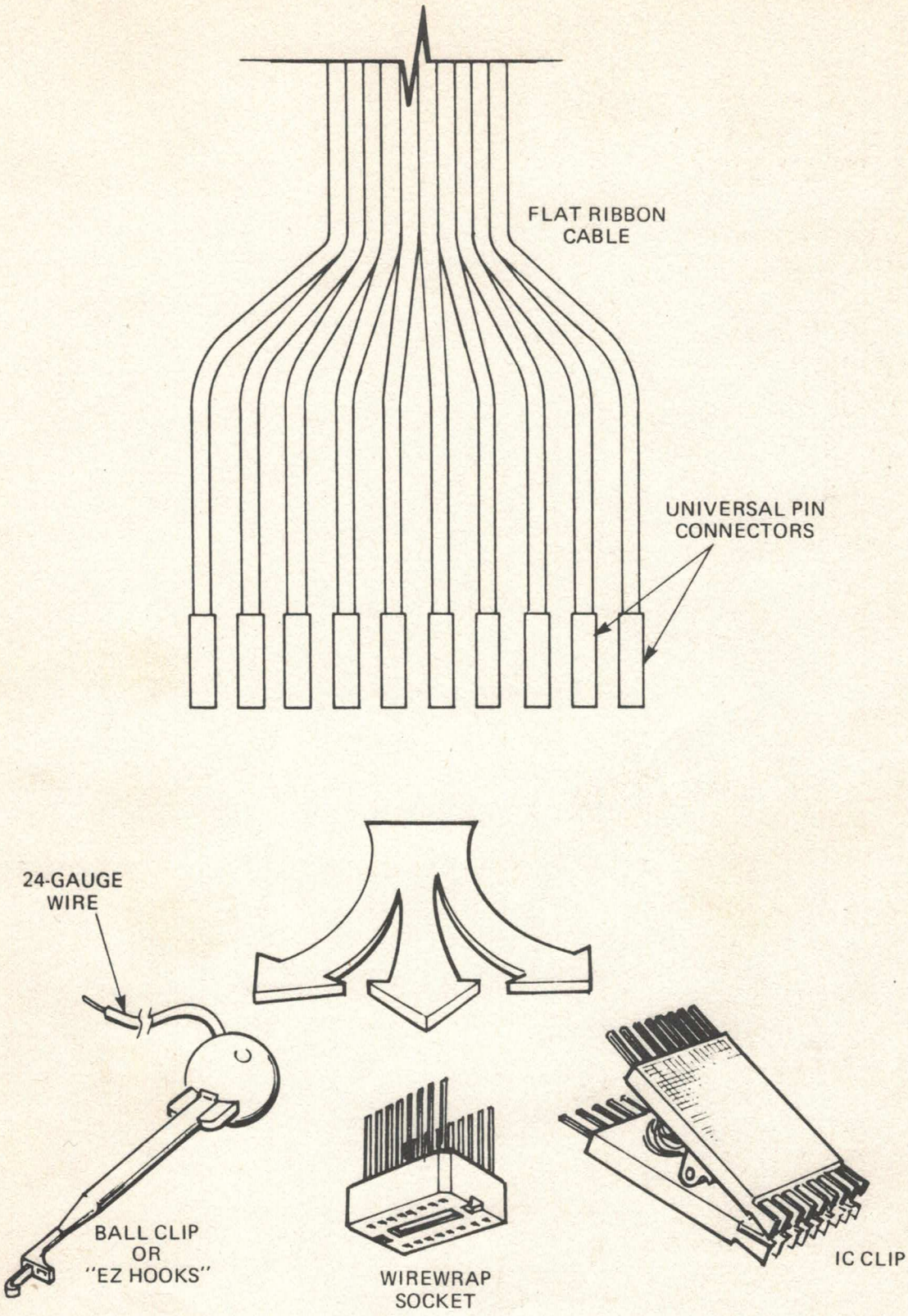


Fig. 3-4b. Data probe interfacing techniques.

4.0 HOW IT WORKS

The operation of the Model 10 Trigger Expander can be best understood by referring to the block diagram and the schematic in Figures 4-1 and 7-1, respectively.

U1, U2, U8 and U9 are configured to form an octal 3:1 multiplexer. DISPLAY MUX switch S11 selects the data byte, the upper address byte or lower address byte for collection by the Model 100A Analyzer.

U3, U4, U5 and U6 form a 16-bit address comparator. HEX address switches S1-S4 cause an inverted 16-bit address to appear on the input of the 16-bit comparator while the probe address inputs A0-A15 form the other inputs. All exclusive-OR gates are "wire-ANDed" so the output will be high only when the address on probe pins A0-A15 match the 16-bit address sent into the HEX thumbwheel switches. The output of the comparator is further qualified by trigger qualifier Q_0. This qualifier can be set to "1," "0," or "X" by switch S9. U7A forms the "wire-AND" function with the ADDTRIG+ signal.

The clock circuitry is comprised of U14A, U14B, U14C, U15A and U15B, along with switches S8 and S12. The clock qualifier Q_1 is buffered or inverted by U15A or U14A. Switch S8 selects either the buffer (straight-through path), inverter, or pull-up resistor for "1," "0," "X" qualification. Note that Q_1 is used to selectively sample data on the bus. For example, the Q_1 input can be connected to the R/W line to allow the analyzer to collect only STORE operations from the microprocessor's data bus.

The input clock is applied to U14B and U15B to generate both true and complement signals with minimum active edge skew. Switch S12A selects the inversion of the clock signal sent to the Model 100A and to U10A for address comparator sampling. S12B selects the positive clock polarity for use by the delay counters U11-U13 and trigger indicator flip-flop U10B. This scheme permits clock polarity selection with zero hold time for the data relative to the clock for the Model 10 in the stand-alone mode. (NOTE, HOWEVER, WHEN USING THE

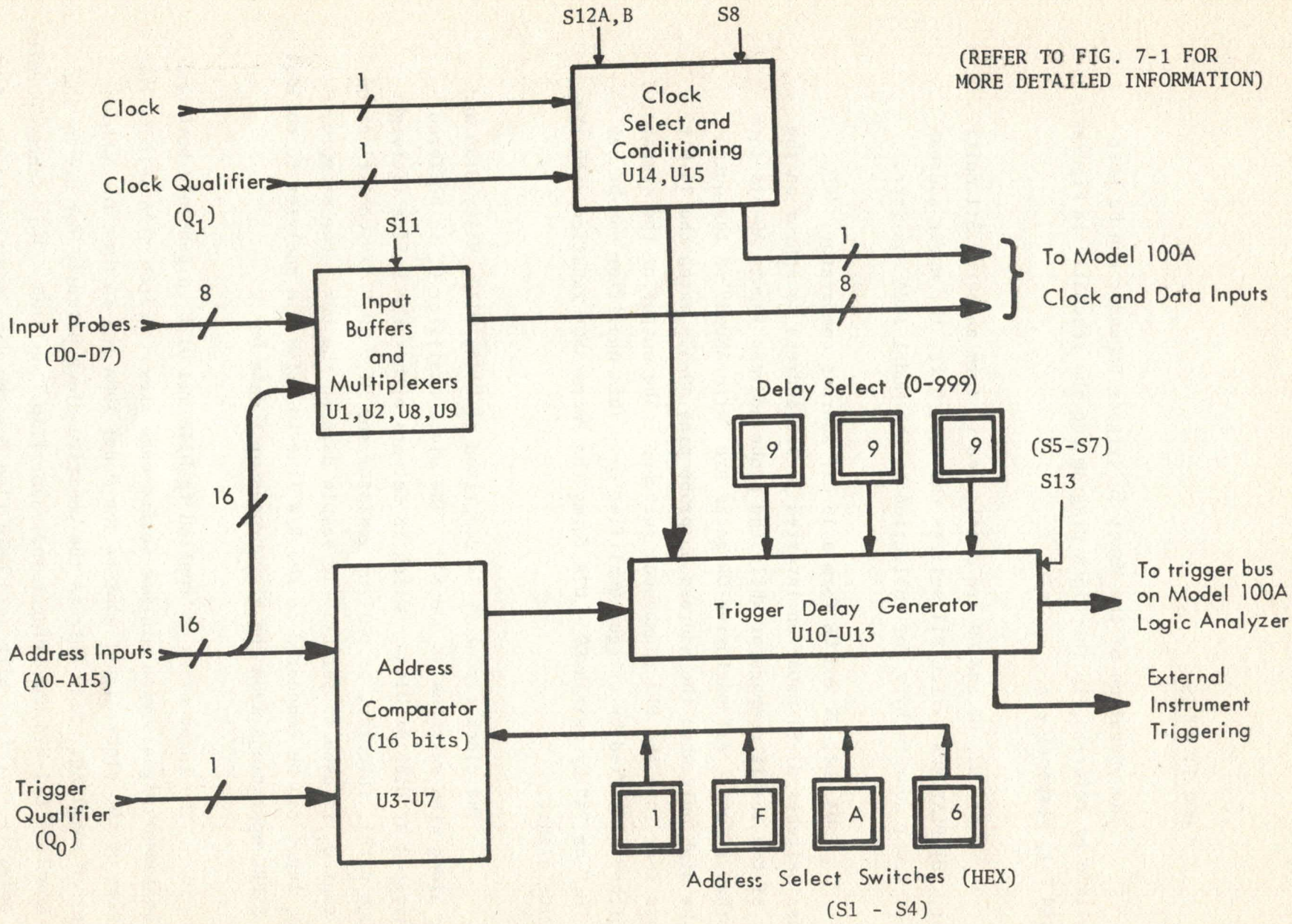


Fig. 4-1. Block diagram of Model 10 Trigger Expander.

MODEL 10 WITH THE MODEL 100A, THE MODEL 100A CLOCK POLARITY SWITCH SHOULD ALWAYS BE SET TO THE FALLING EDGE (↘) POSITION.)

U11-U13 and switches S5-S7 comprise the digital delay function of the trigger expander. Switches S5-S7 and resistors R17-R31 generate a "compliment of 9's compliment" 3-digit BCD number which is loaded into binary UP counters, U11-U13. This loading is performed every clock cycle until the trigger occurs and U10A is set. The counter mode controls are then switched to the count mode and UP counting proceeds on subsequent clock pulses. If delay mode switch S13A is set to the CLOCK position, the counter will be incremented each clock cycle after triggering has occurred. If S13A is in the TRIG position, the counter is incremented only when a valid address trigger word is present. In this way, it is possible to set the address switches--say at the beginning of a loop--and delay triggering of the analyzer for an integral number of loop iterations. For microprocessor loop analysis, this feature is far more useful than counting clock pulses particularly if the number of clock pulses per loop is not constant.

When the counter reaches the maximum count (999), TC+ goes high and enables the analyzer trigger bus via AND gates U7B and U7C. The inputs of this gate are controlled by switch S10. In the SYNC position, gates U7B and U7C satisfy the trigger bus when trigger flip-flop U10A has been set and the delay counter has reached terminal count (i.e., TC+ is high). Then, when data inputs to the Model 100A agree with the Model 100A input switches, the analyzer will trigger. When switch S10 is in the OFF position, all inputs to gates U7B and U7C are a logic "1" and the Trigger Expander has no effect on the triggering of the Model 100A. In the ASYNC position, S10 directly passes the address trigger bus ADDTRIG+ to the BNC output jack via gates U7B and U7C. This mode is useful when the Model 10 is functioning as an asynchronous word recognizer in the stand-alone mode.

When using the delay feature of the Model 10/Model 100A, several interesting and useful modes are possible. Table 4-1 describes what will be seen as the first word of the display for all four combinations of the POS/NEG time and CLOCK/TRIG delay switches. For positive time, the display is

Table 4-1

Delay Value Set To n ($1 \leq n \leq 999$)

MODEL 100A DISPLAY MODE	Model 10 Delay Select	
	CLOCK DELAY	TRIG DELAY
POSITIVE TIME	First word of truth table is data at MUX output n clock pulses after the occurrence of the trigger word.	First word of truth table is data at MUX output after n+1 trigger occurrences. (Note trigger is delayed by n occurrences.)
NEGATIVE TIME	First word of truth table is data at MUX output after (n-15) clock pulses.	First word of truth table is data at MUX output 15 clock pulses before n+1 trigger occurrences.

simply delayed for n clocks or triggers. (Note that analyzer triggering is delayed by the number of events set on the DELAY switches. Therefore, in the TRIG position, the analyzer actually displays after n+1 trigger occurrences.)

In the negative time mode, the interpretation is somewhat less obvious. For example, if the DELAY switch is set to "008" CLOCK delays, the first word of the truth table will be the output of the DISPLAY MUX a 8 minus 15 or -7 clock pulses relative to the trigger word. In other words, the seven data words preceding the trigger, the trigger itself, and the eight data words following the trigger will be displayed. This is a useful feature which allows viewing both pre- and post-triggering with a single data collection. In general, with the controls set for NEG TIME and TRIG DELAY, the display will show the 15 events preceding n+1 trigger occurrences and the trigger itself.

When triggering the Model 100A/Model 10 on unique addresses, the Model 100A trigger select switches are normally set to the "X" (don't care) position. When these switches are placed in the "1" and "0" positions, they can provide further qualification. This qualification on the output of the Model 10 multiplexer (Model 100A data inputs) occurs <u>after</u> all address qualification and delay requirements are satisfied. One easy way to visualize this is that in the POS TIME mode, the Model 100A trigger switches will place <u>additional</u> qualification on what will be the <u>first</u> word of the <u>display</u>. In the NEG TIME mode, the qualification occurs on what will be the <u>last</u> word of the <u>display</u>. When the display multiplexer switch is set to DATA, there will be a total of 24 bits (+ Q_0) which can specify the trigger : 16 address bits specified by the Model 10 ADDRESS switch and 8 data bits specified by the Model 100A trigger switches.

The open collector signal TRIGBUS+ is "wire-ANDed" to the Model 100A open collector trigger bus. Further "wire-AND" expansion of this bus is possible using the Model 10 trigger output BNC jack.

Reset switch S14 is in parallel with the Model 100A reset switch and has the same function. When the Model 10 is used as a stand-alone word recognizer, this reset switch can be used to arm the unit for a pending occurrence of the preset trigger word.

5.0 GETTING THE KIT TOGETHER

Although the Model 10 has two PC boards as compared to the single board in the Model 100A, it is actually easier to assemble. The reason is that there is no power supply to wire up, fewer switches to align, and only one BNC connector instead of four. The exploded view in Figure 5-3 illustrates these points.

It's important to note that all active components are tested before the kit leaves the factory. Therefore, you shouldn't have any difficulty getting the Model 10 to work properly as long as you carefully follow the step-by-step instructions in this section. In fact, it's a good idea to first familiarize yourself with all of the assembly steps and all of the parts of the Model 10 before you begin "getting it together."

The following is a list of recommended tools and some hints on their proper usage:

1. Low-power soldering station such as a Weller Model W-TCP, including moist sponge for wiping the tip: Use a small tip on the soldering iron and periodically clean it by wiping it on the moist sponge. When soldering, use 60/40 rosin core solder ONLY. Never, NEVER use acid core or externally applied fluxes. Also, never allow the tip to remain in contact with the PC board for more than 10 seconds. If you're not getting a shiny solder joint after applying the tip of the iron and the solder for a few seconds, then something must be wrong with the iron or solder you're using. (The Model 10 PC board is specially treated so that the solder should flow quickly and easily.)

2. Hex wrench: The easiest way to install the BNC connector is to use a ½" hex wrench. If one is not available, use pliers--but be sure you're able to tighten the connector securely without damaging anything.

3. Small pair of wire cutters: Use these to trim the leads of all resistors, capacitors, and thumbwheel switches after soldering. It's not necessary to trim the leads of any of the IC sockets (except possibly J1).

4. Small pair of long nose pliers: Use these to carefully make the bends required to install the resistors and axial lead capacitors. (You can make this job a lot easier if you have one of those commonly available wedge-shaped, plastic lead bending tools.)

5. An inexpensive, 2X magnifying glass: This is a great way to inspect solder joints. Scan the board systematically and you'll be surprised what kind of potential problems even a low-cost, low-power, magnifying glass can uncover for you.

6. Patience: This is the most useful tool of all. If you take your time and inspect each step along the way, you'll save yourself a lot of grief later.

Misc. Assembly Hints - Before you begin, consider the following general hints which will assist you in performing the assembly of the PC boards:

1. Use the Parts List to identify all components.

2. "Color in" components as you locate them in the assembly drawings of Figure 5-1 and 5-2.

3. Install all resistors so that the tolerance band is toward the right for all those that are horizontally-oriented; and facing toward the bottom of the board for all those that are vertically-oriented. This will help you to rapidly identify resistor values for later checkout and troubleshooting. (A resistor color-code chart is provided at the rear of the manual.)

4. Install all components of the same height at one time. Then lay a piece of cardboard or other flat material over the components to hold them in place as you turn the PC board over for soldering.

5. Never, NEVER use flux remover on the PC board after any of the rockers, paddles, or thumbwheel switches are installed. Even the vapor from the solvent can destroy the lubrication of the switches.

6. Note that one of the sockets supplied with the kit is a high-profile 16-pin DIP socket (J1). Make certain that this socket is mounted at the upper left-hand-corner of Board 2. (In some kits, this socket is a wire-wrap type, in others it has solder tails: either type is acceptable.)

7. Note also that the interconnecting plug (P1) for J1 has two different pin diameters: the pins coming out of one side are smaller in thickness than the pins on the opposite side. MAKE CERTAIN THAT THE LARGER DIAMETER PINS ARE INSERTED INTO THE UNDER SIDE OF BOARD 1 AS SHOWN IN FIGURE 5-3; OTHERWISE P1 WILL NOT MATE WITH J1.

The parts list for the Model 10 is shown next. If you find any discrepancies or damaged components prior to assembly, write to Paratronics, Inc. describing your problem so we can take the appropriate action.

Table 5-1

MODEL 10 PARTS LIST

Board 1:

All resistors are ¼-watt, 5% tolerance:

R33-R40, R44	4.7K ohm
R41-43	1.0K ohm
R45	470 ohm
C13	15pf ceramic disc capacitor
C9	47uf 15V electrolytic capacitor
C10-C12	.1uf 50V ceramic disc capacitor
U14	SN74LS132/9LS132 quad 2-input NAND schmidt trigger (15-volt inputs only)
U15	SN74LS32/9LS32 quad 2-input OR gate (15-volt inputs only)
U10	SN74LS73 dual JK flip-flop
U7	SN74S15 Schottky triple 3-input AND gate with open collector outputs
S8-S11	3-position double-throw paddle switch
S12-S13	double-pole-double-throw rocker switch
S14	double-pole-double-throw rocker switch with spring return
L1	LED HP5082-4860 or equivalent
P1	double-male 16-pin DIP plug
Misc.	PC board, four 14-pin IC sockets, mounting hardware

Board 2:

All resistors are ¼-watt, 5% tolerance:

R1-R16	4.7K ohm
R17-R28 R32	1.0K ohm
R29-R31	220 ohm

Board 2 continued

C1	47µF 16V electrolytic capacitor
C2-C8	.1µF 50V ceramic disc capacitor
U1, U2, U8, U9	SN74LS367/9LS367 HEX three-state buffer (15-volt inputs only)
U3, U4, U5, U6 SIGNETICS ONLY	SN74LS136/9LS136 quad EXCLUSIVE-OR gates with open collector outputs (15-volt inputs only)
U11, U12, U13	SN74LS160 or SN74LS162 decimal counters
S1-S4	Hexadecimal (16-position) thumbwheel switch with end plates
S5-S7	Decimal (10-position) thumbwheel switch with end plates
J1	16-pin high profile DIP socket for mating with P1 on Board 1
J2	50-pin flat ribbon header
Misc.	Flat ribbon and input probe assembly; BNC connector; mounting hardware; four 14-pin sockets; seven 16-pin sockets; case; hookup wire; etc.

ASSEMBLY INSTRUCTIONS

STEP	PROCEDURE	FIGURE
	Steps 1-7 apply to the assembly of Board #1. This is the smaller of the two boards. Note that all components in the following steps (except the interconnecting DIP plug in step 7) are inserted from the labeled side.	
(✓) 1.	Mount and solder all resistors in place. Before soldering, double-check to be sure that all resistors are properly located.	5-1
(✓) 2.	Mount and solder four 14-pin IC sockets in place.	5-1
(✓) 3.	Mount and solder the 0.1uF capacitors in place. Then mount the polarized 47uF capacitor, making certain that it is oriented properly.	5-1
(✓) 4.	Next, mount the two DPDT rocker switches S12 and S13. Then mount the DPDT spring return rocker switch, S14, MAKING SURE THAT THE CUTOFF MOUNTING EAR FACES TOWARDS RESISTOR R42 (near the top of the board). NOTE: BEFORE SOLDERING IN PLACE, MAKE CERTAIN THAT THESE SWITCHES ARE SEATED ALL THE WAY DOWN AND ARE PERPENDICULAR TO THE PC BOARD; OTHERWISE, THE TOP OF THE CASE WILL NOT MATE PROPERLY. (Hint: Hold the board vertically as you solder the switches in place so that you can be sure that they are truly perpendicular. Then temporarily install the top cover and check that the cutouts permit free switch movement.)	5-1

CAUTION

DO NOT USE FLUX REMOVER IN STEPS 4 and 5: DAMAGE TO SWITCH LUBRICATION WILL RESULT.

MODEL 10 BOARD 1

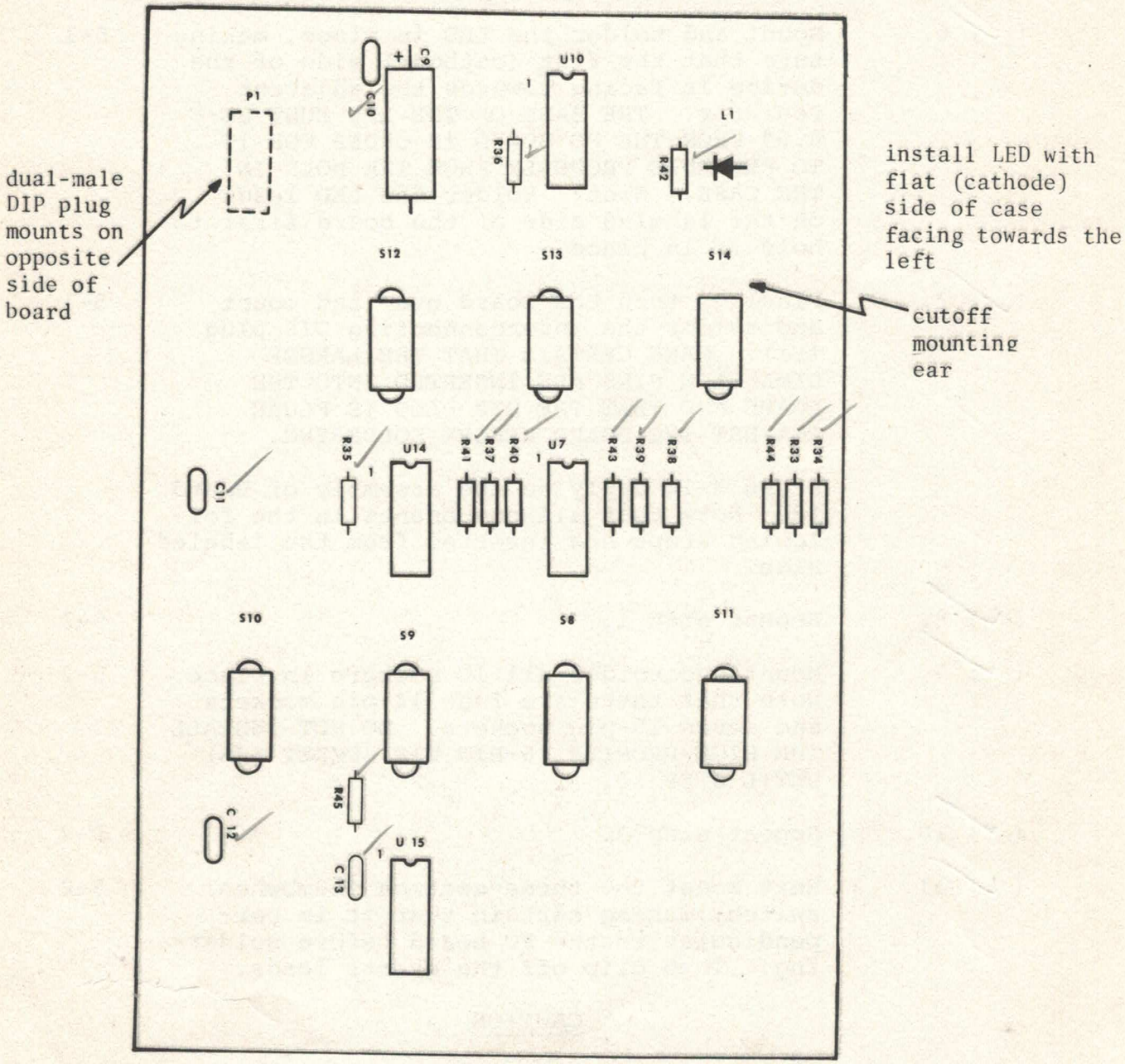


Fig. 5-1. Model 10 Board #1 component layout.

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STEP	PROCEDURE	FIGURE
(✓) 5.	Now mount the four paddle switches. Observe the note in step 4 before soldering in place.	5-1
(✓) 6.	Mount and solder the LED in place, making sure that the flat (cathode) side of the device is facing towards the adjacent resistor. THE BASE OF THE LED MUST BE 0.9" FROM THE PC BOARD IN ORDER FOR IT TO PROTRUDE PROPERLY FROM THE HOLE IN THE CASE. Hint: Solder the LED leads on the labeled side of the board first to hold it in place.	5-1
(✓) 7.	Finally, turn the board over and mount and solder the interconnecting DIP plug (P1). MAKE CERTAIN THAT THE LARGER DIMENSION PINS ARE INSERTED INTO THE BOARD AND THAT THE DIP PLUG IS FLUSH AGAINST THE BOARD BEFORE SOLDERING.	5-1
	Steps 8-14 apply to the assembly of Board #2. Note that all components in the following steps are inserted from the labeled side.	
(✓) 8.	Repeat step 1.	5-2
(✓) 9.	Mount and solder all IC sockets in place. Note that there are four 14-pin sockets and seven 16-pin sockets. DO NOT INSTALL THE HIGH-PROFILE 16-PIN DIP SOCKET (J1) UNTIL STEP 14.	5-2
(✓) 10.	Repeat step 3.	5-2
(✓) 11.	Next mount the three-section thumbwheel switch, making certain that it is perpendicular to the PC board before soldering. Then clip off the excess leads.	5-2
	CAUTION	
	DO NOT USE FLUX REMOVER IN STEPS 11 and 12.	

MODEL 10 BOARD 2

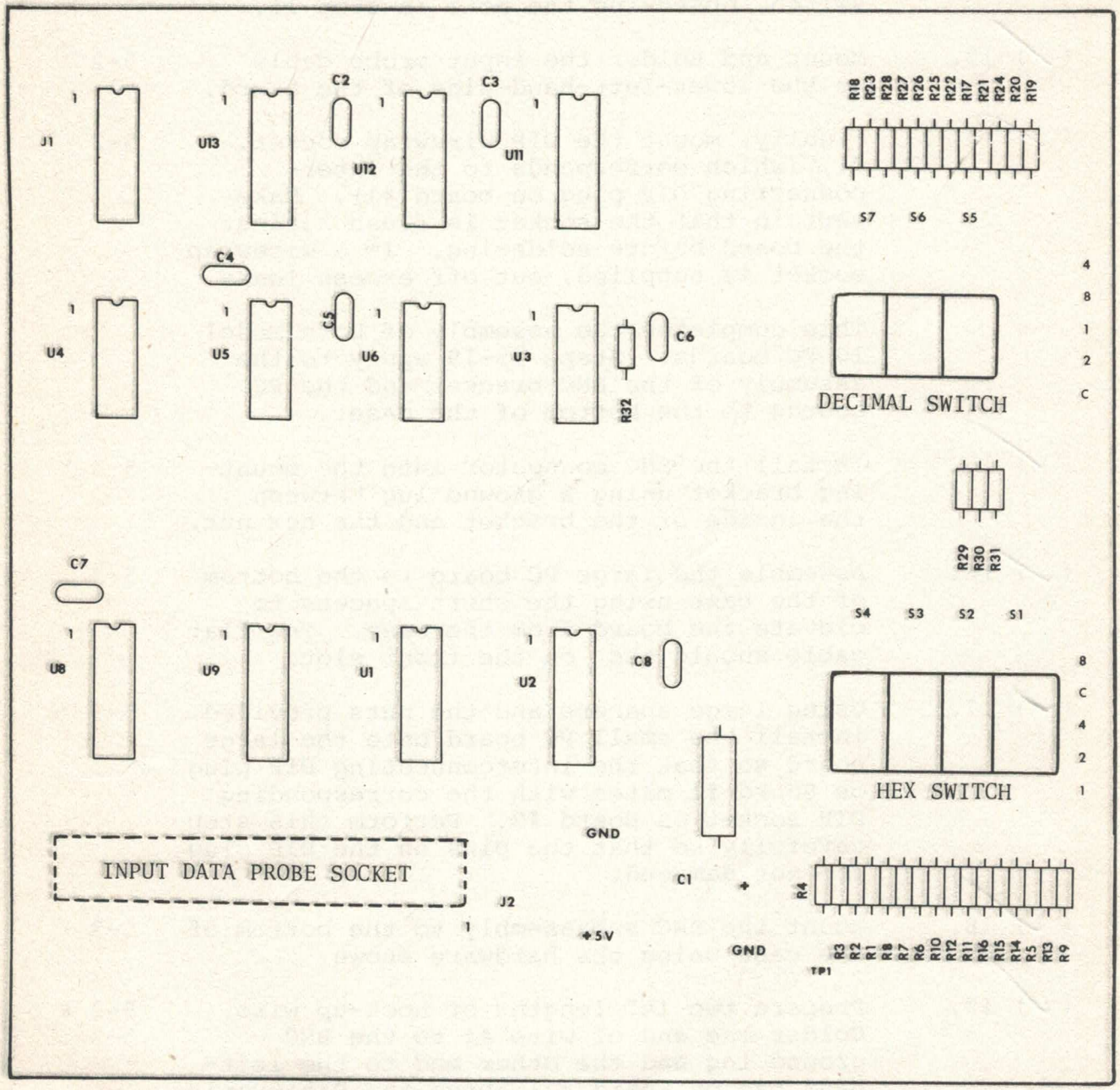


Fig. 5-2. Model 10 Board #2 component layout.

STEP	PROCEDURE	FIGURE
(✓) 12.	Now mount the four-section thumbwheel switch, observing the note in step 11.	5-2
(✓) 13.	Mount and solder the input probe cable at the lower-left-hand-side of the board.	5-2
(✓) 14.	Finally, mount the DIP wirewrap socket, J1, (which corresponds to the interconnecting DIP plug on board #1). Make certain that the socket is flush against the board before soldering. If a wirewrap socket is supplied, cut off excess leads. This completes the assembly of both Model 10 PC boards. Steps 15-19 apply to the assembly of the BNC bracket and the PC boards to the bottom of the case.	5-2
(✓) 15.	Install the BNC connector into the mounting bracket using a ground lug between the inside of the bracket and the hex nut.	5-3
(✓) 16.	Assemble the large PC board to the bottom of the case using the short spacers to elevate the board from the case. The flat cable should rest on the front slot.	5-3
(✓) 17.	Using large spacers and the nuts provided, install the small PC board onto the large board so that the interconnecting DIP plug on Board #1 mates with the corresponding DIP socket on Board #2. Perform this step carefully so that the pins on the DIP plug are not damaged.	5-3
(✓) 18.	Mount the BNC subassembly to the bottom of the case using the hardware shown.	5-3
(✓) 19.	Prepare two 1½" lengths of hook-up wire. Solder one end of wire #1 to the BNC ground lug and the other end to the left-hand pad on Board #2, above the Paratronics, Inc. label. Solder one end of wire #2 to the solder post on the BNC connector, and the other end to the right-hand pad above the Paratronics, Inc. label.	5-2 & 5-3

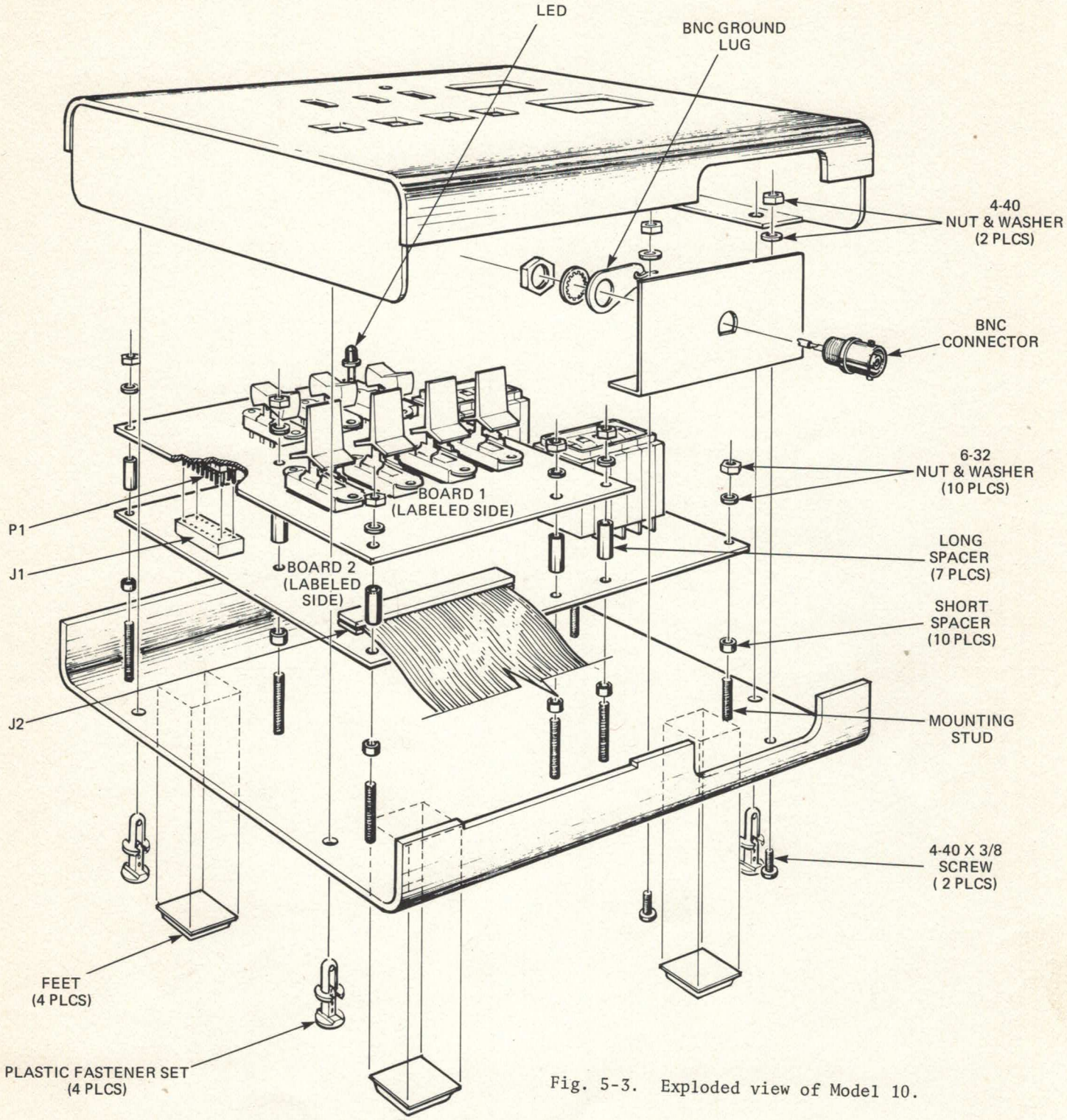


Fig. 5-3. Exploded view of Model 10.

STEP	PROCEDURE	FIGURE
(✓) 20.	Install all IC's, making absolutely sure that they are located and oriented properly; otherwise, they may be damaged when power is later applied. Your Model 10 is now ready for checkout. Please go to the next section before installing the top cover. NOTE: FOR TROUBLESHOOTING PURPOSES, THE PC BOARDS CAN BE REMOVED FROM THE BOTTOM OF THE CASE AS A UNIT. TO DO THIS, CAREFULLY UNSOLDER THE TWO BNC LEADS AT THE BNC CONNECTOR. THEN LIFT THE TWO BOARDS TOGETHER FROM THE THREADED CASE POSTS. HINT: INSERT FIVE #6 SCREWS (1½" long) IN THE MOUNTING HOLES TO HOLD THE LONG SPACERS AND THE TWO BOARDS TOGETHER. TIGHTEN DOWN WITH #6 HEX NUTS. (IF IT BECOMES NECESSARY TO SEPARATE THE BOARDS, A 16-PIN FLAT RIBBON ADAPTOR CABLE WILL BE REQUIRED TO INTERCONNECT THE TWO BOARDS.)	
(✓) 21.	After satisfactory checkout, install the top cover to the bottom of the case using the four plastic fastener sets. If the optional baseplate is used, the fasteners must be inserted into the baseplate first. NOTE: IF IT IS NOTICED THAT THE SWITCHES DO NOT LINE UP WITH THE MOUNTING HOLES, IT WILL BE NECESSARY TO LOOSEN THE PC BOARD NUTS AND SLIDE THE BOARDS AROUND SLIGHTLY. IF THIS DOESN'T WORK, THEN YOU MUST REMOVE ONE OR BOTH PC BOARDS FROM THE BOTTOM OF THE CASE AND DESOLDER, ADJUST, AND RESOLDER THE MISALIGNED SWITCH.	5-3
(✓) 22.	Install the four press-on feet to the bottom of the case. If the optional baseplate is used, mount the Model 10 to the baseplate first and then use the feet cutouts as a guide.	5-3

* * *

THIS COMPLETES THE ASSEMBLY OF THE MODEL 10

6.0 CHECKING IT OUT

The Model 10 can be checked out either with the Model 100A or with an auxiliary +5V ±5% (300 ma) power supply. For operation and checkout with the Model 100A, the 16-pin DIP plug portion of the flat cable assembly of the Model 10 should be inserted into the Model 100A input socket. This requires removal of the Model 100A top cover by pulling out FOUR plastic fasteners (two on each side). The original input probe plug and cable of the Model 100A are not used.

For operation and checkout without the Model 100A, +5V should be CAREFULLY applied to pin 9 of the 16-pin DIP plug and ground at pin 16.

6.1 PRELIMINARY CHECKOUT

Leave all input probes of the Model 10 unconnected. Set the controls of the Model 10 as follows:

Control	Setting
Q_0	"X"
Address select	"FFFF"
All other switches	(settings not important)

Now monitor pin 6 of U7 with a logic probe, scope or voltmeter. It should be a logic 1 (at approximately +5V) indicating that the address comparator has a "match." (Floating address inputs are treated as logic 1's.) For all other address switch settings, or if the Q_0 qualifier is switched to the "0" position, pin 6 of U7 should be at the logic 0 (0.4V) state.

6.2 CHECKING OUT THE MODEL 10 WITH THE MODEL 100A

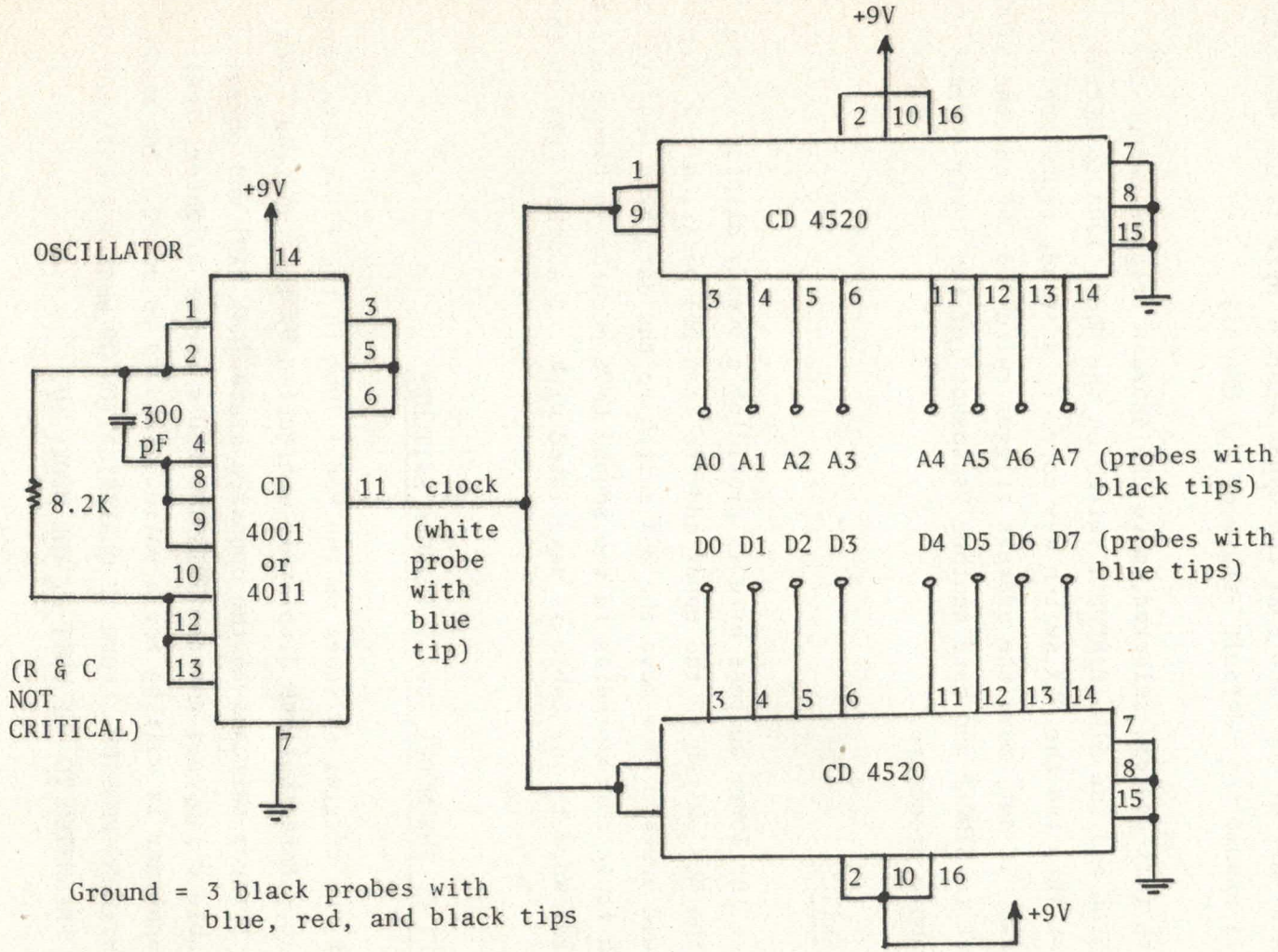
Connect the Model 100A HOR, VERT, and BLANK outputs to an oscilloscope for display. The test circuit in Figure 6.2-1 or a similar one which cycles at least 16 bits should be used.

INITIAL SET-UP

Connect address inputs A0 through A7 and data inputs D0 through D7 to the test circuit. (Leave A8 through A15 unconnected at this time.) Connect the clock input to the test circuit clock. Set the controls on the Model 100A and Model 10 as follows:

Model 100A Control Settings	
Display format	HEX
Clock edge	negative-going
Display mode	POS TIME
SINGLE/REPEAT	SINGLE
D0-D7	ALL "X"

Model 10 Control Settings	
Clock edge	positive-going
Delay select	CLOCK
DELAY	"000"
Address trigger	OFF
Q_0, Q_1 qualifiers	"X"
ADDRESS	"FF00"
Display MUX	LO ADDR



CD 4520 = CMOS DUAL
BINARY COUNTER

Fig. 6.2-1. Simple CMOS counter circuit for checking out the Model 10.

OBTAINING A VALID ADDRESS FOR TRIGGERING

Press either RESET switch and note the top word in the truth table, which is a "randomly" selected value since the address trigger switches are OFF and the upper 4 bits and lower 4 bits of the first dual CMOS binary counter may not be counting together. Now change the HEX address to read FFXY where X and Y are the HEX equivalents of the top word in the truth table. (The FF portion of this address is a result of the fact that the upper address byte is not connected and therefore will assume the "default" state of all ONE's.)

With this address selected, move the address trigger switch on the Model 10 to SYNC and the SINGLE/REPEAT switch on the Model 100A to REPEAT. If the address set into the the HEX switch was correct, a steady truth table display should appear. If not, move the address trigger switch to OFF and the SINGLE/REPEAT switch back to SINGLE and take another "snapshot" of the lower address byte. Then repeat the above procedure.

TESTING THE MUX SWITCH

Once the lower address byte is providing a steady display in the SYNC mode, move the MUX switch to the upper address (center) position: a display of all ONE's should appear. Now move the MUX switch to the data byte position and observe the truth table corresponding to the second CMOS counter in Figure 6.2-1. Note that the first word in the table is associated with the address FFXY in the HEX switch.

TESTING THE AFFECT OF THE MODEL 100A'S TRIGGER SWITCHES

Set the trigger switches on the Model 100A to the first data word in the truth table. Note that the display is unaffected by this setting. Now move one or more trigger switches to the opposite state (not "X") and observe that the truth table disappears and the TRIG IND LED's become brighter, indicating that the analyzer is waiting for a valid data word to occur. THE MODEL 100A'S TRIGGER SWITCHES PROVIDE A FORM OF QUALIFICATION ON WHATEVER DATA (OR ADDRESS BYTES) ARE PRESENTED TO THE UNIT BY THE MODEL 10.

TESTING THE DELAY

Before proceeding, check to be sure that the CLOCK/TRIG switch on the Model 10 is set to CLOCK. Then return all trigger switches on the Model 100A to "X." The truth table for the data should again appear steady on the CRT. Now, switch the Model 100A to the SINGLE mode to store the display and set the trigger switches to the third data byte in the truth table, counting from the top. Press either RESET switch and observe that the truth table disappears. Next, set the delay switch to 002 and observe that the truth table reappears, with the third data byte now at the top of the table. Move the delay to 003, press RESET, and note that the analyzer does not trigger. This exercise illustrates how the delay feature of the Model 10 and the trigger switches of the Model 100A can be used to trigger on a data word occurring up to 1000 clock pulses after the address word.

Move all of the trigger switches on the Model 100A back to "X," and the SINGLE/REPEAT switch back to REPEAT. Then set the delay to 000 and the MUX switch to the lower address byte position and a steady truth table should appear as before. Now increment the delay by one integer at a time and note that the entire table shifts up towards the top of the screen as the delay is increased. When 015 is set into the delay, the word that was at the bottom of the table with a delay setting of 000 will now appear at the top.

Now set the delay back to 000 and change the POS/NEG TIME switch on the Model 100A to NEG. Note that the lower address byte, which previously appeared at the top of the truth table, is now at the bottom. Next, increment the delay in integer steps and watch this word move towards the top of the display. When 015 is reached, the lower address byte set into the HEX switch should appear at the top of the screen.

TESTING THE UPPER ADDRESS BYTE

Interchange the probes corresponding to the lower address byte (black tips) and the upper address byte (red tips) and change the HEX address

switch to XYFF. Then repeat the above steps.

TESTING THE TRIG FEATURE

Set the delay switch back to 000 and switch the CLOCK/TRIG switch to TRIG. Now, increment the "hundreds" position of the delay switch, i.e., 100, 200, 300, etc. As this setting is increased, the number of input trigger words which must occur before a truth table will be displayed increases one-hundred-fold per step. Depending on the clock frequency of the test circuit oscillator, the display should begin to flicker as the delay is increased since greater intervals of time must pass before each truth table is permitted to occur.

TESTING THE QUALIFIER

The qualifiers Q_0 and Q_1 can now be statically checked out with a simple test. With both Q_0 and Q_1 input probes left open, the Model 100A/Model 10 should trigger with the qualifiers in the "1" or "X" positions and not trigger when either is to "0."

Now repeat the test with both qualifier inputs grounded. The analyzer should trigger in the "0" or "X" positions, but not trigger if either qualifier is set to "1."

6.3 CHECKING OUT THE MODEL 10 AS A STAND-ALONE WORD RECOGNIZER

In order to check out the Model 10 as a stand-alone word recognizer, the TRIG output should be viewed with an oscilloscope which should be triggered independently from the circuit under test. For example, the falling edge of the most significant bit of the test circuit should be used to trigger the scope by connecting the MSB to the external trigger input of the scope. The word recognizer should be connected to the test circuit as described in Section 6.2 above. Now, the relative timing of the output pulse with respect to the counter MSB can be observed as different delay values and address values are set into the word recognizer. This excercise illustrates how the Model 10 can add digitally delayed sweep capability to an ordinary scope.

If any difficulty in checkout is encountered, refer to Section 7.0 for troubleshooting guidelines. If everything checks out, install the top cover using the four plastic fasteners as described in Section 5.0, assembly step 21.

7.0 WHAT IF IT DOESN'T WORK RIGHT?

Although all active components of each Model 10 kit are thoroughly tested at the factory, it's still possible that one will fail during or shortly after assembly. However, as shown in Figure 7-1, the circuit is straightforward and relatively easy to troubleshoot; but if you can't find the problem, we'll do everything we can to help.

7.1 CHECKING YOUR WORK

A large majority of problems associated with kit-building can be traced to minor errors in assembly. The following checklist will help you find most assembly-related problems:

1. Check to make certain that all IC's are located correctly and oriented with pin 1 in the proper position. If an IC has been installed backwards and power is applied, it will probably overheat and be destroyed. See Figures 5-1 and 5-3.

2. Check all resistors to make sure they are the proper value and in the proper position.

3. Make sure all capacitors are installed correctly. Check the polarity of the two electrolytic types.

4. Inspect all solder joints. A low-power (2X) magnifying glass is useful here. Check to make sure all connections are shiny and that there are no solder bridges shorting to adjacent pads.

5. Make certain that P1 on Board 1 and J1 on Board 2 mate correctly.

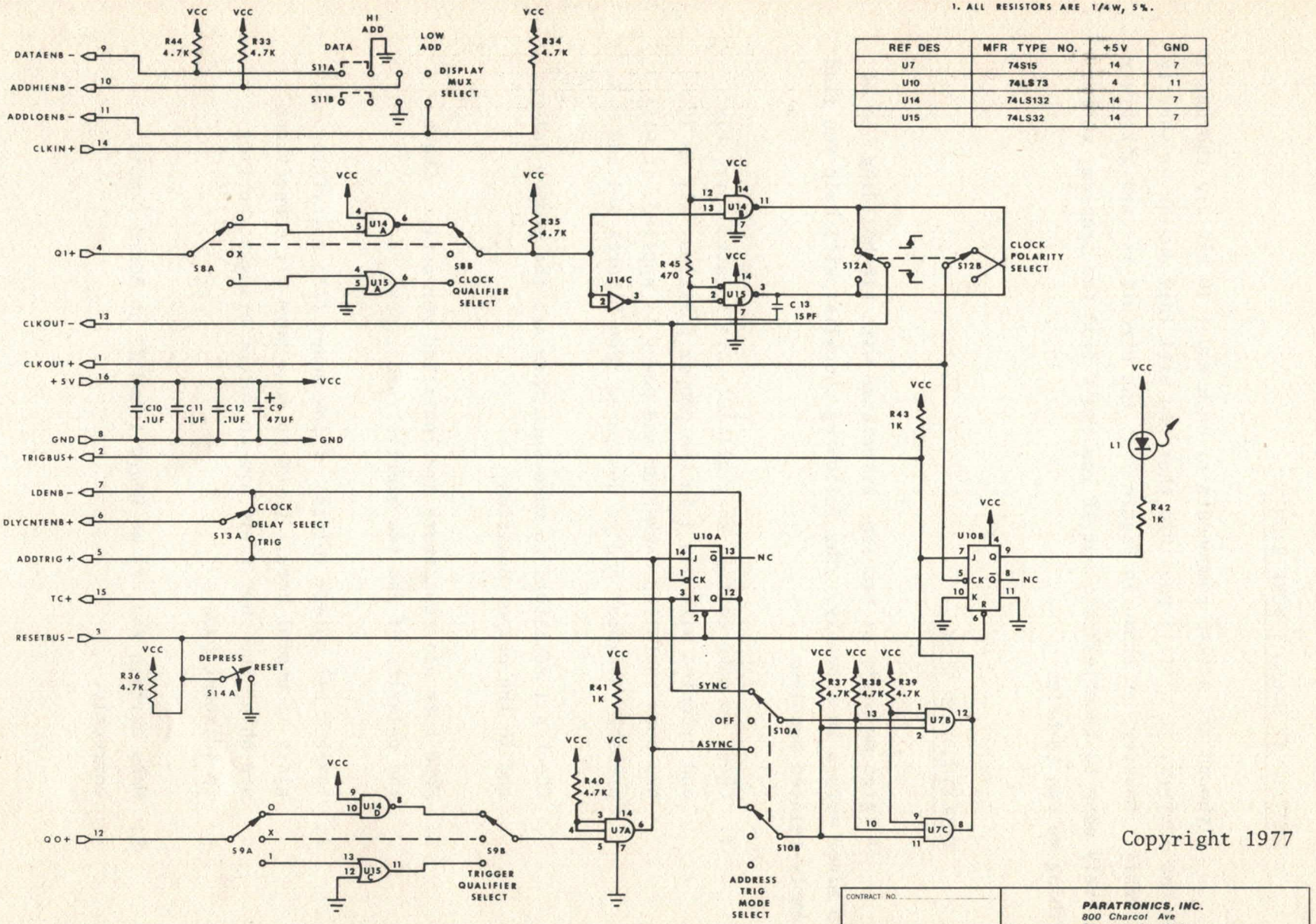
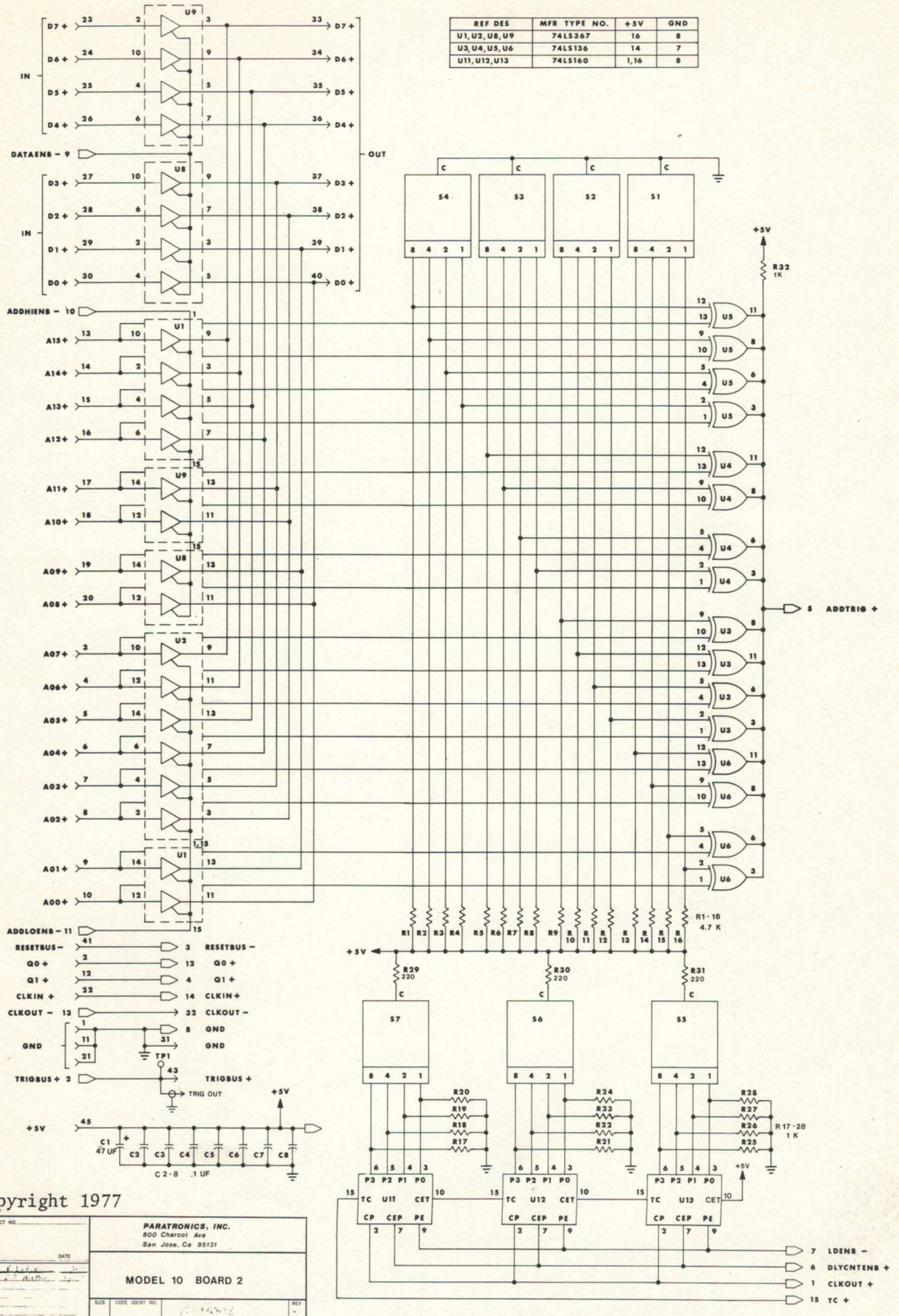


Fig. 7-1a. Model 10 Board 1.

CONTRACT NO.	PARATRONICS, INC. 800 Charcot Ave San Jose, Ca 95131		
APPD / DATE	MODEL 10 BOARD 1		
DR – WILSON	SIZE	CODE IDENT NO.	REV.
CHK – F. Matthews 1/11/77		1C-0002	D
STRU	SCALE	SHEET OF	
MATL			
T.C.			
PKG.			
ENGR – F. Matthews 1/–			
DSGN SUPV			



CONTRACT NO.	PARATRONICS, INC. 800 Charcot Ave San Jose, Ca 95131
APPD DATE	MODEL 10 BOARD 2
DR CHK STRU MATL TC PKG ENGR SSN SUPV	SIZE CODE IDENT NO. REV SCALE SHEET OF

Fig. 7-1b. Model 10 Board 2.

TABLE 7-1

MODEL 10 TRIGGER EXPANDER TROUBLESHOOTING CHART

SYMPTOM	PROBABLE CAUSE	REMEDY
DATA, HIADD, or LOADD bit(s) stuck	Open connection on input cable or failure of U1, U2, U8, or U9.	Trace continuity to identify open probe. Replace (or swap) 74LS/9LS367 to locate failed IC.
NO TRIGGERING (ADDTRIG+ always at logic 0)	Failure in input probe lines or failure in U3, U4, U5, or U6.	Leave all address inputs open. Set ADDRESS to "FFFF" and Q_0 to X. Unplug U3-U6 from their sockets one at a time to determine which is pulling ADDTRIG+ low. Swap to determine if input or IC is at fault.
DELAY PROBLEMS	Resistors R17-R31 installed incorrectly, or one or more of counter IC's U11-U13 have failed.	Try and locate failed decade and isolate by swapping IC's U11-U13. With delay set to "000," pin 15 of each counter should be at a logic 1 after input is clocked.
CLOCK or QUALIFIER PROBLEM	Poor solder joints on switches S8, S9 or S12. U14 or U15 failed. Open input probe on clock, Q_0 or Q_1.	Isolate problem by probing clock or qualifier signals from input cable through U14 or U15 and switches.

If no obvious assembly problems are detected, try and locate the symptom in Table 7-1. If your difficulty is not covered by the table, write to us for assistance:

Customer Service Dept.
Paratronics, Inc.
800 Charcot Avenue
San Jose, CA 95131

NOTE: DO NOT RETURN THE MODEL 10 WITHOUT OUR AUTHORIZATION. See Section 11.0 for complete information concerning service.

8.0 OPERATING THE MODEL 10 BY ITSELF AS A WORD RECOGNIZER

The Model 10 Trigger Expander was designed to operate both with the Model 100A logic analyzer and as a stand-alone word recognizer. As a stand-alone word recognizer, an external +5V ±5% 300 ma power supply is required. Power should be carefully supplied via the 16-pin input plug with ground at pin 16 of the plug and +5 volts at pin 9. No connection should be made to the other pins of the 16 pin DIP plug. A typical stand-alone application is shown in Figure 8-1.

8.1 SYNCHRONOUS OPERATION

For operation in the synchronous mode, the Model 10 ADDRESS TRIGGER mode switch must be set to the SYNC position. A signal for trigger qualification can be connected to the Q_0 input and selected by the three-position Q_0 switch. If the trigger qualifier is not used, the switch should be set to the "X" position; otherwise the "1" or "0" position can be selected as appropriate.

The clock may be qualified with the input line Q_1. The set-up and hold requirements are described in Figure 3-3. The sampling of the address and qualifier are determined by which input clock edge is selected by the clock polarity switch.

In operation, the address inputs of the Model 10 are connected to the circuit-under-test. The desired trigger word (up to 16 bits) is set into the HEX address thumbwheel switches. For best results, unused address inputs should be grounded and the corresponding bits of the address select switch should be set to a logic 0. For example, if address bits A_{15} and A_{14} are unused, the inputs should be grounded and the two most significant bits should be set to 0. This corresponds to HEX address 0-3. If an unused address

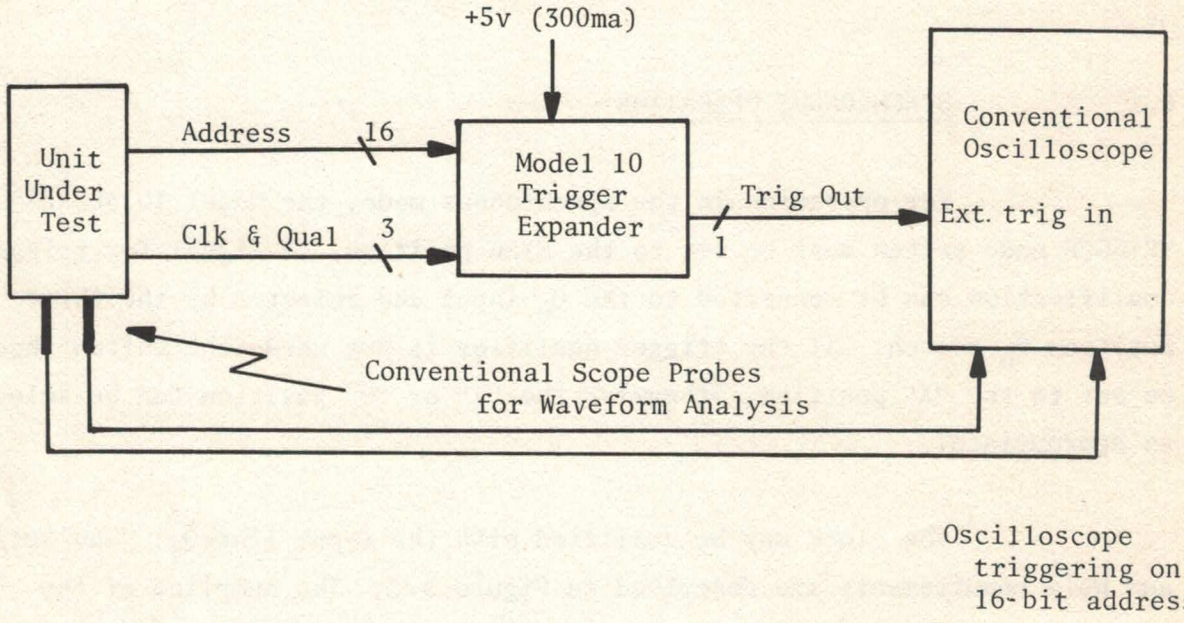


Fig. 8-1. Typical stand-alone application of the Model 10.

input is left ungrounded, it will appear as a logic 1 to the Trigger Expander and must be accounted for when setting the HEX address switch. (Note: Floating address inputs are more susceptible to noise.)

The Model 10 will now function as a word recognizer with digital delay. If the delay mode switch is set to CLOCK, a positive TTL trigger pulse will occur at the BNC output n clock pulses after the address trigger word matches the address switch value, where n is the value in the delay switch (n is between 0 and 999). If n is set to zero, there will be no delay and the output pulse will be generated "immediately" (actually, within 30 ns) following the sampling clock edge. If the delay mode switch is set to TRIG, the output pulse will be delayed for n address trigger occurrences. This function is useful in triggering external equipment after a number of passes through a program loop.

The output pulse is an active high open collector TTL level. The internal pull-up resistor is 1K ohm and the sink capability is 20 MA.

When used as a word recognizer, the display multiplex function is not used. The reset switch should be depressed, arming the word recognizer and illuminating the trigger LED. When the first occurrence of the trigger occurs, the LED indicator will turn off giving a visual indication that triggering has occurred.

8.2 ASYNCHRONOUS OPERATION

The Model 10 Trigger Expander may also be used as an asynchronous word recognizer. This is accomplished by switching the address trigger mode to ASYNC. In the ASYNC mode, no clock signals are required and the clock and Q_1 inputs may be left unconnected. Also, the clock polarity switch delay mode and delay thumbwheel switches are inactive. A positive TTL level will occur at the BNC output whenever the address inputs and Q_0 qualifier input

match the address switches and Q_0 switch. This is a purely combinatorial path, the only delay being the propagation time of the gates involved (nominally 30 ns). Because there is no clock sampling, glitches on the address inputs can be passed to the TRIG output. If this occurs, the trigger qualifier Q_0 may be used to "strobe" the address. Also, further qualification or address comparator expansion may be made using the Q_0 input and external TTL compatible logic.

8.3 TYPICAL USES OF THE MODEL 10 AS A WORD RECOGNIZER

Below are listed a few uses of the Model 10 as a word recognizer. As you gain familiarity with the instrument, you will undoubtedly devise other useful applications. If you have a unique application, let us know about it.

WORD RECOGNIZER APPLICATIONS

* Use the Model 10 to trigger on a specific computer program address and count the occurrences with a counter or totalizer. This quickly identifies the frequency or number of specific execution sequences.

* Use the Model 10 to spot a specific digital word or state and then trigger a conventional or storage oscilloscope. This permits time domain analysis of digitally related signals.

* Use the Model 10 to expand the triggering capabilities of other logic analyzers. It is often the case that triggering of an analyzer requires more bits than are available. The Model 10 can give 32-bit triggering capability to 16-bit analyzers.

* Use the Model 10 to generate precise digital delays for analysis of serial bit streams with a conventional oscilloscope. For example, if the Model 10's clock is connected to a stable system clock and the word recognizer is triggered on the frame sync of a serial stream, the delay function can be used to "walk" the trigger pulse through the stream, permitting time domain oscilloscope analysis of signals at any position within the bit stream.

9.0 OPERATING THE MODEL 10 WITH OTHER LOGIC ANALYZERS

The Model 10 Trigger Expander was designed to work with other logic analyzers as well as the Model 100A. These include other Paratronics' logic analyzers as well as those of other manufacturers.

9.1 OPERATION WITH THE MODEL 150 "S-100 BUS GRABBER"

The Paratronics' Model 150 "S-100 BUS GRABBER" is a single-board logic analyzer designed specifically to plug into and monitor the popular S-100 microcomputer bus.

By itself, it has many of the features of the combined Model 10 and Model 100A Analyzer, including 24-bit triggering capability and one/zero oscilloscope display. The Model 150 has an input socket compatible with the Model 10 Trigger Expander as well as a switch position that permits it to be used as a stand-alone analyzer. When the Model 10 is plugged into the Model 150 input socket, the instrument has all of the delay and qualifying features of the Model 100A/Model 10 combination. A typical application is shown in Figure 9.1-1.

9.2 OPERATION WITH THE PARATRONICS' MODEL 500 SCOPE-A-LYZER

The Model 500 SCOPE-A-LYZER is a new, high-performance, portable logic analyzer/oscilloscope combination scheduled for production in the last quarter of 1977. The unit will feature a variable input threshold 16-channel analyzer combined with a high-performance 2-channel oscilloscope. The Model 500 input buffer pod has a socket for connection to the Model 10 Trigger Expander. This expands the SCOPE-A-LYZER for full 32-bit (+qualifiers) trigger capability. See Figure 9.2-1 for additional information.

9.3 OPERATION WITH OTHER LOGIC ANALYZERS

The Model 10 can serve as a pre-qualifier for other analyzers in either the synchronous or asynchronous trigger modes. The trigger pulse output of the Model 10 BNC should be connected to the analyzer's trigger bus or qualifier input. With this set-up, the analyzer's input channels can be used to observe other signals while the Model 10 provides address triggering. One example would be to use the Model 10 to trigger a high speed digital timing analyzer. In this manner, the 4 or 8 high speed analyzer input channels can be used to provide time domain analysis of specific signals related to a particular address occurrence.

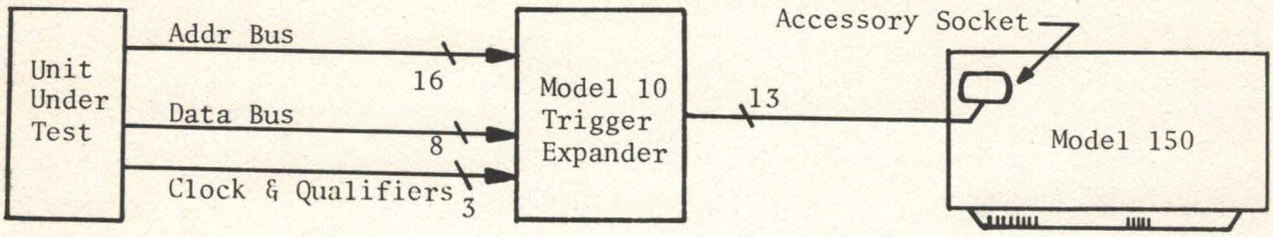


Fig. 9.1-1. Using the Model 10 with the Model 150 S-100 BUS-GRABBER.

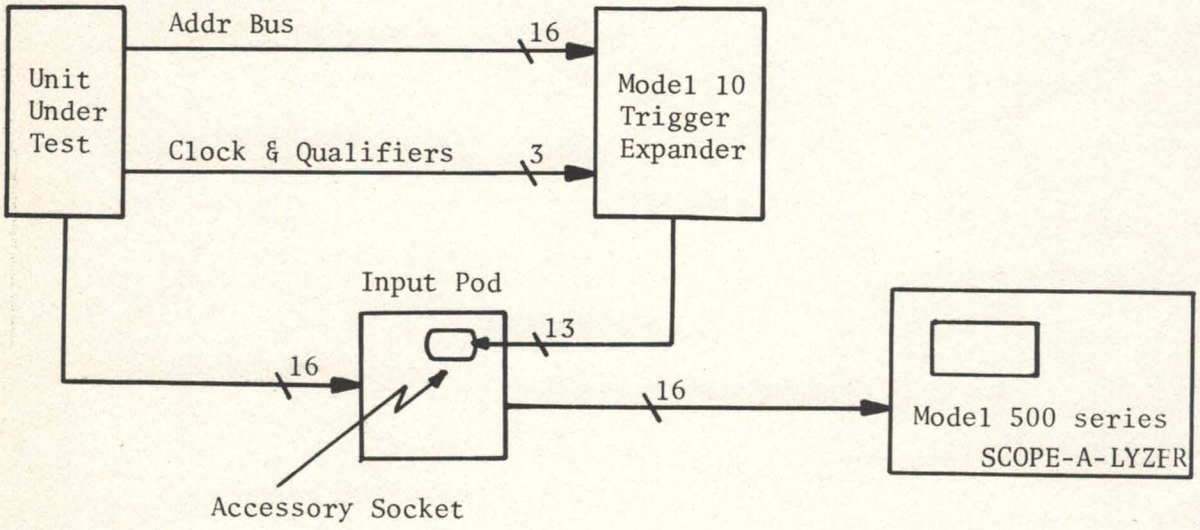


Fig. 9.2-1. Using the Model 10 to expand the Model 500-series SCOPE-A-LYZER to 32 bits.

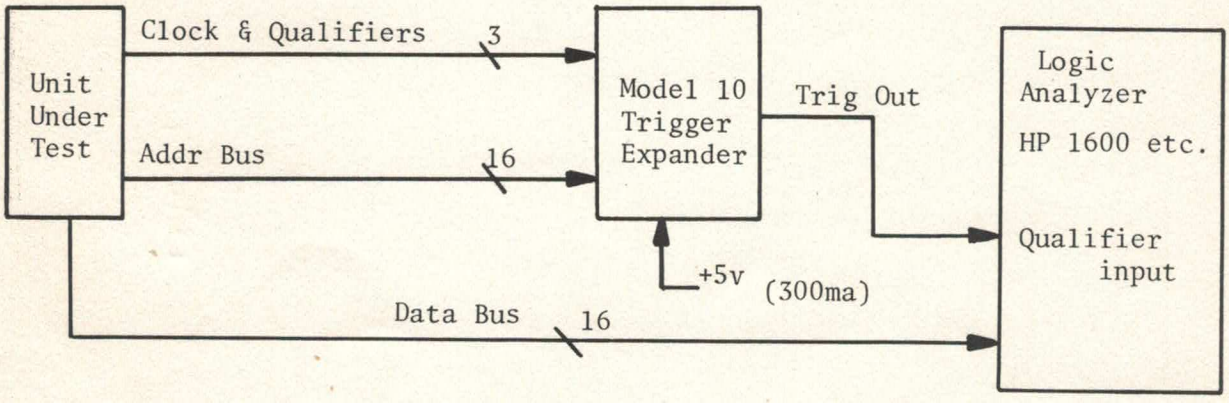


Fig. 9.3-1. Using the Model 10 to expand the triggering capability of other analyzers.

10.0 S-100 BUS APPLICATION EXAMPLE

If you have a computer with an S-100 bus, the following demonstration example will show you how useful the Model 10 Trigger Expander is in tracing program and data flow.

1. Set the Model 100A controls as follows: HEX, REPEAT, negative clock edge, POS TIME, and the trigger switches to "X" (don't care).

2. Set the Model 10 controls as follows: negative clock edge, CLOCK, DELAY=000, SYNC, Q_0 QUALIFIER="X," Q_1 QUALIFIER="X," DISPLAY MUX=HIADDR, ADDRESS=0000.

3. Connect the Model 100A/Model 10 combination to the S-100 bus as follows:

MODEL 10 PROBE		S-100 BUS PIN NO.
GROUND	-	Pin 50, etc.
CLOCK	-	DBIN, Pin 78
D0	-	DI0, Pin 95
D1	-	DI1, Pin 94
D2	-	DI2, Pin 41
D3	-	DI3, Pin 42
D4	-	DI4, Pin 91
D5	-	DI5, Pin 92
D6	-	DI6, Pin 93
D7	-	DI7, Pin 43
A0	-	Pin 79
A1	-	Pin 80
A2	-	Pin 81
A3	-	Pin 31
A4	-	Pin 30
A5	-	Pin 29
A6	-	Pin 82
A7	-	Pin 83
A8	-	Pin 84
A9	-	Pin 34
A10	-	Pin 37
A11	-	Pin 87
A12	-	Pin 33
A13	-	Pin 85
A14	-	Pin 86
A15	-	Pin 32

4. Next, run the following program which will read every address in the 64K address space. (An 8080 microcomputer is assumed; otherwise use an equivalent program.)

Address (HEX)	HEX Code	MNEMONIC
0000	23	INX H
0001	7E	MOV A,M
0002	C3	JUMP
0003	00	(address of
0004	00	jump)

5. You should observe all zeros on the scope display except for the third, ninth, and fifteenth line which will be incrementing.

6. Switch the Model 10 MUX to display the low address byte. You should observe the program address execution sequence.

7. Switch the Model 10 to display the data byte. You should now observe the program actually being read out of memory.

8. Set the address thumbwheels on the Model 10 to "0145." Switch the Model 100A to the single mode (SNGL). You should see the data read out of address 0145 on the first line of the display. You can read the contents of any address you wish by setting the address on the Model 10 and pressing reset.

9. You may now experiment with paging through the program using the delay feature of the Model 10. Simply increment the delay and observe the program "walk" up the display.

11.0 THE WARRANTY AND RETURN SHIPPING INFORMATION

LIMITED WARRANTY

This warranty becomes valid only after the WARRANTY REGISTRATION CARD, packed with each unit, is filled out and mailed to Paratronics, Inc. (hereinafter P.I.) within ten (10) days from the date of equipment delivery.

Your analyzer instrument, purchased in factory ASSEMBLED & TESTED form, is guaranteed against all defects in materials and workmanship for a period of one (1) year from the date of delivery to the original user. All factory assembled units returned to P.I. POSTPAID during the one year period will be replaced or restored to proper working condition and returned to the sender without charge.

The KIT version of the instrument is guaranteed against defects in supplied parts for a period of ninety (90) days from the date of delivery to the original user. Defective parts returned to P.I., POSTPAID, during the 90-day warranty period, will be replaced free of charge.

NOTE: THIS WARRANTY DOES NOT APPLY TO DAMAGE CAUSED BY SHIPPING, ACCIDENT, UNAUTHORIZED REPAIR, IMPROPER KIT ASSEMBLY, ABUSE, MISUSE, OR MODIFICATION; OR TO INCONVENIENCES OR CONSEQUENTIAL DAMAGES OCCASIONED BY THE INSTRUMENT, OR BY BREACH OF ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT THERETO. FURTHER, NO AGREEMENT EXTENDING OR MODIFYING THIS WARRANTY IN ANY WAY WHATSOEVER WILL BE BINDING UPON P.I. UNLESS EXECUTED BY A DULY AUTHORIZED OFFICER OF THE COMPANY.

This warranty gives you specific legal rights, and you may also have other rights which depend on local jurisdiction.

If you have a problem with the Model 10 kit or factory assembled unit, see where you fit in the categories listed below and follow the directions given:

1. You've purchased a kit or assembled unit from Paratronics, Inc., from one of our dealers or from your local stocking representative and it's still covered by the warranty:

Write to Paratronics, Inc., explaining the problem in as much detail as possible. We'll promptly provide assistance and a RETURN AUTHORIZED NUMBER (R.A.N.), if required. Once you receive the R.A.N., send the part or unit to us POSTPAID and we'll replace or repair it free of charge.

2. You've purchased a kit or assembled unit from Paratronics, Inc., from one of our dealers, or from your local stocking representative and out-of-warranty service is required (i.e., the warranty has expired, or factory labor is required to put a kit into proper operating condition):

Follow the procedure in No. 1 above. However, when you return the unit to us, POSTPAID, enclose $25.00 to cover repair costs. If the problem is relatively simple, we'll refund the unused portion of your remittance. On the other hand, if the problem requires extensive repair, we'll provide you with an estimate of the total cost and await your authorization before proceeding.

3. Your particular situation is not covered by the above:

Write to us and tell us all about it. We'll do everything we can to help.

NOTE: IF YOU'VE PURCHASED AN ASSEMBLED UNIT FROM A DEALER OR INDIVIDUAL WHO HAS ASSEMBLED IT HIMSELF FROM THE KIT VERSION, IT IS NOT COVERED BY THE WARRANTY. IF YOU ARE HAVING DIFFICULTY, TAKE IT BACK TO THE ORIGINAL SELLER. IF YOU DON'T GET SATISFACTION, GET A R.A.N. AND FOLLOW THE PROCEDURE IN NO. 2 ABOVE. WE'LL DO EVERYTHING WE CAN TO HELP.

SHIPPING INSTRUCTIONS

1. Pack the unit or component carefully. Use plenty of foam or other cushioning material and high-quality tape. When shipping a complete unit, use the original container, if available, and pay particular attention to protecting the front panel controls and the finish on the case.

SUGGESTION: SINCE MOST OF THE CIRCUITRY IS CONTAINED ON THE TWO PC BOARDS, YOU MAY FIND IT CONVENIENT AND LESS COSTLY TO SHIP ONLY THE BOARDS AND BNC BRACKET ASSEMBLY.

2. DO NOT RETURN ANYTHING WITHOUT A RETURN AUTHORIZATION NUMBER (R.A.N.).

3. Ship the unit or component, POSTPAID, to: Paratronics, Inc., 800 Charcot Avenue, San Jose, CA 95131.

4. For your own protection, we recommend that the shipment be insured against loss or damage.

APPENDIX

MICROCOMPUTER APPLICATIONS

Note: This section contains much of the Model 10 applications information presented in the Model 100A Manual. Also contained is additional applications information not previously published.

A.1 LOGIC ANALYSIS OF THE INTEL 8080

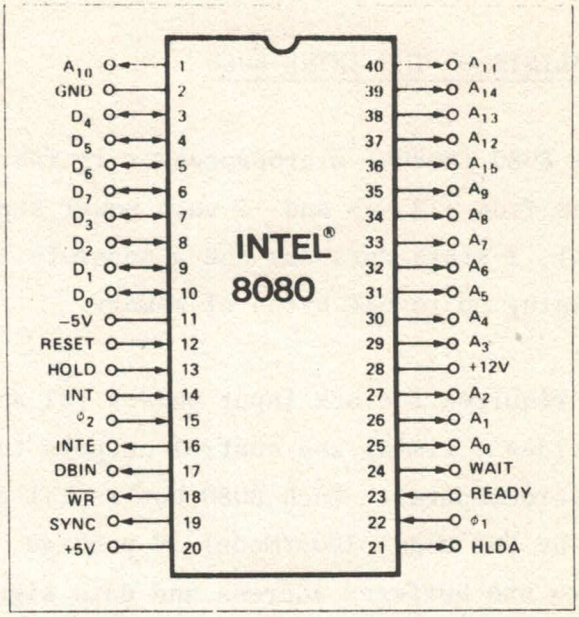
The INTEL 8080 (8080A) microprocessor is fabricated using NMOS technology and operates from +12, +5 and -5 volt power supplies. It utilizes an 8-bit, bidirectional, 3-state data bus and a separate 16-bit, 3-state address bus for addressing up to 65K bytes of memory.

The 8080 requires 2 clock input phases (Ø1 and Ø2) and 4 control inputs. The chip provides 6 timing and control outputs to other subsystems associated with the microcomputer. Each 8080 bus is TTL-compatible and can be monitored directly by the Model 100A/Model 10 package. However, it is always good practice to use buffered address and data signals, if available.

The pin assignments and functions of the 8080 are shown in Figure A.1-1 for your reference.

The next two tables illustrate the connections and control settings for analysis of the 8080 with the Model 100A and the Model 10 Trigger Expander. All interconnections to the 8080 (and all other microprocessors) are through the Model 10.

Model 10 Input Probes	8080 Monitoring Points
Ground	Vss or microcomputer ground
Clock	Ø2
D0-D7 (data)	data bus
A0-A15 (address)	address bus
Q_0 (trigger qualifier)	$\overline{WR}$ (pin 18)



Signal Description

A_{15}-A_0	Address to memory or I/O device number for up to 256 input and 256 output devices. A_0 is LSB.
D_7-D_0	Bidirectional communication between memory, CPU, and I/O devices.
Sync	Signal to indicate the beginning of each machine cycle.
DBIN	Data Bus In signal indicates to external circuits that data bus is in input mode. (Enables the gating of data from I/O or memory onto data bus.)
READY	Valid memory or input data available on data bus. Used to synchronize 8080 with slower memory or I/O devices.
WAIT	Acknowledges that 8080 is in a wait state.
$\overline{WR}$	The write signal used for memory write or I/O output
HOLD	Requests 8080 to enter the HOLD state.
HLDA	The HOLD ACKNOWLEDGE signal responds to HOLD and indicates that address and data buses will go to high impedance state.
INTE	Interrupt Enable signal indicates content of internal interrupt enable flip-flop. Inhibits interrupt when flip-flop is reset.
INT	Interrupt request is recognized at end of current instruction or while halted.
RESET	While activated, the program counter is reset, program will start at 0 in memory. INTE and HLDA are reset.
Φ1, Φ2	External clocks; non-TTL compatible.

Fig. A.1-1. INTEL 8080 (8080A) pin assignments and signal definitions.

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier	"0" for write qualify; "1" for read
Q_1 (clock qualifier)	OFF
Delay select	CLOCK or TRIGGER delay
Delay set	0-999, as required
Address set	4-digit HEX address, as required
Address trigger mode	OFF or SYNCHRONOUS, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	OCTAL
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

With the above set-up, a 16-bit address can be preset to initiate triggering, at which point the display will show all of the associated program steps on the data bus.

Through the use of internal multiplexers, the Model 10 has the additional capability to permit display of the data bus, the upper byte of the memory address, and the lower byte. Also, the ability to select the write request ($\overline{WR}$) line as a trigger qualifier provides the useful feature of triggering the analyzer only when the contents of a memory location or I/O address is being modified.

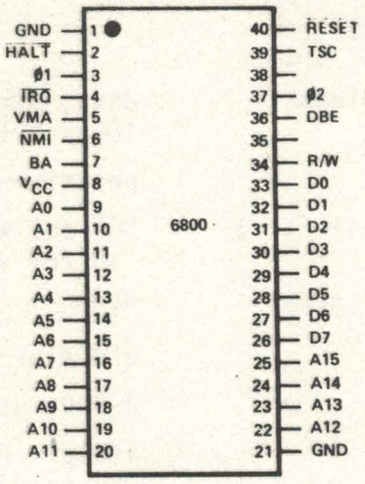
Using the delay feature of the Model 10, triggering can be delayed for a preset number of clock cycles or trigger occurrences. This feature is useful for paging through your program or for capturing the "nth" time a particular memory reference is made.

A.2 LOGIC ANALYSIS OF THE MOTOROLA 6800

The MOTOROLA 6800 microprocessor is fabricated using NMOS technology and operates from a single +5 volt power supply. It utilizes a three-state 16-bit address bus for addressing up to 65K bytes of memory or I/O devices, and operates with a bidirectional, three-state 8-bit data bus. The maximum clock rate is 1 MHz. All 6800 signals are compatible with the Model 10 Expander inputs; however, it's good practice to interface with the buffered side of the data bus and address bus whenever possible. Figure A.2-1 illustrates the 6800's pin assignments and signal descriptions.

The next two tables describe the connections and control settings required using the Model 100A/Model 10 package. All connections to the 6800 microprocessor system are made through the Model 10.

Model 10 Input Probes	6800 Monitoring Points
Ground	Vss or microcomputer ground
Clock	Ø2
D0-D7 (data)	data bus
A0-A15 (address)	address bus
Q_0 (trigger qualifier)	R/W (pin 34)
Q_1 (clock qualifier)	VMA (pin 5)



Signal Description

$\overline{\text{HALT}}$	CPU halted
$\overline{\text{IRQ}}$	Interrupt request pending
VMA	Address bus data is valid
$\overline{\text{NMI}}$	Non-maskable interrupt
BA	Address bus is available, CPU in wait state
$\overline{\text{RESET}}$	Initialize CPU
TSC	Address bus and R/W line at high-impedance
DBE	Data bus drivers are enabled
R/W	Read operation into CPU, otherwise Write operation

Fig. A.2-1. Motorola 6800 pin assignments and control signal descriptions.

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte lower byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write qualifier; "1" for read
Q_1 (clock qualifier)	"1"
Delay select	CLOCK or TRIGGER delay
Delay set	0-999, as required
Address set	4-digit HEX address, as required
Address trigger mode	OFF or SYNCHRONOUS, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

With the above configuration, the Model 10 can be triggered by the 6800's reference to a specific address. Also, qualifying the input clock on the VMA signal allows the analyzer to sample 6800-directed bus activity only. And by setting the trigger qualifier to "0," the analyzer will trigger only on a write operation. Finally, triggering can be delayed up to 999 clock pulses or trigger occurrences by setting the appropriate delay mode into the Model 10. This feature is useful in the analysis of 6800 program loops.

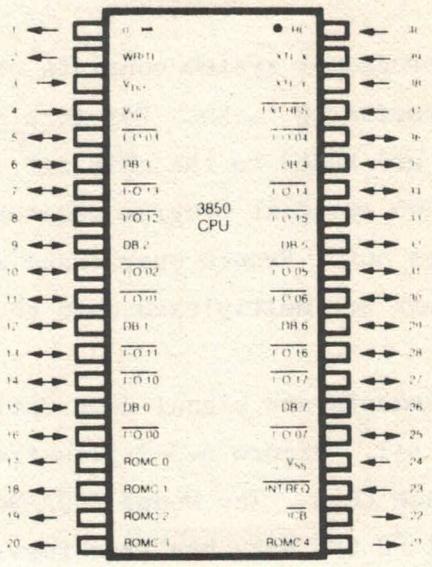
A.3 LOGIC ANALYSIS OF THE FAIRCHILD F8 MICROPROCESSOR

The F8 microprocessor system consists of a two-chip set which is capable of many basic processing tasks. For more complex functions, memory access and interface chips are added to the chip set. The F8 system is unique in that each chip has its own resident program counter, thus eliminating the need for a dedicated address bus. Branch operations which necessitate updating the internal address counters are multiplexed onto the data bus.

The pin assignments and signal descriptions for the 3850 F8 CPU chip are shown in Figure A.3-1. Figure A.3-2 illustrates the same information for the 3853 Memory Interface Chip. The Model 100A/Model 10 combination readily permits the analysis of all F8 CPU data bus transfers and I/O operations.

The Model 10 address inputs are connected to the appropriate points on the 3853 memory interface chip which permits the full 16-bit address bus to be used as a trigger source. The following tables describe this and other connections and control settings for the Model 100A/Model 10 analyzer system.

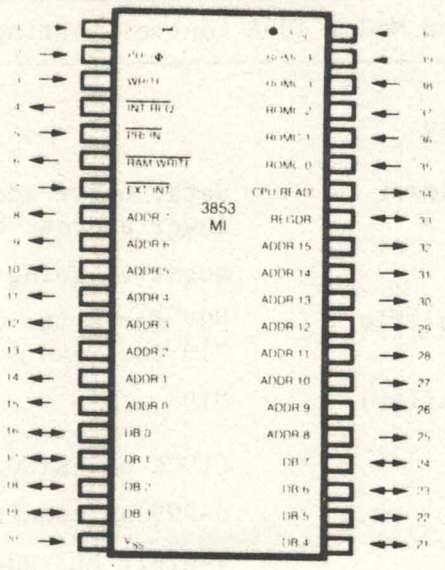
Model 10 Input Probes	3853 Monitoring Points
Ground	Vss or microprocessor ground
Clock	WRITE (pin 3)
D0-D7 data inputs	DBØ-DB7
AØ-A15 address inputs	ADDRØ-ADDR15
Q_0 (trigger qualifier)	$\overline{\text{RAM WRITE}}$
Q_1 (clock qualifier)	CPU READ



Signal Description

DB0-DB7	Bidirectional data bus
I/O 00-I/O 07	I/O Port zero
I/O 10-I/O 17	I/O Port one
ROMC 0-ROMC 4	Output control lines
RC	RC timing input
XTL-X	Crystal clock inputs
XTL-Y	External clock inputs
EXT RES	External reset
$\overline{\Phi}$, WRITE	Output clocks
$\overline{\text{ICB}}$	Interrupt control bit
$\overline{\text{INT REQ}}$	Interrupt request
V_{dd}, V_{ss}, V_{gg}	Power

Fig. A.3-1. Fairchild F8 pin assignments and signal definitions.



Signal Description

DB0 - DB7	Bidirectional data bus
ADDR0 - ADDR15	Address out
Φ Write	Clocks in
INT REQ	Interrupt request out
PRI IN	Priority in line
RAM WRITE	Write line out
EXT IN	External interrupt line in
REGDR	Register drive line
CPU READ	CPU read line out
ROMC0 - ROMC4	Control lines in
V_{ss} V_{dd} V_{gg}	Power lines

Fig. A.3-2. Fairchild F8 memory interface chip pin assignments and signal definitions.

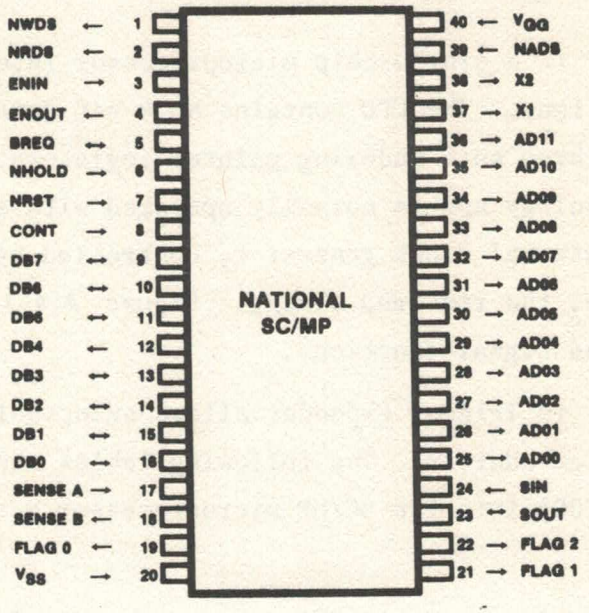
Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	negative-going
Q_0 (trigger qualifier)	"0" for write qualify, "1" for read
Q_1 (clock qualifier)	"1"
Delay select	CLOCK or TRIGGER delay
Delay set	0-999 as required
Address set	4-digit HEX address, as required
Address trigger mode	OFF or SYNCHRONOUS, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

A.4 LOGIC ANALYSIS OF THE SC/MP MICROPROCESSOR

The SC/MP is a single-chip microprocessor intended for general-purpose control applications. The CPU contains an 8-bit data bus and a 12-bit address bus along with three auto-indexing pointer registers. The SC/MP uses low-cost P-Channel technology and is normally operated with a +12 volt supply across V_{GG} & V_{SS}. An internal clock generator, controlled by an external RC circuit or XTAL, provides the required timing. Figure A.4-1 illustrates the SC/MP pin assignments and signal functions.

The Model 10 Trigger Expander allows selectable, delayed triggering of any SC/MP system address. The following tables show how to connect the Model 10 and Model 100A into the SC/MP microprocessor system.

Model 10 Input Probes	SC/MP Monitoring Points
Ground	V_{GG} (microprocessor ground)
DO-D7 (data inputs)	DBØ-DB7
AO-A11 (address inputs)	ADØØ-AD11
A12-A15 (address inputs)	ground
Clock	NRDS (pin 2)
Q_0 (trigger qualifier)	ENOUT (pin 4)
Q_1 (clock qualifier)	not connected



Signal Description

DB0-DB7	Data bus
AD00-AD11	Address bus
FLAGØ-FLAG2	User assigned, general-purpose bit
X1, X2	To external timing xtal/cap.
NWDS	Write strobe output
NRDS	Read strobe output
ENIN	Enable input
ENOUT	Enable output
BREQ	Bus request input/output
NHOLD	Hold lengthens input/output cycle
NRST	Reset input
CONT	Continue input
SENSEA-SENSEB	General purpose status inputs
NADS	Address strobe output
SIN	Serial input
SOUT	Serial output
V_{SS}	Positive supply voltage
V_{GG}	Negative supply voltage

Fig. A.4-1. SC/MP pin assignments and signal definitions.

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"1" for write qualify, "0" for read
Q_1 (clock qualifier)	off
delay select	CLOCK or TRIGGER delay
delay set	0-999, as required
address set	3-digit HEX addresses as required (Upper HEX digit=0)
address trigger mode	OFF or SYNCHRONOUS as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger Switches	as required

This configuration allows the user to monitor or trigger from the address bus or data bus of the SC/MP. The qualifier can be used to permit a read or write operation to trigger the analyzer.

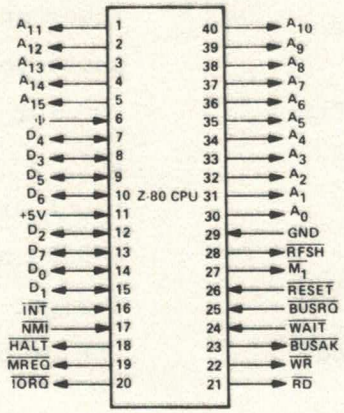
A.5 LOGIC ANALYSIS OF THE ZILOG Z-80

The Z-80 CPU is a third-generation, single-chip, microprocessor that is "upward compatible" with the INTEL 8080. The chip is fabricated using N-channel, silicon-gate, MOS technology and operates from a single +5 volt supply. All signals are TTL compatible.

The Z-80 can operate at a 1.6 usec. instruction speed, which is somewhat faster than the 8080. The Z-80's pin assignments and signal definitions are illustrated in figure A.5-1.

The Model 100A/10 combination can be used to trigger from the Z-80's address bus while monitoring the data bus. The following two tables indicate the required system connections and control settings for the Model 100A and the Model 10.

Model 10 Input Probes	Z-80 Monitoring Points
Ground	V_{ss} or microcomputer ground
D0-D7 (data inputs)	D0-D7 (data bus)
A0-A15 (address inputs)	A0-A15 (address bus)
Clock	Ø
Q_0 (trigger qualifier)	$\overline{WR}$



Signal Description

A_0-A_{15}	Tri-state address bus
D_0-D_7	Tri-state data bus
$\overline{M_1}$	Machine opcode fetch cycle
$\overline{MREQ}$	Memory request
$\overline{IORQ}$	I/O address valid
$\overline{RD}$	Memory read
$\overline{WR}$	Memory write
$\overline{RFSH}$	Refresh request
$\overline{HALT}$	Indicates CPU halted
$\overline{WAIT}$	Input to place CPU in wait state
$\overline{INT}$	Interrupt request
$\overline{NMI}$	Non maskable interrupt request
$\overline{RESET}$	CPU initialization
$\overline{BUSRQ}$	Request to CPU for control of address and data busses
$\overline{BUSAK}$	Acknowledge to external device for bus grant

Fig. A.5-1. Z-80 pin assignments and signal definitions.

Model 10 and Model 100A Control Settings	
Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write; "1" for read
Q_1 (clock qualifier)	OFF
Delay select	CLOCK or TRIGGER delay
Delay set	0-999, as required
Address set	4-digit HEX address
Address trigger mode	OFF or SYNCHRONOUS as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	OCTAL
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

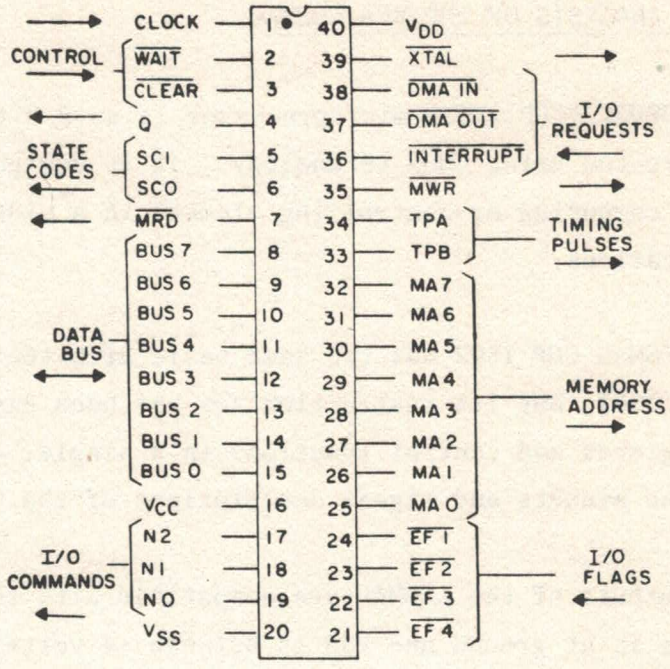
The above tables permit the triggering of the Model 10 on a selected address occurence. Note that the Q_0 qualifier may be used to trigger on either read or write operations.

A.6 LOGIC ANALYSIS OF THE RCA COSMAC

The COSMAC (CDP 1802) microprocessor is an 8-bit, one chip, device which is fabricated using CMOS technology. It is designed to be used as a general-purpose computing or controlling element in a wide range of stored-program applications.

The COSMAC CDP 1802 has the same basic architecture of its predecessor, the CDP 1801, but its instruction set has been expanded and it incorporates both register and control functions in a single, 40-pin package. Figure A.6-1 shows the pinouts and signal descriptions of the CDP 1802.

All outputs of the COSMAC are compatible with the Model 10's inputs as long as Vss is at ground and Vdd is between +4 volts and +15 volts. However, to avoid affecting microprocessor operation at the higher speeds, use buffered address and data buses, if possible.



Signal Descriptions

CLOCK	External clock input
WAIT, CLEAR	Control mode inputs
Q	Single bit output
SC0, SC1	CPU state signals
BUS0, BUS7	CPU data bus
V_{cc}	Output pull-up rail
N0, N1, N2	I/O commands
V_{ss}	Most negative supply (ground)
V_{dd}	Most positive supply
XTAL	Crystal input for on-chip oscillator
DMA IN, DMA OUT, INTERRUPT	I/O request inputs
TPA, TPB	Timing pulse outputs
MA0, MA7	Memory address (multiplexed)
EF1, EF4	I/O flag inputs

Fig. A.6-1. RCA COSMAC CDP 1802 pin assignments and signal definitions.

The next two tables describe the connections and control settings required when using the Model 10 with the Model 100A to analyze the operation of the COSMAC microprocessor.

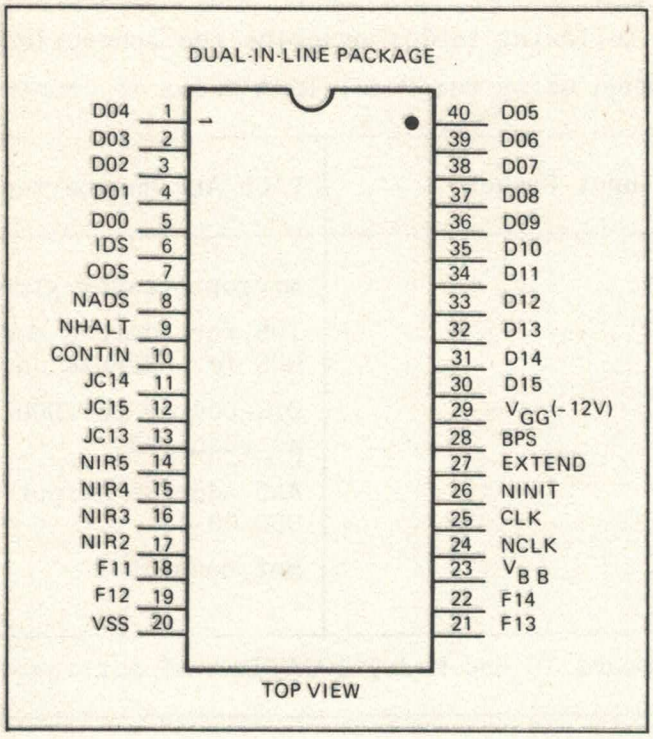
Model 10 Input Probes	COSMAC Monitoring Points
Ground	Vss or system ground
Clock	TPB (pin 33)
D_0-D_7 (data)	data bus
A_0-A_7 (lower byte)	MA_0-MA_7
A_8-A_{15} (upper byte)	upper address latch outputs
Q_0 (trigger qualifier)	$\overline{MWR}$ (pin 35)
Q_1 (clock qualifier)	not used

Model 10 and Model 100A Control Settings

Model 10	
Display multiplexer	data, upper address byte, lower address byte
Clock edge	positive-going
Q_0 (trigger qualifier)	"0" for write qualifier; "1" for read
Q_1 (clock qualifier)	OFF
Delay select	CLOCK or TRIGGER delay
Delay set	0-999, as required
Address set	4-digit HEX address, as required
Address trigger mode	OFF or SYNCHRONOUS, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger switches	as required

A.7 LOGIC ANALYSIS OF THE PACE SYSTEM

The National PACE is a 16-bit, single-chip microcomputer implemented in P channel MOS technology. It is compatible with the Model 10 input circuitry when the system is operating from the standard +5v (V_{ss}), Gnd, and -12v (V_{gg}) supplies. The address and data are time-multiplexed on a single 16-bit bidirectional bus. For systems which include the address latch element (ALE), 16 address bits and 8 data bits can be monitored. Figure A.7-1 shows the Pace Chip pinouts and signal descriptions.



Signal Description

CLK, NCLK	True and compliment clocks
$D_{ØØ}$ - D_{15}	Input/output data bus
IDS	Input data strobe
ODS	Output data strobe
NADS	Address data strobe
EXTEND	Clock cycle extend
N INIT	Initialize
N HALT	Control panel halt
CONTIN	Continue
BPS	Base page select
JC 13, 14, 15	Conditional jump inputs
F 11, 12, 13, 14	Status outputs
NIR 2, 3, 4, 5,	Interrupts
V_{BB}	Input substrate voltage
V_{GG}	Input power (-12V)
V_{SS}	Input power (+5V)

Fig. A.7-1. PACE pin assignments and signal definitions.

The following tables describe the connections and control settings required when using the Model 100A/Model 10 combination

Model 10 Input Probes	PACE/ALE Monitoring Points
Ground	microprocessor ground
Clock	IDS for Address and Data-in ODS for Address and Data-out
D_0-D_7	D15-D08 or D07-D00 as required
A_0-A_{15}	ALE Address outputs UDO 00-15
Q_0, Q_1	not connected

Model 10 and Model 100A Control Settings

Model 10	
Display multiplexer	data, upper address byte, lower address byte.
Clock edge	negative-going
Q_0, Q_1 qualifiers	both "X"
Delay select	CLOCK or TRIGGER delay
Delay set	0-999 as required
Address set	4-digit HEX address as required
Address trigger mode	OFF or SYNCHRONOUS as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	HEX
SINGLE/REPEAT	as required
POS/NEG TIME	as required
Trigger Switches	as required in combination with address trigger.

For convenience, an octal 2:1 multiplexer could be easily configured using two octal three-state buffers (SN74LS241 or equivalent) to multiplex both the upper and lower byte of the PACE data bus to the eight D_0-D_7 inputs.

A.8 LOGIC ANALYSIS OF BIT-SLICE MICROPROCESSORS

Microprogrammed minicomputers, based on the popular bit-slice chips such as the AM2901, the INTEL 3002, and the SBP0400, are another example of complex digital hardware which can readily be analyzed using the Model 100A/ Model 10 combination. Generally, these bit-slice chips contain several general registers, one or more working registers, and an arithmetic logic unit (ALU), and can be concatenated to form a minicomputer whose word length can be any practical multiple of two to four bits.

Figure A.8-1 is a simplified block diagram of a typical minicomputer based on a bit-slice microprocessor. Note the use of a microprogrammed control structure, which permits the user to define and implement his own instruction set. And since these chips are usually fabricated using TTL technology rather than MOS, their instruction execution times are at least an order of magnitude faster than the 8080-type microprocessor. Thus, both speed and user flexibility govern the choice of bit-slice elements for use in a minicomputer.

When using the Model 10/Model 100A combination with a bit-slice minicomputer, one of the most useful monitoring points is the control memory address bus, which forms the address of the microprogram memory and thus selects the microcontrol word. Then, with the input clock probe connected to the correct phase of the system clock, the user can trace the microinstruction sequence of the minicomputer. This ability is essential for debugging microprograms or even verifying the correct operation of an existing machine.

The control memory address bus is connected to the address inputs of the Model 10. (Up to 16 are available.) The remaining data inputs of the Model 10 can be used to probe different sections of the minicomputer, as required. As an example, let's investigate the probe connections and control settings required to check out an 8-bit divide algorithm which we've just completed microprogramming. Refer to the tables for appropriate monitoring points.

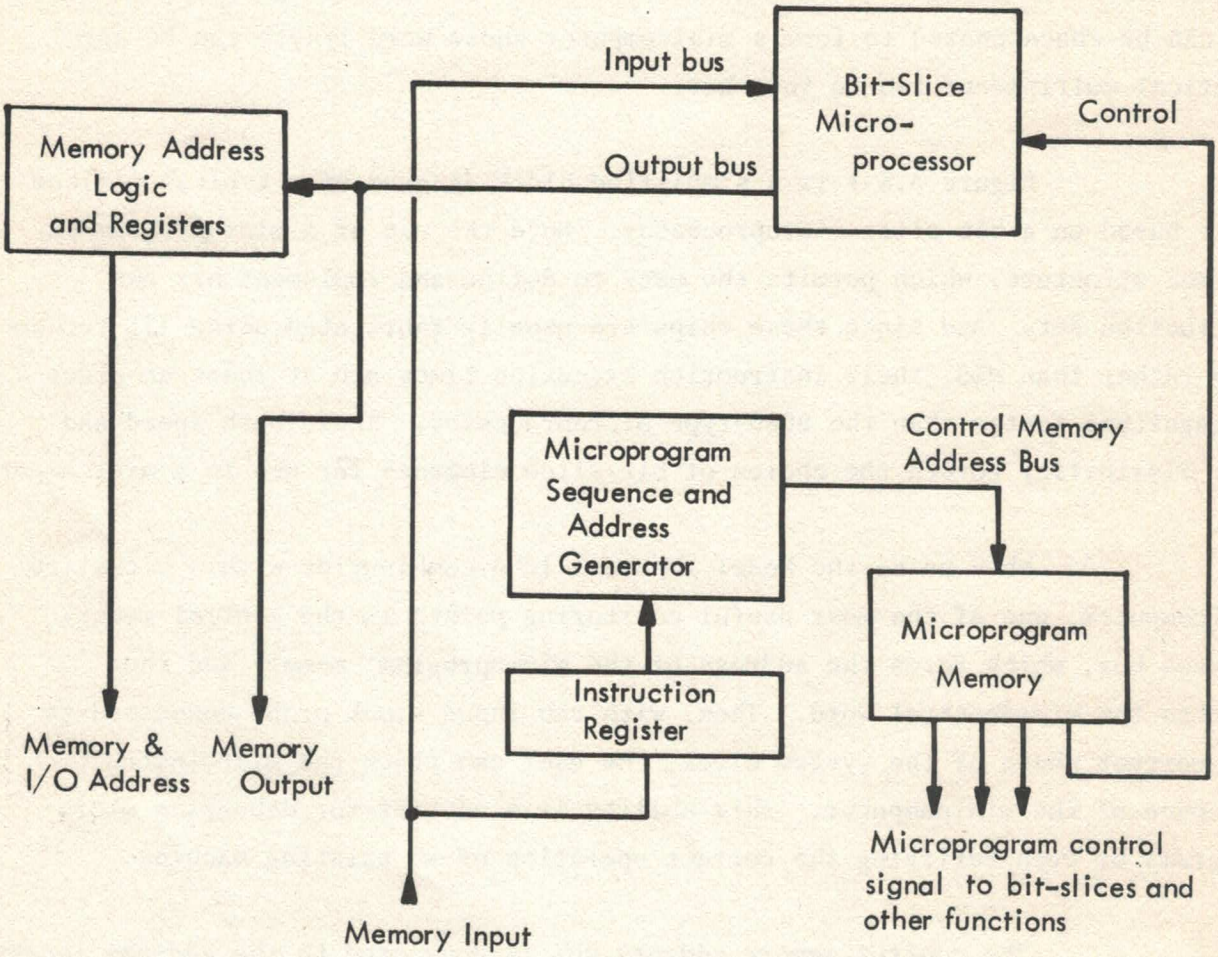


Fig. A.8-1. Basic bit-slice computer block diagram.

Model 10 Input Probes	Bit-Slice Monitoring Points
Ground	system ground
D_0-D_7 (data inputs)	ALU output
A_0-A_{15} (address inputs) (ground unused inputs)	control memory address bus
Clock	system clock
Q_0-Q_1 (qualifiers)	not used

Model 10 and Model 100A Control Settings

Model 10	
Address set	4-digit start of divide microprogram
Address trigger mode	SYNCHRONOUS
Clock	active edge of system clock
Qualifiers	OFF
Display multiplexer	data, upper address byte, lower address byte
Delay select	clock
Delay set	0-999, as required
Model 100A	
Clock edge	negative-going
HEX/OCTAL	as required
SINGLE/REPEAT	REPEAT
POS/NEG TIME	POS
Trigger switches	all "X"

With the above connections and control settings, place the minicomputer in a loop which is executing the divide instruction with a known set of operands. Set the display multiplexer to the lower address byte to view the steps of the microprogram (which has been previously prepared from a microflow chart). If the sequence is longer than 16 microinstructions, "walk through" the microprogram by simply increasing the trigger delay.

Now, by selecting the appropriate position of the display multiplexer, view the data at the output of the ALU for each microprogram step. And by moving the data probes to the various control and status signals, these signals can be observed as the divide algorithm is being executed.

Thus, in summary, the Model 100A/Model 10 package reduces microprogram development, debugging, and troubleshooting to a relatively straight-forward task. Without this or similar instruments, the advanced, high-performance machines now appearing on the market would be more costly--if not impossible--to develop.

A.9 FIELD SERVICE APPLICATIONS

The Model 100A/Model 10 combination is ideal for the field servicing of mini and microcomputers. Including the mounting baseplate, the analyzer package shown in Figure 2-2 weighs under 8 pounds and measures only 18.5" x 8.5" x 2.5". Thus, its small size and weight permits easy transportation in a compact, Samsonite-type suitcase.

For those applications where the field service engineer is using the Model 100A/Model 10 package to troubleshoot and repair the same type of equipment at different installations, it is convenient to utilize a dedicated input probe set-up. Here, IC clips and ball clips can be interfaced with the input probes so that the computer's main buses can be rapidly accessed.

As an example of the usefulness of the Model 100A/Model 10 package in the field, assume that the service engineer is called in to fault-isolate a subtle program-related problem. The customer has been complaining that after a few minutes of operation of a particular program, the computer would repeatedly "de-rail" (i.e., crash) to memory location $FFFA_{HEX}$ and halt. However, other programs seem to operate normally. With the input probes A_8-A_{15} monitoring the memory address bus and probes D_0-D_7 connected to the data bus, the field service engineer has all of the visibility he needs to isolate the problem. The troubleshooting procedure is as follows:

1. Set the HEX address switch on the Model 10 to FFFA, the MUX switch to data byte and the qualifiers to "X."

2. Set the Model 100A to NEG TIME and SINGLE mode.

3. Set the Model 100A's trigger switches to "X."

4. Arm the Model 100A/Model 10 package by depressing either RESET switch.

5. Run the program in question.

When the program de-rails, the resulting scope truth table display will show the program steps on the data bus leading up to the invalid computer state. From this display and with the aid of a program listing, the engineer observes that the program is crashing just after a branch instruction, but otherwise every program step on the data bus looks normal.

Next, the field service engineer changes the MUX switch setting to the lower address byte and again arms the analyzer. This time, when the program de-rails, the truth table shows the events on the lower half of the address bus. Again, cross checking with the listing reveals that all is normal.

Finally, the above procedure is repeated with the MUX switch set to the upper address byte. Now it is observed from the display that one of the higher-order bits on the memory address bus, several steps before the execution of the branch instruction, has suddenly changed from a logic 0 to a logic 1. This change is occurring during an address arithmetic operation whose result is being used to generate the faulty branch address.

Having located the intermittent bit on the address bus, the field service engineer must isolate the underlying cause. Taking advantage of the DELAY feature of the Model 10, he dials in the setting required to place the faulty address byte at the bottom of the truth table. Then, with the TRIG output connected to the trigger input of his scope, he monitors (in real time) both the input and output timing waveforms associated with the faulty bit on the memory address register. He observes that the output is changing to a logic 1 while the input appears to remain at a logic 0. Taking a closer look, this logic 0 voltage is "sitting" at 1.2 volts, leaving very little noise margin against transients coupling in as nearby bits are changing state.

The field service engineer then replaces the IC driving the faulty bit of the memory address register, observes that the logic 0 voltage is now under 0.8 volts for all bits, and again runs the program. This time the computer operates flawlessly.

Without a logic analyzer, the rapid troubleshooting and correction of program-related problems becomes a difficult--if not an impossible--task. The use of the analyzer can significantly reduce system downtime, which can be costly to the end-user.

A.10 PRODUCTION TESTING

Thorough testing of a microprocessor-based product requires an instrument package like the Model 100A/Model 10 combination to aid in verifying that the product is performing properly. Below is a list of some of the specific checks that can be incorporated into an acceptance test procedure (ATP). Note that a dedicated test adapter between the Model 100A/Model 10 package and the system-under-test could be constructed to permit rapid system interconnection and switching of input signals. On the system side, the associated cable can be terminated in a labeled IC clip arrangement, or by a connector which mates with a test receptacle designed into the system.

Elements of an ATP

1. Use the clock delay feature to page through the test program.

2. Connect the TRIG output to a counter, set the trigger switches to a specific machine state and record the number of trigger occurrences. (This will tell the operator how many times a specific execution sequence has occurred. Averaged over a period of time, this number can provide a measure of machine throughput.)

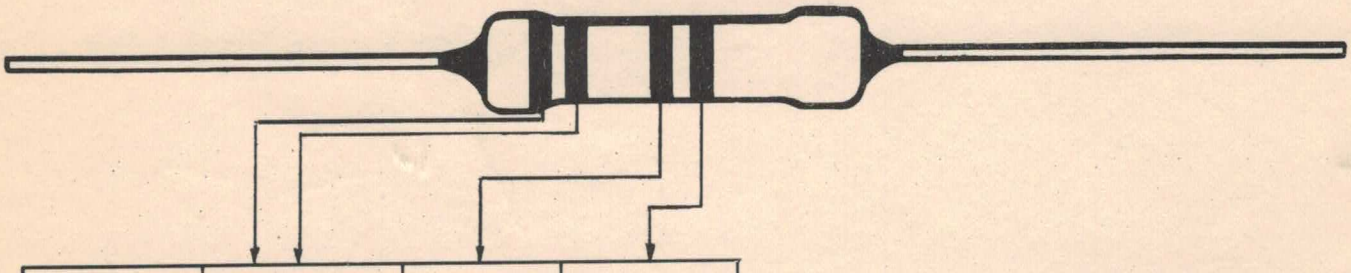
3. Switch the TRIG output to a scope's input and monitor the timing and/or noise margins of critical signals as a function of specific machine states.

4. Verify the contents of ROMS and other memory devices.

5. Use the clock qualifier to verify certain program sequences such as READ, STORE or I/O operation.

6. Use the trigger qualification and delay features to permit the display of the machine's state after "n" passes through a test loop.

RESISTOR COLOR CODING



Color	1st, 2nd Significant Figure	Multiplier	Tolerance
Black	0	1	
Brown	1	10	±1%
Red	2	10^2	±2%
Orange	3	10^3	
Yellow	4	10^4	
Green	5	10^5	±0.5%
Blue	6	10^6	
Violet	7	10^7	
Grey	8	10^8	
White	9	10^9	
Silver		10^{-1}	
Gold		10^{-2}	±5%

1st band: digit
2nd band: digit
3rd band: digit
4th band: multiplier
5th band: tolerance

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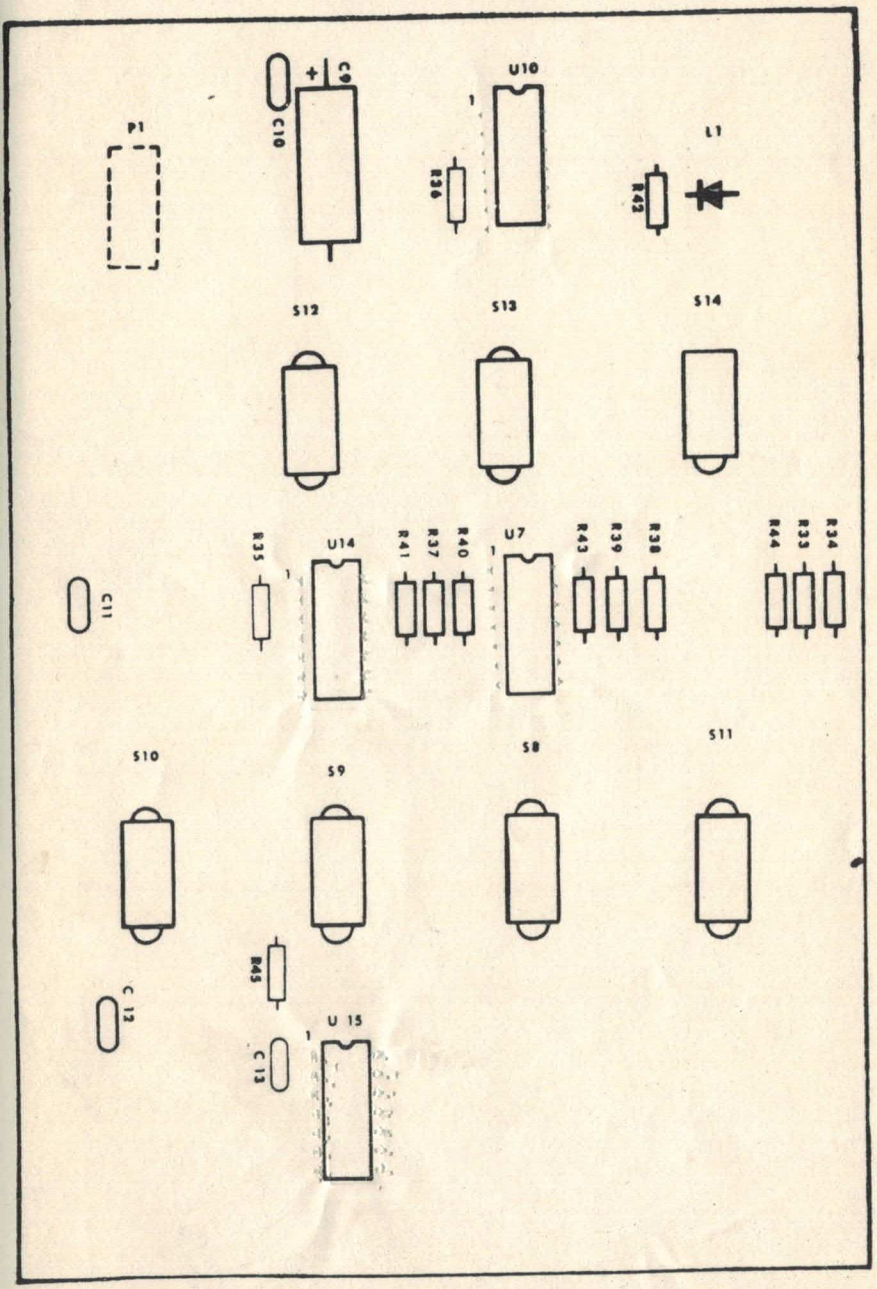
MODEL 10 BOARD 1



MODEL 10 BOARD 2