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OPTION 06
I/O COMMUNICATION INTERFACE
SERVICE MANUAL ADDENDUM

TO THE DAS 9100 SERIES SERVICE MANUAL (PART NUMBERS 062-5848-00, 01 AND UP)

The 062-5848-00 manual set is a package consisting of loose leaf binders with manuals and addenda. Each manual and addendum in the set has its own part number starting with the prefix 070.

This addendum contains service information specific to the Option 06 I/O Communication Interface.

Refer to the *DAS 9100 Series Service Manual* for information on other DAS products, including mainframes, instrument modules, probes, and options.

How To Use This Addendum. This addendum is organized similarly to the *DAS 9100 Series Service Manual:* sections in the addendum correspond to the sections in the service manual. You can either leave the addendum whole and place it in one of the service manual binders, or you can separate the sections and insert them after the corresponding section in the main manual.

NOTE: You can order an extra service manual binder (Vol. III) by requesting P/N 016-0769-00.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO THE OPERATOR'S SAFETY SUMMARY AND SERVICE SAFETY SUMMARY IN THE DAS 9100 SERIES SERVICE MANUAL PRIOR TO PERFORMING ANY SERVICE.

MANUAL REVISION STATUS

PRODUCT: OPTION 06 I/O COMMUNICATION INTERFACE SERVICE MANUAL ADDENDUM

This manual supports the following versions of this product: All

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SEPT 1983	Original Issue
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OPERATOR'S SAFETY SUMMARY

See the Operator's Safety Summary at the front of the *DAS 9100 Series Service Manual.*

SERVICE SAFETY SUMMARY (FOR QUALIFIED SERVICE PERSONNEL ONLY)

See the Service Safety Summary at the front of the *DAS 9100 Series Service Manual.*

INTRODUCTION AND SPECIFICATIONS

This document provides instructions for maintaining the DAS 9100 Series Option 06 I/O Communication Interface. The service technician may need information found in the operators and service manuals for the DAS 9100 Series logic analyzer to fully understand how the DAS and the communication interface work together.

The documents are:

DAS 9100 Series Operator's Manual	070-3624-01
DAS 9100 Series Service Manual Volume 1	070-3625-01
DAS 9100 Series Service Manual Volume 2	070-3836-01
DAS Operator's Manual Addendum Option 06 Communication Interface	070-4570-00

GENERAL DESCRIPTION

The DAS 9100 Series Option 06 I/O Communication Interface provides the communication between a DAS and an external controller, or a DAS and the peripherals attached to the system.

The Option 06 I/O Communication Interface features are:

- Programmable high-speed port-to-port transfer
- RS-232 DCE channel for direct connection to a printer
- GPIB interface binary-compatible with existing DAS GPIB
- Master/Slave/Host RS-232 interface
- Up to 64K of DAS addressable ROM
- RS-170 video output capabilities
- Diagnostic capabilities

You may order the Option 06 interface installed in the DAS mainframe or separately. It is a plug-in circuit module providing port-to-port transfers, GPIB, RS-232, and video interfaces.

You must have a DAS Controller board 670-7475-03 in your DAS for Option 06 to function properly. These Controller boards are normally installed in DAS mainframes with serial number B050100.

You must have version 1.11 firmware or higher in your DAS mainframe for Option 06 to function properly.

PHYSICAL DESCRIPTION

The DAS 9100 Series Option 06 I/O Communication Interface consists of a plug-in circuit module (the I/O Interface board) and a back panel insert (the I/O Connector Panel) with appropriate connecting cabling. Figure 1-1 shows the Option 06 I/O Communication Interface in a DAS mainframe.

The I/O Interface board is installed in the DAS mainframe I/O interface slot.

NOTE

The I/O communication interface slot is in the same area in the Color DAS 9129 as it is in the Monochrome DAS 9109 , but it is on the opposite side of the mainframe center divider panel.

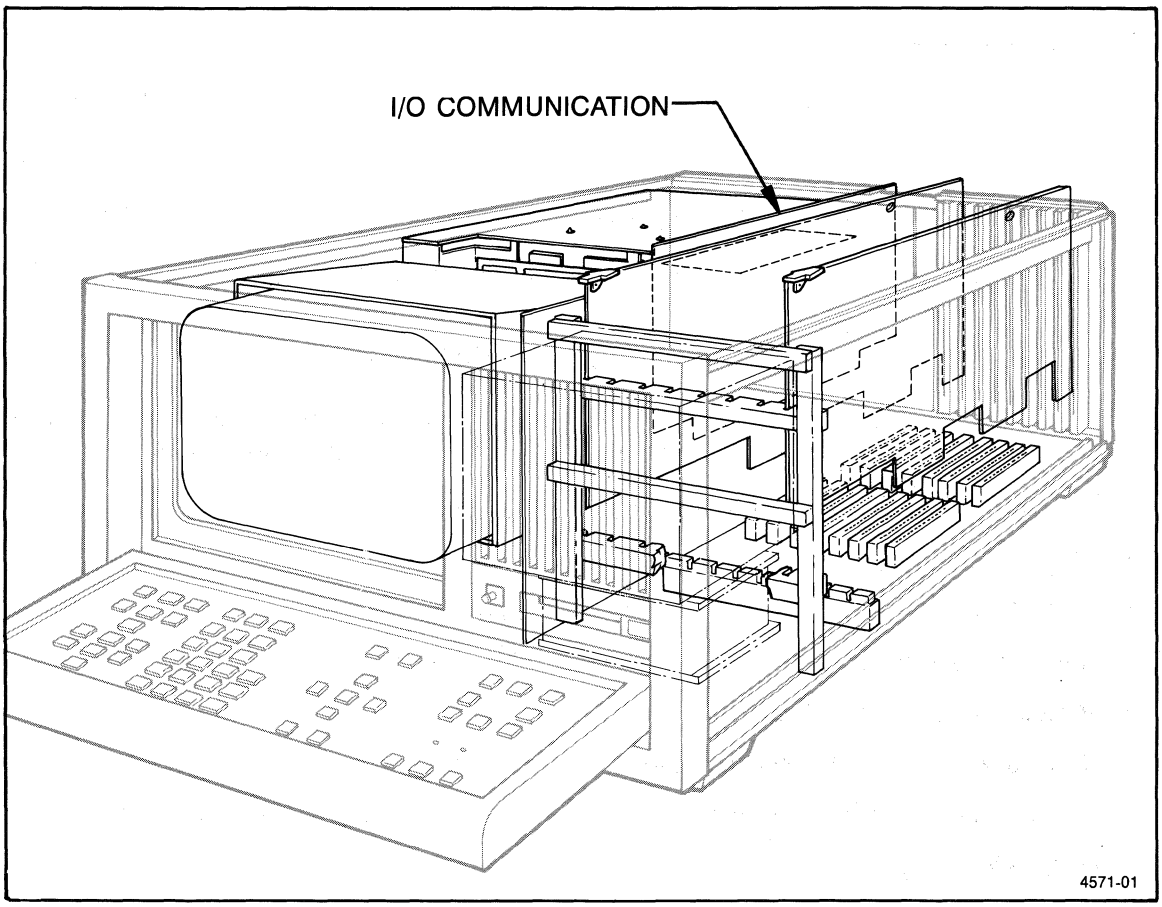


Figure 1-1. Option 06 I/O Communication Interface location.

ELECTRICAL DESCRIPTION

All DAS test operations may be extended through the use of an I/O communication interface providing RS-232, GPIB (IEEE 488), and hard copy interfaces.

RS-232 PORTS

The RS-232 Master/Slave port allows two DAS systems to be linked together for master/slave transmission between the two instruments. The master DAS serves as the controller for setting up and operating another DAS in a remote location. The RS-232 master/slave mode is controlled by entries made in the INPUT/OUTPUT menu of the DAS system. Either system can have a monochrome or color mainframe.

The RS-232 Printer port connects the DAS to a printer.

GPIB INTERFACE

A GPIB interface allows parallel data transmission between the DAS and any compatible host controller. In this mode, the DAS serves as a talker and listener, while the host controller automatically controls all menu setup and test functions. The I/O interface with its smart port controller allows fast GPIB port-to-port data transmission.

COMPOSITE VIDEO OUTPUT

The composite video output may be used with any compatible hard copy or monitor unit. The I/O communication interface has composite monochrome and separate color video signals. These features allow documentation of test results and operating parameters.

FIELD INSTALLATION

DAS91F6 is the field-installed version of the Option 06 Communication Interface for the DAS9129 (color) mainframe; also 9121-9124; and for 9101-4 and 9109 (serial number B020100 and up).

DAS91F601 is the field installed version of the Option 06 Communication Interface for the DAS9109 (monochrome) mainframe; and for 9101, 9102, 9103, 9104 (serial number B019999 and below).

The DAS91F6 and DAS91F601 must be installed by a qualified service technician.

STANDARD ACCESSORIES

The DAS 9100 Series Option 6 Communication Interface includes the following standard accessory:

070-4570-00 — DAS Operator's Manual addendum Option 06 I/O Communication Interface

OPTIONAL ACCESSORIES

The DAS 9100 Series Option 6 Communication Interface includes the following optional accessories.

012-0630-01 — Interconnect cable (2-meter GPIB cable)
012-0630-02 — Interconnect cable (4-meter GPIB cable)
012-0991-00 — Interconnect cable (2-meter GPIB cable)
012-0991-01 — Interconnect cable (1-meter GPIB cable)
012-0991-02 — Interconnect cable (4-meter GPIB cable)
012-0815-00 — Interconnect cable (2-meter RS-232 cable)
012-0074-00 — Cable assembly (42-inch 75Ω coaxial)
175-2753-00 — Cable assembly (120-inch 75Ω coaxial)
070-4571-00 — DAS Service Manual addendum Option 06 I/O Communication Interface
067-0980-01 — Service Maintenance Kit

SPECIFICATIONS

PERFORMANCE CONDITIONS

Instrument characteristics given in this section are valid under the following conditions:

- The mainframe must be operating as a part of an appropriately configured instrument system.
- The instrument system must be in an operating environment whose limits are described in this section.
- The instrument system must have been calibrated at an ambient temperature of between +20°C and +30°C after a 30-minute warmup.

Any applicable conditions not listed above but unique to a particular characteristic are expressly stated as part of the characteristic.

ENVIRONMENTAL SPECIFICATIONS

The environmental specifications for the operation of the DAS 9100-Series Option 06 I/O Communication Interface meet, or exceed, those specified for the operation of the DAS 9109 mainframe.

The non-operating environmental specifications for this instrument are those stated for a Class V instrument in Tektronix Standard 062-2853-00, including the specifications pertaining to the transportation of the packed instrument.

SAFETY SPECIFICATIONS

The safety specifications for the operation of this instrument meet, or exceed, those specified for the operation of the DAS 9109 mainframe.

ELECTRICAL SPECIFICATIONS

Table 1-1
ELECTRICAL SPECIFICATIONS – POWER

Characteristics	Performance Requirements	Supplemental Information
Inputs (from mainframe)		
+5 V Power supply		+5 V, ±5% 1.1 amps typical
+12 V Power spply		+12 V, ±10% <100 mA
−12 V Power supply		−12 V, ±10% <100 mA

Table 1-2
ELECTRICAL SPECIFICATIONS – Option 06 RS-232 DATA TERMINAL EQUIPMENT (MASTER/SLAVE) PORT

Characteristics	Performance Requirements	Supplemental Information
Baud Rates (keyboard select)		300, 600, 1200, 2400, 4800 and 9600
Input impedance		3k Ω to 7k Ω
Input levels MARK or OFF		−25 V to −3 V
SPACE or ON		+3 V to +25 V
Input Signals Connected		
Received Data		Pin 3
Clear To Send		Pin 5
Data Carrier Detect		Pin 8
Ring Indicator		Pin 22 (connected but not used)
Output Impedance		≤1k Ω
Output Levels MARK or OFF		≤−6 V
SPACE or ON		≥+6 V
Output signals connected		
Transmitted Data		Pin 2
Request To Send		Pin 4
Data Terminal Ready		Pin 20
Other Ground		Pin 1 Case Ground
Signal Ground		Pin 7 Instrument Ground

Table 1-3
ELECTRICAL SPECIFICATIONS – Option 06 RS-232 DATA COMMUNICATION EQUIPMENT (PRINTER) PORT

Characteristics	Performance Requirements	Supplemental Information
Baud Rates		300, 600, 1200, 2400, 4800, and 9600
Input Impedance		3k Ω to 7k Ω
Input levels		
Transmitted Data		Pin 2
Request To Send		Pin 4 (Direct connection to Clear To Send)
Data Terminal Ready		Pin 20
Output Impedance		≤1k Ω
Output Signals		
Received Data		Pin 3
Clear To Send		Pin 5 (Direct connection to Request To Send)
Data Set Ready		Pin 6
Carrier Detect		Pin 8

Table 1-4
[a]ELECTRICAL SPECIFICATIONS-GPIB

Characteristics	Performance Requirements	Supplemental Information
Minimum baud rate		[b]100 k bytes per second
Maximum baud rate		200 k bytes per second

[a]The electrical specifications of this interface conforms to the electrical specifications contained in the IEEE 488-1978, (Standard Digital Interface for Programmable Instrumentation).When the smart port controller is controlling the data transfer,the the transfer rate does not include the time required for entering the software code for the transfer.

[b]These transfer rates apply only if the DAS is the slowest device on the bus. All GPIB transfers occur at the speed of the slowest device connected to the lines.

Composite Video B/W

The electrical specifications of this interface conforms to the RS 170-59 specifications.

Color Video Signal

Table 1-5
ELECTRICAL SPECIFICATIONS – Option 06 COLOR SIGNAL OUTPUT

Characteristics	Performance Requirements	Supplemental Information
TTL levels		Standard LS drive capabilities
Horizontal sync(L)		0 to 0.4
Vertical sync(L)		0 to 0.4V
Green(H)		2.4V
Red(H)		2.4V
Ground		Chassis

OPTIONS

No options are planned for the DAS 9100 Series Option 06 I/O Communication Interface. The unit is installed in the DAS mainframe at the I/O interface position. Only one I/O Interface can be installed in the DAS mainframe.

OPERATING INSTRUCTIONS

I/O CONNECTORS

RS-232 INTERFACES

The Master/Slave RS-232 connector (on the left) provides a serial data interface for use with the DAS. It may be used to establish master/slave transmission between two DAS systems, or it may be used for transmitting GPIB instructions between a DAS and a host controller.

The RS-232 PRINTER interface (on the right) may be used with a printer.

For information on how to establish DAS master/slave transmission, refer to the *Input Output Menu* section of the DAS Operator's manual. For GPIB information, refer to the GPIB Programming section of the DAS Operator's manual.

Figure 3-1 shows the RS-232 Connectors.

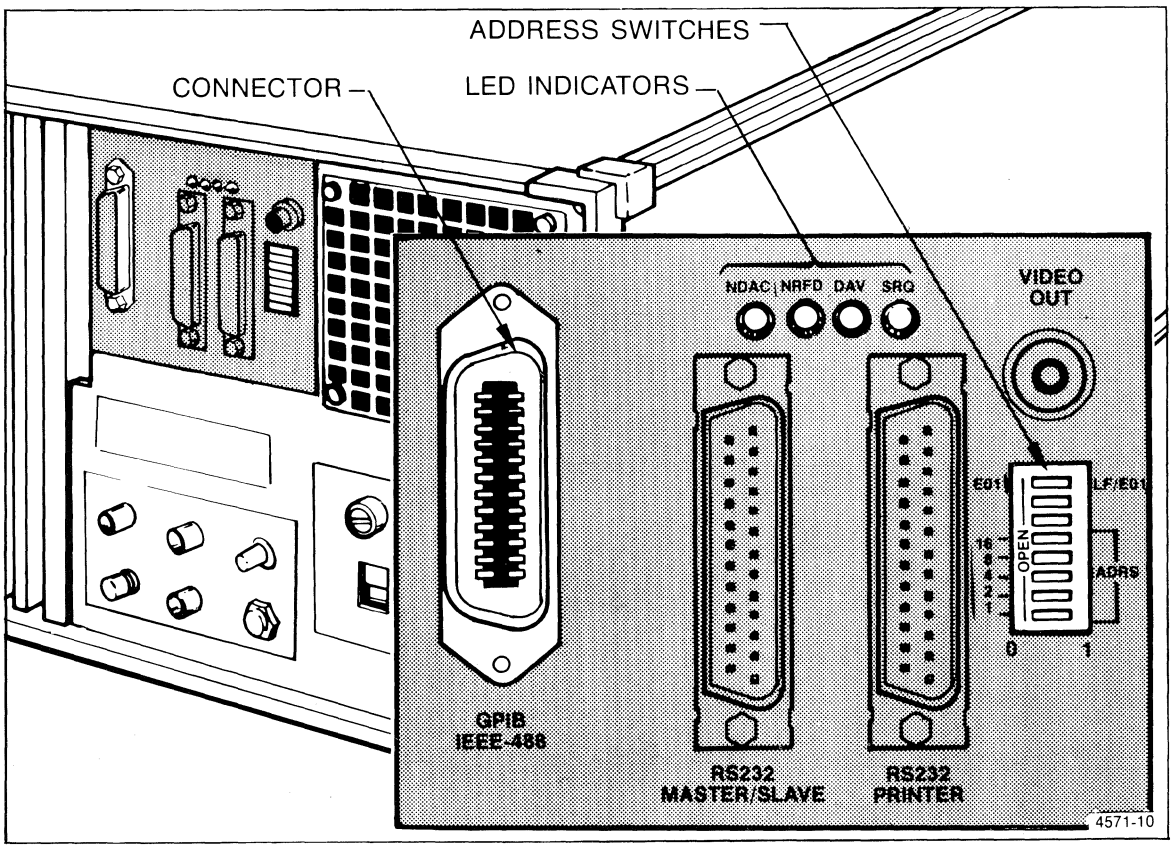


Figure 3-1. Option 06 I/O Communication Interface with LED Indicators, Address Switches, GPIB Connectors, and RS-232 Connectors.

Master/Slave RS-232 Connector

Eight pins are used:
- Pin 1 —Case Ground
- Pin 2 —Transmitted Data
- Pin 3 —Received Data
- Pin 4 —Request to Send
- Pin 5 —Clear to Send
- Pin 7 —Signal Ground
- Pin 8 —Carrier Detect
- Pin 20—Data Terminal Ready

Printer Connector

Seven pins are used:
- Pin 2 —Transmitted Data
- Pin 3 —Received Data
- Pin 4 —Request to Send
- Pin 5 —Clear to Send
- Pin 6 —Data Set Ready
- Pin 8 —Carrier Detect
- Pin 20—Data Terminal Ready

NOTE

If the Master/Slave RS-232 Interface is used with a modem, the modem should be configured for: No Auto Disconnect, No Loss of Carrier Detect, and No Abort Time Disconnect.

The Option 06 Master/Slave RS-232 connector can also be used in a null-modem mode, where the lines are connected without use of a modem. For this purpose, you can use the null-modem optional accessory or you can wire the communicating interfaces as shown below.

RS-232 Connector		RS-232 Connector	
Case Ground	Pin 1	Pin 1	Case Ground
Transmitted Data	Pin 2	Pin 3	Received Data
Received Data	Pin 3	Pin 2	Transmitted Data
Request to Send	Pin 4	Pin 8	Carrier Detect
Clear to Send	Pin 5	Pin 20	Data Terminal Ready
Signal Ground	Pin 7	Pin 7	Signal Ground
Carrier Detect	Pin 8	Pin 4	Request to Send
Data Terminal Ready	Pin 20	Pin 5	Clear to Send

When the Master/Slave RS-232 interface is used for GPIB transmission, only pins 2, 3, and 7 need to be connected. If a null modem is used, it must cross pins 2 and 3. Pin 5 can be toggled by the host controller to inhibit DAS character transmissions.

A minimum connection for the Printer Interface is pins 2, 3, and 7. Pin 5 may be toggled by the Printer to inhibit DAS transmission (high -- transmission, low -- no transmission).

GENERAL PURPOSE INTERFACE BUS (GPIB)

The General Purpose Interface Bus (GPIB) allows the DAS to communicate with any GPIB-compatible controller. The DAS operates as a talker and listener, but not a controller.

For detailed GPIB information, refer to the GPIB Programming section of the DAS Operator's Manual.

Figure 3-1 indicates the GPIB connectors and indicators located on the mainframe's back panel.

GPIB Switches. The eight DIP switches are used for setting the DAS talker/listener address on the bus. They are also used for specifying the end-of-message terminator character.

Switches 4-8 -- select the DAS talker/listener address.

Switch 1 -- selects the end of message terminator.

To set the primary GPIB address of the DAS, use a pen or other pointed object to set the address switches to the binary equivalent of the desired decimal address. For example, to set the DAS address to 12_{dec}, set the address switches to the binary equivalent as shown in Figure 3-2.

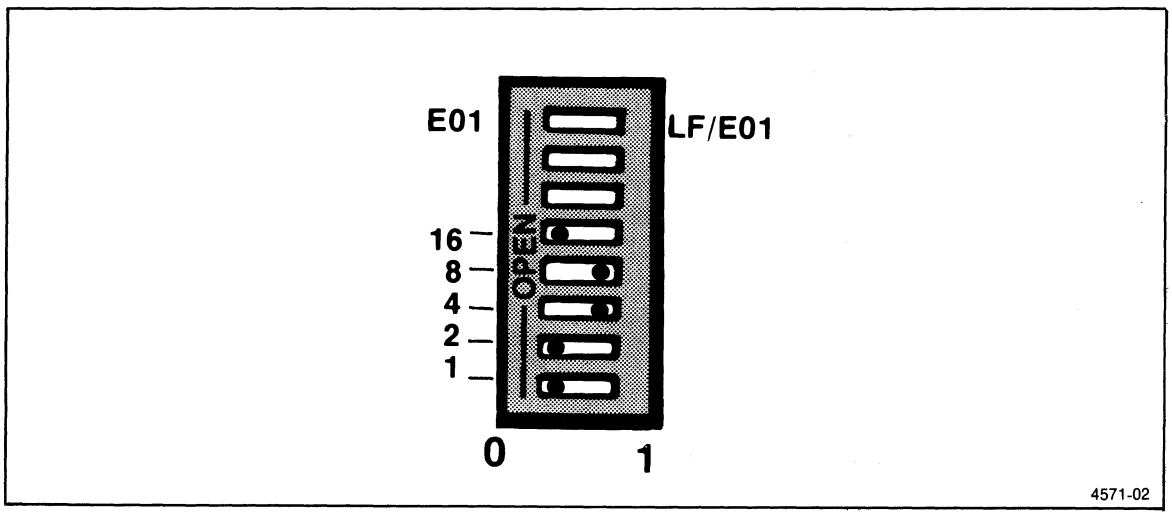


Figure 3-2. Address switch settings for GPIB address 12.

The Input/Output menu displays a readout of the GPIB address. If you are using an RS-232 interface with GPIB address 31, the readout appears as GPIB OFFLINE.

Switch 1 of the address selection switches (see Figure 3-2) sets the DAS end of the message terminator.

Switch 1 set to ON tells the DAS to

- accept LF or EOI as the end-of-message terminator.
- send CR followed by LF at the end of every message, with EOI asserted concurrently with the LF.

Switch 1 set to 0 tells the DAS to

- accept EOI only as the end of the message terminator.
- Assert EOI concurrently with the last byte of the message.

GPIB LEDs. The four LEDs indicate the current handshaking protocol in use between the DAS and the GPIB bus. They also indicate if a Service Request (SRQ) is present.

- SRQ Service Request
- NDAC Handshaking Protocol
- NRFD andshaking Protocol
- DAV Handshaking Protocol

GPIB Connector. The contact assignments for the GPIB connector are as follows:

Contact	Signal Line
1	DI01
2	DI02
3	DI03
4	DI04
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	SHIELD
13	DI05
14	DI06
15	DI07
16	DI08
17	REN
18	GROUND (6)
19	GROUND (7)
20	GROUND (8)
21	GROUND (9)
22	GROUND (10)
23	GROUND (11)
24	GROUND, LOGIC

COMPOSITE VIDEO INTERFACE

The composite video BNC connector provided with Option 06 may be used with any compatible hard copy or monitor unit. This connector is located on the mainframe's back panel as shown in Figure 3-1 under the name VIDEO OUT. Control of this interface is handled via the connected hard copy or monitor instrument.

NOTE

Be sure to read the composite video specifications carefully to ensure compatibility between the DAS video composite signal and a hard copy or monitor unit. These specifications are located in the first section of this manual under Specifications.

COLOR VIDEO SIGNAL

The Color Video Signal Jack can be reached through an opening on the back of the DAS to the left of the I/O Interface board.

See Figure 3-3.

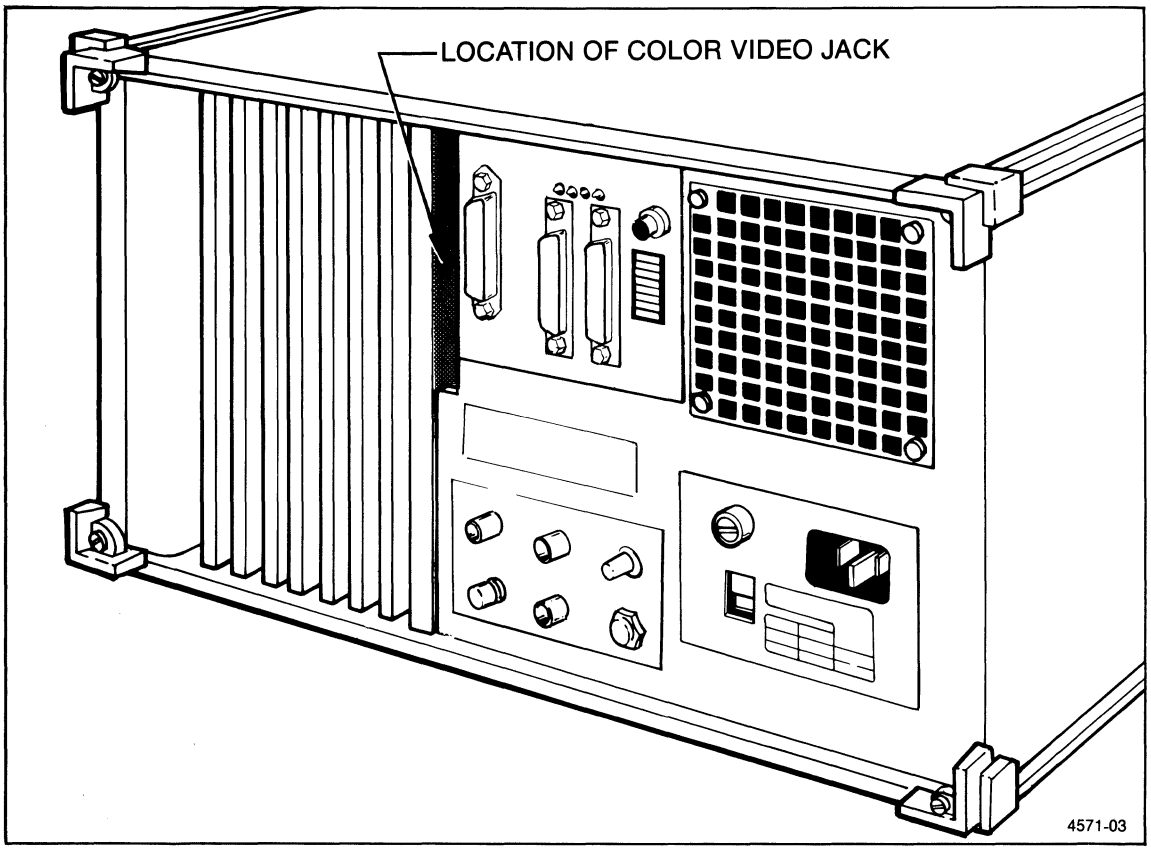


Figure 3-3. Location of the color video signal jack.

The pin outputs locations are as follows:

Pin	Location	Output
TTL levels		LS drive capabilities
Horizontal sync		(low true)
Vertical sync		(low true)
Green (high true)		(high true)
Red (high true)		(high true)
Ground		

KEYBOARD CONTROLS AND INDICATORS

MENU SELECTION

INPUT OUTPUT — This key accesses the Input Output Specification menu and displays it on the DAS screen. The functions of this menu only apply if the appropriate options (tape drive, Option 01, Option 06) are installed in the mainframe.

MENU FAMILIARIZATION

I/O FUNCTION

The tape drive operations, the RS-232 master/slave transmission, and the RS-232 Printer operation are controlled via the INPUT OUTPUT menu. GPIB transmission, over the GPIB or RS-232 interface, is controlled via the connected controller unit.

THEORY OF OPERATION

GENERAL DESCRIPTION

The Option 06 I/O Communication Interface schematics are marked off into functional blocks. The functions of all circuits within each block, the interaction between blocks, and the interaction between the I/O Communication Interface board and the rest of the DAS system is described in detail in this section. While reading this section, refer to the Option 06 I/O Communication Interface block diagram (Figure 4-1), and the schematics found in the *Diagrams and Circuit Board Illustrations* Section of this manual.

The DAS 9100 Series Option 06 I/O Communication Interface consists of an I/O Connection Panel on the back of the DAS; and a circuit board, the I/O Communication Interface board, installed in the DAS I/O interface slot. The panel and board are connected with a cable.

Schematics 88, 89, and 90 show the I/O Communication Interface board. Schematic 91 shows the smaller I/O Interface Connector board, which is attached to the I/O Connection Panel.

This I/O interface requires firmware version 1.11 firmware, or higher, and a DAS Controller board 670-7475-03. These Controller boards are normally installed in DAS mainframes with serial number B050100.

The Option 06 I/O Communication Interface connects the DAS to five different types of interface devices. These are:

- a GPIB (IEEE 488)
- an RS-232 Data Communications Equipment port, such as another (modem-equipped) DAS or a host computer
- an RS-232 Data Terminal Equipment port (e.g., a printer)
- a device that accepts black and white composite video signals (RS-170-compatible)
- a monitor that accepts TTL-level synchronization and color video signals

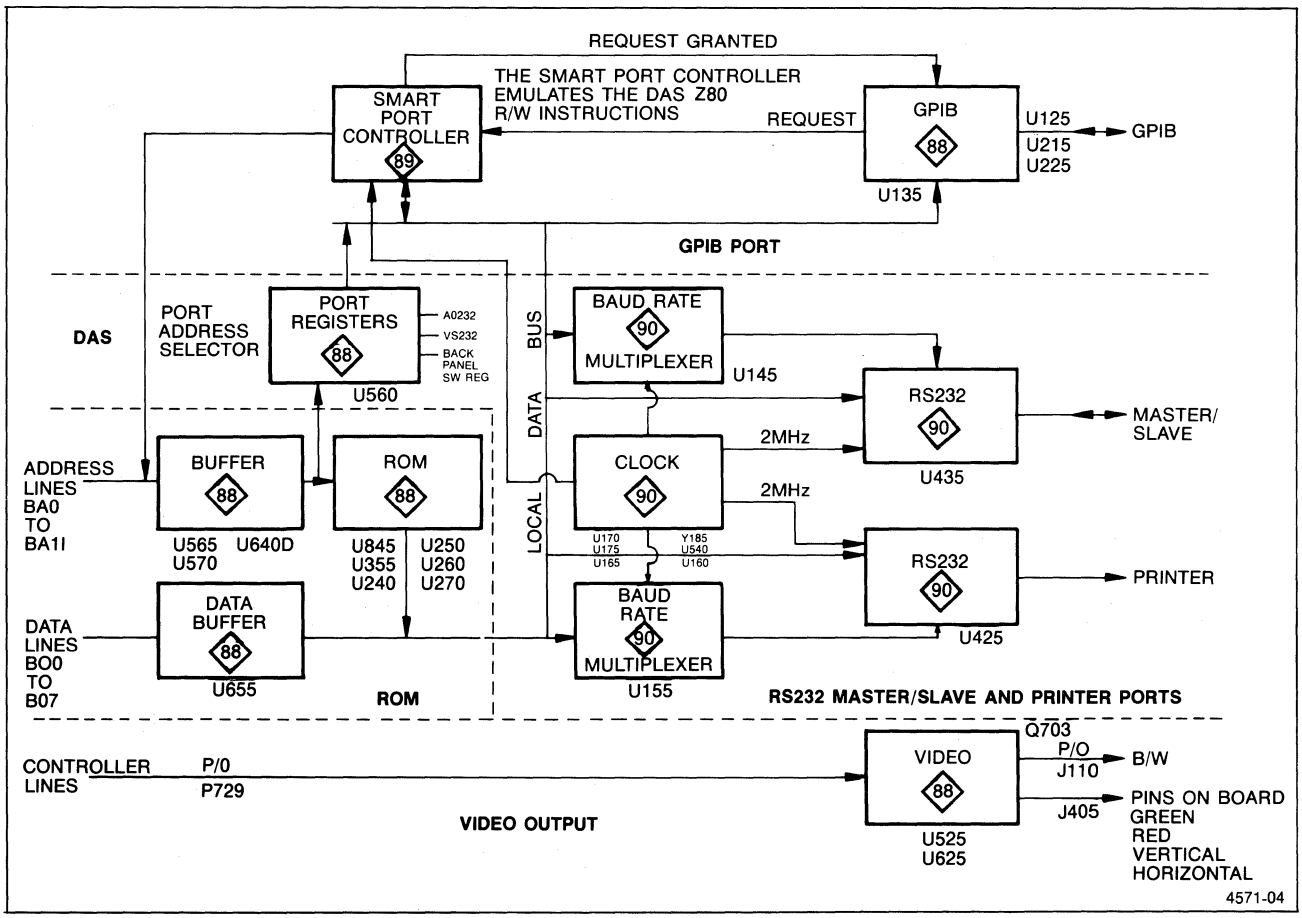


Figure 4-1. Option 06 I/O Communication Interface block diagram.

CIRCUIT DESCRIPTION

The I/O board interface circuitry takes data and control signals from the DAS Controller board and uses these signals to control the GPIB and RS-232 interfaces and to retrieve instructions from the firmware. The bidirectional data bus driver (U655) is always enabled except when Port 0F2*hex* is accessed. To prevent data bus contention, the data direction through the data bus driver is from the DAS controller to the Option 06 board, except during an Option 06 READ.

Buffers U215B and U315 transmit the GPIB address switch setting of the DAS when they are enabled.

U425 is the RS-232 Printer interface controller, U435 is the RS-232 Master/Slave interface controller, and U135 is the GPIB interface controller.

ROM

The DAS Z80 microprocessor can address up to 64K of programmable ROM in the Option 06. This memory is divided into eight 8K pages. The paging register is controlled by writing to port 00*hex*. Bits 0-2 determine which page is resident. Bits 3 through 7 are ignored. When power is first turned on, and before the first write to the paging register, page 0 is selected.

The four ROMs in the I/O communication interface that hold firmware to control the GPIB and RS-232 interfaces are U240, U250, U260, and U270. U570, U565, and U640D buffer the address bus and control signalsfrom the interconnect to communication interface ROMs. One of the four ROMs is selected by the data latched by the memory map register (U345). The data in the memory map register is decoded by U355 which, in turn, enables the selected ROM.

OR gate U455B detects when the ROMs are to be read and provides the enable signal for the memory map decoder. The ROM enable signals are SEL SLOT(L) and PERSONALITY(L), both of which are low true. When this combination of low true signals occurs, OR gate U455B outputs a low to enable the memory map decoder U355. U355 then decodes inputs A and B to select the ROM to be read. The ROM is selected by the three lowest data bits (LD0, LD1, and LD2) in conjunction with BRD(L). Table 4-1 shows the I/O communication interface ROM select code.

Table 4-1
I/O ROM SELECT CODES

D1	D0	Selected ROM
0	0	U240
0	1	U250
1	0	U260
1	1	U270

GPIB PORT

When a GPIB bus operation is selected, the DAS is both a talker and a listener, but not a controller. A controller, such as the Tektronix 4050 series or the Hewett-Packard HP98XX series, can communicate with the DAS using the GPIB interface and perform all operations for the DAS. The controller sends mnemonic commands to the DAS system. The DAS interprets these commands and performs the required tasks.

The GPIB address is set with the DIP switches on the back panel of the DAS mainframe. The switches define the binary GPIB address code (OFF = 0, ON = 1). The GPIB address switch buffers U215B, and U315 transmits the back-panel GPIB address-switch information to the DAS system.

The back-panel switch positions bits 0-4 represent a binary-encoded number from 0 to 31. A number between 0 and 30 (inclusive) corresponds to the available GPIB address, while address 31 (all switches on) specifies that the GPIB is disabled and that RS-232 Master/Slave port is active. Switch positions bits 5 and 6 are not connected. Switch position bit 7 specifies the terminator required for GPIB messages. If bit 7 is 1 (ON), then the message terminator is a CR (0D*hex*), LF (0A*hex*), and EOI. If bit 7 is 0 (OFF), then the terminator is just EOI.

The GPIB functions and the allowed subsets of these functions are defined by the IEEE 488-1978 Standard. The functions and subsets that apply to the DAS are listed in Table 4-2.

Table 4-2
DAS 9100 SERIES GPIB INTERFACE FUNCTIONS SUBSETS

Function	Description
SH1	Source handshake. Complete capability.
AH1	Acceptor handshake. Complete capability.
T6	Basic talker. Responds to Serial Poll, Untalk If My Listen Address (MLA) is received.
L4	Basic listener. Unlisten if My Talk Address (MTA) is received.
SR1	Service Request. Complete capability.
RL1	Remote Local. Complete capability.
PPO	Does not respond to Parallel Poll.
DC1	Device Clear. Complete capability.
DT1	Device Trigger. Complete capability.
CO	No Controller function.

The GPIB interface is implemented using the Texas Instruments intergated circuit TMS9914 (U135), which performs the interface function between an IEEE 488-1975/78 GPIB and a microprocessor. The TMS9914 chip communicates with the microprocessor by an I/O-mapped 8-bit data bus and provides a 16-bit bus to interface with the GPIB. IEEE 488-1975/78 standard protocol is handled automatically in Talker or Listener operational modes.

The IEEE 488 standard uses the negative logic convention for the GPIB lines. The FALSE state is represented by a high voltage (>2.0 V); the TRUE state is represented by a low voltage (<0.8 V). The GPIB terminations of the TMS9914 use this convention. For example, if Data Valid is true, the DAV line is pulled low by the device. The controller chip terminations are connected to the GPIB cable through non-inverting buffers to obtain the correct signal polarity. Buffers U125 and U225 are functionally dedicated GPIB bus transceivers used to isolate the GPIB controller chip from the GPIB data bus cable. Table 4-3 lists the TMS9914 pin functions and describes each function.

NOTE

The terminations on the microprocessor side of the 9914 are in positive logic, making it compatible with the DAS microprocessor. The manufacturer of the TMS9914 GPIB controller circuit labels the data transfer bits D7-LSB and D0-MSB and the data input/output lines DI01-LSB and DI08-MSB. When in DMA mode, the sense of the DBIN line is reversed compared to normal microprocessor read/writes.

Table 4-3
TMS9914 PIN FUNCTIONS

Name	Pin	Function
ACCRQ(L) (GPIB REQ)	1	ACCESS REQUEST: this line goes low to request a direct memory access.
ACCGR(L)	2	ACCESS GRANTED: when received from the direct memory access controller, this line enables the byte onto the data bus.
CE(L)	3	CHIP ENABLE: When this line is low the chip is active.
WE(L)	4	WRITE ENABLE: when low, this line indicates to the TMS9914 that data is being written to one of its registers.
DBIN	5	DATA BUS IN: a high state indicates to the TMS9914 that a read is about to be carried out by the MPU. A low state indicates a read during DMA mode.
RS0 RS1 RS2	6 7 8	REGISTER SELECT LINES: determines which register is addressed by the MPU during a read or write operation.
INT(L)	9	INTERRUPT: sent to the MPU to cause a branch to a service routine.
D7 (lsb)	10	Data transfer bits on the MPU side of the device.
D6 D5 D4 D3 D2 D1 D0 (msb)	11 12 13 14 15 16 17	
CLOCK(L)	18	CLOCK: up to 4 MHz clock.
RESET(L)	19	RESET: initializes the TMS9914 at power-up.
	20	Ground reference voltage.
TE	21	TALK ENABLE: controls the direction of transfer of the line transceivers.
REN	22	REMOTE ENABLE: sent by the system controller to select control either from the front panel or from the GPIB.
IFC	23	INTERFACE CLEAR: sent by the bus system controller to set the interface system to a known quiescent state. The bus system controller becomes the bus controller in charge.

Table 4-3 (Cont.)
TMS9914 PIN FUNCTIONS

Name	Pin	Function
NDAC	24	NOT DATA ACCEPTED: handshake signal. Acceptor sets this high when it has latched the data from the I/O lines.
NRFD	25	NOT READY FOR DATA: handshake signal. Sent by acceptor to indicate readiness for the next byte.
DAV	26	DATA VALID: handshake signal controlled by source to show acceptors when valid data is present on the bus.
EOI	27	END OR IDENTIFY: if ATN is high, this indicates the end of a message block. If ATN is low, the bus controller is requesting a parallel poll.
ATN	28	ATTENTION: sent by bus controller in charge when low interface commands are being sent over the DIO lines. When this signal is high, the DIO lines carry data.
SRQ	29	SERVICE REQUEST: set low by a device to indicate a need for service.
CONT(L)	30	CONTROLLER: controls the direction of the transfer of the bus transceivers for the bus management lines (ATN and SRQ). When high, the device is the bus controller in charge.
DIO8 (msb) DI07 DI06 DI05 DI04 DI03 DI02 DI01 (lsb)	31 32 33 34 35 36 37 38	DIO8 through DIO1 are the data input/output lines on the DI07 32 GPIB side. These pins connect to the IEEE 488 bus via non-inverting transceivers.
TR	39	TRIGGER: activated when the GET command is received over the interface or the FGET command is given by the MPU.
	40	Supply voltage (+5 V nominal).

SMART PORT CONTROLLER

Refer to the Smart Port Controller (SPC) block diagram (Figure 4-2) and SPC schematic 89 (found in the *Diagrams and Circuit Board Illustrations* section) while reading this section.

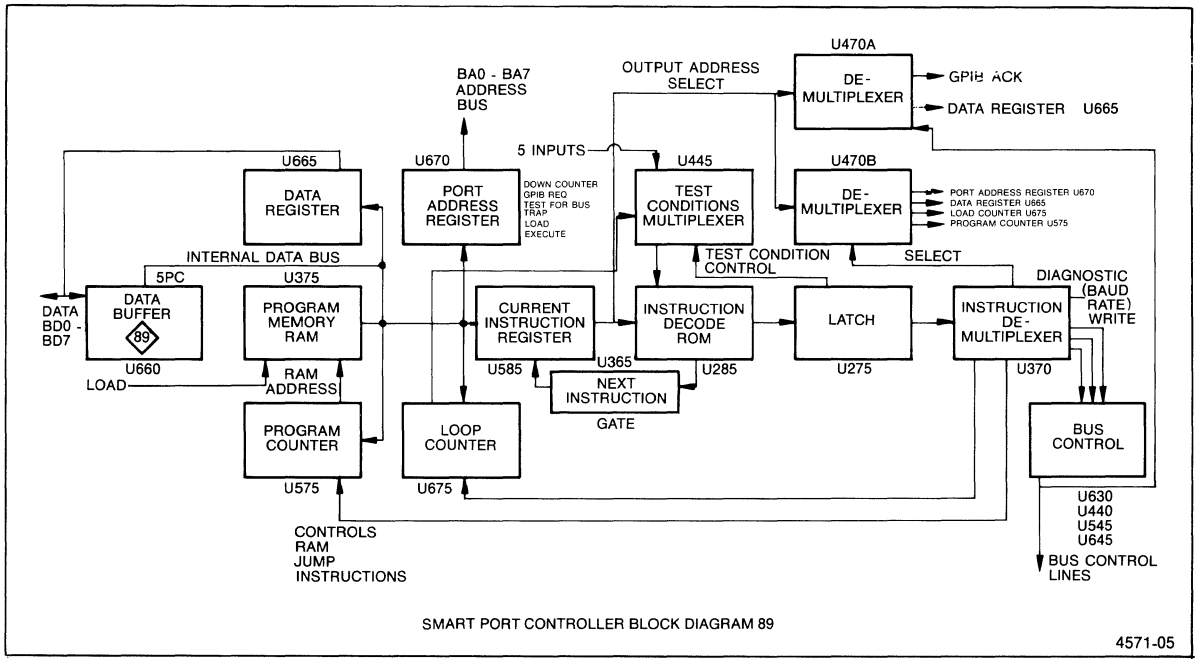


Figure 4-2. Smart Port Controller block diagram.

The Smart Port Controller is a hardware state machine designed to emulate the DAS microprocessor (Z80) port read and write instructions. Because the Smart Port Controller is dedicated hardware, it can perform port-to-port transfers at a much higher rate than the Z80. The purpose of the Smart Port Controller is to send and receive GPIB data over the GPIB interface at rates of 200K bytes/sec. The Smart Port Controller cannot, however, be used with the RS-232 UARTs (Universal Asychronous Receiver and Transmitter) because the UARTs do not have the necessary handshake lines.

The Smart Port Controller executes programs written to its memory by the DAS Z80 as shown by the programming model in Figure 4-3. Programs of this type transfer data between ports in the DAS port address space. The maximum program length is 256 bytes.

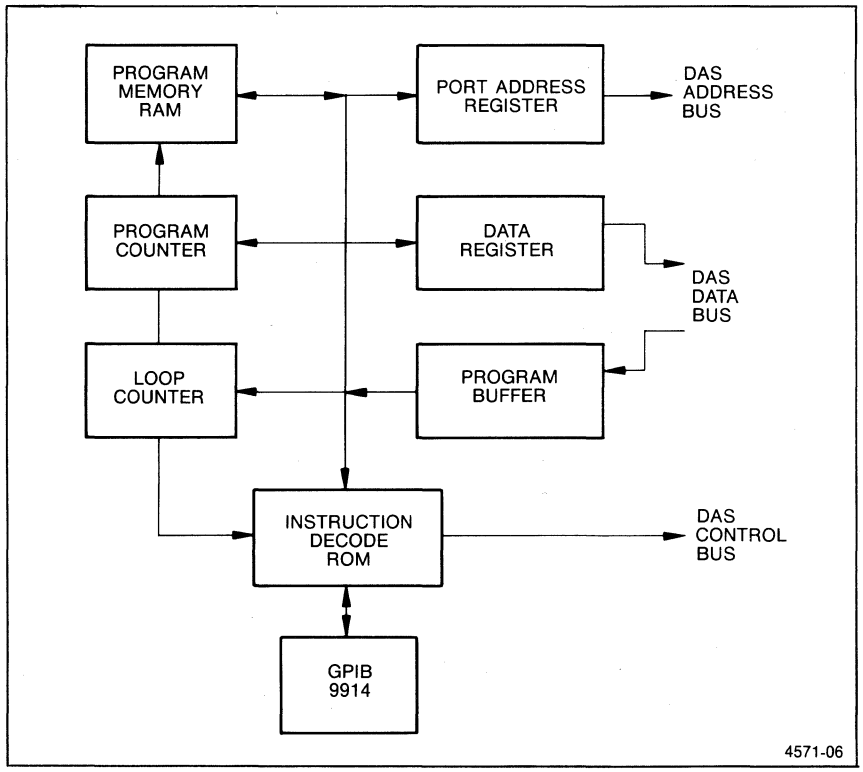


Figure 4-3. Smart Port Controller Programming Model for programs written by the DAS Z80 and executed by the SPC.

SPC Operating Modes

The SPC is always in one of three modes. These are:

- Load Program
- Execute Program
- Halt

The SPC initializes at power-up to the Load Program mode. It enters Execute Program mode when the DAS Z80 reads from port 0F2*hex* after a program has been loaded. The last instruction in a program is always halt, which causes the SPC to enter the Halt mode. When the SPC executes the halt instruction, it loops on itself and waits for the instruction to enter the Load Program mode. The SPC enters the Load Program mode when a *read* from port 0F3*hex* is detected. The SPC then scans for load write or begin execution read. The same program can be repeatedly executed by reading from the load port to force the Load Program mode, and then reading from the execute port. When U465 (pin 9) is high, the Load Program mode is executed. When U585 (pin 10) and U465 (pin 9) is low, the SPC is in Halt mode.

SPC Registers

The SPC can load four eight-bit registers. They are:

- the Port Address Register (U670)
- the Data Register (U665)
- the Program Counter (U575)
- the Loop Counter (U675)

The port address register always drives the lower eight bits of the address bus during a transfer. In this way, the port address register specifies which port in the DAS Z80 port space is addressed.

When specified as the source, the data register places an eight-bit byte onto the DAS data bus.

The program counter can be loaded for a jump. The loop counter can be loaded and decremented. Because of the hardware implementation, the loop counter must be loaded with the ones complement of the number of counts desired; for example, if a count of ten (00001010) is desired, then 0F5*hex* (11110101) must be loaded.

The decrement, test, and jump non-zero operations are all implemented in one instruction in the SPC. The same method is used in the Z80 DJNZ instruction.

SPC Transfers

When a transfer occurs, one of two devices is specified as the destination and one of three devices is specified as the source of the transfer. The valid destinations are:

- the GPIB controller
- the port addressed by the port address register.

The three sources are:

- the GPIB controller
- the port addressed by the port address register
- the SPC data register.

NOTE

When the transfer source for the GPIB port is instruction 1XX010ss and the source is the Data Register (ss = 00), the port addressed by the Smart Port Controller's (SPC) address port register must be a non-existent port. Otherwise, the correct data to be transfered to the GPIB in the SPC's data register is replaced by the data at the addressed port.

Table 4-4 lists some of the DAS port assignments.

Table 4-4
PARTIAL DAS PORT ASSIGNMENTS

Port	R/W	Function
000*hex*	W	ROM Mapping Register
0A0*hex*	W	Baud Rate Generator Master/Slave
0AF*hex*	R/W	Phantom Port used for NOP R/W
0F0*hex*	R	Back Panel Address Switches
0F1*hex*	W	Baud Rate Generator Printer Port
0F1*hex*	R	Baud Rate Read-Back Port (diagnostic use only)
0F2*hex*	R	Execute Program Command to SPC
0F3*hex*	R	Load Program command to SPC
0F3*hex*	W	Load Program into SPC Memory
0F4*hex*	R/W	Data Register Master/-Slave 8251A
0F5*hex*	R/W	Control Register Master/-Slave 8251A
0F6*hex*	R/W	Data Register Printer 8251A
0F7*hex*	R/W	Control Register Printer 8251A
0F8*hex*	R	9914 Interrupt Status 0
0F9*hex*	R	9914 Interrupt Status 1
0FA*hex*	R	9914 Address Status
0FB*hex*	R	9914 Bus Status
0FC*hex*	R	9914 Address Switch
0FE*hex*	R	9914 Command-Pass-Through

Table 4-4 (Cont.)
PARTIAL DAS PORT ASSIGNMENTS

Port	R/W	Function
0F0*hex*	W	9914 Interrupt Mask 0
0F9*hex*	W	9914 Interrupt Mask 1
0FB*hex*	W	9914 Auxiliary Command
0FC*hex*	W	9914 Address Register
0FD*hex*	W	9914 Serial Poll
0FE*hex*	W	9914 Parallel Poll
0FF*hex*	R/W	9914 Data Register

The DAS mapping registers must be programmed to match the port for an SPC transfer. Program the SPC before the transfer is started. The program can map the DAS mapping registers for the port before the transfer and remap the DAS mapping registers with the startup code at the end of the transfer if the code is in an unmapped address space. The startup code could reside in an unmapped space of the mapping registers and map the card in for the data transfer and out at the end of a data transfer.

If an interrupt occurs, the interrupting routine may use a different space of the DAS mapping registers. Because of this, interrupts must be disabled during a transfer. When the interrupt is disabled, it is not possible for any other routine to run the mapping registers while a transfer is in progress.

To abort a transfer, read port 0F3*hex*. Reading this port returns the SPC to the Load Program mode.

The SPC takes control of the DAS bus by asserting the bus request line and the DAS microprocessor releases the bus by asserting the bus acknowledge line.

The SPC takes control of the DAS bus using the bus request/bus acknowledge line; the CRT controller uses the same line. Because they share the same line, conflicts may arise. For this reason, the CRT controller must be disabled during a smart port transfer.

SPC Memory

At power-up, the Smart Port Controller enters the Load Program mode. As it enters this mode, the SPC zeros the microprogram counter and waits for the incoming bytes to load into the program memory. The DAS Z80 loads the program by writing to an I/O port (0F3*hex*). Every time there is a port write, a flag is set for the SPC. When this flag is encountered, the program counter is incremented so that the next write goes to the next sequential memory location. The SPC can accept data about four times faster than the DAS Z80 can send it.

When the program is loaded, execution is begun by reading from port address 0F2*hex*. Bit 5 of the port 0F0*hex* (switch register port) indicates when the SPC has completed the program execution; a 1 indicates still busy, while a 0 indicates program complete. After a program has run to completion, the DAS Z80 can force a return to the Load Program mode by reading from port 0F3*hex*.

For diagnostic purposes, the data read, when port 0F2*hex* is addressed, is the contents of the SPC data register. Use such a data read with caution. If the SPC is in the Load Program mode, the read starts the program's execution. Conversely, if the SPC is executing the halt instruction, the read will have no effect.

SPC INITIALIZATION

The SPC is in the Load mode at power-up. To load data into the Program Memory RAM (U375), the Write Enable line, WE(L) (pin 21) of the Program Memory RAM must be enabled. The WE(L) signal comes from the OR gate (U455). This line is controlled by two signals. These are:

- Buffered Bus Write Control LWR(L)
- WE(L) the Load Command (Port 0F3H) from U560 (schematic 88) pin 12

The bus signals sent to the SPC are buffered. At the buffer, the signal name changes, but the signal does not. For example, BWR(L) is the same as LWR(L). The LWR signal is confined to the Option 06 I/O Communification Interface board.

When the program has been loaded into the Program Memory RAM by the DAS firmware, the DAS starts the program by issuing an Execute command (a READ from I/O port 0F2*hex* to the SPC. This command comes from pin 13 of U560 through the RS latch (U465). The microcode in the Instruction Decode ROM (U285) controls the operation of the SPC.

The Execute command calls the microcode for the Execute mode. In the Execute mode, line 4 on the Test Condition Multiplexer (U445) goes low, causing the Instruction Decode ROM to clear the program counter (U575) and fetch the first instruction from the Program Memory RAM. This causes pin 9 of U445 to go low and starts the program loaded into the Program Memory RAM. After each instruction from the Instruction Decode ROM has been executed, the program counter is incremented to fetch the next instruction.

The current instruction is loaded into the Current Instruction Register (U585), which in turn controls the Instruction Decode ROM (U285).

The instruction programs in the Instruction Decode ROM are:

- load program into memory
- halt
- jump
- load data register
- load port address register
- load the loop counter
- transfer data register to the GPIB port
- transfer DAS port to the GPIB port
- transfer data register to the DAS port
- transfer data register to the baud rate generator port (diagnostics)
- transfer GPIB to the DAS port
- diagnostic instructions

Tables 4-5 lists the SPC opcode, ROM address, and instruction set.

Table 4-5
SMART PORT CONTROLLER

OPCODE		ROM ADDRESS OF MICRO-INSTRUCTION	DESCRIPTION
HEX	BINARY 76543210		
00	0XX00000	000 - 00F	Special instruction for loading MEM (DO NOT USE)
01	0XX00001	010 - 01F	HALT, CLEAR PROGRAM COUNTER
84	1XX00100	040 - 04F	JUMP, (address follows)
85	1XX00101	050 - 05F	LOAD DATA REGISTER (data follows)
86	1XX00110	060 - 06F	LOAD PORT REGISTER (address follows)
87	1XX00111	070 - 07F	LOAD LOOP COUNTER (count follows)
	1XX100SS		Transfer to GPIB Group
88	1XX01000	080 - 08F	FROM DATA REGISTER
89	1XX01001	090 - 09F	FROM DAS PORT
8A	1XX01010	0A0 - 09F	FROM GPIB (illegal)
8B	1XX01011	0B0 - 0BF	UNUSED
	1XX100SS		TRANSFER TO DAS PORT GROUP
90	1XX10000	100 - 10F	FROM DATA REGISTER
91	1XX10001	110 - 11F	FROM DAS PORT (to phantom port)
92	1XX10010	120 - 12F	FROM GPIB
93	1XX10011	130 - 13F	UNUSED
	1XX110SS		TRANSFER TO BAUD RATE GEN GROUP
A8	1XX11000	180 - 18F	FROM DATA REGISTER (diagnostics)
A9	1XX11001	190 - 19F	FROM DAS PORT (not used)
AA	1XX11010	1A0 - 1AF	FROM GPIB (not used)
AB	1XX11011	1B0 - 1BF	UNUSED
9C	1XX11100	1C0 - 1CF	Decrement & Jump if non-zero (ADDRESS follows)
9F	1XX11111	1F0 - 1FF	Special diagnostic instruction (DO NOT USE)

The current microinstruction in the Instruction Decode ROM is the input to register U275. Bits 0 through 2 are fed back to the input of the Instruction Decode ROM (U285) to function as a microcode program counter. These three lower bits increment from 0 to 7 to execute the program in the ROM for that particular instruction. At the same time the Instruction Decode ROM is providing this microinstruction, it is monitoring the test bit conditions that are being sent to the Test Condition Multiplexer (U445) at input address A3. The instruction in the Decode ROM is divided into two parts; the value of the test bit determines which one is accessed.

The test conditions (when the SPC is in Execute mode) are:

- Loop Counter going to 0
- GPIB REQ
- Test for Bus Trap

The test conditions (when the SPC is in Load mode) are:

- Load
- Execute

The programs in the Instruction Decode ROM (U285) use the mode information to determine which control signals to output.

FOUR SPC PROGRAM INSTRUCTION DESCRIPTIONS

Four SPC program instruction descriptions are listed to show the operation of the SPC. These instructions are:

- load data register
- load port address register
- load the loop counter
- transfer data register to GPIB

Load Data Register

The instruction for loading the data register is opcode 85*hex* which comes from the program memory RAM. This opcode points to the SPC starting address (050*hex* or 058*hex* depending on the value of the test bit) of the instruction stored in the Instruction Decode ROM. Figure 4-4 is the timing diagram for the Load Data Register instruction.

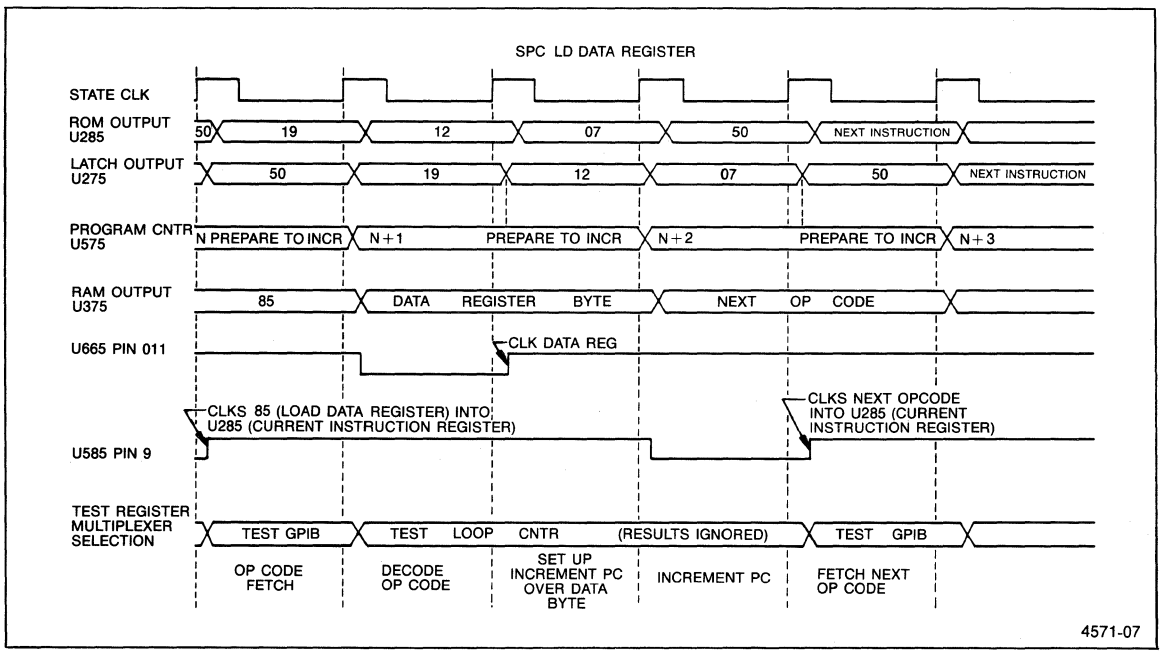


Figure 4-4. Smart Port Controller timing diagram for the Load Data Register instruction.

Part of the address to the Instruction Decode ROM is the lower five bits output from the Program Memory RAM (U375). These five bits are the upper five bits of the address to the Instruction Decode ROM. The lower three bits of the address are fed back from the ROM output. The lower three bits are the address for the next microinstruction. The fourth address bit is the latched output of the Test Condition Multiplexer (U445).

The microinstruction to load the data register is in the Instruction Decode ROM at address 50_{hex}. This microinstruction may hold, jump, or increment between addresses 50_{hex} to $5F_{hex}$. The status of the Test Condition bit (value of 0 or 1) at address A3 of the Instruction Decode ROM determines which microinstruction is selected. In the case where the test condition is meaningless, the upper and lower microinstruction is the same for a Test Condition bit equal to 1 or 0.

The first command from the Load Data Register program is a 19_{hex} from the Instruction Decode ROM. This command selects the test loop counter by outputting a 0_{hex} to both the A and B control inputs of the Test Condition Multiplexer (U445). For this instruction, the result of the test condition bit is meaningless and has no effect

Bits 3, 4, and 5 of the microinstruction control signal drive the Instruction Demultiplexer (U370). For the micro instruction code 19_{hex}, output 3 (pin 12) of the Instruction Demultiplexer is selected, enabling the Control Demultiplexer (U470B). The control for U470B comes from the lower two bits of the current instruction (85_{hex}). In this case, output 1 (pin 11) of U470B is selected, which drives the clock input to Data Register U665 low.

The next microinstruction is 12_{hex}. This microinstruction drives the clock input to the Data Register (U665) high so that data latches into the data register. At the same time, the Program Counter (U575) is set up to increment when the next state clock pulse occurs.

The state clock pulse that clocks the next microinstruction (07_{hex}) into the latch (U275), also increments the program counter. When the program counter is incremented, the Program Memory RAM (U375) outputs the next opcode. This microinstruction (07_{hex}) drives the clock input of the Current Instruction Register (U585) low by driving all three inputs of NAND gate U365 high.

The next microinstruction is 50_{hex}. This microinstruction sets the clock input of the Current Instruction Register (U585) high, loading the next opcode instruction into the input register. The Test Condition Multiplexer (U445) is set to test D2 GPIB REQ (L). At the same time, the Program Counter (U575) is set to increment when the next state clock pulse occurs.

The next-to-last microinstruction always drives the clock input of the Current Instruction Register address (U585) low. The last microinstruction is always 50_{hex}, which is required to increment the program counter.

Load Port Address Register

The instruction to load the Port Address Register starts at decode ROM address 60_{hex}.

For the instruction Load Port Address Register, the Control Demultiplexer (U470B) selects output 2. Output 2 is the clock input signal to the Port Address Register (U670). The operation of the Load Port Address Register instruction is the same as the operation of the Load Data Register instruction, except that the data output of the memory RAM is moved into the Port Address Register. See *Load Data Register* in this section of the manual.

Load Loop Counter

The instruction to load the Loop Counter (U675) starts at Decode ROM address 70_{hex}.

For the instruction Load Loop Counter, output 3 of the Control Demultiplexer (U470B) is selected. Output 3 is the load signal to the Loop Counter (U675). The operation of the Load Loop Counter instruction is the same as the operation of the Load Data Register instruction, except that data from the memory RAM is clocked into the loop counter. The count is the complement of the count wanted, because the loop counter is an up counter. See *Load Data Register* in this section of the manual.

Transfer Data Register to GPIB

The instruction to load the GPIB port starts at address 80_{hex} in the decode ROM. The 80_{hex} instruction tests the GPIB REQ line and waits until the GPIB transfer is ready. When the GPIB transfer is ready, the Decode ROM outputs an $E9_{hex}$. If the GPIB port is not ready, the decode ROM outputs microinstruction 41_{hex} until a GPIB REQ (L) = 0 is asserted. The instruction EA_{hex} is then issued.

Instruction EA_{hex} selects output 5 of the Instruction Demultiplexer (U370). The demultiplexer output drives the Bus Request line (BREQ) low and pin 14 of the Bus Trap flip-flop high. Bits 6 and 7 from the decode ROM select the Bus Trap test bit (input 3) of U445, and drive the signal BRD and BWR (Read and Write) lines high (no read or write).

NOTE

BRD and BWR are not driven by the SPC, until the SPC traps the bus.

When Bus Acknowledge (BACK) is received, it triggers the Bus Trap flip-flop (U630), which drives the Bus Trap test bit low. In addition, BACK enables the Control Demultiplexer (U470A). The control demultiplexer output enables Data Register (U665). When the bus trap test signal is low, the Instruction Decode ROM outputs the microinstruction $7A_{hex}$. This microinstruction holds BWR high, and BRD and GPIB acknowledge ACK(L) low. Now the Instruction Decode ROM outputs a $7B_{hex}$ microinstruction, which continues to drive BRD and GPIB ACK low.

NOTE

When the transfer source for the GPIB port is instruction 1XX010ss and the source is the data register (ss = 00), the port addressed by the SPC Address Port Register must be a non-existent port. Otherwise, the correct data to be transferred to the GPIB in the the SPC's Data Register is in contention with the data at the addressed port.

While BRD and GPIB ACK are low, the lower bits of the address bus are driven by the port address register. When BRD goes low, data is transferred from the SPC Data Register (U665) to the GPIB Controller (U135 on schematic 88).

RS-232 MASTER/SLAVE AND PRINTER PORTS

Master/Slave Port (RS-232 DTE)

The Master/Slave port is a standard RS-232 Data Terminal Equipment (DTE) port. The serial-to-parallel data conversion is performed by an Intel 8251A UART. The 8251A Request To Send (RTS) and Clear To Send (CTS) RS-232 pins are connected to the corresponding RS-232 signals. The 8251A Data Set Ready input pin is connected to the Carrier Detect RS-232 signal. The RS-232 signal Data Terminal Ready is connected to +12V through a 2.7K resistor.

The baud rate generator circuits for the RS-232 Master/Slave port and the RS-232 Printer port are identical. The available baud rates are identical and the maximum baud rate is 9600.

Printer Port (RS-232 DCE)

The Printer Port is an RS-232 Data Communications Equipment (DCE) port which is implemented using another 8251A UART. This RS-232 channel is wired as a Data Communications Equipment interface. The 8251A's RTS pin controls the DSR interface signal. The 8251A CTS pin is connected to the DTR interface signal. The Request To Send RS-232 interface signal is connected directly to the Clear To Send interface signal. The Carrier Detect interface signal is hard-wired to true (+12V through a 2.7K resistor).

The baud rate generator circuits for the RS-232 Printer port and the RS-232 Master/Slave port are identical. The available baud rates are identical and the maximum baud rate is 9600.

The transmitter and the receiver channel are properly interfaced to the printer connector. The printer port can input characters. By allowing the printer port to input characters, it is possible to support X-ON (control Q, 011_{hex}) and X-OFF (control S, 013_{hex}) handshake protocol.
The Master/Slave and Printer port both use an 8251A UART (U435 and U425 on schematic 90). Table 4-6 lists the 8251A pin functions.

The output buffers are common to both the Master/Slave and Printer ports. Buffers U635, U415, and U510 are line drivers used to isolate the RS-232 chips from the RS-232 system interface.

Table 4-6
8251A PIN FUNCTIONS

Name	Pin	Function
D0	27	D0 through D7 are tri-state bidirectional data bits that interface the data bus and the 8251A. Data, control words, command words, and status information are transmitted by these bits.
D1	28	
D2	1	
D3	2	
D4	5	
D5	6	
D6	7	
D7	8	
RxD	3	RECEIVE DATA: this pin receives the serial data input.
GND	4	GROUND: the ground reference voltage for the IC.

Table 4-6 (Cont.)
8251A PIN FUNCTIONS

Name	Pin	Function
TxC(L)	9	TRANSMITTER CLOCK: controls the rate at which characters are transmitted.
WR(L)	10	WRITE: when low, informs the 8251A that the CPU is writing data or control words to the 8251A.
C/[D(L)]	12	CONTROL/DATA: in conjunction with the WR(L) and RD(L) inputs, informs the 8251A whether the word on the data bus is a data character (low) or a control word or status information (high).
RD(L)	13	READ: when low, informs the 8251A that the CPU is reading data or status information from the integrated circuit.
RxRDY	14	RECEIVER READY: indicates that the IC contains a character that is ready to be sent to the CPU.
TxRDY	15	TRANSMITTER READY: indicates to the CPU that the transmitter is ready to accept a data character.
SYNDET/BD not used	16	SYNC DETECT/BREAK DETECT: acts as either an input or an output. When used as an output, the pin goes high to indicate that the SYNC character has been located and identified. When used as an input, a positive-going signal causes the IC to start assembling data characters on the rising edge of the next RxC(L) signal.
CTS(L)	17	CLEAR TO SEND: when low, enables transmission of serial data if the TxEnable bit in the command byte is set to a logic 1.
TxEMPTY	18	TRANSMITTER EMPTY: goes high when the IC has no characters to transmit.
TxD	19	TRANSMITTER DATA: outputs the serial data and control words from the IC.
CLK	20	CLOCK: used to generate internal timing. No external inputs or outputs are referenced to CLK.
RESET	21	RESET: when high, forces the IC into an idle mode.
DSR(L)	22	DATA SET READY: general-purpose one-bit inverting input port.
RTS(L)	23	REQUEST TO SEND: general-purpose one-bit inverting output port.
DTR(L)	24	DATA TERMINAL READY: general-purpose one-bit inverting output port.

Table 4-6 (Cont.)
8251A PIN FUNCTIONS

Name	Pin	Function
RxC(L)	25	RECEIVER CLOCK: controls the rate at which the serial data is to be received.
Vcc	26	Supply voltage (+5 volts nominal).

VIDEO OUTPUT

There are five video output signals: a composite monochrome video signal and four TTL-level video signals.

The composite monochrome video output signal appears at the BNC connector on the back panel. OR gate U625C forms the composite video signal (B/W) from the HORZ SYNC, VERT SYNC, and VIDEO(L) signals. Transistor Q703 is the final driver for the composite video output signal.

NOTE

The composite video output must be properly terminated (75Ω) to ground for proper signal levels. Most peripherals (monitors and hard copiers) provide the correct termination.

The color TTL-level signals are VERTICAL SYNC (L), HORIZONTAL SYNC (L), GREEN, and RED. These signals appear on five square pins (pin 1 red, pin 2 green, pin 3 vertical sync, pin 4 horizontal sync, and pin 5 ground). These pins are located at the back of the main Option 06 I/O Communication Interface board (located in the DAS I/O interface slot).

CAUTION

No protection is provided for these TTL video outputs. Connecting these outputs to other than passive inputs can cause damage to the DAS.

I/O INTERFACE CONNECTOR

The I/O interface connector is a sub-assembly of the Option 06 I/O Communication Interface. This sub-assembly is attached to the back panel of the DAS mainframe and contains the GPIB connector, the two RS-232 connectors, and the composite video (B/W) connector for the I/O communication interface.

In addition, the I/O connector also holds four LEDs and a set of DIP switches. The four LEDs indicate the GPIB status. The DIP swiches select the DAS Talker/Listener address on the GPIB and select the type of terminal end-of message terminator.

VERIFICATION AND ADJUSTMENT PROCEDURES

INTRODUCTION

This section of the manual contains only functional check procedures. These procedures, along with the test setup information at the beginning of this section, allows a qualified technician to verify the operation of the I/O Communication Interface.

The Option 06 has no adjustments or performance verification procedures.

Functional Check Procedures. These tests verify that the device being tested is operational or that repair is necessary. The procedures exercise the main interfaces of the device and checks its internal features. These tests can be used to determine whether repair is necessary

Test Setup Information. The procedures in this section require some test equipment, setups and general information. This information and a list of suggested test equipment is presented at the beginning of each functional check.

FUNCTIONAL CHECK PROCEDURES

This functional check procedure has three parts. The first part requires only the following piece of equipment:

- DAS mainframe with the Option 06 I/O Communication Interface installed

The second and third parts of the functional check requires specialized equipment. The following equipment is required for the checks:

- Tektronix 4050 Series Desktop Computer with Data Communications Interface
- Tektronix DAS 9100 Series Logic Analyzer with a 91A32 Data Acquisition Module
- RS-232 cable 012-815-00
- GPIB cable 012-0630-03
- null modem (constructed according to the schematics as shown in Figure 5-3 and 5-4)

NOTE

All BASIC programs found in this text must be run on a 4051 Tektronix computer to avoid incompatabilities with other versions of BASIC. If you have a different controller, you will have to develop a program for it which is the equivalent of the one provided.

The 4051 stimulates and reads the RS-232 and GPIB ports of the DAS I/O communication interface. The null modem allows the 4051 and the DAS to communicate without a regular modem.

For instructions on the use of the DAS menus, refer to the *Operating Instructions section of the DAS 9100 Series Operator's manual.*

FUNCTIONAL CHECK, PART 1

GPIB Address Switch Operation Verification

1. Set the address switches on the back of the DAS mainframe to 01. This is done by setting the DIP switch on the back of the DAS as shown in Figure 5-1 (which shows Switches 1, 2, and 3 are left in an indeterminate state).

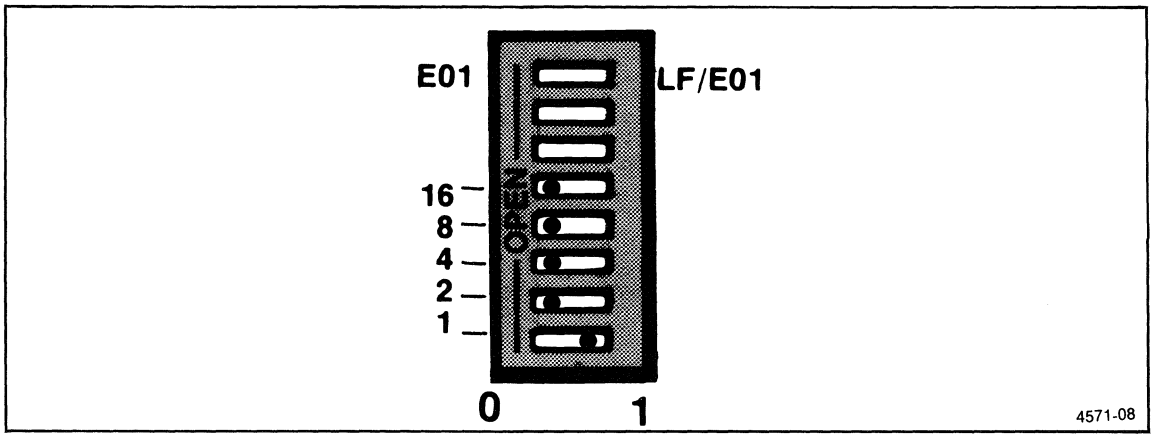


Figure 5-1. DAS rear panel GPIB address switch set to 1.

2. Remove any connectors attached to the GPIB or RS-232 ports on the back panel of the mainframe.
3. Turn on the mainframe.
4. Shortly after the power-up sequence is finished, the SRQ light on the back panel turns on.
5. Press the INPUT OUTPUT key to enter the Input Output menu.
6. The Input Output menu will display a message at the top that says GPIB TALK/LISTEN ADDRESS: 1.
7. Change the setting of the DIP switch on the back panel of the DAS mainframe to Address 31 as shown in Figure 5-2.

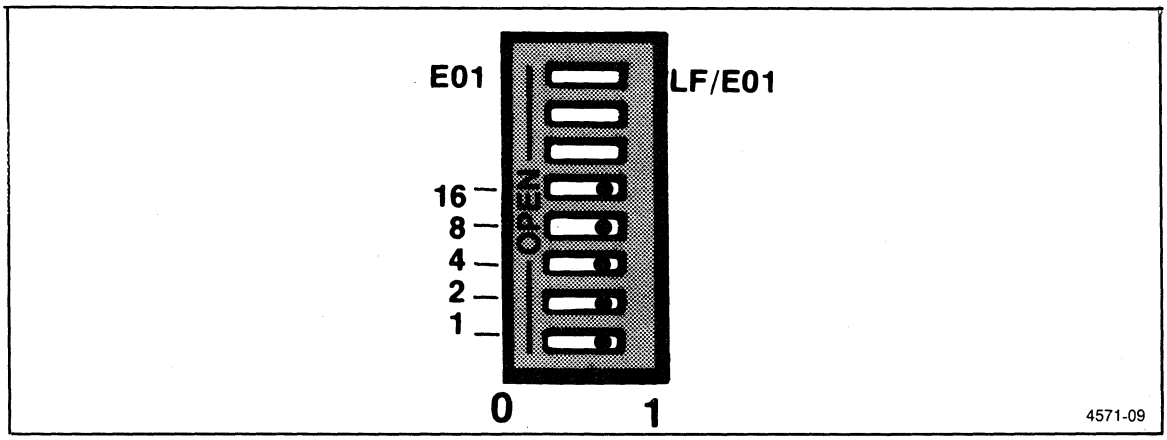


Figure 5-2. DAS rear panel GPIB Address Switch set to 31.

8. The message on the Input Output menu will change to GPIB OFFLINE and the SRQ light will go off.

NOTE

Part 2 of the I/O Communication Interface functional check requires a controller (Tektronix 4050 Desktop computer series or equivalent). A Tektronix 4051 with the Data Communications Interface (Option 01) is used to perform the following tests.

FUNCTIONAL CHECK, PART 2

GPIB and RS-232 Verification

1. Turn off the DAS. Do not turn on any of the other instruments yet.
2. The 4051 Option 01 has two possible output configurations: that of a terminal or that of a modem. The standard output of the 4051 a modem. If you are using the standard output of the 4051, then construct the null modem shown in Figure 5-3.

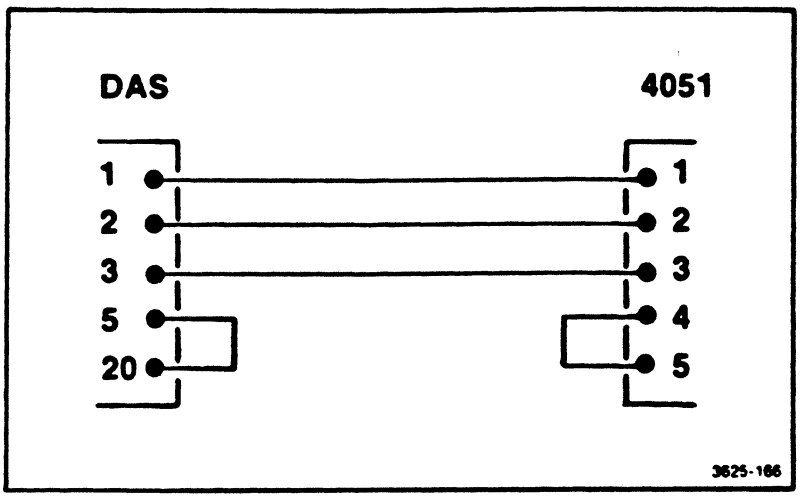


Figure 5-3. Null modem circuit for modem output configuration for a 4051, Option 01.

The 4051 Option 01 has an interconnect cable as an accessory that makes the output of the 4051 Option 01 look like a terminal. If this cable is used in the test set up, construct the null modem shown in Figure 5-4.

3. Attach the null modem to one end of the RS-232 cable. Connect the RS-232 cable with the null modem between the DAS RS-232 port and the 4051 RS-232 port.
4. Connect the GPIB cable between the DAS GPIB port and the 4051 GPIB port.
5. Set the GPIB address on the back of the DAS to 01, as shown in Figure 5-1.
6. Turn on the 4051.
7. Load the program given in Table 5-1 into the 4051.
8. Run the program just loaded into the 4051.

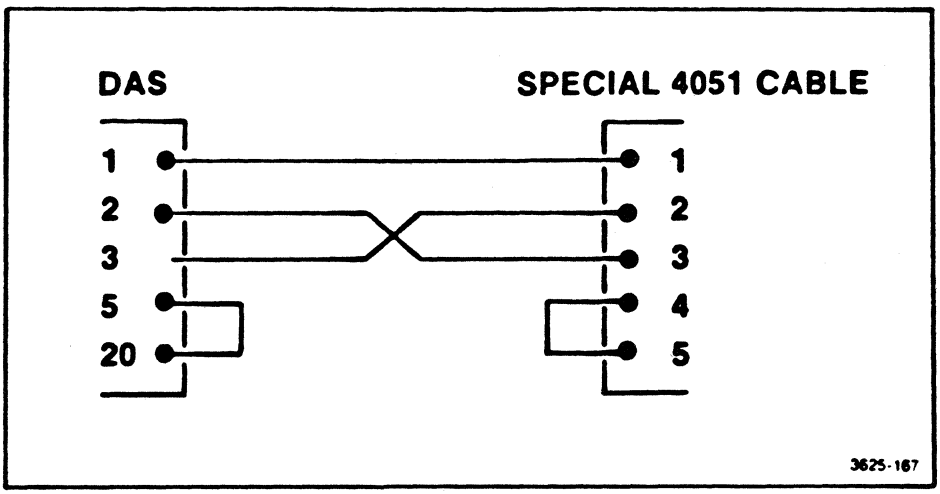


Figure 5-4. Null modem circuit for terminal output configuration of a 4051, Option 01.

9. Enter 1, followed by a carriage return on the 4051 keyboard, for the address of the DAS.
10. Turn on the DAS and wait for the 4051 to indicate Power-On.
11. On the 4051, press user-defined key number 1. This initiates the GPIB test.
12. While the test is running, examine the four LEDs on the back of the DAS. All of the LEDs should flash independently. Some of the LEDs are brighter than others.

The GPIB test may be restarted as desired by pressing user-defined key number 1 again.

The GPIB port on the DAS has now been verified as operational. The next steps verify the operation of the RS-232 port.

13. On the 4051, press user-defined key number 2. This initiates the RS-232 test.
14. Set the GPIB address on the back of the DAS to 31 (off line), as shown in Figure 5-2.
15. Press the INPUT OUTPUT key on the DAS to enter the Input Output menu. The message at the top of the menu will read GPIB OFFLINE.
16. Set the DEVICE field to RS-232. Set the BAUD RATE field to 2400.
17. The DAS is now ready for the test. Press RETURN (carriage return) on the 4051.
18. Watch the DAS screen carefully. The screen will change to the power-up display. The screen will then become blank and flash the message RS-232 IS ON THE AIR. The message has a very short duration. The DAS screen will then return to its original state.
19. Watch the DAS screen carefully for the message. The RS-232 test can be performed again by pressing the user-defined key number 2 followed by a carriage return on the 4051.

This test is completed. The test setup may now be dismantled.

Table 5-1 lists the program used to test the GPIB and RS-232 interfaces of the Option 06 I/O Communication Interface.

NOTE

This BASIC program is written for Tektronix 4050 series graphic computing systems only. The program must be run on a Tektronix computer to avoid incompatabilities with other versions of BASIC. If you have a different controller, you will have to develop a program for it which is the equivalent of the one provided.

After loading the test program into the 4051, save the program on a 4051 tape. This eliminates having to enter the program a second time should this test need to be performed again.

Table 5-1
GPIB AND RS-232 TEST PROGRAM

```
  1  ON SRQ THEN 3000
  2  GO TO 99
  4  GO TO 1000
  8  GO TO 2000
 12  GO TO 1000
 99  PAGE
100  PRINT "DAS9100 RS-232/GPIB CHECKOUT PROGRAM V1.0"
110  PRINT "****************************************"
120  PRINT
130  PRINT "USE USER DEFINED KEYS TO INITIATE TESTS"
140  PRINT "--------------------------------------"
150  PRINT
160  PRINT "UDK #1 - GPIB/LED CHECKOUT SEQUENCE"
170  PRINT "UDK #2 - RS-232 CHECKOUT SEQUENCE"
190  PRINT
210  PRINT
220  PRINT "ENTER ADDRESS FOR DAS: ";
230  INPUT D1
240  PRINT
250  PRINT "PLEASE TURN ON DAS"
260  WAIT
270  END
990  REM ***** CHECKOUT IEEE 488 INTERFACE *****
1000 ON SRQ THEN 2280
1005 PAGE
1010 PRINT "DAS GPIB LIGHT TEST"
1011 PRINT "** IF BUS HANGS, THEN FAILURE SHOULD BE ASSUMED **"
1020 WBYTE @17:
1030 FOR I=1 TO 72
1040 WBYTE @D1+32:-255
1050 WBYTE @D1+64:
1060 RBYTE X
1062 X=ABS(X)
1065 IF X<>255 THEN 1140
1070 PRINT ". ";
1080 FOR J=1 TO 50
```

Table 5-1 (Cont.)
GPIB AND RS-232 TEST PROGRAM

```
1090    NEXT J
1100    NEXT I
1110    PRINT
1120    PRINT "TEST COMPLETED"
1130    END
1140    PRINT
1150    PRINT "FAILURE - DATA LINES NOT CORRECT"
1160    PRINT "DATA BUS SHOULD BE: 255 INSTEAD OF: ";X
1990    REM ***** CHECKOUT THE RS-232 INTERFACE *****
2000    PAGE
2005    PRINT "RS-232 CHECKOUT SEQUENCE"
2010    PRINT
2020    PRINT "MAKE SURE ADDRESS SWITCHES ON BACK OF THE DAS ARE"
2030    PRINT "SET TO ADDRESS 31 (GPIB OFFLINE) AND THE BAUD RATE"
2040    PRINT "OF THE DAS IS SET TO 2400"
2050    PRINT
2060    PRINT "PRESS <CR> WHEN READY"
2070    INPUT A$
2080    PRINT
2090    CALL "RATE",2400,5,2
2100    CALL "PRLIST"
2110    PRINT @40:"LOCKOUT ON"
2120    PRINT @40:"DEFAULT;ERASE 0,24"
2130    PRINT @40:"MESSAGE 2,20,20,'RS-232 IS ON THE AIR'"
2140    PRINT @40:"SCREEN?"
2150    INPUT @40:A$
2160    A$=SEG(A$,POS(A$,"S",1),10)
2170    IF A$<>"SCREEN ON;" THEN 2260
2180    PRINT @40:"LOCKOUT?"
2190    INPUT @40:A$
2195    A$=SEG(A$,POS(A$,"L",1),11)
2200    IF A$<>"LOCKOUT ON;"THEN 2260
2210    PRINT @40:"LOCKOUT OFF;DEFAULT"
2220    PRINT
2230    PRINT "TEST COMPLETE"
2250    END
2260    PRINT "COMMUNICATIONS ERROR"
2270    END
2280    POLL A,B;D1
2290    RETURN
3000    POLL A,B;D1
3010    POLL A1,B1;D1
3020    IF B1=B THEN 3240
3030    IF B<>65 THEN 3060
3040    PRINT "POWER-ON"
3050    GO TO 3220
3060    IF B<>97 THEN 3090
```

Table 5-1 (Cont.)
GPIB AND RS-232 TEST PROGRAM

```
3070    PRINT "COMMAND ERROR"
3080    GO TO 3190
3090    IF B<>98 THEN 3120
3100    PRINT "EXECUTION ERROR"
3110    GO TO 3190
3120    IF B<>99 THEN 3150
3130    PRINT "SYSTEMS ERROR"
3140    GO TO 3190
3150    IF B<>101 THEN 3180
3160    PRINT "POD CHECK"
3170    GO TO 3220
3180    PRINT "SRQ: ";B;
3190    RETURN
3200    INPUT @D1:E$
3210    PRINT " ";A$
3220    ON SRQ THEN 3000
3230    RETURN
3240    PRINT "INTERRUPT FAILURE"
3250    PRINT "CHECK GPIB INTERRUPT PATH"
3260    PRINT "CHECK INTERRUPT MUX IN #4"
```

FUNCTIONAL CHECK, PART 3

Smart Port Controller Verification

This functional check requires a DAS 91A32 Data Acquisition Module in slot 2.

1. Turn off the DAS. Do not turn on any of the other instruments yet.
2. Connect the GPIB cable between the DAS GPIB port and the 4051 GPIB port.
3. Turn on the 4051.
4. Load the program given in Table 5-2 into the 4051.

NOTE

This BASIC program is written for Tektronix 4050 series graphic computing systems only. The program must be run on a Tektronix computer to avoid incompatabilities with other versions of BASIC. If you have a different controller, you will have to develop a program for it which is the equivalent of the one provided.

Table 5-2
SPC TEST PROGRAM

```
 10  ON SRQ THEN 220
 20  REM If transfer hangs up, the Data Acquisition Module may not be in the slot
 30  REM specified in the HSACQ command; DCL (Device Clear) aborts the DAS
 40  REM transfer. To send DCL command type WBYTE @ 20:
 50  PRINT "enter address for DAS:"
 60  INPUT D1
 70  PRINT @D1: "HSSTART SYS"
 80  REM ask for acquisition of 91A32 in slot 2
 90  PRINT @D1: "HSACQ? 2"
100  REM read all four pods, one sequence at a time
110  WBYTE @D1+64:
120  REM
125  FOR I=1 TO 4*512
130  RBYTE Z
140  PRINT Z;
150  REM if acqmen not full, all 512 seqs will not be transfered
160  IF Z<0 THEN 180
170  NEXT I
180  PRINT "DONE"
190  REM clear the OPERATION COMPLETE srq so SRQ msg is not displayed
200  POLL A,B; D1
210  END
220  REM You do not want to poll during transfer or when handshake is stopped
230  RETURN
```

5. Set the GPIB address on the back of the DAS to 01, as shown in Figure 5-1.
6. Turn on the DAS and wait for the 4051 to indicate Power-On.
7. Run the program just loaded into the 4051 by entering run followed by a carriage return. This initiates the GPIB test.

The DAS screen will go blank and the 4051 screen will display the contents of the acquisition RAM on the 91A32. When the 4051 screen is full, press the HOME PAGE key to allow the test to continue. When the test is complete, the 4051 will display a DONE message. The DAS will display PRESS MENU KEY TO EXIT.

The GPIB test may be restarted as desired by repeating step 7.

The high speed GPIB port using the SPC has now been verified as operational.

This completes the functional test of the DAS I/O comunication interface. The test setup may now be dismantled.

PERFORMANCE CHECK PROCEDURES

There is no performance check procedure for the Option 06 I/O Communication Interface. The functional check is sufficient to verify the operation of the I/O Communication Interface.

ADJUSTMENT PROCEDURES

There is no adjustment procedure for the Option 06 I/O Communication Interface.

MAINTENANCE: GENERAL INFORMATION

Tektronix maintains repair and recalibration facilities at its local Field Service Centers and the Factory Service Center. For further information or assistance, contact your local Tektronix Field Office or representative.

MAINTENANCE PRECAUTIONS

SOLDERING

Most of the components in the instrument are soldered in place. If it is necessary to replace a soldered part, use a 15 W soldering iron to prevent heat damage to the circuit board or components. Excessive heat will lift circuit runs on the circuit board.

The flux in the solder may leave a residue on the circuit board that can provide a high resistance leakage path and affect instrument operation. Be sure to clean off this residue. Isopropyl alcohol may be used.

LIGHT-EMITTING DIODES (LEDS)

To avoid damage to the LEDs, always keep soldering time and temperature to a minimum. Do not bend the leads or apply force when inserting the leads into circuit board holes. Clean the circuit board holes of all excess solder before attempting to install a new LED.

NOTE

Damage to the LEDs may not be immediately apparent. Always follow the precautionary measures listed above when handling the LEDs.

STATIC PRECAUTIONS

CAUTION

Static discharge can damage any semiconductor in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 6-1 for the relative susceptibility of various classes of semiconductors. Static voltages of 1—30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive components or assemblies.
3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies should be performed only in a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.
7. Do not slide the components over any surface.
8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only special anti-static suction type or wick type desoldering tools.

NOTE

Damage to electrical components may not be immediately apparent. Always follow the precautionary measures listed above when handling static-sensitive components.

Table 6-1
RELATIVE SUSCEPTIBILITY OF SEMICONDUCTORS TO STATIC DISCHARGE DAMAGE

Semiconductor Class	Danger Voltage[a]
MOS or CMOS	100 - 500 V
ECL	200 - 500 V
Schottky signal diodes	250 V
Schottky TTL	500 V
High-frequency bipolar transistors	400 - 600 V
JFETs	600 - 800 V
Linear microcircuits	400 - 1000 V
Low-power Schottky TTL	1200 V

[a]Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.

TEST EQUIPMENT REQUIRED FOR MAINTENANCE

Test equipment required to service the instrument is listed under *Troubleshooting Equipment* in the *Maintenance: Troubleshooting* section of this manual.

TOOLS REQUIRED FOR MAINTENANCE

The following tools are those most often needed when servicing the instrument:

Tool	Tektronix Part No.
1. Soldering iron, (15 W)	
2. Rosin core solder, 60/40	
3. Isopropyl alcohol	
4. Lint-free dust cloth	
5. Soft-bristle brush	
6. IC extractor	
7. Desolder tool	
8. Solder wick	
9. Magnetic screwdrivers, 7 inch shank and 4 inch shank	
10. POZIDRIV-type magnetic bits, 2 inch and 1 inch	
11. TORX-type magnetic bit, size T-20	003-0866-00
12. Angled tweezers, 6 inch	
13. Long-nose pliers	
14. 1/4 inch combination open/box wrench	
15. Plastic alignment tool, 5 inch	
16. Fiber adjustment tool, 9 inch	
17. Open-end wrench, 7/16 inch	
18. Allen wrenches, 0.050 inch, 1/16 inch and 5/64 inch	
19. Circuit board ejector	214-3154-00

DISASSEMBLY/INSTALLATION PROCEDURES

WARNING

Dangerous electric-shock hazards inside the mainframe may be exposed when the covers are removed. Be sure power is off and the power cord is disconnected before removing the covers. After the covers are removed, wait five minutes AFTER the warning lamp on the capacitor bracket board stops flashing before proceeding. Disassembly procedures should only be attempted by qualified service personnel.

Reassembly procedures are the reverse of the disassembly procedures in most cases. Separate reassembly instructions are provided only when necessary.

Unless otherwise noted, screws mentioned in the text are the pan-head, POZIDRIV type. Size specifications are provided for most screws.

In the following procedures, directional terms (top, bottom, left, right, etc.) are based on the assumption that the DAS is in a normal, upright position and the user is facing the front of the instrument.

GENERAL DISASSEMBLY PRECAUTIONS

CAUTION

DO NOT attempt any disassembly or installation procedures if power is on.

DO NOT disconnect connectors from the back of the mainframe by pulling on the cables; pull only on the connectors.

DO NOT remove connectors between circuit boards by pulling on the wires; pull only on the connectors.

DO NOT press or pull on components when manipulating circuit boards.

GUARD against static discharge damage by following the precautions listed in Maintenance Precautions in this section.

REMOVING PANELS AND COVERS

Top Panel

Figure 6-1 illustrates how to remove the top panel and the module compartment cover.

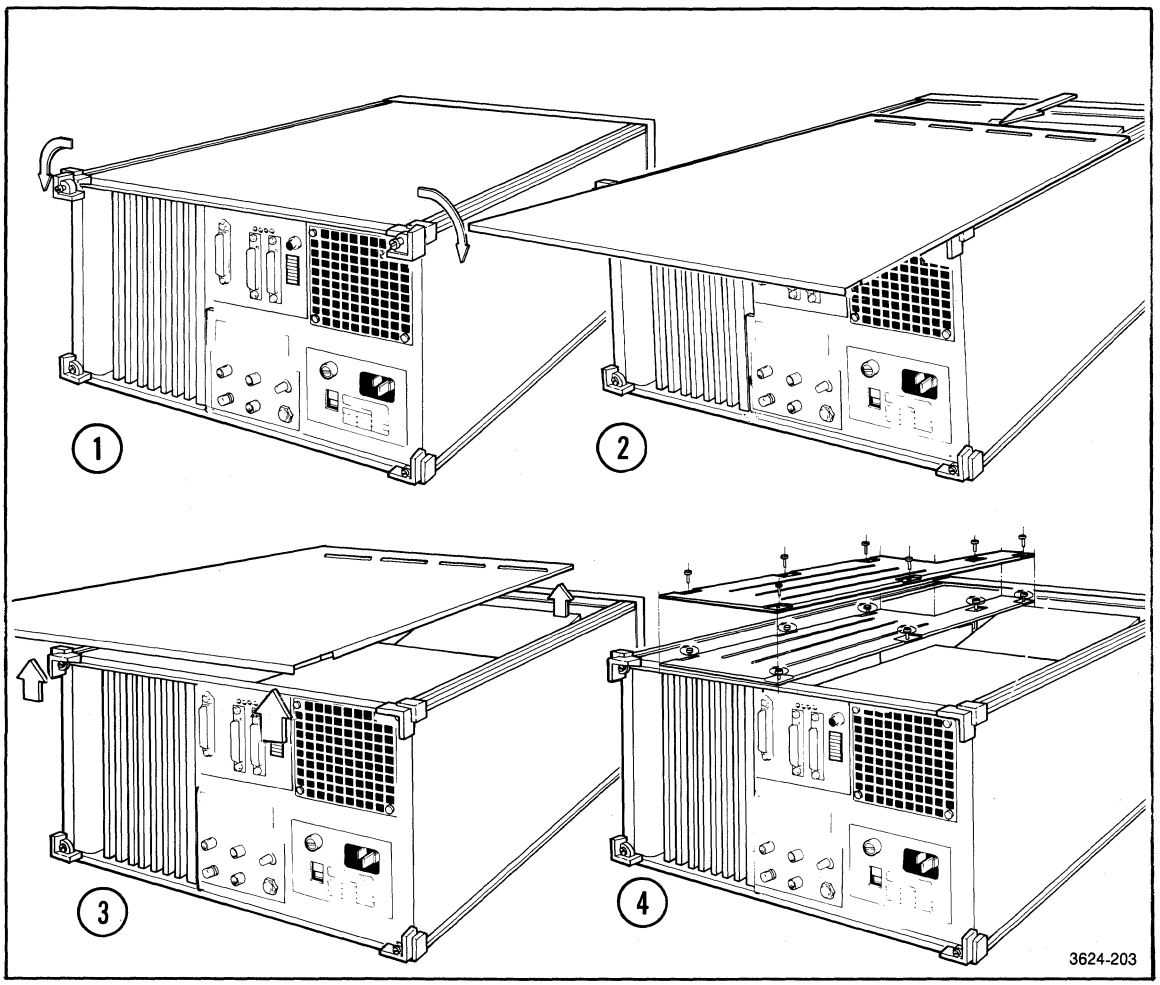


Figure 6-1. Top panel and module compartment cover removal.

1. Loosen the two large slotted screws in the upper corners of the back panel. Rotate the brackets behind these screws until they no longer block the edge of the top panel.
2. Press backward on the ridges at the front of the top panel. Simultaneously, pull on the rear edge until the front edge disengages.

3. Lift the panel up and off the mainframe.
4. Loosen the slotted-head screws that secure the module compartment cover until approximately 1/4 inch of each screw is exposed. Grasp the front edge of the cover and lift it off the mainframe.

INSTALLING/REMOVING INSTRUMENT MODULES

WARNING

Hazardous voltages may be exposed when the I/O panel and circuit board are installed. Be sure power is off and the power cord is disconnected. After power-down, wait five minutes AFTER the warning lamp on the capacitor bracket board stops flashing before starting this procedure. This will allow the filtering capacitors to discharge.

Module Installation

1. Position the module over the bus slot, with the ejector tab toward the front of the mainframe. Make sure this tab is parallel to the top of the module.
2. Insert the module between the guide slots at the top of the mainframe. This procedure is easiest if you align the module with the rear guide first.
3. Slide the module down through the slots until its connectors (P729 on the board) is resting on top of the bus slot connectors on the Interconnect board (J131 on the board).

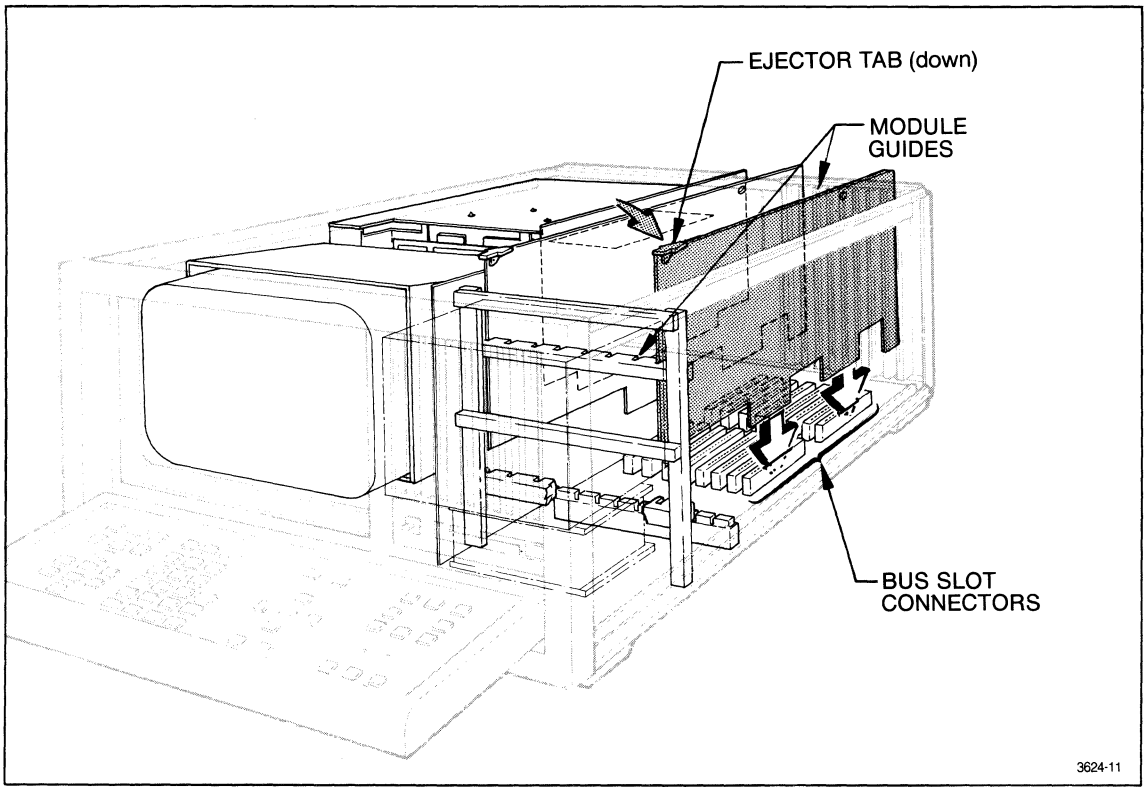


Figure 6-2. Installing an instrument module in the mainframe.

4. Push the module down into the bus slot connectors. Press firmly on the board, but do not press on components.

Module Removal

Figure 6-3 illustrates the procedure for removing a module from the mainframe.

CAUTION

Probes must be disconnected from the rear of the instrument modules before attempting to remove the modules. Failure to observe this precaution can damage connectors on probes and modules.

1. Disconnect and remove probes from the rear of the instrument modules.
2. Insert the circuit board ejector tool in the small hole located in the upper rear corner of the module, then brace it against the rear edge of the mainframe.
3. Use the ejector tool to pry up the back end of the module. Simultaneously, pull up on the inside edge of the module's ejector tab. You will feel the module disengage from the bus slot connectors.
4. Grasp the top of the module and pull it straight up. Do not pull on components.

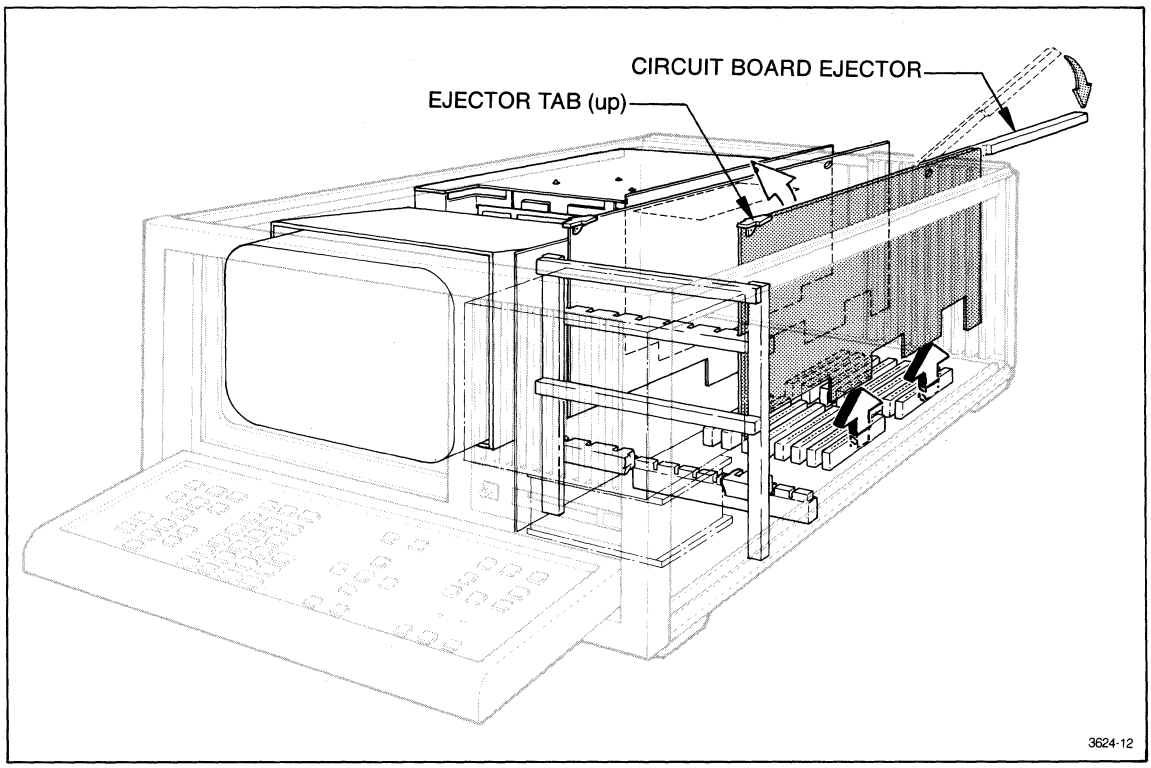


Figure 6-3. Removing an instrument module from the mainframe.

Installing the Option 06 I/O Communication Interface

The Option 06 I/O Communication Interface consists of a plug-in circuit board (the I/O Interface Communication Interface board) for insertion into slot 8; and a back panel insert (the I/O Connection panel) with appropriate connectors and plugs. Refer to Figure 6-4.

1. Unplug the mainframe from the power source.
2. Remove the top panel, the module compartment cover, and the power supply compartment cover. Wait five minutes AFTER the warning lamp on the capacitor bracket board stops flashing before proceeding to the next step.
3. Remove the plastic cover over the capacitors, if necessary.
4. Unplug the cable connecting the I/O Communication interface board to the I/O Connector Panel.
5. Remove the board currently installed in slot 8, if one is installed.
6. Remove the four screws (6-32 x 0.250) in the blank section of the back panel immediately to the left of the power supply fan cover, and remove the blank panel.
7. Install the I/0 Connector panel using the screws removed from the blank panel. If your mainframe is a Monochrome Mainframe, 9101-9104 (serial number B019999 or below) line the lower inside edge of the hole to protect the bottom of the I/O Connector panel as it is installed.
8. Position the ribbon cable as shown in Figure 6-4.

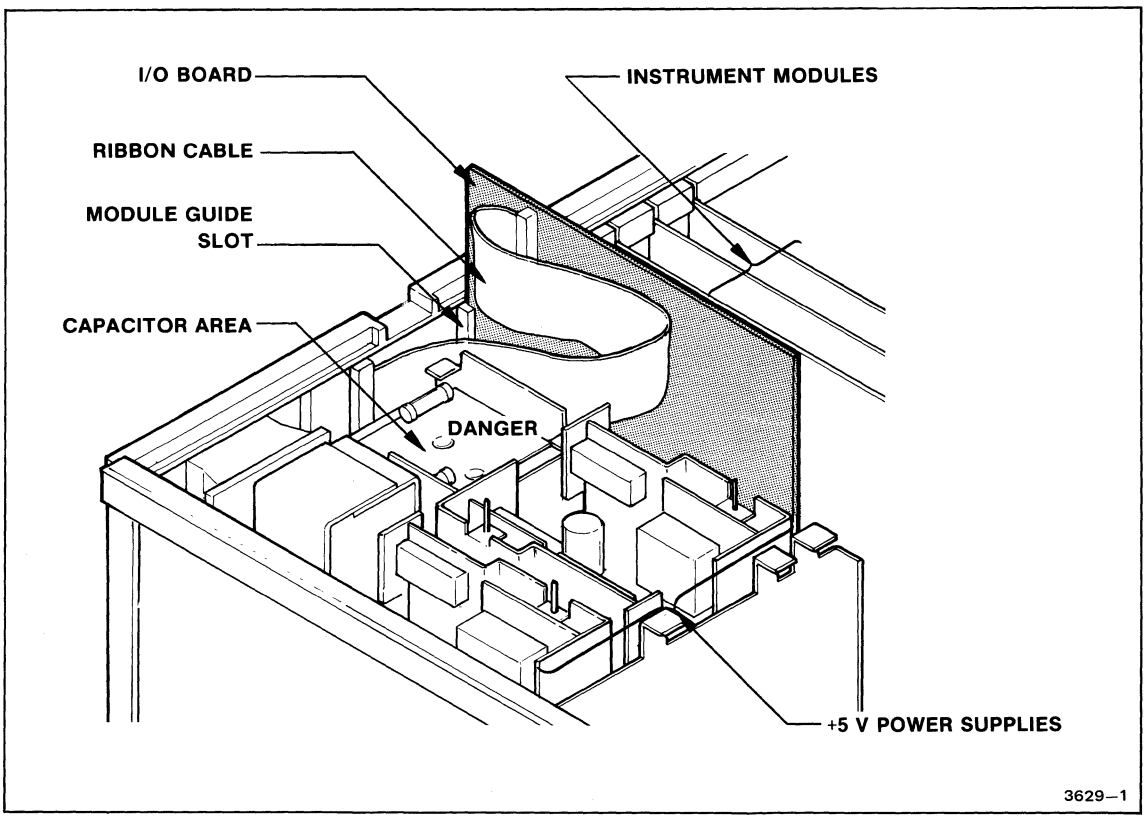


Figure 6-4. Installing the I/O Communication Interface board.

9. Insert the I/O Interface board in the guide slots. Lower the board until the ribbon cable connector can be attached to J110. If needed, adjust the distance between the guide slots to fit the board by loosening the twelve screws on the Power Supply Frame. Move the bracket until the board slides in guide slots
10. Attach the connector to J110. Be sure to align the pins properly; pin 1 is marked on the board, and is identified on the plug.
11. Slide the circuit board down the guide slots until its connectors (P729 on the board) rest on top of the bus slot connectors (J131).
12. Press the board down evenly and firmly. Do not press on components.

Removing the I/O Communication Interface Board

Figure 6-5 illustrates the procedure for removing the I/O Interface board.

1. Unplug the unit.
2. Remove the top panel, the module compartment cover, and the power supply compartment cover. Wait five minutes AFTER the warning lamp on the capacitor bracket board stops flashing before proceeding to the next step.
3. Insert the end of the circuit board ejector tool in the small hole in the upper rear corner of the circuit board in slot 8.
4. Brace the ejector tool against the back edge of the mainframe, then pry up the back end of the circuit board.

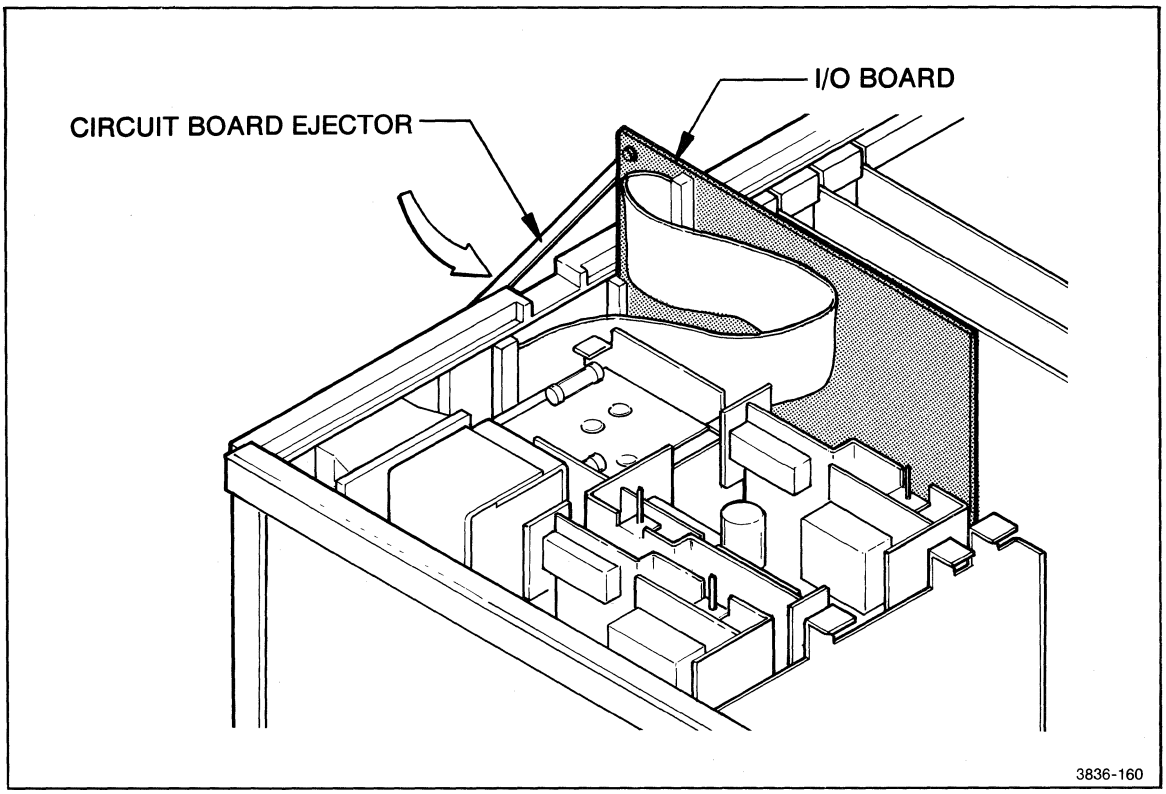


Figure 6-5. Removing the I/O Communication Interface board.

5. Grasp the top of the board and lift straight up a few inches until the ribbon cable connector is accessible. Do not pull on components.
6. Disconnect the ribbon cable from the circuit board.
7. Pull the board out of the mainframe.

Removing the I/O Connector Panel

1. Remove the four screws (6-32 x 0.250) securing the I/O connector panel to the mainframe rear casting.
2. Disconnect the ribbon cable from the I/O Communication Interface board.
3. Pull the I/O Connector panel out, taking care not to damage the ribbon cable.

INTERIOR CLEANING

WARNING

Hazardous voltages may be exposed during interior cleaning of the DAS. Be sure power is off and the power cord is disconnected. After power-down, wait five minutes AFTER the warning lamp on the capacitor bracket board stops flashing before starting this procedure. This will allow the filtering capacitors to discharge.

Internal cleaning should be done with a dry, low-velocity stream of air. A soft bristle brush is useful for cleaning around components. If a liquid must be used for minor internal cleaning, use isopropyl alcohol.

Should the interior of the instrument be so dirty as to require a thorough cleaning, it can be washed according to the wash procedure below.

CAUTION

DO NOT wash the power switch. The power switch must be covered during washing procedures.

When washing near unsealed electromechanical components like the keyboard keys and the tape drive sensing switches, use as little washing action as possible. This is to prevent washing the lubricant out of the switches and getting an excess of detergent into the contact areas of the switches.

DO NOT use a freon-based cleaner for cleaning the circuit boards. Freon will destroy aluminum capacitors.

DO NOT use fluorocarbon-base, spray cleaners or silicon spray lubricants on switches or switch contacts. These sprays may damage the circuit board material or plastic parts, and leave a dust-collecting residue. If necessary, New improved NO NOISE may be used as a lubricant.

1. Disassemble the instrument to the point that all areas requiring washing are easily accessible. The amount of disassembly required will vary according to the instrument configuration and the options installed. During disassembly, refer to the *Disassembly/Installation Procedures* described earlier in this section.
2. Cover the main power switch in the front of the mainframe to prevent detergent from getting inside.
3. Spray-wash components with a 5% solution of mild detergent and water. (Kelite, or equivalent, is a usable mild detergent).

NOTE

After performing the previous steps, be sure to perform the following procedure on the bus connectors on the interconnect board and on the connectors on the instrument modules, power supplies, and options.

4. Thoroughly rinse components with clean water.
5. Blow-dry components with low velocity air.
6. Spray all switch contact areas and connectors with isopropyl alcohol, wait 60 seconds, then blow dry with low velocity air.
7. Heat all components in an oven or compartment using circulating air at +51 to +65°C (+125 to +150°F).
8. If necessary, the contact areas of push switches can be lubricated with New Improved NO NOISE.

INSPECTION

Inspect the instrument for broken connections, frayed wires, poorly seated components, leaking capacitors, damaged hardware, and heat damaged components.

Repair any obvious problems. However, take particular care if you find any heat damaged parts. Overheating usually indicates other circuit problems. To prevent a recurrence of the damage, find and correct the cause of the overheating (see the *Maintenance: Troubleshooting* section).

POWER-UP SELF TEST

The power-up self-test can indicate when maintenance is required. If any of the power-up diagnostics are not passed when the instrument is turned on, maintenance is required. Additional in-depth diagnostic routines are discussed in the *Troubleshooting* and the *Diagnostic Test Description* sections.

CORRECTIVE MAINTENANCE

OBTAINING REPLACEMENT PARTS

All electrical and mechanical replaceable parts for the instrument can be obtained through your Tektronix Field Office or representative. However, many of the standard electrical components can be obtained locally. Before purchacing an ordinary part, check the Replaceable Parts list for value, tolerance, rating, and description.

CAUTION

Check the parts list before replacing electrical components. If the part is called out as screened or burned-in, the replacement part must also be screened or burned-in or the repair may not be effective.

NOTE

When selecting replacement parts, remember that the physical size and shape of a component may affect its performance in the instrument. All replaceable parts should be direct replacements unless it is known that a different component will not adversely affect instrument performance.

Most of the mechanical parts and some of the electrical parts in this instrument are manufactured by Tektronix. Some parts are manufactured or selected by Tektronix to satisfy particular requirements, or are manufactured to certain specifications for Tektronix. To determine the manufacturer of a part, refer to the Parts List Cross Index of Code Number to Manufacturer. This is found in the Replaceable Parts list.

When ordering replacement parts from Tektronix, include the following information:

1. Instrument type
2. Instrument serial number
3. A description of the part (if electrical, include the component number)
4. Tektronix part number

MAINTENANCE: TROUBLESHOOTING

The Option 06 I/O Communication Interface consists of five major parts:

- Communication interface to the DAS—If the communication interface to the DAS is nonfunctioning, it causes some problems that are difficult to work around. Troubleshoot these problems first.
- RS-232 Interfaces—The RS-232 interfaces are the least complicated of the two remaining interfaces. Troubleshoot the RS-232 interfaces next.
- GPIB Interface—The GPIB interface is the last part of the Option 06 I/O Communification Interface to troubleshoot.
- Composite Video Output—The composite video output involves very few components, so no troubleshooting procedures are included here. Since the composite video output doesn't interact with any other circuits on the I/O interface, you can troubleshoot it at any point.
- Color Video Signals—Four TTL level signals have been added for color video: /VERTICAL SYNC (L), /HORIZONTAL SYNC (L), GREEN, and RED. A ground reference is also provided. These signals appear on 5 square pins located at the back of the I/O Communication Interface board (located in slot 8).

INTRODUCTION

When troubleshooting the DAS, you should run the internal diagnostics first. If you are not familiar with DAS diagnostic capabilities, you should read the description of the DAS Diagnostics in Section 8, *Maintenance: Diagnostic Test Descriptions* of the *DAS 9100 Series Service Manual*.

Enter the Diagnostics menu and turn on LOOPING in the menu. Then run the diagnostics on the suspect module. Loop on all of the tests in each function. Stop when you reach the first function failure. Note the failed function name and test number. Then look up the failed function and test number in this section.

Some failures are not captured by the diagnostics. If a module is not functioning but the diagnostics all pass, see *Troubleshooting* in this section for further information.

There are two sets of diagnostics: Powerup and Diagnostic Menu. The Powerup Diagnostics run automatically. The Diagnostic Menu Diagnostics can be entered by pressing the DAS START SYSTEM key.

DIAGNOSTICS

POWERUP DIAGNOSTICS

During the DAS power-up, a checksum is performed on the ROMs located on the Option 06 I/O Communication Interface board. If the checksum is correct, two additional functional tests are performed on the circuit board: a Baud Rate Multiplexer test and a Smart Port Controller (SPC) test.

The Baud Rate Multiplexer functional test consists of two sub-tests.

- Printer Port Baud Rate Multiplexer test
- Master/Slave Port Baud Rate Multiplexer test

The SPC functional test consists of three sub-tests.

- Data Register Test (outputs 55*hex*)
- Data Register Test (outputs AA*hex*)
- Loop Counter test

DIAGNOSTIC MENU DIAGNOSTICS

By pressing the DAS START SYSTEM key, you enter a more extended set of diagnostic tests:

Function 0 - Baud Rate Multiplexer tests:	Test 0: Printer Port Baud Rate Multiplexer test Test 1: Master/Slave Port Baud Rate Multiplexer test
Function 1 - SPC tests:	Test 0: Data Register test (55*hex*) Test 1: Data Register test (AA*hex*) Test 2: Loop Counter Test Test 3: Back Panel Address Switch Buffer to the Printer Baud Rate Write Port Data Transfer Test
Function 2 - GPIB Tests:	Test 0: Reset test Test 1: Listener Mode test Test 2: Talker Mode test
Function 3 - RS-232 Tests:	Test 0: DSR test (requires RS-232 cable) Test 1: M/S to Printer Port transfer test (requires RS-232 cable) Test 2: Printer to M/S port transfer test (requires RS-232 cable)
Function 4 - Baud Rate tests:	Test 0: 300 Baud test (requires RS-232 cable) Test 1: 600 Baud test (requires RS-232 cable) Test 2: 1200 Baud test (requires RS-232 cable) Test 3: 2400 Baud test (requires RS-232 cable) Test 4: 4800 Baud test (requires RS-232 cable) Test 5: 9600 Baud test (requires RS-232 cable)
Function 5 ROM Part Numbers:	Test 0: List of ROM Part Numbers by slot number

INTERFACE PROBLEMS

Sometimes the diagnostics cannot function. This may be caused by the following problems:

PROBLEM:	**Blank screen.**
POSSIBLE CAUSE:	The DAS is not working.
ACTION:	If the DAS does not come up, remove all the DAS modules except the Controller and Trigger Modules. If the DAS still does not come up, refer to the *DAS 9100 Series Service Manual* to check the DAS kernal ROM. If the DAS does come up, reinstall the modules one at a time. Power up after each installation and check for a board failure.

CAUTION

Do not install the modules while the DAS is powered up. The modules will be damaged.

If the Option 06 I/O Communication Interface is causing the problem, it can cause the DAS controller to lose control of the system. The Option 06 takes the data bus away from the DAS controller and never releases it.

Check for the following signals at the indicated pin at P729: INT0 at pin B9, INT1 at pin A30, INT2 at pin B29. If any of the signals are stuck low, trace the signal back to the DAS.

Check the signal BREQ at pin A26 on connector P729. If the signal is low, trace the signal back through U545 and U440. If the signal is stuck high, Check for bad ROM, data buffer (U655) or address buffers (U565,and U570) on the I/O Communication Interface board.

PROBLEM: **SLOT 8 not listed in menu.**

POSSIBLE CAUSE: The DAS determines that an Option 06 I/O Interface board is present by checking the control register of the M/S RS-232 controller (U435). The DAS looks for any value except FF_{hex}. The FF_{hex} means there is no module in slot 8. If FF_{hex} is read back, the RS-232 controller does not receive a chip select signal.

ACTION: Check the chip select signal at pin 11 of U435 during power-up. If the chip select signal is present, check for LRD(L) at pin 13 of U435. In addition, check for data on the data buffer U655. Each line of the data buffer should toggle high and low.

PROBLEM: **SLOT 8 listed in menu but board cannot be accessed for diagnostics or normal operation.**

POSSIBLE CAUSE: The ROM on the I/O communication interface can not be accessed. The signals PORT8 (L) at pin 9 of U455, SEL SLOT(L) at pin 4 of U455, PERSONALITY(L) at pin 5 of U455, LOWR(L) at pin 5 of U640, or BRD(L) at pin 6 of U640, are missing. These signals are required to activate the chip select, mapping register clock, and output enable signals for the ROM.

ACTION: Verify that the signals SEL SLOT(L) at pin 4 of U455, PERSONALITY(L) at pin 5 of U455, and BRD(L) at pin 6 of U640 are all low during a ROM read. If all the signals are low, check the chip select signal from U355.

Verify that all three outputs of the Map Register (U345) are moving during power-up. If the outputs are not moving, Check for signals LWR(L) at pin 5 of U640 and PORT8(L) at pin 9 of U455 during power-up.

PROBLEM: **No PASS/FAIL information for SLOT 8 at power-up.**

POSSIBLE CAUSE: Same as above.

ACTION: Same as above.

PROBLEM: **FLASHING CHECKSUM MESSAGE**

POSSIBLE CAUSE: A ROM is bad.

ACTION: Replace the ROM indicated by the checksum. The message displayed for a ROM on the Option 06 Communication Interface board is CHECKSUM "8,N" where N equals any number between 0 and F.

N = 4 or 8 replace U240
N = 1 or 5 replace U250
N = 2 or 6 replace U260
N = 3 or 7 replace U270

DIAGNOSTIC TEST DESCRIPTION

The schematic diagrams in the *Diagrams* section have been color coded aid the user during the following Functions. See color legend on each schematic in the *Diagrams* section.

FUNCTION 0: BAUD RATE MULTIPLEXER TESTS

TEST 0: Printer Baud Rate Multiplexer Tests

These parts are found on schematic 90 unless otherwise specified.

This test checks the Printer Baud Rate Write port (U140A), the Baud Rate Read port (U645A), and the control circuits consisting of Port Address Selector (U560 on schematic 88), Clock Gate (U460D), and Enable Gate (U525A). The baud rate multiplexer commands 00_{hex}, 08_{hex}, 10_{hex}, and 18 (*hex*) are written into the Printer Baud Rate Write port (address F1 hex) and verified by reading them back through the Baud Rate Read port (address F1 *hex*).

ERROR: EXPECTED DATA 00_{hex}, 08_{hex}, 10_{hex} or 18_{hex}.
ACTUAL DATA: FF (*hex*).

POSSIBLE CAUSE: One of the five components (U140A, U460D, U525A, U560, or U645A) involved in test is not operating.

ACTION: Trigger on pin 13 of clock gate (U460D), and verify that the clock signals are present on the clock pin 9 of U140A, the output pins 10 and 15 of U140A and the enable pin 1 of U645A. If clock signals are present, replace U645. Otherwise replace U140 or U460. If the trigger signal on pin 13 of U460 is not present, replace Port Address Selector (U560 on schematic 88).

ERROR: EXPECTED DATA 00_{hex}, 08_{hex}, 10_{hex} OR 18_{hex}.
ACTUAL DATA: Any value other than FF_{hex} or the expected data

POSSIBLE CAUSE: One of the output lines of Write Port U140A or input lines of Read Port, U645A, is stuck at 0 or 1.

ACTION: Trigger on pin 13 of clock gate U460, and check these lines.

TEST 1: Master/Slave Baud Rate Multiplexer Test

These parts are found on schematic 90 unless otherwise specified.

This test checks the Master/Slave Baud Rate Write port, U340, the Baud Rate Read port U645A, and the control circuits consisting of Clock Gates U360, U365B, and U460A and Enable Gate U525A. The baud rate multiplexer commands 00_{hex}, 02_{hex}, 04_{hex}, and 06_{hex} are written into the Master/Slave Baud Rate Write port address $A0_{hex}$ and verified by reading them back through the Baud Rate Read port address $F1_{hex}$.

ERROR: EXPECTED DATA = 00_{hex}, 02_{hex}, 04_{hex} OR 06_{hex}
ACTUAL DATA = FF_{hex}

POSSIBLE CAUSE: One of the six components (U340, U360, U365B U460, U525A, and U645A) involved in the test is not operating.

ACTION: Loop on the test, then trigger on pin 6 of clock gate U365B, and verify that the enable pulse is present on the output pins 10 and 15 of U340 and the chip enable pin 1 of U645A. If the pulses are all present, replace U645, If a pulse is missing, replace U340. If the trigger signal on pin 6 of U365 is not present, then check the preceding NAND and AND gates for the logic to produce the enable pulse (U365 high, U360 low, and U460 high).

ERROR: EXPECTED DATA 00_{hex}, 08_{hex}, 10_{hex} or 18_{hex}
ACTUAL DATA: Any value other than FF_{hex} or the expected data

POSSIBLE CAUSE: One of the output lines of Write Port U140A, or input lines of Read Port U645A, is stuck at 0 or 1.

ACTION: Trigger on pin 6 of U365 and check these lines.

FUNCTION 1: SMART PORT CONTROLLER TESTS

NOTE

The Option 06 I/O Communication Interface requires the DAS Controller board 670-7475-03.

These Controller Modules are installed in DAS mainframes with serial numbers B040100 and above. The DAS Controller Module 670-7475-02 and below works on all diagnostic tests except Smart Port Controller Test 3.

TEST 0: Data Register Test (55_{hex})

These parts are found on schematic 89 unless otherwise specified.

This test loads a program into the SPC Program Memory RAM (U375) that outputs a 55_{hex} to the SPC Data Buffer (U665). After it is loaded, the SPC is given an execute command and bit 5 of the Address Switch buffer is monitored to determine when the program has finished executing. After it is finished, the Data Register (U665) is read back and checked for a value of 55_{hex}.

ERROR: EXPECTED DATA = 55*hex*
ACTUAL DATA = CC*hex*

POSIBLE CAUSE: Defective Address Switch buffer.

ACTION: The CC*hex* data indicates that the SPC execution in process bit went high but never went low. Loop on the test and, using a scope triggered from U315, output enable pin 1 or 15, verify that SPC input pin 12 and output pin 11 is low during output enable. If input is low, but the output is high replace U315 on schematic 88. If the input is high, the problem is in the SPC (see *Troubleshooting the SPC* at the end of this section).

ERROR: EXPECTED DATA = 55*hex*.
ACTUAL DATA = Any value other than 55*hex* or CC*hex*.

POSSIBLE CAUSE: SPC not operating or defective data register.

ACTION: Loop on the test. Verify that the SPC Data Register (U665) is receiving a clock pulse (pin 11) and a output enable pulse (pin 1). If there is no output enable pulse check the input of the OR gate (U555D pin 13). Replace U555 if pulse is present, otherwise replace Port Address Selector (U560 on schematic 88. If there is no clock pulse, the SPC is not operating (see *Troubleshooting the SPC* at the end of this section).

If both pulses are present, trigger on the clock pulse and check the inputs of U665 for 55 *hex* during the clock pulse period. If they are present replace the Data Register U665. Otherwise the SPC is not operating (see *Trouble Shooting the SPC* at the end of this section).

POSSIBLE CAUSE: Program not being loaded into Program Memory RAM (U375).

ACTION: Loop on the test and check for memory write enable pulses on pin 21 of U375. If the pulses are there, use a scope or logic analyzer to see if the following program is present on the input to the RAM during the time that the WRITE ENABLE signal is low.

1: 85*hex* Load Data Register
2: 55*hex* Data to be loaded
3: 04*hex* Jump-halt
4: 02*hex* Jump address (Jump-halt addr)

If the write enable pulses are not present, check gate U455D and Port Address Selector (U560)

If the above pattern is not present, check SPC Data Buffer U660 for an enable pulse and input data (85*hex*, 55*hex*, 04*hex*, 02*hex*). If the pattern is present, the problem is somewhere else in the SPC (see *Trouble Shooting the SPC* at the end of this section).

TEST 1: Data Register Test (AA*hex*)

(This test is the same as test 0 except it outputs a AA*hex* instead of a 55*hex*)

TEST 2: Loop Counter Test

These parts are found on schematic 89.

This test checks the ability of the Loop Counter (U675) to decrement six times and output a 66 (*hex*) to the SPC Data Register. The test pattern loaded into the Program Memory RAM follows the sequence described below. Even though the microinstructions say decrement, the counter is really an incrementing counter. Therefore, the count loaded must be the complement of the actual count desired. The carry out bit (CO) goes low when the counter reaches a count of FF*hex*.

byte 0: Load loop counter.
byte 1: Count to be loaded F9*hex* (which is complement of 06*hex*).
byte 2: Decrement & jump if not zero.
byte 3: Jump address (byte 8).
byte 4: Load data out register.
byte 5: Data to be loaded (11*hex*).
byte 6: Jump.
byte 7: Jump address (28*hex*) ;Error end test.
byte 8: Decrement & jump if not zero.
byte 9: Jump address (byte 0E*hex*).
byte A: Load data out register.
byte B: Data to be loaded (22*hex*).
byte C: Jump.
byte D: Jump address (28*hex*); Error end of test.
byte E: Decement jump if not zero.
byte F: Jump address (14*hex*).
byte 10: Load Data Register.
byte 11: Data to be loaded (33*hex*).
byte 12: Jump.
byte 13: Jump address 28*hex*; Error end of test.
byte 14: Decement jump if not zero.
byte 15: Jump address 1A*hex*.
byte 16: Load Data Register.
byte 17: Data to be loaded (44*hex*).
byte 18: Jump.
byte 19: Jump address 28*hex*.
byte 1A: Decement jump if not zero.
byte 1B: Jump address 20*hex*.
byte 1C: Load Data Register.
byte 1D: Data to be loaded (55*hex*).
byte 1E: Jump.
byte 1F: Jump address. 28*hex*.
byte 20: Decrement & jump if not zero; Count will be zero.
byte 21: Jump address (26*hex*).
byte 22: Load data register.
byte 23: Data to be loaded (66*hex*).
byte 24: Jump.
byte 25: Jump address (28*hex*).
byte 26: Load data register.
byte 27: Data to be loaded (BB*hex*); Error, did not decrement to zero.
byte 28: Jump & halt.
byte 29: Jump address (28*hex*); End of pattern.

ERROR: EXPECTED DATA = 66*hex*
ACTUAL DATA: 11*hex* through 55*hex*

POSSIBLE CAUSE: Defective Loop Counter (675), wrong count loaded into counter, defective counter control lines, or defective test condition multiplexer U445.

ACTION: Loop on the test and check control lines I0 and I1 and Carry Out (CO) of the loop counter pins 2, 11, and 14 of U675 for the timing diagram as shown in Figure 7-1.

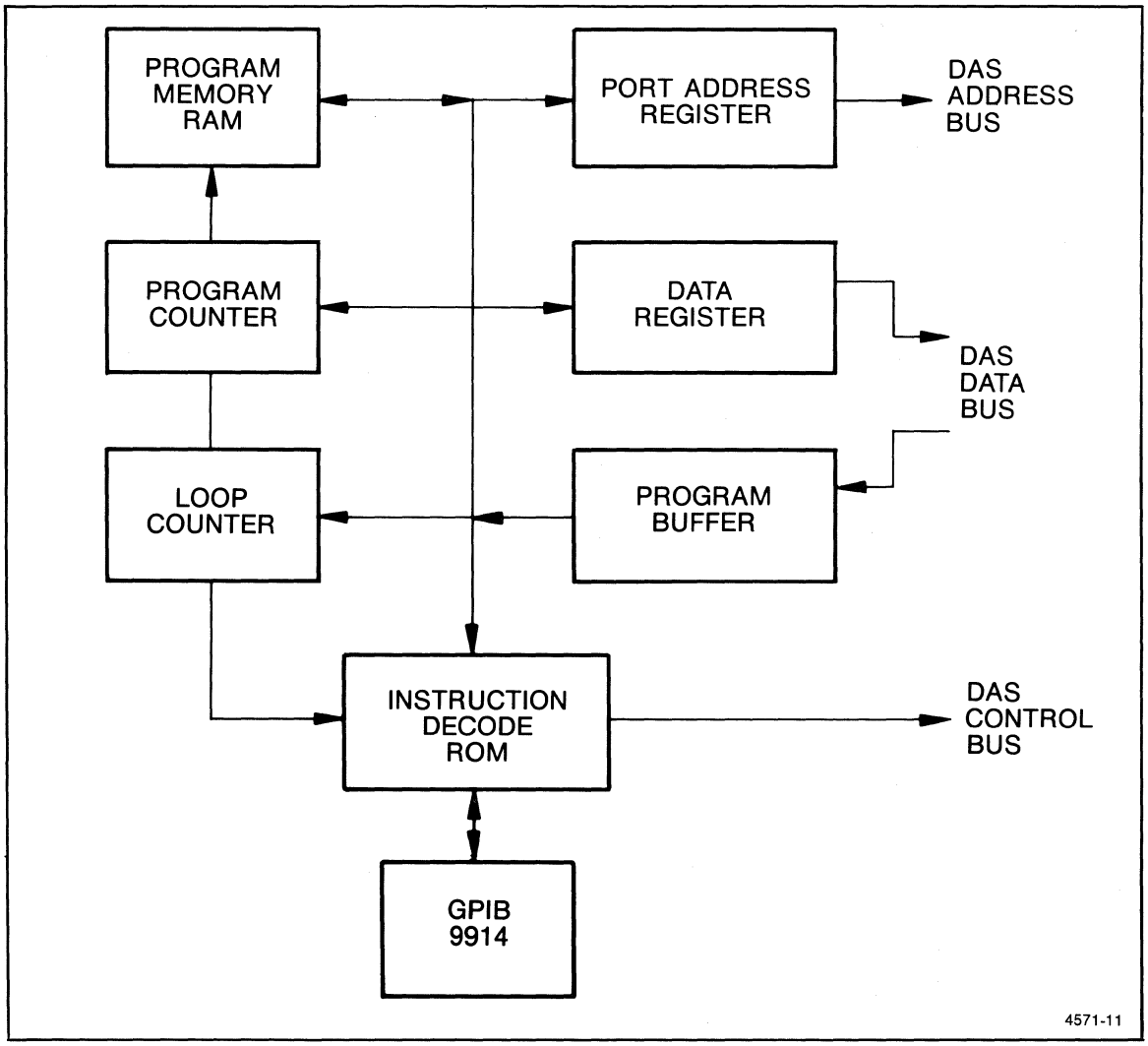


Figure 7-1. Control line timing diagram.

NOTE

If the signals in Figure 7-1 are present, check to see that the CO output is being transmitted through the test condition multiplexer *U445. If not, replace U445.*

If the control signals are present but there is no CO signal, check to see that a count of F9hex is on the counter input during the load command. If it is, replace the counter. If the control signals are wrong or not present, see the SPC Troubleshooting Procedure *at the end of this section.*

TEST 3: Back Panel Address Switch Buffer to the Printer Baud Rate Write Port Data Transfer Test

These parts are found on schematic 89.

This test checks the ability of the SPC to control the transfer of data from one port to another. Normally, this mode would be used to transfer data from the DAS to the GPIB port or from the GPIB port to the DAS. Since the DAS configuration to allow this transfer may not be present, the Back Panel Switch port on the Option 06 I/O Communication Interface board is used as the source and the Printer RS-232 Baud Rate Write port is used as the destination.

Since the Printer baud rate write port is programmed by bits 3 and 4, only these two bits can be read from from the Back Panel Address Switch. These two bits are the middle two bits on the address switch. The switches actual position (on or off) at the start of the test programs the Printer Baud Rate Write port.

In this test, the SPC takes control of the data bus from the DAS Controller board using the signals BREQ(L) and BACK(L). The SPC drives BRD(L) to read the back panel address switches. In addition, the SPC drives DIAG WR(L) to write the data from the back panel address switches into the printer baud rate write port.

ERROR: EXPECTED DATA = SWITCH BIT 3 AND 4
ACTUAL DATA = CC*hex*

POSSIBLE CAUSE: No bus request generated BREQ(L).

ACTION: Loop on the test with the display off and check to see that a BREQ(L) signal is present on pin 6 of U545C. You should see a 3 to 4 μs negative going pulse that occurs appoximately once every 350 ms. If it is not present, trace it back through U545C and U440A.

POSSIBLE CAUSE: Bus Acknowledge not getting through U630A.

ACTION: Loop on the test with display off and check for a Bus Trap Signal at pin 13 of U630A. This signal is a 2 to 3 μs negative going pulse occuring once every 350 ms. If a pulse is not present, check for a negative going pulse of approximately the same width and period on pin 1 and 14 of U630A.

NOTE

If the signals are present, on pins 1 and 14 of U630A, replace U630. If the signal is not getting to pin 14, trace the signal back through U540E and U370. If the BACK(L) signal is not getting to pin 1, then either the BREQ(L) signal is not getting to the DAS Controller Module or the BACK(L) signal is not getting from the DAS Controller board to the Option 06 I/O Communication Interface board. Check the DAS Controller Module for the signal.

ERROR: EXPECTED DATA = SWITCH BITS 3 AND 4
ACTUAL DATA = UNEXPECTED DATA OR CC (*hex*)

POSSIBLE CAUSE: SPC address out register, U670, not working.

ACTION: Loop on the test with display off and trigger on the SPC address out register (U670) enable pin 1. Verify that address F0 (hex) is present on the address out register output pins during the time of the enable pulse.

If F0*hex* is not present on the U670 output, check U670 for a F0*hex* at its input when its clock input at pin 11, goes high.

POSSIBLE CAUSE: Back panel address switch registers U215B or U315, not working.

ACTION: Place the DAS in normal operation and select the INPUT/OUTPUT menu. The switch address is displayed after the GPIB TALK/LISTEN ADDRESS:. Change the address switch setting and recall the INPUT/OUTPUT menu. Verify that the GPIB TALK/LISTEN ADDRESS has changed to the new switch setting. If it does not, monitor the inputs to the switch registers, U215B and U315 while changing the switch settings. If the inputs do not change, replace the switch. Otherwise replace the related switch registers U215B or U315.

POSSIBLE CAUSE: Read/Write SPC control buffer U645 not working.

ACTION: Loop on the test with display off. Trigger on U645 enable pin 19. Verify that BRD, pin 5, goes low during the time of the low on the enable pin. The enable pulse is a 2-3 μs negative-going pulse with a period of about 350 ms. Check the other output pins on U645 for correct levels (pin 9 high, pin 7 low, and pin 3 high).

Troubleshooting the Smart Port Controller

Before using an Oscilloscope or logic analyzer to test the SPC, analyze the problem based on the results of the SPC diagnostic tests.

If the DAS makes it through the power-up sequence and displays the diagnostic menu for slot 8, it can be assumed that the address buffers, the data bus transceiver and the bus control circuits are working. You know this because the power-up sequence does a checksum on the ROMs in the Option 06 communication interface. If the diagnostic tests for slot 8 are displayed in the DAS Diagnostic menu, part of the ROM in the communication interface is working.

The power-up sequence also executes the Baud Rate Multiplexer test which checks the baud rate write and read back ports. These ports are used as the destination in SPC test 3, which tests the ability of the SPC to perform a DAS bus data transfer from the GPIB back panel switch address register to the baud rate write ports. Therefore, if all the tests pass during power up except the SPC test, the problem is in the SPC circuitry. Table 7-1 lists the the circuit components found in the SPC and describes their function.

SPC Tests 0 and 1 are the simplest of the four tests and involve the fewest number of components. If these two tests pass, but one of the other two fail, the problem is in one of the circuit components checked by SPC tests 2 and 3.

SPC Test 2 requires the proper operation of all the components checked in tests 0 and 1 plus the loop counter,U675, and the NOR gate U530, pins 8,9, and 10. If this is the only test failing refer to the *SPC Test 2* in this section.

SPC Test 3 requires the proper operation of the components used in tests 0 and 1 plus the bus control components U630, U645, U540 (pins 10 and 11), U440A, and U545 (pins 5 and 6). If this test is the only one failing, see *SPC Test 3* in this section.

The correct functional operation of all components listed in Table 7-1 plus those listed above is required for tests 0, 1, 2, and 3 to pass. A failure in any of these components can cause all SPC tests to fail. A procedure is described on the following pages to help isolate the faulty component.

Table 7-1
SPC COMPONENTS

Component	Description	Function
U560	Port Address Selector	Decodes SPC Load and Execute commands and selects the Back Panel Address Switch buffer, Master/Slave, or Printer RS-232 port.
U660	SPC Data Buffer	Program Memory RAM is loaded through this register.
U375	Program Memory RAM	Contains SPC control program.
U455D	Load enable gate	Enable the Program Memory RAM write enable input.
U575	Program Counter	Controls the addressing of the Program Memory RAM.
U465A	Execute Program command test bit.	Controls the state of the Execute Test Bit.
U465B	Test bit select control.	Determines when the test bits for load and execute are monitored by controlling the state of the C input (pin 9) of Test Condition Multiplexer U445.
U465C	"Byte Loaded" Test Bit.	Controls the state of the Load Test Bit.
U445	Test Condition Multiplexer.	Selects one of five test bit conditions.
U585	Current Instruction Register.	Holds the current instruction from the Program Memory RAM.
U285	Instruction Decode ROM.	Decode the current instruction.
U275	ROM output latch.	Holds the current decoded instruction. Bits 7-6 are fed to control inputs A and B of the Test Condition Multiplexer (U445), bits 5-3 are fed to control inputs A, B and C of the Instruction Demultiplexer (U370), and bits b2-b0 are used as address bits b2-b0 of the Instruction Decode ROM and as inputs to the Next Instruction gate (U365C).
U370	Instruction Demultiplexer.	Decodes bits b5-b3 of ROM output latch into one of eight control lines as follows: Y7 Access Granted (ACCGR) input to GPIB (not used in any diagnostic tests). Y6 Enable Printer Baud Rate Write port, U140 (used in test 3).

Table 7-1 (Cont.)
SPC COMPONENTS

Component	Description	Function
		Y5 Outputs Bus Request (BREQ) through U440 and U545 and enables Bus Acknowledge latch, U630 (used in test 3). Y4 Control of I0 and I1 inputs to PC, U575 (used in tests 0,1,2, and 3). Y3 Enable control demultiplexer, U470B (used in tests 0,1,2, and 3). Y2 Increment Program Counter, U575 (used in tests 0,1,2, and 3). Y1 Increment Loop Counter, U675 (used in test 2). Y0 Clears Bus Acknowledge latch, U630 (used in test 3).
U440B	Test bit to Instruction Decode ROM, address A3, latch.	Outputs the selected test bit from U445 to input address A3 of the Instruction Decode ROM, U285.
U365C	Next instruction gate.	Clocks the next instruction from Program Memory RAM into Current Instruction Register.
U470B	Instruction de-multiplexer.	Decodes inputs A and B from the output of the Current Instruction Register (U585), as follows: A B Function 0 0 Controls I0 of Program Counter, U575 (used in tests 0, 1, 2, and 3). 1 0 Clocks Program Memory RAM output into SPC Data Register, U665 (used in tests 0, 1 and 2). 0 1 Clocks Program Memory RAM output into SPC Address Register, U670 (used in test 3). 1 1 Loads Loop Counter, U675 (used in test 2).

Finding the Defective SPC Component

The heart of the SPC consists of fourteen components (described earlier) all connected in one feedback loop. A failure in any one of these components causes the entire SPC to stop functioning.

To aid in the isolation of the fault, a means is provided to break this loop and force execution of a special debugging program in the Instruction Decode ROM at address $1F0_{hex}$. By moving the strap at connector J689 (located near U675) to pins 2 and 3, the output of the Instruction Memory RAM is disabled and placed in a high-impedance state. This forces all 1's onto the Current Instruction Register (U585). If U585 is working, the debugging program in the Instruction Decode ROM (U285) is executed. This program is a continous loop test.

The following procedure tests some portion of all the components making up the SPC except the Program Memory RAM (U575), SPC Data Buffer (U660), Data Register (U665), Address Register (U670), gates, (U455 and U555) and flip-flops (U465A and U465B). These components have to be tested by looping on SPC tests 0.

Troubleshooting Procedure

Turn the DAS power off and remove the Option 06 Communication Interface board (Refer to the *Maintenance: General Information* Section of this manual for instructions to remove the board). Remove the jumper on the Extender board that connects A26 (BREQ) signal from the Option 06 I/O Communication Interface board to the DAS bus. Removing the jumper prevents the test from grabbing the DAS bus and causing the DAS to affect the operation of the SPC.

Place the Extender board on the Option 06 board and reinstall the board in the DAS I/O Interface slot.

Move the jumper on the Option 06 Communication Interface board at J689 (located next to U675) from pins 1 and 2 to pins 2 and 3. This jumper connection disables the Program Memory RAM, U375, and forces its output into a high impedance state.

Power up the DAS. Once the power is turned on, the test runs continuously.

NOTE

The DAS display may be blank or have meaningless characters on the screen. The blank screen or the meaningless characters have no effect on the procedures.

NOTE

To stop the test and return to normal operation, turn off the DAS, relace the jumper on the Extender board, and move the jumper J689 back to positions 1 and 2. Now the DAS is ready for normal operation. Power up the DAS.

NOTE

Modifying the Option 02 Extender board for use with Option 06: The Option 06 I/O Communications Interface board has an Extender board available as an optional accessory. It is recommended that you use this Extender board during troubleshooting. However, in an emergency, the Option 02 Extender board can also be modified for use in troubleshooting the Option 06 I/O Communication Interface board. Solder 18 gauge wire across pins 20, 27, and 42 on both sides *of the Option 02 Extender board.*

The Option 02 Extender board with this modification may not give as satisfactory results as the Option 06 Extender board.

Do not attempt to troubleshoot the Option 06 I/O Communication Interface board with an unmodified Option 02 Extender board.

The program stored in the Instruction Decode ROM (U285), is running. This program repeatedly increments the ROM output pins b0-b2, b3-b5 and b6-b7 from 000_{bin} through 111_{bin} except for b6-b7 which increment from 00_{bin} to 11_{bin}. The three groups of pins are all incremented in unison (i.e., they all start with 000_{bin} or 00_{bin} at the same time).

Verify that this is happening by triggering the scope or logic analyzer from pin 8 of U365 and monitoring the outputs of the Instruction Decode *ROM* (U285). If it is not incrementing, check for one of the following possible causes:

- SPC bus connected to input of Current Instruction Register U585 is not floating. Check it with a scope and a 10K pull-up resistor tied to +5V. If the inputs are floating, they are +5V.
- Output of Current Instruction Register U585, is not $1F_{hex}$. This could be caused by U585 being defective, or by the instruction not geting clocked into U585 by the clock pulse from U365, or by the Master Reset pin 1 of U585 being stuck low.
- Check to see if there is a clock pulse on pin 9 of U585 and that the Master Reset pin 1 of U585 is high. If the Master Reset pin is high and there isn't a clock pulse, one can be forced by temporarily shorting it to ground and removing the short. Try this and see if a $1F_{hex}$ gets clocked into the register.
- If the Master Reset is stuck low, check inverter U540D and latch U465. If the Master Reset is not stuck low replace U585.
- If $1F_{hex}$ is clocked into U585, then the problem is in the Instruction Decode ROM (U285), the ROM output latch (U275), or the NAND gate (U365).
- If the output of the Instruction Decode ROM is incrementing, verify that the output of the ROM output latch is incrementing. If it is not, check the clear input of the latch (pin 1) for a high signal and its clock input (pin 11) for a 40MHz clock. If the inputs are correct replace U275.
- Verify that the output of the Instruction Demultiplexer (U370) is incrementing through all of its outputs. If it is not, replace it.
- Check the output of inverter U540E (pin 10), and OR gate U460 (pins 6 and 8), to make sure the input pulse is getting through.
- Verify that there is an output (pin 8) at NAND gate U530.

- Check that the carry out (pin 14) of Loop Counter U675 has an output signal. The counter is loading an FF*hex* each time the IO (pin 2) goes low and outputing a carry out each time it is incremented (when pin 10 of NOR gate U530 goes low) and it receives a clock signal at pin 1.
- Check the output of Flip-flop U440A (pin 6) to make sure that it is toggling. If it is not check for toggling signals on pins 1, 2, and 3. If they are correct, replace U440.
- The output of inverter U545, is low because disconnecting the BREQ signal opened the open collector output circuit of U545. The pull-up resistor was disconnected when the strap was removed on the extender card.
- Verify that the output (pin 9) of U470 goes low each time that the enable (pin 15) goes low. The other two inputs and the other three outputs are all be high.
- Verify that the output (pin 5) of Test Condition Multiplexer U445, is toggling.
- Verify that the output (pin 9) of U440B is toggling. If it is not, make sure it has a clock signal. Check that the clock frequency is 8 MHz.
- Check the Program Counter U575 address output pin 22. This pin is toggling. If it is not check the clock and input control pins. If they are present, replace U575.
- To verify that all of the Program Counter address lines are working, short pin 3 of the Instruction Demultiplexer U370 to ground. This causes all of U370 outputs to increment preventing the Program Counter from being loaded with an FF*hex*. This causes all the output lines of the Program Counter to increment.
- The operation of the load test bit latch U465D, (pins 13, 14, and 15) can be checked by monitoring its output (pin 13) while alternately shorting its input (pin 15) to ground. (Its output goes high each time the input is shorted to ground.)

If this procedure did not isolate the problem, the problem is in a component outside of this test, or a portion of a component outside of this test. These components are:

- the program memory RAM (U575)
- SPC data buffer (U660)
- data out register (U665)
- address register (U670)
- gates (U455 and U555)
- flip-flops (U465A and U465B)

These components are tested by looping on SPC tests 0 or 1 (see *Troubleshooting the Smart Port Controller* procedure in this section and use for test 0).

FUNCTION 2: GPIB TESTS

TEST 0: GPIB Reset Test

These parts are found on schematic 88.

This test resets the GPIB controller U135 by loading the Auxiliary Command register (address FB hex) with an 80hex, clearing the reset and then reading the Address Status register (address FA hex) for 00*hex*.

ERROR: EXPECTED DATA = 00_{hex}
ACTUAL DATA = Any value other than 00_{hex}

POSSIBLE CAUSES: There are no clock and chip enable signals at the GPIB controller U135 input or the controller is not working.

ACTION: Loop on the test and verify that the GPIB controller is getting a chip enable signal (pin 3 of U135). If it is not, check the inputs of U525D and U540A. Verify that there is a clock pulse on pin 18 of U135. If not, check the clock divider U175B. If all signals are present, disconnect the cable from the GPIB connector. If it still doesn't pass, replace U135.

TEST 1: GPIB Listener Mode Test

This test places the GPIB in the listener mode by programming the Auxiliary Command register with an 89_{hex} and then reading the Address Status register for an 04_{dec} in the device listen mode.

ERROR: EXPECTED DATA = 04_{hex}
ACTUAL DATA = Any value other than 04_{hex}

POSSIBLE CAUSES: (Same as Test 0)

ACTION: (Same as Test 0)

TEST 2: GPIB Talker Mode Test

This test places the GPIB in the listener mode by programming the Auxilliary Command register with an $8A_{hex}$ and then reading the Address Status register for an 02_{dec}, in the device talker mode.

ERROR: EXPECTED DATA = 02_{hex}
ACTUAL DATA = Something other than 02_{hex}

POSSIBLE ACTION: (Same as Test 0)

ACTION: (Same as Test 0)

Troubleshooting the GPIB

The method for troubleshooting tne GPIB port is to stimulate it in a repetitive manner. To do this, use a Tektronix 4051 Desktop Computer, or the equivalent.

Connect a GPIB cable between the port on the 4051 and the port on the DAS. Then set the DIP switch on the back of the DAS so switch number 8 is closed and all others are open.

Power-up the 4051 and enter the program listed in Table 7-2.

NOTE

All BASIC programs found in this text are written for a Tektronix 4050 series computer, and may be incompatible with other versions of BASIC. If you have a different controller, you will have to develop a program for it which is the equivalent of the one provided.

Table 7-2
GPIB STIMULATION PROGRAM

```
100  ON SRQ THEN 200
110  PRINT @ 1:"ID?"
120  INPUT @ 1: R$
130  PRINT R$
140  GOTO 110

200  POLL A0,B0;I
210  PRINT B0
220  RETURN
```

This program repeatedly asks address 1 on the GPIB to identify itself. The device at address 1 should respond with its identification after each request.

Power up the DAS. When the power-up self test is finished, enter the Input Output menu. Verify that the top of the display has the message "GPIB TALK/LISTEN ADDRESS: 1".

NOTE

If the DAS does not display the proper message at the top of the screen, the interface between the I/O Interface and the DAS is not operational. Repair the DAS I/O Interface problem before troubleshooting the GPIB.

Now enter RUN on the 4051.

1. If the DAS GPIB port is operating properly, the screen of the 4051 should display the DAS identification number, filling the entire page to the bottom.
2. If the 4051 displays "GP INTERFACE BUS I/O ERROR" on the screen, examine the Input Output menu of the DAS. Make sure the message at the top of the screen calls out address 1. If the address is not set to 1, check the setting of the DIP switch on the back of the DAS.
3. If two-way communications with the DAS cannot be established, try a one way communication.

   If the DAS does not respond with its identification, the following procedure attempts to tell the DAS to enter the Channel Specification menu.

   On the 4051, press <BREAK> twice. This will stop execution of the program. Press <HOME PAGE> on the 4051. On the 4051 enter (with no line number)

   PRINT @ 1: "CHANNEL"

The DAS screen should change to the Channel Specification menu. If the screen does not change, the communication is not reaching the DAS. The GPIB controller 9914 (U135) or the buffers (U125 and U225) are suspect. Running the Diagnostics may help find the problem.

FUNCTION 3: RS-232 TEST

These parts are found on schematic 90 unless otherwise specified.

NOTE

A standard RS-232 cable must be connected between the Master/Slave RS-232 port and the Printer RS-232 port for all of the RS-232 tests.

TEST 0: DSR Test

This test checks for a high on the Master/Slave DSR (pin 22 U435) input and the ability of the Master/Slave RS-232 controller 8251A to read it. The high is provided by a pull-up resister on the CD pin of the Printer RS-232 port.

ERROR: EXPECTED DATA = 80*hex*
ACTUAL DATA = 00*hex*

POSSIBLE CAUSE: No pull-up resistor on CD pin 9 of the Printer port connector or a defective input receiver (U415), pin 10 and 8.

ACTION: Check for a high on the input (pin 10) of U415. If it is not high, check the pull-up resistor on pin 9 of the Printer port connector. If it is high, check for a low on the output (pin 8) of U415, and replace U415 if it is not there.

ERROR: EXPECTED DATA = 80*hex*
ACTUAL DATA = Something other then 80*hex* or 00*hex*.

POSSIBLE CAUSE: The RS-232 controller 8251A, U435 is defective. No clock signal or no chip select signal.

ACTION: Check for the presence of a clock on pin 20 of U435. If it is not there, trace it back through the clock circuitry U175, U170, and Y185. If it is present, turn the display off, loop on the test and check for a chip select pulse at pin 11 of U435. If it is present, replace U435.

If the chip select pulse is not present, trace it back through gate U555 schematic 88 and Port Address Selector (U560 schematic 88).

TEST 1: Master/Slave to Printer Port Data Transfer test.

NOTE

TXRDY and RXRDY are internal bits in the RS-232 controller (8215A) status register and not a signal on the output pins of the chip.

This test transmits the characters 0 through 256 from the Master/Slave port to the Printer port. It first enables the Master/Slave transmitter and waits for a TXRDY (Transmitter Ready) signal from the Master/Slave port controller 8251A. If it does not get a TXRDY signal within a specified time, a fail message and the message TST1-XMIT TIME OUT are displayed in the bottom left corner of the screen.

If it does get the TXRDY command, it loads the first character and waits for the RXRDY (Receiver Ready) signal fromt the Printer port controller 8251A. If it does not get RXRDY signal within a specified time, a FAIL message and a TST1-RECEIVER TIME OUT message is displayed. If it does get the RXRDY signal, it reads the character from the Printer port data bus and compares it against the transmitted character. This is repeated for each character from 0 to 256. The characters are transmitted at a baud rate of 9600 baud.

ERROR: EXPECTED DATA = 00*hex* through FF*hex*
ACTUAL DATA = TST1-XMIT TIME OUT

POSSIBLE CAUSE: The controller 8251A (U435) is defective, no clock signal, or no chip select signal.

ACTION: Check for the presence of a baud rate clock at pin 20 of U435. If it is not there, trace the signal back through the clock circuitry (U175, U170 and Y185). If the signal is present, turn off the DMA to clear the display, loop on the test, and check for a chip select pulse on pin 11 of U435. If it is present, replace U425.

If the chip select signal is not present, trace it back through gate U555 and Port Address Selector (U560).

ERROR: EXPECTED DATA = 00_{hex} - FF_{hex}
ACTUAL DATA = RECEIVER TIME OUT

POSSIBLE CAUSE: Defective transmitter (U435), line driver (U635), or line receiver (U415).

ACTION: Trigger on the U435 chip select pin 11 and check the data path from TD (Transmit data), pin 19 of U435, to the RD (Receive data) pin 3 of U425. Verify the data transfer by following the signal path. If the data is lost, replace the faulty component (U435, U415,or U635).

POSSIBLE CAUSE: Defective receiver U425 or baud rate clock.

ACTION: Check for the presence of a baud clock at pin 9 or pin 25 of U425. If it is present, replace U425.

If it is not present, trace the baud rate clock path back through the baud rate multiplexers and the clock circuitry. It would also be helpful to check the results of the Baud Rate Multiplexer test (Test 0) and the Baud Rate test (Test 4).

ERROR: EXPECTED DATA = 00_{hex} - FF_{hex}
ACTUAL DATA = Anything else, but without a time out message

POSSIBLE CAUSE: Defective receiver U425.

ACTION: Replace U425.

TEST 2: Printer to Master/Slave port data transfer test.

NOTE

TXRDY and RXRDY are internal bits in the RS-232 controller (8215A) status register and not a signal on the output pins of the chip.

This test transmits the characters 0 through 256 from the Printer port to the Master/Slave port. It first enables the Printer transmitter and waits for a TXRDY (Transmitter Ready) signal from the Master/Slave RS-232 controller, 8251A. If it does not get a TXRDY signal within a specified time, a fail message and the message TST2-XMIT TIME OUT is displayed in the bottom left corner of the screen.

If it does get the TXRDY command, it loads the first character and waits for the RXRDY (Receiver Ready) signal from the Master/Slave port RS-232 controller, 8251A. If it does not get RXRDY signal within a specified time, a FAIL message and a TST2-RECEIVER TIME OUT message is displayed. If it does get the RXRDY signal, it reads the character from the Master/Slave port data bus and compares it against the transmitted character. This is repeated for each character from 0 to 256. The characters are transmitted at a baud rate of 9600 baud.

ERROR: EXPECTED DATA = 00_{hex} - FF_{hex}
ACTUAL DATA = TST2-XMIT TIME OUT

POSSIBLE CAUSES: Defective RS-232 controller 8251A (U425).

ACTION: If Test 0 and Test 1 passed and this test failed, replace U425. If all three tests failed, use the troubleshooting procedures described in tests 0 and 1 to isolate the problem.

ERROR: EXPECTED DATA = 00_{hex} - FF_{hex}
ACTUAL DATA = RECEIVER TIME OUT

POSSIBLE CAUSE: Defective transmitter (U425), line driver (U635), or line receiver (U415).

ACTION: Trigger on the U425 chip select pin 11 and check the data path from TD (Transmit data), pin 19 of U425, to the RD (Receive data) pin 3 of U435. Verify the data transfer by following the signal path. If the data is lost, replace the faulty component (U415, U425, or U635).

POSSIBLE CAUSE: Defective receiver U425 or baud rate clock.

ACTION: Check for the presence of a baud clock at pin 9 or pin 25 of U435. If it is present, replace U425.
If it is not present, trace the baud rate clock path back through the baud rate multiplexers and the clock circuitry. It would also be helpful to check the results of the Baud Rate Multiplexer test (Test 0) and the Baud Rate test (Test 4).

ERROR: EXPECTED DATA = 00_{hex} - FF_{hex}
ACTUAL DATA = Anything else, but without a time out message

POSSIBLE CAUSE: Defective receiver U435.

ACTION: Replace U435.

FUNCTION 4: BAUD RATE TESTS

TEST 0 Through 5:

These parts are found on schematic 90.

The numbers displayed under the ADDRESS heading on the Diagnostic menu are the baud rate being tested and *not* the address of the test that is read back. The tests are similar and the following description covers all of the tests.

Function 4 - Baud Rate tests:
Test 0: 300 Baud test (requires RS-232 cable)
Test 1: 600 Baud test
Test 2: 1200 Baud test
Test 3: 2400 Baud test
Test 4: 4800 Baud test
Test 5: 9600 Baud test

All tests require the RS-232 cable.

These tests check the baud rates of 300, 600, 1200, 2400, 4800, and 9600. The tests use the Z80 clock to measure the time it takes to transfer the characters 55_{hex} from the Master/Slave RS-232 port to the Printer RS-232 port.

The baud rate multiplexer and the 8251A divide factors are programmed first and then the Master/Slave transmitter is enabled. When TXRDY goes true, a counter is started and 55_{hex} is loaded into the transmitter data register which causes the data to be transmitted. If TXRDY does not go true within a specified time, a FAIL message and the error code 6666_{hex} are displayed for the ACTUAL data.

After the data has been transmitted, the Printer port status register is monitored for RXRDY. When RXRDY goes true, the counter is stopped and the data is read and compared to 55_{hex}. The count is displayed as the ACTUAL data. If RXRDY does not go true within a specified time, a FAIL message and the error code 7777_{hex} are displayed as ACTUAL data.

If the read data is not equal to 55_{hex}, the error code 5555_{hex} is displayed as ACTUAL data. The count is compared against high and low limits.

If it is below the low limit, the low limit is displayed as EXPECTED data and the actual count is displayed as ACTUAL data.

If the count is above the high limit, the high limit is displayed as EXPECTED data and the actual count is displayed as ACTUAL data.

If the count is within the high and low limits, the actual count is displayed as both EXPECTED and ACTUAL data (this results in the EXPECTED data varying a little from test to test).

NOTE

TXRDY and RXRDY are internal bits in the RS-232 controller (8215A) status regester register and not a signal on the output pins of the chip.

The baud rates, clock frequency, 8251A divide factors, and the low and high limits are as shown in Table 7-3.

Table 7-3
BAUD RATE TEST

TEST NO	BAUD RATE	CLOCK RATE	DIVIDE BY	LOW LIMIT	HI LIMIT IN HEX
0	300 baud	19. 2KHz	64	7CE	85A
1	600 baud	38. 4KHz	64	3D5	425
2	1200 baud	76. 8KHz	64	1F0	210
3	2400 baud	38. 4KHz	16	F3	103
4	4800 baud	76. 8KHz	16	83	8B
5	9600 baud	153. 6KHz	16	39	43

Troubleshooting the Baud Rate Circuits
The following troubleshooting procedure assumes that Test 3 passed. If both Tests 3 and 4 failed, use the troubleshooting procedures in Test 3 first.

The problems this test detects that Test 3 did not are the clock operating at the wrong frequency, or the baud rate multiplexers, U145 and U155, or the baud rate counter, U165, stuck on the wrong frequency.

ERROR: EXPECTED DATA = Within limits.
ACTUAL DATA = Out of limits

POSSIBLE CAUSE: Defective baud rate counter, U160.

ACTION: Check the outputs of U160 for frequencies of 19.2KHz, 38.4KHz, 76.8KHz and 153.6KHz. If they are all off, check the input frequency for a frequency of 307.7KHz. If the 307.7KHz is off, check U165 (pin 2) for an input frequency of 4MHz.

POSSIBLE CAUSES: Defective baud rate multiplexers, U145 or U155.

ACTION: Loop on Function 4 the Baud Rate Tests. Press the DAS SELECT key until you are looping on the test that failed (Test 0 to 5). Using Table 7-3, determine the clock frequency for the test that failed. This clock frequency is on the RS-232 controllers (pin 9 and 25 of U425 and U435). If the frequency is wrong, trace the signal back through multiplexers U145 and U155 to U160.

If the frequency at the multiplexer is correct (U145 or U155), check the select inputs to the multiplexers driven by U140 and U340. If these inputs are correct change the multiplexer in the effected circuit (U145 or U155).

If the frequency is wrong, check the outputs of U160 for frequencies of 19.2KHz, 38.4KHz, 76.8KHz and 153.6KHz. If they are all off, check the input frequency for a frequency of 307.7KHz. If the 307.7KHz is off, check U165 (pin 2) for an input frequency of 4MHz.

FUNCTION 5: ROM PART NUMBERS

This is not really a test. Its main intent is to display the part numbers of all ROMs in the DAS (except the Interpreter ROM on the DAS Controller Module). This provides an easy method of checking the ROMs for the correct part numbers. In addition, this test checks the ROM paging registers in the Option O6 I/O Communication Interface board which includes memory map register U345 and memory map decoder, U355.

The test reads the part number stored in ROM. If it reads an FFFF*hex*, it ignores it. Otherwise it checks the item identification number in the ROM header and compares it against the item identification number of the previously read ROMs on the board. If it does not find an identical number it displays the part number it did find.

NOTE

The Trigger board has two ROMs with the same part number stored in them, even though one of them is really a 160-1039-XX. Also the Option 06 I/OCommunication Interface board lists both ROM part numbers twice. This is because the two 16K ROMs are treated as if they were four 8K ROMs .

ERROR: Display does not list all of the ROM part numbers on the Option 06 Communication Interface board.

POSSIBLE CAUSE: Defective ROM memory map register U345 and memory map decoder U355.

ACTION: Using a logic analyzer, verify that the ROM select outputs of U345 (pin 15) and U355 (pins 12, 13, 14 and 15) toggle high and low when the Rom Part Numbers, test 5, is executed.

POSSIBLE CAUSE: Bad ROM

ACTION: Since the diagnotics are in one of the ROMs the only ROM that could be bad is the GPIB ROM.

TROUBLESHOOTING: GENERAL INFORMATION

The following equipment is required to troubleshoot the I/O communication interface:

- DAS mainframe
- DAS 9100 Service Maintenance Kit (includes an extender board for the I/O Interface)
- 2 Channel Oscilloscope, with probes
- TEKTRONIX 4051 Desktop Computer with Option 01 the Data Communications Interface.
- RS-232 cable 012-0815-00
- GPIB cable 012-0630-03

POWER-UP CHECKSUM TEST

Power-up the DAS and enter the Input Output menu.

Locate the DIP address switch on the back panel of the DAS. This switch is used to set the address of the DAS on the GPIB. Set switch for GPIB address 1.

Verify that the message GPIB TALK/LISTEN ADDRESS: 1 is present on the display at the top of the Input Output menu.

1. If this message is present, the interface between the DAS and the I/O communication interface is probably functioning properly.
2. If the message appears at the top of the screen, but calls out the wrong address (e.g., GPIB TALK/LISTEN ADDRESS: 0) the problem is in the address switch or the GPIB address register.
3. If the message does not appear at the top of the screen, the problem is probably in the ROM decoding area or in the data and address buffers.
4. If the ROM decoders and address and data buffers are good, then a power-up checksum error indicates a problem in the ROM.

SECTION 8

MAINTENANCE: DIAGNOSTIC TEST DESCRIPTIONS

See the section on *Troubleshooting* for the Diagnostics information.

REFERENCE INFORMATION

ERROR CODES AND INDICATORS

ERROR AND PROMPTER MESSAGES

Table 9-1 lists the changes and additions in the and prompter messages that may appear on the monitor screen.

Table 9-1
ERROR AND PROMPTER MESSAGES

RS-232 MUST BE OFF TO PRINT	Return to the I/O Menu and select the OFF status.
PRINTER STOPPED	This message indicates the printer function has been halted with the DAS STOP key. This is not an error condition.
SCREEN RESTORE STOPPED	This message indicates the screen restore function has been halted with the DAS STOP key. This is not an error condition.
ENTER A VALUE BETWEEN 30 AND 90	The page length must be between 30 to 90 lines long.

ROM CHECKSUM CODES

If the DAS detects a checksum error upon power-up, an error code is displayed at the top of the screen reading ROM CHECKSUM ERROR. The message also contains a numeric code that corresponds to a socket location on a DAS board. The code is interpreted as shown in Table 9-2.

Table 9-2
ROM CHECKSUM ERROR CODES

Code	Location	Part Location Number
8,1	Op. 06 I/O Interface	U250
8,2	Op. 06 I/O Interface	U260
8,3	Op. 06 I/O Interface	U270
8,4	Op. 06 I/O Interface	U240
8,5	Op. 06 I/O Interface	U250
8,6	Op. 06 I/O Interface	U260
8,7	Op. 06 I/O Interface	U270

The I/O Communication Interface board is located in slot 8.

TEST POINT, JUMPER AND ADJUSTMENT LOCATIONS

There are two ground points located on the I/O Communication Interface board. One on the far left edge, and one on the far right edge. These test points are located on schematic 90, and numbered TP387 and TP404.

The Color Video Output Jack, J405, schematic 88, is located on the left edge of the I/O Communication Interface board.

I/O MAPS

The following set of table lists all the I/O ports in the Option 06 I/O Communication Interface.

Table 9-3
PARTIAL DAS PORT ASSIGNMENTS

Port	R/W	Function
000*hex*	W	ROM Mapping Register
0A0*hex*	W	Baud Rate Generator Master/Slave
0AF*hex*	R/W	Phantom Port used for NOP R/W
0F0*hex*	R	Back Panel Address Switches
0F1*hex*	W	Baud Rate Generator Printer Port
0F1*hex*	R	Baud Rate Read-Back Port (diagnostic use only)
0F2*hex*	R	Execute Program Command to SPC
0F3*hex*	R	Load Program command to SPC
0F3*hex*	W	Load Program into SPC Memory
0F4*hex*	R/W	Data Register Master/Slave 8251A
0F5*hex*	R/W	Control Register Master/Slave 8251A
0F6*hex*	R/W	Data Register Printer 8251A
0F7*hex*	R/W	Control Register Printer 8251A
0F8*hex*	R	9914 Interrupt Status 0
0F9*hex*	R	9914 Interrupt Status 1
0FA*hex*	R	9914 Address Status
0FB*hex*	R	9914 Bus Status
0FC*hex*	R	9914 Address Switch
0FE*hex*	R	9914 Command-Pass-Through
0F0*hex*	W	9914 Interrupt Mask 0

Table 9-3 (Cont.)
PARTIAL DAS PORT ASSIGNMENTS

0F9*hex*	W	9914 Interrupt Mask 1
0FB*hex*	W	9914 Auxiliary Command
0FC*hex*	W	9914 Address Register
0FD*hex*	W	9914 Serial Poll
0FE*hex*	W	9914 Parallel Poll
0FF*hex*	R/W	9914 Data Register

SIGNAL GLOSSARY

Following is a list of signals used in the Option 06 I/O Communication Interface. They are arranged alphabetically. They contain the signal name, and a brief description of the signal function.

BREQ(L): The peripheral device requests control of the data bus from the controller card. This message replaces the WAIT1(L) message.

BACK(L): The controller card has released the Mother board, the address bus, and the data bus. This messages replaces the M1(L) message.

GPIB REQ(L): This is a service request to the Smart Port Controller.

GPIB ACK(L): This is an acknowledgement of the service request to the Smart Port Controller.

TRAPPED(L): The Smart Port Controller has taken control of the Address and Data Bus.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

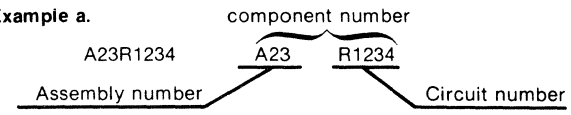
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

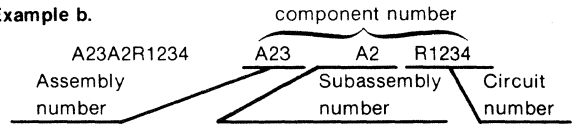
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000JR	MUSASHA WORKS OF HITACHI LTD	1450 JOSUIHON-CHO	KODAIRA-SHI, TOKYO, JAPAN
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P.O. BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
50364	MONOLITHIC MEMORIES	1165 E ARQUES AVENUE	SUNNYVALE, CA 94086
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
CODE 54	331 NOT FOUND		
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
75378	CTS KNIGHTS, INC.	400 REIMANN AVE.	SANDWICH, IL 60548
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A41A1	670-7788-00			CKT BOARD ASSY:I/O OPTION ENHANCED	80009	670-7788-00
A41A2	670-8141-00			CKT BOARD ASSY:I/O INTERFACE CONN	80009	670-8141-00
	----- -----			(DAS 9109 ONLY)		
A41A3	670-7789-00			CKT BOARD ASSY:I/O INTERFACE CONN	80009	670-7789-00
	----- -----			(DAS 9129 ONLY)		
A41A1	670-7788-00			CKT BOARD ASSY:I/O OPTION ENHANCED	80009	670-7788-00
A41A1C149	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C154	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C158	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C164	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C174	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C178	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C233	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C274	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C284	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C323	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C340	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C349	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C364	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C388	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C424	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C454	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C510	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C525	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C530	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C547	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C581	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C629	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C633	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C648	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C661	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C676	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C754	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1C776	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A41A1Q703	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A41A1R117	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A41A1R118	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A41A1R119	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A41A1R215	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A41A1R411	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A41A1R432	307-0446-00			RES,NTWK,FXD FI:10K OHM,20%,(9) RES	91637	MSP10A01-103M
A41A1R554	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A41A1R603	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A41A1R604	321-0186-00			RES.,FXD,FILM:845 OHM,1%,0.125W	91637	MFF1816G845R0F
A41A1R617	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A41A1R618	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A41A1R619	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A41A1R701	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A41A1R716	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A41A1R717	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A41A1R718	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A41A1U125	156-1414-02			MICROCIRCUIT,DI:OCTAL GPIB BUS XCVR	27014	DS75160A
A41A1U135	156-1444-01			MICROCIRCUIT,DI:NMOS,GPIB ADAPTER	01295	TMS9914NL
A41A1U140	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A41A1U145	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A41A1U155	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A41A1U160	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A41A1U165	156-0844-02			MICROCIRCUIT,DI:SYN 4 BIT CNTR,SCRN	01295	SN74LS161A
A41A1U170	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN IN	01295	SN74LS73
A41A1U175	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN IN	01295	SN74LS73
A41A1U215	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A41A1U225	156-1415-01			MICROCIRCUIT,DI:OCTAL GPIB,XCVR MANAGEMENT	27014	DS75161A
A41A1U240	160-2353-00			MICROCIRCUIT,DI:I/0-1 PROGRAMMED	80009	160-2353-00
A41A1U250	160-2354-00			MICROCIRCUIT,DI:I/0-2 PROGRAMMED	80009	160-2354-00
A41A1U275	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A41A1U285	160-0929-00			MICROCIRCUIT,DI:512 X 8 BIPOLAR PROM,PRGM	80009	160-0929-00
A41A1U315	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A41A1U340	156-0392-02			MICROCIRCUIT,DI:QUAD LATCH,W/CLEAR	80009	156-0392-02
A41A1U345	156-0392-03			MICROCIRCUIT,DI:QUAD LATCH W/CLEAR	01295	SN74S175NP3
A41A1U355	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A41A1U360	156-0985-01			MICROCIRCUIT,DI:DUAL 5 INPUT NOR GATE,SCRN	04713	SN74LS260
A41A1U365	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A41A1U370	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A41A1U375	156-1594-00			MICROCIRCUIT,DI:2048 X 8 SRAM	000JR	HM6116P-3(DD-24)
A41A1U415	156-0878-01			MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A41A1U425	156-0877-04			MICROCIRCUIT,DI:USART	34335	AM8251A
A41A1U435	156-0877-04			MICROCIRCUIT,DI:USART	34335	AM8251A
A41A1U440	156-1611-00			MICROCIRCUIT,DI:DUAL D TYPE EDGE-TRIGGERED	07263	74F74
A41A1U445	156-0994-02			MICROCIRCUIT,DI:8 INPUT DATA SEL/MUX	01295	SN74LS151NP3
A41A1U455	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A41A1U460	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A41A1U465	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH,SCRN	01295	SN74LS279NP3
A41A1U470	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A41A1U510	156-0878-01			MICROCIRCUIT,DI:QUAD LINE RCVR,SCRN	80009	156-0878-01
A41A1U515	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A41A1U525	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A41A1U530	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A41A1U535	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A41A1U540	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A41A1U545	156-0724-02			MICROCIRCUIT,DI:HEX INV W/OC OUT,BURN-IN	01295	SN74LS05
A41A1U555	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A41A1U560	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A41A1U565	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A41A1U570	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A41A1U575	156-1732-00			MICROCIRCUIT,DI:OCTAL COUNTER	50364	SN74LS461
A41A1U585	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A41A1U615	156-0530-02			MICROCIRCUIT,DI:QUAD 2-INP MUX,SCRN	01295	SN74LS157P3
A41A1U625	156-0730-02			MICROCIRCUIT,DI:QUAD 2-INP NOR BFR,BURN-IN	01295	SN74LS33
A41A1U630	156-0387-02			MICROCIRCUIT,DI:DUAL J-K FF,BURN IN	01295	SN74LS73
A41A1U635	156-0879-01			MICROCIRCUIT,DI:QUAD LINE DRIVER,SCRN	80009	156-0879-01
A41A1U640	156-0852-02			MICROCIRCUIT,DI:HEX DRVR W/3 STATE INP	01295	SN74LS367NP3
A41A1U645	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A41A1U655	156-1111-02			MICROCIRCUIT,DI:OCTAL BUS TRANSCEIVERS	01295	SN74LS245JP3
A41A1U660	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A41A1U665	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A41A1U670	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A41A1U675	156-1732-00			MICROCIRCUIT,DI:OCTAL COUNTER	54331	SN74LS461
A41A1Y185	119-1329-00			OSCILLATOR,RF:CRYSTAL CONTROLLED,24MHZ	75378	MX0-50-1

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A41A2	670-8141-00			CKT BOARD ASSY:I/O EXTENDER	80009	670-8141-00
A41A2C100	283-0775-00			CAP.,FXD,MICA D:1764 PF,1%,500V	00853	D19-5F17640F0
A41A2DS120	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A2DS125	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A2DS130	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A2DS135	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A2S250	260-1721-00			SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5
A41A2W210	175-7353-00			CA ASSY,SP,ELEC:13.25 INCH LONG,RIBBON	80009	175-7353-00
A41A3	670-7789-00			CKT BOARD ASSY:I/O INTERFACE CONNECTOR	80009	670-7789-00
A41A3C100	283-0775-00			CAP.,FXD,MICA D:1764 PF,1%,500V	00853	D19-5F17640F0
A41A3DS120	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A3DS125	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A3DS130	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A3DS135	150-1061-01			LT EMITTING DIO:RED,660NM,50MA MAX	50434	HLMP-1301
A41A3S250	260-1721-00			SWITCH,ROCKER:8,SPST,125MA,30VDC	00779	435166-5
A41A3W210	175-7353-00			CA ASSY,SP,ELEC:13.25 INCH LONG,RIBBON	80009	175-7353-00

COLORS ON SCHEMATICS

Introduction

Some of the schematics in this section are color-coded. This coding indicates the flow of the self-diagnostic tests contained in the DAS. Each separate color stands for an individual diagnostic function. The correlation between colors and functions is indicated in the legend at the lower left corner of each color schematic.

PARTS OF THE COLOR SCHEMATICS

There are three parts to each color schematic in this manual:

- **Color.** The color follows the lines of the schematics that are first used by a diagnostic function.
- **Legend.** The legend makes the correlation between colors and specific diagnostic functions.
- **Function Tags.** The function tag at the beginning and end of each colored line indicates all functions that are present on the line.

The colors on the schematics indicate the presence of a diagnostic self-test at the point the color is present. The specific color at any point on the schematic indicates only the first diagnostic function that is run at that point on the board. (This has been done to avoid possible confusion arising from trying to show multiple colors on a single line.)

Note, however, that if the diagnostic test functions are run in the recommended sequence, then any circuitry that was tested by a previous test is not shown in the color of the most recent test. Only the new circuitry that is tested by a diagnostic function is indicated in the colors of the schematics.

NOTE

Any color will always stand for the same test on all schematics for one board. That same color may be used on schematics for another board and signify an entirely different diagnostic test function. Colors are consistent on any one board, but do not try to relate colors on one board to colors on another board -- there is no correlation.

To indicate which colors correspond to each diagnostic test, there is a legend near the lower left corner of the schematic. Refer to this legend whenever the DAS self-diagnostics are used to troubleshoot a board. On any schematic or set of schematics for a board, one color always stands for the same diagnostic function.

At the point where a colored line enters or leaves a schematic, there is a note that refers to the functions on that line. Use these function tags when tracing the sources of diagnostic tests through the schematics or when looking for circuitry common to more than one test. All diagnostic functions that enter or leave the page at that point are indicated by the function tag.

USING THE COLOR IN TROUBLESHOOTING

The color on the schematics is designed exclusively as a troubleshooting aid. Three examples follow that show how the colors can be used to find circuit faults.

One Diagnostic Function Failure

Start the troubleshooting procedure by running all the DAS diagnostic functions on the board to be repaired. Suppose only one of the tests failed. Note the function that failed, and flip to the schematics for that board. Refer to the legend on the schematic page to see which color corresponds to the function that failed. Any point on the schematic that shows the color corresponding the the diagnostic function is the probable location of the failure.

Multiple Diagnostic Function Failures

Start the troubleshooting procedure by running all the DAS diagnostic functions on the board to be repaired. Suppose more than one of the tests failed. Note the functions that failed as well as the numbers of the functions. Flip to the schematics for the board to be repaired. Refer to the legend on the schematic page to find out which color corresponds to the diagnostic function with the lowest number.

Since more than one diagnostic function failed, the failure must be in circuitry that is common to all of the failed tests. This means the failure is on the color that corresponds to the lowest function number. Find the areas on the schematics that show that color. Now refer to the function tags at the beginnings and ends of lines of this color. Use the function tags to define an area in the failed color that contains all of the failed diagnostic functions. This area will probably be much smaller than the area covered by the selected color.

No Diagnostic Function Failures

When troubleshooting failures not detected by the diagnostics, first define the type of failure and the possible causes. Next, examine the white (uncolored) areas of the schematics that might contain this type of circuit fault. (You need only examine the white areas since all colored areas are covered by the diagnostics.)

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

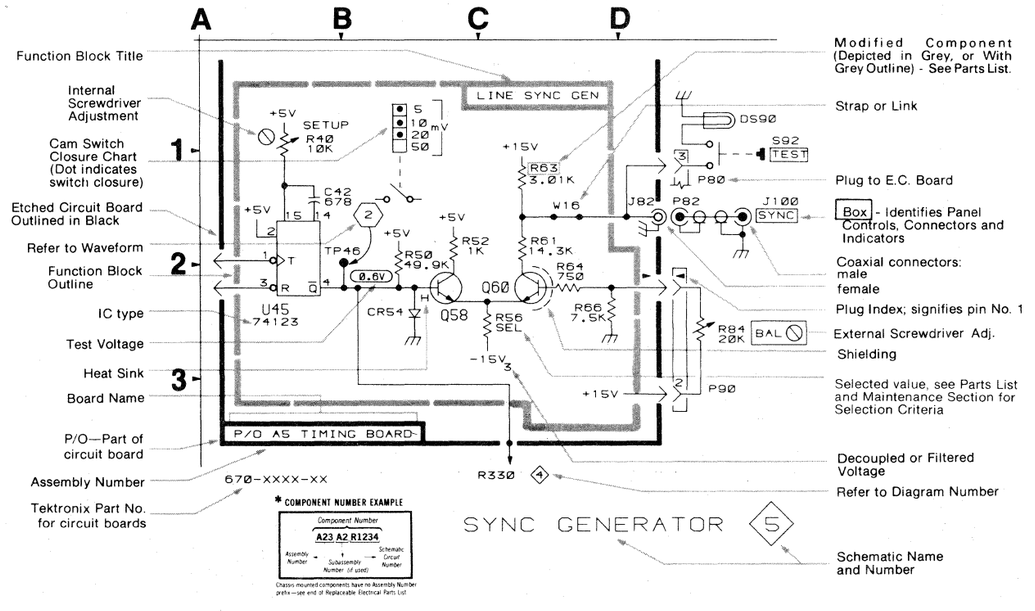
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



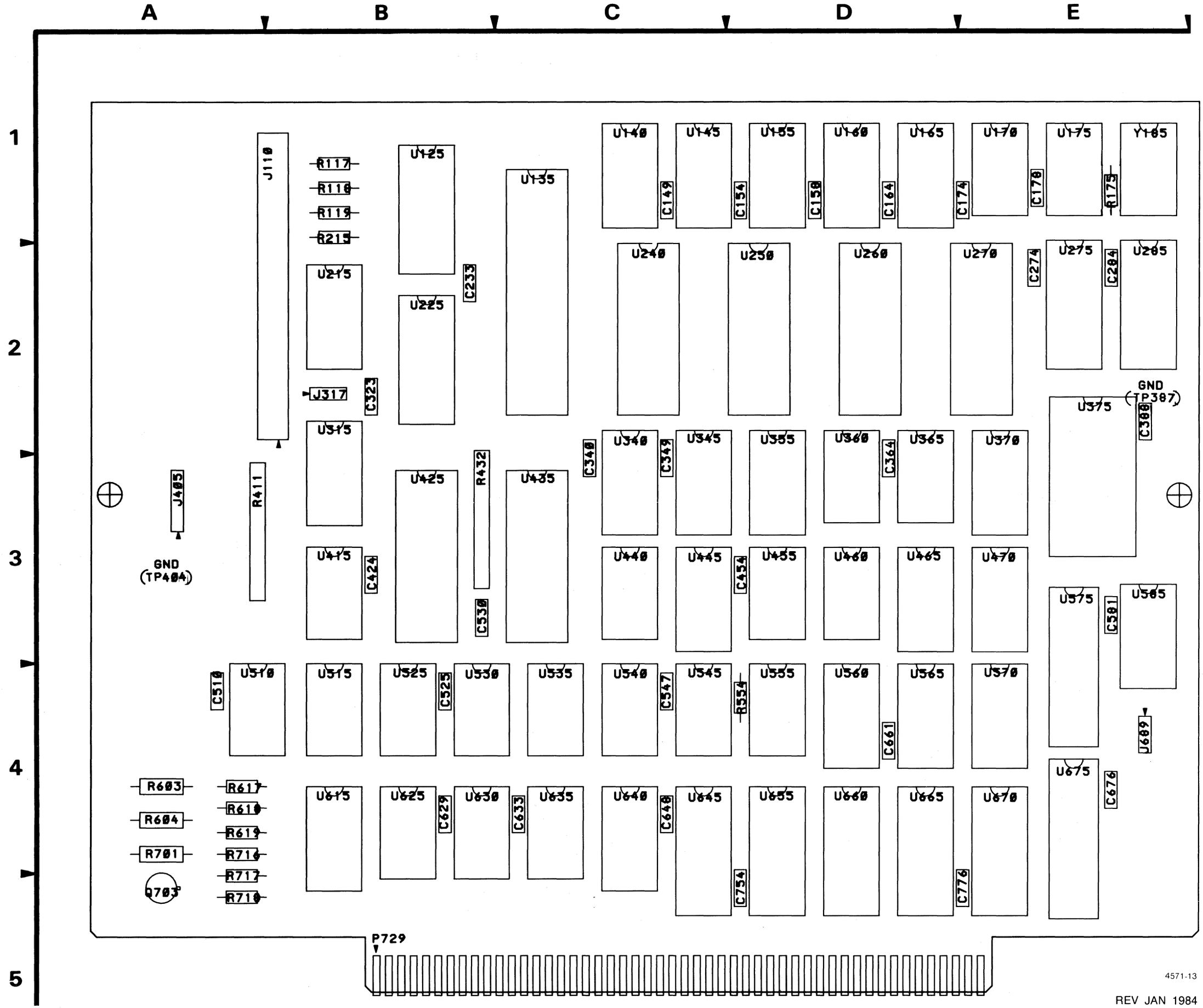


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Figure 11-1. A41A1 I/O Communication Interface Board Component Location

Table 11-1
OPTION 06 I/O COMMUNICATION INTERFACE GPIB

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C754	D4	D4
J110	A4	A1
J110	F1	A1
J110	F2	A1
J317	B5	B2
J405	F1	A3
P729	D1	B4
P729	A5	B4
P729	F5	B4
P729	A1	B4
Q703	F1	A4
R117	F5	B1
R118	F4	B1
R119	F4	B1
R215	F4	B1
R411	A4	A3
R432	E4	B3
R554	D4	D4
R603	E1	A4
R604	F1	A4
R617	E1	A4
R618	F1	A4
R619	E1	A4
R701	F1	A4
R716	F1	A4
U125	F2	B1
U135	E3	C2
U215A	F4	B2
U215B	B4	B2
U225	F3	B2
U240	C2	C2
U250	C3	D2
U260	C3	D2
U270	C3	E2
U315	B5	B3
U345	B3	C3
U355	C3	D3
U455B	B1	D3
U455C	B1	D3
U525B	E1	B4
U525C	E1	B4
U525D	E2	B4
U530D	D3	B4
U535C	E3	C4
U535D	E3	C4
U540A	D2	C4
U540B	D3	C4
U545D	D4	C4
U555A	C5	D4
U555B	D3	D4
U555C	C5	D4
U560	C4	D4
U565A	A3	D4
U565F	A2	D4
U570A	A3	E4
U570D	A2	E4
U615	E3	B4
U625	E1	B4
U640B	A2	C4
U640C	A2	C4
U640D	A3	C4
U655	D4	D4

The colors on this page correspond to the following Option 06 diagnostic functions:

- POWER-UP
- 0 BAUD RATE MULTIPLEXER
- 1 SMART PORT CONTROLLER
- 1 LOOP COUNTER
- 1 ADDRESS SWITCH BUFFER
- 2 GPIB
- 3 RS-232
- 4 BAUD RATE

For more information, refer to the Troubleshooting section.

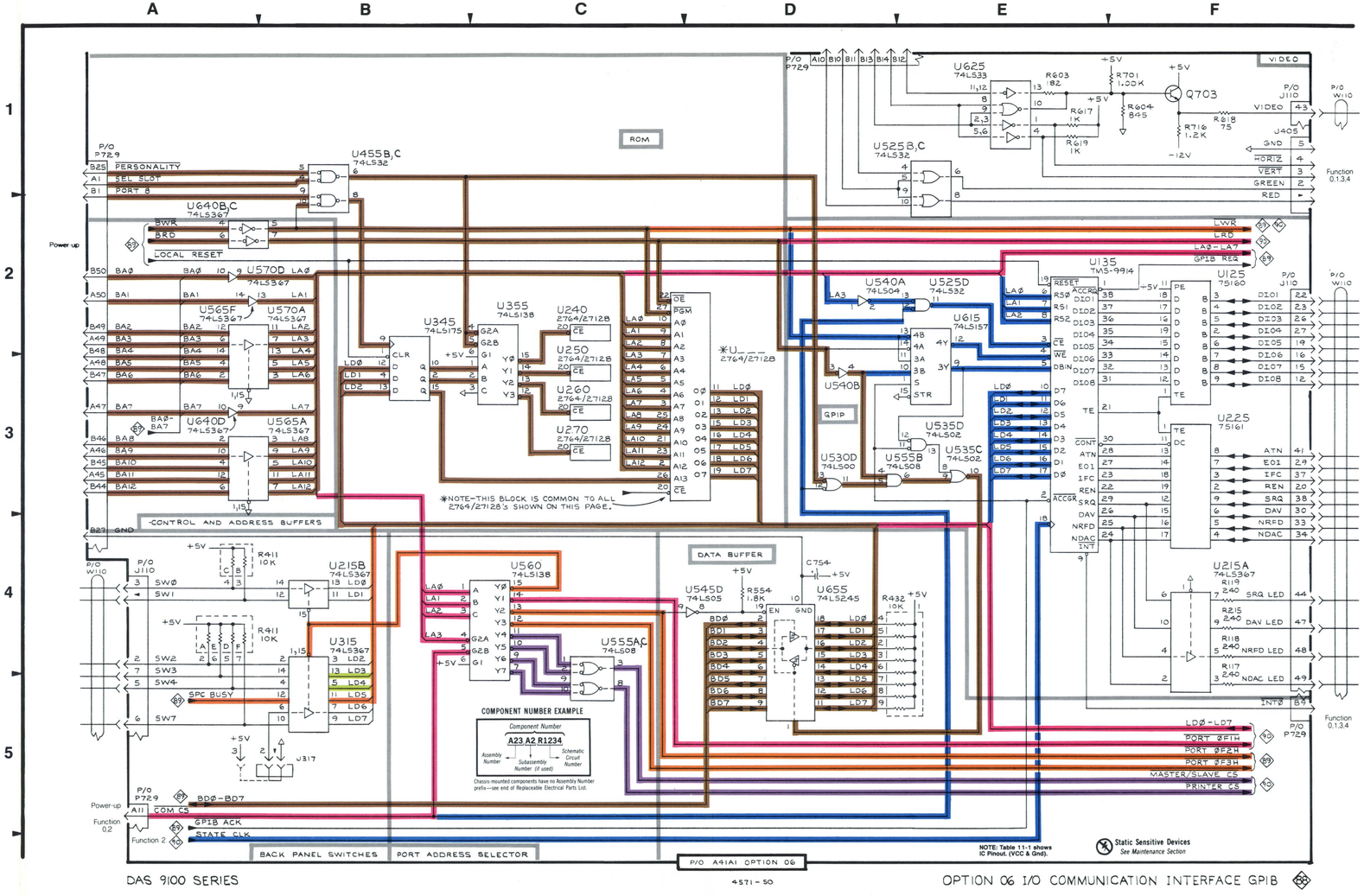


Table 11-2
OPTION 06 I/O COMMUNICATION INTERFACE SPC

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J689	D3	E4
P729	F2	B4
P729	A1	B4
U275	C2	E2
U285	B2	E2
U365C	C2	D3
U370	E2	E3
U375	C3	E3
U440A	F1	C3
U440B	B3	C3
U445	D2	C3
U455D	C1	D3
U460B	F2	D3
U460C	F2	D3
U465	D2	D3
U470	F2	E3
U530C	F3	B4
U540D	D3	C4
U540E	E1	C4
U545C	F1	C4
U555D	F2	D4
U575	B5	E3
U585	B2	E3
U630A	E1	B4
U640A	B1	C4
U645B	F4	C4
U660	B5	D4
U665	F5	D4
U670	E5	E4
U675	D5	E4

The colors on this page correspond to the following Option 06 diagnostic functions:

POWER-UP

0 BAUD RATE MULTIPLEXER

1 SMART PORT CONTROLLER

1 LOOP COUNTER

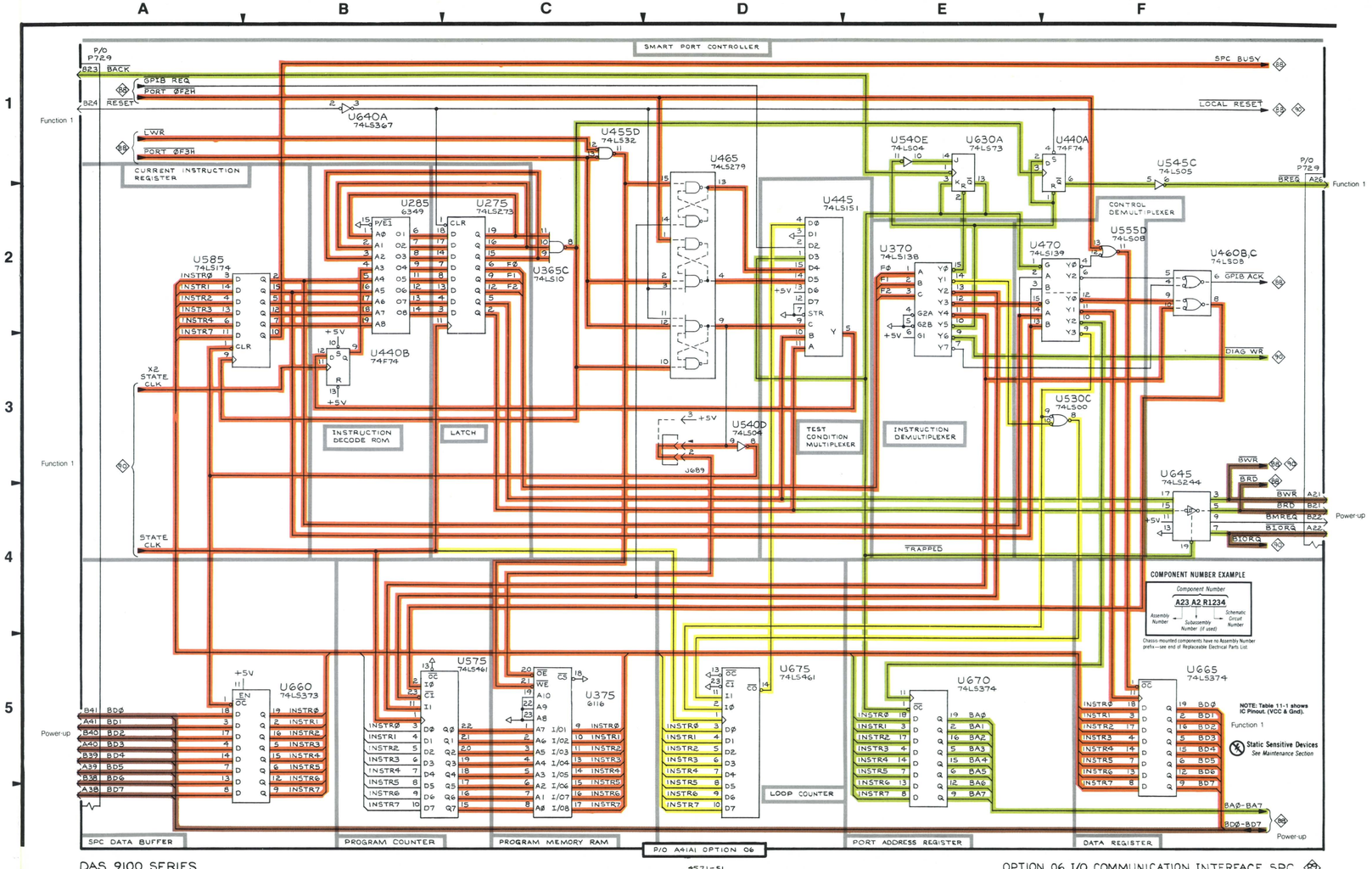
1 ADDRESS SWITCH BUFFER

2 GPIB

3 RS-232

4 BAUD RATE

For more information, refer to the Troubleshooting section.



DAS 9100 SERIES

OPTION 06 I/O COMMUNICATION INTERFACE SPC

P/O A41A1 OPTION 06 SPC

Table 11-3
OPTION 06 I/O COMMUNICATION INTERFACE RS 232

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C149	F3	C1
C154	F3	D1
C158	F3	D1
C164	F3	D1
C174	F3	D1
C178	F3	E1
C233	F3	B2
C274	F3	E2
C284	F3	E2
C323	F3	B2
C340	F3	C3
C349	F3	C3
C364	F3	D3
C388	F3	E2
C424	F3	B3
C454	F3	D3
C510	F3	A4
C525	F3	B4
C530	F3	B3
C547	F3	C4
C581	F3	E3
C629	F3	B4
C633	F3	C4
C648	F3	C4
C661	F3	D4
C676	F3	E4
C776	F3	D4
J110	A4	A1
J110	F5	A1
P729	F3	B4
*R175	C3	E1
R411H	A5	A3
R411I	A5	A3
R717	F5	A4
R718	F5	A4
TP387	F4	E2
TP404	F4	A3
U140A	C1	C1
U140B	E4	C1
U145	E2	C1
U155	E2	D1
U160	D2	D1
U165	C2	D1
U170A	B3	E1
U170B	B3	E1
U175A	F2	E1
U175B	B3	E1
U340	C1	C3
U360	B1	D3
U365B	B1	D3
U415	B4	B3
U425	D4	B3
U435	C4	C3
U460A	B2	D3
U460D	B1	D3
U510	B5	A4
U515C	E4	B4
U515D	E4	B4
U525A	B1	B4
U540C	C4	C4
U540F	C2	C4
U545A	F4	C4
U635	F5	C4
U645A	C1	C4
Y185	A3	E1

***SEE PARTS LIST FOR SERIAL NUMBER RANGES.**

The colors on this page correspond to the following Option 06 diagnostic functions:

POWER-UP

0 BAUD RATE MULTIPLEXER

1 SMART PORT CONTROLLER

1 LOOP COUNTER

1 ADDRESS SWITCH BUFFER

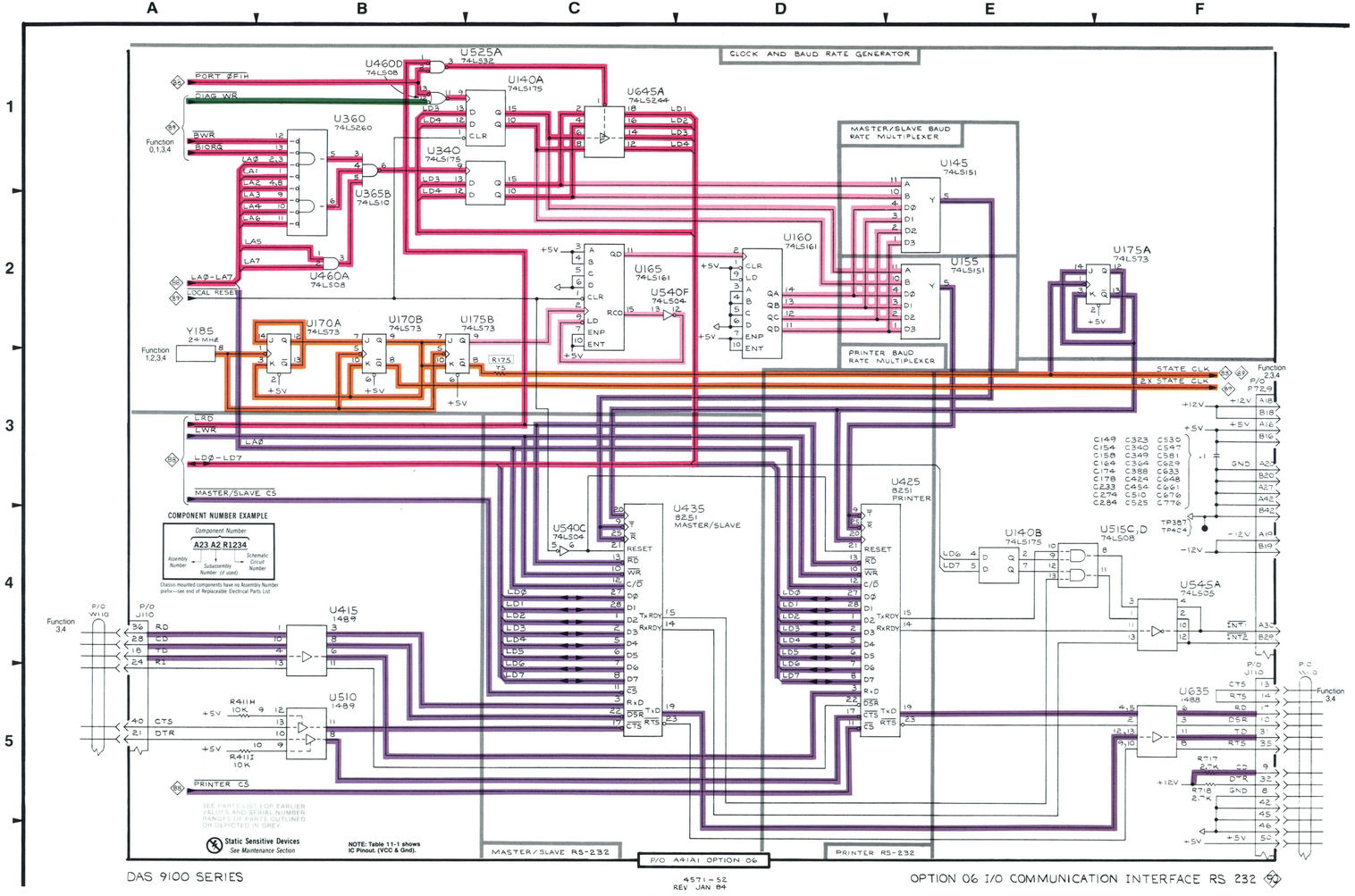
2 GPIB

3 RS-232

4 BAUD RATE

For more information, refer to the Troubleshooting section.

The colors on this page correspond to the following Option 06 diagnostic functions:



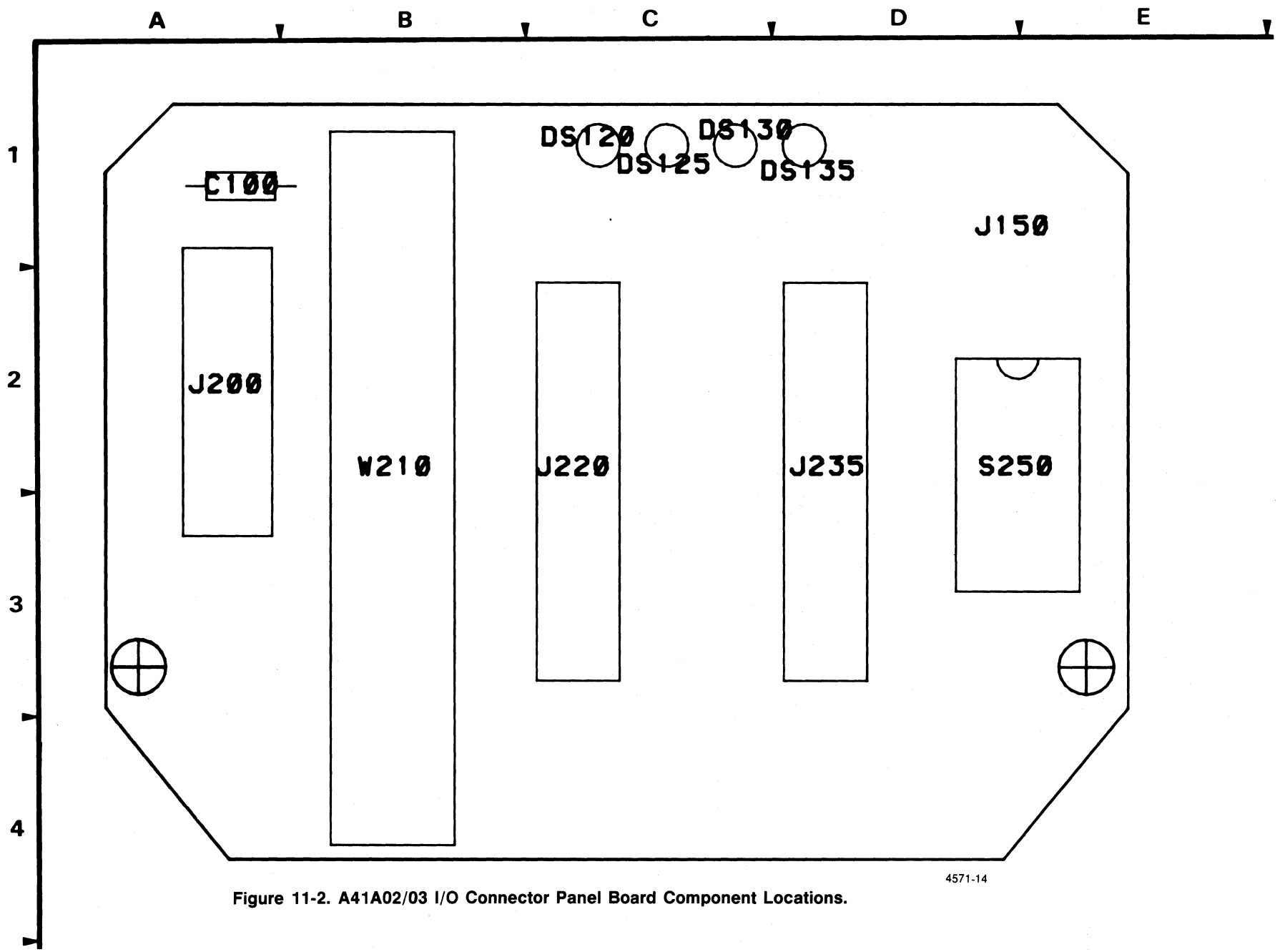
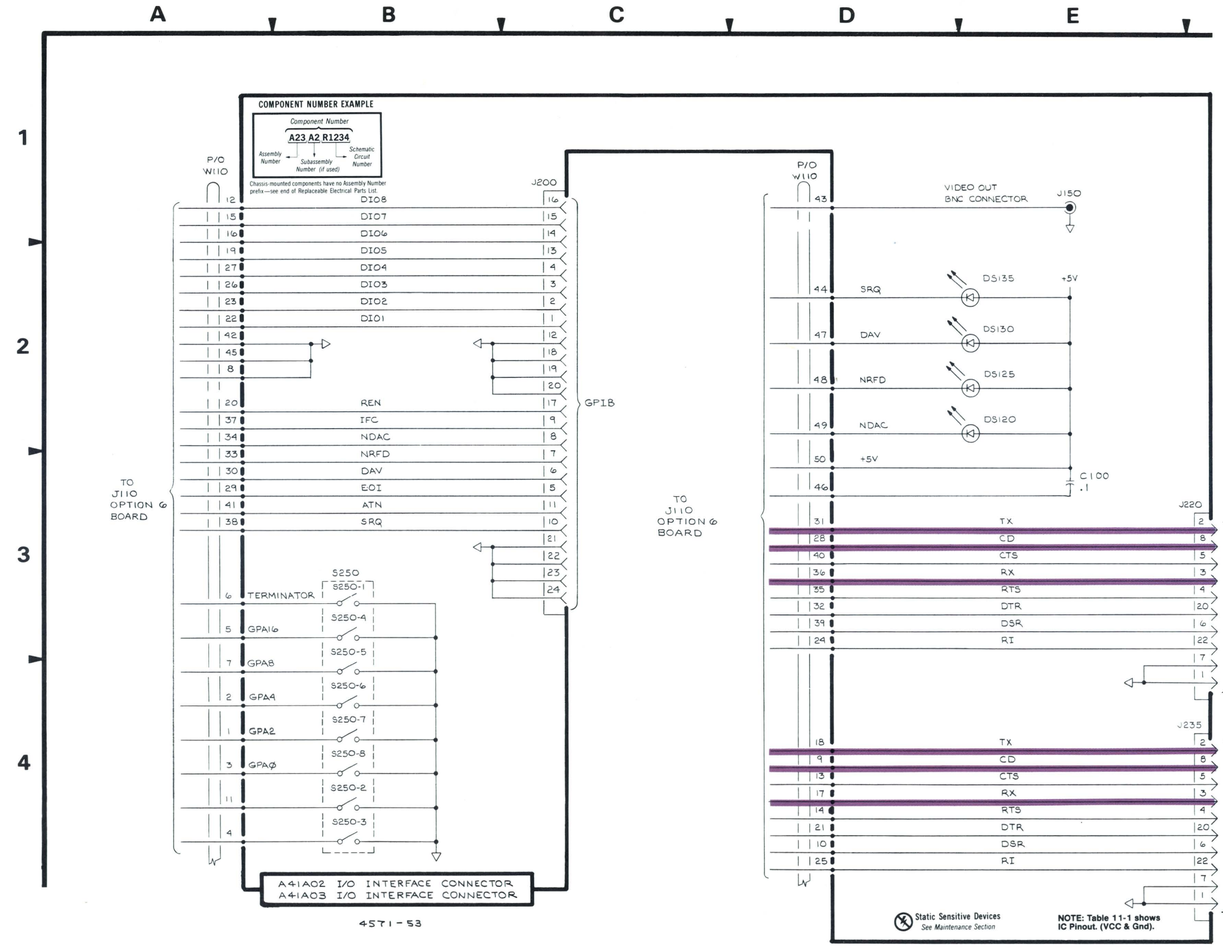


Figure 11-2. A41A02/03 I/O Connector Panel Board Component Locations.

The colors on this page correspond to the following Option 06 diagnostic functions:

3 RS-232

For more information, refer to the Troubleshooting section.



DAS 9100 SERIES

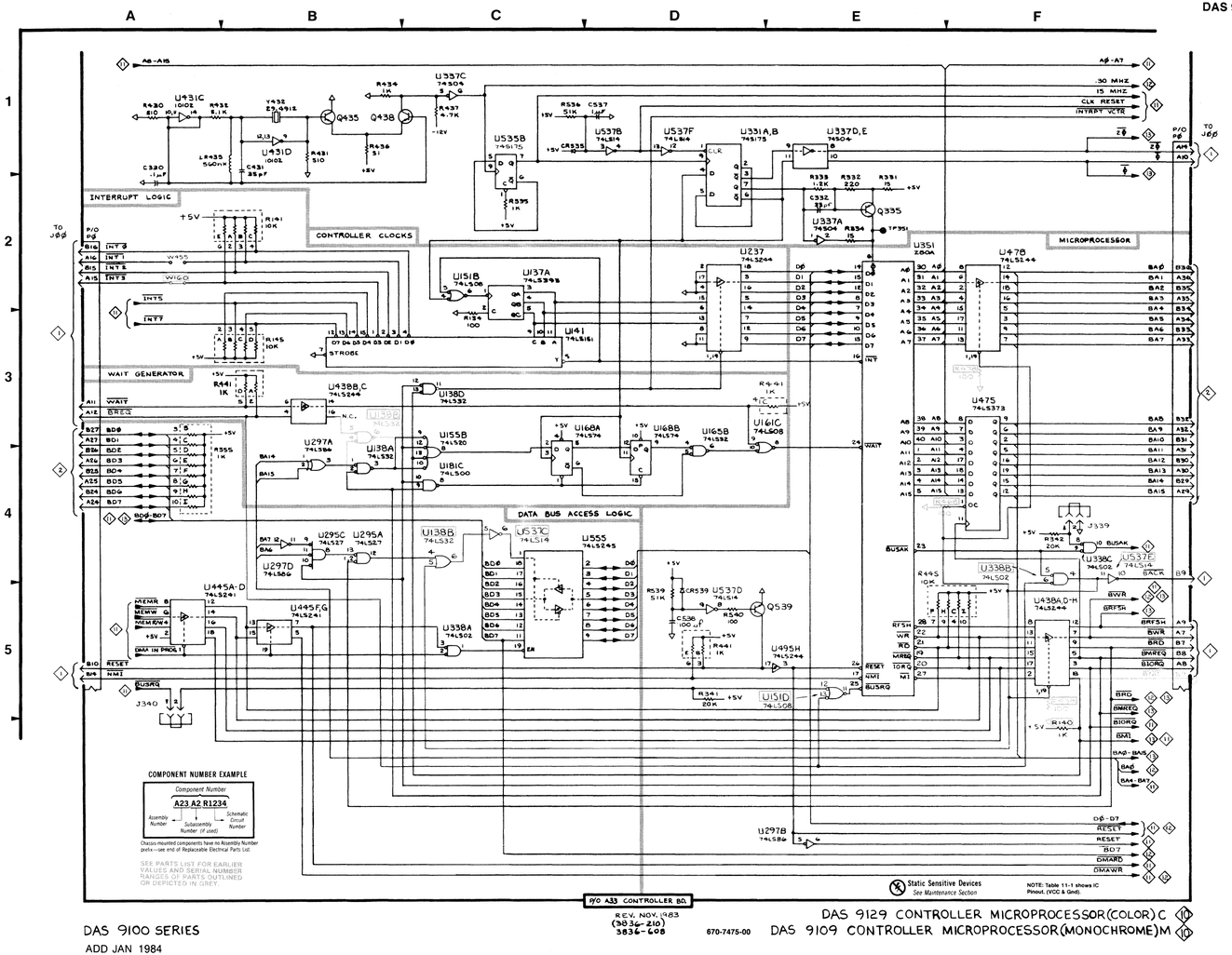
OPTION 06 I/O INTERFACE CONNECTOR

Table 11-11CM

CONTROLLER C ◇10◇ , M ◇10◇

ASSEMBLY A33 (670-7475-00)

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C330	A2	B2	R555H	A4	D3
C332	E2	B2	R555I	A4	D3
C431	B1	B2	TP351	E2	C2
C536	D1	B2	U137A	C2	B1
C538	D5	C2	U138A	B4	C1
CR535	C1	B2	U138B	B3	C1
CR539	D5	C2	U138D	C3	C1
J339	F4	C2	U141	C3	C1
J340	A5	C2	U151B	C2	C1
LR435	B1	B2	U155B	C4	C1
P0	A2	D3	U161C	D4	D1
P0	F1	D3	U165B	D4	D1
Q335	E2	B2	U168A	C4	D1
Q435	B1	B2	U168B	D4	D1
Q438	C1	B2	U181C	C4	D1
Q539	D5	C2	U237	D2	B1
R134	C3	B1	U295A	B4	E1
R141A	B2	C1	U295C	B4	E1
R141B	B2	C1	U297A	B4	E1
R141C	B2	C1	U297B	E5	E1
R141E	B2	C1	U297D	B4	E1
R145A	B3	C1	U331A	D1	B2
R145B	B3	C1	U331B	D1	B2
R145C	B3	C1	U337A	E2	B2
R145D	B3	C1	U337C	C1	B2
R331	E2	B2	U337D	E1	B2
R332	E2	B2	U337E	E1	B2
R333	E2	B2	U338A	C5	C2
R334	E2	B2	U338C	F4	C2
R341	D5	C2	U351	E2	C2
R342	F4	C2	U431C	A1	B2
R430	A1	B2	U431D	B1	B2
R431	B1	B2	U438A	F5	C2
R432	A1	B2	U438B	B3	C2
R434	B1	B2	U438C	B3	C2
R436	B1	B2	U438D	F5	C2
R437	C1	B2	U438E	F5	C2
R438	F5	C2	U438F	F5	C2
R441A	B3	C2	U438G	F5	C2
R441B	D5	C2	U438H	F5	C2
R441D	B3	C2	U445A	A5	C2
R441E	D5	C2	U445B	A5	C2
R445C	F5	C2	U445C	A5	C2
R445F	E5	C2	U445D	A5	C2
R445H	F5	C2	U445F	B5	C2
R445I	F5	C2	U445G	B5	C2
R468	F4	D2	U475	F4	D2
R478	F3	D2	U478	F2	D2
R535	C2	B2	U495H	E5	E2
R536	C1	B3	U535B	C1	B2
R539	D5	C2	U537B	D1	B2
R540	D5	C3	U537C	C4	B2
R555B	A3	D3	U537D	D5	B2
R555C	A3	D3	U537F	D1	B2
R555D	A4	D3	U555	C5	C3
R555E	A4	D3	W160	A2	C1
R555F	A4	D3	W455	A2	C2
R555G	A4	D3	Y432	B1	B2



DAS 9129 CONTROLLER MICROPROCESSOR(COLOR) C ◇10◇
DAS 9109 CONTROLLER MICROPROCESSOR(MONOCHROME) M ◇10◇

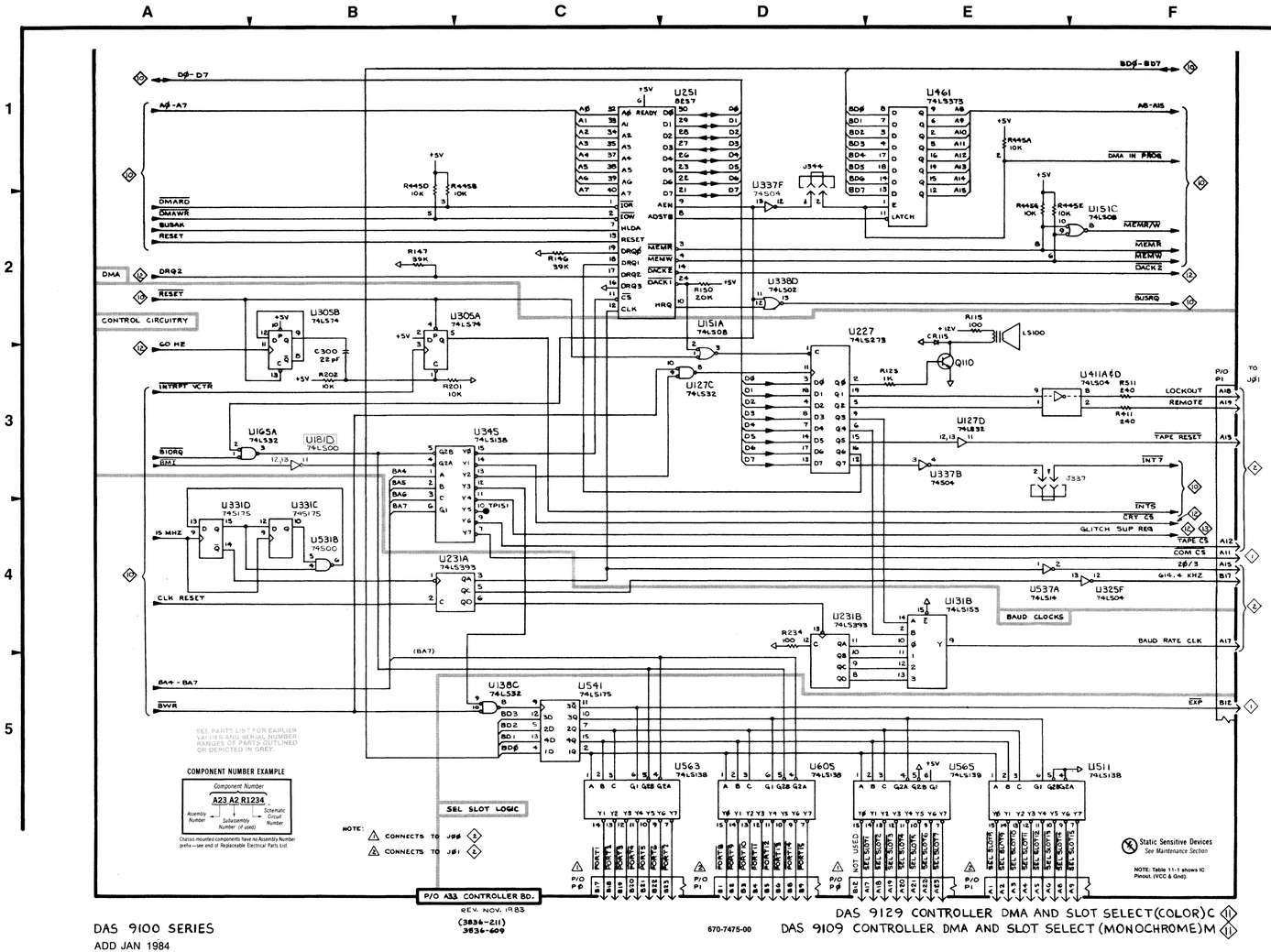
DAS 9100 SERIES
ADD JAN 1984

Table 11-12CM

CONTROLLER C ◇11◇ , M ◇11◇

ASSEMBLY A33 (670-7475-00)

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C300	B3	A2	U127D	E3	B1
CR115	E2	A1	U131B	E4	B1
J337	E3	B2	U138C	C5	C1
J344	D1	C2	U151A	D3	C1
LS100	E2	A1	U151C	F2	C1
P0	C5	D3	U165A	B3	D1
P0	D5	D3	U227	D3	B1
P1	F3	B3	U231A	C4	B1
P1	D5	B3	U231B	D5	B1
P1	E5	B3	U251	C2	C1
Q110	E3	A1	U305A	B3	A2
R115	E2	A1	U305B	B3	A2
R125	E3	B1	U325F	F4	B2
R146	C2	C1	U331C	B4	B2
R147	B2	C1	U331D	A4	B2
R150	D2	C1	U337B	E3	B2
R201	C3	A2	U337F	D2	B2
R202	B3	A2	U338D	D2	C2
R234	D4	B1	U345	C3	C2
R411	F3	A2	U411A	E3	A2
R445A	E1	C2	U411D	E3	A2
R445B	B1	C2	U461	E1	D2
R445D	B1	C2	U511	E5	A3
R445E	E2	C2	U531B	B4	B2
R445G	E2	C2	U537A	E4	B2
R511	F3	A2	U541	C5	C3
TP151	C4	C1	U563	C5	D3
U127C	D3	B1	U565	E5	D3
			U605	D5	A3



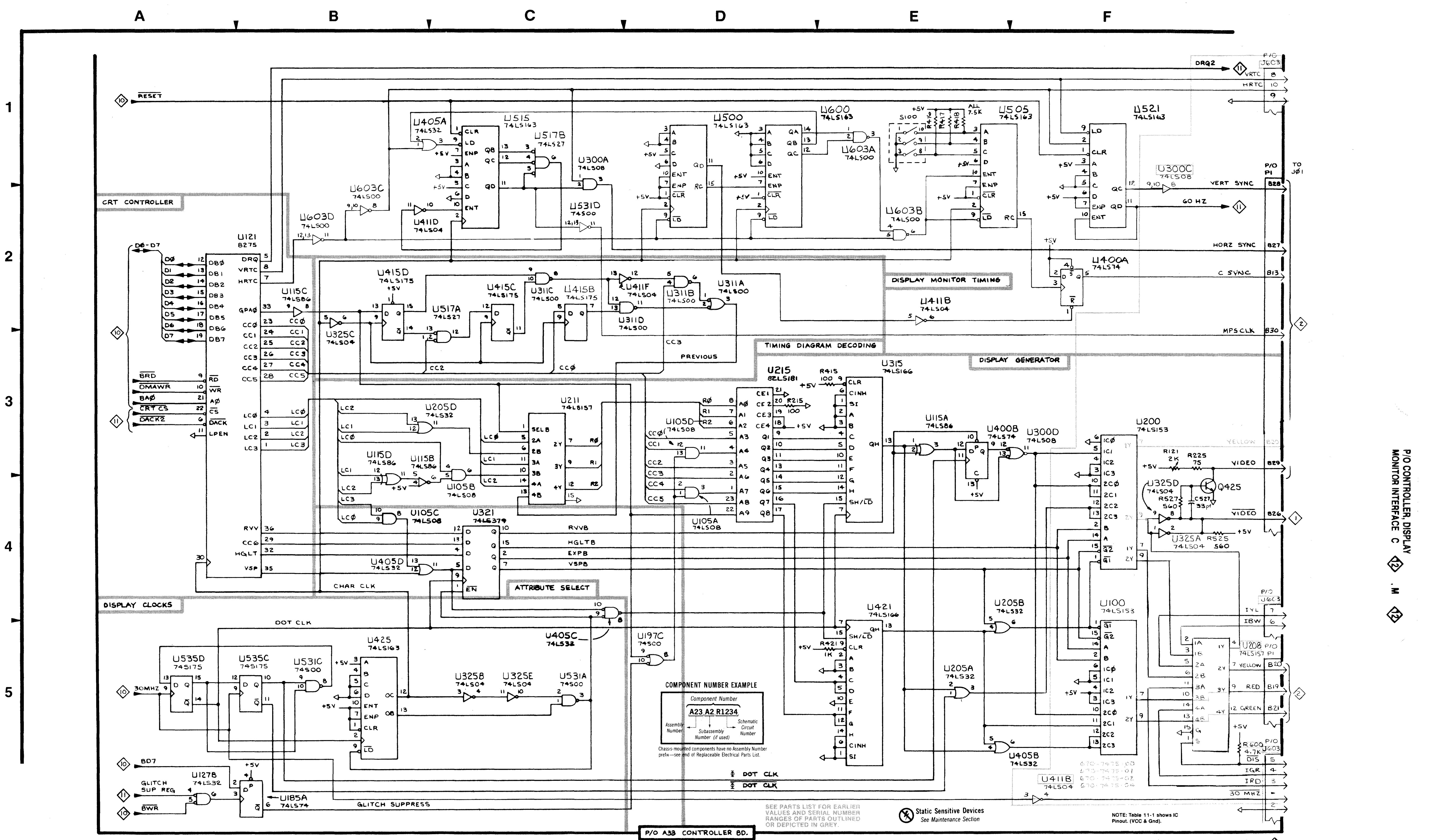
DAS 9100 SERIES
ADD JAN 1984

Table 11-13CM

CONTROLLER C ⟨12⟩ , M ⟨12⟩

ASSEMBLY A33 (670-7475-00)

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C527	F4	B3	U315	E3	A2
P1	F1	B3	U321	C4	B2
Q425	F4	B2	U325A	F4	B2
R121	F3	B1	U325B	C5	B2
R215	D3	B1	U325C	B2	B2
R225	F3	B1	U325D	F4	B2
R415	E3	B2	U325E	C5	B2
R416	E1	A2	U400A	F2	A2
R417	E1	A2	U400B	E3	A2
R418	E1	A2	U405A	C1	A2
R421	E5	B2	U405B	E5	A2
R525	F4	B2	U405C	C4	A2
R527	F4	B3	U405D	B4	A2
S100	E1	A1	U411B	E2	A2
U100	F5	A1	U411D	B2	A2
U105A	D4	A1	U411F	D2	A2
U105B	C4	A1	U415B	C2	A2
U105C	B4	A1	U415C	C2	A2
U105D	D3	A1	U415D	B2	A2
U115A	E3	A1	U421	E5	B2
U115B	B4	A1	U425	B5	B2
U115C	B2	A1	U500	D1	A3
U115D	B4	A1	U505	E1	A3
U121	B2	B1	U515	C1	A3
U127B	A5	B1	U517A	C3	A3
U185A	B5	E1	U517A	C2	A3
U197C	D5	E1	U517B	C1	A3
U200	F4	A2	U521	F1	B3
U205A	E5	A1	U531A	C5	B2
U205B	E5	A1	U531C	B5	B2
U205D	B3	A1	U531D	C2	B2
U211	C3	A1	U535C	B5	B2
U215	D3	A1	U535D	A5	B2
U300A	C1	A2	U600	D1	A3
U300D	F3	A2	U600A	E2	A3
U311A	D2	A2	U603A	E1	A3
U311B	D2	A2	U603B	E2	A3
U311C	C2	A2	U603C	B2	A3
U311D	D2	A2	U603D	B2	A3



DAS 9129 CONTROLLER DISPLAY MONITOR INTERFACE (COLOR) C ⟨12⟩

REV. NOV. 1983 (3836-212) 3836-610

670-7475-00 DAS 9109 CONTROLLER DISPLAY MONITOR INTERFACE (MONOCHROME) M ⟨12⟩

DAS 9100 SERIES

ADD JAN 1984

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

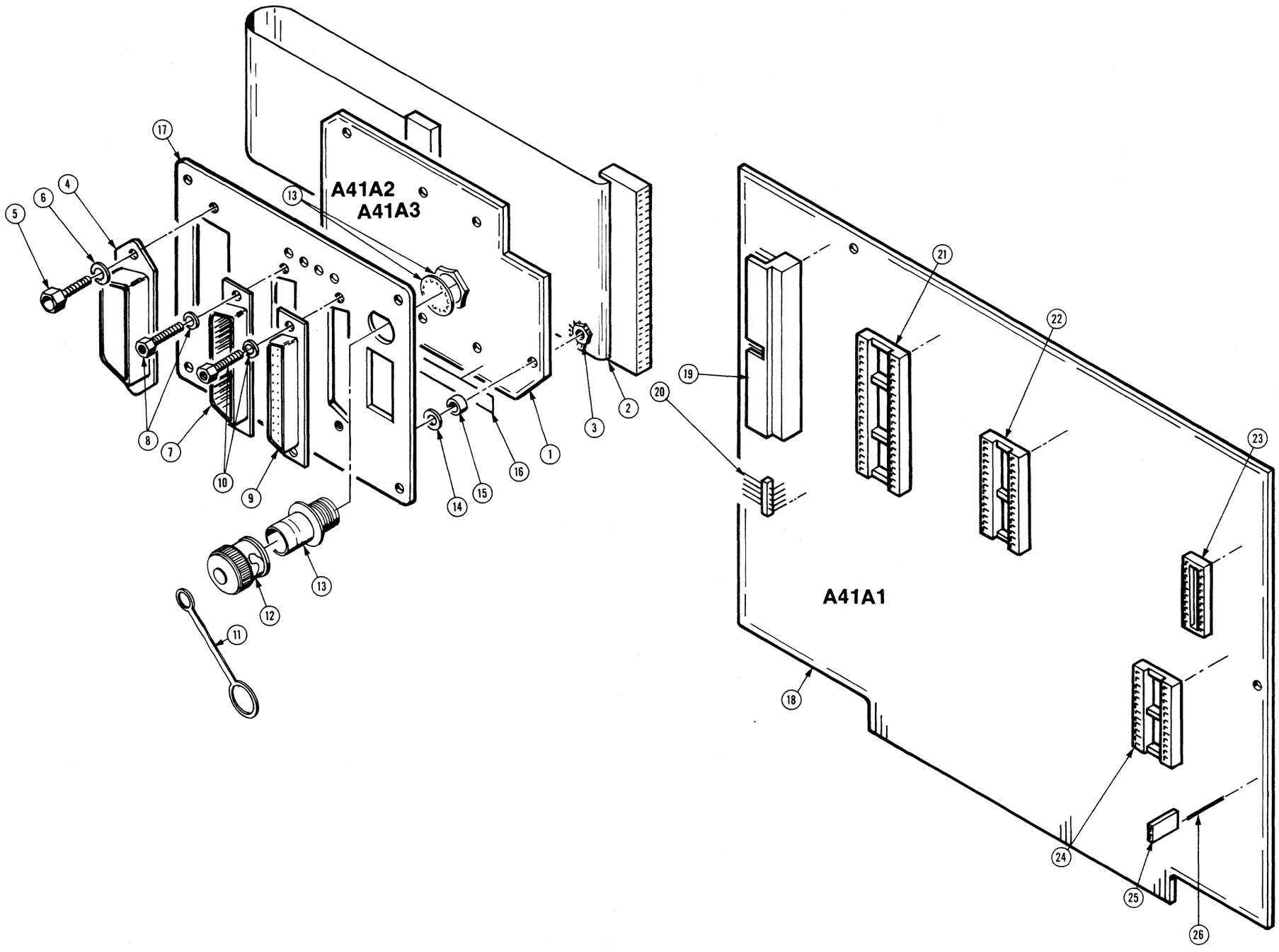
"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
02660	BUNKER RAMO CORP., CONNECTOR DIVISION	2801 S 25TH AVENUE	BROADVIEW, IL 60153
04919	COMPONENT MANUFACTURING SERVICE, INC.	1 COMPONENT PARK WEST	BRIDGEWATER, MA 02379
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
29587	BUNKER-RAMO CORP., AMPHENOL INDUSTRIAL DIV.	1830 S. 54TH AVE.	CHICAGO, IL 60650
71468	ITT CANNON ELECTRIC	666 E. DYER RD.	SANTA ANA, CA 92702
74868	BUNKER-RAMO CORP., THE AMPHENOL RF DIV.	33 E. FRANKLIN ST.	DANBURY, CT 06810
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
91836	KINGS ELECTRONICS CO., INC.	40 MARBLEDALE ROAD	TUCKAHOE, NY 10707

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	----- -----			1		CKT BOARD ASSY:I/O INTFC CONN		
	----- -----			-		(SEE A41A3,A41A2 REPL)		
-2	----- -----			1		.CA ASSY,SP,ELEC:(SEE W210 REPL)		
	333-0141-01			1		.PANEL,REAR:W/CONNECTORS	80009	333-0141-01
	----- -----			-		.(DAS 9129 ONLY)		
	333-3066-01			1		.PANEL,REAR:W/CONNECTORS	80009	333-3066-01
	----- -----			-		.(DAS 91F6 OPTION 01 ONLY)		
						.**********(ATTACHING PARTS)**********		
-3	210-0586-00			2		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	OBD
						.**********(END ATTACHING PARTS)*********		
	----- -----			-		.REAR PANEL ASSY INCLUDES:		
-4	131-2203-02			1		..CONN,RCPT,ELEC:CKT BD,24 CONT,FEMALE	29587	57-20240-11(398)
						..**********(ATTACHING PARTS)**********		
-5	214-2871-00			2		..HARDWARE KIT:STANDOFF,W/NUT & LOCK WASHE	00779	552633-1
-6	210-0069-00			2		..WASHER,LOCK:0.168 ID X 0.293 " OD,SPLIT	83385	OBD
						..**********(END ATTACHING PARTS)*********		
-7	131-0813-00			1		..CONN,RCPT,ELEC:CKT BD,25 CONT,FEM	80009	131-0813-00
						..**********(ATTACHING PARTS)**********		
-8	131-0890-00			2		..LOCK,CONNECTOR:4-40 X 0.312 L	71468	D 20418-2
						..**********(END ATTACHING PARTS)*********		
-9	131-0971-00			1		..CONN,RCPT,ELEC:CKT BD MT,25 CONT,FEMALE	71468	DB25-SH
						..**********(ATTACHING PARTS)**********		
-10	131-0890-00			2		..LOCK,CONNECTOR:4-40 X 0.312 L	71468	D 20418-2
						..**********(END ATTACHING PARTS)*********		
-11	346-0045-00			1		..STRAP,CONN COV:BNC ONE END,POLYPROPYLENE	80009	346-0045-00
-12	200-0678-00			1		..COVER,ELEC CONN:BNC,SHORTING	91836	KC89-58TR5
-13	131-0274-00			1		..CONNECTOR,RCPT,:BNC	91836	KC79-67
-14	210-0870-00			2		..WASHER,FLAT:0.14 ID X 0.312 INCH OD STL	12327	OBD
	----- -----			-		..(DAS 91F6 OPTION 01 ONLY)		
-15	129-0442-00			2		..SPACER,POST:0.125 L,W/4-40 THD THRU	80009	129-0442-00
-16	337-2113-00			1		..SHIELD,ELEC:CKT BD,PLASTIC	80009	337-2113-00
-17	333-0141-00			1		..REAR PANEL:	80009	333-0141-00
	----- -----			-		..(DAS 9129 ONLY)		
	333-3066-00			1		..REAR,PANEL:	80009	333-3066-00
	----- -----			-		..(DAS 91F6 OPTION 01 ONLY)		
-18	----- -----			1		CKT BOARD ASSY:I/O OPTION ENHANCED		
	----- -----			1		(SEE A41A1 REPL)		
-19	131-2860-00			1		.CONN,RCPT,ELEC:HEADER,2 X 25,0.1 SPACING	22526	65461-008
-20	131-1425-00			1		.CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 3	22526	65521-136
-21	136-0757-00			1		.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-22	136-0755-00			1		.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-23	136-0752-00			1		.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-24	136-0751-00			1		.SKT,PL-IN ELEK:MICROCKT,24 PIN	09922	DILB24P108
-25	131-0993-00			2		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-26	131-0608-00			8		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
						STANDARD ACCESSORIES		
	070-4570-00			1		MANUAL,TECH:OPERATORS	80009	070-4570-00
						OPTIONAL ACCESSORIES		
	012-0074-00			1		CABLE ASSY,RF:75 OHM COAX,42.0 L	80009	012-0074-00
	012-0630-01			1		CABLE,INTCON:2 METERS LONG	74868	AC30111102 REVC
	012-0630-02			1		CABLE,INTCON:4.0 METERS LONG	02660	OBD
	012-0815-00			1		CABLE,INTCON:2.0 METERS	04919	OBD
	012-0991-00			1		CABLE,GPIB:LOW EMI,2 METER	22526	81190-020
	012-0991-01			1		CABLE,GPIB:LOW EMI,1 METER	22526	81190-010
	012-0991-02			1		CABLE,GPIB:LOW EMI,4 METER	22526	81190-040
	070-4571-00			1		MANUAL,TECH:SERVICE	80009	070-4571-00
	175-2753-00			1		CABLE ASSY:75 OHM COAX,120.0 L	80009	175-2753-00
	067-0980-01			1		CAL FIXTURE:DAS SERVICE MAINT KIT	80009	670-8246-00

FIG. 1 EXPLODED



Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 12-8-83 Change Reference: C2/1183 REV

Product: OPTION 06 I/O CUMMUNICATION INTERFACE Manual Part No.: 070-4571-00

DESCRIPTION

SN B010100 & UP

PARTS LIST AND DIAGRAM ADDITION

SECTION 10 REPLACEABLE ELECTRICAL PARTS

ADD:

A41A1R175	317-0750-00	RES 75 OHM 1/8W 5%

SECTION 11 DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

DIAGRAM 90

ADD:

R175 in series with pin 8 of U175B.

Table 11-3

ADD:

Circuit Number	Schem Location	Board Location
R175	C3	E1